The Pennsylvania State University

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FABRICATION, CHARACTERIZATION AND PHYSICS OF III-V TUNNELING FIELD EFFECT TRANSISTORS FOR LOW POWER LOGIC AND RF APPLICATIONS

A Dissertation in

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by

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ABSTRACT

Fundamental physics sets the limit on the minimum sub-threshold swing of MOS transistor to 60mV/decade at room temperature. As a result, supply voltage scaling to reduce the power dissipation in the chip comes at the penalty of increased static power dissipation. At the same time, consumer demand for higher performance and lower power microchips is driving the need to continue scaling CMOS technology. Two possible approaches to solve the supply voltage scaling issue are: (1) Transport enhancement through high mobility material systems. (2) Threshold voltage scaling through steep switching devices. Tunneling field effect transistors (TFET) based on inter band tunneling of carriers are a promising candidate to realize steep switching slope and thus enable supply voltage scaling. In particular, tunneling transistors within the III-V compound semiconductor system are of interest since the tunneling efficiency is high due to the direct bandgap and lower effective mass of tunneling carriers. Further, wide range of compositionally tunable tunneling barrier height is possible within the III-V material system.

This dissertation focusses on experimental investigation of III-V n-channel and p-channel TFET targeting low power logic as well as RF applications. Gate stack engineering for demonstration of steep switching slope in $In_{0.65}Ga_{0.35}As/GaAs_{0.4}Sb_{0.6}$ n-channel TFET is discussed. $In_{0.9}Ga_{0.1}As/GaAs_{0.18}Sb_{0.82}$ near-broken-gap n-channel TFET with enhanced ON state performance is then presented. Further, a novel planarization scheme to incorporate co-planar waveguide structure in vertical TFET is also introduced and high frequency switching in $In_{0.9}Ga_{0.1}As/GaAs_{0.18}Sb_{0.82}$ n-channel TFET

demonstrated. Impact of tunnel barrier engineering on the low frequency noise performance of n-channel TFET is then investigated through experiments and analytical modeling. Strategy to improve high-κ/$GaAs_xSb_{1-x}$ interface for p-channel TFET demonstration is then presented. Electrical and material characterization of p-channel GaSb, $In_{0.65}Ga_{0.35}As/GaAs_{0.4}Sb_{0.6}$ and InAs/GaSb TFETs incorporating the proposed gate stack is discussed. A physics based analytical model is also introduced to gain insight into the output characteristics of III-V TFET.

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Chapter 1

Introduction

Miniaturization of the metal oxide semiconductor field effect transistor (MOSFET) has resulted in exponential growth of transistor density on a chip and the switching speed, and also a dramatic reduction in the cost of a logic gate [1-2]. As more transistors are packed in a chip, the net power dissipation also increased to a point where thermal management became a major issue. As a result, the power dissipation in a chip is constrained to 100W and the supply voltage was required to be scaled further in order to pack more transistors in the chip [3]. The net power dissipation, P_{total} in a logic circuit is the sum of the dynamic power dissipation $P_{dynamic}$ and the static power dissipation P_{static} given by [4],

$$P_{total} = P_{dynamic} + P_{static} = \alpha C_{eff} V_{cc}^2 f + I_{leak} V_{cc} \quad (1\text{-}1)$$

where α represents the activity factor, C_{eff} is the system capacitance, f represents the clock frequency, V_{cc} represents CMOS supply voltage and I_{leak} is the system leakage current. Reduction in the supply voltage by a factor x leads to reduction in $P_{dynamic}$ by a factor x^2 and P_{static} by a factor x. However, it turns out that scaling V_{cc} is not very straightforward. The drive current in the ON state of a ballistic MOSFET is given by [5],

$$I_{ON} = w C_{inv} V_{inj} (V_{cc} - V_{th}) \quad (1\text{-}2)$$

where w is the width of the MSOFET, C_{inv} is the inversion capacitance, V_{inj} is the source injection velocity. Hence, to maintain the ON state performance of the transistor, the threshold voltage V_{th} of the transistor will also need to be scaled along with V_{cc}. However reduction in V_{th} also leads to an increase in the static power dissipation due to the exponential increase in the OFF state leakage current I_{off} given by,

$$I_{off} = wI_o 10^{\frac{-V_{th}}{SS}} \quad (1\text{-}3)$$

where I_o is the targeted OFF state current and SS is the sub-threshold slope (Figure 1-1 (a)). This is due to the fundamental limitation in the lowest SS that can be achieved in a MOSFET.

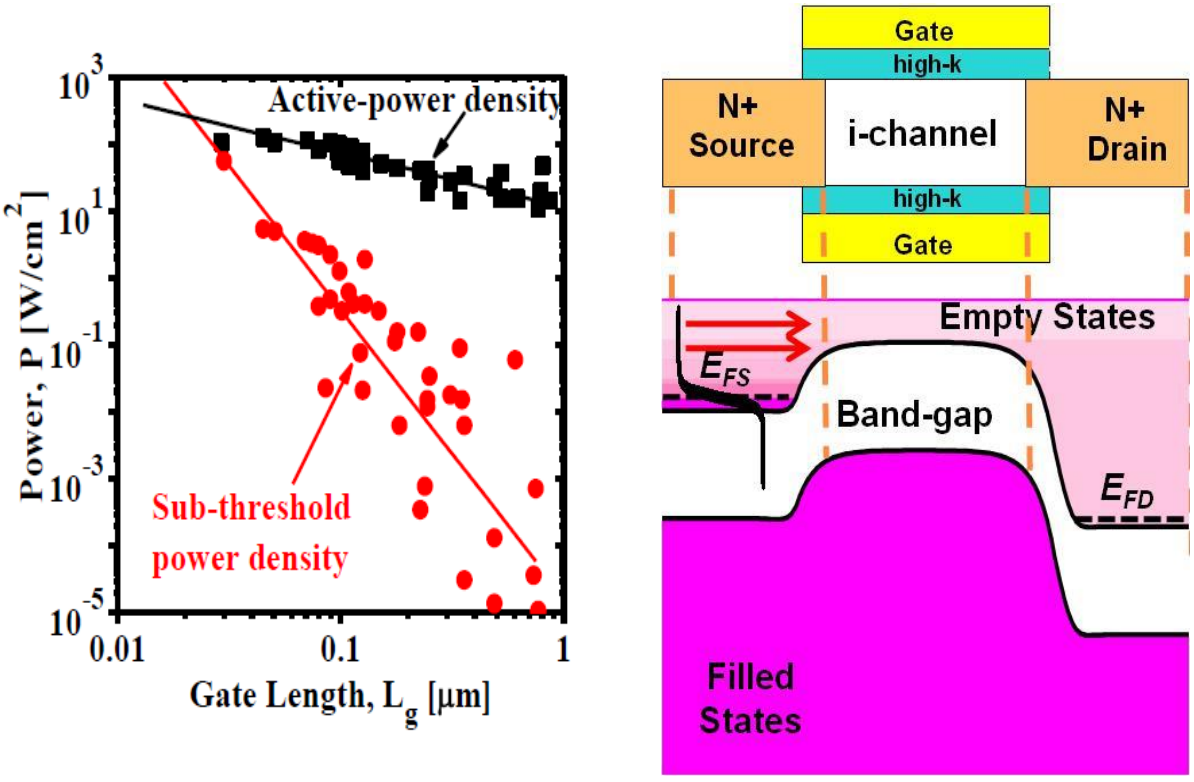

Figure 1-1. (a) Static or sub-threshold power dissipation has increased as the gate length of the MOSFET scaled. (b) Energy band-diagram showing the carrier injection mechanism in a MOSFET.

In a MOSFET, as the gate voltage is reduced to the sub-threshold regime, the energy barrier for carriers in the source to enter the channel region increases. Carriers in the source follow a Fermi distribution of energy and some of them have high enough energy to surmount this barrier and reaches the drain of the MOSFET by diffusion process. This contributes to the

sub-threshold leakage current in a MOSFET. The sub-threshold swing defined as the change in gate voltage required to reduce the sub-threshold current by one order of magnitude is given by:

$$SS = \frac{dV_g}{d\Psi_s}\frac{d\Psi_s}{d(log_{10}I_D)} = \left(1 + \frac{C_{dep}}{C_{ox}}\right) ln10 \frac{\kappa T}{q} \quad (1\text{-}4)$$

where V_g is the gate bias, Ψ_s is the surface potential, C_{dep} is the depletion capacitance, C_{ox} is the gate oxide capacitance and T is the temperature. Hence, at room temperature (300K), SS is limited to 60mV/decade.

Innovations in the transistor architecture namely strained silicon at 90nm node and high-k/metal gate technology to replace poly silicon/SiO2 gate stack and tri-gate technology at the 22nm node have helped scale the supply voltage moderately [6]. Scaling the supply voltage in the future technology nodes poses a significant challenge. Two different approaches have been proposed to further scale the supply voltage [7]: (1) Enhancement of the transport properties: From Equation (1-2), increasing V_{inj} by replacing silicon with high mobility material such as the III-V compound semiconductor can maintain the same ON state performance even with scaled supply voltage and non-scaled threshold voltage. (2) Scale the threshold voltage: In this approach, novel devices will be used working on different fundamental physics from that of the MOSFET which can achieve SS lower than 60mV/decade. This class of devices is called steep slope devices.

Many steep slope devices have been proposed based on modifying either of the two factors in Equation (1-4). Some of the proposed devices which modify the first factor in Equation (1-4) are negative-capacitance field effect transistor [8-10] or micro- or nano-electromechanical (M/NEM) movable electrodes in M/NEM-FET or NEM relay devices [11-13], in which the instability points between the electrical and the mechanical force are used to define abrupt transitions between the OFF and ON states. However, electromechanical devices suffer from limitations, such as voltage-scaling limitations, reliability issues and a stringent need for a

controlled environment for robust operation. Steep slope devices which alter factor 2 in Equation (1-4) works on modification of the carrier-injection mechanism such as impact ionization [14] and band-to-band tunneling [15-17].

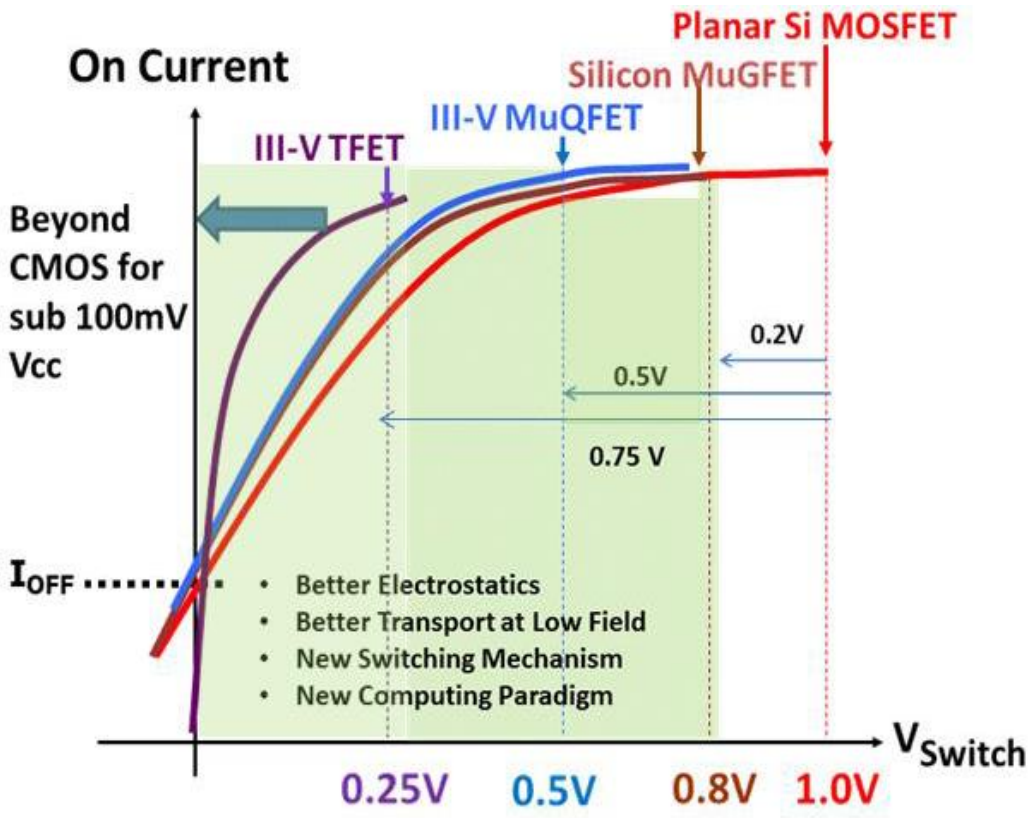

Figure 1-2. Future device focus on threshold voltage scaling and transport enhancement.

Tunneling field effect transistors (TFETs) based on band-to-band tunneling of carriers have been identified as a promising steep slope device. In TFET, carriers get injected into channel through inter-band tunneling of carriers from the source under the influence of a gate electric field. The reverse biased tunnel junction in TFET eliminates the high energy tail present in the Fermi-Dirac distribution of the valence band electrons in the p+ doped source region and allows sub-kT/q SS. This allows TFETs to achieve, in principle, much higher I_{ON}/I_{OFF} ratio over a given gate voltage swing compared to the MOSFET.

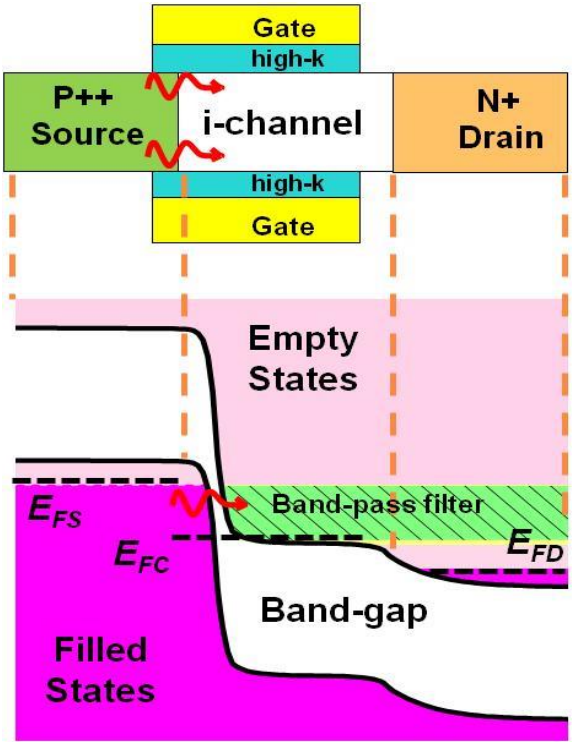

Figure 1-3. Energy band-diagram showing the carrier injection mechanism in a TFET.

I. Why III-V Semiconductor for TFET?

TFET based on Si is an easy choice in terms of compatibility with the CMOS process flow and achieving a high quality interface between high-κ gate dielectric and Si channel. Figure 1-4 shows the simulated transfer characteristics (I_{DS}-V_{GS}) of TFET based on different materials system by solving non-local band-to-band generation model self consistently with Poisson's and continuity equation [18]. For the simulations, Sentaurus Technology Computer Aided Design (TCAD) software was used. Effect of quantization due to structural confinement in thin body structures has been considered [19]. Also included is the transfer characteristics of Si based MOSFET. Though, Si TFET shows SS steeper than 60mV/dec at room temperature the drive current in the ON state is very low in comparison to the state of the art MOSFET.

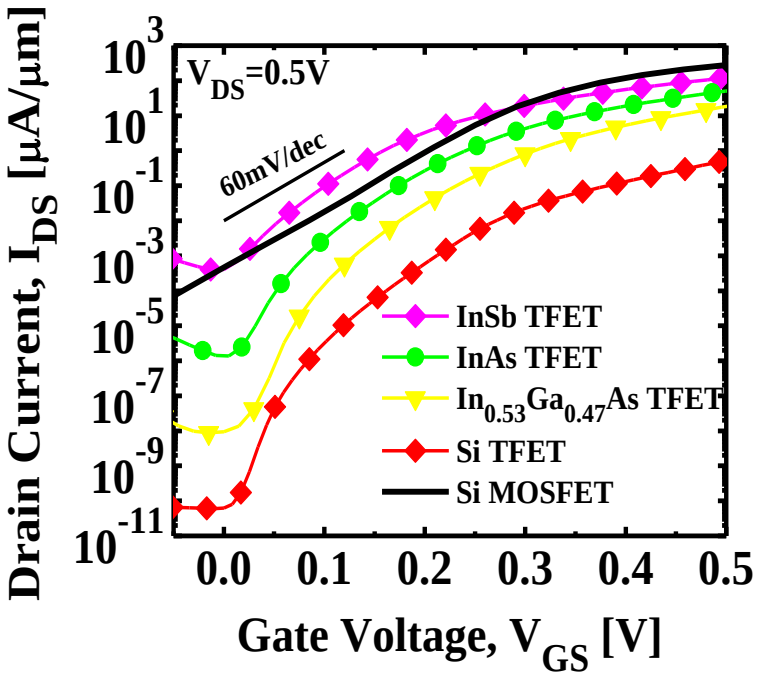

Figure 1-4. Simulated I_{DS}-V_{GS} characteristic of TFET based on different material systems.

Tunneling probability through a triangular potential barrier calculated using the Wentzel-Kramers-Brillouin (WKB) approximation is given by [20][21][22],

$$T = exp^{\frac{-4\sqrt{2m_r}E_g^{1.5}}{3q\hbar}} exp^{\frac{-E_\perp}{E}} \quad (1\text{-}5)$$

where q is the charge on an electron, F is the average junction field, $E_\perp$ is the transverse component of the total carrier energy and $E = q\hbar F/\sqrt{2m_r E_{Beff}}$ which determines the impact of the transverse-energy-state carriers on the tunneling magnitude. In the above expression, m_r is the tunneling effective mass defined by $\frac{1}{m_r} = \frac{1}{m_c} + \frac{1}{m_v}$. The effect on tunneling by the transverse states is minimized by high electric field, small effective mass and narrow bandgap. Hence reducing bandgap should increases the transmission probability and improve the ON state performance of TFET. From Figure 1-4 it is clear that as we move towards smaller band-gap material system like InSb the drive current increases. However, at the same time the OFF state leakage current also increases. Parasitic leakage mechanisms such as the Shockley-Read-Hall

generation [22][23] within the reverse biased p-i-n diode and the drain side BTBT generation leakage increase exponentially reducing the on-off ratio substantially in such low bandgap material systems.

Heterojunction TFET can simultaneously achieve high ON current and low OFF state leakage. In a heterojunction TFET the source and the channel can have large band-gaps. However, at the source-channel junction, the barrier for tunneling is significantly reduced. Figure 1-5 shows the energy band-diagram of a homojunction and heterojunction TFET. In the case of a homojunction TFET where the material is same throughout the source, channel and the drain, the barrier height is the same as the bandgap of the material. In the case of heterojunction TFET, the barrier height for tunneling at the source-channel junction is significantly reduced. This reduced barrier height is denoted by E_{Beff}. E_{Beff} is given by [24][25][26],

$$.E_{Beff} = E_{V\,(source)} - E_{C\,(channel)} \quad (1\text{-}6)$$

Hence, from Equation (1-5) transmission probability is significantly enhanced as E_g is now replaced by E_{Beff}. Further, the OFF state leakage current is still comparable to that of a homojunction TFET since the bandgap of source and channel material are large.

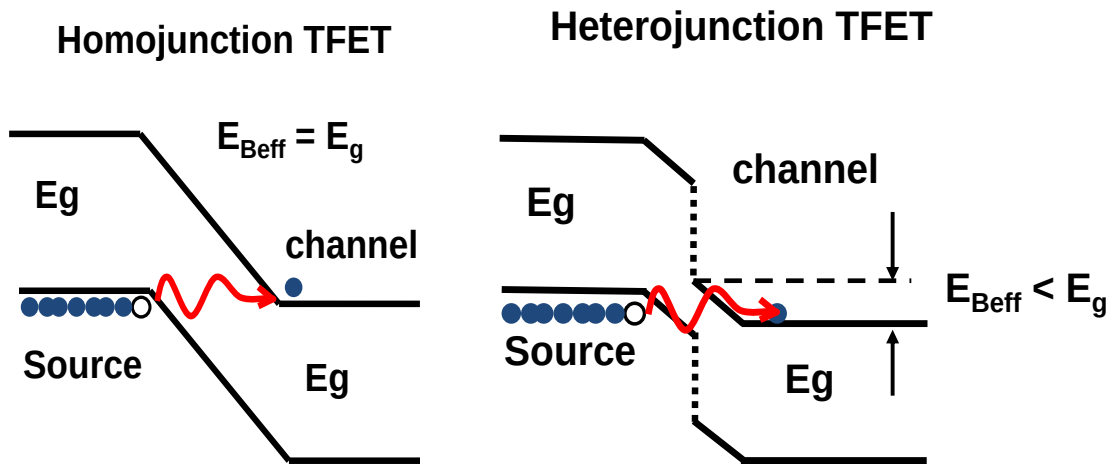

Figure 1-5. Energy banddiagram showing E_{Beff} reduction in heterojunction TFET.

Arsenide-antimonide hetero-junctions within the III-V semiconductor materials system provide a wide range of lattice-matched, compositionally tunable effective barrier heights [27]. Figure 1-5 shows varying band alignments for $GaAs_xSb_{1-x}/In_yGa_{1-y}As$ heterojunction. It should be noted that for n-channel TFET, the channel material is $In_yGa_{1-y}As$ and the source material is $GaAs_xSb_{1-x}$ whereas for p-channel TFET, the channel material is $GaAs_xSb_{1-x}$ and the source material is $In_yGa_{1-y}As$. By tuning the compositions of indium in $In_yGa_{1-y}As$ and antimony in $GaAs_{1-x}Sb_x$, various lattice matched combinations with varying E_{Beff} can be achieved. For example, the combination that is lattice matched to InP intrinsically makes an E_{Beff} =0.5eV. As the composition of In in $In_yGa_{1-y}As$ and Sb in $GaAs_xSb_{1-x}$ is increased, the E_{Beff} reduces and for the combination that is lattice matched to InAs, E_{Beff} ≈0eV. Further, the lower effective mass of the tunneling carriers and direct band-gap of the III-V material system increases the efficiency of band to band tunneling.

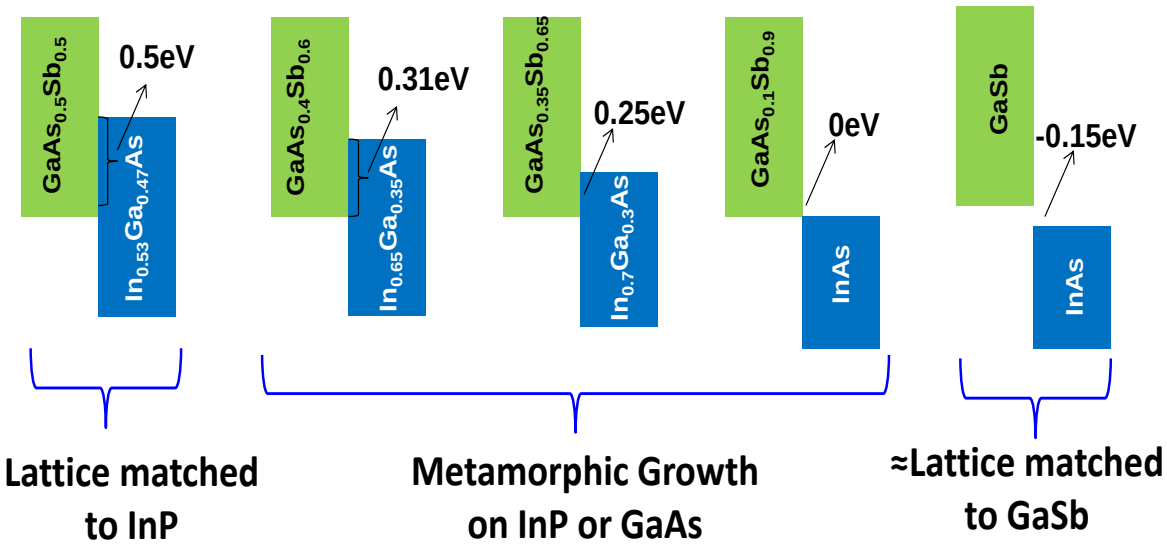

Figure 1-6. Tunable E_{Beff} can be achieved within the III-V semiconductor material system.

All the TFET structures presented in this dissertation are grown using molecular beam epitaxy (MBE) to ensure high quality and abrupt heterojunctions. Abrupt junctions make sure that we achieve the tunnel barrier height we design, the interface is nearly free of defects or Tamm

states that can unnecessarily increase the on-off ratio and the junction electric field is maximized due to the abrupt doping profiles. The TFET layers were grown using solid source MBE at IQE Bethlehem, PA [28]. Vertical TFETs are fabricated on the MBE grown wafer using a top down approach as discussed in chapter 2. Vertical TFETs provide the additional advantage of reduced footprint and saving in chip area compared to planar TFET [29].

II. Organization of Dissertation

Chapter 2 discusses the gate stack engineering of $In_{0.65}Ga_{0.35}As/GaAs_{0.4}Sb_{0.6}$ n-channel TFET. Chapter 3 presents a novel planarization scheme developed to incorporate co-planar waveguide structure in a vertical TFET. Tunneling barrier engineered $In_{0.65}Ga_{0.35}As/GaAs_{0.4}Sb_{0.6}$ is demonstrated with gigahertz small signal switching performance and record high drive current in the category of TFET. Flicker noise characterization and analytical modeling of $In_{0.7}Ga_{0.3}As$ homojunction and $In_{0.7}Ga_{0.3}As/GaAs_{0.35}Sb_{0.65}$ heterojunction is presented in chapter 4. In chapter 5, gate dielectric integration strategy for p-channel TFET is discussed. Design, fabrication and characterization of GaSb homojunction and InAs/GaSb heterojunction TFET is described in chapter 6. Analytical modeling of the output characteristics of a III-V TFET is introduced in chapter 7. Chapter 8 summarizes the key contributions of this dissertation and suggests future work.

Chapter 2

Gate Stack Engineering and Demonstration of kT/q Switching Slope in $In_{0.65}Ga_{0.35}As/GaAs_{0.4}Sb_{0.6}$ Heterojunction n-channel TFET

I. Introduction

Many experimental TFET results based on Si [30][31][32], Ge [33], SiGe [34] and III-V [35][36][37][38][39] material systems have been reported. The demonstrated results either achieve steep switching slope [30][31][32][35] or high drive currents [33][34][38][39]. However, in order to outperform MOSFET at low supply voltages, TFET should achieve low switching slope as well as high drive currents [37][39]. A hetero-junction TFET which simultaneously achieve high drive current as well as steep switching slope is yet to be demonstrated. Three key ingredients required to demonstrate low switching slope in a heterojunction TFET are: (1) Good quality of the heterojunction with low defect density. (2) Low electrical oxide thickness of the gate dielectric. (3) Good quality interface between the dielectric and semiconductor.

This chapter focuses on gate stack engineering of $In_{0.65}Ga_{0.35}As/GaAs_{0.4}Sb_{0.}$heterojunction n-channel TFET. In-situ nitrogen plasma treatment is found to improve the characteristics of the metal oxide semiconductor capacitor (MOSCAP) in comparison to ex-situ chemical cleaning. A self-aligned nano-pillar process flow for TFET fabrication is introduced and the improvement in electrical characteristics with nitrogen passivation is quantified. Further, thermal evaporation gate metallization scheme is shown to drastically improve the MOSCAP as well as TFET characteristics in comparison to the electron-beam evaporation scheme. Fast IV measurements are performed to minimize the interface state response and demonstrate kT/q switching slope at drain voltage of 0.5V. The results are then benchmarked with the state of the art TFET data.

II. Experimental Procedure

Figure 2-1 (a) shows the schematic layer structure of $In_{0.65}Ga_{0.35}As/GaAs_{0.4}Sb_{0.6}$ heterojunction TFET grown on semi-insulating InP substrate using solid source molecular beam (MBE) epitaxy. Linearly graded $Al_{1-x}In_xAs$ buffer was used accommodate the lattice mismatch between the active layers ($In_{0.65}Ga_{0.35}As/GaAs_{0.4}Sb_{0.6}$) and the InP substrate. InAs like surface termination was implemented while switching from $GaAs_{0.4}Sb_{0.6}$ to $In_{0.65}Ga_{0.35}As$ to maintain high quality the heterojunction [39][41]. This was achieved by adding 1-2 monolayers of Indium prior to $In_{0.65}Ga_{0.35}As$ layer while ramping up the As flux from 40% to 100%. The effective barrier height (E_{Beff}) for this material system is expected to be 0.31eV (figure 2-1 (b)).

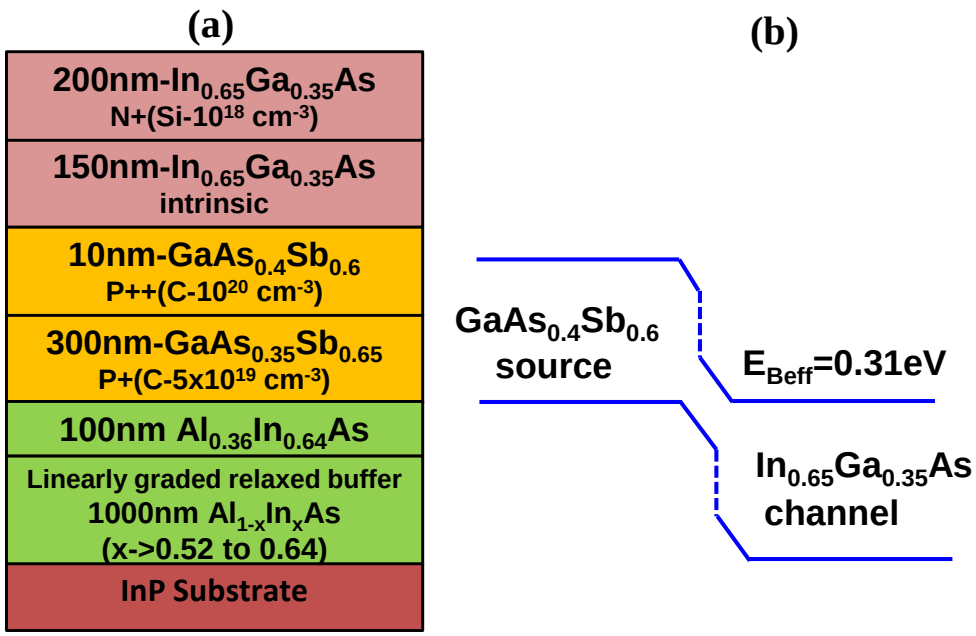

Figure 2-1. (a) Schematic of the MBE grown layer structure of the TFET. (b) Energy band-diagram showing E_{Beff} of 0.31eV.

For the ex-situ cleaned MOSCAP fabrication, lightly n-type doped ($5x10^{17}$ cm^{-3}) bulk $In_{0.53}Ga_{0.47}As$ substrate was degreased in acetone, methanol and IPA. The MOSCAP sample was dipped in 1:10 HCl:DI water solution for 2 minutes and immediately dipped in dilute NH_4OH solution (5%) for 1 minute. The sample was then immediately loaded in the rapid thermal

annealing (RTA) chamber to carry out annealing in nitrogen ambient for 7 minutes, at 400^{o}C. The sample was then immediately transferred to the atomic layer deposition (ALD) chamber at a temperature of 300^{o}C. 200 cycles of trimethylaluminum (TMA) pre-pulsing was performed followed by deposition of 4nm of HfO_2 at a pressure of 400mTorr and temperature of 300^{o}C. Platinum gate metal was deposited using electron-beam evaporation technique through a shadow mask. Post gate metal forming gas anneal (FGA) was carried out in the RTA chamber at 300^{o}C for 10 minutes.

For the in-situ nitrogen plasma cleaned MOSCAP fabrication, n-type $In_{0.53}Ga_{0.47}As$ with a doping of $1x10^{17}$ cm^{-3} grown by MBE on InP was used. After a 3 minutes clean in buffered HF solution, samples were transferred to the ALD chamber where they were exposed to 7 cycles of nitrogen plasma and TMA pulses. Each cycle consisted of a nitrogen gas set-up step (5 seconds at 20mTorr), a nitrogen plasma pulse [inductively coupled plasma (ICP) power of 100W at 20 mTorr for 2 seconds], a pump step (5 seconds),a short TMA pulse (40ms), followed by an Ar gas draw/purge step (7 seconds). After 9 of these cycles, a final nitrogen plasma pulse was added (100W ICP power at 20 mTorr for 2 s), followed by 4 s of a N2 stabilization step. The valve between the plasma and main reaction chambers was opened only during the nitrogen plasma pulse to avoid precursor contamination to the plasma chamber. The substrate temperature was 300^{o}C for both plasma cleaning and ALD HfO_2 growth. The chamber reactor was held at 200 mTorr during oxide deposition. The deposition cycle used was as follows: a TEMAH (tetrakis[ethylmethylamino]hafnium) pulse for 1 s (flowing 250 sccm Ar gas through a bubbler held at 60^{o}C) followed by an Ar gas purge step (7seconds) then a short pulse of deionized water (500ms) followed by pump (7 seconds) and Ar gas purge (5 seconds) steps. After dielectric deposition, the samples were annealed in a tube furnace at 400^{o}C for 15 minutes in forming gas at atmospheric pressure. The gate metal comprised of either electron-beam evaporated palladium or thermally evaporated nickel. No post gate metal anneal was performed.

Figure 2-2 shows the fabrication process flow of the vertical TFET [42]. Fabrication starts with degreasing the wafer in acetone, methanol and IPA. This was followed by chemical cleaning in HF:DI water solution (1:50) for 30 seconds. The sample was then immediately loaded into the sputtering chamber where 300nm of Molybdenum was deposited. The Molybdenum coated wafer was then patterned by electron-beam lithography to define etch mask patterns. Etch mask comprising of 30nm Titanium/60nm Chromium was deposited using electron-beam evaporation process. Molybdenum and the underlying semiconductor regions comprising of the N+ drain, intrinsic channel and P+ source were etched to form vertical pillar like structure. Citric acid based wet etch was then carried out to selectively etch $In_{0.65}Ga_{0.35}As$ over Molybdenum to create an under-cut. Gate oxide was then deposited using atomic layer deposition after appropriate surface preparation either through chemical cleaning or plasma cleaning (same as in the case of MOSCAP). Using electron-beam lithography the gate region was patterned and then gate metal was deposited either using electron-beam evaporation process or thermal evaporation process. The gate metal rests on the sidewalls of the pillar and the under-cut prevents any shorting between the gate metal and the top N+ region. Next, source contact was defined using electron-beam lithography and oxide was etched off using a dry etch recipe. Source contact comprising of Ti/Pd/Au was evaporated using the electron-beam evaporation process. An inter layer dielectric (ILD) was then spin coated and cured within nitrogen ambient at $250^{o}C$ for 1hour. ILD was then etched back in oxygen plasma until the top of the Molybdenum was exposed. Drain contact was then defined by electron-beam lithography and drain metal comprising of Ti/Pd/Au was evaporated using electron-beam evaporation process and then lifted off. Finally, ILD was etched off from the gate and source regions using oxygen based plasma so that electrical contact can be established with the contacts. Figure 2-3 shows the cross section transmission electron microscopy (TEM) image of the fabricated TFET.

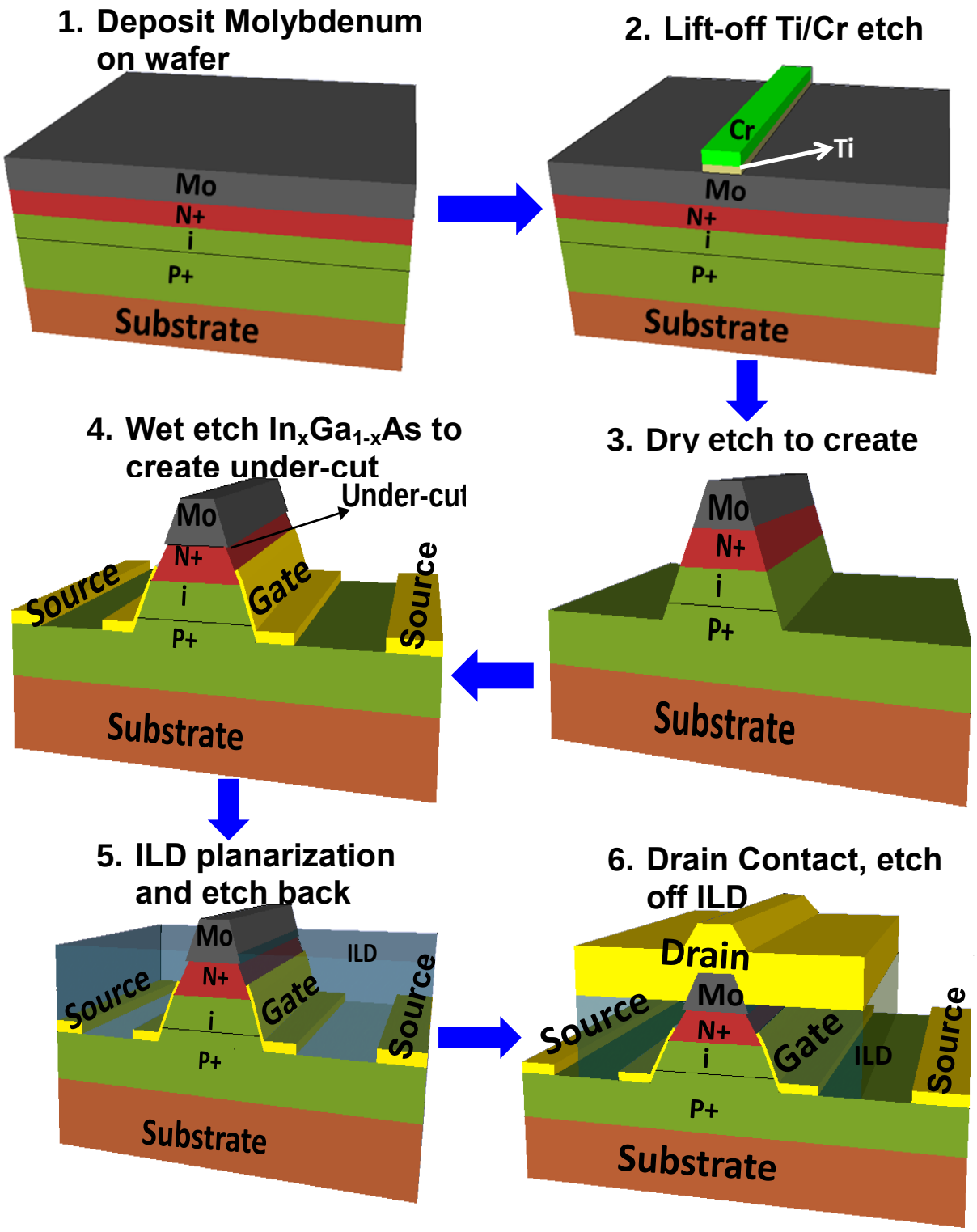

Figure 2-2. Schematic of the nano-pillar process flow for TFET fabrication.

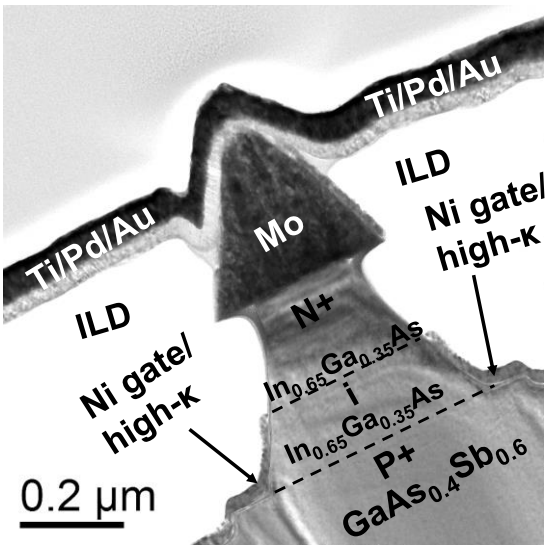

Figure 2-3. Cross section TEM image of the fabricated TFET using the process flow described in figure 2-2.

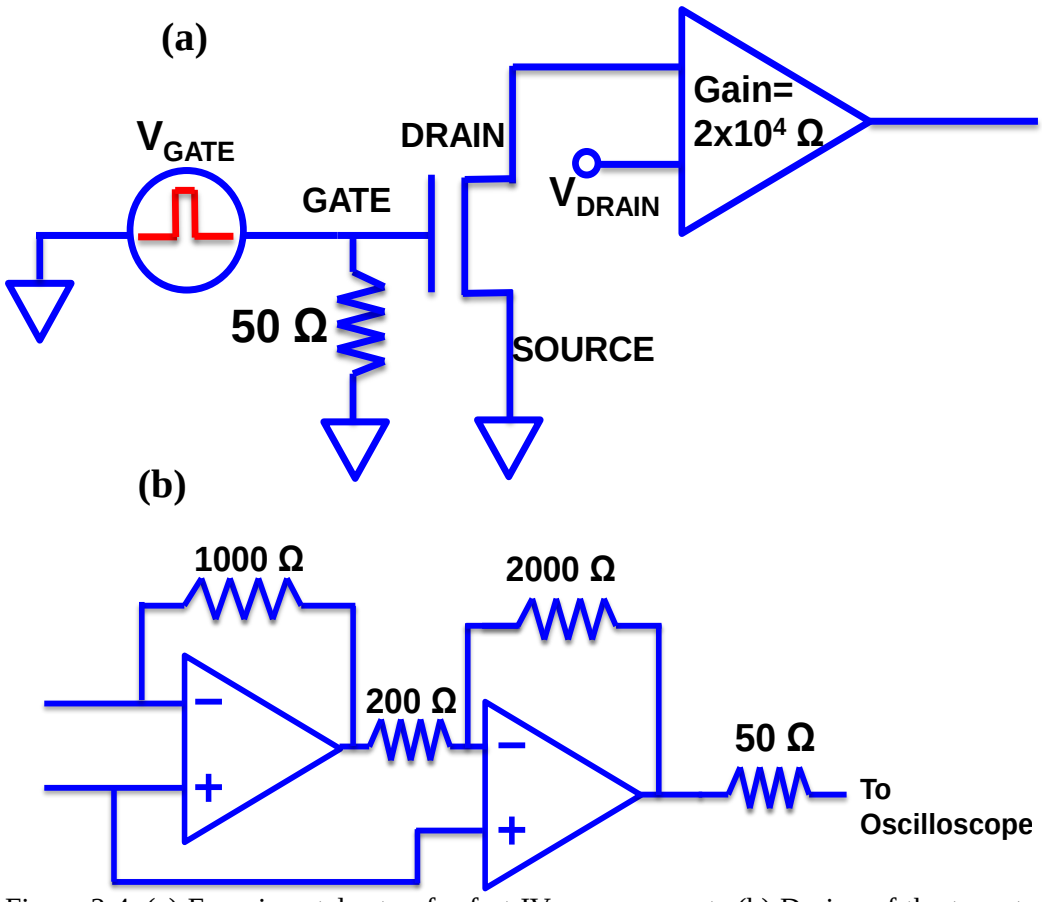

Figure 2-4. (a) Experimental setup for fast IV measurements (b) Design of the two stage current to voltage converter.

Figure 2-4 (a) shows the experimental setup for the fast IV measurements .The input gate voltage pulse had a rise time of 1μs. A current pre-amplifier was connected between the drain terminal and the drain supply voltage. A low pass filter was connected at the output of the drain supply to ensure a stable voltage supply. The pre-amplifier consisted of a two stage trans-impedance amplifier, each stage having an OPAMP as the amplifier with negative feedback through resistors as shown in Figure 2-5 (b). The overall gain of the amplifier was $2x10^4$. The gate probe was terminated with 50 ohms to avoid any reflections during the high frequency gate voltage pulsing. Agilent 81110 function generator was used to create the gate voltage pulses and the drain current response was recorded in LeCroy oscilloscope. The skew between the input voltage pulse and the output voltage in the oscilloscope was properly accounted for.

III. Material Characterization

The structural property of the TFET was characterized by cross-sectional TEM. Figure 2-5 shows the cross-section TEM image of the $In_{0.65}Ga_{0.35}As/GaAs_{0.4}Sb_{0.6}$ TFET structure. All layers were labeled in the figure and $In_{0.65}Ga_{0.35}As/GaAs_{0.4}Sb_{0.6}$ denoted by arrow. It can be seen that the linearly graded $Al_{1-x}In_xAs$ buffer layer effectively accommodates the lattice mismatch induced defects between the active layers and the InP substrate. It can also be seen that no threading dislocations were observed in both the $GaAs_{0.4}Sb_{0.6}$ and $In_{0.65}Ga_{0.35}As$ layers and their interface at this magnification, indicating a threading dislocation density on the order of or below $10^7 cm^{-2}$ in this region. The low dislocation density within active layers and the $In_{0.65}Ga_{0.35}As/GaAs_{0.4}Sb_{0.6}$ suggests high crystalline quality of the TFET structure which is crucial for the device performance in the fabricated TFET [43].

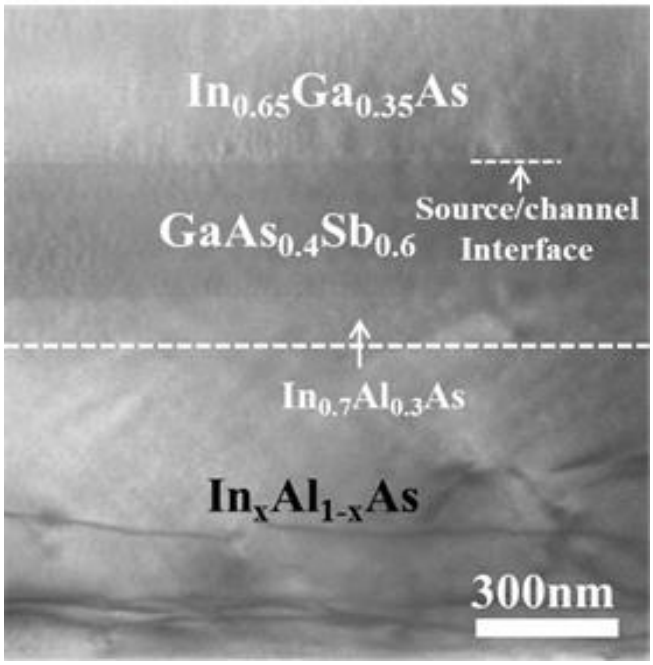

Figure 2-5. Cross-section TEM image of TFET structure. No threading dislocations were found in the $In_{0.65}Ga_{0.35}As$ and $GaAs_{0.4}Sb_{0.6}$ layers.

IV. Results and Discussions

Figure 2-6 (a-b) show the measured capacitance-voltage (CV) and conductance-voltage (GV) characteristics respectively of the MOSCAP with ex-situ surface cleaning and before the FGA for the frequency range from 75KHz to 1MHZ. The gate metal was electron-beam evaporated platinum. CV characteristic was found to be highly dispersive and stretched out, indicative of high levels of interface states density (D_{it}). MOSCAP achieved accumulation capacitance density of 1.55μF/cm^2 at 1MHz corresponding to an electrical oxide thickness (EOT) of 2.2nm. Figure 2-6 (c-d) show the CV and GV characteristics of the MOSCAP after FGA. The dispersion in the CV characteristics is significantly reduced in comparison to the pre-annealed CV data. Further, conductance peak was also significantly reduced, indicating a reduction in midgap D_{it} [44]. Maximum accumulation capacitance density of 1.55μF/cm^2 at 1MHz was maintained even after the FGA.

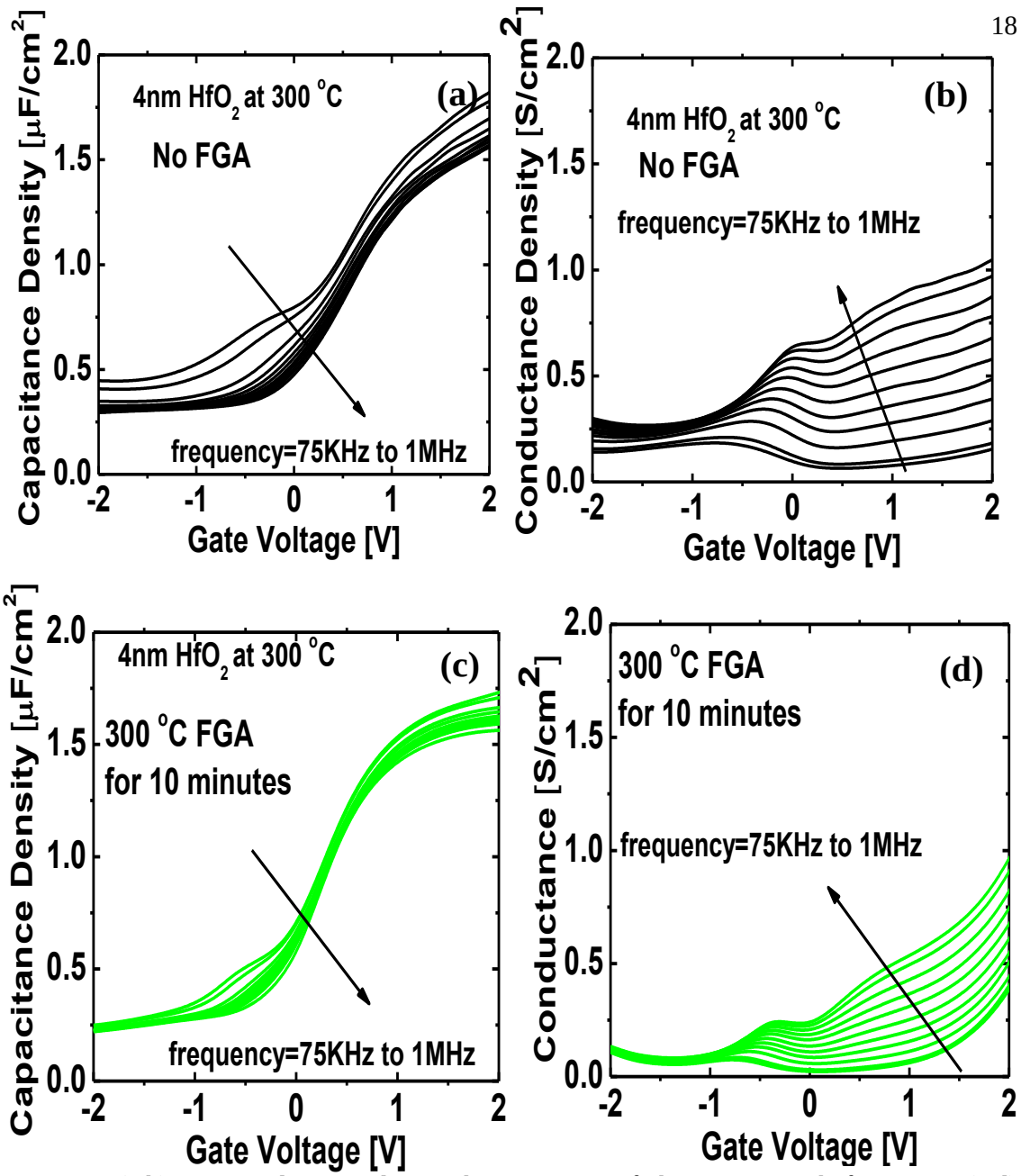

Figure 2-6. (a-b) Measured CV and GV characteristics of the MOSCAP before FGA (c-d) Measured CV and GV characteristics of the MOSCAP after FGA at 300°C for 10 minutes.

Figure 2-7 (a) shows the transfer characteristics of the fabricated TFET with the same gate stack as in the MOSCAP shown in figure 2-5. However, it should be noted that the pre-annealed gate stack uses a palladium gate metal instead of platinum gate metal used in the MOSCAP in figure 2-6 (a). TFET without FGA achieved ON state current (I_{ON}) of 60 μA/μm at V_{DS}=0.5V. TFET with FGA on the other hand achieved I_{ON} of 115 μA/μm at V_{DS}=0.5V. Further,

drain induced barrier thinning (DIBT) measured at 5nA/μm reduced from 0.32V before FGA to 0.16V after FGA. Lower DIBT is indicative of better electrostatics in the TFET. Figure 2-7 (b) shows the switching slope (SS) measured as function of drain current (I_{DS}) and for V_{DS}=0.05V. A minimum SS of 350mV/decade was achieved without FGA whereas with FGA minimum SS of 175mV/decade was achieved.

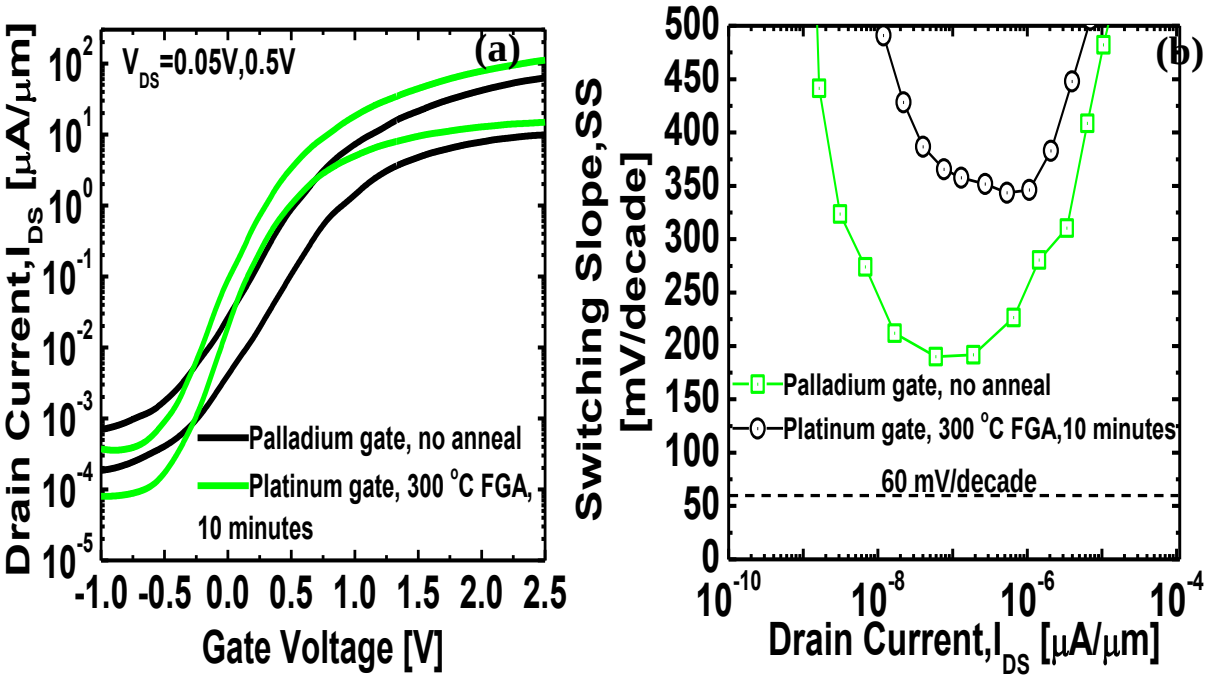

Figure 2-7. a) I_{DS}-V_{GS} characteristics of TFET with and without FGA (b) SS characteristics of TFET with and without FGA.

Though the improvement with FGA is significant, the SS is still poor compared to the desired value. This could be attributed to the thicker EOT of 2.2nm and high density of D_{it}. Interface states is known to degrade the SS of a TFET through trap assisted tunneling and followed by thermionic emission [45] into the conduction band of the channel (TAT). Figure 2-8 is a schematic illustration of TAT in a TFET.

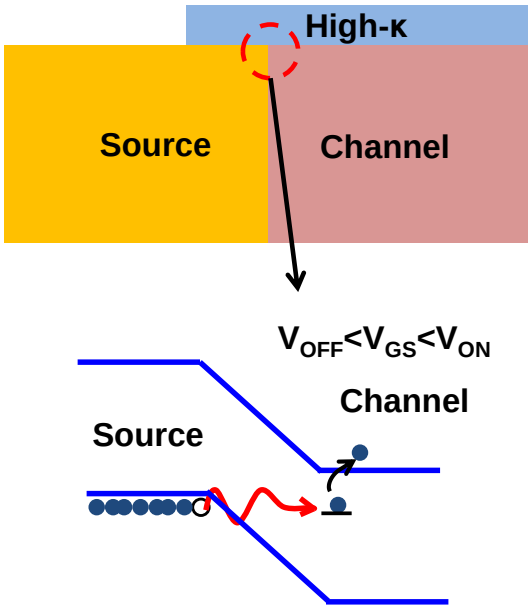

Figure 2-8. Schematic showing TAT mechanism which degrades SS in TFET.

It was recently shown that nitrogen passivation of $In_{0.53}Ga_{0.47}As$ [46][47] reduces the density of midgap states. At the same time, nitrogen passivation also allowed for better nucleation of the ALD precursor and enabled demonstration of sub-1nm equivalent oxide thickness [46]. Density functional theory calculations on GaAs surface showed that in the nitrogen passivated surface, N-N dimers replaced As-As dimers. As-As dimers are known to introduce states within the bandgap. N-N dimers on the other hand do not introduce states in the bandgap and hence results in reduction in the D_{it} [48].

Figure 2-9 (a-b) show the measured CV and GV characteristics of nitrogen passivated MOSCAP with HfO_2 thickness of 4nm measured in the frequency range 75KHz to 1MHz. Frequency dispersion was seen to be significantly lower in comparison to the ex-situ cleaned MOSCAP shown in figure 2-5 (c). Further, the frequency dependent "hump" at negative gate bias is also much lower indicative of lower density of midgap D_{it}. Accumulation capacitance density of 0.8 $\mu F/cm^2$ corresponding to an EOT of 4.3nm was achieved. Figure 2-9 (c-d) show the

measured CV and GV characteristics of nitrogen passivated MOSCAP with HfO_2 thickness of 3nm measured in the frequency range 75KHz to 1MHz. The frequency dependent "hump" [43] is found to be slightly higher than in MOSCAP with 4nm HfO_2. Further, the peak value of conductance density was also found to be higher in the 3nm HfO_2 MOSCAP, another indicator of midgap D_{it}.

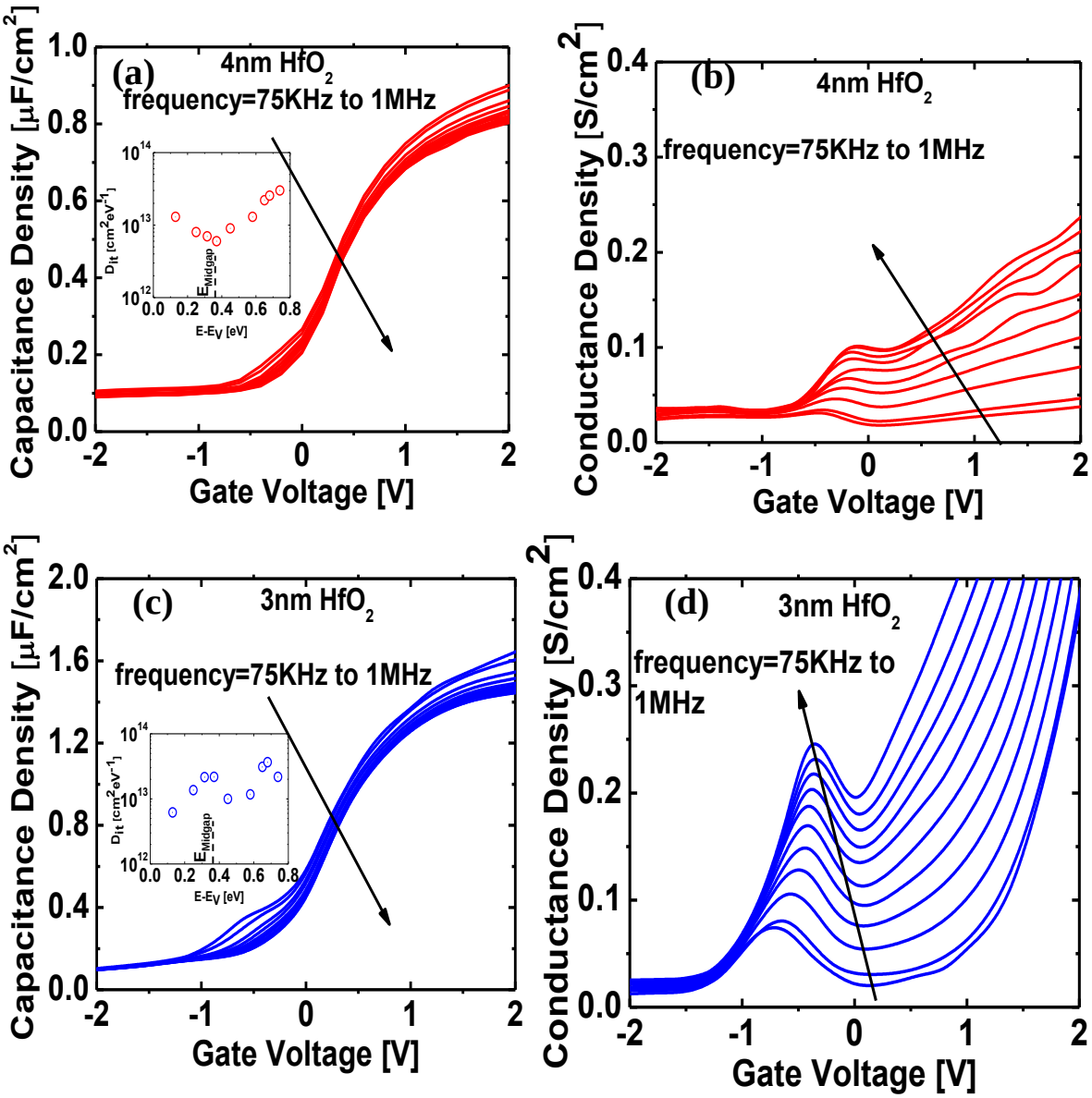

Figure 2-9. (a-b) Measured CV and GV characteristics of nitrogen passivated MOSCAP with 4nm HfO_2. (c-d) Measured CV and GV characteristics of nitrogen passivated MOSCAP with 3nm HfO_2.

Accumulation capacitance density of 1.5µF/cm2 was achieved corresponding to EOT of 2.3nm. The inset of Figure 2-9 (a) and Figure 2-9 (c) show the D_{it} as a function of position in the bandgap extracted using Terman method. Midgap D_{it} was $5x10^{12}cm^{-2}eV^{-1}$ in the case of 4nm HfO_2 MOSCAP and $2x10^{13}cm^{-2}eV^{-1}$ in the case of 3nm HfO_2 MOSCAP. Increased conductance at higher gate bias in the 3nm HfO_2 MOSCAP was due to gate leakage (not shown).

TFETs were fabricated to evaluate the impact of nitrogen passivation and gate oxide scaling. Figure 2-8 (a) shows the transfer characteristics of TFET measured at V_{DS}=0.05V, 0.5V and at T=300K. In both cases, I_{ON} of 200µA/µm was achieved. This corresponds to a 75 % increase in I_{ON} in comparison to the TFET shown in Figure 2-6. DIBT was measured to be 0.14V and 0.1V in TFET with 3nm HfO_2 and 4nm HfO_2 respectively. Figure 2-8 (b) shows the SS measured as a function of drain current. A minimum switching slope of 160 mV/decade was achieved in 3nm HfO_2 as well as 4nm HfO_2 TFET. Thus even though EOT in 3nm HfO_2 TFET was smaller than the 4nm HfO_2 TFET, the SS performance is similar. This could be attributed to the higher level of midgap D_{it} seen in the 3nm HfO_2 MOSCAP. Thus thinner EOT compensated for the higher midgap D_{it} resulting in comparable minimum SS. It should be noted that even though nitrogen passivation has improved the overall TFET characteristics, SS is still poor.

It is known that X-ray and high energetic ions generated during the electron-beam evaporation process can significantly damage the oxide/semiconductor interface [49] [50]. Further, it is also possible that growth of interfacial layer takes place during the electron-beam evaporation process which would reduce the EOT of the gate stack. Thermal evaporation process is known to cause less damage to the oxide/semiconductor interface. To evaluate the impact of gate metallization scheme, MOSCAP was fabricated with gate stack comprising of nitrogen passivated 4nm HfO_2 and thermally evaporated Ni gate metal. Figure 2-9 (a-b) show the measured CV and GV characteristics. Dramatic improvement was seen. Accumulation capacitance density of $2.25µF/cm^2$ was reached corresponding to an EOT of 1.5nm. Dispersion in

the CV characteristic was also much lower in comparison to the MOSCAP with electron-beam evaporated gate metal. The frequency dependent "hump" in the negative bias regime as well as the conductance peak was reduced significantly. Thus thermal evaporation scheme allowed for simultaneous reduction of density of midgap D_{it} and scaling of EOT. Next, TFET was fabricated to evaluate the impact of gate metallization scheme.

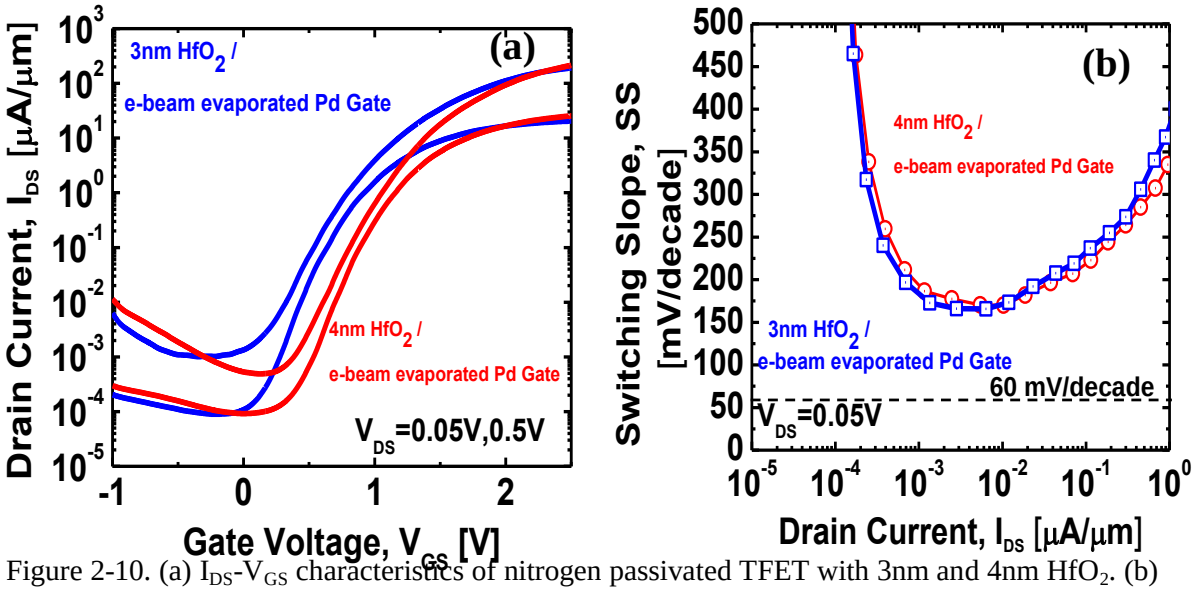

Figure 2-10. (a) I_{DS}-V_{GS} characteristics of nitrogen passivated TFET with 3nm and 4nm HfO_2. (b) SS characteristics of nitrogen passivated TFET with 3nm and 4nm HfO_2.

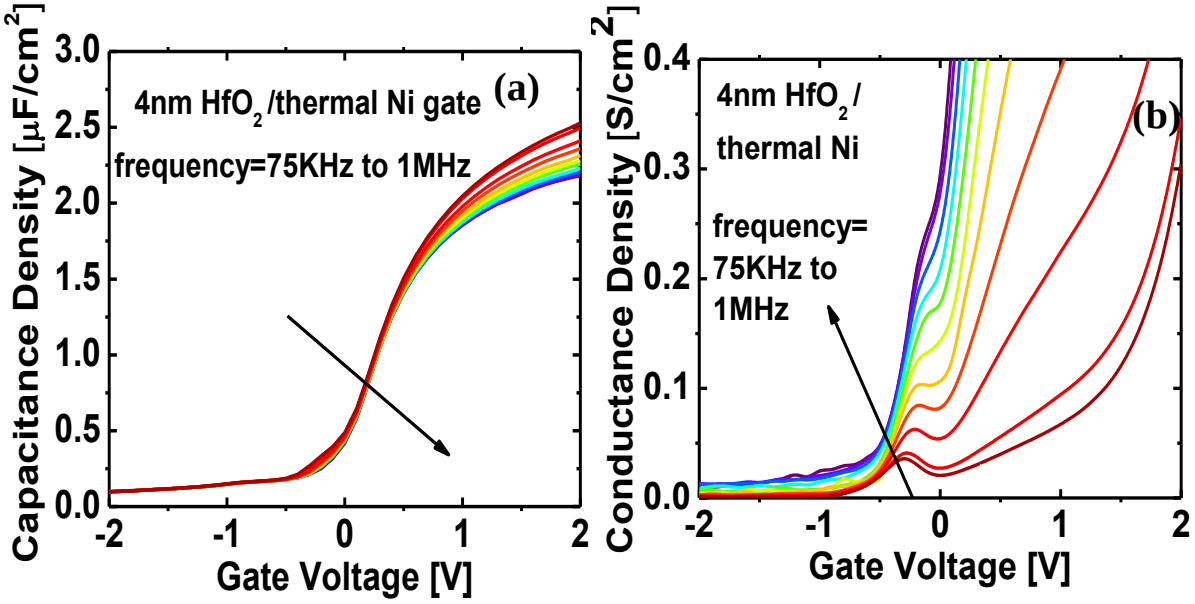

Figure 2-11. (a-b) Measured CV and GV characteristics of MOSCAP with nitrogen passivation and thermally evaporated Ni gate metal.

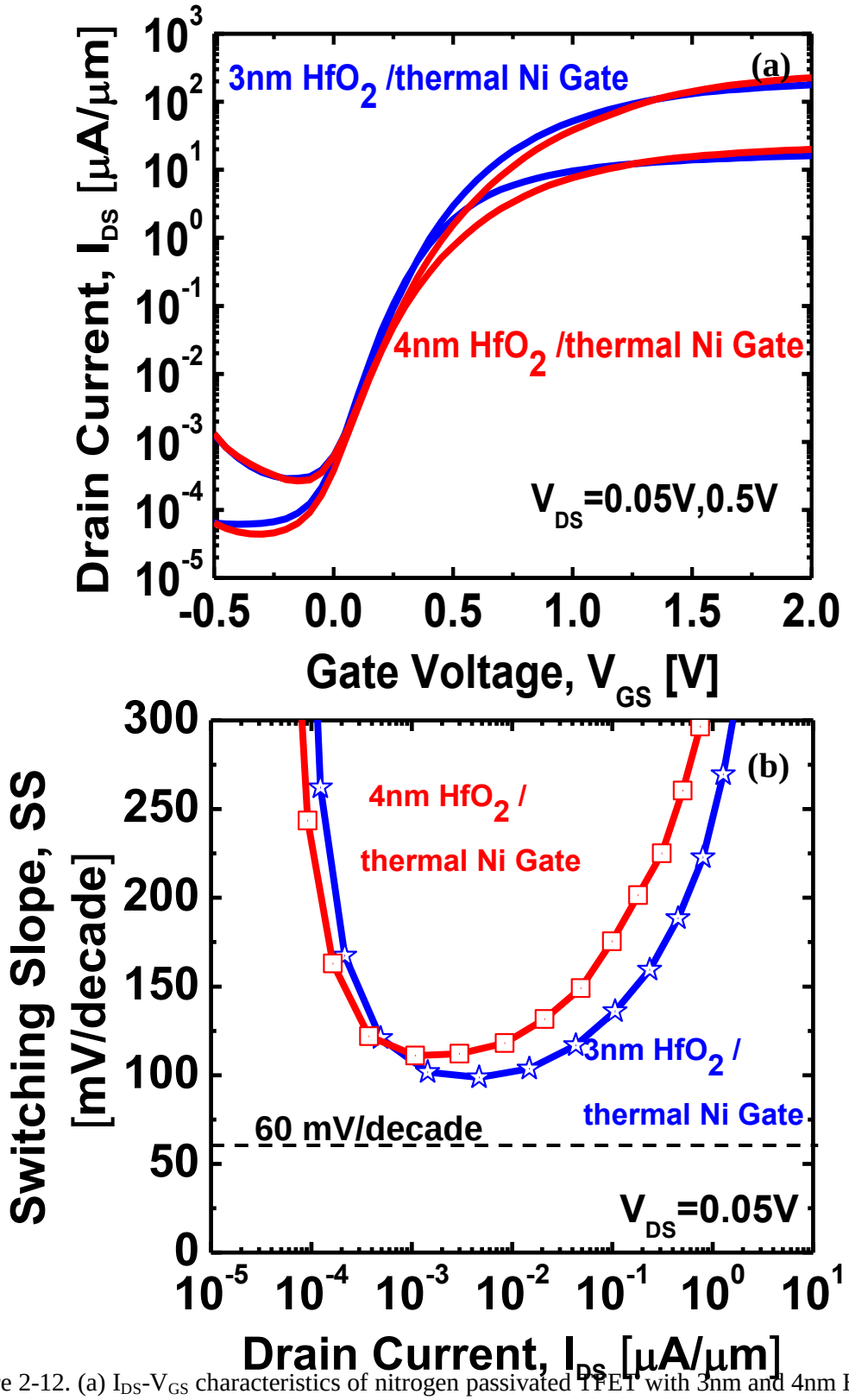

Figure 2-12. (a) I_{DS}-V_{GS} characteristics of nitrogen passivated TFET with 3nm and 4nm HfO_2 and thermal Ni as gate metal. (b) SS characteristics of nitrogen passivated TFET with 3nm and 4nm HfO_2 and thermal Ni as gate metal.

Figure 2-12 (a) shows the transfer characteristics of TFET with 3nm HfO_2 and 4nm HfO_2 measured at V_{DS}=0.05V and 0.5V. In both the TFETs, I_{ON} of 220µA/µm was achieved at V_{DS}=0.5V. This corresponds to a 10 % increase from TFET with electron-beam evaporated gate metal. I_{ON}/I_{OFF} ratio of $7x10^5$ was achieved at V_{DS}=0.5V. Further, DIBT was also close to zero in both the TFETs. Figure 2-13 (b) shows the SS as a function of drain current at V_{DS}=0.05V. In the 4nm HfO_2 TFET, a minimum SS of 105mV/decade was achieved. In the 3nm HfO_2 TFET, a minimum SS of 97mV/decade was achieved. Reduction in SS from 4nm HfO_2 TFET to 3nm HfO_2 TFET could be attributed to EOT scaling. Thus reduction in gate metallization induced damage resulted in significant improvement in device characteristics through scaling EOT and reduction in D_{it}. Figure 2-13 shows the output characteristics of the TFET with 3nm HfO_2 as a function of gate bias. Excellent saturation in the output characteristics was achieved. Negative differential resistance (NDR) was also observed for negative drain bias in the output characteristics. Presence of NDR is an indication of high quality of the tunnel junction.

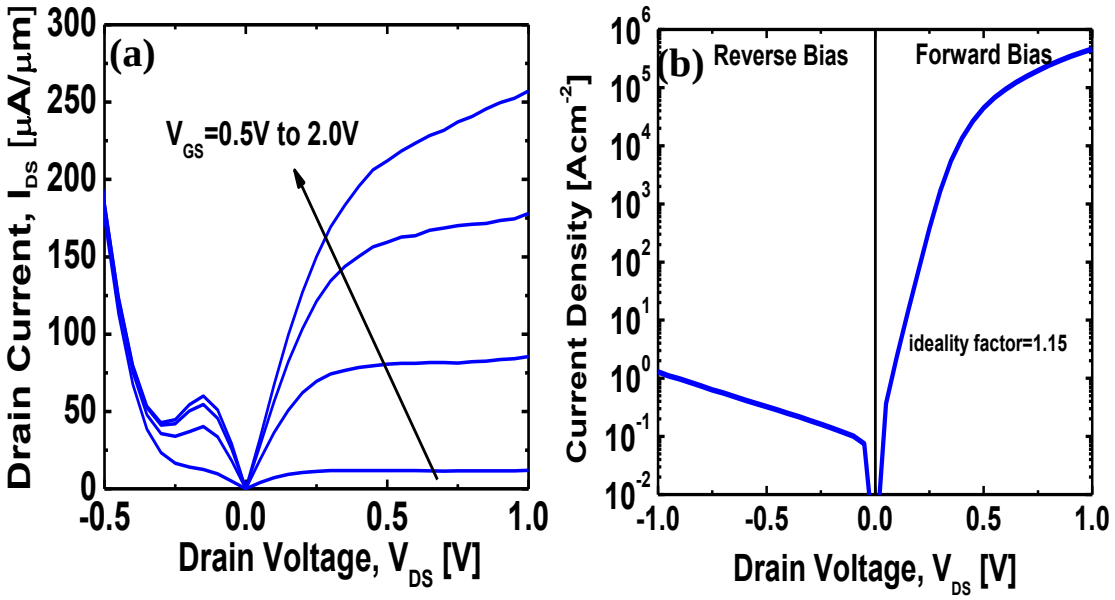

Figure 2-13. (a) Output characteristics of TFET of nitrogen passivated TFET with 3nm HfO_2. (b) Two terminal diode characteristics of the ungated TFET.

Figure 2-13 (b) shows the two-terminal diode characteristics of the TFET (ungated). Ideality factor of 1.15 was extracted over current range of $1Acm^{-2}$ to $10^{3}Acm^{-2}$, which indicates good quality of the heterojunction. Further, the reverse leakage current scaled as a function of cross-section area of the diode indicating less damage to the sidewall during the etch process.

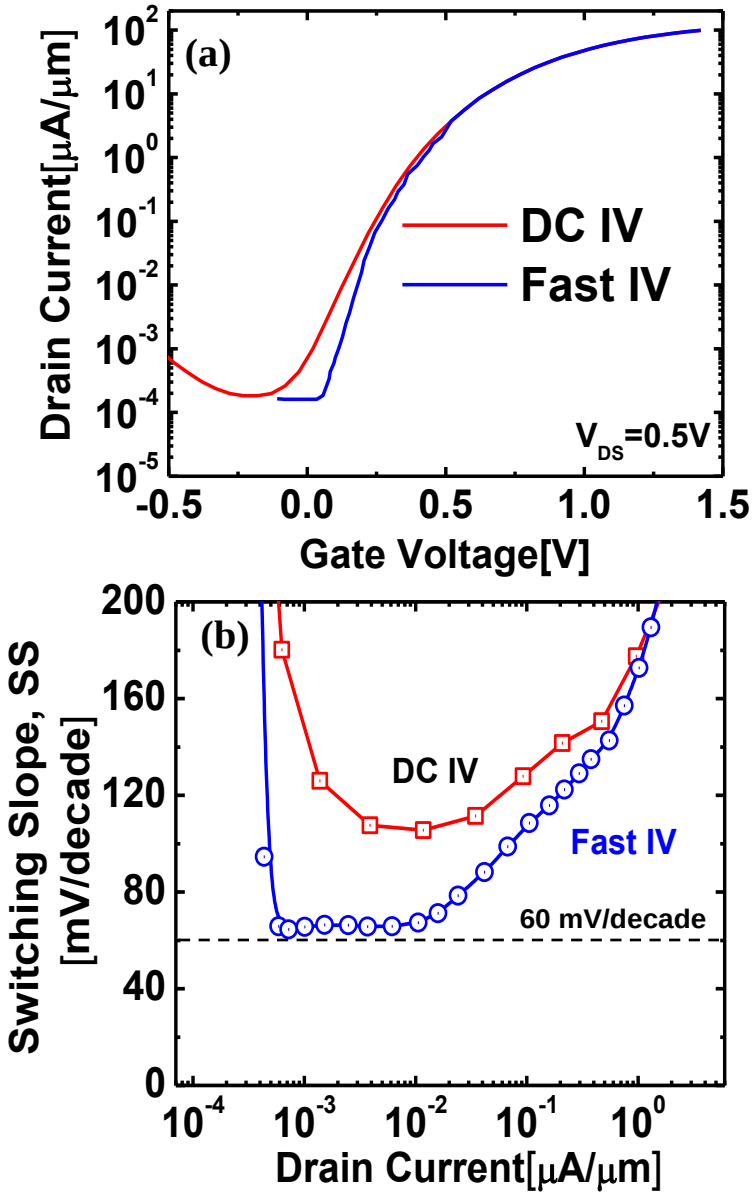

Figure 2-14. (a) Comparison of DC and fast I_{DS}-V_{GS} characteristics of nitrogen passivated TFET with 3nm HfO_2 and thermal Ni gate metal. (b) SS improvement of nitrogen passivated TFET with 3nm HfO_2 and thermal Ni gate metal with fast IV measurement.

To minimize the trap response in the 3nm HfO_2 TFET, fast IV measurement was carried out. The rise time of the gate voltage pulse was 1μs and V_{DS} was kept at 0.5V. Figure 2-13 (a-b) shows the I_{DS}-V_{GS} and SS characteristics in comparison with the DC characteristics. Significant steepening in the I_{DS}-V_{GS} characteristic is observed with fast IV measurements. A minimum SS (SS_{MIN}) of 64mV/decade was achieved with fast IV measurements.

Figure 2-15 summarizes the evolution of SS_{MIN} measured at V_{DS}=0.5V. With in-situ nitrogen plasma treatment, SS_{MIN} improved from 210mV/decade 185mV/decade. Using thermal gate metal evaporation technique SS_{MIN} drastically reduced to 120mV/decade. By scaling of EOT (reduction in HfO2 thickness from 4nm to 3nm), SS_{MIN} further reduced to 105mV/decade. Finally, using fast IV measurements, trap response was minimized and this SS_{MIN} of 64mV/decade was achieved.

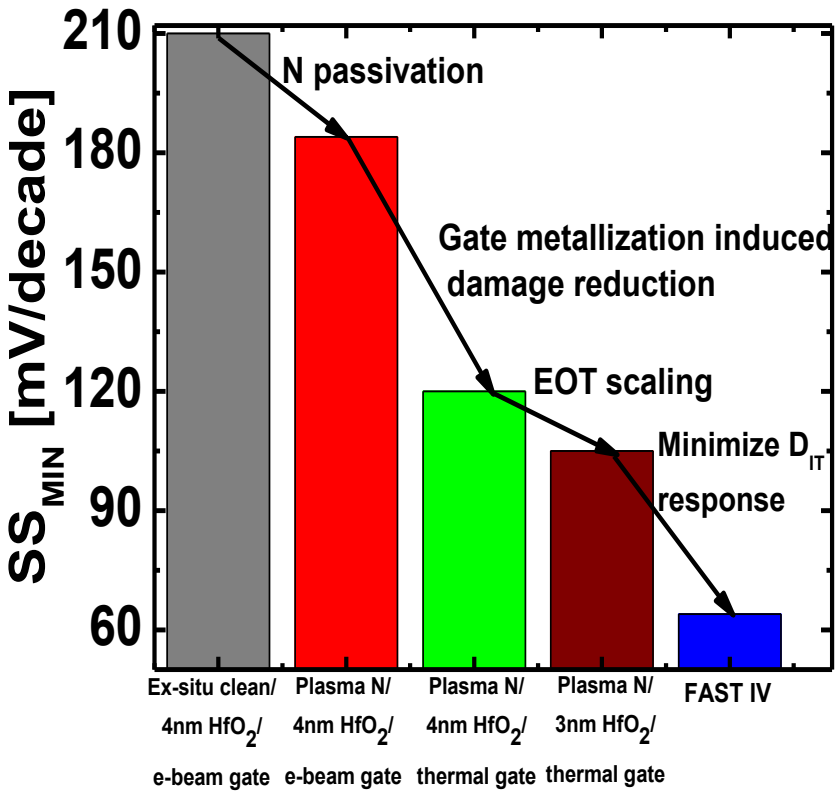

Figure 2-15. Evolution of SS_{MIN} at V_{DS}=0.5V with gate stack engineering and fast IV measurements.

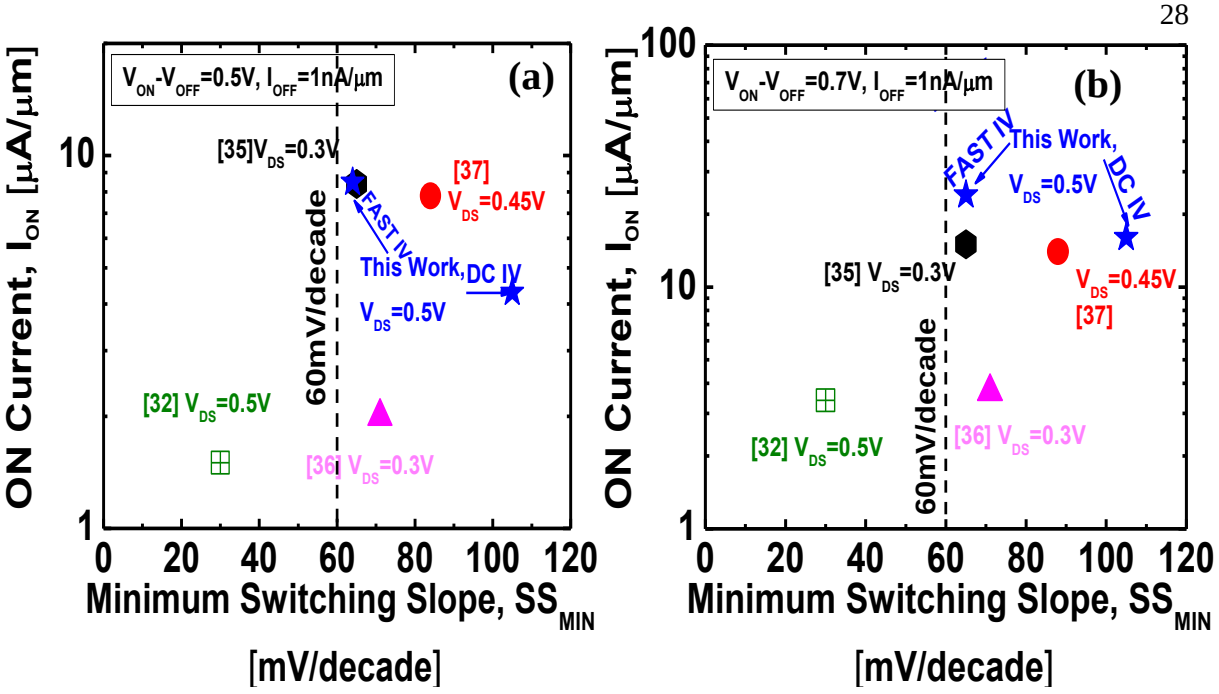

Figure 2-16. (a) Benchmarking I_{ON} vs SS_{MIN} at V_{ON}-V_{OFF}=0.5V.(b) Benchmarking I_{ON} vs SS_{MIN} at V_{ON}-V_{OFF}=0.7V.

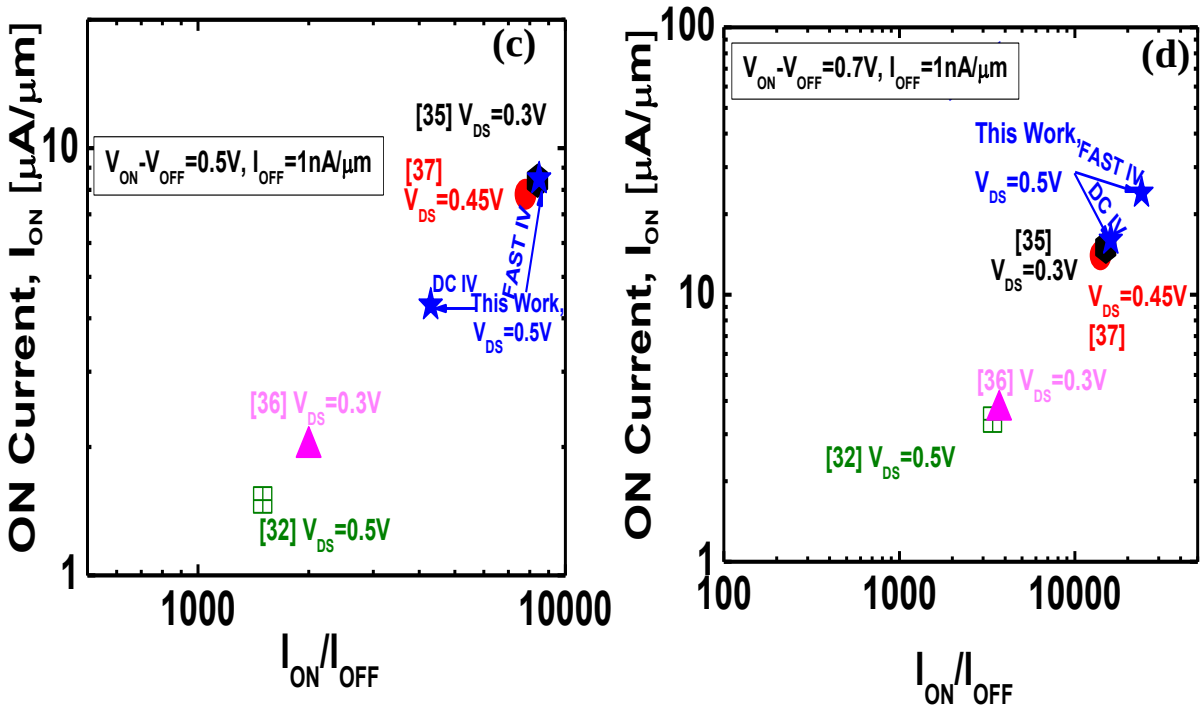

Figure 2-17. (a) Benchmarking I_{ON} vs I_{ON}/I_{OFF} at V_{ON}-V_{OFF}=0.5V. (b) Benchmarking I_{ON} vs I_{ON}/I_{OFF} at V_{ON}-V_{OFF}=0.7V.

V. Benchmarking and Projections

Figure 2-16 (a) shows I_{ON} as a function of SS_{MIN} in comparison with the best TFET experimental data reported till date. I_{OFF} was fixed at 1na/μm and V_{ON}-V_{OFF} was fixed at 0.5V. It can be seen that the performance of TFET presented in this chapter was comparable to $In_{0.53}Ga_{0.47}As$ TFET reported in [35] and outperformed other reported TFET. At a slightly higher V_{ON}-V_{OFF} of 0.7V, TFET reported in this chapter outperformed all other reported TFETs in terms of achieving highest I_{ON} maintaining lowest SS_{MIN} (Figure 2-16 (b)). Figure 2-17 (a-b) shows I_{ON} as a function of I_{ON}/I_{OFF} measured at V_{ON}-V_{OFF} of 0.5V and 0.7V respectively. At V_{ON}-V_{OFF} of 0.5V, TFET presented in this work showed comparable performance as $In_{0.53}Ga_{0.47}As$ TFET reported in [35] whereas at V_{ON}-V_{OFF} of 0.7V showed the best performance in terms of achieving high I_{ON} as well as I_{ON}/I_{OFF} ratio.

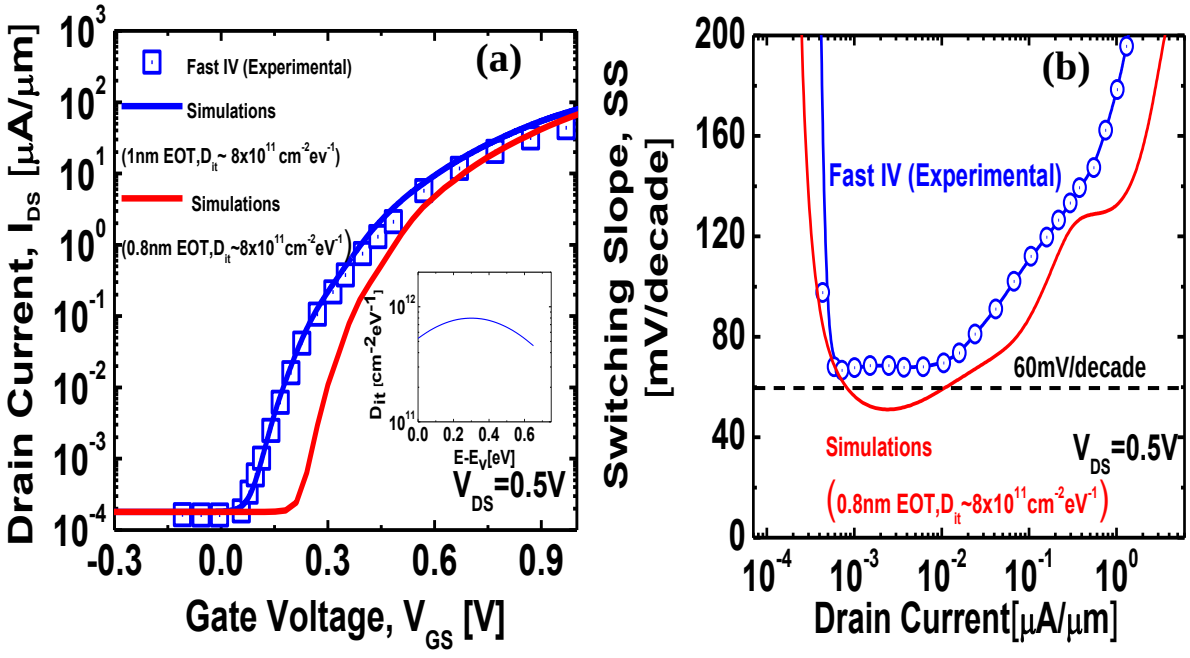

Figure 2-18. (a) Calibration and projection of I_{DS}-V_{GS} characteristic of TFET using numerical simulations. (b) Comparison of experimental and projected SS as a function of drain current.

Figure 2-18 (a) shows the calibration of the fast IV data using numerical simulations. The D_{it} profile used for simulations is shown in the inset. Good match with measured characteristics is seen assuming midgap D_{it} of $8x10^{11}cm^{-2}eV^{-1}$. With further scaling of EOT, SS is expected to be below 60mV/decade over a range of drain current as shown in Figure 2-18 (b).

VI. Conclusions

To summarize, in this chapter it was shown that nitrogen passivation combined with thermal gate metallization scheme enabled EOT scaling and D_{it} reduction. $In_{0.65}Ga_{0.35}As/GaAs_{0.4}Sb_{0.6}$ heterojunction TFET fabricated with the above gate stack showed much improved characteristics in terms of low SS, DIBT and high $I_{ON.}$ With fast IV measurements, SS was further reduced to 64mV/decade which is one of the lowest reported in the category of III-V TFET. Benchmarking against the state of the art TFET results showed that $In_{0.65}Ga_{0.35}As/GaAs_{0.4}Sb_{0.6}$ heterojunction TFET achieved highest drive current at V_{ON}-V_{OFF} of 0.7V in the category of TFET.

Chapter 3

Development of a Planarization Scheme and Demonstration of Gigahertz Switching in $In_{0.9}Ga_{0.1}As/GaAs_{0.18}Sb_{0.82}$ n-channel TFET

I. Introduction

All experimental demonstration of TFET till date has focused on the DC characteristics like the switching slope and the ON state drive current. The high frequency switching characteristics of TFET have not been explored. TFET can potentially operate at very high frequencies in the range of gigahertz with lower operating power in comparison to CMOS [29] which is handy for applications where power concerns are critical, such as processing and transmitting information from devices implanted inside the human body.

This chapter presents a novel planarization scheme developed to incorporate co-planar wave guide structures in a vertical TFET. Incorporation of the waveguide structure allowed for the demonstration of the high frequency characteristics of the tunnel FET for the first time. The cut off frequency of a transistor to first order depends on the ratio of transcondunctance to the overall gate capacitance. Hence, in order to enhance the TFET performance in the high frequency regime, a near broken-gap material system was selected with enhanced DC transconductance in comparison to staggered-gap TFET demonstrated in chapter 2. $In_{0.9}Ga_{0.1}As/GaAs_{0.18}Sb_{0.82}$ material system was chosen to realize a near broken-gap TFET. The fabricated near broken-gap TFET exhibited gigahertz small signal switching performance at V_{DS} of 0.3V. Further, the near broken-gap TFET also exhibited highest reported ON state current among any reported TFET till date.

II. Experimental Procedure

Figure 3-1 (a) shows the layer structure of $In_{0.9}Ga_{0.1}As/GaAs_{0.18}Sb_{0.82}$ TFET grown using solid source molecular beam epitaxy (MBE) on lattice mismatched InP substrate. Linearly graded $In_xAl_{1-x}As$ buffer was used to prevent the defects from extending into the critical regions of the TFET. Figure 3-1 (b) shows the schematic of the heterojunction band alignment of this structure. Effective barrier height of 0.04eV was expected in this TFET structure. Hence $In_{0.9}Ga_{0.1}As/GaAs_{0.18}Sb_{0.82}$ material system allowed demonstration of a near-broken gap TFET (NBTFET). Internal photoemission (IPE) spectroscopy was performed to measure the band-alignment of NBTFETs. Figure 3-2 (a) shows the experimental setup used for IPE measurements. $In_{0.9}Ga_{0.1}As$ layer was thinned down to 10nm by wet etching in a 1:20 hydrogen peroxide:citric acid solution. 15nm of Al_2O_3 was deposited by atomic layer deposition (ALD) technique at 200 ^oC. Graphene was used as the gate metal electrode for the IPE measurements. Graphene was grown by chemical vapor deposition process on a copper foil and transferred to the sample. The incident light with photon energy from 1.5 eV to 6.0 eV was produced by a 150 Watt broadband Xenon light lamp used in conjunction with a grating monochromator. The output beam from the monochromator was collimated by an achromatic UV-grade lens, and then focused down to a millimeter-size spot by another similar achromatic lens. The graphene electrode surface of the sample was placed normal to the beam at the focal plane. The bias applied across the MOS capacitor was supplied by a regulated power supply and the current recorded by an electrometer at different photon energies [51]. NBTFET for DC characterization was fabricated using the process flow described in chapter 2. Prior to the gate oxide deposition, sample was dipped in a 1:10 HCl:DI water solution for 2 minutes and immediately loaded into the ALD chamber where a bilayer stack comprising of 1nm Al_2O_3 and 3.5nm HfO_2 was deposited at a temperature of 200 ^oC. Palladium gate metal was evaporated using electron-beam evaporation technique. For the RF

measurements, Anritsu 37269B Vector Network Analyzer was used. Keithley interactive test environment software was used for S-parameter modeling.

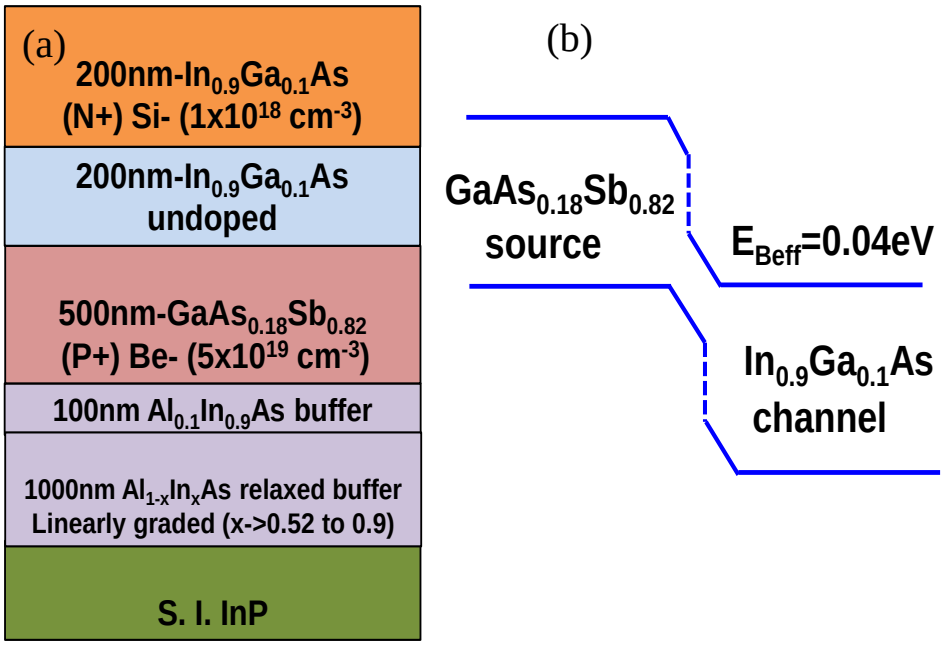

Figure 3-1. (a) Schematic of the MBE grown layer structure of the NBTFET (b) Energy band-diagram showing E_{Beff} of 0.04eV in NBTFET.

III. Material Characterization

Figure 3-2 (b) shows the yield plot as a function of incident photon energy for various gate biases. The barrier height for holes (Φ_h) from the $In_{0.9}Ga_{0.1}As$ conduction band (CB) to the Al_2O_3 valence band (VB) was found to be 3.05 eV from the field independent yield plot (Figure 3-2 (b)). The corresponding Φ_h for the $GaAs_{0.18}Sb_{0.82}$ CB to the Al_2O_3 VB was measured to be 3.72 eV (Figure 3-2(c)). The band-gap of $GaAs_{0.18}Sb_{0.82}$ at room temperature is 0.69eV [52]. Hence, within the limits of measurement accuracy, the effective tunneling barrier (E_{Beff}) of the NBTFET was determined to be 0.02eV. Figure 3-2 (d) illustrates the complete band-alignment of the NBTFET.

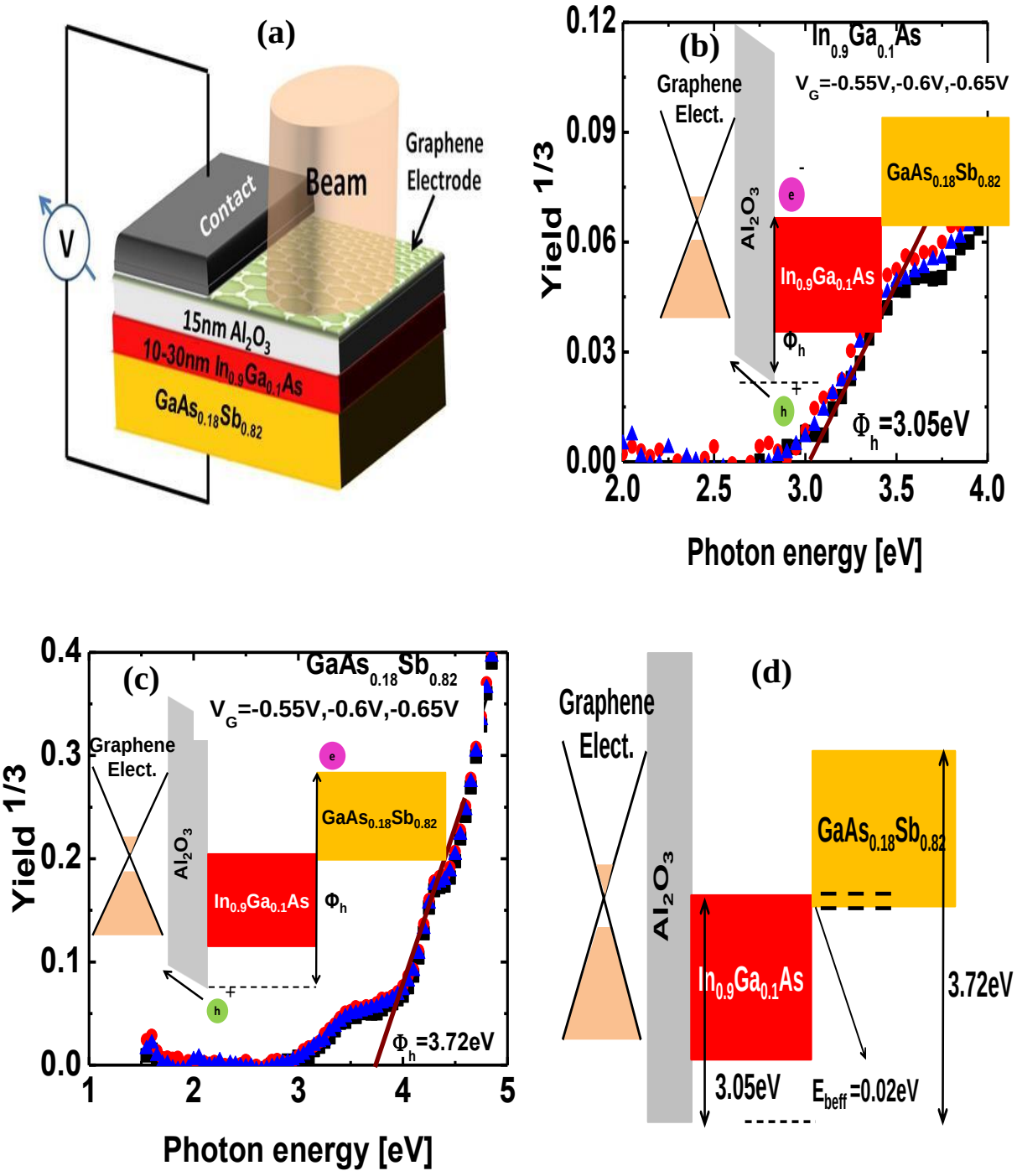

Figure 3-2. (a) Internal photo emission spectroscopy (IPE) experimental setup using graphene as a transparent electrode. (b) Barrier height for hole emission from $In_{0.9}Ga_{0.1}As$ is measured to be 3.05eV. (c) Barrier height for hole emission from $GaAs_{0.18}Sb_{0.82}$ is measured to be 3.72eV. (d) The as-grown NBTFET has an effective barrier height of 0.02eV.

IV. Electrical Characterization

Figure 3-3 (a) shows the DC transfer characteristics of the TFET at V_{DS}=0.05V, 0.5V and measured at temperatures T=77K, 150K and 300K. At T=300K, TFET exhibited ON state current (I_{ON}) of 680μA/μm at V_{DS}=0.5V and V_{GS}=2V. At T=300K, OFF state current (I_{OFF}) is close to 1μA/μm at V_{DS}=0.05V. As the measurement temperature was reduced to T=77K, I_{OFF} reduced to $4x10^{-2}$ μA/μm. Figure 3-3 (b) shows the switching slope (SS) as function of the drain current (I_{DS}) for V_{DS}=0.05V and measured at T=300K, 150K and 77K. Minimum SS at T=300K is 600mV/decade at drain current (I_{DS}) of 10 μA/μm. As the measurement temperature is reduced, I_{OFF} reduces as well as Fermi level movement efficiency improves. Thus at T=77K, a minimum SS of 120mV/decade is achieved at I_{DS} of 0.5μA/μm.

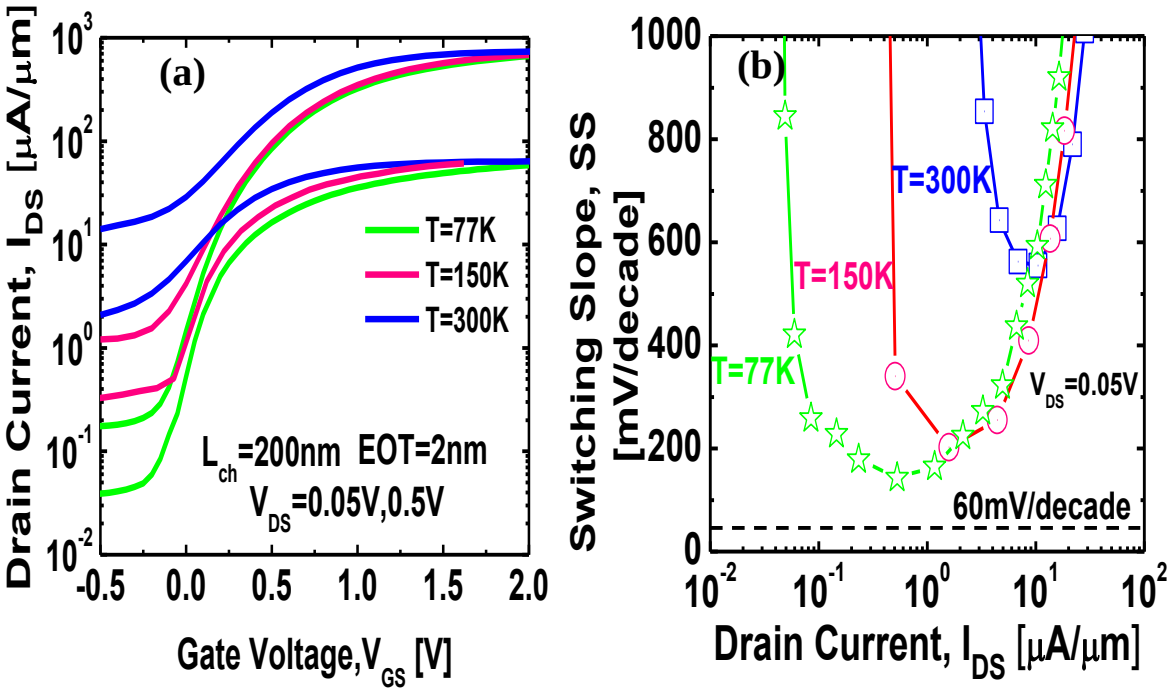

Figure 3-3. (a) Temperature dependent transfer characteristics of NBTFET showing improved I_{ON}/I_{OFF} at low temperature. (b) Switching slope as a function of drain current showing improvement at lower temperature.

Figure 3-4 (a) shows the transcondutance (G_M) characteristics of the NBTFET measured at V_{DS}=0.5V and T=300K. TFET exhibited peak G_M of 680 μS/μm at V_{DS}=0.5V. Figure 3-4 (b)

shows the output characteristics as a function of gate voltage measured at T=300K and 77K. Good saturation in the output characteristics was observed. Further, negative differential resistance characteristic was observed in the output characteristics for negative applied drain bias, indicating high quality tunnel junction and band to band tunneling dominated carrier transport.

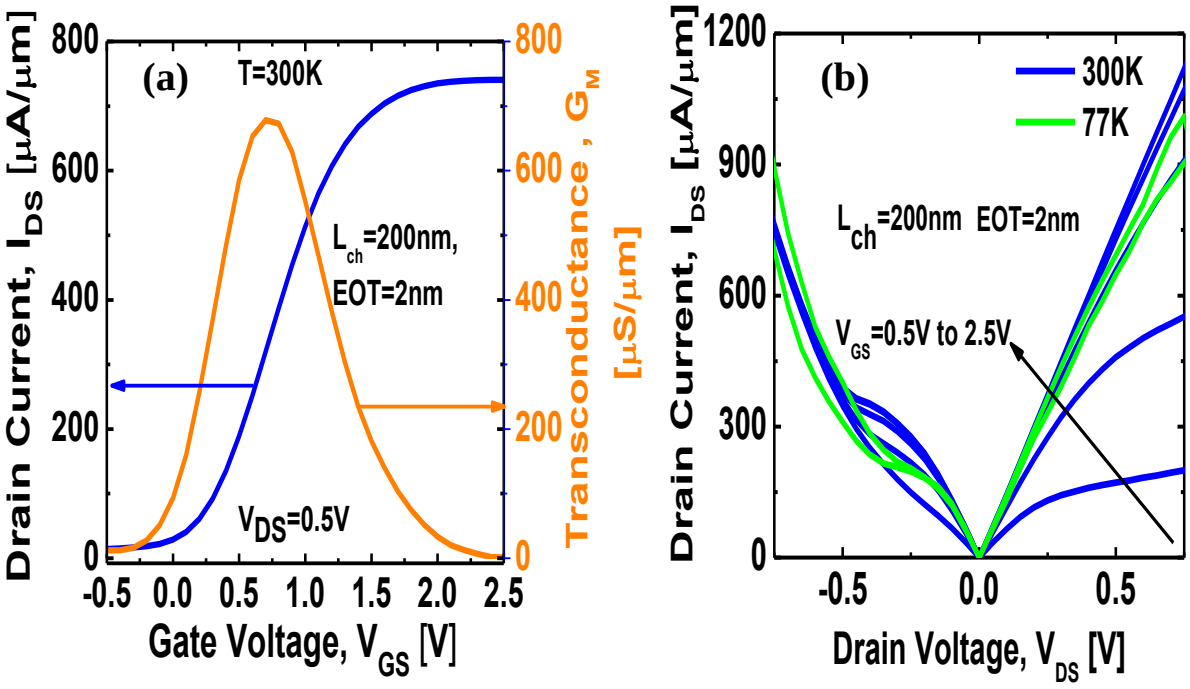

Figure 3-4. (a) NBTFET exhibits peak extrinsic G_M of 680μS/μm at T=300K, V_{DS}=0.5V. (b) Output characteristics of NBTFET at T=300K and T=77K showing the presence of NDR for negative drain bias voltage.

Measured I_{DS}-V_{GS} characteristics at V_{DS}=0.5V was calibrated against numerical simulations using Sentaurus Technology Computer Aided Design (TCAD) software [18] incorporating D_{it} of $5x10^{12}$ $cm^{-2}eV^{-1}$ as shown in Figure 3-5 (a). TCAD calibration allowed for extraction of electron quasi Fermi level movement in the fabricated NBTFET. Electron quasi Fermi level was found to move from deep inside the conduction band edge in the ON state, to close to midgap as the gate voltage is reduced until bulk leakage dominated the overall device characteristics. Figure 3-5 (b) shows the trap time constant calculated as a function of position in the bandgap for T=300K,150K and 77K using capture cross section of InAs [53]. The response

time of the traps close to midgap at room temperature was close to 1µs. With 1µs gate voltage pulsing, traps in the energy range from the mid-gap to 0.03eV away from midgap (towards the conduction band) can be suppressed. With 100ns gate voltage pulsing, traps in the energy range from the mid-gap to 0.1eV (towards the conduction band) can be suppressed.

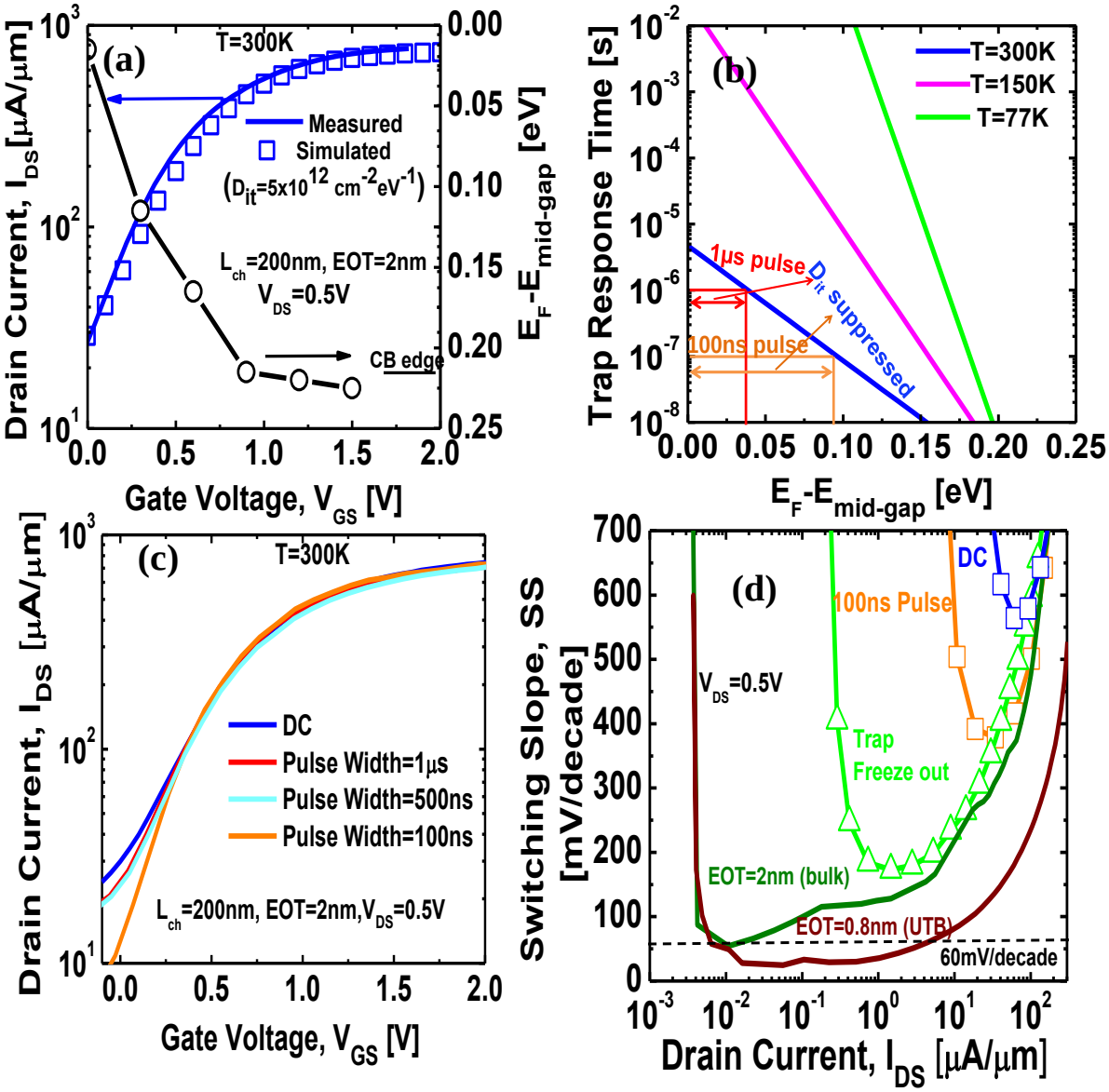

Figure 3-5. (a) Numerical simulation calibrated to measured I_{DS}-V_{GS} characteristics at T=300K is used to map the electron quasi-Fermi level movement in the channel (b) Simulated electron trap response time in $In_{0.9}Ga_{0.1}As$ is used to estimate the gate voltage pulse width required to suppress D_{it} response. (c) Transfer characteristics at T=300K, V_{DS}=0.5V for varying gate pulse widths. (d) SS as a function of drain current at V_{DS}=0.5V showing improvement with pulsing, reduction in leakage floor and EOT scaling.

Figure 3-5 (c) shows the transfer characteristics of the TFET measured at V_{DS}=0.5V and for various gate voltage pulsing time: no gate pulsing (DC), 1µs gate pulse, 500ns gate pulse, and 100 ns gate pulse. With 100ns gate voltage pulsing, significant steepening in the transfer characteristics was observed. Figure 3-5 (d) shows SS as a function of drain current. Minimum SS of 400mV/decade was achieved with 100ns gate voltage pulsing in comparison to SS of 600 mV/decade obtained under DC biasing conditions. High SS even with 100ns gate pulsing arises from the high leakage floor at T=300K. Reducing the measurement temperature to T=77K further reduced the SS. Using TCAD models calibrated against the measured data, ideal simulation of the bulk TFET structure was performed with an EOT of 2nm. Minimum SS of close to 60mV/decade was achieved. With ultra-thin body (UTB) dimension and scaled EOT of 0.8nm, sub-60mV/decade can be achieved over a range of two orders of magnitude of drain current.

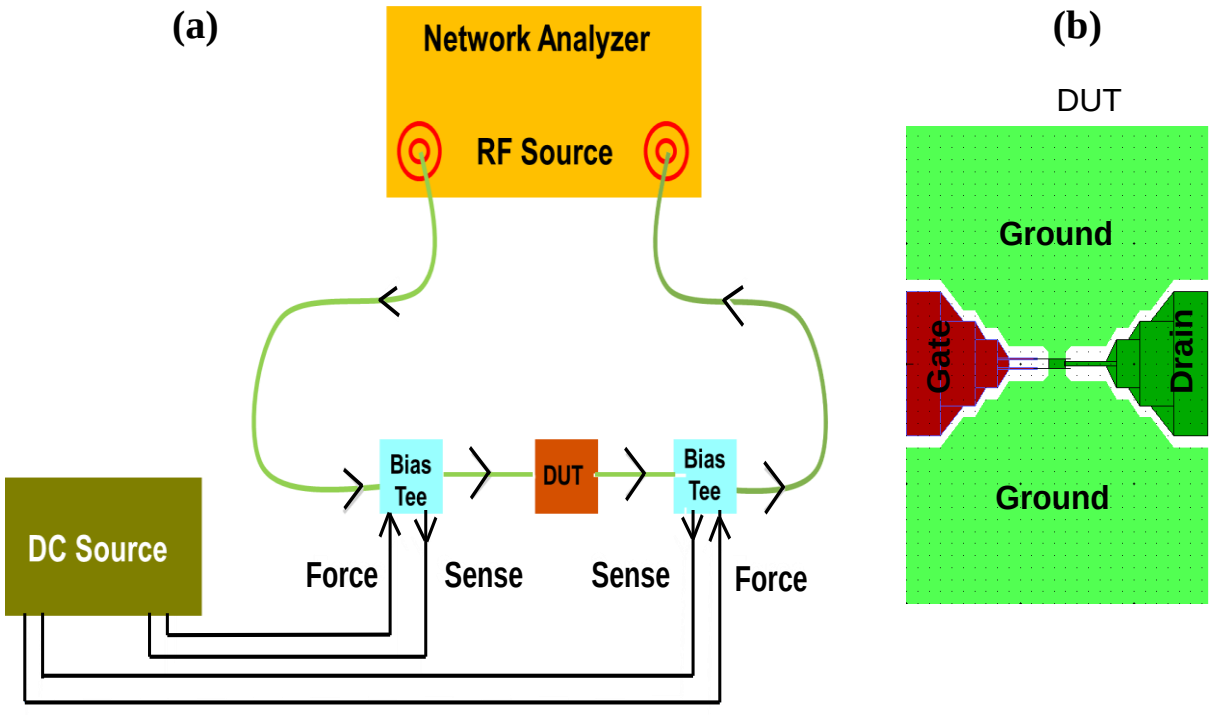

Figure 3-6. (a) Schematic of the experimental setup for RF measurements. (b) Schematic of the co-planar waveguide structure used to incorporate 50 ohm termination in the device for the RF measurements.

Figure 3-6 (a) shows the schematic of the experimental setup used for RF measurements. The network analyzer sends in the RF input signals to the gate terminal and collects the RF output signal from the drain terminal. The input and output ports of the device under test (DUT) need to be terminated with 50 ohms impedance. This is to make sure that the high frequency signal does not get attenuated before reaching the input port or the receiving port of the network analyzer. Coplanar ground-signal-ground waveguide structure is an easy way to incorporate 50 ohms termination in the DUT. However, the fabricated NBTFET had the gate and source contacts at the bottom and drain contact on the top, isolated by the interlayer dielectric (ILD). Hence, a planarization scheme was required which would allow for incorporation of a coplanar ground-signal-ground waveguide structure in vertical TFET.

Figure 3-7 shows the schematic of the process flow developed for the incorporation of co-planar waveguide structure in the vertical NBTFET. The process flow begins with blanket deposition of 20nm of aluminum on the fabricated vertical NBTFET using electron-beam evaporation process. Next, via patterns were created on the top of the aluminum layer using electron-beam lithography technique. Aluminum from the regions where via patterns were created was then etched off using BCl_3/Ar based dry etch plasma. The sample was then exposed to oxygen based plasma during which dry etch of the interlayer dielectric took place. Aluminum being resistant to the oxygen plasma based dry etch protected the interlayer dielectric in all areas except the VIA. It should also be noted that the etched via developed significant sidewall. Hence, electron-beam evaporation of metal would result in a conformal coating along the sidewall ensuring continuity between pads in the top and bottom planes Otherwise, electroplating technique would have required to fill the VIA which was roughly 1µm deep. Next, the sample was exposed to BCl_3/Ar plasma during which aluminum was removed by the dry etch process. Ground-signal-ground pads were then defined using electron-beam lithography and the metal stack comprising of Ti/Pd/Au deposited using electron-beam evaporation technique.

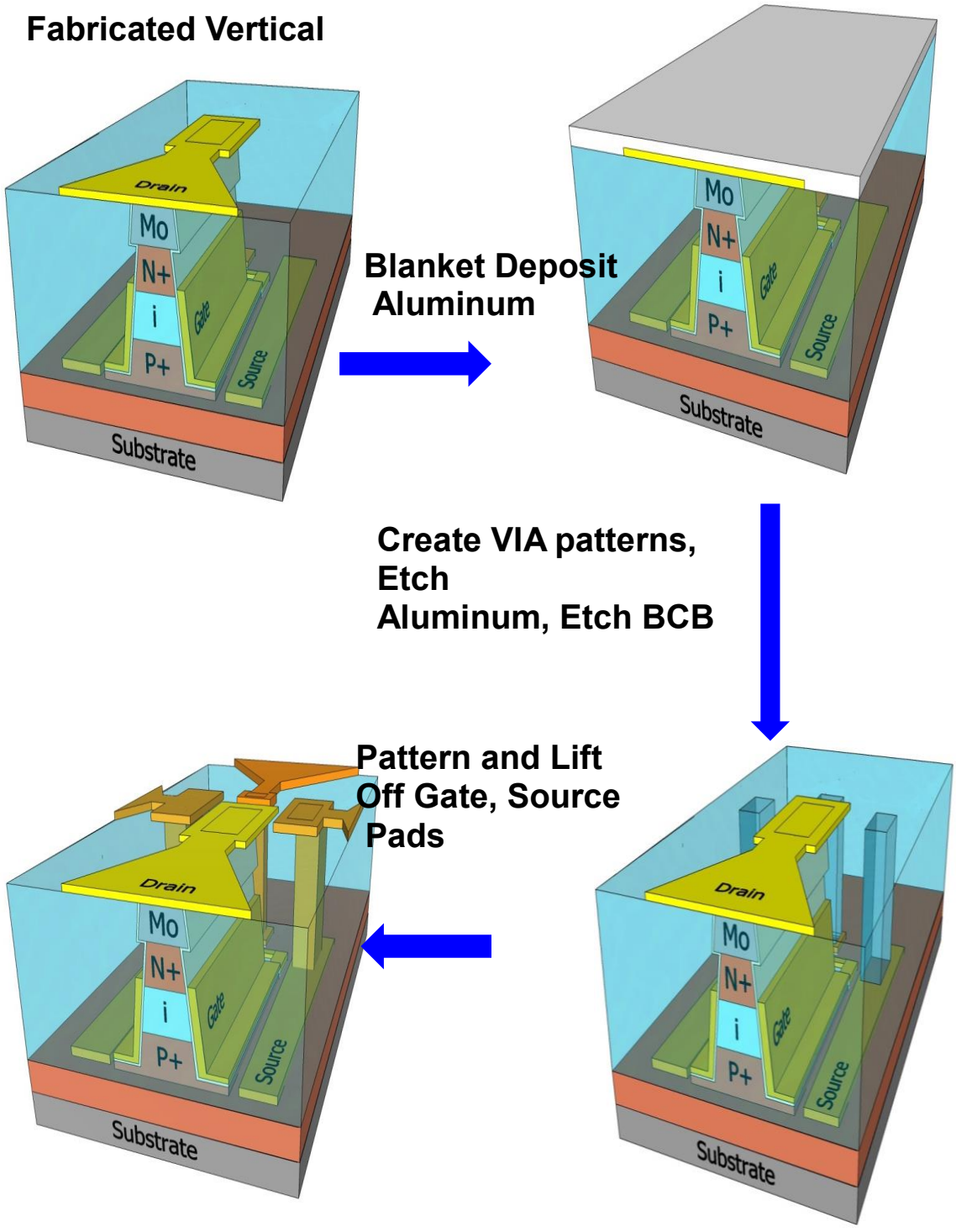

Figure 3-7. Schematic showing the process flow developed to incorporate ground-signal-ground waveguide structure in the vertical TFET.

Figure 3-8 (a) shows the top view false colored SEM image of the fabricated NBTFET. Figure 3-8 (b-c) shows the measured and modeled S-parameters in the frequency range from 40MHz to 20GHz for V_{DS}=0.3V and 0.5V respectively. The gate voltage was set such that G_M is at its maximum value. The measured and modeled values are in excellent agreement with each other.

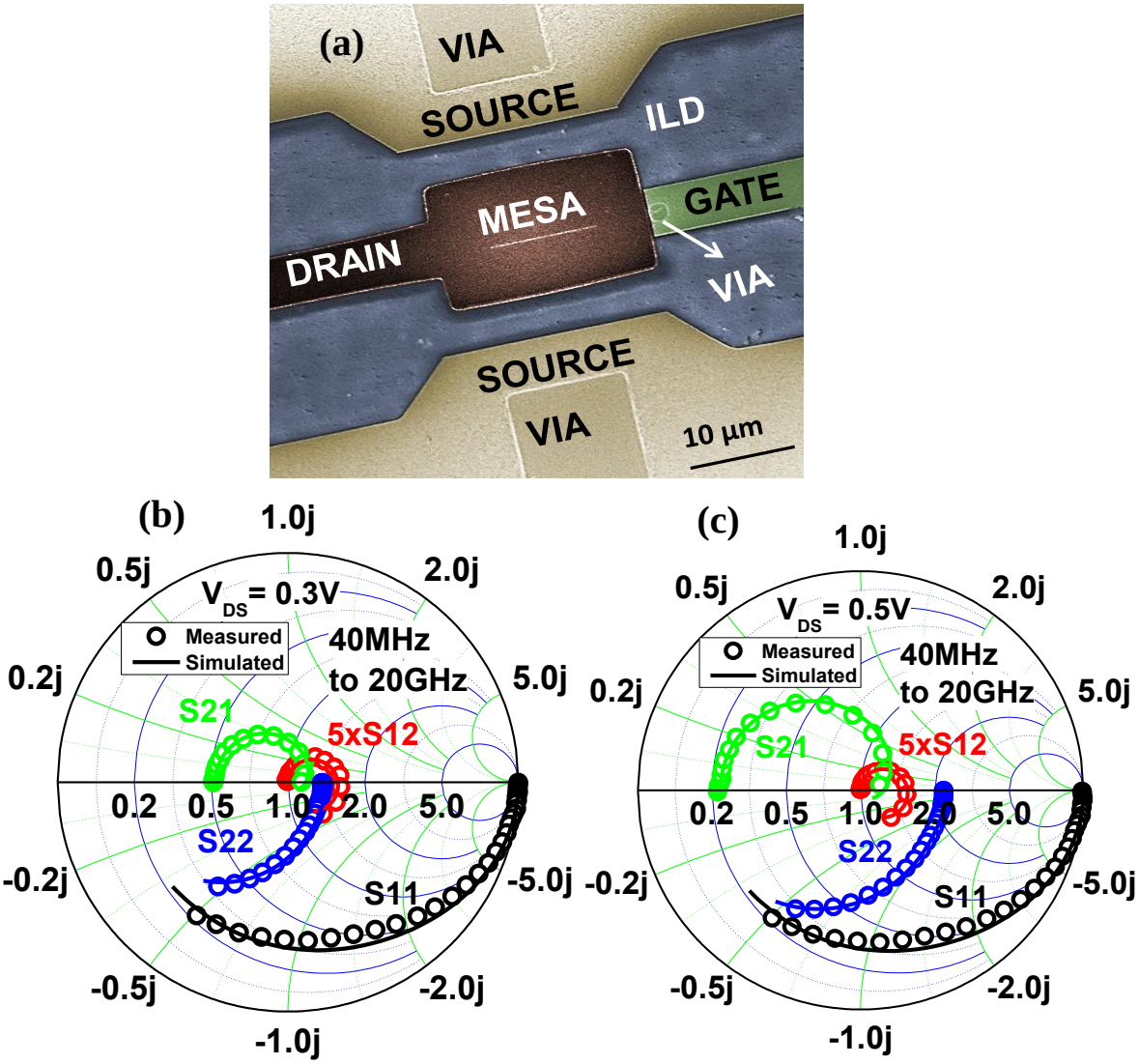

Figure 3-8. (a) Top view SEM image of the fabricated NBTFET. (b) Measured and modeled s-parameters for the frequency range 40MHz to 20GHz at V_{DS}=0.3V (c) Measured and modeled s-parameters for the frequency range 40MHz to 20GHz at V_{DS}= 0.5V.

Figure 3-9 (a-b) shows the equivalent circuit model of the NBTFET before and after de-embedding process. De-embedding allowed for removal of the parasitic pad capacitances between gate and source, gate and drain, drain and source (denoted by C_{pgs},C_{pgd} and C_{pds} respectively). However, the parasitic capacitances such as the gate-source overlap along the sidewall, gate-source overlap in the lateral direction could not be de-embedded.

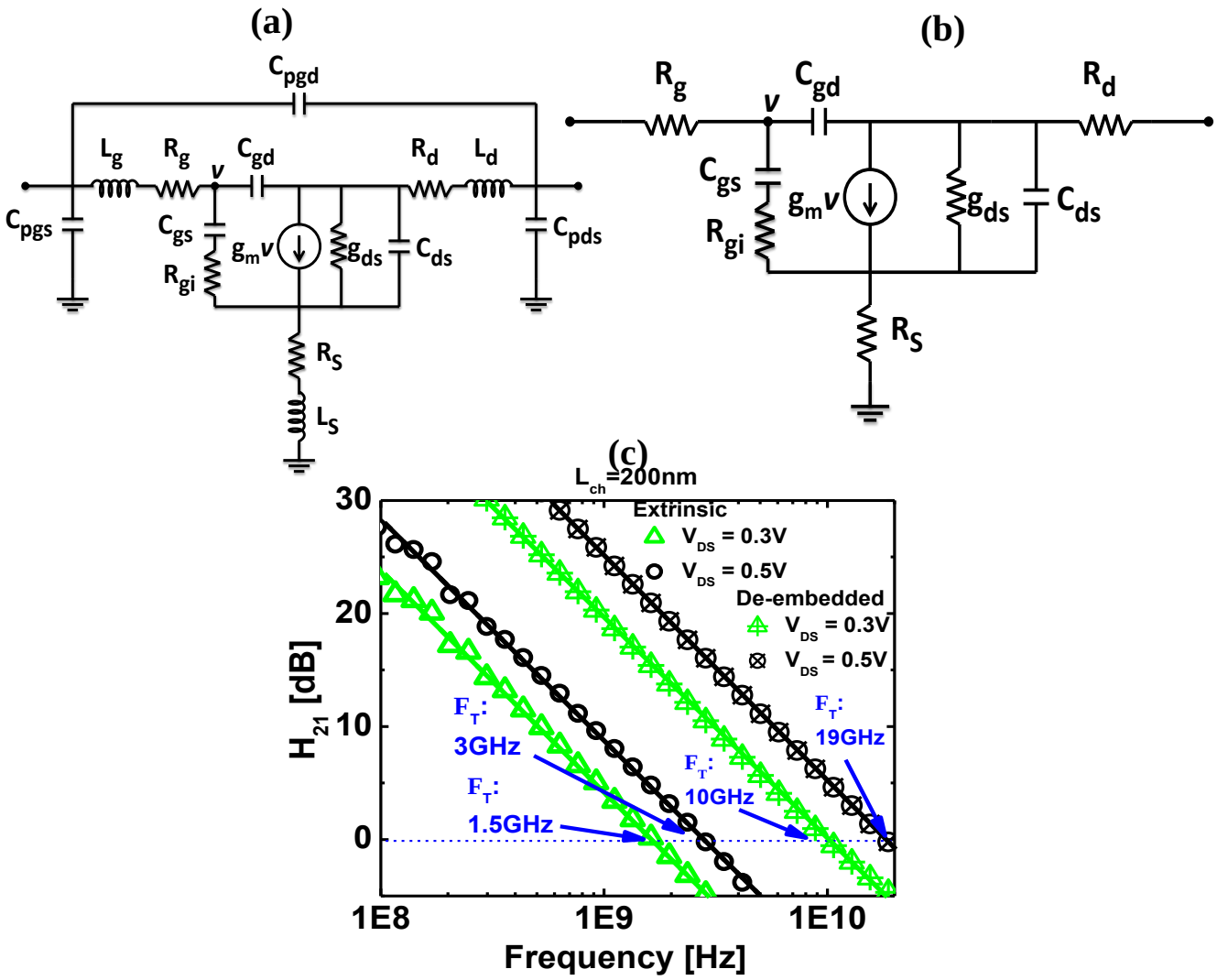

Figure 3-9 (a) Equivalent circuit model of the NBTFET without de-embedding (b) Equivalent circuit model of the NBTFET after de-embedding (c) Measured and modeled H_{21} parameter at V_{DS}=0.5V and 0.3V. After de-embedding, F_T of 10GHz and 19GHz are measured at V_{DS}=0.3V and 0.5V respectively. RF G_M=700μS/μm is measured at V_{DS}=0.5V.

Figure 3-9 (a) shows the measured and modeled H_{21} parameter from which the cut-off frequency (F_T) can be extracted. NBTFET exhibited extrinsic F_T of 1.5Ghz and 3Ghz at V_{DS}=0.3V and 0.5V respectively. F_T after de-embedding increased to 10Ghz and 19Ghz respectively at V_{DS}=0.3V and 0.5V respectively.

To further probe the intrinsic switching characteristics of the NBTFET, numerical simulations were carried out. Figure 3-10 (a) shows the false colored cross-section TEM of the NBTFET. Figure 3-10 (b) shows the schematic of the structure considered for simulations to replicate the cross-section TEM. Figure 3-10 (c) illustrates the parasitic capacitances and resistances in the simulated structure.

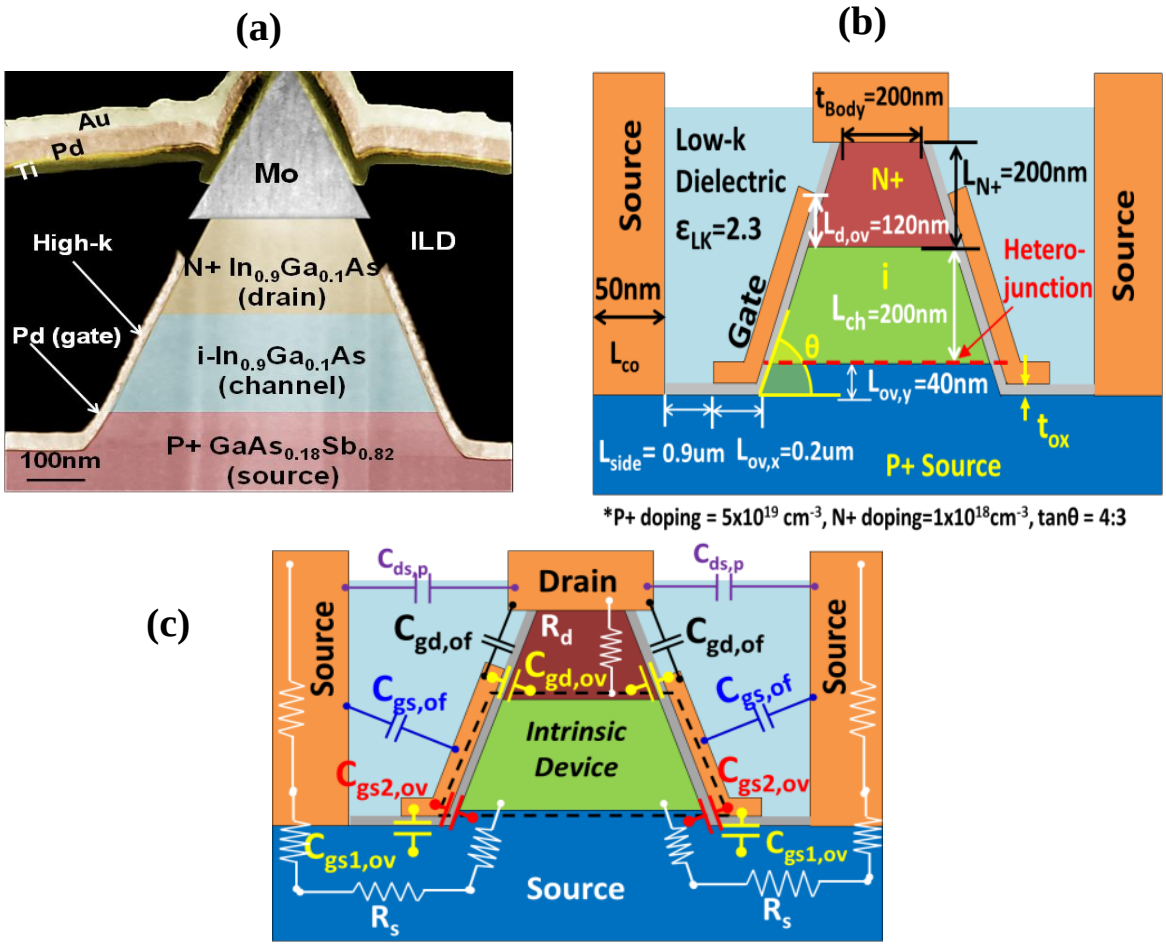

Figure 3-10. (a) False colored cross-section TEM image of the NBTFET (a) 2D schematic of the NBTFET used to perform numerical simulation. The geometric parameters were obtained from the TEM (b) Illustration of the parasitic resistances and capacitances in the NBTFET.

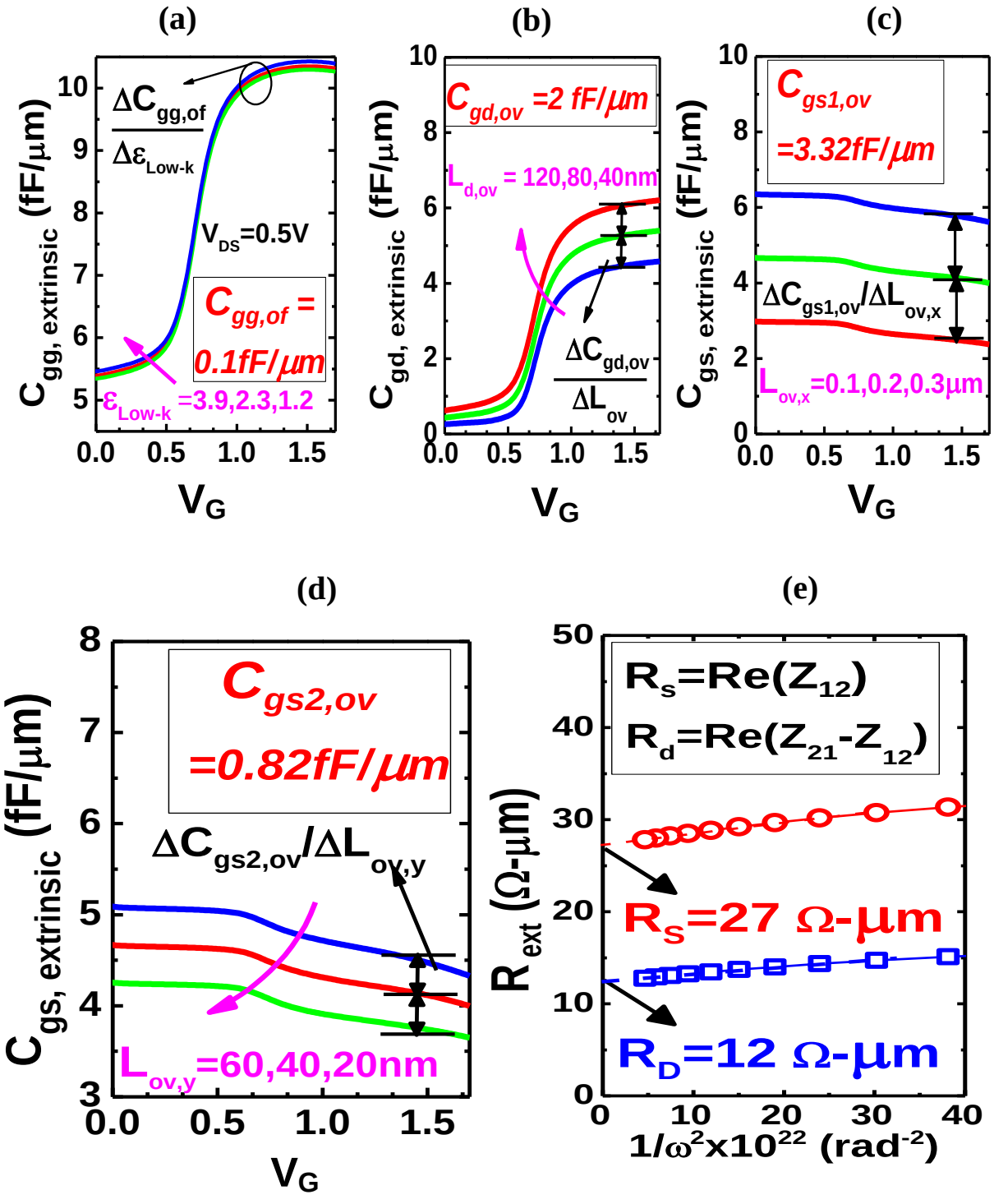

Figure 3-11. (a) Extraction of total fringe capacitance $C_{gg,of}$ by varying the dielectric constant of ILD. (b) Extraction of gate-drain overlap capacitance $C_{gd,ov}$ by varying the gate-drain overlap (c-d) Extraction of gate-source overlap capacitance $C_{gs1,ov}$ and $C_{gs2,ov}$ by varying the gate-source overlap (e) Extraction of the series resistances R_S and R_d by the Z parameter analysis method.

Parasitic capacitances comprised of fringing capacitances ($C_{ds,p}$,$C_{gd,of}$,$C_{gs,of}$) and overlap capacitances ($C_{gs1,ov}$,$C_{gs2,ov}$,$C_{gd,ov}$). The series resistances comprised of the source side series resistance R_s and the drain side series resistance R_d. Parasitic capacitances and resistances were extracted using the approach described in ref [29]. To extract the fringe capacitance, the dielectric constant of the ILD was varied. Fringe capacitance was then extracted as the ratio of change in extrinsic gate capacitance to the change in the dielectric constant of ILD. Similarly, gate-drain and gate-source overlap capacitances were extracted by varying the gate-source and gate-drain overlaps respectively. R_s and R_d were extracted using the Z parameter analysis method described in ref [29].

Figure 3-11 (a) shows the percentage contribution of different source of parasitic capacitances in the fabricated NBTFET at V_{DS}=0.3V and 0.5V. Gate-source and gate-drain capacitances dominated the overall parasitic capacitance. Figure 3-11 (b) shows the simulated F_T as a function of gate bias. Simulations matched the measured F_T at V_{DS}=0.3V and 0.5V. After de-embedding the parasitic capacitances, F_T improved to 22GHz and 39GHz at V_{DS}=0.3V and 0.5V respectively.

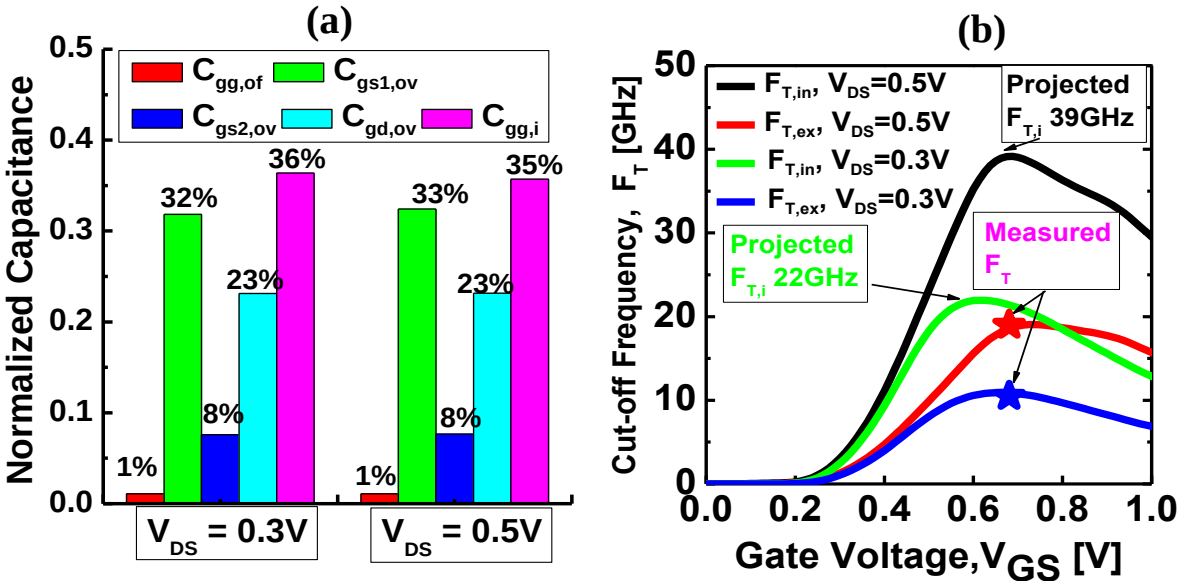

Figure 3-12. (a) Percentage contribution of various capacitance components at V_{DS}=0.3V and 0.5V. (b) Measured FT is in agreement with the simulations.

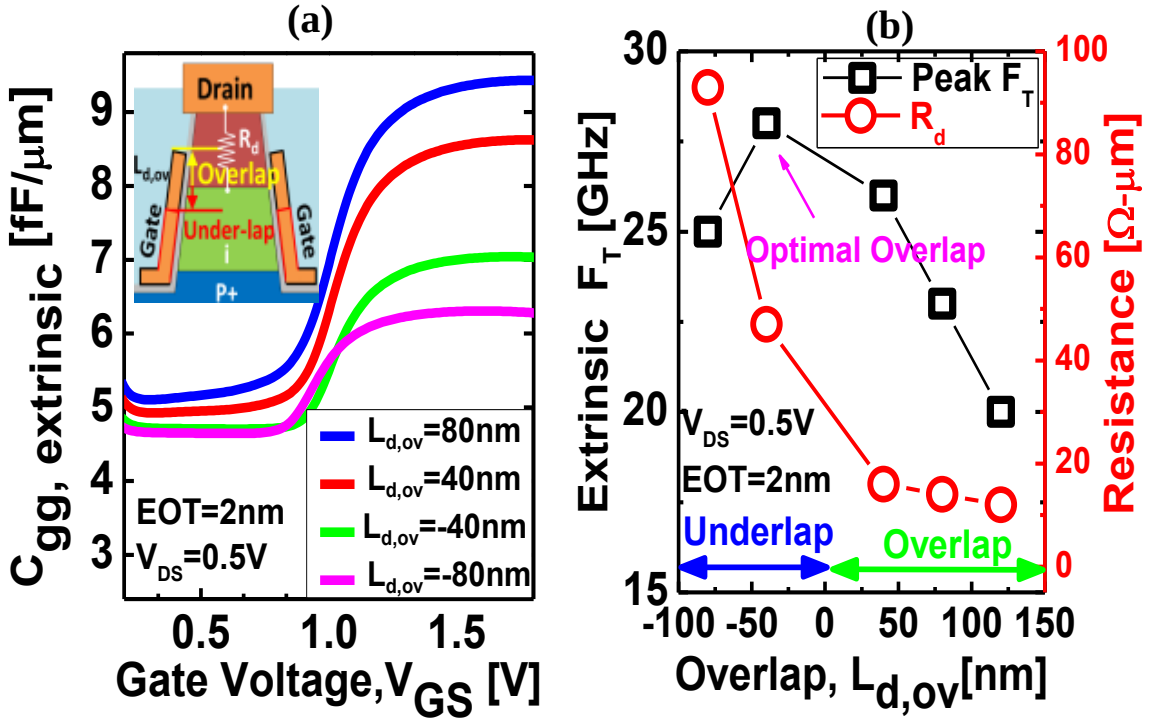

Figure 3-13. (a) Extrinsic gate capacitance, C_{gg} as a function of the gate bias showing increase with increasing gate-drain overlap. Inset shows the schematic of the structure simulated (b) F_T is found to be optimum with a gate-drain underlap of 40nm.

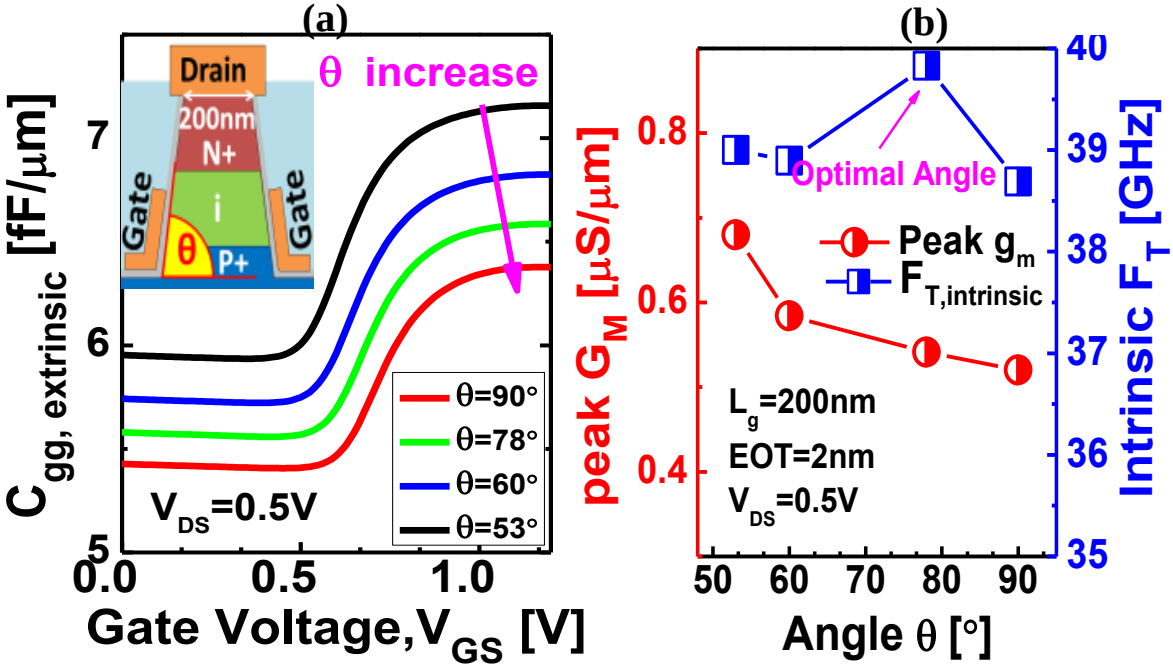

Figure 3-14. (a) C_{gg} as a function of gate bias showing increase in magnitude as the sidewall becomes more tapered. Inset shows the schematic of the structure simulated (b) Peak G_M reduced as the etched sidewall becomes less tapered, F_T is optimum at an angle of 80°.

Simulations were further carried out using the calibrated models to optimize the NBTFET structure which gave maximum F_T performance. Figure 3-12 (a) shows the impact of gate-drain overlap on the extrinsic gate capacitance. As expected, with increased gate-drain overlap, the extrinsic gate capacitance increased. Further, with increase in gate-drain overlap, the drain side series resistance also decreased. F_T was found to be optimum with a gate-drain underlap of about 30nm (Figure 3-12 (b)). The impact of the sidewall angle of the NBTFET on the F_T of the NBTFET was also investigated. As shown in figure 3-13 (a), as the sidewall becomes more vertical, the gate capacitance decreases. Hence F_T is expected to increase as the side wall becomes more vertical. However, it was found that the transconductance reduces as the sidewall becomes more vertical. This is because the spread in the band-to-band generation rate becomes more as side wall becomes more vertical. Thus, F_T was found to be optimum with a nearly vertical sidewall angle (Figure 3-13 (b)). Simulations were performed to compare the RF performance of NBTFET with state of the art CMOS. Figure 3-15 (a) shows the schematic of the NBTFET with scaled device dimensions. The geometric parameters of the NBTFET are listed in Table 3-1. Figure 3-15 (b) shows the simulated extrinsic F_T as a function of I_{DS} and for varying channel lengths. TFET is found to outperform state of the art CMOS by achieving higher F_T at a lower drain current or lower DC power dissipation.

V. Conclusions

Near broken-gap $In_{0.9}Ga_{0.1}As/GaAs_{0.18}Sb_{0.82}$ TFET was demonstrated with record high drive current in the category of TFET. A novel planarization scheme was developed which allowed for experimental demonstration of high frequency switching characteristics of TFET. $In_{0.9}Ga_{0.1}As/GaAs_{0.18}Sb_{0.82}$ TFET exhibited gigahertz F_T at V_{DS} as low as 0.3V. Optimized TFET can outperform CMOS in terms of both DC and RF characteristics with lower DC biasing power.

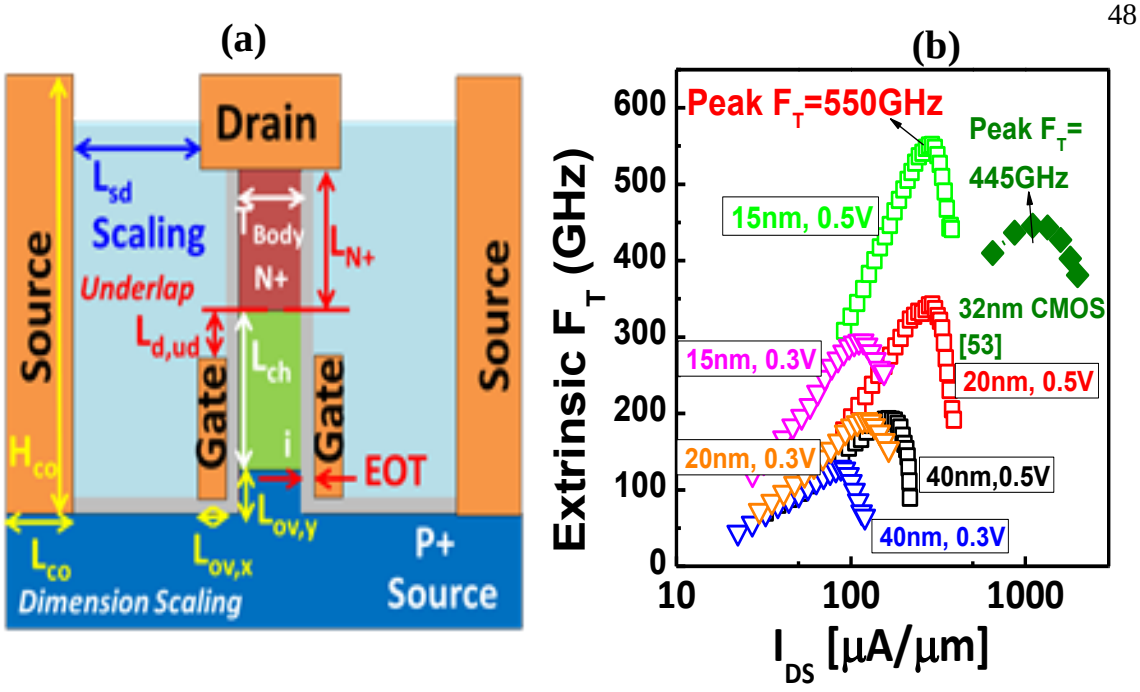

Figure 3-15. (a) Schematic of the optimum NBTFET for RF performance with scaled device dimensions (b) Comparison of the projected extrinsic FT of NBTFET compared to 32nm CMOS.

L_{ch} (nm)	40nm	20nm	15nm
T_{body} (nm)	5	5	5
EOT(nm)	**0.5**	0.5	0.5
L_{sd} (nm)	100	50	30
$L_{d,ud}$ (nm)	20	10	7
$L_{ov,x}$ (nm)	10	5	5
$L_{ov,y}$ (nm)	5	2	1
L_{co} (nm)	20	10	10
L_{N+}(nm)	40	40	30

Table 3-1. Geometric scaling parameters of the NBTFET structure shown in Figure 3-15 (a).

Chapter 4

Impact of Tunnel Barrier Engineering on Flicker Noise Characteristics of TFET-Experiments and Analytical Modeling

I. Introduction

Low frequency noise poses a serious concern for operation of logic circuits as well as memories as the supply voltage is scaled [54][55][56]. In a radar or communication device like a smartphone, the signal's phase noise is largely determined by the flicker noise level in the transistors used [57]. Further, low frequency noise magnitude increases with the reduction in the device dimensions, hence they are of even more concern at the scaled technology nodes [58]. Low frequency noise can also be used as a diagnostic tool for characterizing the interface between high-k dielectric and semiconductor [55]. Low frequency noise in MOSFETs has been studied extensively. In MOSFETs, low frequency noise appears either in the form of random telegraph noise with a 1/frequency^2 dependence or in the form of flicker noise with a 1/frequency dependence, depending on the density of the high-κ/semiconductor interface traps [55]. However, there exists very limited literature on the low frequency noise characteristics of TFET. A recent report states the presence of random telegraph noise in Si based TFET [59] However, flicker noise in III-V TFETs has not been studied yet.

In this chapter, flicker noise in $In_{0.7}Ga_{0.3}As$ homojunction (homoJn) and $In_{0.7}Ga_{0.3}As/GaAs_{0.35}Sb_{0.65}$ heterojunction (heteroJn) III-V TFET is studied. Analysis of the DC characteristics of TFET as a function of temperature is used to identify the dominant transport mechanism. Flicker noise measurements are carried out as a function of temperature. A number fluctuation based model is developed to explain the measured flicker noise characteristics at T=77K where transport is dominated by band to band tunneling alone.

II. Experimental Procedure

Figure 4-1 (a-b) show the layer structure of homoJn and heteroJn TFET respectively. Both structures were grown using solid source molecular beam epitaxy (MBE) on lattice mismatched semi-insulating InP substrate. Linearly graded $In_xAl_{1-x}As$ buffer was used to prevent the defects from extending into the critical regions of the TFET. For the heteroJn TFET, InAs like surface termination was employed while switching from $GaAs_{0.35}Sb_{0.65}$ to $In_{0.7}Ga_{0.3}As$ as explained in chapter 2. Figure 4-1 (c)-(d) show the band diagram of homoJn and heteroJn TFET respectively. HeteroJn TFET exhibits an effective barrier height (E_{Beff}) of 0.25eV in comparison to the homoJn TFET with E_{BEff}=0.58eV (the bandgap of $In_{0.7}Ga_{0.3}As$).

Both homoJn and heteroJn TFETs were fabricated suing the process flow described in chapter 2. Prior to the gate oxide deposition, both the samples were dipped in a 1:10 HCl:DI water solution for 2 minutes for removing the native oxide and then immediately loaded into the atomic layer deposition (ALD) chamber at 250 ^oC. Five cycles of TMA pre-pulsing was carried out followed by deposition of a bi-layer oxide stack comprising of 1nm Al_2O_3 and 3.5nm HfO_2. Palladium gate metal was deposited using electron-beam evaporation technique. Equivalent oxide thickness (EOT) for this gate stack is expected to be 2.3nm. No post-deposition annealing was performed. The DC electrical characterization was performed using an HP 4156A parameter analyzer.

Figure 4-2 shows the experimental setup for flicker noise measurements. DC gate bias was provided by a source measure unit (SMU) connected to a low pass filter of cut off frequency 1Hz. The low pass filter ensured a stable DC bias free of external noise. The drain bias was supplied by a battery operated current pre-amplifier which provided a stable DC bias. The pre-amplifier converted the drain current to a voltage which can then be analyzed. The output voltage

from the pre-amplifier was connected to a digital spectrum analyzer (DSA) which analyzed the different frequency components of the noise in the drain current.

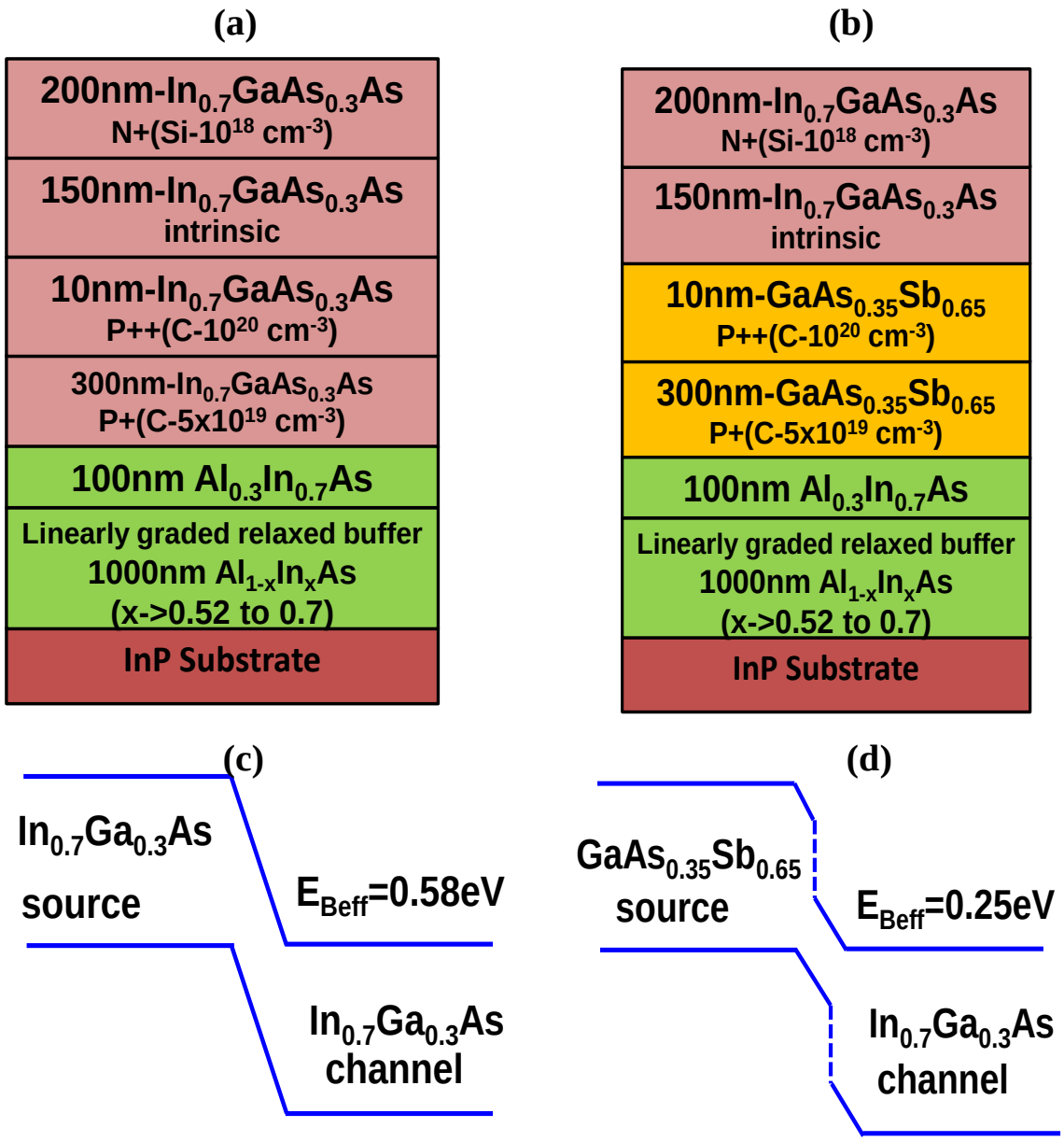

Figure 4-1. (a-b) MBE grown layer structure of homoJn and heteroJn TFET on InP substrate .(c) Energy band diagram effective barrier height of 0.58eV in homojn TFET. (d) Energy band diagram showing effective barrier height of 0.25eV in heteroJn TFET.

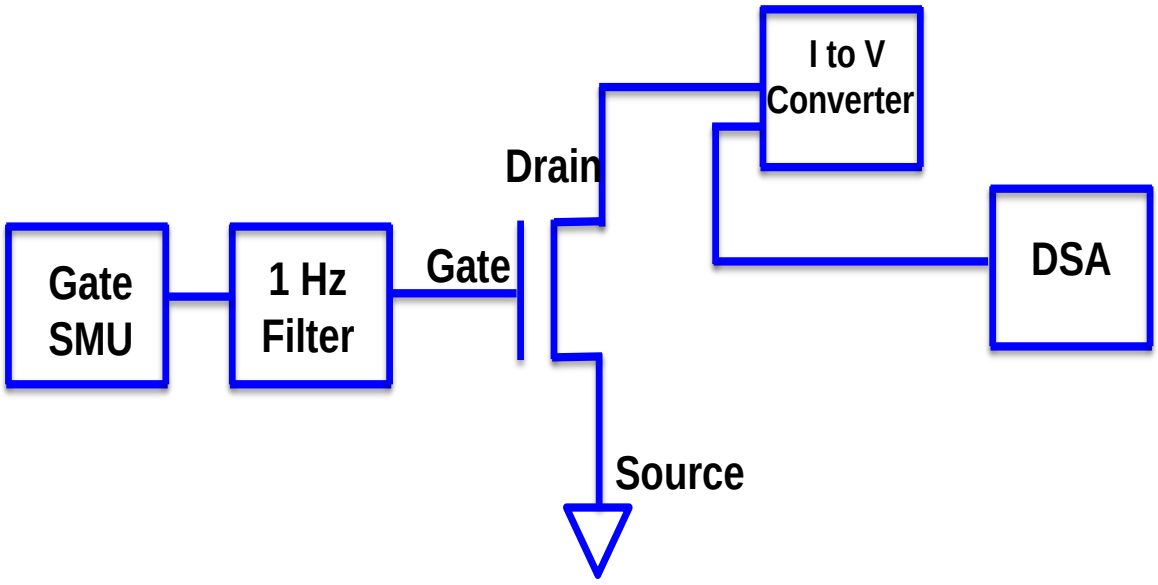

Figure 4-2. Schematic of the experimental setup for flicker noise measurement

III. DC Characterization

Figure 4-3 (a-b) show the transfer characteristics of the homoJn and hetJn TFET respectively at V_{DS}=0.5V and measured at temperatures T=300K, 220K, 150K and 77K. HomoJn TFET exhibited ON state drive current (I_{ON}) of 20 µA/µm at T=300K and V_{DS}=0.5V. HeteroJn TFET on the other hand exhibited I_{ON} of 300 µA/µm at T=300K. The enhanced I_{ON} in heteroJn TFET is due to the lower value of E_{Beff}. In both homoJn and hetJn TFETs, the I_{ON} was to decrease with decreasing temperature. Band to band tunneling current density decreases with reduction in temperature due to increase in bandgap. Hence, the observed trend is indicative of the fact that band to band tunneling is the dominant mechanism of current conduction. If current conduction were dominated by drift-diffusion, then I_{ON} was expected to decrease as the temperature was increased due to the lowering of mobility. Figure 4-3 (c-d) show the switching slope (SS) as a function of drain current of homoJn and heteroJn TFET respectively. HomoJn TFET exhibited a

minimum SS of 180mV/decade at T=300K. In comparison, heteroJn TFET exhibited a minimum SS of 200mV/decade at T=300K.

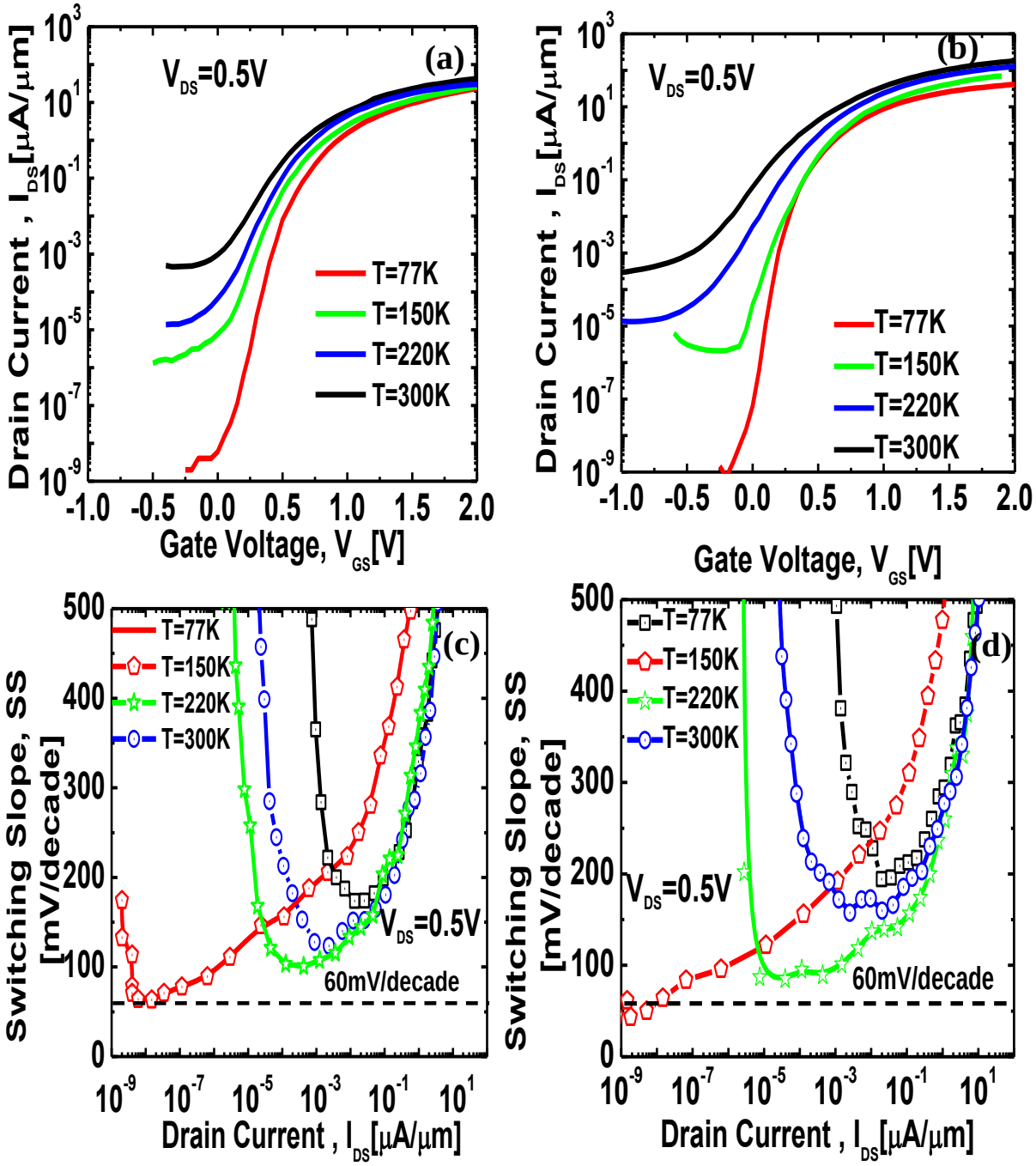

Figure 4-3. (a-b) I_{DS}-V_{GS} characteristics of homoJn and heteroJn TFET respectively measured as function of temperature. (c-d) SS characteristics of homoJn and heteroJn TFET respectively measured as a function of temperature. SS improved at lower temperature due to suppression of TAT.

Trap assisted tunneling followed by thermionic emission (TAT) is known to be the SS degradation mechanism in TFETs [45]. As the measurement temperature was reduced, SS improved due to suppression of TAT. HomoJn TFET exhibited a minimum SS of 60mV/decade and heteroJn TFET exhibited a minimum SS of 40mV/decade at T=77K. TCAD simulations were carried out to model the transfer characteristics at T=77K. A dynamic non-local band-to -band tunneling (BTBT) model [18] was used to calibrate the experimental data at T=77K and TAT models were ignored. Table 4-1 lists the parameters used to calibrate the experimental data. Excellent agreement between measured and modeled characteristics confirms that at , band to band tunneling alone was the mechanism of transport.

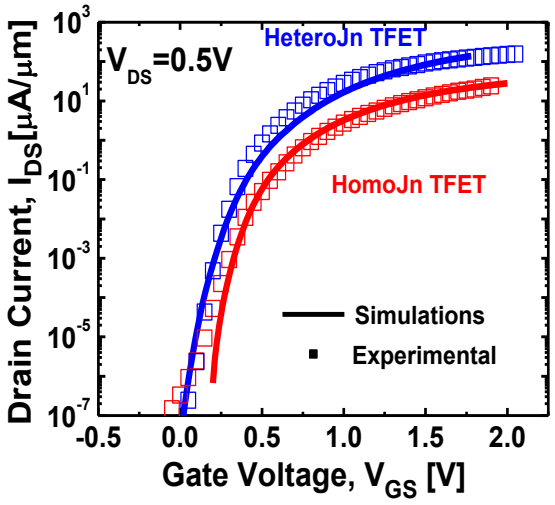

Figure 4-4. TCAD calibration of the experimental data at T=77K.

Parameter	HomoJn TFET	HeteroJn TFET
EOT (nm)	2.3	2.3
Source Doping(cm^{-3})	$5x10^{19}$	$5x10^{19}$
m_r	$0.019m_0$	$0.022m_0$
E_{Beff} (eV)	0.64	0.31

Table 4-1. Simulation parameters used to model the measured transfer characteristics at 77K.

IV. Flicker Noise Characterization and Modeling

Figure 4-5 shows the low frequency noise characteristics of homoJn and heteroJn TFET normalized to the square of the drain current. The measurements were carried out at T=300K and 77K and at a gate bias corresponding to drain current of 2μA/μm, V_{DS}=0.5V. The measured noise spectrum follows the 1/frequency trend at T=300K and T=77K indicating the presence of distribution of traps into the oxide. Recently reported noise measurements on Si TFET showed 1/frequency^2 spectrum possibly due to better quality of the SiO_2/Si interface. Figure 4-6 (a) shows the drain current normalized noise spectrum of homoJn and heteroJn TFET measured at T=300K and V_{DS}=0.5V and plotted as a function of the drain current. The noise magnitude of homoJn and heteroJn was comparable at T=300K where both band to band tunneling and TAT dominated the carrier transport. Figure 4-6 (b) shows the drain current normalized noise spectrum of homoJn and heteroJn TFET measured at T=77K and V_{DS}=0.5V. Due to reduction in the temperature, noise magnitude dropped down by roughly an order of magnitude compared to T=300K. Further, heteroJn TFET exhibited lower noise magnitude than homoJn TFET at T=77K where band to band tunneling was the mechanism of carrier transport.

There exists three schools of thought as far as the origin of flicker noise in MOSFET is concerned: (1) Number fluctuation model where flicker noise is assumed to be due to random trapping and de-trapping of carriers in the channel resulting in fluctuation in the drain current [60]. (2) Mobility fluctuation model where the mobility of the carriers fluctuates due to scattering by phonons leading to fluctuation in the drain current [61]. (3) Unified model where the drain current fluctuation is a combined effect of both number fluctuation and mobility fluctuation [62]. With proper gate stack engineering, the carrier transport in TFET is expected to be dominated by band-to-band tunneling than trap assisted tunneling at room temperature. Hence flicker noise modeling was performed on the measured data at T=77K. Further, since the carrier transport is

limited by band-to-band tunneling rather than drift-diffusion within the channel, a number fluctuation based model was developed to model the measured characteristics at T=77K.

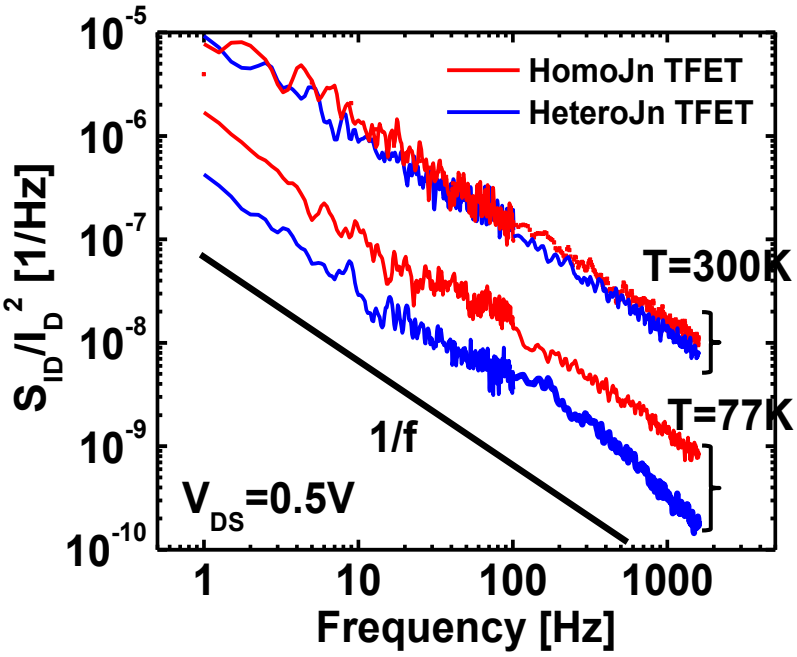

Figure 4-5. Normalized drain current noise spectrum at I_{DS}= 2μA/μm follows 1/f trend.

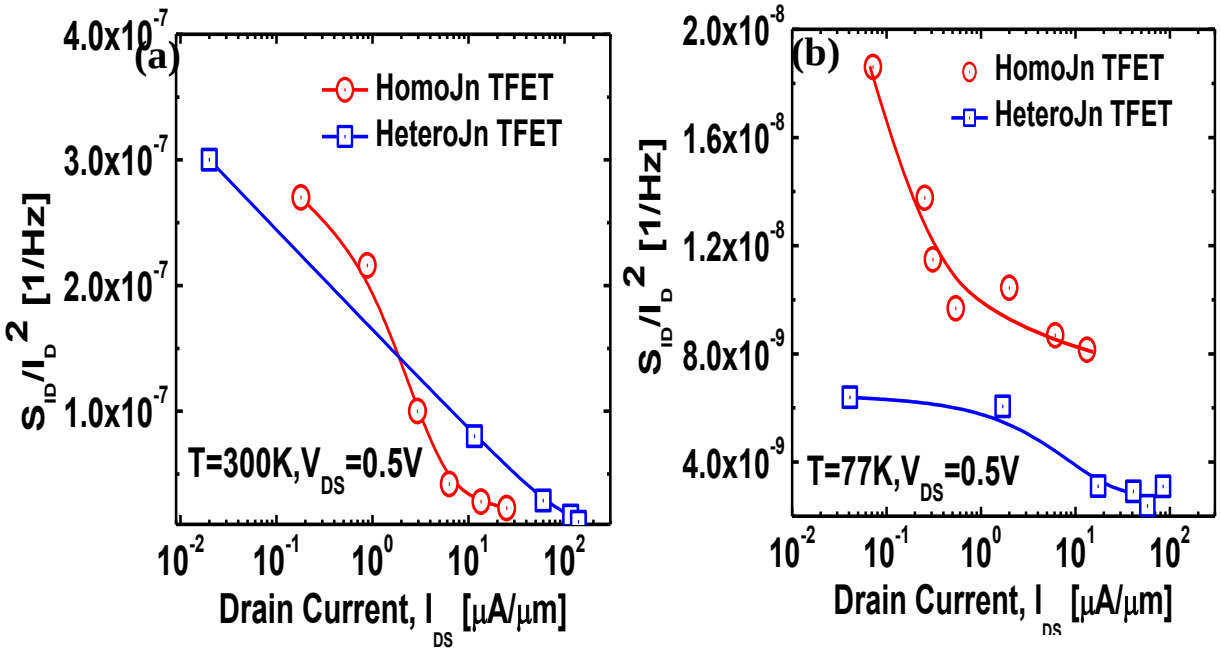

Figure 4-6. (a-b) Normalized drain current noise spectrum as a function of drain current measured at T=300K and T=77K respectively.

The band to band limited current in a TFET is independent of the channel length (assuming no short channel effects exist). Hence, in order to develop a number fluctuation theory, an effective channel length L' needs to be defined. L' was defined as the distance over which the band-to-band generated carriers interact with the traps in the oxide/channel interface. L' is expected to be much shorter than the actual channel length of the TFET and can be determined based on the spread of the band-to-band generated carriers in the channel. Figure 4-7 (a-b) shows the band-to-band generation rate of electrons and holes extracted from the dynamic non-local 2D numerical simulation of the TFETs. For a given drain current, L' was found to be smaller in homoJn TFET in comparison to heteroJn TFET. This is because heteroJn TFET has a lower E_{Beff} and hence requires only a smaller electric field to attain the same drive current as in the case of a homoJn TFET (Figure 4-8 (a-b)). The tunneling current can empirically be written as a function of the electric field F as [18] :

$$I_{BTBT} = AF^2 exp\left(\frac{-B}{F}\right) \tag{4-1}$$

where the parameter A is given by

$$A = \frac{\pi m_r^{0.5} q^2}{9h^2[E_{Beff}^{0.5}]} \tag{4-2}$$

and the parameter B is given by

$$B = \frac{\pi^2 m_r^{0.5} E_{Beff}^{1.5}}{qh} \tag{4-3}$$

Electrons in the effective channel region with energy around the channel electron quasi-fermi level (E_{FN}) get trapped to and de-trapped from the traps in the oxide (at the interface and extending into the oxide) (Figure 4-9). The fluctuation in the trapped charge translates to a fluctuation in the electric field as given by

$$\Delta F = \frac{\Delta Q}{\varepsilon_{ox}} \tag{4-4}$$

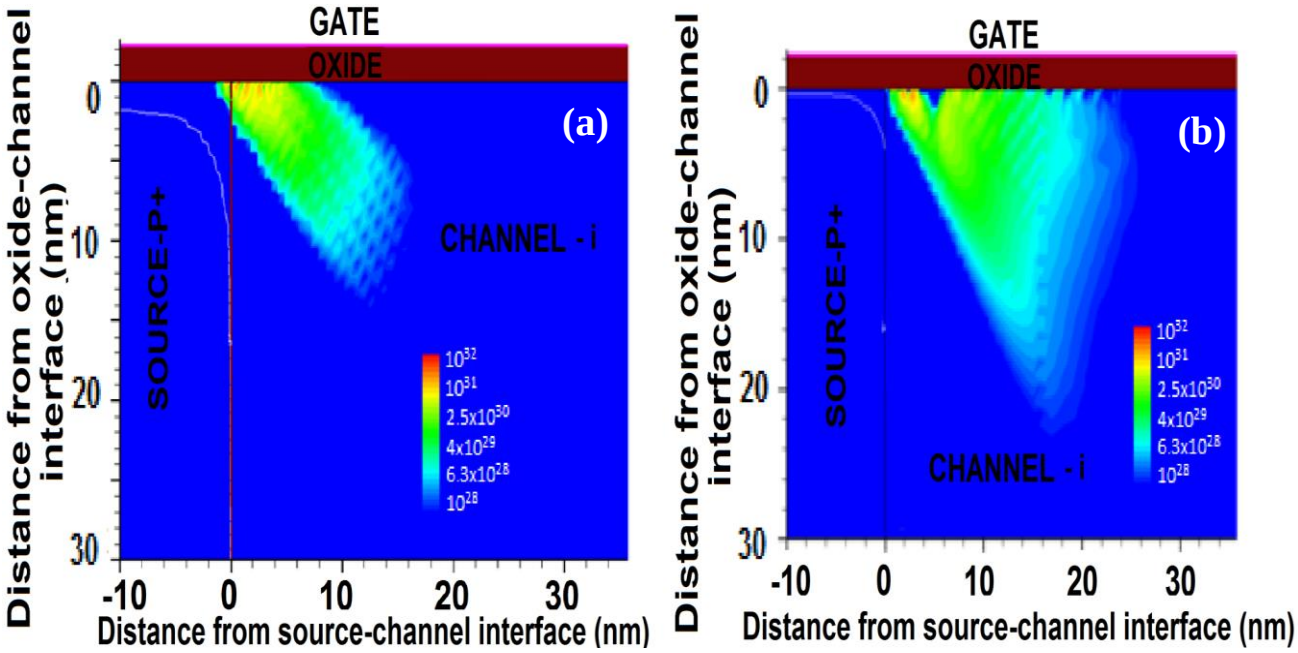

Figure 4-7. (a-b) Contour plot of electron band-to band generation for homoJn and heteroJn TFET respectively.

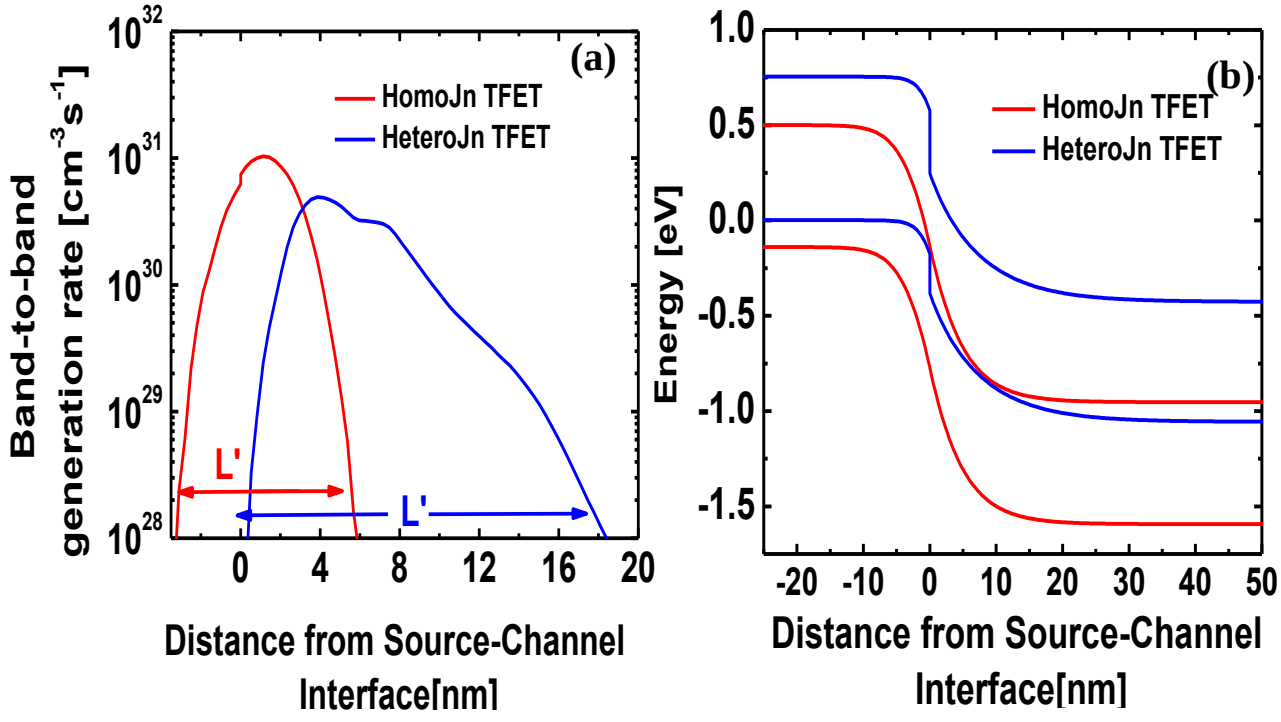

Figure 4-8. (a) Effective channel length L' is defined based on the spread of band-to-band generated electrons. (b) Higher electric field in homoJn TFET compared to heteroJn TFET for a given drain current.

The fluctuation in the electric field leads to a fluctuation in the tunneling current as evident from Equation (4-1). Fluctuations in the trapped charge lead to fluctuation in the junction electric field which, in turn, affects the band-to-band generation rate. Noise spectrum due to the fluctuation of charge due to the trap at a distance 'x' from the oxide-channel interface is given as [62]

$$S_{\Delta Q} = q^2 S_{\Delta Nt} = q^2 \frac{\tau_t}{1+w^2\tau_t^2} N_t f_t(1-f_t) \tag{4-5}$$

where τ_t is the trap time constant given by [62],

$$\tau_t(x) = \tau_0 exp(-\alpha x) \tag{4-6}$$

In the above expression, τ_0 is the time constant of the trap at the oxide-channel interface and the parameter α is given by [62], $\alpha = \frac{4\pi}{h}\sqrt{2m_x^*\phi_B}$ where ϕ_B is the offset between the conduction band of the channel and the oxide. The noise spectrum after integrating contribution of the traps extending into the oxide is given as:

$$\frac{S_{I_{ds}}}{{I_{ds}}^2} = \left(\frac{2}{F} + \frac{B}{F^2}\right)^2 \frac{q^2 N_t(E_{fn})}{\varepsilon_{ox}^2 WL'\alpha f} \tag{4-7}$$

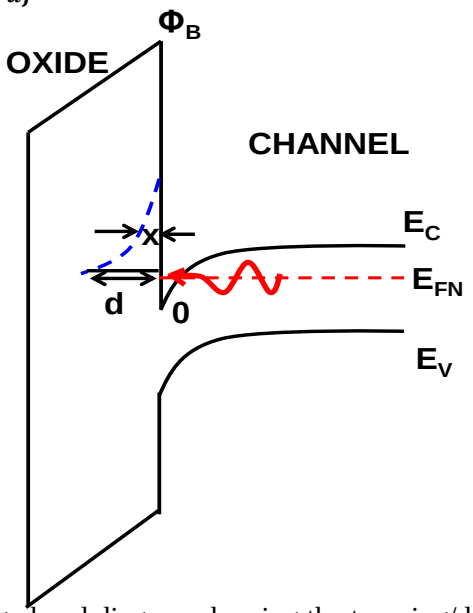

Figure 4-9. Schematic energy band diagram showing the trapping/de-trapping of electrons around E_{FN} into the trap states in the oxide.

It should be noted that spectrum of relative fluctuation due to discrete trap varies as $\mathbf{1/L'^2}$. However, after summing up the response from traps over region L', the overall noise spectrum shows a $1/\boldsymbol{L'}$ dependence. For hetJn TFET, at a given drain current, though the electric field is smaller, smaller value of B parameter and larger $\boldsymbol{L'}$ results in lower flicker noise level. Figure 4-10 shows the modeled noise data at T=77K using equation. N_{it} of $1x10^{13}$ cm^{-2} was assumed to model the experimental data. The model gives a good match with experimental data.

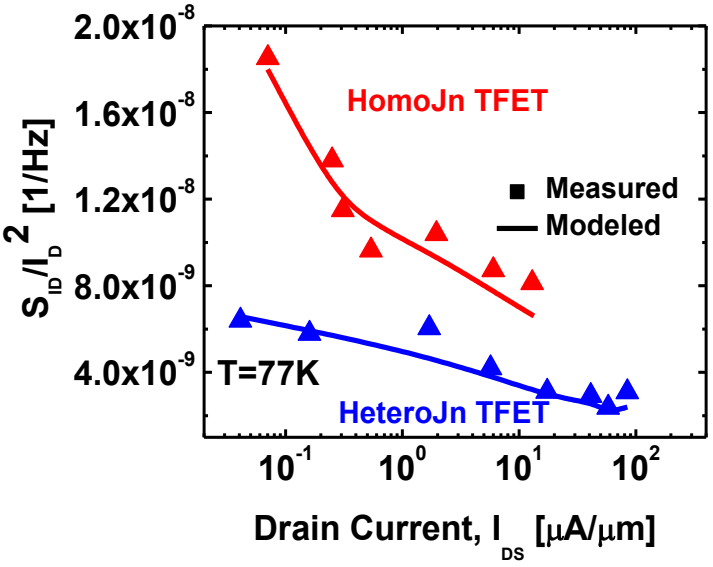

Figure 4-10. Analytical model is in excellent agreement with the experimental data.

V. Conclusions

Low frequency noise measurements were performed in $In_{0.7}Ga_{0.3}As$ homojunction and $In_{0.7}Ga_{0.3}As/GaAs_{0.35}Sb_{0.65}$ heterojunction TFET at T=300K and T=77K. At T=300K where both BTBT and TAT dominated, homojunction and heterojunction TFETs exhibited comparable noise magnitues. At T=77K where BTBT dominated, heterojunction TFET exhibited lower noise magnitude. Using numerical simulations calibrated to measured data, analytical model was developed to explain the measured noise characteristics. Lower noise in heterojunction TFET is promising for RF applications.

Chapter 5

Low Temperature Atomic Layer Deposited High-k Dielectric for p-channel Tunneling Field-Effect Transistor

I. Introduction

Realizing energy-efficient complementary logic circuits requires the development of a high- performance p-channel TFET (pTFET) within the same material system as the n-channel counterpart. A major challenge for demonstration of pTFET is the integration of the gate stack with acceptably low values of interface state density across the bandgap. Recent efforts have focused on the upper part of the bandgap and the quality of high-κ/ III-As compound semiconductor interfaces has been considerably improved by employing surface passivation schemes, such as $(NH_4)_2S$ or NH_4OH solution [63], in-situ As de-capping [64], surface cleaning, and native oxide removal using hydrogen or nitrogen plasma [65][47]. A few studies have reported on the integration of high-κ dielectrics with an antimonide such as GaSb with focus on the lower part of the bandgap between the midgap and the valence band [66][67][68][69][70][71], whereas mixed arsenide/antimonides have not been addressed.

In this chapter, the effect of the temperature used in the atomic layer deposition process (ALD) on the quality of a high-κ/$GaAs_{0.35}Sb_{0.65}$ interface is investigated. It is shown that reducing the deposition temperature from 250 to 110°C results in improved charge modulation of the semiconductor and a reduced interface trap density (D_{it}) response in a metal oxide semiconductor capacitor (MOSCAP), as determined by the Terman method. Furthermore, $GaAs_{0.35}Sb_{0.65}/In_{0.7}Ga_{0.3}As$ hetero-junction pTFET devices with gate stacks deposited at a low temperature shows an improved I_{ON}/I_{OFF} ratio and switching slope performance.

II. Experimental Procedure

Epitaxial $GaAs_{0.35}Sb_{0.65}$ layers were grown on a lattice-mismatched InP substrate employing a linearly graded $Al_{1-x}In_xAs$ metamorphic buffer layer grown using solid-source molecular beam epitaxy (MBE). The doping concentration of $GaAs_{0.35}Sb_{0.65}$ is $1x10^{16}$ cm^{-3}. For MOSCAP fabrication, samples were degreased in acetone and methanol for 5min each and rinsed in isopropyl alcohol (IPA), followed by a dipping in concentrated HCl solution ($HCl:H_2O$ = 1:1) for 5 min and an IPA rinse. The samples were then immediately loaded into the ALD chamber and 10 cycles of Al_2O_3 were deposited followed by 35 cycles of HfO_2 at deposition temperatures (T_{dep}) of 250°C (sample A) and 110°C (sample B). Pd/Au gate and substrate contact metallization was carried out using electron-beam evaporation after defining gate patterns by electron-beam lithography (Figure 5-1(a)). No post-deposition annealing was performed. Capacitance-voltage (CV) and conductance-voltage (GV) measurements were obtained using a HP 4285A precision LCR meter. X-ray photoelectron spectroscopy (XPS) measurements were carried out using a monochromatic Al K_α X-ray source with a photon energy of 1486.7eV coupled with a seven-channel hemispherical analyzer operated at a pass energy of 15 eV, with all scans taken at an angle of 45° with respect to the sample normal. AANALYZER software was used to de-convolute the XPS peaks [72]. For XPS measurements, ALD oxide thicknesses were kept at 1 nm for Al_2O_3 and 1.4 nm for HfO_2 for the two deposition temperatures of 250°C (sample A) and 110°C (sample B). A heterojunction TFET layer was grown by MBE on a linearly graded $Al_xIn_{1-x}As$ metamorphic buffer to accommodate lattice mismatch to the InP substrate as shown in Figure 5-1 (b). A self-aligned gate nanopillar process flow was applied for the fabrication of vertical TFETs, as detailed in chapter 2. Figure 5-1 (c-d) show the schematic and a false-colored cross-section scanning electron micrograph (SEM) image of the fabricated pTFET. For the gate dielectric deposition, high (250°C, sample A) and low ALD temperatures (110°C, sample B)

were employed, followed by the self-aligned gate metal deposition process to deposit Pd. The electrical characterization of pTFETs was performed using an HP 4156A parameter analyzer.

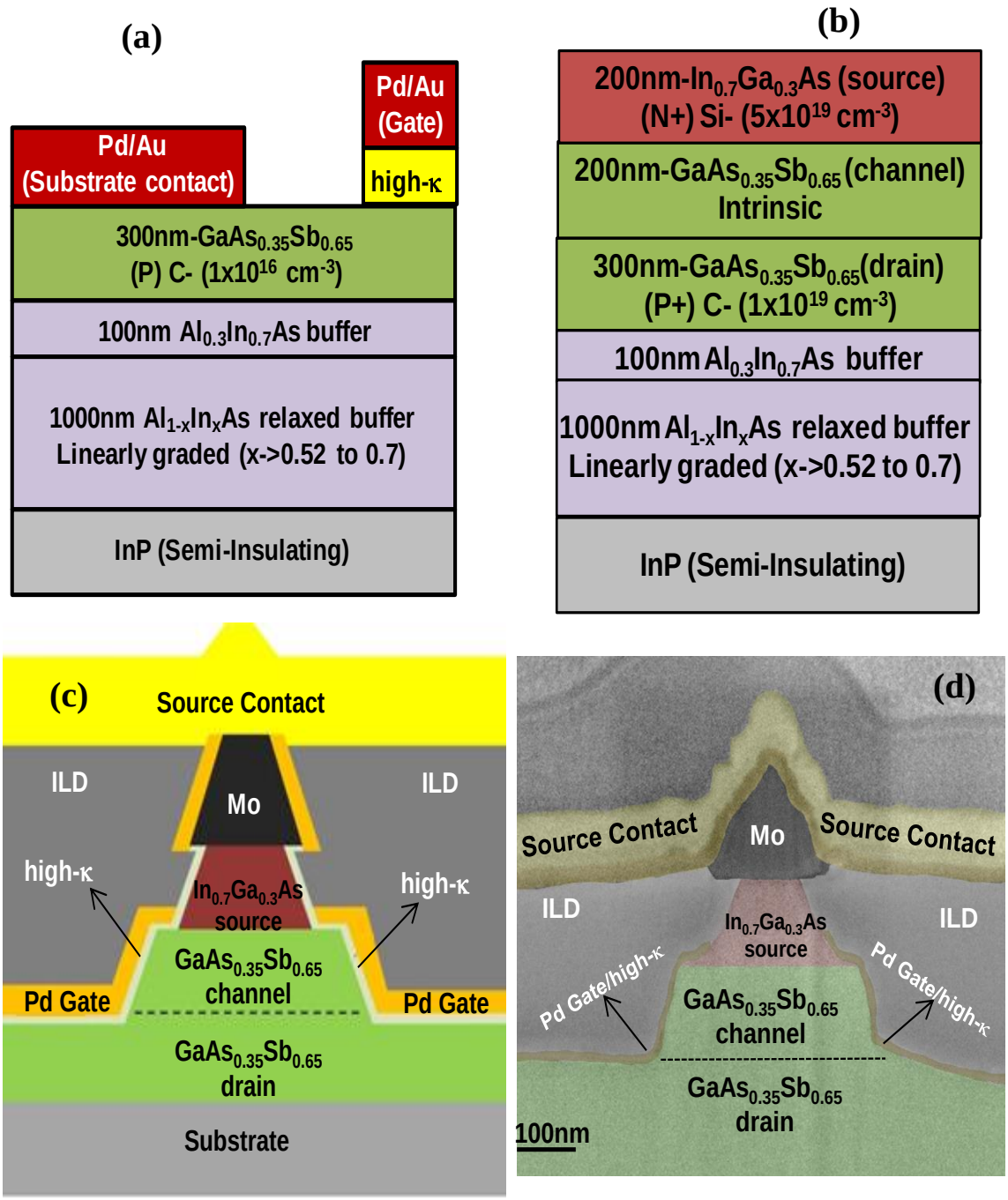

Figure 5-1. (a) Schematic of MOSCAP structure. (b) Schematic of MBE-grown pTFET layer structure. (c) Schematic of fabricated pTFET using inter-layer dielectric (ILD) to isolate the source and gate contacts. (d) False-colored cross -section SEM of the fabricated pTFET.

III. Results and Discussions

Figure 5-2 (a-b) show the CV measurements for MOSCAP samples A and B respectively. Sample A showed only a small capacitance modulation with a gate bias at 300 K, indicating strong Fermi level pinning. Despite the strong frequency dispersion at negative gate bias, the CV characteristics at 150K are more well-behaved with a smaller minimum capacitance of C_{min}=9.5x10^{-8} F/cm^2 suggesting larger band bending. However, an ideal minimum capacitance of 3.9x10^{-8} F/cm^2 was calculated, thus the semiconductor was not fully depleted. The enhanced capacitance modulation at 150K is attributed to two effects: 1) the lower temperature suppresses the D_{it} response and increases the Fermi level movement efficiency; 2) the reduced exponential tail of the electron distribution results in more pronounced carrier modulation and thus enhanced capacitance modulation for a fixed band bending. In contrast, the samples with high-κ deposition at the lower temperatures(sample B) showed much improved CV characteristics, achieving a much smaller minimum capacitance compared to sample A. The CV curves are stretched out and have considerable frequency dispersion indicating a high D_{it}. Figure 2-2 (c-d) show CV characteristics of two additional MOSCAP samples with high-κ dielectrics deposited at 80 and at 150°C, respectively. Higher frequency dispersion and a drop in the capacitance value for a high gate bias due to high gate leakage are observed for the sample with ALD at 80 °C. This is due to the poor quality of the deposited film at the lower deposition temperature. Furthermore, higher stretch-out in the CV curve is observed in the 150°C ALD sample in comparison with the 110 °C ALD sample. A deposition temperature of 110°C was thus found to be optimum. Thus samples A and B represent a compromise between improved interface quality and reduced dielectric quality, such as gate leakage current and dielectric permittivity. Hence, further analysis (D_{it} extraction, pTFET fabrication, and XPS analysis) is focused on samples A and B. Terman method was applied to quantify the interface trap density D_{it} and band bending

for both the samples at 300K. It is to be noted that the conductance method would severely underestimate the D_{it} response since a D_{it} level larger than $C_{ox}/q \sim 8x10^{12}$ $cm^{-2}eV^{-1}$ is expected in this case [73].

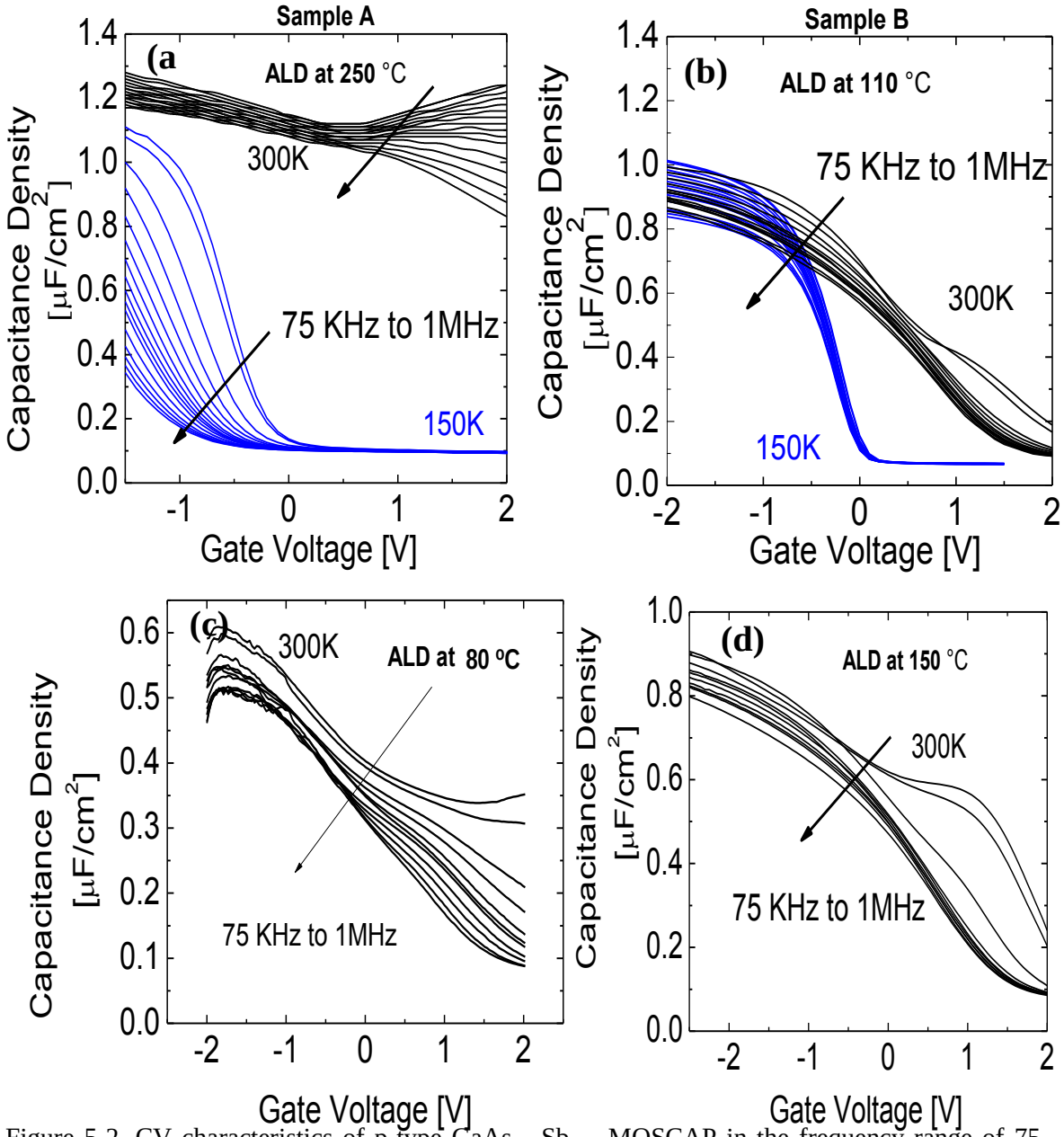

Figure 5-2. CV characteristics of p-type $GaAs_{0.35}Sb_{0.65}$ MOSCAP in the frequency range of 75 KHz to 1 MHz measured at 300 and 150K with Al_2O_3/HfO_2 deposited at (a) 250 °C (sample A) and (b) 110 °C (sample B). C-V characteristics of p-type $GaAs_{0.35}Sb_{0.65}$ MOSCAP in the frequency range of 75 KHz to 1 MHz measured at 300K with Al_2O_3/HfO_2 deposited at (c) 80 °C and (d) 150 °C.

The ideal high frequency CV curve of $GaAs_{0.35}Sb_{0.65}$ was calculated for 300 K with parameters from ref. [52] using the approach published in ref. [44]. Light and heavy holes with masses $m_{lh}=0.06\cdot m_e$ and $m_{hh}=0.29\cdot m_e$ respectively, where m_e is the free electron mass, were taken into account for the valence band. The effect of split-off band population is small at room temperature due to the large energy offset (0.4 eV) and was therefore neglected. The high-frequency CV branch at positive gate bias was calculated from ref. [74]. For a p-type dopant concentration of $1x10^{16}$ cm^{-3}, the flat band condition is met if the Fermi level is 0.17 eV above the valence band edge. Figure 5-3 (a-d) show a comparison between the calculated ideal high frequency and measured 1MHz CV curves as well as the extracted band bending and D_{it}. For the MOSCAPs deposited at 250 and 110°C oxide capacitance densities of 1.4 and 1.1μF/cm^2 were determined, respectively. For the high-κ dielectric film deposited at 250°C a total band bending of around 0.12 eV was achieved. The Fermi level barely moved away from the valence band edge and did not reach the flat band at positive gate bias. Therefore, the flat-band voltage shift could not be determined. High D_{it} levels in the low 10^{14} $cm^{-2}eV^{-1}$ range were extracted (inset in Figure 5-3 (b)). In contrast, for the MOSCAPs with dielectrics deposited at 110°C the total band bending considerably improved (0.31eV) and the flat band condition was reached at a gate bias of 1.1V. The interface trap density was found to be considerably reduced with typical values in the mid to high 10^{13} $cm^{-2}eV^{-1}$ range (inset in Figure 5-3 (d)). The lowest D_{it} value of ~$3\cdot10^{13}cm^{-2}eV^{-1}$ was extracted close to the flat-band condition. The Fermi level moved higher into the bandgap reaching close to the midgap. The D_{it} profile extracted by the Terman method suggests that high interface trap densities are still present close to the midgap and at the valence band edge. The low temperature deposition allowed a reduction of the interface trap density within these bounds.

Figure 5-4 (a) shows the measured transfer characteristic (I_{DS}-V_{GS}) of the pTFET at 300 K for V_{DS} of -0.05 and -0.5V. I_{ON}/I_{OFF} improves from $1x10^2$ in sample set A (blue circles) to

$1.5x10^3$ in sample set B (red squares). The improvement in the I_{ON}/I_{OFF} ratio stems from the improved Fermi level movement efficiency achieved in the channel as seen from the CV analysis (Figure 5-3 (d)).

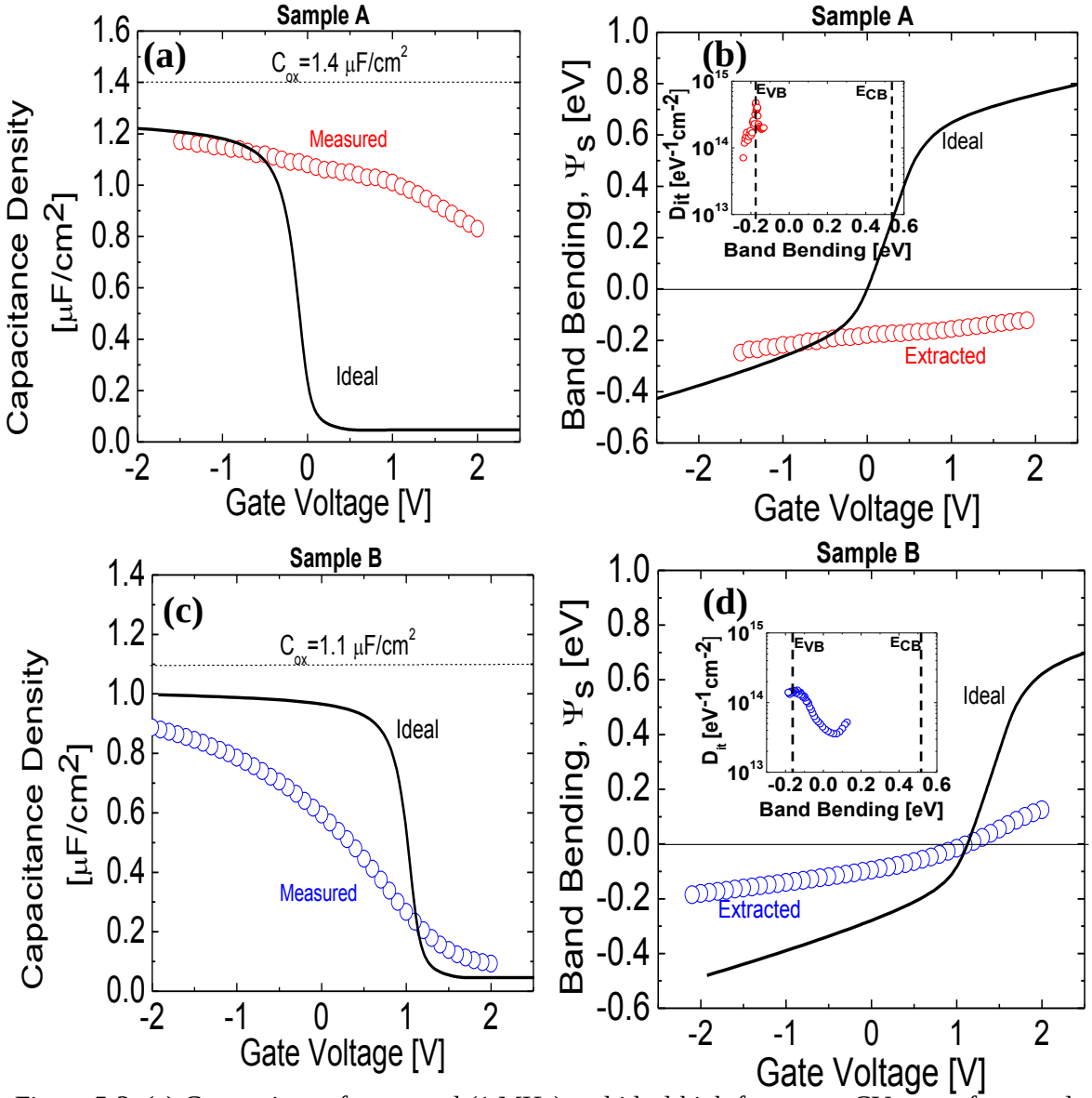

Figure 5-3. (a) Comparison of measured (1 MHz) and ideal high frequency CV curve for sample A MOSCAP with Al_2O_3/HfO_2 deposited at 250 °C. (b) Comparison of ideal and extracted band bending for sample A MOSCAP with Al_2O_3/HfO_2 deposited at 250 °C. (c) Comparison of measured (1 MHz) and ideal high-frequency CV curve for sample B MOSCAP with Al_2O_3/HfO_2 deposited at 110 °C (d)Comparison of ideal and extracted band bending for sample B MOSCAP with Al_2O_3/HfO_2 deposited at 110 °C. The insets in (b) and (d) show the interface trap distribution D_{it} for MOSCAPs with the high-κ dielectric deposited at 250 and 110 °C, respectively.

I_{ON}/I_{OFF} is expected to increase with further improvement in the Fermi level movement until I_{OFF} is limited by the Shockley-Read-Hall (SRH) generation-recombination current [45]. Comparable I_{ON} is observed in both samples at 300K [Figure 5-4 (a)] as expected, as both samples have similar bandbending and D_{it} for high V_{GS} corresponding to the on-state [Figure 5-3 (b-d)]. Figure 5-4 (b) shows a comparison of the switching slope characteristics of the two samples at 300K. Sample B has a minimum SS of 400 mV/decade, compared with 600 mV/decade sample for sample A. Figure 5-4 (c-d) respectively show the I_{DS}-V_{GS} and SS characteristics measured at 77K. The lower I_{ON} at 77K than that at 300K is due to an increase in the bandgap of $In_{0.7}Ga_{0.3}As$ and $GaAs_{0.35}Sb_{0.65}$ at 77K, resulting in changes in the bandalignment at the hetero-junction and an increased tunneling barrier height [17]. SS is improved significantly at 77K in comparison to at 300K due to the reduction in the D_{it} response as well as due to the reduction in the leakage floor. However, the minimum SS achieved even at 77K is only 200mV/decade (sample B). This is due to a lower value of C_{ox} of 1.1μF/cm^2; with further scaling of the oxide, an improved SS can be achieved.

Figure 5-5 (a) shows the output characteristics of sample A and B measured at T=300K and as a function of the gate bias. Both the samples showed poor saturation in the output characteristics. This could be attributed to lower value of C_{ox} and high D_{it} which degrade the device electrostatics. Figure 5-5 (b) shows the output characteristics of sample A and B measured at T=77K and as a function of the gate bias. Sample A showed poor saturation characteristics whereas sample B showed weak saturation indicative of slightly improved electrostatics attributed to lower D_{it}. It should also be noted that negative differential resistance (NDR) was not observed in either of the samples at T=300K and T=77K. This could be due to inefficient band to band tunneling process resulting from poor Fermi level movement efficiency as a result of high D_{it}.

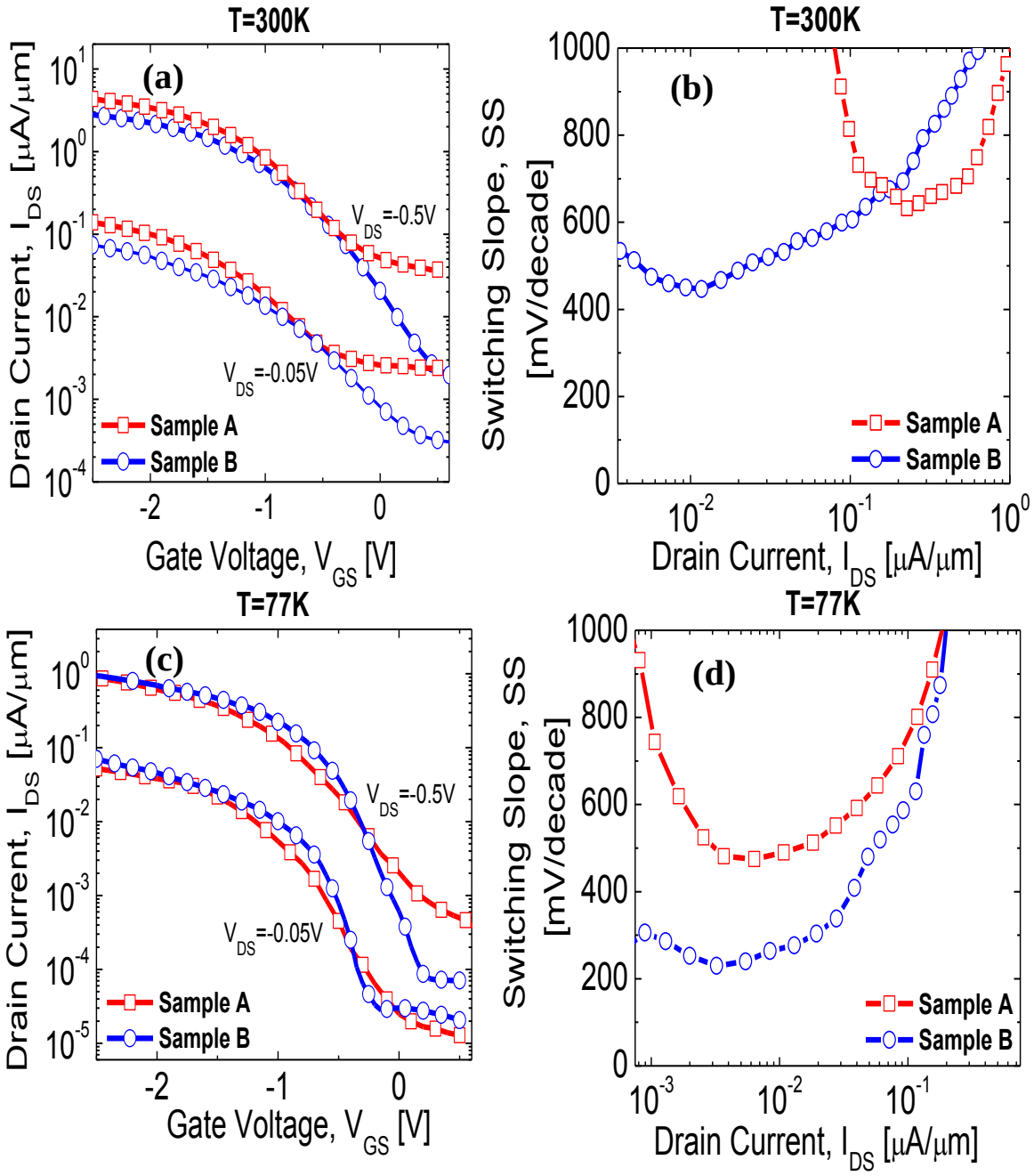

Figure 5-4. (a-b) I_{DS}-V_{GS} and SS characteristics of pTFET with Al_2O_3/HfO_2 deposited at 250 °C (sample A, red squares) and Al_2O_3/HfO_2 deposited at 110 °C (sample B, blue circles) for V_{DS}=-0.05 and -0.5V measured at (a-b) 300K showing improvement in I_{ON}/I_{OFF} and SS with lower deposition temperature ,(c-d) 77K showing improvement in I_{ON}/I_{OFF} and SS due to reduction in SRH leakage floor and suppression of D_{it} response in both samples due to the lower measurement temperature.

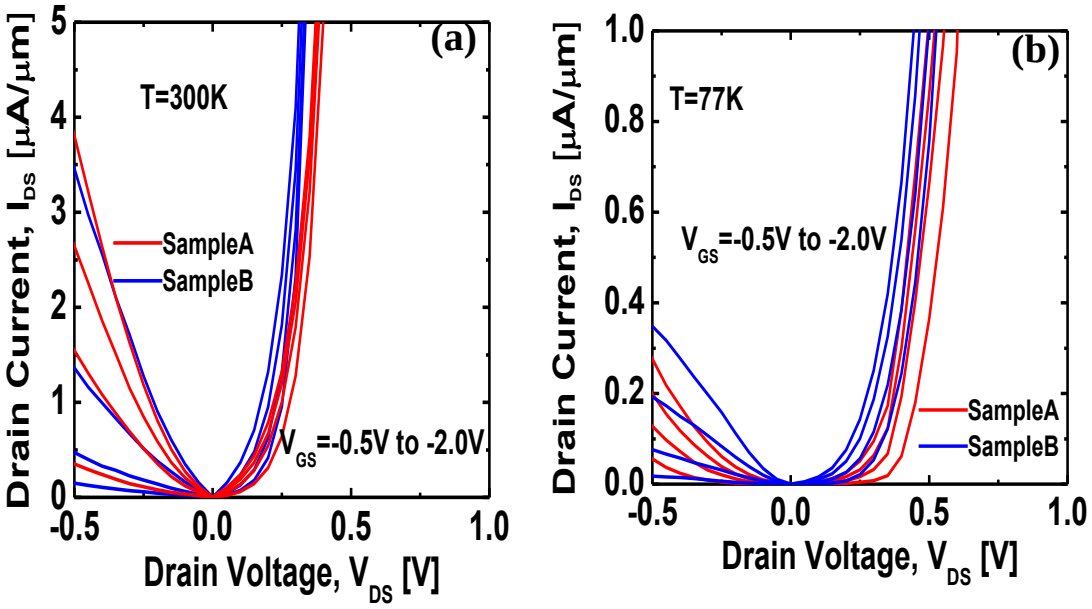

Figure 5-5. (a-b) Output characteristics of pTFET at T=300K and T=77K respectively.

To better understand the improvement of both MOSCAP and pTFET characteristics using the low temperature ALD process, the chemical composition at the high-κ/$GaAs_{0.35}Sb_{0.65}As$ interface was investigated using *exsitu* XPS. Figure 5-5 (a-c) show the high resolution Ga 3*d* (and Hf 4*f*), As 3*d*, and Sb $3d_{3/2}$ core level spectra of the two samples with a high-κ oxide stack of ~1 nm Al_2O_3 and ~1.4 nm HfO_2 deposited at 250°C (sample A) and 110°C (sample B). These XPS samples were subjected to the same chemical pretreatment as the MOSCAP structures. Figure 5-5 (a) shows the Ga 3*d* peak, which is suppressed by the Hf 4*f* core level. This makes it difficult to estimate the amount of gallium oxides present at the interface. An increased signal from the arsenic and antimony oxidation states was seen for the sample processed at 110°C [Figure 5-5 (b) and 5-5 (c), respectively]. Similarly, a large contribution from As-As and Sb-Sb-like states with respect to the bulk As-GaSb and Sb-GaAs components was observed in the case of the lower deposition temperature. The presence of group-V elements and native oxide in sample B, which exhibits better electrical characteristics in the MOSCAP and pTFET, appears counterintuitive.

However, the fact that the peak area of the oxides and elemental states is greater in sample B is not an indication that these states are present at the high-κ/GaSb interface. These states may reside closer to the surface of the HfO_2, which was further confirmed by more surface sensitive As 2*p* spectra (not shown) where arsenic oxidation and As-As states were detected in sample B, while these states were below the XPS detection limit in sample A. The elemental states are most likely to be generated by the decomposition of the native oxides as a result of the "clean-up" effect during the ALD process [63], which subsequently migrate through the high-κ oxide, with the variation in the deposition temperature and corresponding modifications to the composition of the native oxide also a possible factor [75]. Upon diffusion to the surface through the high-κ stack, these states should oxidize due to atmospheric exposure. The 250°C ALD temperature in sample A could be sufficiently high to allow for removal of the metallic species from the surface of the HfO_2, and could explain the large variation in native oxide states between the two samples. The fact that the Ga 3*d* peak profile is very similar for both samples, and there is no detectable signal observed in the more surface- sensitive Ga 2*p* spectra (not shown), suggests that there is no Ga diffusion to the surface within XPS detection limits in sample A or B, as any Ga located at the surface of the HfO_2 would be expected to dominate the Ga 3*d* spectra due to the suppression of the bulk signal by the high-κ oxide overlayer. In addition, the observed trend of the presence of group-V native oxides leading to a better interface is consistent with a reported study on improvement of a dielectric/GaSb interface using low-temperature (200°C) plasma-enhanced ALD (PEALD) Al_2O_3 [66]. In the PEALD GaSb sample, Sboxide was detected at the interface whereas no Sboxide was detected in the ALD sample with the oxide deposited at 300°C. Further investigation is needed to unambiguously identify the exact surface conditions leading to better dielectric/$GaAs_{0.35}Sb_{0.65}$ interfaces.

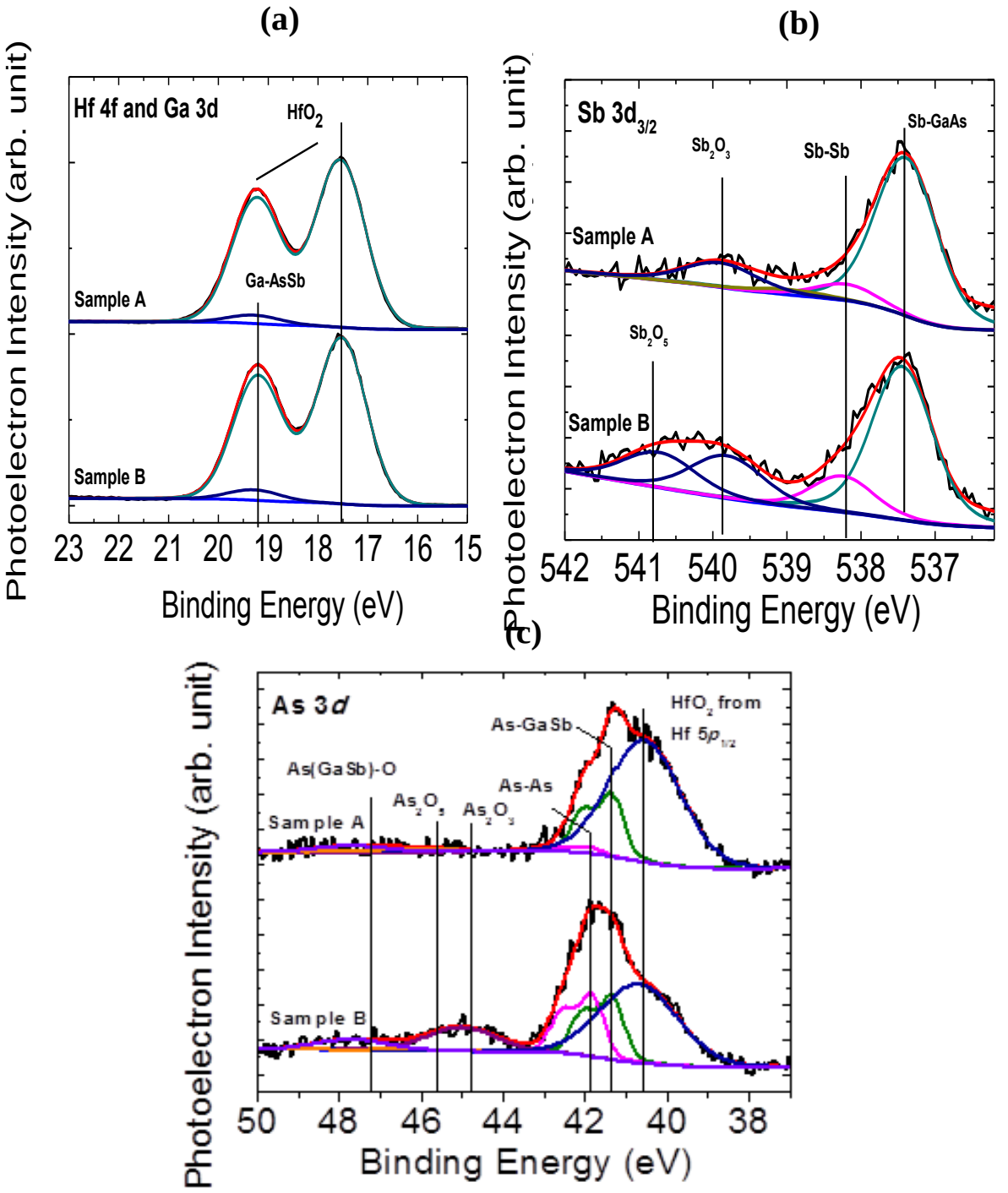

Figure 5-6. Ga 3d, As 3d, and Sb $3d_{3/2}$ spectra for Al_2O_3/HfO_2 deposited at 250 °C (sample A) and at 110 °C (sample B) with ~1 nm Al_2O_3 and 1.4 nm HfO_2 showing (a) Ga 3d spectrum suppressed by Hf 4f core level. (b) As 3d showing presence of As-oxide in sample B (c) Sb $3d_{3/2}$ showing high Sboxide content in sample B.

IV. Conclusions

In summary, the effect of deposition temperature on the quality of a high-κ/$GaAs_{0.35}Sb_{0.65}$ interface was demonstrated. Lowering the high-κ oxide deposition temperature from 250 to 110 °C significantly improved the characteristics of MOSCAP and pTFET devices, which resulted in larger band bending, a reduced D_{it} response, a larger I_{ON}/I_{OFF} and a reduced switching slope. This is the first demonstration of p-channel heterojunction tunneling FETs in a compound semiconductor material system. XPS measurements show the presence of group-V native oxide, which is in agreement with the reported findings on an improved dielectric/GaSb interface employing low temperature PEALD oxide.

Chapter 6

Design, Fabrication and Characterization of InAs/GaSb Heterojunction p-Channel Tunnel FET

I. Introduction

In the previous chapter, gate dielectric integration strategy was discussed to address the high-k/antimonide interface issue in pTFET. A second challenge in the realization pTFET arises from the density of states (DOS) mismatch between the conduction band and the valence band. In n^+ heavily doped source region of III-V pTFETs, the Fermi level is degenerate and located far away from the conduction band edge, thereby preventing efficient energy filtering of conduction band holes as they tunnel from conduction band states into the valence band states in the channel. This results in a fundamental tradeoff between I_{ON} and the switching slope in pTFETs [76]. Further, realization of TFETs in complimentary logic application requires a high performance pTFET. Staggered-gap $In_{0.7}Ga_{0.3}As/GaAs_{0.35}Sb_{0.65}$ pTFET demonstrated in chapter 4 achieved drive current of 5uA/um which is much lower in comparison to the nTFET counterpart.

In this chapter, InAs/GaSb hetero-junction (hetJ) and GaSb homo-junction (homJ) p-channel TFET are experimentally demonstrated using a low temperature atomic layer deposited high-κ gate dielectric. HetJ pTFET exhibited drive current of 35μA/μm in comparison to homJ pTFET which exhibited drive current of 0.3μA/μm at V_{DS}=-0.5V under DC biasing conditions. Additionally, with pulsing of 1μs gate voltage, hetJ pTFET exhibited enhanced drive current of 85μA/μm at V_{DS}=-0.5V which is the highest reported in the category of III-V pTFET. Detailed device characterization is performed through analysis of the capacitance-voltage characteristics, pulsed current-voltage characteristics, and x-ray diffraction studies.

II. Device Design

Atomistic simulations [77] were performed using the non-equilibrium green function method on ultra-thin body double gate TFET structure with body thickness (T_{body}) of 7nm, equivalent oxide thickness (EOT) of 1nm and gate length (L_{gate}) of 32nm (Figure 6-1 (a)). Figure 6-1 (b) shows the transfer characteristics (I_{DS}-V_{GS}) of $In_{0.7}Ga_{0.3}As/GaAs_{0.35}Sb_{0.65}$ and InAs/GaSb TFETs for varying values of source doping (N_S). The gate metal work-functions were adjusted so that I_{OFF} is matched to 5nA/μm in all the simulations.

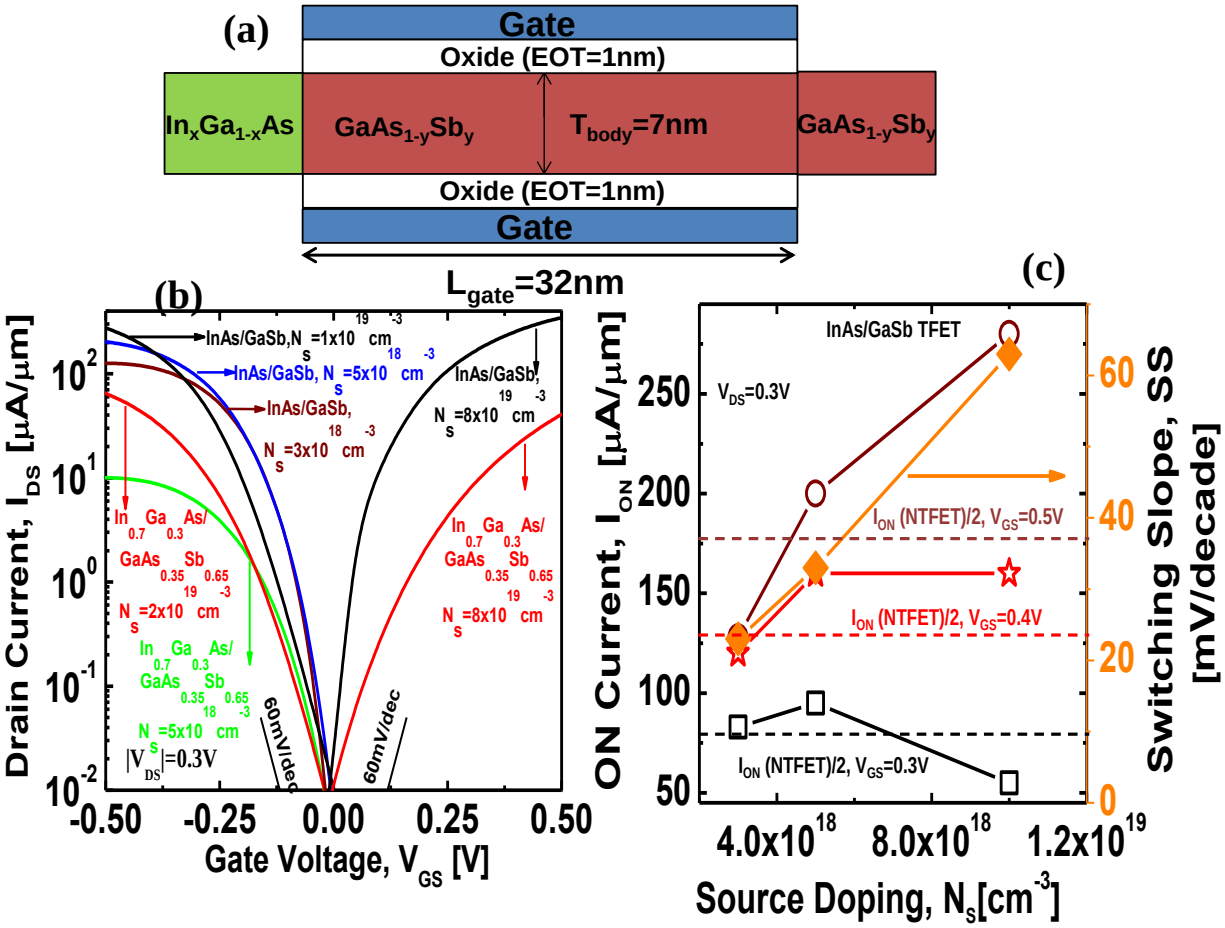

Figure 6-1. (a) Schematic of ultra-thin body PTFET simulated. (b) Transfer characteristics of InAs/GaSb and $In_{0.7}Ga_{0.3}As/GaAs_{0.35}Sb_{0.65}$ pTFET as a function of the source doping. (c) I_{ON} as a function of N_S in InAs/GaSb pTFET.

InAs/GaSb TFET exhibits superior characteristics compared to $In_{0.7}Ga_{0.3}As/GaAs_{0.35}Sb_{0.65}$ due to smaller Eb_{eff}. InAs/GaSb nTFET with $N_S=8x10^{19}cm^{-3}$ exhibits high I_{ON} of 320μA/μm at V_{GS}=0.5V, V_{DS}=0.3V and exhibits sub-60mV/decade SS. InAs/GaSb pTFET on the other hand shows degraded SS for higher N_S due to the low DOS of the conduction band in InAs. Figure 6-1(c) shows I_{ON} of InAs/GaSb pTFET as a function of N_S for different V_{GS}. At V_{GS}= 0.5 and 0.4 V, in order for InAs/GaSb pTFET to deliver half the I_{ON} of InAs/GaSb nTFET, N_S of $5x10^{18}cm^{-3}$ is desired. However, at V_{GS}=0.3V, higher N_S of $1x10^{19}cm^{-3}$ results in lower I_{ON}. This is due to the degraded SS of the pTFET. Hence, depending on the operating voltage, N_S needs to be optimized such that the pTFET delivers enough I_{ON} to complement the performance of nTFET. N_S of $1x10^{19}cm^{-3}$ was adopted for InAs/GaSb hetJ pTFET as well as GaSb homJ pTFET in this chapter.

III. Experimental Procedure

Figure 6-2 (a-b) show the schematic layer structures of InAs-GaSb hetJ pTFET and GaSb homJ respectively, which were grown on GaSb substrates using MBE. AlSb/AlAs super-lattice was used as lattice matched isolation buffer for each structure. Figure 6-2 (c-d) shows the false colored cross-section TEM micrograph of the fabricated hetJn and homJ pTFETs respectively. Fabrication procedure for the hetJn pTFET was same as that described in chapter 2. The only difference was that the source-channel junction in the case of pTFET remained at the top of the layer structure as opposed to bottom of the structure in the case of nTFET. Figure 6-3 shows the process flow for fabrication of GaSb homJ pTFET. For the GaSb homJ sample, 60 nm of Titanium was evaporated prior to Molybdenum sputtering in order to facilitate the self-aligned gate deposition as explained below. Titanium/Chromium hard mask was created on top of Molybdenum after patterning using electron beam lithography. Using Titanium/Chromium as

etch mask, Molybdenum, Titanium and the semiconductor region underneath were etched to form a vertical pillar-like structure.

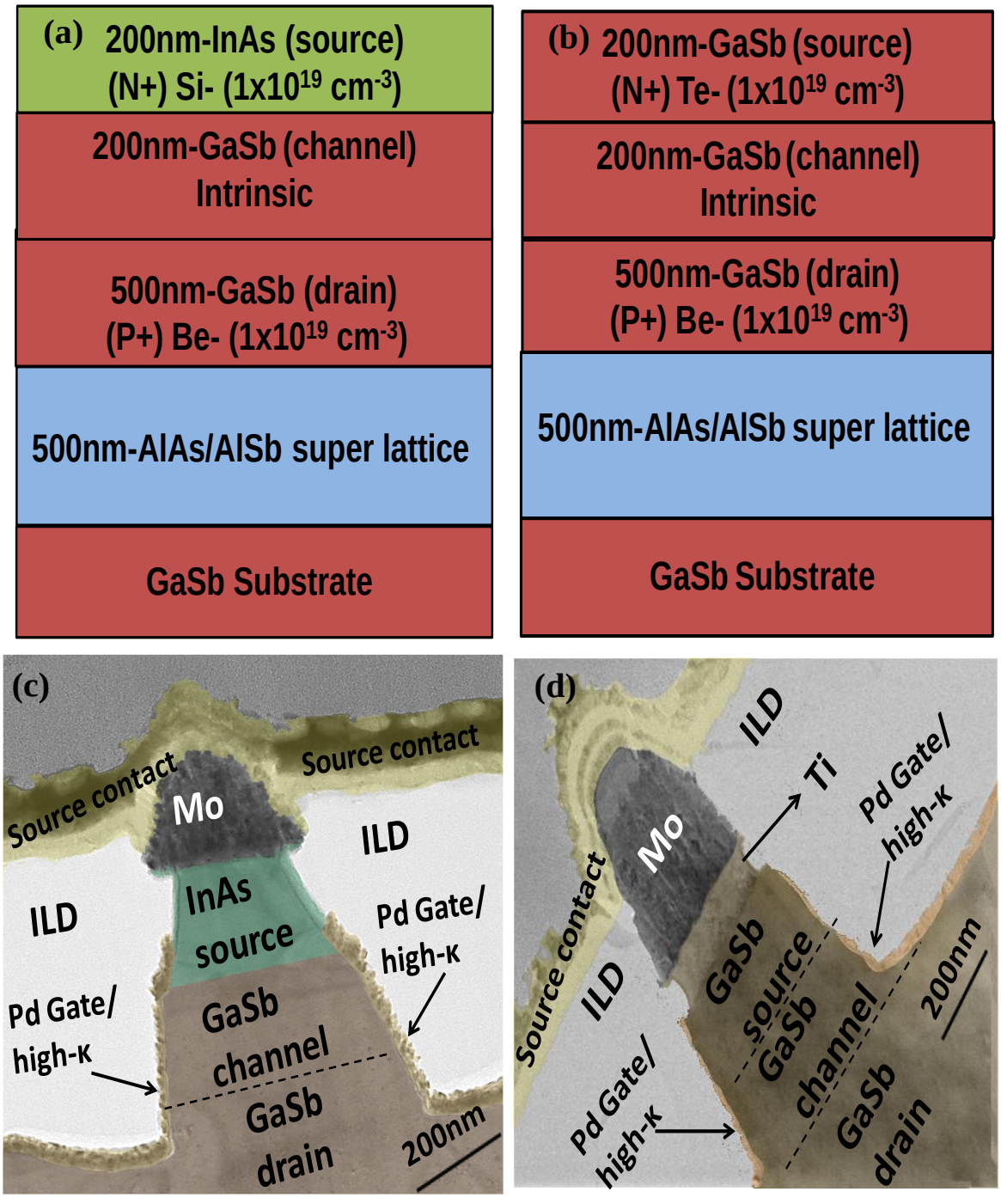

Figure 6-2. (a) Schematic of MBE grown InAs-GaSb hetJ layer structure (b Schematic of MBE grown GaSb homJ layer structure (c) False colored cross section TEM of the fabricated InAs-GaSb hetJ. (d) False colored cross section TEM of the fabricated GaSb homJ pTFET.

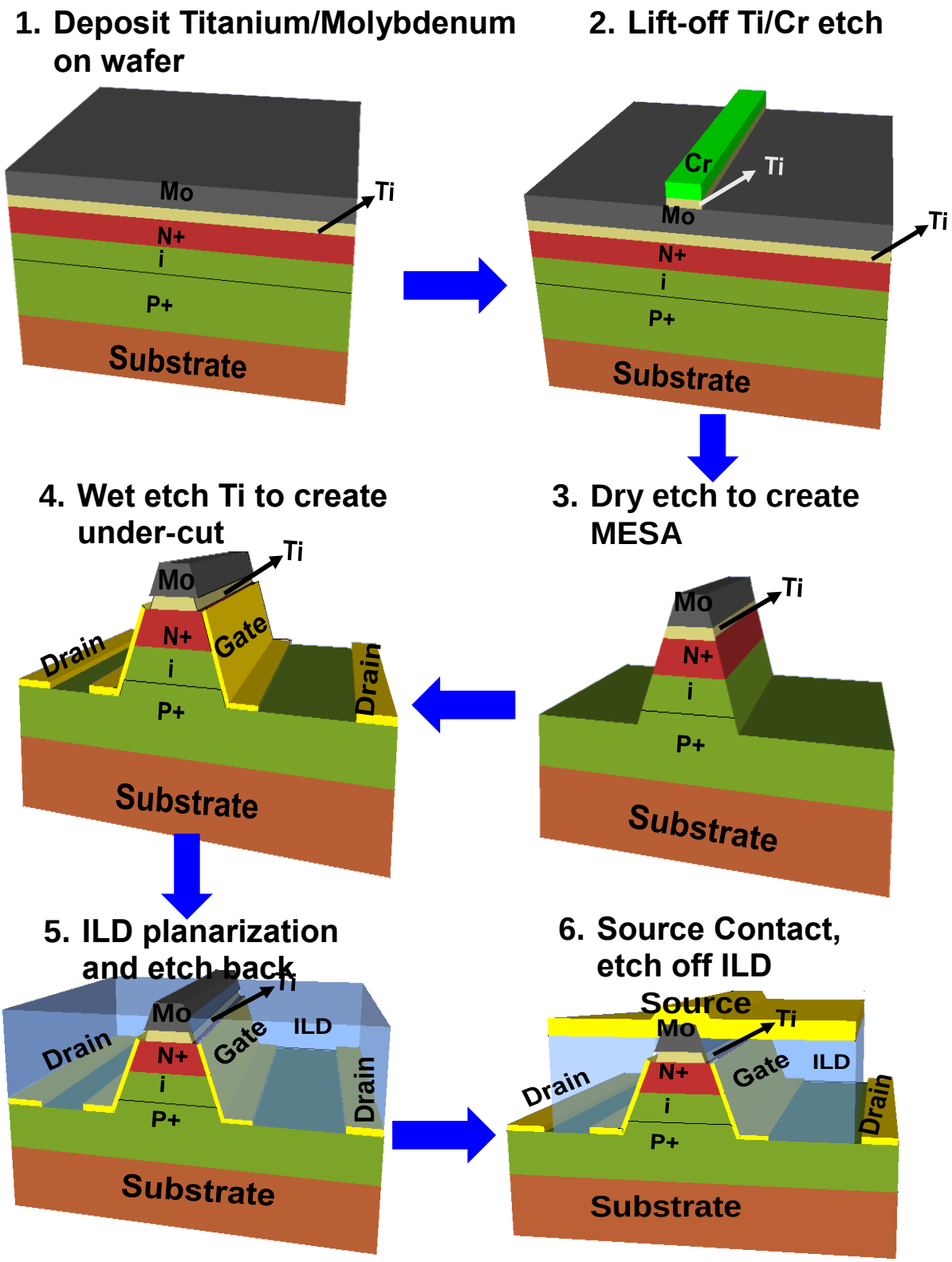

Figure 6-3. Fabrication process flow of the GaSb homJ pTFET.

Selective wet etching of GaSb with respect to Molybdenum is difficult. Hence in the case of GaSb homJ sample, Titanium was selectively wet etched using dilute HF acid solution ($HF:H_2O$=1:100) to create the required undercut. Prior to the gate oxide deposition, both the homJn and hetJn samples were treated in concentrated HCl solution ($HCl:H_2O$ = 1:1) for 5 minutes followed by rinse in isopropyl alcohol (IPA). A bi-layer gate oxide comprising of 1nm Al_2O_3 and 3.5nm HfO_2 was immediately deposited using atomic layer deposition (ALD). Gate metal (Palladium) was deposited by e-beam evaporation after patterning to form a self-aligned gate. Drain contact was then defined, oxide removed using dry-etch and Ti/Pd/Au metal stack evaporated. The samples were then baked in an inter-layer dielectric (ILD) for 60 minutes and then etched back in Oxygen plasma until the top of Molybdenum was exposed. Source contact was then defined and Titanium/Palladium/Gold metal stack evaporated. Finally, ILD was etched off from the active regions of the device. For MOSCAP fabrication, samples were degreased in acetone and methanol for 5 minutes each and rinsed in IPA, followed by a dip in concentrated HCl solution ($HCl:H_2O$ = 1:1) for 5 minutes and an IPA rinse. The samples were immediately loaded into the ALD chamber and gate oxide comprising of 1nm of Al_2O_3 and 3.5nm HfO_2 was deposited. Following patterning the gate pad using electron-beam lithography, Palladium/Gold metal stack was evaporated to form gate contact on the MOSCAP samples. The current voltage characteristics of the pTFETs were measured using an HP parameter analyzer. Capacitance-voltage (CV) and conductance-voltage (GV) measurements were obtained using a HP 4285A precision *LCR* meter type. Keithley 4200 Semiconductor Characterization System with a dual channel 4225 Pulse Measure Unit (PMU) was used for the pulsed I_{DS}-V_{GS} measurements. X-ray reciprocal space maps (RSMs) were obtained using Panalytical X'pert Pro, system with Cu Kα-1 as an x-ray source. Both the symmetric (004) and asymmetric (115) RSMs were recorded from the hetJ pTFET structure.

IV. Optimization and Characterization of Highκ-/GaSb Interface

As discussed in chapter 5, a low temperature ALD improved the high-κ/$GaAs_{0.35}Sb_{0.65}$ interface resulting in improved Fermi level movement efficiency. The improvement in the high-κ/ $GaAs_{0.35}Sb_{0.65}$ stemmed from the presence of Sb-oxide at low ALD temperature (110°C). A similar strategy was adopted for the optimization of the high-κ/GaSb interface. Figure 6-4 (a) shows the CV characteristics of ALD deposited on undoped GaSb at deposition temperatures (T_{dep}) of 110°C, 150°C and 200°C, measured at T=300K. As T_{dep} was reduced, CV characteristics showed improved modulation. Hence, ALD deposition temperature of 110°C was used for pTFET fabrication. The high frequency capacitance density in accumulation was close to 1.1μF/cm^2 which corresponds to an EOT of 3.4nm. Figure 6-4 (b) shows the CV characteristics of ALD deposited at 110°C measured at T=300K and 150K. At T=150K, reduced frequency dispersion and enhanced modulation was seen in the CV characteristics attributed to suppression of trap response at lower temperature.

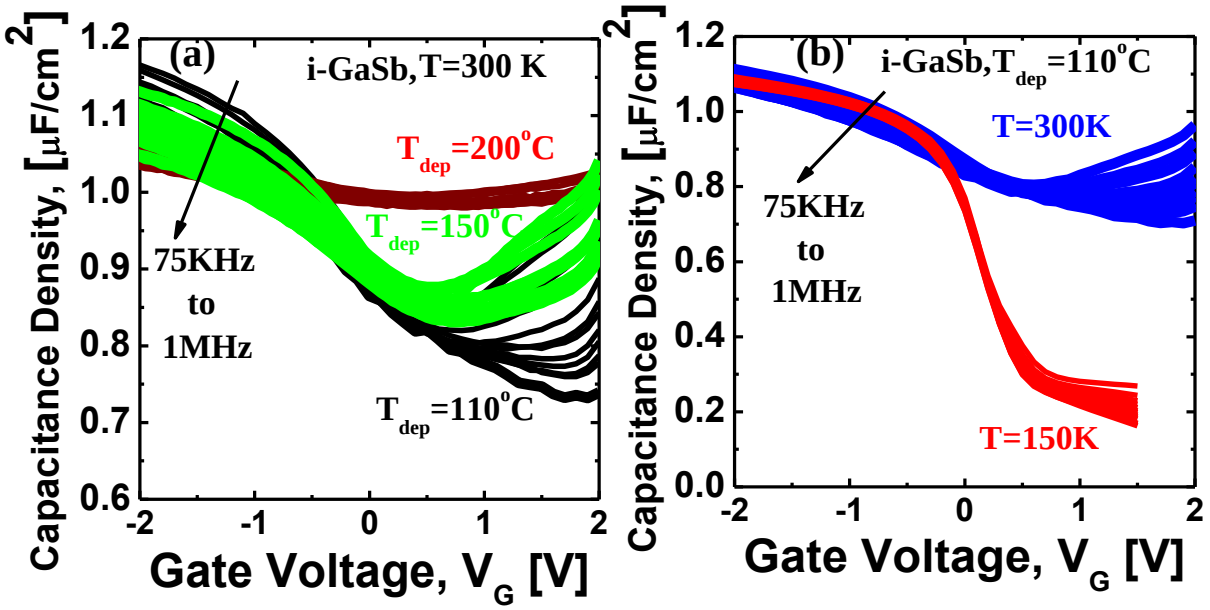

Figure 6-4. (a) C-V characteristics of Al_2O_3/HfO_2 deposited on p-type GaSb in the frequency range of 75 KHz to 1 MHz measured at 300K as a function of deposition temperature (b) C-V characteristics of Al_2O_3/HfO_2 deposited 110 °C and measured at T=300K and T=150K.

The equivalent-circuit modeling technique was used to model the measured CV and GV characteristics and extract D_{it} and trap response time. In this approach, CV and GV characteristics are simulated as a function of frequency for various interface state density (D_{it}) and trap response time values until the error between measured and modeled values are minimized [78][79]. This method is advantageous when the traps extend into the oxide and thus mask the conductance peaks. Traps extending 1nm into the oxide were taken into consideration for modeling [79]. The distribution of traps as a function of distance 'x' away from the high-κ/GaSb interface is given by:

$$N_{it} = N_{it}(0)\exp\left(\frac{-x}{x_{DIGS}}\right) \quad (6\text{-}1)$$

where $N_{it}(0)$ is the trap density at high-κ/GaSb interface, x_{DIGS} is the characteristic decay length which is used as a fitting parameter ($x_{DIGS} = 1\text{Å}$) in the equivalent circuit model. The response time of the traps in the oxide increases exponentially as follows:

$$\tau = \tau_0(E_t)\exp(2kx) \quad (6\text{-}2)$$

where $\tau_0(E_t)$ is the trap response time at x=0 and at a given energy level E_t, k is the wave vector for holes tunneling from the valence band in GaSb to the traps given by:

$$k = \sqrt{2m^*\Delta E_V/\hbar^2} \quad (6\text{-}3)$$

where m* is the hole effective mass, ΔE_V is the valence band offset between high-κ and GaSb. Using ΔE_V=3.4eV [80] and m*=0.044eV [81] k was calculated to be 0.2/Å. Figure 6-5 (a-b) show the measured and modeled CV, GV characteristics which are in good agreement with each other. Figure 6-5 (c) shows the extracted D_{it} as a function of gate voltage and integrated over various depths into the oxide. As more traps extending into the oxide was taken into account, the net integrated D_{it} measured increased. Traps beyond x=0.4nm did not contribute to the net integrated trap density since $x_{DIGS} = 1\text{Å}$.

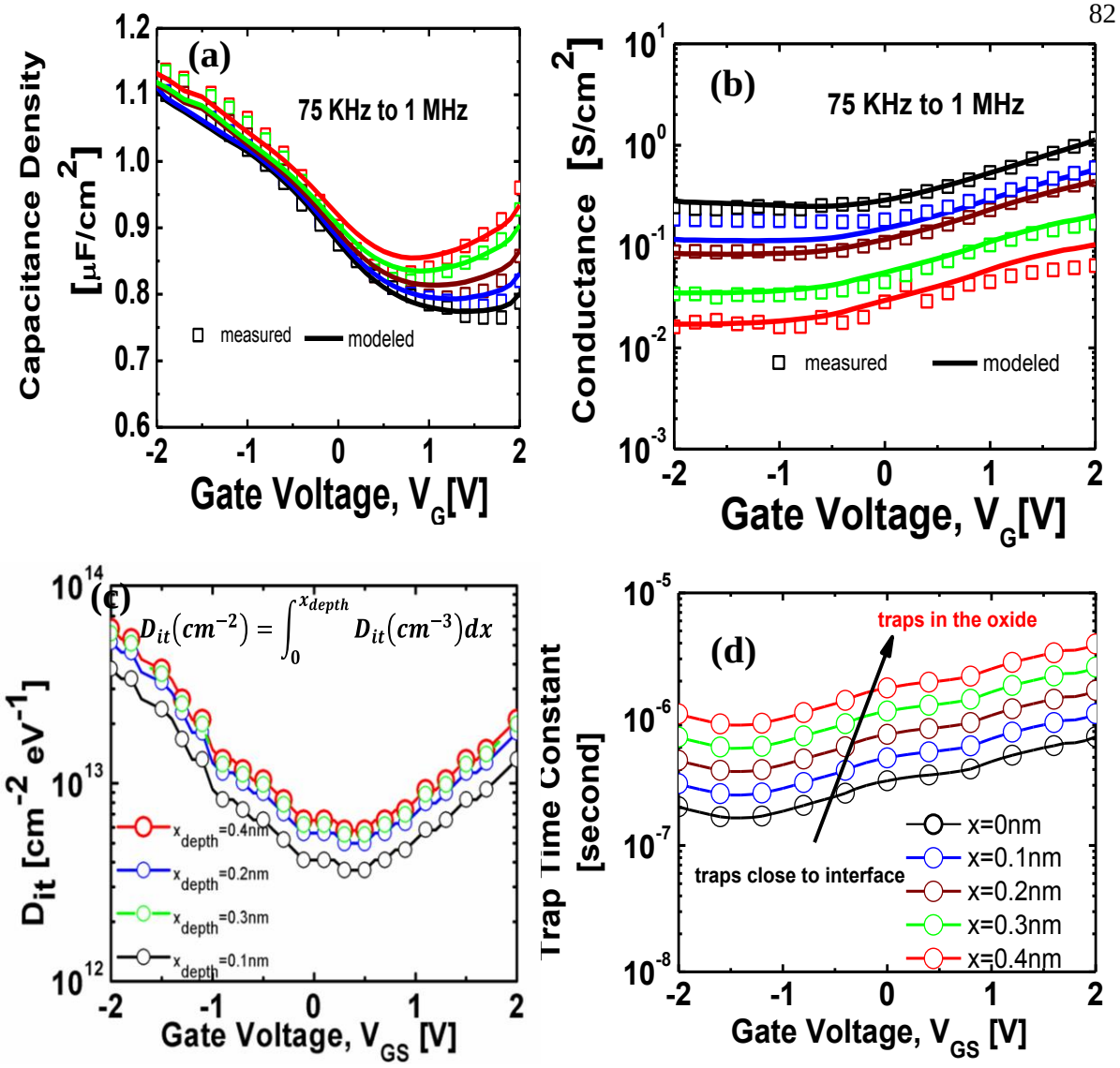

Figure 6-5. (a) Measured and modeled CV characteristics at T=300K as a function of frequency. (b) Measured and modeled GV characteristics at T=300K as a function of frequency (c) Extracted D_{it} as a function of gate voltage taking into account traps distributed into the oxide (d) Extracted trap response time as a function of gate voltage taking into account traps distributed into the oxide

Figure 6-5 (d) shows the extracted trap response time as a function of gate voltage for various trap depths into the oxide. The response time for traps increase exponentially as the distance from the interface increases. However, it should be noted that the factor k is assumed to be independent of gate voltage. This might introduce some error in the calculation of trap time constants as a function of trap position in the oxide. Nevertheless, within the limits of the model

used, the trap response time expected for this high-κ gate stack on GaSb should be faster than 1μs since traps beyond x=0.4nm do not contribute to the overall D_{it}.

Figure 6-6 shows D_{it} as a function of energy location in the bandgap (Eg) of GaSb for T_{dep} of 110°C and 200°C. With T_{dep}=200 °C, the Fermi level is pinned near the valence band edge possibly due to thermal decomposition of Sb-oxide leading to formation of Sb dangling bonds which introduces high D_{it} near valence band. With T_{dep}=110°C, lower density of Sb dangling bonds could be expected due to the presence of Sb-oxide [chapter 5] and thus the Fermi level movement improved to roughly 0.125eV away from the valence band edge.

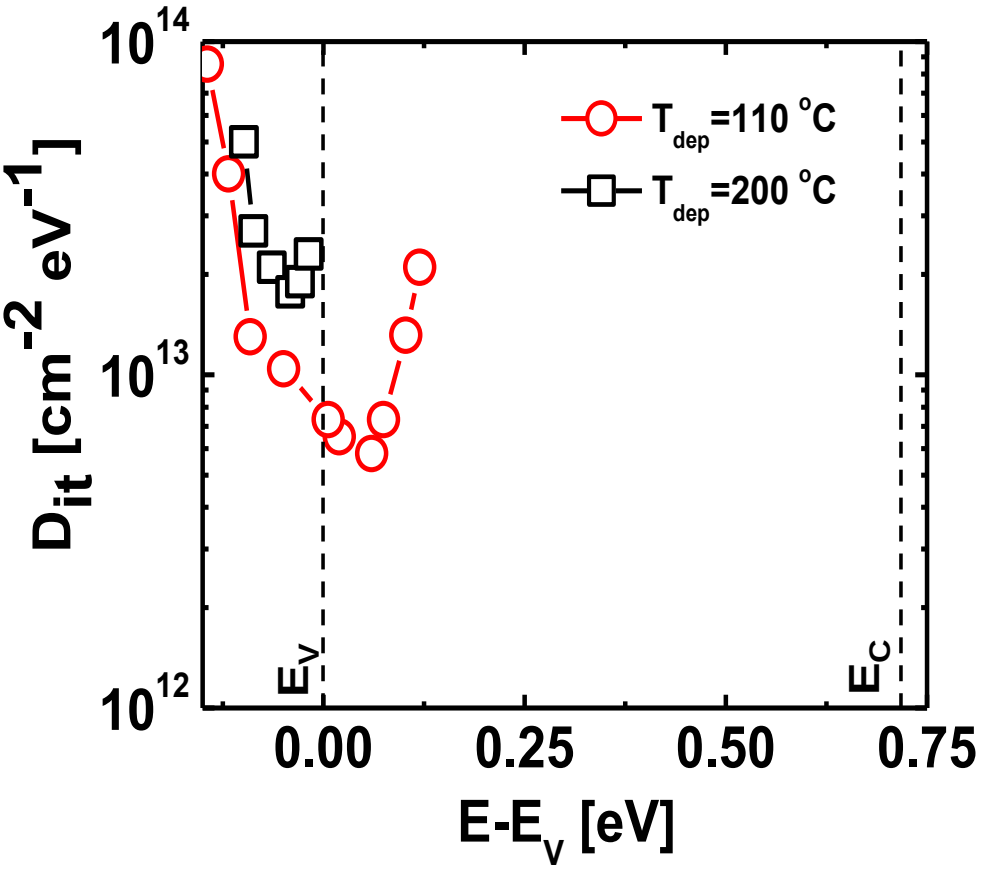

Figure 6-6. D_{it} as a function of energy location in the bandgap for MOSCAP with T_{dep}=110 °C and 200 °C showing lower D_{it} and Fermi level movement at T_{dep}=110 °C.

V. Electrical Characterization

Figure 6-7 (a-b) shows the I_{DS}-V_{GS} characteristics of InAs/GaSb hetJ and GaSb homJ pTFETs respectively at T=300K,150K and for V_{DS}=-0.05V and -0.5V. HetJ pTFET exhibited I_{ON} of 35μA/μm at V_{DS}=0.5V at T=300K. GaSb homJ pTFET in comparison exhibited I_{ON} of 0.3μA/μm at V_{DS}=0.5V and T=300K. The difference in I_{ON} is attributed to change in E_{Beff} from 0.73eV in GaSb homJ to -0.15eV in hetJ pTFET [82]. Reduction in I_{ON} at T=150K is attributed to increase in band-gap with decreasing temperature and thereby increasing the barrier for tunneling from the conduction band in the source to valence band in the channel. I_{OFF} in hetJ pTFET was 1μA/μm and much higher than I_{OFF} =3nA/μm in GaSb homJ pTFET. High I_{OFF} in heterojunction material system compared to a homo-junction material system has been reported in nTFETs and attributed to defects at the heterointerface [41]. It is possible that the hetJ pTFET suffers from high defect density at the hetero-interface leading to high I_{OFF}. I_{OFF} in hetJ pTFET was found to scale with the device cross-section area (product of width and body thickness) which confirmed that I_{OFF} was caused by bulk conduction (not shown). At T=150K, I_{OFF} reduced substantially and I_{ON}/I_{OFF} improves to ~10^4 in both hetJ as well as homJ pTFET. The reduction in I_{OFF} could be attributed to: (1) reduction in the Shockley-Read-Hall generation-recombination current which is a strong function of temperature [45] and (2) suppression of D_{it} response which improved the Fermi-level movement efficiency (Figure 6-4 (b)). Figure 6-7 (c) shows the SS as a function of drain current for both homj and hetJ pTFETs. HetJ pTFET not only exhibited lower SS but the minimum SS was achieved at higher drain current. Further, hetJ pTFET showed lower drain induced barrier thinning (DIBT) in comparison to homj pTFET measured at I_{DS}=1nA/μm and T=150K (Figure 6-7 (d)). Lower SS and DIBT in hetJ pTFET stemmed from the reduced E_{Beff} compared to homJ pTFET which resulted in interband-generation occurring closer to the source/channel interface and resulting in improved electrostatics [83].

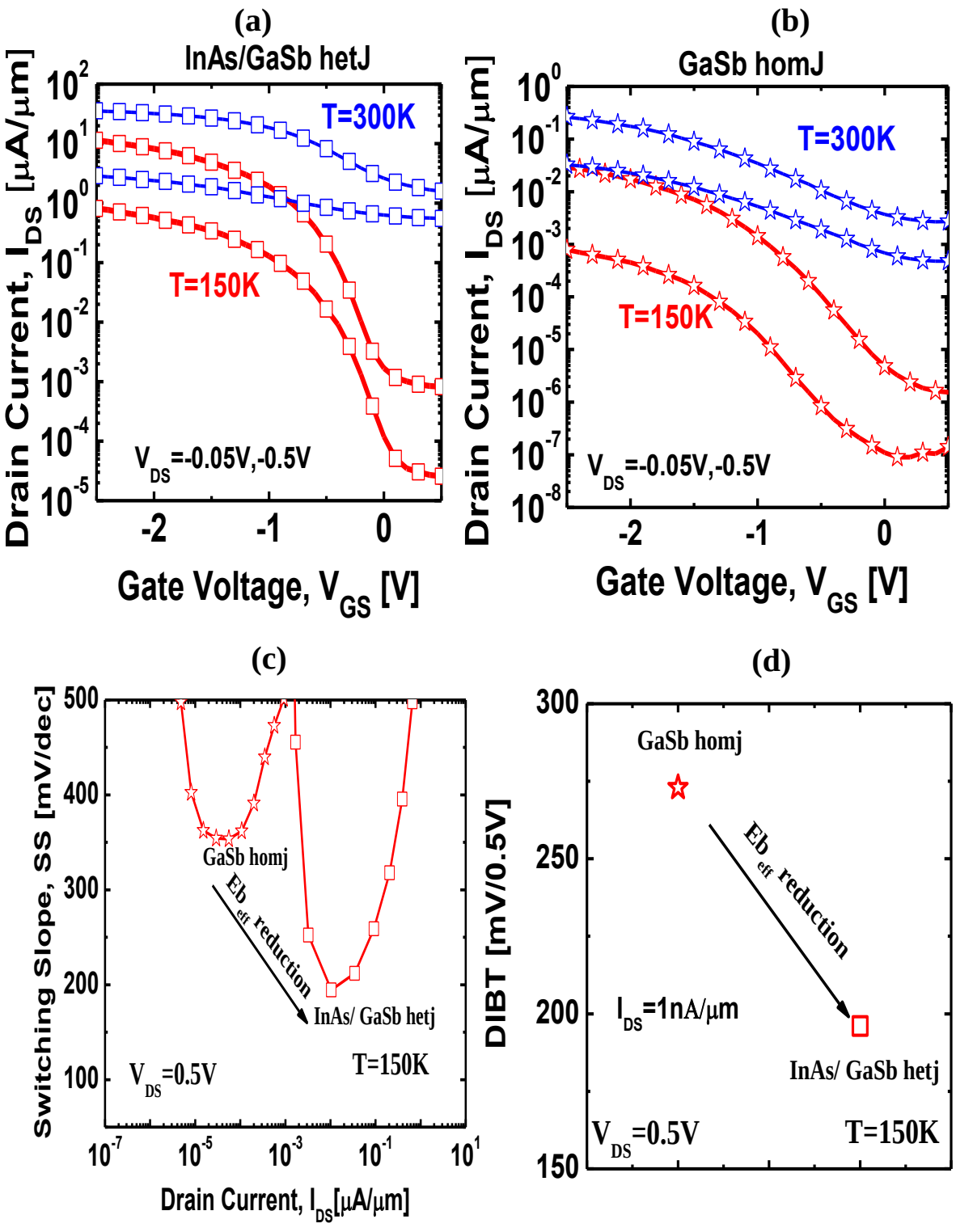

Figure 6-7. (a-b) I_{DS}-V_{GS} characteristics of hetJ and homJ pTFETs at T=300K and 150K (c) SS as a function of drain current at T=150K showing lower SS in hetJ compared to homJ pTFET (d) hetJ pTFET exhibits lower DIBT compared to homJ pTFET at I_{DS}=1nA/μm, T=150K.

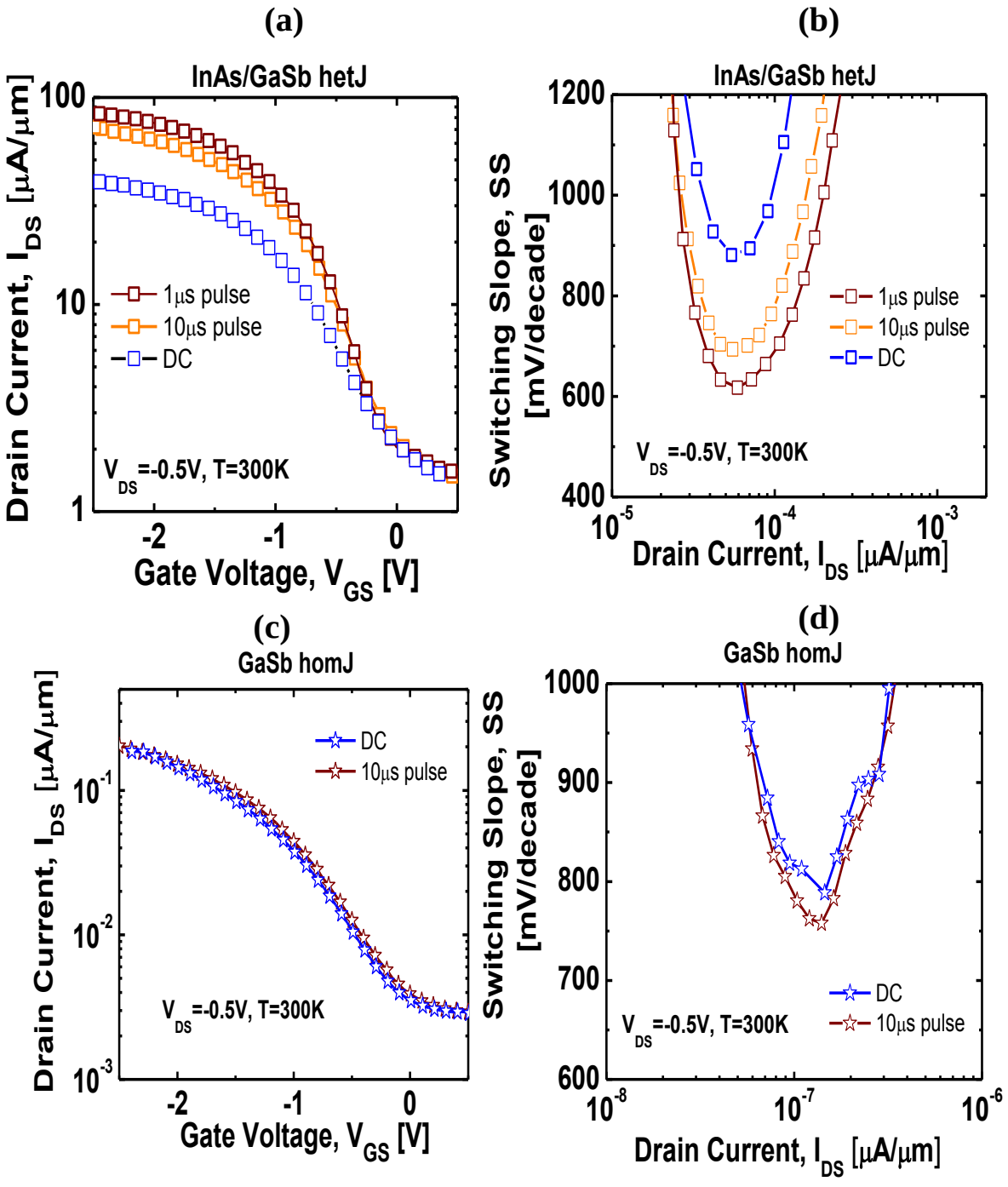

Figure 6-8. (a) I_{DS}-V_{GS} characteristics of hetJ for varying gate voltage pulse widths (b) SS of hetJ pTFET as a function of drain current for varying gate voltage pulse widths (c) I_{DS}-V_{GS} characteristics of homJ pTFET show negligible change in ION with 10μs gate voltage pulsing compared to DC bias conditions (d) SS of homJ pTFET shows negligible change in I_{ON} with 10μs gate voltage pulsing compared to DC bias conditions.

Figure 6-8 (a) shows the I_{DS}-V_{GS} characteristics of hetJ pTFET at V_{DS}=0.5V for varying gate voltage pulse widths. With a gate voltage pulse width of 1µs, I_{ON} increased to 85µA/µm which corresponds to more than 2X improvement over I_{ON} measured under DC bias conditions. Interestingly, with a gate voltage pulse width of 10µs, I_{ON} increased to 70 µA/µm which is roughly 2X of the I_{ON} under DC bias conditions. Figure 6-8 (b) shows the SS of hetJ pTFET as function of drain current for varying gate pulse widths. With 1µs gate pulsing a minimum SS of 500mV/decade was achieved compared to ~1000mV/decade under DC biasing conditions. Further, with 10µs gate pulsing a minimum SS of ~600mV/decade was achieved. As discussed in section IV, the trap response time for high-κ on GaSb was calculated to be faster than 1µs. For additional confirmation, 10µs gate pulsing was carried out and I_{DS}-V_{GS} characteristic measured in homJ pTFET. HomJ pTFETs exhibited negligible change in I_{ON} as well as SS (Figure 6-8 (c-d)). To further understand the anomalous response to gate voltage pulsing in InAs/GaSb, detailed material characterization was performed.

VI. Material Characterization

The relaxation state and residual strain of epilayers within the InAs/GaSb hetJ pTFET structure were obtained from reciprocal space maps (RSMs). Figure 6-9 (a-b) show the symmetric (004) and asymmetric (115) RSMs from this structure. All layers with measured compositions were labeled to the corresponding reciprocal lattice points (RLPs). As shown in Figure 6-9 (a-b) four distinct RLP maxima were found in RSMs of this structure, corresponding to (1) GaSb substrate as well as the GaSb channel/drain layers, (2) InAs source layer, (3) the satellite peaks from AlAs/AlSb super lattice and (4) an extra $GaAs_{1-y}Sb_y$ layer which is not expected from this structure. The composition of As in this layer was determined to be ~2.2%. As an additional confirmation, cross-section TEM of the pTFET structure was taken as shown in Figure 6-9 (c).

The presence of an amorphous layer at the hetero-junction was found, which corresponds to the $GaAs_{0.022}Sb_{0.978}$ layer detected in the XRD experiment.

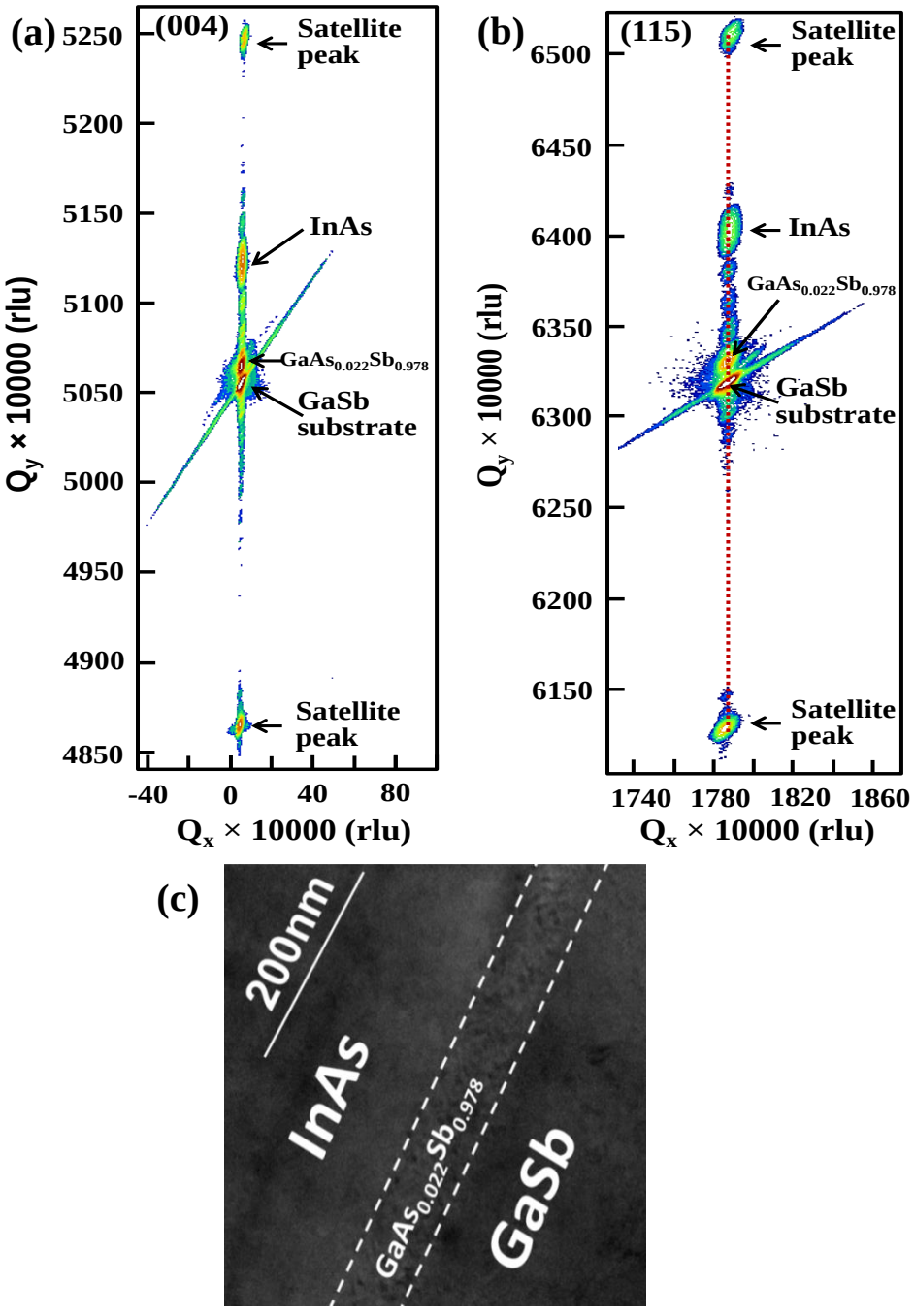

Figure 6-9. (a-b) Symmetric and asymmetric RSM of InAs/GaSb structure showing the presence of $GaAs_{0.022}Sb_{0.978}$ at the hetero-junction. (c) Cross-section TEM of the InAs/GaSb structure confirming the presence of an amorphous layer of $GaAs_{0.022}Sb_{0.978}$ at the heterojunction.

The $GaAs_{0.022}Sb_{0.978}$ layer may be introduced during the switching from GaSb channel layer to InAs source. A proper switching sequence of III/V elements is critical for engineering an abrupt hetero-interface during the growth of mixed As/Sb materials [84-86], otherwise the intermixing between As and Sb atoms will result in uncontrolled layer composition at the hetero-interface, which will cause the change of strain relaxation properties of the epilayer grown on this interface [43]. The change of strain relaxation properties may introduce high density dislocations at the hetero-interface and within the InAs source layer, which explains the high I_{OFF} in the fabricated hetJ pTFET. Besides, the formation of $GaAs_{0.022}Sb_{0.978}$ layer at the hetero-interface will change the band alignment of source/channel, which leads to the increase of tunneling distance and degrade the device performance. Furthermore, the $GaAs_{0.022}Sb_{0.978}$ interfacial layer between InAs source and GaSb channel may also introduce unexpected interface states with the high-κ due to the change of strain relaxation properties, and these trap states could lead to different D_{it} response for the device and might explain the anomalous pulsed I_{DS}-V_{GS} response in hetJ pTFETs.

VII. Benchmarking

Table 6-1 shows the performance comparison of the reported pTFETs within the III-V material system. The gate voltage was chosen sufficiently high enough to account for the stretch out in the I_{DS}-V_{GS} characteristics due to the presence of D_{it}. InAs/GaSb hetJ pTFET exhibits drive current of 85 μA/μm which is the highest reported in the category of III-V pTFET. With the scaling of EOT and the reduction in D_{it}, the device characteristics are expected to improve further.

Material	EOT (nm)	Eb_{eff} (eV)	V_{DS} (V)	I_{ON} (µA/µm)	Reference
InAs-Si	3.65	-	-0.5	0.1	[87]
$In_{0.7}Ga_{0.3}As/GaAs_{0.35}Sb_{0.65}$	3.4	0.25	-0.5	5	Chapter 5
GaSb	3.4	0.73	-0.5	0.3	*This work*
InAs/GaSb	3.4	-0.15	-0.5	85	*This work*

Table 6-1. Benchmarking of I_{ON} against experimentally demonstrated pTFET till date.

VIII. Conclusions

InAs/GaSb hetero-junction and GaSb homo-junction pTFET were grown and fabricated using a low temperature ALD high-κ gate dielectric. The hetJ pTFET exhibited I_{ON} of 35µA/µm at V_{DS}=0.5V under DC biasing conditions. Through modeling of CV and GV characteristics of MOSCAPs fabricated on GaSb substrate, D_{it} and trap response time were calculated as a function of the extent of traps into the oxide. With 1µs gate voltage pulsing, I_{ON} increased to 85µA/µm at V_{DS}=0.5V in hetJ pTFET. Further, even with 10µs gate voltage pulsing, I_{ON} as well as SS improved significantly compared to the DC bias conditions. RSM study on the InAs/GaSb hetero-junction layer revealed the presence of $GaAs_{0.022}Sb_{0.978}$ layer at the hetero-interface which could explain the presence of slow interface traps in the hetJ pTFET. Improvement in the device performance can be achieved through: (a) optimized MBE growth conditions to reduce the defects at the hetero-junction combined with reduction in body thickness which would translate to low I_{OFF} (b) low values of D_{it} to improve Fermi level movement efficiency and improve SS and (c) scaled EOT to improve I_{ON} as well as SS. In addition, density of state engineering would also be required in InAs/GaSb pTFET in order to realize TFET based complimentary logic.

Chapter 7

Understanding the Output Characteristics of III-V Tunneling Field Effect Transistors through Physics Based Analytical Modeling

I. Introduction

TFET drain current is strongly dependent on the electric field at the source-channel tunnel junction, set by the source doping density (N_S). Source doping affects the transfer and output characteristics of the TFETs. The impact of N_S on the transfer characteristics has been established previously using numerical simulations and analytical models [76][88][89]. However, its impact on the output characteristics and the drain current saturation has not been well understood. Both output and transfer characteristic ultimately determine the gain of a transistor, given by the ratio of transconductance to output conductance, which in turn affects the noise margin of TFET SRAM circuits [90].

In this chapter, the drain current saturation mechanism in $In_{0.53}Ga_{0.47}As$ homo-junction TFET is studied through physics based analytical models and TCAD simulations employing dynamic non-local tunneling models. It is shown that the drain current saturation mechanism is intrinsic to any TFET and fundamentally different from that of a long channel MOSFET. The analytical model developed does not rely on the empirical tunneling current equation which assumes a constant junction electric field [91][92], rather an exponentially decaying potential profile in the channel is assumed. Thus, tunneling current is calculated non-locally as a function of position along the tunneling path which is needed to accurately capture the output characteristics. The dependence of the drain current saturation voltage (V_{DSAT}) on the doping of the source region of TFET (N_s) is established using physics-based analytical model and confirmed by TCAD simulations. The dependence of source doping on the switching slope of the

device is investigated and shown that the choice of source doping in a III-V p-channel TFET requires tradeoff between maintaining steep switching and delayed saturation voltage which is of importance for complementary TFET logic.

II. Results and Discussions

Figure 7-1 shows the schematic of the ultra-thin body (UTB) double gate tunnel FET studied. For simplicity of explanation, $In_{0.53}Ga_{0.47}As$ homo-junction TFET is considered with body thickness of 7nm and electrical oxide thickness (EOT) of 1nm. Simulations of the TFET characteristics are carried out using Synopsis Sentaurus TCAD simulator. Dynamic non-local band to band tunneling model is used to compute the non-local tunneling transitions and hence the drain current [18][20].

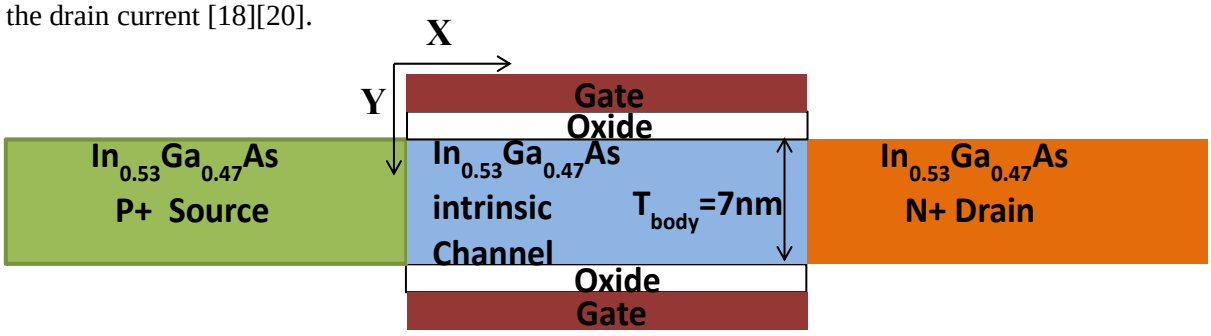

Figure 7-1. Schematic of ultra-thin body TFET used for the analytical model

Figure 7-2 (a-b) show the simulated output characteristics of the UTB MOSFET and TFET respectively at V_{GS} =0.5V and for two different source doping of N_s=5x10^{19} cm^{-3} and 6x10^{18}cm^{-3}. Saturation in the output characteristics of a FET typically occurs gradually over a range of V_{DS}. Hence for convenience, V_{DSAT} was defined to be the drain voltage needed to reach 95% of the peak current. It can be seen that the saturation characteristics of a MOSFET were unchanged by source doping. However, delayed drain current saturation and non-linear turn on was observed in the output characteristics of TFET for lower source doping. As the source doping was increased, the drain current saturation voltage (V_{DSAT}) is seen to reduce progressively as

shown in Figure 7-2 (c). The turn-on at low V_{DS} becomes linear at higher N_s. In order to explain the source doping dependence observed in the output characteristics, an understanding of the saturation mechanism in the homo-junction TFET is presented first.

The available energy window for tunneling between the valence band (VB) edge of the source and the conduction band (CB) edge of the channel is defined by ψ_s. As will be discussed later, ψ_s is controlled both by the gate-source and the drain-source potentials. The tunneling current density in a direct band gap homo-junction bulk or UTB TFET can be calculated based on the Wentzen-Krammel-Brillouin (WKB) model as [18][20]:

$$J_{ds} = \int_{\psi_s} \frac{g\pi}{36h} \int_0^l \left(\frac{dx}{k(x)}\right)^{-1} T1(E)T2(E) \left[\left(exp\left[\frac{\varepsilon - E_{F,n}(l)}{kT}\right] + 1\right)^{-1} - \left(exp\left[\frac{\varepsilon - E_{F,p}(0)}{kT}\right] + 1\right)^{-1}\right] dE \quad (7\text{-}1)$$

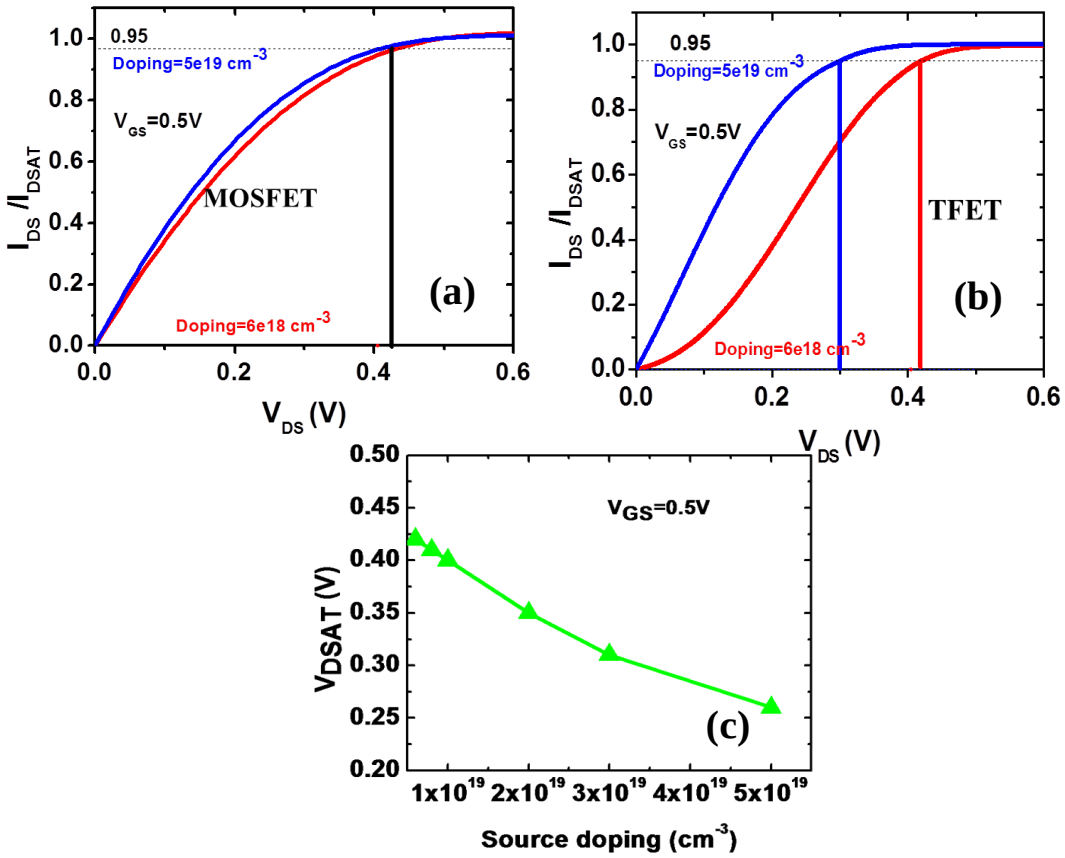

Figure 7-2. (a) Simulated output characteristics of $In_{0.53}Ga_{0.47}As$ MOSFET for two values of source doping (b) Simulated output characteristics of $In_{0.53}Ga_{0.47}As$ TFET for two values of source doping (c) V_{DSAT} of TFET as a function of source doping for a fixed V_{GS}.

$T1(E) = exp\left(-2\int_0^l k(x)dx\right)$ and $T2(E) = 1 - exp\left(-k_m^2 \int_0^l \frac{dx}{k(x)}\right)$ where, k(x) is the imaginary wave vector in the band gap, l is the length of the tunneling path from VB in the source to CB in the channel, E_{Fn} is the Fermi level in the channel, E_{Fs} is the Fermi level in the source. k_m is the maximum transverse (perpendicular) momentum determined by the maximum valence-band energy(ε_{max}) and minimum conduction band energy (ε_{max}) given by:

$k_m^2 = \min(k_{vm}^2, k_{cm}^2)$, $k_{vm}^2 = \frac{2m_v(\varepsilon_{max}-\varepsilon)}{\hbar^2}$, $k_{cm}^2 = \frac{2m_c(\varepsilon-\varepsilon_{min})}{\hbar^2}$

k_{vm} is the maximum transverse momentum in the VB and k_{cm} is the maximum perpendicular momentum in the CB. The perpendicular momentum needs to be conserved in the tunneling process and hence the transmission probability is reduced when k_m is higher [18][20]. Since the tunneling window is defined by ψ_s, it is important to know how the gate and the drain bias influence ψ_s. It has been shown previously that the gate to channel capacitance in a TFET(C_{GG}) is dominated by the gate to drain capacitance (C_{GD}) which leads to enhanced miller capacitance [93]. The enhanced miller capacitance is also found to affect the electrostatics of TFETs as discussed below.

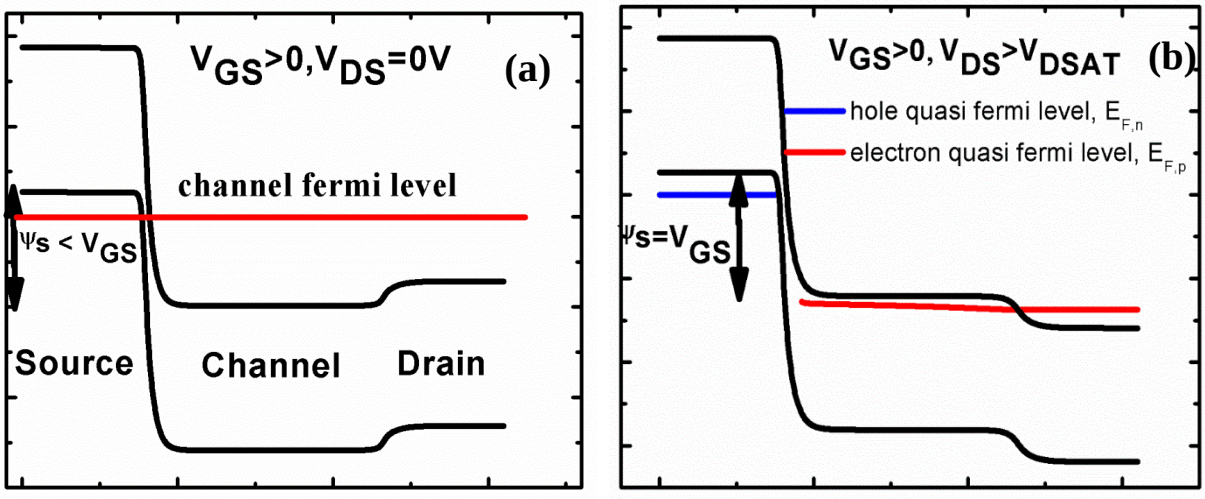

Figure 7-3. (a) Energy band diagram of TFET for V_{DS}=0V showing channel inversion. (b) Energy band diagram at high V_{DS} showing weak inversion of channel due to larger barrier for charge injection from the drain.

Figure 7-3 (a) shows the simulated energy band diagram of TFET for V_{GS}>0V and V_{DS}=0V. The channel is inverted due to injection of electrons from the drain. At higher drain bias (Figure 7-3 (b)), due to the large barrier for electrons from the drain into the channel, the net charge in the channel is low. Lower charge in the channel reduces the voltage drop across the oxide and the surface potential in the channel increases. Hence the surface potential in the channel is controlled not only by the V_{GS}, but also by V_{DS}. This is an intrinsic property of tunnel FETs and is not related to short channel effects. In MOSFETs on the other hand, under high drain bias, gate to source capacitance dominates and the channel is still under inversion due to carriers from the source and the energy barrier for mobile charge injection is controlled by gate alone [93]. Drain current saturation in a long channel MOSFET is due to pinch-off region that is developed near the drain.

The work function of the gate is chosen in such a way that at V_{GS}=0V the VB in the source and the CB in the channel are aligned. Hence ψ_s is also the surface potential in the channel and ψ_s=0V for V_{GS}=V_{DS}=0V. In order to obtain the tunneling window, the change in surface potential of the channel needs to be self consistently calculated as:

$$\psi_s(Q_{ch}) = V_{GS} - \frac{Q_{ch}}{2C_{ox}}, \tag{7-2}$$

$$Q_{ch} = N_c \int_0^{\infty} \frac{\varepsilon^{0.5} d\varepsilon}{1+exp(\varepsilon-\eta_F)}, \tag{7-3}$$

$$\eta_F = \left(\frac{E_{Fch}-E_{Cch}}{kT}\right). \tag{7-4}$$

where C_{ox} is the gate oxide capacitance, Q_{ch} is the net charge in the channel, N_c is the effective density of states of the channel material, E_{Fch} is the electron quasi- fermi level in the channel and E_{Cch} is the conduction band edge in the channel. The density of electrons generated in the channel due to tunneling is low compared to the drain injected electrons and is ignored in Equations 7-2 and 7-3 [93]. The applied drain bias drops across the tunnel junction and hence E_{Fch} remains flat in the channel and is moved by the amount of applied drain bias. However, beyond $V_{DSAT,}$ E_{Fch} is

not flat and V_{DS} drops across the channel (Figure 7-3(b)) . The maximum surface potential is set by the applied gate bias and it occurs when the channel is weakly inverted. Figure 7-4 shows ψ_s as a function of V_{DS} obtained from numerical TCAD simulations, as well as analytical model discussed in Equation 7-2 assuming a flat E_{Fch} in the channel, which are in excellent agreement with each other. Increasing V_{DS} increases the allowed energy window or the available Density of States for tunneling and hence the drain current increases. The drain current begins to saturate when the allowed energy window reaches the maximum value set by V_{GS}. For lower source doping, higher V_{DS} is needed to attain the maximum surface potential. The physical explanation for this mechanism is as follows: Under low V_{DS}, the channel is inverted due to injection of electrons from the drain. Thus a p-n junction like built-in potential is formed which is controlled by the source doping and the gate bias. Lower the built-in potential at V_{DS}=0V, higher is the drain bias needed to increase ψ_S to the maximum value of V_{GS} and TFET enter into saturation. Hence V_{DSAT} is strongly modulated by N_s and V_{GS}

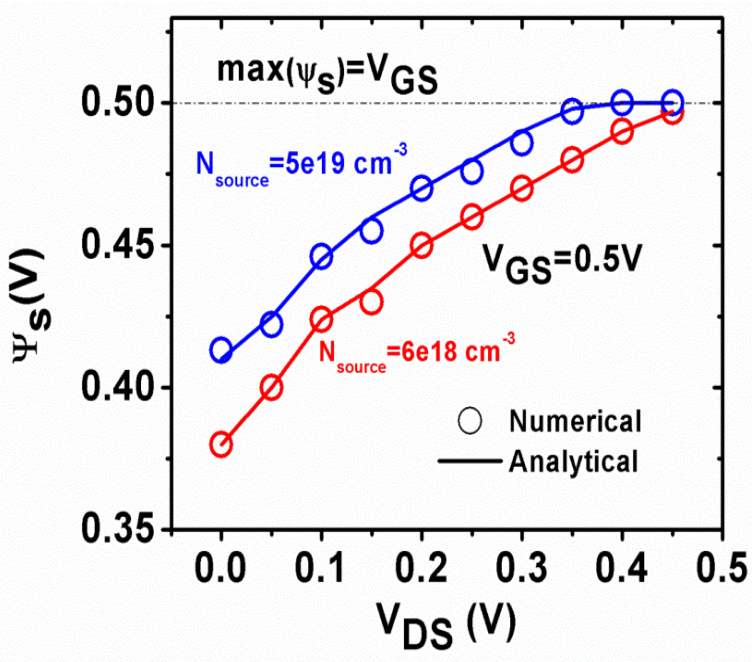

Figure 7-4. Simulated and modeled surface potential as function of VDS for two different source doping illustrates delayed saturation.

In order to further confirm the drain current saturation mechanism, the band to band tunneling current in TFET was calculated using Equation 7-1. An exponentially decaying potential profile ψ_{ch} in the channel is assumed given by: $\psi_{ch} = \left(\psi_s + \frac{E_g}{q}\right) e^{-x/\lambda}$, where E_g is the band-gap, λ is the electrostatic scaling length given by [92][94] $\lambda = \sqrt{\frac{\varepsilon_{ch} t_{body} t_{ox}}{2\varepsilon_{ox}}}$, ε_{ch} is the dielectric constant of the channel material, t_{body} is the body thickness, ε_{ox} is the dielectric constant of the oxide and t_{ox} is the oxide thickness.

Flietner's two band relation [95] is used to determine the imaginary wave vector through the tunneling trajectory as:

$$\frac{\hbar^2 k^2}{2m_r} = \frac{E\left(\frac{E}{E_g} - 1\right)}{\left(1 - \alpha + \alpha \frac{E^2}{{E_g}^2}\right)} \tag{7-5}$$

where m_r is the reduced effective mass given by ,$\frac{1}{m_r} = \frac{1}{m_c} + \frac{1}{m_v}$,m_c is the effective mass of electrons, m_v is the effective mass of holes and $\alpha = 1 - \sqrt{m_c/m_v}$.

Only light hole is considered since heavy hole and split off bands contribute to smaller tunneling probability [96]. The tunneling integrals are thus calculated as a function of energy (E) for the UTB TFET as:

$$2\int_0^l k(x)dx = \frac{2\lambda\pi\sqrt{2m_r}}{\hbar\sqrt{E_g}}\left[\frac{2\psi_s + Eg - 2E}{2} - \sqrt{\psi_s + Eg - E}\sqrt{\psi_s - E}\right] \tag{7-6}$$

$$\int_0^l \frac{dx}{k(x)} = \frac{\hbar\lambda\pi\sqrt{E_g}}{\sqrt{2m_r}\sqrt{\psi_s - E}\sqrt{\psi_s + E_g - E}} \tag{7-7}$$

Finally, the net drain current was calculated by integration over the cross section of the TFET as: $I_{ds} = \iint J_{ds} dA$. The potential in the transverse direction was assumed to be constant due to ultra-thin body dimensions and symmetric double gate. Figure 7-5 shows the comparison of simulated and modeled output characteristics. The peak current has been scaled (scaling factor is ~0.9 for high doping and ~0.1 for low doping) to match simulations. Deviations in the peak

current calculated from the analytical model from TCAD simulations could be attributed to: (a) Ignoring the depletion region in the source (b) Assumption of uniform current density throughout the body (c) approximating $m_c=m_v$ ($\alpha=1$) . Nevertheless, the model captures the delayed saturation as well as non-linear turn on phenomena observed with TFETs.

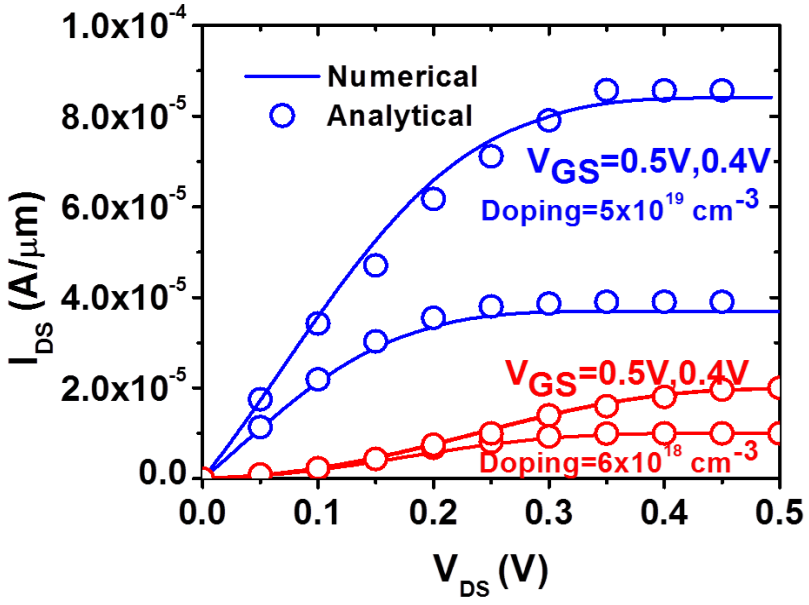

Figure 7-5. Modeled output characteristics match TCAD simulations and captures output saturation and non-linear turn on.

Figure 7-6 (a) shows the different components of transmission probability calculated analytically as a function of energy. It should be noted that the factor T1 itself does not result in the non-linear turn on characteristics of TFETs as reported in a recent work [97]. In fact, it is the component of transmission probability due to the perpendicular momentum (T2) that results in overall transmission probability to decay towards the band edges (CB in the channel and VB in the source). In the output characteristics this results in low currents for low V_{DS} when the transmission probability is decreased due to the higher magnitude of perpendicular momentum (Figure 7-6 (b)). Assuming a constant ψ_s for low and high source doping values, it can be seen from Figure 7-6 (b) that for higher source doping, TFET operates at higher transmission

probability for the same energy window and hence the output characteristic is a linear function. The effect of perpendicular momentum in the transfer characteristics, on the other hand, is to reduce the overall tunneling probability and hence is usually modeled using an increase in the effective bandgap [98].

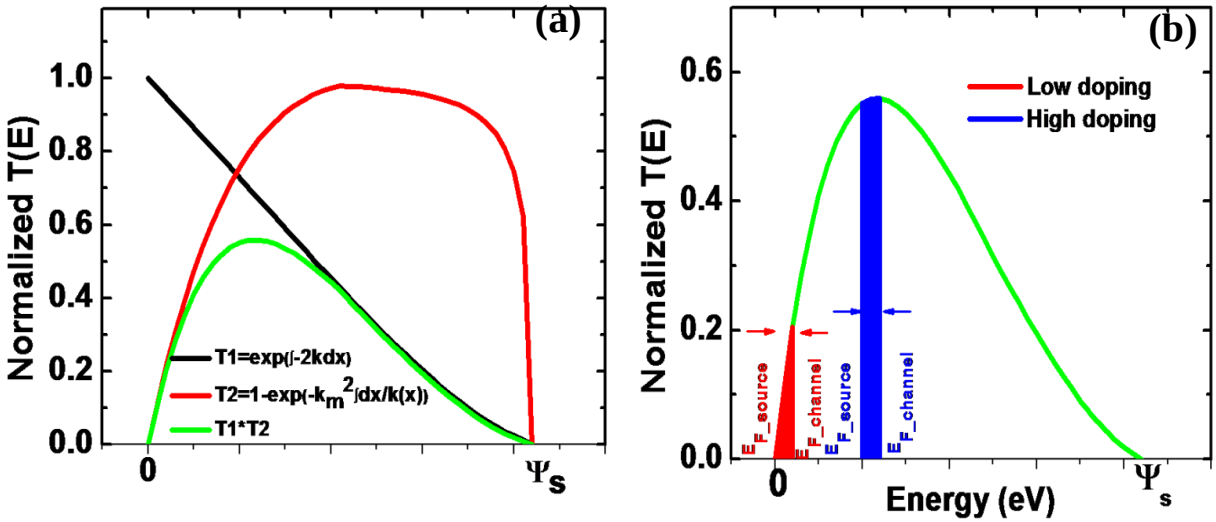

Figure 7-6. (a) Impact of perpendicular momentum is to reduce the overall transmission probability towards the band edges. (b) Shaded region indicates the energy range which participates in tunneling under low V_{DS} for two source doping values.

High values of source doping are desired in TFET to reduce source depletion and improve the drive current (Figure 7-7 (a)). However, in the case of a pchannel TFET, due to the low density of states in the conduction band, the source is significantly degenerate which can result in to dilution of the expected steep switching slope (SS) (Figure 7-7(a)). Thus for III-V p-TFETs additional constraint on delayed saturation needs to be addressed due to tradeoff between the V_{DSAT} and SS (Figure 7-7 (b)). However, this tradeoff is not seen strongly in n-channel TFETs because the Fermi level has lower sensitivity to source doping arising from the higher effective mass for holes compared to electrons. The impact of delayed saturation is to degrade the voltage transfer characteristics of inverter based on TFETs which in turn translates to poor noise margins

of TFET based SRAMS [4]. Exploring strain and orientation engineering to boost the conduction band of pTFETs is a possible solution to circumvent this problem.

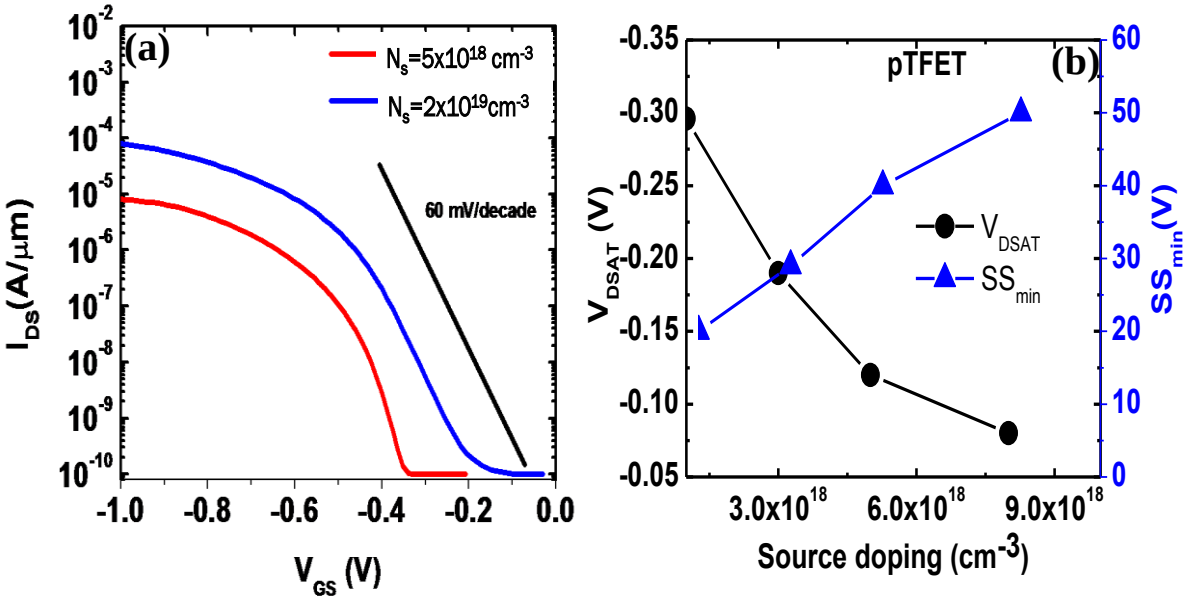

Figure 7-7. (a) Simulated transfer characteristics of pTFET which show dependence of SS on the source doping. (b) Lower doping results in steeper switching slope but also results in delayed output saturation.

III. Conclusions

In this chapter, analytical model was presented which accurately captures the output characteristics of a III-V TFET. The output characteristic of a III-V TFET exhibits source doping dependence. Lower source doping results in delayed saturation as well as non-linear turn on behavior in the output characteristics. Further, due to low density of states effective mass for electrons in source for pchannel TFETs, there is a trade-off between delayed saturation in the output characteristics and the minimum SS achievable.

Chapter 8

Summary and Future Work

The primary goal of this dissertation has been to investigate the feasibility of III-V TFETs for low power logic and RF applications. In chapter 2, it is shown that in-situ plasma cleaning is very critical in passivation of the InGaAs surface prior to gate oxide deposition. Further, it is also shown that gate metal deposition technique also plays a very crucial role in realizing high quality oxide/semiconductor interface. Using in-situ nitrogen plasma cleaning and thermally evaporated Nickel gate metal, a minimum switching slope of 97mV/decade is demonstrated in $In_{0.65}Ga_{0.35}As/GaAs_{0.4}Sb_{0.6}$ heterojunction TFET. Using fast IV measurements, trap response is reduced and a minimum switching slope of 64mV/decade is realized which is one of the lowest reported in the category of III-V TFETs. In chapter 3, tunnel barrier engineered $In_{0.9}Ga_{0.1}As/GaAs_{0.18}Sb_{0.82}$ is demonstrated with record high drive current in the category of TFETs. A novel planarization scheme is also developed which allows implementation of co-planar waveguide structure in a vertical transistor. Thus, high frequency switching characteristics of TFET is experimentally demonstrated for the first time with the cut-off frequency in the gigahertz range. Further, barrier engineering also provides added benefit in terms of reducing low frequency noise magnitude, as discussed in chapter4. For logic applications, a p-channel TFET is also required together with n-channel TFET. The main roadblock for realizing high performance p-channel TFET is integration of high quality dielectric on the antimonide channel. In this regard, it is shown in chapter 5 that a low temperature atomic layer deposition process is preferable for antimonide channel transistors. InAs/GaSb p-channel TFET with this gate stack is demonstrated and a drive current of 85μA/μm achieved, which is highest in the category of III-V p-channel TFET. In chapter 7, source doping dependent output characteristics of III-V TFET is explained

based on analytical models. Source degeneracy issue in p-channel TFET affects the switching slope as well as output characteristics.

I. Realizing Ultra-thin Body Dimension in TFET

The self-aligned gate nano-pillar process flow used for TFET fabrication in this dissertation does not allow for reduction in the body dimensions to the sub-50nm regime mainly due to the following reasons: (1) Etch mask comprising of Titanium (30nm) and Chromium (60nm) is deposited using a lift-off process. Lift-off process is not very effective in realizing sub-100nm dimensions, especially if the metal stack is thick (greater than 30nm). (2) Significant sidewall is formed during etching of the 300nm thick Molybdenum layer itself. As a result, the effective dimension of the etch mask for etching the active device region is much larger. (3) Formation of significant sidewall during the etch process of the active device region which leads to increase in the body dimension.

Figure 8-1 shows the schematic of the proposed process flow to realize ultra-thin body dimensions in vertical TFET. The process flow starts with formation of etch mask on the bare wafer. A negative electron-beam lithography resist hydrogen silsesquioxane (HSQ) will be used as the etch mask. HSQ is a high resolution e-beam resist and once exposed to the e-beam, it is similar to SiO_2 and hence can be used as an etch mask. It also has very low line edge roughness. Next, the active region of the wafer is etched using HSQ as etch mask to form MESA. It has been shown that when the substrate is heated, the etch rate increases, sidewall roughness decreases and also more verticality is achieved [99]. Hence, during the dry etch, substrate needs to be heated. Followed by etch, high-κ dielectric is deposited using atomic layer deposition followed by conformal deposition of the gate metal using sputtering process. Next, inter-layer dielectric (ILD) is spin coated and then etched back. Gate metal and high-κ dielectric is then etched off using dry

etch process. ILD is again spin coated and then etched back appropriately so that the top contact does not short with the gate metal. Finally, top contact is patterned using e-beam lithography and then deposited using e-beam evaporation.

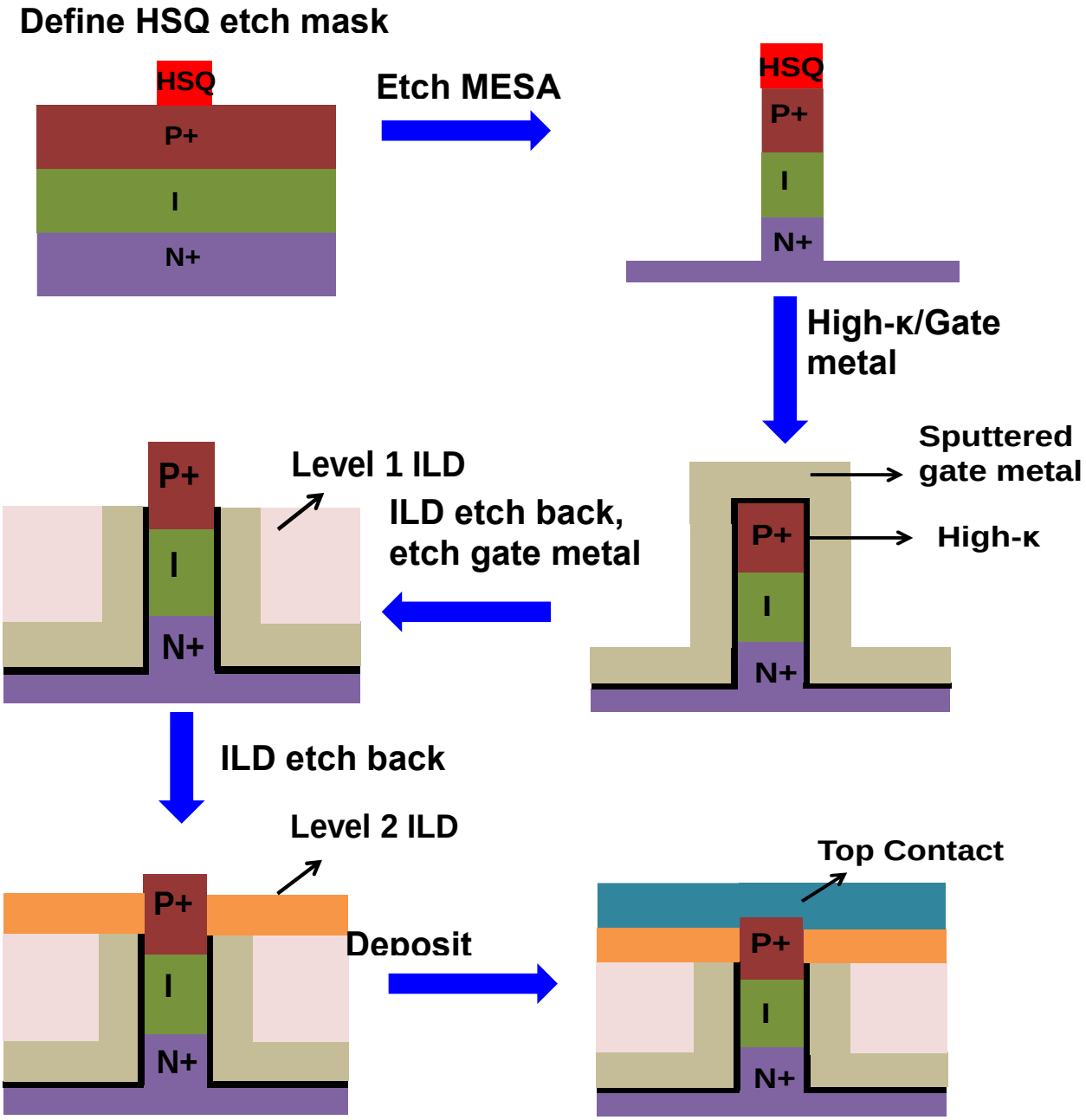

Figure 8-1. Schematic of the proposed process flow to scale the TFET body dimension.

II. Experimental Demonstration of TFET Based Rectifier

RF energy scavenged from sources such as TV stations, cell phone stations and wifi is being widely being to power wireless sensor networks, RFIDs, implantable biomedical devices. In such systems the RF signal is converted to DC voltage using rectifier circuits. Rectification is challenging if the input power level is very low. Low turn on voltage is an important attribute of rectifier circuits. Hence, TFET based rectifier circuits are of interest due to its steep switching slope [100]. Further, unlike in a MOSFET, TFET exhibits unidirectional conduction which would reduce the reverse leakage loss from the sinusoid input [100]. Furthermore, it is demonstrated in chapter 3 that TFET can operate in gigahertz frequency range.

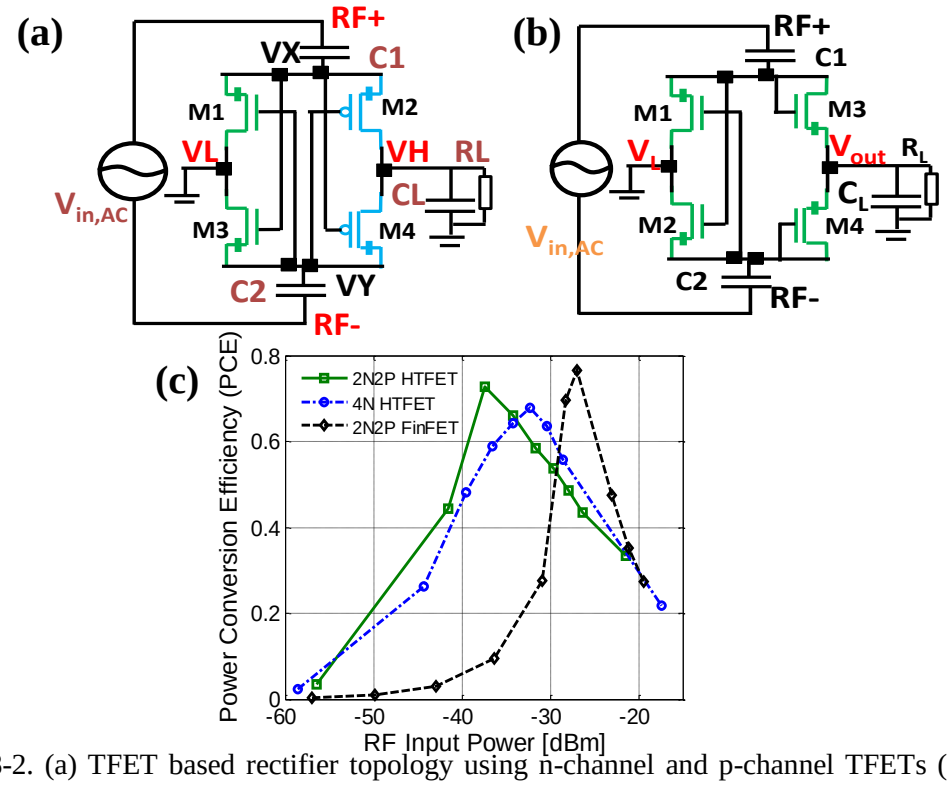

Figure 8-2. (a) TFET based rectifier topology using n-channel and p-channel TFETs (b) TFET based rectifier topology using only n-channel TFETs. (c) Simulated power conversion efficiency shows advantage of TFET over FINFET [100].

An important figure of merit for the rectifier circuits is the power conversion efficiency defined as the ratio of output DC power to the input RF power. Figure 8-3 (a) shows the rectifier circuit topology based on n-channel and p-channel InAs/GaSb heterojunction TFET (HTFET). Figure 8-3 (b) shows the rectifier circuit topology based on n-channel TFET alone. Simulation carried out assuming load capacitance of 1pF, load resistance of 100k and for an input signal of frequency 915 MHz is shown in Figure 8-3 (c). It is clear that TFET based rectifier exhibits significant advantage over FINFET based rectifier in terms of achieving higher power conversion efficiency at lower RF input power. Hence, experimental demonstration of operation of the rectifier circuit and benchmarking its efficiency against CMOS based rectifier circuit is of enormous interest to the research community. In this regard, Figure 8-4 below shows the physical layout of the TFET based rectifier circuit designed to facilitate fabrication of wafer level rectifier circuit. The planarization scheme described in chapter 3 makes it possible to fabricate such a circuit at a wafer level requiring interconnections between different terminals of the vertical TFET.

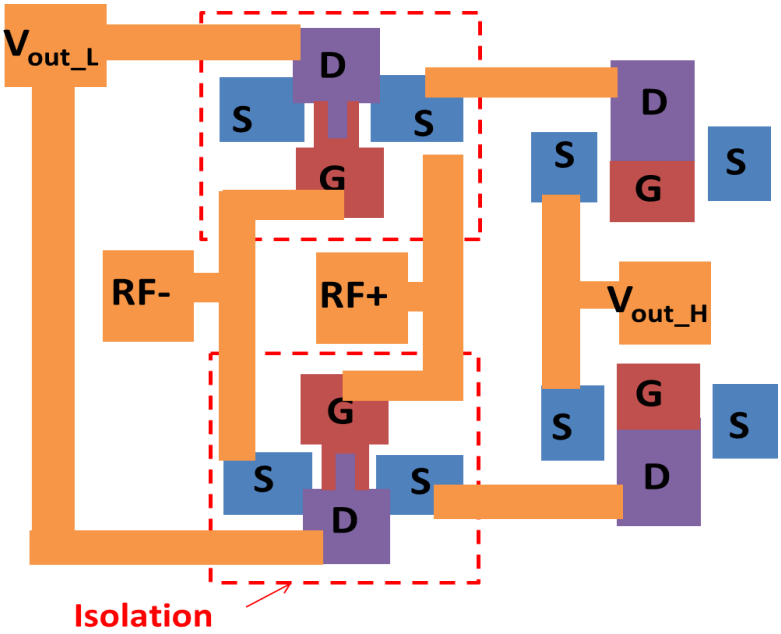

Figure 8-3. Physical layout of the TFET based rectifier for device level experimental demonstration. .

Appendix: Fabrication Process Flow for TFET with GSG Pads

The fabrication details are explained in detail below.

1. Alignment Markers and Dry Etch Mask Definition

- Degrease the III-V sample with Acetone (10mins), Methanol (5mins) and IPA (5mins).
- Rinse with DI water for 1min and blow dry with N_2.
- Spin coat with MMA EL-6 resist at 2000 rpm for 1min.
- Bake at150^{o}C for 3min. Cool the sample for 2mins.
- Spin coat PMMA 950 A3 resist at 4000 rpm for 45secs.
- Bake @ 180^{o}C for 3 mins. Cool the sample for 2 mins.
- Use E-beam lithography (EBL) to write the features. Write features smaller than equal to 5x5μm^2 at dose of 900μC/cm^2 with beam size of 15nm. Write larger features with 420μC/cm^2 using beam size of 120nm.
- Develop the patterns using 1:3 MIBK: IPA for 1min and 30 secs, 1:1 MIBK: IPA for 20 secs followed by 10 secs dip in IPA.
- Rinse in DI water for 30secs and blow dry with N_2.
- Observe for clean and sharp patterns.

2. Dry Etch Mask Deposition

In this step, pillar hard etch mask will be defined using EBL and Lift-off technique.

- Load the developed sample into the evaporator.
- Load Ti and Cr crucibles and wait for vacuum.
- Start depositing once the base pressure comes below 10^{-6} Torr.
- Lift-off the patterns using Remover PG preheated to 60^{o}C.

- Rinse in IPA, DI water and then blow dry with N_2.
- Observe under microscope for a clean lift-off.

3. Pillar Definition Using Dry Etch

In this step, pillars will be defined using Ti/Cr as the hard etch mask.

- Paste the sample on a carrier wafer using double sided thermal tape.
- Clean the back of the carrier wafer before loading into the ICP RIE chamber.
- Load and wait for the lock vacuum to reach below 100mTorr.
- Before running the actual sample for etch, perform chamber clean followed by chamber conditioning with Ar (20sccm) and SF_6 (40sccm). RF1 PWR-125W, RF2 PWR-120W.
- Etch Molybdenum using the same recipe for 400s.
- Perform chamber conditioning with Ar (20sccm), BCl_3(40sccm) and SF_6(10sccm). RF1 PWR-125W, RF2 PWR-500W.
- Etch III-V using the same recipe till bottom P+ source is reached.
- Use Profilometer to verify the total height of the pillar.

4. Pillar Wet Etch Undercut and high-κ Deposition

In this step, wet etch is performed to remove dry etch damage and produce the undercut needed for self-aligned gate contact deposition.

- Rinse the dry etched sample with DI water to remove any residue.
- Create citric acid (100gm+100ml DI water stirred for 40mins) and H_2O_2 solution with 20:1 ratio. Store for 15mins.
- Etch the sample for 1 min to produce undercut in InGaAs of around 50nm.
- Rinse with DI water and blow dry with N_2.
- Dip in 1:10 HCl:DI water solution for 2 minutes and blow dry with N_2.

- Load the sample immediately into a preconditioned ALD chamber with the hot plate maintained at 250^{o}C.
- Close the lid immediately and bring down the pressure to 0.2Torr.
- Wait for 1 min.
- Treat the surface with 5 Cycles of TMA.
- Pulse 10 cycles of TMA and H_2O to deposit 1nm of Al_2O_3.
- Pulse 35 cycles of TEMAH and H_2O in top to deposit 3.5nm of HfO_2.
- Unload the sample and then cool down for 1min.

5. Self-aligned Gate Contact Definition and Deposition

In this step, Pd gate metal is deposited vertically using EBL, evaporation and lift-off technique.

- Spin coat with MMA EL-11 resist at 4000 rpm for 45secs.
- Bake at 150^{o}C for 3min. Cool the sample for 2mins.
- Spin coat PMMA 950 A3 resist at 4000 rpm for 45secs.
- Bake at 180^{o}C for 3 mins. Cool the sample for 2 mins.
- Use EBL to write the features. Write larger features with 420μC/cm^2 using beam size of 120nm.
- Develop the patterns using 1:3 MIBK: IPA for 1min and 30 secs, 1:1 MIBK: IPA for 20 secs followed by 10 secs dip in IPA.
- Rinse in DI water for 30secs and blow dry with N_2.
- Observe for clean and sharp patterns.
- Load into the evaporator and wait for pressure to reach below 10^{-6}Torr
- Deposit 20nm Pd gate metal.

- Lift-off with Remover PG preheated at 60^{o}C, rinse with IPA and DI water.
- Blow dry and observe under microscope for a clean lift-off.

6. Source and Gate Pad Definition and Deposition

In this step, source and gate pad windows are created. High-κ is removed and the pads are formed using EBL, evaporation and Lift-off techniques.

- Spin coat with MMA EL-11 resist at 4000 rpm for 45secs.
- Bake at 150^{o}C for 3min. Cool the sample for 2mins.
- Spin coat PMMA 950 A3 resist at 4000 rpm for 45secs.
- Bake at 180^{o}C for 3 mins. Cool the sample for 2 mins.
- Use EBL to write the features. Write larger features with 420μC/cm^{2} using beam size of 120nm.
- Develop the patterns using 1:3 MIBK: IPA for 1min and 30 secs, 1:1 MIBK: IPA for 20 secs followed by 10 secs dip in IPA.
- Rinse in DI water for 30secs and blow dry with N_2.
- Observe for clean and sharp patterns.
- Dry etch the high-k in ICP RIE using BCl3 (10sccm) and Ar (40 sccm): RF1 PWR: 75W and RF2 PWR: 500W, Time: 25secs
- Load into the evaporator with Ti, Pd and Au crucibles
- Wait for pressure to reach below 10^{-6} Torr
- Deposit 20nm Ti, 20nm Pd and 30nm Au.
- Lift-off the metal with remover PG preheated at 60^{o}C
- Rinse in IPA and DI water and then blow dry with N_2.
- Observe under microscope for clean lift-off.

7. Planarization and Etch Back

In this step, the pillars are planarized using BCB and the BCB is etched back till the top of Mo contact for the top contact formation.

- Spin Coat BCB at 5000rpm for 1min.
- Bake at 140^{o}C for 10mins.
- Load into an oven with N_2 ambient while the hot plate is preset to 140^{o}C.
- Gradually raise the temperature from 140^{o}C to 250^{o}C.
- Cure BCB at 250^{o}C for 1 hr.
- Unload the cured sample once the temperature is below 150^{o}C.
- Cool the sample and load into the RIE chamber.
- Etch BCB in O_2 (80sccm) and CF_4 (20sccm), Pressure 200mT, RF-200W (Capactively coupled RIE).
- Etch in steps until the BCB is below the pillar surface by 200nm. Check the height with Profilometer and or SEM.

8. Drain Pad Definition and Deposition

In this step, drain pads are formed in contact with the Mo on top of the pillars. EBL, E-beam evaporation and Lift-off technique is used.

- Spin coat with MMA EL-11 resist at 4000 rpm for 45secs.
- Bake at 150^{o}C for 3min. Cool the sample for 2mins.
- Spin coat PMMA 950 A3 resist at 4000 rpm for 45secs.
- Bake at 180^{o}C for 3 mins. Cool the sample for 2 mins.
- Use EBL to write the features. Write larger features with 420μC/cm^2 using beam size of 120nm.

- Develop the patterns using 1:3 MIBK: IPA for 1min and 30 secs, 1:1 MIBK: IPA for 20 secs followed by 10 secs dip in IPA.
- Rinse in DI water for 30secs and blow dry with N_2.
- Observe for clean and sharp patterns.
- Remove O_2 plasma induced native oxide with high-κ etch recipe for 25 secs.
- Load into the evaporator with Ti, Pd and Au crucibles.
- Wait for the pressure to reach below 10^{-6} Torr.
- Deposit 20nm Ti, 20nm Pd and 60nm Au.
- Lift-off in Remover PG preheated at 60^{o}C.
- Rinse in IPA and DI water.
- Blow dry with N_2 and observe under microscope for a clean lift-off.

9. VIA Definition and Formation

In this step, VIA is created through BCB using Al as etch mask.

- Load into the evaporator with Al crucible.
- Spin coat with MMA EL-11 resist at 4000 rpm for 45secs.
- Bake at 150^{o}C for 3min. Cool the sample for 2mins.
- Spin coat PMMA 950 A3 resist at 4000 rpm for 45secs.
- Bake at 180^{o}C for 3 mins. Cool the sample for 2 mins.
- Use EBL to write the features. Write larger features with 420μC/cm^2 using beam size of 120nm.
- Develop the patterns using 1:3 MIBK: IPA for 1min and 30 secs, 1:1 MIBK: IPA for 20 secs followed by 10 secs dip in IPA.
- Dry etch the Al in ICP RIE using Cl_2 (30sccm) , BCl_3 (30sccm) and Ar (10 sccm): RF1 PWR: 50W and RF2 PWR: 600W, Time: 30secs

- Etch BCB in O_2 (80sccm) and CF_4 (20sccm), Pressure 200mT, RF-200W (Capactively coupled RIE) for 120secs.
- Dry etch the remaining Al in ICP RIE using Cl2 (30sccm) , BCl3 (30sccm) and Ar (10 sccm): RF1 PWR: 50W and RF2 PWR: 600W, Time: 30secs.

10. GSG Pad Definition and Deposition

- Spin coat with MMA EL-11 resist at 4000 rpm for 45secs.
- Bake at 150^{o}C for 3min. Cool the sample for 2mins.
- Spin coat PMMA 950 A3 resist at 4000 rpm for 45secs.
- Bake at 180^{o}C for 3 mins. Cool the sample for 2 mins.
- Use EBL to write the features. Write larger features with 420μC/cm^2 using beam size of 120nm.
- Develop the patterns using 1:3 MIBK: IPA for 1min and 30 secs, 1:1 MIBK: IPA for 20 secs followed by 10 secs dip in IPA.
- Load into the evaporator with Ti, Pd and Au crucibles.
- Wait for pressure to reach below 10^{-6} Torr.
- Deposit 20nm Ti, 20nm Pd and 60nm Au.
- Lift-off the metal with remover PG preheated at 60^{o}C.
- Rinse in IPA and DI water and then blow dry with N_2.
- Observe under microscope for clean lift-off.

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VITA

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Bijesh Rajamohanan was born in the small town of Kothamangalam in the State of Kerala, India, to Late V. K. Rajamohanan Nair and Lathika Rajamohanan. He did his schooling from Vimalagiri Public School, Kothamangalam. He received his B.S. degree in Electronics and Communication Engineering from the National Institute of Technology Calicut, India, in 2007. From 2007 to 2008, he worked in Cypress Semiconductors, Bangalore, India, as a product engineer. He went to pursue M.S. degree at the Indian Institute of Technology Bombay, India. He received his M.S. degree from the department of Electrical Engineering in 2010. In the fall of 2010, he joined the research group of Prof Suman Datta at Pennsylvania State University where he worked towards his doctorate degree. He received the Ph.D. degree from the Department of Electrical Engineering at Penn State. After his Ph.D., he will be joining SanDisk Corporation where he will be working as a Senior Device Engineer in the Intelligent Memory Systems group in San Jose, California.

During his PhD, he published 7 journal and 7 conference papers with 7 first author publications among them. He was awarded the Melvin P. Bloom Outstanding Doctoral Research Award in Electrical Engineering. The award recognizes outstanding achievement in scholarship and professional accomplishment, and he was honored to be one of the two graduate students within the Electrical Engineering Department at Penn State to receive the award He can be contacted at his email *123.biju@gmail.com*.