CLASSICAL AND COULOMB BLOCKADE III-V MULTI-GATE QUANTUM WELL FIELD EFFECT TRANSISTORS FOR ULTRA LOW POWER LOGIC APPLICATIONS

A Dissertation in
Electrical Engineering
by
Lu Liu

© 2014 Lu Liu

Submitted in Partial Fulfillment of the Requirements for the Degree of

Doctor of Philosophy

May 2014
The dissertation of Lu Liu was reviewed and approved* by the following:

Suman Datta  
Professor of Electrical Engineering  
Dissertation Advisor  
Chair of Committee

Theresa Mayer  
Professor of Electrical Engineering

Jerzy Ruzyllo  
Professor of Electrical Engineering

Vijaykrishnan Narayanan  
Professor of Computer Science and Engineering

Nitin Samarth  
Professor of Physics

Kultegin Aydin  
Professor of Electrical Engineering  
Head of the Department of Electrical Engineering

*Signatures are on file in the Graduate School
ABSTRACT

Low power logic application requires aggressive scaling of supply voltage while maintaining performance. Recently, III-V material systems such as InGaAs and InSb have attracted lots of research interest as a substitute for silicon for future semiconductor industry. The In$_{0.7}$Ga$_{0.3}$As quantum well system is a good n-channel candidate for sub-500mV low power logic application due to their superior electron mobility. On the other hand, aggressive device scaling, into few electron operation regime, provides new opportunity to explore Coulomb oscillation to implement logic in a suitable binary decision diagram (BDD) logic architecture, enabling sub-300mV logic application.

This dissertation focuses on the experimental design, fabrication and characterization of classical and Coulomb blockade multi-gate quantum well field effect transistor (MuQFET), as well as the lead zirconium titanate ferroelectric integration to realize non-volatile operation. Based on comprehensive understanding of measurement results and device modeling, the following key accomplishments are discussed: (1) quasi-ballistic transport in short channel In$_{0.7}$Ga$_{0.3}$As MuQFETs; (2) multi-functional programmable MuQFETs showing short, Coulomb blockade and open mode for reconfigurable BDD logic in the few electron regime near scaling limit; (3) non-volatile ferroelectric gate stack exhibiting more than 40 minutes retention for short, Coulomb blockade and open mode. These features provide the opportunity of implementing low power logic using reconfigurable non-volatile BDD hexagonal fabrics combining with appropriate sensing circuit between BDD stages.
# TABLE OF CONTENTS

List of Figures ........................................................................................................... vi
List of Tables .............................................................................................................. xi
Acknowledgements .................................................................................................... xii

Chapter 1 Introduction ............................................................................................... 1
  1.1 Motivation ........................................................................................................... 1
  1.2 Non-Planar In$_{0.7}$Ga$_{0.3}$As MuQFET for Low Power Logic ......................... 2
  1.3 Further Device Scaling: Approaching Theoretical Minimum Switching Energy ................................................................. 4
  1.4 Coulomb Blockade In$_{0.7}$Ga$_{0.3}$As MuQFET ................................................. 5
  1.5 Organization of This Dissertation .................................................................. 6

Chapter 2 Quasi-Ballistic Classical In$_{0.7}$Ga$_{0.3}$As MuQFET ................................... 7
  2.1 Device Fabrication Process ............................................................................. 7
  2.2 Electrical Characterization and Transport Analysis ........................................ 9
  2.3 Scalability Study of In$_{0.7}$Ga$_{0.3}$As MuQFET .............................................. 14
  2.4 TCAD Simulation ............................................................................................ 17
  2.5 CV/I Delay Metric Benchmark ..................................................................... 18

Chapter 3 Coulomb Blockade MuQFETs for Binary Decision Diagram Logic ............ 20
  3.1 Manipulation of 0D Few Electron Island ....................................................... 20
  3.2 Basic Physics of Coulomb Blockade .............................................................. 22
  3.3 Circuit-Device Co-Design for Reconfigurable Binary Decision Diagram (BDD) Logic .............................................................................. 26
  3.4 Fabrication, Characterization and Simulation of Coulomb Blockade In$_{0.7}$Ga$_{0.3}$As MuQFETs ................................................................. 31
  3.5 Device Scaling and Improvement of Coulomb Blockade Temperature .......... 40
  3.6 Path Switching Efficiency of BDD Node ....................................................... 47

Chapter 4 Non-Volatile and Reconfigurable MuQFETs ........................................... 51
  4.1 Non-Volatile MuQFETs Structure Design ..................................................... 51
  4.2 Characterization of Sputtered Lead Zirconium Titanate (PZT) Film .............. 52
  4.3 Fabrication of Ferroelectric MuQFETs ........................................................... 60
  4.4 Electrical Characterization and Retention Time Measurement of Ferroelectric MuQFETs ............................................................................... 63

Chapter 5 Ultra Low Power Sensing For Cascaded BDD Stages ............................... 73
  5.1 Overview of Hybrid BDD Logic Circuit ....................................................... 73
5.2 Traditional Sense Amplifier and Energy-Delay Benchmark of Hybrid BDD Circuit
............................................................74
5.3 Possible Low Power Sensing Using Stochastic Resonance ......................77
Appendix A Device Fabrication Process Recipe ........................................85
Appendix B Tools Used for Device Fabrications ........................................89
Appendix C Nextnano Code for 2D Self-Consistent Poisson-Schrodinger Simulation ..............................................................90
Bibliography ..........................................................................................99
LIST OF FIGURES

Figure 1-1 Illustrations of advances in electrostatics, materials, strain engineering and computing paradigms with semiconductor device scaling. The technologies introduced in this dissertation are highlighted with blue box. ........................................2

Figure 1-2 (a) Epitaxial layer structure for In$_{0.7}$Ga$_{0.3}$As MuQFET, and simulated energy band diagram (b) and electron density profile (c). .................................................................3

Figure 1-3 (a) schematic of classical III-V MuQFET; (b) $I_D$-$V_G$ characteristic comparison of MuQFET with silicon FINFET.................................................................4

Figure 1-4 Switching energy and operational electron number scaling are plotted in silicon n-MOSFET. The scaling curve of III-V transistors is steeper than that of silicon transistors due to lower density of states. .................................................................5

Figure 1-5 Schematic of non-classical (NC) III-V MuQFET; (b) $I_D$-$V_G$ characteristics of III-V NC-MuQFET exhibiting Coulomb oscillations at T=300K. ..................................................6

Figure 2-1 In$_{0.7}$Ga$_{0.3}$As MuQFET fabrication process. ................................................................................8

Figure 2-2 (a) Tilted scanning electron microscope image (false colored) and (b) schematic of a single fin classical MuQFET............................................................................................................9

Figure 2-3 Cross-section layer structure and SEM image of MuQFET after focused ion beam cut. .................................................................................................................................9

Figure 2-4 (a) $I_D$-$V_G$ transfer characteristic of MuQFET with $L_G$=100nm; (b) subthreshold swing (SS) is plotted as a function of gate length for different fin width. .........................10

Figure 2-5 (a) source to drain total resistance as function of gate length. The cross point gives the external resistance; (b) components analysis of total resistance.....................12

Figure 2-6 From multi-fin long channel MuQFET, high-frequency C-V measurement (background subtracted) gives out the channel carrier density ($W$=40nm). .........................12

Figure 2-7 Experimentally extracted mobility as a function of channel electron density in In$_{0.7}$Ga$_{0.3}$As MuQFET ($W$=40nm)..................................................................................13

Figure 2-8 Room temperature effective mobility reduces when scaling gate length, indicating quasi-ballistic transport for short channel In$_{0.7}$Ga$_{0.3}$As MuQFET. .........................13

Figure 2-9 $V_{normx}$ versus $x/L_G$ for long channel and short channel assuming heavy doped source/drain at $V_S$=$V_D$=0, $V_G$=-1V. The source/drain field becomes dominating in determining channel potential as $L_G$ is comparable with electrostatic scaling length in short channel.................................................................15

Figure 2-10 $V_{normx}$ profile for transistor structure 1-5 listed in Table 2-1........................................16
Figure 2-11 Simulated and measured transfer characteristics. The red curve indicates potential improvement due to process optimization to external resistance and interface trap density.

Figure 2-12 CV/I delay metrics for In$_{0.7}$Ga$_{0.3}$As MuQFETs and silicon transistors.

Figure 3-1(a) A schematic of single electron transistor fabricated by bottom-up approach. The nanoparticle is chemically synthesized and assembled to electrodes on chip. (b) A schematic of single electron transistor confined by e-beam lithography defined Schottky electrodes on AlGaAs/GaAs 2DEG.

Figure 3-2 (a) basic construct of a single electron transistor; (b) energy diagram for a SET in blockade state; (c) energy diagram for a SET in transmitting state; (d) I$_D$-V$_G$ characteristic of a SET.

Figure 3-3(a) The source/drain Fermi level is closer to filled state. Finite V$_D$ brings down the drain Fermi level and align with one filled state in the nanodot causing electron transmission. (b) The source/drain Fermi level is closer to the unfilled state. Finite V$_D$ lowers the chemical potential in the nanodot due to capacitive coupling effect. The blockaded transport disappears when the unfilled state align with source Fermi level. (c) Schematic of Coulomb diamond. The red and blue edges correspond to the scenarios described in (a) and (b) respectively.

Figure 3-4 A single electron transistor inverter voltage transfer characteristics (VTC) for gate coupling ratio 0.4.

Figure 3-5 A schematic of an XOR BDD circuit. Each decision node is a Y junction consisting two Coulomb blockade transistors with opposite logic input.

Figure 3-6 Comparison of various device configurations of few electron transistors.

Figure 3-7 (a) A decision node consisting of two reconfigurable SETs at each path. The transistor can be programmed to execute logic functionality in the active Coulomb blockade mode, as well as act as the open or short path. (b) A 2D reconfigurable hexagonal fabric consisting of programmable devices (programming lines and inactive logic input lines to open and short path are not drawn). In this figure, A $\oplus$ B and A+B are demonstrated in the same fabric.

Figure 3-8 (a) Schematic of Coulomb blockade MuQFET fabrication with split gate and control gate. (b) Schematic of fabricated Coulomb blockade MuQFET. (c) Scanning electron microscope image of a Coulomb blockade MuQFET.

Figure 3-9 Classical I$_D$-V$_G$ measurement of Coulomb blockade MuQFET showing robust modulation from split gate and control gate voltage at 77K.

Figure 3-10 I$_D$-V$_{CG}$ characteristic for three different operation modes in logarithmic and linear scale (T=4K).
Figure 3-11 Self-consistent Poisson-Schrodinger simulation of electron density in the MuQFET working in short, Coulomb blockade and open mode (T=4K).

Figure 3-12 Self-consistent Poisson-Schrodinger simulation of conduction band profile in the MuQFET working in short, Coulomb blockade and open mode (T=4K).

Figure 3-13 Stability plot of MuQFET operating in Coulomb blockade mode at 4.2K. The extracted parameters: C_S=4aF, C_D=5.6aF, C_G=0.3aF.

Figure 3-14 Comparison of simulations using SIMON 2.0 and experimental results.

Figure 3-15 Stability plot simulated by SIMON 2.0 using parameters extracted from Figure 3-13.

Figure 3-16 (a) Top view and (b) tilted view of scanning electron microscope images of Coulomb blockade MuQFET with scaled fin width and split gate separation.

Figure 3-17 Short, Coulomb blockade and open mode operation of MuQFET at 77K.

Figure 3-18 I_D-V_{CG} characteristic of MuQFET showing Coulomb oscillation at 77K.

Figure 3-19 Drain conductance stability plot of MuQFET at 77K.

Figure 3-20 I_D-V_{CG} characteristic of Coulomb blockade MuQFET for T=77K, 97K and 117K. Coulomb oscillation starts to disappear at above 117K.

Figure 3-21 (a) Capacitance components of the Coulomb blockade MuQFET. (b) Control gate components: C_{CG, TOP} and C_{CG, SIDE}. C_{CG, TOP} scales with fin width while C_{CG, SIDE} does not.

Figure 3-22 The nanodot addition energy E_A (black) components: Coulomb charging energy E_C (red) and quantized energy level E_Q (blue) for silicon quantum dot.

Figure 3-23 Scanning electron microscope image (false color) of a decision node consisting of two Coulomb blockade MuQFETs in each path.

Figure 3-24 Measured stability plot of the device in the left and right path (V_{SG}=-0.8V) at T=77K.

Figure 3-25 (a) I_D-V_{CG} characteristic of the devices of left and right path at 77K. (b) I_D is plotted as a function of logic input X after transforming the data in the V_{CG} window in Figure 3-24. (c) y=IDL/IDR is plotted as a function of logic input X. (d-f) Path switching at 4K. The V_{CC} can be reduced from 300mV to 100mV in order to change current from background level to Coulomb peak.

Figure 3-26 Switching efficiency as a function of V_{CC}.

Figure 4-1 A schematic of the non-volatile MuQFET structure.

Figure 4-2 Phase diagram of Pb[Zr_{1-x}Ti_{x}]O_3.
Figure 4-3 A schematic of PZT unit cell showing the displacement of Ti or Zr atom. ..........54

Figure 4-4 Capacitance-voltage characteristic of MOS capacitors without (a) and with PZT layer (b). .................................................................56

Figure 4-5 Capacitance-voltage loop with voltage sweep ranges from ±2V to ±10V. ..........56

Figure 4-6 Capacitance-voltage characteristic for different gate voltage ramping rates. ....57

Figure 4-7 Schematics of volatile and non-volatile gate stack of MuQFETs. .........................59

Figure 4-8 Map of device operation modes as a function of programming voltage.................59

Figure 4-9 A schematic of fabrication process flow of non-volatile MuQFET with ferroelectric gate stack. ..................................................................................61

Figure 4-10 (a) Tilted scanning electron microscope image of a single electron transistor; (b) Cross-section schematic along transport direction; (b) false colored transmission electron microscope image of cross-section indicated in (a); (c) a magnified view of the outlined region in (b) ..............................................................62

Figure 4-11 Energy dispersive X-ray spectroscopy characterization of the chemical composition in the transmission electron microscope image.........................................62

Figure 4-12 Programmability of the fabricated SET. (a) I_D-V_CG for open, Coulomb blockade and shot mode at V_D=1mV; (b) self-consistent Poisson-Schrodinger simulation shows the electron density within the device geometry in Figure 2(c) (V_CG=0V); (c) Drain conductance contour as a function of V_CG and V_D at V_SG=-1.5V and T=4K (Coulomb oscillation diamond). (d) Device parameters extracted from Coulomb diamond size and edge slope...........................................................................64

Figure 4-13 (a-c) The split gate bias V_SG and measured coupling resistance RT is plotted as a function of time for short, Coulomb blockade and open mode. The schematics below show the remnant polarizations in the ferroelectric layer and electron density distribution in the quantum well. The measurement was done with V_DS=1mV, V_CG=0V and T=4K. The device used to extract tunnel resistance has a 500nm split gate separation.........................................................................................................................66

Figure 4-14 Coulomb oscillations I_D-V_CG are measured for different times in retention stage. The programming time scale is shown in Figure 4-13(b). -7.5V pulse programming voltage is removed at t=0. .........................................................68

Figure 4-15 Depolarization effects in the non-volatile Coulomb blockade device.................68

Figure 4-16 Tunnel resistance is plotted as a function of time for different V_CG. The tunnel resistance reduction is less than 10% for more than 5 min over V_CG range from -1V to 0V range for the first and second Coulomb diamond. ..........................69
Figure 4-17 Schematics of fringing electric field in non-volatile MuQFET with thick and thin ferroelectric films.................................................................70

Figure 4-18 (a) Antifuse-like programming strategy proposed in [18]. (b) Schematic of non-ferroelectric SG and reference gate. The differential voltage cannot work as intended. (c) Schematic of ferroelectric SG and ferroelectric reference gate. The polarizations in the SG and reference gate cancel each other in terms of depletion or accumulation. (d) A possible split gate structure for differential programming voltage with ferroelectric SG and non-ferroelectric reference gate. .............................................71

Figure 5-1 A schematic of a reconfigurable BDD logic stage. The programming circuits in blue color are mostly idle..................................................................................74

Figure 5-2 A schematic of low supply voltage BDD logic with sense amplifier.................75

Figure 5-3 Energy-delay of 8-input XOR logic using complementary gates and hybrid MuQFET BDD with sense amplifier. ...........................................................................................................76

Figure 5-4 A simulation of improvement of SNR when signal passes through LCD stochastic resonator. With arbitrary unite, signal amplitude is 9, noise amplitude is 2, threshold is 10. Signal frequency is 1Hz and sampling rate is 10000s⁻¹. The plots show (a) input signal, (b) output signal, (c) power spectrum density of input signal and (d) power spectrum density of output signal...................................................................................79

Figure 5-5 Sense amplifier consisting of amplification circuit and LCD resonator. The signal Y₁ loss swing in logic operation in BDD fabric compared to initial signal X. The amplification circuit partially recovers the swing and the LCD resonator utilize the stochastic resonance to improve signal to noise ratio and fully recover the signal swing in the output Y..........................................................80

Figure 5-6 A schematic of single electron box simulation. The 1st electron charges at 0.2V in the stationary DC simulation.................................................................81

Figure 5-7 Simulation results of nanodot charge..............................................................82

Figure 5-8 Correlation between input V(t) and output Q(t) as a function of thermal noise level..................................................................................................................82

Figure 5-9 (a) Schematic of experimental setup to measure stochastic resonance in Coulomb blockade devices. Input impedance of oscilloscope is 1MΩ. (b) I_D-V_D characteristic at 4K, V_SL=-0.8V, V_CG=0V. Frequency of the input square wave is 100Hz, offset is 0V and amplitude is 40mVPP. (c) Output wave of oscilloscope as a function of time. (d) Correlation between output and input waveform is plotted as a function of noise rms amplitude.................................84
LIST OF TABLES

Table 2-1 Transistor structures and electrostatic scaling length comparison. EOT of quantum well structure has included the InP/InAlAs barrier. .............................................. 16

Table 3-1 Device parameters extracted from Figure 3-20. .............................................. 42

Table 3-2 Full comparison of device geometry and electrical parameters for the device in Chapter 3.4, scaled device in Chapter 3-5 and projected device operating at room temperature ........................................................................................................................................ 44

Table 3-3 Capacitance and Resistance parameters extracted from Figure 3-24. ...................... 48
ACKNOWLEDGEMENTS

I would never have been able to finish my dissertation without the guidance of my advisory committee members, help from friends, and support from my family and wife.

First I would like to express my deepest gratitude to my doctorate advisor, Dr. Suman Datta, for his excellent guidance, patience and providing me the opportunity to work in semiconductor device research. His passion and altitude towards exploration of device engineering is the best natures that I should develop to go further as a device engineer. I would also like to express my gratitude to Dr. Vijay Narayanan for the helpful guidance in the logic architecture work. I would like to express my gratitude to Dr. Theresa Mayer, Dr. Ruzyllo and Dr. Nitin Samarth for helpful discussions throughout my Ph.D. journey on my research work.

My device fabrication work relied on the use of nanofabrication facility at Penn State. I would like to convey my sincere thanks to the staff, especially to Chad Eichfeld, Bangzhi Liu, Bill Drawl, Guy Lavallee, Kathy Gehoski, Yan Tang, Shane Miller, and Jaime Reith for their trainings and sharing of their knowledge and experience. Also, I need to thank Joshua Maier and Xiaojun Wen and Trevor Clark for the help in material characterization.

I would also express my gratitude to my collaborations. I especially would like to thank Vinay Saripalli for your great contribution to the device-circuit co-design work, and Saurabh Mookerjea for your guidance when I was new to cleanroom work. I would also thank Feng Li, Dheeraj Mohata, Ashkar Ali, Arun Thathachary, Rajiv Misra, Dave Rench, Wei-Chieh Kao, Euichul Hwang, Bijesh Rajamohanan, Ashish Agrawal, Mike Barth, Himanshu Manda, Nidhi Agrawal, Eugene Freeman and Nikhil Shakla for your help technical discussions and help in experimental setup.

Finally, I would like to thank my parents, Fuhui Liu and Yajuan Lu, who raised my very well with a healthy body, strong sense of responsibility, courage and positive attitude towards
difficulties. I would like to thank my wife Yaoting Deng who gives me most support and courage to complete the long PhD journey. The life with her in Penn State pursuing PhD together would be my most precious memory in lifetime.
Chapter 1

Introduction

1.1 Motivation

In the past sixty years, the semiconductor technology has revolutionized from the first transistor in Bell’s laboratory [1] to the state of the art silicon 3D transistor [2]. In the scaling trend predicted by Moore’s law [3], accompanied with increasing transistor count per area, supply voltage scales down as well [4]. The voltage scaling is fundamental to achieving energy efficient digital logic circuits due to the quadratic reduction in dynamic energy with supply voltage scaling. The traditional MOSFET scaling strategy is reducing the gate length and supply voltage by the same factor (1/k) so that circuit speed is improved by k and the power dissipated per device is scaled by 1/k^2. However, below 100nm technology, the non-scalable threshold voltage in MOSFET has prevented voltage scaling in proportion to gate length [4-5]. The threshold voltage in MOSFET is limited by sub-threshold swing, which naturally becomes worse in short channel transistor. On the other hand, as supply voltage scales down, the insufficient drive current leads to problems in gate delay. Therefore, innovation in electrostatics to enhance short channel performance, as well as materials and strain engineering to boost channel mobility is essential to improve energy-performance efficiency as shown in Figure 1-1. High-k/metal gate stack was introduced in 45nm Si technology [5]. The need for improved short-channel electrostatics has forced a shift to the multi-gate three-dimensional structure in 22nm Si technology [2]. III-V compound semiconductors such as In_{x}Ga_{1-x}As (x=0.53-0.7) and InSb are being actively researched as replacement for silicon for low supply voltage logic applications due to their superior transport properties [6-10]. Also, computing paradigm evolution is required as a natural
result of device innovations [11]. This dissertation will consider the features with outline in Figure 1-1 and explore their device-circuit implementations [12].

![Figure 1-1 Illustrations of advances in electrostatics, materials, strain engineering and computing paradigms with semiconductor device scaling. The technologies introduced in this dissertation are highlighted with blue box.](image)

### 1.2 Non-Planar In$_{0.7}$Ga$_{0.3}$As MuQFET for Low Power Logic

In$_{0.7}$Ga$_{0.3}$As quantum well is a high electron mobility system widely used in high speed electronics [6,8,9]. The epitaxial layer structure and band profile from NextNano [13] self-consistent Poisson-Schrodinger simulation are shown in Figure 1-2. The ultra-thin In$_{0.7}$Ga$_{0.3}$As channel is located between high band-gap In$_{0.52}$Al$_{0.48}$As barrier layers. The n-type doping layer (silicon) is separated from the transistor channel, which can effectively reduce the Coulomb scattering from ionized dopant atoms. The simulated electron density profile confirms that the electron transport is restricted in the In$_{0.7}$Ga$_{0.3}$As channel without parallel conduction in the In$_{0.52}$Al$_{0.48}$As buffer layer. The experimental Hall measurement shows the electron mobility in In$_{0.7}$Ga$_{0.3}$As quantum well can be as high as 10000cm$^2$/Vs at room temperature [9].
The III-V materials have lower density of states allowing less carriers transport compared to silicon at high supply voltage. However, the advantage of high carrier mobility enables III-V channel beats silicon at low supply voltage. Take advantage of both electrostatics and transport properties, it is expected that III-V semiconductors (InGaAs) system is a strong candidate as channel in a multi-gate configuration in sub-14nm technology node for low-V_{DD} (<0.5V) operation. Figure 1-3(a) illustrates the schematic of a III-V multi-gate quantum-well field effect transistor (MuQFET) with wrap gate and high-k/metal gate. The I_D-V_G simulation of a III-V MuQFET with L_G of 22nm shows a 2x improvement in I_{ON} over Si MOSFET at V_{CC}=0.5V at constant I_{OFF} (Figure 1-3(b)) [12].

Figure 1-2 (a) Epitaxial layer structure for In_{0.7}Ga_{0.3}As MuQFET, and simulated energy band diagram (b) and electron density profile (c).
1.3 Further Device Scaling: Approaching Theoretical Minimum Switching Energy

Figure 1-4 shows the estimated switching energy of silicon n-FET scaling as a function of gate length [14-15]. At the same time, the number of electrons involved in the switching behavior is logarithmically reduced. When the device is scaled down to sub-5nm, the energy consumed in the transistor switching is approaching the theoretical limit $kT\ln 2$, which is single electron operation [16]. At this scale close to the scaling limit, it is still not clear and very questionable whether the traditional MOSFET configuration still can provide robust characteristic due to challenges like direct source to drain tunneling and severe short channel effects. For sub-300mV logic applications, complementary logic might be inaccessible even with multi-gate III-V FETs due to insufficient current drivability at such low supply voltage and reduction in the gain in the transfer characteristics at logic gate level. On the other hand, instead of strong coupling between channel and source/drain, the weak coupling provides unique Coulomb oscillations naturally utilizing the single electron charging effect in the aggressively scaled dimensions. Unlike performance degradation in short channel MOSFET, smaller dimensions enable higher ON/OFF ratio in Coulomb oscillations in single electron transistor. Therefore this dissertation will continue to explore the possible low power device solution and associated logic architecture near the scaling limit, by converting the 1D MuQFET channel to 0D with few electrons confined.
Figure 1-4 Switching energy and operational electron number scaling are plotted in silicon n-MOSFET. The scaling curve of III-V transistors is steeper than that of silicon transistors due to lower density of states.

1.4 Coulomb Blockade In$_{0.7}$Ga$_{0.3}$As MuQFET

Nanoscale devices that transport and store few or single electron, already implemented in low supply voltage memory, have also attracted recent research interest for energy efficient logic applications [12,17-19]. Yet majority of these few electron devices suffer from low transconductance, degraded output resistance, and often from a lack of complementary logic (n and p-channel device) solution [18], making it essential to co-explore the device design with a non-CMOS architecture. The binary decision diagram (BDD) logic architecture has been proposed as a suitable candidate for implementing logic with these single electron transistors [19]. By modifying the gate stack of MuQFET, the Coulomb blockade MuQFET illustrated in Figure 1-5, which uses a pair of split gate to confine nanodot and a top control gate to modulate potential, can exhibit Coulomb oscillations as single electron transistor. Figure 5 shows its $I_D$-$V_G$ simulation exhibiting Coulomb oscillations. The fabrication process is compatible with top-down
CMOS fabrication, which makes the Coulomb blockade MuQFET a promising emerging device for low power hybrid logic circuit.

Figure 1-5 Schematic of non-classical (NC) III-V MuQFET; (b) $I_D$-$V_G$ characteristics of III-V NC-MuQFET exhibiting Coulomb oscillations at T=300K.

1.5 Organization of This Dissertation

Chapter 2 will discuss the fabrication, characterization and modeling of classical In$_{0.7}$Ga$_{0.3}$As MuQFET. In particular, the analysis of carrier transport in the channel will be analyzed showing quasi-ballistic transport in short channel devices. The device energy-delay metrics will also be modeled and compared with silicon transistor. Chapter 3 will address converting the MuQFET channel from 1D to 0D using electrostatic confinement. The 0D channel in few electron regime exhibits Coulomb oscillation characteristic. Further, the tunable electrostatic barrier allows programming the device into three modes. Chapter 4 will discuss adding non-volatile feature into the MuQFETs in Chapter 3 using ferroelectric gate stack. Chapter 5 will provide an overview of the hybrid BDD circuits and discuss low power sensing strategy.
Chapter 2

Quasi-Ballistic Classical In$_{0.7}$Ga$_{0.3}$As MuQFET

2.1 Device Fabrication Process

The InGaAs MuQFET is fabricated on an In$_{0.52}$Al$_{0.48}$As/In$_{0.7}$Ga$_{0.3}$As/In$_{0.52}$Al$_{0.48}$As quantum well wafer epitaxially grown by IQE Inc. The layer structure was shown in Figure 1-6. The mobility of quantum well is further enhanced by compressive strain from lattice mismatch between In$_{0.52}$Al$_{0.48}$As and In$_{0.7}$Ga$_{0.3}$As. The defects level is smaller than 40cm$^{-2}$. An InP cap layer is deposited on the surface to improve the interface quality between semiconductor and dielectric.

The device fabrication flow is shown in Figure 2-1. After surface cleaning with hot acetone and IPA, the lithography alignment markers (20nm Ti/80nm Au) were made by e-beam lift-off process. Then the multi-fin and single-fin were defined by e-beam lithography and low power BCl$_3$/Ar dry etch. The patterned fin widths vary from 10nm to 500nm. A 5s dip in very diluted H$_2$SO$_4$:H$_2$O$_2$:H$_2$O (1:3:200) solution would smooth the etched sidewall. Afterwards, the source/drain pads are made by ebeam lift-off process. The source/drain stack is based on Ni/Ge diffusive contact on GaAs based III-V compound [20]. Ge is used to dope InAlAs/InGaAs and Ni catalysts Ge diffusion reaction. A slight BCl$_3$/Ar etch was used to remove InP cap in source/drain region since InP prevents Ni/Ge diffuse into semiconductor. Ni (10nm)/Ge (30nm)/Au (60nm) metal stack was deposited by evaporation and lifted-off in remover PG. The sample was annealed at 350°C for 90s in N$_2$ to form alloy Ohmic contact. After a 1:50 HCl surface treatment, the high-k dielectric stack (1nm Al$_2$O$_3$/3.5nm HfO$_2$) was deposited at 250°C. Al$_2$O$_3$ forms a better interface with InP/InGaAs in Cambridge thermal atomic layer deposition system, while the HfO$_2$
provides high dielectric constant to enhance gate control. The gate region was defined by e-beam lithography and Pd (20nm)/Au (60nm) gate was made by e-beam lift-off process. Finally, a combination of Cl₂ dry etch and 1:50 HF wet etch was used to remove the Al₂O₃/HfO₂ dielectric on the source/drain contact. The In₀.₇Ga₀.₃As MuQFET fabrication process recipes are listed in Appendix A.

Figure 2-1 In₀.₇Ga₀.₃As MuQFET fabrication process.

Figure 2-2 shows the schematic and scanning electron microscope image of the fabricated single fin In₀.₇Ga₀.₃As MuQFET. The source and drain are connected by one active fin surrounding by the wrap gate. The dummy fins are used to reduce proximity effect when exposing large area with small beam. These dummy fins can significantly enhance ebeam lithography resolution of central active fin, serving as proximity effect correction structure. Figure 2-3 shows the cross-section scanning electron microscope after a focus ion beam treatment on the active fin. Multi-fin long channel structure is also fabricated to facilitate the capacitance-voltage measurement.
2.2 Electrical Characterization and Transport Analysis

The fabricated classical MuQFETs were measured in a Cascade probe station system using HP semiconductor parameter analyzer under room temperature. The transfer characteristic with 100nm gate length for 10nm and 40nm fin width is plotted in Figure 2-4 (a). The On current is over 100μA/μm with 0.5V drain bias. The subthreshold swing is 250mv/dec for $W_{\text{fin}}=40\text{nm}$ and 120mV/dec for $W_{\text{fin}}=10\text{nm}$. Figure 2-4 (b) lists the measured sub-threshold swing for different fin width and gate length, which confirms that narrower fin width with tri-gate configuration, can effectively improve the electrostatics and reduce short channel performance degradation. Also the
sub-threshold voltage shift positively with reducing fin width, which implies that it is possible to make enhancement mode MuQFET by engineering fin width together with gate work function.

![Figure 2-4](image)

Figure 2-4 (a) $I_D-V_G$ transfer characteristic of MuQFET with $L_G=100$nm; (b) subthreshold swing (SS) is plotted as a function of gate length for different fin width.

In order to analyze the transport in the channel, the channel mobility needs to be extracted. Effective carrier mobility is extracted from total source to drain resistance $\frac{V_D}{I_D} = \left( \frac{L_G}{W_{FIN}} \right) \left( \frac{1}{N_{SQHEFF}} \right) + R_{Ext}$. The external resistance $R_{Ext}$ and sheet carrier density $N_S$ are needed to extract effective carrier mobility. In Figure 2-5(a), the source to drain total resistance is plotted as a function of gate length with different gate bias for 40nm fin width. The crossover point of resistance curves gives out the external resistance (5kΩ*um) which does not respond to gate modulation. This crossover point also indicates the correction of gate length $\Delta L_G$. The actual gate length is larger than physical gate length because the gate fringing electric field penetrates into the source/drain extension region. In Figure 2-5(b), the resistance components consisting of channel resistance and external resistance are plotted. The total resistance is dominated by external resistance with gate overdrive. In Figure 2-6, the high-frequency capacitance-voltage measurement is conducted in multi-fin long channel MuQFETs with the same fin width. The channel charge density is calculated from integration of capacitance-voltage curve. With
extracted external resistance and channel carrier density, the effective mobility is plotted in Figure 2-7. The extracted strained quantum well mobility is around 3000-6000 cm²/Vs. From Figure 2-7, it is observed that the mobility reduces with gate length. In Figure 11, the mobility at 1x10¹² cm² carrier density is plotted as a function of gate length. The reduction of effective mobility in short channel transistor is predicted by Landau’s 1D quasi-ballistic transport formalism [21-22]. Considering the ballistic transport, the effective mobility

\[ \frac{1}{\mu_{\text{eff}}} = \frac{1}{\mu_{\text{diff}}} + \frac{1}{\mu_{\text{ball}}} \]

The diffusive component \( \mu_{\text{diff}} \) is a constant, and the ballistic component is expressed as

\[ \mu_{\text{ball}} = \frac{2q(L_G + \Delta L_G)}{m^*\pi v_{TH}} \]

where the \( m^* \) is the carrier effective mass and \( v_{TH} \) is the thermal velocity. The effective mobility has diffusive component and ballistic component. The diffusive mobility in long channel drift-diffusion process is independent of transport length. However, the ballistic component is proportional to gate length. This theorem explains the effective mobility reduction with gate length. In Figure 2-8, using the parameters as shown, the experimentally extracted mobility well fits the quasi-ballistic transport formula, which means the electron transport is in quasi-ballistic regime for short channel MuQFET. The quasi-ballistic transport requires the carrier mean free path is comparable with the transport length. The mean free path of carrier can be roughly calculated from thermal velocity and mean free time by \( \lambda = v_{TH}\tau/2 \), and \( \tau \) can be estimated from mobility \( \mu = qm^*/\tau \). Assuming \( v_{TH} = 7.5 \times 10^7 \text{cm/s} \) and \( \mu = 4000 \text{cm}^2/\text{Vs} \), the mean free path \( \lambda \approx 290\text{nm} \) in agreement with the gate length dimension in these MuQFETs. Recent study on bend resistance measurement directly verifies the quasi-ballistic transport phenomenon in this \( \text{In}_{0.7}\text{Ga}_{0.3}\text{As} \) quantum well system [23].
Figure 2-5 (a) source to drain total resistance as function of gate length. The cross point gives the external resistance; (b) components analysis of total resistance.

Figure 2-6 From multi-fin long channel MuQFET, high-frequency C-V measurement (background subtracted) gives out the channel carrier density (W=40nm).
Figure 2-7 Experimentally extracted mobility as a function of channel electron density in In$_{0.7}$Ga$_{0.3}$As MuQFET (W=40nm).

\[
\frac{1}{\mu_{\text{eff}}} = \frac{1}{\mu_{\text{ballistic}}} + \frac{1}{\mu_{\text{diffusive}}}
\]

\[\mu_{\text{diffusive}} = 8000 \text{ cm}^2/\text{V} \cdot \text{s}\]

\[\mu_{\text{ballistic}} = 2qL/m^*\pi v_{\text{th}}\]

\[v_{\text{th}} = 7.5 \times 10^7 \text{ cm/s}\]

Figure 2-8 Room temperature effective mobility reduces when scaling gate length, indicating quasi-ballistic transport for short channel In$_{0.7}$Ga$_{0.3}$As MuQFET.
2.3 Scalability Study of In₀.₇Ga₀.₃As MuQFET

Figure 2-4(b) has shown the degradation of MuQFET subthreshold swing (SS) and drain induced barrier lower (DIBL) when scaling gate length. However, these experimental results greatly suffer from not fully optimized fabrication process in gate dielectric. To systematically study the potential scalability of transistors, the electrostatic scaling length is very important parameter. In a transistor, the electrostatic scaling length $\Lambda$ is defined as the slope of exponential potential change from source/drain to the channel. Better electrostatic control of gate provides shorter penetration length of source/drain electric field into channel. In the long channel transistor, if $V(0)$ is the source channel boundary potential and $V(ch)$ is the potential in the flat channel region, the potential profile $V(x)$ can be analytically expressed as

$$V(x) \approx V(0) + (V(ch) - V(0))(1 - \exp(-x/\Lambda)) .$$

Then the normalized the potential is defined

$$V_{norm}(x) = 1 - \frac{V(x) - V(0)}{V(ch) - V(0)} = \exp\left(-\frac{x}{\Lambda}\right)$$

where $V_{norm} = 1$ when $x/L_G=0$, and $V_{norm} = 0$ when $x/L_G>>\Lambda$. 
Figure 2-9 \(V_{\text{norm}}(x)\) versus \(x/L_G\) for long channel and short channel assuming heavy doped source/drain at \(V_S=V_D=0, V_G=-1\)V. The source/drain field becomes dominating in determining channel potential as \(L_G\) is comparable with electrostatic scaling length in short channel.

Figure 2-9 shows the potential profile in long channel and short channel transistors. In the long channel (\(L_G \gg \Lambda\)), most channel region exhibits flat potential profile under gate modulation. When the gate length is scaled down and becomes comparable with electrostatic scaling length (\(L_G < 5\Lambda\)), the exponential profile modulated by the source/drain can no longer be neglected. The shared channel charge control by the source/drain induced SS and DIBL degradation. Therefore \(\Lambda\) is a characteristic length of scalability below which the transistor greatly suffers short channel effect. High dielectric constant, thin semiconductor body and thin dielectric result in small electrostatic scaling length \(\Lambda\). In a two dimensional model, \(\Lambda\) can be analytically calculated as

\[
\Lambda \approx \frac{\varepsilon_S}{\sqrt{2\varepsilon_{\text{ox}}}} \left(1 + \frac{\varepsilon_{\text{ox}}T_S}{4\varepsilon_{\text{ox}}T_{OX}}\right)T_{OX}.
\]

In three dimensional structures, the electrostatic scaling length can be obtained from simulation in Sentaurus device [24]. Figure 2-10 and Table 2-1 show the simulated potential profiles from In_{0.7}Ga_{0.3}As MuQFETs along with planar quantum well FET and two other device configurations.
including a surface channel $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ FINFET [6] and a lattice matched non-planar $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ FET [8]. It is evident MuQFET shows superior scalability compared to the planar QWFET for the same EOT, which is consistent with the trend observed in Figure 2-4. The $\text{In}_{0.7}\text{Ga}_{0.3}\text{As}$ MuQFET has comparable scalability as the state-of-art non-planar devices.

![Figure 2-10 $V_{\text{norm}}(x)$ profile for transistor structure 1-5 listed in Table 2-1.](image)

Table 2-1 Transistor structures and electrostatic scaling length comparison. EOT of quantum well structure has included the InP/InAlAs barrier.

<table>
<thead>
<tr>
<th>Device</th>
<th>Oxide</th>
<th>EOT(A)</th>
<th>$\Lambda$ (nm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 Planar QWFET</td>
<td>10nm $\text{Al}_2\text{O}_3$</td>
<td>57.8</td>
<td>22.1</td>
</tr>
<tr>
<td>2 MuQFET</td>
<td>10nm $\text{Al}_2\text{O}_3$</td>
<td>57.8</td>
<td>12</td>
</tr>
<tr>
<td>W=40nm</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>3 MuQFET</td>
<td>1nm $\text{Al}_2\text{O}_3$</td>
<td>24</td>
<td>5.8</td>
</tr>
<tr>
<td>W=40nm</td>
<td>3nm $\text{HfO}_2$</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
2.4 TCAD Simulation

TCAD simulation in Synopsys Sentaurus [24] is deployed to project the potential performance with further dimension scaling. The simulation approach of the short channel MuQFETs capturing the non-equilibrium electron overshoot effect is discussed in literature [25]. The Sentaurus model uses an effective mobility in modified Canali model:

\[ \mu_{\text{EFF}}(E) = \frac{(1+\alpha)\mu_{\text{LOW}}}{\alpha + \left[1 + \frac{1+\alpha\mu_{\text{LOW}}^2}{v_{\text{SAT}}^2}\right]^{1/\beta}}. \]

The fitting parameters are: \( v_{\text{SAT}} = 9.5 \times 10^7 \text{ cm/s} \), \( \alpha = 0 \) and \( \beta = 0.6 \). Here, \( v_{\text{SAT}} \) is the saturation velocity and \( \beta \) is a constant reflecting the steepness of the carrier velocity profile in the channel. The default value of these parameters are as \( v_{\text{SAT}} = 0.93 \times 10^7 \text{ cm/s} \) and \( \beta = 2 \) for electrons by default. However, in order to take into account the velocity overshoot effect at high fields and maintain the accurate velocity at low fields, a high saturation velocity value and a lower than unity beta value are used to prevent large error in low field situation within the drift-diffusion simulation framework [26-28]. Fermi statistics is used in the simulation. Further, in order to capture the non-fully-optimized process, a series resistance \( R_{\text{external}}/2 = 2.5 \Omega \times \text{um} \) at the source/drain side and an interface trap density \( 7.5 \times 10^{12} \text{ cm}^{-2}\text{eV}^{-1} \) are included in the simulation to match the experimental \( I_{\text{ON}} \) and subthreshold slope. The simulation was running in the clusters in Micro-System Design Laboratory in Computer Science and Engineering department. Figure 2-11
shows the simulated curve in comparison with the experimental results. Potential process optimization of series resistance (80Ω*um) and D_IT interface (<1×10^{11} cm^{-2} eV^{-1}) will significantly improve the drive current and subthreshold slope.

![Simulation vs Experiment](image)

Figure 2-11 Simulated and measured transfer characteristics. The red curve indicates potential improvement due to process optimization to external resistance and interface trap density.

### 2.5 CV/I Delay Metric Benchmark

In a digital circuit, the gate delay and system speed is strongly related to the transistor delay determined by the transistor key characteristic [29]. The simplest expression of transistor delay for trend analysis is CV/I delay metric. The CV/I delay metric is calculated as \( \tau = CV_D/I_{ON} \). Ignoring the Miller capacitance and diffusion capacitance, the capacitance can be estimated by \( C \approx \varepsilon_{OX}WL/t_{OX} \). Gate capacitance and \( I_{ON} \) for III-V MuQFETs can be simulated in Sentaurus Device calibrated with the experimental results. As a comparison, the analysis for the 32nm silicon planar MOSFET and 22nm silicon FINFET is also done using Sentaurus Device model calibrated with the results reported in literature [30].

Figure 2-12 compares the CV/I delay metrics for silicon transistors and In_{0.7}Ga_{0.3}As MuQFETs [30]. With potential improvement of semiconductor/oxide interface
(D\text{rr} \approx 10^{11}/\text{cm}^2*\text{eV}) \text{ and external resistance, the CV/I delay of 150nm In}_{0.7}\text{Ga}_{0.3}\text{As MuQFET is almost comparable with 32nm silicon MOSFET due to high drive current capability. If the MuQFET is scaled down to 22nm and use the same EOT and fin width as 22nm silicon FinFET, CV/I delay is 32% less than silicon FINFET of comparable geometry. The III-V MuQFET serves as a good candidate for the next few generation logic transistors. More importantly, the III-V MuQFETs sense amplifier can be on-chip integrated with Coulomb blockade Boolean logic block to enable sub-300mV non-CMOS logic as discussed in this dissertation.}

Figure 2-12 CV/I delay metrics for In$_{0.7}$Ga$_{0.3}$As MuQFETs and silicon transistors.
Chapter 3

Coulomb Blockade MuQFETs for Binary Decision Diagram Logic

3.1 Manipulation of 0D Few Electron Island

Nanoscale devices that transports and store few or single electron, already implemented in low supply voltage memory, have attracted recent research interests for sub-300mV logic applications [18,31-33]. Manipulation and 0D few electron island is the fundamental requirement for single electron electronics and photonics. Particularly, in addition to the nanometer dot size and quantum confinement in all dimensions, accurate control of coupling strength (capacitive and resistive) between the island and the device terminals (source/drain/gate) is essential to low power logic applications. Manipulation and control of few electron dots have been studied in the last twenty years [33-37]. In general, there are two different types of fabrication techniques to build nanodot devices: bottom up-approach and top-down approach. The bottom-up approach involves the synthesis and assembly of metal or semiconductor nanoparticles [33-36]. Figure 3-1(a) shows an example of single electron transistor fabrication process with bottom-up approach. The dielectric confining the nanoparticle can be oxide, organic polymers or air gap. The synthesized dot can easily reach sub-10nm diameter without fancy tools. However, the standard deviation of the dot dimension is large and assembly process has high failure rate with high device density. The top-down approach is based on nanolithography techniques to pattern nanoscale structure on the semiconductor wafer. Figure 3-1(b) shows a single electron transistor defined by negative biased Schottky electrodes based on AlGaAs/GaAs 2DEG. The confinement can be from either band structure or electrostatic. Compared to bottom-up approach, the top-down approach heavily relies on the resolution of e-beam lithography tool and is costly to fabricated
sub-10nm dots. However, the nanolithography based process is compatible with current state-of-the-art silicon CMOS technology, which has decent control of device variations in very large scale integration. More important, the option of electrostatic confinement in the top-down fabrication may provide tunable coupling strength between nanodot and electrodes, which is required to do device modes programming in Boolean logic architecture as discussed in Chapter 3.3.

Figure 3-1(a) A schematic of single electron transistor fabricated by bottom-up approach. The nanoparticle is chemically synthesized and assembled to electrodes on chip. (b) A schematic of single electron transistor confined by e-beam lithography defined Schottky electrodes on AlGaAs/GaAs 2DEG.
3.2 Basic Physics of Coulomb Blockade

The simplest device in which the effect of Coulomb blockade can be observed is so-called single electron transistor (SET). The basic construct of SET is shown in Figure 3-2(a). The transistor channel is typically a nanodot, which is weakly coupled with source/drain Fermi reservoir via tunnel resistance and capacitance. The source/drain to dot tunnel resistance has to be large enough to separate the dots from the source/drain leads. Starting with the energy-time statement of the uncertainty principle, $\Delta E \Delta t > \hbar / 2\pi$, and taking $\Delta t$ to be the RC lifetime of the island $R_t C_{\text{total}}$ and $\Delta E$ to be the charging energy $q^2 / 2C_{\text{total}}$, we find

$$\frac{q^2}{2C_{\text{total}}} R_t C_{\text{total}} > \frac{\hbar}{2\pi}$$

$$R_t > \frac{\hbar}{q^2}$$

In this case, the de Broglie wave of the electron is localized in the nanodot. A third terminal is coupled with the nanodot with insulating dielectric to modulate the nanodot potential. Usually the dielectric should be thick enough so that the conductance to the third gate terminal is negligible.

The electron energy levels in the nanodot are sketched in Figure 3-2(b-c). The addition energy $E_A$ required to fill another electron to the nanodot has two components: the classic self Coulomb charging energy $e^2 / 2C_{\text{total}}$ and quantized energy level $E_Q$. For nanodot larger than 10nm, the charging energy dominates in the addition energy. When dot size is smaller than 10nm, the quantized energy level gap begins to play an important role. Figure 3-2(b) shows the Coulomb blockade state in which no accessible energy levels are within tunneling range of the electron (red) on the source contact. All energy levels on the island electrode with lower energies are occupied. When a positive voltage is applied on gate terminal, the next unoccupied energy level is lowered as shown in Figure 3-2(c). The electron (green) can tunnel onto the island, occupying a
previously vacant energy level. From there it can tunnel onto the drain electrode where it inelastically scatters and reaches the drain electrode Fermi level. If we sweep the gate voltage at fixed drain bias, the transistor periodically switches between blockade state and transmitting state, resulting in the oscillation transfer characteristic as shown in Figure 3-2(d).

Three conditions must be achieved to observe Coulomb blockade: (1) The drain bias must be smaller than $E_A/q$; (2) The coupling resistance between source/drain and nanodot must be greater than $\hbar/q$ to localize the electron wave inside the nanodot; (3) The thermal energy in source contact plus the thermal energy in the nanodot, in the scale of $k_B T$, must be sufficiently smaller than the addition energy $E_A$, otherwise the electron will be able to pass the nanodot via thermal excitation. Experimental observation of Coulomb blockade usually requires $E_A > 8k_B T$.

Finite DC bias has two effects in breaking Coulomb blockade state. Let us assume positive $V_{DS}$ and analyze the dynamic in the band profile. Obvously the drain bias can bring
down the drain Fermi energy level. When the bias is large enough to align drain Fermi level with a filled energy level in the nanodot, carrier begins to transmit from source to drain through this energy level as shown in Figure 3-3(a). On the other hand, the drain terminal is capacitively coupled to the nanodot with finite capacitance $C_D$. When the drain bias lowers the unfilled energy level in the nanodot to align with source Fermi level, the transmission also takes place in Figure 3-3(b). Either effect, which comes first, determines the boundary of the Coulomb blockade state. In the drain conductance $G_D=I_D/V_D$ contour plot as a function of $V_G$ and $V_D$, the blockaded transport state (low $G_D$) exists in a diamond shape as shown in Figure 3-3(c). The width of diamond is determined by gate coupling effect $q/C_G$ and the maximum height is $q/C_{total}$. The blue edge line indicates the capacitively coupling effect takes place at smaller VDS since the Fermi level is closer to the unfilled state. The slope determines the coupling ratio $C_G/C_L$. Yet when the Fermi level is closer to the filled state, the drain Fermi level lowering effect is responsible for the red edge line. Solving the geometry in the triangle gives the slope of the red edge is $C_G/(C_{total}-C_D)$ or $C_G/(C_G+C_S)$ if parasitic capacitance is negligible. The case with negative drain bias can be analyzed in similar ways. The Coulomb diamond contour provides the method to calculate the device parameter from electrical conductance measurement.
Figure 3-3(a) The source/drain Fermi level is closer to filled state. Finite $V_D$ brings down the drain Fermi level and align with one filled state in the nanodot causing electron transmission. (b) The source/drain Fermi level is closer to the unfilled state. Finite $V_D$ lowers the chemical potential in the nanodot due to capacitive coupling effect. The blockaded transport disappears when the unfilled state align with source Fermi level. (c) Schematic of Coulomb diamond. The red and blue edges correspond to the scenarios described in (a) and (b) respectively.
3.3 Circuit-Device Co-Design for Reconfigurable Binary Decision Diagram (BDD) Logic

In Figure 3-2(d), it is evident that the Coulomb blockade degrades when drain bias $V_D$ is comparable with the discrete energy gap $E_A/q$. However, the gate bias window width needs to be at least $E_A/2q*(C_{\text{total}}/C_G)$ to go from valley to peak in Coulomb oscillations. Thus the complementary pass transistor logic has intrinsic problem to go from valley to peak with direct drain-to-gate connections, due to low $C_G/C_{\text{total}}$ ratio in these non-robust nanoscale devices. Also, few electron devices usually suffer from low trans-conductance, degraded output resistance, and, often, from a lack of complementary logic (n and p-channel device) solution. Figure 3-4 shows a single electron transistor inverter with practical $C_G/C_{\text{total}}=0.4$ gate coupling ratio [38]. The inverters have VTC curves with slope<-1 and cannot function as logic gate. All these issues make it essential to co-explore the few electron device design in conjunction with a non-CMOS but preferably Boolean logic architecture. Researchers have proposed binary decision diagram (BDD) logic architecture as a suitable candidate for implementing logic with these few electron devices. Figure 3-5(a) shows a schematic of BDD 3-input XOR circuit consisting of decision nodes. In each decision node, there is a Coulomb blockade device in each path. The logic input $X$ determines the Coulomb blockade or transmitting state in the transistor and route the electron into left or right path to implement logic functionality. Unlike cascaded logic, BDD logic does not require devices with decent transfer gain within the BDD stack.
Figure 3-4 A single electron transistor inverter voltage transfer characteristics (VTC) for gate coupling ratio 0.4.

Figure 3-5 A schematic of an XOR BDD circuit. Each decision node is a Y junction consisting two Coulomb blockade transistors with opposite logic input.
On the other hand, the Coulomb blockade transistors, close to the limit of scaling, potentially have high defect rate and variability. It is quite likely certain part of the BDD circuit is not functional properly due to device failure. Thus reconfigurability becomes vital to the BDD architecture. Eachempati et al. [18] proposed the reconfigurable architecture based on 2D hexagonal device fabric like field programmable gate array (FPGA). This scenario requires devices in each path of decision node to be multi-functional- not only to perform as a decision node edge using its Coulomb blockade functionality and execute the path switching function but also to implement a short or an open path along certain edges of the two-dimensional hexagonal fabric. There are several reported single electron transistor configurations as shown in Figure 3-6.

In the simplest construct, the tunnel barriers can be a few nanometer thick insulator films physically situated between the source/drain and the nanodot acts as the Coulomb island [33, 39-40]. The disadvantage of physical insulator barrier is that the tunnel resistance is determined by the film thickness and the conduction band barrier height, which cannot be modulated once the device is fabricated. To achieve a programmable operation, one can harness the depletion created by two negatively biased split gates region as an electrically tunable tunnel barrier. The coupling strength between the source/drain reservoirs and the Coulomb island can be continuously modulated by the split gate voltage [41-43]. In certain voltage range, the split gate fringing electric field modulate the dot potential to show Coulomb blockade while retain coupling resistance greater than $h/q^2$. However, it is not preferred to apply logic input to the split gate and have unstable source/drain to dot coupling strength in practical design. In this thesis we build the device structure with split gate to program device mode and independent top control gate to modulate dot potential. These devices have been shown to have the required programmability feature and allow implementation of reconfigurable BDD logic as discussed in the next parts of this chapter.
Figure 3-6 Comparison of various device configurations of few electron transistors.

Figure 3-7 shows a node of a two-dimensional hexagonal fabric implementing reconfigurable BDD logic with the novel programmable ferroelectric SET at each non-vertical edge and a conductive nanowire at each vertical edge. The non-vertical edge can be programmed by the split gate to perform logic functions in the Coulomb blockade mode, as well as act as short or open path. For example, if the two transistors are in active Coulomb blockade mode, passive path switching of messenger electrons through either left edge (X=1) or right edge (X=0) happens at the decision node according to the logic input to control gate. With such hexagonal arrays, the logic function mapping is reconfigurable as shown in Figure 3-8, where the same hexagonal fabric can be reconfigured from A+B to A⊕B. More complex logic functions can be implemented with BDD mapping techniques [18].
Figure 3-7 (a) A decision node consisting of two reconfigurable SETs at each path. The transistor can be programmed to execute logic functionality in the active Coulomb blockade mode, as well as act as the open or short path. (b) A 2D reconfigurable hexagonal fabric consisting of programmable devices (programming lines and inactive logic input lines to open and short path are not drawn). In this figure, A⊕B and A+B are demonstrated in the same fabric.

Instead of programming each decision node edge, Shiratori et al recently proposed programming of only the leaf nodes with SiNₓ programmable switches [19]. Our approach is a super-set of this technique since the decision nodes at the leaf of a binary tree achieve a functionality as the programmable leaf node. Our approach uses a similar number of programmable nodes with complexity O(2ʰ), where h is the depth of the binary tree. Further, the
link level programmability helps to better adapt to faults and in achieving more compact circuits when exploiting techniques such as reduced ordered BDD.

### 3.4 Fabrication, Characterization and Simulation of Coulomb Blockade \( \text{In}_{0.7}\text{Ga}_{0.3}\text{As} \) MuQFETs

To meet the requirement of reconfigurable BDD logic, the devices need to have confined 0D Coulomb island and electrical tunable tunnel barriers in the transport direction. In a classical MuQFET, the electrons transport in a 1D nanowire channel which is confined in two dimensions by the InAlAs barrier and the physical fin width. In order to form a quantum dot confined in all dimensions, additional tunnel junctions are needed in the transport directions. In the Coulomb blockade MuQFET as shown in Figure 3-8(a), a pair of split gates is used instead of single wrap gate in classical MuQFET. The separation between the split gates is around 80nm. The negative bias of the spit gates may deplete the region below them and result in additional confinement in the transport direction, so that a nanodot dot is formed in the quantum well between split gates. The split gate (SG) bias determines the coupling strength. On top of the split gate, a top control gate (CG) stack with thicker oxide is placed on the quantum dot. The top control gate controlling the potential of the confined nano dot may result in coulomb oscillations.

Similar to classical MuQFET fabrication process, the first step is to make alignment marker and test structure. The source/drain diffusive contacts stack Ni/Ge/Au are formed after fin patterning using e-beam lithography and BCl₃/Ar dry etch. 350° C contact stack annealing in N₂ ambient is used to drive the metal stack into semiconductor and form Ohmic contact to quantum well. The split gate dielectric is 10nm atomic layer deposited Al₂O₃ at 250° C. The process of split gate with narrow gap is very sensitive to the process conditions and environments. It requires full optimization of dose in e-beam writing and accurate temperature control in the development.
And successful lift-off requires smooth deposition rate without power spikes. It is recommended to do dose test and scanning electron microscope characterization on a spare In$_{0.7}$Ga$_{0.3}$As quantum well sample with Al$_2$O$_3$ coating before processing the device sample. After split gate patterning, another layer of 20nm Al$_2$O$_3$ is coated using atomic layer deposition. Then the control gate is patterned with careful alignment with error smaller than 50nm. Finally, the dielectric on the source, drain and split gate pads are etched by Cl$_2$/Ar plasma and BOE for probe test. The detailed fabrication process is provided in Appendix. The scanning electron microscope image of fabricated non-classical MuQFET is shown in Figure 3-8(c) and the dimensions are labeled in Figure 3-8(b).

Figure 3-8 (a) Schematic of Coulomb blockade MuQFET fabrication with split gate and control gate. (b) Schematic of fabricated Coulomb blockade MuQFET. (c) Scanning electron microscope image of a Coulomb blockade MuQFET.
Figure 3-9 Classical $I_D$-$V_G$ measurement of Coulomb blockade MuQFET showing robust modulation from split gate and control gate voltage at 77K.

We first measured the classical $I_D$-$V_G$ of this device and plotted in Figure 3-9. The split gate and control gate can both modulate the carrier concentration and create depletion region. The control gate exhibits less efficient carrier modulation than the split gate due to thicker dielectric. From the split gate separation, fin width and quantum well thickness, the dimension of Coulomb island was roughly estimated to be 80nm×40nm×12nm, which results in less than 15meV Coulomb gap. It is not possible to observe Coulomb blockade at room temperature. Even at 77K Coulomb blockade was not observed for this device. Therefore we conducted the measurement at 4.2 Kelvin using liquid helium in Lakeshore cryogenic probe station.

Compared to the gated nanoparticle transistor, the Coulomb blockade MuQFET has electrical tunable coupling strength between source/drain and the nanodot. The coupling strength continuously becomes weaker when the split gate bias enlarges the depletion region. Depending
on the coupling strength, the device can work in three different modes. In Figure 3-10 (a)(b), we plotted the measured $I_D-V_{CG}$ in both logarithmic scale and linear scale with three different split gate voltages. This plot reveals the short, coulomb blockade and open mode operation of this device at 4.2K. The corresponding electron density and band profile calculated from self-consistent Poisson-Schrödinger simulation in nextnano® is profiled in Figure 3-11 and Figure 3-12. The three modes of operation are: (1) $V_{SG}=0V$, tunnel barriers collapse and the device is a classical MuQFET gated by control gate (short mode). Since the modulation efficiency of control gate is weaker than that of the split gate, the drain current can be kept larger than the peak of Coulomb oscillation and the device is always in ON state in a large $V_{CG}$ range (no less than -1.5V); (2) $V_{SG}=-1V$, the split gates moderately deplete the 1D nanowire resulting in around 2.5MΩ tunneling resistance. From Figure 3-12 and Figure 3-13, it is clear that two tunnel barriers forms and they isolate a nanodot from source/drain Fermi reservoir. When $V_{CG}$ sweeps, the electron energy level of the nanodot periodically match and mismatch the source/drain Fermi level resulting in conductance oscillation (Coulomb blockade mode); (3) $V_{SG}=-2V$, the split gates heavily deplete the MuQFET fin resulting in only background leakage current (open mode). The Coulomb oscillation, if any, is hidden among the background current and noise. The electron density simulation shows that the deletion is so strong that the nanodot even disappears as shown in Figure 3-12.
Figure 3-10 $I_D$-$V_{CG}$ characteristic for three different operation modes in logarithmic and linear scale ($T=4K$).
Figure 3-11 Self-consistent Poisson-Schrodinger simulation of electron density in the MuQFET working in short, Coulomb blockade and open mode (T=4K).
Figure 3-12 Self-consistent Poisson-Schrödinger simulation of conduction band profile in the MuQFET working in short, Coulomb blockade and open mode (T=4K).

Figure 3-13 shows the measured drain conductance ($G_D=I_D/V_D$) as a function of $V_{GS}$ and $V_{DS}$ (stability plot) at Coulomb blockade mode. Using the Coulomb diamond analysis method in Figure 3-4(c), the device parameters can be extracted from the size and the slope of the diamond.
The dot capacitances coupling with the three terminals are $C_S=4\,aF$, $C_D=5.6\,aF$, $C_G=0.3\,aF$ and the tunnel resistance $R_T=4.3\,M\Omega$ if assuming $R_S=R_D=R_T$. These parameters are essential to conduct device simulations for circuit design.

Figure 3-13 Stability plot of MuQFET operating in Coulomb blockade mode at 4.2K. The extracted parameters: $C_S=4\,aF$, $C_D=5.6\,aF$, $C_G=0.3\,aF$.

The Coulomb blockade simulation starting from basic material and device level (material properties, Poisson equation, quantum mechanics and electron transport) is very sophisticated and there is no well established simulation methodology. SIMON 2.0 is a device and circuit simulator using Monte Carlo method [44]. It allows transient and stationary simulations of arbitrary circuits consisting of tunnel junctions, capacitors, resistors and voltage source. The source and drain junctions are tunnel junction with finite resistance and capacitance. The gate terminal is coupled to the nanodot with infinite resistance and finite capacitance. Using the experimental extracted resistance and capacitance parameter, the simulations are shown in Figure 3-14 and Figure 3-15. The simulation does not capture parasitic effects: (1) control gate, not perfectly aligned within the
split gates, modulate the resistance in the source/drain extension region; (2) the control gate fringing field has finite impact on the tunnel junction resistance. Thus compared to the simulated curve, the experimental conductance peak level rises up when $V_{CG}$ sweeps positively. In general, the simulator captures the coupling effects between terminals and dots correctly. It well predicts oscillation period and blockaded region.

Figure 3-14 Comparison of simulations using SIMON 2.0 and experimental results.

Figure 3-15 Stability plot simulated by SIMON 2.0 using parameters extracted from Figure 3-13.
3.5 Device Scaling and Improvement of Coulomb Blockade Temperature

Device scaling is vital to semiconductor industry to manufacture high density, low cost and high performance CMOS chip. For Coulomb blockade devices, dimensional scaling provides similar benefits. More important, device scaling is essential to rise up the operating temperature and realize room temperature Coulomb blockade. The primary challenge to scale the Coulomb blockade MuQFET is the finite resolution of lithography. The EBPG5-HR ebeam writer in Penn State Nanofab can produce ~40 nm etched nanowire and ~80 nm separated split gate at its maximum capability. Further smaller feature greatly suffers from edge roughness patterned by 13 nm beam. With advanced tool Vistec 5200, available in Penn State Nanofab since March 2012, has much better control of edge roughness using sub-5 nm beam. It is able to define 10 nm nanowire and ~20 nm separated split gate with optimized recipe. The process details are provided in Appendix. We measured this device under 77K in Lakeshore cryogenic probe station. Figure 3-17 shows the scanning electron microscope image of a scaled Coulomb blockade MuQFET. The nanowire width is around 13 nm and the split gate is separated by 24 nm gap. Figure 3-17 demonstrates successful program of short, Coulomb blockade and open mode at 77K. The Coulomb oscillations for different V_{DS} are shown in Figure 3-18. The degraded I_{peak}/I_{valley} is observed with increased drain bias. The stability plot is in Figure 3-19 clearly shows four Coulomb diamonds. The extracted capacitance and resistance parameters are listed in Table 3-1. Figure 3-20 shows the temperature effect on the Coulomb oscillations. As temperature increases, the thermal energy starts to overcome the blockaded transport. The I_D-V_{CG} almost loses oscillation characteristic when temperature is above 117K (k_BT=10meV).
Figure 3-16 (a) Top view and (b) tilted view of scanning electron microscope images of Coulomb blockade MuQFET with scaled fin width and split gate separation.

Figure 3-17 Short, Coulomb blockade and open mode operation of MuQFET at 77K.
Figure 3-18 $I_D$-$V_{CG}$ characteristic of MuQFET showing Coulomb oscillation at 77K.

Figure 3-19 Drain conductance stability plot of MuQFET at 77K.

Table 3-1 Device parameters extracted from Figure 3-20.

<table>
<thead>
<tr>
<th>No.</th>
<th>$C_S$ (aF)</th>
<th>$C_D$ (aF)</th>
<th>$C_{CG}$ (aF)</th>
<th>$R_T$ (MΩ)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1.38</td>
<td>0.93</td>
<td>0.241</td>
<td>4.60</td>
</tr>
<tr>
<td>2</td>
<td>1.44</td>
<td>0.96</td>
<td>0.256</td>
<td>2.64</td>
</tr>
<tr>
<td>3</td>
<td>1.45</td>
<td>0.95</td>
<td>0.263</td>
<td>1.67</td>
</tr>
</tbody>
</table>
Figure 3-20 $I_D$-$V_{CG}$ characteristic of Coulomb blockade MuQFET for $T$=77K, 97K and 117K. Coulomb oscillation starts to disappear at above 117K.

Figure 3-21 shows the capacitance components in a Coulomb blockade MuQFET. The split gate capacitance, due to fringing electric field, is usually negligible (<5% of total capacitance). The tunnel junction capacitance $C_S/C_D$ is proportional to the fin width. The data in Table 3-2 confirms that $C_S/C_D$ scales at the same pace with $W_{FIN}$. The reduction of junction capacitance contributes to higher temperature operation. In comparison, $C_{CG}$ has no significant impact to device operating temperature determined by the total capacitance. Yet high gate coupling ratio $C_{CG}/C_{total}$ is preferred in the practical BDD circuit design. In fact, as shown in Table 3-2, $C_{CG}$ naturally scales much slower than $C_S$ and $C_D$. Because control gate wraps around the nanodot, $C_{CG}$ has two components, $C_{CG,\text{TOP}}$ from top and $C_{CG,\text{SIDE}}$ from the sidewall gate. $C_{CG,\text{TOP}}$ is proportional to $W_{FIN}\times D_{SG}$, yet $C_{CG,\text{SIDE}}$ only scales with $D_{SG}$. On the other hand, using thinner dielectric also slows down $C_{CG}$ scaling, but is helpful to improve $C_{CG}/C_{total}$. Table 3-2
shows the Coulomb blockade energy increases by 4X. The estimated nanodot size has been reduced from 34nm to sub-20nm.

Figure 3-21 (a) Capacitance components of the Coulomb blockade MuQFET. (b) Control gate components: \( C_{CG, TOP} \) and \( C_{CG, SIDE} \). \( C_{CG, TOP} \) scales with fin width while \( C_{CG, SIDE} \) does not.

Table 3-2 Full comparison of device geometry and electrical parameters for the device in Chapter 3.4, scaled device in Chapter 3-5 and projected device operating at room temperature.

<table>
<thead>
<tr>
<th></th>
<th>Device in chapter 3.4 (#1104)</th>
<th>Scaled Device in chapter 3.5 (#1307)</th>
<th>Scaling Factor</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>1st diamond</td>
<td>1st diamond</td>
<td>2nd diamond</td>
</tr>
<tr>
<td>( W_{FIN}(\text{nm}) )</td>
<td>40</td>
<td>13</td>
<td>0.3</td>
</tr>
<tr>
<td>( D_{SG}(\text{nm}) )</td>
<td>80</td>
<td>24</td>
<td>0.3</td>
</tr>
<tr>
<td>( T_{OX1}(\text{nm}) )</td>
<td>10</td>
<td>10</td>
<td>1</td>
</tr>
<tr>
<td>( T_{OX2}(\text{nm}) )</td>
<td>20</td>
<td>10</td>
<td>0.5</td>
</tr>
<tr>
<td>( C_{CG}(\text{aF}) )</td>
<td>0.3</td>
<td>0.241</td>
<td>0.256</td>
</tr>
<tr>
<td>( C_{S}(\text{aF}) )</td>
<td>4</td>
<td>1.38</td>
<td>1.44</td>
</tr>
<tr>
<td>( C_{D}(\text{aF}) )</td>
<td>5.6</td>
<td>0.93</td>
<td>0.96</td>
</tr>
<tr>
<td>( C_{\Sigma}(\text{aF}) )</td>
<td>10</td>
<td>2.44</td>
<td>2.66</td>
</tr>
<tr>
<td></td>
<td>16</td>
<td>66</td>
<td>60</td>
</tr>
<tr>
<td>------------------</td>
<td>-----</td>
<td>-----</td>
<td>-----</td>
</tr>
<tr>
<td>( q^2/C_\Sigma ) (meV)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( k_B T ) (meV)</td>
<td>0.344</td>
<td>6.6</td>
<td>6.6</td>
</tr>
<tr>
<td>@4K</td>
<td>@77K</td>
<td>@77K</td>
<td></td>
</tr>
<tr>
<td>( q^2/(C_\Sigma k_B T) )</td>
<td>46</td>
<td>10</td>
<td>9</td>
</tr>
<tr>
<td>Diameter (nm)</td>
<td>34</td>
<td>14</td>
<td>0.0</td>
</tr>
<tr>
<td>( C_{gd}/C_\Sigma )</td>
<td>0.03</td>
<td>0.098</td>
<td>0.092</td>
</tr>
</tbody>
</table>
Besides the Coulomb charging energy, the quantization energy becomes significant when the devices is further scaled, especially for low effective mass system like InGaAs. Figure 3-22 shows the addition energy components from Coulomb charging energy and quantization energy for both In$_{0.7}$Ga$_{0.3}$As and silicon. The quantization energy is calculated using NANOHub Quantum Dot tool [45]. The Coulomb energy is calculated using charged sphere model [46]. The energy and approximate dimension of device #1104 and #1307 listed in Table 3-2 are also marked on the figure. It is clear that the In$_{0.7}$Ga$_{0.3}$As system allows larger dimensions of quantum dot for the same total addition energy required by the working temperature (10k_B T). It is expected that the estimated dimension for room temperature Coulomb blockade in ~2nm in silicon while ~5nm in In$_{0.7}$Ga$_{0.3}$As. The suggested dimensions for the room temperature Coulomb blockade MuQFET is $W_{FIN}=4$nm, $T_{QW}=5$nm, and $D_{SG}=6$nm.

![Figure 3-22 The nanodot addition energy $E_A$ (black) components: Coulomb charging energy $E_C$ (red) and quantized energy level $E_Q$ (blue) for silicon quantum dot.](image-url)
3.6 Path Switching Efficiency of BDD Node

After discussing the device characteristic, this part will look into basic switch behavior in a BDD decision node. In a BDD decision node in Figure 3-7, the logic input $X$ and $\bar{X}$ is used to set opposite state in the left and right path when the split gate bias set the devices in Coulomb blockade mode. Within a period of Coulomb oscillations, the logic 1 state is assigned at peak and the 0 state is located at $V_{\text{peak}}-V_{CC}$. The logic input window $[0, V_{CC}]$ should match $[V_{\text{peak}}-V_{CC}, V_{\text{peak}}]$. We do the following transform:

\[
\begin{align*}
V'_{CGL} &= V_{CG} - (V_{\text{peak}} - V_{CC}) \\
V'_{CGR} &= V_{\text{peak}} - V_{CG} \\
X &= V'_{CGL}/V_{CC} \\
\bar{X} &= V'_{CGR}/V_{CC}.
\end{align*}
\]

The current ratio $\gamma = I_{DL}/I_{DR}$ is a function of $X$, which reaches minimum when $X = 0$ and maximum when $X = 1$. $\eta = \gamma(1)/\gamma(0)$ is defined as switching efficiency. If the two Coulomb blockade devices are perfectly identical, $\gamma(0) = \gamma(1)^{-1}$, and $\eta = \gamma(1)^2 = \left\frac{I_{\text{max}}}{I_{\text{min}}}\right^2$.

Figure 3-23 shows the scanning electron microscope of a fabricated decision node. The two devices were measured at 77K. The Coulomb diamonds are shown in Figure 3-24 and the extracted devices parameters are shown in Table 3-3. Figure 3-25(a) shows the $I_{DL}-V_{CG}$ characteristic of the devices of left and right path. There is 15% current variations and 0.015V voltage shift between the two device characteristics. At 77K, a $V_{CG}$ window of 300mV is large enough to change the current from background level to the first Coulomb peak. After doing voltage transform for the data in this $V_{CG}$ window using Equation , the $I_{DL}$ and $I_{DR}$ as a function of logic input $X$ are plotted in Figure 3-25(b). Figure 3-25(c) shows the current ratio $\gamma = I_{DL}/I_{DR}$ as a function of logic input $X$. The switching efficiency $\eta$ of this decision node is around 70 with 300mV $V_{CC}$ at 77K. However, much sharper Coulomb peaks enable reduction of $V_{CC}$ from
300mV to 100mV to change the current from background leakage to peak. The same analysis is shown in Figure 3-25(d-f) when reduce temperature to 4K. With $V_{CC} = 100$mV, this decision node can achieve switching efficiency $\eta \approx 10^4$. Figure 3-26 compares the switching efficiency for different $V_{CC}$ selection window at 77K and 4K derived from the experimental data. The maximum switching efficiency at 77K is around 80 (from peak to valley). At 4K, the switching efficiency cannot reach theoretical peak to valley maximum because the current cannot go below the background current (~5x10^{-12}A). Thus, the switching efficiency saturates at $10^4$ at 4K.

Figure 3-23 Scanning electron microscope image (false color) of a decision node consisting of two Coulomb blockade MuQFETs in each path.

Figure 3-24 Measured stability plot of the device in the left and right path ($V_{SG} = -0.8$V) at T=77K.

Table 3-3 Capacitance and Resistance parameters extracted from Figure 3-24.

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Left Branch</th>
<th>Right Branch</th>
</tr>
</thead>
<tbody>
<tr>
<td>$G_D$ ($q^2/h$)</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>


<table>
<thead>
<tr>
<th></th>
<th>1st</th>
<th>2nd</th>
<th>1st</th>
<th>2nd</th>
</tr>
</thead>
<tbody>
<tr>
<td>$C_{CG}$ (aF)</td>
<td>0.226</td>
<td>0.240</td>
<td>0.225</td>
<td>0.236</td>
</tr>
<tr>
<td>$C_S$ (aF)</td>
<td>2.39</td>
<td>2.49</td>
<td>3.28</td>
<td>3.41</td>
</tr>
<tr>
<td>$C_D$ (aF)</td>
<td>2.37</td>
<td>2.41</td>
<td>2.51</td>
<td>2.61</td>
</tr>
<tr>
<td>$R_T$ (MΩ)</td>
<td>3.45</td>
<td>2.73</td>
<td>4.45</td>
<td>3.53</td>
</tr>
</tbody>
</table>

Figure 3-25 (a) $I_D-V_{CG}$ characteristic of the devices of left and right path at 77K. (b) $I_D$ is plotted as a function of logic input $X$ after transforming the data in the $V_{CG}$ window in Figure 3-24. (c) $\gamma = I_{DL}/I_{DR}$ is plotted as a function of logic input $X$. (d-f) Path switching at 4K. The $V_{CC}$ can be
reduced from 300mV to 100mV in order to change current from background level to Coulomb peak.

![Graph](image)

Figure 3-26 Switching efficiency as a function of $V_{CC}$.

In summary, this chapter discussed the design and experimental work of the non-classical Coulomb blockade MuQFET. The MuQFET can be reconfigured into short, Coulomb blockade and open mode by electrostatically changing the coupling strength between nanodot and source/drain. Clear 77K Coulomb oscillation has been achieved by scaling the fin width to 13nm and split gate separation 25nm. The fabricated BDD decision node consisting of two Coulomb blockade MuQFETs shows switching efficiency 80 at 77K and over 10000 at 4K.
Chapter 4

Non-Volatile and Reconfigurable MuQFETs

4.1 Non-Volatile MuQFETs Structure Design

The last chapter discussed that the MuQFETs with split gate and control gate can exhibit Coulomb oscillations for BDD logic. Compared to the single electron transistors consisting nanoparticle coated with thin dielectric, the MuQFETs has tunable barrier and can seamlessly transit among short, Coulomb blockade and open mode by programming the split gate voltage. On the other hand, unlike the non-volatile physical barrier, the electrostatic barriers are volatile and programming mode is not retained once the split gate bias is removed. The application of MuQFETs will be limited by the consistent external voltage applied to the split gate in the switching operation. Practically a device that retains the states can achieve zero-static power consumption in idle mode without loss of state. Such a scenario is vital in low-activity and ultra low standby power logic circuits employed in applications such as power-constrained distributed sensor nodes or implantable electronics [47-48]. Therefore this chapter will explore how to achieve both mode programmability and non-volatility in MuQFETs.

Inspired by the memory devices, the approach to achieve non-volatility can be either charge trapping [49] or ferroelectric gate stack [50]. The SONOS-like structures [51] to implement charge trapping in these narrow split gates will go beyond the fabrication capability in university cleanroom. Thus the ferroelectric gate stack is preferred to realize non-volatile programming in MuQFETs. The proposed device structure change is shown in Figure 4-1. A layer of ferroelectric is incorporated into the split gate stack. The polarization of ferroelectric material is dependent not only on the current electric field but also on its history, yielding a hysteresis loop. The ferroelectric film can have a spontaneous nonzero remnant polarization when
the current external electric field is removed after the polarization is activated. Therefore after an initial programming pulse, the remnant polarization in the ferroelectric film may provide the required electric field to deplete the barrier region. Depending on the initial programming voltage, the level of remnant charge in the ferroelectric will set short, Coulomb blockade or open mode in a non-volatile manner. Further, an erasing field in the opposite direction of the remnant polarization can serve to reset the device state for the next possible device programming. This scenario is the key to energy-efficient reconfigurable BDD fabrics [52].

Figure 4-1 A schematic of the non-volatile MuQFET structure.

4.2 Characterization of Sputtered Lead Zirconium Titanate (PZT) Film

Lead zirconium titanate is an inorganic compound with the chemical formula Pb[Zr$_{1-x}$Ti$_x$]O$_3$ (0≤x≤1). Also called PZT, it is a ceramic perovskite material that exhibits marked ferroelectric and piezoelectric properties. PZT-based materials have been used in ultrasound transducers, ceramic capacitors, ceramic resonators, STM/AFM actuators and ferroelectric random access memories (FeRAM) [53]. The crystal structure of PZT depends on the atom
composition and the temperature. The phase change chart of PZT is shown in Figure 4-2 [54]. Above Curie temperature, PZT has a cubic structure. The centro-symmetric crystal structure does not exhibit ferroelectric. Depending on the relative composition of titanium and zirconium, the structure of PZT exhibits a rhomboheral or tetragonal crystal structure below Curie temperature. The tetragonal or rhomboheral crystal structure, distorted along (001) or (111) direction from cubic structure, has broken symmetry along one direction, which allows the titanium or zirconium atom to have a displacement near the central position as shown in Figure 4-3. This displacement allows charge separation between positive and negative charge centers which causes an electric dipole behavior. Localized group of dipoles with parallel orientation are called Weiss domains. The Weiss domains are randomly oriented in the PZT crystal. There is no net polarization due to this randomness. When an external electric field is applied to the PZT the electric dipoles of the domains align roughly in the same direction. The alignment stays to cause remnant polarization even when the external electric field is removed. The phase boundary between rhomboheral and tetragonal structures at the composition Zr:Ti~0.52:0.48 is known to exhibit the best ferroelectric property.
Figure 4-2 Phase diagram of Pb\[Zr_{1-x}Ti_x\]O_3.

Figure 4-3 A schematic of PZT unit cell showing the displacement of Ti or Zr atom.

A PZT MOS capacitors chip was first fabricated and characterized before designing MuQFET process. P-type (doping is around 1×10^{15} cm^-3) silicon substrate cleaned by SC1 and SC2 solution. This clean method will leave a few angstrom of high quality native oxide on silicon substrate. Around 5nm HfO_2 film was deposited on silicon substrate. The HfO_2 film serves as the
dielectric layer to reduce leakage, as well as the diffusion barrier of PZT. PZT deposition can be either sol-gel deposition or RF sputtering. RF sputtering is much easier method to get specified thickness of PZT film compared to the sol-gem deposition. The PZT film was deposited using Kurt-Lesker CMS-18 RF sputtering tool. The single PZT sputtering target is comprised of PbO, TiO2 and ZrO2 in the stoichiometric composition. The sputtering process is kept at low deposition rate (around 1.2nm/min). The targeted PZT thickness is 400nm in this MOS capacitor device. The deposition usually takes several hours. The amorphous PZT was crystallized at 550°C for 2min in oxygen ambient in All-Win 610 RTA system. The MOS cap gate consisting of Pd (20nm) /Au (60nm) is formed using evaporation and lift-off after lithography. For comparison, a sample without PZT sputtering and annealing is also fabricated in parallel.

Figure 4-4 shows the capacitance-voltage characteristic of the samples without and with PZT layer. The sample with PZT layer shows 0.22V hysteresis in the capacitance-voltage loop while the one without PZT layer shows no hysteresis. It is evident that the hysteresis comes from the PZT layer. Figure 4-5 shows the capacitance-voltage loop with voltage rangeing from ±2V to ±10V. Higher voltage induces higher polarization within the PZT layer and causes larger hysteresis. Figure 4-6 shows the capacitance-voltage characteristic with different gate voltage ramping rates in the measurement. The hysteresis voltage shift has negligible relationship with gate voltage sweeping rate, which means ferroelectric switching behavior instead of trapped charge relaxation.
Figure 4-4 Capacitance-voltage characteristic of MOS capacitors without (a) and with PZT layer (b).

Figure 4-5 Capacitance-voltage loop with voltage sweep ranges from ±2V to ±10V.
Based on the results in Figure 4-5, it is possible to estimate the dielectric constant and remnant field of the PZT layer.

The maximum capacitance in the depletion region is calculated without a PZT layer,

\[
1/C_{\text{max}} = (\varepsilon_0 \varepsilon_{\text{high-k}} / d_1)^{-1} + (\varepsilon_0 \varepsilon_{\text{PZT}} / d_2)^{-1} = (\varepsilon_{\text{SiO2}} \varepsilon_0 / EOT_1)^{-1}.
\]

With the PZT layer,

\[
1/C_{\text{max}} = (\varepsilon_0 \varepsilon_{\text{high-k}} / d_{\text{high-k}})^{-1} + (\varepsilon_0 \varepsilon_{\text{SiO2}} / d_{\text{SiO2}})^{-1} + (\varepsilon_0 \varepsilon_{\text{PZT}} / d_{\text{PZT}})^{-1} = (\varepsilon_{\text{SiO2}} \varepsilon_0 / EOT_2)^{-1}
\]

Thus, \((\varepsilon_0 \varepsilon_{\text{PZT}} / d_{\text{PZT}})^{-1} = (\varepsilon_{\text{SiO2}} \varepsilon_0 / EOT_2)^{-1} - (\varepsilon_{\text{SiO2}} \varepsilon_0 / EOT_1)^{-1}\)

\[
\varepsilon_{\text{PZT}} = 1300.
\]

Gate to substrate bias should satisfy

\[
V_g = \varphi_s + \frac{|\sigma_s(\varphi_s)|}{C_{\text{stack}}} - P_d(E_{\text{PZT}}) \frac{d_{\text{PZT}}}{\varepsilon_{\text{PZT}} \varepsilon_0}.
\]
For flat band, surface potential is zero. Si surface charge is zero. Shift of flat band voltage is calculated as

\[ \Delta V_{fb} = -\Delta P_d (0) \frac{d_{PZT}}{\varepsilon_{PZT} \varepsilon_0} = 2P_r \frac{d_{PZT}}{\varepsilon_{PZT} \varepsilon_0}. \]

For a voltage sweep from -2V to 2V, \( \Delta V_{fb} = 0.22V \), so remnant polarization \( P_r = 0.3\mu C/cm^2 \).

For a voltage sweep from -10V to 10V, \( \Delta V_{fb} = 12.1V \), so remnant polarization \( P_r = 17\mu C/cm^2 \).

In the next step, a few calculations are helpful to estimate the required level of programming voltage to initiate the remnant polarization for short, Coulomb blockade and open mode. The cross-section of volatile and non-volatile gate stacks are shown in Figure 4-7. In volatile stack,

\[ V_{sg} = \varphi_{s_{EFF}} (V_{sg}) + \frac{\mid \sigma_{s_{EFF}} (V_{sg}) \mid}{C_{stack1_{EFF}}}. \]

If a PZT layer with remnant polarization is used to create the same depletion charge,

\[ 0 = \varphi_{s_{EFF}} (V_{sg}) + \frac{\mid \sigma_{s_{EFF}} (V_{sg}) \mid}{C_{stack2_{EFF}}} - P_d (E_{PZT}) \frac{d_{PZT}}{\varepsilon_{PZT} \varepsilon_0}. \]

And, the capacitance difference between volatile and nonvolatile stack is from the PZT layer,

\[ \frac{1}{C_{stack2_{EFF}}} = \frac{1}{C_{stack1_{EFF}}} + \frac{d_{PZT}}{\varepsilon_{PZT} \varepsilon_0}. \]

Therefore, from the equations above, the relationship between VSG and required polarization can be expressed as:

\[ \frac{[P_d (E_{PZT}) - \mid \sigma_{s_{EFF}} (V_{sg}) \mid] \varepsilon_{PZT} \varepsilon_0}{d_{PZT}} = V_{sg}. \]
If we consider the delta doping level is $2 \times 10^{12} \text{cm}^{-2}/q=0.32 \text{uC/cm}^2$, the $\sigma_{s,\text{EFF}}$ is negligible compared to polarization that goes to several uC/cm$^2$. Therefore, for open mode ($V_{SG}=-2 \text{V}$), the required polarization is $P_R=6 \text{uC/cm}^2$. And for Coulomb blockade mode ($V_{SG}=-1 \text{V}$), the required polarization is $P_R=2.9 \text{uC/cm}^2$. Figure 4-5 has given an rough estimation of remnant polarization as a function of programming voltage $V_{SG}$ calculated from half of the flatband voltage shift in [-$V_{SG},V_{SG}$] loop. Based on the relationship of remnant polarization and programming voltage, the estimated mode map as a function of programming voltage is shown in Figure 4-8. This map can serve as a guideline of non-volatile MuQFETs programming voltages.

Figure 4-7 Schematics of volatile and non-volatile gate stack of MuQFETs.

Figure 4-8 Map of device operation modes as a function of programming voltage.
4.3 Fabrication of Ferroelectric MuQFETs

The non-volatile, reconfigurable SET was also fabricated on the same strained \( \text{In}_{0.7}\text{Ga}_{0.3}\text{As} \) quantum well heterostructure. The device fabrication flow is described in Figure 4-9. An array of fins 40nm wide is first defined with electron beam lithography and etched by low power \( \text{BCl}_3/\text{Ar} \) in PlasmaThemo Versalock tool. 10nm thick hafnium dioxide (HfO\(_2\)) high-k dielectric was deposited using atomic layer deposition (ALD) at 250°C. 130nm thick \( \text{Pb}[\text{Zr}_{0.52}\text{Ti}_{0.48}]\text{O}_3 \) (PZT) ferroelectric dielectric was deposited in the Kurt Lesker CMS-18 RF sputtering system. Thinner PZT layer makes fabrication easier to shrink the aspect ratio, but the PZT will not crystallize properly in the post annealing if the thickness is less than 130nm. The single PZT sputtering target is comprised of \( \text{PbO}, \text{TiO}_2 \) and \( \text{ZrO}_2 \) in the stoichiometric composition. The sputtering rate is kept at around 1.2nm/min. The amorphous PZT was crystallized at 550°C for 2min in oxygen ambient in All-Win 610 RTA system. After etching the dielectric in the contact region, a tri-layer metal stack comprising of \( \text{Ni} (10\text{nm})/\text{Ge} (30\text{nm})/\text{Au} (80\text{nm}) \) was deposited to form the source/ drain contact using an evaporation and lift-off process. The split gate (SG) electrode pattern with separation distance ranging from 60nm to 500nm was defined by e-beam lithography. The split gate stack comprising of \( \text{Ti}(40\text{nm})/\text{Au}(40\text{nm})/\text{Cr}(150\text{nm}) \) tri-layer metal stack was formed using evaporation and lift-off process. A well-controlled \( \text{CHF}_3/\text{CF}_4 \) PZT dry etch was conducted using split gate metal as a mask and stopped at HfO\(_2\) layer. Typically the chromium mask was consumed and less than 5nm HfO\(_2\) was over-etched. Another 20nm HfO\(_2\) thick was deposited and a top control gate (CG) consisting of \( \text{Ti} (40\text{nm})/\text{Au} (40\text{nm}) \) thick metal stack was patterned using. Finally, the source/drain contacts were opened through the oxide using Cl\(_2\) dry etch. Figure 4-10 shows the tilted scanning electron microscope image of a fabricated SET. There is only one active central fin width connecting source and drain. The neighboring dummy fins are used to reduce electron deflection into the
central fin during patterning. The control gate width was extended around 100nm to compensate for the possible alignment error. The transmission electron microscope image of the plane along the transport direction is shown in Figure 4-10(a). The magnified view of the outlined region of Figure 4-10(b) is shown in Figure 4-10(c). Figure 4-11 shows the energy dispersive X-ray spectroscopy characterization of the chemical composition in the transmission electron microscope image. The HfO₂ has prevented PZT diffusion into the semiconductor layer.

Figure 4-9 A schematic of fabrication process flow of non-volatile MuQFET with ferroelectric gate stack.
Figure 4-10 (a) Tilted scanning electron microscope image of a single electron transistor; (b) Cross-section schematic along transport direction; (b) false colored transmission electron microscope image of cross-section indicated in (a); (c) a magnified view of the outlined region in (b).

Figure 4-11 Energy dispersive X-ray spectroscopy characterization of the chemical composition in the transmission electron microscope image.
4.4 Electrical Characterization and Retention Time Measurement of Ferroelectric MuQFETs

From the split gate separation, fin width and quantum well thickness, the dimension of Coulomb island was estimated to be 60nm×40nm×12nm, which results in approximately 20meV of Coulomb charging energy. Due to the thick PZT layer, it is almost impossible to scale the device to work at 77K. Thus, the measurement was still conducted in a cryogenic probe station at 4.2 Kelvin using liquid helium, sufficiently low to observe the Coulomb Blockade in our devices.

First of all, the device is characterized in a volatile manner as discussed in Chapter 3. In Figure 4-12(a), the $I_D-V_{CG}$ for three different $V_{SG}$ values were measured and plotted for $V_D=1$mV. Both the split gate and control gate leakage were negligible (around $10^{-12}$A). We experimentally confirmed the volatile open, Coulomb blockade and short device operation modes programmed by the split gate voltage. With the device geometry, as confirmed by the TEM image Figure 4-10(b), the corresponding electron density was calculated using a self-consistent Schrödinger Poisson approach in NextNano® simulator as shown in Figure 4-12(b). We could identify the three modes of operation: (1) short mode at $V_{SG}=0$V; (2) Coulomb blockade mode at $V_{SG}=-1.5$V; (3)open mode at $V_{SG}=-3$V. Figure 4-12(c) shows the drain conductance contour as a function of $V_D$ and $V_{CG}$ at $V_{SG}=-1.5$V. The device parameters in Figure 4-12(d) are extracted from the Coulomb diamond size and edge slope. The gate coupling factors $C_G/C_{\Sigma}$ are estimated to be 2.8% and 1.7% for the first and second Coulomb diamond, where $C_{\Sigma}=C_{CG}+C_S+C_D$ is the total capacitance. The total capacitance provides a rough estimate of the island diameter of 32nm and 36nm from the first and second diamonds, respectively, if we approximate the Coulomb island as an isolated disc of radius $r=C_{\Sigma}/8\varepsilon$. The simulated electron density profile in Figure 3(c) shows the Coulomb island diameter to be around 40nm in extent along the transport direction, which is in agreement with estimation from the measured Coulomb diamond. The extracted device
parameters are listed in Figure 3(d). The Coulomb island size, which is mostly controlled by the split gate bias and separation, does not change much with control gate modulation.

Figure 4-12 Programmability of the fabricated SET. (a) $I_D$-$V_{CG}$ for open, Coulomb blockade and shot mode at $V_D=1$ mV; (b) self-consistent Poisson-Schrodinger simulation shows the electron density within the device geometry in Figure 2(c) ($V_{CG}=0$V); (c) Drain conductance contour as a function of $V_{CG}$ and $V_D$ at $V_{SG}=-1.5$V and T=4K (Coulomb oscillation diamond). (d) Device parameters extracted from Coulomb diamond size and edge slope.

Due to the ferroelectric split gate stack, the fabricated SET can be operated in a non-volatile fashion after removal of the split gate bias. Below the Curie temperature, the displacement of Ti or Zr from the central position in the PZT unit cell creates an electric dipole. The dipoles are initially randomly oriented in PZT film after crystallization and cooling. A programming voltage forces these individual dipoles to reorient along the electric field direction (electrical poling). When the programming electric field is removed, the dipoles remain fairly aligned resulting in remnant polarization. The remnant polarization in the PZT ferroelectric dielectric layer will maintain the depletion region in the access region thus retaining the tunnel
resistance values. As a first step, the tunnel resistance as a function of programming voltage was experimentally studied. In this work, the tunnel resistance is extracted from time dependent drain current measurements. It is also the metric to characterize the device retention time. However, the tunnel resistance cannot be directly calculated simply as $V_D/2I_D$ for Coulomb blockade devices due to oscillating current and possible peak shift. Thus, for the tunnel resistance extraction, we used a transistor with the same structure and dimension, but with a larger split gate separation (500nm), fabricated in parallel with the Coulomb blockade devices. It has the same tunnel resistance, but does not operate in Coulomb blockade regime due to the large separation distance between the split gate electrode pair. Figures 4-13 (a-c) illustrate the program, retention and reset modes of operation of the non-volatile SET. During the programming stage ($t<0$), the selected programming pulses of amplitude 0V, -7.5V and -12V were applied to the split gate. For non-volatile operation, in order to sufficiently polarize the PZT, a much larger programming voltage needs to be applied on the split gate as compared to the volatile operation in Figure 3. During the retention stage, the activated remnant polarization maintained the device mode after the programming voltage was removed. In the recovery stage, a split gate voltage of amplitude 2V was used to erase the remnant polarization and to reset the device to its initial state. In Figures 4-13 (a-c), the extracted tunnel resistance is plotted as a function of time for three modes at $V_D=1mV$ and $V_{CG}=0V$. Less than 20% change in the tunnel resistance was observed during the entire 80 minute retention measurement period for the Coulomb Blockade and short operating modes, and no discernible change in tunnel resistance was observed for the open mode. The schematics of electron density and polarizations are shown below the tunnel resistance retention plots in Figure 4-13.
Figure 4-13 (a-c) The split gate bias $V_{SG}$ and measured coupling resistance $RT$ is plotted as a function of time for short, Coulomb blockade and open mode. The schematics below show the remnant polarizations in the ferroelectric layer and electron density distribution in the quantum well. The measurement was done with $V_{DS}=1\text{mV}$, $V_{CG}=0\text{V}$ and $T=4\text{K}$. The device used to extract tunnel resistance has a 500nm split gate separation.

After confirming the non-volatile behavior of three modes programming, we focus on non-volatile Coulomb oscillation measurement. The program strategy is shown in Figure 4-13(b). In Figure 4(d), the $I_D-V_{CG}$ characteristic of the SET Coulomb blockade mode plotted at different times in the retention stage shows that the device maintained non-volatile Coulomb blockade characteristic for more than 40 minutes with partial retention loss. In the Coulomb Blockade mode, the ferroelectric depolarization effects result in loss of remnant polarization over time leading to weaker depletion, which enlarges the Coulomb island and reduces the coupling.
strength to the source/drain reservoirs. This is observed in the form of both reduced Coulomb oscillation period and reduced tunnel resistance as shown in Figure 4-14. This verifies the necessity of using the device with large split gate separation instead of Coulomb blockade device to do tunnel resistance measurement as discussed in Figure 4-13. The drain current of the Coulomb blockade device is not only affected by the tunneling resistance which is a function of $V_{CG}$, $V_D$ and remnant polarization, but also is dependent of the Coulomb period change. It is noted that the current level change over time in Figure 4-14 is faster than the tunnel resistance change in Figure 4-13(b) with no control gate bias. This is due to effect of the fringe electric field emanating from the control gate and terminating on the ferroelectric sidewall. Hence, in addition to the self-depolarization (depolarization field, charge trapping in the ferroelectric) in the split gate stack [55], any fringing electric field from the control gate bias (either $V_{CG}$ sweep in the device measurement or logic input in circuits’ topology) tends to disturb the remnant polarization and degrade the retention characteristics as shown in Figure 4-15. Figure 4-16 shows the tunnel resistance as a function of time at different control gate biases. It is observed that over a control gate voltage range of the first and second coulomb diamond (-1V~0V), the tunnel resistance reduction is less than 10% for a period larger than 5min. The key improvement to avoiding the control gate disturbance in future devices will be the pursuit of reduction of the ferroelectric layer thickness so as to reduce the control gate modulation on the PZT sidewall. Ultra-thin (less than 10nm) ferroelectric dielectrics will allow the split gate metal to shield most of the fringing field and mitigate the disturbance effect from the control gate and increase the retention time.
Figure 4-14 Coulomb oscillations $I_D-V_{CG}$ are measured for different times in retention stage. The programming time scale is shown in Figure 4-13(b). -7.5V pulse programming voltage is removed at $t=0$.

Figure 4-15 Depolarization effects in the non-volatile Coulomb blockade device.
Figure 4-16 Tunnel resistance is plotted as a function of time for different $V_{CG}$. The tunnel resistance reduction is less than 10% for more than 5 min over $V_{CG}$ range from -1V to 0V range for the first and second Coulomb diamond.

Thin ferroelectric film is important to vertical device scaling, as well as retention characteristic improvement. Figure 5-5 shows the schematic of gate fringing electric field using thick and thin ferroelectric film. The thin film allows the split gate metal shield most of the fringing field. In this scenario, the remnant polarization is less likely to be disturbed by the control gate voltage signal. Recently, there are reports in ultra-thin (less than 10nm) ferroelectric dielectrics such as $Zr_{0.5}Hf_{0.5}O_2$ [56] and $BaTiO_3$ [57]. They are more compatible with CMOS fabrication process compared to PZT. The challenges are that these thin film crystallization require either bi-layer TiN stress or lattice match with the substrate. The proper thin ferroelectric film integration will mitigate the disturbance effect from the control gate and increase the retention time. On the other hand, the PZT ferroelectric gate stack needs relatively high supply voltage to perform the programming operation. This could be circumvented by using the complementary ferroelectric capacitor structure where the voltage swing generated by the
capacitive coupling effect of the capacitor pair is large enough to perform the programming action at low supply voltages [58].

Figure 4-17 Schematics of fringing electric field in non-volatile MuQFET with thick and thin ferroelectric films.

In a large BDD fabric, it is preferred to use differential split gate voltage to implement antifuse-like programming strategy [18] to save programming resources. A local reference is needed to realize differential $V_{SG}$. The charge behavior is determined by voltage difference between split gates and channel. Usually the differential voltage does not work as intended in a volatile programming manner (Figure 4-18(a)). For example, a $V_{SG}=V_{SG,REF}$ bias condition would give double gate modulation of channel instead of differential voltage. However, in a non-volatile manner, the remnant polarizations can be established by differential $V_{SG}$. The differential $V_{SG}$ programming is possible in a non-volatile manner if the gate structure is properly designed. It is straightforward to think of using the split gate structure in figure 4-18 (b) with source/drain floating in programming stage. Indeed polarizations can be established according the $V_{SG}-V_{SG,REF}$ if channel pins to no potential. Yet the remnant polarizations in the reference gate tend to cancel the depletion effect of split gate in the retention stage. It is helpful to remove the ferroelectric in the reference gate and use the polarization in split gate to create depletion barriers.
programming stage, \( V_{SG} - V_{SG, REF} \) set the device mode with source/drain floating. Then in the retention stage, the source/drain is biased at certain small voltage according to the location in BDD fabric. The remnant polarizations maintain the device operation mode.

Figure 4-18 (a) Antifuse-like programming strategy proposed in [18]. (b) Schematic of non-ferroelectric SG and reference gate. The differential voltage cannot work as intended. (c) Schematic of ferroelectric SG and ferroelectric reference gate. The polarizations in the SG and reference gate cancel each other in terms of depletion or accumulation. (d) A possible split gate structure for differential programming voltage with ferroelectric SG and non-ferroelectric reference gate.

In summary, this chapter has discussed the experimental feasibility of a programmable non-volatile Coulomb blockade MuQFET. The MuQFET utilizing ferroelectric split gate is experimentally realized based on a multi-gate InGaAs nanowire configuration. The MuQFET exhibits both programmable characteristics and reasonable retention time, which provides a suitable platform for realizing ultra low power reconfigurable BDD logic. Binary decision diagram implemented with programmable non-volatile MuQFETs presents an interesting opportunity for designing future ultra-low power logic circuits. The transistor level
reconfigurability using split gate concept that we have demonstrated in this work is essential to realize reconfigurable BDD architecture to address device to device variation, while the non-volatility feature stemming from incorporating a ferroelectric dielectric in the split gate stack is paramount for addressing static power consumption.
Chapter 5

Ultra Low Power Sensing For Cascaded BDD Stages

5.1 Overview of Hybrid BDD Logic Circuit

The primary aim of this work is to explore device solutions for ultra low power logic. Chapter 2 reveals the short channel In$_{0.7}$Ga$_{0.3}$As MuQFET is in quasi-ballistic transport regime. Taking advantage of both multi-gate and high mobility channel, the compressively strained In$_{0.7}$Ga$_{0.3}$As MuQFET shows good scalability as well as superior transport properties. The energy-delay metrics shows that the In$_{0.7}$Ga$_{0.3}$As MuQFET is a promising substitute of silicon transistor for sub-500mV applications. In Chapter 3, the MuQFETs with split gate and control gate experimentally shows robust programmability among short, Coulomb blockade and open modes. The multi-functional MuQFETs allows reconfigurable mapping of logic functions into BDD hexagonal fabrics. Furthermore, the ferroelectric gate stack was experimentally integrated into Coulomb blockade MuQFETs in Chapter 4. The non-volatile feature is essential to share resources and achieve zero standby power in the programming control circuits. Based on these devices, we proposed Coulomb blockade devices co-designing with reconfigurable BDD logic architecture for sub-300mV logic. The Coulomb blockade devices are employed in a reconfigurable BDD fabric to implement logic functionality.

Besides the BDD logic fabric, a practical logic system requires peripheral circuitry including the address decoders to pass the programming voltage to the targeted device, as well as sense amplifiers to recover the signal swing for next stage. Figure 5-1 shows a schematic of a complete BDD logic circuit. The address decoders are can be designed in a similar approach as read-write memories [59] and they are mostly idle due to infrequent programming activities for
these non-volatile devices. However, sense amplifier is the main power consumption in hybrid circuit since there is no ground path in the BDD logic fabric [52, 60-61]. The classical MuQFET is a suitable low power device solution for the sense amplifier circuits. This chapter will give an example of traditional current controlled sense amplifier circuit and analyze the energy-delay metric. Further, possible solutions to improve the signal to noise ratio in the sense amplifier will be briefly discussed.

![Diagram of a reconfigurable BDD logic stage. The programming circuits in blue color are mostly idle.](image)

Figure 5-1 A schematic of a reconfigurable BDD logic stage. The programming circuits in blue color are mostly idle.

### 5.2 Traditional Sense Amplifier and Energy-Delay Benchmark of Hybrid BDD Circuit

It has been proposed using BDD stack to implement Boolean logic functions, followed by a differential CMOS sense amplifier consisting either silicon or III-V transistors in order to reduce leakage and perform amplification to drive the next BDD logic stack [38,46-47]. There are quite a few sense amplifier designs in literatures [60-61] for pass transistor logic and read-write memories. The driver and sense amplifier may consist of MOSFETs or classical MuQFETs.
Figure 5-2 shows a schematic of a possible low supply voltage BDD logic stage with a current-controlled latch sense amplifier proposed by Saripalli et al [38]. The root of the BDD stack is driven with a supply voltage with 125mV, and the sense amplifier is driven with voltage ranging from 150mV-250mV. The programming control circuit is idle.

Based on the experimental extracted parameters in Figure 3-13, the \( I_D-V_{CC} \) was simulated in SIMON and populated into a look-up-table, and a Verilog-A look-up-table model is created for the Coulomb blockade device. The classical MuQFET and FINFET was used calibrated Sentaurus model. Circuits are built using instances of the Verilog-A device model and are simulated using Cadence® Spectre®. The details of simulation are published by Saripalli et al [38]. Usually, the static energy is the main energy consumption in BDD-sense amplifier circuit. In the BDD-sense amplifier circuit, beside the small gate leakage, the leakage paths only exist in driver and sense amplifier, which is independent of circuit complexity. In CMOS, every logic
gate has leakage current from power supply to ground. Therefore, sufficient circuit complexity allows hybrid BDD to outperform CMOS when static power dominates. Figure 5-3 compares the energy-delay metrics of 8-input XOR logic using both silicon FINFET and III-V MuQFET complementary gate and BDD-sense amplifier logic. In the CMOS trend, the energy first decreases with supply voltage due to reduction of dynamic part. Then the curve rises due to static energy increases with supply voltage. It is noted that both CMOS and sense amplifier energy are dominated by static energy when supply voltage is scaled below 0.25V. The energy delay performance of the BDD logic with sense-amplifier already shows 50% and 22% reduction in minimum energy compared to silicon FINFETs and III-V MuQFETs complementary logic in this 8-input XOR. More complexity will allow more significant energy saving in BDD-sense amplifier circuit. On the other hand, the drawback of BDD circuit is that the delay is not optimized level for high performance application.

Figure 5-3 Energy-delay of 8-input XOR logic using complementary gates and hybrid MuQFET BDD with sense amplifier.
5.3 Possible Low Power Sensing Using Stochastic Resonance

Chapter 5.2 has discussed the sense amplifier at the terminal node of BDD stack to recover the signal to noise ratio and drive the next BDD logic stage. Besides the voltage swing problem, the signal to noise ratio (SNR) might get degraded due to finite switching efficiency at each decision node. And SNR get worse when the dimensions of BDD fabric increase. Development of novel sensing techniques incorporated with low power sense amplifier is required for practical logic applications.

Stochastic resonance is a phenomenon wherein a signal, that is normally too weak to be detected by a sensor, can be boosted by adding white noise to the signal [61-62]. Stochastic resonance has been observed in many electronic, electromagnetic, physical or biological systems. Usually there are several requirements for stochastic resonance: (1) a threshold under which the signal is not detectable; (2) white noise self-correlation time (1/bandwidth) has to be adequately smaller than system characteristic time; (3) input signal period is sufficiently longer than the system characteristic time. The white noise can be either from intrinsic device noise or external white noise source.

Whether stochastic resonance can effectively improve SNR is still under debates [63-65]. Luchinsky et.al [63] has theoretically proven that the SNR of the output must be worse than that of the input in small signal regime. As for large signal regime, the linear response theory is no longer valid. Some experimental and theoretical studies have been able to show significant SNR improvement for large signal response [66-68]. Among all these, level crossing detector (LCD) was proposed as the most efficient stochastic resonator that is able to significantly improve SNR up to 2-3 orders [67-68].

The LCD is a very simple unit of electronics widely used in measurement techniques and FM radios. Its fires neurons in the following way: a short uniform spike with duration τ₀ is
initiated at its output whenever the voltage at its input goes through the threshold in the increasing direction. The SNR of output can be better than the input if the following conditions are satisfied: (1) signal amplitude is larger than the noise rms amplitude; (2) noise rms amplitude is smaller than the offset between signal low level and threshold; (3) signal amplitude plus noise rms exceeds the threshold; (4) LCD pulse duration $\tau_0$ is much larger than the noise self-correlation time $(1/f_0)$. LCD can serve as a filter to remove noise in the sense amplifier between BDD stages. LCD is independent of signal frequency due to its non-dynamic stochastic resonance. Figure 5-4 shows a simulation that a signal with amplitude 9 in arbitrary unit, mixing with white noise with rms amplitude 2, goes through a LCD resonator with threshold 10. The input and output time domain waveform and power density spectrum are plotted. The system reaches resonance condition when the firings at high level are very frequent, as well as the wrong firings at the low level are suppressed. It can be seen in Figure 5-4(b) that the output is recovered to clean square wave. Comparing the power spectrum density of input and output in Figure 5-4(c) and (d). The SNR of the output is improved due to noise level is suppressed by 10dB. There is some noise dominated by Jitter noise and rare random firing in low signal level in the output.
Figure 5-4 A simulation of improvement of SNR when signal passes through LCD stochastic resonator. With arbitrary unite, signal amplitude is 9, noise amplitude is 2, threshold is 10. Signal frequency is 1Hz and sampling rate is 10000s\(^{-1}\). The plots show (a) input signal, (b) output signal, (c) power spectrum density of input signal and (d) power spectrum density of output signal.

Figure 5-5 shows a proposed sense amplifier design based on the traditional amplification circuit and LCD stochastic resonator. The threshold of the resonator is set at initial signal swing. The output swing Y\(_1\) from the BDD stage is partially recovered. The swing of Y\(_2\) is close to still under the threshold in the amplification circuit. The LCD filters the noise of Y\(_2\) and set the swing of the output Y to the threshold exactly matching the initial signal swing.
Figure 5-5 Sense amplifier consisting of amplification circuit and LCD resonator. The signal $Y_1$ loss swing in logic operation in BDD fabric compared to initial signal $X$. The amplification circuit partially recovers the swing and the LCD resonator utilize the stochastic resonance to improve signal to noise ratio and fully recover the signal swing in the output $Y$.

On the other hand, besides the possible sensing improvement in the sense amplifier, the Coulomb blockade phenomenon naturally gives a threshold in the Coulomb blockade devices. The single electron stochastic resonance has already been reported in literatures [61-62]. Parallel systems are able to effectively enhance signal to noise ratio due to the stochastic nature of white noise. Thus, there is also an opportunity to do architecture innovation of parallel devices utilizing stochastic resonance effect in the BDD logic stage. Although how to use the stochastic resonance effect in the BDD stage is very challenging and still lack of clear solution. A series of preliminary studies of single electron stochastic resonance were conducted and described below.

**Preliminary Results of Single Electron Stochastic Resonance**

The stochastic resonance at single device level was studied in simulation using SIMON 2.0, which allows tuning of intrinsic noise level by changing temperature. In Figure 5-6, a single electron box is used to simulate the single electron stochastic resonance. In the stationary DC simulation, the $1^{st}$ electron charges into the nanodot at 0.2V bias, which is the threshold in this
system. The input signal offset is 0V and the amplitude is 0.02V, which is much smaller than the threshold. Thus there is no tunnel event without any thermal noise as shown in Figure 5-6. If temperature is raised, the thermal noise can excite electrons into the nanodot. The simulation result at T=25K in Figure 5-7 shows strong correlation between input and output signal. However, if the thermal noise is greater than the optimal level, the noise itself negatively impact the signal to noise ratio in the output Q(t), as shown in the chart at T=300K. The normalized input-output correlation between can be calculated as

\[ C = \frac{\langle S_{IN}S_{OUT} \rangle - \langle S_{IN} \rangle \langle S_{OUT} \rangle}{\sqrt{\langle S_{IN}^2 \rangle - \langle S_{IN} \rangle^2} \sqrt{\langle S_{OUT}^2 \rangle - \langle S_{OUT} \rangle^2}} \]

Figure 5-8 shows the correlation between input V(t) and the output Q(t) as a function of simulation temperature T. The optimal thermal noise level is achieved at T=25K. However, if the practical charge detector sensitivity is concerned, the 5×10^{-29} C is hard to capture by most equipment. Therefore, it is useful to consider a concept called detector threshold. In this simulation, the detector threshold is set at 1×10^{-21} C, which describes intrinsic the root mean square noise amplitude in the detector. The resonance noise amplitude shifts to higher value due to the detector threshold.

Figure 5-6 A schematic of single electron box simulation. The 1st electron charges at 0.2V in the stationary DC simulation.
Figure 5-7 Simulation results of nanodot charge.

Figure 5-8 Correlation between input V(t) and output Q(t) as a function of thermal noise level.
Besides the simulation, experimental work in exploring the stochastic resonance was also conducted in the fabricated Coulomb blockade device. It is proffered to correlate the output current with the input voltage in experimental setup due to the difficulty in detecting the charge in the nanodot. Since there are no bi-stable states in the $I_D$-$V_{CG}$, it is not likely to observe enhanced $I_D$-$V_{CG}$ correlation with optimal noise level. However, the $I_D$-$V_D$ provides a Coulomb blockade and linear region similar to MOSFET OFF and ON states in transfer characteristic. The experimental setup is shown in Figure 5-9(a). The Agilent 81150a function generator provides the drain bias has three components: (1) offset voltage $V_0=0$; (2) input signal $V_{\text{SIGNAL}}(t)$, square wave with 40mV$_{\text{PP}}$ amplitude; (3) white Gaussian noise $V_{\text{NOISE}}(t)$. The offset and input signal generated from Channel 1 is coupled with noise generated from Channel 2. The digital oscilloscope with 1MΩ impedance is used to detect the source to drain current. Figure 5-9(b) shows the $I_D$-$V_D$ characteristic of the Coulomb blockade MuQFET at 4K. The signal to the drain is within the Coulomb blockade region. Figure 5-8(c) shows the time dependent input and output signal stored in the oscilloscope at $V_{\text{NOISE}}=0$, 30mV and 50mV. Figure 5-9(d) shows the input-output correlation as a function of noise root mean square amplitude. The results shows moderate noise indeed helps weak signal detection. The correlation reaches a peak when the resonance noise amplitude provides the hopping rate roughly equal to the frequency of the input noise. Beyond the resonance noise amplitude, the increased noise amplitude lowers the correlation between the output and input level. The measured resonance noise level is 30mV in this system.
Figure 5.9 (a) Schematic of experimental setup to measure stochastic resonance in Coulomb blockade devices. Input impedance of oscilloscope is 1MΩ. (b) $I_D-V_D$ characteristic at 4K, $V_{SG}=-0.8\,\text{V}$, $V_{CG}=0\,\text{V}$. Frequency of the input square wave is 100Hz, offset is 0V and amplitude is 40mV<sub>PP</sub>. (c) Output wave of oscilloscope as a function of time. (d) Correlation between output and input waveform is plotted as a function of noise rms amplitude.
Appendix A

Device Fabrication Process Recipe

The general process flow was already discussed in Chapter 2-4. In the Appendix, the details of each process module are listed

1. Source/drain metal stack and alignment marker

A. Use IPA/acetone to clean the surface if the surface does not react with the solution;
B. Spin MMA El 11 solution at 4000rpm for 45s, or MMA El 6.5 solution at 2000rpm for 60s;
C. Bake sample at 150 °C for 3min;
D. Spin PMMA A3 solution at 4000rpm for 45s;
E. Bake sample at 180 °C for 3min;
F. Mount the sample on to the Vistec 5200 lithography tool holder #3. Align sample under microscope if needed. The angle error must be smaller than 0.2°.
G. Find the alignment marker if alignment is needed. Make sure the tool can properly calibrate the substrate and give translation and transpose correction.
H. Fracture the .gds mask to .gpf layout files. The resolution can be 5nm for the small feature, and 50nm for the large feature. The beams are 100nA for large feature and 0.5nA for small feature. Expose the sample with e-beam dose 280-300uC/cm² for the large feature and 340-400 uC/cm² for the small feature. It is recommended to test dose array before defining small feature.
I. Develop in MIBK:IPA=1:1 solution for 1min. Dip in IPA for 15s and rinse with DI water.
J. Check the pattern under microscope. If some part of the pattern is not fully developed, do another 5-30s develop in MIBK:IPA=1:1 solution.
K. Load developed sample into Semicore evaporator chamber. Place metals into the e-beam evaporation chuck or thermal evaporation boat

L. Evaporate metal at moderate rate (0.5-1.3A/s) when the pressure is reduced less than 2×10^-6 Torr.

M. Cooling the chamber for 20min before open the chamber.

N. Place sample into heated remover PG (80 °C water bath) and wait at least 1h.

O. Rinse the sample and check under microscope. The lift-off process has around 10% failure rate. If the lift-off is not successful, try to use ultrasonic to treat the sample for half an hour and check.

P. Place into the sample into the All-win AG 610 RTA and do 350C/90s annealing for Ni/Ge/Au diffusive contact. If the contact is based on Ti/Au on n++ layer, do not anneal.

II. Fin definition and isolation trench

The following process is based on positive resist and mask design in a negative tone.

A. Use IPA/acetone to clean the surface if the surface does not react with the solution;

B. Spin PMMA A3 solution at 2000rpm for 60s. This gives around 200nm PMMA etch mask. If it is not sufficient in the RIE process, spin another layer PMMA on top.

C. Bake sample at 180 °C for 3min;

D. Mount the sample on to the Vistec 5200 lithography tool holder #3. Align sample under microscope if needed. The angle error must be smaller than 0.2°.

E. Fracture the .gds mask to .gpf layout files. The resolution can be 5nm for the small feature, and 50nm for the large feature. The beams are 100nA for large feature and 0.5nA for small feature. Expose the sample with e-beam dose 340uC/cm² for the large feature and 340-360 uC/cm² for the small feature. It is recommended to test dose array before defining small feature.

F. Develop in MIBK:IPA=1:3 solution for 1min. Dip in IPA for 15s and rinse with DI water.
G. Check the sampler under microscope. It is very likely that the sample is not fully developed. Develop another 5s and check again. If needed, several develop loops are required.

H. Mount the sample onto 6inch silicon carrier wafer and load into PT Versalock tool.

I. Run the existing InGaAs etch recipe under “Datta” folder. Check the etch conditions: pressure= 2mTorr, T=25C, BCl\textsubscript{3} flow=15sccm, Ar flow=45sccm, RF power 1=50W, RF power 2=75W, DC bias=0, etch time=270s. This etch MuQFET wafer by 60nm. Do purging twice before unloading sample.

J. Use hot remover PG to remove photo resist. Check under optical microscope and examine using scanning electron microscope if necessary.

III. Atomic layer deposition of HfO\textsubscript{2} and Al\textsubscript{2}O\textsubscript{3} using Cambridge Savannah ALD system.

A. Set the deposition temperature at 250 °C and stabilize the temperature. Do a 20 cycle’s dummy run. Make sure the water and metal precursor pulses showing up.

B. Clean the wafer with 1:50 H\textsubscript{2}SO\textsubscript{4} solution and load into the ALD chamber immediately.

C. Run the existing recipe of Al\textsubscript{2}O\textsubscript{3} or HfO\textsubscript{2}. The deposition rate is around 1A/s.

IV. Gate metal stack.

In general, the gate metal process is similar to the source/drain metal. Just deposit the correct metal (Pd/Au or Ti/Au). The split gate formation is a bit complicated and discussed in separate part.

V. Ultra fine features: fin with ~10nm width and split gate with ~25nm separation

The process to form split gate is based on process II and process I. However, due to the small separation between the split gate fingers, the split gate often merges without opening a gap. And often, the fabricated dimension is not the mask dimension. To solve this problem, one needs to do
a dose array test from 260-450uC/cm², and check the pattern under scanning electron microscope after lift-off. The process may vary a lot due to uncontrollable conditions in the facility. It is recommended to do the dose test 1-2 days before the split gate patterning and pick up the dose that gives best resolution. On the other hand, one needs to have sufficient tolerance of process variation in the mask design. A good approach is to design multiple devices with a series of fin widths and split gate separation increasing from 10nm to 200nm by 20nm step. Pick up the right device under scanning electron microscope. Do the post pad wiring process.

VI. HfO₂ and Al₂O₃ etch
A. Back the sample at 180 ° C if the sample can sustain this temperature.
B. Load into PT Versalock tool and run the Al₂O₃ etch recipe. Check the conditions: pressure=5mTorr, RF1 power=75W, RF2 power=500W, Cl₂ flow=10sccm, Ar flow=40sccm. The etch rate is around 10nm/min
C. Dip into BOE 1:10 for 5s to remove residual oxide.
D. Use hot remover PG to strip resist.

VII. PZT deposition, annealing and etch
A. Load the sample into the Kurt-Lesker CMS-3 sputtering tool. Run the default PZT sputtering recipe developed by tool administrator. Contact the tool administrator to install PZT target 1 day before PZT deposition.
B. Anneal in 550°C for 2 min in oxygen ambient in All-Win 610 RTA system.
C. Etch with the etch recipe: pressure=5mTorr, RF1 power=100W, RF2 power=700W, CF₄=50sccm, Ar=20sccm. The etch rate is around 100nm/min. Make sure do a etch rate test on dummy sample.
Appendix B

Tools Used for Device Fabrications

Semicore Evaporator

Kurt-Lesker CMS-18 Sputtering System

Cambridge Savannah ALD

All Win 610 RTA

PT Versalock Etch Tool

Vistec 5200 Ebeam Lithography System
Appendix C

Nextnano Code for 2D Self-Consistent Poisson-Schroedinger Simulation

! Edit the device structure, grid, and quantum region if needed.

!***** OVERALL SIMULATION PARAMETERS ****************************

! so far only dimension = 1 is possible
! orientation specifies the axes which are simulated

$simulation-dimension
  dimension = 2
orientation = 1 1 0
Send_simulation-dimension

$global-parameters
  lattice-temperature = 300d0 ! Kelvin
Send_global-parameters

$numeric-control
  simulation-dimension = 2
Send_numeric-control

! Flow control is the possibility to control the actual computation. 
! Sometimes it is faster to first calculate the potential classically and 
! after that do the Schroedinger.
! For kp solution it is almost impossible to calculate current because of 
! the amount of time needed. So a solution is to take a classical solution 
! first (scheme 4), save the data in output-raw-data and then take scheme 3 !
! to read in data and solve kp.
!
! flow-scheme 1:  1. calculate nonlinear Poisson classically 
!  2. calculate current classically 
!  3. calculate nonlinear Poisson as specified in input
!
! flow-scheme 2:
!  1. calculate nonlinear Poisson as specified in input 
!  2. calculate current as specified in input
!
! flow-scheme 3:
!  1. read in potentials and Fermi levels 
!  2. calculate eigenfunctions as specified in input 
! (you have to specify the correct name of the directory)
!
! flow-scheme 4:
!  1. calculate nonlinear Poisson classically 
!  2. calculate current classically

$simulation-flow-control
  flow-scheme = 2

raw-directory-in = raw_data1/
raw-potential-in = no
strain-calculation = zero-strain-amorphous
Send_simulation-flow-control

$domain-coordinates
domain-type = 1 1 0
x-coordinates = -17.5d0 17.5d0
y-coordinates = -10d0 60d0
hkl-x-direction-zb = 1 0 0
hkl-y-direction-zb = 0 1 1
pseudomorphic-on = InP
growth-coordinate-axis = 0 1 0
Send_domain-coordinates

! The domain Type in 1D is usually 0 0 1, which means that the simulated dimension
! is the 0 0 1 axis.
! z-coordinates specifies the size of the simulated region in [nm]
! pseudomorphic-on specifies the substrate material and therefore determines strain

***** END OVERALL SIMULATION PARAMETERS

***** REGIONS AND CLUSTERS

!We specify 9 regions in the simulation area.
!As you can see they do not completely fill the simulation area. The resulting rest
!area is automatically assigned as region number 10.
!So you have always one region more than you actually specified.
Regions

!InP ext
region-number = 1 base-geometry = rectangle region-priority = 1
x-coordinates = -7.5d0 7.5d0
y-coordinates = -10d0 0d0
!InAlAs bot
region-number = 2 base-geometry = rectangle region-priority = 1
x-coordinates = -7.5d0 7.5d0
y-coordinates = 0d0 29d0
!InAlAs delta
region-number = 3 base-geometry = rectangle region-priority = 1
x-coordinates = -7.5d0 7.5d0
y-coordinates = 29d0 30d0
!InAlAs top
region-number = 4 base-geometry = rectangle region-priority = 1
x-coordinates = -7.5d0 7.5d0
y-coordinates = 30d0 32d0
!InGaAS channel
region-number = 5 base-geometry = rectangle region-priority = 1
x-coordinates = -7.5d0 7.5d0
y-coordinates = 32d0 46d0
!InAlAs cap
region-number = 6 base-geometry = rectangle region-priority = 1
x-coordinates = -7.5d0 7.5d0
y-coordinates = 46d0 48d0
!InP cap
region-number = 7 base-geometry = rectangle region-priority = 1
x-coordinates = -7.5d0 7.5d0
y-coordinates = 48d0 50d0

!metal1
region-number = 8 base-geometry = rectangle region-priority = 1
x-coordinates = -17.5d0 17.5d0
y-coordinates = 55d0 60d0

!metal2
region-number = 9 base-geometry = rectangle region-priority = 1
x-coordinates = -17.5d0 -12.5d0
y-coordinates = 0d0 55d0
!metal2
region-number = 10 base-geometry = rectangle region-priority = 1
x-coordinates = 12.5d0 17.5d0
y-coordinates = 0d0 55d0

$end_regions

!-----------------------------------------------------!
! For every boundary between regions, there has to exist a grid-line.
! And between these grid-lines there are a certain number of nodes, which determine
! the resolution of the simulated region.
! In order to specify inhomogeneous grids you can use a grid factor different from one
! This means that the distance between each node is increased by this factor from i to i+1
!-----------------------------------------------------!
$grid_specification
grid-type = 1 1 0
x-grid-lines = -17.5d0 -12.5d0 -7.5d0 7.5d0 12.5d0 17.5d0 !
!+++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++!
x-nodes = 5 5 60 5 5 ! in the interior, 0.5 nm gridding, else 1 nm gridding
lx-nodes = 24 24 9 24 24 ! 1 nm gridding
lx-nodes = 12 12 9 12 12 ! in the interior, 1 nm gridding, else 2 nm gridding (for k.p)
!lx-nodes = 12 6 5 6 12 ! in the interior, 1 nm gridding, else 2 nm gridding (for k.p)
!+++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++!
x-grid-factors = 1d0 1d0 1d0 1d0 1d0 !

y-grid-lines = -10d0 0d0 29d0 30d0 32d0 46d0 48d0 50d0 55d0 60d0 !
!+++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++!
y-nodes = 10 29 1 2 14 2 2 5 5 ! in the interior, 0.5 nm gridding, else 1 nm gridding
ly-nodes = 24 24 9 24 24 ! 1 nm gridding
ly-nodes = 12 12 9 12 12 ! in the interior, 1 nm gridding, else 2 nm gridding (for k.p)
ly-nodes = 12 6 5 6 12 ! in the interior, 1 nm gridding, else 2 nm gridding (for k.p)
!+++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++!
y-grid-factors = 1d0 1d0 1d0 1d0 1d0 1d0 1d0 1d0 1d0

Send_grid_specification

!-----------------------------------------------------!
! A cluster is a group of regions. Every region has to belong to a cluster, but a
! cluster can contain several regions. This is useful, if you want to construct more
! complicated objects of more regions, which have the same material.
$region
cluster-number = 1  region-numbers = 1 !InP  ext
cluster-number = 2  region-numbers = 2 3 4 6 !InAlAs
cluster-number = 3  region-numbers = 5 !InGaAs
cluster-number = 4  region-numbers = 7 !InP
cluster-number = 5  region-numbers = 8 9 10 !metal
cluster-number = 6  region-numbers = 11 !high-k
Send_region-cluster

****** END REGIONS AND CLUSTERS *********************************************************

****** MATERIALS AND ALLOY PROFILES *********************************************************

!---------------------------------------------------------------!
!All materials used in the simulation region, are listed here. A material has to
!be assigned to each cluster.
!In the case of alloys, an alloy function has to be specified.
!---------------------------------------------------------------!
$material
material-number = 1
material-name = InP
cluster-numbers = 1 4

material-number = 2
material-name = Al(x)In(1-x)As
cluster-numbers = 2
alloy-function = constant

material-number = 3
material-name = In(x)Ga(1-x)As
cluster-numbers = 3
alloy-function = constant

material-number = 4
material-name = TaSiO-III
cluster-numbers = 6

material-number = 5
material-name = Metal
cluster-numbers = 5
Send_material

$alloy

material-number = 2
function-name = constant
xalloy = 0.48d0
material-number = 3
function-name = constant
xalloy = 0.53d0
Send_alloy

$doping
doping-function-number = 1 ! acts as separator
doping-concentration = 2d1 !2E19 doping
position = 0d0 1d0

Send_doping-function

impurity-number = 1 ! properties of this impurity type have to be specified later
impurity-type = n-type ! n-type, p-type, trap
impurity-name = my-name ! a name (for later use - planned to read params from data base)
number-of-energy-levels = 1 ! number of energy levels of this impurity
energy-levels-relative = 0.0058d0 ! energy relative to `nearest` band edge (n-type -> cond.band, else val.band)

degeneracy-of-energy-levels = 2 ! degeneracy of energy levels

Send_impurity-parameters

poisson-boundary-conditions
! gate
poisson-cluster-number = 1 ! an integer number (dense numbering as usual)
region-cluster-number = 5 ! an integer number which refers to an existent region-cluster
applied-voltage = 0.00d0 !o! apply voltage to poisson-cluster (required for Dirichlet)
boundary-condition-type = Ohmic
contact-control = voltage
!schottky-barrier = 0.576d0

!sub
poisson-cluster-number = 2 ! an integer number (dense numbering as usual)
region-cluster-number = 1 ! an integer number which refers to an existent region-cluster
applied-voltage = 0.00d0 !o! apply voltage to poisson-cluster (required for Dirichlet)
boundary-condition-type = Ohmic
contact-control = voltage
!schottky-barrier = 0.576d0

Send_poisson-boundary-conditions !o!

voltage-sweep
sweep-number = 1
sweep-active = yes
poisson-cluster-number = 1
step-size = 0.1d0
number-of-steps = 5
data-out-every-nth-step = 1

Send_voltage-sweep

****** END MATERIALS AND ALLOY PROFILES
*****************************************************
### Quantum Regions and Clusters

**Quantum-regions**

- **region-number**: 1
- **base-geometry**: rectangle
- **x-coordinates**: -8.5d0 8.5d0
- **y-coordinates**: 0d0 51d0

**Send_quantum-regions**

**Quantum-cluster**

- **cluster-number**: 1
- **region-numbers**: 1
- **deactivate-cluster**: no

**Send_quantum-cluster**

### Quantum Models

**Quantum-model-holes**

- **model-number**: 1
- **model-name**: effective-mass
- **cluster-numbers**: 1
- **valence-band-numbers**: 1 2 3
- **max-eigenvalue**: 100 100 100
- **max-energy**: 1d0 1d0 1d0
- **number-of-eigenstates-per-band**: 10 10 10
- **boundary-condition-001**: Neumann
- **boundary-condition-001**: Dirichlet
- **method-of-brillouin-zone-integration**: simple-integration
- **num-kp-parallel**: 100

**Send_quantum-model-holes**

**Quantum-model-electrons**

- **model-number**: 1
- **model-name**: effective-mass
- **model-name**: 8x8kp
- **cluster-numbers**: 1
conduction-band-numbers = 1 2 3  
! to select bands (minima) handled in Schrödinger equation
separation-model = eigenvalue  
! to determine separation between classic and quantum density
('eigenvalue','energy','edge_model')
!max-eigenvalue = 100 100 100  
! has to be present but is ignored !!
max-eigenvalue = 50  
! has to be present but is ignored !!
maximum-energy-for-eigenstates = 1d0 1d0 1d0  
! has to be present but is ignored !!
max-energy = 1d0  
! has to be present but is ignored !!
number-of-eigenvalues-per-band band (minimum) = 10 10 10  
! how many eigenenergies have to be calculated in each band (minimum)
number-of-eigenvalues-per-band band (minimum) = 50  
! how many eigenenergies have to be calculated in each band (minimum)
maximum-energy-for-eigenstates = 1d0 1d0 1d0  
! has to be present but is ignored in separation model : 'eigenvalue'
maximum-energy-for-eigenstates = 1d0  
! has to be present but is ignored in separation model : 'eigenvalue'
quantization-along-axes = 1 1 0  
! zero's and one's: to select quantization direction|plane|3D
boundary-condition-001 = Neumann  
! Neumann or (Dirichlet|dirichlet|DIRICHLET). Nonsens input means Neumann (default)
boundary-condition-001 = Dirichlet  
! Neumann or (Dirichlet|dirichlet|DIRICHLET). Nonsens input means Neumann (default)
method-of-brillouin-zone-integration = simple-integration  
! 'special-axis' (only for 0001 quantization direction in wurtzite), 'simple-integration', 'gen-dos'
um-kp-parallel = 100  
! number of k points for brillouin-zone discretization
Send_quantum-model-electrons

! ***** END QUANTUM MODELS *****************************************
!parameter: cb001: conduction band 1
! qr001: quantum region 1
! sg001: schroedinger equation 1
! min001: minimum eigenvalue
! max010: maximum eigenvalue
! deg001: number of subsolution
! _dir: boundary condition (dir,neu)
!
the file 'sg-structure.dat' provides some information about the
structure of the 1-band solutions.
meaning of : num_sg
! for different band energies, different schroedinger
! equations have to be solved. These are numbered by num_sg
!
! num_deg
! for equal energy but different masses again, different
! equations have to be solved, which are then numbered by num_deg
!
------------------------------------------------------------
!
$output
------------------------------------------------------------
!
$end_output
------------------------------------------------------------
!
$end_output
------------------------------------------------------------
!
$end_output
------------------------------------------------------------
!
$end_output
------------------------------------------------------------
!
$end_output
------------------------------------------------------------
!
$end_output
------------------------------------------------------------
!
$end_output
------------------------------------------------------------
!
$end_output
------------------------------------------------------------
!
$end_output
------------------------------------------------------------
!
$end_output
------------------------------------------------------------
!
$end_output
------------------------------------------------------------
!
$end_output
------------------------------------------------------------
!
piezo-electricity = yes !
pyro-electricity = yes !
interface-density = yes !
$end_output-densities !

******************************************************************************

******** END BAND STRUCTURE AND DENSITIES ******************************************

******* OUTPUT STRAIN *************************************************************

******** END OUTPUT STRAIN ****************************************************
Bibliography


[9] S. Datta, G. Dewey, J. M. Fastenau, M. K. Hudait, D. Loubychev, W. K. Liu, M. Radosavljevic, W. Rachmady and R. Chau, "Ultrahigh-Speed 0.5 V Supply Voltage In$_{0.7}$Ga$_{0.3}$As


VITA

Lu Liu

EDUCATION:

- Pennsylvania State University, University Park, PA, U.S. 08/2009-05/2014
  PhD, Electrical Engineering Advisor: Prof. Suman Datta
- National University of Singapore, Singapore 08/2008-07/2009
  PhD student, Electrical Engineering, quit in good standing
- Peking University, Beijing, China 08/2004-07/2008
  Bachelor of Science, Physics

PUBLICATION:

-Journals

-Conferences
L. Liu, V. Saripalli, V. Narayanan and S. Datta, “Experimental Investigation of Scalability and Transport in In0.7Ga0.3As Multi-Gate Quantum Well FET (MuQFET)”, Device Research Conference (DRC), Santa Barbara, CA, pp. 17-18, June 2011.
L. Liu, V. Saripalli, E. Hwang, V. Narayanan and S. Datta, “Experimental Demonstration of Modulation Doped In0.52Al0.48As/In0.7Ga0.3As/In0.52Al0.48As Quantum Well FINFET with Split Wrapped Gates”, 219th Electrochemical Society (ECS) Meeting, Montreal, QC, Canada, May 2011.