A NOVEL APPROACH FOR FABRICATING NANOCHANNEL TEMPLATES FOR Si NANOWIRE GROWTH AND TRANSISTOR FABRICATION

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by

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ABSTRACT

For the past decades, silicon nanowire (SiNW) has been extensively studied due to their unique electric, optical, and mechanical properties and great compatibility with modern integrated circuits industry. Researchers have successfully demonstrated its potential applications in many fields, such as high performance transistors, high resolution and sensitivity bio and chemical sensors and so on. Scientists even predicted it is most likely that SiNW transistor will become the final winner for the competition of future generation transistor architecture. Therefore, it is very obvious that SiNW has become the rising star for future nanoelectronics. Up to date, many efforts have been devoted to synthesizing SiNW. In general, there are two main categories in terms of SiNW growth methods, and post growth device fabrication and assembly: “grow-and-place” and “grow-in-place”. For “grow-and-place” approach, intensive post growth treatments are needed to fully realize SiNW device application, which leads to higher cost and lower throughput. For “grow-in-place” approach, the SiNW is grown on the substrate, where the final device will be fabricated, and there is no post growth treatments needed. This approach improves the throughput and cost of “grow-in-place” approach. However, it is still a great challenge for realizing mass production of SiNW based device due to the lack of well-controlled nanofabrication techniques with lower cost and higher throughput.

To resolve some of these above-mentioned issues, in this thesis, we have developed a novel approach for fabricating nanochannel templates for SiNW growth and further device applications. This method represents “grow-in-place” approach and takes full advantages of “grow-in-place” approaches. However, it has several improvements
compared with “grow-in-place” approach in terms of the fabrication of nanochannel templates, and catalyst patterning and control. We have investigated two alternative sacrificial materials for nanochannel templates, which are further used for encapsulated SiNW growth. Those two alternative sacrificial materials are polymers of specified properties and amorphous silicon. Specifically, we have explored the NXR 3022 polymer, which is water soluble, and NXR 1025 polymer, which is general solvent soluble. In addition, we have investigated and optimized the patterning techniques of sacrificial polymer based on the throughput, patterning cost and polymer compatibility with subsequent process steps. Taking into account of all the factors, we have chosen new nanoimprinting lithography to pattern the polymers. Detailed procedures and issues encountered during the nanochannel fabrication process will be discussed. For inorganic amorphous silicon, we have successfully demonstrated its capability as the sacrificial material of nanochannel. The advantages of using amorphous silicon are as follows: process simplicity, great compatibility with further processes as well as its ease of dry removal for forming nanochannels.

Through this novel proposed approach, we have successfully grown SiNW with high-quality surface and structure properties: smooth surface morphology, prefect single crystal structure, and excellent electrical characteristics. The detailed information will be discussed in this thesis. Additionally, we have successfully fabricated the accumulation mode MOSFET (AMOSFET) on grown SiNW. The device performance was characterized through I-V measurements and it has shown excellent device performance with high on and off current ratio and sharp subthreshold swing.
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Chapter 1

Introduction to nanowire synthesis and potential applications

Several decades ago, nanotechnology as a new technique defined as manipulation of matter at the atomic or molecular scale caught many researchers and scientists’ eyes from both academic and industrial fields. Since then it has become extremely popular due to its potentially significant improvements for other technologies and devices, like the conventional integrated circuits used in most of commercial consumer and defense electronics devices. For both of the consumer and defense market, the overall trend and demand is to develop higher performance, smaller volume and lower cost electronics devices. Recently, with the application and rapid development of nanotechnology, more and more miniature electronics devices with significantly improved performance and more functions are developed and constantly released into the consumer electronics market as predicted by Moore’s law, which is named by Gordon Moore, the former CEO of Intel, who made the prediction that the density of transistors integrated on a given circuit chip will be approximately two times larger than previous ones every two years[1].

According to the International Technology Roadmap for Semiconductors (ITRS), for the next ten or more years, nanotechnology will still play crucial role in promoting the technology revolution in many fields, such as chemical and biological engineering and even environmental engineering. Nanotechnology has a broad range as demonstrated from its definition from the formation of nanoparticles, nanotubes and nanowires or nanorods, utilization of nonmaterials to the fabrication of nanodevices. Among them, the nanomaterials including nanoparticles, nanotubes and nanowires have attracted more attentions due to their unique electronic, optical and mechanical properties for potential
applications in many different fields. In this thesis, we mainly discuss the one-dimensional nanostructures, which have been extensively researched for decades and also have been successfully synthesized through different approaches. The details will be discussed in the following.

1.1 One-Dimensional Nanostructures

According to Moore’s law, the size of devices will be continuing to decrease for the next ten more years using the advanced nanotechnology fabrication techniques. However, eventually it will hit the wall and there is no any space to keep miniaturizing the devices any more. In addition, the cost for fabricating such nanodevices will be inversely proportional to the size of nanofeature and it will be significantly increased. Scientists were wondering what is going to happen next to get over such bottle neck and continue promoting the technology revolutions. Therefore, one-dimensional (1-D) nanostructures have become promising candidates to resolve such problems and recently they also have attracted tremendous attentions due to their inherent small feature size, which renders them perfect candidates for forming nanodevices without expensive advanced fabrication processes involved. So through the utilization of one dimensional nanostructures, it is highly possible and feasible to follow the Moore’s law continuing increasing the active devices density on a given chip, improving the device performance and keeping the cost low in the meantime. For one dimensional nanostructures, there are mainly two categories: nanotubes and nanowires.

In terms of nanotubes, researches have been focused on the single wall and multi-wall carbon nanotubes due to its interesting electronic, thermal and mechanic properties,
such as the strong ability for enduring very high electric current density, which is thousand times greater than most of the metals such as gold [2], and known ballistic thermal conduction [3]. Scientists have successfully demonstrated the potential applications of carbon nanotubes (CNT) in many fields including CNT field effect transistors [4], electrical cables and wires [5], and CNT solar cells [6]. There are still some limitations for realizing large scale CNT applications due to the difficulty of selectively and precisely producing either metallic CNTs or semiconductor CNTs and the lack of abilities to reliably control electrical conductivity through doping [7].

Unlike nanotubes, nanowire researches have covered wide range semiconducting materials including silicon (Si), germanium (Ge), gallium nitride (GaN), indium phosphide (InP), and zinc oxide (ZnO2) and researchers have successfully grown those nanowires [8-17]. Compared with CNTs, the semiconducting nanowires have several advantages. First, these nanowires have only the semiconducting property, not the metallic property, like what CNTs could possibly own. In addition, the doping of those nanowires could be well controlled through those well established and mature techniques developed in modern integrated circuit semiconductor industry. Finally, the shape of nanowires could be manipulated and theoretically there are no limitations to any shape. Experimentally, circular [18], triangular [19] and rectangular [20] shaped semiconducting nanowires have been demonstrated.

The another interesting part for one dimensional nanostructures is that heterostructure nanostructures could be obtained through proper doping and composition control for a certain optimized growth condition. People have successfully synthesized both radial [21] and axial heterostructure nanowires [22]. Due to their unique
heterostructures, those nanowires have been commonly used for higher performance nanoelectronics, such as, nanowire LEDs [23] and tunneling field effect transistors [24].

Up to date, enormous semiconducting nanowires have been intensively investigated and studied. Among those various researched nanowires, Silicon nanowires are the most popular ones and have gathered most attentions due to the following advantages:

1. Silicon nanowires’s full compatibility with modern Si dominated integrated circuit semiconductor industry, which will make the whole fabrication process even cheaper and simpler.

2. It is easier to explore and investigate some unique properties demonstrated by smaller nanostructures including the effects on bandgap with dimensions shrinking and even quantum confinement mechanism since bulk Si material properties have been well researched and understood [25].

1.2 Silicon Nanowire synthesis

Due to Si nanowires’ potential applications in many fields, many efforts have been made to synthesize Si nanowires. Scientists have developed numerous ways to synthesize Si nanowires and generally there are two main categories for Si nanowires synthesis including top-down approaches and bottom-up approaches.

1.2.1 Top-down approaches

There are several types of top-down Si nanowire fabrication approaches and all of them involved either electron beam lithography or optical lithography patterning technique and later dry etching or wet etching process. Recently, research group in
Durham University of United Kingdom successfully fabricated as small as 10nm in diameter single crystal Si nanowires using optical lithography through top-down fabrication approach [26]. Fig. 1-1 (a-f) shows the whole fabrication process flow [26].

In this approach, it started with silicon on insulator (SOI) substrates with the top silicon and buried oxide thickness around 145nm and 400nm, respectively. Here the silicon layer is heavily n-type doped and it is covered by 60 nm thick silicon nitride layer (Si3N4) deposited by plasma enhanced chemical vapor deposition (PECVD), which acts as a mask for later wet etching process. To make Si nanowires from this stacked thin film structures, they used optical lithography to pattern the top Si3N4 layer first as shown in Fig. 1-1 (a). And then the substrate went through a KOH anisotropic wet etching and

**Fig. 1-1:** The whole schematic process flow for the fabrication of single crystal Si nanowire. Figures have been adapted from reference [26].
thermal oxidation processes, as can be seen from Fig. 1-1 (b-c). Subsequently, the Si3N4 mask layer was removed by boiling phosphorus acid etching as demonstrated in Fig. 1-1 (d). Finally, Fig. 1-1 (e-f) shows the second KOH anisotropic wet etching was performed and followed by the buffered oxide etcher (BOE) to remove the thermal oxide on one side wall of the Si nanowires and completely expose the nanowires.

For this approach, there are several disadvantages here. First, the use of expansive SOI wafer will increase the whole fabrication cost. In addition, the huge amount of wet etching chemicals used for the fabrication also cause potential environmental pollutions. Secondly, it is very difficult to control the surface roughness of fabricated Si nanowires. Because the side wall roughness of Si nanowires is partially depended on the roughness of top Si3N4 mask layer, which was patterned and dry etched through plasma. Although in their work, they put great efforts trying to optimize the lithography and dry etching conditions to minimize the line edge roughness of SiN4 mask layer, the side wall roughness of Si nanowires is still not optimal. Finally, the shape of fabricated Si nanowires through this approach will be limited to inverse triangle like cross section as shown in Fig. 1-2 (f), which is not ideal structure for later device applications, specifically for field effect transistors applications.

1.2.2 Bottom-up approaches

In bottom-up approaches, there are also several different methods to synthesize Si nanowires including thermal evaporation, laser assisted Si nanowire growth, chemical vapor deposition (CVD) and molecular beam epitaxy (MBE). Among those methods, the chemical vapor deposition (CVD) methods based on vapor-liquid-solid (VLS)
mechanism have received the most attentions and are the most commonly used ones to synthesize Si nanowires [27]. The concept of vapor-liquid-solid mechanism was first brought up by R.S. Wagner in 1964 [28] and the detailed will be discussed in the following.

Figure 1-2 [29] demonstrates how the VLS nanowire growth mechanism works. As shown in Fig. 1-2 (A), there are volatile gaseous silicon precursor and metal catalyst involved in the VLS process. When Si source gas reached the metal catalyst heated above the metal and Si eutectic temperature, the Si containing vapor will decompose and form Si on the surface of metal catalyst as described in the following chemical reactions. (Fig.1-2(B)). Later Si will diffuse into the gold and form the liquid like gold and Si alloy system. Continuing flowing the Si source gas, more Si diffused into the liquid like alloy system. When supersaturation state is reached, Si will precipitate out as shown in Fig.1-2 (C) and the nanowires get grown in length and gold cap will remain on the top as shown in Fig.1-2(D).

$$\text{SiH}_4 \text{ (gas)} \rightarrow \text{Si (solid)} + 2\text{H}_2 \text{ (gas)}$$

$$\text{SiCl}_4 \text{ (gas)} + 2\text{H}_2 \text{ (gas)} \rightarrow \text{Si (solid)} + 4\text{HCl (gas)}$$

$$\text{SiH}_2\text{Cl}_2 \text{ (gas)} \rightarrow \text{Si (solid)} + 2\text{HCl (gas)}$$
Fig. 1-2: Demonstration of VLS Si nanowire growth. Figures have been adapted from reference [29].

Here the volatile precursor serves as silicon source for Si nanowire growth and there are multiple silicon precursors including silane (SiH4) and silicon tetrachloride (SiCl4). In terms of metal catalyst choice, the guiding rule is that as long as a metal would be able to form eutectic phase with Si, and then that metal has the potential to be used as the catalyst for Si nanowire growth. Some metals like Ti, Ag and Pd form high temperature eutectic phase with Si (above 800°C) as shown in Fig. 1-3 (c)(e)(f) [30-32]. Others like Au, Al and Zn form relatively lower temperature eutectic phase with Si as seen in Fig. 1-3 (a) (b) (d) [30-32]. Among those above mentioned metals, gold is the commonly used catalyst due to several reasons. First, gold forms lower temperature eutectic phase with Si (around 363°C), which is suitable for lower temperature CVD Si nanowire growth. Second, gold has excellent chemical stability and is inert to most of chemicals and gases even at high temperature. Therefore, gold catalyzed CVD Si nanowire growth system does not need expensive advanced pumping system to support
ultra high vacuum. Finally, Si has very low solubility in gold at eutectic temperature (around 19% as shown in Fig.1-3 (a)) and gold would not create deep defect levels in Si as well.

**Fig. 1-3**: Phase diagram of Au/Si, Al/Si, Ag/Si, Zn/Si, Ti/Si and Pd/Si metal-silicon system. Figures have been adapted from reference [30] [31] [32].

Figure 1-4 shows the experiment set up of growing Si nanowire by combing SiO thermal evaporation with VLS growth mechanism [33]. In this approach, first, the SiO granulate source materials and gold coated Si wafer are put in the different quartz boats.
And then they are loaded into quartz tube inside tube furnace of three zones, respectively as shown in Fig. 1-4. Subsequently, the whole system will be pumped to a high vacuum with both Turbo molecular pump and mechanical pump, and then flew nitrogen gas into the system to get an inert environment. Finally, the SiO and gold coated substrate will be heated to a certain temperature, respectively. Upon heating on solid SiO material, it will experience decomposition process producing Si and silicon dioxide demonstrated from following chemical reaction, and then the produced Si will form eutectic liquid like alloy with gold on heated silicon wafer and with the constant supply of silicon, the gold/Si alloy will be supersaturated and then Silicon nanowires get grown out of it.

\[ \text{SiO} \rightarrow \text{Si} + \text{SiO}_2 \]

**Fig.1-4:** Schematic experimental system to grow Si nanowire. Figures have been adapted from reference [33].

Recently, scientists have successfully grown Si nanowire by Molecular beam epitaxy (MBE) [34]. In this approach, the ultra high vacuum (UHV) MBE system with the capability of depositing Si and Au by electron beam evaporation is used. At the
beginning, the substrate is heated to a temperature in between 500 °C and 570 °C, and then a thin gold film will be deposited and annealed to form the gold cluster seeding for later Si nanowire growth. After gold deposition is done, Si electron beam evaporation will be started immediately. The evaporated Si atoms will be absorbed by gold clusters upon reaching the substrate surface yielding the gold and Si eutectic alloy system and with constant supply of Si atoms, the Si nanowires will be grown due to Si precipitation beyond supersaturation state. For this approach, there are several disadvantages. First, the growth rate is very slow, which makes this approach less manufacturable. Second, it is difficult to control the diameter of nanowires and researchers found only nanowires with diameter larger than 40nm can be achieved [34].

The laser assisted Si nanowire growth method was first developed by Charles M. Lieber’s group from Harvard University in 1998 [35]. Fig. 1-5 (a) shows the experiment set up for growing nanowire through laser ablation [35]. In this approach, the researchers proposed the following possible growth mechanism as shown in Fig. 1-5 (b). Firstly, the high energy laser lights go through the lens system and get focused on the Si and Fe compound target materials producing a hot, dense vapor of Si and Fe species. Secondly the hot vapor will be able to condense into small clusters due to the collisions among Si and Fe species and carrying gas. Furnace tube has to be maintained at a temperature of above Si and Fe eutectic temperature (in this case around 1200 °C) in order to keep the condensed nanoclusters in liquid like state. Thirdly, nanowire growth starts once liquid like Si-Fe nanoclusters reach supersaturation state and it will keep going until the grown nanowires are transported out of the hot tube zone through carrying gas and get collected on the cold finger, where the liquid like Si-Fe nanoclusters will be solidified. Although Si
nanowires have been successfully synthesized through this approach, there are still some problems and limitations existing. For example, it is impossible to precisely control the diameter of grown Si nanowires, which is determined by the size of Si and Fe nanoclusters.

![Diagram showing the growth setup of Si nanowires](image1.png)

a. Schematic of Si nanowire growth set up [35].

![Diagram showing the proposed growth mechanism](image2.png)

b. Proposed Si nanowire growth mechanism [35]

Fig. 1-5: Demonstration of Si Nanowire growth by laser ablation approach. Figures have been adapted from reference [35].

1.3 Silicon Nanowire potential applications

Si nanowires own surface-dependent physical and chemical properties due to their inherently small feature size. By taking full advantage of those unique properties,
scientists have successfully demonstrated Si nanowires various applications in electronic devices, sensors, batteries and solar cells. Although many Si nanowires applications are still in early investigation stages, they have shown the great potential and hope for future large scale applications and currently some applications are even very close to be put in the market.

1.3.1 Si nanowire transistors

Si nanowires field effect transistors are one of earliest applications demonstrated by scientists and also the most commonly researched ones. Recently, Walter M. Weber ‘s group from Germany have developed a novel reconfigurable Silicon nanowire transistors [37]. The transistor core is made of axial metal (NiSi$_2$)-intrinsic (Si)-metal (NiSi$_2$) heterostructure nanowire with diameter in 20nm and the shell is composed of thermally grown SiO$_2$ serving as gate oxide dielectrics as shown in Fig. 1-6 (left). Here, the heterostructure NWs fabrication processes are as follows. Firstly, the SiNWs were grown through VLS process and then dispersed onto SiO$_2$ coated Si substrate. Subsequently, thermal oxidation process was performed to form SiO$_2$ shell. Thirdly, patterning, SiO$_2$ wet etching and Ni deposition at both ends of NWs were conducted. Finally, they did rapid thermal annealing to form the NiSi$_2$/intrinsic Si/ NiSi$_2$ NW axial heterostructures. The segments of NiSi$_2$ from both sides of nanowire acting as source and drain form Schottky junction with intrinsic Si on the interface. Unlike the conventional SiNWs FET transistors, this novel reconfigurable transitors have two independent gates, one of which has the same function as the one in conventinal SiNWs FET transistors and tunes the channle condutance though NW, whereas the other one is used to control the polarity of
transistors (p or n). Fig. 1-6 (right) shows the excellent electrical characteristics with on and off current ratio up to $1 \times 10^9$.

The interesting part for this novel transistor architecture is that a universal transistor can be reversely converted to p-FET or n-FET only by applied external electrical signal, which is a biggest advantage for modern CMOS based integrated circuits. Because this novel transistor technology would make the hardware platform flexibly reconfigured to a certain polarity during operation to conduct different job functions without the need of adding more devices into the integrated circuits as CMOS based technology did. Therefore, it is highly promising to develop more compact and flexible integrated circuits out of this novel technology.

**Fig. 1-6**: (left) Schematic of reconfigurable SiNW FET structure and (right) measured transfer characteristics as p (red) FET and n (blue) FET. Figures have been adapted from reference [36].

### 1.3.2 Si nanowire solar cells

For decades, Si has been the main choice of photovoltaic devices and will remain dominating renewal green energy field due to its superior photo-electronic properties. Commercial single crystal Si solar cells have the energy conversion efficiency as high as
24%. However, the whole costs for fabricating such single crystal cells are still huge, which will limit its large scale applications.

Recently, Peidong Yang’s group from University of California, at Berkeley has developed novel SiNWs based solar cells [37]. Fig.1-7 shows the fabrication process of vertically aligned SiWs array. First, it started with dip coating an n-type silicon substrate in silica bead solution (Fig. 1-7 (a)) and then performed deep reactive ion etching (DRIE) process using the closely packed beads as an etching mask yielding vertically aligned nanowires (Fig. 1-7 (c)). Thirdly, the silica beads etch mask was removed in HF acid solution and SiNWs were cleaned through standard cleaning process (Fig.1-7 (d)). Finally, the SiNWs went through the boron diffusion doping process to produce p-n junction.

Through the use of ordered silicon nanowire array, they have been able to achieve as high as 10% energy conversion efficiency due to the substantial light trapping enhancement in those solar cells. In addition, the fabrication costs are greatly reduced through the relatively simple and scalable aqueous chemistry process. Their work not only have shown the great promise to an economically viable path toward high efficiency, low cost single crystal thin film solar cells, but also successfully demonstrated that silicon nanowires could possibly be the top candidate for large scale solar cell applications in the near future.
1.3.3 Si nanowire chemical and biosensors

SiNWs own extremely high surface to volume ratio and inherently small feature size, which make them a perfect candidate for sensing applications including chemical sensors and biosensors. In 2001, Charles M. Lieber’s group from Harvard University has developed the ultra high sensitivity SiNW chemical and bio sensor for real time pH detection and protein bonding detection, respectively [38].

For conventional SiNWs FET, the applied gate voltage can accumulate or deplete the charges in SiNWs, therefore tune the active channel conductance of SiNWs. That is very similar to that of how the SiNWs chemical sensors work and the only difference is that for SiNWs chemical sensors, there is no need for externally applying gate voltage to control the conductance of SiNWs as SiNWs FET does. For SiNWs chemical sensor, the nanowires were modified first by specific chemical agent as shown in Fig. 1-8 (A) and then such chemical agent would go through protonation and deprotonation process when in contact with specific to-be detected chemical solution, which will cause the change of the surface charges of SiNWs, therefore the conductance change of SiNWs [38]. Fig. 1-8 (C) shows the conductance correspondence with pH value.
Fig. 1-8: SiNWs chemical sensor. (A) Schematic of the conversion of SiNW FET into SiNW chemical sensor. (C) Conductance versus pH value. Figures have been adapted from reference [38].

Figure 1-9 (A) shows the SiNW biosensor. The SiNW is modified with biotin, which will be selectively attached to a certain protein, as shown in Fig. 1-9 (A). This binding process will cause the change of SiNW conductance as seen in Fig. 1-9 (B). By the conductance change, we would be able to tell whether the detected protein exists or not. When the protein solution concentration was changed from 25 nM used in Fig. 1-9(B) to lower concentration of 25 pM, smaller conductance change could be noticed as shown in Fig. 1-9 (E). Through this way we would be able to determine the maximal sensitivity of such nanowire sensor. If the nanowire is not modified by specific protein, there will be no conductance change as shown in Fig. 1-9 (C). Fig.1-9 (D) shows there is almost no or very little change in conductance as well, if the detected solution is full of biotin receptor and equivalent amount of protein. Because in this case, the protein already preboned with
biotin receptor from the solution and there are not excessive protein left for binding with biotin on the surface of SiNWs.

Fig. 1-9: Real-time SiNWs biosensor. (A) Schematic of biotin modified SiNW and subsequent certain protein attachment to the SiNW surface. (B) Plot of conductance versus time before and after the addition of higher concentration protein solution. (C) Conductance versus time for unmodified SiNW before and after the addition of protein solution. (D) Conductance versus time for biotin modified SiNW before and after the addition of protein-biotin bonded solution. (E) Conductance versus time for biotin modified SiNW before and after the addition of lower concentration protein solution, compared with the one used in (B). Figures have been adapted from reference [38].
1.4 Summary

This chapter introduced the history of one dimensional nanostructures at the beginning. Then the focus is pointed onto the Si nanowires since they are most common researched and have greatest potential for future applications in many fields. Later, the different types of Si nanowire synthesis techniques were discussed in details. Finally, Si nanowire based devices from FET, optoelectronics to chemical and biosensors were specifically described.

1.5 Research objectives and thesis organization

This thesis includes an experimental investigation on the capping layer material and sacrificial layer material used for fabricating encapsulated nanochannel template for SiNW growth. The purpose was to optimize and improve the encapsulated grow-in-place approach demonstrated previously by our group. The objectives were to:

1. Investigate the effects of oxide capping layer on SiNW growth and obtain the optimal capping layer for high quality SiNW growth.
2. Explore alternative sacrificial material for nanochannel template formation and optimize the process flow towards the high throughput and low cost manufacturing purpose.
3. Fabricate high performance transistor on SiNW grown by the improved encapsulated grow-in-place approach.

The work done in this thesis for realizing those above mentioned objectives is organized in the following manner:
Chapter 2 reviews the most commonly investigated SiNWs assembling techniques for further device fabrication and analyzes the advantages, challenges and limitations for each single specific assembling technique.

Chapter 3 introduces my novel approach for fabricating nanochannel template for SiNW growth and investigation of sacrificial polymer materials for nanochannel formation.

Chapter 4 introduces the improved approach based on the one described in chapter 3 for fabricating nanochannel template for SiNW growth by using amorphous Si as sacrificial channel material.

Chapter 5 demonstrates the accumulation mode field effect transistors (AMOSFET) fabrication through encapsulated grown SiNWs using above discussed approach and devices characterization results.

Chapter 6 summarizes the work that has been done in this thesis and discusses the potentials of what could be done for further improvements in the future.
Chapter 2

Silicon nanowire assembling techniques for device fabrication

2.1 Introduction

As discussed in chapter one, SiNWs are one of the most investigated one-dimensional nanostructures and have attracted extensive attentions due to its unique properties and greatest compatibility with modern Si dominated semiconducting industry. A great number of efforts have been made to explore SiNWs potential applications in many fields ranging from electronics, sensing and environmental safety to green energy fields. Scientists even predicted that SiNWs transistors are most likely to be next generation transistor architecture in the future [39]. Up to date, many methods have been successfully developed to synthesize SiNWs as described in chapter one. However, in order to make devices out of SiNWs, it needs some assembling techniques to align those synthesized SiNWs on specific substrates where the final devices will be fabricated or developing novel template assisted SiNW growth approaches, for which no further assembling steps are needed. The former approaches are called “grow and place” approaches and the later called “grow in place” approaches. Detailed information in terms of those two approaches will be discussed in this chapter.

2.2 Grow and place approaches

For “grow and place” approaches, basically there are two steps involved. Therefore, they are often called two-steps approaches. The first step is synthesis of SiNWs using the methods described in chapter one, such as metal catalyzed CVD VLS growth process. The second step is the positioning of synthesized SiNWs on the desired
substrate for later specific devices fabrication. The positioning step is very challenging due to the extremely small size of grown SiNWs. However, to realize the full potential of SiNWs and make devices from them, it requires the development of well-controlled and predictable assembly techniques for synthesized nanowires. Up to date, researchers have successfully demonstrated some assembling techniques such as surface patterning fluidic alignment [40-41] and electric field assisted assembly methods [14].

2.2.1 Aligning nanowires through surface patterning fluidic alignment techniques

Basically, there are two types of surface patterning fluidic alignment techniques: “separating and aligning nanowires from solution by flowing through microfluidic channels” [40] and “SiNWs alignment by Langmuir-Blodgett technique” [41]. For both of techniques, the SiNWs are grown first on the substrate and then are harvested into solution (usually IPA) with the assistance of ultrasound agitation. Subsequently, the SiNWs will be aligned by solution manipulation and assembly techniques and then final microscopic inspection is needed to make sure the SiNWs well positioned. Finally, the devices will be fabricated on those aligned SiNWs through conventional optical lithography, etching and thin film deposition processes.

Figure 2-1 shows the schematic of separating and aligning nanowires from solution by flowing through microfluidic channels [29] [40]. For this technique, it started with SiNWs synthesis through metal catalyzed CVD VLS growth process as shown in Fig. 2-1(a) [29] [40]. And then the grown SiNWs are subsequently suspended into solution. The nanowires in the solution are aligned by passing the suspensions of NWs into the microfluidic channels, which are formed by prefabricated poly (dimethylsiloxlane) PDMS mold and a specific flat substrate, where the final devices will
be fabricated. Through this technique, the parallel and crossed arrays of SiNWs can be obtained by flowing perpendicularly sequential flow on top of the first aligned layer as shown in Fig. 2-1 (b). Ultimately, after the aligned single or crossed arrays of SiNWs undergoes the optical or field effect secondary electron microscopy (FESEM) inspection to confirm the appropriate positioning of nanowires, the thin film transistors (TFT) of SiNWs are fabricated as shown in Fig.2-1 (c).

**Fig. 2-1**: Schematic procedure of SiNWs alignment by combing fluidic alignment with surface patterning techniques. (a) The schematic flow of SiNWs synthesis, alignment and transistor fabrication. (b) Single and crossed double layer SiNWs alignments by flowing nanowire solution through microfluidic channels. (c) The top view optical micrograph image of SiNWs TFT devices. Figures have been adapted from reference [29] [40].

Figure 2-2 shows the second type of surface patterning assisted fluidic alignment technique and that is Langmuir-Blodgett technique [41]. In this technique, the SiNWs in a monolayer of surfactant are compressed on a Langmuir-Blodgett trough and then the SiNWs could be aligned with tunable average interspacing, which is controlled by the compression process as shown in Fig. 2-1 (a). Subsequently, the aligned SiNWs are
transferred to a desired substrate in order to produce parallel and well-ordered SiNWs arrays as seen in Fig. 2-1 (b). For this approach, it could also produce the crossed double SiNWs structures with layer by layer assembly and perpendicularly transferring the second aligned SiNWs on top of the first aligned SiNWs [41].

For these two techniques described above, there are several disadvantages. First, these techniques are labor intensive and typically have low yield due to the huge loss of nanowires during solution manipulation processes, which make SiNWs devices impossible for large scale practical applications. Second, it is very difficult to control the interspacing among nanowires. Usually there are multiple nanowires attached together producing wire bundles. Therefore, these techniques worked very well for fabricating multiple SiNWs based devices, but it is impossible to obtain the single SiNW device. Finally, it is extremely challenging to get the perfectly parallel nanowire arrays. Most of the time, the nanowires are aligned at an angle with each other.
2.2.2 Aligning nanowires by electric field assisted assembly technique

In order to fully realize the highly integrated SiNWs based devices for practical applications, it is necessary to develop an economical technique to align and assemble those nanowires into well-ordered arrays. In 2001, Charles M. Leiber’s group has developed a technique of aligning nanowires from solution by using electric field as shown in Fig. 2-3[14]. In this technique, the SiNWs suspension was dispersed on the
substrate patterned with electrodes. When the high frequency AC voltage is applied, the SiNWs in the solution will be captured and aligned between electrodes due to dielectrophoresis force as demonstrated in Fig. 2-3 (a). Fig. 2-3 (b) shows the results of aligning multiple nanowires between two parallel electrodes. For best alignment yield and outcome, electrodes fingers could be used yielding spatially positioned nanowires array as shown in Fig. 2-3 (c). In addition, this technique is also capable of producing crossed NWs structure by changing electric field direction for the second layer alignment as shown in Fig. 2-3 (d).

Compared with the surface patterning fluidic alignment techniques, this electrical field assisted alignment technique is better in many ways, such as, the improved controllability for both of interspacing between nanowires and positioning of nanowires, and the ability of obtaining spatially positioned individual nanowire array. However, for this approach, there are still several disadvantages. First, usually multiple nanowires are occupying the same location. In addition, aligned nanowires are not perfectly parallel, but at a certain angle with each other and even crossed as can be seen from Fig. 2-3 (b), which will cause the significant yield loss of alignment. Second, this technique only works best for “site” by “site” nanowire alignment as shown in Fig. 2-3 (c). However, it is labor intensive and time consuming. Therefore, it is not economically practical for large scale applications. Third, even for “site” by “site” alignment, nanowires are often aligned at certain angle to the electrode fingers as well, as seen in Fig. 2-3 (c). Finally, the yield is pretty low and typically found to be around 10%-30%, which is not viable for mass production manufacturing purpose.
Fig. 2-3: Parallel and crossed nanowire assembly by electric field assisted technique. (a) Schematic of parallel nanowire assembly process with electric field, (b) The SEM image of large scale aligned nanowires between two parallel electrodes. (c) The SEM image of individually aligned nanowires between two electrode fingers. (d) The SEM image of two cross aligned nanowires. Figures are adapted from [14].

2.3 Grow-in-place approaches

As discussed in previous section, the disadvantages of grow and place approaches are very obvious. Therefore, researchers tried to develop new approaches that no post growth alignment processing steps are needed and the NWs are grown in the size, orientation and position of desired for final devices. In 2004, Stanely Williams’ group demonstrated the approach of growing NWs between two opposing vertical wall, which is also called nanobridges approach [42]. In the same year, our group proposed the concept of “grow-in-place” NWs growth approaches [29] [43-49]. For these approaches,
the NWs are grown with the controlled dimensions, orientation and positions. In some sense, the nanobridges approach could be also classified into “grow-in-place” approaches and detailed information will be discussed in the following sections.

### 2.3.1 Self aligned nanowire growth

Figure 2-4 (A) demonstrates the nanobriges approach of growing SiNWs [42]. It starts with the patterning of silicon substrate through optical lithography and etching processes (Fig. 2-4 (a)). Secondly, the gold catalysts were obliquely deposited on one of two opposing side walls of the silicon trench (Fig. 2-4 (b)). Subsequently, the samples were loaded into CVD chamber for the metal catalyzed VLS growth process. The nanowire started lateral growth from the side where metal catalyst got deposited and eventually it would bridge the trench of silicon forming robust nanobridges between two opposing vertical walls of patterned trench (Fig. 2-4 (c) and (d)). Fig. 2-4 (B) shows the typical growth results [42]. As seen from those FESEM side view images, the nanowires were grown in variable length and diameter. In addition, most of wires were grown randomly inside the trench, instead of bridging the trench, which will lead to lower nanowire growth yield.

Those grown nanowire arrays could be connected with each other through two electrodes patterned on the substrate for specific applications, such as SiNWs nanosensors. In some cases, the nanowires could be self connected when those two opposing vertical walls are made of conducting materials. For this approach, It looks like it is unnecessary to perform any post SiNWs growth alignment procedures for device fabrication. However, extra “grow and place” processing steps are still needed for making
isolation and integration of devices. Furthermore, it is still not possible for making single nanowire devices using this approach. Therefore, strictly speaking, it is not ideal “grow-in-place” approach and only takes some advantages of “grow-in-place” approach.

**Fig. 2-4:** (A) Schematic of SiNW growth by nanobridges approach, (a) patterned trench, (b) metal catalyst oblique deposition, (c) SiNW growth between two vertical walls, (d) Bridging across the trench. (B) FESEM side view images of trench and SiNW growth results by nanobridges approach. Figures have been adapted from reference [42].

### 2.3.2 Extruded nanowire growth

As discussed in previous sections, to make full use of SiNWs devices for practical applications, there are several requirements that need to be met.

1. Excellent control on nanowire growth, such as grown nanowire dimensions, orientation, the number of grown nanowires, interspacing among nanowires and position where the nanowires are desired to be grown.

2. The grown nanowires could be self aligned and assembled and there are no post growth assembling processes needed.
3. The potential and capability of making nanowire device fabrication, isolation and integration easy and simple.

4. Lower cost and higher yield.

According to discussion in previous sections, it is very obvious that for grow and place approaches and even self aligned nanobridge approach, it is still very challenging to meet most of those requirements listed above. However, the “grow-in-place” approaches have the greatest potential and capability to solve the challenges faced with grow and place approaches and self aligned nanobridge approach. For “grow-in-place” approaches, basically they include two types of methods: extruded nanowire growth method and encapsulated nanowire growth method.

Figure 2-5 shows the schematic of nanowire growth by extruded approach [29] [46-47]. The detailed process flow is as follows:

1. Gold nanowire patterning by electron beam lithography (Fig. 2-5 (a)).

2. SiO2 capping layer deposition, patterning by optical lithography and plasma dry etching to partially expose the gold nanowire (Fig. 2-5 (b)).

3. Partial removal of gold nanowire by wet gold etchant leaving small gold slug inside the channel (Fig. 2-5 (c)).

4. SiNWs growth through gold catalyzed CVD VLS growth process (Fig. 2-5 (d)).

   In this approach, the SiNW was grown first inside of the nanochannel, and then it exited the nanotunnel and continued growing unconfined. Fig. 2-6 shows the typical SiNW growth results. As can been seen, the nanowires have varied dimension and growth angle and they are approximately following Gaussian distribution [46]. Therefore,
for this technique, it has greatest control on the SiNW growth position, but less control on the growth direction and dimensions of nanowire.

**Fig. 2-5:** The schematic diagram of extruded nanowire growth approach. (a) The patterning of gold nanowire serving as catalyst. (b) The capping layer patterning. (c) Controlled gold wet removal leaving small gold slug inside the channel for catalyst. (d) SiNW growth by gold catalyzed CVD process.
Fig. 2-6: The typical SiNWs growth results by extruded approach. (A) Histogram of grown SiNWs diameter and angle with normal direction of oxide capping layer. (B) The FESEM image of grown SiNW. Figures have been adapted from reference [46].

2.3.3 Encapsulated nanowire growth

Because of the deficiencies of the extruded nanowire growth approach as described above, our group have made great efforts trying to improve that and developed the encapsulated nanowire growth approach [29] [44-46]. In this technique, the SiNWs are completely confined within the nanochannel during growth. Therefore, the dimensions and growth direction of SiNWs could be precisely controlled by the prefabricated nanochannel template. Fig. 2-6 shows the schematic of encapsulated nanowire growth approach. The complete process flow is detailed as follows:

1. The gold nanowires formed by Electron-beam Lithography patterning, gold deposition and lift off process. (Fig. 2-6 (a))

2. Plasma enhanced vapor deposition (PECVD) SiO2 capping layer deposition all over the entire wafer and then opening up window for next step partial gold removal by optical lithography definition and dry etching processes. (Fig. 2-6 (b))

3. Partial gold removal by commercially available wet gold etchant and this Au is to be a sacrificial material creating an empty template but part of it will be allowed to remain and be the required VLS catalyst (Fig. 2-6 (c))

4. SiNWs growth within the nanochannel through gold catalyzed chemical vapor deposition VLS growth process. (Fig. 2-6 (d))

5. Partially remove the capping layer to expose the grown SiNW for further device fabrication. (Fig. 2-6 (e))
Figure 2-7 shows the typical SiNW growth results by encapsulated growth approach [51]. As seen, the grown SiNW has very bad morphology with voids and rough surface. Two assumptions have been proposed to explain these phenomena detailed as follows:

1. Some residual material remains in the empty nanochannel template after the gold nanowires are wet etched.

2. The PECVD deposited SiO2 used as capping layer has some surface roughness at the SiO2/ sacrificial Au interface and it is most likely that surface roughness is transferred to the grown SiNWs since they are growing along the walls of the nanochannel template. In addition, it could also form bonds with the growing SiNWs. When partially exposing the SiNWs through combination of plasma dry etching and BOE wet etching processes, the bonds are broken and voids are formed.

Theoretically, it seems like that this encapsulated nanowire growth approach owns the capability of solving all the problems and challenges faced with extruded nanowire growth approach. However, in reality there are still some challenges needed to be solved to take the full advantage of this encapsulated nanowire growth method. For example, researchers in our group found that the small gold slug left inside the channel serving as catalyst has to be less than one micron in length in order to get nanowire growth [29] [46]. Otherwise, the SiNWs are grown with poor quality as discussed above and sometimes there is even no growth at all as observed in my experiments. However, it is extremely difficult to keep uniform size of the gold slug among nanochannels across the whole substrate. There are two possible reasons associated with that. First the gold
wet etching rate is not uniform across the wafer and it is affected by many factors, such as the diffusion rate of reactant and by product into and out the nanochannel, the reaction temperature and the external agitation so on. Second, the critical dimension (CD) of gold nanowire across the whole sample might be different caused by a great number of factors, including the resolution of the electron beam lithography and the type of resist used, gold deposition methods and the conditions of lift off process and so on. Therefore, variable size of gold slug was formed inside the nanochannel, which will lead to low growth yield of SiNWs. Because the nanowire growth is highly sensitive to the amount of gold left inside the channel. In addition, the gold wet etching is very challenging and time consuming as well, especially for long channel due to the limited diffusion length of liquid chemical reactants within nanochannel, which make it impossible for practical applications. Finally, the capping layer material and surface roughness might cause low quality SiNWs growth as described above, which are another factors threatening the growth yield of SiNWs and will discuss more in the following sections.
Fig. 2-7: The schematic diagram of encapsulated nanowire growth approach. (a) The patterning of gold nanowire serving as both catalyst for SiNWs growth and sacrificial layer of nanochannel. (b) Capping layer patterning to open up the etching window. (c) Partial gold removal by commercially available wet gold etchant and this Au is to be a sacrificial material creating an empty template but part of it will be allowed to remain and be the required VLS catalyst. (d) SiNW growth inside the channel through gold catalyzed chemical vapor deposition VLS growth mechanism. (e) Partially removing the capping layer and exposing the SiNW for device fabrication.

Fig. 2-8: FESEM image of grown SiNW by encapsulated approach using PECVD deposited SiO2 as capping alayer. Image has been adapted from reference [46].
In order to verify the assumptions of affecting the quality and morphology of grown nanowires as discussed above, we switched the capping layer from PECVD deposited SiO2 to atomic layer deposition (ALD) grown SiO2 layer since ALD deposition technique is supposed to produce thin films with smoother surface roughness due to its unique depositing mechanism and extremely low deposition rate. However, the typical growth results are not coming out as expected and similar low quality problems still exist as shown in Fig. 2-8. Therefore, we highly suspected the surface roughness of capping layer might not be the main factor or at least not the only factor, which caused such problems as shown in Fig. 2-7 and Fig. 2-8.

Therefore we continued using ALD but switched the capping layer material to ALD Al2O3. This capping layer material dependence study was done by Chris Winter, a graduate student in our group [45]. Surprisingly, the void problems were gone and very nice SiNWs with excellent surface morphology were grown, as can be seen from Fig. 2-9 [45]. Based on above results, we have made such assumption that the type of material used as capping layer might be the only factor or at least the main factor, which affects the surface morphology of grown SiNWs. Later, we attempted to use the physical vapor deposition (PVD) method to grow Al2O3 for capping layer, as comparison to the ALD grown Al2O3 capping layer. For PVD deposition, it is supposed to produce thin films with rougher surface. As expected from the assumption made above, the rougher surface of PVD deposited Al2O3 capping layer has very little effect or even no effect on the growth result at all and the SiNWs are grown with nice surface morphology as shown in Fig. 2-10, which further verifies that the morphology of grown SiNWs is affected least by the surface roughness of capping layer and most by the material itself of capping layer.
Fig. 2-9: FESEM image of grown SiNW by encapsulated nanwire growth approach using ALD deposited SiO2 as capping layer.

Fig. 2-10: FESEM image of grown SiNW by encapsulated nanowire growth approach using ALD deposited Al2O2 as capping layer.
Later, we have explored the other high dielectric constant oxide (high k) as alternative of capping layer, such as HfO2. There are two reasons for choosing HfO2 as capping layer. First, HfO2 as one of high k dielectrics has been commonly used for gate oxide of transistors in both academic and industry field. Therefore, if HfO2 as capping layer of the nanochannel template works for high quality SiNWs growth, and then it has the potential of being incorporated into the SiNW transistors as gate oxide, which will simplify the further SiNW based transistor fabrication processes. Second, we tried to find whether there is a certain correlation of the SiNWs growth results with the dielectric constant. According to SiNW growth results of using ALD and PVD deposited Al2O3, and PECVD and ALD deposited SiO2 as capping layer, respectively, it seems like that the better growth results are produced with higher k material as capping layer. Therefore, the material with higher k than SiO2 and Al2O3 should be picked and here it comes to HfO2. Fig. 2-11 and Fig. 2-12 shows the SiNW growth results by using ALD deposited
and PVD deposited HfO2 as capping layer. High quality SiNWs with good surface morphology are obtained as well, as expected from our original reasoning regards to the correlation of SiNW growth results with dielectric constant of capping layer. Therefore, in some sense, the correlation might be existing and more work needs to be done to further verify that.

In table 2-1, we summarized the SiNW growth results and found that using ALD deposited Al2O3 and HfO2 as capping layer could give us the best SiNW growth result. Considering the further SiNW transistor application, using ALD deposited HfO2 as capping layer might be the best choice due to its higher dielectric constant, which would benefit the device performance, such as lower gate leakage current.

![Image](image.jpg)

**Fig. 2-12:** FESEM image of grown SiNW by encapsulated growth approach using ALD deposited HfO2 as capping layer.
Fig. 2-13: FESEM image of grown SiNW by encapsulated growth approach using PVD deposited HfO2 as capping layer.

<table>
<thead>
<tr>
<th></th>
<th>Surface roughness of SiNWs grown</th>
<th>Quality for gate oxide of AMOSFET</th>
</tr>
</thead>
<tbody>
<tr>
<td>PVD SiO2</td>
<td>Bad</td>
<td>Bad</td>
</tr>
<tr>
<td>ALD SiO2</td>
<td>Bad</td>
<td>Medium</td>
</tr>
<tr>
<td>PVD Al2O3</td>
<td>Fairly smooth</td>
<td>Bad</td>
</tr>
<tr>
<td>ALD Al2O3</td>
<td>Smoothest</td>
<td>Fairly good</td>
</tr>
<tr>
<td>PVD HfO2</td>
<td>Fairly smooth</td>
<td>Not good</td>
</tr>
<tr>
<td>ALD HfO2</td>
<td>Smoothest</td>
<td>Best</td>
</tr>
</tbody>
</table>

Table 2-1: Summary of the SiNW growth results by encapsulated growth approach using SiO2, Al2O3 and HfO2 films with different deposition methods as capping layer of the nanochannel template.

2.4 Summary

In this chapter, SiNW assembling techniques for further device applications have been discussed in details and basically, it includes “grow and place approaches” and
“grow-in-place approaches”. In terms of the controllability to nanowire dimension, process complexity, fabrication cost and overall yield, the “grow-in-place approaches” are superior to the “grow and place approaches”. Therefore, this chapter mainly focused on the grow-in-place approaches. Two types of grow-in-place approaches were introduced and discussed, such as, extruded growth approach and encapsulated growth approach. Table 2-2 summarized and compared the two methods in terms of the controllability to the dimension and position of nanowire, growth direction, the quality of grown SiNW, the total yield and potential device performance. As can be seen clearly from that table 2-2, the encapsulated nanowire growth approach has yielded results better than those of extruded nanowire growth approach.

<table>
<thead>
<tr>
<th></th>
<th>Quality of SiNWs grown</th>
<th>Size and growth direction control of SiNWs</th>
<th>Yield and Device performance</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Extruded approach</strong></td>
<td>High</td>
<td>No control</td>
<td>Good</td>
</tr>
<tr>
<td><strong>Encapsulated approach</strong></td>
<td>High</td>
<td>Good control</td>
<td>Potentially better</td>
</tr>
</tbody>
</table>

Table 2-2: Comparison of the extruded SiNW growth approach and the encapsulated SiNW growth approach in terms of the controllability to the dimension and position of nanowire, growth direction, the quality of grown SiNW, the total yield and potential device performance.

According to above discussions, apparently the encapsulated nanowire growth approach with optimize capping layer could grow high quality self-aligned and
assembled SiNWs with precisely controlled dimension and position, and growth direction. However, there are still some spaces for continuing improving this method and make it more suitable for manufacturing purpose. For instance, in this technique, the expensive and time-consuming electron beam lithography is used in what has been developed in our group for patterning the gold nanowire, which serves as both sacrificial material for forming the nanochannel and catalyst for SiNWs growth. In addition, the problems associated with gold wet etching uniformity and difficulty inside the long channel as discussed above also need to be solved. Finally, besides the gold wet etching problems, using gold as sacrificial layer is not economically friendly and impractical as well for large scale SiNW applications since that will increase the total fabrication cost and it is also kind of waste to that precious and rare metal. In the following chapters, the thesis will focus on the improvements made to solve those challenges and will discuss them in details.
Chapter 3

Novel approach for fabricating nanochannel template for SiNW growth and investigation of sacrificial material for nanochannel formation

As discussed in chapter 2, there are several challenges faced in encapsulated nanowire growth approach with optimized capping layer. To solve these problems, this thesis proposes a novel approach for fabricating nanochannel template for SiNW growth. Additionally, this thesis explores the alternatives of sacrificial material for nanochannel formation in order to replace gold as sacrificial material. For this approach, it is based on and improves the previously developed encapsulated growth approach with optimized capping layer by our group. Therefore, the approach is capable of solving the challenges involved with that encapsulated approach while maintaining all the benefits of it. Specifically, this thesis is seeking to replace the expensive and time consuming electron beam lithography with high throughout and low cost nanoimprinting lithography for patterning the sacrificial material of nanochannel template. Furthermore, the thesis found the polymer materials are the best candidates as a replacement of gold sacrificial material for nanochannel formation, considering the nanoimprinting lithography patterning technique used. Because the polymer material could be directly imprinted on the substrate without intensive and complex process steps involved, which will make the fabrication process simpler and easier. In this thesis, we have explored the two polymers as sacrificial material of nanochannel template, including water soluble imprinting resist (NXR-3022, Nanonex Corp.) and thermoplastic imprinting resist (NXR-1025, Nanonex Corp.), which is soluble in general mild solvents, such as acetone, isopropyl alcohol (IPA) and toluene and so on.
3.1 Introduction to nanoimprinting lithography

Nanoimprinting lithography is a high-throughput, low-cost and high resolution lithographic technique, which was proposed by Stephen Y. Chou’s group from Princeton University in 1996 [50-52]. Nanoimprinting lithography takes full advantages of both conventional optical lithography and e-beam lithography and has the capability of patterning sub-10nm feature with high throughput and low cost. Therefore, it is more likely to become a manufacturing technology. In addition, nanoimprinting lithography has the ability to pattern 3-dimensional structures [53]. Recently, Chou’s group has reported the printing of sub-20nm wide graphene ribbon arrays with excellent uniformity over large area and process repeatability [54]. To date, Scientists have successfully demonstrated nanoimprint lithography’s applications for fabricating nanoscale electronics including high electron mobility transistors, photodetectors, silicon quantum-dots, quantum-wires, and ring transistors [55 - 59].

Basically, for nanoimprinting lithography, there are two steps: imprinting step and pattern transfer step, as shown in Fig. 3-1[60]. During imprinting step, the prefabricated mold with desired nanostructures is first pressed onto the precoated substrate with resist, and then removed from the substrate. In the second step, the anisotropic reactive ion etching (RIE) process is performed to remove the residual resist and complete the pattern transfer process. There are many different types of nanoimprinting lithography such as, electrochemical nanoimprinting and laser assisted direct imprinting so on [61-62]. Among them, thermoplastic nanoimprinting lithography (T-NIL) and UV nanoimprinting lithography (UV-NIL) are the most commonly used ones.
3.1.1 Thermoplastic nanoimprinting lithography (T-NIL)

Figure 3-2 shows the schematic of typical T-NIL process. At the beginning, a thin layer of thermoplastic imprinting resist is spincoated onto the sample substrate and the recommended resist thickness is within 50-200nm range for successful imprinting [60]. Then the mold, which is generally made of Si or SiO2 coated Si wafers and has predefined features, is brought into contact with the sample and they are pressed together for certain amount of time under a specific pressure. When the sample substrate is heated up above the glass transition temperature of thermoplastic imprinting resist, the polymer becomes a liquid polymer and fills up the void features in the mold through capillary force. After being cooled down, the mold is separated from the sample and the resist pattern is left on the substrate. The mold needs to be coated by anti-adhesive monolayer
of self-assembled (SAM) for easier mold separation from sample substrate without damaging the mold, the sample or sometimes the transferred resist pattern on the substrate. Usually, after T-NIL there is some residual layer left among the transferred features and its thickness is determined by the original imprinting resist thickness. Therefore, anisotropic RIE is needed for removing the residual layer. Since the features in the resist are also usually transferred by etching to material below the resist, RIE is also used for pattern transfer into the underneath substrate. Since most thermoplastic imprinting resists can be easily removed by the wet solvents, such as acetone or IPA, cleaning up after pattern transfer is straightforward.

Fig. 3-2: The schematic of thermoplastic NIL process: (a) thermoplastic resist coated sample substrate and mold with desired nanostructures fabricated through e-beam lithography, (b) mold is put in contact with thermoplastic imprinting resist, (c) mold separation from sample substrate, and (d) anisotropic RIE etching to remove residual resist layer. Figures have been adapted from reference [63].

Recently, researchers have successfully developed the advanced thermoplastic NIL without remaining residual layer as shown in Fig. 3-3 [64]. In this technique, first, the imprinting resist layer is transferred from sample substrate to the mold after
thermoplastic NIL. (Fig. 3-3 (a)) And then resist residual layer is removed by solvent developer or dewetting method. (Fig. 3-3 (b-c)) Finally, the isolated imprinting resist lines are transferred from the mold to specific substrate for further applications. There are several advantages for this technique. First, there is no plasma RIE process involved, which could further increase the throughput and lower the cost of nanoimprinting process. Second, this technique nondestructively removes residual layer and could be used for organic nanoelectronics applications, which is sensitive to RIE process.

![Fig. 3-3: The schematic of T-NIL without residual layer: (a) layer transfer from substrate to mold, (b) residual layer removal with solvent, (c) resist removal with dewetting. Figures have been adapted from reference [64].](image)

### 3.1.1 UV- nanoimprinting lithography (UV-NIL)

Figure 3-4 shows the schematic of typical UV-NIL process. Firstly, a UV sensitive and curable resist is dispersed or spincoated on the sample substrate and the mold is normally made of transparent material like fused silica or quartz. And then the mold is put down and in contact with the substrate. A similar filling process into the trench on the mold as in T-NIL happens and subsequently the resist is cured by UV light exposure thereby
becoming crosslinked. After mold separation, a similar residual etching process through RIE would be needed and also pattern transfer process can be used to transfer the pattern in resist onto the underneath material. Unlike thermoplastic imprinting resist, most of the UV imprinting resists become insoluble in general mild or even strong solvents, like PG remover or 1165 remover after being crosslinked through UV exposure. Therefore, oxygen plasma treatment is needed for removing the top crosslinked UV imprinting resist after pattern transfer.

Compared with T-NIL, the UV-NIL technique is more expensive and complex for the following reasons:

1. In UV-NIL technique, the mold is usually made of expensive quartz, which could increase the cost of UV-NIL. However, for T-NIL, the mold could be cheaper Si wafer or SiO2 coated Si wafer.

2. The imprinting system of UV-NIL integrated with UV lights source is more complex and cost more as well.

3. For UV-NIL, the sample substrate needs to be double polished for successful imprinting, which would increase the cost of UV-NIL as well.
Fig. 3-4: The schematic of UV NIL process: (a) UV resist coated substrate and mold with desired nanostructures fabricated by e-beam lithography, (b) mold is pressed into UV resist with UV radiation to harden the resist, (c) mold removal from sample substrate, (d) anisotropic RIE dry etching to remove residual UV resist layer and underneath layer. Figures have been adapted from reference [63].

In 2004, researchers have developed a novel UV-NIL technique that can achieve the imprinted resist patterns without residual layer as shown in Fig. 3-5 [65]. This technique combines the UV-NIL with optical lithography and takes the advantages of them. The big difference from standard UV-NIL is the mold and in this technique, a mask mold with metal on top of the protruding patterns is used for blocking lights from exposing the residual layer, thereby being developed away in the developer after imprinting. For this approach, the imprinted feature might have tails on both sides due to the diffraction of lights causing partial exposure of residual layer and it will become even worse for thicker residual layer and smaller features.
Fig. 3-5: The schematic of CNP technique, (a) a mask mold and SU-8 resist coated substrate, (b) imprinting with mask mold and UV flood exposure, (c) mold separation from substrate, (d) residual layer using through SU-8 developer. Figures have been adapted from reference [65].

3.2 Nanochannel template fabrication by exploiting different sacrificial materials

In this thesis, we proposed the novel nanochannel templates fabrication method, which combines the use of thermal nanoimprinting lithography, a sacrificial polymer nanowire etching technique, and conformal ALD deposition. As previously discussed, the use of nanoimprinting lithography and sacrificial polymer allows us to solve the challenges faced with the current encapsulated template growth approach with optimized capping layer while taking full advantages of it, including the precise control of the width,
length, interspacing, position and orientation of the grown SiNWs. Therefore, this improved approach provides the viable path towards the mass production applications. Fig. 3-6 shows the schematic of novel nanochannel template fabrication technique by nanoimprinting lithography. The detailed fabrication processes are as follows:

1. It starts with oxide coated Si or glass substrate. And then define the gold strip serving as catalyst on substrate by e-beam lithography patterning, thermal gold deposition and lift off process. (Fig. 3-6 (a) )

2. Sacrificial polymer nanowire for nanochannel formation is patterned by thermoplastic nanoimprinting lithography and anisotropic RIE residual layer etching after nanoimprinting and its dimension is 100nm and 40nm in width and height, respectively. (Fig. 3-6 (b) )

3. Cap the sacrificial polymer nanowire through ALD deposited Al2O3 and then define the window to expose partially the polymer nanowire for further etching process. (Fig. 3-6 (c) )

4. Sacrificial polymer nanowire wet removal by solvents or water to form the nanochannel. (Fig. 3-6 (d) )

5. Confined SiNWs VLS growth using the above fabricated nanochannel template. (Fig. 3-6 (e) )

6. Finally, remove part of the capping layer to partially expose the grown SiNW for device fabrication. (Fig. 3-6 (f) )

In this thesis, only several samples were prepared with glass substrate for later Raman spectroscopy characterization and the rest of samples were prepared on the Si substrate with 2um thick thermal SiO2 and 10nm ALD HfO2 on the top and those oxides
are used for insulating, smooth nanochannel floor surface and etching blocking layer when removing the capping layer through BOE wet etching to expose partially the grown SiNWs. Because ALD deposited HfO2 film is highly resistant to BOE wet etching. Therefore, it is an excellent etching masking layer.

![Image](image.png)

**Fig. 3-6:** The schematic of nanochannel template fabrication and SiNW growth: (a) gold catalyst patterning, (b) polymer nanowire patterning by T-NIL, (c) defining window to expose partially polymer nanowire, (d) removal of polymer nanowire, (e) confined SiNW growth within nanochannel through VLS, (f) partially expose the grown SiNW for device fabrication.

In this thesis, the imprinting mold is made of Si substrate with 2um thick thermally grown oxide. It was patterned by e-beam lithography (Zep520A resist used). And then RIE process was performed in MERIE to form SiO2 trench and the dimension of the etched trench is around 125nm and 210nm in width and height, respectively, as shown in Fig. 3-7. Finally, the resist was stripped away in PG remover. Usually the mold is cleaned in Nanostrip for 15mins at 75°C in order to remove possible organic contaminations within the mold for defect free imprinting.
Fig. 3-7: FESEM image of T-NIL mold made of SiO2 coated Si substrate without removing the resist etching mask.

3.2.1 Single layer nanoimprinting for patterning the sacrificial polymer

In this thesis, at the beginning, we explored single layer T-NIL for patterning the sacrificial polymer nanowire. The used imprinting resist could be serving as sacrificial material and therefore direct imprinting of sacrificial polymer is simple and straightforward. There are two types of T-NIL resists, which could be used as sacrificial polymer. One is water soluble imprinting resist (NXR-3022, Nanonex Corp.), and the other is general mild solvents soluble imprinting resist (NXR-1025, Nanonex Corp.). Considering the further wet removal of sacrificial polymer NW, the NXR-3022 imprinting resist is more economically and environmentally friendly. Because it is water soluble and free from any mild or harsh solvents. However, this thesis has exploited both
of them as sacrificial polymer for investigating the possible alternatives of sacrificial materials thereby optimizing that.

### 3.2.1.1 Water soluble polymer

Fig. 3-8 shows the schematic of sacrificial polymer patterning through T-NIL and RIE procedures. Specifically, the imprinting process (250 psi, 150 °C, 5 min, Nanonex NX-2000 imprinter) was performed on the substrate with pre-patterned gold strip, obtaining a 110 nm high and 100 nm wide resist nanowire with around 150 nm residual layer as shown in Fig. 3-9. Then, O₂ plasma etching (50 sccm, 500 W, 10 mTorr, 55 s) was performed to remove the residual layer. After oxygen plasma treatment, the surface of sacrificial polymer nanowire got modified and roughened as shown in Fig. 3-10. We have attempted to tune the etching conditions (pressure, power and etching gas) for improving the roughening problems. However, none of them worked.

![Diagram](image)

**Fig. 3-8:** Schematic of sacrificial polymer patterning through T-NIL and RIE procedures: (a) NXR-3022 coated substrate, (b) patterned sacrificial polymer nanostructure formed by T-NIL and RIE.
Fig. 3-9: FESEM image of as-imprinted sacrificial polymer nanowire on sample substrate with pre-patterned gold strip.

Fig. 3-10: FESEM image of sacrificial polymer nanowire after oxygen plasma RIE process to remove residual layer.
3.2.1.2 Solvent soluble polymer

As discussed above, the water soluble imprinting resist is not suitable for sacrificial polymer for forming nanochannel due to the surface roughening problem after O₂ plasma treatment. Therefore, we switched the sacrificial polymer to another imprinting resist (NXR-1025), which could be dissolved in general solvents such as, acetone, IPA and toluene so on. The similar imprinting process as NXR-3022 did was performed. Specifically, the imprinting process (250 psi, 95 °C, 5 min, Nanonex NX-2000 imprinter) was performed on the substrate with pre-patterned gold strip as catalyst (500 nm in width and 20 nm in height), obtaining a 140 nm high and 100 nm wide resist nanowire with around 195 nm residual layer, as shown in Fig. 3-11. Then, O₂ plasma etching (50 sccm, 250 W, 10 mTorr, 2 min 10 s) was performed to remove the residual layer. For NXR-1025 imprinting resist, its glass transition temperature is lower than that of NXR-3022 and around 55 °C. Therefore, it is necessary to perform lower power O₂ plasma etching for NXR-1025 imprinting resist. We have observed that the patterned sacrificial polymer nanowire reflowed and was widened substantially during the plasma etching, when the etching power was set up to be 500 W. However, similar etching problems were observed again after oxygen plasma treatment as shown in Fig. 3-12. Further experiments also found that the polymer roughened and modified by O₂ plasma becomes not soluble in the solvents any more. According to the above results, apparently, the direct imprinting of sacrificial polymer is not the best option for making nanochannel template. The possible solutions to solve these problems are as follows:

1. Exploring the advanced imprinting technique without residual layer
2. Utilizing double layer imprinting technique and transferring pattern down to sacrificial polymer.

**Fig. 3-11**: FESEM image of as-imprinted sacrificial polymer nanowire on sample substrate with pre-patterned gold strip.
3.2.2 Double layer imprinting for patterning sacrificial polymer

We have developed the double layer T-NIL approach for patterning the sacrificial polymer in order to solve the etching problems faced with single layer direct imprinting of sacrificial polymer. In this technique, we have combined the water soluble polymer (NXR-3022) with solvent soluble polymer (NXR-1025) due to their great compatibility, such as no intermixing on the interface. Fig. 3-13 shows the schematic of sacrificial polymer patterning through double layer T-NIL and RIE procedures. The specific process is as follows:

1. Spin coating sample substrate with both imprinting resist. (Fig. 3-13 (a))
2. The double layer structure was nanoimprinted (250 psi, 95 °C, 5 min, Nanonex NX-2000 imprinter) on the substrate with pre-patterned gold strip as catalyst (500 nm in width and 20 nm in height) and then O₂ RIE (50 sccm, 250 W, 10 mTorr, 1min 30 s) was performed to remove the residual layer. (Fig. 3-13 (b))
3. A continued O₂ RIE etched through the 50 nm thick sacrificial polymer layer masked by the top imprinting resist. (Fig. 3-13 (c))
4. Stripping the top imprinting resist in methyl isobutyl ketone (MIBK) solvent, which is only dissolving NXR-1025 without hurting the bottom sacrificial polymer. (Fig. 3-13 (d))

Figure 3-14 shows the FESEM image of patterned sacrificial polymer after top imprinting resist removal. As can be seen from this image, the top imprinting resist was not completely removed and some residuals were still left on only side of the patterned nanowire. In our experiments, we have observed that the residuals always exist no matter...
how long the sample was soaked in MIBK solvent. A possible explanation is as follows: the top part of imprinting resist was modified and roughened during oxygen RIE process, and then they become insoluble in MIBK solvent. However, the bottom part of the imprinting resist was less affected by the oxygen plasma treatment and they are still soluble in MIBK solvent. Ideally, the top imprinting resist should be stripped away once the bottom supporting structure is dissolved. However, due to capillary force, the undissolved imprinting resist would be still attached to the underneath patterned sacrificial polymer.

Fig. 3-13: Schematic of sacrificial polymer patterning through double layer T-NIL and RIE procedures: (a) NXR-3022 and NXR-1025 coated substrate, (b) patterning of the top imprinting resist(NXR-1025) through T-NIL and RIE, (c) pattern transfer to the bottom sacrificial polymer(NXR-3022) through RIE, (d) the top imprinting resist removal in methyl isobutyl ketone (MIBK).
3.3 Summary

In this chapter, we have presented the novel approaches for fabricating nanochannel template by combing the use of nanoimprinting lithography and the sacrificial polymer. Specifically, two methods have been discussed including the single layer imprinting technique for directly patterning the sacrificial polymer on the substrate and double layer imprinting technique for indirectly patterning the sacrificial polymer by pattern transfer. In addition, two polymers have been investigated for the potential of being sacrificial material for nanochannel formation involving water soluble polymer and solvent soluble polymer. However, due to the etching problems of polymers in single layer imprinting and residuals in double layer imprinting, as described previously, none of these approaches would work for our purpose. Therefore, it requires new solutions to
solve these problems. In the next chapter, we have developed the new approach for solving these problems by switching the sacrificial polymer to inorganic amorphous Si and will discuss in details.
Chapter 4

Novel approach for fabricating nanochannel template for SiNW growth using amorphous Si as sacrificial channel material

The novel approach of fabricating nanochannel template by the use of both T-NIL and sacrificial polymer for encapsulated SiNW growth was discussed in chapter 3. In this research, we will continue modifying and utilizing this approach. These modifications and the resulting challenges from experimental design and fabrication process optimization are presented in detail in this Chapter.

4.1 Introduction

As described in chapter 3, new solutions are required for solving the etching problems of sacrificial polymer for forming nanochannel. Therefore, in this chapter, we have developed the new approach for fabricating nanochannel template by switching the sacrificial polymer to inorganic amorphous Si. This new approach is built on and improves the approach of fabricating nanochannel template by combining the use of T-NIL and polymer sacrificial material, as discussed in chapter 3, while maintaining the benefits of that approach. In this research, we explored and utilized the amorphous Si as sacrificial material for nanochannel formation for several reasons: first, amorphous Si is a cheaper material and could be easily deposited by either PVD or PECVD deposition technique. Second, amorphous Si is compatible with most of fabrication processes used in this research. Third, amorphous Si is also commonly researched and many related processes have been well understood and established. Finally, unlike sacrificial polymer material, amorphous Si could be isotropically dry etched in dedicated etching tool using
xenon difluoride gas (XeF2). That is the biggest advantage and key unique of choosing amorphous Si as sacrificial material for nanochannel formation. Because the dry etching removal of amorphous Si could provide the following benefits:

First, it is faster to remove sacrificial material by dry etching process, especially for long nanochannel template, compared with wet removal of sacrificial material by liquid chemicals. Because the vapor gas used in dry etching of amorphous has longer diffusion length than the liquid regents of their counterparts. Therefore, the vapor reactive gas could easily diffuse into the channel in nanoscale to etch away the sacrificial material. Meanwhile, the volatile by products produced in dry etching process could be pumped out from the nanochannel in a short time as well. Second, this dry etching process is highly selective to other materials. Recently, researchers also found it becomes extremely selective when inert gas, such as nitrogen, argon or helium is added into the etching gas of XeF2 [66].

4.2 Experiment design and process optimization

In this section, the process development and optimization for fabricating nanochannel template by using amorphous Si as sacrificial material will be presented in detail. Unlike polymer sacrificial material, there are several factors that needs to be taken into account when designing experiments and optimizing fabrication process.

First, amorphous Si could not be directly nanoimprinted on substrate as polymer sacrificial material did, as described in previous chapter. Therefore, amorphous Si thin film needs to be patterned by pattern transfer process masked by imaging resist, which could done by either e-beam lithography or nanoimprinting lithography technique.
Second, gold catalyst used in this research for SiNW growth can be easily diffused into the amorphous Si thin film. Therefore, the diffusion problem needs to be considered when performing the experiments design.

Third, the etching resistance of capping layer and floor material of nanochannel to XeF₂ etching gas needs to be considered seriously, although we have pointed out that XeF₂ etching gas is highly selective to most of materials. Because the lateral etching rate of sacrificial amorphous Si confined within nanoscale size is much slower than that of its counterparts in open and without any confinement.

4.2.1 Nanochannel template fabrication process

Figure 4-1 shows the schematic demonstrating the nanochannel fabrication process using amorphous Si as sacrificial material. First, 10nm thick ALD deposited HfO₂ thin film was put on the Si substrate with 2um thermally grown SiO₂. There are three functions for this HfO₂ thin film. First, it provides smooth surface of nanochannel floor. Second, it is extremely resistant to XeF₂ etching. Therefore, it protects the nanochannel floor being etching during sacrificial removal. Finally, it is highly resistant to BOE etching and so it acts as blocking layer when removing the capping layer through BOE wet etching to expose partially the grown SiNWs. Subsequently, 50 nm sacrificial amorphous Si was sputtered on the ALD HfO₂ coated substrate. Next, amorphous Si was patterned by e-beam lithography and anisotropic RIE process (2 mTorr, 30 sccm SF₆/10 sccm Ar, 250 W, 35 s) to form as shown in Fig. 4-2. Next, 40 nm Al₂O₃ and 200 nm SiO₂ was deposited by ALD and PECVD, respectively, as capping layer, and then the capping layer was patterned by optical lithography to open up the window to partially
expose the amorphous Si nanowire. Next, XeF$_2$ etching was performed to remove the amorphous Si forming the nanochannel (3 Torr, 65 cycles). Next, gold catalyst strip (300 nm in width, 500 nm in length and 50 nm in height) was defined using e-beam lithography and deposited at the one end of the empty nanochannel. There is 100 nm overlap between the gold strip and capping layer of the empty nanochannel so that gold catalyst could sit right next to the empty nanochannel. Finally, gold catalyst was capped by 400 nm thick SiO$_2$ deposited by e-beam evaporation. Once the nanochannel template fabrication was completed, the SiNWs were grown through a VLS growth process accomplished in a low pressure chemical vapor deposition (LPCVD) furnace. And then grown SiNWs were partially exposed for device fabrication. These two steps will be discussed in detail later in the following section.

Fig. 4-1: Schematic of nanochannel template fabrication process for SiNW growth using amorphous Si as sacrificial material and further SiNW VLS growth for device fabrication: (a) deposition of sacrificial amorphous Si thin film (b) patterning of amorphous Si nanowire, (c) capping layer defining to open up window exposing partially the amorphous Si nanowire, (d) sacrificial amorphous Si nanowire removal to form the
nanochannel by XeF$_2$ isotropic dry etching, (e) gold catalyst patterning and oxide capping layer deposition to wrap gold.

Fig. 4-2: FESEM image of patterned amorphous Si nanowire without stripping resist.

4.2.2 Si nanowire growth in the prefabricated nanochannel template

SiNW VLS growth was performed in an Atomate LPCVD system at a temperature of 500$^\circ$C, a total pressure of 13 Torr, and a 100 sccm flow rate of SiH$_4$ and H$_2$, in which silane is diluted to 10 % in H2. The total growth time was 1 hour and 15 mins. Finally, the furnace was purged with N$_2$ and then pumped until the system was cooled down to room temperature. This process results in SiNW growth in the nanochannels, as shown in Fig. 4-3.
After SiNW is grown in the nanochannel template, it needs to be partially exposed for further device fabrication as shown in Fig. 4-3. First, the capping layer is patterned by optical lithography, and then dry etched to remove PECVD deposited oxide. Next, the sample is wet etched in BOE to remove the remaining ALD deposited Al$_2$O$_3$ nanochannel interfacial layer. The reason for performing dry etching first and then wet etching to remove oxide capping layer is that dry etching could possibly damage and roughen the surface of SiNWs, which will degrade the device performance. After this step, the photoresist is removed and BOE etching (1 min) is conducted to remove the native oxide formed on the surface of SiNWs. Subsequently, the sample is etched by commercially available TFA gold etchant for 1 min (Transene, Inc) to remove possible gold residual on the surface of SiNW, especially on the tip as shown in Fig.4-3.

**Fig. 4-3:** Schematic of SiNW grown in the nanochannel template and etching of capping layer to partially expose SiNW: (a) prefabricated nanochannel template, (b) SiNWs grown in the nanochannel template, (c) a portion of capping layer removed to partially expose SiNW, (d) the grown SiNW was cleaned by BOE and gold etchant.
4.3 Encapsulated grown SiNW characterizations

After the SiNWs have been grown in the nanochannel template, exposed and cleaned, they are characterized to determine their physical dimensions, surface morphology and electrical and structural properties including crystallinity, and conductivity.

4.3.1 FESEM characterization

The size and morphology of the grown SiNWs was analyzed using Carl Zeiss field-emission scanning electron microscope (FESEM) equipped with a backscattered electron detector and energy dispersive spectrometer (EDS). The FESEM overview image and high-magnification close-up FESEM image of SiNWs grown using the previously described approach have been shown in Fig. 4-4 and Fig. 4-5, respectively. From these images, it can be clearly observed that the SiNW has grown and been exposed, as being perpendicular to the oxide capping layer left for anchoring SiNWs. In addition, high-magnification close-up FESEM image also shows smooth morphology of the exposed SiNW and the size is around 100 nm in width, which is approximately the same size as the nanochannel fabricated using the above described fabrication process. Therefore, this encapsulated nanochannel templates approach not only provides a good way to precisely control the position of the wires on the substrate as well as the growth direction and the dimensions of the grown nanowires, but also it has the greatest capability of growing high quality SiNWs. Unlike previously described “grow and place” approaches, the approach also offers a simple and suitable way to fabricate single nanowire device and investigate the nanowire properties without advanced post growth alignment and assembling techniques.
**Fig. 4-4:** FESEM overview image of exposed SiNW with part of capping layer left for anchoring the exposed SiNW.

**Fig. 4-5:** Higher magnification image of exposed SiNW.
4.3.2 Raman and TEM characterization for crystallinity

Raman characterization to determine crystallinity of the grown SiNWs using the approach of discussed in this chapter was performed using Renishaw inVia Raman Microscope. The laser excitation was set to 514.5 and focused to a spot size of between 0.8 -1.0 µm using a 100x microscope objective.

Figure 4-6 shows the results for Raman spectroscopy analysis of the sample with SiNWs growing in the nanochannel templates fabricated on the glass substrate and a comparison sample of blank glass slide. For the sample with SiNWs, there is a strong peak found and located around 520 cm\(^{-1}\), which only indicates the crystal property of grown SiNWs, but not guarantee it has single crystal structure.

In order to determine the grown SiNWs are single crystal, high resolution transmission electron microscopy (HRTEM, JEOL, EM-2010 F) analysis was performed. For this purpose, the single SiNW was grown and exposed first. And then it was cut radially by focused ion beam (FIB, FEI Company Quanta 200 3D Dual Beam FIB), in which thin gold was deposited on top of the nanowire so that a good image could be obtained for easily locating the nanowire. Next, the SiNW piece was put in a TEM copper grid and subsequently loaded into TEM for imaging.

Figure 4-7 shows HRTEM cross section image of a SiNW grown in the nanochannel template fabricated by above mentioned approach. In this image, the ordered lattice structure can be observed, which indicates it is single crystal. In addition, the electron diffraction determines its crystal orientation is \(<111>\), as shown in Fig. 4-7 (C). Therefore, we could confirm the encapsulated grown SiNWs are single crystal based on the results of Raman spectroscopy and HRTEM.
Fig. 4-6: Raman spectroscopy result for the samples of SiNW grown in the nanochannel templates on the glass substrate and bare glass substrate without SiNW.

Fig. 4-7: HRTEM image of a SiNW: A) TEM intersection image of SiNW, B) higher magnification TEM image of SiNW, C) electron diffraction of SiNW indicating its (111) crystal orientation.
4.3.3 Electrical properties characterization

After growth, the SiNWs are characterized to determine the resistivity/conductivity by four point probe approach. Fig. 4-8 shows the schematic for fabricating four point probes on SiNWs and the specific process flow is as follows. First, after the SiNWs were grown and partially exposed by using a portion of the template as an anchor, the sample was dipped in buffered oxide etch (BOE) solution for removing the native oxide. Subsequently, gold etching was performed in a commercially available gold etchant (Type, TFA, Transene, Inc) in order to remove any gold remnants on the surface of grown SiNWs. Next, the sample was subjected to dry thermal oxidation (700 °C for 4 h) to grow roughly 10 nm oxide. (Fig. 4-8 (a)) This thermally grown oxide will be used for gate dielectrics of SiNW transistor and will be discussed in next chapter. Next, the four point probes were patterned by optical lithography and etched in BOE solution to remove the thermally grown oxide exposing SiNW for forming contacts. (Fig. 4-8 (b)) Finally, the contacts were formed by e-beam deposition (1 nm Ti and 80 nm Ni) and lift off process. (Fig. 4-8 (c)) in this research, Ti has been used as adhesion layer and Ni as electrode metal, which was investigated and optimized as four point probes contacts by former graduate student (Dr. Garg) [46]. Fig. 4-9 shows the top view FESEM image of four point probes fabricated on encapsulated SiNW grown in the nanochannel templates fabricated by the previously described above. The probes are 2 µm in width and spaced apart of 2 µm between neighboring probes. In this research, no annealing process is needed for improving the contacts as the four point probe approach can avoid the effect of contact resistance. In addition, the high temperature annealing process will silicide the SiNW and affects its resistivity.
Fig. 4-8: Schematic of process steps for fabricating four point probes on a partially exposed SiNW grown in the nanochannel templates: (a) dry thermal oxidation to grow approximately 10 nm thick oxide, (b) patterning of four point probes by optical lithography and BOE etch, (c) metal electrode contacts formed by e-beam deposition and lift off process.

Fig. 4-9: Top view FESEM image of four point probes fabricated on encapsulated SiNW grown in the nanochannel templates fabricated by the previously described above.

Figure 4-10 shows the schematic of four point probe measurement built on a SiNW. In this technique, a known voltage is swept across the two outer probes leading to
the current flowing through the nanowire. And then the voltage difference across the two inner probes is measured. The biggest advantage of this four point probes techniques is that it allows us to calculate resistance of SiNW segments between two inner probes without considering the contact resistance effect since there is no current flowing across the two inner contacts. Once the resistance of SiNW is known, the bulk resistivity can then be calculated by combining the NW’s dimensions and above calculated resistance. The equations used for calculating both of resistance and resistivity are shown in the following.

\[ R_{23} = \frac{V_{23}}{I_{14}} \] \hspace{1cm} (4.1)

\[ \rho_{SiNW} = R_{23} \times \frac{WH}{L_{23}} \] \hspace{1cm} (4.2)

Where W and H are the width and height of SiNW and L\textsubscript{23} is the length of SiNW between two probe 2 and probe 3. These parameters could be measured from the FESEM analysis. The Fig. 4-11 shows the measured current-voltage (I-V) characteristics (Agilent 5145C Oscilloscope). The resistance of grown SiNW could be taken from the slope of this linear curve and it is around $1.58 \times 10^{10} \Omega$. And then the resistivity can be calculated using above equation (100 nm wide by 40 nm high SiNW with spacing of 2 \( \mu \)m between probe 2 and probe 3). The resistivity is around 3160 \( \Omega \)-cm, which is lower than bulk silicon ($10^5 \Omega$-cm) [67-69]. The resistivity varied a little among wires ranging from 3000 \( \Omega \)-cm to 5200 \( \Omega \)-cm (around $10^3 \Omega$-cm) due to the different amount of gold incorporated into SiNW during growth. According to the lower resistivity than bulk silicon, the conclusion could be made that the Au catalyst unintentionally dopes the SiNW, which has been supported by previous study in our group [46] and the linear relation of I-V graph also demonstrates is p-type doped, which has been reported by other groups [29, 67-74].
Fig. 4-10: Schematic demonstrating four point probe measurement built on a SiNW.

Fig. 4-11: Experimental results of four point IV characteristics of grown SiNW.
4.4 Summary

In this chapter, a novel approach of fabricating nanochannel templates for SiNW growth has been demonstrated. In this approach, the sacrificial material has been switched from gold to the amorphous Si and this change has solved challenges faced with the encapsulated nanochannel templates approach using gold as sacrificial material. The SiNWs were also successfully grown with good morphology characterized by FESEM. In addition, the Raman spectroscopy and TEM characterization were performed to determine the crystallinity. Finally, four point probe measurements were conducted to characterize the electric properties of grown SiNWs.
Chapter 5

Field Effect Transistors on nanochannel template grown encapsulated SiNW

Recently, nanowire devices have been attracting tremendous interest due to the scaling limit of conventional silicon devices. Among these nanowire devices, SiNW devices have been intensely investigated and shown the greatest promise for future applications due to its excellent compatibility with current Si dominated semiconductor industry and well understood and established material properties. Therefore, in this thesis, the main purpose of developing a novel approach of fabricating nanochannel templates for SiNW growth is to fabricate SiNW based devices in an easy and simple way without post growth alignment and assembling techniques involved, which points the way towards the large scale applications of SiNWs based devices. As discussed in chapter 4, we have successfully grown SiNWs in our nanochannel templates fabricated by using the amorphous Si as sacrificial nanochannel material. Therefore, in this chapter, we will explore the fabrication and performance of FETs on our encapsulated grown SiNWs. Up to date, scientists have developed different transistor structures and fabrication methods for making nanowire transistors, including top-gate structure, back-gate structure and top-back combination structure. Among them, the accumulation mode MOSFET is the simplest transistor structure, which will be used for fabricating our SiNW based transistors.

5.1 Introduction to AMOSFT

The first concept of accumulation mode metal oxide field effect transistor (AMOSFET) was originated from the concept of gated resistor, which was proposed by
Julius E. Lilienfeld in 1925 [75]. However, this type of transistor concept has not been realized experimentally until 2007. It was first demonstrated experimentally by our group using SiNWs grown by our “grow-in-place” approaches [48, 76-77]. In the following couple of years, several other groups have reported similar transistor structures with different names, such as junctionless FETs, vertical slit FETs and nanowire pinch-off transistors [78-83] and in principle, all of them have worked as gated resistors.

Figure 5-1 shows the schematic of AMOSFET on an n type substrate. As can been seen, the AMOSFET is structurally different from the conventional MOSFET. Since there is only one doping type used (n doping or p doing) and no junctions needed as conventional MOSFETs do. Therefore, it is an extremely simple transistor structure. Compared with conventional MOSFET devices, AMOSFETs have the following advantages: first, its fabrication process is extremely simple and easy, which could lower down the overall cost of making devices. Therefore, it shows the greatest promise for mass manufacturing applications. Besides the easy fabrication of AMOSFETs, its device performance is comparable and even could be better than MOSFETs when appropriate design is made. Second, with the constant scaling of nanoelectronics following Moore’s law, it becomes extremely challenging and difficult to control precisely the depth and length of shallow junctions within nanoscale and as discussed above, those shallow junctions are necessary for conventional MOSFETs. Therefore, the side effects would arise caused by inadequate control of doping for forming the shallow junctions used in the nanoelectronics, which would significantly affect the devices performance and sometimes even lead to device failures.
Due to the structure difference of AMOSFET with conventional MOSFET as discussed above, in principle, they are fundamentally different from each other as well. The overall operating mechanism of AMOSFET has been investigated numerically by our group [76-77]. Fig. 5-2 shows the schematic of AMOSFET operation under the on and off state. Since the active layer is p type doped, the device is turned on when negative gate voltage is applied with holes accumulating right underneath the gate region. The current will flow from source to drain when negative drain voltage is applied. As can be noticed, the AMOSFET is a majority carrier dominated device, contrary to conventional MOSFET (minority dominated device). The device is turned off when sufficiently enough positive gate voltage is applied with gated region depleted completely. Upon continuing increasing the gate voltage, some minorities (electrons) will be produced and accumulated underneath the gated region. However, the device is still under off state. Because the source and drain regions are p type doped and the p-n-p junction will be
formed blocking the current flow from source to drain. As noticed from Fig. 5-2 (b), the active layer has to be thin enough in order to completely deplete the gated region and turn off the device, which means nanoscale thickness is required to ensure the depletion of entire channel thickness. Therefore, this transistor structure is highly suitable for nanowire based devices. That is also the reason why the concept of AMOSFET has never been experimentally demonstrated until recently the nanotechnology techniques have been developed. The device would be saturated under on state, when more negative drain voltage is applied with the transverse electric field depleting the holes under the gated region.

![Fig. 5-2: schematic of AMOSFET operation: (a) on state with p type active layer, (b) off state with p type active layer.](image-url)
Table 5-1 shows the comparison of device physics for MOSFET and AMOSFET and summarizes all the difference between AMOSFETs and conventional MOSFETs and thin film transistors. In this table, $C_{ox}$ and $I_d$ is gate oxide capacitance and drive current, $\mu$ and $N_D$ are mobility and doping density, $q$ is a constant number, $T_{Si}$, $W_{Si}$ and $L$ are the height, width and length of the channel, $V_{TH}$ and $V_{SD}$ threshold voltage and source and drain voltage, respectively. According to the equations of drive current for both conventional MOSFET and AMOSFET, It can be clearly seen the difference between them. For conventional MOSFET, its drive current is controlled by the product of mobility and oxide capacitance. Therefore, the drive current is affected by heavy doping, which degrades the mobility due to scattering effects. However, for AMOSFETs, the drive current is a product of mobility and doping concentration, which means it is independent on gate oxide capacitance.

$$I_D \approx \mu C_{ox} \frac{W_{Si}}{L} (V_{SD} - V_{TH})^2$$

Conventional MOSFETs

$$I_D \approx q \mu N_D \frac{T_{Si} W_{Si}}{L} V_{SD}$$

AMOSFETs

<table>
<thead>
<tr>
<th>Device Type</th>
<th>Drive Current Proportional to</th>
<th>Dependence on Doping Density $N_D$ due to</th>
</tr>
</thead>
<tbody>
<tr>
<td>MOSFET (c-Si)</td>
<td>$C_{ox} \times \mu$ product</td>
<td>Mobility dependence on $N_D$</td>
</tr>
<tr>
<td>Conventional TFT</td>
<td>$C_{ox} \times \mu$ product</td>
<td>Mobility dependence on $N_D$</td>
</tr>
<tr>
<td>(a-Si and Poly-Si)</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
| AMOSFET (SiNWs)      | $N_D \times \mu$ product      | 1. Proportional to $N_D \times \mu$ product  
|                      |                               | 2. Mobility dependence on $N_D$         |

**Table 5-1:** The comparison of device physics for MOSFET and AMOSFET. This table has been adapted from reference [77].
5.2 AMOSFETs on encapsulated SiNWs

As discussed in previous chapter, the SiNWs have been successfully grown in the encapsulated nanochannel template fabricated by using amorphous Si as sacrificial layer. This technique has precise control on the nanowire size, position, growth direction and interspacing. Therefore, these grown SiNWs are self-positioned and self-assembled and could be directly fabricated into specific devices without post growth assembling processing steps needed. In this section, the AMOSFET on SiNWs grown in our encapsulated templates will be discussed.

5.2.1 AMOSFETs fabrication on encapsulated SiNWs

Figure 5-3 shows the schematic process steps for fabricating AMOSFETs on encapsulated SiNWs. Specifically, the overall fabrication process is as follows: after the nanowire growth and partially exposed by removing a portion of the capping layer, the sample was subjected to annealing process in N$_2$ atmosphere at 700° C for 3h and the anneal would push gold on the surface of SiNW moving towards into the core and further dope the SiNW. Next, BOE etching was performed to remove native oxide formed on the surface of SiNW. Subsequently, gold wet etching was carried out in commercially available gold etchant (Type TFA, Transene, Inc) to remove any possible gold remnants on the surface of SiNW. And then the nanowires were dry thermally oxidized to grow approximately 10 nm shell oxide on the surface of SiNW serving as gate dielectrics for the AMOSFET devices, as shown in Fig. 5-3 (a). Next, the source and drain region were patterned to expose SiNW for forming contacts by optical lithography and BOE wet etching as shown in Fig. 5-3 (b). Subsequently, 1 nm Ti adhesion layer and 100 nm Ni
metal electrode was deposited by e-gun evaporation and then lift off process was performed forming the source and drain metal contacts. Finally, gate metal was defined by optically lithography patterning and metal deposition (70 nm Ti as metal contact and 70 nm Ni as protecting layer from oxidation of Ti contact). Fig. 5-4 shows the FESEM image of fabricated AMOSFET device.

**Fig. 5-3**: Schematic process steps for fabricating AMOSFET on encapsulated SiNWs: (a) dry thermal oxidation to grown approximately 10nm SiO₂ as gate dielectrics, (b) patterning of source and drain region to expose SiNW for forming contacts by optical lithography and BOE wet etching, (c) Ti adhesion layer and Ni metal electrode deposition and lift off, (d) gate metal contact definition by optical lithography patterning, metal deposition and lift off.
5.2.2 Transfer characteristics of AMOSFETs on encapsulated SiNWs

After the AMOSFETs of SiNWs were fabricated, the sample was subjected to a thermal annealing process in forming gas environment (10% H₂ in N₂) at 400°C for 15 min in order to improve contact resistance and reduce interface states. Fig. 5-5 shows the experimental transfer characteristics of an AMOSFET on encapsulated SiNW at fixed $V_{DS} = -0.1$ V and the graph is plotted on the semilogarithmic scale. As can be seen, this device is in the on state when a negative gate voltage is applied, which agrees with the results that the encapsulated SiNWs are p doped. The threshold voltage is around 0 V, which means this device is normally on. In addition, this AMOSFET has an on current of a few nanoamperes with the On-state/Off-state current ($I_{on}/I_{off}$) ratio of around $10^6$, which is comparable with the results of AMOSFETs fabricated on extruded SiNWs and way better than that of AMOSFETs fabricated on encapsulated SiNWs grown in the nanochannel templates formed using gold as sacrificial layer and PECVD deposited SiO₂ as capping layer as shown in figure 5-6. The second parameter to characterize the transistor
performance is subthreshold swing and it characterizes how fast the transistors could be transitioned to on and off state. Experimentally, the subthreshold swing could be calculated from the slope of linear portion of the plot of logarithmic drain current versus gate voltage at fixed source and drain voltage. For our AMOSFETs fabricated on encapsulated SiNWs grown using the approach as discussed in this thesis, the subthreshold swing is around 92 mV/dec, as calculated from Fig. 5-5 transfer characteristics and it is the best result achieved among the AMOSFETs on encapsulated SiNWs and even comparable with the result reported by our group for AMOSFETs on an extruded SiNWs.

![Fig. 5-5: Experimental transfer characteristics of AMOSFET on encapsulated SiNWs.](image-url)
Fig. 5-6: Experiment transfer characteristics of AMOSFET on encapsulated SiNWs grown in the nanochannel templates using gold as sacrificial and PECVD deposited SiO\textsubscript{2} as capping layer. The figure has been adapted from reference [46].

5.3 Summary

In this chapter, at the beginning, the AMOSFETs were introduced, which is quite different from the well-understood conventional MOSFETs. For this type of transistor, it has extremely simple transistor structure. However, it has the potential of demonstrating excellent device performance. Therefore, it makes the AMOSFETs highly attracted to mass production applications. And then the successfully fabricated the AMOSFETs on our encapsulated SiNWs grown in the nanochannel templates fabricated using amorphous Si as sacrificial material were demonstrated. In addition, the device performance of these AMOSFETs has been characterized showing good performance with high on and off current ration and low subthreshold swing, as discussed above. Therefore, the approach developed in this thesis for fabricating the nanochannel templates for encapsulated SiNWs growth has the greatest potential for large scale manufacturing applications.
6.1 Summary

In this thesis, we introduced a novel approach for fabricating nanochannel templates for encapsulated SiNW growth and further device fabrication. In our research, at the beginning, we investigated the effects of the capping layer of nanochannel template on the quality of grown SiNWs and found that high dielectric constant oxides including Al$_2$O$_3$ and HfO$_2$ would be the optimal candidates for capping layer of nanochannel template. Using these oxides as capping layer of nanochannel template, high quality SiNWs with good surface morphology has been successfully grown in the nanochannel templates.

Further, we have explored several alternatives for sacrificial material of nanochannel template to replace the gold sacrificial material, which has been developed previously by our group. Although currently it shows several challenges using the organic polymer as sacrificial material for nanochannel template, the results obtained in our research have demonstrated the organic polymers would still be of the great interest to nanochannel template fabrication and there are potentials for being used as sacrificial materials.

Then we switched the sacrificial material from polymer materials to inorganic amorphous Si for fabricating the nanochannel templates for SiNWs growth. High quality SiNWs with good surface morphology and crystal structure have been successfully grown in nanochannel templates fabricated using amorphous Si as sacrificial layer. From the electric characterization, we have shown that the grown SiNWs are p type doped.
Finally, the AMOSFET devices have been successfully fabricated on our encapsulated grown SiNWs in the nanochannel templates fabricated by using amorphous Si as sacrificial material. From the electrical characterizations, these AMOSFETs have shown high performance with high on and off current ratio and sharp subthreshold slope.

6.2 Future work

More future work could be done in order to continue optimizing the nanochannel fabrication and transistor fabrication, making the whole fabrication processes as manufacturable as possible.

First, in this thesis, we have used the e-beam lithography to pattern the sacrificial material producing the amorphous Si nanowire for further nanochannel formation. In order to make this process manufacturable, the e-beam writing could be replaced by high throughput and low cost nanoimprinting lithography.

Second, in this research, the gold catalyst for VLS SiNW growth has been patterned by e-beam lithography. This could also be replaced by advanced stamping methods using gold nanoparticle and specific self assembling monolayer.

Third, in this research, we have explored several alternatives of sacrificial materials including water soluble polymer, solvent soluble polymer and inorganic amorphous Si. However, more work needs to be done for continuing optimizing the sacrificial materials and some possible candidates are as follows: thermally decomposable polymer and UV decomposable polymer which could be patterned by nanoimprinting lithography.
Fourth, more alternative metal catalysts for SiNW growth could be explored including cheaper Al, Cu and even metal compounds in order to avoid the use of expensive gold and possible contaminations Au catalyst might cause to active devices.

Fifth, for AMOSFET transistors, high k materials including HfO₂ and Al₂O₃ could be explored for gate oxide of SiNW AMOSFETs, which has the potential to continue improving the transistor performance.

Sixth, other properties of grown SiNWs using the approach we have developed could be investigated for exploring more applications of SiNWs, such as photoluminescence and electroluminescence effect.

Seventh, other type of nanowires could be grown using the approach we have developed in this thesis for different applications, such as GaN nanowire and GaN/AlGaN heterogeneous nanowire, which are very popular nanowires for high performance transistor and optoelectronics applications.
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SELECTED PUBLICATIONS

Journal publications: