The Pennsylvania State University

The Graduate School

Department of Materials Science and Engineering

PASSIVATION OF INGAN/GAN NANOPILLAR LIGHT EMITTING DIODES

A Thesis in

Materials Science and Engineering

by

Won Hyuck Choi

Submitted in Partial Fulfillment
of the Requirements
for the Degree of

Master of Science

August 2013

The thesis of Won Hyuck Choi was reviewed and approved* by the following:

Suzanne E. Mohney
Professor of Materials Science and Engineering and Electrical Engineering
Thesis Co-Advisor

Jian Xu
Associate Professor of Engineering Science & Mechanics and
Adjunct Professor of Electrical Engineering
Thesis Co-Advisor

Joan M. Redwing
Professor of Materials Science and Engineering, Chemical Engineering and Electrical Engineering
Chair, Intercollege Graduate Degree Program in Materials Science and Engineering

*Signatures are on file in the Graduate School

ABSTRACT

Recently, InGaN/GaN based blue light emitting diodes (LEDs) have become widely available commercially, but their efficiency is reduced due to the quantum confined Stark effect (QCSE) induced by the InGaN/GaN mismatch. These LEDs, when combined with a phosphor or other LEDs, can be used to provide white lighting, and maximizing their energy efficiency is desirable. Therefore, a new LED structure using nanopillars has been studied, which increases the surface area for light to escape as well as reducing the quantum confined Stark effect in order to improve the device efficiency. However, when InGaN/GaN nanopillars are prepared by dry etching, N vacancies and group Ⅲ oxides are created on the nanopillar sidewalls, causing excessive leakage current and non-radiative surface recombination. As a result, the internal quantum efficiency drops, and it degrades the device efficiency. In this research, reducing the etch rate and adding consecutive KOH wet etching and $(NH_4)_2S$/ isopropanol passivation steps were studied to reduce the sidewall damage and increase the device efficiency. The photoluminescence intensity in nanopillars prepared with the slow etch rate (0.18 nm/s) was 2 times higher than that of planar structures. In nanopillar LEDs, an additional 4 times higher electroluminescence intensity and suppressed leakage current under reverse and forward bias were recorded with sulfur passivation.

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

ACKNOWLEDGEMENTS

While I was performing this nanopillars LED project, there have been many people who have offered guidance and support. First of all, I would like to thank my co-advisors who are Dr. Suzanne E. Mohney and Dr. Jian Xu for offering me good guidance to accomplish this project successfully. I also appreciate Dr. Joan M. Redwing, another committee, for reviewing my thesis and giving good advice at my defense. I express my appreciation to Dr. Guanjun You, Jie Liu, Zhenyu Jiang, Michael Abraham, and Li Wang who provided me experimental support. Furthermore, I would like to thank my labmates, Joshua Yearsly, Shih-ying Yu, Anna Domask, Joyce Lin, and Katherine C. Kragh-Buetow, for helping me to use equipment and chemicals safely. My appreciation also goes out to nanofab staff, Guy Lavallee and Shane Miller, for providing assistance with dry etching tool operation. Most importantly, I express my deepest gratitude to my family for their sacrifice. Finally, I would like to acknowledge financial support of this research from the National Science Foundation.

Chapter 1

Introduction

1.1 General information on InGaN/GaN planar and nanopillar LEDs

A light-emitting diode (LED) is a semiconductor light source using the electroluminescence effect, which is explained by recombination of holes and excited electrons and released energy in the form of photons under forward bias [1]. The LED is a potential light source which can replace incandescent or fluorescent lamps due to its superior properties such as high luminescence efficiency, low energy consumption, long lifetime and quick response [2]. The light emitting diodes are currently used in various applications such as general lighting, traffic signals, aviation lighting and automotive lighting.

The white color LED is produced by packaging LED devices with three different primary colors of red, green and blue, which are determined by the unique energy gaps of the semiconductor materials. Among these three primary color LEDs, blue LEDs based on InGaN/GaN multi quantum wells have been an issue because obtaining high efficiency from blue LEDs is more difficult. Both InGaN and GaN have direct band gaps, and their band gap energies are 2.0 eV-3.4 eV and 3.4 eV. The band gap energy of InGaN is changeable depending on the ratio of InN to GaN in the $In_xGa_{1-x}N$ alloy. Figure 1-1 shows a cross sectional image of conventional planar InGaN/GaN LED. The n electrode is deposited on n-GaN, and the transparent p electrode (indium tin oxide) is deposited on p-GaN. Blue light is emitted when positive voltage is applied to the p electrode, whereas

negative voltage is applied to cause electron and hole recombination across the InGaN/GaN multi quantum well. Figure 1-2 shows the recombination process with a band diagram [2]

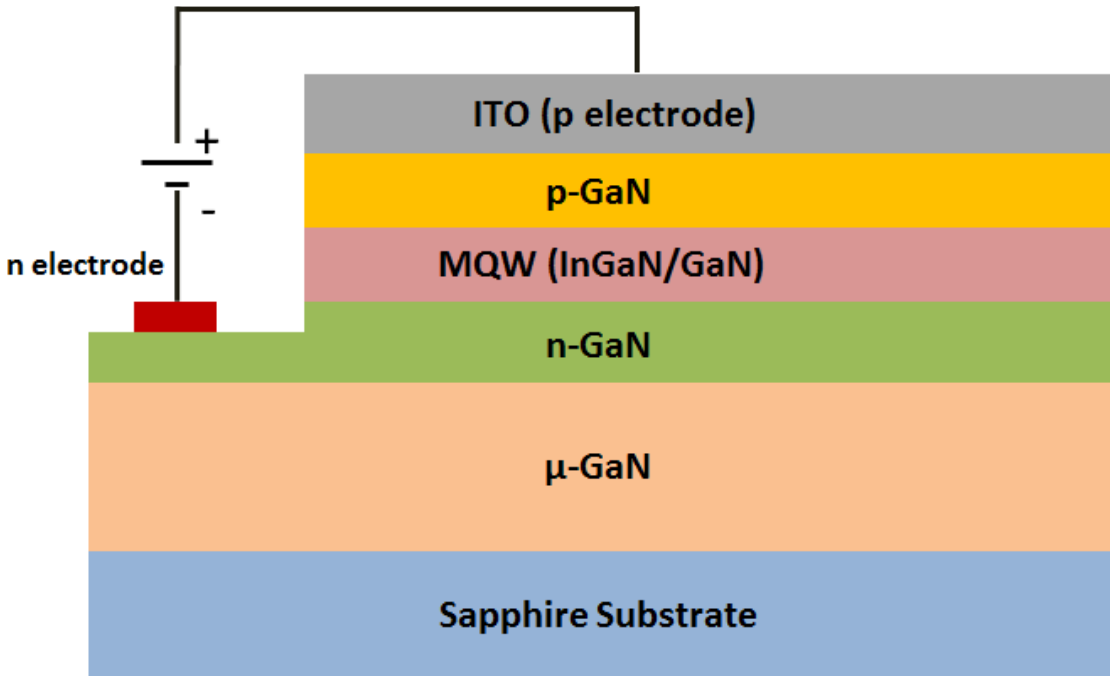


Figure **1-1** A cross sectional schematic of an InGaN/GaN planar LED.

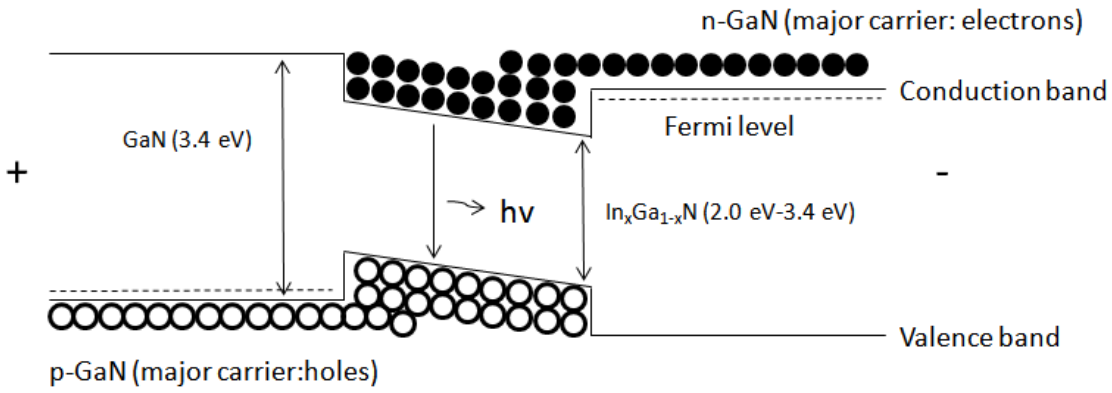


Figure **1-2** Energy band diagram of an InGaN/GaN LED.

There has been an issue with the InGaN/GaN planar LED sturucture. When the InGaN/GaN multi quantum well is deposited by the metal organic chemical vapor deposition (MOCVD) technique, the mismatch at the interface between InGaN and GaN layers induces strain in the multi quantum well. The piezoelectric field induced by the strain at the multi quantum well shifts electrons and holes to the opposite sites. As a result, it interrupts hole and electron recombination, and the internal quantum efficiency of the LED is degraded [3]. This phenomenon is called the quantum confined Stark effect (QCSE) [4], and it is one of the main reasons for the efficiency droop that happens at high injection current [5]. In order to avoid this quantum confined Stark effect, researchers have been studying how to release the strain in the LED device. Therefore, they have designed a new LED structure called the nanopillar or nanorod. Figure 1-3 shows the cross sectional image of a nanopillar LED. The p-GaN, MQW, and n-GaN regions are divided into nanopillars, and the gaps of the nanopillars are filled by dielectric material to prevent electrical shorting.

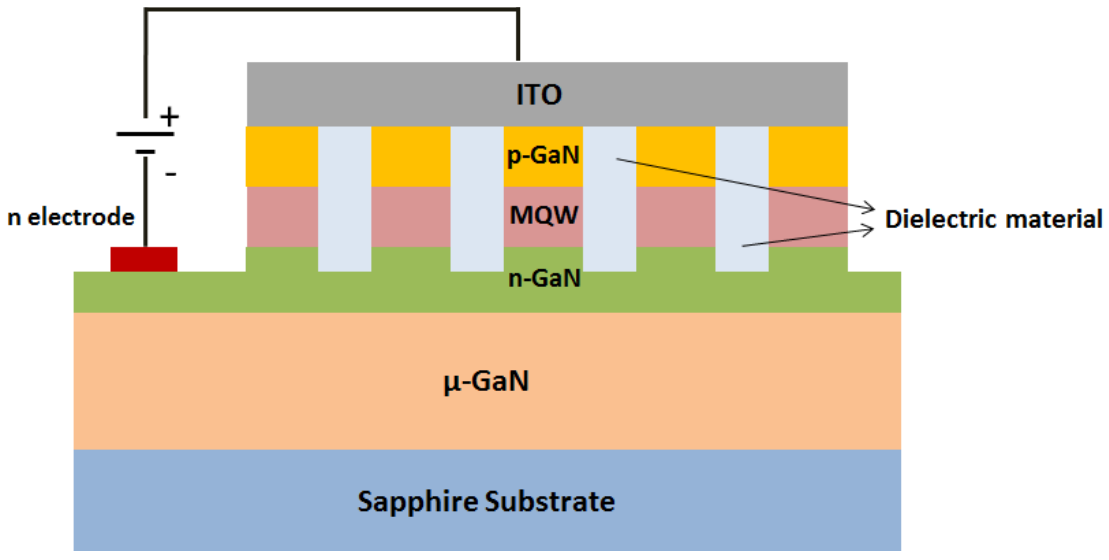


Figure **1-3** A cross sectional schematic of InGaN/GaN nanopillar LED.

The strain released by nanopillar formation enhances the internal quantum efficiency of the LED device [3]. In addition, increased surface areas act as pathways where generated photons escape, and the light extraction efficiency is enhanced. The improvement of internal quantum efficiency and extraction efficiency improves the device performance [6].

1.2 Photoluminescence comparison of planar and nanopillar LEDs

The light emission efficiency of planar and nanopillar LEDs can be compared using photoluminescence (PL) intensity. The active region of an ideal LED emits one photon for every electron injected, and the internal quantum efficiency is defined as

$$\eta_{\text{int}} = \frac{\text{number of photons emitted from active region per second}}{\text{number of electrons injected into LED per second}} = \frac{P_{\text{int}}/(h\nu)}{I/e}$$

P_{int} means the optical power emitted from the active region, h is Planck's constant, ν is frequency, I is the injection current, and e is elementary charge.

Photons generated in the active region have to escape from the LED die to the free space to emit light, and the light extraction efficiency and expressed by

$$\eta_{\text{extraction}} = \frac{\text{number of photons emitted into free space per second}}{\text{number of photons emitted from active region per second}} = \frac{P/(h\nu)}{P_{\text{int}}/(h\nu)}$$

P means the optical power emitted into free space, P_{int} is the optical power emitted from the active region, h is Planck's constant, ν is frequency.

The external quantum efficiency is defined by the ratio between photons emitted into free space and injected electrons and expressed by the below equation [1].

$$\eta_{\text{ext}} = \frac{\text{number of photons emitted into free space per second}}{\text{number of electrons injected into LED per second}} = \frac{P/(h\nu)}{I/e} = \eta_{\text{int}}\eta_{\text{extraction}}$$

P means the optical power emitted into free space, *h* is Planck's constant, ν is frequency, *I* is the injection current, and *e* is elementary charge.

A preliminary comparison of planar and nanopillar LEDs can be performed using the photoluminescence intensity, even though practical devices operate by electroluminescence. For photoluminescence,

$$I = A\eta_{\text{abs}}\eta_{\text{extraction}}\eta_{\text{int}} \text{ [7]}$$

Photoluminescence (PL) intensity (*I*) is determined by the light emitting area (*A*), the absorption efficiency of the pumping laser (η_{abs}), the light extraction efficiency ($\eta_{\text{extraction}}$), and the internal quantum efficiency of the quantum well structure (η_{int}). Light emitting area increases due to larger surface area by forming nanopillars compared to planar structures. Also, the absorption efficiency of the pumping laser and the light extraction efficiency increase because of the cylindrical shape and small diameter of the nanopillars [8]. As mentioned before, internal quantum efficiency improves due to strain release [3]. The above equation explains why nanopillar LED devices show the better performance than planar LEDs when comparing PL intensity. This reason is why nanopillar devices should be developed in the future work.

1.3 Literature review of nanopillar LEDs

In the nanopillar LED development, two different techniques have been studied by researchers: bottom up and top down techniques. Because of the difficuly to grow uniform nanopillars by bottom up techniques [6], [8] the top down nanopillar formation technique was chosen for this research. Figure 1-4 shows the general techniques forming nanopillar LEDs with dry etching [9].

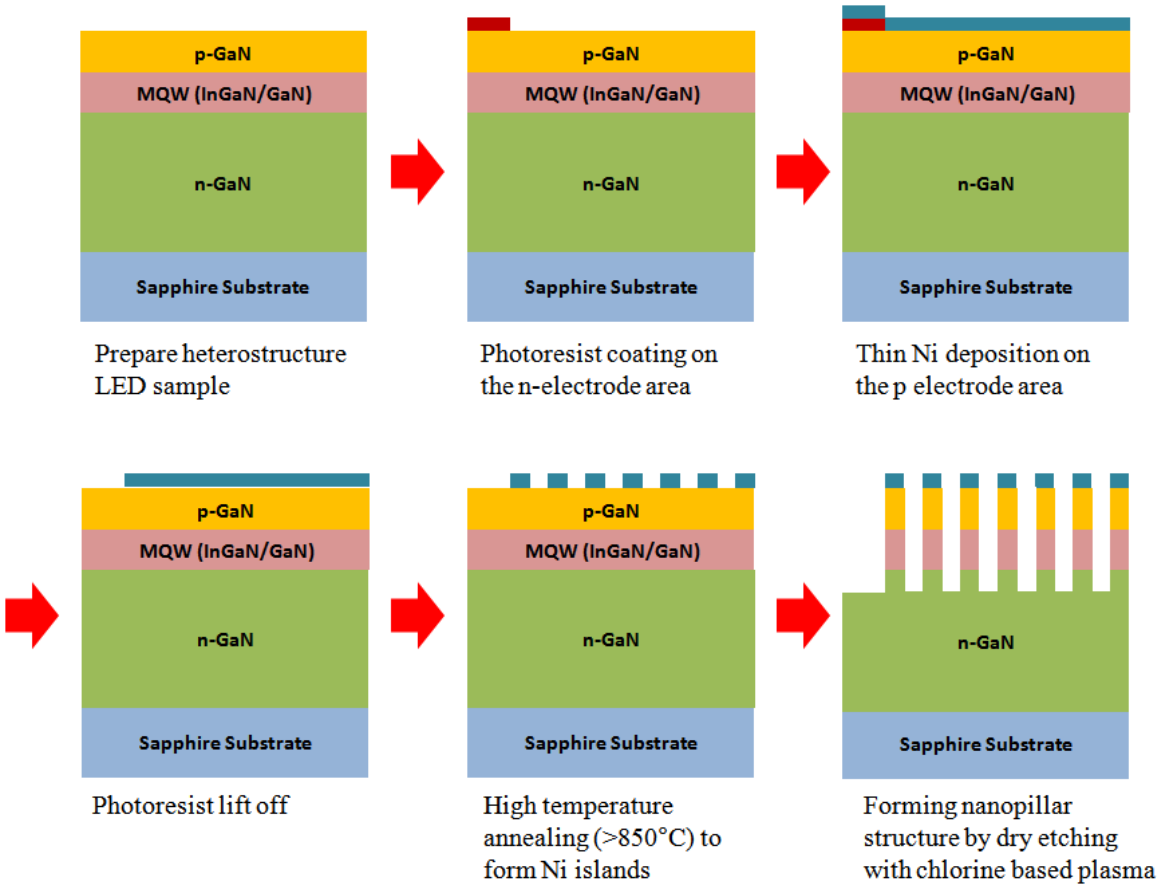


Figure **1-4** Top down nanopillar LED formation by dry etching adapted from [9].

1.4 Research objective

Top down nanopillar LEDs created by the dry etching technique face great challenges to be used for practical applications because of leakage current and non-radiative surface recombination which degrade internal quantum efficiency and device performance [10]. First of all, the leakage current occurs at damaged sidewalls created by dry etching [9], [10]. When MQW layers, the InGaN/GaN heterostructure, are etched by chlorine based plasma, N is preferentially etched over Ga due to the stronger binding energy of Ga-O over Ga-N. Generated nitrogen vacancies have shallow donor energy levels and enhance conduction. As a result, the generated nitrogen vacancies work as leakage current pathways and act like non radiative recombination centers [11]. In addition, GaO_x, InO_x created on the nanopillar sidewalls cause non-radiative surface recombination [12].

In this reasearch, passivation techniques to reduce the sidewall damage on the nanopillars were discussed. First of all, the passivation effect was confirmed comparing photoluminescense intensities on nanopillar and planar InGaN/GaN heterostructure samples. In addition, the nanopillar LEDs were fabricated with regard to other key process steps for transparent ohmic contact to p-GaN and oblique deposition as well as the results from passivation experiments. Then, electroluminescense and I-V (current-voltage) measurements were used for the device characterization. The research objective was to examine if the device efficiency could be increased by suppressing leakage current and enhancing internal quantum efficiency using the passivation techniques.

Chapter 2

Literature review

In this chapter, literature on the key process steps to determine device performance, such as nanopillar formation, passivation techniques to reduce the sidewall damage, methods for forming transparent ohmic contacts to p-GaN, and oblique deposition were reviewed. The experiments for each process set up would be conducted based on the literature review.

2.1 Nanopillar formation

In this study, the top down nanopillar formation technique by dry etching was chosen, and selecting the proper patterning techniques was required. Currently, e-beam lithography has been used for patterning uniform and high resolution nano-features, but its disadvantage for the commercial device fabrication is low throughput and high cost [13][14]. Alternatively, many research groups studied the various techniques to form self-assembled nanomasks, providing high throughput and low cost. The sorts of self-assembled nanomasks were classified into self assembled Ni clusters, silica nanoparticles, and ITO nanospheres.

First of all, the self-assembled Ni clusters were formed by the following procedures. On the InGaN/GaN heterostructure sample, a thick silicon dioxide (SiO_2) or silicon nitride (Si_3N_4) layer and a thin Ni layer were deposited by plasma-enhanced chemical vapor deposition (PECVD) and e-beam evaporation, consecutively. Then the sample was heated by rapid thermal annealing (RTA) under N_2 at 800-900℃ for 1 min to

form various nanometer sized Ni clusters. These Ni clusters and SiO_2 or Si_3N_4 layers were used as the first and second masks when LED nanopillars were formed by dry etching. The advantage of this technique was that the nanopillar dimension was controllable with varying the Ni layer thicknesses [13]. Second, a spin coated monolayer of silica nanoparticles was used as an etch mask. The monolayer of silica nanoparticles was coated by electrostatic force on the p-GaN surface, and the nanopillar dimension was determined by the diameters of the silica nanoparticles. The advantage of this technique is the availability to form uniform patterning [14]. Finally, indium tin oxide (ITO) nanospheres were used as an etch mask. ITO nanospheres were formed by wet etching an ITO layer with the very dilute hydrochloric acid (HCl) (3%). The mechanism is explained by the preferential wet etching of In_2O_3 at the grain boundaries and remaining nanodots of the In_2O_3 and SnO_2 mixture. The advantage of this technique is the availability to obtain high density nanospheres and nanopillars by dry etching [15]. Top view of nanopillar patterns created by those three different techniques was described in Figure 2-1.

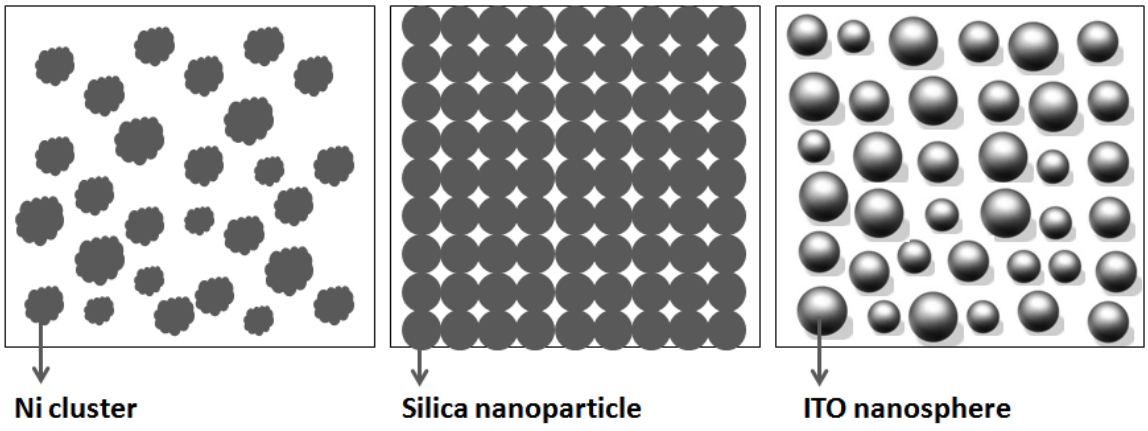


Figure **2-1** Three different self-assembled nanomasks adapted from [13], [14], and [15].

2.2 Techniques to reduce the sidewall damage

Research groups implemented various techniques to reduce the sidewall damage such as lowering InGaN/GaN MQW etch rate, wet chemical treatment, wet oxidation, nanopillar gapfilling with dielectric materials, and $(NH_4)_2S$ passivation. First of all, Yu et al. demonstrated PL intensity enhancement upon lowering etch rate and claimed that slower etch rate contributed to reducing the sidewall damage [16]. Also, wet chemical and oxidation were used for reducing the sidewall damage. Zhu et al. showed that the wet chemical treatments such as HCl, KOH, H_3PO_4 were effective and claimed HCl was the best chemical treatment by showing 14 times PL intensity enhancement compared to the planar structure [17]. However, neither Yu et al. nor Zhu et al. showed optical and electrical data from nanopillar LEDs because they obtained PL data from only nanopillars for their studies. Chiu et al. proved that the sidewall damage was recovered by using photo enhanced chemical (PEC) wet oxidation and showed the improvement with EL and I-V (current-voltage) data [18, 19]. The research groups studied Spin On Glass (SOG) [20-23], SiO_2 [24, 25], and SU-8 [14] for nanopillar gapfilling and demonstrated the effectiveness by showing the better performance of nanopillar LEDs rather than planar LEDs using the I-V, EL, and output power comparison. Finally, Yang et al. studied the $(NH_4)_2$ treatment, which was effective for recovering the sidewall damage. They explained that $(NH_4)_2$ removed the unstable native oxide which had surface states and formed a monolayer of sulfides. As a result, leakage current and nonradiative surface recombination decreased. They showed the recovery of the sidewall damage by I-V characteristics [26]. However, they did not present any EL data after the sulfur passivation.

2.3 Transparent ohmic contacts to p-GaN

Forming ohmic contacts to p-GaN on top of the nanopillar is a critical issue because poor ohmic contacts lead to a large voltage drop, which degrades device reliability and efficiency [27]. Achievement of ohmic contacts to p-GaN is very difficult because of the high activation energv (~170 meV) of the Mg dopant, which leads to a modest hole concentration ($<10^{18}$ cm^{-3}). In this section, various techniques for lowering the specific contact resistivity (SCR) between metals and p-GaN were introduced. In addition, transparent conductive oxide (TCO) contacts to p-GaN were described because high transmittance is another critical factor for the LED devices. There also have been lots of attempts to achieve high quality TCO contacts to p-GaN.

2.3.1 Approaches to achieve metal/p-GaN ohmic contact

Because of the importance of ohmic contact formation to p-GaN for optoelectronic devices, lots of techniques were introduced by various researchers. The techniques can be classified into three different groups: surface treatment, introducing high work function metals and annealing, and forming NiO interlayers.

A. Surface treatment

Native oxide is easily formed on the p-GaN surface because of strong bonds between O and Ga. The native oxide can act as a barrier interrupting hole transport between the metal and semiconductor. It may also play a role in Fermi level pinning, whereby the effect of the metal work function on the Schottky barrier height is reduced.

In order to remove the native oxide, various kinds of surface treatment techniques have been studied. Commonly used solutions were dilute HCl [28], buffered oxide etch (BOE) [29], dilute HF [30] and KOH [31]. Among these surface treatments, BOE treatment offered the best performance to achieve ohmic contacts to p-GaN, and long treatment times were more effective than short times. The research groups who used the BOE treatment techniques showed that the Fermi level on the surface of GaN shifted to the acceptor level near the valence band and lowered the barrier height. Then ohmic contacts were achieved by these surface treatments with high work function metals such as Pt and Pd or bilayers including these metals [29].

Some research groups claimed that the native oxide is not completely removed by a one-step surface treatment and is possibly formed again during deposition under vacuum in an open system. Therefore, two-step surface treatments were introduced by other researchers in order to prevent re-oxidation. The first step was to use buffered oxide etch (BOE). Then the sample was treated by $(NH_4)_2S$ for the second step. When GaN sample was dipped in $(NH_4)_2S$ solution, sulfide was formed on the GaN surface because of stronger Ga-S bonding than Ga-O bonding. The strong sulfide bonding lasts more than a few months and prevents native oxide formation [32].

Another effort to improve the ohmic contact by surface treatment was intentional change of the surface states. Lee et al. oxidized the p-GaN surface at 750 °C in air and then dipped the sample in $(NH_4)_2S$ solution for 30 min. As a result, they assumed that Ga vacancies were generated on the surface, and the Fermi level position was shifted towards the valence band [33]. Another effort was to utilize N_2 plasma to activate more Mg acceptors by removing nitrogen vacancies from Mg_{Ga}-V_N deep donors [34].

B. Introducing high work function metals and annealing

p-GaN has a very high work function close to 7.5 eV. Therefore, achieving high quality ohmic contact to p-GaN is difficult because the highest work function of a metal (Pt) is just 5.65 eV, and there also could be Fermi level pinning on the interface between metal and p-GaN. In order to overcome the barrier, various attempts were performed by researchers to form ohmic contacts by using high work function metal alloys and annealing, such as Pt/Ru ($2.2 \times 10^{-6}\ \Omega \cdot cm^2$) [35], Pt/Pd/Au ($3.1 \times 10^{-5}\ \Omega \cdot cm^2$) [36], Pd/Ir/Au ($2 \times 10^{-5}\ \Omega \cdot cm^2$) [37], Ti/Pt/Au ($4.2 \times 10^{-5}\ \Omega \cdot cm^2$) [38], Pd/Ni/Au ($2.4 \times 10^{-5}\ \Omega \cdot cm^2$) [39], Pd/Ru ($2.4 \times 10^{-5}\ \Omega \cdot cm^2$) [40], Pd/Re ($8.7 \times 10^{-4}\ \Omega \cdot cm^2$) [41], and Pt/Ni/Au ($5.1 \times 10^{-4}\ \Omega \cdot cm^2$) [42]. All of these contacts were annealed at the temperatures between 350 °C to 700 °C in N_2 ambient. The main concepts to utilize the high work function of metals and annealing are as follows. When the high work function of metals such as Pd and Pt are deposited on the p GaN and are annealed, Ga outdiffuses from the p-GaN surface, and interfacial phases such as Pd and Pt gallides are formed. As the result, Ga vacancies are generated on the p-GaN surface and lead to reduction of SCR. The high work function of the Pd and Pt-rich alloys also presumably result in a reduced barrier height [35].

C. Forming NiO interlayer

The Ni/Au contact annealed in air ambient was tested by many research groups, and the range of low SCRs from 10^{-4} to $10^{-6}\ \Omega \cdot cm^2$ were produced [43]-[51]. The main mechanism why Ni/Au alloy produces low SCR is as follows. When the p-GaN/Ni/Au

contacted sample is annealed in air, Ni outdiffuses to the surface through Au, while Au indiffuses to p-GaN because this sample is annealed in air, and Ni forms NiO at the surface. According to Ho's model, NiO is a p-type semiconductor, which enhances the hole concentration while high work function Au islands are formed on the p-GaN interface. There is a hole notch at the heterojunction because of the band offset between p-NiO and p-GaN, and hole flows through this hole notch. Also, a very low Schottky barrier of 0.2 eV is formed between Au (5.1 eV) and p-NiO (4.9 eV). This unique structure yields the low SCR [43].

One research group built different metal alloy layers including Ni to form ohmic contacts. Song et al. used Ni-Mg solid solution/Au and Zn-Ni solid solution/Au contacts and produced the low SCRs of 3.0×10^{-5} and $5.2 \times 10^{-5}\ \Omega \cdot cm^2$ [52], [53]. Both samples were annealed at ~550 °C for 1 min in air. Other groups formed Ni–Co/Au [54], Ni/Cu [55], Ni/Pd/Au [56], and Ni/Au–Zn [57] contacts by annealing in air. The range of contact resistivity obtained was 10^{-5}–$10^{-6}\ \Omega \cdot cm^2$.

2.3.2 Tranparent Ohmic contacts to p-GaN

Transparent ohmic contacts are very important for the optoelectronic devices such as LEDs, photodetectors, and laser diodes in order to enhance light emission efficiency. Recently, semi transparent thin Ni/Au electrodes have been used commercially. However, these metal-based semi transparent materials have some drawbacks such as low refractive index, bad current spreading and thermal instability [58]. In order to overcome these drawbacks, the studies of ohmic contacts between transparent conductive oxides and p-GaN have been performed.

Indium tin oxside (ITO) is a kind of transparent conductive oxide (TCO) that is a good current spreading layer and has high transparency of over 90 % in the visible spectrum and low electrical resistivity less than 5×10^{-4} Ω·cm. Due to its good electrical and optical properties, there have been lots of efforts to form ITO contacts to p-GaN [59]. However, ohmic contact formation between ITO and p-GaN is difficult due to ITO's low work function (4.7 eV) [60]. Therefore, the techniques inserting various ultra thin layers such as InGaN, Ag, Ni-based alloys, Cu doped Indium Oxide (CIO), and Sn-Ag alloys between ITO and p-GaN and then annealing in air at high temperature were introduced by research groups to achieve a high quality ITO ohmic contact to p-GaN.

First of all, InGaN was used for a strained layer. The SBH of the p-GaN/$In_{0.15}Ga_{0.85}N$/ITO contact was calculated to be 2.3 eV, while the SBH of the ITO/GaN contact was 2.7 eV. The use of strained InGaN reduced the SBH by 0.4 eV. Also, the polarization effect of InGaN increased the hole concentration and enhanced the hole tunneling current. After annealing at 550 °C for 1 min, the specific contact resistivity of 3.2×10^{-5} Ω·cm^2 was obtained [61].

Song et al. used 1nm of Ag between ITO and p GaN, and then they annealed the sample at 500°C for 1 min in an air. As a result, they obtained the SCR of 1.17×10^{-4} Ω·cm^2 and transparency of 96%. The reduction of SBH is explained by two causes. First, a Ag-Ga solid solution was formed and produced the acceptor-like Ga vacancies on the GaN surface, and it increased the carrier concentration and reduced band bending. Second, the inhomogeneous Schottky barriers were formed due to Ag nanodots by

breaking up the ultra thin Ag layer, and the electric field distribution at the metal semiconductor interface lowered the barrier height [62].

Many other research groups introduced thin Ni based layers or solid solutions between ITO and p-GaN to obtain low SCR. Hong et al. formed Ni (10 nm)/ITO (250 nm) contacts and annealed them at 500 °C in air and obtained the SCR of 8.6×10^{-4} Ω·cm^2. The main mechanism was explained by forming the NiO layer between p-GaN and ITO [63]. Chae et al. formed p-GaN/ZnNi solid solution (5 nm)/ITO and annealed it at 500 °C for 1 min in an O_2, and the SCR of 1.27×10^{-4} Ω·cm^2 and transmission of ~90 % was obtained [64]. Other researchers formed Ni bilayer contacts such as Ni(2 nm)/ Au(3 nm)/ ITO(60 nm) [65] and Ru(5 nm)/Ni(5 nm)/ITO(60 nm) [66], and then they annealed the samples at ~500 °C for 1 min in air or O_2. They both yielded SCR of 2.0×10^{-4} Ω·cm^2 with transmittances of 90 % and 92 %. Also, Cu-doped indium (CIO) (3 nm) [67], Sn-Ag alloy (6 nm) [68] and ITO contacts were formed and annealed at 530 °C - 630 °C for 1 min in air. These contacts produced the SCRs of 1.56×10^{-4} Ω·cm^2 and 4.72×10^{-4} Ω·cm^2 with high transmittance.

2.4 Oblique deposition on top of the nanopillars

In most practical nanopillar LEDs, SOG, SiO_2, and polymers are used as the gapfilling materials to reduce the sidewall damage from dry etching. However, the gapfilling techniques have some drawbacks. First, controlling thickness and uniformity of the dielectric material is very difficult. Incomplete gap filling of the dielectric materials causes the localized current injection and creates leakage current paths. Second, the

additional coating process increases the fabrication cost as well as reduces production yield. Therefore, Lee et al. introduced oblique ITO deposition techniques to overcome the drawbacks and create direct and selective contact on the top of nanopillars.

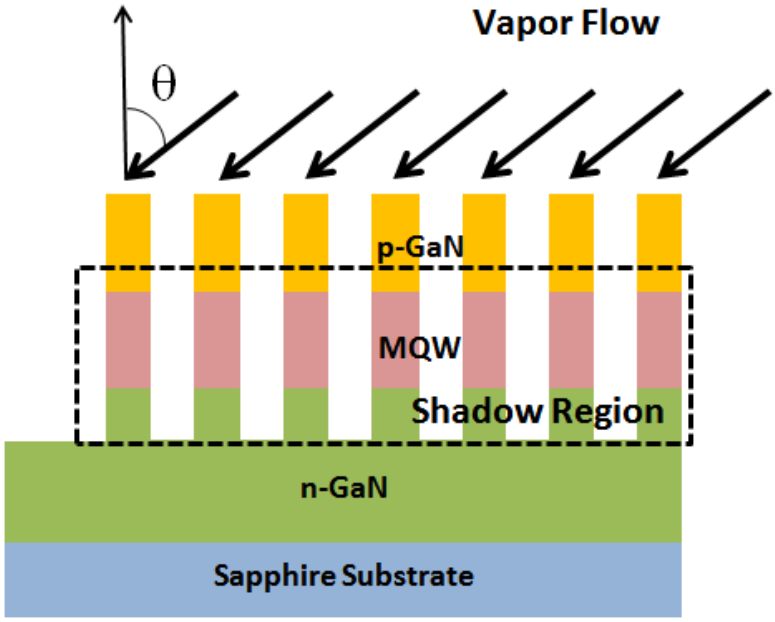


Figure **2-2** A schematic of incident vapor flow selectively growing on the top of the nanopillars adapted from [69].

Figure 2-2 shows slanted ITO grown on the top of nanopillars by oblique angle deposition using e-beam evaporation. For the oblique angle deposition, the sample stage was on the substrate which has a certain tilt angle with respect to the vapor flow direction. Since e-beam evaporation is directional, the ITO was deposited only on the tops of nanopillars due to a "shadowing effect", and LEDs avoided the electrical short. Then, a successive blanket ITO layer was deposited on the slanted ITO layers and creates a continuous surface morphology to improve the film quality. As a result, the electrical current from the p-electrode is spread out to isolated nanopillars [69].

Chapter 3

Experimental procedures

In this chapter, experimental procedures for key process steps such as nanopillar formation, passivation techniques to reduce the sidewall damage, methods for forming transparent ohmic contacts to p-GaN, and oblique deposition were introduced. Also, tools for the process and characterization were presented.

3.1 Nanopillar formation

For the nanopillar patterning, three different self-assembled masks: Ni clusters, silica nanoparticles and ITO nanospheres, have been introduced by various research groups. In this study, the self-assembled mask which has the highest density and yield with 100 nm average diameter was required. The density of self-assembled Ni clusters is lower than that of silica nanoparticles and ITO nanospheres. Even though the densities of the silica nanoparticles and ITO nanospheres are comparable, forming silica nanoparticles with high yield is difficult to implement because serious yield degradation is expected when they are unsuccessfully coated. Therefore, ITO nanospheres were chosen as the proper self-assembled mask because they satisfied all of the requirements such as high density and yield with average 100 nm diameter. Figure 3-1 presents the schematic of process flow for forming nanopillars by dry etching with ITO nanospheres.

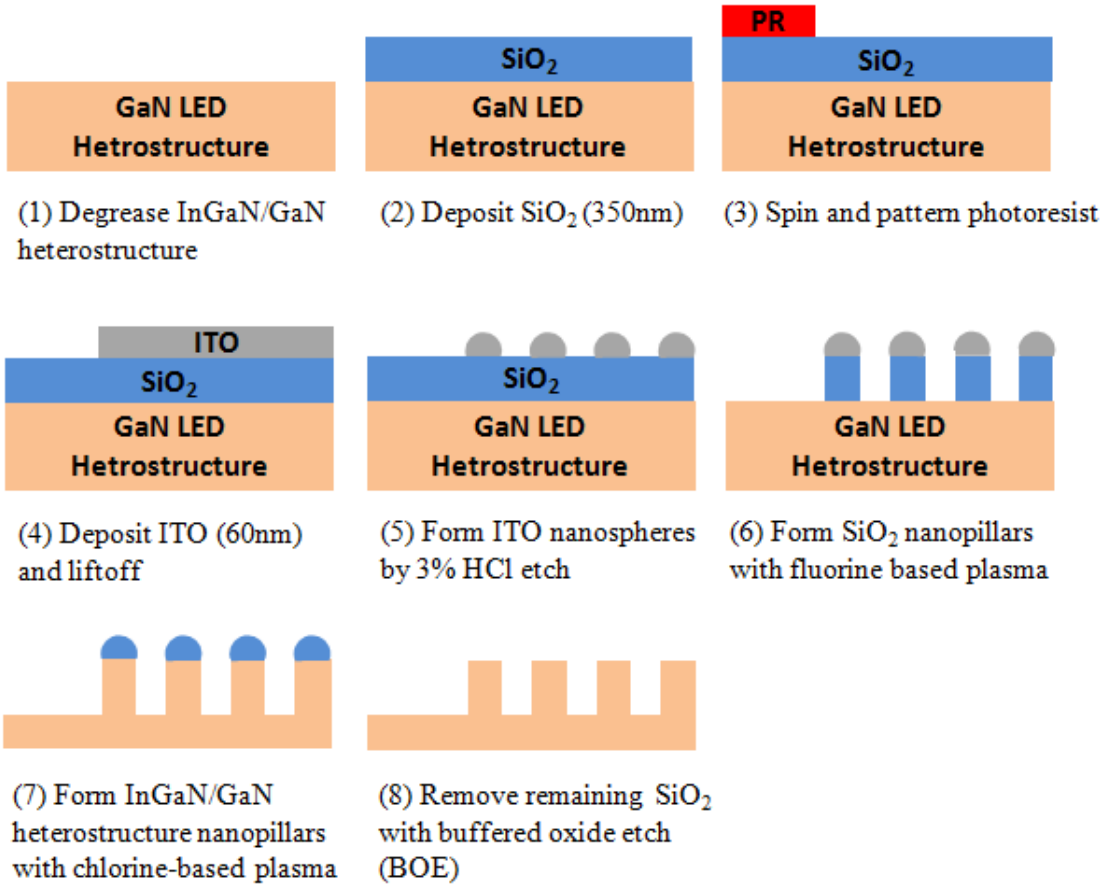


Figure **3-1** A schematic of the process flow for forming nanopillars with ITO nanospheres.

(1) First, InGaN/GaN heterostructure samples are degreased using acetone and isopropanol for 5 min each. Then, they are rinsed in de-ionized (DI) water and dried with a N_2 gun.

(2) The 350 nm SiO_2 layer is deposited on the degreased samples by Plasma Enhanced Chemical Vapor Deposition (PECVD).

(3) Photoresist is coated over the n-electrode region on the SiO_2 layer.

(4) The 60nm Indium Tin Oxide (ITO) layer is deposited by e-beam evaporation, and then the ITO layer over the photoresist is lifted off.

(5) The deposited ITO layer over the p-electrode region is chemically etched with 3 % HCl for 30 s. Then, the ITO nanospheres with the average diameter of 100 nm are self-assembled.

(6) SiO_2 nanopillars are formed beneath the self-assembled ITO nanospheres using a fluorine-based plasma.

(7) Consecutively, InGaN/GaN heterostructure nanopillars are formed beneath the SiO_2 nanopillars using chlorine based plasma.

(8) The remaining SiO_2 nanopillars are removed by the 10 min 1:10 Buffered Oxide Etch (BOE) treatment.

The nanopillars are formed by two step etching processes with fluorine based dry etching and chlorine based dry etching using ITO nanospheres as the mask.

First, SiO_2 nanopillars were formed by fluorine based dry etching beneath ITO nanospheres. In this study, two types of fluorine gases of CF_4 and CHF_3 were used, and the recipes varying the ratios of CF_4 to CHF_3 were tested in order to confirm if the etching selectivity against ITO nanospheres were changed. Higher density SiO_2 nanopillars were expected to be formed with the higher selectivity against ITO nanospheres. Also, the higher density SiO_2 nanopillars were expected to generate the higher density InGaN/GaN nanopillars.

For the next step, InGaN/GaN heterostructure nanopillars were formed by chlorine based dry etching beneath SiO_2 nanopillars.

$$BCl_3+e \rightarrow BCl_2+Cl+e$$

$$BCl_2+Cl_2 \rightarrow BCl_3+Cl \quad [70]$$

The above reactions show how the chlorine based plasma is dissociated from Cl_2 and BCl_3. BCl_2 dissociated from BCl_3 acts as the passivation source while Cl plasma etches the sidewalls [70]. Therefore, the nanopillar profile can be varied by adjusting the ratio of Cl_2 to BCl_3. In this study, the recipes with various ratios of Cl_2 to BCl_3 were tested in order to find the recipe forming the vertical profiles.

3.2 Techniques to reduce the sidewall damage

In the previous chapter, various techniques to reduce the sidewall damage were reviewed: lowering InGaN/GaN MQW etch rate, wet chemical treatment, wet oxidation, nanopillar gapfilling with dielectric materials, and $(NH_4)_2S$ passivation. The gapfilling technique has some problems such as localized current injection by incomplete gap filling and enhancing the fabrication cost as well as reducing production yield [69]. Also, using tools required for wet oxidation was not available. Therefore, the technique combining different methods of lowering InGaN/GaN MQW etch rate and consecutive wet etching and $(NH_4)_2S$ passivation was chosen in order to maximize the effect for the reduction of sidewall damage.

Zhu et al. [24] claimed that HCl, KOH and H_3SO_4 were effective for reducing the sidewall damage. In this study, KOH was chosen for the wet chemical treatment because the chemical reaction was more established by other researchers. The reason why the

KOH treatment is effective for reducing the sidewall damage is explained as follows. The Ga rich surface formed on the nanopillar sidewalls after the dry etching acts as the leakage current path, as shown in Figure 3-2 [11]. When the dry etched nanopillars are treated by KOH solution, KOH selectively etches the extra Ga on the nanopillar sidewalls by the following reaction.

$$GaN + OH^- + 3H_2O \rightarrow Ga(OH)_4^- + NH_3 \text{ [71]}$$

$Ga(OH)_4^-$ is soft and soluble in water. As a result, the ratio of Ga to N on the sidewalls becomes well balanced, and the leakage current paths are diminished.

For the $(NH_4)_2S$ passivation, the mechanism is explained by the following reaction.

$$2NH_4^+ + S^{2-} \leftrightarrow NH_3 + NH_4^+ + HS^- \leftrightarrow 2NH_3 + H_2S \quad (1)$$

$$GaAs + H_2S \leftrightarrow Ga_{x'}S_{y'} + As_{x''}S_{y''} + RO^- + H_2\uparrow \quad (2) \text{ [72]}$$

When the $(NH_4)_2S$ is mixed with the solvent which has lower dielctric constant, the equilibrium is more shifted to the right in equation (1). Then, the sulfur formation happens with the GaAs by the reaction (2) [72]. Bessolov et al. claimed that the harder covalent bonding between the III-V semiconductor and S was formed after the passivation in the solution of $(NH_4)_2S$/ solvent with a lower dielectric constant than in the usual aqueous sulfide solutions [73]. Because MQW in LED hetero-structure consists of InGaN/GaN multiayers, $Ga_{x'}S_{y'}$ and $In_{x''}S_{y''}$ are expected to be created by $(NH_4)_2S$ treatment. In this study, $(NH_4)_2S$/isopropanol (ISP) (dielectric constant of 18.23) solution was used to remove the native oxide and form the strong sulfide bonding on the InGaN/GaN sidewall surface and then prevents the re-oxidation.

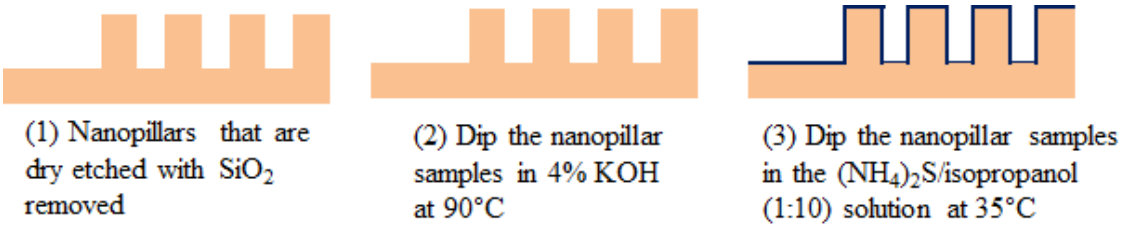


Figure **3-2** The process flows with the two step passivation treatments.

(1) Prepare the nanopillars with dry etching and SiO_2 removed.

(2) Dip the nanopillar samples into the KOH at 90˚C.

(3) Dip the nanopillar samples into the 20-24 % $(NH_4)_2S$/isopropanol (1:10) solution at 35˚C.

Figure 3-2 shows the process flows of the two step passivation technique, and the processes were implemented at 90℃ and 35℃ each for the better reaction.

Photoluminescence

Photoluminescence is the non-destructive technique used for characterizing the passivation effect on the III–V semiconductors.

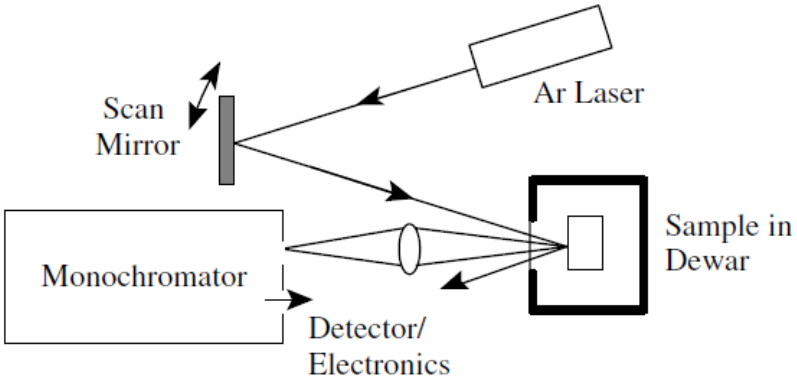


Figure **3-3** A schemetic of photoluminescence arrangement [74].

Figure 3-3 shows the schematic photoluminescence arrangement. The sample is excited with optical sources such as lasers with energy hv > Eg, and the detector detects the emitted light generated by the radiatively recombined electron-hole pairs. Then the spectrograph shows the photoluminescence intensity as a function of wavelength [74].

$$I = A\eta_{\text{abs}}\eta_{\text{extraction}}\eta_{\text{int}} \text{ [7]}$$

Photoluminescense (PL) intensity (I) is determined by the light emitting area (A), the absorption efficiency of the pumping laser (η_{abs}), the light extraction efficiency ($\eta_{\text{extraction}}$), and the internal quantum efficiency of the quantum well structure (η_{int}).

In this study, the light emitting area, the absorption efficiency of the pumping laser and the light extraction efficiency are expected to be comparable because the nanopillars used for the passivation treatments have almost the same structures. Therefore, PL intensity difference represents the internal quantum efficiency difference. The surface recombination originating defects causes the non-radiative recombination rather than radiative recombination and emits heat instead of the light [74]. Because the internal quantum efficiency can be evaluated by the ratio between the radiative recombination and non-radiative recombination, depending on the defect states on the sidewalls, the passivation effects can be confirmed by the PL intensity comparison.

3.3 Transparent ohmic contacts to p-GaN

When the nanopillars are treated by the two step passivation technique of KOH and $(NH_4)_2S$, the top of p-GaN is also treated by the chemicals simultaneously. Therefore, it is necessary to confirm the effect of the two step passivation technique on the surface

of p-GaN. From the literature review, Lee et al. reported that KOH is effective for improving the contact to p-GaN because KOH removes the native oxide on the p-GaN and lowers the Schottky barrier height [75]. Jang et al. reported that sulfide treatment improves the contact because of the sulfide replacing the native oxide [32]. Also, the literature that demonstrated the annealing effect in the ITO contact to p-GaN was reviewed to design the appropriate experimental plans for this study. Su et al. claimed that high transparency and low specific contact resistivity were obtained when the ITO deposited on the p-GaN is annealed at 600℃ under N_2 for 10 min [76].

In this study, two kinds of experiments were performed. The first experiment is testing whether the combination of the two step chemical treatments and high temperature N_2 annealing is effective for improving the ITO contact to p-GaN. The second experiment is to confirm if the ITO contact to p-GaN contact improves by inserting high work function metals such as Pd, Ni and Pt between ITO and p-GaN. The experimental procedures follow the below process steps.

(1) 5 mm by 5 mm sized p-GaN samples are degreased by acetone then isopropanol for 5min each. Then, they are rinsed by de-ionized (DI) water and dried by nitrogen gun.

(2) Dip the samples into 1:10 BOE solution in order to remove the native oxide on the sample surface, rinse them in DI water and dry in N_2. Then dip the samples into 0.4% KOH solution at 35 ℃ for 90 s and 20-24 % $(NH_4)_2S$/ISP 1:10 solution at 35 ℃ for 20 s.

(3) Circular transmission line model (C-TLM) test structures are patterned on the p-GaN by the following process steps.

a. Dehydrate at 200 °C for 5 min.

b. Spin coat the sample with SF11 at 3000 rpm for 45 s. (D09/30/45)

c. Softbake the sample at 170 °C for 5 min.

d. Spin coat the sample with SPR3012 at 4000 rpm for 45 s. (D09/40/45)

e. Softbake the sample at 95 °C for 1 min.

f. Expose the patterned sample at 8 mW/cm^2 for 7.6 s using MABA6

g. Develop the sample in CD 26 for 2 min and inspect the sample under microscope

(4) Expose the patterned sample in the UV ozone system to remove the carbon contamination on the surface of p-GaN.

(5) Load the patterned samples in the e-beam evaporation system (Edwards), and wait until the chamber pressure is lowered below 10^{-7} Torr.

(6) Deposit ITO or other thin metals.

(7) Soak the ITO or metal deposited samples into the PG remover at 85 °C with 800 rpm spinning speed. The samples are rinsed in isopropanol and water and dried.

(8) The current versus voltage (I-V) characteristics are measured using four probes and a Keithley 236 source measurement unit.

Circular transmission line model

The quality of contact is determined by the specific contact resistivity comparison. In this study, the circular transmission line model is used to calculate ρ_C. Figure 3-4 shows the CTLM patterns and the measurements.

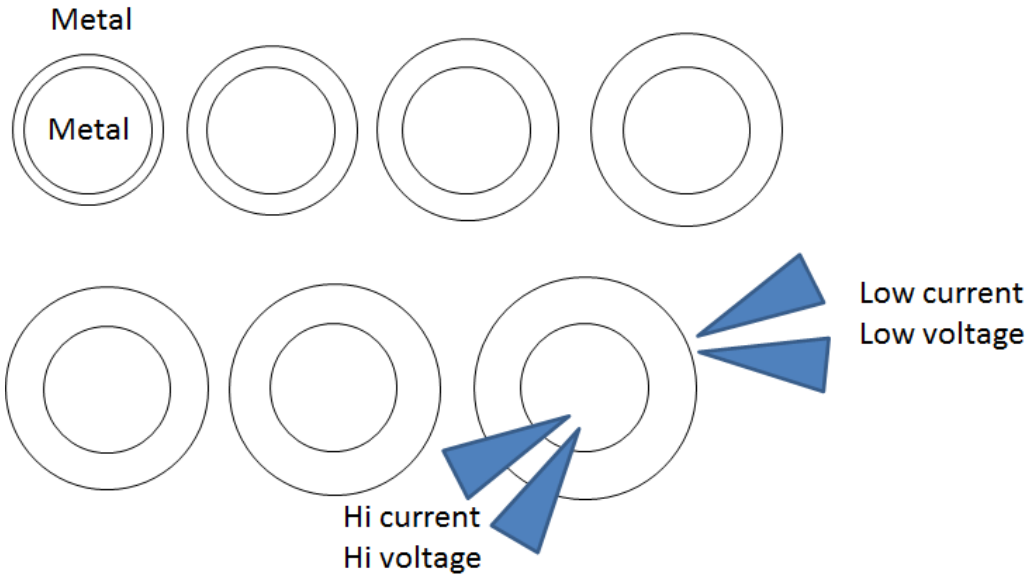


Figure **3-4** CTLM patterns and the I-V characterization technique.

For the I-V characterization, the 7 CTLM patterns which have the same 40 μm inner radius and different outer radiuses from 42 μm to 54 μm with 2 μm gap difference. Two high current and voltage tips are touched on the inner metal area, and the other two low current and voltage probe tips are touched on the outer metal area. Then a current sweep is performed and the voltage is measured. For the better reliability of the measurements, at least three different sets are measured.

According to Marlow and Das [77], the voltage drop across the gap of d at the applied current is:

$$\Delta V = \frac{i_0 R_s}{2\pi}\left[\ln\left(\frac{r_1}{r_0}\right) + \frac{L_T}{r_0}\frac{I_0(r_0/L_T)}{I_1(r_0/L_T)} + \frac{L_T K_0(R_1/L_T)}{r_1 K_1(r_1/L_T)}\right]$$

R_s: The sheet resistance of semiconductor

i_0: Applied current

L_T: Transfer length

r_0: The radius of the circular inner region

r_1: The radius of the circular outer region

I_0: The modified Bessel function of the first kind of order zero

I_1: The modified Bessel function of the first kind of order one

K_0: The modified Bessel function of the second kind of order zero

K_1: The modified Bessel function of the second kind of order one,

From above equation, a non-linear curve is obtained from the graph of total resistance as a function of gap spacing. Then, the method of least squares to fit the non-linear curve is utilized to estimate the accurate R_s and L_T using a series expansion of the Bessel functions. Also, ρ_c and R_s are calculated by the following equations.

$$L_T = \sqrt{\frac{\rho_C}{R_S}}; \qquad R_C = \frac{\rho_C}{L_T}$$

For the ITO contact to p-GaN, it is hard to obtain the linear I-V curves because the specific contact resistivity is not low enough. Therefore, all of the R_T data calculated from the voltage at the current of 1 mA.

3.4 Oblique deposition on the top of the nanopillars

Because the gaps of the nanopillars are not filled by the passivation technique, general blanket ITO deposition is not available in this study. Therefore, the oblique ITO deposition technique was chosen in order to avoid the electrical short occurring from depositing ITO on the n-GaN region. For the oblique deposition, the e-beam evaporation tool called Axxis was used.

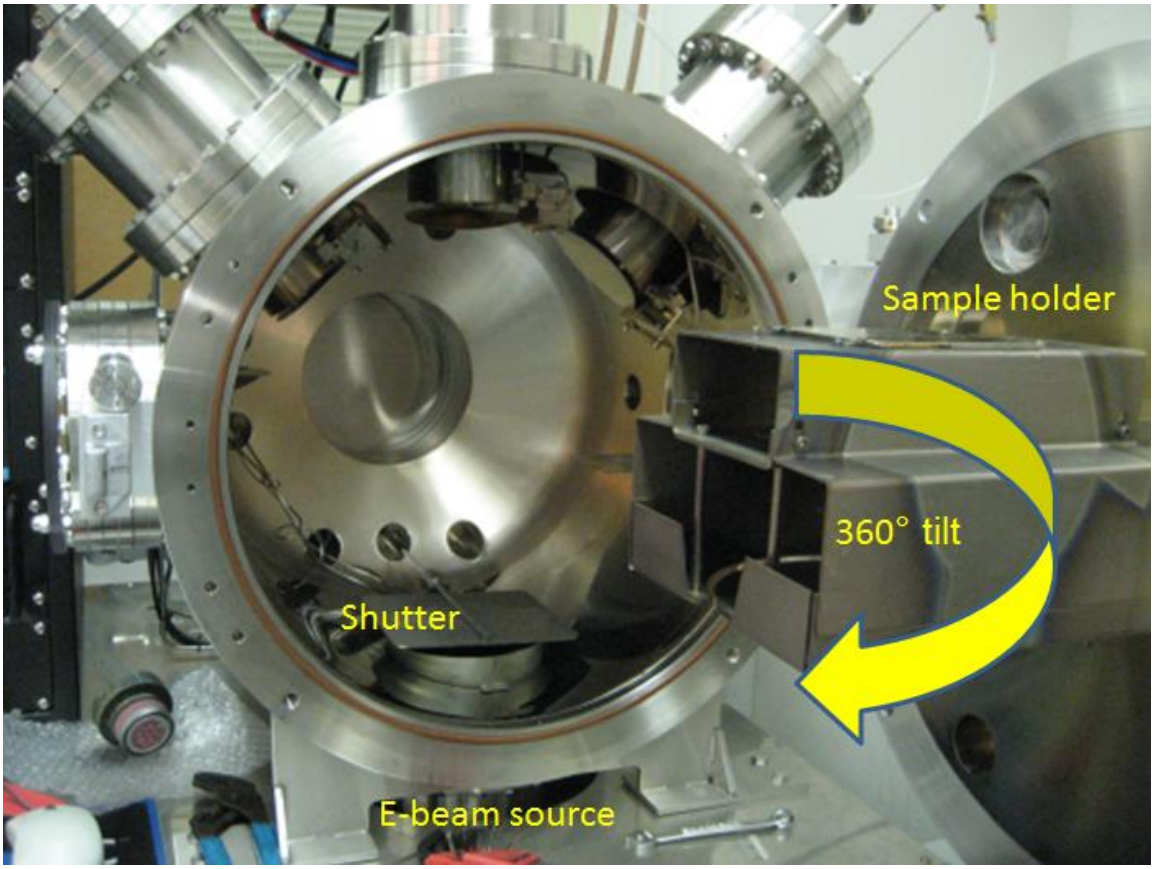


Figure **3-5** Inside the Axxis system.

In the Axxis system, the sample holder is tilted up to 360°. Therefore, the ITO can be deposited at any angle. Figure 3-5 shows the inside the Axxis system.

Chapter 4

Experimental results

In this chapter, experimental results of key process steps such as nanopillar formation, passivation techniques to reduce the sidewall damage, methods for forming transparent ohmic contacts to p-GaN, and oblique deposition are presented. The best exprerimental results from the each process step will be reflected in the nanopillar LED device fabrication.

4.1 Nanopillar formation

The nanopillars were formed by three successive process steps: ITO nanosphere formation by HCl wet etching, and SiO_2 and InGaN/GaN two step dry etching. Figure 4-1 shows the FESEM image of ITO nanospheres formed by 3 % HCl treatment for 30 s.

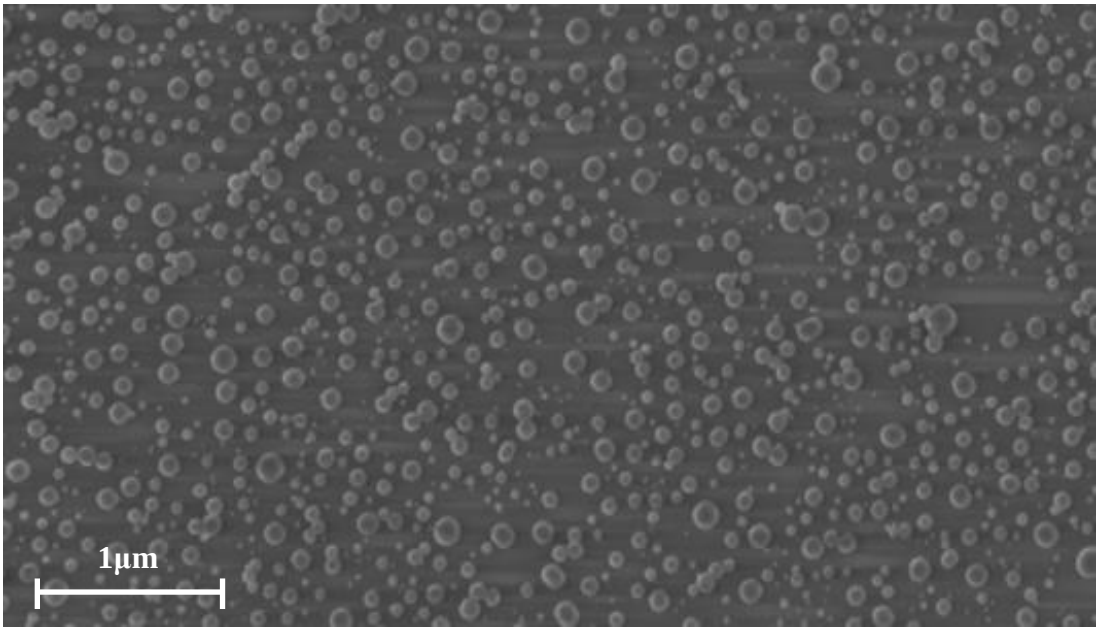


Figure **4-1** The FESEM image of ITO nanospheres.

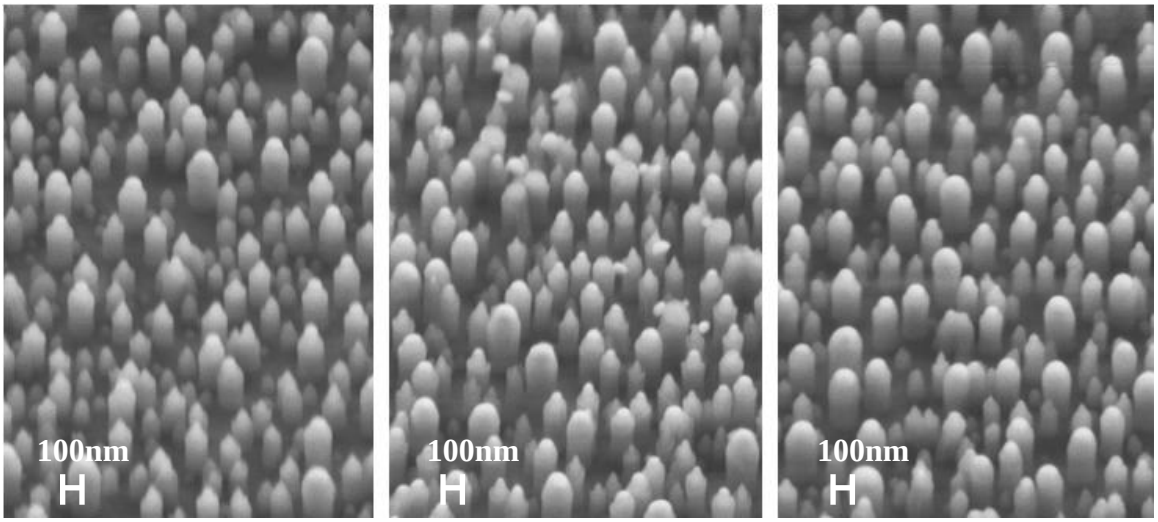


Figure **4-2** The FESEM images of SiO_2 nanopillars formed using various recipes with different CF_4/CHF_3 ratios (from left to right: 50 sccm; 35 sccm/15 sccm; 30 sccm/20 sccm).

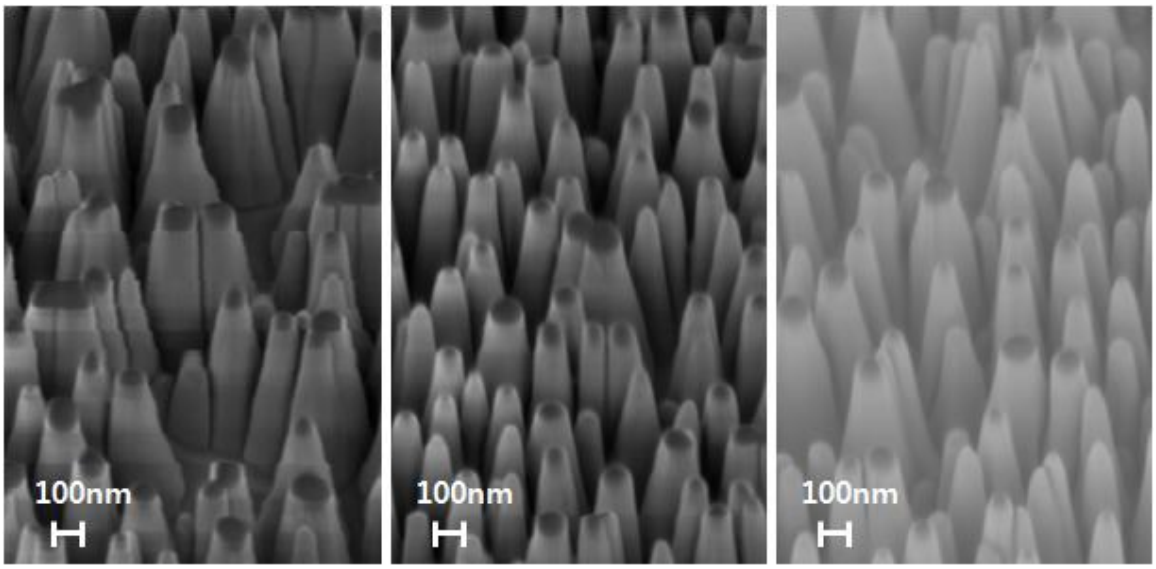


Figure **4-3** The FESEM images of InGaN/GaN nanopillars formed using various recipes with different Cl_2/BCl_3 ratios (from left to right: 19 sccm/14 sccm; 21 sccm/12 sccm; 23 sccm/10 sccm).

SiO_2 nanopillar profile was altered when the ratios of CF_4 to CHF_3 were varied while other variables were kept constant (pressure: 5 mTorr, ICP power: 700 W, RIE power: 150 W, time: 127 s) as shown in Figure 4-2. Also, the InGaN/GaN nanopillar profile was altered when the ratios of Cl_2 to BCl_3 were varied while other variables were kept constant (Ar: 20 sccm, pressure: 10 mTorr, ICP power: 500 W, RIE power: 200 W, time: 200 s) as shown in Figure 4-3. The most vertical and highest density InGaN/GaN nanopillars were created by the two step dry etching using the recipes including CF_4/CHF_3 (35 sccm/15 sccm) and Cl_2/BCl_3 (21 sccm/12 sccm), and they were used for the passivation tests.

4.2 Techniques to reduce the sidewall damage

In this section, the PL intensities were compared with different InGaN/GaN nanopillar etch rates and treatment techniques.

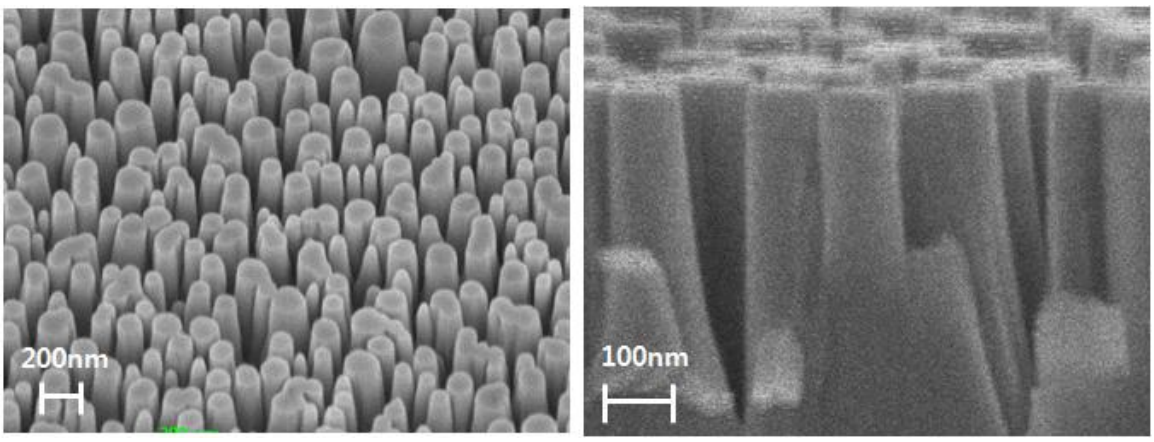


Figure 4-4 The FESEM images of InGaN/GaN nanopillars created using the dry etching recipes including CF_4/CHF_3 (35 sccm/15 sccm) and Cl_2/BCl_3 (21 sccm/12 sccm) at InGaN/GaN etch rate of 3.5 nm/s (left: 30° tilted view, right: cross-sectional view).

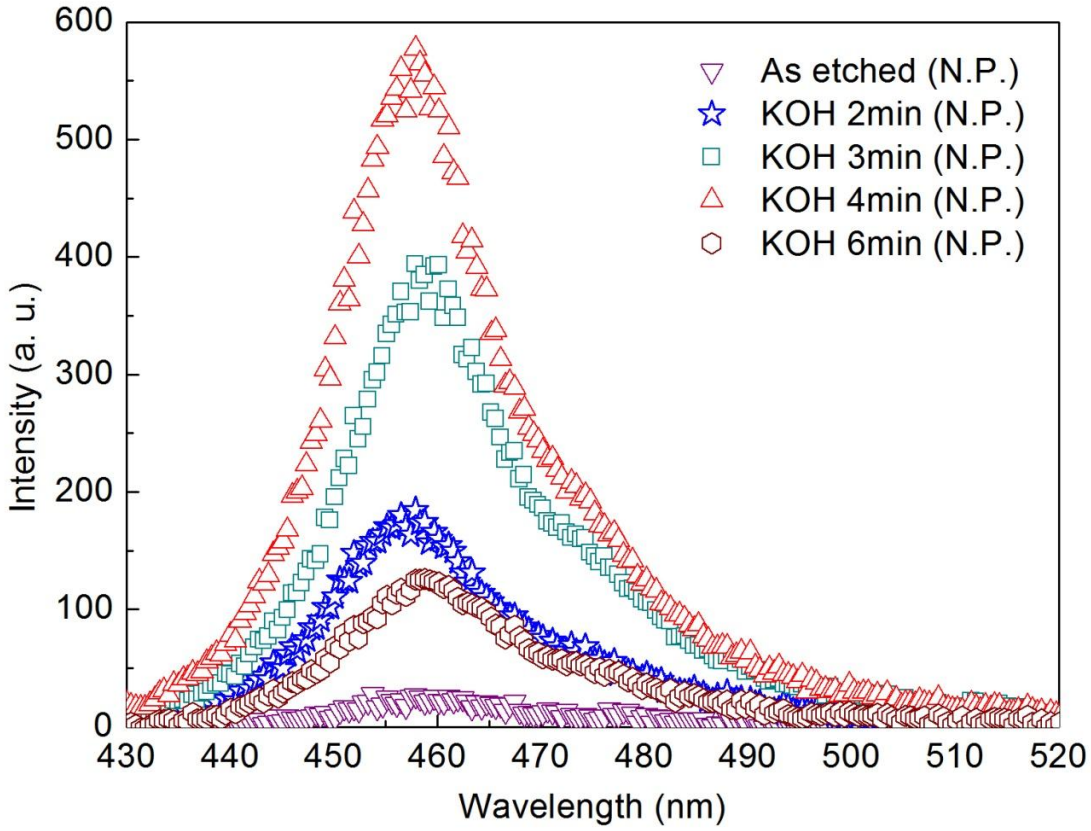


Figure **4-5** PL spectra of nanopillars created at 3.5 nm/s etch rate and then treated in 4% KOH solutions at various times.

Figure 4-4 shows the FESEM images of InGaN/GaN nanopillars created at InGaN/GaN etch rate of 3.5 nm/s. For the passivation test, these nanopillars were treated by 4 % KOH solutions at 90℃ for different times. The PL characterization results are shown in Figure 4-5, and the best results were obtained from 4 % KOH treatment for 4 min. These experimental results demonstrate that the high concentration requires shorter treatment time, and PL intensity increases up to a saturation time and decreases over the saturation time.

For the next experiment, the nanopillar samples were treated by the two step passivation technique of 4 % KOH and $(NH_4)_2S$/ISP=1:10.

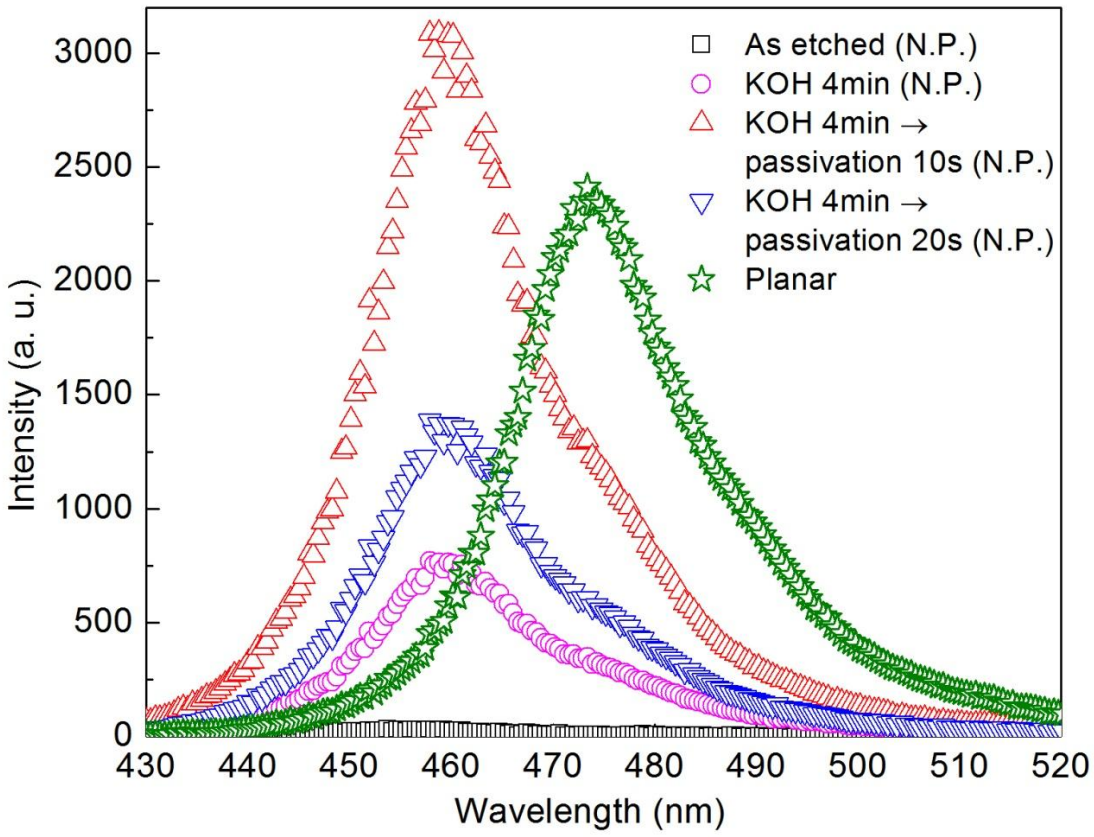


Figure **4-6** PL spectra of the InGaN/GaN nanopillars created with the 3.5 nm/s etch rate followed by the two step 4 % KOH and $(NH_4)_2S$/ISP=1:10 treatments at various times.

When the nanopillar samples were treated with 4 % KOH for 4 min and a $(NH_4)_2S$/ISP=1:10 solution for 10 s, consecutively, the best result of 1.3 times higher PL intensity than the planar structure was obtained as shown in Figure 4-6. In addition, a blue shift occurred in the as etched nanopillars compared to the planar structure, and it represents the reduction of the QCSE induced by the strain relaxation.

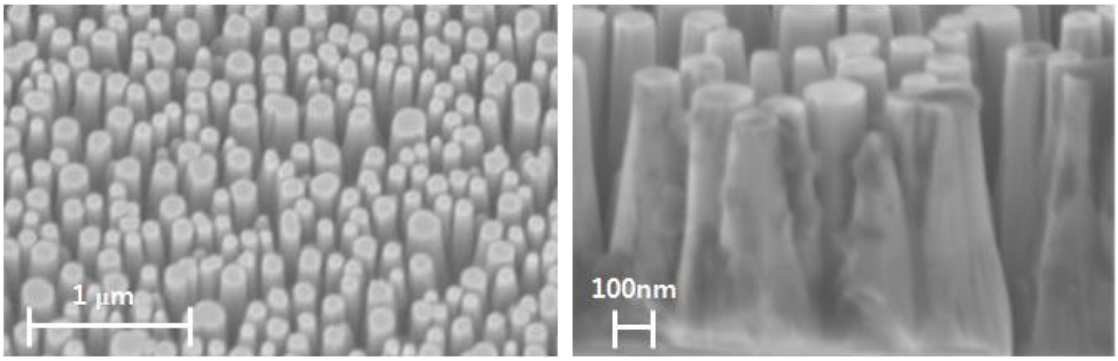


Figure **4-7** The FESEM images of the InGaN/GaN nanopillars created at the 0.18 nm/s etch rate (left: 30° tilted view, right: cross-sectional view).

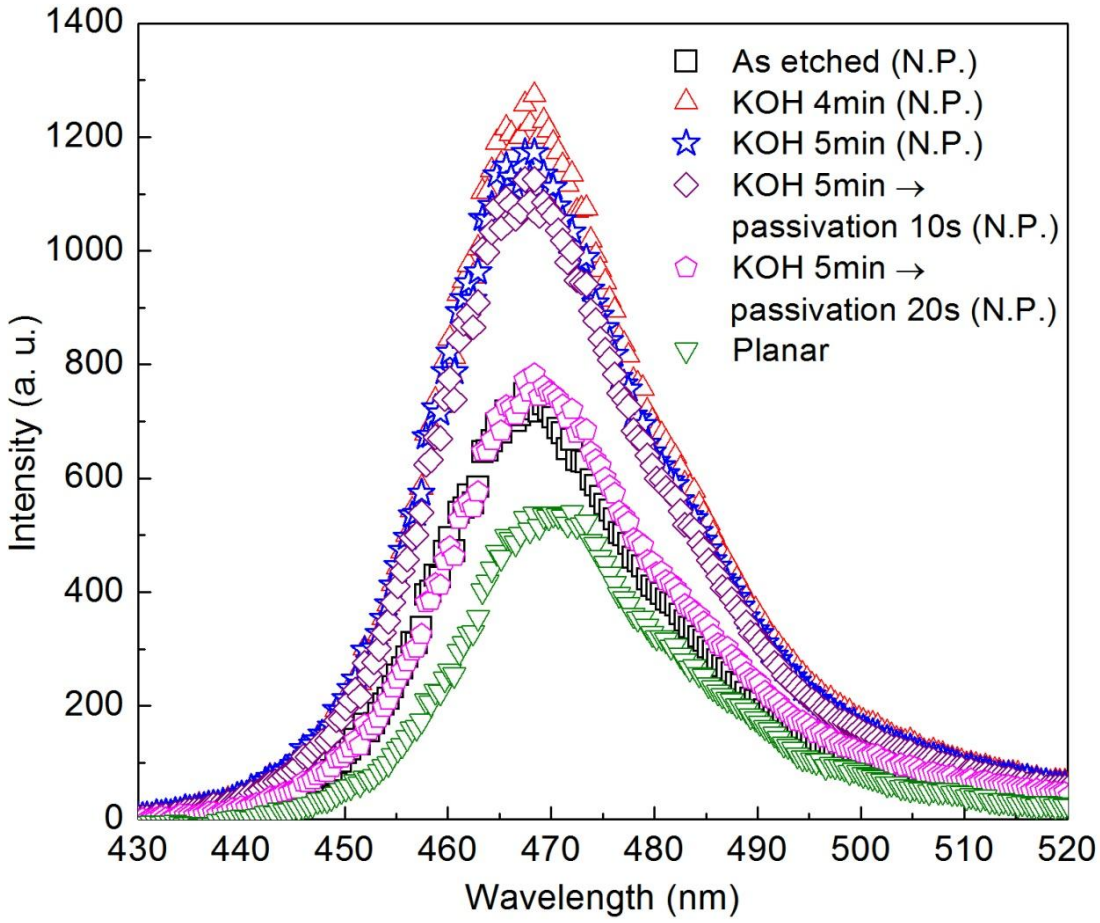


Figure **4-8** PL spectra of InGaN/GaN nanopillars created at the 0.18 nm/s etch rate followed by the two step 4 % KOH and $(NH_4)_2S$/ISP=1:10 treatments at various times.

The next experiment was to form the nanopillar profile with a slower etch rate to confirm if the slower etch would reduce the sidewall damage by itself. The dry etching recipe for SiO_2 etching was unchanged, but the dry etching recipe for InGaN/GaN etching was modified to Cl_2: 21 sccm, BCl_3: 12 sccm, pressure: 6 mTorr, ICP power: 100 W, RIE power: 10 W, time: 3600 s. Then the InGaN/GaN etch rate dropped to 0.18 nm/s. The nanopillar profiles is shown in Figure 4-7. In order to confirm the passivation effect, the nanopillars created by the slow etch rate recipe were treated by the two step passivation technique. In Figure 4-8, the PL intensity of the nanopillars created by the slow etch rate recipe is 1.3 times higher than the PL intensity of the planar structure. After the two step passivation of 4 % KOH for 5 min and $(NH_4)_2S$/ISP=1:10 for 10 s, the PL intensity of the nanopillars were 2 times higher than the PL intensity of the planar structure. The blue shift was less significant compared to the fast dry etching.

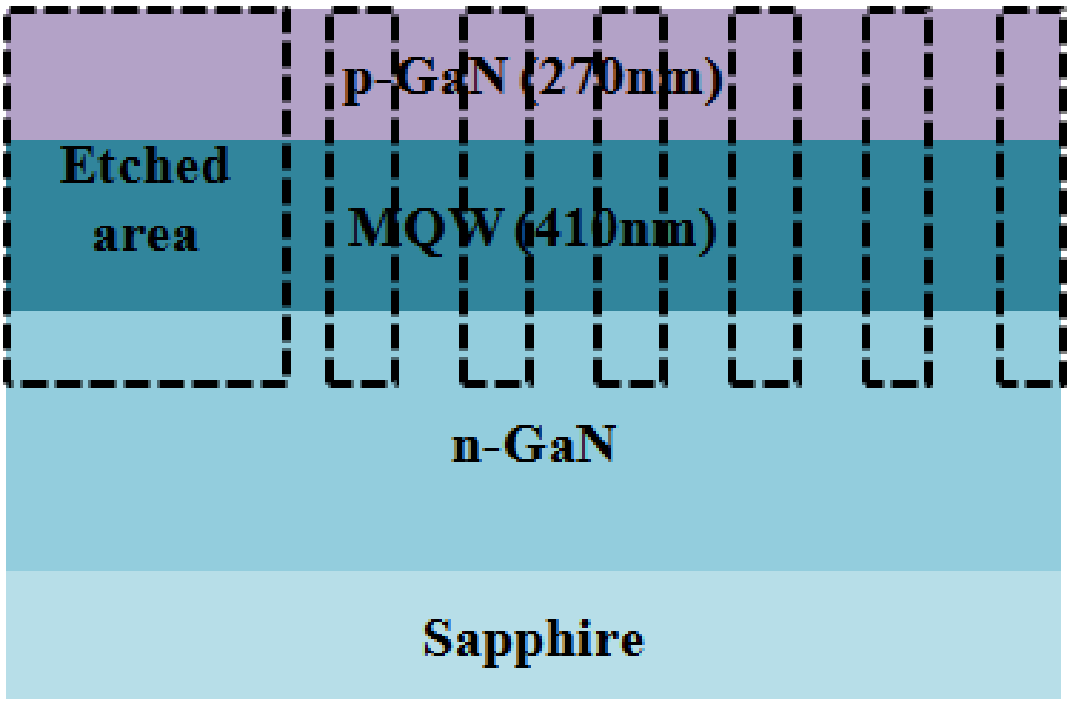


Figure **4-9** The sketch of InGaN/GaN heterostructure.

The InGaN/GaN heterostructure sample consists of approximate 410 nm of p-GaN and 270 nm of multi quantum wells and very thick n-GaN from the top to bottom. The sketch is shown in Figure 4-9. For device fabrication, the n-GaN layer must be exposed in order to deposit the ohmic contact on n-GaN. Therefore, the InGaN/GaN nanopillars etched at the slower etch rate with the deeper target depth of 850 nm is better for device fabrication. The previous etching depth was just 650 nm.

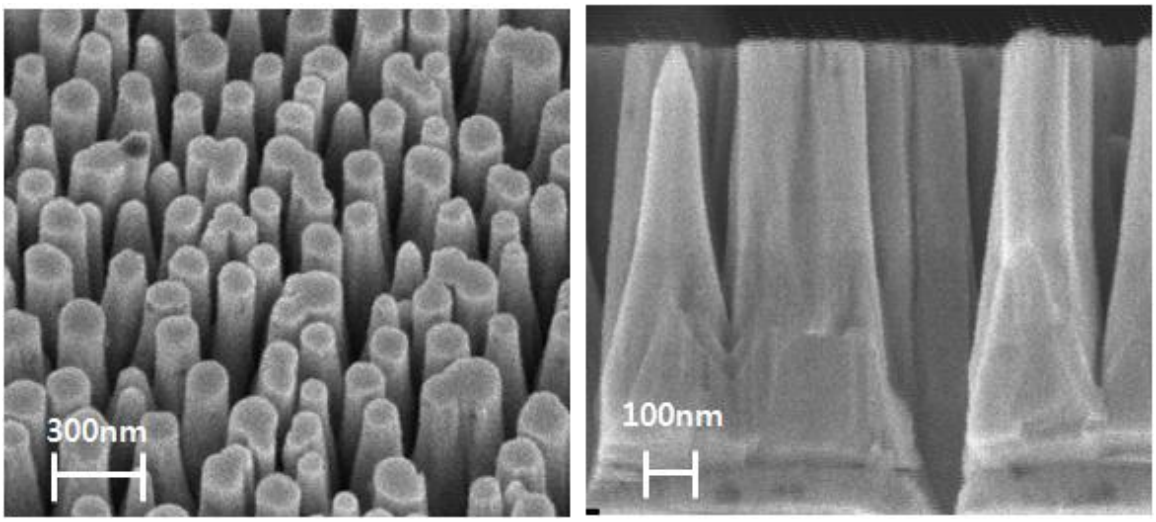


Figure **4-10** The FESEM images of InGaN/GaN nanopillars created at the 0.18 nm/s etch rate with greater etching depth (over 850 nm)

Figure 4-10 shows the nanopillar profiles with deeper etching. Dry etching recipe for SiO_2 etching was unchanged, but the ratio of Cl_2 to BCl_3 in InGaN/GaN etching recipe was modified from 21 sccm/12 sccm to 27 sccm/6 sccm to enhance the selectivity against SiO_2 nanopillars. Also, the etching time increased from 3600 s to 4200 s. As a result, the nanopillars with the average etching depth of 850 nm were created.

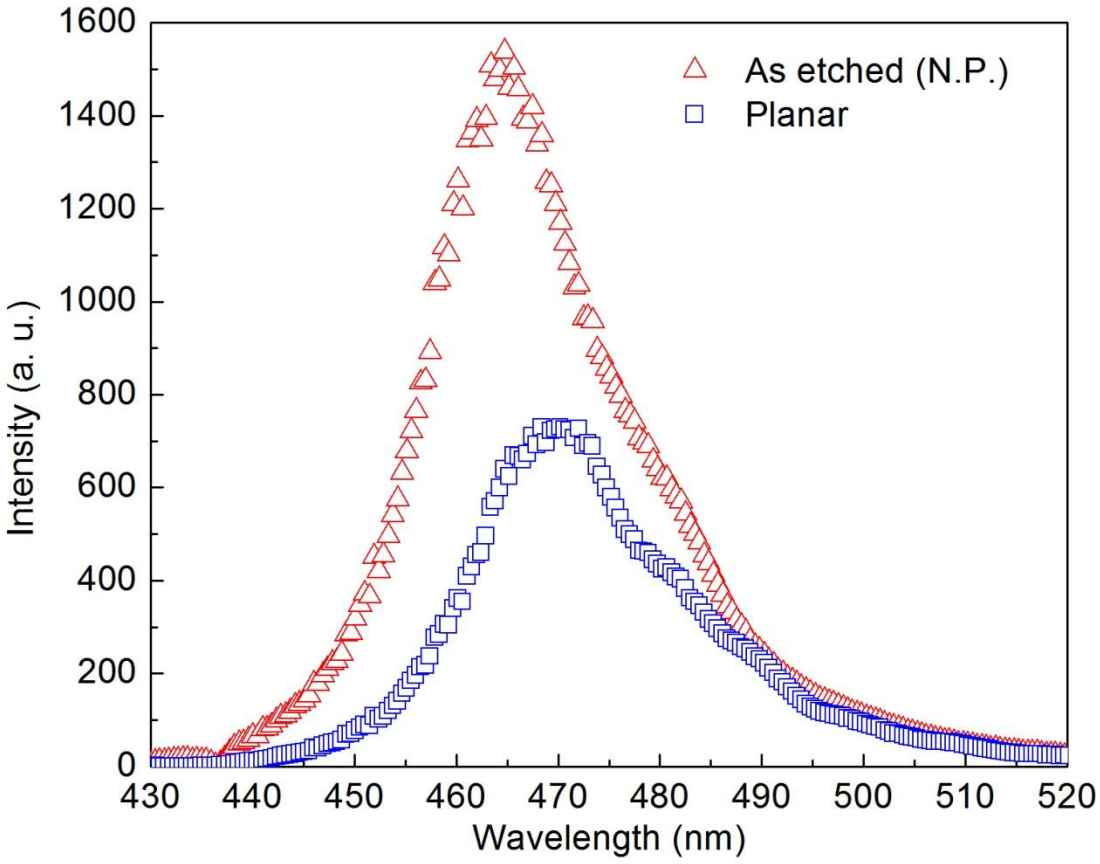


Figure **4-11** PL spectra of InGaN/GaN nanopillars created at 0.18 nm/s etch rate with deeper etching depth.

Figure 4-11 shows the PL intensity comparison between the nanopillar and planar structure. Without any passivation, the nanopillars showed a 2.1 times higher PL intensity compared to the planar structure. The full exposure of the MQW region explains the additional enhancement of PL intensity and blue shift. For device fabrication, the nanopillars prepared at a deeper target etch depth and slow etch rate were used without KOH treatment due to the possibility to attack of the p-GaN layer on top of the nanopillars.

4.3 Transparent ohmic contact to p-GaN

In order to confirm if the combination of surface treatment and N_2 annealing is effective to lower the specific contact resistivity, the following experiments were implemented. The surfaces of the p-GaN samples were treated by one to three step surface treatments such as 1:10 BOE only; 1:10 BOE and $(NH_4)_2S$/ISP; and BOE, 0.4 % KOH, and $(NH_4)_2S$/ISP. Then the samples were annealed at 600℃ under N_2 in the RTA for various times. Table 4-1shows the experimental data. In these experiments, the p-GaN samples which have the following Hall data were used. p: $2.67x10^{19}$ cm^{-3}, mobility: 0.468 cm^2/Vs, resistivity : 0.5017 ohm-cm, the thickness of p-GaN: 170 nm.

Contact	Avg. Rsh (Ω/□)	Avg. ρc (Ω/cm^2)
Au/Ni/p-GaN, Air, 500°C, 10min	$2.4x10^{4}$	$2.4x10^{-3}$
ITO/p-GaN, as deposited	$4.0x10^{4}$	$4.5x10^{-2}$
ITO/p-GaN, N_2, RTA 600°C, 1min	$4.1x10^{4}$	$5.5x10^{-3}$
ITO/p-GaN, N_2, RTA 600°C, 5min	$5.5x10^{4}$	$5.8x10^{-3}$
ITO/p-GaN, N_2, RTA 600°C, 10min	$7.9x10^{4}$	$4.0x10^{-3}$
ITO/p-GaN, N_2, RTA 600°C, 15min	$8.7x10^{4}$	$5.7x10^{-3}$
ITO/p-GaN, $(NH_4)_2S$+ISP(1:10) 20s, as deposited	$4.5x10^{4}$	$3.9x10^{-2}$
ITO/p-GaN, $(NH_4)_2S$+ISP(1:10) 20s, N_2, RTA 600°C, 1min	$4.6x10^{4}$	$5.3x10^{-3}$
ITO/p-GaN, $(NH_4)_2S$+ISP(1:10) 20s, N_2, RTA 600°C, 5min	$5.9x10^{4}$	$5.1x10^{-3}$
ITO/p-GaN, $(NH_4)_2S$+ISP(1:10) 20s, N_2, RTA 600°C, 10min	$7.3x10^{4}$	$5.1x10^{-3}$
ITO/p-GaN, $(NH_4)_2S$+ISP(1:10) 20s, N_2, RTA 600°C, 15min	$9.0x10^{4}$	$4.8x10^{-3}$
ITO/p-GaN, 0.4% KOH 90s+$(NH_4)_2S$+ISP(1:10) 20s, as deposited	$4.8x10^{4}$	$4.1x10^{-2}$
ITO/p-GaN, 0.4% KOH 90s+$(NH_4)_2S$+ISP(1:10) 20s, N_2, RTA 600°C, 1min	$4.5x10^{4}$	$6.0x10^{-3}$
ITO/p-GaN, 0.4% KOH 90s+$(NH_4)_2S$+ISP(1:10) 20s, N_2, RTA 600°C, 5min	$5.6x10^{4}$	$5.7x10^{-3}$
ITO/p-GaN, 0.4% KOH 90s+$(NH_4)_2S$+ISP(1:10) 20s, N_2, RTA 600°C, 10min	$6.8x10^{4}$	$5.6x10^{-3}$
ITO/p-GaN, 0.4% KOH 90s+$(NH_4)_2S$+ISP(1:10) 20s, N_2, RTA 600°C, 15min	$8.3x10^{4}$	$6.1x10^{-3}$

Table **4-1** Specific contact resistivities depending on the different surface treatments and annealing conditions.

The experimental results proved that the specific contact resistivities did not much improve by varying the surface treatments. Also, the specific contact resistivity improved when the sample was annealed at 600℃ under N_2 in the rapid thermal annealing (RTA) for 1 min, but it did not improve further at longer time.

The next experiment was to confirm if inserting a thin metal film of a high work function metal between ITO and p-GaN is effective for lowering the specific contact resistivity. The experimental results are shown in Table 4-2. In these experiments, the p-GaN samples which have the following Hall data were used. p: $8.4x10^{17}$ cm^{-3}, mobility: 6.5 cm^2/Vs, resistivity: 0.95 ohm-cm, sheet resistance: ~26,000 ohm/sqr.

Contact	Avg. Rsh (Ω/□)	Avg. ρc ($Ω/cm^2$)
Au/Ni/p-GaN, Air, 500°C, 10min	$2.4x10^4$	$2.4x10^{-3}$
ITO(100nm)/p-GaN, $(NH_4)_2S$+ISP(1:10) 20s, as deposited	$4.9x10^4$	$1.5x10^{-1}$
ITO(100nm)/Ni(2nm)/p-GaN, $(NH_4)_2S$+ISP(1:10) 20s, as deposited	$5.1x10^4$	$5.6x10^{-2}$
ITO(100nm)/Pd(2nm)/p-GaN, $(NH_4)_2S$+ISP(1:10) 20s, as deposited	$3.7x10^4$	$6.9x10^{-2}$
ITO(100nm)/Pt(2nm)/p-GaN, $(NH_4)_2S$+ISP(1:10) 20s, as deposited	$4.0x10^4$	$8.0x10^{-2}$

Table **4-2** The difference of specific contact resistivities depending on inserting high work function metals between ITO and p-GaN.

The specific contact resistivity improved when thin metals such as Ni, Pd, and Pt were inserted between ITO and p-GaN. Among the three kinds of high work function metals, inserting thin Ni was the most effective to improve the contact. Based on those experimental results, the proper ITO contact conditions were determined for device fabrication.

4.4 Oblique deposition on top of the nanopillars

In order to prevent the electrical short by depositing ITO on the n-GaN region, the oblique ITO deposition was tested. First, the ITO was deposited at the angles of -30°/30° and -45°/45° with 300 nm each and then at 0° with 100nm (nominal value).

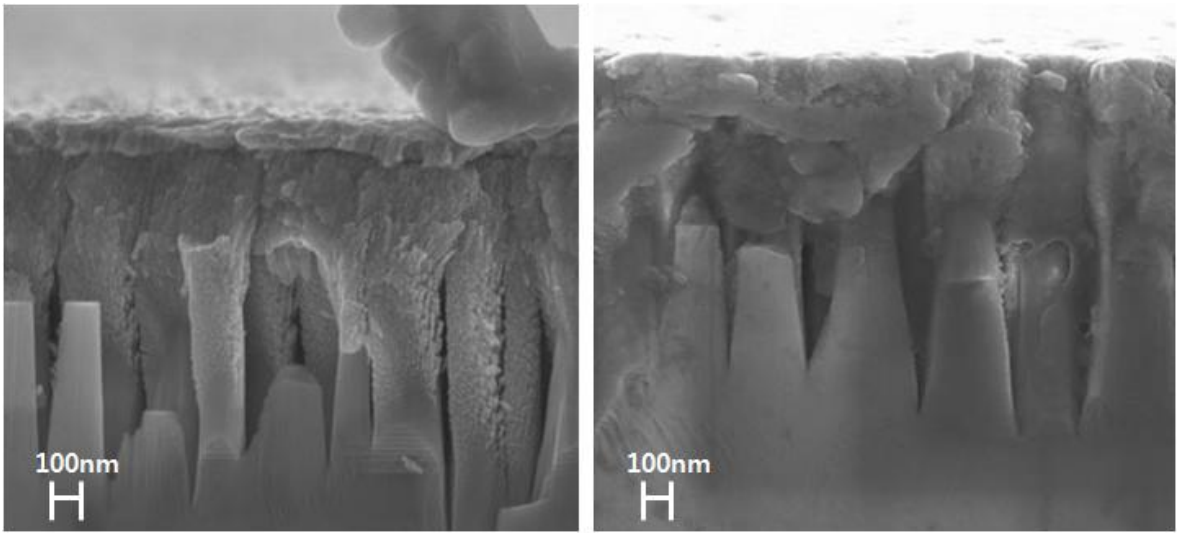


Figure **4-12** The slanted ITO deposition for different nominal deposition thickness and oblique angle (left: 300 nm/300 nm/100 nm at -30°/30°/0°, right: 350 nm/350 nm/ 100 nm at -45°/45°/0°).

Figure 4-12 shows ITO was deposited on the MQW region in both cases, possibly causing the electrical short. Also, ITO can be deposited on the n-GaN region at 0° deposition if the slanted ITO does not fill all of the holes between nanopillars. Therefore, other angled deposition processes were designed as shown in Figure 4-13.

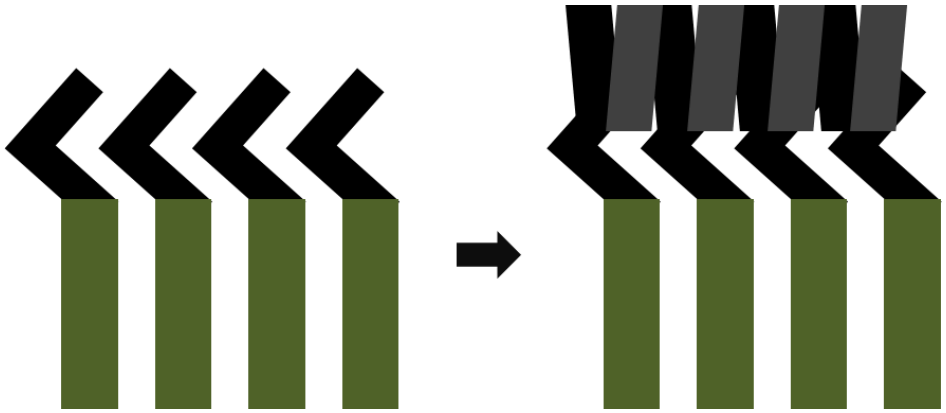
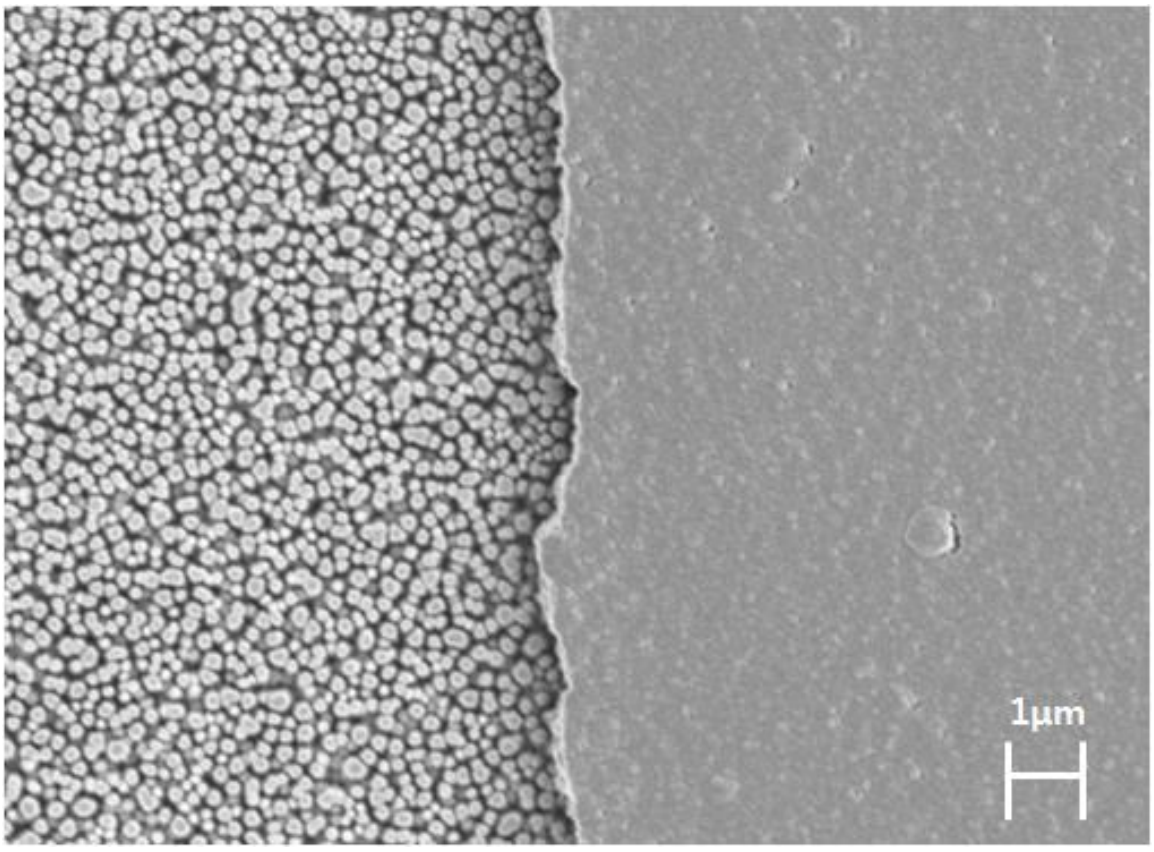


Figure **4-13** The slanted ITO deposition at the oblique angles of -65°/65° and then -45°/45°.



Uncovered area Covered area

Figure **4-14** The FESEM image of the slanted ITO deposition at the oblique angles of -65°/65° and then -45°/45° with 300 nm (nominal value) at each angle.

Figure 4-14 shows the top view of the oblique deposited ITO at -65°/65° and -45°/ 45° with 300 nm deposited at each angle. The FESEM image shows that ITO covered all the top of nanopillars without the blanket deposition. This ITO deposition technique was chosen for the device fabrication, and the absence of electrical short was confirmed by electrical characterization.

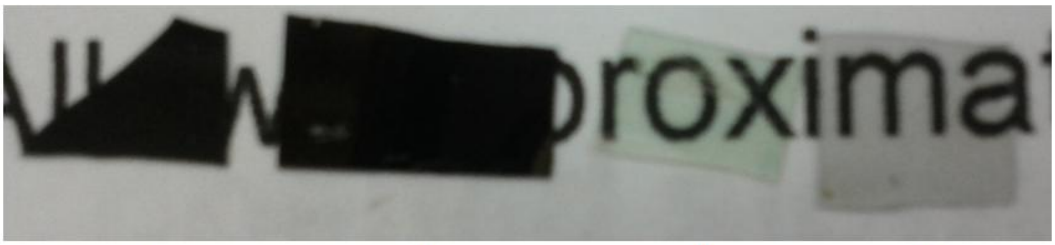
Chapter 5

Device fabrication and characterization

In this chapter, InGaN/GaN nanopillar LED devices without and with sulfur passivation were fabricated based on the preliminary data reported in the chapter 4. After the device fabrication, electrical and optical characterization was performed.

5.1 InGaN/GaN nanopillar LED device fabrication

On top of the nanopillars, ITO film was deposited at the angles of 65°/ -65°/ 45°/ -45° with 300 nm each (nominal value) to create a transparent ohmic contact to p-GaN as reported in chapter 4. However, the ITO film lost its transparency because its thickness was too great (actual thickness: 600 nm). In order to check if ITO film becomes transparent in a certain annealing condition, various annealing tests were conducted in air and N_2 at 500℃. The annealing temperature was lowered by 100℃ compared to the preliminary experiments in order to keep sulfur passivation effectiveness.



(a) (b) (c) (d)

Figure **5-1** Images of deposited ITO on the glasses annealed under different conditions. (a) as deposited, (b) annealed at 500℃ under N_2 in the RTA for 1 min, (c) annealed at 500℃ under air in the tube furnace for 10 min, (d) annealed at 500℃ under air in the tube furnace for 10 min and then annealed at 500℃ under N_2 in the RTA for 1 min.

According to the experimental results represented in Figure 5-1, ITO became transparent when it was annealed in air rather than N_2. With regard to the ITO annealing test results, a process flow was designed and demonstrated in Figure 5-2.

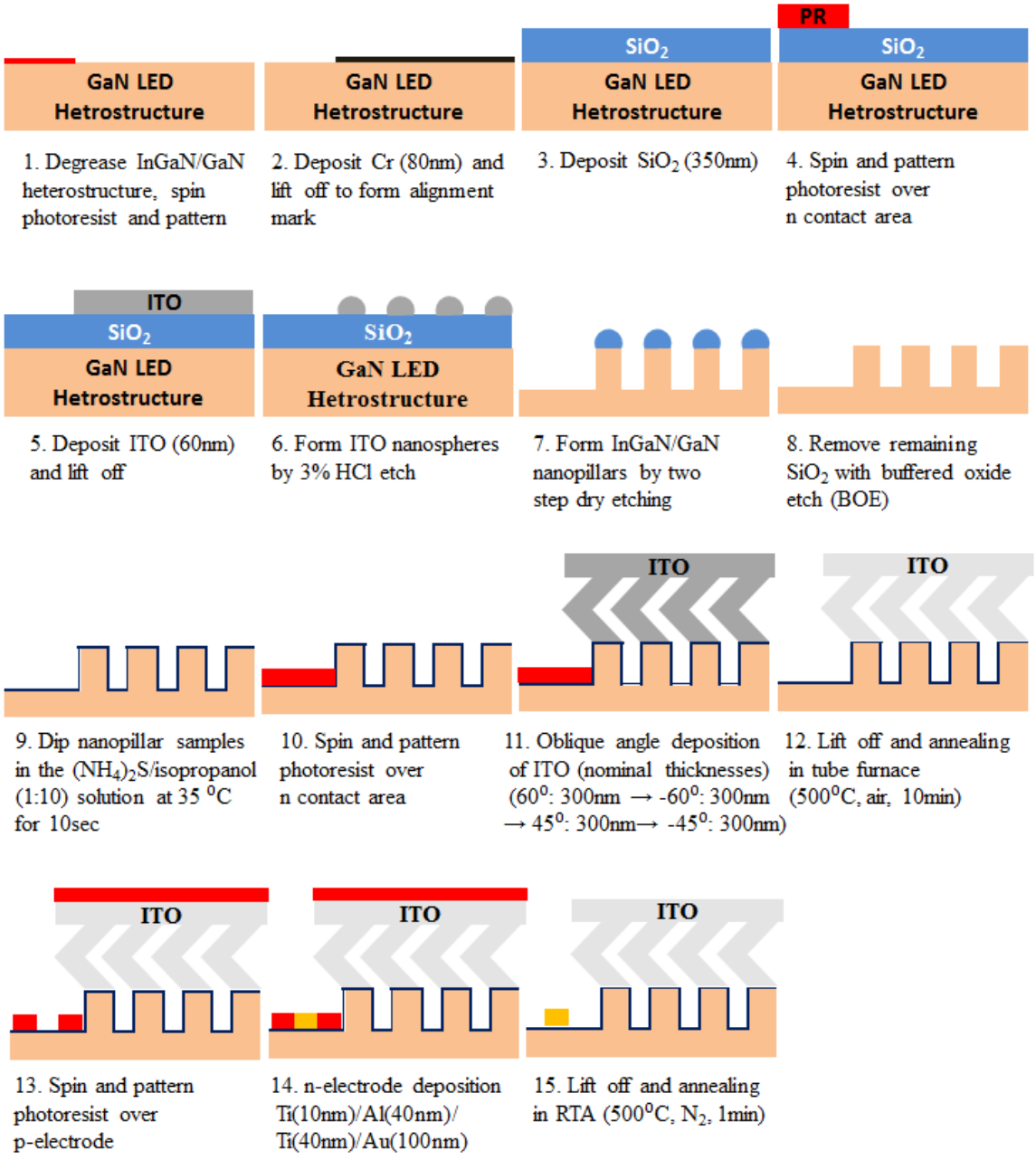


Figure **5-2** A process flow of the InGaN/GaN nanopillar device fabrication.

(1) Degrease InGaN/GaN heterostructure, spin photoresist and pattern.

(2) Deposit Cr (80 nm) and lift off to form alignment mark.

(3) Deposit SiO_2 (350 nm) by PECVD.

(4) Spin and pattern photoresist over n contact area.

(5) Deposit ITO (60 nm) by e-beam evaporation and lift off.

(6) Form ITO nanospheres by 3 % HCl etch.

(7) Form InGaN/GaN nanopillars by two step dry etching using fluorine and chlorine based plasma.

(8) Remove remaining SiO_2 with buffered oxide etch (BOE).

(9) Dip the nanopillar samples in the $(NH_4)_2S$/ isopropanol (1:10) solution at 35℃ for 10 s or not.

(10) Spin and pattern photoresist over n contact area.

(11) Oblique angle deposition of ITO (nominal thicknesses)

(60°: 300 nm → -60°: 300 nm → 45°: 300 nm→ -45°: 300 nm).

(12) Lift off and annealing in tube furnace (500℃, air, 10 min).

(13) Spin and pattern photoresist over p-electrode.

(14) n-electrode deposition of Ti (10 nm)/Al (40 nm)/Ti (40 nm)/Au (100 nm).

(15) Lift off and annealing in RTA (500℃, N_2, 1 min).

The InGaN/GaN nanopillar devices without and with passivation were fabricated by the above process flow. For the next step, electrical and optical characterization was performed.

5.2 Electrical and optical characterization

Electrical and optical characterization results of the nanopillar devices without and with passivation are displayed as an I-V curve and the spectrum of electroluminescence (EL). PL was used for the nanopillar characterization in preliminary experiments. On the other hand, EL was used for the nanopillar device characterization. PL and EL have a similarity in terms of detecting the light emission generated by radiative recombination of electron and hole pairs. On the other hand, they have a difference in terms of using different energy sources of laser and electrical field.

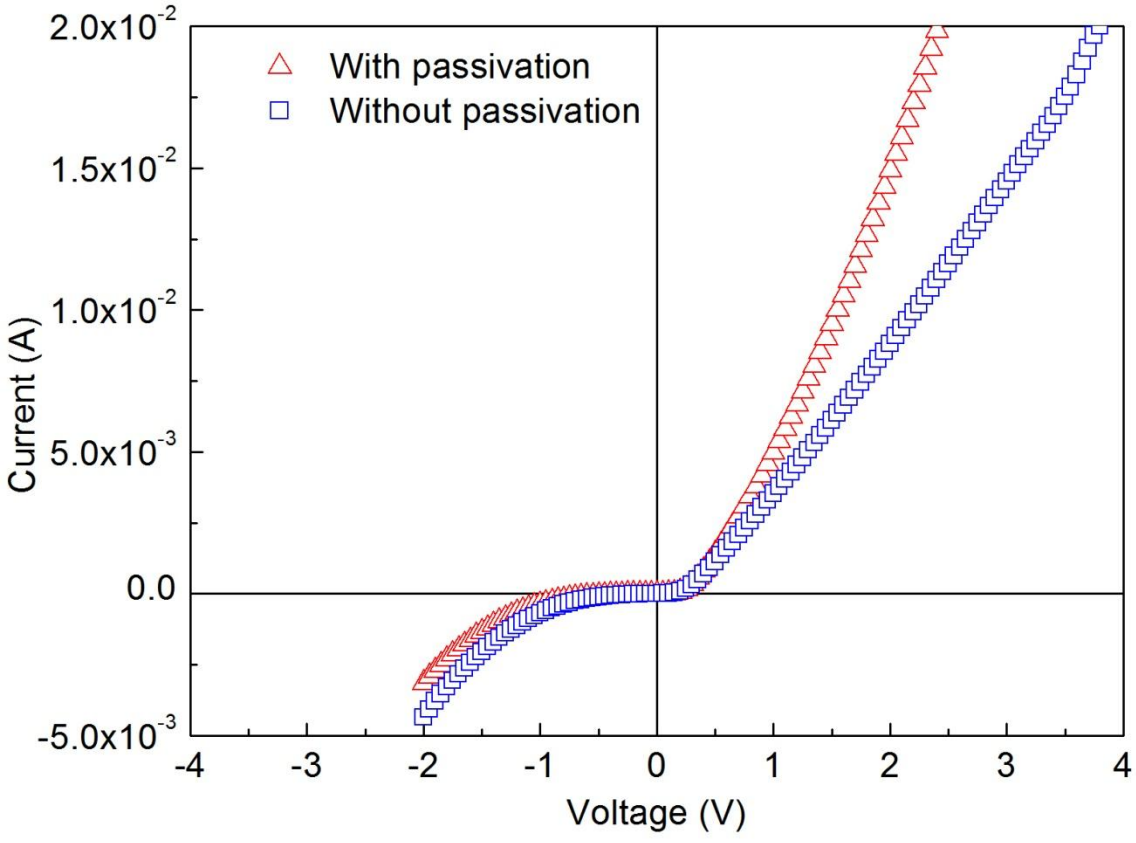


Figure **5-3** I-V characterization results of nanopillar device without and with passivation.

Figure 5-3 shows the I-V characterization results. The absence of an electrical short was confirmed, but the leakage current was observed in both the devices without and with passivation under reverse bias. Also, light emission was not detected in electroluminescence characterization. The reason why the light emission was not detected can be explained by the following. The leakage current shown under reverse bias is caused by the existence of surface defects on the sidewalls, which suppress the light emission by depressing the radiative recombination. Because the leakage current was observed in both devices without and with sulfur passivation, the sulfur passivation was not regarded as the reason for the leakage current. Therefore, the annealing step was assumed to be the main cause for the leakage current because the annealing step was not proven to be acceptable in the preliminary experiment. Therefore, a modified process flow leaving out the annealing steps was redesigned.

5.3 InGaN/GaN nanopillar LED device fabrication leaving out annealing

Based on the assumption that the leakage current happens due to the defects created on the sidewall by annealing, a modified process flow leaving out annealing steps was designed. Before the device fabrication, the ability to achieve the ohmic contact to n-GaN and the transparent ohmic contact p-GaN without annealing was confirmed.

In previous device fabrication, Ti (10 nm)/Al (40 nm)/Ti (40 nm)/Au (100 nm) layers were deposited on the n-GaN, and then the ohmic contact was accomplished by annealing in N_2 at 500℃ for 1 min. However, whether Ti (10 nm)/Al (40 nm)/ Ti(40 nm)/Au (100 nm) forms an ohmic contact to to n-GaN without annealing was not known. On the other hand, Cho et al. reported another technique to form the ohmic

contact to n-GaN with Cr based metal layers [78]. In order to choose a proper contact method, Ti/Al and Cr based contacts to n-GaN were compared in parallel, and the I-V characterization results were demonstrated in Figure 5-4.

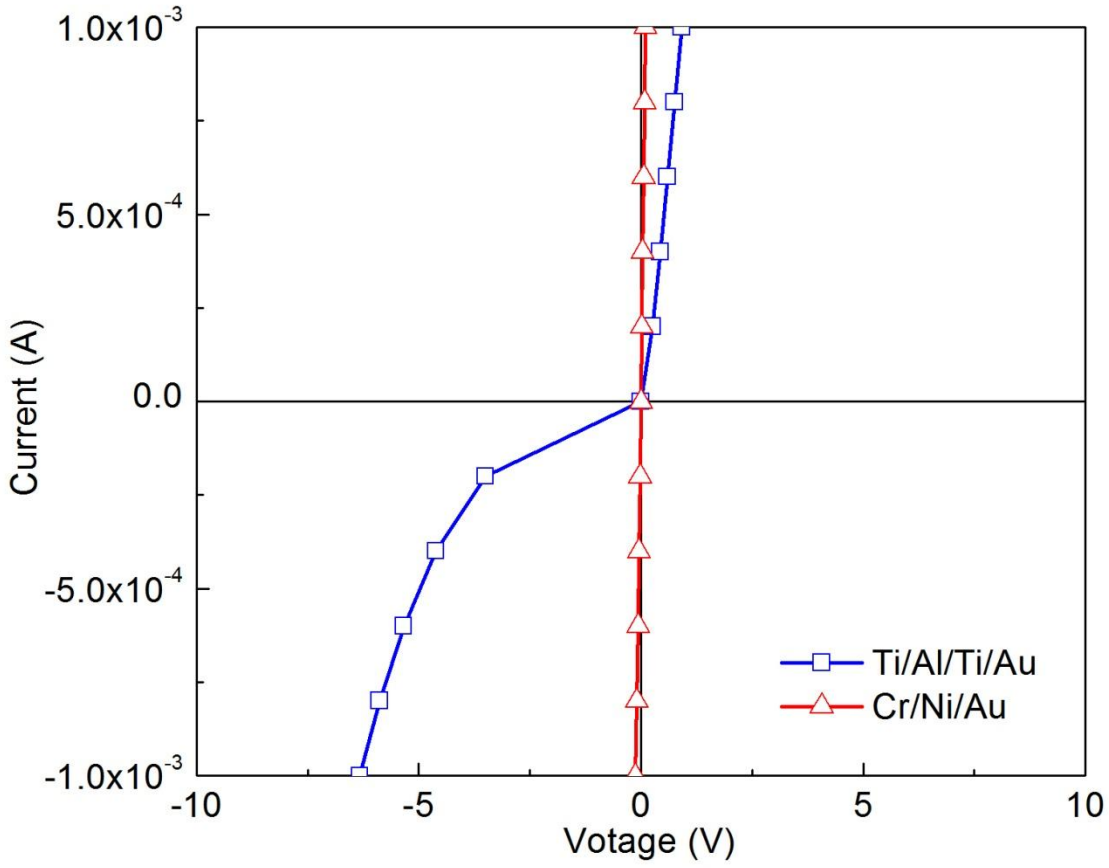


Figure **5-4** I-V characterization results of Ti/Al and Cr based contacts to n-GaN.

According to the I-V characterization results, the Cr based contact to n-GaN showed the better ohmic behavior. Therefore the Cr based contact to n-GaN was chosen for device fabrication.

Next, the transparent ITO ohmic contact to p-GaN was accomplished by annealing under air at 500℃ for 1 min in a tube furnace as in previous device fabrication.

However, the technique to achieve transparent ITO ohmic contact to p-GaN without annealing was also considered at this moment. In chapter 4, the contact improvement by inserting high work function metals of Pd, Ni, and Pt between ITO and p-GaN was proved, and Ni showed the best performance. Based on the preliminary experiments, two assumptions were examined. First, Ni might form the better ohmic contact than ITO to p-GaN without annealing. Second, oblique deposited Ni might show the better transparency than blanket depositied Ni.

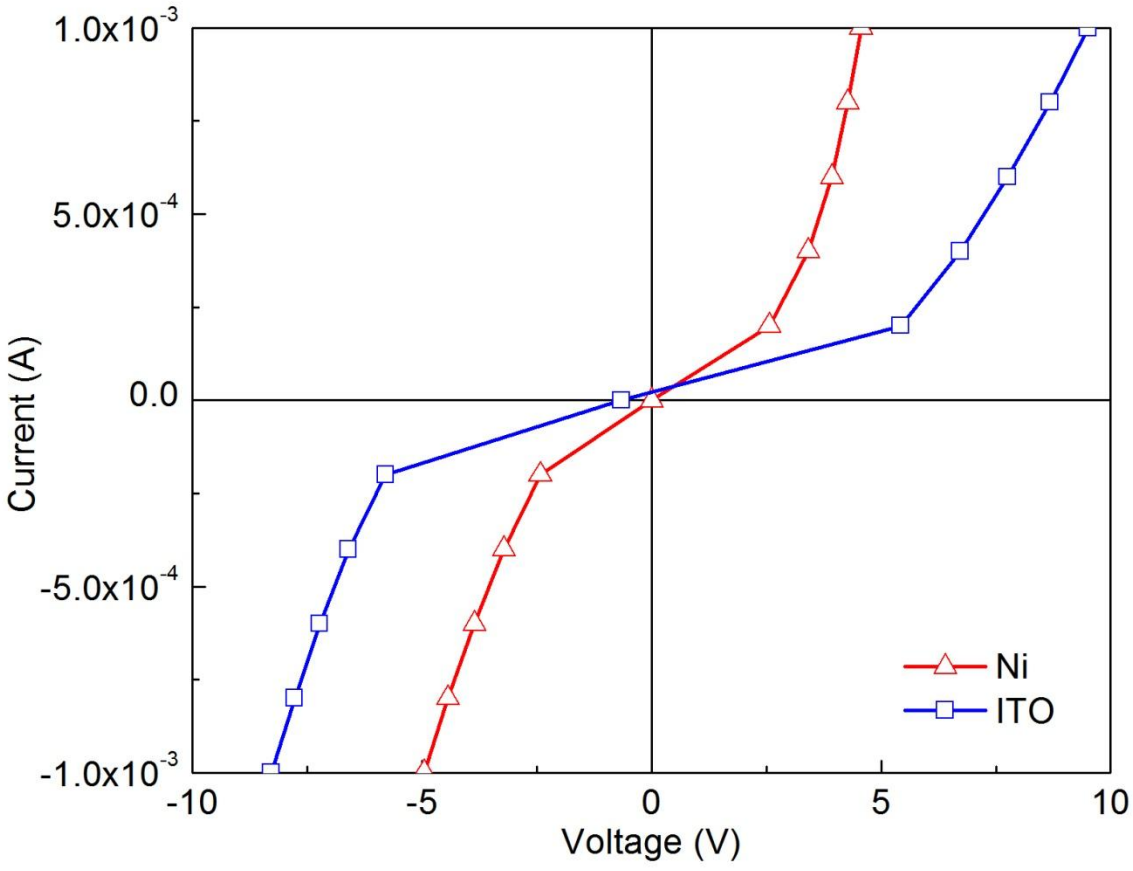


Figure **5-5** I-V characterization results of Ni and ITO contacts to p-GaN.

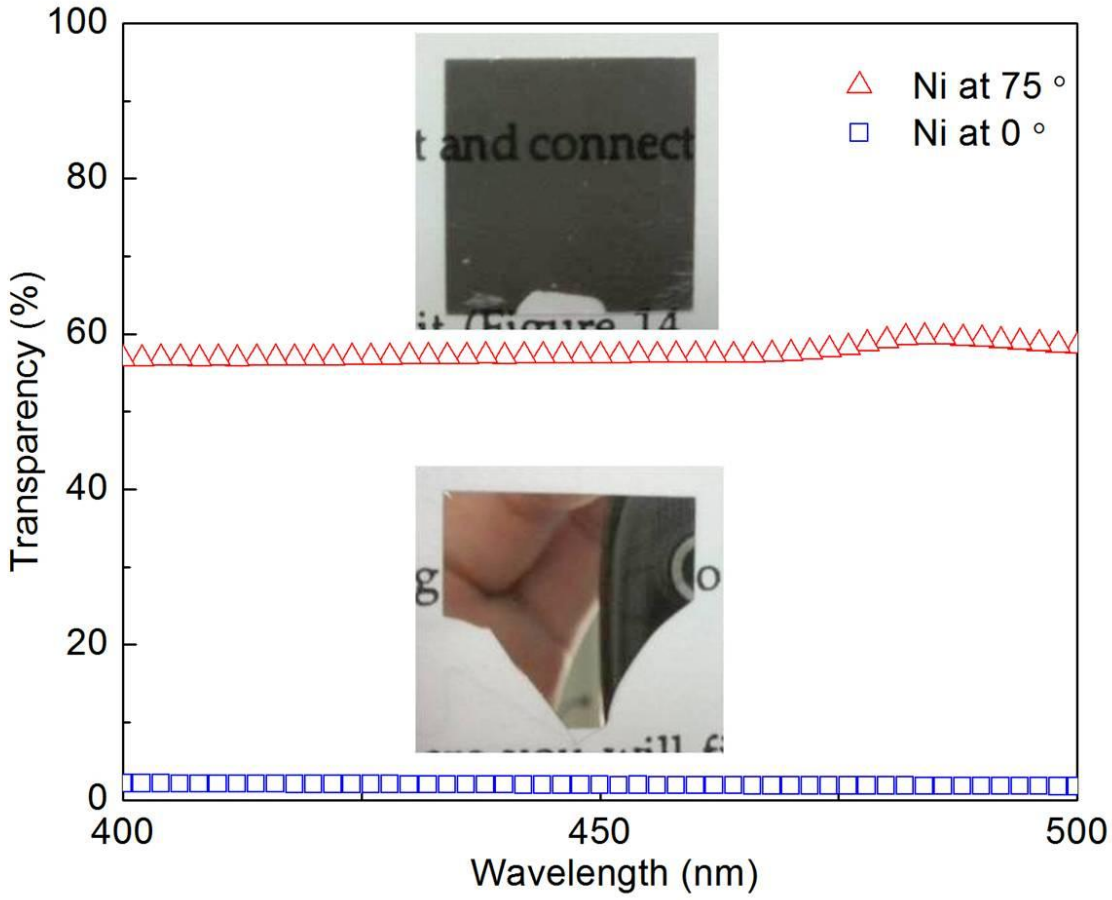


Figure **5-6** Transparency comparison of oblique and blanket deposited Ni.

Figure 5-5 and 5-6 show two different experimental results. According the experimental results, Ni showed the better ohmic behavior than ITO to p-GaN, and oblique deposited Ni demonstrated much higher transparency than blanket deposited Ni. In Figure 5-6, letters are shown through the oblique deposited Ni, but they are not shown through the blanket deposited Ni. With regard to these experimental results, oblique deposited Ni was chosen for the contact to p-GaN in device fabrication. Additional blanket Ni deposition on the oblique deposited Ni was not performed to absolutely avoid the electrical short and keep high transparency.

In order to verify that if the electrical short was completely prevented, the cross-section of the nanopillars was characterized by FESEM, and the images are shown in Figure 5.7. The cross-sectional FESEM images demonstrated that Ni obliquely deposited on the nanopillars only.

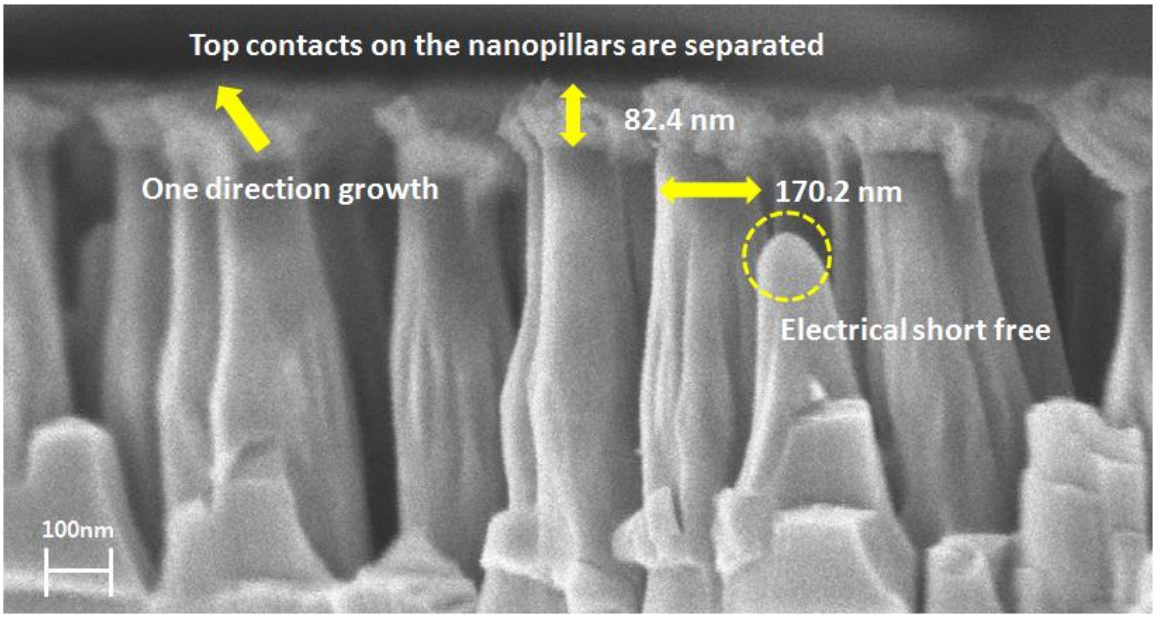


Figure **5-7** The cross-sectional FESEM image of Ni deposited at an oblique angle of 75° to a nominal thickness of 180nm on top of the nanopillars.

Based on the preliminary data, a modified process flow was designed, and it was demonstrated in Figure 5-8.

Modified process flow

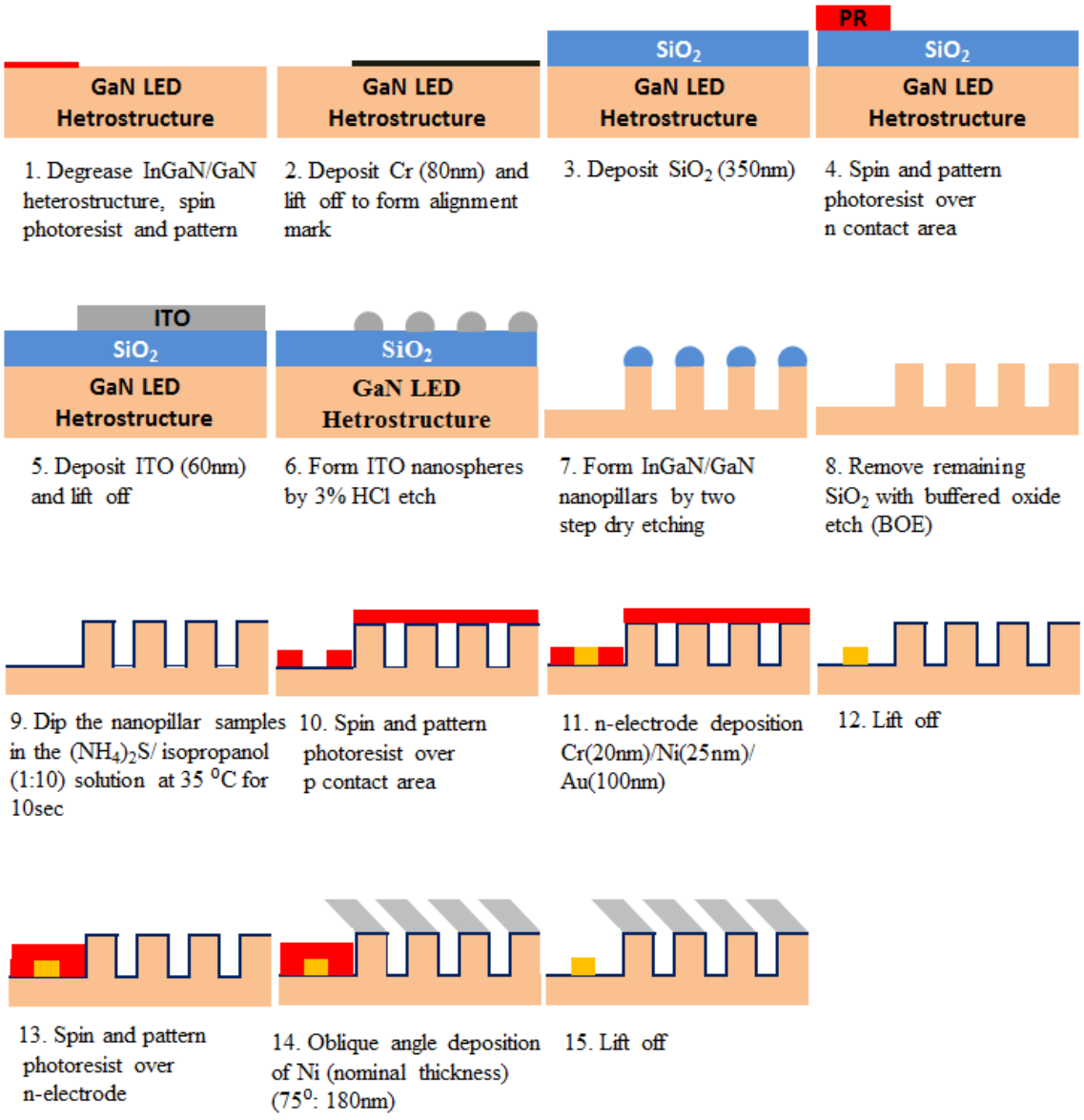


Figure **5-8** A modified process flow of InGaN/GaN nanopillar device fabrication leaving out annealing steps.

(1) Degrease InGaN/GaN heterostructure, spin photoresist and pattern.

(2) Deposit Cr (80 nm) and lift off to form alignment mark.

(3) Deposit SiO_2 (350 nm) by PECVD.

(4) Spin and pattern photoresist over n-contact area.

(5) Deposit ITO (60 nm) by e-beam evaporation and lift off.

(6) Form ITO nanospheres by 3 % HCl etch.

(7) Form InGaN/GaN nanopillars by two step dry etching using fluorine and chlorine based plasma.

(8) Remove remaining SiO_2 with buffered oxide etch (BOE).

(9) Dip the nanopillar samples in the $(NH_4)_2S$/ isopropanol (1:10) solution at 35℃ for 10 s.

(10) Spin and pattern photoresist over p contact area.

(11) n-electrode deposition of Cr (20 nm)/ Ni (25 nm)/ Au (100 nm).

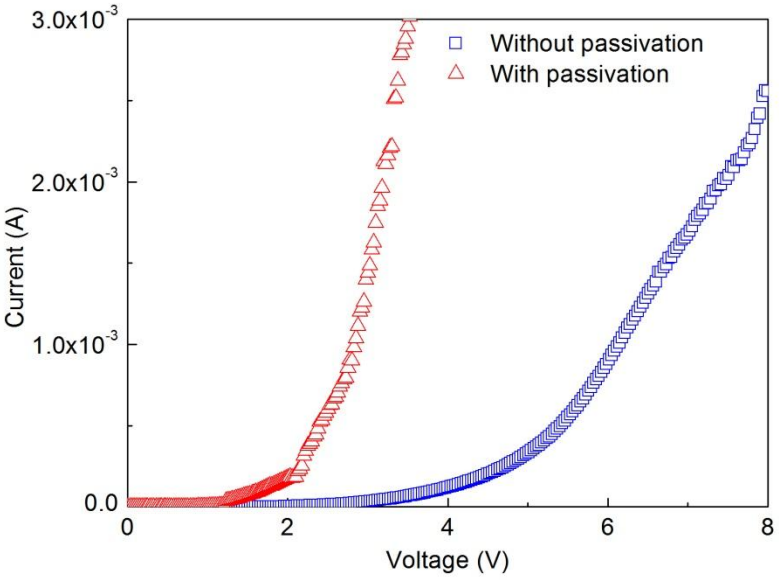
(12) Lift off.

(13) Spin and pattern photoresist over n-electrode.

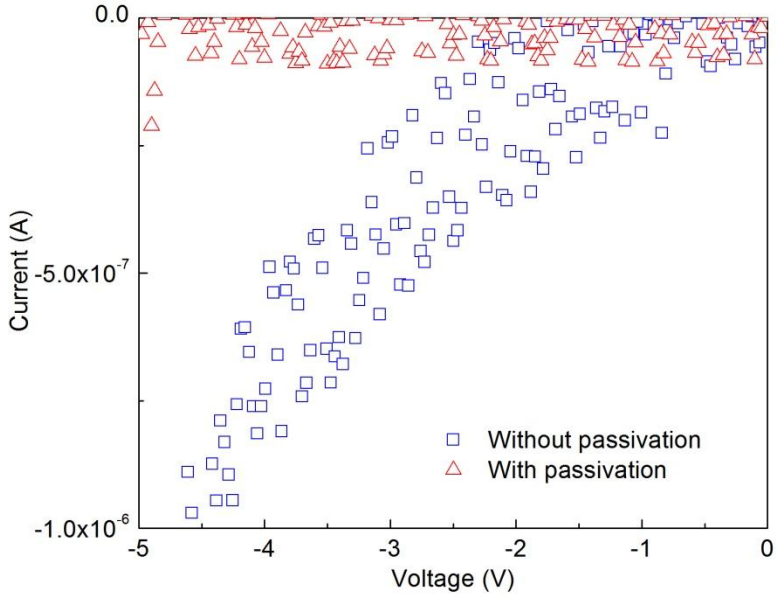
(14) Oblique angle deposition of Ni (nominal thickness) (75°: 180 nm).

(15) Lift off.

5.4 Electrical and optical characterization



(a)



(b)

Figure **5-9** I-V characterization results of nanopillar devices without and with passivation under (a) forward bias, (b) reverse bias.

Suppressed leakage current was demonstrated under reverse bias in both devices without and with passivaiton compared to previous devices fabricated including annealing steps in Figure 5-9. Also, less leakage current in reverse bias and higher current in forward bias were observed in nanopillar devices with rather than without passivation.

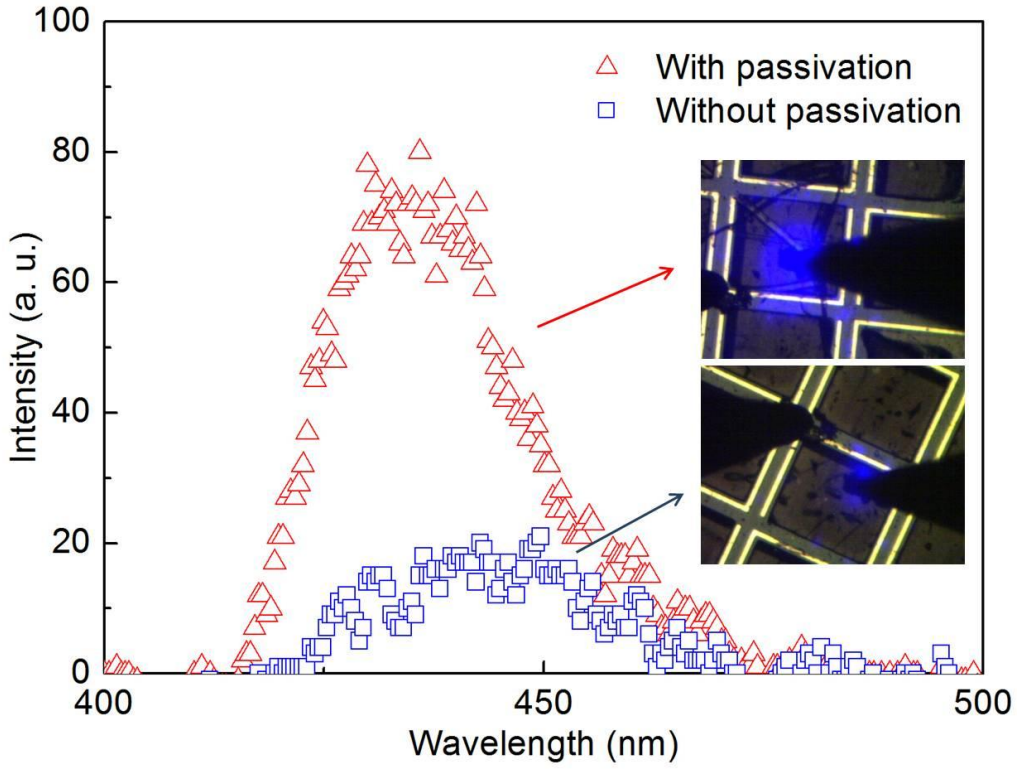


Figure **5-10** EL characterization in nanopillar devices without and with sulfur passivation as fabricated (current: 3mA, pulse width: 500μs, duty cycle: 50%).

4 times higher EL intensity was recorded in the nanopillar device with passivation than without passivation as shown in Figure 5-10. Because all the nanopillars were isolated, the light emission happened in a spot where the probe tips touched the pillars. The blue shift of the passivated LED sample indicates an increased carrier density in the MQW area, causing radiative recombination.

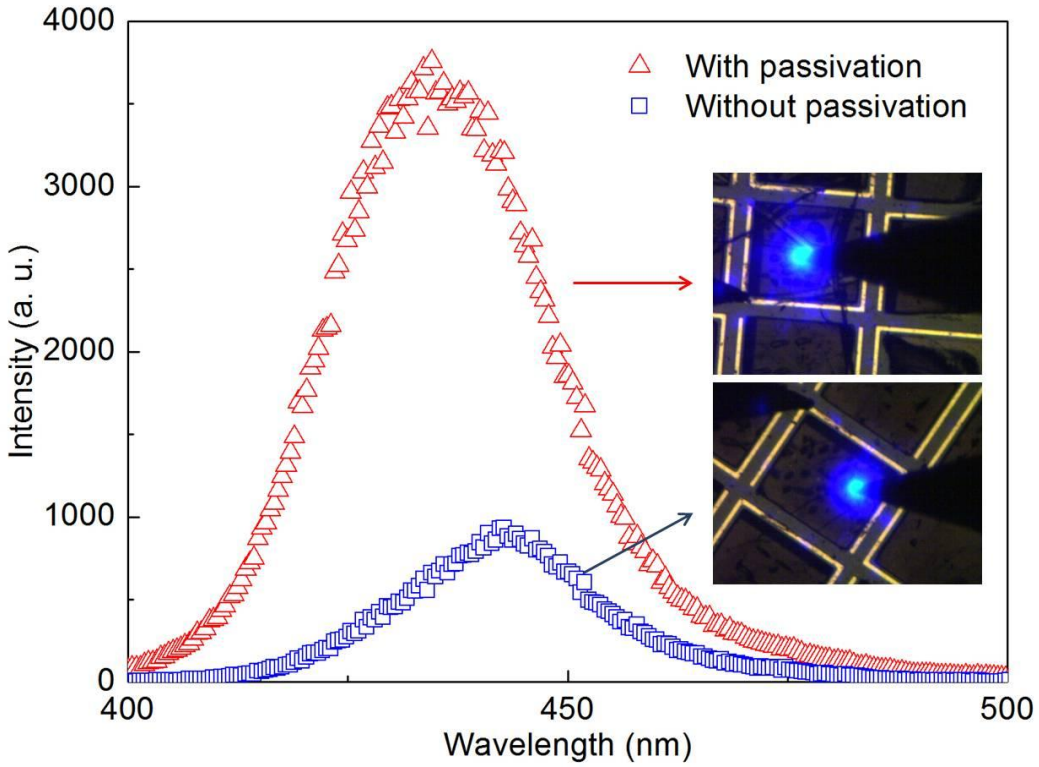


Figure **5-11** EL characterization in nanopillar devices without and with sulfur passivation 50 days after stored in a desiccator (current: 3mA, pulse width: 500μs, duty cycle: 50%).

50 days after both LEDs were stored in a desiccator, the EL characterization was repeated at the same spots in order to check the stability of sulfur passivation. Finally, the comparable results were obtained as shown in Figure 5-11. For more reliable EL comparison, the measurements were performed under following restrictions. The light emission was captured with both LEDs while the same pulsed current of 3 mA was prolonged under the same detector position. Also, the measurements were repeated at 3 different spots in each device to ensure the reproducibility.

Chapter 6

Conclusion and future work

6.1 Conclusion

When InGaN/GaN nanopillar LEDs are prepared by dry etching, N vacancies and GaO_x, InO_x are created on the nanopillar sidewalls, increasing the leakage current and causing non-radiative surface recombination. As a result, the internal quantum efficiency drops, and it degrades the device efficiency. In this study, lowering the etch rate and using a two step techniques of consecutive KOH wet etching and $(NH_4)_2S$/ isopropanol passivation were studied to reduce the sidewall damage and improve the device efficiency. PL intensity in nanopillars prepared by the slow etch rate (0.18 nm/s) was 2 times higher than that of planar samples. In nanopillar LEDs, an additional 4 times higher EL intensity and suppressed leakage current under reverse and forward bias were recorded with rather than without sulfur passivation.

The effects of lowering InGaN/GaN etch rate and sulfur passivation can be explained by the following. First, the etch rate was reduced by the elimination of Ar and reduced ICP and RIE power. Then, the physical bombardment on the sidewall of nanopillers was lessened, and the etch rate difference between Ga and N was diminished simultaneously. As a result, the surface defects (generally N vacancies) on the sidewalls were reduced. That is why the slow etching was helpful to improve the light emission. KOH wet etching was less effective for the nanopillars created at the slow etch rate rather than the fast etch rate because the sidewall damage was already reduced by the slow dry etching.

Second, when nanopillar LEDs were treated by the $(NH_4)_2S$/ISP solution, a sulfur monolayer was coated on the nanopillar sidewall, with S replacing O. Then, the non-radiative recombination was suppressed on the InGaN/GaN nanopillar surface. As a result, the light emission improved, and leakage current was suppressed.

6.2 Future work

In this study, the data obtained from electrical and optical characterizations demonstrated that device efficiency was improved by sulfur passivation. However, the reason why the non-radiative recombination on the InGaN/GaN nanopillar surface was depressed by sulfur passivation was not clearly explained. Therefore, literature was reviewed in order to find evidence supporting the mechanism in terms of materials characterization. Based on the X-ray photoelectron spectroscopy (XPS) data for the planar samples, Ga 2p spectra appeared while O 1s spectra disappeared [79][80][81]. Also, Huh et al. demonstrated that the O peak disappeared while the S peak appeared Auger electron spectroscopy (AES) [82]. Those materials characterization results indicate the GaO_x was dissociated to Ga and O by the sulfur treatment, and GaS_x was created. In addition, Chang et al. showed that In-O bonding disappeared while In-S bonding appeared by XPS characterization, in addition to change in the valence band maximum and Fermi level on the surface [83].

Sik et al. explained the reduction of recombination velocity on the GaAs surface from sulfur passivation. When the GaAs was treated with a $(NH_4)_2S$ solution, the surface Fermi-level position was modified due to the new surface trap associated with As–S and Ga–S bonds. The surface Fermi level was shifted away from the midgap due to the

formation of the S-related chemical bonds. As a result, the shifted Fermi level position induced a reduction of the nonradiative surface recombination velocity, and hence, PL intensity increased [84].

With regard to above references, the following assumption was made. Valence band edge shifts (changes in band bending near the surface) occur on the InGaN/GaN nanopillar surface after sulfur passivation due to the generation of In-S and Ga-S chemical bonds. Then, the Fermi level shifts upon the valence band edge shifts, and the new Fermi level position depresses non-radiative surface recombination. Finally, the light emission intensity increases and improves the device performance.

In order to prove the validity of the above assumption, XPS characterization with a InGaN/GaN planar sample to see the effect of passivation on etched surface and TEM characterization with a InGaN/GaN nanopillar sample to see the sulfur bonding on the sidewall are recommended future work.

References

[1] E. Fred Schubert, **Light emitting diode second edition**, 2nd ed, Cambridge, 2006.

[2] Nakamura, Shuji, Pearton, S. J, Fasol, and Gerhard, **The blue laser diode: the complete story**, 2nd ed, Springer, 2000.

[3] V. Ramesh, A. Kikuchi, K. Kishino, M. Funato and Y. Kawakami, "Strain relaxation effect by nanotexturing InGaN/GaN multiple quantum well," J. Appl. Phys., vol. 107, no. 11, pp. 114303, Jun. 2010.

[4] Tetsuya Takeuchi, Shigetoshi Sota, Maki Katsuragawa, Miho Komori, Hideo Takeuchi, Hiroshi Amano and Isamu Akasaki, "Quantum confined Stark effect due to piezoelectric fields in GaInN strained quantum wells," Jpn. J. Appl. Phys., vol. 36, no. 4A, pp. L382-L385, Feb. 1997.

[5] Min-Ho Kim, Martin F. Schubert, Qi Dai, Jong Kyu Kim and E. Fred Schubert, "Origin of efficiency droop in GaN-based light-emitting diodes," Appl. Phys. Lett., vol. 91, no. 18, pp. 183507, Oct. 2007.

[6] Hwa-Mok Kim, Yong-Hoon Cho, Hosang Lee, Suk Il Kim, Sung Ryong Ryu, Deuk Young Kim, Tae Won Kang and Kwan Soo Chung, "High-Brightness Light Emitting Diodes Using Dislocation-Free Indium Gallium Nitride/Gallium Nitride Multiquantum-Well Nanorod Arrays," Nanoletters vol. 4, no. 6, pp. 1059-1062, May 2004.

[7] Yu Zhi-Guo, Chen Peng, Yang Guo-Feng, Liu Bin, Xie Zi-Li, Xiu Xiang-Qian, Wu Zhen-Long, Xu Feng, Xu Zhou, Hua Xue-Mei, Han Ping, Shi Yi, Zhang Rong and Zheng You-Dou, "Influence of dry etching damage on the internal quantum

efficiency of nanorod InGaN/GaN multiple quantum wells," Chin. Phys. Lett., vol. 29, no. 7, pp. 078501, Feb. 2012.

[8] Akihiko Kikuchi, Mizue Kawai, Makoto Tada and Katsumi Kishino, "InGaN/GaN multiple quantum disk nanocolumn light-emitting diodes grown on (111) Si Substrate," Jpn. J. Appl. Phys., vol. 43, no 12A, pp. L1524–L1526, Nov. 2004.

[9] Jihong Zhu, Liangji Wang, Shuming Zhang, Hui Wang, Degang Zhao, "The fabrication of GaN-based nanopillar light-emitting diodes," Journal of Applied Physics, vol. 108, no. 7, pp. 074302, Oct. 2010.

[10] Ji-Myon Lee, Kug-Seung Lee, and Seong-Ju Park, "Removal of dry etch damage in p-type GaN by wet etching of sacrificial oxide layer," Vac. Sci. Technol. B, vol. 22, no. 2, pp. 479-482, Feb. 2004.

[11] Qiming Li, Karl R. Westlake, Mary H. Crawford, Stephen R. Lee, Daniel D. Koleske, Jeffery J. Figiel, Karen C. Cross, Saeed Fathololoumi, Zetian Mi and George T. Wang, "Optical performance of top-down fabricated InGaN/GaN nanorod light emitting diode arrays," Optics Express, vol. 19, no. 25, pp. 25528-25534, Dec. 2011.

[12] H. W. Choi, S. J. Chua, A. Raman, J. S. Pan, and A. T. S. Wee, "Plasma-induced damage to n-type GaN," Appl. Phys. Lett., vol. 77, no. 12, pp. 1795-1797, August. 2000.

[13] H. W. Huang, C. C. Kao, T. H. Hsueh, C. C. Yu, C. F. Lin, J. T. Chu, H. C. Kuo,

and S. C. Wang, “Fabrication of GaN-based nanorod light emitting diodes using self-assemble nickel nano-mask and inductively coupled plasma reactive ion etching,” Mater. Sci. Eng. B, vol 113, pp. 125–129, July 2004.

[14] M. Y. Hsieh, C. Y. Wang, L. Y. Chen, M. Y. Ke, and J. J. Huang, “InGaN–GaN Nanorod Light Emitting Arrays Fabricated by Silica Nanomasks,” IEEE J. Quantum Electron., vol.44, no 5, pp. 468-471, May 2008.

[15] Ji Hye Kang, Hyung Gu Kim, Hyun Kyu Kim, Hee Yun Kim, Jae Hyoung Ryu, Periyayya Uthirakumar, Nam Han, and Chang-Hee Hong, “Improvement of Light Output Power in InGaN/GaN Light-Emitting Diodes with a Nanotextured GaN Surface Using Indium Tin Oxide Nanospheres,” Japanese Journal of Applied Physics, vol. 48, pp. 102104, Oct. 2009.

[16] Yu Zhi-Guo, Chen Peng, Yang Guo-Feng, Liu Bin, Xie Zi-Li, Xiu Xiang-Qian, Wu Zhen-Long, Xu Feng, Xu Zhou, Hua Xue-Mei, Han Ping, Shi Yi, Zhang Rong, and Zheng You-Dou, “Influence of dry Etching damage on the internal quantum efficiency of nanorod InGaN/GaN multiple quantum wells,” Chin. Phys. Lett., vol. 29, no. 7, pp. 178501, Feb. 2012.

[17] Zhu Ji-Hong, Zhang Shu-Ming, Sun Xian, Zhao De-Gang, Zhu Jian-Jun, Liu Zong shun, Jiang De-Sheng, Duan Li-Hong, Wang Hai, Shi Yong-Sheng, Liu Su-Ying, Yang Hui, “Fabrication and Optical Characterization of GaN-Based Nanopillar Light Emitting Diodes,” Chin. Phys. Lett., vol. 25, no. 9, pp. 3485-3488, May 2008.

[18] C H Chiu, T C Lu, H W Huang, C F Lai, C C Kao, J T Chu, C C Yu, H C Kuo, S C

Wang, C F Lin and T H Hsueh, “Fabrication of InGaN/GaN nanorod light-emitting diodes with self-assembled Ni metal islands,” Nanotechnology, vol. 18, pp. 445201. Sep 2007.

[19] Ching-Hua Chiu, Ming-Hua Lo, Tien-Chang Lu, Peichen Yu, H. W. Huang, Hao-Chung Kuo, Shing-Chung Wang, “Nano-processing techniques applied in GaN-Based Light-Emitting Devices with self-assembly Ni nano-masks,” Journal of Lightwave Technology, vol. 26, no. 11, pp. 1445-1454, June 2008.

[20] Cheng-Yin Wang, Liang-Yi Chen, Cheng-Pin Chen, Yun-Wei Cheng, Min-Yung Ke, Min-Yann Hsieh, Han-Ming Wu, Lung-Han Peng, and JianJang Huang, “GaN nanorod light emitting diode arrays with a nearly constant electroluminescent peak wavelength,” Optics Express, vol. 16, no. 14, pp. 10549-10556, July 2008.

[21] Min-Yung Ke, Cheng-Yin Wang, Liang-Yi Chen, Hung-Hsien Chen, Hung-Li Chiang, Yun-Wei Cheng, Min-Yann Hsieh, Cheng-Pin Chen, and JianJang Huang, “Application of Nanosphere Lithography to LED Surface Texturing and to the Fabrication of Nanorod LED Arrays,” IEEE Journal Of Selected Topics In Quantum Electronics, vol. 15, no. 4, pp. 1242-1248, Aug. 2009.

[22] Liang-Yi Chen, Hung-Hsun Huang, Chun-Hsiang Chang, Ying-Yuan Huang, Yuh-Renn Wu, and JianJang Huang, “Investigation of the strain induced optical transition energy shift of the GaN nanorod light emitting diode arrays,” Optics Express, vol. 19, no. S4, pp. A900-907, July 2011.

[23] J. Bai Q. Wang and T. Wang, “Greatly enhanced performance of InGaN/GaN nanorod light emitting diodes,” Phys. Status Solidi A, vol. 209, no. 3, pp.477-480, Feb. 2012.

[24] Liang-Yi Chen, Ying-Yuan Huang, Chun-Hsiang Chang, Yu-Hsuan Sun, Yun-Wei Cheng, Min-Yung Ke, Cheng-Pin Chen, and JianJang Huang, "High performance InGaN/GaN nanorod light emitting diode arrays fabricated by nanosphere lithography and chemical mechanical polishing processes," Optics Express, vol. 18, no. 8, pp. 7664-7669, April 2010.

[25] Min-An Tsai, Peichen Yu, C. L. Chao, C. H. Chiu, H. C. Kuo, S. H. Lin, J. J. Huang, T. C. Lu, , and S. C. Wang, "Efficiency Enhancement and Beam Shaping of GaN–InGaN Vertical-Injection Light-Emitting Diodes via High-Aspect-Ratio Nanorod Arrays," IEEE Photonics Technology Letters, vol. 21, no. 4, pp. 257-259, Feb. 2009.

[26] Y. Yang and X. A. Cao, "Removing plasma-induced sidewall damage in GaN-based light-emitting diodes by annealing and wet chemical treatments," J. Vac. Sci. Technol. B, vol. 27, no. 6, pp 2337-2341, Oct. 2009.

[27] T. Shen, G. Gao, and H. Morkoc, "Recent developments in ohmic contacts for III–V compound semiconductors," J. Vac. Sci. Technol. B, vol. 10, no. 5, pp. 2113–2132, May 1992.

[28] J. Sun, K. A. Rickert, J. M. Redwing, A. B. Ellis, F. J. Himpsel, and T. F. Kuech, "p-GaN surface treatments for metal contacts," Appl. Phys. Lett., vol. 76, no. 4, pp. 415–417, Jan. 2000.

[29] J.-S. Jang and T.-Y. Seong, "Mechanisms for the reduction of the Schottky barrier heights of high-quality nonalloyed Pt contacts on surface-treated p-GaN," J. Appl. Phys., vol. 88, no. 5, pp. 3046–3066, Sep. 2000.

[30] H. Ishikawa, S. Kobayashi, Y. Koide, S. Yamasaki, S. Nagai, J. Umezaki, M. Koike,

and M. Murakami, “Effects of surface treatments and metal work functions on electrical properties at p-GaN/metal interfaces,” J. Appl. Phys., vol. 81, no. 3, pp. 1315–1322, Feb. 1997.

[31] J.-L. Lee, J. K. Kim, J.W. Lee, Y. J. Park, and T. Kim, “Effect of surface treatment by KOH solution on ohmic contact formation of p-type GaN,” Solid State Electron., vol. 43, no. 2, pp. 435–439, Feb. 1999.

[32] J.-S. Jang, S.-J. Park, and T.-Y. Seong, “Formation of low resistance Pt ohmic contacts to p-type GaN using two-step surface treatment,” J. Vac. Sci. Technol. B, Microelectron., vol. 17, no. 6, pp. 2667–2670, Nov. 1999.

[33] Chi-Sen Lee, Yow-Jon Lin, and Ching-Ting Lee, “Investigation of oxidation mechanism for ohmic formation in Ni/Au contacts to *p*-type GaN layers,” Appl. Phys. Lett., Vol. 79, No. 23, 3, 3815-3817, Oct. 2001.

[34] Y. Tang, D. You, J. Xu, X. Li, X. Li, and H. Gong, “Reduction of ohmic contact resistivity on p-GaN using N_2 plasma surface treatment at room temperature,” Semicond. Sci. Technol., vol. 21, no. 12, pp. 1597–1599, Oct. 2006.

[35] J.-S. Jang, S.-J. Park, and T.-Y. Seong, “Low resistance and thermally stable Pt/Ru ohmic contacts to p-type GaN,” Phys. Stat. Sol. (C), vol. 180, no. 1, pp. 103–107, Jul. 2000.

[36] H.-K. Kim, T.-Y. Seong, I. Adesida, C. W. Tang, and K. M. Lau, “Lowresistance Pt/Pd/Au ohmic contacts to p-type AlGaN,” Appl. Phys. Lett.,vol. 84, no. 10, pp. 1710–1712, Mar. 2004.

[37] J. W. Bae1, T. Hossain, I. Adesida1, K. H. Bogart, D. Koleske, A. A. Allerman, and J. H. Jang, “Low resistance ohmic contact to *p*-type GaN using Pd/Ir/Au multilayer scheme,” J. Vac. Sci. Technol. B 23(3), 1072, Jun. 2005.

[38] L. Zhou, W. Lanford, A. T. Ping, I. Adesida, J. W. Yang, and A. Khan, “Low resistance Ti/Pt/Au ohmic contacts to *p*-type GaN,” Appl. Phys. Lett., Vol. 76, No. 23, 3451, April. 2000.

[39] H. Cho, T. Hossain, J. Bae, and I. Adesida, “Characterization of Pd/Ni/Au ohmic contacts on p-GaN,” Solid State Electron., vol. 49, no. 5, pp. 774–778, May 2005.

[40] J.-S. Jang, C.-W. Lee, S.-J. Park, T.-Y. Seong, and I. T. Ferguson, "Low resistance and thermally stable Pd/Ru ohmic contacts to p-type GaN," J. Electron. Mater., vol. 31, no. 9, pp. 903–906, Feb. 2002.

[41] V. Rajagopal Reddy, S.-H. Kim, J. O. Song, and T.-Y. Seong, "Low resistance and thermally stable Pd/Re ohmic contacts to p-type GaN," Semicond. Sci. Technol., vol. 18, no. 6, pp. 541–544, Jun. 2003.

[42] J.-S. Jang, I.-S. Chang, H.-K. Kim, T.-Y. Seong, S. Lee, and S.-J. Park, "Low-resistance Pt/Ni/Au ohmic contacts to p-type GaN," Appl. Phys. Lett., vol. 74, no. 1, pp. 70–72, Jan. 1999.

[43] J.-K. Ho, C.-S. Jong, C. C. Chiu, C.-N. Huang, C.-Y. Chen, and K.-K. Shih, "Low resistance ohmic contacts to p-GaN," Appl. Phys. Lett., vol. 74, no. 9, pp. 1275–1277, Mar. 1999.

[44] J.-K. Ho, C.-S. Jong, C. C. Chiu, C.-N. Huang, K.-K. Shih, L.-C. Chen, F.-R. Chen, and J.-J. Kai, "Low resistance ohmic contacts to p-GaN achieved by the oxidation of Ni/Au films," J. Appl. Phys., vol. 86, no. 8, pp. 4491–4493, Oct. 1999.

[45] Y.-J. Lin, Z.-D. Li, C.-W. Hsu, F.-T. Chien, C.-T. Lee, S.-T. Shao, and H.-C. Chang, "Investigation of degradation for ohmic performance of oxidized Au/Ni/Mg-doped GaN," Appl. Phys. Lett., vol. 82, no. 17, pp. 2817–2819, Apr. 2003.

[46] Z. Z. Chen, Z. X. Qin, Y. Z. Tong, X. D. Hu, T. J. Yu, Z. J. Yang, L. S. Yu, G. Y. Zhang, W. L. Zheng, Q. J. Jia, and X. M. Jiang, "Effects of oxidation by O_2 plasma on formation of Ni/Au ohmic contact to p-GaN," J. Appl. Phys., vol. 96, no. 4, pp. 2091–2094, Aug. 2004.

[47] D. Mistele, F. Fedler, H. Klausing, T. Rotter, J. Stemmer, O. K. Semchinova, and J. Aderhold, "Investigation of Ni/Au-contacts on p-GaN annealed in different atmospheres," J. Cryst. Growth, vol. 230, no. 3/4, pp. 564–568, Sep. 2001.

[48] T. Maeda, Y. Koide, and M. Murakami, "Effects of NiO on electrical properties of NiAu-based ohmic contacts for p-type GaN," Appl. Phys. Lett., vol. 75, no. 26, pp. 4145–4147, Dec. 1999.

[49] J. K. Sheu, Y. K. Su, G. C. Chi, W. C. Chen, C. Y. Chen, C. N. Huang, J. M. Hong,

Y. C. Yu, C. W. Wang, and E. K. Lin, “The effect of thermal annealing on the Ni/Au contact of p-type GaN,” J. Appl. Phys., vol. 83, no. 6, pp. 3172–3175, Mar. 1998.

[50] C.-S. Lee, Y.-J. Lin, and C.-T. Lee, “Investigation of oxidation mechanism for ohmic formation in Ni/Au contacts to p-type GaN layers,” Appl. Phys. Lett., vol. 79, no. 23, pp. 3815–3817, Dec. 2001.

[51] H. W. Jang, S. Y. Kim, and J.-L. Lee, “Mechanism for ohmic contact formation of oxidized Ni/Au on p-type GaN,” J. Appl. Phys., vol. 94, no. 3, pp. 1748–1752, Aug. 2003.

[52] J.-O. Song, D.-S. Leem, S.-H. Kim, J. S. Kwak, O. H. Nam, Y. Park, and T.-Y. Seong, “GaN-based light-emitting diodes with Ni–Mg solid solution/Au p-type ohmic contact,” Solid State Electron., vol. 48, no. 9, pp. 1597–1600, Sep. 2004.

[53] J.-O. Song, D.-S. Leem, and T.-Y. Seong, “Low-resistance and transparent ohmic contacts to p-type GaN using Zn–Ni solid solution/Au scheme,” Appl. Phys. Lett., vol. 84, no. 23, pp. 4663–4665, May 2004.

[54] K.-W. Kim, H.-G. Hong, J.-O. Song, J.-H. Oh, and T.-Y. Seong, “Low resistance and transparent Ni–Co solid solution/Au ohmic contacts to p-type GaN for green GaN-based LEDs,” Superlattices Microstruct., vol. 44, no. 6, pp. 735–741, Dec. 2008.

[55] S. H. Liu, J. M. Hwang, Z. H. Hwang, W. H. Hung, and H. L. Hwang, “Ohmic contact to p-type GaN using a novel Ni/Cu scheme,” Appl. Surf. Sci., vol. 212/213, pp. 907–911, May 2003.

[56] C.-F. Chu, C. C. Yu, Y. K. Wang, J. Y. Tsai, F. I. Lai, and S. C. Wang, “Low-resistance ohmic contacts on p-type GaN using Ni/Pd/Au metallization,” Appl. Phys. Lett., vol. 77, no. 21, pp. 3423–3425, Nov. 2000.

[57] D.-H. Youn, M. Hao, H. Sato, T. Sugahara, Y. Naoi, and S. Sakai, “Ohmic contact to p-type GaN,” Jpn. J. Appl. Phys., vol. 37, pt. 1, no. 4A, pp. 1768–1771, Jun. 1998.

[58] J.-O. Song, J. S. Kwak, Y. Park, and T.-Y. Seong, “Improvement of the light output of InGaN-based light-emitting diodes using Cu-doped indium oxide/indium tin oxide p-type electrodes,” Appl. Phys. Lett., vol. 86, no. 21, p. 213 505, May. 2005.

[59] K. L. Chopra, S. Major and D. K. Pandya, “Transparent Conductors—A Status

Review," Thin Solid Films, 102 (1983) 1-46, Dec. 1982.

[60] T. Minami, "Transparent conducting oxide semiconductors for transparent electrodes," Semicond. Sci. Technol., vol. 20, no. 4, pp. S35–S44, Apr. 2005.

[61] J.-S. Jang and T.-Y. Seong, "Low-resistance and thermally stable indium tin oxide ohmic contacts on strained p- $In_{0.15}Ga_{0.85}N$/p-GaN layer," J. Appl. Phys., vol. 101, no. 1, p. 013 711, Jan. 2007.

[62] J.-O. Song, D.-S. Leem, J. S. Kwak, Y. Park, S. W. Chae, and T.-Y. Seong, "Improvement of the luminous intensity of light-emitting diodes by using highly transparent Ag–indium tin oxide p-type ohmic contacts," IEEE Photon. Technol. Lett., vol. 17, no. 2, pp. 291–293,Feb. 2005.

[63] R.-H. Horng, D.-S. Wuu, Y.-C. Lien, and W.-H. Lan, "Low-resistance and high-transparency Ni/ITO ohmic contacts to p-type GaN," Appl. Phys. Lett., vol. 79, no. 18, pp. 2925–2927, Oct. 2001.

[64] S. W. Chae, K. C. Kim, D. H. Kim, T. G. Kim, S. K. Yoon, B. W. Oh, D. S. Kim, H. K. Kim, and Y. M. Sung, "Highly transparent and lowresistant ZnNi/indium tin oxide ohmic contact on p-type GaN," Appl. Phys. Lett., vol. 90, no. 18, p. 181 101, Apr. 2007.

[65] S. Y. Kim, H. W. Jang, and J.-L. Lee, "Effect of an indium-tin-oxide overlayer on transparent Ni/Au ohmic contact on p-type GaN," Appl. Phys. Lett., vol. 82, no. 1, pp. 61–63, Jan. 2003.

[66] Ho Won Jang, Jong Kyu Kim, Soo Young Kim, Hak Ki Yu, and Jong-Lam Lee, "Ohmic contacts for high power LEDs," phys. stat. sol. (a) 201, No. 12, 2831–2836, Jul. 2004.

[67] J.-O. Song, J. S. Kwak, Y. Park, and T.-Y. Seong, "Improvement of the light output of InGaN-based light-emitting diodes using Cu-doped indium oxide/indium tin oxide p-type electrodes," Appl. Phys. Lett., vol. 86, no. 21, p. 213 505, May 2005.

[68] J.-O. Song, K.-K. Kim, H. Kim, Y.-H. Kim, H.-G. Hong, H. Na, and T.-Y. Seong, "Formation of low-resistance and transparent indium tin oxide ohmic contact for high-brightness GaN-based light-emitting diodes using a Sn–Ag interlayer," Mater. Sci. Semicond. Process., vol. 10, no. 4/5, pp. 211–214, Aug.–Oct. 2007.

[69] Ya-Ju Lee, Shawn-Yu Lin, Ching-Hua Chiu, Tien-Chang Lu, and Hao-Chung Kuo, "High output power density from GaN-based two-dimensional nanorod light-emitting diode arrays," Applied Physics Letters, vol. 94, no. 14, pp. 141111, April 2009.

[70] M. V. Malyshev, V. M. Donnelly, A. Kornblit, and N. A. Ciampa, "Percent dissociation of Cl_2 in inductively coupled, chlorine-containing plasmas," J. Appl. Phys., vol. 84, no. 1, pp. 137–146, April 1998.

[71] J.L. Weyher, S. Miiller, I. Grzegoryh, and S. Porowski, "Chemical polishing of bulk and epitaxial GaN," Journal of Crystal Growth, vol. 182, pp. 17-22, April 1997.

[72] Vasily N. Bessolov, Elena V. Konenkova, and Mikhail V. Lebedev, "Sulfidization of GaAs in alcoholic solutions: a method having an impact on efficiency and stability of passivation," Materials Science and Engineering, vol. B44, pp. 376-379, 1997.

[73] Vasily N. Bessolov, Elena V. Konenkova, and Mikhail V. Lebedev, "Solvent effect on the properties of sulfur passivated GaAs," J. Vac. Sci. Technol. B, vol. 14, no. 4, pp 2761-2766, April 1996.

[74] Dieter K. Schroder, **Semiconductor Material and Device Characterization**, 3rd ed, Arizona State University, Tempe, AZ, 2006.

[75] Jong-Lam Lee, Jong Kyu Kim, Jae Won Lee, Yong Jo Park, and Taeil Kim, "Effect of surface treatment by KOH solution on ohmic contact formation of p-type GaN," Solid-State Electronics, vol. 43, pp. 435-438, July 1998.

[76] Shui-Hsiang Su, Cheng-Chieh Hou, Meiso Yokoyama, Ruei-Shiang Shieh, and Shi-Ming Chen, "Temperature effect on the optoelectronic properties of GaN-based light-emitting diodes with ITO p-contacts," Journal of The Electrochemical Society, vol. 154 , no. 5, pp. J155-J158, Mar. 2007.

[77] Gregory S. Marlow and Mukunda B. Das, "The effects of contact size and non-zero metal resistance on the determination of specific contact resistance," Solid State Electronics, vol. 25, no. 2, pp. 91-94, August 1981.

[78] Hyun Kyong Cho, Sun-Kyung Kim, and Jeong Soo Lee, "An improved non-alloyed ohmic contact Cr/Ni/Au to n-type GaN with surface treatment," J. Phys. D: Appl. Phys. vol. 41, pp. 175107, June 2008.

[79] Chul Huh, Sang-Woo Kim, Hyun-Min Kim, Dong-Joon Kim, and Seong-Ju Park, "Effect of alcohol-based sulfur treatment on Pt Ohmic contacts to p-type GaN," Appl. Phys. Lett., vol. 78, no. 13, pp. 4591–4593, Jan. 2001.

[80] Se-Yeon Jung, Tae-Yeon Seong, Hyunsoo Kim, Kyung-Soo Park, Jae-Gwan Park, and Gon Namgoong, "Electrical Properties of Ti/Al Ohmic Contacts to Sulfur-Passivated N-Face n-Type GaN for Vertical-Structure Light-Emitting Diodes ," Electrochemical and Solid-State Letters, vol. 12, no. 7, pp. H275-H277, May, 2009.

[81] Jong Kyu Kim, Jong-Lam Lee, Jae Won Lee, Yong Jo Park, and Taeil Kim, "Effect of surface treatment by $(NH_4)_2S$ solution on the reduction of ohmic contact resistivity of p-type GaN," J. Vac. Sci. Technol. B, vol. 17, no 2, pp. 497-499, Mar/Apr 1999.

[82] Chul Huh, Sang-Woo Kim, Hyun-Soo Kim, In-Hwan Lee, and Seong-Ju Park, "Effective sulfur passivation of an n-type GaN surface by an alcohol based sulfide solution," J. Appl. Phys., vol. 87, no. 9, pp 2640-2642, Jan. 2000.

[83] Yuh-Hwa Chang, Yen-Sheng Lu, Yu-Liang Hong, Cheng-Tai Kuo, and Shangjr Gwo, and J. Andrew Yeh, "Effects of $(NH_4)_2Sx$ treatment on indium nitride surfaces,"

J. Appl. Phys., vol. 107, pp 043710, Feb. 2010.

[84] H. Sik, Y. Feurprier, C. Cardinaud, G. Turban, and A. Scavennec, “Reduction of recombination velocity on GaAs surface by Ga-S and As-S bond-related surface states from $(NH_4)_2S$ treatment,” J. Electrochem. Soc., vol. 144, no. 6, pp. 2106-2114, June 1997.