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ON THE ATOMIC SCALE DEFECTS INVOLVED IN THE NEGATIVE BIAS TEMPERATURE INSTABILITY IN 4H-SiC MOSFETs

A Thesis in

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by

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ABSTRACT

We utilize electrically detected magnetic resonance (EDMR) to explore the effects of the negative bias temperature instability (NBTI) in 4H-SiC metal oxide semiconductor field effect transistors (MOSFETs). EDMR spectra due to oxygen vacancies, or E' defect centers are generated in p-channel MOSFETs under elevated temperatures and modest negative gate bias stressing. The E' concentration is shown to increase in response to increasing stress temperature. Our use of in-situ EDMR stress measurements suppresses recovery contamination and shows that the NBTI generated E' centers disappear upon temperature stress removal. No such defect appears under the same stressing conditions for comparably-processed n-channel MOSFETs. In both types of devices, the silicon vacancy is the dominating central defect detected by EDMR, though this defect appears independent of and is unchanged by the NBTI stressing conditions. We conclude that E' precursor sites at or very near the oxide/semiconductor interface in 4H-SiC pMOSFETs are activated under the negative bias temperature instability. Such defects may lead to large threshold voltage shifts and greatly reduced carrier mobility observed in the SiC/SiO_2 system.

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LIST OF ABBREVIATIONS

BAE	bipolar amplification effect
CVD	chemical vapor deposition
D_{IT}	interface state density
E_C	energy of conduction band
E_T	energy of trap level
E_V	energy of valence band
EDMR	electrically-detected magnetic resonance
EPR	electron paramagnetic resonance
GE	General Electric
HC	hot carrier
I_B	body current
I_D	drain current
I_{SD}	source/drain current
L_{CH}	channel length
L_{Diff}	diffusion length
MOSFET	metal-oxide-semiconductor field-effect-transistor
N_F	fixed charge
N_{IT}	interface traps
N_M	mobile ions
N_{OT}	oxide traps
NBTI	negative bias temperature instability
NO	nitric oxide
N_2O	nitrous oxide
SDR	spin dependent recombination
Si	silicon
SiC	silicon carbide
SNR	signal-to-noise ratio
V_T	device threshold voltage
V_F	forward bias
VLSI	very-large-scale integration

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Chapter 1 – Introduction

From communication and transportation to space exploration and beyond, most electronics depend on the ever-evolving transistor for its fast switching operation and reliability. Presently, the industry is dominated by the silicon (Si) based metal-oxide-semiconductor field-effect transistor (MOSFET), but the incorporation of new semiconducting materials in devices increasingly aspires to replace Si where it is not aptly suited. Silicon carbide (SiC) based electronics are being developed for the high-temperature, high-power, and high-radiation environments under which conventional Si semiconductor operation is limited. While SiC is not drastically different in atomic structure from Si and because both Si and SiC thermally form a similar native oxide [silicon dioxide (SiO_2)], SiC is somewhat able to borrow some of the processing techniques that have brought Si its tremendous success. In other cases, however, apparent differences in oxide quality and processing currently disallow SiC from demonstrating its full potential. Improving SiC device processing has been a large focus in the scientific community because of SiC's vast reliability compared to Si when used in more extreme operating environments.

SiC MOS technology is less efficient than Si because of its poor oxide quality and considerably imperfect interface region between semiconductor and oxide. The rough interface of SiC/SiO_2 primarily acts to reduce the effective channel mobility, which is typically less than 100 cm^2/V-s, thereby reducing the MOSFET's gain and ability to effectively carry current. Coupled with a coarse surface, SiC's poor oxide quality renders the device more susceptible to harmful threshold voltage (V_T) shifts and gate leakages than comparable Si devices. On an atomic level, such problems can be attributed to the overwhelming presence of interface state densities; fixed oxide charges; and charge carrier trapping, tunneling, and scattering. While these material issues were

first discovered and, in many cases, reduced in Si technology, their presence in SiC has yet to be reasonably controlled. Furthermore, the biggest reliability issue in Si technology, the negative bias temperature instability (NBTI), has reared itself again with even more drastic consequences for SiC. As is the case for Si, SiC devices under the negative bias and high temperature conditions of NBTI exhibit channel mobility degradation, increased leakage currents, and unreasonable V_T shifts that vehemently disable switching operation of sensitive circuits. While somewhat improved upon but still unresolved in Si, far less is known about these problems in SiC. For devices that aim to operate in high temperature and high power environments, NBTI-induced effects of this magnitude are rather unaccommodating.

In this work, we utilize electrically detected magnetic resonance (EDMR), a device-oriented variation of electron paramagnetic resonance (EPR) to study the atomic-scale defects involved with NBTI in the SiC/SiO_2 system. The objective of the experiment is to measure (in-situ) the spin-dependent recombination (SDR) current of SiC lateral MOSFETs while stressed at high temperatures and modest oxide fields. In the past, defining the roles of various NBTI-induced defects has proven difficult because much of the damage recovers shortly after the stress is removed. Capturing such recovery through conventional characterization techniques usually requires bias sweeping or bias interruption, both of which obscure the activity and representation of the active defects. Our strategy is favorable in that no interruption or alteration in gate-bias is made to measure the SDR current. We suppress defect recovery contamination while probing the NBTI generated, atomic-scale defects responsible for device performance degradation.

This work represents a contribution to the understanding of NBTI effects in SiC devices. It is hoped that this work will help to facilitate improved device processing that can reduce or eliminate the performance limiting effects of NBTI. Our results are reminiscent of the NBTI-

induced defects observed in the Si/SiO_2 system, though this is the first study to report the presence of NBTI generated E' activation in SiC pMOSFETs.

Chapter 2 – Background

Silicon carbide is a material of interest for modern electronic devices. Its ability to function under high temperature and high power environments can enable drastic improvements to a wide range of applications and systems [1]. These improvements include, amongst many others, high-voltage switching for public power distribution [2], higher-rated controls and sensors for more fuel-efficient aircraft and automotive engines, and more robust microwave electronics for satellite, radar, and communication systems [3]. Also, due to its large band gap (~3eV) and low intrinsic carrier concentration, SiC is an exceptional candidate for use as a semiconducting material in modern diode rectifiers and power MOSFETs. In the particular realm of power devices, operation above 600°C has been demonstrated [4], and commercially available SiC power MOSFETs are already rated for use at (as high as) 100 Amperes at 1200 Volts blocking voltage [5]. The harsh nature of these conditions well exceeds those in which corresponding silicon devices are able to perform, though many issues still prevent SiC transistors from reaching their theoretical advantages. The most recognized challenge, thus far, has been creating a SiC/SiO_2 interface with a tolerable interface state density (D_{IT}), as noted in [6]. Interface states have a very large corresponding effect on what is perhaps the most inhibiting reliability issue in Si based pMOSFET operation: the negative bias temperature instability (NBTI). Because SiC and Si share the same natural oxide (SiO_2) and it is defects in this oxide and at the semiconductor/oxide interface largely responsible for NBTI in Si, it invites the question whether NBTI is also of concern in SiC.

This chapter surveys important material parameters of SiC, some basic concepts of MOSFET operation, and comparisons between NBTI related issues identified in both Si and SiC.

2.1 Silicon Carbide

The existence of a silicon-carbon bond was first proposed as early as 1824 by Jöns Jacob Berzelius [7]. It was not until 1903, however, that chemical analysis of an ancient meteorite led to the discovery of the natural mineral *Moissanite* (SiC) [8]. Moissanite is believed to have existed well before the birth of our solar system – a galactic traveler generated in carbon rich atmospheres of red giant stars and ancient supernova remnants. SiC grains are said to have been trapped in meteorites that were materializing from the deposits of cloud debris during the massive gravitational formation of our solar system [8]. A synthetic form of silicon carbide was realized and used as an abrasive just slightly before this discovery. In 1893, Edward Acheson patented a resistance furnace which was used to heat coke and silica to form a synthesis of carbon and corundum (Al_2O_3), what he termed as *Carborundum.* [9]. Having an extremely high hardness on *Moh's Scale* (9.2-9.5), SiC began to be mass-produced for use in the abrasives industry. While abrasives remain SiC's main commercial application, single-crystalline semiconducting substrates of SiC were grown via sublimation [10] in 1955 (Lely process), marking its induction as a candidate for use in semiconductor devices.

Most of the beneficial intrinsic electrical properties of SiC have been known for many years and at the advent of the semiconductor electronics age, SiC was first considered a promising material candidate for early transistors. However, one important prerequisite for mass-production of transistors includes wafer reproducibility in terms of size and quality [1]. The crystallization studies of Jan Czochralski in 1916 accidentally led to the invention of a revolutionary growth technique (Czochralski process) that provides pure and reproducible, high-quality wafers [11]. This method, which employs the use of a seed crystal on which a semiconducting material is melted and recrystallized, provides very pure crystalline substrates for commonly used

semiconductor materials such as silicon, germanium, and gallium arsenide (GaAs). SiC, on the other hand, sublimes rather than melting at reasonable pressures and thus cannot be formed under such growth techniques. It is this obstacle that prevented the use of SiC for semiconductor substrates in electronic devices until the 1980's [1]. Furthermore, as SiC was neglected for its irreproducibility and poor crystalline quality, Si was quickly becoming the leading material for nearly all transistor technology and saw many years of commercial process refinement while SiC fell by the wayside.

Eventually, modifications to the Lely and Acheson processes involving heating in graphite crucibles resulted in larger and better quality SiC crystal growth [12] and even further advancements via chemical vapor deposition (CVD) provide for most of the substrates used in device manufacturing today [13]. In simple terms, SiC CVD involves heating a SiC substrate in a chamber under flowing carbon and silicon containing gases. The gases decompose and deposit onto the wafer which allows the growth of a well-ordered SiC epilayer. This growth process is normally carried out at temperatures between 1400 and 1600°C and at pressures between 0.1 and 1 atmosphere, resulting in a growth rate on the order of ~1mm/hr [14].

Still, shortcomings in crystal quality due to undesirable crystalline defects have largely stalled the progress of SiC electronics research and the realization of SiC's hypothetical advantages for use in semiconductor electronics. In broad terms, eliminating stoichiometric defects in SiC crystals such as edge, screw, and basal plane dislocations has proven especially difficult [15]. Of highest interest to this research are the defects located at the SiC/SiO_2 interface, which may perpetuate, both, from these crystal defects and from otherwise common device fabrication methods. The bonding arrangement at the lattice-mismatched interface typically provides inherent defects and the most likely candidates for defect precursors that can be activated under

certain circumstances, such as device operation at conditions similar to those applied in NBTI stressing. The point of this research is to uncover the defect(s) specifically involved with NBTI-induced degradation in SiC MOS transistors in hopes to foster an atomic-level understanding of and project ideas to reduce or eliminate such precursor sites. *If a more reliable SiC/SiO_2 interface can be realized and NBTI can be controlled, SiC may soon be able to provide advantages over Si for reliable operation in high-temperature and high-power applications.*

2.1.1 Crystal Structure

There are over 250 known crystal structures for SiC, each differing in their Si-C bilayer stacking sequence. While these structures all consist of 50% carbon atoms and 50% silicon atoms, each polytype exhibits distinct electrical semiconductor properties. In terms of manufacturing reproducible and acceptable substrates, only a few of these polytypes are able to be used as electronic semiconductors: 3C-SiC, 4H-SiC, and 6H-SiC. 3C-SiC, sometimes referred to as β-SiC, is the only polytype with a cubic lattice crystal structure. The non-cubic polytypes are referred to as α-SiC; among the other various crystal structures, 4H and 6H-SiC are the only two polytypes with hexagonal symmetry [1]. Because various electrical properties are anisotropic with respect to crystallographic orientation, it is important to consider further the bilayers of these polytypes and how they may affect semiconductor device operation.

Each bilayer can be considered as a single layer of silicon atoms coupled to a single layer of carbon atoms. The planar sheet formed by a given bilayer is termed the basal plane, and the crystalline c-axis, or the [0001] direction, is defined as normal to the bilayer plane. The various bilayer stacking sequences of the 3C, 4H, and 6H polytypes are illustrated in Figure 2.1.

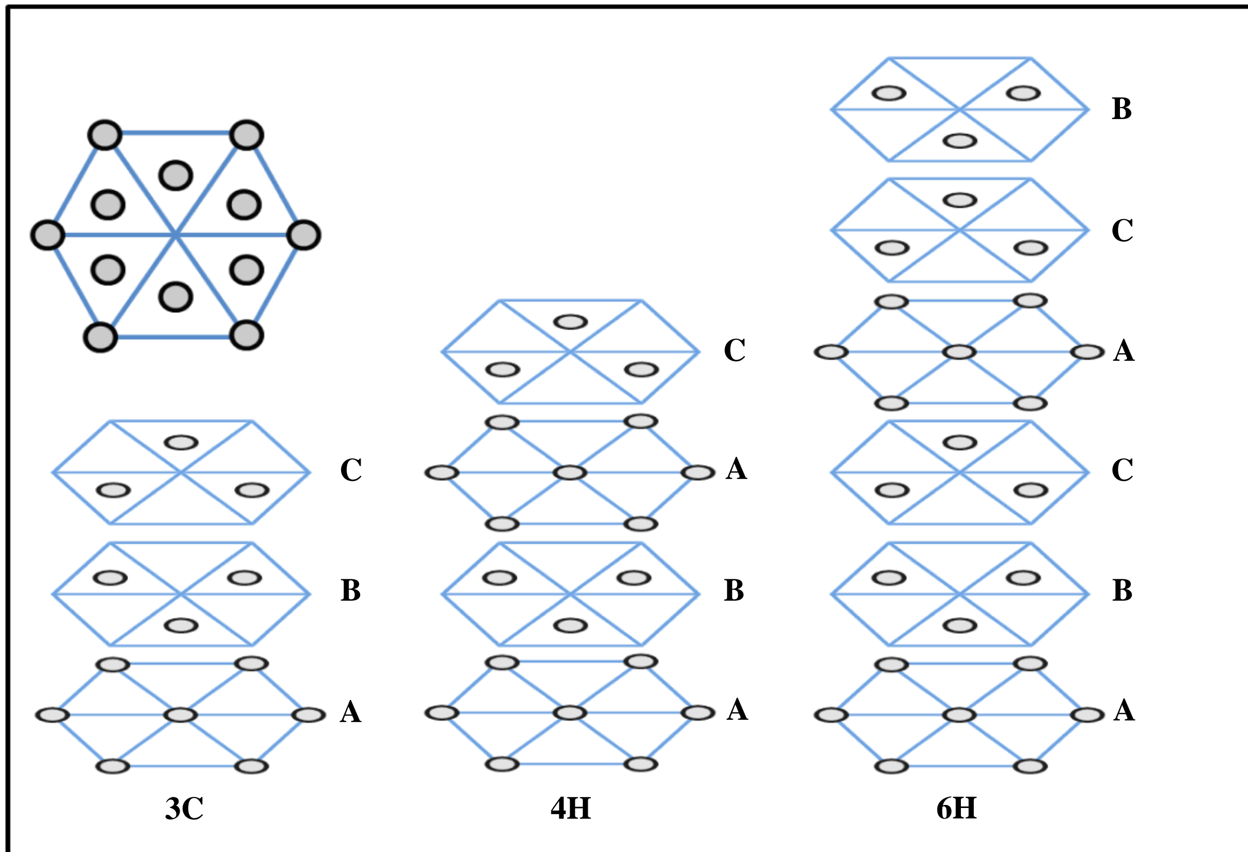

Figure 2.1: Bilayer stacking sequences for 3C-, 4H-, and 6H-SiC polytypes. Note: Only silicon atoms are shown. The silicon atoms have tetrahedral coordination; each is covalently bonded to four carbon atoms.

As shown, it requires 3, 4, or 6 bilayers to define a unit cell along the c-axis for the respective 3C, 4H, and 6H polytypes. Such stacking provides distinct faces for SiC, marking it as a polar semiconductor, in that, normal to the c-axis, one surface is terminated with silicon atoms (Si-face) and the opposite end with carbon atoms (C-face) [16]. For several reasons discussed in the next section, most SiC semiconductor devices are of the 4H polytype and nearly all devices, because of its better stability for 4H growth, are grown on the C-face. That is, growing from a 4H-SiC seed atop the C-face results in successful homoepitaxial growth with strict 4H structure propagation. It has been observed that growth atop the Si-face seed often results in a switching

from the 4H to 6H polytype [17]. All of the devices measured in this study are of the 4H polytype and are grown on the C-face of the SiC substrate.

Regarding this study, one of the most important facets of SiC crystallography is the growth of its native oxide. Like silicon, SiC will form a thermal SiO_2 oxide under sufficient heating in an oxygen rich environment. This permits SiC device technology to adopt and implement some of the successful advancements made in the Si/SiO_2 system, but differences in oxide quality and device processing again limit SiC MOSFETs from reaching their full potential. Inadequacies in the quality of the oxide and SiC/SiO_2 interface provide for an unacceptably higher number of charge traps and interface states than in Si/SiO_2. Charge traps are accountable for the onset of free-carrier Coulombic scattering which is shown to drastically reduce the effective channel mobility [18]. This is known to severely limit transistor gain and current-carrying capabilities [1]. Such interface traps and near-interface oxide traps are also known to cause significant shifts in the ideal threshold voltage and proliferations in gate-leakage currents [18]. Short order changes in V_T can especially occur from filling and emptying said traps via gate bias stressing, a topic of concern to this study. Also of concern, particularly because of its impediments under NBTI, is the manifestation of mobile ion impurities within the poor-quality gate oxide [18]. The implications of these harmful deficiencies with respect to NBTI are discussed in later sections.

From a crystallographic standpoint, many of these interface states and charge traps likely result from off-angle polishing-induced surface roughness (Figure 2.2), step-bunching during homoepilayer growth, and the presence of carbon species that are incorporated into the growing SiO_2 film [19]. Though most of the carbon from the SiC converts to gaseous species and escapes during thermal oxidation, trace amounts near the interface have proven detrimental to oxide electrical quality [20]. Often, annealing steps usually involving nitric- or nitrous-oxide (NO or

N_2O, respectively) are incorporated after thermal oxide growth to favorably passivate dangling bonds or reduce trap centers. Such anneals typically decrease interface traps, but they have also been shown to intensify the damaging effects of NBTI (in the Si/SiO_2 system, for example) [21]. Other improvements have been achieved, however, through the use of deposited oxides. Sridevan *et al.* have shown large increases in channel carrier mobility through the use of thick deposited gate oxides [22]. Agarwal *et al.* have made interesting arguments about the future of insulators on SiC substrates. They have pointed out that SiC's wide band gap acts to reduce the potential barrier encountered by charge carriers which will ultimately result in an increase in more harmful oxide tunneling processes. They claim that a perfect thermally grown oxide on atomically seamless SiC would still be less reliable than Si thermal oxides [23]. It is possible, if not probable, that SiC may eventually see the incorporation of alternative gate-insulators for full realization of high-power and high-temperature advantages. In the interim, a better understanding of interface states and trapping centers in SiC/SiO_2 can help to improve the current SiO_2 oxide based-device processing. *Understanding the evolution of the Si/SiO_2 system can help to predict issues that might be expected in the chemically similar SiC/SiO_2 system. This thesis investigates the defects associated with SiC and SiO_2 as they relate to NBTI and attempts to understand their correlations and differences to provide helpful insight for improving current SiC device technology.*

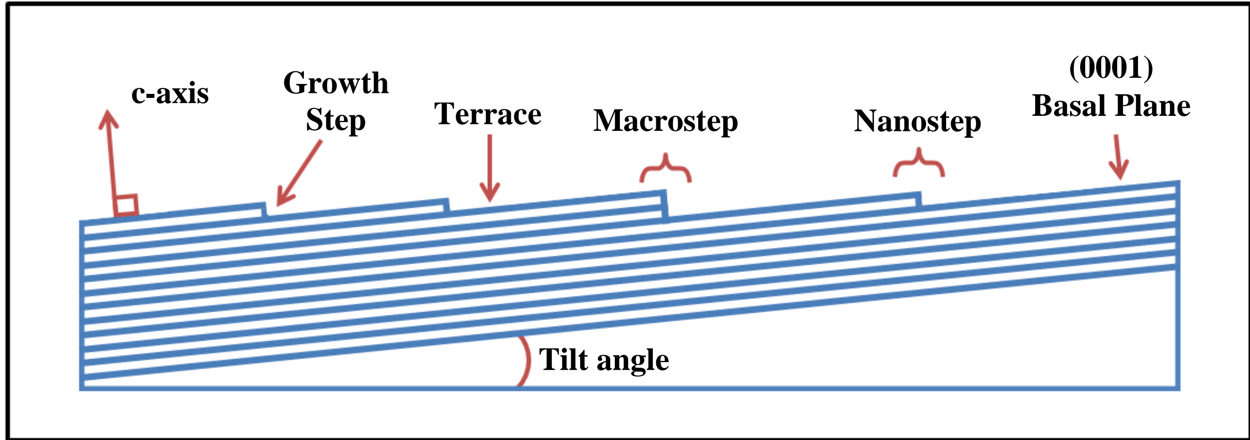

Figure 2.2: Cross-sectional illustration of "off-axis" polished SiC showing surface roughness via step bunches. Devices are typically grown on a surface which is a few degrees off-axis. Adapted from [16] [24].

2.1.2 Electrical Properties

As previously mentioned, the objective for SiC (as a semiconductor material) is to reliably perform in high temperature and high-power applications. Its abilities to do this result from some of SiC's unique material properties [25] [26].

The ability for SiC to perform at high temperatures is due to its low intrinsic carrier concentration, n_i (a result of its relatively large bandgap, E_g). In an intrinsic semiconductor, the intrinsic carrier concentration is the concentration of carriers that are thermally excited across the bandgap and thus enabled to partake in conduction. This, for example, can be considered the concentration of electrons in the conduction band. This quantity is also equal to the concentration of holes that, as a result, were created and left behind in the valence band. The intrinsic carrier concentration and bandgap are related as a function of temperature via

$$n_i = \sqrt{N_c N_v} \exp\left[\frac{-E_g}{2kT}\right], \tag{2.1}$$

where N_c and N_v are the effective density of states in the conduction and valence band, respectively, and k is Boltzmann's constant. From this relationship, two important trends are noted:

(1) At constant temperature, larger bandgap materials have lower intrinsic carrier concentrations, i.e. fewer carriers can be excited across a larger bandgap

(2) At constant bandgap energy, increasing temperature results in an exponentially increasing intrinsic carrier concentration, i.e. increasing the temperature of the system promotes increased thermal excitation of carriers

Semiconductor devices are usually operated in temperature ranges where conductivity is controlled not by intrinsic carriers but rather by intentionally added dopant impurities [25]. With increasing temperature, device operation suffers and is eventually overcome by unacceptable conductivity control as the intrinsic carrier concentration begins to exceed the intentional doping concentration. In most Si devices, a relatively large intrinsic carrier concentration influences such conductivity and limits device operation to junction temperatures of about 300°C [1]. Because SiC has a much larger bandgap and thus much lower intrinsic carrier concentration, it can withstand much higher temperatures before uncontrolled conductivity becomes an issue. SiC theoretically permits reliable operation and conductivity control at temperatures exceeding 800°C.

In conjunction with SiC's relatively large bandgap, its high thermal conductivity and high breakdown field also allow operation under high power densities. Particularly, the high breakdown field enables a thinner and heavier-doped blocking voltage region. This results in a drastic decrease in the blocking region resistance, R_D, as shown for a typical power DMOSFET

in Figure 2.3 [27]. SiC's high breakdown field and large bandgap predominantly allow much faster switching times than in comparably rated silicon switching devices, thereby enabling them to operate at a faster switching frequency with greater efficiency, i.e., with less switching energy loss. The switching energy loss of a device is reflected by the amount of time required for the device to stop flowing current once a bias has been applied to turn the device off. Reducing switching energy loss permits the use of relatively smaller components that can help to reduce the total system size and weight [1]. Furthermore, the high thermal conductivity of SiC allows for more efficient removal of heat energy generated by the active device. SiC's ability to operate at high temperatures permits a reduction or, possibly, an elimination of the precautions taken to cool devices and keep them from overheating and thus offers even greater reductions in the system size [1].

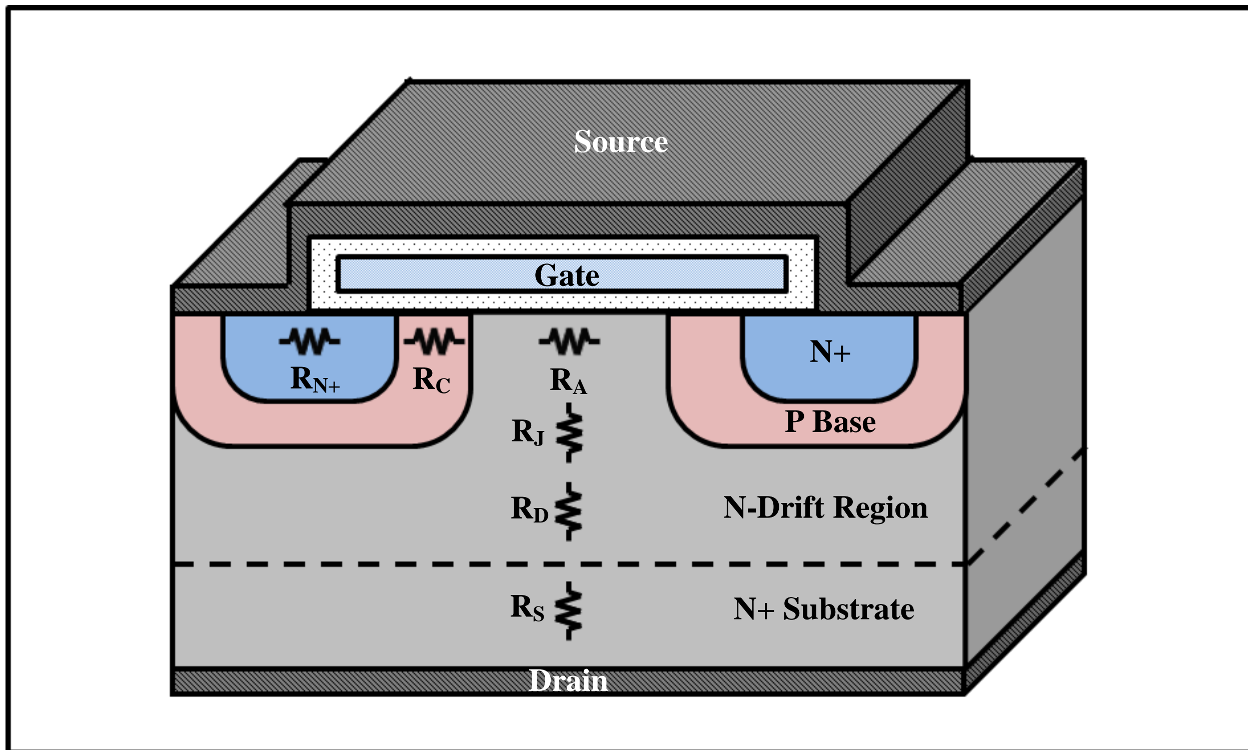

Figure 2.3: A schematic illustration of a power DMOSFET showing the various internal resistances. R_{N+} is the resistance from the N+ sources diffusion, R_C the channel resistance, R_A the accumulation layer resistance, R_J the resistance from p base pinch off, R_D the drift region resistance, and R_S the substrate resistance. Adapted from [27].

Some of the discussed electrical properties of SiC are compared against those of the more common Si and GaAs semiconductor materials and highlighted in Table 2.1. From this information, it can also be seen that 4H-SiC has many natural advantages over other SiC polytypes, which is why it is the polytype of choice for SiC device fabrication. It is the polytype with the largest bandgap (and therefore lowest n_i) and thus the most reliable candidate for high temperature device performance. When compared to 6H-SiC, its substantially higher carrier mobility is also a significant advantage, provided device processing and cost issues are roughly equal. The mobility anisotropy of 6H-SiC make it a poor candidate for vertical power devices, perhaps some of the most significant device structures for SiC [1].

Property	Silicon	GaAs	3C-SiC	4H-SiC	6H-SiC
Bandgap (eV)	1.12	1.43	2.3	3.2	3.0
Intrinsic Carrier Concentration at 300K (cm^{-3})	10^{10}	1.8×10^{6}	10	10^{-7}	10^{-5}
Thermal Conductivity (W/cm-K)	1.5	0.5	3 – 5	3 – 5	3 – 5
Breakdown Field at $N_D = 10^{17} cm^{-3}$ (MV/cm)	0.6	0.6	> 1.5	‖c-axis: 3.0	‖c-axis: 3.2 ⊥c-axis: > 1
Electron Mobility at $N_D = 10^{16} cm^{-3}$ (cm^2/V-s)	1200	6500	750	‖c-axis: 800 ⊥c-axis: 800	‖c-axis: 60 ⊥c-axis: 400
Hole Mobility at $N_A = 10^{16} cm^{-3}$ (cm^2/V-s)	420	320	40	115	90

Table 2.1: Electrical properties of SiC and other semiconductor materials

2.2 The Metal-Oxide-Semiconductor Field-Effect-Transistor

The metal-oxide-semiconductor field-effect-transistor (MOSFET) is currently the cornerstone of integrated circuit design. Its relatively small size allows billions of devices to be fabricated into a single integrated chip. Presently, silicon is the basis for most transistor technology as it provides a convenient native oxide and is one of the most abundant elements in the Earth's crust, second only to oxygen. The process refinements for developing Si MOSFETs have spanned now around 60 years, which brings us to two important points:

(1) The Si/SiO_2 interface has been nearly perfected. There are very few interfacial defects and though having several times redefined the theoretical limitations, we are now rapidly approaching atomic scale processing.

(2) Silicon has its boundaries. A demand for more robust devices to operate in harsh environments signals for a new and more suitable technology.

SiC MOSFETs are great candidates for such demands, though it must be noted that they, while still in early developmental stages, possess many issues preventing them from full commercialization. It is worth noting, however, that Si MOSFETs faced many similar developmental challenges that required extensive research and developmental implementations to overcome. A brief review of the MOSFET will help to better understand the measurements contained herein.

Following from Figure 2.4, the majority of the device is comprised of the substrate. This is usually doped to be either n-type (for p-channel devices) or p-type (for n-channel devices) via the incorporation of intentional dopant impurities, normally elements having one less (acceptors) or one more (donors) valence electron. Imbedded into the substrate are the source drain regions, which are also doped but of opposite carrier type. The gate oxide and gate complete the basic structure of a lateral MOSFET. Both an n-channel MOSFET (nMOS) and p-channel (pMOS) are also illustrated in Figure 2.4.

The operation of the MOSFET, as inferred by its name, is based on the field-effect. This involves using a gate voltage to induce a field across the insulating oxide for selective control of the channel region. The channel region is situated between the source and drain, particularly located in the semiconductor side of the interface region between the oxide and semiconductor.

The gate can be used to invert the carrier concentration in the MOSFET channel region to promote current flow from source to drain. The device can also be biased with opposite gate polarity to accumulate charge of the majority type and prevent current flow. In this sense, the MOSFET is essentially configured as a bias-controlled switch. The bias at which the switch can be turned on is often considered to be the threshold voltage.

Relevant to this work, the threshold voltage is of greatest concern as its changes under NBTI create one of the largest hindrances in the advancement of power MOSFETs. Threshold voltage instability, as well as the observed reduction in charge carrier mobility, is considered a result of interface states and oxide traps that exist at the interface between the oxide and semiconductor. Such defects are either inherent in the material or created during fabrication. Regardless, their function in disrupting current flow and trapping charge that could otherwise be used for conduction drastically reduces device efficiency. Understanding these defects in the SiC/SiO_2 system is the specific aim of this work.

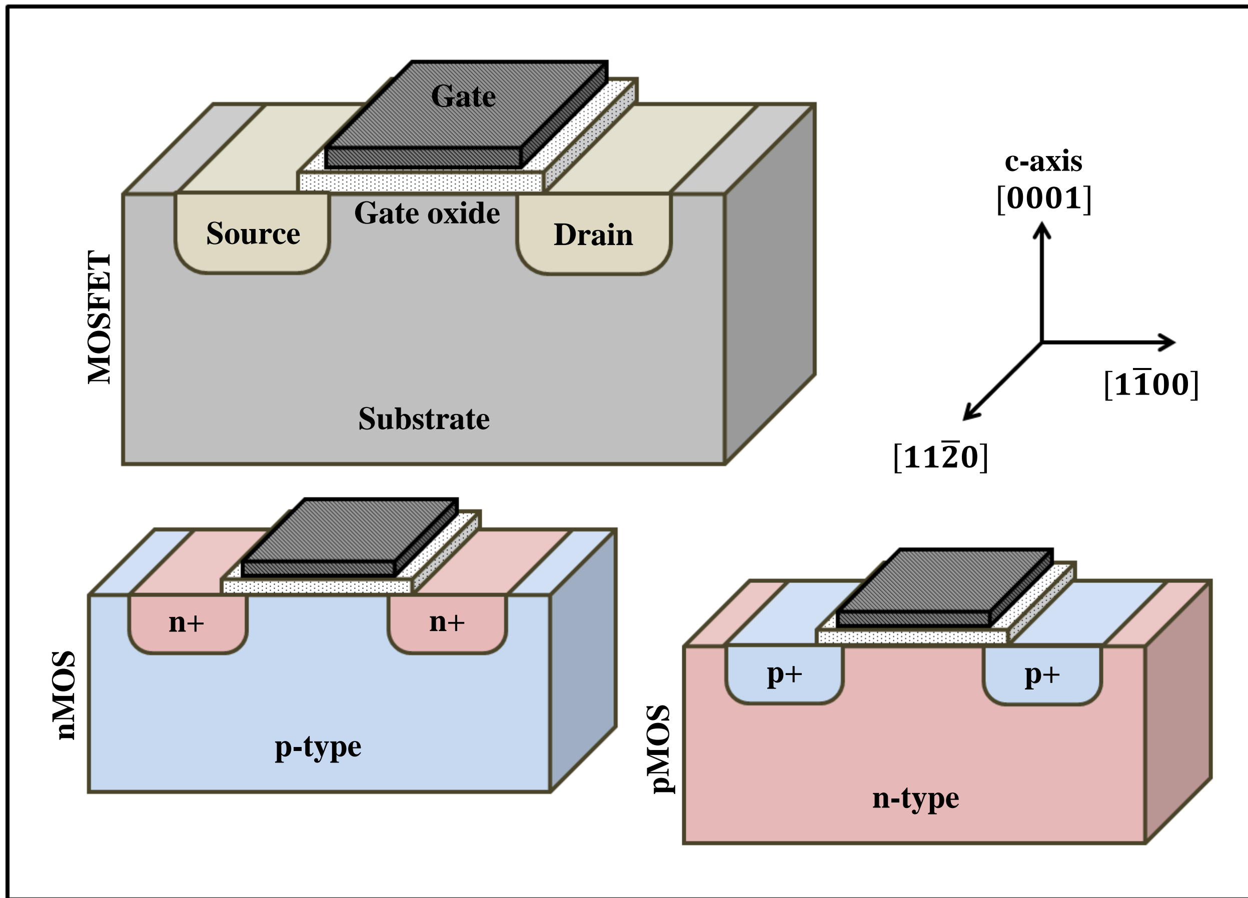

Figure 2.4: A schematic illustration of the lateral MOSFET. A basic MOSFET is shown to illustrate the various regions of the device, and both an nMOS and pMOS transistor is shown to illustrate the respective doping of the device regions.

2.3 The Negative Bias Temperature Instability

The negative bias temperature instability (NBTI) is commonly observed in silicon-based pMOSFETs when stressed under negative gate voltages and elevated temperatures. NBTI manifests itself through V_T shifts, channel mobility degradation, and drain current reduction [6] and is generally attributed to positive oxide charge and interface trap generation [28] [29]. Typical stress temperatures range from 100-150°C with oxide electric fields usually below 6 MV/cm, i.e., fields less than those responsible for hot carrier degradation [30]. NBTI usually occurs during the “on” state of the device, or when the semiconductor is sufficiently inverted at

the interface to allow channel conduction. While it has been shown that either negative gate bias or elevated temperature alone can produce NBTI, a stronger and faster effect results from their combination. In silicon, NBTI primarily occurs in *p*-channel MOSFETs under a negative gate bias, but appears inconsequential under positive bias and inconsequential under either negative *or* positive bias in *n*-channel MOSFETs [31]. Such instability may lead to timing shifts in integrated circuit technology, an especially problematic event for complementary MOSFETs (CMOS). CMOS implements parallel *p* and *n* channel devices as logic gates for drastic reduction in switching losses. If certain mismatches exceed a specified tolerance, asymmetric deviation in turn-on voltage and degradation in timing paths from either device can lead to malfunction of time and power sensitive logic circuits. While certain fabrication techniques can skirt or minimize the harmful effects of such degradation, there exists a tradeoff that will likely compromise other important design parameters such as operating power, noise margins, and valuable chip area.

While NBTI is yet to be fully understood in the Si/SiO_2 system, considerably less is known about its presence in the SiC/SiO_2 system. Some of the observed effects of NBTI in SiC are reminiscent of those observed in Si, offering early counsel for encountered and expected SiC device problems. Still other issues must be treated with caution as the newer SiC technology works its way through other complications not immediately correlated with other semiconductor developmental accomplishments. This section briefly surveys the history of NBTI in both the Si/SiO_2 and SiC/SiO_2 systems.

2.3.1 NBTI in the Si/SiO_2 System

NBTI was considered important fairly early in the history of Si-based semiconductor devices. Deal *et al.* theorized that problems at the semiconductor/oxide interface were the reason they

observed positive charge build up when stressing devices at high temperature and negative biases [32]. Similar experiments performed by Jeppson *et al.* led them to their early reaction-diffusion model which proposed that the dissociation of a Si-H bond at the interface resulted in the creation of an interface state, oxide charge, and hydroxyl group [33]. Jeppson noted that such damage was slowly recoverable upon removal of stress.

For the next several years, the adoption of NBTI-resistant nMOS technology naturally slowed the research and concern of NBTI. In the late 1980's, however, digital logic circuits began to incorporate complimentary n-channel and p-channel devices (CMOS) for improvements in switching frequency and reductions in power consumption. These considerations and the added benefit of a reduction in required chip space resulted in the nearly immediate implementation of CMOS in very-large-scale integration (VLSI) devices [34] . The reintroduction of pMOS technology reminded the community of the earlier NBTI-induced reliability issues and resurged research efforts to reduce their harmful effects.

Earlier magnetic resonance studies utilizing spin dependent recombination (SDR) [35] and EPR [36] have helped to quantify NBTI in the Si/SiO_2 system and project possibilities for it in SiC/SiO_2. Campbell *et al.* have reported NBTI to be dominated by Si/SiO_2 interface traps known as P_b centers [35]. The results concerning E' generation were considered tentative in that SDR is not necessarily best suited for their detection (only those centers near the interfacial region act to alter the resonance current that is measured). Ryan *et al.* performed similar experiments using conventional EPR (which probes the entire oxide) to not only show that E' centers were created under NBTI, but that their contribution was significant [36]. It was shown that NBTI generated a considerable concentration of E' centers ($1x10^{11}cm^{-2}$) and that upon removal of stress, they fully recovered [36]. These findings supported that NBTI was at least partially triggered by hole

capture in the Si inversion layer at an E' precursor site, a neutral oxygen vacancy, which eventually leads to the depassivation of local interface trap precursors. This experiment supported the earlier statistical model of Lenahan [37], discussions of Lenahan and Campbell, and the later, expanded model of Grasser [38] which predicted an E'/P_b center interaction involving hydrogen to be one of the important physical processes occurring under NBTI. The experiment by Ryan and model of Grasser also agree in that the generated E' centers should recover quickly upon removal of stress. In particular, recovery contamination has been a large source of error and disagreement because of the bias interruption usually required to measure V_T. Like in the experiment of Ryan *et al*., our resonance measurements are made during device stressing thereby eliminating such contamination.

2.3.2 NBTI in the SiC/SiO_2 System

Perhaps one of the most indicative signs of NBTI is the characteristic threshold voltage shift under temperature and bias stressing. While evident in Si, this event is even more drastic and apparent in SiC. Lelis *et al.* have shown extensive evidence of such V_T shifts [18] [39] [40] [41] in state-of-the-art SiC n-channel transistors and power DMOSFETs, a result well correlated with theirs and others' earlier work in the Si system. Marinella *et al.* have shown evidence of NBTI in technologically relevant n-type SiC MOS capacitors [6] and of late there has been one EDMR study reporting tentative NBTI effects, but certainly stress-induced V_T shifts in rather defect-rich SiC p-channel MOSFETs [42].

In recent studies performed by Lelis and coworkers, it was shown that short, alternate negative and positive gate bias stressing at room temperature on SiC lateral n-channel MOSFETs resulted in V_T shifts on the order of 0.25-0.5V [39]. The devices were stressed with modest fields across

the oxide in the range of ±0.5MV/cm to ±2MV/cm. In general, negative bias stressing consistently yielded negative threshold voltage shifts, while positive bias stressing yielded positive V_T shifts [18] [39] [41]. The polarity of the shift is explained in terms of interface and oxide traps wherein, under negative bias, for example, an imbalance between interface traps (negatively charged) and oxide traps (positively charged) results in a net positive trapped charge, which in turn causes a negative V_T shift [39]. The shifts were speculated to be a consequence of charges interacting with existent near-interfacial oxide traps that likely formed in the company of carbon and strained SiO_2. In particular, the traps are consistently thought to be or be related to an oxygen vacancy defect known as the E' center, a defect shown, as previously mentioned, to be a major NBTI concern in the Si/SiO_2 system. Like in silicon, the trap-induced V_T shifts were attributed to a charge tunneling event wherein charges, as a response to bias, empty and fill the traps located very near the SiC/SiO2 interface. This conjecture was further upheld when it was shown that longer stress times and increasing gate biases, applied independently, both resulted in further increased V_T instabilities [39].

Later work incorporated bias stressing as a function of temperature, which garnered results that both upheld these same instabilities and provided insight for a new mechanism concerning V_T shifts [18]. These tests were also performed on nearly state-of-the-art 4H-SiC n-channel MOSFETs which received a post-oxidation NO anneal. It was observed that bias stressing at temperatures between 100-200°C caused more dramatic V_T changes both in the same and, in some cases, an opposite direction with respect to gate bias polarity [18]. A shift of the same bias polarity is consistent with previously mentioned charge tunneling while the observed opposite shift was correlated with bias-induced movement of mobile ions within the oxide. In the case of a positive bias, for example, electrons are expected to fill traps and/or holes are expected to be

emitted, lending to a positive V_T shift. If on the other hand there is a strong presence of mobile ions, those that are positively charged are expected to migrate to the interface and those that are negatively charged will drift towards the gate electrode, leading to a net negative V_T shift [18].

Lelis *et al.* have also reported similar instabilities in SiC power DMOSFETs [40]. From their study, it is worth noting that devices stressed at high temperature alone exhibited far less instabilities than those stressed under combined temperature and bias stressing [40]. As an aside, this important result is also shown in the work presented herein, providing a strong correlation for expected device behavior and the magnetic resonance spectra observed.

In comparison to Si, interfacial charge in the SiC/SiO_2 system is noted to be much more significant, resulting in even worse NBTI-induced device performance degradation [41]. In addition to threshold voltage shifts, this has serious implications for the effective channel mobility. While coulombic scattering diminishes the actual mobility, an additional repercussion of excessive charge trapping includes the reduction of the number of free carriers [43]. Adopted for the SiC/SiO_2 system as well, terminology standardization for Si MOSFETs categorized gate oxide and interface charge to fall under either oxide traps (N_{OT}), interface traps (N_{IT}), fixed charge (N_F), or mobile ions (N_M) [44]. Consideration of reducing the density of interface traps (D_{IT}) lead to the adoption of a common Si device fabrication method - incorporation of a nitrogen-based post-oxidation anneal [45]. In SiC, this method has shown mixed success. While such anneals help to reduce D_{IT}, they have also, in some cases, promoted negative threshold voltages as there still remains a preponderance of positively charged oxide traps. These render the devices in an always-on state making them less effectively utilized as switching devices. Similarly, nitrogen annealing has sometimes lead to MOSFETs having high off-state leakage currents [41]. However, Lelis *et al*. have studied the effects of such post-oxidation NO anneals

on the V_T instability and report that devices having not received such anneals exhibit approximately a 3 times larger instability than those that did [41]. In its favor, it is clear that a nitrogen-based anneal acts to reduce the number of switching oxide traps, and interestingly it has been well documented that nitrogen annealing also reduces interface traps [45] [46]. Even so, Lelis *et al.* note that it is difficult to deconvolve the effects from both kinds of traps and that there is likely the presence of two or more defects affecting device performance [41]. For example, EDMR studies have shown the Si vacancy, a trap in the SiC, to be a dominating interface defect [47] [48]. The Si vacancy is observed in this study as a central defect in both n- and p-channel SiC MOSFETs and is observed simultaneously with an NBTI-induced E' or E'-related defect in p-channel devices.

Marinella *et al.* have observed similar NBTI effects in n-type 4H-SiC MOS capacitors [6]. They demonstrate that the NBTI-induced increase in N_{IT} can be somewhat recovered by removing the negative gate bias or applying a positive one. While it can be said that the mechanisms responsible for NBTI in SiC aren't well understood, the process of their self- and aided-recovery is even more of a mystery. Another study worth noting is a recent EDMR study by Aichinger *et al.* in which 4H-SiC pMOSFETs were surveyed, marking the first EDMR study on such devices [42]. The authors note a negative V_T shift with response to negative-bias high temperature stressing but do not observe any change in the EDMR line shape. They did observe a change in EDMR amplitude. Furthermore, the structure that is observed is rather convoluted and suggests a defect complex, which may be overshadowing any possible contributions of already very sensitive NBTI-induced defects. From this, they conclude that recombination centers at the device interface have little responsibility for NBTI-induced degradation. *We have somewhat of a*

counter-observation wherein the study presented herein shows the presence of NBTI-induced E' or E'-related defects at the interface or near interface region of 4H-SiC pMOSFETs.

Of the differences between Si and SiC, Zhang *et al.* make important conjectures about the effects of hydrogen and nitrogen [49]. In Si, hydrogen plays a large role in the passivation of processing-induced interface traps and defects created under NBTI. In SiC, however, hydrogen has been less effective at passivating similar interface traps and its role in NBTI remains less clear. The effects of nitridation in SiC in reducing some of these interface traps may additionally complicate things by adversely incorporating nitrogen-related trap levels at the SiC/SiO_2 interface [49]. In Si/SiO_2, nitrogen is known to increase NBTI though it has been shown to stabilize some of the dramatic V_T shifts observed in SiC/SiO_2 NBTI studies, as previously mentioned [41]. It may be possible that nitrogen incorporation above the levels responsible for interface trap reduction play a role in NBTI-related degradation in both systems. The authors have importantly summarized that in SiC MOS devices, the activation energies for NBTI and PBTI are generally analogous to those observed for SiO_2 on Si, but that it has proven more difficult, as stated in [41], to separate the effects of oxide and interface traps than in Si because of SiC's larger bandgap [50]. Therefore, it is not a far stretch to assume the same NBTI-induced defects responsible for degradation in the Si/SiO_2 system are likely culprits for similar degradation observed in SiC/SiO_2, though to what extent nitrogen helps or hinders remains unsolved. *This study measures NBTI in SiC pMOS devices that have received post-oxidation nitrogen annealing and shows that NBTI is a large concern even in devices subjected to this processing.*

Chapter 3 – Presentation and Discussion of Techniques

The EDMR technique (BAE) used in this study is a slight modification to gated-diode SDR, both of which are hinged upon the principles of EPR theory. In solid-state physics, EPR has been an influential technique for the identification of important paramagnetic defects in a wide range of material systems. EDMR supplies similar information about the most technologically relevant defects currently limiting performance in various state-of-the-art electronic devices. An overview of these techniques is given, starting with a few basic principles of EPR.

3.1 Electron Paramagnetic Resonance

Electron paramagnetic resonance spectroscopy involves the interaction of electromagnetic radiation with electron magnetic moments [51]. An unpaired electron, due to its spin, has an inherent magnetic moment which promotes orientation with or against an applied magnetic field. This results in a discrete energy level splitting [52]. When the magnitude of this energy splitting matches the energy of applied electromagnetic radiation, resonance is observed. More complex environments and bonding configurations render variations in this simple energy splitting model to provide unique resonance patterns for all paramagnetic defects. Since this depends heavily on the local surroundings of the defect, the variety of observable resonance patterns often leads to detailed and important information regarding the physical and chemical nature of this paramagnetic site.

In broader terms, quantum theory states that an electron is a negatively charged particle whose spin gives rise to an intrinsic angular momentum. A rotating charged particle is known to produce a magnetic field that leads to an associated magnetic moment [53]. The electron's magnetic moment exhibits random orientation until it is influenced by a large magnetic field,

such as the external field applied in EPR. An unpaired electron in such a field, because of its +½ or –½ spin state, has two possible orientations (parallel or anti-parallel to the field) and thus two orientation dependent energies [54]. This field induced polarization splits the spin system into two discrete energy levels, a process known as the Zeeman effect [51]. The Zeeman splitting is illustrated in Figure 3.1.

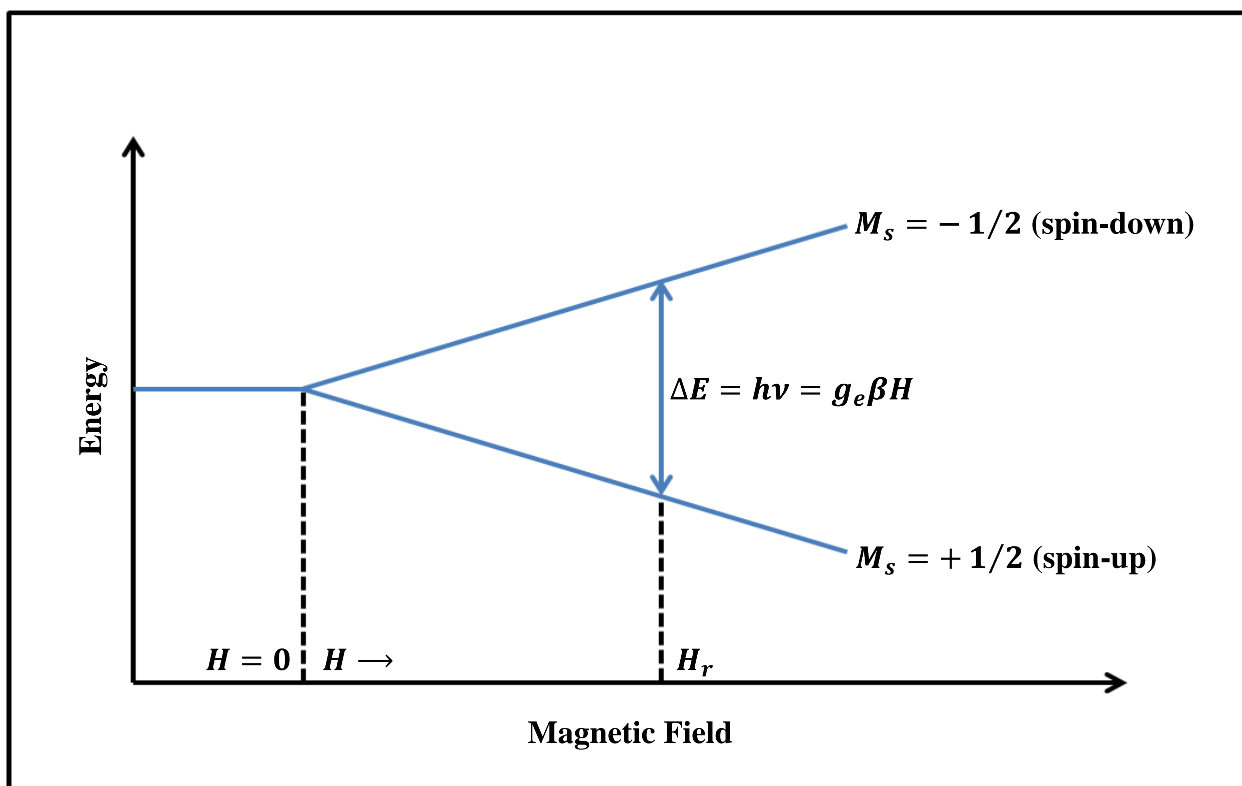

Figure 3.1: Zeeman-energy splitting for the simplest case of an unpaired electron as a function of magnetic field. M_s represents the electron spin quantum number and H_r is the field at which resonance occurs.

In EPR, the large, slowly varying magnetic field is complimented by a perpendicularly oriented high frequency electromagnetic field [54]. This is usually provided via microwave excitation, typically at X-band frequency (~9.5GHz), and has energy expressed as the product of Planck's constant, h, and the field's frequency, ν. When the energy from the microwave radiation is equal

to the Zeeman energy splitting, an electron in the lower energy state is able to absorb the applied energy and "flip" its spin orientation to that of the higher energy state [53] [54]. Likewise, the electron in the upper energy state is able to release energy and "flip" its orientation to that of the lower energy state. From Boltzmann statistics, the sample has a *net* absorption of energy. This is the phenomenon of EPR and for the case of an isolated electron may be expressed as

$$h\nu = g_e \beta H, \tag{3.1}$$

where g_e is the free-electron g-value (2.002319), β is the Bohr magneton (9.274015×10^{-28} J/G), and H is the magnitude of the applied magnetic field [51]. Equation 3.1 represents a simple resonance case in which an electron has no interaction with its surroundings. Since the g value (a second-rank tensor) depends heavily on the local bonding environment, more complex defect structures result in altered energy splitting schemes. This is manifested through changes in the g parameter and requires analysis and decoding of the obtained resonance spectrum. For systems pertinent to this research, deviations from simple resonance are mostly due to spin-orbit coupling and electron-nuclear hyperfine interactions [51] [54], both of which lead to an effective contribution to the local magnetic field.

At this point, it is worth noting that the research contained herein is mostly affected by spin-orbit coupling, but hyperfine interaction analysis has largely provided for the identification of NBTI-induced defects within the aforementioned studies. For completeness, both spin-orbit coupling and electron-nuclear hyperfine interactions are briefly discussed.

3.1.1 Spin-orbit Coupling

Spin-orbit coupling is the term described by an electron's spin interaction with its motion about a nucleus - an effect of the angular momentum involved in the electron's wave function. From a qualitative picture of the Bohr atomic model, it is noted that the electron orbits the nucleus. Observing this scenario from the electron, however, it appears that the positively charged nucleus orbits the electron. The nucleus generates a local magnetic field that additionally influences the electron's behavior in the large applied field [51] [54]. The effect from this additional field scales with the orbital angular momentum of the electron (**r** x **p**), the localization of the electron, and the nuclear charge [55]. These contributions are included into the resonance condition by replacing g_e with a second rank tensor often referred to as the g-tensor [51] [54], which reflects the symmetry of the defect. The anisotropy of defects and their respective g-tensor values can help identify as well as separate overlapping structure from multiple defects. This point must be treated with caution in that an orientation dependence of the defect requires that the sample has certain symmetry, i.e. it is crystalline. In the case of polycrystalline or amorphous materials, $g_{\parallel}$, $g_{\perp}$ and all possible orientations between are observed simultaneously. Few defects will align *parallel with* and most defects will align *perpendicular to* the applied magnetic field, as illustrated in Figure 3.2a. The absorption spectrum under these circumstances often reflects what is called a powder pattern. A simple depiction of this with no hyperfine interference is illustrated in Figure 3.2b. The E' center, as previously mentioned, is a defect located within the oxide and at/near the semiconductor/oxide interface. Due to the amorphous nature of SiO_2, the E' center, with optimized spectrometer settings and no other defect overlap exhibits such a powder pattern under resonance. In this study, the effects of spin-orbit coupling

are used to *identify the nature of the detrimental, NBTI-induced E' center in SiC p-channel MOSFETs*.

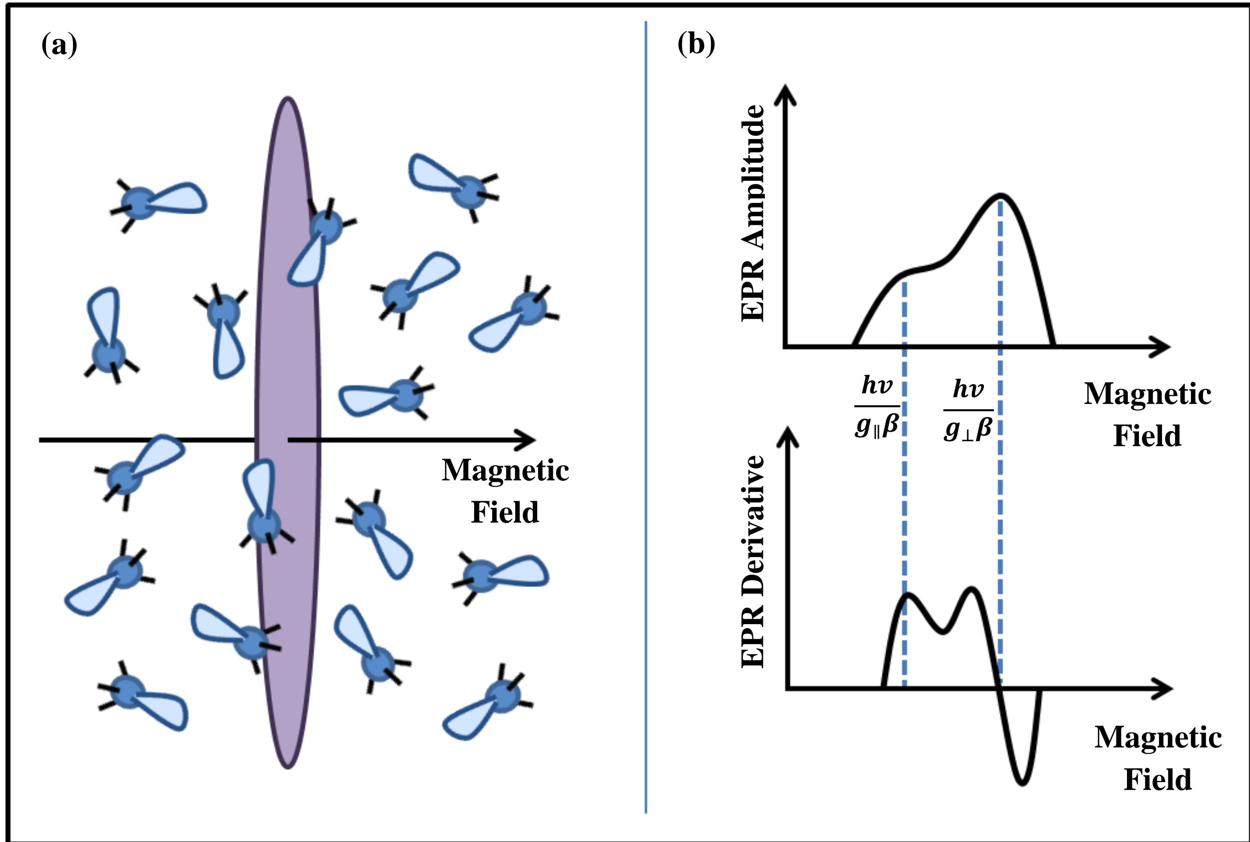

Figure 3.2: An illustration of a powder pattern observed in EPR. (a) shows the random defect alignment with respect to the magnetic field and (b) the resulting EPR spectrum of the powder pattern.

3.1.2 Electron-Nuclear Hyperfine Interactions

Electron-nuclear hyperfine interactions also affect the local field; they describe the interaction of an electron with nearby magnetic nuclei. All nuclei with an odd number of neutrons, protons, or both have a nuclear magnetic moment and thus generate a local magnetic field. Since each nucleus has a unique moment, no two nuclear isotopes can produce the same hyperfine interactions. This often provides detailed chemical information about the defect under study.

Furthermore, since these interactions depend strongly on the localization of the electron wave function, additional quantum details may be uncovered.

The local magnetic field provided by a nuclear magnetic moment alters the resonance condition by splitting the Zeeman levels into (2I + 1) states, where I represents the nuclear quantum spin number [51]. The result is (2I + 1) additional resonance lines centered about the initial resonance field [51]. The spacing of these additional spectral lines scales with the localization of the electron wave function on the nucleus. Their relative intensities are proportional to the paramagnetic abundance of the nearby magnetic nuclei. If only a single magnetic nucleus interacts with an unpaired electron, the resonance condition becomes [51] [35]:

$$h\nu = g\beta H + m_I A \tag{3.2}$$

where m_I is the nuclear-spin quantum number and A is the nuclear hyperfine tensor. Of course, in the absence of magnetic nuclei, the $m_I A$ term is zero. This lends to the differences observed when the magnetic field is oriented parallel or perpendicular to the axis of symmetry for the defect of interest [56].

3.2 Electrically Detected Magnetic Resonance

The onset of advanced technology development in the early 1950's generated abundant work for the semiconductor electronics industry. Research and development following the invention of the transistor [57] [58] led to rapid improvements in electronic circuits with a newly acclaimed, power amplifying and signal switching device pushing the frontier. While EPR had proven and would continue to prove an excellent characterization technique for mostly all of the materials going into these devices, continuing improvements to the devices themselves started to necessitate additional measurement techniques. What defects, for example, were affecting

device performance at the interface and junction regions of these transistors? What when it was required to study the behavior of these defects during device operation, and in concentrations smaller than those detectable by EPR ($\approx 10^{10}$ defects/cm^3)? In 1972, the work of Lepine [59] heralded answers to some of these important questions with the introduction of his EPR based technique, Spin Dependent Recombination (SDR). Unbeknownst at the time, it would also encourage a myriad of techniques under the general category of electrically detected magnetic resonance (EDMR), techniques that probe physical, atomic-scale events that limit device efficacy, such as recombination, scattering, and tunneling. We utilize conventional SDR with slight modifications made to the biasing scheme under the Bipolar Amplification Technique (BAE).

3.2.1 Spin Dependent Recombination

Spin-dependent recombination (SDR) adapts the EPR spin flipping phenomenon to alter recombination current in fully processed devices. Under resonance, a change in device current (ΔI) proceeds as a result of the presence of defects assisting in unwanted device recombination. Recombination centers are rendered paramagnetic and similar as in EPR, they will appear in the observed spectrum to offer details of the atomic structure involved. In conventional SDR, the device is biased such that the source/drain to substrate current is dictated by recombination at the interfacial region of the transistor.

SDR was first explained by the combination of the Shockley-Read-Hall (SRH) model for recombination [60] [61] and the Pauli exclusion principle. A SRH recombination event is one in which a deep level trap hosts as a capture site for and allows the recombination of both a conduction electron and a hole. The Pauli exclusion principle prohibits the capture process when the carrier and trap center possess the same spin quantum number. However, the event is

permitted under resonance when the spin of the electron in the defect is "flipped." The resonance flipping increases the probability of coupling opposite spin orientations and thus increases the device recombination current, the asserted spin dependent current measured in SDR. The Lepine model for SDR is illustrated in Figure 3.3.

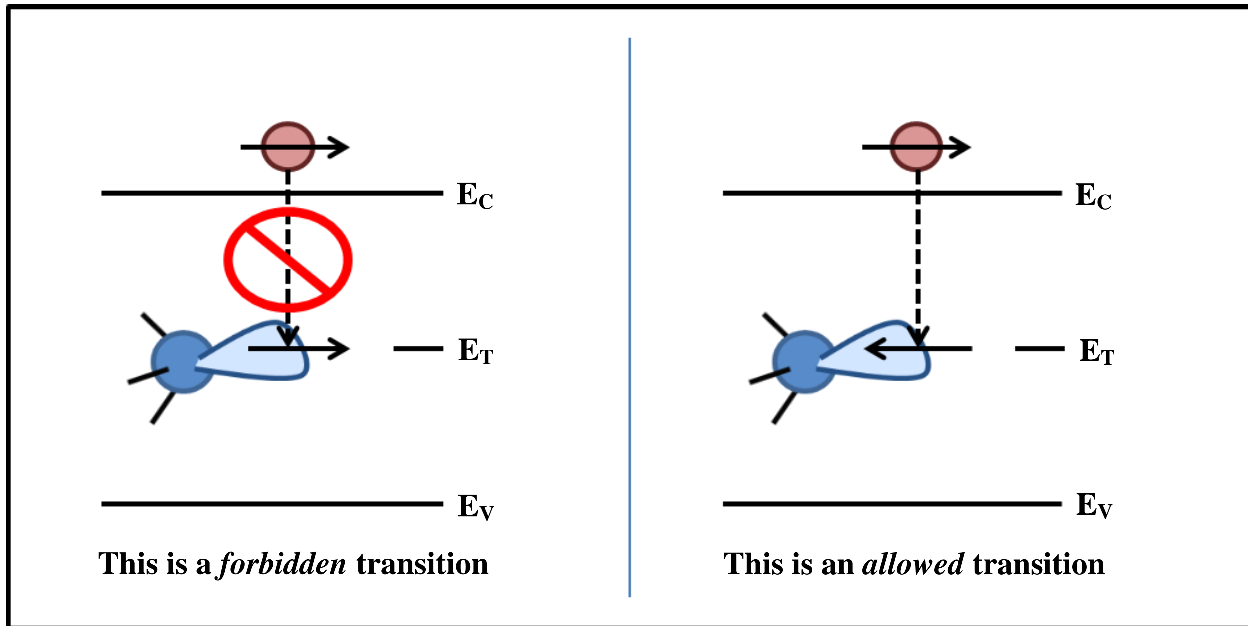

Figure 3.3: Illustration of the Lepine model for SDR. The EPR spin-flipping event and Pauli exclusion principle enhance device recombination current. E_C, E_T, and E_V are the energy levels for the conduction band, trap level, and valence band, respectively.

At resonance, the relative change of the investigated current ($\Delta I/I$) is a strong determinant of the sensitivity limit and signal-to-noise ratio (SNR) of SDR. Lepine projected relative changes to be on the order of 10^{-6} [59] but later work showed possible changes of 10^{-4} [56] [62] and even 10^{-2} [63], such a value approaching perhaps that required by single spin detection. The Kaplan-Solomon-Mott (KSM) model extended Lepine's to incorporate the possibility of spin coupling prior to the recombination event [64]. They asserted that two spins can be coupled and then can either recombine or dissociate, but not interact with other electrons or holes [64]. The KSM model predicted a larger SDR effect than the Lepine model, which better upheld the

experimental data coming forth. Still, progress in the field shows even greater increases in spin detection which calls into question at least some of the physical explanations for SDR.

3.2.2 BAE

The bipolar amplification effect (BAE) is a recent modification to conventional SDR that, under certain circumstances, greatly amplifies the SDR current and concentrates the measurement sensitivity to the semiconductor/oxide interface [63]. This is accomplished by modifying the conventional biasing scheme such that contributions to the device recombination current from the body of the semiconductor are limited and those from the interface are emphasized. With such enhancements, relative current changes as high as 6.8% have been initially reported [63].

Figure 3.4 illustrates the difference in biasing schemes between conventional SDR and the BAE. In conventional SDR, the source and drain are tied together and forward biased (V_F) with respect to the body. The resulting current (I_B=I_{SD}) is sensitive to recombination in the depletion region below the interface, but also in the space charge regions of the source/body and drain/body pn junctions. Contributions from the latter can especially skew the SDR response to the more technologically relevant semiconductor/interface defects. Furthermore, spin-independent diode diffusion currents from the source/body and drain/body regions are superimposed onto the SDR current, thereby adversely diminishing the measurement sensitivity [63]. In the BAE, the source and drain are disconnected from one another and the drain current (I_D) is measured against a zero volt DC potential [63]. An optional modification, though not utilized in this study, is to force a constant current to the source terminal. In the BAE biasing scheme, V_F promotes an enhanced minority carrier concentration at the interface to allow deep level recombination to occur in the transistor channel region. The applied gate voltage is then used to modify the surface potential at the interface to increase the range that carriers can travel. When the carrier diffusion length

(L_{Diff}) exceeds the transistor channel length (L_{CH}), a drain current will begin to appear. Also, if the forward bias of the source/body region exceeds that of the built in voltage, the SDR current within the junction space charge begins to disappear (this is so when the forward bias exceeds the junction's built in voltage by a few tenths of a volt [65] [66]). Under this circumstance and the criteria for $L_{Diff}>L_{CH}$, I_D is essentially sensitive to resonance induced changes occurring strictly in the channel region of the device at or very near the semiconductor/oxide interface [63]. *The BAE is utilized in this study to investigate NBTI-induced interface and near-interface defects in p-channel and n-channel SiC MOSFETs.*

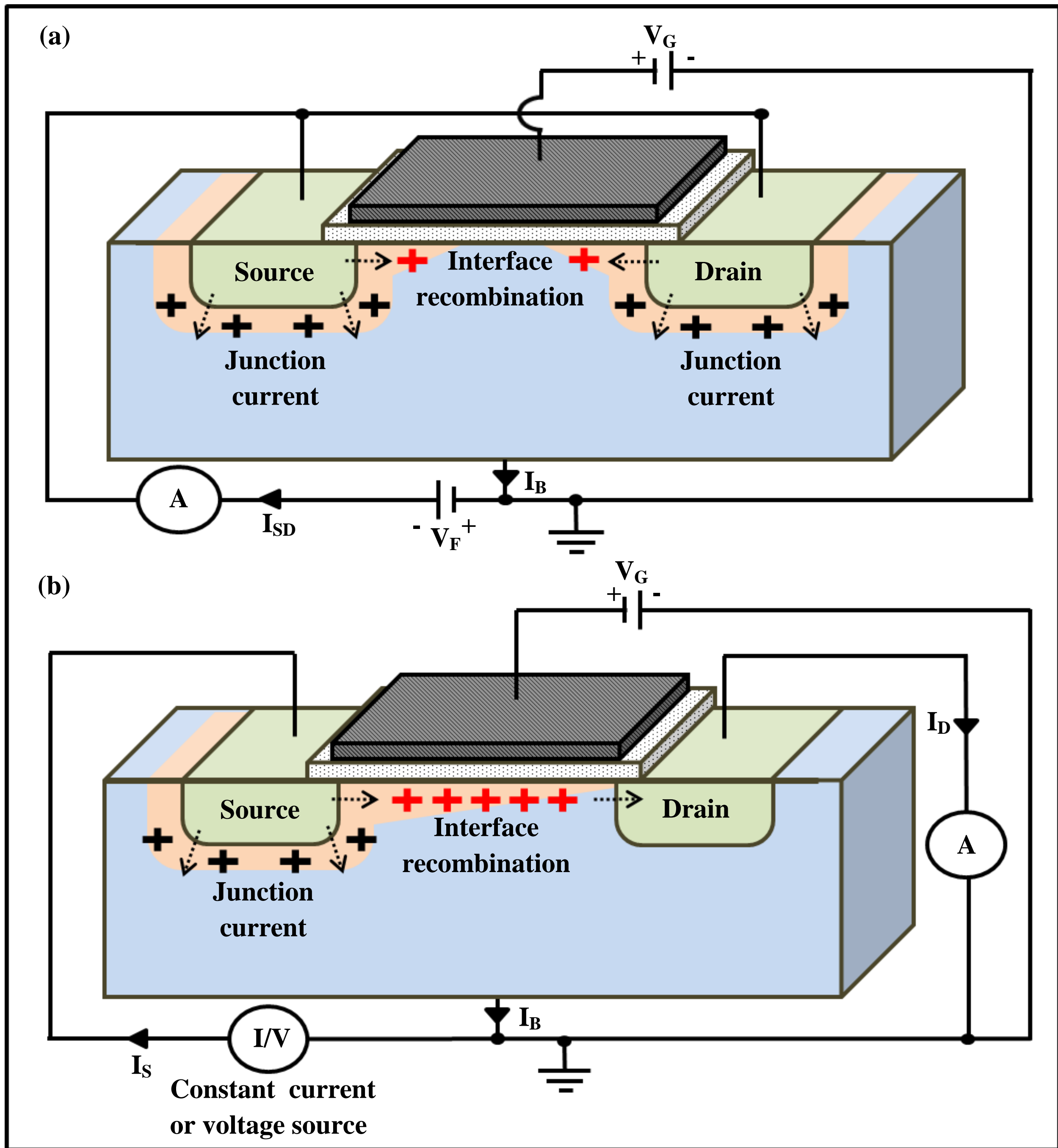

Figure 3.4: An illustration of the device biasing scheme in conventional SDR (a) and the BAE technique (b).

Chapter 4 – Sample Devices and Equipment Used

4.1 Samples

4.1.1 pMOS

Measurements were performed on 100µm x 100µm 4H SiC lateral p-channel MOSFETs provided by General Electric (GE). The source and drain regions were doped with aluminum and the SiO_2 gate dielectric was a 50 nm thermally grown oxide that received an NO post-oxidation anneal. To perform the BAE, we applied a 2.5 V reverse bias to the shorted source and body contacts and -5 V to the gate. The biasing scheme was chosen to maximize the relative change in SDR current at resonance ($\Delta I/I$) as well as provide a modest negative gate bias required of NBTI.

4.1.2 nMOS

The n-channel devices used in this study are technologically similar to the above-mentioned p-channel FETs, though they were provided by a different manufacturer. The CREE n-channel lateral MOSFETs had a 4 times larger gate area (200µm x 200µm) than the GE devices, but a very similar thermally grown SiO_2 gate dielectric with the same approximate thickness of 50nm. As in the p-channel FETs, the n-channel devices also received an NO post-oxidation anneal. They have an effective channel mobility of approximately 22 cm^2/V-s. Dopant atoms were introduced during epitaxial growth.

4.2 Equipment

The custom-built EDMR spectrometer utilized in this study is similar to a standard EPR spectrometer with slight modifications made to the detection scheme. While EPR detects

changes in microwave absorption, EDMR measures changes in device recombination current *due to* microwave absorption.

Measurements were made at room and elevated temperatures with modest gate stressing on a custom built SDR spectrometer consisting of a Resonance Instruments 8330 series X-band microwave bridge, a TE_{102} microwave cavity, and an electromagnet controlled by a custom field controller that incorporates a Lakeshore 475 DSP Gaussmeter. The magnetic field was calibrated using a strong pitch standard under a conventional EPR scheme.

Measurements were made both at room temperature and select elevated temperatures using a Bruker ER 4111VT variable temperature unit. SDR currents were measured using a Stanford Instruments SR570 current preamplifier and SR830 lock-in amplifier with a 2 kHz modulation frequency provided by the lock-in amplifier. A schematic illustration of the system is shown below in Figure 4.1.

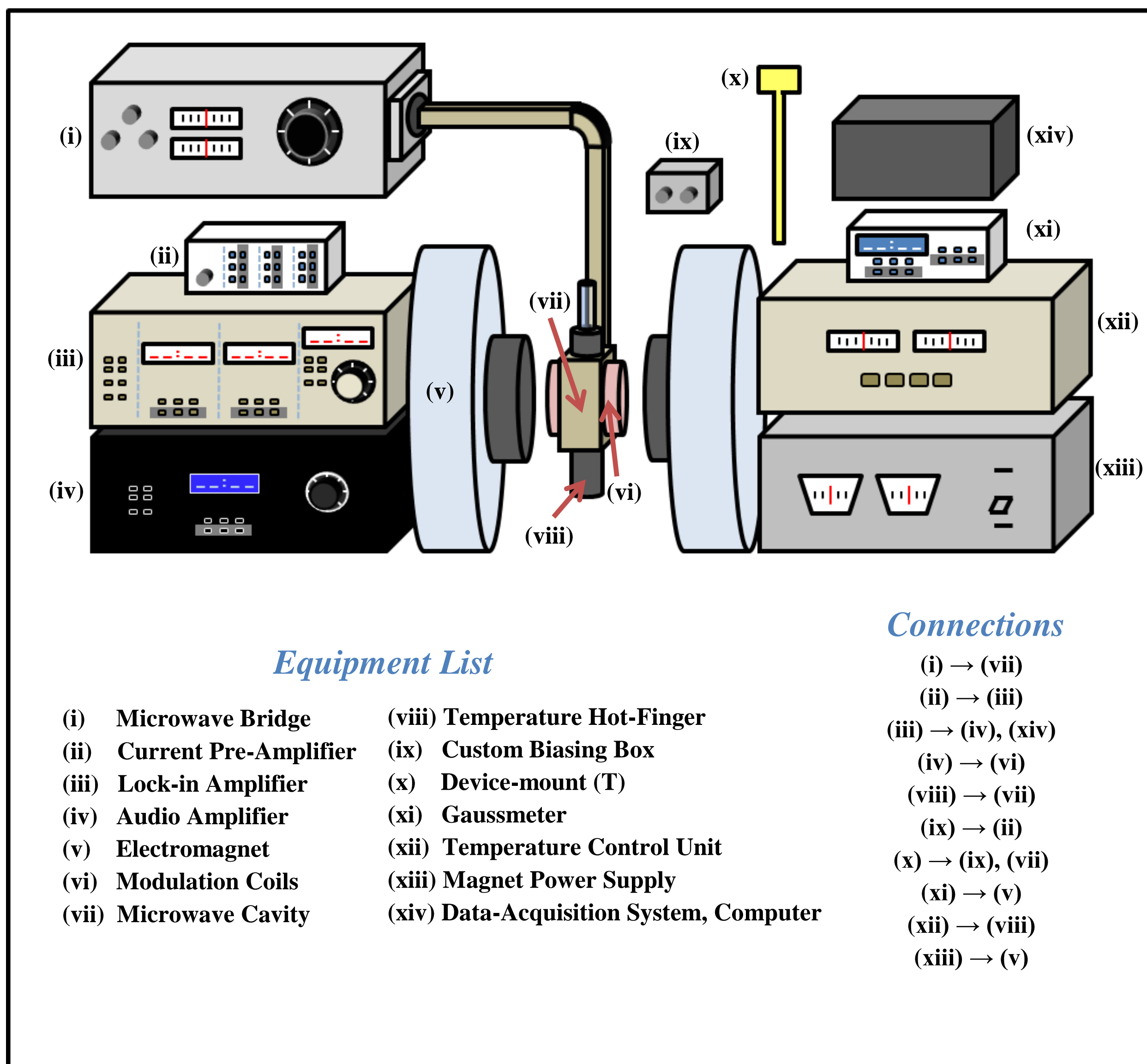

Figure 4.1: A schematic illustration of the EDMR set-up used in this study. The EDMR spectrometer is very similar to an EPR spectrometer with only subtle differences in the detection scheme, whereby EDMR employs the use of a current preamplifier to measure EDMR in fully processed devices.

Chapter 5 – Experimental Results

We present evidence of an oxygen vacancy in 4H-SiC pMOSFETs. This defect, known as the E' center, is activated under the negative bias temperature instability. The defect is detected through the bipolar amplification effect, which is a biasing modification made to spin dependent recombination that focuses the measurement directly to the semiconductor/oxide interface. The E' centers in the pMOS devices show an increase in concentration with increasing temperature while the devices maintain an unchanging bias. Recovery occurs very soon after the removal of temperature stressing even while maintaining the negative bias. Identical measurements are made in nearly identical SiC nMOSFETs which do not show such activation of E' defects but rather a slight increase in the amplitude of the central signal, which is very likely the silicon vacancy. Recovery of the NBTI-induced defect concentration increase similarly occurs rather quickly upon removal of temperature stress. The silicon vacancy is also observed in the pMOS samples but exhibits a very slight decrease in amplitude under increasing stress temperature. Results are given that correspond with the literature in terms of threshold voltage shifts in the case for the nMOS devices but can only tentatively be linked to the defects that appear in the resonance measurements and their relation to NBTI. Minimal threshold voltage shifts are observed in the pMOS samples.

Figure 5.1-Figure 5.4 show the SDR magnetic resonance spectra of a pMOS device first measured at room temperature, followed by increasing 10°C increment temperatures (one increment per figure) between 140 and 170°C, and lastly returned to room temperature. The forward bias of the source/substrate and the gate bias were held constant at 2.5V and -5V, respectively, throughout the measurement so as to purposefully examine the effects of NBTI during stress without interrupting the device under test. The biases were chosen based on two

criteria. The first was to fit the requirements for the BAE so as to both maximize the current response of the device (and thus SNR) and to fit within the narrow window in which SDR can be observed. The second was conveniently not a sacrifice for SNR but a reasonable stress bias for NBTI. Across the 50nm, -5V corresponds to an oxide field of -1MV/cm. So configured, some inference can be gathered concerning the recovery in so far as the measurement is purely a function of changing temperature but not bias. The signal that repeatedly appears at $g \approx 2.0032$ throughout the figures (and the entire study) is consistent with that of the silicon vacancy [47] [48]. The signal that appears only under bias stress at high temperature at $g \approx 2.0008$ is the NBTI activated E' center. Its seemingly small concentration may be a slight misrepresentation of its importance in NBTI as it is considered mostly to be an oxide vacancy with only limited involvement at the interface. The BAE is very sensitive to the interface but only weakly sensitive to E' centers in the oxide. This is the first EDMR study that shows the presence of an E' center in pMOS SiC though one aforementioned study discredited its involvement [42]. There may be certain fundamental impediments that prevented its appearance in this earlier study, however. The first is that the devices used were considerably rich in defects such that their SDR response clearly included multiple defects superimposed on one another, such that any response from potential E' centers could be overshadowed. Second, the measurements utilized conventional SDR, which as mentioned, is prone to recombination within the junction regions of the source/substrate and drain/substrate regions, which can include defects that further eclipse any response of the sensitive E' center. A third possible explanation for the absence of such E' centers is that after the device was stressed, it was allowed to cool to room temperature before the SDR spectrum was measured. As seen in our study, and similarly in studies by Ryan *et al.* in

the Si/SiO_2 system [36], such an effect would not be measured upon removal of temperature stress.

Figure 5.5 shows the response from the pMOS device measured at increasing temperatures. The amplitude of the E’ center increases with increasing temperature (further illustrated via the narrowed window in Figure 5.6), while the amplitude of the silicon vacancy slightly decreases. In terms of $\Delta I/I$, this is shown in Figure 5.7.

Figure 5.8 shows a comparison between similar nMOS and pMOS 4H-SiC devices stressed under the same -5V gate bias at 150°C. The source/substrate forward bias of the pMOS was similar as before, 2.5V, while the nMOS source/substrate junction was biased at -3V, so as to elicit a comparable SDR response as restricted under the BAE. The largest processing difference between the two devices (aside from one being n-channel and the other p-channel) is the smaller gate area in the pMOS device (100μm x 100μm) than in the nMOS (200μm x 200μm) with all other properties and processing steps being relatively similar. The largest SDR difference is the absence of the E’ signal in the nMOS device as a function of temperature and bias stress, though the nMOS device does exhibit a response from the Si vacancy similar to that observed in the pMOS device. This result alone is not enough to exclude the involvement of NBTI activated E’ centers in nMOS SiC because of the differences in surface potential and hole concentration at the interface. It does however suggest that high temperature alone does not trigger the activation of E’ centers.

Figure 5.9 shows a similar study to that of Figure 5.2 except on the aforementioned nMOS device. The device was biased with a source/substrate forward bias of -3V and a -5V gate voltage, which corresponds to a -1MV/cm stress field across the oxide. As before, the device

was measured at room temperature, then at 150°C, then again at room temperature while maintaining an unchanged bias. The signal that appears at g = 2.0030 is again consistent with the silicon vacancy. Unlike in the pMOS stress experiment, an E' center does not appear in the case of the NBTI stressed nMOS device. There is however a slight increase in the amplitude of the silicon vacancy, which effectively recovers upon return to room temperature.

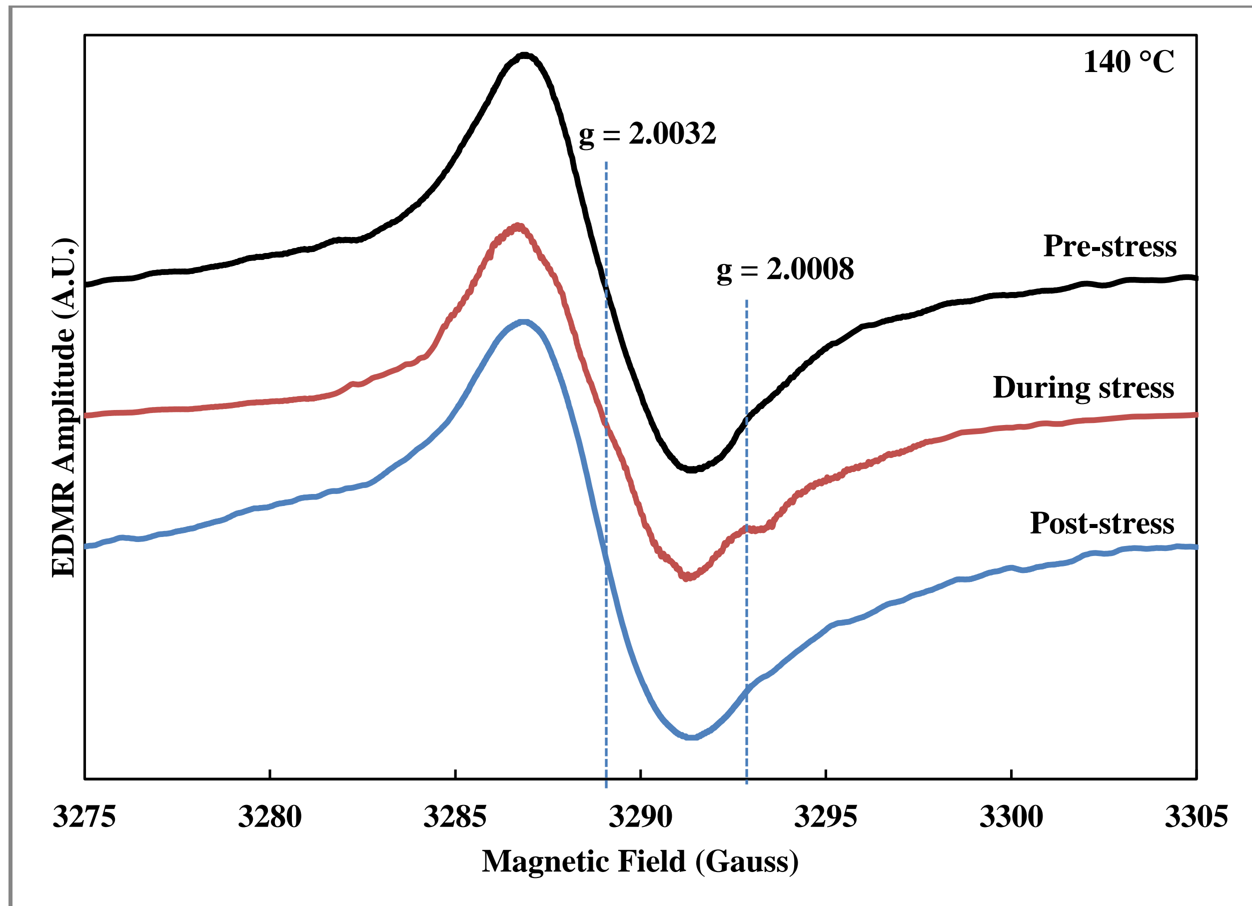

Figure 5.1: SDR spectrum observed for 4H-SiC lateral pMOSFET using the BAE technique. The device was configured with a 2.5V source/substrate forward bias and the drain was held at a 0.0V potential. A gate bias of -5V was applied and maintained through all three measurements. From the top, the first spectrum represents the SDR response of the device at room temperature. The second spectrum represents the SDR response of the device at 140°C. The third spectrum represents the SDR response of the device after removal of the temperature stress. The signal with g = 2.0032 that appears in all of these spectra is consistent with that of the silicon vacancy. The signal with g = 2.0008 that appears only when the negatively biased device is stressed at high temperature is consistent with that of an E' center.

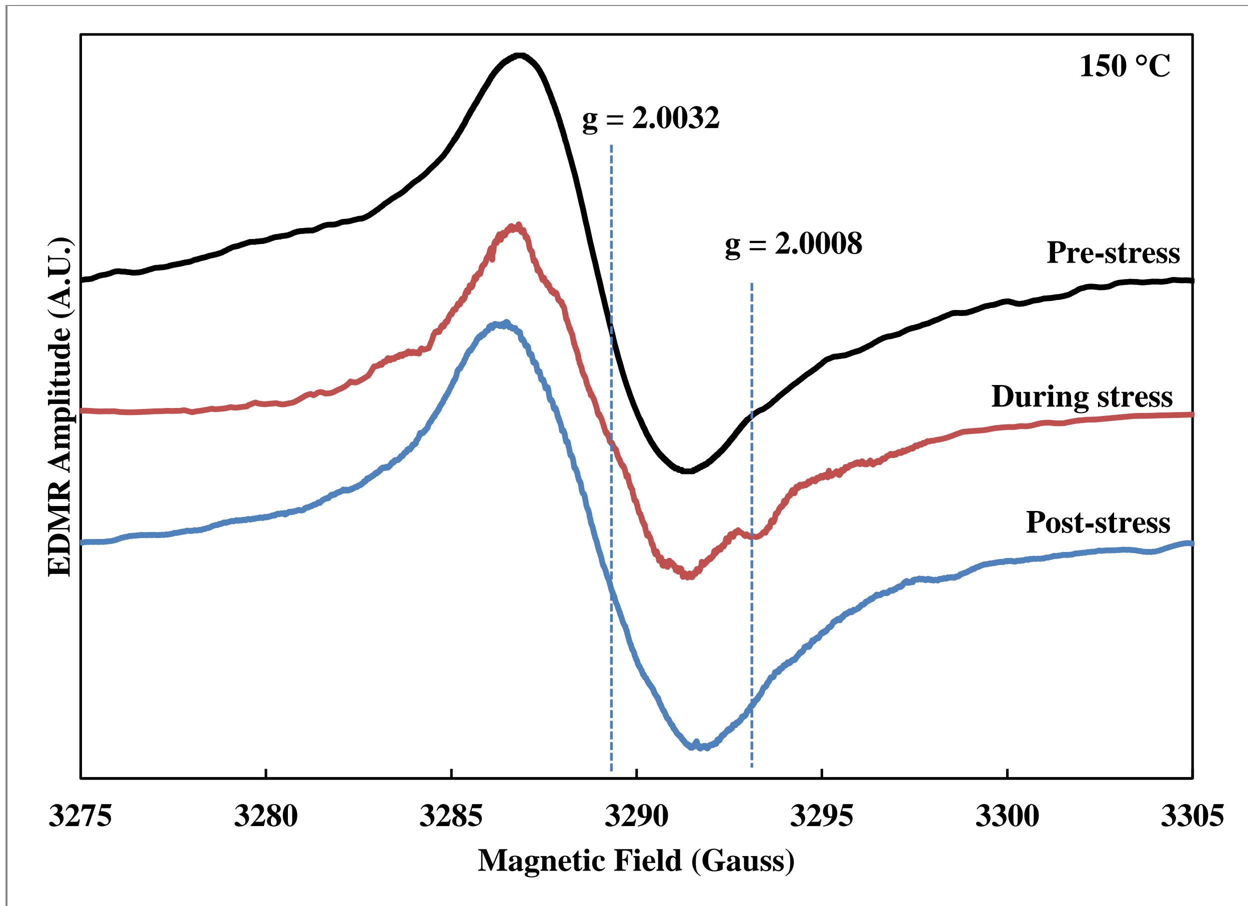

Figure 5.2: SDR spectrum observed for 4H-SiC lateral pMOSFET using the BAE technique. The device was configured with a 2.5V source/substrate forward bias and the drain was held at a 0.0V potential. A gate bias of -5V was applied and maintained through all three measurements. From the top, the first spectrum represents the SDR response of the device at room temperature. The second spectrum represents the SDR response of the device at 150°C. The third spectrum represents the SDR response of the device after removal of the temperature stress. The signal with g = 2.0032 that appears in all of these spectra is consistent with that of the silicon vacancy. The signal with g = 2.0008 that appears only when the negatively biased device is stressed at high temperature is consistent with that of an E' center.

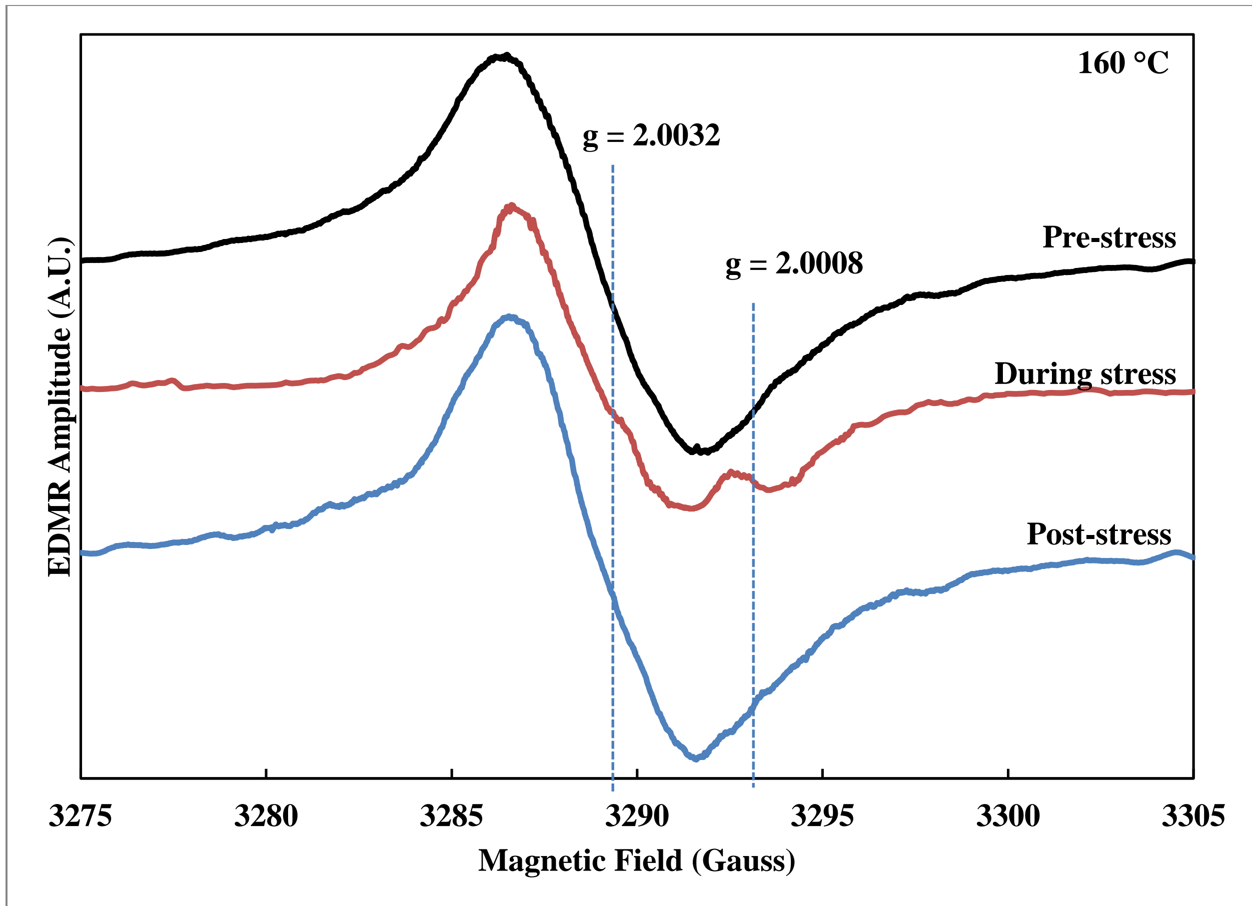

Figure 5.3: SDR spectrum observed for 4H-SiC lateral pMOSFET using the BAE technique. The device was configured with a 2.5V source/substrate forward bias and the drain was held at a 0.0V potential. A gate bias of -5V was applied and maintained through all three measurements. From the top, the first spectrum represents the SDR response of the device at room temperature. The second spectrum represents the SDR response of the device at 160°C. The third spectrum represents the SDR response of the device after removal of the temperature stress. The signal with g = 2.0032 that appears in all of these spectra is consistent with that of the silicon vacancy. The signal with g = 2.0008 that appears only when the negatively biased device is stressed at high temperature is consistent with that of an E' center.

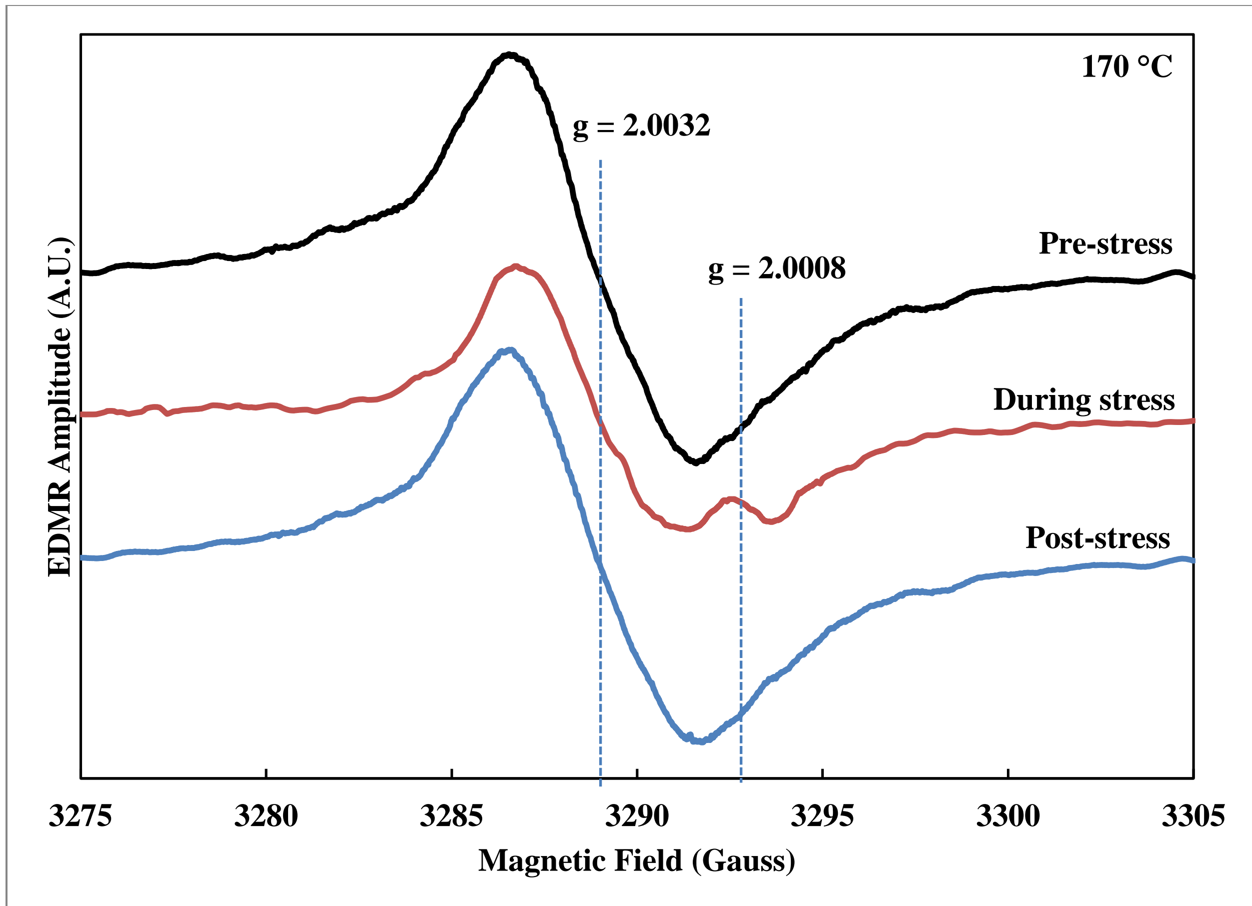

Figure 5.4: SDR spectrum observed for 4H-SiC lateral pMOSFET using the BAE technique. The device was configured with a 2.5V source/substrate forward bias and the drain was held at a 0.0V potential. A gate bias of -5V was applied and maintained through all three measurements. From the top, the first spectrum represents the SDR response of the device at room temperature. The second spectrum represents the SDR response of the device at 170°C. The third spectrum represents the SDR response of the device after removal of the temperature stress. The signal with g = 2.0032 that appears in all of these spectra is consistent with that of the silicon vacancy. The signal with g = 2.0008 that appears only when the negatively biased device is stressed at high temperature is consistent with that of an E' center.

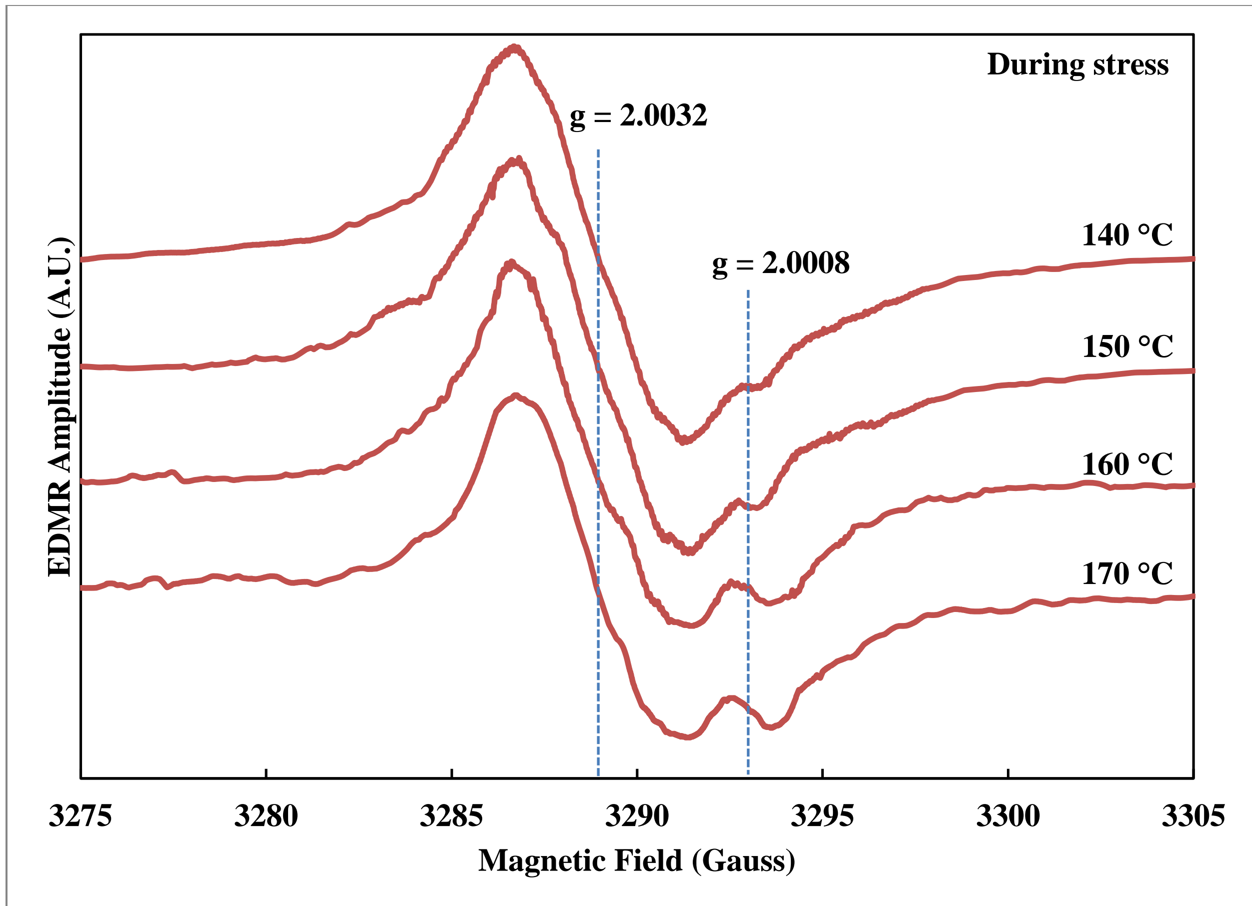

Figure 5.5: SDR spectrum observed for 4H-SiC lateral pMOSFETs using the BAE technique. The devices were configured with a 2.5V source/substrate forward bias and the drain was held at a 0.0V potential. A gate bias of -5V was applied in each of the four measurements. From the top, the first spectrum represents the SDR response of the device at 140°C. The second spectrum represents the SDR response of the device at 150°C. The third spectrum represents the SDR response of the device at 160°C. The fourth spectrum represents the SDR response of the device at 170°C. The signal with g = 2.0032 that appears in all of these spectra is consistent with that of the silicon vacancy. The signal with g = 2.0008 that also appears in each case is consistent with that of an E' center. The growing amplitude of the E' signal represents an increase in concentration with increasing stress temperature.

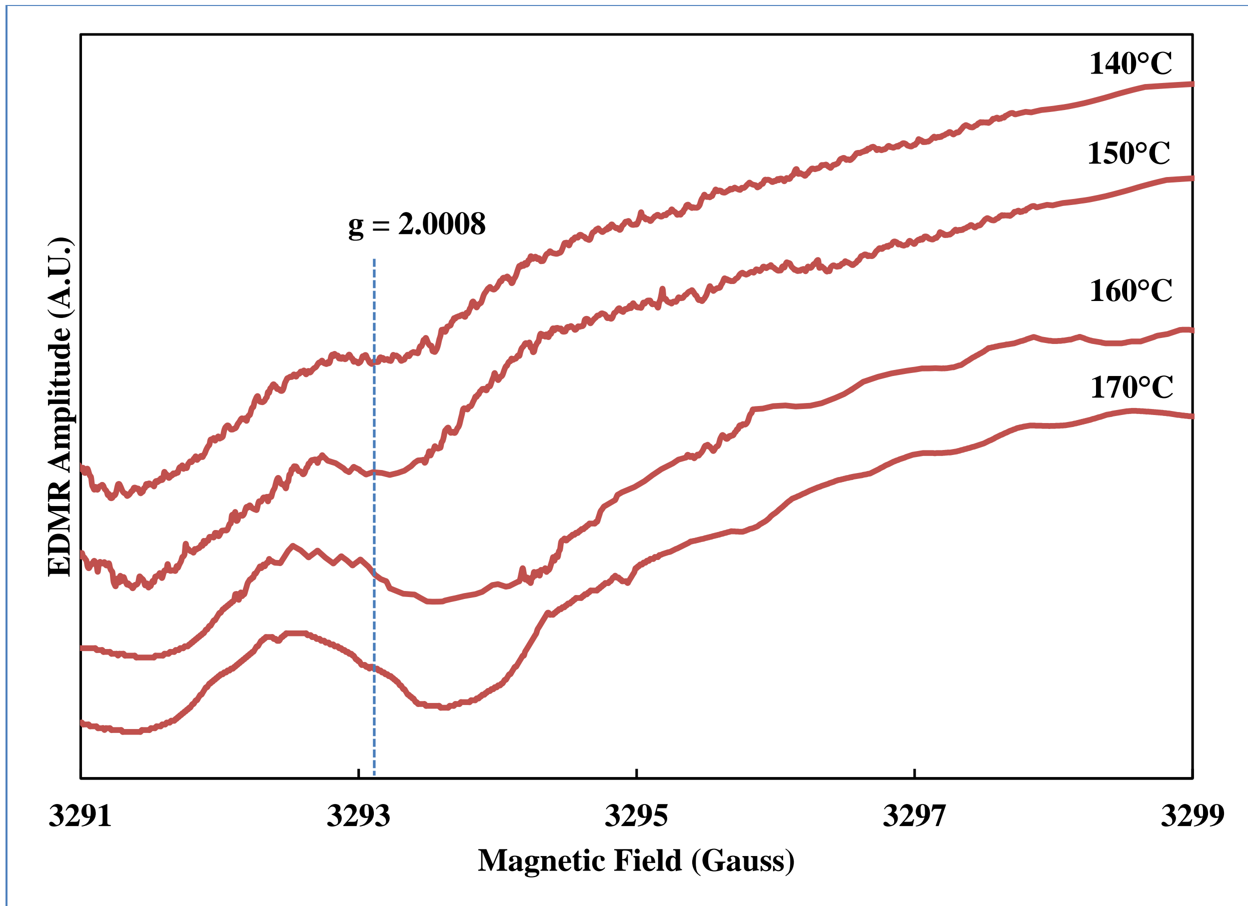

Figure 5.6: Narrowed SDR spectrum highlighting the E' center observed in 4H-SiC lateral pMOSFETs using the BAE technique. The devices were configured with a 2.5V source/substrate forward bias and the drain was held at a 0.0V potential. A gate bias of -5V was applied in each of the four measurements. From the top, the first spectrum represents the narrowed SDR response of the device at 140°C. The second spectrum represents the SDR response of the device at 150°C. The third spectrum represents the SDR response of the device at 160°C. The fourth spectrum represents the SDR response of the device at 170°C. The signal with g = 2.0032 that appears in all of these spectra is consistent with that of the silicon vacancy. The signal with g = 2.0008 that also appears in each case is consistent with that of an E' center. The growing amplitude of the E' signal represents an increase in concentration with increasing stress temperature.

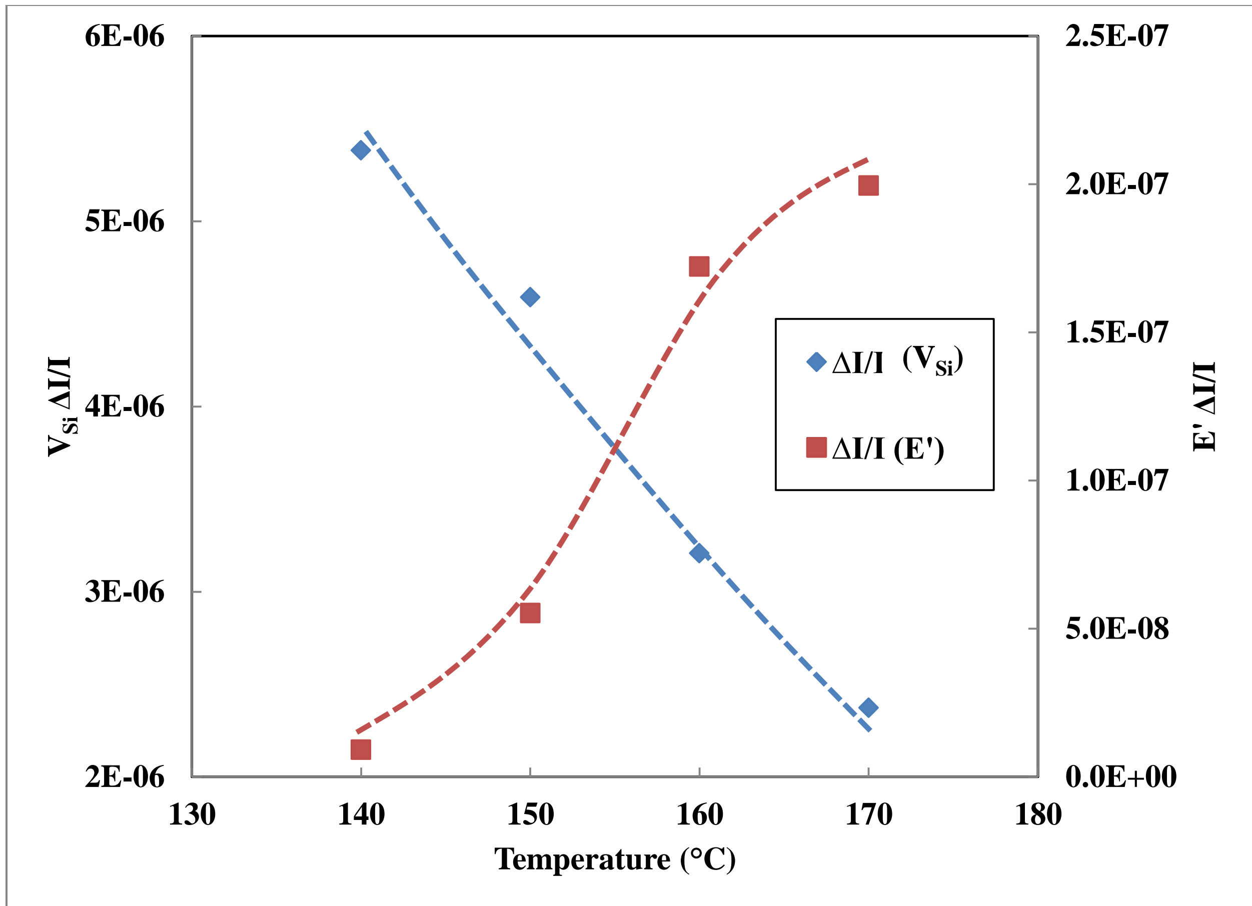

Figure 5.7: ΔI/I values for the silicon vacancy and E' centers observed in bias/temperature stressed 4H-SiC pMOSFET as a function of temperature. A relative increase in ΔI/I for the E' center is observed as a function of increasing temperature. Inversely, a decrease in ΔI/I for the silicon vacancy is observed as a function of increasing temperature.

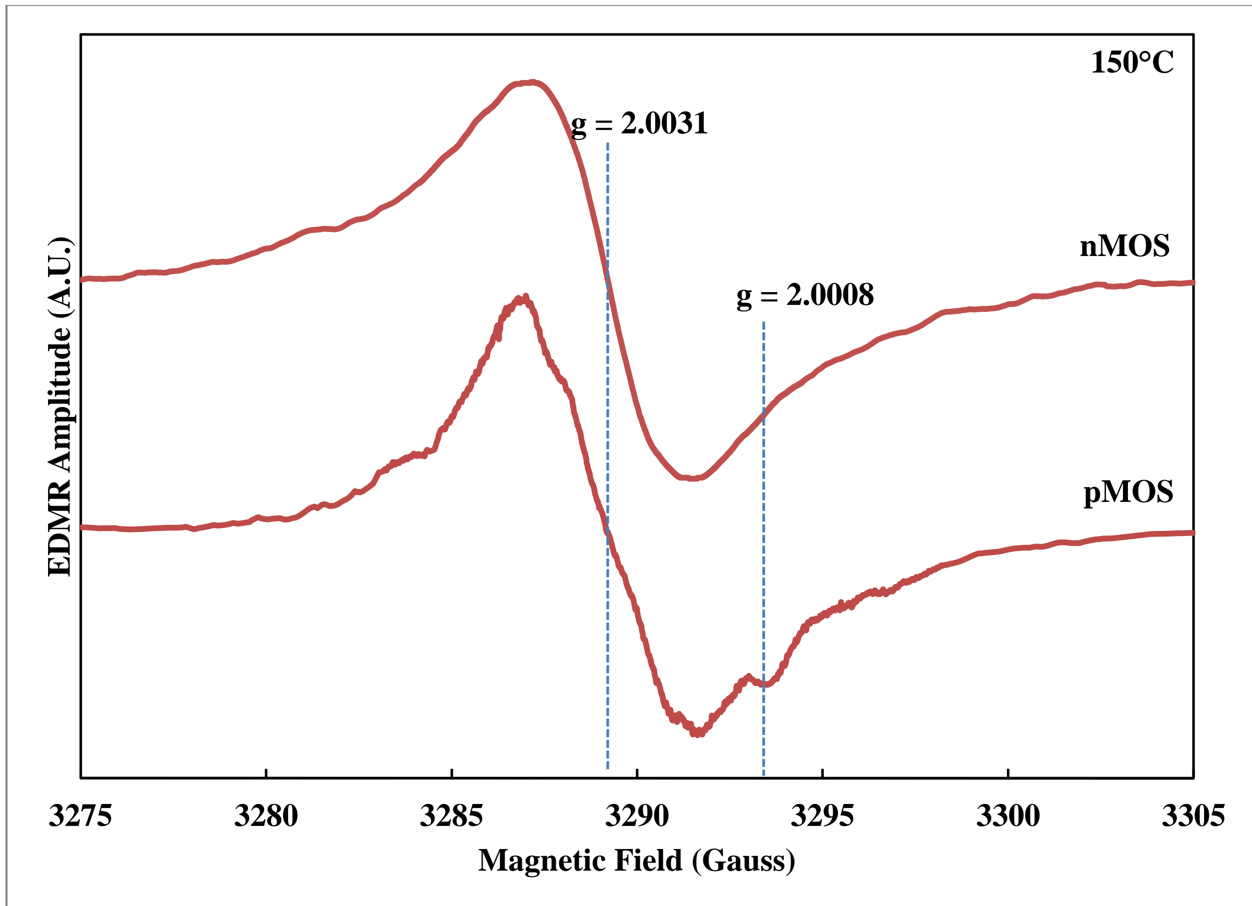

Figure 5.8: SDR spectrum observed for 4H-SiC lateral nMOSFET and pMOSFET using the BAE technique. The nMOS device was configured with a -2.5V source/substrate forward bias and the drain was held at a 0.0V potential. The pMOS device was configured with a 2.5V source/substrate forward bias with the drain also held at a 0.0V potential. A gate bias of -5V was applied to both devices. From the top, the first spectrum represents the SDR response of the nMOS device at 150°C. The second spectrum represents the SDR response of the pMOS device at 150°C. There is clear generation of an E' center in the pMOS device under negative bias temperature stress. There appears to be no E' generation under the same conditions for the nMOS device.

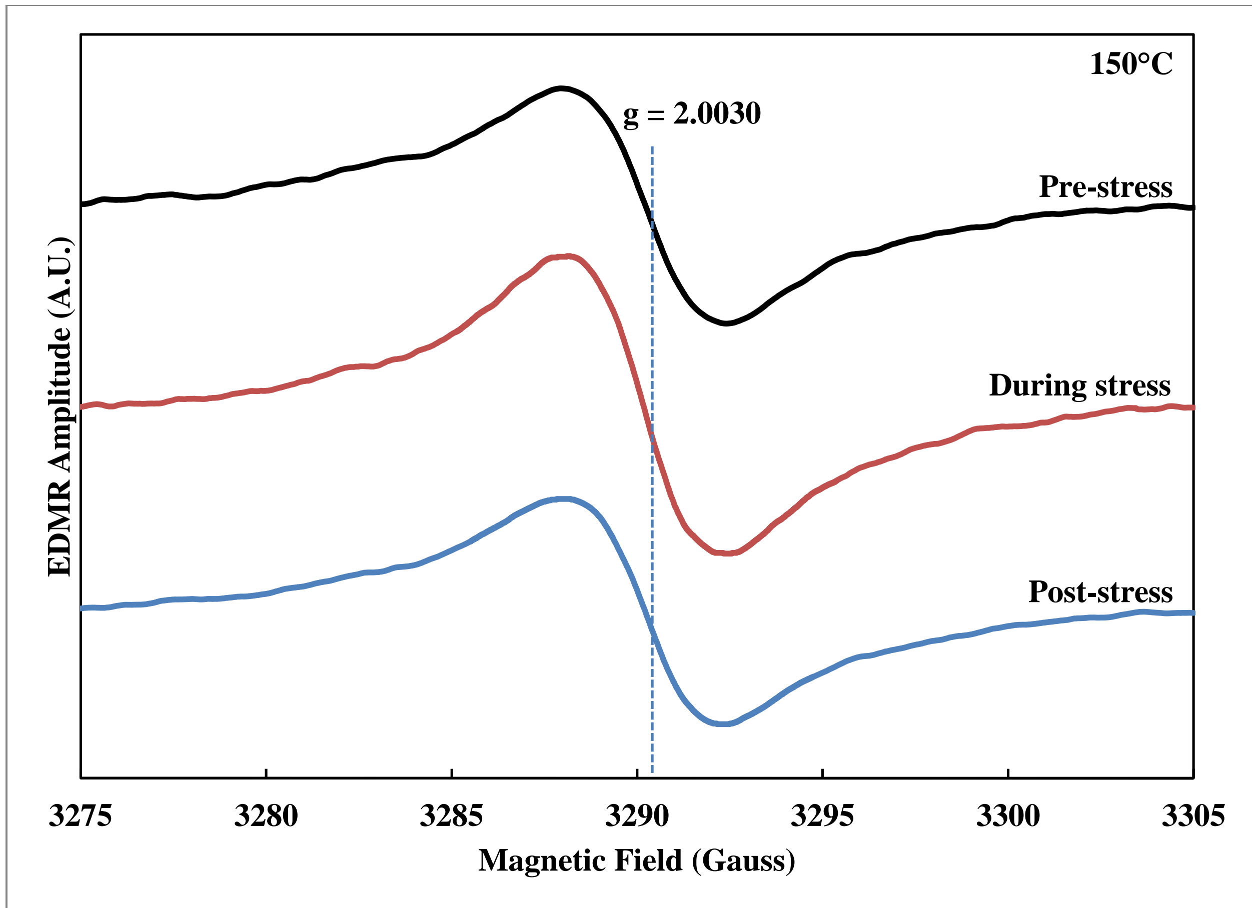

Figure 5.9: SDR spectrum observed for 4H-SiC lateral nMOSFET using the BAE technique. The device was configured with a -2.5V source/substrate forward bias and the drain was held at a 0.0V potential. A gate bias of -5V was applied and maintained through all three measurements. From the top, the first spectrum represents the SDR response of the device at room temperature. The second spectrum represents the SDR response of the device at 150°C. The third spectrum represents the SDR response of the device after removal of the temperature stress. The signal with g = 2.0030 that appears in all of these spectra is consistent with that of the silicon vacancy. Under the combined bias and temperature stress there is a slight amplification of the spectrum by a factor of approximately 1.3.

Chapter 6 – Conclusions

The promise for SiC as a replacement material to Si in MOS technology lies in its inherently advantageous material properties. SiC's large concentration of defects, however, seriously inhibit its integration into the high power and high temperature systems that are demanding it. SiC has been successfully adapted to fit some of the models that govern Si device fabrication although some important differences between the semiconductor/oxide interface and oxide itself create for problems that are yet to be resolved. Such issues are further complicated under the negative bias temperature instability under which the SiC/SiO_2 system shows some of its largest problems. Drastic carrier mobility reductions, threshold voltage shifts, and increased leakage currents among others mark some debilitating problems that are still yet to be fully understood.

We report on the creation of an NBTI-induced oxygen vacancy known as the E' center in 4H-SiC p-channel MOSFETs that actively responds to increasing temperature and quickly recovers upon removal of temperature stressing. These results represent the first study to definitively show the existence of the NBTI-induced defect in SiC and are largely consistent with similar experiments performed in the Si/SiO_2 system. The recovery of the E' center, also consistent with that shown in the Si/SiO_2 system, occurs in full and probably very quickly. However, due to the nature of the signal averaging involved with our resonance measurements, it is difficult to quantify the time frame in which recovery occurs. Of the similar measurements made in nMOSFETs, no definitive evidence of an E' defect is shown, though its relevancy cannot be excluded from NBTI considerations.

The work presented herein should be a springboard for important follow-up measurements to further characterize the NBTI-induced issues in SiC. These may include, for example, a testing matrix that compares differently processed devices, further measurements on nMOS devices with

threshold voltage shifts representative of charge tunneling from an E' center, increased stress fields and/or temperatures, SDR measurements of radiation induced NBTI degradation, effects of positive bias stressing, effects of recovery, etc. By understanding and controlling the presence of NBTI-generated defects, SiC devices may be manufactured to soon operate more reliably in the harsh conditions in which they are queried to.

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