AN INVESTIGATION OF LOCAL NANOMORPHOLOGY AND DOPING AT THE METAL-SEMICONDUCTOR INTERFACE

A Dissertation in
Materials Science and Engineering
by
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Submitted in Partial Fulfillment
of the Requirements
for the Degree of

Doctor of Philosophy

May 2013
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Abstract

The fabrication and characterization of ohmic contacts to n-In$_{0.53}$Ga$_{0.47}$As epilayers and methods of engineering the metal/InGaAs interface to reduce contact resistance are addressed in this thesis. InGaAs is an important material for the continued development of high speed, aggressively scaled transistors, and a fundamental understanding of the formation and behavior of low-resistance ohmic contacts to InGaAs is vital to address issues such as reducing parasitic resistance and improving processing reliability.

Cross-sectional transmission electron microscopy (XTEM) characterization and Schottky barrier height fitting was used to better understand the origins of low contact resistance and properties after thermal annealing for non-alloyed contacts to n$^+$- and n-InGaAs, given constant surface preparation of UV-ozone and buffered oxide etch (BOE). For heavily-doped InGaAs, the specific contact resistance was found to have a greater dependence on metal selection and ex situ surface preparation. The more highly-reactive Pd- and Pt-based contacts resulted in low specific contact resistances ($3.6 \pm 0.3 \times 10^{-8}$ and $7.1 \pm 0.6 \times 10^{-8}$ Ω-cm$^2$), while Mo-based contacts were significantly lower ($2.7 \pm 0.6 \times 10^{-7}$ Ω-cm$^2$) due to the presence of an interfacial oxide. On the other hand, Pd- and Mo-based contacts on lightly-doped InGaAs did not show significant differences in specific contact resistance due to a larger contribution of the Schottky barrier to the overall current transport. The Schottky barrier height extracted using I-V-T measurements suggest a pinned Fermi level at 0.24 eV for contacts with little or no interfacial oxide layer. The performance of the contacts after annealing at 350°C/1 h was adequate in terms of lateral diffusion and interfacial quality. The specific contact resistance of the Mo contact improved to $(1.2 \pm 0.1) \times 10^{-7}$ Ω-cm$^2$ due to degradation of the interfacial oxide. Slight increases in the effective specific contact resistances for the Pd- and Pt-based contacts were attributed to increases in semiconductor sheet resistance below the contacts due to significant reaction depths, whereas the true specific contact resistances varied lit-
tle. Comparisons with the same contacts to p$^+$-InGaAs also revealed very similar behavior, which could be traced back to the interfacial oxide and metal selection. Pd-based contacts to both n$^+$- and p$^+$-InGaAs resulted in the lowest specific contact resistances and good thermal stability; the unique properties of the Pd-based contacts are discussed and speculated upon.

Two methods of engineering the metal/InGaAs interface were also explored in order to address complexities in ex situ surface preparation and the need for heavily-doped material. Enhanced topography at the semiconductor surface containing features with dimensions on the order of the depletion width spaced sufficiently apart have been predicted to increase the electric field at the interface and the active surface area of the ohmic contact. Before contact metallization, refractory TiB$_2$ thin film etch masks were fabricated on lightly-doped n-In$_{0.53}$Ga$_{0.47}$As using electron beam glancing angle deposition (GLAD). Films of varying intercolumnar spacing and thickness were deposited by modifying the thin film deposition process parameters. Selective wet etching and reactive ion etching (RIE) of the InGaAs was used to roughen the surface, which was characterized by atomic force microscopy (AFM). Ohmic contacts of Ti/Pt/Au were fabricated on the modified surfaces and correlated with the InGaAs roughness and lateral dimensions. Specific contact resistance was reduced up to 85% when RIE was used to modify the InGaAs surface, and features with dimensions 30–50 nm wide and 2–3 nm deep were obtained. The multi-step GLAD etching process produced InGaAs surfaces that had root mean square (RMS) roughnesses 2 times higher and lateral dimensions almost 2 times larger (depending on GLAD and etching parameters) compared with surfaces etched without the GLAD etch mask. This multi-step etch method using a GLAD film shows potential as a method for introducing controlled nanomorphology at a substrate surface.

A Pd/Si/Pd solid-phase regrowth (SPR) contact was fabricated to n-In$_{0.53}$Ga$_{0.47}$As epilayers using a low-temperature, two-step annealing process that resulted in the formation of shallow, ultra-low resistance ohmic contacts with little lateral diffusion. An optimum Pd/Si atomic ratio of 1.5 was needed in order for the SPR process to contribute to the lowest contact resistances. Extremely low specific contact resistances on the order of $9 \times 10^{-8}$ and $1.8 \times 10^{-8}$ Ω-cm$^2$, respectively, were measured for both lightly and heavily-doped n-InGaAs. The ohmic behavior for the lightly-doped epilayers was confirmed by I-V-T measurements and Schottky barrier height modeling to be due to the addition of increased Si dopant concentration of about $1.0 \times 10^{19}$ cm$^{-3}$ at the InGaAs interface from the SPR process. XTEM analysis was used to corroborate the SPR mechanism with the electrical measurements at each step of the annealing process.
# Table of Contents

List of Figures x

List of Tables xv

Acknowledgments xvi

Chapter 1 Introduction and Background 1

1.1 III-V Compound Semiconductors . . . . . . . . . . . . . . . . . . . 1
1.2 Low-Resistance Ohmic Contacts . . . . . . . . . . . . . . . . . . . . 2
1.3 Metal-Semiconductor Contacts . . . . . . . . . . . . . . . . . . . . . 3
  1.3.1 Schottky-Mott Model . . . . . . . . . . . . . . . . . . . . . . . 3
  1.3.2 Bardeen Model and Fermi-level Pinning . . . . . . . . . . . . 4
  1.3.3 Current Transport Mechanisms . . . . . . . . . . . . . . . . . 7
1.4 Characterization of Metal-Semiconductor Interfaces . . . . . . . . . 8
  1.4.1 Specific Contact Resistance . . . . . . . . . . . . . . . . . . . 8
    1.4.1.1 Circular Transmission Line Method (CTLM) . . . . 9
    1.4.1.2 Refined Transmission Line Method (RTLM) . . . . 11
  1.4.2 Interface Morphology . . . . . . . . . . . . . . . . . . . . . . . 11
    1.4.2.1 Transmission Electron Microscopy (TEM) . . . . 11
    1.4.2.2 Focused Ion Beam (FIB) Sample Preparation . . . . 12
    1.4.2.3 Z-Contrast Scanning TEM (STEM) . . . . . . . . . . 13
    1.4.2.4 X-ray Energy Dispersive Spectroscopy (XEDS) . . 13
    1.4.2.5 Electron Energy Loss Spectroscopy (EELS) . . . . 14
    1.4.2.6 Atomic Force Microscopy (AFM) . . . . . . . . . . 14
    1.4.2.7 Auger Electron Spectroscopy (AES) . . . . . . . . . 15
1.5 Thesis Outline . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 15
Chapter 2 Literature Review

2.1 Planar Contacts

2.1.1 Introduction

2.1.2 Semiconductor Surface Before Contact Metallization

2.1.3 Choice of Contact Metallization

2.1.3.1 Titanium Based Contacts

2.1.3.2 Molybdenum Based Contacts

2.1.3.3 Palladium Based Contacts

2.2 Nanopatterned Contacts

2.2.1 Introduction

2.2.2 Fabrication Methods and Patterning

2.2.3 Thin Film Deposition: Glancing Angle Deposition

2.3 Solid-Phase Regrowth (SPR) Contacts

2.3.1 Introduction

2.3.2 Solid-Phase Regrowth Mechanism

2.3.3 SPR Contacts to n-GaAs and n-InGaAs

2.3.3.1 Pd/Ge Contacts

2.3.3.2 Pd/Si Contacts

2.3.3.3 Effect of Layer Thicknesses

Chapter 3 Experimental Methods

3.1 Planar Contacts

3.1.1 Fabrication of Contacts

3.1.1.1 Photolithography

3.1.1.2 Surface Preparation and Metallization

3.1.1.3 Liftoff, Mesa Alignment and Etching

3.1.1.4 Thermal Annealing

3.1.2 Electrical Measurements

3.1.3 TEM Characterization

3.1.3.1 Sample Preparation Using Focused Ion Beam

3.1.3.2 Morphological and Chemical Analysis

3.1.4 I-V-T Measurements

3.1.4.1 Barrier Height Calculations

3.2 Nanopatterned Contacts

3.2.1 Initial Wet Etch Calibration and Thin GLAD Etch Masks

3.2.1.1 Samples, Materials and Etchants

3.2.1.2 Etch Rate Calibration and Selectivity Testing

3.2.1.3 Confirmation of 2-Step Etch Process

3.2.1.4 Contact Fabrication

3.2.1.5 Electrical Characterization
Chapter 4 Planar Contacts

4.1 Introduction ............................................. 48
4.2 Specific Contact Resistance Results ...................... 48
4.2.1 Comparison of Different Contact Metals .............. 48
4.2.2 Annealing Results .................................. 49
4.3 Materials Characterization ................................ 51
4.3.1 Annealed Mo Contact ................................ 51
4.3.2 Annealed Pd Contact ................................. 53
4.3.3 Annealed Pt Contact ................................. 56
4.4 Effect of Reaction Depth on Extracted Specific Contact Resistance .................. 57
4.5 Calculation of Effective Barrier Heights to n-In_{0.53}Ga_{0.47}As .................. 59
4.6 Discussion .................................................. 61
4.6.1 Specific Contact Resistance Versus Metal ............ 61
4.6.2 Interfacial Reactions and Thermal Annealing .......... 65
4.7 Comparison to p-InGaAs ................................ 67
4.7.1 Pd, Pt and Mo Contacts to p^{+}-InGaAs .............. 68
4.8 Current Transport Trends Versus Metallization In n- and p-Type InGaAs ........ 70
4.9 Conclusions .............................................. 76

Chapter 5 Nanopatterned Contacts

5.1 Introduction .............................................. 79
5.2 Initial Wet Etch Selectivity Testing ....................... 80
Chapter 6  Solid-Phase Regrowth Contacts

6.1 Introduction ................................................. 112
6.2 Specific Contact Resistance of Pd/Si/Pd Contacts ............... 113
   6.2.1 Effect of Annealing Temperatures and Times .......... 113
   6.2.2 Effect of Pd/Si Ratio ................................ 115
6.3 XTEM and XEDS Characterization ................................ 118
   6.3.1 As-deposited Contacts ................................ 118
   6.3.2 First-step Annealed Contacts ......................... 119
   6.3.3 Second-step Annealed Contacts ....................... 120
6.4 Current Transport and Field-Emission Modeling .................. 124
6.5 Pd/Si/Pd Contacts to p-InGaAs ............................ 126
   6.5.1 Specific Contact Resistance Results .................. 128
   6.5.2 Comparison to Contacts to n-InGaAs .................. 129
6.6 Conclusions ................................................ 130

Chapter 7  Summary and Future Work

7.1 Summary .................................................. 131
7.2 Future Work ............................................... 134

Appendix A  I-V-T Equations

A.1 Specific Contact Resistance as a Function of Temperature .... 137
A.2 Current Transport Modeling ................................. 139
## List of Figures

1.1 Schematic of parasitic resistances in a MOS device. (Adapted from [7, 12, 13, 14]). .................................................. 2
1.2 Contact formation to HEMTs via a non-alloyed contact to a heavily-doped cap layer (left), and an alloyed contact where metal reacts deeply through the barrier layers (right). (Adapted from [17]) . . . . 3
1.3 Energy band diagrams of metal-semiconductor contact before and after they are brought into intimate contact in the case of an n-type semiconductor. .......................................................... 5
1.4 Energy band diagram of metal-semiconductor contact with interfacial layer and interface states. (Adapted from [15]). .................. 6
1.5 Schematic energy band diagram showing TE, TFE, and FE current transport across the Schottky barrier in a metal-semiconductor contact in forward bias. ......................................................... 7
1.6 FIB lift-out of a cross-section at the metal-semiconductor contact edge: (a) a lamella is milled out at the site of interest, (b) a W manipulator probe is used to transfer the lamella to the Cu grid; (c) the lamella is then milled to electron transparency. ........................................... 12
2.1 Typical electron beam evaporation configuration for GLAD. Flux is delivered at an oblique angle, $\alpha$, relative to the substrate normal. . 25
2.2 The SPR mechanism. (Adapted from [97]). ............................... 27
3.1 Schematic of desired process flow for nanopatterned contacts. ....... 38
3.2 Schematic of as-deposited Pd/Si/Pd SPR contact stack. ............... 44
4.1 Specific contact resistance data for the 9 nm Mo, Pt and Pd contacts to $n^+$-In$_{0.53}$Ga$_{0.47}$As before and after annealing at 350°C/1 h in Ar. . 50
4.2 Bright field XTEM images of annealed 9 nm Mo contact to $n^+$-InGaAs. 52
4.3 HAADF STEM image and XEDS line scan of annealed 9 nm Mo contact to $n^+$-InGaAs. ................................................................. 52
4.4 Background subtracted EELS core level peak edges from spectra taken within the Mo layer, InGaAs epilayer, and interfacial layer of annealed 9 nm Mo contact to n+InGaAs. ................................................................. 54
4.5 AES surface scans of the InGaAs epilayer and the Au pad of the annealed 9 nm Mo contact to n+InGaAs. ................................................................. 54
4.6 Bright field XTEM images of annealed 9 nm Pd contact to n+InGaAs. 55
4.7 HAADF STEM image and XEDS line scan of annealed 9 nm Pd contact to n+InGaAs. ................................................................. 55
4.8 Bright field XTEM images of annealed 9 nm Pt contact to n+InGaAs. 56
4.9 HAADF STEM image and XEDS line scan of annealed 9 nm Pt contact to n+InGaAs. ................................................................. 57
4.10 Specific contact resistance as a function of temperature for the Pd and Mo contacts to n-In0.53Ga0.47As (ND = 5 × 10^{17} cm^{-3}) with a selected TFE curve corresponding to 0.24 eV plotted. ................................................................. 60
4.11 Schematic band diagrams of the forward biased (a) lightly and (b) heavily-doped contacts with a thin interfacial oxide of t_{ox} and different depletion widths (not to scale), along with the likely conduction mechanisms. ................................................................. 63
4.12 Calculated specific contact resistance as a function of doping concentration and barrier heights for n+In0.53Ga0.47As. Experimental data from the Pd, Pt and Mo contacts are plotted along with Mo contacts from [62]. ................................................................. 65
4.13 Specific contact resistances of Pd, Pt and Mo contacts to p+InGaAs; as-deposited and after cumulative annealing (courtesy of Shih-ying Yu). 69
4.14 Calculated specific contact resistances versus acceptor concentration for p+InGaAs for various barrier heights in the TFE regime at 300 K. ................................................................. 70
4.15 Measured and corrected specific contact resistances for contacts to n+ and p+InGaAs. ................................................................. 72
4.16 Modeled Schottky barrier heights vs. metal work functions for the as-deposited Mo, Pd, and Pt contacts to n+In0.53Ga0.47As (ND = 3 × 10^{19} cm^{-3}) and p+In_{x}Ga_{1−x}As (x = 0.50−0.47) (NA = 8 × 10^{19} cm^{-3}). 75

5.1 Comparison of etch rates of InGaAs and planar TiB_{2} film using various citric acid:H_{2}O_{2} ratios. Where error bars are not shown, the error is within the plot symbol. ................................................................. 80
5.2 Comparison of etch rates using citric acid:H_{2}O_{2} (20:1) solution. 81
5.3 Etch depths versus etch time for heavily and lightly-doped InGaAs epilayers using citric acid:H_{2}O_{2} (50:1) solution. Where error bars are not shown, the error is within the plot symbol. ................................................................. 82
5.4 AES spectra of various surfaces before and after modified 2-step etch process. ............................................................. 83
5.5 Extracted electrical data from modified contacts using TiB$_2$ GLAD etch mask deposited at 75° and 25 s, with InGaAs etched at various times, and etched-only control contact: (a) specific contact resistances and (b) sheet resistances. ............................................................. 86
5.6 Extracted electrical data from modified contacts using TiB$_2$ GLAD etch mask deposited at 80° and 25, 50, and 75 s, with InGaAs etched at 28 s, and etched-only control contact: (a) specific contact resistances and (b) sheet resistances. ............................................................. 87
5.7 AFM images of surfaces of control samples: (a) as-received and (b) etched 28 s. ............................................................. 88
5.8 AFM images of modified samples of Set A: (a) 28 s (b) 42 s, and (c) 56 s. ............................................................. 89
5.9 RMS roughness values for Set A and control samples. Where error bars are not shown, the error is within the plot symbol. .............. 89
5.10 AFM images of modified samples of Set B: (a) 25 s (b) 50 s, and (c) 75 s. ............................................................. 90
5.11 RMS roughness values for Set B and control samples. Where error bars are not shown, the error is within the plot symbol. .............. 90
5.12 PSD for Set A and control samples. ............................................................. 91
5.13 PSD for Set B and control samples. ............................................................. 92
5.14 TiB$_2$ thickness as a function of deposition time for 75° and 80° vapor angles at 2 Å/s evaporation rate. Where error bars are not shown, the error is within the plot symbol. ............................................................. 95
5.15 SEM images of TiB$_2$ film surface at various deposition times deposited at 75° vapor angle at 2 Å/s evaporation rate: (a) 125 s, (b) 250 s, (c) 500 s, and (d) 1000 s. ............................................................. 96
5.16 SEM images of TiB$_2$ film surface at various deposition times deposited at 80° vapor angle at 2 Å/s evaporation rate: (a) 125 s, (b) 250 s, (c) 500 s, and (d) 1000 s. ............................................................. 97
5.17 Calculated TiB$_2$ thickness as a function of deposition time deposited with 2 Å/s evaporation rate. ............................................................. 97
5.18 Measured TiB$_2$ thickness as a function of vapor angle deposited with 2 Å/s evaporation rate for 500 s. Where error bars are not shown, the error is within the plot symbol. ............................................................. 98
5.19 Calibration of evaporation rate to achieve 50 nm TiB$_2$ GLAD films with a constant deposition rate as a function of vapor angle. Where error bars are not shown, the error is within the plot symbol. .............. 98

xii
5.20 SEM images of TiB film surface and fracture cross-sections deposited at the same deposition rate of 0.07 nm/s to about 50 nm but at different vapor angles: (a) 80°, (b) 75°, and (c) 60°.

5.21 SEM images of thicker TiB GLAD films deposited at 75° having undergone the 2-step etch procedure with greater than 64 s InGaAs etch and 2 min BOE: (a) 16 nm (b) 32 nm, and (c) 49 nm.

5.22 SEM images of (a) as-received InGaAs surface, etched with CA:H2O2 (50:1) at various times: (b) 16 s (c) 70 s (d) 103 s, and (e) 256 s.

5.23 SEM images of TiB2 GLAD film deposited at 75° with thickness of about 30 nm: (a) as-deposited, etched with diluted BOE solution at various times: (b) 5 s (c) 10 s and (d) 15 s.

5.24 SEM images of TiB2 GLAD film deposited at 75° with a thickness of about 30 nm which underwent the 3-step etch process: (a) as-deposited; (b) etched with diluted BOE solution for 5 s; etched with CA:H2O2 (50:1) for (c) 32 s (d) 64 s, and (e-f) TiB2 removed using BOE.

5.25 SEM images of TiB2 GLAD film deposited at 75° with thickness of about 30 nm after RIE: (a) as-deposited; (b) etched with diluted BOE solution for 3 s: RIE for (c) 30 s (d) 60 s, and (e) 90 s.

5.26 AFM images InGaAs surface after TiB2 GLAD film deposited at 75° with thickness of about 30 nm undergoing 3-step etch process: (a) 30 s (b) 60 s, and (c) 90 s.

5.27 SEM images of InGaAs surface (a) etched with CA:H2O2 (50:1) for 56 s and (b) after subsequent UV-ozone treatment.

5.28 SEM images of InGaAs surface etched with CA:H2O2 (50:1) for 50 s after (a) UV-ozone and BOE strip and (b) UV-ozone treatment.

5.29 Specific contact resistances for (a) Set 1 and (b) Set 2, which underwent a 3-step modification process with RIE and additional UV-ozone treatment.

6.1 Specific contact resistance versus second-step annealing times at 380°C at two different diffusion barrier thicknesses.

6.2 Specific contact resistance versus second-step annealing temperatures at 40 s.

6.3 Specific contact resistance versus Pd/Si ratio at two optimized two-step annealing parameters.

6.4 Specific contact resistance versus Pd/Si ratio for select SPR contacts to heavily-doped epilayers.

6.5 Bright field XTEM of as-deposited Pd/Si/Pd contact.
6.6 XTEM images of Pd/Si/Pd contact after annealing at 200°C/30 s: (a) bright field XTEM showing first-step anneal of contact structure (inset: SAD pattern of silicon (bright) layer) and (b) HAADF STEM image. ................................................................. 119
6.7 XTEM images of 370°C second-step anneal: (a) bright field and (b) HAADF STEM with XEDS line scan. ......................... 120
6.8 (a) Bright field XTEM and (b) HAADF STEM images after 380°C second-step anneal showing that the silicide remaining only reacts approximately 5-7 nm into the semiconductor epilayer at some points (dashed line shows original interface); (c) Pd$_2$Si/InGaAs interface with corresponding FFT images. ........................................ 122
6.9 XTEM image of 400°C second-step anneal: (a) bright field image and (b) close-up of annealed Pd/Si/Pd region. ..................... 123
6.10 HAADF STEM image and XEDS line scan of 380°C second-step anneal, but with 30 nm Ti diffusion barrier. ...................... 124
6.11 Specific contact resistances plotted over a range of temperatures and dopant concentrations for specific SBHs. Measured $\rho_c = 1.1 \times 10^{-7}$ $\Omega$-cm$^2$ for lightly-doped SPR contact with ratio 1.5 and annealed at 200°C for 30 s and 380°C for 40 s is also plotted. ..................... 125
6.12 Required doping density vs. SBH at $T=300$ K to obtain the average measured (a) $\rho_c = 1.8 \times 10^{-8}$ $\Omega$-cm$^2$ for the heavily-doped SPR contact and (b) $\rho_c = 1.1 \times 10^{-7}$ $\Omega$-cm$^2$ for the lightly-doped SPR contact. For $N_D = 3.0 \times 10^{19}$ cm$^{-3}$, the $\phi_b = 0.24$ eV. Using $\phi_b = 0.24$ eV, the doping density required to obtain measured $\rho_c = 1.1 \times 10^{-7}$ $\Omega$-cm$^2$ is $1.0 \times 10^{19}$ $\Omega$-cm$^{-3}$. .................................................. 127
6.13 Trend of specific contact resistances throughout annealing process for optimized Pd/Si/Pd SPR contact to p-InGaAs with Pd/Si ratio = 1.5. 128
## List of Tables

<table>
<thead>
<tr>
<th>Table</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>3.1</td>
<td>As-deposited contacts to $n^+$-In$<em>{0.53}$Ga$</em>{0.47}$As ($N_D = 3 \times 10^{19}$ cm$^{-3}$) with Ti/Pt/Au (15/15/100 nm) diffusion barrier.</td>
</tr>
<tr>
<td>4.1</td>
<td>Summary of extracted data from I-V measurements for as-deposited contacts to $n^+$-InGaAs. All contacts had a Ti/Pt (15/15 nm) diffusion barrier (Pt in the case of the Ti contact), and underwent the same surface preparation procedure (10 min UV-ozone and 2 min BOE).</td>
</tr>
<tr>
<td>4.2</td>
<td>Summary of extracted I-V data of 9 nm Mo, Pt and Pd contacts to $n^+$-In$<em>{0.53}$Ga$</em>{0.47}$As, as-deposited and *after annealing at 350°C/1 h.</td>
</tr>
<tr>
<td>4.3</td>
<td>Corrected (C) specific contact resistances for the annealed (350°C/1 h) contacts compared to the measured (M) as-deposited and annealed (350°C/1 h) contacts for Pd and Pt contacts to $n^+$-In$<em>{0.53}$Ga$</em>{0.47}$As. Measured reaction depths are taken from available TEM images.</td>
</tr>
<tr>
<td>4.4</td>
<td>Corrected (C) annealed (270°C/4 h and 350°C/1 h) specific contact resistances compared to measured (M) as-deposited and annealed values for Pd and Pt contacts to $p^+$-InGaAs. Measured reaction depths are taken from available TEM images.</td>
</tr>
<tr>
<td>5.1</td>
<td>Conditions for modified InGaAs using thin TiB$_2$ GLAD etch masks and CA:H$_2$O$_2$ (50:1) InGaAs etchant before contact deposition.</td>
</tr>
<tr>
<td>5.2</td>
<td>Characteristic feature spacing determined from PSD spectra.</td>
</tr>
<tr>
<td>5.3</td>
<td>GLAD Parameters for TiB$_2$ films in e-beam evaporation system.</td>
</tr>
<tr>
<td>5.4</td>
<td>3-step etch parameters for contacts where the InGaAs underwent RIE using BCl$_3$/Ar.</td>
</tr>
<tr>
<td>5.5</td>
<td>3-step etch parameters for contacts where the InGaAs underwent wet etching using CA:H$_2$O$_2$ (50:1).</td>
</tr>
</tbody>
</table>
Acknowledgments

I am deeply grateful to my advisors, Professors Suzanne Mohney and Douglas Wolfe, for their guidance, encouragement, and support of me and my research from the day I first came to Penn State until the completion of this dissertation. I particularly appreciate them for first, taking a chance on me, and secondly, for their efforts to guide, to motivate, and to help me find my passions. Most importantly, I thank them for believing in me, especially in the face of seemingly insurmountable obstacles.

I thank Professors Suman Datta and Joan Redwing for serving on my committee. This work was supported by the Penn State Applied Research Laboratory and Intel Corporation; thank you to Niloy Mukherjee for useful discussions. I am indebted to several people for their direct contributions to this work, especially Joshua Yearsley and Shih-ying Yu, for the fabrication and characterization of many samples, Ashish Agrawal and Euichul Hwang, for helpful discussions regarding simulations, and Ke Wang, for assisting with transmission electron microscopy. I also thank Chad Eichfeld, Tim Tighe, Vince Bojan and many others for training and advising me on lithography and various characterization techniques. I particularly thank Trevor Clark for advising me about electron microscopy and my research, and Tom Medil, for teaching me everything about thin film deposition.

This dissertation would also not have been completed without the help of additional former and current colleagues at Penn State. I would especially like to thank: Brian Downey and Robert Dormaier, for sharing their insights on life and talents with regards to processing; Michael Abraham, for late-night discussions and table tennis; Amber Romasco-Tremper, for being the most encouraging officemate; Kalissa Andre, for giving me shelter when I was homeless and for standing with me in the freezing cold for 4 hours; Sarah Eichfeld, for sharing the best advice and stories and introducing me to Schottky and Ashes; Jessica Leung, for eating lunch with me and being my partner in crime; and Ryan White, for being my buddy since the beginning.

Finally, this journey would not be possible without the unwavering encouragement of my dear friends, especially my 4th of July family, Carey Chen and Tracy Tsai, and my twin, Ken Lin, and the never ending love, patience and support of my family.
1.1 **III-V Compound Semiconductors**

III-V compound semiconductors are currently being investigated as materials for integration in future generations of devices, such as complementary metal-oxide semiconductor (CMOS) transistors that meet the requirements for nodes beyond 22 nm [1, 2, 3], tunneling field effect transistors (TFETs), high electron mobility transistors (HEMTs), and heterojunction bipolar transistors (HBTs). The materials are of interest due to their high electron mobilities; compared with Si, InGaAs has an electron mobility almost 10 times higher and is of particular interest. Specifically, InGaAs has already been established as a channel material for HEMTs [4, 5, 6, 7] for use in high-speed applications with demonstrated high current-gain cutoff frequencies over 600 GHz [3]. InGaAs is also of particular interest for wide-bandwidth HBTs for high-speed telecommunications applications [8, 9].

However, in order to successfully implement these materials into current CMOS technology and to improve current HEMT and HBT performance, there are many challenges. Some of these challenges include difficulty in surface passivation [10], low hole mobility in p-type material, and the low density of states “bottleneck” [11]. One of the most important concerns is the increase in parasitic resistance as device dimensions are scaled to very small feature lengths, thus requiring a source resistance of $<50 \, \Omega \, \mu m$ [3] in order to maintain high cutoff frequencies and low-power operation. A schematic of the parasitic resistances in a MOS device is shown in Figure 1.1.
1.2 Low-Resistance Ohmic Contacts

Metal contacts are essential to any semiconductor transistor, and ohmic contacts in particular are needed to supply current with a relatively small voltage drop compared with the voltage drop over the active region of the device [15]. At scaled dimensions, the ohmic contacts of a transistor device are increasingly becoming a limitation to performance. Contact resistance can contribute \( \sim 30\text{-}40\% \) of the total external resistance [16]. Specific contact resistances of about \( 1\text{-}2 \times 10^{-8} \, \Omega\text{-cm}^2 \) to \( n^+\text{-InGaAs} \) are thus required in order to maintain performance analogous to current contacts made to \( n^+\text{-Si} \) [3].

For integration into very large scale integrated (VLSI) circuit applications and for improvement in device performance, ohmic contacts for these very small devices also need to have certain physical requirements in order to avoid reliability issues during fabrication and operation. The ohmic contacts must possess minimal lateral diffusion and shallow penetration depths, especially as dimensions between the contact and gate decrease. In HEMTs, traditional alloyed contacts formed to buried channels are problematic in this regard, and non-alloyed (i.e. minimal reaction) contacts for heavily-doped InGaAs cap layers have been used to address these concerns [17]; the differences are shown in Figure 1.2. In HBTs, shallow, non-alloyed contacts are also preferred due to decreasing base thicknesses [9].

However, the performance of such non-alloyed contacts can be improved by a better understanding of certain factors, including surface preparation and metallization,
which greatly affect the ohmic contact characteristics. Also, alternative methods to fabricating ohmic contacts to InGaAs should be considered, either through interface engineering and/or through the introduction of excess doping at the interface. For example, the realization of low-resistance ohmic contacts to lightly-doped n-InGaAs would eliminate the need for heavily-doped cap layers in HEMTs. In this thesis, the characteristics of the ohmic contact interface to InGaAs are investigated through the use of advanced materials characterization techniques, and two methods are proposed and employed in order to alter the interface by introducing topography and doping.

1.3 Metal-Semiconductor Contacts

When a metal is contacted to a semiconductor, there exists a potential barrier. By controlling the height and width of this barrier, the current transport can be altered. Ohmic contacts generally require a low barrier height or width in order to maximize current conduction, while rectifying contacts may require fine control of barrier heights.

1.3.1 Schottky-Mott Model

The ideal case of the metal-semiconductor contact can be described by the Schottky-Mott model [18]. Figure 1.3 shows the band diagrams before and after
contact, where \( \phi_m \) is the metal work function, \( \phi_s \) is the semiconductor work function, \( \chi_s \) is the semiconductor electron affinity, \( E_F \) is the Fermi level, \( E_{Vac} \) is the vacuum level, \( E_C \) is the energy at the bottom of the conduction band, \( E_V \) is the energy at the top of the valence band, \( E_g \) is the semiconductor band gap, \( \phi_b \) is the barrier height, and \( w_d \) is the width of the depletion region. Here, when separate systems of an n-type semiconductor and a metal with a high work function are brought into contact, the respective Fermi levels of both systems must align to establish thermal equilibrium. Electrons from the higher energy levels in the semiconductor flow to the metal, creating a depletion region at the semiconductor surface that extends a characteristic length into the semiconductor. An electric field is created here due to uncompensated positive donor ions in the depletion region, giving rise to the potential difference between the metal and semiconductor. The energy barrier for electrons in the metal can then be defined as

\[
\phi_b = \phi_m - \chi_s
\]  

(1.1)

which is independent of doping or applied voltage, and is defined as the Schottky-Mott limit. For a metal in contact with a p-type semiconductor, the energy barrier is

\[
\phi_b = E_g - (\phi_m - \chi_s)
\]  

(1.2)

1.3.2 Bardeen Model and Fermi-level Pinning

Practical contacts generally do not adhere to the ideal Schottky-Mott limit. In many cases, the barrier height may be independent of the metal work function. An additional factor, called surface or interface states, was proposed by Bardeen to also affect the barrier height [18, 19]. The origins and nature of interface states is still being researched to this day [20]. In general they are based on several basic practical concerns. Before contact metallization, the semiconductor surface may be exposed to air, resulting in surface reconstruction or oxidation. The presence of the metal itself may also introduce chemical defects due to reaction at the interface, or the valence electron charge density may be redistributed [21].

The Bardeen model assumes that there is a thin insulating layer containing lo-
calized states at the insulator-semiconductor interface, which is shown schematically in Figure 1.4. These interface states occupy a neutral level, $\phi_0$, as measured from the top of the valence band. Because the junction overall is electrically neutral, the negative charge on the metal surface plus the positive charge in the depletion region due to uncompensated donors, plus the charge of the interface states, must equal zero. If the neutral level is below the Fermi level, the interface states contain a net positive charge, resulting in negatively charged acceptor states between $\phi_0$ and $E_F$. If the neutral level is above the Fermi level, the interface states contain a net negative charge, resulting in positively charged donor states between $\phi_0$ and $E_F$. The effect of this non-neutrality in either case is that $E_F$ must align with $\phi_0$ to maintain a neutral net interface-trap charge [15]. For large densities of surface states, $\phi_0$ will be at the same energy as $E_F$, thus “pinning” the Fermi level at the surface. The Bardeen limit is denoted as

$$\phi_b = E_g - \phi_0$$

(1.3)

making the barrier height independent of the metal work function.

In III-V compounds, the surface Fermi level position has been shown to be pinned for a variety of metals, rendering the barrier height almost completely independent of metal work function [15]. Thus, it is often difficult to control the Schottky barrier
height in this way to improve ohmic contact resistance. The origin of the interface states is not conclusive. Some have attributed the interface states to the presence of the metal itself, in that the metal wavefunction is able to penetrate a finite distance within the semiconductor at certain energies, commonly referred to as metal-induced gap states (MIGS) [18]. Recently, interfacial oxide layers have been investigated for insertion at the metal/n-Si, n-Ge, n-GaAs and n-InGaAs interfaces to form M-I-S contacts in order to modify the effective barrier heights and shift Fermi-level pinning [22, 23, 24]. The use of a tunneling dielectric is proposed to prevent MIGS from penetrating deeply within the semiconductor, or to induce an electronic dipole with the semiconductor native oxide, thus shifting the Fermi-level pinning towards the conduction band edge. Others have studied the surface reconstruction behavior of InGaAs and the effect on Fermi-level pinning [25, 26, 27]. These efforts go to show that when designing ohmic contacts for III-V compounds such as InGaAs, the choice of metal, surface preparation and interfacial reaction are critical factors of study in order to be able to engineer a low-resistance contact.
1.3.3 Current Transport Mechanisms

Current transport through the metal-semiconductor interface is due primarily to majority carriers (electrons in the n-type case). There are two primary methods of current transport across the Schottky barrier which determine the conduction properties. One method is thermionic emission (TE) over the barrier from the semiconductor to the metal, which typically applies to moderately-doped semiconductors ($\sim 10^{17} \text{ cm}^{-3}$). The other method is quantum-mechanical tunneling through the barrier at energies below the top of the barrier, which can occur for very highly doped semiconductors. Tunneling can occur at energies close to the Fermi energy, especially at low temperatures and high doping, which is denoted as field emission (FE). At higher temperatures, the tunneling probability increases, and there is a maximum contribution of electrons at a certain energy above the conduction band [18]. At this energy above the conduction band, thermionic-field emission (TFE) occurs. These current transport mechanisms are shown schematically in Figure 1.5.

![Figure 1.5. Schematic energy band diagram showing TE, TFE, and FE current transport across the Schottky barrier in a metal-semiconductor contact in forward bias.](image)

For Ohmic contacts, highly-doped semiconductor layers are generally preferred in order to narrow the depletion region and promote electron tunneling through the barrier via FE. Other current transport that may occur through the barrier includes recombination in the space charge region, diffusion of electrons in the depletion region, and hole injection.
1.4 Characterization of Metal-Semiconductor Interfaces

1.4.1 Specific Contact Resistance

The electrical performance of the metal-semiconductor contact is characterized by the contact resistance. The contact resistance can be expressed by the quantities termed contact resistance ($\Omega$) or specific contact resistance, $\rho_c$ (\(\Omega\cdot\text{cm}^2\)). The specific contact resistance takes into account the metal-semiconductor interface as well as the regions below and above the interface [28]. The specific contact resistance is the typical figure of merit used to compare various ohmic contacts because it is independent of contact size, and it is used in this thesis to compare the ohmic contact performance. It is defined as

$$\rho_c = \left( \frac{\partial V}{\partial J} \right)_{V=0}$$

(1.4)

where $V =$ applied voltage and $J =$ current density across the metal-semiconductor contact. When dominated by thermionic emission, $J$ is defined as:

$$J = A^*T^2 \exp \left( \frac{-q\phi_b}{kT} \right) \left[ \exp \left( \frac{qV}{kT} - 1 \right) \right]$$

(1.5)

where $A^* =$ Richardson’s constant, $T =$ absolute temperature, $\phi_b =$ barrier height, $k =$ Boltzmann’s constant, and $q =$ elementary electron charge. $J$ is a function of the applied voltage, barrier height, the total doping concentration, $N$, and temperature. The specific contact resistance is usually defined in the three current transport regimes [15], where for TE,

$$\rho_c \propto \exp \left( \frac{q\phi_b}{kT} \right)$$

(1.6)

and for TFE,

$$\rho_c \propto \exp \left( \frac{q\phi_b}{E_{00} \coth(E_{00}/kT)} \right)$$

(1.7)

and for FE,

$$\rho_c \propto \exp \left( \frac{q\phi_b}{E_{00}} \right)$$

(1.8)
and where the tunneling parameter is defined by,

\[ E_{00} = \frac{h q}{4\pi} \left( \frac{N_D}{m^* \varepsilon_s} \right)^{1/2} \]  

(1.9)

where \( h \) = Planck’s constant, \( N_D \) = total donor concentration, \( m^* \) = effective mass, and \( \varepsilon_s \) = permittivity of semiconductor. The actual specific contact resistance expressions, as derived by Padovani and Stratton [29], are shown in Appendix A.

By inspection of the derived expressions, the specific contact resistance is a function of barrier height in all three regimes, the doping concentration in TFE and FE, and temperature in TE and TFE. In TE, the specific contact resistance is dependent on the barrier height only, while in FE, it is related to the doping concentration by the factor \( \exp(N_D^{-1/2}) \). Thus, the main methods for reducing the contact resistance in ohmic contacts are to increase the doping concentration in the semiconductor and to decrease the barrier height by, for example, introducing heavily-doped surface layers or altering the metallization, respectively.

1.4.1.1 Circular Transmission Line Method (CTLM)

In order to measure the specific contact resistance, the most commonly used method is the transmission line method (TLM) test structure. This method consists of multiple rectangular contacts on the semiconductor surface spaced at varying distances apart, \( d \), and the lateral current flow between a particular metal-semiconductor contact is represented by an equivalent circuit containing the semiconductor sheet resistance, \( R_{sh} \), and the specific contact resistance, \( \rho_c \).

In this model, the length over which the majority of the current is transferred is considered. This characteristic distance inside the contact from its edge, called the transfer length, \( L_T \), is where \( 1/e \) of the total current has been transferred between the metal and semiconductor, and is defined as

\[ L_T = \sqrt{\frac{\rho_c}{R_{sh}}} \]  

(1.10)

The total resistance measured over each contact spacing is plotted as a function of \( d \). From the linear fit of this plot, the contact resistance, \( R_c \), can be determined; at
\( d = 0, \ R = 2R_c \). From extrapolation of the fit line, \( 2L_T \) is extracted where \( R = 0 \), and \( \rho_c \) and \( R_{sh} \) can then be extracted. The TLM method is valid assuming that the semiconductor sheet resistance does not vary below or between the interface of the contact, and that the metal sheet resistance is negligible. In this thesis, Au layers were always deposited as the topmost contact layer in order to ensure negligible metal sheet resistance. Another important criterion that must hold for the TLM model is

\[
\rho_c > 0.2R_{sh}t^2
\]  

(1.11)

where \( t \) is the semiconductor epilayer thickness [28].

However, in this thesis, a modified form of the TLM method, called the circular TLM (CTLM), is used primarily as the standard method of measuring specific contact resistance. The CTLM structure is advantageous mainly because of the ease of fabrication compared with the standard TLM structure. For the standard TLM test structure, an isolation mesa must be fabricated in order to prevent measurement of current flow from the contacts away from the region beyond the test structure, which leads to a second alignment step during lithography.

In the CTLM structure, concentric ring structures are fabricated with inner metallic pads and an outer conducting region, with various gap spacings. The total resistance for each gap is then measured in a similar manner and plotted as a function of gap spacing. The total resistance, \( R_T \), is represented by the function as described by Marlow and Das [30] and Ahmad and Arora [31]:

\[
R_T = \frac{R_{sh}}{2\pi} \left[ \ln \left( \frac{d + r_0}{r_0} \right) + \frac{L_T I_0(r_0/L_T)}{r_0 I_1(r_0/L_T)} + \frac{L_T}{d + r_0} K_0((d + r_0)/L_T) \right] 
\]  

(1.12)

where \( d \) is the gap spacing, \( r_0 \) is the radius of the inner contact pads, and \( I_0, I_1, K_0 \) and \( K_1 \) are modified Bessel functions. Unlike the TLM geometry, \( R_T \) versus \( d \) as measured cannot be represented by a linear fit. In this thesis, the data points of the total resistance versus \( d \) plot are fitted according to Equation 1.12 using the Levenberg-Marquardt method in order to extract the \( R_{sh} \) and \( L_T \) to calculate \( \rho_c \).
1.4.1.2 Refined Transmission Line Method (RTLM)

A refined TLM (RTLM) test structure is also used in this thesis, specifically for contacts made to heavily-doped epilayers. This RTLM test structure, as developed by Dormaier et al. [32], is used for contacts where the specific contact resistances are expected to be in the range of $10^{-8} \ \Omega \cdot \text{cm}^2$ or below and where the semiconductor sheet resistance is low. In these circumstances, the resistive contribution of the metal contact becomes more significant compared with that of the semiconductor, thus resulting in either an overestimation or underestimation of the contact resistance. An overestimation may occur since the standard TLM test structure ignores the resistive contribution of the metal as measured by the voltage probes between the current probes and the front edges of the contact pads, as the contact pads are treated as isopotentials. An underestimation may occur if the current and voltage probes are placed in certain configurations because there is also less uniform current spreading. The RTLM test structure consists of metal pads with high length-to-width aspect ratios with extension arms. The current probes are placed at the back center of the pads, while the voltage probes are placed close to the front edge of the metal pads so that the potential is uniformly distributed laterally across the pads.

1.4.2 Interface Morphology

1.4.2.1 Transmission Electron Microscopy (TEM)

To analyze the physical morphology and chemistry of the metal-semiconductor interface, TEM is one of the most important material characterization techniques available. TEM enables the imaging of interfacial reactions and interface morphology and the collection of diffraction information, with spatial resolutions reaching $< 1$ nm, depending on the probe size and application. Spatially resolved chemical analysis can also be performed, thus revealing information about phase formation and reactions across the interface. The images and chemical information collected can be used to correlate microstructure, crystallography and chemistry with the electrical performance of the contacts.
1.4.2.2  Focused Ion Beam (FIB) Sample Preparation

The main drawbacks associated with TEM are difficult sample preparation and small sampling size. The sample must be electron transparent and extremely thin in order to take advantage of the technique to collect high-resolution images and chemical information about the metal-semiconductor contact. Typically, cross-sectional TEM (XTEM) samples are needed in order to observe the metal-semiconductor interface, and are fabricated via manual grinding and ion milling. However, large blanket layers are usually needed when using this method.

The focused ion beam (FIB) has recently emerged in the last two decades as a tool to fabricate site-selective XTEM samples for a variety of materials [33]. FIB typically refers to a dual-beam system with a scanning electron microscope and a focused ion beam column, usually equipped with a Ga ion source. The ion source is used to mill or etch material. For XTEM sample preparation, a technique called lift-out is used, where a small lamella (typically 10–20 µm long) is cut out at the site of interest on the sample. The lamella is removed by using a W manipulator probe and transferred to a TEM sample grid, as shown in Figure 1.6. In order to attach this probe to the lamella, a carrier gas containing a chemical precursor for Pt or W is flowed in the chamber and chemically reacts with the ion beam, subsequently solidifying on the area of interest. The lamella is then milled to electron transparency using the ion beam. Typical lift-out methods are the total release method [34, 35] and the Hitachi method [36].

![Figure 1.6](image)

**Figure 1.6.** FIB lift-out of a cross-section at the metal-semiconductor contact edge: (a) a lamella is milled out at the site of interest, (b) a W manipulator probe is used to transfer the lamella to the Cu grid; (c) the lamella is then milled to electron transparency.

However, there are several disadvantages to using FIB to fabricate XTEM samples.
The use of the Ga ion source for milling results in the incorporation of Ga within the sample, which may appear during chemical analysis. The ion beam can also be strong enough to create amorphous damage on the surfaces of the cross-section, which can degrade image quality in the TEM. It is also difficult to fabricate samples that are thinner than those made manually due to the resolution of the SEM.

In this thesis, FIB was used to prepare cross-sectional samples of the contacts at specific regions of interest, usually at the contact pad edge. This allowed the observation of possible lateral diffusion at the contact edge, as well as the measurement of changes in reaction depth by using the semiconductor surface as a reference point.

1.4.2.3 **Z-Contrast Scanning TEM (STEM)**

Scanning TEM uses a converged electron probe that is rastered across the TEM sample. An image is formed from the intensity of electron diffraction as a function of the probe position. This technique is quite useful for the analysis of metal-semiconductor interface cross-sections. Because of the small probe sizes that can be used (< 1 nm), phase-specific, spatially-resolved chemical information from samples may be gathered by using analytical techniques such as X-ray energy dispersive spectroscopy (XEDS) and electron energy loss spectroscopy (EELS) in STEM mode.

Z-contrast STEM imaging, commonly known as high angular annular dark field (HAADF) STEM imaging, may be utilized as a supplementary technique to bright-field (BF) TEM imaging in order to better differentiate heavier elements and interface boundaries due to chemical differences within the specimen. An annular detector with a large radius (> 50 mrad) is used so that only the high-angle scattered electrons from the sample are collected. Thus, the scattering can be approximated by the Rutherford scattering cross-section, and is proportional to the square of the atomic mass, $Z^2$ [37].

1.4.2.4 **X-ray Energy Dispersive Spectroscopy (XEDS)**

When using a TEM equipped with XEDS capabilities, XEDS is useful to quickly identify elements present within a TEM sample. Characteristic x-rays are generated from the sample due to incident electrons ionizing atoms within the sample. An electron from an outer electron shell fills the hole left by the core-shell electron,
resulting in an x-ray with that particular energy difference of the electron shells.

In this thesis, XEDS was used in STEM mode to collect elemental information within metal contact layers and as a function of probe position across the metal-semiconductor interfaces. However, XEDS was not used to quantitatively measure chemical composition of the layers because of the lack of standards. Instead, the relative concentrations of each element is analyzed based on the relative peak intensities from the collected spectra by standardless fitting (using theoretical k-factors to relate the two). Typically, there can be up to 10–20% error associated with this method [37], but it is still useful to qualitatively assess the chemical compositions within the contact layers.

1.4.2.5 Electron Energy Loss Spectroscopy (EELS)

To analyze very thin (< 3 nm) interfacial layers in XTEM of metal-semiconductor contacts, EELS analysis in STEM mode was used in addition to XEDS. EELS has several advantages over XEDS for this purpose. The spatial resolution in XEDS is inferior because there is an interaction volume in the sample associated with x-ray emission. There may also be spurious x-rays detected from either other areas in the sample or from the grid and holder.

In EELS, the electron beam is transmitted through the TEM sample, and the inelastic scattering energy losses are directly measured at that point in the sample. Thus, the spatial resolution is dependent on the probe size and the thickness of the sample. To determine elements present in such thin layers, it is useful to collect spectra in the high-energy loss portion of the EELS spectrum. In this area of the spectrum, the peaks are characteristic of the initial electron energy (TEM electron source) minus the binding energy of the electron for a certain element [38].

1.4.2.6 Atomic Force Microscopy (AFM)

AFM is used to physically probe a surface to determine the topography with a nanometer lateral resolution in three dimensions [39]. Typically, for inorganic materials and thin films, AFM is operated in tapping mode, where a very sharp Si tip (about 5 nm radius) is brought close to the surface of a sample (about 50–150 Å above the sample). The interatomic van der Waals forces between the tip and the atoms on the
surface are detected. The tip is oscillated at its resonant frequency as it continuously taps the surface and lifts off the surface. The oscillation frequency is maintained by an electronic feedback loop. A laser is directed on the top of the tip to determine the amount of deflection, which is then translated as the surface topography in the AFM image. AFM is very useful for quantifying surface parameters such as roughness, which is applicable to analyzing the surfaces of contact pads after annealing or the smoothness of the semiconductor epilayer.

1.4.2.7 Auger Electron Spectroscopy (AES)

AES is a versatile surface analysis technique that can be used to identify elemental composition of the atoms within a small sampling depth between 5–100 Å; it also has good spatial resolution and for some elements it can have a very low detectability limit of about 100 ppm [39]. Characteristic Auger electrons are generated from the sample due to incident electrons ionizing atoms within the sample. An electron from an outer shell electron fills the hole left by an ejected core-shell electron, resulting in the ejection of another outer shell electron which overcomes the binding energy of the core-shell electron and leaves with the remaining energy. In regards to analyzing the metal-semiconductor interfaces, AES can be used to determine the presence of elemental diffusion to the surface of the contacts.

1.5 Thesis Outline

This thesis is organized into seven chapters. Chapter 1 introduces the motivation for the work and the relevant background of metal-semiconductor interfaces and characterization techniques used. Chapter 2 contains a literature overview of the three types of ohmic contacts to n-In$_{0.53}$Ga$_{0.47}$As fabricated and studied in this thesis. The experimental methods used to fabricate and characterize these contacts are described in Chapter 3. Chapter 4 describes the fabrication and characterization of several planar, non-alloyed contacts to heavily-doped n$^+$-InGaAs and determination of effective Schottky barrier heights. The implications of the contact resistance behavior with respect to heat treatment and doping concentration are discussed. Chapter 5 describes the fabrication and characterization of non-alloyed contacts where the InGaAs
interface was modified to form nanopatterned features, and the effect on decreasing contact resistance. Chapter 6 describes the characterization of contacts formed via the solid-phase regrowth mechanism, which resulted in the introduction of doping at the metal/InGaAs interface. A summary of the thesis is contained in Chapter 7, along with proposals for future studies based on this work.
Chapter 2

Literature Review

2.1 Planar Contacts

2.1.1 Introduction

An alternative method to using the traditional liquid-phase regrowth or alloyed ohmic contacts used for III-V HEMT and MOS devices is to use non-alloyed, planar, shallow, ohmic contacts to a heavily-doped cap layer like n$^+$-InGaAs [17, 40]. Such contacts have been used with some success and have resulted in very low specific contact resistances of $< 10^{-7}$ Ω-cm$^2$ in many cases, as it has been demonstrated that very high doping concentrations leads to current transport via tunneling through a decreased depletion region [41, 42, 43]. These contacts are also desirable considering the importance of thermal stability during fabrication and operation of devices.

However, it is often challenging to create stable contacts to In-containing semiconductors such as InGaAs at high temperatures (300–450°C) as compared to GaAs because of the increased volatization of the As due to stronger bonding between In-Ga and In-As bonds [44, 45, 46]. Additionally, it is often difficult to compare the results and determine trends of various studies, as there are several important factors that are known to significantly affect the specific contact resistance of ohmic contacts to InGaAs, especially those prepared ex situ and at room temperature. Specifically, these studies often used a combination of various surface preparation techniques, deposition methods, metallizations, and heat-treatments.
2.1.2 Semiconductor Surface Before Contact Metallization

Various surface treatment methods have been found to result in widely varying specific contact resistance results. The main methods of surface treatment for preparing contacts to InGaAs, or the related materials GaAs or InAs, involve attempting to completely strip the native oxide in order to promote a clean and uniform surface, which is believed to promote a more intimate metal-semiconductor contact. Usually, acid or alkaline solutions and a subsequent rinsing in water are used to strip the native oxide. More recent reports have indicated that purposely growing an oxide on the surface by using UV-ozone treatment followed by removal of this oxide resulted in decreased specific contact resistance. For InGaAs, it has been found by various surface characterization techniques that due to oxidation, the semiconductor surface becomes As-rich due to the preferential formation of In and Ga oxides, with simultaneous reduction of As oxides to elemental As. This As-rich semiconductor surface is a result of the preferential formation of In and Ga oxides due to their lower formation energies.

After removal of the native oxide or of a grown oxide, various surface studies have also shown an As-rich semiconductor surface along with elemental As with thicknesses that correlate to the initial oxide layer [47]. Additionally, this elemental As layer has been found to have a higher binding energy than the As from the bulk InGaAs according to XPS studies. It has also been postulated that oxidation results in the replacement of As atoms with O, resulting in these excess As atoms with extra unbound electrons. Historically, surface states which accompany this As-rich surface along with subsequent Fermi-level pinning have impeded the efficacy of III-V MOS devices [27, 48]. A more complete review of InGaAs surfaces after surface oxidation and removal is available by Dormaier [49].

In that same study, Dormaier also used XPS surface analysis to correlate a variety of surface preparation treatments on InGaAs with the performance of Pd-based ohmic contacts, and discussed the implications for contacts based on other metals including TiW, Ti, Mo and Pt. It was found that the optimal surface preparation procedure for creating low-resistance ohmic contacts to InGaAs consisted of a 10 min UV-ozone treatment followed by a 2 min buffered oxide etch (BOE) and 15 s water rinse. An increased concentration of Ga oxides at the surface corresponded to an increase in
specific contact resistance, while the use of the UV-ozone treatment served to remove hydrocarbon residue on the surface, resulting in lower specific contact resistance.

The choice of deposition method may also affect the resulting specific contact resistance. Dormaier also found that the same contacts (TiW, Ti, and Mo) to n-InGaAs fabricated via sputtering versus electron-beam deposition resulted in lower specific contact resistances. During sputtering, extra metal atoms may physically penetrate the excess As layer due to the higher operating pressure and increased physical bombardment. The reason for the decrease in specific contact resistance may be due to the altered semiconductor surface as a result of increased physical bombardment of particles during sputter deposition. This effect can introduce the creation of defects, which may give rise to trap-assisted tunneling. Other types of enhanced current transport such as this, in addition to tunneling through a thin barrier due to heavy doping concentrations, have not been widely studied, and may in fact be quite important to consider for ohmic contacts to III-V materials.

2.1.3 Choice of Contact Metallization

Another factor that may affect the properties of ohmic contacts to InGaAs is the choice of metallization. However, the choice of metallization and its effect on the specific contact resistance has not been widely investigated for n-InGaAs, given uniform surface preparation methods. In general, the traditional non-alloyed ohmic contacts used are Ti-based metallizations. There have been many different results using Ti-based contacts albeit with various surface preparation, annealing and deposition conditions [50, 51, 52, 53, 54, 55, 56, 57, 58]. Other metals studied for contacting n-InGaAs include TiW [59, 60], Mo [61, 62, 63], Pd [57, 58, 64, 65], WSi [66, 67] and ErAs [68]. In consideration of uniform surface preparation and deposition methods, it is interesting to note that Dormaier et al. [32] suggests that there may be in fact some metal-dependent phenomena that is contributing to increased current transport in the case of certain metals, most notably Pd. In the following subsections, selected metal contacts will be reviewed; these metals were chosen because their variation in work functions and reactivities with InGaAs make it interesting to compare the resulting ohmic contact performance and can give insight into possible interface phenomena due to the choice of metal.
2.1.3.1 Titanium Based Contacts

As an alternative to the Ni-Ge-Au alloyed contact, Ti-based contacts have often been reported for non-alloyed ohmic contact schemes to n-InGaAs [53, 55, 63, 64] or graded InAs/InGaAs heterostructures [51, 52, 56, 66]. Compared to the Ni-Ge-Au scheme, the Ti/Pt/Au metallization used has better thermal stability with less degradation of specific contact resistance after annealing at temperatures from 300–400°C, as AuIn is shown to form along with the penetration of Au, Ni and Ge into the InGaAs layer while Ga and In penetrate into the metal. As-deposited, the Ti/Pt/Au contact was reported to have specific contact resistances with values of \( \rho_c \geq 2 \times 10^{-7} \Omega\cdot\text{cm}^2 \), using surface treatments consisting of NH\(_4\)OH or dilute acid to strip the native oxide, even on n\(^+\)-InGaAs layers with doping up to 5 \( \times \) 10\(^{19} \) cm\(^{-3}\). However, at higher annealing temperatures (> 300°C), degradation of the Ti/InGaAs interface often occurred in the form of outdiffusion of Ga, In and As into the Ti layer and the formation of TiAs phase [45, 55], resulting in non-uniform interfaces, slight consumption of the InGaAs layer and increased specific contact resistances. Ti/Pd/Au [59, 64, 69] contacts for n\(^+\)-InGaAs did not perform much better, and resulted in degradation after annealing at temperatures greater than 300°C.

TiW contacts [59, 60] have also been explored in order to improve upon the thermal stability of Ti/Pt/Au contacts. These contacts consisted of sputtered TiW deposited on n\(^+\)-InGaAs with Si doping of 3.5 \( \times \) 10\(^{19} \) and 5 \( \times \) 10\(^{18} \) cm\(^{-3}\) and surfaces treated using UV-ozone with either an NH\(_4\)OH or HCl rinse. Low specific contact resistances of 7.3 \( \times \) 10\(^{-9} \) and 1.29 \( \times \) 10\(^{-8} \) \( \Omega\cdot\text{cm}^2 \) with good thermal stability up to 500°C were reported. However the use of sputtering required more complex fabrication steps because of the increased difficulty of liftoff.

2.1.3.2 Molybdenum Based Contacts

For improved thermal stability, Mo has emerged as a candidate for contacting n-InGaAs because of its high melting point and relative ease of deposition with respect to other refractory metals such as W and Pt. Mo contacts to n-GaAs have also been shown to be stable up to 400°C [44]. Wakita et al. [63] measured Mo/Au contacts to Si-doped n\(^+\)-InGaAs with a carrier concentration of 2.4 \( \times \) 10\(^{19} \) cm\(^{-3}\). The surface was treated with dilute HF and acetic acid. The as-deposited specific contact resistance
was \( 2 \times 10^{-7} \ \Omega\text{-cm}^2 \) and this value only increased slightly upon annealing at 300°C for 2 h. Interestingly, they compared Mo contacts on both thick (> 20 nm) and thin (6–10 nm) InGaAs layers; the specific contact resistances for Mo contacts to thin InGaAs layers were higher. After annealing, XTEM indicated Mo had interdiffused with the very thin InGaAs layers, which correlated to a higher increase in specific contact resistance, while with the thick InGaAs layers, pockets of unidentified amorphous regions along the interface had formed.

More recently, very low specific contact resistances were reported of as-deposited 10 nm in situ [61] and 20 nm ex situ [62] Mo contacts to \( n^{+}-\text{In}_{0.53}\text{Ga}_{0.47}\text{As} \) with \( n = 3.6 \times 10^{19} \) and \( 4.8 \times 10^{19} \ \text{cm}^{-3} \), respectively. The in-situ Mo contacts had a measured \( \rho_c = 1.3 \times 10^{-8} \ \Omega\text{-cm}^2 \) but SIMS profiles showed out-diffusion of In and Ga into the Au layer and diffusion of Ti into the InGaAs layer after annealing at 400°C/1 min, which correlated to slight increase in specific contact resistance; they attributed this to porous gaps within the thin Mo layer. The as-deposited ex situ contacts showed comparable values of \( \rho_c = 1.1 \times 10^{-8} \) and \( 1.5 \times 10^{-8} \ \Omega\text{-cm}^2 \) for samples treated with UV-ozone/HCl/atomic H and UV-ozone/HCl cleaning, respectively.

### 2.1.3.3 Palladium Based Contacts

Palladium behaves much differently than either Ti or Mo when in contact with InGaAs. From previous studies of Pd reactions with GaAs and InGaAs, metastable Pd-GaAs [44] and Pd-InGaAs [70] phases form readily at low temperatures (< 300°C), and has the ability to uniformly penetrate the native oxide of the GaAs surface, unlike the similar metal Ni, whose reaction with GaAs can be inhibited by interfacial oxide layers [71]. Because of its high work function (5.12 eV), Pd is expected to produce a lower barrier height on p-InGaAs rather than n-InGaAs based on the Schottky-Mott model. Surprisingly, Pd contacts have been found to result in low specific contact resistances for both n and p-type GaAs and InGaAs [40, 57, 64, 65, 72, 73, 74]. This makes the Pd contact to InGaAs particularly attractive for devices where contacts are needed for n and p regions.

The formation of the Pd-GaAs phase at low temperatures has been thought to be the reason that the Pd contacts have shown improved thermal stability versus Ti or Pt contacts to GaAs. This phase was shown to be present even after annealing
at temperatures over 300°C, and the corresponding specific contact resistance values to p⁺-InGaAs stayed on the order of $10^{-6}$ Ω-cm² [64, 69, 74]. Chor et al. [65] measured a two times lower minimum specific contact resistance for Pd/Ti/Pt/Au and Pt/Ti/Pt/Au contacts versus Ti/Pd/Au contacts to p⁺-InGaAs doped to $1 \times 10^{19}$ cm⁻³; additionally, an optimal thickness of 10 nm was required for the Pd layer to result in the minimum specific contact resistance ($\rho_c \approx 1 \times 10^{-6}$ Ω-cm²) after annealing at 400°C. It was suggested that the initial layer thickness of Pd affected the phase formation of a Ga-rich Pd-GaAs phases at high temperature with optimal composition, corresponding to a minimum specific contact resistance, because of the amount of Pd available to form As-rich Pd-GaAs phases at lower temperatures. In contrast, a Ga-Ti-O layer was suggested to explain the degradation of the contact resistance in the case of the Ti/Pt/Au contact after annealing.

Dormaier’s [49] comparison of Mo-, Ti-, Pt- and Pd-based contacts to n-InGaAs with a constant surface preparation resulted in consistently low values for the Pd-based contacts, even after annealing. For as-deposited Pd-based contacts, it was proposed that enhanced tunneling due to the introduction of defect-assisted tunneling was occurring, as gap states might be present above the Fermi level due to the high work function of Pd. To explain the low resistance for the annealed Pd contacts, it was proposed that because of the fast diffusion of Pd within the InGaAs, trap-assisted tunneling may be enhanced by Pd interstitials beneath the interface as well as the reacted region. However, further interface characterization is needed in order to further confirm these ideas.

### 2.2 Nanopatterned Contacts

#### 2.2.1 Introduction

Even though non-alloyed contacts have been widely employed for heavily doped semiconductor layers with good success, there are still barriers to reducing the specific contact resistance, namely Fermi-level pinning [18, 40, 75] and limits in doping concentration with regards to solid solubility [75], necessitating alternative approaches of contact formation. One such approach takes into account interface morphology at the metal-semiconductor interface, which can play a significant role in the resulting
contact resistance.

The use of nanoscale features and patterned arrays has been proposed for metal-semiconductor contacts [76, 77]. For example, nanoparticles inserted within transparent ohmic contacts resulted in lower contact resistances and increased light extraction in light-emitting diodes [77], while nanoroughened surfaces have been considered as a strategy to lower ohmic contact resistance for wide bandgap semiconductors [76, 78, 79]. The desire to fabricate nanoscale features is also widespread for a number of electronic and optical applications, as they are useful for increasing surface area for catalytic growth surfaces [80] and for sensor devices [81, 82].

2.2.2 Fabrication Methods and Patterning

Nanoscale contacts have been investigated both theoretically [83, 84, 85] and experimentally [76, 78, 86] as an alternative method to reduce specific contact resistance. Enhanced conduction has been shown to occur in contacts with feature geometries approaching length scales on the order of the depletion width, due to a reduced barrier thickness, even without a reduction in the Schottky barrier height [85]. The presence of nanoscale features with sharp curvatures in silicide-Si shallow p-n junctions resulted in higher electric fields [83], allowing for a greater contribution of tunneling current towards the overall conductance. In the case of heavily doped semiconductors, it may be more difficult to incorporate nanoscale features with sizes approaching the proper length scales because of the few nanometer-sized depletion widths, but numerical modeling [84] has shown that such features could be advantageous in that they can also increase the active interfacial area of the contact, thereby contributing to a lower specific contact resistance.

Previous attempts to fabricate nanoscale features in semiconductors have involved modifying the semiconductor surface via wet chemical or dry etching before contact metal deposition; however, the decrease in specific contact resistance values was not sufficient [87, 88]. More recently, nanoscale contacts with etch masks fabricated non-lithographically have been explored. A porous anodic alumina template was deposited as a reactive ion etch (RIE) mask for lightly doped n-GaN [78], while a thin film of Ni was deposited and then annealed to form agglomerated islands to serve as a wet chemical etch mask for lightly doped p-GaN [86]. In these studies, it was concluded
that contacts deposited on the resulting nano-roughened surfaces, consisting of features with small radii of curvature, showed reduced contact resistances and effective Schottky barrier heights due to decreased depletion widths and increased contact area.

The main disadvantage of the aforementioned fabrication methods is the additional modification of the semiconductor surface before contact metallization, namely exposure to the mask components, polymers, and/or heat treatment. Also, it is desirable to control the dimensions of the etch mask in sub-100 nm length scales. Downey et al. [84] predicts that in order to maximize the tunneling current for a specific doping density, feature curvatures should approach the size of the barrier thickness (∼depletion width), and be placed a certain distance apart (∼2x depletion width) to prevent overlapping depletion regions.

2.2.3 Thin Film Deposition: Glancing Angle Deposition

In this thesis, the use of glancing angle deposition (GLAD) is proposed in order to deposit porous, dimensionally-controlled thin films to serve as etch masks for the semiconductor substrate in order to fabricate nanotopography. In GLAD, thin films of specific microstructure and density can be tailored three dimensionally on a nanometer scale through control of the substrate rotation with respect to the vapor flux [89, 90, 91, 92]. Porous and high surface area GLAD films consisting of a variety of morphologies, including pillars, zig-zags, and helices, have been fabricated and envisioned for use in applications such as sensors, catalysis, and optical interference filters [93, 94, 95, 96]. The development of such porous columnar microstructures is a result of allowing the vapor to arrive at the substrate at an oblique incident angle (α > 70° with respect to the substrate normal), as shown in Figure 2.1.

Due to the oblique deposition angle, shadowed regions are created opposite to the incident vapor and adjacent to initial atomic clusters formed during the nucleation stage, thus allowing subsequent vapor to deposit preferentially on the preexisting material. Under low adatom mobility conditions, growth of isolated columns with high porosity is favored mainly due to this enhanced atomic self-shadowing mechanism. These columns are tilted towards the incident vapor flux and are generally randomly distributed unless the substrate is deliberately patterned. Patterning introduces pref-
Figure 2.1. Typical electron beam evaporation configuration for GLAD. Flux is delivered at an oblique angle, $\alpha$, relative to the substrate normal.

differential nucleation sites, which can delay column extinction due to otherwise increased competition from surface diffusion [93, 94]. Substrate rotation is added in conjunction with the oblique angle flux deposition to control the shape of the columns on a nanometer scale; rotation can also help to orient the columns closer to normal to the substrate [91], as the vapor flux arrives from different directions.

The film density and columnar spacing has been found to be a direct function of the vapor incidence angle. The column spacing scales with the incidence angle according to $(1 + 1/\cos \alpha)$ [91]. Additionally, the size, spacing and densities of the isolated columns can be controlled by careful selection of the deposition material and deposition conditions. A material with low adatom mobility, i.e., high melting point, is more conducive to fabricating films with higher porosity and smaller column diameters. Important deposition parameters such as rate and thickness can be controlled relatively easily because conventional physical vapor deposition methods such as evaporation or sputtering are used in GLAD [92, 95]. The ability to tailor the size and spacing of the thin films of a variety of materials using GLAD potentially makes it a novel method to create features with specific dimensions in the sub-100 nm regime.
Furthermore, the porosity and anisotropic structure of GLAD thin films allows gases and liquids to penetrate between the isolated columns [90], possibly enabling their use as an etch mask. Utilizing a GLAD film as a wet chemical etch mask allows for more customization and less expense compared to traditional methods such as e-beam lithography. The substrate should also incur less damage than if otherwise subjected to annealing or dry etching. Most significantly, an etch mask with nanometer scale openings can be fabricated.

2.3 Solid-Phase Regrowth (SPR) Contacts

2.3.1 Introduction

Another method of engineering the metal/semiconductor contact interface is by introducing excess doping through specific metallurgical interactions with the metal contacting layer through annealing. Annealing at temperatures near the eutectic temperature of the metal-semiconductor system can cause the compound semiconductor to dissolve, followed by the regrowth or precipitation of the semiconductor that is heavily-doped by the metal overlayer or of the formation of an alloyed epitaxial layer [71, 97, 98].

The widely used Ni-Ge-Au contact to GaAs is formed through a liquid-phase regrowth process [17]. In this process, the contact melts after annealing at temperatures greater than the Au-Ge eutectic temperature of 361°C, causing GaAs to dissolve. Upon cooling, a solid GaAs phase doped heavily with Ge regrows above the underlying GaAs, contributing to the contact’s ohmic characteristics. However, these contacts provide unsatisfactory morphology, as they can react quite deeply and show substantial lateral diffusion due to the presence of a liquid phase at the interface. Thus, these liquid-phase regrowth contacts are unsuitable for contacting shallow junctions and for use in new devices that require the utmost control of extremely small contact dimensions.

Solid-phase regrowth (SPR) contacts have been studied extensively since the 1980s as an alternative method to forming alloyed contacts to III-V based devices. The SPR process involves a regrowth mechanism involving solid-state reactions occurring at temperatures substantially below the melting point of the interfacial phases, resulting
in regrown layers that are laterally uniform. This mechanism was first described on III-V semiconductors, specifically n-GaAs, by Sands, Marshall and Wang in 1988 [98], and has since been demonstrated and expanded upon using several different metal-III-V semiconductor systems.

2.3.2 Solid-Phase Regrowth Mechanism

The SPR mechanism consists of a series of solid-state reactions occurring at several temperatures. Typically, a near-noble metal such as Pd or Ni is used as the first contacting layer. The use of these metals is necessary for the SPR mechanism and they provide several advantages. Pd and Ni react to form compounds with GaAs in the solid state at low temperatures (≲ 200°C), and they are easy to deposit using typical physical vapor deposition techniques [99, 100]. Pd is preferred as the initial metal layer because Ni reacts much more deeply with GaAs than Pd.

![Figure 2.2. The SPR mechanism. (Adapted from [97]).](image)

The SPR mechanism is shown schematically in Figure 2.2 for an Si/Pd/n-GaAs system. First, the reactive metal (M = Pd) consumes the semiconductor to form a metastable M-III-V compound at low annealing temperatures. This compound then reacts with the Si (or Ge) overlayer to form a M-silicide (or M-germanide). The silicide is thermodynamically stable and drives a decomposition reaction of the M-III-V compound. Epitaxial regrowth of the adjacent crystalline semiconductor occurs as a result. Excess Si is then transported to the regrown III-V region, forming a thin, heavily-doped n⁺-GaAs layer at the M-silicide/GaAs interface. The following
equations may be used to describe this SPR mechanism.

\[ 4\text{Pd} + \text{GaAs} \rightarrow \text{Pd}_4\text{GaAs} \quad (2.1) \]

\[ \text{Si} + 2\text{Pd} \rightarrow \text{Pd}_2\text{Si} \quad (2.2) \]

\[ 2\text{Si} + \text{Pd}_4\text{GaAs(Si)} \rightarrow 2\text{Pd}_2\text{Si} + \text{GaAs(Si)} \quad (2.3) \]

The overlayer metal is chosen carefully in order to ensure that the decomposition reaction of the intermediate phase is driven to the right. Because Si and Ge are n-type dopants for GaAs and InGaAs, and because of the high stability of silicides and germanides, these metals are particularly good overlayer candidates for forming low resistivity SPR contacts. The resulting electrical performance of the contact however depends on the extent of the reactions throughout the SPR process and the resulting morphology at the interface, and thus can vary depending on the combination of metal selection and layer thicknesses, and the exact annealing temperatures, times and environments.

2.3.3 SPR Contacts to n-GaAs and n-InGaAs

SPR contacts to n-GaAs with the Pd/Ge and Pd/Si base structure have been studied the most extensively and result in the lowest specific contact resistances \(< 10^{-7} \ \Omega\text{-cm}^2\) compared to other bilayer structures, such as Pd/In [101, 102, 103], Ge/Ni [104] and Ni/Si [100, 105]. The SPR mechanism differs slightly between the Pd/Ge and Pd/Si system, as well as the resulting morphology and thermal stability. While most SPR contact studies were done on n-GaAs, there have been only a few studies done on n-InGaAs and p-GaAs.

2.3.3.1 Pd/Ge Contacts

The first SPR Pd/Ge contact to n-GaAs was demonstrated by Marshall [106]. After annealing, the Pd was found to react completely with a thicker Ge layer to form PdGe with excess amorphous Ge. The excess Ge is then transported to the
GaAs interface and forms an epitaxial Ge layer above the GaAs. This contact resulted in specific contact resistance of \( < 10^{-6} \ \Omega\text{-cm}^2 \). In order to maintain this low value, it was found that the Ge layer had to be 50 nm thicker than the Pd layer and that there needed to be a minimum initial thickness of Pd. Initially, the low specific contact resistance was thought to be due primarily to the small conduction band discontinuity at the Ge/GaAs interface and thus a lower effective barrier height. Later, low-temperature measurements revealed that the current transport was due to tunneling, most likely through a thin n\textsuperscript{+}-GaAs layer at the interface. TEM, Rutherford backscattering (RBS) and X-ray diffraction (XRD) characterization after annealing at low temperatures further revealed the formation of a thin Pd\textsubscript{x}GaAs layer that later decomposed at higher temperatures [107]. These early studies revealed that the layer thicknesses, the interaction between the Pd and GaAs, the formation of the intermediate Pd\textsubscript{x}GaAs phase, and the presence of an n\textsuperscript{+}-GaAs layer are all important in determining the electrical characteristics of the contact. Indeed, many subsequent studies have shown evidence of this SPR mechanism for various Pd/Ge contacts to n-GaAs and n-InGaAs that result in quite low specific contact resistances ranging from 2–5 \( \times 10^{-7} \ \Omega\text{-cm}^2 \) with different original semiconductor doping concentrations [108, 109, 110, 111, 112, 113, 114, 115, 116].

Pd/Ge contacts to n-InGaAs have not been studied as extensively as for n-GaAs. However, there is evidence that the analogous series of reactions occurs via the SPR mechanism with Pd/Ge contacts to GaAs, and that the resulting planar contact is formed with minimal consumption of the semiconductor after annealing [70, 117, 118, 119]. Ressel et al. [70] studied a Pd/Ge contact deposited on In\textsubscript{0.53}Ga\textsubscript{0.47}As using XTEM and showed the formation of a polycrystalline, hexagonal Pd\textsubscript{4}In\textsubscript{0.53}Ga\textsubscript{0.47}As layer after annealing at 225\degree C. This phase then decomposes at higher temperatures and regrowth of the InGaAs occurs; Ge then grows epitaxially higher than 350\degree C. Yeh et al. [119] measured specific contact resistances as low as 2 \( \times 10^{-7} \ \Omega\text{-cm}^2 \) for Pd/Ge contacts annealed at 425\degree C and 60 s. They also used SIMS analysis to explain that the outdiffusion of Ga and In to the contact layer due to dissociation of InGaAs during the SPR process resulted in Ga and In vacancies in the InGaAs that allow Ge to occupy these sites to heavily dope the semiconductor.
2.3.3.2 Pd/Si Contacts

SPR Pd/Si contacts differ slightly from the Pd/Ge contacts in that solid phase transport and epitaxial growth of Si do not occur at annealing temperatures below 400°C [97]. However, analogous to the Pd/Ge contacts, an epitaxial Pd$_x$GaAs was also formed at low annealing temperatures. At higher annealing temperatures though, contacts became ohmic and a Pd$_x$Si layer was found adjacent to the GaAs interface. Thus it was also speculated that a thin n$^+$-GaAs layer was formed as a result of the SPR process in this system. The formation of this heavily-doped GaAs layer may be a result of Si diffusion into the intermediate Pd$_x$GaAs compound before regrowth. The Si is then transported to the regrown GaAs where it preferentially occupies Ga sites. It was found that this mechanism is a likely possibility because the Pd$_x$GaAs phase is slightly As rich [97, 120], and because Pd$_x$GaAs and Pd$_2$Si were found to have the same crystal structure [121], enabling Si to diffuse through the the Pd$_2$Si lattice easily at the intermediate annealing temperatures. The thickness of the regrown layer was shown to be about 10 nm, and a thin n$^+$ surface layer was shown to be responsible for the tunneling current transport seen in these contacts [122].

The Pd/Si contacts still resulted in consistently higher specific contact resistances than the Pd/Ge contacts, possibly due to higher melting point of Si. However, the Pd/Si contacts have better thermal stability while still showing uniform interfaces and surface morphologies [122, 123, 124, 125]. The specific contact resistance of these contacts has been improved slightly by adding additional thin layers of Si or Ge within the Pd layer before the annealing process. The specific contact resistance achieved in this study was 2–4 × 10$^{-7}$ Ω-cm$^2$ [123]. In comparison, the poor thermal stability of the Pd/Ge contacts may be due to the interdiffusion of Ge with GaAs at the interface [109, 110].

Pd/Si contacts to InGaAs have only been fabricated in a few more recent studies [126, 127]. In these studies, the lowest achieved specific contact resistance was 3.9 × 10$^{-7}$ Ω-cm$^2$ after annealing at 400°C for 20 s for an n-InGaAs epilayer doped 1 × 10$^{19}$ cm$^{-3}$. Using XRD it was concluded that Pd$_2$Si was formed after annealing at temperatures greater than 375 and 30 s, coinciding with when the specific contact resistances dropped to < 10$^{-6}$ Ω-cm$^2$. The contacts also remained relatively stable at annealing temperatures up to 450°C and had uniform interfaces with minimal voids.
at the metal-semiconductor interface. However, the SPR process was not verified comprehensively in these studies.

2.3.3.3 Effect of Layer Thicknesses

The electrical properties of the Pd/Ge and Pd/Si SPR contacts were found to vary according to the different combinations of metal layers with respect to layer thicknesses. It is generally observed that for regrowth to occur in the Pd/Ge system, an excess of the Ge overlayer is required, where the Ge/Pd thickness ratio is greater than 1, to enable the stoichiometric PdGe phase to form [128]. The excess Ge may also be necessary in order to prevent binary Pd$_2$Ge, PdAs$_2$ and PdGa phases from forming and contributing to less uniform contact metallurgy [129]. Hao et al. [130] showed that the Pd/Ge layer thickness ratio was important to achieving low specific contact resistance to GaAs; the same ratio with different thicknesses resulted in similar specific contact resistances for a constant annealing condition at 340°C for 30 min. Kim et al. [118] compared a Pd/Ge and Pd/Ge/Pd contact to n-InGaAs. The Pd/Ge/Pd contact achieved a slightly lower specific contact resistance compared to the Pd/Ge contact ($1.1 \times 10^{-6}$ versus $3.7 \times 10^{-6} \text{\Omega-cm}^2$), but they did not explain whether the different metal structure contributed to this slight decrease.

In the case of Pd/Si SPR contacts to GaAs, a study by Wang et al. [122] fabricated ohmic contacts with initial atomic Si/Pd ratios $\geq 0.65$ and $< 0.65$. They found that excess Si was necessary in order to form ohmic contacts after annealing at 375°C for 30 min, and that the excess Si could also retard contact degradation. RBS analysis showed that the Pd was consumed completely to form a Pd disilicide and an amorphous Si layer containing some Pd was leftover. However, for Si/Pd ratio $\sim 0.53$, contacts were non-ohmic for annealing temperatures between 250 and 600°C. It is clear that an excess of the overlayer metal is needed in order for the SPR process to occur and ultimately form ohmic contact properties; however additional layers within the contact stack may also affect the precise starting ratio required of the Pd/Si or Pd/Ge layers.
Experimental Methods

3.1 Planar Contacts

3.1.1 Fabrication of Contacts

Non-alloyed contacts were fabricated on epitaxial layers of Si-doped In$_{0.53}$Ga$_{0.47}$As grown by metal-organic vapor phase epitaxy (MOVPE) on semi-insulating InP wafers. Both lightly-doped ($N_D = 5 \times 10^{17}$ cm$^{-3}$) and heavily-doped ($N_D = 3 \times 10^{19}$ cm$^{-3}$) epilayers with thicknesses of 50 nm were used. Individual samples consisted of cleaved sections 1×1 cm or less in size.

3.1.1.1 Photolithography

Immediately prior to photolithography, all samples were first degreased in acetone, isopropanol and de-ionized (DI) water in an ultrasonicator for 1 min each and blown dry with compressed nitrogen. The samples were then dehydration baked for at least 1 min at 100°C or greater. A GCA 8000 i-Line Stepper was used to optically expose a dual-layer resist stack consisting of NANO SF9/SPR3012, followed by development using CD-26 (tetramethyl ammonium hydroxide, or TMAH), deep UV flood exposure and final development using PMGI XP101A (tetraethylammonium hydroxide solution).

Circular transmission line method (CTLM) test structures with nominal gap spacings of 0.5–20 μm were defined on the lightly-doped epilayers. Similarly, refined trans-
Table 3.1. As-deposited contacts to $n^+\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ ($N_D = 3 \times 10^{19} \text{ cm}^{-3}$) with Ti/Pt/Au (15/15/100 nm) diffusion barrier.

<table>
<thead>
<tr>
<th>Sample</th>
<th>Contact Metal</th>
<th>Thickness (nm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>A1</td>
<td>Ti</td>
<td>15</td>
</tr>
<tr>
<td>A2</td>
<td>Mo</td>
<td>30</td>
</tr>
<tr>
<td>A3</td>
<td>Pt</td>
<td>5</td>
</tr>
<tr>
<td>A4</td>
<td>Pd</td>
<td>2</td>
</tr>
<tr>
<td>B1</td>
<td>Mo</td>
<td>9</td>
</tr>
<tr>
<td>B2</td>
<td>Pt</td>
<td>9</td>
</tr>
<tr>
<td>B3</td>
<td>Pd</td>
<td>9</td>
</tr>
</tbody>
</table>

mission line method (RTLM) test structures with nominal gap spacings of 0.6-10 µm were defined on the heavily-doped epilayers.

3.1.1.2 Surface Preparation and Metallization

After photolithography, samples were subjected to a UV-ozone surface treatment for 10 min at 0.9 SLPM in an 80% nitrogen/20% oxygen atmosphere, where the samples were placed 4 cm below the lamp (PR-100 UV-Ozone Photoreactor, UVP, Inc., San Gabriel, CA). The UV-ozone treatment serves to remove organic contaminants and to grow a uniform oxide layer about 1-2 nm thick [73]. Afterwards, the oxide was etched using a buffered oxide etch (BOE) solution (10:1) for 2 min. The samples were immediately loaded into an electron beam evaporation chamber.

Metal sources were loaded into the deposition chamber at least 12 hours beforehand and pumped down. After loading the samples, the chamber was pumped down to a base pressure of less than $3 \times 10^{-7}$ in about 90 min. First, a titanium getter was performed by evaporating Ti evaporant for about 2 min while the samples were shielded from the electron beam source in order to further minimize residual oxygen within the chamber. Metallizations consisted of an initial contacting metal of Ti, Mo, Pd or Pt of varying thicknesses followed by a Ti/Pt/Au diffusion barrier. The metal sources have the following purities: Ti (99.995%), Mo (99.95%), Pd (99.95%), Pt (99.99%), Au (99.999%). Table 3.1 shows the varying metallizations of the as-deposited contacts to the heavily-doped epilayer. To reduce heating of the sample during deposition, a 30 min cool-down period was allowed between the deposition of the Ti and Au layers.
3.1.1.3 Liftoff, Mesa Alignment and Etching

After metal deposition, samples were placed in a solution of Remover PG (n-methyl pyrrolidinone) for standard liftoff of photoresist. For those samples patterned with the RTLM test structure, a second photolithography step was required in order to fabricate mesa etch masks for current isolation around the contact pads. SPR3012 resist was spun on these samples followed by proper alignment of the mesa mask, exposure and development. The exposed InGaAs areas were wet-etched for 80 s at room temperature using a solution of lactic acid, phosphoric acid, anhydrous citric acid, and hydrogen peroxide (6 mL:1 mL:1 g:1 mL), as prepared previously by Dormaier et al. [32], followed by removal of the etch mask. The resulting mesa edges have a maximum tolerance of < 500 nm wider than the edge of the metal pads.

3.1.1.4 Thermal Annealing

Select contacts (B1, B2, B3 of Table 3.1) were annealed in a Thermolyne 79400 tube furnace in a gettered argon ambient in order to study the contact properties after heat treatment. The annealing conditions for these contacts were 350°C for 1 hour. RTLM gap edges were observed after annealing by SEM in order to confirm that there was negligible lateral diffusion of the metal before performing I-V measurements.

3.1.2 Electrical Measurements

Four-point probe current-voltage (I-V) measurements were performed with a Keithley 238 parameter analyzer with linear current sweep and voltage measurement. At least four sets of CTLM or RTLM patterns were measured for each sample. For both CTLM and RTLM I-V measurements, the average resistance for each gap was calculated from the measured resistances in the range of -0.6 mA to +0.6 mA.

Gap spacings and mesa widths were measured using SEM and calibrated with a magnification reference standard (MRS-3, Geller Microanalytical Laboratories) at the same working distances. Specific contact resistance, sheet resistance, total contact resistance, and transfer length values were then extracted from plots of resistance versus gap spacing. CTLM data points were fitted using the Levenberg-Marquardt method and RTLM data points were fitted using the linear least squares method.
3.1.3 TEM Characterization

After contact fabrication and I-V characterization, select samples were examined by cross-sectional TEM (XTEM) to study the contact interface morphology.

3.1.3.1 Sample Preparation Using Focused Ion Beam

All samples were first sputter-coated with a 100 nm protective layer of tantalum. An FEI Quanta 200 3D Dual Beam Focused Ion Beam was used to lift out thin cross-sections from specific sites located adjacent to gap/metal-semiconductor contact edges. Protective layers of Pt were deposited by e-beam, and then by ion-beam gas assisted chemical vapor deposition within the chamber. Lift-out was performed using the Hitachi Method. Specimens were then transferred to a copper Omniprobe half-grid using an Omniprobe tungsten manipulator and finally thinned to electron transparency.

3.1.3.2 Morphological and Chemical Analysis

XTEM images were taken on a JEOL 2010F field emission microscope. Bright field (BF) and high angle annular dark field (HAADF) scanning TEM (STEM) images were taken. STEM images were taken using a probe size of 0.7 nm. Selected area electron diffraction (SAED) and fast Fourier transform (FFT) images were acquired to provide phase information on certain layers of the samples. DigitalMicrograph (Gatan, Inc.) was used to obtain calibrated FFT images from the recorded micrographs.

X-ray energy dispersive spectroscopy (XEDS) was performed to detect elements present in the cross-sectional samples. Drift-corrected spot scans and line scans were taken as needed. ESVision (Emispec/FEI) was used to perform background Brehmsstrahlung signal removal. In ESVision, a third order polynomial function is fitted to each manually specified background region in a spectrum. In the background regions of the elemental peaks, a cubic spline of the adjacent background area is used to model these regions. The polynomial fit is then subtracted from the spectrum. Standardless peak fitting was used, where peaks in the spectrum are fitted to theoretical Gaussian peaks, and subsequent integrated intensities are calculated. From this peak fitting routine, atomic percentages were determined using calculated k-values and a thin-foil approximation.
Electron energy loss spectroscopy (EELS) was used to determine chemical composition from layers within the cross-sectional samples. A probe size of 0.5 nm was used to collect EELS spectra in DF detection mode with a 2 mm aperture and a camera length of 15 cm. Spectra were collected starting from 350 eV with a dispersion of 0.50 eV/channel. Drift corrected line scans were taken as needed. DigitalMicrograph was used to quantify the spectra and perform background subtraction according to a power law fit. Intensities of peak edges were then plotted over the electron energy loss.

3.1.4 I-V-T Measurements

A Lakeshore cryogenic probe station and a Hewlett-Packard 4156A Semiconductor Parameter Analyzer were used to perform four-point probe I-V measurements at 77 and 220 K. Lightly-doped n-InGaAs as-deposited contacts with Mo/Ti/Pt/Au (9/15/15/100) and Pd/Ti/Pt/Au (2/10/15/70 nm) were measured with linear current sweep and voltage measurement. High-temperature I-V measurements were also taken for the same contacts at 350 and 400 K on a hot stage (Signatone, Model S-1045) using a Keithley 238 parameter analyzer with linear current sweep and voltage measurement. After each elevated temperature measurement, the contact was remeasured at room temperature to ensure that there were no irreversible changes in electrical performance due to possible higher temperature reactions. The average resistance for each gap was calculated from the measured resistances in the range of -1 mA to +1 mA. The gap spacing measurements for all I-V-T measurements used were the same as taken initially at room temperature. Average specific contact resistances were calculated over four CTLM sets at each temperature.

3.1.4.1 Barrier Height Calculations

The specific contact resistance data for the Pd and Mo contact was plotted as a function of measurement temperature. n-In$_{0.53}$Ga$_{0.47}$As with carrier concentrations $n = 5 \times 10^{17}$ and $3 \times 10^{19}$ cm$^{-3}$, respectively, were used in the calculations. Using the FE, TFE and TE current transport equations as described in Appendix A, the theoretical specific contact resistance values were plotted over the range of the measurement temperatures given various barrier heights. These curves were then compared to the
experimental data in order to determine the lower and upper bounds regarding the barrier height and the best curve fit to the experimental data.

3.2 Nanopatterned Contacts

3.2.1 Initial Wet Etch Calibration and Thin GLAD Etch Masks

3.2.1.1 Samples, Materials and Etchants

All samples used for the fabrication of nanopatterned contacts were Si-doped In$_{0.53}$Ga$_{0.47}$As grown by MOVPE on semi-insulating InP wafers. Wafers with both lightly-doped ($N_D = 1 \times 10^{17}$ cm$^{-3}$) and heavily-doped ($N_D = 3 \times 10^{19}$ cm$^{-3}$) epilayers with thicknesses of 250 nm and 50 nm, respectively, were used.

Metal films were deposited via GLAD on InGaAs substrates at various angles ($\alpha = 75–85^\circ$) and thicknesses (< 20 nm) to initially serve as the etch mask material. TiB$_2$ was initially chosen because of its high melting point (2920°C), which makes it a good candidate to form porous films using GLAD due to the relatively low adatom mobility, and relative ease of evaporation. Citric acid (CA):hydrogen peroxide (H$_2$O$_2$) wet etchant solutions with various ratios were initially chosen as the InGaAs etchant. This wet etchant is well-known and commonly used for etching InGaAs. The etch mechanism can be described as a series of reactions, where the H$_2$O$_2$ oxidizes the surface of the InGaAs, and then the citric acid subsequently removes the oxidized layer [131]. Finally, an HF:NH$_4$F (10:1) (i.e. buffered oxide etch, BOE) solution was used as the TiB$_2$ etchant. After each etch step, a 15 s DI water rinse was performed. A schematic of the desired process flow is shown in Figure 3.1.

3.2.1.2 Etch Rate Calibration and Selectivity Testing

The CA:H$_2$O$_2$ etchant for the InGaAs was first tested in order to ensure that the etch rate for the InGaAs was much faster compared to the TiB$_2$ (high selectivity for InGaAs over TiB$_2$), and the BOE etchant was tested in order to ensure that it would completely etch the TiB$_2$ but would not appreciably etch the InGaAs substrate.
First, anhydrous citric acid was dissolved in DI water at a ratio of 1 g:1 mL and continuously stirred for at least 12 hours to ensure complete dissolution. Various volumes of 30% H$_2$O$_2$ were then mixed in with this solution to form the final CA:H$_2$O$_2$ etchant with ratios of 50:1, 20:1, 10:1 and 5:1. The CA:H$_2$O$_2$ wet etchant of different ratios was used in order to calibrate an etch rate on the lightly-doped InGaAs epilayers. No special surface treatment was performed on the InGaAs before etching. A small drop of polymethyl methacrylate (PMMA) photoresist was deposited on the surface of the samples and left to cure on a hot plate at 60°C for a few minutes. The samples were then submerged into the CA:H$_2$O$_2$ wet etchant solutions for various times and rinsed for at least 15 s with DI water and blown dry with N$_2$. The etch depth was measured using contact profilometry, using at least 6 measurements and taking the average. Optical profilometry was used to confirm the results from contact profilometry when possible.

To test the selectivity of the CA:H$_2$O$_2$ wet etchant for InGaAs over TiB$_2$, this etchant was used to measure etch depths on a planar TiB$_2$ thin film of about 137 nm deposited by e-beam evaporation, and a GLAD TiB$_2$ film of about 50 nm. The CA:H$_2$O$_2$ solution with 50:1 ratio was ultimately selected due to its slower etch rate of InGaAs, and relatively high selectivity over TiB$_2$. The etch depth and rates of this solution for the planar TiB$_2$ versus the GLAD TiB$_2$ film were more difficult to measure by contact profilometry due to the extreme roughness of the GLAD film. However, the etch rate of the GLAD film was not substantially faster than the planar film since the film was still visible by eye even for the fastest etch times used. The 50:1 CA:H$_2$O$_2$ was then calibrated further for the etch rate using several different etch
times on the same sample. Both lightly-doped and heavily-doped InGaAs samples were tested to confirm that the etch rate did not change with doping.

### 3.2.1.3 Confirmation of 2-Step Etch Process

In order to further confirm the high selectivity of the CA:H$_2$O$_2$ (50:1) wet etchant of InGaAs over TiB$_2$ and the complete removal of the TiB$_2$ thin film, AES was performed on the surfaces after each step in the process using an FE Auger Electron Spectrometer. Two control samples were also measured, a planar TiB$_2$ film $\approx 137$ nm thick deposited on Si and the as-received InGaAs epilayer. Thin ($\approx 3$ nm) and thick ($\approx 50$ nm) GLAD TiB$_2$ films deposited on InGaAs were selected and subjected to the 2-step etch process. The first etch step consisted of a 14 s etch of the InGaAs using the 50:1 CA:H$_2$O$_2$ solution; the second etch step consisted of a 2 min BOE etch to completely remove the TiB$_2$ film. The AES surface scans were taken from 50–1300 eV with a 0.2 eV/step resolution with at least 5 cycles each. A 5 point Savitzky and Golay (SG) quadratic polynomial smoothing and differentiation routine was performed on the data in CasaXPS (Casa Software Ltd.).

AFM scans were also performed on the surfaces of these same samples at each step to observe changes in root mean square (RMS) roughness. Another as-received sample (with no TiB$_2$ etch mask) etched with 50:1 CA:H$_2$O$_2$ was also scanned, in order to compare its roughness with the other samples that had undergone the 2-step etch process.

### 3.2.1.4 Contact Fabrication

Samples prepared for contact fabrication were cleaved into sections $1 \times 1$ cm or less in size. Immediately prior to photolithography, all samples were first degreased in acetone, methanol and DI water in an ultrasonicator for 1 min each and blown dry with compressed nitrogen. The samples were then dehydration baked for at least 1 min at 100°C or greater. A GCA 8000 i-Line Stepper was used to optically expose a dual-layer resist stack consisting of NANO SF6/SPR3012, followed by development using CD-26, deep UV flood exposure and final development using PMGI XP101A. CTLM test structures with inner diameters of 80 $\mu$m and nominal gap spacings of 0.5-20 $\mu$m were defined on the lightly-doped and heavily-doped epilayers.
After photolithography, samples were cleaved into smaller samples consisting of at least 4 CTLM sets per sample. These samples were then divided into pairs, where one served as a control sample, while the other one underwent the GLAD etch mask deposition and subsequent 2-step etching procedure.

Before metal deposition, each pair of samples was subjected to a UV-ozone surface treatment for 10 min at 0.9 SLPM in an 80% nitrogen/20% oxygen atmosphere, where the samples were placed 4 cm below the lamp. Afterwards, the oxide was etched using a BOE (10:1) for 2 min. The samples were immediately loaded into an electron beam evaporation chamber.

The chamber was pumped down to a base pressure of less than $3 \times 10^{-7}$. First, a titanium getter was performed by evaporating Ti (99.995%) evaporant for about 2 min while the samples were shielded from the electron beam source in order to further minimize residual oxygen within the chamber. The following metal contact layers were then deposited in the following order: Pd (99.95%) or Ti, followed by a diffusion barrier consisting of Pt (99.99%) and Au (99.999%); the evaporation rates for each were 1.0 or 2.5, 2.0, and 1.0 Å/s, respectively. The thicknesses of the Pd and Ti were 3 nm and 10 nm, respectively, while the Pt/Au barrier was 25/70 nm. After metal deposition, liftoff was performed by placing the samples in Remover PG.

### 3.2.1.5 Electrical Characterization

Four-point probe I-V measurements were performed with a Keithley 238 parameter analyzer with linear current sweep and voltage measurement. At least four sets of CTLM patterns were measured for each sample. For the CTLM I-V measurements, the average resistance for each gap was calculated from the measured resistances in the range of -0.1 mA to +0.1 mA.

Gap spacings and mesa widths were measured using SEM and calibrated with a magnification reference standard (MRS-3, Geller Microanalytical Laboratories) at the same working distances. Specific contact resistance, sheet resistance, total contact resistance, and transfer length values were then extracted from plots of resistance versus gap spacing. CTLM data points were fitted using the Levenberg-Marquardt method.
3.2.1.6 Quantification of Surface Morphology

An AFM (Veeco Nanoscope) with a < 5 nm radius Si tip operated in non-contact, tapping mode was used to characterize the size and depth of the possible features using blank, witness samples with the GLAD TiB$_2$ etch mask that concurrently underwent the two-step etching procedure and the same surface treatment but that were not subjected to the contact metal deposition. The surface morphologies after the GLAD of the TiB$_2$ etch mask, two-step etching process, and surface preparation before each contact deposition was compared to the surface of degreased, as-received InGaAs pieces. The change in RMS roughness ($R_q$) and surface area were determined using AFM imaging analysis software (Digital Instruments NanoScope). The quantitative average width of the features was determined using a 2-dimensional power spectral density (2DPSD) function. The PSD function is a Fourier transform of surface heights in the image; the 2DPSD represents the variation of PSD magnitude as a function of the spatial frequencies [94, 132].

3.2.2 Development of Thick GLAD Etch Masks

3.2.2.1 GLAD Parameter Testing

A series of TiB$_2$ GLAD films were deposited on InGaAs epilayers cleaved into pieces of the size 1x1 cm. The epilayers were degreased using acetone, methanol and DI water. The samples were then submerged in BOE (10:1) for 2 min before loading into the evaporation chamber.

During the GLAD evaporation, the evaporation rate used was based on the quartz crystal monitor which was originally calibrated for a normal deposition. The starting amount of TiB$_2$ source material was measured out to be approximately 8 g for each deposition.

After deposition, the surface morphology of the films was observed using FESEM. Small pieces were cleaved off in order to look at the fracture cross-sections, which were mounted on a stub perpendicular to the electron beam in the SEM. The InGaAs epilayer was always measured along with the film thickness, in order to take into account the actual tilt of the sample. The tilt of the sample was calculated based on comparing the measured epilayer with the nominal thicknesses given. The actual
film thickness was then calculated using this calculated tilt angle.

3.2.2.2 Three-Step Etch Process and Contact Fabrication

Moderately-doped n-InGaAs epilayers with $N_D = 5 \times 10^{17} \text{ cm}^{-3}$ with a thickness of 50 nm were used. For each set of samples, both CTLM patterned samples and blank samples were loaded into the evaporation chamber after undergoing a UV-ozone clean for 10 min at 1.0 SLPM and 4 cm below the lamp, and a 2 min BOE strip. The GLAD film was then deposited with varying thicknesses at a vapor angle of 80 degrees.

A modified 3-step etch process was ultimately used before fabricating the final set of contacts. The first step consisted of using a diluted BOE (10:1) solution containing 90% DI water:10% BOE. The diluted BOE etch was then applied at various times, followed by the InGaAs etch using either the wet or dry etch, and finally the TiB$_2$ film was completely removed using BOE solution.

Three modified samples and one unmodified sample, all with at least 4 CTLM patterns each, were then prepared for concurrent contact deposition. The samples underwent a UV-ozone clean for 10 min, followed by a 2 min BOE strip, along with 3 blank, modified witness samples of the same GLAD and etching conditions. The samples were submerged concurrently during the BOE strip, and then always rinsed in DI water for 15 s before loading into the evaporation chamber. Ti/Pt/Au contacts with thicknesses of 9/15/100 nm were deposited on the 4 CTLM patterned samples. Following deposition, lift-off was performed. I-V measurements and analysis were performed on all contacts, using the methods described previously.

3.3 Solid-Phase Regrowth Contacts

3.3.1 Fabrication of Contacts

The SPR contacts were fabricated on epitaxial layers of Si-doped In$_{0.53}$Ga$_{0.47}$As grown by MOVPE on semi-insulating InP wafers. Both lightly-doped ($N_D = 1 \times 10^{17} \text{ cm}^{-3}$) and heavily-doped ($N_D = 3 \times 10^{19} \text{ cm}^{-3}$) epilayers with thicknesses of 250 nm and 50 nm, respectively, were used. Additional SPR contacts were fabricated on 30
nm epitaxial layers of heavily Be-doped In$_x$Ga$_{1-x}$As ($N_A > 5 \times 10^{19}$ cm$^{-3}$, where $x = 0.50 - 0.47$) grown by molecular-beam epitaxy (MBE) on 200 nm unintentionally doped (UID) InP on semi-insulating InP wafers. Individual samples consisted of cleaved sections 1×1 cm or less in size.

### 3.3.1.1 Photolithography

Immediately prior to photolithography, all samples were first degreased in acetone, isopropanol and DI water in an ultrasonicator for 1 min each and blown dry with compressed nitrogen. The samples were then dehydration baked for at least 1 min at 100°C or greater. A GCA 8000 i-Line Stepper was used to optically expose a dual-layer resist stack consisting of NANO SF9/SPR3012, followed by development using CD-26, deep UV flood exposure and final development using PMGI XP101A.

CTLM test structures with nominal gap spacings of 0.5-20 µm were defined on the lightly-doped epilayers. Similarly, RTLM test structures with nominal gap spacings of 0.6-10 µm were defined on the heavily-doped epilayers.

### 3.3.1.2 Surface Preparation and Metallization

After photolithography, samples were subjected to a UV-ozone surface treatment for 10 min at 0.9 SLPM in an 80% nitrogen/20% oxygen atmosphere, where the samples were placed 4 cm below the lamp. Afterwards, the oxide was etched using BOE (10:1) for 2 min. The samples were immediately loaded into an electron beam evaporation chamber.

The chamber was pumped down to a base pressure of less than $3 \times 10^{-7}$. First, a titanium getter was performed by evaporating Ti (99.995%) evaporant for about 2 min while the samples were shielded from the electron beam source in order to further minimize residual oxygen within the chamber. The following metal contact layers were then deposited in the following order: Pd (99.95%), Si (99.999%), Pd, Ti, Au (99.999%); the evaporation rates for each were 1.0, 1.5, 1.0, 2.0, and 1.3 Å/s, respectively. Figure 3.2 shows the varying thicknesses of the metal layers in the as-deposited contact stack. To reduce heating of the sample during deposition, a 30 min cooldown period was allowed between the deposition of the Ti and Au layers.
3.3.1.3 Liftoff, Mesa Alignment and Etching

After metal deposition, samples were placed in a solution of Remover PG for standard liftoff of photoresist. For those samples patterned with the RTLM test structure, a second photolithography step was required in order to fabricate mesa etch masks for current isolation around the contact pads. SPR3012 resist was spun on these samples followed by proper alignment of the mesa mask, exposure and development. The exposed InGaAs areas were wet-etched for 80 s at room temperature using a solution of lactic acid, phosphoric acid, anhydrous citric acid, and hydrogen peroxide (6 mL:1 mL:1 g:1 mL), followed by removal of the etch mask. The resulting mesa edges have a maximum tolerance of < 500 nm wider than the edge of the metal pads.

3.3.1.4 Rapid Thermal Annealing

After deposition of the metal layers and liftoff, the samples were annealed in a rapid thermal anneal furnace (AG Associates Heatpulse 610) in an argon ambient in order to form the ohmic contact. A silicon cover wafer was used in order to minimize arsenic vapor loss from the InGaAs semiconductor by maintaining an overpressure of arsenic over the samples.

Several annealing conditions were tested in order to optimize the contact. A two-step anneal was ultimately used for all samples except those created for materials characterization of the first-step anneal. The first-step anneal took place at 200°C for 30 s, and then the temperature was ramped up immediately afterwards for the final anneal, which ranged from 360°C–400°C for 15–50 s.
3.3.2 Electrical Characterization

Four-point probe I-V measurements were performed with a Keithley 238 parameter analyzer with linear current sweep and voltage measurement. At least four sets of CTLM or RTLM patterns were measured for each sample. For both CTLM and RTLM I-V measurements, the average resistance for each gap was calculated from the measured resistances in the range of -0.6 mA to +0.6 mA.

Gap spacings and mesa widths were measured using SEM and calibrated with a magnification reference standard (MRS-3, Geller Microanalytical Laboratories) at the same working distances. Specific contact resistance, sheet resistance, total contact resistance, and transfer length values were then extracted from plots of resistance versus gap spacing. CTLM data points were fitted using the Levenberg-Marquardt method and RTLM data points were fitted using the linear least squares method.

3.3.3 Transmission Electron Microscopy

After contact fabrication and electrical characterization, select samples were examined by XTEM to study the morphology before, during and after SPR contact formation. The microstructural evolution was then correlated with the electrical data taken at each step.

3.3.3.1 Sample Preparation Using Focused Ion Beam

All samples were first sputter-coated with a 100 nm protective layer of tantalum. An FEI Quanta 200 3D Dual Beam Focused Ion Beam was used to lift out thin cross-sections from specific sites located adjacent to gap/metal-semiconductor contact edges. Protective layers of W were deposited by e-beam, and then by ion-beam gas assisted chemical vapor deposition within the chamber. Lift-out was performed using either the Total Release Method or Hitachi Method. Specimens were then transferred to a copper Omniprobe half-grid using an Omniprobe tungsten manipulator and finally thinned to electron transparency.
3.3.3.2 Morphological and Chemical Analysis

XTEM images was primarily taken on a JEOL 2010F field emission microscope, with additional images taken on JEOL 2010 LaB$_6$ and Philips EM420T microscopes. Bright field (BF) and HAADF STEM images were taken. STEM images were taken using a probe size of 0.7 nm. Selected area electron diffraction (SAED) and fast Fourier transform (FFT) images were acquired to provide phase information on certain layers of the samples. DigitalMicrograph was used to obtain calibrated FFT images from the recorded micrographs. XEDS was performed to assess elemental composition. Drift-corrected spot scans and line scans were taken as needed. ESVision was used to perform background Brehmsstrahlung signal removal. Integrated intensities were then calculated using the standardless quantification algorithm.

3.3.4 Current Transport

3.3.4.1 I-V-T Measurements

A Lakeshore cryogenic probe station and a Hewlett-Packard 4156A Semiconductor Parameter Analyzer were used to perform four-point probe I-V measurements in the temperature range of 77–300 K. A select SPR contact to lightly-doped n-InGaAs with Pd/Si ratio of 1.5 and annealed at 200°C/30 s and 380°C/40 s was measured with linear current sweep and voltage measurement. Analogous to the room temperature I-V measurements, four CTLM sets were measured at each temperature (77, 150, 225, 300 K). The average resistance for each gap was calculated from the measured resistances in the range of -1 mA to +1 mA. The gap spacing measurements used were the same as taken initially at room temperature. Average specific contact resistances were calculated over four sets at each temperature.

3.3.4.2 Field Emission Modeling

In order to model the field-emission current transport behavior in the contacts, the field emission model for metal-semiconductor current transport was employed, as described in Appendix A. Degenerately doped n-In$_{0.53}$Ga$_{0.47}$As was assumed, and a Richardson’s constant of $A^* = 8.88 \times 10^4$ A/(m$^2$K$^2$) was used to calculate theoretical specific contact resistance values with respect to Schottky barrier heights (SBH)
($\phi_b = 0.2-0.4$ eV) and total donor concentrations ($N_D = 4 \times 10^{18} - 3 \times 10^{19}$ cm$^{-3}$) over a range of temperatures from 77-300 K. For any given SBH, the experimentally measured specific contact resistance values were matched with the donor concentration required to obtain these values. The required $N_D$ concentrations for specific contact resistance values measured at room temperature for both the lightly-doped contact and a heavily-doped contact were then plotted versus a range of SBHs in order to extract effective SBHs for a particular contact.
Planar Contacts

4.1 Introduction

This chapter compares the performance of various non-alloyed contacts fabricated to $n^+\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ in terms of specific contact resistance, morphological characterization, and thermal stability. Specifically, Ti/Pt/Au, Mo/Ti/Pt/Au, Pt/Ti/Pt/Au and Pd/Ti/Pt/Au contacts prepared using an optimized surface preparation method consisting of UV-ozone and BOE are analyzed. The contact interface is characterized with respect to the resulting interfacial morphology and chemistry. The trends in the resulting specific contact resistances before and after annealing are explained in terms of interface morphology and metal-dependent phenomena.

4.2 Specific Contact Resistance Results

4.2.1 Comparison of Different Contact Metals

The measured specific contact resistances of the Pd-, Pt-, Mo-, and Ti-based contacts to $n^+\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ of various thicknesses displayed an interesting trend. The Pd contacts consistently showed the lowest value, the Pt contacts were slightly higher, and finally the Mo and Ti resulted in values that were an order of magnitude higher than the Pt and Pd contacts. A summary of the contacts made to the heavily-doped InGaAs and the relevant extracted values is shown in Table 4.1.
Table 4.1. Summary of extracted data from I-V measurements for as-deposited contacts to n⁺-InGaAs. All contacts had a Ti/Pt (15/15 nm) diffusion barrier (Pt in the case of the Ti contact), and underwent the same surface preparation procedure (10 min UV-ozone and 2 min BOE).

<table>
<thead>
<tr>
<th>Sample</th>
<th>Metal</th>
<th>Thickness (nm)</th>
<th>$\rho_c$ (Ω-cm$^2$)</th>
<th>$R_{sh}$ (Ω/□)</th>
<th>$R_c$ (Ω-µm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>A1</td>
<td>Ti</td>
<td>15</td>
<td>$(3.0 \pm 0.8) \times 10^{-1}$</td>
<td>29.6 ± 1.9</td>
<td>29.6 ± 0.2</td>
</tr>
<tr>
<td>A2</td>
<td>Mo</td>
<td>30</td>
<td>$(3.2 \pm 0.5) \times 10^{-7}$</td>
<td>26.0 ± 1.0</td>
<td>28.8 ± 1.1</td>
</tr>
<tr>
<td>A3</td>
<td>Pt</td>
<td>5</td>
<td>$(4.6 \pm 0.5) \times 10^{-8}$</td>
<td>27.6 ± 0.8</td>
<td>11.3 ± 0.5</td>
</tr>
<tr>
<td>A4</td>
<td>Pd</td>
<td>2</td>
<td>$(2.3 \pm 0.2) \times 10^{-8}$</td>
<td>28.8 ± 0.7</td>
<td>8.07 ± 0.4</td>
</tr>
<tr>
<td>B1</td>
<td>Mo</td>
<td>9</td>
<td>$(2.7 \pm 0.6) \times 10^{-7}$</td>
<td>24.9 ± 0.6</td>
<td>25.8 ± 1.5</td>
</tr>
<tr>
<td>B2</td>
<td>Pt</td>
<td>9</td>
<td>$(7.1 \pm 0.6) \times 10^{-8}$</td>
<td>26.4 ± 0.4</td>
<td>13.6 ± 0.5</td>
</tr>
<tr>
<td>B3</td>
<td>Pd</td>
<td>9</td>
<td>$(3.2 \pm 0.3) \times 10^{-8}$</td>
<td>27.3 ± 0.5</td>
<td>9.28 ± 0.4</td>
</tr>
</tbody>
</table>

The data was divided into two sets of samples, Set A and Set B. Set A was initially prepared in order to compare the four different contact metals with previous results by Dormaier [32]. In this previous study, these same contacts were fabricated on Si-doped n⁺-In$_{0.86}$Ga$_{0.14}$As epilayers ($N_D = 1 \times 10^{19}$ cm$^{-3}$) with the same surface preparation procedure. For the as-deposited contacts, that study showed a similar trend as the data from Set A. However, Set A shows higher overall values, where the specific contact resistance of the Pd contact is approximately an order of magnitude higher, while the Pt, Ti and Mo contacts are slightly higher compared to their counterparts in the previous study. The increase in specific contact resistance for the contacts made to n⁺-In$_{0.53}$Ga$_{0.47}$As versus n⁺-In$_{0.86}$Ga$_{0.14}$As was expected due to the smaller expected barrier in the latter.

Set B consisted of the Mo, Pt and Pd contacts, except with constant as-deposited nominal thicknesses of 9 nm in order to directly compare the different contact metals. The Ti contact was omitted because it displayed similar specific constant values as the Mo contact. Additionally, the Mo contact was more interesting because it has not been as extensively studied as the Ti contact to n-InGaAs, but has been previously demonstrated to result in extremely low specific contact resistance values [61, 62].

4.2.2 Annealing Results

The samples from Set B were annealed at 350°C for 1 h in Ar ambient in order to study the change in specific contact resistance after high temperature aging. After
annealing, the surface of the contacts were inspected using SEM to confirm that there was no significant lateral diffusion into the RTLM gaps and to ensure that the Au surface was still smooth.

<table>
<thead>
<tr>
<th>Sample</th>
<th>Contact</th>
<th>$\rho_c$ ($\Omega\cdot\text{cm}^2$)</th>
<th>$R_{sh}$ ($\Omega/\Box$)</th>
<th>$R_c$ ($\Omega\cdot\mu\text{m}$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>B1</td>
<td>Mo</td>
<td>$(2.7 \pm 0.6) \times 10^{-7}$</td>
<td>$24.9 \pm 0.6$</td>
<td>$25.8 \pm 1.5$</td>
</tr>
<tr>
<td>B1*</td>
<td>Mo</td>
<td>$(1.2 \pm 0.1) \times 10^{-7}$</td>
<td>$26.9 \pm 0.3$</td>
<td>$18.3 \pm 0.3$</td>
</tr>
<tr>
<td>B2</td>
<td>Pt</td>
<td>$(7.1 \pm 0.6) \times 10^{-8}$</td>
<td>$26.4 \pm 0.4$</td>
<td>$13.6 \pm 0.5$</td>
</tr>
<tr>
<td>B2*</td>
<td>Pt</td>
<td>$(8.4 \pm 0.2) \times 10^{-8}$</td>
<td>$27.2 \pm 0.2$</td>
<td>$15.1 \pm 0.2$</td>
</tr>
<tr>
<td>B3</td>
<td>Pd</td>
<td>$(3.2 \pm 0.3) \times 10^{-8}$</td>
<td>$27.3 \pm 0.5$</td>
<td>$9.3 \pm 0.4$</td>
</tr>
<tr>
<td>B3*</td>
<td>Pd</td>
<td>$(4.6 \pm 0.4) \times 10^{-8}$</td>
<td>$27.6 \pm 0.5$</td>
<td>$11.2 \pm 0.3$</td>
</tr>
</tbody>
</table>

Table 4.2. Summary of extracted I-V data of 9 nm Mo, Pt and Pd contacts to $n^+\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$, as-deposited and *after annealing at 350°C/1 h.

The Pd contact once again showed significantly lower specific contact resistance values, but slightly increased values after annealing. The specific contact resistance of the Pt contact increased slightly after annealing as well. However, the value decreased for the Mo contact after annealing. The sheet resistance values extracted for all contacts were fairly constant even after annealing, indicating that the sheet resistance between the contacts did not change much even with annealing. The results are summarized in Table 4.2 and shown visually in Figure 4.1.

Figure 4.1. Specific contact resistance data for the 9 nm Mo, Pt and Pd contacts to $n^+\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ before and after annealing at 350°C/1 h in Ar.
4.3 Materials Characterization

In order to better understand the change in specific contact resistance after annealing, XTEM images were taken for samples B1, B2 and B3, the annealed 9 nm Mo, Pt and Pd contacts. Additionally, XEDS, EELS and Auger surface scans were collected to observe the interfacial reactions throughout the contact metallization and metal-semiconductor interface.

4.3.1 Annealed Mo Contact

The annealed Mo contact is shown in XTEM and STEM images in Figure 4.2 and 4.3. There is little lateral diffusion at the edge of the contact, and the Mo did not react deeply within the InGaAs epilayer. However, there is a very thin, amorphous layer approximately 1 nm thick present between the Mo and the InGaAs. The contrast of this layer is brighter than both the adjacent Mo and InGaAs. This layer is not due to TEM imaging artifacts as a result of sample tilt; the presence of this layer is confirmed in the HAADF STEM image, where the measured thickness is the same and the contrast is darker than the adjacent layers. An XEDS spot scan of this layer was also recorded. According to the XEDS, there is a significant Mo signal along with As, In and Ga signals present.

However, the XEDS signal was difficult to interpret even with a very small probe size (0.5 nm) because of interference or fluorescence of elements contained within the adjacent layers (Mo, InGaAs) and also the sample grid (Cu). In STEM HAADF mode, because the contrast of the thin layer was much darker than the adjacent Mo and InGaAs layers, and closer in appearance to the Ti layer, the composition of the thin layer was expected to be light in mass and have a low average Z-number. Also, in STEM HAADF mode, also known as Z-contrast imaging, the mass-thickness contrast is proportional to $Z^2$ and somewhat dependent on density because of the prevalence of high-angle Rutherford scattering. Comparing the densities and average Z values of possible compounds that might form between the Mo/InGaAs interface at 350°C, the most likely candidates for the identity of this interfacial layer were the oxides of In, Ga or As, or a combination of these oxides.

As discussed previously, the particular surface preparation used here results in an
Figure 4.2. Bright field XTEM images of annealed 9 nm Mo contact to $n^+$-InGaAs.

Figure 4.3. HAADF STEM image and XEDS line scan of annealed 9 nm Mo contact to $n^+$-InGaAs.

InGaAs surface consisting of elemental As and possible native oxides due to short air exposure before loading into the deposition chamber. Of the stable oxides of InGaAs, the As-oxides are predicted to be the least stable, followed by the In- and Ga-oxides based on the comparison of their bulk free energies of formation [26]. It has also been noted, for InGaAs surfaces, that at increased temperatures, the composition of the native oxide layer can change, as the amount of As-oxides usually decreases through evaporation and the number of In 3+ and Ga 3+ oxidation states increases [26, 133, 134]. Thus, it is predicted that the oxide formed after 350°C/1 h would most likely be either $\text{Ga}_2\text{O}_3$ or $\text{In}_2\text{O}_3$, or a combination of both. However, because
these contacts involve thin-film reactions occurring at non-equilibrium conditions, and includes the presence of Mo/Ti/Au cap layers, the interfacial layer is probably a combination of both oxides along with elemental As segregated at the oxide-InGaAs interface.

In order to better determine the identity of the thin layer, EELS line scans were then performed across the InGaAs/Interfacial layer/Mo interfaces in STEM HAADF mode. Using a probe size of 0.5 nm and a step size of 6.4 Å, the EELS spectra were recorded in the range of 350–970 eV. Within the InGaAs epilayer, the In K peak edge was detected. Within the interfacial layer, the O K peak edge appeared within the In peak, while the In peak edge persists. As the electron probe moves to the adjacent Mo layer, Mo M peak edges appear while the In and O peak edges completely disappear. Selected background-subtracted EELS spectra taken from the InGaAs epilayer and interfacial layer are shown in Figure 4.4. The EELS spectra indicate that the interfacial layer is composed of an In-oxide, since the In edge remains when the O edge appears. The layer may additionally contain either Ga or As as well; however, EELS spectra were not collected at the higher peak energies where these elements display peaks. Because the sample was prepared using a FIB and milled using a Ga ion beam, it would also be difficult to interpret the presence of Ga within such a thin layer. Molybdenum was not detected. From the EELS spectra collected, it was concluded that the thin layer contained In-oxide. This result confirms that the Mo layer was unreactive with the substrate even after annealing.

Additionally, AES surface scans were collected from the surface of the Au film on the Mo contact. The AES surface scans shown in Figure 4.5 reveals the presence of In on the surface of the annealed contact. Indium was not detected throughout the contact layers in the EDS line scans of the XTEM, indicating that a small amount of In had probably out-diffused all the way to the surface.

### 4.3.2 Annealed Pd Contact

The annealed Pd contact is shown in the XTEM and STEM images in Figures 4.6 and 4.7. The micrographs show that the Pd has reacted to an average depth of 10 nm within the InGaAs epilayer to form a Pd$_x$InGaAs phase. The Pd has also reacted with the adjacent Ti layer. Additionally, there is little lateral diffusion at the edge
Figure 4.4. Background subtracted EELS core level peak edges from spectra taken within the Mo layer, InGaAs epilayer, and interfacial layer of annealed 9 nm Mo contact to n$^+$-InGaAs.

Figure 4.5. AES surface scans of the InGaAs epilayer and the Au pad of the annealed 9 nm Mo contact to n$^+$-InGaAs.

of the contact. The XEDS line scan reveals that there is significant As out-diffusion from the InGaAs, and the As has settled at the Pd/Ti interface interface. This As-outdiffusion is accompanied by the transformation of As-rich Pd-In-Ga-As phases (at room temperature to moderate annealing temperatures) to Ga-rich Pd-In-Ga-As
phases at higher annealing temperatures (around 400°C) [65, 69]. A similar effect has been seen in annealed Pd/GaAs; as the annealing temperature is increased, the initial Pd$_x$GaAs ternary phase formed begins to decompose, transitioning from As-rich so that Ga becomes more mobile, to Ga-rich at 350°C, where As becomes mobile [65, 100, 135].

![Figure 4.6. Bright field XTEM images of annealed 9 nm Pd contact to n$^+$-InGaAs.](image)

Figure 4.6. Bright field XTEM images of annealed 9 nm Pd contact to n$^+$-InGaAs.

![Figure 4.7. HAADF STEM image and XEDS line scan of annealed 9 nm Pd contact to n$^+$-InGaAs.](image)

Figure 4.7. HAADF STEM image and XEDS line scan of annealed 9 nm Pd contact to n$^+$-InGaAs.
4.3.3 Annealed Pt Contact

The annealed Pt contact is shown in the XTEM and STEM images in Figure 4.8 and 4.9. There is an observed 10 nm Pt$_x$InGaAs phase below the original Pt/InGaAs interface after annealing, but no significant intermixing at any of the other metal layers. There is also a bright interfacial region corresponding to an oxide layer containing In, Ga, As and Pt, which was confirmed by EELS analysis in similar contacts annealed at 270°C. The XEDS line scan suggests that in the reacted region, Pt is present along with In, Ga and As, and that in the contact Pt layer, In and Ga are present near the interface. Furthermore, because little or no As is detected in the Pt contact layer, the reacted region can be considered As rich. Ternary phase diagrams of As-In-Pt and As-Ga-Pt suggest the possible formation of Ga-Pt and In-Pt phases in the Pt contact layer, as well as Ga-Pt, In-Pt, As-Pt, and As-In-Ga-Pt phases in the reacted region; however further characterization is required to determine the exact phases present. Since the Pt/InGaAs contact was annealed at 350°C, it is likely that an As-Pt phase is present in the reacted region, as Pt-As reaction products have been observed by others, such as by Leech et al. [136], who observed Pt-As reaction products forming in Pt/InGaAs contacts above 375°C using backside secondary ion mass spectrometry (SIMS) depth profiling.

![Figure 4.8. Bright field XTEM images of annealed 9 nm Pt contact to n$^+$-InGaAs.](image-url)
4.4 Effect of Reaction Depth on Extracted Specific Contact Resistance

Because the change in specific contact resistance after annealing for the Pt and Pd contacts was very slight compared to the Mo contact, it is useful to look at the possible error that may arise from an increase in the semiconductor sheet resistance under the contact [28], due to significant reaction depths relative to the InGaAs epilayer thickness of the Pt and Pd after 350°C/1 h annealing.

For these calculations, the reduced thickness of the epilayer due to large reaction depth increases the sheet resistance underneath the contact, $R_{sh}$, subsequently increasing the extracted specific contact resistance. Assuming a metallic reaction product and a simple scaling of the sheet resistance with thickness, the $R_{sh}$ is thus expected to increase by a fraction depending on the reaction depth, and is expressed as:

$$R_{sc} = R_{sh} \times \left( \frac{t_{epi}}{t_{epi} - x} \right)$$  \hspace{1cm} (4.1)

where $R_{sc}$ is the new semiconductor sheet resistance under the contact, $t_{epi}$ is the total InGaAs epilayer thickness, and $x$ is the reaction depth relative to the original interface. Then the total resistance between two contacts, $R_T$, is modified from

$$R_T = \frac{R_{sh} \cdot d}{Z} + 2R_c$$  \hspace{1cm} (4.2)
where $d$ is the gap spacing and $Z$ is the contact width, to

$$R_T = \frac{R_{sh}d}{Z} + 2\frac{R_{sc}L_{Tc}}{Z}$$

(4.3)

where $L_{Tc} = \sqrt{\rho_c/R_{sc}}$ and is the new transfer length.

For the annealed Pd and Pt contacts, the reaction depths as measured in the TEM micrographs were used to estimate $R_{sc}$ from the $R_{sh}$ extracted from the plots of the $R_T$ versus $d$ values, which were experimentally measured. Equation 4.3 was used to back calculate $L_{Tc}$ and $\rho_c$. The original $d$ spacings and contact widths, $Z$, are used for each RTLM set. This calculated $\rho_c$ represents the corrected specific contact resistance for the annealed contact while accounting for the reaction depth; it is expected that the value should be smaller than the originally measured specific contact resistance, depending on the depth of reaction. The results of these calculations were compared to the measured specific contact resistances for the as-deposited and annealed Pd and Pt contacts, as shown in Table 4.3.

<table>
<thead>
<tr>
<th>Pd/Ti/Pt/Au</th>
<th>$\rho_c$ (Ω-cm$^2$)</th>
<th>$R_{sh}$ (M) or $R_{sc}$ (C) (Ω/□)</th>
<th>$x/t_{epi}$ (nm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>As-deposited (M)</td>
<td>$(3.6 \pm 0.3) \times 10^{-8}$</td>
<td>27.3 ± 0.5</td>
<td>N/A</td>
</tr>
<tr>
<td>350$^\circ$C/1 h (M)</td>
<td>$(4.6 \pm 0.4) \times 10^{-8}$</td>
<td>27.6 ± 0.5</td>
<td>N/A</td>
</tr>
<tr>
<td>350$^\circ$C/1 h (C)</td>
<td>$(3.7 \pm 0.3) \times 10^{-8}$</td>
<td>34.5 ± 0.6</td>
<td>10/50 (TEM)</td>
</tr>
<tr>
<td>Pt/Ti/Pt/Au</td>
<td>$\rho_c$ (Ω-cm$^2$)</td>
<td>$R_{sh}$ (M) or $R_{sc}$ (C) (Ω/□)</td>
<td>$x/t_{epi}$ (nm)</td>
</tr>
<tr>
<td>As-deposited (M)</td>
<td>$(7.1 \pm 0.6) \times 10^{-8}$</td>
<td>26.4 ± 0.4</td>
<td>N/A</td>
</tr>
<tr>
<td>350$^\circ$C/1 h (M)</td>
<td>$(8.4 \pm 0.2) \times 10^{-8}$</td>
<td>27.2 ± 0.2</td>
<td>N/A</td>
</tr>
<tr>
<td>350$^\circ$C/1 h (C)</td>
<td>$(7.0 \pm 0.2) \times 10^{-8}$</td>
<td>32.4 ± 0.3</td>
<td>8/50 (TEM)</td>
</tr>
</tbody>
</table>

Table 4.3. Corrected (C) specific contact resistances for the annealed (350$^\circ$C/1 h) contacts compared to the measured (M) as-deposited and annealed (350$^\circ$C/1 h) contacts for Pd and Pt contacts to n$^+$-In$_{0.53}$Ga$_{0.47}$As. Measured reaction depths are taken from available TEM images.

The corrected specific contact resistances of the annealed contacts are actually close to the measured specific contact resistances of the as-deposited contacts for both the Pd and Pt contacts. Thus, the measured values for the annealed samples seem to be overestimates due to the increase of the semiconductor sheet resistance underneath the contact. This finding indicates that any interfacial reaction products formed at these temperatures did not result in changes in barrier height, despite slight changes in stoichiometry due to As, Ga or In outdiffusion.
4.5 Calculation of Effective Barrier Heights to n-In$_{0.53}$Ga$_{0.47}$As

The trend in different specific contact resistance values of the Pd, Pt and Mo contacts to the heavily-doped epilayer is interesting in light of the general acceptance that the Fermi level of n-InGaAs is pinned below the conduction band, with a Schottky barrier height of approximately 0.2 eV [137, 138]. It is thus expected that the choice of metal contact is negligible to significantly change the specific contact resistance regardless of work function. However, the results in the previous sections have shown that the Pd metal results in a consistently lower specific contact resistance than either the Pt, Mo or Ti metals. Subsequently, I-V-T measurements were performed in order to determine if there were any possible differences in the SBHs as a result of using different metals.

Barrier height calculations were first performed for the as-deposited Pd and Mo contacts to n-InGaAs epilayers with carrier concentration $n = 5 \times 10^{17} \text{ cm}^{-3}$. First, the experimentally measured specific contact resistance values were plotted over the temperature range of 77–400 K (for the Pd contact, 220–400 K, due to instrument malfunction). It is interesting to note that the specific contact resistance values are comparable for both the Mo and Pd contacts, which was not the case for the similar contacts made to the more heavily-doped epilayers. Also, the temperature dependence of the specific contact resistance values for both contacts compare well with each other, and both vary linearly with $\log(\rho_c)$ versus $T$.

The total donor concentration was taken to be $N_D = 5 \times 10^{17} \text{ cm}^{-3}$. The characteristic tunneling energy, $E_{00}$, was then calculated and compared to $kT$ in order to determine whether FE, TFE or TE was expected for these contacts. In this case, $E_{00} \approx kT$, indicating that primarily TFE is expected at the barrier. However, using the exact analysis as described in Rhoderick [18], TFE is valid at $kT > 2qE_{00}[\ln(-4\phi_b/\xi)]^{-1}$, which corresponds to $T > 130$ K. Next, the specific contact resistances were calculated assuming either FE, TFE or TE, as described in Appendix A, as a function of the total donor concentration and $\phi_b$ over $T = 77–400$ K. The lowering of the Schottky barrier height with doping is accounted for by including the change in effective mass, $m^*$, with doping according to a linear fit based on the values of $m^* = 0.041m_0$.
at $N_D = 2 \times 10^{17} \text{ cm}^{-3}$ and $m^* = 0.074m_0$ at $N_D = 6 \times 10^{18} \text{ cm}^{-3}$ [139], and the effect of image force barrier lowering [15]. The calculated curves using several barrier heights are plotted along with the experimentally measured values. The best fit TFE curve to the experimental data is shown in Figure 4.10. As expected, the experimental data fits best with the TFE curve for specific contact resistance down to $T \approx 130$ K. The barrier height that results in the specific contact resistance values close to the experimental data is approximately 0.24 eV.

![Figure 4.10](image)

**Figure 4.10.** Specific contact resistance as a function of temperature for the Pd and Mo contacts to n-In$_{0.53}$Ga$_{0.47}$As ($N_D = 5 \times 10^{17} \text{ cm}^{-3}$) with a selected TFE curve corresponding to 0.24 eV plotted.

Barrier height calculations were also performed for the n$^+$-InGaAs epilayer with $N_D = 3 \times 10^{19} \text{ cm}^{-3}$. Here, field emission is valid and the resulting specific contact resistance values versus temperature are expected to remain fairly constant even for different barrier heights. At room temperature, the experimental data for the as-deposited 9 nm Pd contact to the n$^+$-InGaAs falls near the average specific contact resistance value calculated using a barrier height of 0.24 eV. On the other hand, for the as-deposited 9 nm Mo contact to the n$^+$-InGaAs, the measured value falls near the value calculated using an effective barrier height of 0.40 eV.
4.6 Discussion

4.6.1 Specific Contact Resistance Versus Metal

The experimental data for the specific contact resistance versus temperature for the Mo and Pd contacts to the lightly-doped InGaAs reveals current transport via a TFE mechanism, roughly corresponding to a Schottky barrier height of 0.24 eV. It is interesting to note that the specific contact resistance for both contact metals were comparable, as opposed to the order of magnitude difference for the as-deposited contacts to heavily-doped InGaAs. In that case, the specific contact resistance of the as-deposited Pd contact corresponded to a calculated barrier height of about 0.27 eV following the FE mechanism of current transport. This corresponds well with the 0.24 eV extracted for the contacts made to the more moderately doped InGaAs, and lies close to the expected barrier height of 0.2 eV for other metal contacts to n-In$_{0.53}$Ga$_{0.47}$As. However, the specific contact resistance of the as-deposited Mo contact to the heavily-doped InGaAs corresponded to a calculated barrier height of around 0.40 eV. The higher extracted apparent barrier height for the Mo contact versus the Pd contact in the heavily-doped case suggests that there may be some physical phenomena occurring at the interface that is affecting the resulting current transport.

In particular, there are several factors that have revealed themselves to be of interest based on the experimental results described in the previous sections. One factor is the resulting interface chemistry due to the surface preparation and any subsequent changes as a result of contact metallization. Another related factor is the presence, type and thickness of the interfacial layer and its effect on tunneling resistance. These factors subsequently affect the thermal stability of the different metal contacts.

As noted before, in the heavily-doped case, the Pd and Pt contacts consistently resulted in significantly lower specific contact resistances than those of the Mo and Ti contacts, even with a consistent surface preparation procedure. The UV-ozone treatment and BOE oxide strip procedure was observed to result in an InGaAs surface terminated by elemental As. The known reactivity of the Pd and Pt with InGaAs at lower temperatures ($\lesssim 200^\circ$C) results in penetration of thin native oxide layers, while
the Mo does not react with the InGaAs at all until very high annealing temperatures. Recalling the TEM micrographs of the annealed 9 nm Pd and Mo contacts to heavily-doped InGaAs, the higher apparent barrier height and specific contact resistance of the as-deposited Mo contact can be correlated to the observed 1 nm oxide layer at the interface of the annealed Mo contact. This oxide layer was probably also present in the as-deposited case, due to the formation of Ga or In native oxides after the surface clean and short exposure in air before loading into the deposition chamber, as there was no significant reaction with the adjacent Mo layer after annealing.

The dominant current transport mechanism for the contacts to the heavily-doped InGaAs was field-emission through a very narrow depletion region. Thus, the effect of an oxide layer at the interface on the measured specific contact resistance will affect the current transport more significantly for the heavily-doped case. The total current transport can be described in terms of two resistances in series. These resistances are due to the tunneling through the depletion region and tunneling through the oxide layer. The approximate widths of the depletion regions can be calculated for both heavily and lightly-doped cases, assuming a barrier height of 0.24 eV, by using the depletion approximation [18],

\[ w_d = \sqrt{\frac{2\varepsilon_s V_{bi}}{qN_D}} \]  

(4.4)

where \( w_d \) is the depletion width, \( \varepsilon_s \) is the permittivity of semiconductor, and \( V_{bi} \) is the built-in potential and is equal to \( \phi_b - \xi \). Assuming a barrier height of 0.24 eV, the depletion width for a contact to the heavily-doped case is calculated to only be about 4 nm, as compared to 29 nm for the lightly-doped case. Thus, the resistance due to tunneling through the thin oxide becomes less significant in the lightly-doped case because the resistance to current transport due to TFE is so much higher and therefore becomes dominant. In the heavily-doped case, the resistance due to tunneling through the oxide layer is more comparable to the resistance due to tunneling through the narrow depletion region, leading to an increase in the observed effective barrier height. Schematic band diagrams of the forward biased lightly and heavily-doped contacts with a thin interfacial oxide of \( t_{ox} \) and different depletion widths, along with the likely conduction mechanisms, are shown in Figure 4.11.

In the case of the as-deposited Pt contact and Pd contacts to the heavily-doped
InGaAs, the lower specific contact resistances and barrier heights relative to the Mo contact can partly be attributed to the higher reactivity of these metals with InGaAs, resulting in the dispersion of the native oxide at the interface. The TEM analysis of the annealed Pd contact suggests the formation of a Pd$_x$InGaAs phase that has reacted with the InGaAs to a depth of about 15 nm relative to the original Pd/InGaAs interface. This phase is observed to form in the as-deposited case and at low temperatures [70]. It is thus reasonable to conclude that there is no interfacial layer in our as-deposited case either, resulting in the modeled, pinned 0.27 eV barrier height and lower specific contact resistance.

The specific contact resistance of the as-deposited Pt contact can also be explained by this phenomenon. The TEM analysis of the annealed Pt contact showed not only a 10 nm deep reaction region of Pt and InGaAs relative to the original Pt/InGaAs interface, but also a thin (0.8 nm) interfacial layer consisting of In-, Ga-, As-oxides and Pt. It can be suggested that there was also an initial interfacial oxide layer in the as-deposited contact. The higher specific contact resistance of the Pt contact versus the Pd contact may be due to the lower reactivity of Pt with InGaAs at the same temperatures, and thus the less uniform penetration of the interfacial oxide. On the other hand, the higher reactivity of the Pt with InGaAs compared with Mo resulted
in lower specific contact resistance in the same case due to the thinner interfacial oxide layer.

The deleterious effects of the interfacial oxide layer on contact resistance can also be examined from the perspective of the surface preparation and the extremes of the Pd and Mo metals’ ability to penetrate the oxide layer. Additionally, because Mo is of particular interest due to its promise for better thermal stability compared with Pd, it is desirable to better understand the Mo-InGaAs interface in the formation of an ex situ contact. Specifically, the surface preparation may be playing a more significant role in the performance of the Mo contact compared to that of the Pd or Pt contacts precisely because of its lower reactivity with InGaAs. The lowest specific contact resistance reported for an ex situ, non-alloyed contact to n-In$_{0.53}$Ga$_{0.47}$As was in fact fabricated using Mo after a UV-ozone/HCl/atomic H surface clean [62]; however, the InGaAs layer contained an active donor concentration of $5 \times 10^{19}$ cm$^{-3}$, which was higher than many other studies. This doping concentration can be inputted into the barrier height calculations; in order to obtain their lowest reported $\rho_c = 1.1 \times 10^{-8}$ Ω-cm$^2$, a barrier height of 0.25 eV is extracted. In order to obtain their reported value of $\rho_c = 1.5 \times 10^{-8}$ Ω-cm$^2$ (no atomic H clean), the extracted barrier height was found to be between 0.26 and 0.30 eV.

These extracted barrier heights reveal that a very stringent surface preparation technique or an in situ fabrication process is needed to achieve an extremely low resistance ohmic contact using Mo. In fact, XPS has revealed that atomic H surface treatment has been shown to remove As-oxide and elemental As from the InGaAs surface [140]. Additionally, the barrier heights extracted correspond well with those of our Pd contacts to heavily-doped InGaAs (0.27 eV) and those of the Pd and Mo contacts to the lightly-doped InGaAs (0.24 eV). Thus, the increase in extracted barrier height in our Mo contacts to heavily-doped InGaAs (0.40 and 0.35 eV) is probably directly due to the presence of the interfacial layer, which causes an increase in resistance to tunneling. The calculated specific contact resistances as a function of barrier heights and doping concentrations are plotted along with experimentally measured specific contact resistance values at room temperature in Figure 4.12.

The effect of the interfacial layer for the different metals in the heavily-doped case reveals the importance of the metal-InGaAs interface in the ohmic contact resistance,
especially when the dominant current transport mechanism is tunneling through a thin barrier.

### 4.6.2 Interfacial Reactions and Thermal Annealing

The behavior of the three different metal contacts after annealing at 350°C/1 h was interesting and in general can shed light on the metal/InGaAs interface and the effect on current transport behavior in these ohmic contacts.

The stability of the Mo contact after annealing was interesting in that the specific contact resistance decreased, which was the opposite of the Pd and Pt contacts to heavily-doped n-InGaAs. By comparing the interfacial reactions of the three contacts from the TEM analysis, it is observed that the Mo does not readily react with the excess As at the interface nor with the interfacial oxide observed consisting of In and/or Ga and As oxides. The decrease in specific contact resistance may be due to degradation of the interfacial layer, as In outdiffusion to the Au surface was detected.
(by AES), indicating that the oxide layer may be reacting slightly with either the As and Ga from the InGaAs, allowing In to dissociate and outdiffuse towards the surface through the degraded oxide.

In the case of the annealed Pd contact, the specific contact resistance did not change significantly after annealing at 350°C. For Pd/GaAs systems, at low temperatures (<300°C), the Pd is the dominant mobile species, and it has been observed that thin (10–12 nm) capped Pd reacts readily with GaAs to form a ternary Pd$_x$GaAs that remains metastable up to 600°C. Above 600°C, vertical stratification occurs resulting in PdAs$_2$ and PdGa layers [141], which may be detrimental to the contact resistance. Similarly, for InGaAs, the initial formation of a quartenary Pd$_x$InGaAs phase that is stable up to 350°C is expected, and is probably responsible for the good thermal stability at this annealing temperature in our contacts. Indeed, based on similar annealed Pd/Ge contacts to InGaAs made by Ressel et al. [70], the TEM analysis of the Pd contact also suggests the formation of a Pd$_x$InGaAs phase after annealing. Additionally, the rapid outdiffusion of As observed beyond the reacted Pd layer in the contact after annealing did not seem to deteriorate the specific contact resistance. The Ti layer was effective at preventing further outdiffusion of As at the annealing temperature used. Chor et al. [64] also observed similar behavior for Pd/Ti/Pd/Au contacts to n$^+$-InGaAs annealed at 350°C; however, the specific contact resistance did degrade after annealing at 450°C due to increased intermixing of layers and substantial As outdiffusion. Finally, compared to the Mo contact, the native oxide probably has no effect on the barrier height because it has been completely dispersed due to the initial formation of the quartenary Pd$_x$InGaAs phase.

In the annealed Pt contact, the specific contact resistance also did not change significantly even after annealing at 350°C/1 h. The reaction of the thin Pt is different than Pd. The TEM images revealed a 0.8 nm thin interfacial layer and reaction of Pt with InGaAs below the original Pt/InGaAs interface. The interfacial layer containing Pt, In, Ga, As and O is probably the result of the reaction of the Pt with the initial oxide formed after surface treatment. Previous studies on Pt-based contacts to n-GaAs have described the formation of a PtAs$_2$ semiconducting phase after annealing between 300–400°C, which correlated with an increase in barrier height [142, 143]. However, it was difficult to confirm the formation of PtAs$_2$ in the TEM analysis, which
supports the observation of an insignificant change in specific contact resistance after annealing. The lack of As outdiffusion may also be contributing to the good electrical stability at the annealing temperature. The XEDS analysis showed that there is less As outdiffusion in the layers beyond the contact layer as compared to the case of the Pd contact. This behavior was also observed in Pt thin film reaction studies to GaAs, where the As remains below the original GaAs/Pt interface even after annealing up to 600°C [141]. This was said to be due to Pt and Ga being the dominant mobile species, as there is a large electronegative difference between Pt and Ga, initially resulting in Pt in-diffusion and Ga out-diffusion [100].

4.7 Comparison to p-InGaAs

Non-alloyed contacts based on Pd, Pt and refractory metals have also been studied on p+-InGaAs. Again, for the contacts to p-type InGaAs, increased doping, surface treatment and contact metallization are the main factors affecting the specific contact resistance. Non-alloyed contacts to p-In$_{0.53}$Ga$_{0.47}$As with doping concentrations of $1–2 \times 10^{19}$ cm$^{-3}$ generally result in specific contact resistances on the order of $10^{-6}$ Ω-cm$^2$ or higher, depending on the surface preparation and metallization used [64, 65, 69, 72, 73, 74, 136, 144]. Recently, specific contact resistances on the order of $10^{-9}$ and $10^{-8}$ have been demonstrated for Ir- [145] and W-based [146] contacts to p-In$_{0.53}$Ga$_{0.47}$As with measured carrier concentrations from $1–2 \times 10^{20}$ cm$^{-3}$ using a UV-ozone/HCl/H$_2$O surface clean. Lysczek et al. [73] used UV-ozone followed by NH$_4$OH for the surface treatment for selective electroless Pd/Ru/Au contacts and obtained a specific contact resistance of $2.1 \times 10^{-7}$ Ω-cm$^2$ on p-InGaAs ($N_A = 5 \times 10^{19}$ cm$^{-3}$), which was almost an order of magnitude lower than when HCl was used in place of NH$_3$OH. Dormaier [49] concluded that by using UV-ozone treatment and BOE, specific contact resistance values could be lowered by half an order of magnitude compared to using HCl surface treatment for Pd- and Pt-based contacts to heavily-doped p-InGaAs (with a thin n-InGaAs cap).

Particularly interesting is the trend of specific contact resistance with respect to metallization. Chor et al. [64, 65] found that Pd/Ti/Pd/Au contacts to p-InGaAs ($N_A = 1 \times 10^{19}$ cm$^{-3}$) consistently resulted in the lowest specific contact resistance
compared with Ti/Pt/Au (\(\sim 2\) times higher) contacts with \(\text{NH}_4\text{OH}\) surface preparation. Yu et al. [74] also found that by introducing Pd and Pt contacting layer below the Ti/Pt/Au contact to p-InGaAs (\(N_A = 1-2 \times 10^{19} \text{ cm}^{-3}\)) with BOE surface treatment decreased the specific contact resistance by about 2 times, with the Pd resulting in the lowest values. Jang et al. [72] also found that Pd/Ir/Au contacts resulted in about a 2 times lower specific contact resistance than Ir/Au contacts for p-InGaAs (\(N_A = 1 \times 10^{19} \text{ cm}^{-3}\)). The commonality of the Pd contacting layer for low specific contact resistances in various studies is interesting because for p-InGaAs, metals with higher work functions such as Pt and Ir are predicted to form lower-resistance contacts because of the predicted lower Schottky barrier height.

### 4.7.1 Pd, Pt and Mo Contacts to p\(^+\)-InGaAs

In order to further study the Pd, Pt and Mo-based contact metallizations on InGaAs, the same contacts (M/Ti/Pt/Au, 9/15/15/100 nm) were fabricated by a colleague, Shih-ying Yu, on Be-doped p\(^+\)-In\(_x\)Ga\(_{1-x}\)As epilayers (\(x = 0.50-0.47\)) with the same surface preparation as for the n-type contacts and annealed cumulatively in Ar at 270°C and 350°C. The specific contact resistances were measured and compared to the previous results on the n\(^+\)-In\(_{0.53}\)Ga\(_{0.47}\)As. The results of the p-type study are shown in Figure 4.13.

Again, the as-deposited Mo contacts exhibited specific contact resistances over an order of magnitude higher than the Pt and Pd contacts, and the Pd contact was again the lowest, with the lowest \(\rho_c = 1.9 \times 10^{-8} \text{ \Omega}\cdot\text{cm}^2\). The specific contact resistance of the as-deposited Pt contact was an order of magnitude higher than the as-deposited Pd contact. The Pd < Pt < Mo specific contact resistance trend is similar to that of the as-deposited n-type contacts, indicating that in the Pd case the interfacial oxide layer has probably been dispersed due to the strong reaction of the Pd with the InGaAs. The p-type barrier heights from 0.4 to 0.5 were modeled for \(N_A = 5-9 \times 10^{19} \text{ cm}^{-3}\) in order to compare the current transport behavior for the Pd metals in both cases. In the p-type case, the hole effective mass and image force lowering are also considered when determining the barrier height used to calculate specific contact resistances. The hole effective mass takes into account the contribution from the effective masses of the light holes, \(m_{lh}^* = 0.05m_0\) [139], and heavy holes, \(m_{hh}^* = 0.47m_0\)
Specific contact resistances of Pd, Pt and Mo contacts to p$^+$-InGaAs; as-deposited and after cumulative annealing (courtesy of Shih-ying Yu).

\[ m_h^* = \left( \frac{m_{th}^*}{2} + \frac{m_{hh}^*}{2} \right)^{2/3} \]

The current transport was predicted to be in the TFE regime for these barrier heights and acceptor concentrations. A plot of calculated specific contact resistance versus total acceptor concentration is shown in Figure 4.14.

The barrier height to p-type InGaAs, $\phi_{bp}$, for the as-deposited Pd contact is expected to be 0.5 eV since $E_g = 0.74$ eV [148] for In$_{0.53}$Ga$_{0.47}$As at 300 K, and $E_g = \phi_{bn} + \phi_{bp}$, where $\phi_{bn} = 0.24$ eV, the n-type barrier height, was previously calculated. When comparing the calculated specific contact resistances with that of $\rho_c = 1.92 \times 10^{-9}$ $\Omega$-cm$^2$ of the as-deposited Pd contact, the best match with 0.5 eV corresponds to the value calculated using $N_A = 8 \times 10^{19}$ cm$^{-3}$. This value is reasonable for the acceptor concentration of the p-type epilayer according to the information given.

The behavior of the specific contact resistance of the contacts to p-type InGaAs after annealing for the three different metallizations is interesting when compared with the corresponding annealed contacts to n-type InGaAs. For the p-type Mo contact, the specific contact resistance steadily decreased almost an order of magnitude after cumulative annealing up to 350$^\circ$C, which mirrored the trend for the n-type case.
Figure 4.14. Calculated specific contact resistances versus acceptor concentration for p\(^+\)-InGaAs for various barrier heights in the TFE regime at 300 K.

The specific contact resistances of the annealed Pd and Pt contacts to the p-type InGaAs were corrected according to the reaction depths measured in the available TEM images (270°C/4 h for p-type and 350°C/1 h for n-type), and the results are shown in Table 4.4. For the Pd contact, the specific contact resistance after annealing at 270°C/4 h did not change, but after annealing at 350°C increased slightly. On the other hand, the specific contact resistances decreased slightly after annealing at 350°C for the Pt contact.

4.8 Current Transport Trends Versus Metallization In n- and p-Type InGaAs

In order to reconcile the trends in specific contact resistance and thermal stability behavior for both the n- and p-type contacts, several explanations are proposed in this section that are relevant to better understanding the current transport behavior in the Pd-, Pt- and Mo-based ohmic contacts. Figure 4.15 shows a summary of the
specific contact results for all the 9 nm contacts, along with the corrected values taking into account the known reaction depths.

For the Mo/Ti/Pt/Au contacts, recall that the interfacial oxide that may be present in the as-deposited n-type contact due to ex situ preparation is the significant factor in the determining the higher contact resistance in the heavily-doped InGaAs. Also, an increase in effective barrier height was calculated when compared to the heavily-doped Pd contact due to the increased tunneling distance required. The same phenomenon may be present in the as-deposited Mo contact to p-type InGaAs, as the specific contact resistance here was over an order of magnitude higher than the Pd and Pt contacts. The thermal stability behavior was also similar in both cases for Mo. After annealing at 350°C, the specific contact resistances decreased significantly in both the n- and p-type contacts. The TEM and AES analysis from the annealed sample indicated an unreactive Mo layer and slight degradation in the interfacial oxide, corresponding to the improved contact resistance.

Comparing the results of the Pd and Pt contacts for both the n- and p-type contacts is more complex due to the metals’ higher reactivity with InGaAs as compared to Mo. The significant reaction depths compared to the epilayer thickness resulted in an overestimation of the specific contact resistances for the annealed contacts.

In the Pd case, the native oxide is penetrated by the fast diffusion of Pd and

<table>
<thead>
<tr>
<th>Pd/Ti/Pt/Au</th>
<th>$\rho_c$ (Ω-cm²)</th>
<th>$R_{sh}$ (M) or $R_{sc}$ (C) (Ω/□)</th>
<th>$x/t_{epi}$ (nm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>As-deposited (M)</td>
<td>(1.9 ± 0.5)×10⁻⁸</td>
<td>596 ± 7</td>
<td>N/A</td>
</tr>
<tr>
<td>270°C/4 h (M)</td>
<td>(2.5 ± 1.1)×10⁻⁸</td>
<td>585 ± 21</td>
<td>N/A</td>
</tr>
<tr>
<td>270°C/4 h (C)</td>
<td>(1.9 ± 0.8)×10⁻⁸</td>
<td>798 ± 28</td>
<td>8/30 (TEM)</td>
</tr>
<tr>
<td>350°C/1 h (M)</td>
<td>(6.0 ± 1.3)×10⁻⁸</td>
<td>600 ± 14</td>
<td>N/A</td>
</tr>
<tr>
<td>350°C/1 h (C)</td>
<td>(4.0 ± 0.8)×10⁻⁸</td>
<td>900 ± 21</td>
<td>10/30 (TEM)</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Pt/Ti/Pt/Au</th>
<th>$\rho_c$ (Ω-cm²)</th>
<th>$R_{sh}$ (M) or $R_{sc}$ (C) (Ω/□)</th>
<th>$x/t_{epi}$ (nm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>As-deposited (M)</td>
<td>(2.6 ± 0.4)×10⁻⁷</td>
<td>658 ± 17</td>
<td>N/A</td>
</tr>
<tr>
<td>270°C/4 h (M)</td>
<td>(1.9 ± 0.3)×10⁻⁷</td>
<td>682 ± 7</td>
<td>N/A</td>
</tr>
<tr>
<td>270°C/4 h (C)</td>
<td>(1.9 ± 0.3)×10⁻⁷</td>
<td>682 ± 7</td>
<td>0/30 (TEM)</td>
</tr>
<tr>
<td>350°C/1 h (M)</td>
<td>(1.4 ± 0.1)×10⁻⁷</td>
<td>721 ± 12</td>
<td>N/A</td>
</tr>
<tr>
<td>350°C/1 h (C)</td>
<td>(1.1 ± 0.2)×10⁻⁷</td>
<td>983 ± 16</td>
<td>8/30 (TEM)</td>
</tr>
</tbody>
</table>

Table 4.4. Corrected (C) annealed (270°C/4 h and 350°C/1 h) specific contact resistances compared to measured (M) as-deposited and annealed values for Pd and Pt contacts to p⁺-InGaAs. Measured reaction depths are taken from available TEM images.
Figure 4.15. Measured and corrected specific contact resistances for contacts to n⁺- and p⁺-InGaAs.
the initial formation of the Pd<sub>x</sub>InGaAs phase at low temperatures, and likely in the as-deposited case. Pt is not known to disperse the native oxide as readily as Pd due to lower reactivity with InGaAs. The mirroring trends of the as-deposited specific contact resistances, where Pd < Pt < Mo, in both n- and p-type contacts reveals that the ability of the Pd and Pt to disperse the native oxide to varying degrees and form a more intimate contact with the InGaAs is a large factor to forming a low-resistance ohmic contact in both n<sup>+</sup>- and p<sup>+</sup>-type InGaAs.

In particular, the formation of the Pd<sub>x</sub>InGaAs phase is essential to the low resistance and stability of the Pd contact to both the n<sup>+</sup>- and p<sup>+</sup>-InGaAs. From the modeling of the n-type barrier heights, the as-deposited Pd contact to n<sup>+</sup>-InGaAs contact had a barrier height close to that of the experimentally “pinned” value of 0.2 eV for n-In<sub>0.53</sub>Ga<sub>0.47</sub>As. Assuming that the formation of the quaternary phase and the complete dispersion of the native oxide are responsible for a pinned Fermi level, it was expected that a reciprocal barrier height close to 0.5 eV would be formed for the Pd contact to p<sup>+</sup>-InGaAs (not taking into account energy gap narrowing with increased doping concentration). In the as-deposited Pd contact to p<sup>+</sup>-InGaAs, an acceptor concentration of 8 × 10<sup>19</sup> cm<sup>−3</sup> and p-type barrier height of 0.48 eV was a good match with the measured specific contact resistance value at 300 K.

There was a slight increase in specific contact resistance after annealing in the p-type case for Pd, which was still acceptable in terms of thermal stability. The increase in specific contact resistance after annealing could be due to redistribution of the Be dopants of some kind. Studies of Pd-based contacts [149] and Mn/Au contact [150] to p-GaAs have shown by SIMS that an outdiffusion of Be towards the GaAs surface occurred after annealing, due to the strong reactivity of the contact with GaAs and the fast diffusion of Be dopant, resulting in increased concentration at the interface. However, in these studies, the pileup of the Be at the interface did not seem to contribute to extremely low contact resistances on its own; the Pd contact had to include another element such as Zn that could fill Ga vacancies produced by the Pd-GaAs reaction and act as acceptors. The p-InGaAs epilayers used in this thesis were doped to higher concentrations of Be than in these studies (> 5 × 10<sup>19</sup> vs. 1 × 10<sup>19</sup> cm<sup>−3</sup>). The thickness of the Pd layer was also much thinner (9 nm) than those used for the p-GaAs/Pd/Au contacts and the Pd-silicide contacts in those studies (> 50 nm).
It has also been observed that the diffusion behavior of Be is concentration dependent in GaAs due to the increase in concentration of Be interstitials as the concentration approaches the solubility limit of Be in GaAs [151] and similarly in InGaAs [152]. At very high Be concentrations (3 \times 10^{19} \text{ cm}^{-3}) in post-growth annealed In_{0.53}Ga_{0.47}As, the effective diffusion coefficient was determined to be 1.8 \times 10^{-13} \text{ cm}^2/\text{s} by analysis of SIMS depth profiles [152]. The diffusion length, \( x \), as a result of the annealing time can be roughly estimated by using the solution to Fick’s first law and the relationship \( x \sim \sqrt{Dt} \), where \( D \) is the diffusion coefficient and \( t \) is the time. For the Pd contacts to p\(^+\)-InGaAs annealed at 350°C/1 h, \( x \) is calculated to be 33 nm. Recalling that the InGaAs epilayer used was 30 nm, and is comparable to the estimated diffusion length of Be after annealing, it is possible that rapid diffusion of Be out to the thin Pd\(_2\)InGaAs phase or to the underlying InP has occurred, leading to increased contact resistance.

The Pt contacts to n- and p-InGaAs showed a slightly different trend. In the n-type case the specific contact resistance did not change significantly after annealing, while in the p-type case it decreased slightly after annealing. Because the specific contact resistance did not change as significantly as for the Mo contacts after annealing, this suggests that changes in an interfacial oxide may not be overwhelmingly determining the contact resistance as it might for a relatively unreactive contact such as Mo. However, because the specific contact resistance is still not as low as the Pd-based contact, the interfacial layer still probably plays an important role. At low temperatures, there is some Pt reaction with the InGaAs surface oxide, which could have resulted in some penetration of the oxide, resulting in lower specific contact resistances than the Mo initially. In the p-type case, the slight decrease in the specific contact resistance after annealing at 350°C could be due to increased reaction of the Pt with the InGaAs along with incomplete dispersion of the oxide. Because of the overall smaller effect of the oxide on the contact resistance of the Pt compared with the Mo, the slight dispersion of the oxide might cause a more significant change in the p-type case due to differences in current transport due to variations in oxide-semiconductor band offsets and hole versus electron effective masses.

The barrier heights were modeled for the as-deposited Pt and Mo contacts to n\(^+\)- and p\(^+\)-InGaAs as well. Their barrier heights were larger than the respective barrier
heights for the Pd contacts in both cases. In general, the metal work functions of the Pt, Pd and Mo do not correlate with the modeled barrier heights in our samples in accordance to Schottky-Mott theory, as shown in Figure 4.16. Possible extrinsic interface states due to Pt-InGaAs reaction could shift the barrier height positively in one case (n or p) but negatively in the other case (p or n). However, it is unclear why the barrier height is shifting upwards for the Pt contact (relative to the Pd contact) for both the p-type and n-type cases.

![Figure 4.16](image)

**Figure 4.16.** Modeled Schottky barrier heights vs. metal work functions for the as-deposited Mo, Pd, and Pt contacts to $n^+\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ ($N_D = 3 \times 10^{19} \text{ cm}^{-3}$) and $p^+\text{In}_x\text{Ga}_{1-x}\text{As}$ ($x = 0.50–0.47$) ($N_A = 8 \times 10^{19} \text{ cm}^{-3}$).

The consistently low specific contact resistances of the Pd contacts to both the heavily-doped n- and p-type InGaAs may also be due to other metal-dependent phenomena that is assisting in current transport. It has been speculated previously that in Pd/Ti/Pt/Au contacts to n-InGaAs [32] and Pd/Ge/Ti/Pt contacts to p-GaAs [58], there may be tunneling occurring via defect states, in addition to direct tunneling through the barrier. These defect states may originate from the initial interaction of the Pd thin film with InGaAs, as Pd was found to be a fast diffuser in GaAs. For
thin Pd films on GaAs, the Pd is the dominant mobile species [99]. Additionally, Olowolafe et al. [153] determined that the penetration of 50 nm Pd into GaAs was diffusion-controlled with a low activation energy of 1.4 eV, and Chen et al. [149] estimated a diffusion distance of 177 nm after 450°C annealing. The fast diffusion of Pd in GaAs is said to occur by diffusion on GaAs interstitial sites due to the low observed activation energy and does not disturb the host lattice [154]. Thus, depending on the thickness of the deposited Pd, there would be a certain depth below the Pd/InGaAs interface where there could be a concentration of Pd point defects, which would be located within the depletion region. These defects would be present below the reacted region within the InGaAs bulk to some extent, even after annealing up to 350°C. The electronic levels of Pd have not been studied in InGaAs, but it is predicted here that they would lie near energy levels near the midgap. Rh and Ir deep levels in In_{0.53}Ga_{0.47}As were determined to have near-midgap energy levels as well. These levels are commonly associated with a specific transition metal acceptor level, and the levels will trend with 3d, 4d, and 5d metals on the periodic table [155]. Thus, diffused Pd defects with midgap energy levels, or possibly other energy levels, could play a role in trap-assisted tunneling in both the heavily-doped n- and p-type case. Additionally, in the p-type case, the specific contact resistance of the as-deposited Pt contact was also over 10 times higher than the Pd contact, while in the n-type case, it was only over 2 times higher. This suggests that in the p-type case, the enhanced tunneling speculated for Pd may lower the contact resistance to a larger extent since the current transport is predicted to be TFE as opposed to FE in the n-type case, where it may not have as much of an effect.

4.9 Conclusions

Ohmic contacts to n^+-InGaAs were investigated with various metals, including Pd, Pt and Mo. The specific contact resistances before and after annealing of these metals were correlated with the morphology and chemistry at the metal-semiconductor interface using primarily TEM analysis. Schottky barrier heights were also extracted based on I-V-T measurements of contacts to lightly-doped n-InGaAs and specific contact resistance modeling.
Mo contacts showed the best morphological stability after annealing as compared with the Pt and Pd. This observation was explained by the differences in reactivity with the InGaAs surface due to the surface preparation method. The Mo contact does not react readily with the oxide on InGaAs at 350°C, while the Pd and Pt contacts were able to penetrate the oxide and react with the InGaAs epilayer, resulting in increased outdiffusion of As at this high temperature or the reaction of Pt with the oxide, respectively. However, the reaction depths of the Pd and Pt after annealing, as measured in TEM, were shown to result in an overestimation of the specific contact resistances, indicating that the current transport was governed by other factors rather than the reaction products.

Pd and Mo contacts to lightly-doped InGaAs did not result in significantly different specific contact resistances. It was revealed that the surface preparation of the InGaAs for ex situ contacts was very important for ohmic contacts to n⁺-InGaAs due to decreased barrier width and current tunneling. A Schottky barrier height of 0.24 eV was extracted for as-deposited Pd and Mo contacts in the lightly-doped case. The effective barrier heights were found to increase in certain cases in the heavily-doped InGaAs contacts, and this finding was correlated with observed interfacial layer or reactions with the InGaAs surface using TEM analysis.

The same contacts to heavily-doped p-InGaAs were tested and compared. Trends in current transport from the results of both sets of contacts were analyzed. It was concluded that the native oxide interfacial layer was the significant factor affecting the specific contact resistance for the Mo contacts. Increased reaction with the interfacial oxide contributed to slightly lower resistance for the Pt contacts. For Pd contacts, the dispersion of the native oxide, and possibly trap assisted tunneling induced by defects due to Pd diffusion in InGaAs that may be enhancing current transport, contributing to very low specific contact resistances in contacts to both n⁺- and p⁺-InGaAs.

In order to design improved non-alloyed ohmic contacts to n⁺- and p⁺-InGaAs it is important to recognize the interfacial morphology and chemistry as a consequence of surface preparation as well as the reactivity of the metal. Special consideration of these factors must be given for very heavily-doped InGaAs, as slight changes in defect concentration or interfacial oxides can modify the current transport behavior for different metallizations. Out of the contact metals studied, Pd-based non-alloyed con-
contacts resulted in the lowest specific contact resistances to both n- and p-type InGaAs, given the surface treatment and annealing conditions. Many metal contact systems to InGaAs that may also satisfy requirements for good thermal stability and low thermal budget relative to the Pd-based contacts have yet to be developed. Finally, it is difficult to obtain ultra-low resistance contacts to lightly-doped InGaAs by non-alloyed contacts even considering surface preparation or metal selection. Thus, it is desirable to explore methods of ohmic contact formation to InGaAs through other avenues, including by engineering the metal/semiconductor interface or by introducing excess doping through novel interfacial reactions.
Chapter 5

Nanopatterned Contacts

5.1 Introduction

This chapter describes the fabrication of nanoscale features at the surface of n-InGaAs as a means of engineering the metal/semiconductor interface and the methods of characterization of these surfaces. Metal contacts were deposited on these surfaces and specific contact resistance measurements were made and compared to those of a planar surface. Specifically, glancing angle deposition (GLAD), selective wet etching and reactive ion etching were employed to alter the surface characteristics of a planar InGaAs surface non-lithographically. Electrical measurements of subsequent contact metallizations resulted in a slight decrease in contact resistance and were correlated with nanoscale surface features. The GLAD processing parameters are also correlated to the feature sizes of the resulting thin films. The effect of both the deposition process parameters and etching characteristics on the semiconductor surface structure, and the contact resistance of subsequently prepared ohmic contact metallizations are discussed.
5.2 Initial Wet Etch Selectivity Testing

5.2.1 Etch Rate Testing

As described previously, the citric acid:H$_2$O$_2$ InGaAs etchant with different ratios by volume were tested in order to determine their selectivity with a normally deposited TiB$_2$ film about 137 nm thick. Based on the etch rates determined in DeSalvo et al. [131], the InGaAs etch times for the different ratios were chosen in order to obtain a target etch depth of 40 nm. For each ratio, the etch rates of both the InGaAs and the TiB$_2$ film were then calculated from contact profilometry measurements, and are shown in Figure 5.1. The etch rate of the InGaAs was much higher than that of the film, with selectivities 9 to 30 times higher, with the selectivity increasing with larger CA:H$_2$O$_2$ ratio.

To further examine the selectivity of the etchant with respect to the use of the TiB$_2$ as an etch mask, a comparison of the different etch rates of a CA:H$_2$O$_2$ (20:1) solution for InGaAs, a GLAD TiB$_2$ film and a planar TiB$_2$ film is shown in Figure 5.2. The etch rate of the GLAD TiB$_2$ film was almost 2 times larger than that of the planar film. Compared to the normally deposited film, the GLAD film probably resulted in

![Figure 5.1. Comparison of etch rates of InGaAs and planar TiB$_2$ film using various citric acid:H$_2$O$_2$ ratios. Where error bars are not shown, the error is within the plot symbol.](image-url)
a more porous morphology with higher surface area and lower density, which enabled a faster etch rate. In terms of selectivity, the etch rate for InGaAs was about 30 times higher than that of the planar TiB$_2$ film and about 20 times higher than that of the GLAD film, which indicated that the TiB$_2$ thin film was a good candidate as an etch mask to create features on the order of 50 nm deep.

![Graph showing etch rates of InGaAs, TiB$_2$ (Planar), and TiB$_2$ (GLAD)](image)

**Figure 5.2.** Comparison of etch rates using citric acid:H$_2$O$_2$ (20:1) solution.

The CA:H$_2$O$_2$ solution with ratio 50:1 was ultimately chosen due to its slower and more controllable etch rate of InGaAs and subsequent TiB$_2$ films. The solution was further calibrated at different depths on both lightly and heavily-doped InGaAs to ensure that the doping density did not significantly affect the etch rate. Indeed, the etch rate did not change with respect to doping density, and the average etch rate for InGaAs was calibrated to be about 46.8 nm/min, and is shown in Figure 5.3. Based on the selectivity experiments of the CA:H$_2$O$_2$ (20:1), the etch rate of the GLAD TiB$_2$ film using the 50:1 solution was approximately 2.5 nm/min.

To remove the TiB$_2$ film to complete the 2-step etch process, the film was etched using a BOE (10:1) solution for 2 min. Initially, an H$_2$O$_2$ (30%) solution was used, but it was found that the film was not able to be completely removed using this solution even after 12 hours.
Figure 5.3. Etch depths versus etch time for heavily and lightly-doped InGaAs epilayers using citric acid:H$_2$O$_2$ (50:1) solution. Where error bars are not shown, the error is within the plot symbol.

5.2.2 AES of Surfaces

Figure 5.4 shows AES performed on surfaces before and after the 2-step etch process of both thin (≈ 3–4 nm) and thick (≈ 50 nm) TiB$_2$ GLAD films on InGaAs to confirm the high selectivity of the CA:H$_2$O$_2$ wet etchant and the complete removal of the TiB$_2$ thin film after BOE etching. For the AES scans, the modified 2-step etch consisted of CA:H$_2$O$_2$ (50:1) for 14 s, followed by H$_2$O$_2$ (30%) for 5 min and finally BOE (10:1) for 2 min. All subsequent 2-step etches did not involve the H$_2$O$_2$ etch, as it was found that the BOE was better able to remove the TiB$_2$ completely.

The AES spectra of the two control samples, a planar TiB$_2$ film ≈ 137 nm thick deposited on Si and the as-received InGaAs epilayer and an as-received InGaAs epilayer, were compared with the 2-step etched surfaces. For both of the as-deposited GLAD TiB$_2$ films along with the control film, the Ti and B peaks can be seen in the AES spectra, indicating that the film was present in all cases. After the 2-step etching was performed on the samples with the GLAD films, the In, Ga and As peaks were seen in the AES spectra, indicating that the TiB$_2$ films were completely removed after the 2-step etch process.
5.3 Thin GLAD Etch Masks

5.3.1 GLAD and Etching Parameters

Lightly-doped InGaAs epilayers were used to test the change in ohmic contact resistance due to the 2-step etching procedure. For the epilayer doping of $1 \times 10^{17}$ cm$^{-3}$, the optimal feature size and spacing needed in order to lower the specific contact resistance significantly was calculated according to the numerical simulation results by Downey et al. [84]. Based on that study, the optimal feature size should have a radius equal to the depletion width formed due to a metal-semiconductor contact and have spacing on the order of 2 times this depletion width. Using the given doping concentration and an assumed Schottky barrier height of 0.2 eV for n-In$_{0.53}$Ga$_{0.47}$As [137, 138, 156], the optimal feature size was calculated to be about 53 nm. Thus, the optimal spacing should be about 100 nm between features.

In order to obtain this optimal feature size and spacing, the main parameters that
were varied were the GLAD vapor angle, the TiB$_2$ film thickness, and the etching time of the InGaAs. Initially, the etch time was varied for a given deposition angle and thickness. The deposition angle was set at 75° and the deposition time was set at 25 s. Various InGaAs etch times were used so that different etch depths would be expected based on the previously calibrated etch rate.

By increasing the deposition vapor angle to 80°, larger shadowing lengths were expected, and thus the column spacing of the GLAD film was expected to be larger. Another set of samples were deposited at this higher angle but also with various thicknesses by increasing the deposition time. Constant InGaAs etch times were used in this set. By altering the thickness of the GLAD film, the column spacing at the surface of the film can change due to increased physical shadowing. A thicker film overall should also be able to withstand a longer InGaAs etch time, allowing a deeper etch of the InGaAs.

An additional pair of ohmic contacts was fabricated to serve as the control condition. For this modified contact, the InGaAs surface was directly etched with CA:H$_2$O$_2$ (50:1) for 28 s. This contact was compared with the modified contacts that underwent the 2-step etch procedure with the various GLAD films and etch times. Table 5.1 shows the conditions used to modify the InGaAs surface before contact deposition.

<table>
<thead>
<tr>
<th>Sample</th>
<th>TiB$_2$ Vapor (degree)</th>
<th>TiB$_2$ Dep. Time (s)</th>
<th>InGaAs Etch Time (s)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Etch only</td>
<td>N/A</td>
<td>N/A</td>
<td>28</td>
</tr>
<tr>
<td>A1</td>
<td>75</td>
<td>25</td>
<td>28</td>
</tr>
<tr>
<td>A2</td>
<td>75</td>
<td>25</td>
<td>42</td>
</tr>
<tr>
<td>A3</td>
<td>75</td>
<td>25</td>
<td>56</td>
</tr>
<tr>
<td>B1</td>
<td>80</td>
<td>25</td>
<td>28</td>
</tr>
<tr>
<td>B2</td>
<td>80</td>
<td>50</td>
<td>28</td>
</tr>
<tr>
<td>B3</td>
<td>80</td>
<td>75</td>
<td>28</td>
</tr>
</tbody>
</table>

**Table 5.1.** Conditions for modified InGaAs using thin TiB$_2$ GLAD etch masks and CA:H$_2$O$_2$ (50:1) InGaAs etchant before contact deposition.

### 5.3.2 Electrical Characterization Results

For each surface modification condition listed in Table 5.1, a Ti/Pt/Au ohmic contact to the modified InGaAs surface was fabricated in a concurrent deposition with an unmodified control sample, where the InGaAs surface was not purposely
altered in any way, and a blank InGaAs piece used for surface characterization. Before contact metallization or surface characterization, for each trio of samples, a standard cleaning procedure was performed, which involved a 10 min UV-ozone surface clean at 1.0 SLPM and a 2 min BOE etch. These procedures were described in more detail in the Experimental Methods (Chapter 3).

For each pair of ohmic contacts, the sheet resistances extracted from each pair of samples did not vary significantly, indicating that the intentional surface modification did not change the thickness or resistance under the contact metal. This allowed a valid comparison of the extracted specific contact resistances between the unmodified control samples and their etched counterparts using the CTLM model. The extracted sheet resistances of all the unmodified and modified contacts averaged $357 \pm 18.0 \ \Omega/\square$.

### 5.3.2.1 Specific Contact Resistance After Surface Modification

For the modified samples of set A from Table 5.1, with TiB$_2$ GLAD etch masks deposited at 75° for 25 s, and InGaAs etched at different times, the extracted specific contact resistances and sheet resistances are shown in Figure 5.5, where they are compared to their corresponding unmodified contact from the same deposition. The specific contact resistances decreased by about 28–44% from their unmodified counterpart. Compared with the 20% decrease for the control sample etched without an etch mask for 28 s, the improvement was also greater. The unmodified samples had extracted specific contact resistances ranging from $6.0–8.5 \times 10^{-5} \ \Omega$-cm$^2$, while the values ranged from $3.3–6.0 \times 10^{-5} \ \Omega$-cm$^2$ for the modified samples. The variation in the original specific contact resistances for the unmodified samples could be due to environmental fluctuations from batch to batch, especially during sample cleaning and metal deposition.

Similarly, for the modified samples of set B from Table 5.1, with TiB$_2$ GLAD etch masks deposited at 80° for 25, 50 and 75 s, and InGaAs etched at 28 s, the pairs of extracted specific contact resistances and sheet resistances are shown in Figure 5.6, along with the control pair. There did not seem to be a significant decrease in specific contact resistance for the constant etch time of 28 s. The modified samples exhibited a specific contact resistance of around $4.6 \times 10^{-5} \ \Omega$-cm$^2$. 
Figure 5.5. Extracted electrical data from modified contacts using TiB_2 GLAD etch mask deposited at 75° and 25 s, with InGaAs etched at various times, and etched-only control contact: (a) specific contact resistances and (b) sheet resistances.
Figure 5.6. Extracted electrical data from modified contacts using TiB$_2$ GLAD etch mask deposited at 80° and 25, 50, and 75 s, with InGaAs etched at 28 s, and etched-only control contact: (a) specific contact resistances and (b) sheet resistances.
5.3.3 AFM Analysis

5.3.3.1 RMS Roughness

In order to further examine the modified surfaces and attempt to correlate the surface morphology with the electrical data, AFM scans were performed for corresponding blank witness samples that also were subjected to the TiB$_2$ deposition and 2-step etch process. All subsequent image processing was done on 1x1 $\mu$m images with 512 pixel/line resolution. A first-order plane fitting followed by a first-order flattening routine was performed using Nanoscope (Bruker) software. Two control samples were also scanned, an as-received InGaAs sample and an InGaAs sample etched for 28 s with CA:H$_2$O$_2$ (50:1). Before the AFM scans, both of these samples were treated with UV-ozone and BOE strip, mimicking the surface cleaning conditions before metal contact deposition. The AFM images for the two control samples are shown in Figure 5.7. As expected, the as-received sample had a very smooth surface with a very low $R_q$ (RMS roughness). After etching the InGaAs surface with the CA:H$_2$O$_2$ (50:1) etchant for 28 s, bumps became visible throughout the surface and the $R_q$ increased slightly.

![AFM images of surfaces of control samples: (a) as-received and (b) etched 28 s](image)

**Figure 5.7.** AFM images of surfaces of control samples: (a) as-received and (b) etched 28 s.

For the modified samples of Set A (75°/25 s deposition time GLAD parameters), the $R_q$ increased slightly compared with the control samples as the InGaAs etch time was increased, but then decreased slightly after the 56 s etch. The AFM images for these modified samples are shown in Figure 5.8, and a comparison of the $R_q$ values
with the control samples are shown in Figure 5.9. The overall increased \( R_q \) of each of the modified samples correlates to the higher decrease in specific contact resistance as compared with the control sample that was etched without any GLAD etch mask.

![AFM images of modified samples of Set A](image)

**Figure 5.8.** AFM images of modified samples of Set A: (a) 28 s (b) 42 s, and (c) 56 s.

![RMS roughness values](image)

**Figure 5.9.** RMS roughness values for Set A and control samples. Where error bars are not shown, the error is within the plot symbol.

For the 80°/28 s etch modified samples of Set B (Figure 5.10), the increase in \( R_q \) (Figure 5.11) was not as large as the modified samples of Set A. Compared with the as-received samples, there was a slight increase in \( R_q \) after it was etched for 28 s, but for the modified samples, the \( R_q \) did not increase much higher. The average \( R_q \) values for the modified samples of Set B were lower than those of Set A, suggesting that more etching of the substrate may have occurred in the samples of Set A. Additionally, in Set B, there was no significant decrease in specific contact resistance as compared to the corresponding un-modified contacts or the 28 s etched control sample.
The actual thicknesses of the GLAD film for the 80° vapor case were too thin to measure, and may not actually vary as much as expected with respect to the deposition times, which may indicate why there did not seem to be any significant change in roughness for any condition within this set. The etch time of the InGaAs may be more important in creating increasing roughness of the surface in the case of such thin GLAD films. The typical line profiles of these AFM scans all show peak-to-peak heights less than 5 nm, indicating that the InGaAs was not being etched to the depths based on the calibrated etch rates. The thin GLAD films might be too thin and may be prone to lower selectivity at these thicknesses when using the CA:H₂O₂ (50:1) etchant.

![AFM images](image)

**Figure 5.10.** AFM images of modified samples of Set B: (a) 28 s (b) 50 s, and (c) 75 s.

![RMS roughness graph](image)

**Figure 5.11.** RMS roughness values for Set B and control samples. Where error bars are not shown, the error is within the plot symbol.
5.3.3.2 PSD Analysis

In addition to comparing the RMS roughness of the modified surfaces, the characteristic lateral feature widths can also be examined from the AFM images using pulsed spectral density information. This data reveals information about spatial frequency, which can vary even if the $R_q$ values are similar for different samples.

For the modified samples of Set A and B, their 2DPSD functions are plotted in Figure 5.12 and 5.13 along with those of the as-received substrate and of the etched sample without a GLAD mask. The shape of the PSD curves for the etched samples are characteristic of randomly rough surfaces, where there is a transition point between the plateau region (low frequency region) and the linear region (high frequency region). In the linear region, the roughness is self-similar, where the magnitude of the individual height deviations from the mean value along a profile of the surface varies in a constant manner over the entire length scale [132].

![Figure 5.12. PSD for Set A and control samples.](image)

For the case of the modified or etched samples, the characteristic feature sizes were extracted by taking the inverse of the spatial frequency at the transition point of the 2DPSD curves, and are in the range of 18–50 nm, as shown in Table 5.2. These values were estimated to be at the intersection of the linear best fit curves with boundaries from 0 to $x_1$ and $x_2$ to 256, where $x_1 = x - 5$, $x_2 = x + 5$, and $x$ is the best initial
Figure 5.13. PSD for Set B and control samples.

guess for the spatial frequency at the transition point. The curve for the as-received surface shows no clear transition point over the frequency range, indicating that it is a very smooth surface, as expected. In the samples of Set A, the modified surfaces have larger feature sizes when compared with the control sample and the modified samples of Set B. Set B has features sizes similar to that of the control sample. These results correlate with the slightly higher RMS roughness of Set A samples. The smoother surfaces of Set B may contribute to the unchanged specific contact resistance after surface modification.

<table>
<thead>
<tr>
<th>Set and Sample</th>
<th>GLAD Angle-Deposition Time /InGaAs Etch Time</th>
<th>Spatial Freq. (μm⁻¹)</th>
<th>Characteristic Feature Size (nm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Etch only</td>
<td>As-Received/28s</td>
<td>36 ± 0.1</td>
<td>28 ± 0.1</td>
</tr>
<tr>
<td>A1</td>
<td>75°-25 s/28 s</td>
<td>30 ± 0.5</td>
<td>33 ± 1</td>
</tr>
<tr>
<td>A2</td>
<td>75°-25 s/42 s</td>
<td>20 ± 2</td>
<td>50 ± 5</td>
</tr>
<tr>
<td>A3</td>
<td>75°-25 s/56 s</td>
<td>27 ± 0.2</td>
<td>37 ± 0.3</td>
</tr>
<tr>
<td>B1</td>
<td>80°-25 s/28 s</td>
<td>36 ± 0.2</td>
<td>28 ± 0.2</td>
</tr>
<tr>
<td>B2</td>
<td>80°-50 s/28 s</td>
<td>57 ± 0.1</td>
<td>18 ± 0.03</td>
</tr>
<tr>
<td>B3</td>
<td>80°-75 s/28 s</td>
<td>35 ± 0.2</td>
<td>29 ± 0.2</td>
</tr>
</tbody>
</table>

Table 5.2. Characteristic feature spacing determined from PSD spectra.

At such short deposition times at these high vapor angles, the effect of the etch times on the modification of the surface is more significant than the effect of the
change in deposition time. Undercutting or low selectivity may have been possible during the duration of the etch, for the samples of the 80° vapor case (Set B) as the density of these films may be lower compared to those deposited in the 75° vapor case (Set A).

Also the TiB$_2$ GLAD layer, however seemingly porous at the surface, seemed to also be inhibiting the wet etch rate of the InGaAs etchant. Larger pores and thicknesses were needed to fabricate the deeper features predicted for the particular doping concentration of the InGaAs epilayer.

5.4 GLAD Film Processing Refinement

In order to better understand the GLAD process parameters and their effects on the morphology, thickness and porosity of the resulting film, a series of deposition parameters were studied. TiB$_2$ GLAD films were studied using SEM and image analysis software. The parameters for this study are applicable to the particular deposition system and InGaAs substrate, and TiB$_2$ material. The most important parameters involved in determining the GLAD film morphology were the vapor angle, thickness and substrate rotation. Several sets of GLAD TiB$_2$ depositions were performed and displayed in Table 5.3.
<table>
<thead>
<tr>
<th>Run</th>
<th>Angle (deg.)</th>
<th>Evaporation Rate (Å/s)</th>
<th>Deposition Time (s)</th>
<th>Deposition Rate (nm/s)</th>
<th>Thickness QCM (nm)</th>
<th>Thickness Actual (nm)</th>
<th>Rotation Speed (rpm)</th>
<th>Thickness/revolution (nm/rev)</th>
</tr>
</thead>
<tbody>
<tr>
<td>A01</td>
<td>75</td>
<td>2</td>
<td>125</td>
<td>0.05</td>
<td>25</td>
<td>7.1 ± 1.0</td>
<td>9</td>
<td>0.38</td>
</tr>
<tr>
<td>A02</td>
<td>75</td>
<td>2</td>
<td>250</td>
<td>0.03</td>
<td>50</td>
<td>8.5 ± 0.5</td>
<td>9</td>
<td>0.23</td>
</tr>
<tr>
<td>A03</td>
<td>75</td>
<td>2</td>
<td>500</td>
<td>0.06</td>
<td>100</td>
<td>32 ± 1</td>
<td>9</td>
<td>0.43</td>
</tr>
<tr>
<td>A04</td>
<td>75</td>
<td>2</td>
<td>1000</td>
<td>0.05</td>
<td>200</td>
<td>54 ± 4</td>
<td>9</td>
<td>0.36</td>
</tr>
<tr>
<td>B05</td>
<td>80</td>
<td>2</td>
<td>125</td>
<td>N/A</td>
<td>25</td>
<td>Very thin</td>
<td>9</td>
<td>N/A</td>
</tr>
<tr>
<td>B06</td>
<td>80</td>
<td>2</td>
<td>250</td>
<td>N/A</td>
<td>50</td>
<td>Very thin</td>
<td>9</td>
<td>N/A</td>
</tr>
<tr>
<td>B07</td>
<td>80</td>
<td>2</td>
<td>500</td>
<td>0.05</td>
<td>100</td>
<td>23 ± 2</td>
<td>9</td>
<td>0.31</td>
</tr>
<tr>
<td>B08</td>
<td>80</td>
<td>2</td>
<td>1000</td>
<td>0.05</td>
<td>200</td>
<td>46 ± 2</td>
<td>9</td>
<td>0.31</td>
</tr>
<tr>
<td>C09</td>
<td>85</td>
<td>2</td>
<td>500</td>
<td>0.02</td>
<td>100</td>
<td>7.5 ± 0.6</td>
<td>9</td>
<td>0.1</td>
</tr>
<tr>
<td>C10</td>
<td>80</td>
<td>2</td>
<td>500</td>
<td>0.05</td>
<td>100</td>
<td>23 ± 2</td>
<td>9</td>
<td>0.31</td>
</tr>
<tr>
<td>C11</td>
<td>75</td>
<td>2</td>
<td>500</td>
<td>0.06</td>
<td>100</td>
<td>32 ± 1</td>
<td>9</td>
<td>0.43</td>
</tr>
<tr>
<td>C12</td>
<td>60</td>
<td>2</td>
<td>500</td>
<td>0.12</td>
<td>100</td>
<td>58 ± 0.4</td>
<td>9</td>
<td>0.77</td>
</tr>
<tr>
<td>C13</td>
<td>45</td>
<td>2</td>
<td>500</td>
<td>0.14</td>
<td>100</td>
<td>70 ± 5</td>
<td>9</td>
<td>0.93</td>
</tr>
<tr>
<td>D14</td>
<td>85</td>
<td>7.9 (Failed)</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
</tr>
<tr>
<td>D15</td>
<td>80</td>
<td>2.8</td>
<td>773</td>
<td>0.07</td>
<td>215</td>
<td>58 ± 3</td>
<td>9</td>
<td>0.5</td>
</tr>
<tr>
<td>D16</td>
<td>75</td>
<td>2.0</td>
<td>775</td>
<td>0.06</td>
<td>155</td>
<td>46 ± 2</td>
<td>9</td>
<td>0.39</td>
</tr>
<tr>
<td>D17</td>
<td>60</td>
<td>1.1</td>
<td>773</td>
<td>0.06</td>
<td>85</td>
<td>43 ± 2</td>
<td>9</td>
<td>0.37</td>
</tr>
</tbody>
</table>

Table 5.3. GLAD Parameters for TiB<sub>2</sub> films in e-beam evaporation system.
For the first two sets of A and B, the vapor angle was changed as a function of deposition time with a constant evaporation rate of 2 Å/s in order to determine the deposition rate as compared to a sample deposited under regular (0°) vapor angle conditions. The actual measured thicknesses were measured by fracture cross-sections in FESEM. The evaporation rate was measured by a quartz crystal monitor placed below the samples and calibrated for normal TiB₂ deposition conditions. The substrate rotation was also kept constant at 9 revolutions per minute. For the vapor angles of 75° and 80°, the deposition time was changed from 125 to 1000 s. The measured thicknesses are shown in Figure 5.14.

![Figure 5.14](image.png)

**Figure 5.14.** TiB₂ thickness as a function of deposition time for 75° and 80° vapor angles at 2 Å/s evaporation rate. Where error bars are not shown, the error is within the plot symbol.

The corresponding SEM surface images for the samples deposited at 75° and 80° are shown in Figure 5.15 and 5.16, respectively. It was observed that as the thickness becomes larger for a given vapor angle, the columnar structure of the film became more individually well-defined at the surface, indicating that the dominant mechanism at larger thicknesses is physical shadowing rather than diffusion.

For various vapor angles, Figure 5.17 shows a comparison of the predicted film
thickness versus the deposition time for normally deposited films at the evaporation rate of 2 Å/s based on the measured thicknesses for samples deposited at 75° and 80°. Recalling the contacts of the previous section, where the deposition times were 25, 50, and 75 s, the actual film thicknesses are very small and vary according to the vapor angle used. For 75° films with 25 s deposition times, the actual film thickness is probably about 1.6 nm. For the 80° films with 25, 50 and 75 s deposition times, the actual film thicknesses can be extrapolated to be 1.2, 2.3, and 3.5 nm, respectively.

GLAD films of Set C were deposited at different vapor angles with the constant evaporation rate of 2 Å/s and 500 s deposition time. The measured thickness as a function of vapor angle is shown in Figure 5.18. The non-linear relationship reveals an increase in the source-to-substrate distance as the angle is increased. Thus, it was important to determine the ratios between deposition time and thickness for each vapor angle in order to calibrate evaporation rates.

The calibrated evaporation rates were used in order to achieve films of the same thicknesses with the same deposition rate over several vapor angles. After calibration of the evaporation rate, GLAD films predicted to be about 50 nm thick were
Figure 5.16. SEM images of TiB$_2$ film surface at various deposition times deposited at 80° vapor angle at 2 Å/s evaporation rate: (a) 125 s, (b) 250 s, (c) 500 s, and (d) 1000 s.

Figure 5.17. Calculated TiB$_2$ thickness as a function of deposition time deposited with 2 Å/s evaporation rate.
Figure 5.18. Measured TiB\textsubscript{2} thickness as a function of vapor angle deposited with 2 Å/s evaporation rate for 500 s. Where error bars are not shown, the error is within the plot symbol.

deposited at 60°, 75°, and 80° with the same deposition rate of about 0.07 nm/s. The calibrated evaporation rates and the comparison between the QCM and actual measured thicknesses are shown in Figure 5.19.

Figure 5.19. Calibration of evaporation rate to achieve 50 nm TiB\textsubscript{2} GLAD films with a constant deposition rate as a function of vapor angle. Where error bars are not shown, the error is within the plot symbol.
The SEM images in Figure 5.20 show that the surface morphology reveals much more porosity at the higher vapor angle. Even at 60 degrees, there is very little porosity, and the cross-sectional images also reveal that there are very distinct columns for the films deposited at 75° and 80°, whereas the film deposited at 60° are still quite dense. As the angle increases, the density of the columns and porosity between columns increases, due to increased physical shadowing.

![SEM images of TiB₂ film surface and fracture cross-sections deposited at the same deposition rate of 0.07 nm/s to about 50 nm but at different vapor angles: (a) 80°, (b) 75°, and (c) 60°.](image)

**Figure 5.20.** SEM images of TiB₂ film surface and fracture cross-sections deposited at the same deposition rate of 0.07 nm/s to about 50 nm but at different vapor angles: (a) 80°, (b) 75°, and (c) 60°.

It was concluded that thicker GLAD films would serve as better etch masks than the very thin ones used in the previous section to make the ohmic contacts. However, it is of note that there is very little porosity in the films when they are very thin as compared to the thick ones. It is difficult for the wet etchant to reach into the substrate if there is little space between the columnar structures of the film near the substrate surface.
5.5 Thick GLAD Films

It was difficult to etch InGaAs through the thin GLAD etch mask and as a result there was only a small change in specific contact resistance after the 2-step wet etching procedure. The refinement of the GLAD process parameters showed that in addition to the vapor angle, the thickness of the film was also important in determining the column development and porosity at the surface of the film. Thicker films were also deemed to have better selectivity with the InGaAs etchant for the same etch time.

5.5.1 Wet Etch Selectivity

For TiB$_2$ GLAD films deposited at 75° with different thicknesses, the 2-step etch procedure was performed with longer etch times, and SEM images of the surfaces are shown in Figure 5.21. AES survey scans were used to determine the elements present on the surface after each step of the etching procedure. It was found that for 64 s InGaAs etch, the film seemed to have been completely removed when the thickness was 16 nm. Delamination of the film may have occurred due to agitation of the etchant. For films with thicknesses above 30 nm, the 64 s and longer InGaAs etch seemed to etch the film significantly so that the morphology looked flatter and damaged, but there was still TiB$_2$ on the surface. After complete removal by BOE, there was no Ti or B present. Additionally, the surface had a bumpy morphology. An AFM scan of the final surface shows more roughness, with an RMS roughness of 2.5 nm, as compared with the as-received InGaAs surface. However, the peak-to-peak feature height is only on average 5–8 nm, which indicates that the wet etchant was not able to penetrate the substrate, possibly due to the film not being completely porous.

InGaAs surfaces etched directly at different times using the CA:H$_2$O$_2$ (50:1) etchant were also examined by SEM in order to compare with those etched with a TiB$_2$ etch mask. The SEM images of Figure 5.22 show that even without an etch mask, the etchant seemed to roughen the InGaAs surface and leave uneven areas on the surface. This result was consistent with the 64 s etched sample with the 16 nm etch mask from Figure 5.21. The roughening of the surface using this etchant may be due to preferential etching in the proximity of defects, contamination or lithographic
Figure 5.21. SEM images of thicker TiB$_2$ GLAD films deposited at 75° having undergone the 2-step etch procedure with greater than 64 s InGaAs etch and 2 min BOE: (a) 16 nm (b) 32 nm, and (c) 49 nm.

features [157].

The etching results here indicated that a TiB$_2$ GLAD film thicker than 30 nm was recommended, if an etch time of over 64 s was used. Otherwise, the GLAD film was either etched completely or delaminated from the substrate. This 64 s etch time corresponded to an etch depth of 50 nm, but the resulting features in the InGaAs after the film removal did not correspond to this depth. No matter the thickness,
the GLAD film seemed to be impeding the ability of the InGaAs etchant to have a similar etch rate as calibrated from InGaAs samples with photoresist.

Figure 5.22. SEM images of (a) as-received InGaAs surface, etched with CA:H₂O₂ (50:1) at various times: (b) 16 s (c) 70 s (d) 103 s, and (e) 256 s.

5.5.2 Three-Step Etch

To introduce more porosity to the TiB₂ GLAD film, the film itself was etched for very short times using a very diluted BOE solution (90% H₂O:10% BOE) before the
2-step etch process. The SEM surface images in Figure 5.23 show the as-deposited GLAD films at 75° with deposition rate of 0.07 nm/s and thickness of 30 nm. After short etching times using the diluted BOE solution, the GLAD film was etched non-uniformly, resulting in random, larger spacing between columns, until it was completely etched away.

![SEM images of TiB2 GLAD film deposited at 75° with thickness of about 30 nm: (a) as-deposited, etched with diluted BOE solution at various times: (b) 5 s (c) 10 s and (d) 15 s.](image)

The 2-step etch was then applied after short, diluted BOE etch times and is shown in Figure 5.24. An InGaAs etch time of 32 s was chosen in light of the knowledge that the 56 s and 64 s etch times were able to remove or damage the TiB2 film for the samples with thicknesses less than 30 nm. After removal of the film by BOE, there looked like there were large areas where the film had acted as an etch mask. AFM images of this surface also showed features about 15 nm from peak-to-peak and a larger RMS roughness of 4.3 nm, larger than for the modified surfaces using the very thin GLAD films. When using an InGaAs etch time of 64 s, it seemed like the GLAD film was not able to withstand the etchant as long, as it looked like much of
the film was being undercut by the etchant. The resulting surface after film removal had a lower RMS roughness of 1.3 nm, with smaller features as a consequence.

![SEM images](image)

**Figure 5.24.** SEM images of TiB$_2$ GLAD film deposited at 75° with a thickness of about 30 nm which underwent the 3-step etch process: (a) as-deposited; (b) etched with diluted BOE solution for 5 s; etched with CA:H$_2$O$_2$ (50:1) for (c) 32 s (d) 64 s, and (e-f) TiB$_2$ removed using BOE.

### 5.5.3 Dry Etching

In order to prevent undercutting from occurring as a result of using the wet-etchant, reactive ion etching was attempted to replace the InGaAs wet etch step from the 3-step etch procedure. An ICP RIE was used with a recipe of Ar/BCl$_3$ 12/48 sccm at 3 mTorr with a sample bias of 100 W and ICP power of 75 W to etch the InGaAs. The RIE etch rate was calibrated on an InGaAs epilayer patterned with photoresist lines spaced about 2-4 microns apart. With no other initial surface clean such as BOE, the etch rate was calculated to be 0.67 nm/s.

Using a GLAD film deposited at 75° with thickness of about 30 nm, the film was first etched with the diluted BOE solution for 3 seconds. SEM images in Figure 5.25 clearly show that increased porosity at the surface was achieved as compared with the as-deposited sample. The RIE times of 30, 60, and 90 s were chosen for the InGaAs samples with GLAD films deposited. For the sample etched for 90 s, the film seemed
to be damaged and rounded. After the RIE, the film was removed using BOE, and the AFM images are shown in Figure 5.26. The RMS roughness of these respective InGaAs surfaces increased with RIE times from 2.0 to 5.8 to 13.0 nm.

![SEM images of TiB$_2$ GLAD film deposited at 75$^\circ$ with thickness of about 30 nm after RIE: (a) as-deposited; (b) etched with diluted BOE solution for 3 s: RIE for (c) 30 s (d) 60 s, and (e) 90 s.]

![AFM images InGaAs surface after TiB$_2$ GLAD film deposited at 75$^\circ$ with thickness of about 30 nm undergoing 3-step etch process: (a) 30 s (b) 60 s, and (c) 90 s.]

A second sample was etched at 45 s and 70 s. It was observed that for samples etched at 70 s and higher, the GLAD film seemed to be damaged and became rounded, or the film might have been completely etched away. AFM and SEM images show that an etch time of 45 to 60 s is needed to introduce roughness to the sample.
5.5.4 UV-Ozone Treatment

In order to improve the consistency of the InGaAs etch rate, the increased roughness of the wet etching alone on the control samples of InGaAs was also explored. The large bumps in the surface after successively longer etch times were suspected to be a hinderance to a smooth, consistent etch rate. After etching at 56 s to create an etch depth of 35 nm, there were large bumps randomly distributed on the InGaAs surface. These bumps may be due to photoresist residue on the surface of the InGaAs after photolithography. Photoresist residue is known to be about 2–3 nm thick; the wet-etching rate may be impeded by this residue, causing increased roughness due to non-uniform etching of the material. Using UV-ozone treatment for 10 min, the surface of the etched sample was removed of the large bumps, as shown in Figure 5.27.

![Figure 5.27. SEM images of InGaAs surface (a) etched with CA:H$_2$O$_2$ (50:1) for 56 s and (b) after subsequent UV-ozone treatment.](image)

Before wet-etching, the UV-ozone treatment was also tested to see how that would affect the appearance of the etched surfaces, and are shown in Figure 5.28. For a 50 s etch with UV-ozone treatment before etching, the resulting surface looked smoother but the etch rate was much slower, probably due to the oxide grown on the surface. With the addition of the BOE strip, the etched InGaAs had very small bumps and a slightly higher etch rate, but the bumps were not as large or as dispersed as that of the etched surface with no UV-ozone treatment. It was concluded that after photolithography, a UV-ozone treatment was necessary in order to allow more consistent wet etching rates and more uniform etching at some point before InGaAs etching is performed.
Figure 5.28. SEM images of InGaAs surface etched with CA:H$_2$O$_2$ (50:1) for 50 s after (a) UV-ozone and BOE strip and (b) UV-ozone treatment.

5.5.5 Contact Fabrication

Final sets of Ti/Pt/Au (9/15/100 nm) contacts were then fabricated taking into consideration the previous observations about the use of the thick GLAD etch mask. Two sets of contacts were fabricated using RIE during the 3-step procedure while another two sets were fabricated using CA:H$_2$O$_2$ (50:1) during the 3-step etch procedure. The GLAD and etch parameters used to modify the samples before contact deposition for the RIE and wet-etched samples are shown in Tables 5.4 and 5.5, respectively. In all sets, an unmodified control sample (CTRL) was included. In some cases, an etched-only control sample (ET) was also included where no GLAD film was deposited before etching the InGaAs. For all samples, UV-ozone treatment and BOE strip was performed after photolithography and before either GLAD and/or etching of the InGaAs, and again before contact deposition. The GLAD film was fabricated on all samples within the same deposition.
<table>
<thead>
<tr>
<th>Set - Sample</th>
<th>GLAD TiB₂</th>
<th>Target</th>
<th>Etch 1: TiB₂</th>
<th>Etch 2: InGaAs</th>
<th>Etch 3: TiB₂</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Angle (deg.)</td>
<td>Thickness (nm)</td>
<td>dBOE (s)</td>
<td>RIE (s)</td>
<td>BOE (s)</td>
</tr>
<tr>
<td>1-A</td>
<td>80</td>
<td>50</td>
<td>5</td>
<td>20</td>
<td>120</td>
</tr>
<tr>
<td>1-B</td>
<td>80</td>
<td>50</td>
<td>5</td>
<td>40</td>
<td>120</td>
</tr>
<tr>
<td>1-C</td>
<td>80</td>
<td>50</td>
<td>5</td>
<td>60</td>
<td>120</td>
</tr>
<tr>
<td>1-CTRL</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
</tr>
<tr>
<td>2-A</td>
<td>80</td>
<td>50</td>
<td>3</td>
<td>40</td>
<td>120</td>
</tr>
<tr>
<td>2-B</td>
<td>80</td>
<td>50</td>
<td>8</td>
<td>40</td>
<td>120</td>
</tr>
<tr>
<td>2-C</td>
<td>80</td>
<td>50</td>
<td>10</td>
<td>40</td>
<td>120</td>
</tr>
<tr>
<td>2-ET</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
<td>40</td>
<td>N/A</td>
</tr>
<tr>
<td>2-CTRL</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
</tr>
</tbody>
</table>

Table 5.4. 3-step etch parameters for contacts where the InGaAs underwent RIE using BCl₃/Ar.

<table>
<thead>
<tr>
<th>Set - Sample</th>
<th>GLAD TiB₂</th>
<th>Target</th>
<th>Etch 1: TiB₂</th>
<th>Etch 2: InGaAs</th>
<th>Etch 3: TiB₂</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Angle</td>
<td>Thickness (nm)</td>
<td>dBOE (s)</td>
<td>CA:H₂O₂ (s)</td>
<td>BOE (s)</td>
</tr>
<tr>
<td>3-A</td>
<td>80</td>
<td>50</td>
<td>3</td>
<td>20</td>
<td>120</td>
</tr>
<tr>
<td>3-B</td>
<td>80</td>
<td>50</td>
<td>3</td>
<td>40</td>
<td>120</td>
</tr>
<tr>
<td>3-C</td>
<td>80</td>
<td>50</td>
<td>3</td>
<td>60</td>
<td>120</td>
</tr>
<tr>
<td>3-CTRL</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
</tr>
<tr>
<td>4-A</td>
<td>80</td>
<td>30</td>
<td>3</td>
<td>40</td>
<td>120</td>
</tr>
<tr>
<td>4-B</td>
<td>80</td>
<td>70</td>
<td>3</td>
<td>40</td>
<td>120</td>
</tr>
<tr>
<td>4-ET</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
<td>40</td>
<td>N/A</td>
</tr>
<tr>
<td>4-CTRL</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
</tr>
</tbody>
</table>

Table 5.5. 3-step etch parameters for contacts where the InGaAs underwent wet etching using CA:H₂O₂ (50:1).
For the samples of the contacts modified by RIE during the 3-step etch process (Sets 1 and 2), I-V measurements showed up to 85% decrease in specific contact resistance when compared to the corresponding unmodified control sample. However, the specific contact resistances either stayed the same or slightly increased for the modified samples after the 3-step wet etch process. The specific contact resistances for Set 1 and 2 are plotted in Figures 5.29. Gap spacings for Set 1 were the only ones measured in the SEM; average gap spacings were then used for subsequent sets. The extracted semiconductor sheet resistances of all the contacts in all the sets also did not change significantly, with an average of $458 \pm 41 \ \Omega/\square$.

In Set 1, where the InGaAs etch time was varied from 20-60 s, the lower decrease in specific contact resistance after longer etch times may be due to increased surface damage. In Set 2, where the etch time was kept constant at 40 s, but the GLAD film etching time was varied from 3-10 s, the decrease in specific contact resistance did not seem to vary. The etching of the film using the diluted BOE solution did not make a significant difference in the etch mask before etching of the InGaAs. Additionally, the optimal feature size calculated for the doping density was approximately 30 nm, which corresponded to the calibration of the 40 s etch time resulting in an etch depth of 27 nm.

For Sets 3 and 4, where the InGaAs was etched using the wet etchant rather than RIE, the insignificant changes in specific contact resistances after surface modification was more puzzling. It was possible that the InGaAs surface was not being sufficiently roughened by the etchant due to the presence of the GLAD film. The RIE probably resulted in higher aspect ratio surface features than the wet etchant.

### 5.6 Conclusions

The GLAD method was used to deposit TiB$_2$ films for use as etch masks for InGaAs epilayers. The etched surfaces resulted in random features about 30–50 nm wide but were very shallow at about 2-3 nm deep. Both very thin ($< 5$ nm) and thick (30–70 nm) films were deposited as etch masks. There was an increase in RMS roughness and lateral feature size in the surface of the InGaAs as compared with surfaces that were etched without using a GLAD film, resulting in slight reduction in
Figure 5.29. Specific contact resistances for (a) Set 1 and (b) Set 2, which underwent a 3-step modification process with RIE and additional UV-ozone treatment.
specific contact resistances.

However, it was difficult to achieve deep features using the calibrated etch rates even after modifying the etch and GLAD parameters. There seemed to be a limitation for the ability of the etchant to penetrate the InGaAs within the columnar morphology of the GLAD film. The GLAD method as an etch mask may have an inherent limitation if a smooth surface is used for the substrate, as there would not be sufficient physical shadowing to permit growth of widely spaced columns from just the asperities on the smooth surface. Another limitation is selecting a film and etchant combination that is sufficiently selective with respect to the etch rate of the InGaAs. However, the multi-step etch method using a GLAD film shows potential as a method for introducing controlled nanomorphology at a substrate surface and might be used in other applications where increased surface area may be advantageous.
Chapter 6

Solid-Phase Regrowth Contacts

6.1 Introduction

This chapter presents and discusses Pd/Si/Pd solid-phase regrowth contacts fabricated to n-In$_{0.53}$Ga$_{0.57}$As epilayers as a method to introduce excess dopant at the metal/semiconductor interface. There have been limited studies of Pd/Si based SPR contacts to n-InGaAs. Here a Pd/Si/Pd SPR contact was fabricated using a low-temperature, two-step annealing process that results in the formation of shallow, ultra-low resistance ohmic contacts with little lateral diffusion. The Pd/Si atomic ratio was optimized for the SPR process. Extremely low specific contact resistances on the order of $9 \times 10^{-8}$ and $1.8 \times 10^{-8}$ Ω-cm$^2$, respectively, were measured for both lightly and heavily-doped n-InGaAs. The ohmic behavior for the lightly-doped epilayers was confirmed to be due to the addition of increased Si dopant concentration at the InGaAs interface from the SPR process. XTEM and XEDS analysis was used to corroborate the SPR mechanism with the electrical measurements at each step of the annealing process. An additional study using the same contact was fabricated on heavily-doped p-InGaAs using the same contact as a comparison. The resulting specific contact resistance was unexpectedly low and reveals that other mechanisms may be involved which may have implications for studies involving ohmic contacts to p-InGaAs.
6.2 Specific Contact Resistance of Pd/Si/Pd Contacts

Several annealing times and temperatures were tested in order to determine the optimum two-step annealing parameters of the Pd/Si/Pd SPR contact and the effects on reaching ultra-low specific contact resistances. Additionally, varying layer thicknesses of Pd and Si were studied in order to determine the effect on SPR formation.

6.2.1 Effect of Annealing Temperatures and Times

For the as-deposited SPR contacts to the lightly-doped epilayers of $N_D = 1 \times 10^{17}$ cm$^{-3}$, I-V measurements revealed that they were non-ohmic. After the first-step anneal at 200$^\circ$C and 30 s, the specific contact resistance values were on the order of $10^{-4}$ Ω-cm$^2$.

The first-step annealing time was kept constant at 200$^\circ$C and 30 s in all cases. For two SPR contacts with the same Pd/Si/Pd layer thicknesses but different Ti thicknesses (30 and 40 nm) and a constant second-step anneal time at 380$^\circ$C, Figure 6.1 shows a decrease in specific contact resistance with increasing annealing times. At a second-step anneal time of 40 s, the specific contact resistance also decreases slightly and remains low, as shown in Figure 6.2.

The subsequent second-step annealing conditions chosen were 380–400$^\circ$C at 40 s. A 40 nm Ti layer was chosen because there was found to be a slight diffusion barrier failure for a Ti thickness of 30 nm, as shown in the XTEM and XEDS analysis in Section 6.3. The lowest mean specific contact resistance value of $9 \times 10^{-8}$ Ω-cm$^2$ found for the lightly-doped epilayer with annealing conditions of 200$^\circ$C/30 s and 400$^\circ$C/40 s was significantly lower than previously reported solid-phase regrowth contacts on InGaAs [158].

For SPR contacts made to the heavily-doped epilayer, the specific contact resistances measured in the as-deposited case and after the first-step anneal at 200$^\circ$C/30 s mirrored those of the contacts made to the lightly-doped epilayer. As-deposited contacts were non-ohmic, and contacts measured after the first-step anneal were also on the order of $10^{-4}$ Ω-cm$^2$. However, after annealing of the heavily-doped contacts using the secondary step conditions from 380–400$^\circ$C at 40 s, the minimum specific
Figure 6.1. Specific contact resistance versus second-step annealing times at 380°C at two different diffusion barrier thicknesses.

Figure 6.2. Specific contact resistance versus second-step annealing temperatures at 40 s.
contact resistance measured was $1.8 \times 10^{-8}$ $\Omega$-cm$^2$.

6.2.2 Effect of Pd/Si Ratio

In addition to optimizing the annealing temperatures and times, it was found that changing the thicknesses of the Pd and Si layers within the contact structure was significant for achieving ultra-low specific contact resistances. Previous reports of SPR contacts n-GaAs have studied various combinations of Pd/Ge [130] and Pd/Si [123] layer thicknesses and the effect on specific contact resistance after annealing, but these studies did not report extremely low specific contact resistances.

The layer thicknesses in this thesis were varied in terms of changing the absolute atomic ratio of the total Pd thickness to the Si thickness. This ratio was calculated by determining the total number of atoms per thickness for each element. For example, for an SPR contact with Pd/Si/Pd layers of 30/70/30 nm, the Pd atoms/Si atoms ratio was calculated as $4080/3497 = 1.17$.

The Pd/Si ratio played a great role in achieving low specific contact resistances for SPR contacts to the lightly-doped epilayers. Figure 6.2 shows that for a constant second-step annealing time of 40 s and over a temperature range of 370–400°C, the specific contact resistance of the SPR contact with Pd/Si ratio of 1.36 was significantly higher throughout the entire temperature range compared to an SPR contact with Pd/Si ratio of 1.49. Additionally, the specific contact resistances over a range of Pd/Si ratios are shown for two second-step annealing conditions in Figure 6.3. For both 380°C and 400°C at 40 s, the specific contact resistance decreased with increasing Pd/Si to a minimum value at 1.5, and abruptly increased significantly at ratios greater than 1.5.

This behavior corresponds to that of the Pd/Ge contact by Hao et al. [130], where optimum Pd/Ge layer thickness of similar ratios were found even over different annealing conditions. These optimum ratios were found to be 0.31–0.62 after annealing at 175°C/1 h and 0.44–1.03 after annealing at 340°C/30 min. Their optimum ratio was lower compared to the 1.5 found here, which could be due to different resulting metal-Pd phases (Pd-GaAs versus Pd-InGaAs) formed after the SPR process. Additionally, PdGe is the stable compound formed for the Pd/Ge SPR contact [107, 109], whereas Pd$_2$Si is the stable silicide formed for the Pd/Si SPR contact [159, 160, 161],
over annealing temperatures below 800°C.

The higher specific contact resistances measured for contacts with Pd/Si ratios greater than 1.5 may be due to a lack of excess Si available to dope the InGaAs interface after silicide formation, as would be expected due to the SPR formation process. For Pd/Si ratios less than 1.5, unreacted Si may still be present in the contact stack along with Pd$_2$Si after the two-step annealing. Si is more resistive compared to the Pd$_2$Si phase [162], and the formation of a Schottky barrier between the Si semiconductor and the adjacent metals may contribute to the slightly higher specific contact resistance measured for the lower Pd/Si ratios.

For the SPR contacts made to heavily-doped epilayers, the as-deposited contact also exhibited non-ohmic behavior. On the other hand, specific contact resistances did not vary significantly over different Pd/Si ratios after the optimum second-step annealing parameters, as shown in Figure 6.4. Even including contacts made using un-optimized annealing parameters, the range of specific contact resistance values only varied slightly from $1.8 \times 10^{-8} \pm 1.6 \times 10^{-9}$ to $2.7 \times 10^{-8} \pm 3.2 \times 10^{-9}$ Ω-cm$^2$.

The little variation in specific contact resistance with Pd/Si ratios for the con-
Figure 6.4. Specific contact resistance versus Pd/Si ratio for select SPR contacts to heavily-doped epilayers.

Specific contact resistance to the heavily-doped epilayer may be due to several factors. The high doping concentration present in the epilayer already may be too significant compared to the expected increase in Si doping concentration due to the SPR annealing process or the effect of a Schottky barrier due to the presence of any unreacted Si. Interestingly, a control sample of an as-deposited Pd/Ti/Au contact to the heavily-doped epilayer was measured to have a specific contact resistance within the same range as the SPR contacts formed after annealing. The measured result on the control sample demonstrates that for the heavily-doped epilayer, the SPR annealing process is still required to achieve low specific contact resistance for the Pd/Si/Pd contacts, and can be attributed to the reaction of a significant amount of thick Si. Additionally, it may be inferred that the dramatic decrease in specific contact resistance for the optimized SPR contact with Pd/Si ratio of 1.5 to the lightly-doped epilayer was due to increased Si dopant as a direct result of the SPR annealing process. The introduction of excess Si doping from the SPR contact anneal will be discussed in terms of current transport measurements in Section 6.4.

The nominal ratios of Pd/Si noted here may not accurately reflect the exact amount of available reactants in this particular contact stack. The presence of the Ti
diffusion barrier may result in a lower actual Pd/Si ratio compared to the nominal values because of the reaction of Ti with Pd in a range encompassing the annealing temperatures used [163]. In fact, XTEM images and XEDS in Section 6.3 show Pd reaction with Ti in the as-deposited contacts and after the second-step anneals. Thus, the optimum Pd/Si ratio of 1.5 may be higher than that required for thinner contact stacks or for contact mettallizations without Ti.

6.3 XTEM and XEDS Characterization

In order to further explain the change in the electrical data with respect to the progression of the annealing steps, TEM and EDS was used to study the morphological and chemical changes during each step of the SPR anneal process.

6.3.1 As-deposited Contacts

The XTEM image in Figure 6.5 shows an as-deposited Pd/Si/Pd/Ti/Au contact with nominal deposited thicknesses of 30/70/30/40/90 nm. As-deposited contacts were non-ohmic for both lightly and heavily-doped epilayers, possibly in part due to a thick semiconducting silicon layer that can be seen in the micrograph. Also, it should be noted that both Pd layers have reacted slightly with their adjacent layers of InGaAs, Si and Ti.

![Figure 6.5. Bright field XTEM of as-deposited Pd/Si/Pd contact.](image_url)
6.3.2 First-step Annealed Contacts

Figure 6.6 shows XTEM images of a contact (30/50/30/40/90 nm) annealed at 200°C/30 s. After this first-step anneal, specific contact resistance was still high, on the order of $10^{-4}$ Ω·cm$^2$ even on heavily doped epilayers. This finding is consistent with the expected SPR process, as regrowth does not readily occur at such low temperatures as in the first step anneal. Additionally, the existence of an amorphous Si layer was still present, as confirmed by the SAED pattern (inset in Figure 6.6(a)). As is the expectation after the first-step anneal in the SPR process, Figure 6.6 also confirms the formation of a thick interface layer that has reacted to an approximate depth of 23 nm into the InGaAs. This layer formed due to the low-temperature reaction of Pd and InGaAs, and it is attributed to being the hexagonal Pd$_4$In$_{0.53}$Ga$_{0.47}$As quaternary phase, as identified by Ressel [70]. Additionally, small Kirkendall voids can be observed in the Pd above the reacted quartenary layer in Figure 6.6(b) due to the rapid diffusion of the Pd into the InGaAs at this temperature. The presence of such voids is consistent with those shown in various other SPR contacts [98, 108]. However, the voids found in this Pd/Si/Pd are significantly smaller than those found in Pd/Ge SPR contacts, making Pd/Si/Pd contacts good candidates for contacts with improved thermal stability.

Figure 6.6. XTEM images of Pd/Si/Pd contact after annealing at 200°C/30 s: (a) bright field XTEM showing first-step anneal of contact structure (inset: SAD pattern of silicon (bright) layer) and (b) HAADF STEM image.
6.3.3 Second-step Annealed Contacts

The optimized SPR contacts resulted in minimum specific contact resistances after second-step anneals at 370°C, 380°C, and 400°C at 40 s. The respective XTEM images for contacts at each annealing condition are shown in Figure 6.7, 6.8 and 6.9.

![XTEM image of 370°C second-step anneal](image)

(a) Bright field image

![HAADF STEM image and XEDS line scan](image)

(b) HAADF STEM image and XEDS line scan (arrow indicates direction of XEDS line scan)

**Figure 6.7.** XTEM images of 370°C second-step anneal: (a) bright field and (b) HAADF STEM with XEDS line scan.

Using the contact (30/70/30/40/90 nm) annealed at 380°C/40 s with measured $\rho_c = 1 \times 10^{-7}$ Ω-cm² (Figure 6.8) as a representative XTEM for the second-step anneal, it can be seen in the micrographs that after annealing at this temperature, the thick quaternary phase has decomposed. The formation of Pd$_2$Si in the adjacent contact layer is also confirmed via FFT analysis. The spots in the FFT image were indexed...
and found to be consistent with Pd$_2$Si as seen along the [011] zone axis. The lattice constants were calculated to be $a \approx 6.55 \, \text{Å}$ and $c \approx 3.42 \, \text{Å}$, which match closely to those calculated by Pearson [164] ($a \approx 6.49 \, \text{Å}$ and $c \approx 3.43 \, \text{Å}$) and in Pd/Si SPR contacts analyzed by SAED [122]. The indexed FFT image of the adjacent InGaAs epilayer from the same micrograph revealed a [011] InGaAs zone axis with lattice parameter of $a \approx 5.78 \, \text{Å}$ (compared with $a \approx 5.87 \, \text{Å}$ [165]). The resultant Pd$_2$Si layer also looks quite dense; SPR contacts of Pd/Ge are prone to large voids at the semiconductor/PdGe interface due to electrochemical leaching of the Ge during processing [128] or oxidation of Ge during subsequent device processing [110]. The HAADF STEM image from Figure 6.8(b) at the metal-semiconductor gap edge makes it clear to see that the Pd$_2$Si protrudes shallowly into the final epilayer, only up to 7 nm, with no observable lateral reaction occurring. This feature makes the Pd/Si/Pd SPR contact a good candidate for contacts in very densely packed, thin body devices.

Additional XTEM images for the second-step anneals at 370°C (Figure 6.7) and 400°C (Figure 6.9) substantiate the final step of the SPR process and the formation of low-resistance ohmic contacts. XTEM from all three second-step anneal temperatures indicate the formation of a thick but shallowly penetrating Pd$_2$Si layer adjacent to the InGaAs interface and a regrown region of InGaAs approximately 5–15 nm thick directly beneath the layer. Additionally, the thick amorphous Si layer is no longer present and instead there is a crystalline Si-rich-Pd layer. The quaternary phase has reacted with the excess Si to form the doped, regrown InGaAs region.

XEDS data was taken for the second-step annealed contacts, as shown in Figure 6.7(b). The composition of the regrown region did not vary significantly with that of the epilayer. The regrown region is also expected to correspond closely to the approximate thickness of the reacted quaternary phase from the intermediate annealing step [122], but the XTEM shows that the regrown InGaAs thickness is slightly thinner, possibly due to shorter annealing times than in previous studies. Prior to the use of the optimized layer thicknesses, XEDS data was taken for a 30/70/30/30/90 nm contact annealed at 380°C/40 s, as shown in Figure 6.10. There is an increase in In concentration within the Au layer, which led to the use of a 40 nm Ti diffusion barrier. The XEDS line scan for this contact differed slightly from that of the one for the optimized sample from Figure 6.7(b) in that there is a very high Si signal
Figure 6.8. (a) Bright field XTEM and (b) HAADF STEM images after 380°C second-step anneal showing that the silicide remaining only reacts approximately 5-7 nm into the semiconductor epilayer at some points (dashed line shows original interface); (c) Pd$_2$Si/InGaAs interface with corresponding FFT images.
throughout the scan; however, this may be due to a higher interference of emission signal from the W and Ta protective layers or from the Si in the EDS detector due to the lower number of counts in this scan.

The changes in the XTEM images from the as-deposited contact to the first-step and second-step anneals corroborate the regrowth mechanism and the subsequent decrease in contact resistance. The lowest ohmic contact resistance was found for the second-step anneal at 400°C. Figure 6.9 shows that this contact seemed to have the most interfacial roughness compared with the lower second-step anneal temperatures. The increased roughness may in fact be contributing to the slightly lower contact resistance because of an increase in active surface area.[84]
6.4 Current Transport and Field-Emission Modeling

Following the discussion of the Pd/Si ratio in Section 6.2.2, the presence of excess Si dopant in the regrown InGaAs was determined by I-V-T measurements and field-emission modeling. I-V-T measurements made on a lightly-doped contact with a Pd/Si ratio of 1.5 annealed at 200°C/30 s and 380°C/40 s from 77–300 K resulted in a constant specific contact resistance averaging $1.1 \times 10^{-7}$ Ω-cm$^2$, which did not change significantly with temperature, indicating current transport by field emission.

Degenerately doped n-In$_{0.53}$Ga$_{0.47}$As was assumed, with the effective mass extrapolated based on a linear fit as in Section 4.5. Theoretical specific contact resistance values were then calculated, taking into account image force lowering, over a range of Schottky barrier heights (SBH) ($\phi_b = 0.2–0.4$ eV) and total donor concentrations ($N_D = 4 \times 10^{18}–3 \times 10^{19}$ cm$^{-3}$) over the same range of temperatures at which the experimental values were measured. For a given SBH, the experimentally measured specific contact resistance values were matched with the donor concentrations required to obtain this value. The plots generated for various SBHs are shown in Figure 6.11, and the measured specific contact resistances over the temperature range are plotted on each to show how they compare to the calculated values.

The required $N_D$ concentrations were then plotted versus a range of SBHs in
Figure 6.11. Specific contact resistances plotted over a range of temperatures and dopant concentrations for specific SBHs. Measured $\rho_c = 1.1 \times 10^{-7} \Omega\text{-cm}^2$ for lightly-doped SPR contact with ratio 1.5 and annealed at 200°C for 30 s and 380°C for 40 s is also plotted.
Figure 6.12(a) and 6.12(b) for two select heavily-doped and lightly-doped samples with average measured specific contact resistances of $1.8 \times 10^{-8}$ Ω-cm$^2$ and $1.1 \times 10^{-7}$ Ω-cm$^2$, respectively. As the SBH is increased, the $N_D$ needed to obtain each specific contact resistance value ranges from $2.6 \times 10^{19} - 1.9 \times 10^{20}$ cm$^{-3}$ and $6.5 \times 10^{18} - 5.0 \times 10^{19}$ cm$^{-3}$.

Given the original carrier concentration of $3.0 \times 10^{19}$ cm$^{-3}$ in the heavily-doped epilayer, the SBH is then extracted to be 0.24 eV in Figure 6.12(a). This extracted value closely agrees with the conventional SBH value of 0.2 eV for n-InGaAs [137, 156, 138] and the pinned value extracted in Chapter 4. Using the extracted barrier height of 0.24 eV, the required $N_D$ needed to achieve the measured specific contact resistance value for the lightly-doped case mentioned above can thus be extracted to be $1.0 \times 10^{19}$ cm$^{-3}$ in Figure 6.12(b). Recalling the original carrier concentration of $1 \times 10^{17}$ cm$^{-3}$ in the lightly-doped epilayer, the extracted value is two orders of magnitude higher. This extracted value represents the total donor concentration present in the lightly-doped InGaAs at the contact interface after the final annealing step.

Given that the final donor concentration of the lightly doped samples was extracted to be $1.0 \times 10^{19}$ Ω-cm$^{-3}$, this value was less than the donor concentration present in the heavily doped sample. This comparison combined with the lack of reduction in the specific contact resistance in the heavily doped SPR sample versus its control indicates that the insensitivity of the Pd/Si ratio in heavily doped samples was due to the lack of additional dopant incorporation.

### 6.5 Pd/Si/Pd Contacts to p-InGaAs

An SPR contact to a heavily-doped p-type InGaAs epilayer was fabricated in a similar manner as with the n-type samples. The Pd/Si/Pd/Ti/Au layers in this case had layer thicknesses of 15/27.5/15/40/90 nm. These thicknesses were chosen with the optimized Pd/Si ratio of 1.5 in mind. The Pd/Si/Pd thicknesses were half as thick as those discussed for the heavily-doped n-type contacts discussed in previous sections, but these same thicknesses were also demonstrated to give optimized specific contact resistance values for those contacts as well, as shown in Figure 6.4. Additionally, the
Figure 6.12. Required doping density vs. SBH at T=300 K to obtain the average measured (a) $\rho_c = 1.8 \times 10^{-8}$ $\Omega$-cm$^2$ for the heavily-doped SPR contact and (b) $\rho_c = 1.1 \times 10^{-7}$ $\Omega$-cm$^2$ for the lightly-doped SPR contact. For $N_D = 3.0 \times 10^{19}$ cm$^{-3}$, the $\phi_b = 0.24$ eV. Using $\phi_b = 0.24$ eV, the doping density required to obtain measured $\rho_c = 1.1 \times 10^{-7}$ $\Omega$-cm$^2$ is $1.0 \times 10^{19}$ $\Omega$-cm$^{-3}$. 
use of smaller thicknesses is advantageous for the desire to contact smaller dimension devices.

The purpose of creating the same Pd/Si/Pd SPR contact to p-type InGaAs was to confirm the additional doping due to the SPR anneal. The specific contact resistance of the p-type contact is expected to increase after the SPR process due to the addition of the n-type dopant, Si, which would possibly result in the compensation of acceptors.

### 6.5.1 Specific Contact Resistance Results

As-deposited contacts were ohmic with $\rho_c = (6.3 \pm 0.8) \times 10^{-7} \ \Omega\text{-cm}^2$. This result differs than that of the as-deposited contacts to the n-type epilayer, in that those contacts displayed non-linear I-V behavior. However, the p-InGaAs epilayers are much more heavily doped than those of the n-InGaAs, which may allow the as-deposited contacts to display ohmic behavior.

After the first-step anneal at 200°C/30 s, the specific contact resistance did not change significantly, with measured $\rho_c = (4.1 \pm 2.7) \times 10^{-7} \ \Omega\text{-cm}^2$. After a two-step anneal with the second step at 380°C/40 s, the specific contact resistance decreased to $\rho_c = (4.4 \pm 0.2) \times 10^{-8} \ \Omega\text{-cm}^2$. The decrease in the specific contact resistance after annealing is displayed in Figure 6.13.

![Figure 6.13](image)

**Figure 6.13.** Trend of specific contact resistances throughout annealing process for optimized Pd/Si/Pd SPR contact to p-InGaAs with Pd/Si ratio = 1.5.
6.5.2 Comparison to Contacts to n-InGaAs

Interestingly, because the SPR mechanism was designed to contact n-type material, the trend in specific contact resistance after annealing is not in line with the expected behavior as a result of utilizing the Pd/Si/Pd SPR contact for p-type InGaAs. In fact, Pd/Ge SPR contacts to heavily-doped p-InGaAs and p-GaAs have been demonstrated to have low specific contact resistances as well. Chen et al. [166] used a p-InGaAs epilayer with \( N_A = 1.8 \times 10^{19} \text{ cm}^{-3} \); the contact became ohmic only after annealing at 325°C, and the lowest specific contact resistance was \( 2.3 \times 10^{-6} \Omega\text{-cm}^2 \). Chen et al. [167] used a p-InGaAs epilayer with \( N_A = 2.0 \times 10^{19} \text{ cm}^{-3} \); this contact became ohmic only after annealing over 300°C, and the specific contact resistance was on the order of \( 3 \times 10^{-6} \Omega\text{-cm}^2 \). Han et al. [168] fabricated Pd/Ge SPR contacts to p-GaAs, with \( N_A = 5 \times 10^{19} \text{ cm}^{-3} \), which were ohmic as-deposited, and had a specific contact resistance of \( 6.4 \times 10^{-7} \Omega\text{-cm}^2 \) after annealing at 450°C.

It seems that the introduction of the Si dopant in the Pd/Si/Pd SPR contact may not be large enough to compensate for the extremely high acceptor concentration. Interestingly, Chen et al. [167] showed that for Pd/Ge SPR contacts made to p-InGaAs with \( N_A = 2.9-5.2 \times 10^{18} \text{ cm}^{-3} \), the contacts were non-ohmic at all annealing temperatures, while Ressel et al. [70] made Pd/Ge SPR contacts to p-InGaAs with \( N_A = 7 \times 10^{18} \text{ cm}^{-3} \) that were measured to be \( 1-2 \times 10^{-4} \Omega\text{-cm}^2 \) at annealing greater than 350°C. The decrease in values after the second-step anneal could also be due to the formation of the lower-resistance Pd\(_2\)Si phase and the more complete reaction of the original amorphous Si phase, as predicted by the use of a Pd/Si ratio of 1.5. Another explanation for the unexpected decrease in specific contact resistance could be the formation of a heavily-doped p-n junction due to the introduction of n\(^+\)-Si into the regrown InGaAs region due to the annealing process, thus introducing a tunneling junction [167]. SPR contacts fabricated to less heavily-doped p-InGaAs epilayers may be necessary in order to more clearly determine the effect of the SPR annealing for p-type material.
6.6 Conclusions

The measured specific contact resistance values for the Pd/Si/Pd SPR contacts to n-InGaAs were the lowest achieved considering the original doping of the semiconductor epilayers. The optimization of the Pd/Si atomic ratio played an integral role in achieving these values, along with the implementation of a two-step rapid thermal annealing process. The two-step anneal helps to promote the required reactions necessary for SPR to occur, which include the low activation energy process to form the Pd-InGaAs quaternary phase (0.35 eV [154]), and then the higher activation energy process to form the Pd$_2$Si phase (0.9 eV [169]). The calculation of excess Si dopant introduced due to our Pd/Si/Pd contact compares favorably with previous work of Pd/Ge on n-GaAs, which showed the introduction of $2.0 \times 10^{19}$ Ω-cm$^2$ of Ge [109, 112].
Chapter 7

Summary and Future Work

7.1 Summary

The continued development of scaled transistors based on compound semiconductors such as InGaAs has driven the interest in the methods and science of forming ultra-low resistance ohmic contacts. In this thesis, three types of ohmic contacts to In$_{0.53}$Ga$_{0.47}$As were fabricated and studied. The electrical performance and behavior of these contacts were studied in the context of how the physical and chemical characteristics, directly at and adjacent to the metal/semiconductor interface, affect the current transport. Engineering of the interface through surface topography and introduction of excess doping by solid-state reactions was employed as alternative methods to lower specific contact resistance.

Non-alloyed Pd-, Pt- and Mo-based planar contacts to heavily doped n-InGaAs ($N_D = 3 \times 10^{19} \text{ cm}^{-3}$) with a standardized surface preparation (UV-ozone/BOE) were studied in order to examine metal-dependent phenomena affecting current transport. These contacts were also compared to those similarly fabricated elsewhere on p-InGaAs ($N_A = \text{high } 10^{19} \text{ cm}^{-3}$). The electrical behavior differed depending on the resulting interfacial reactions or lack thereof. Pd-based contacts resulted in the lowest specific contact resistances in both cases ($(3.2 \pm 0.3) \times 10^{-8} \ \Omega\text{-cm}^2$ for n-type and $(1.9 \pm 0.5) \times 10^{-8} \ \Omega\text{-cm}^2$ for p-type), while Mo-based contacts were over an order of magnitude higher ($(2.7 \pm 0.6) \times 10^{-7} \ \Omega\text{-cm}^2$ and $(1.2 \pm 0.5) \times 10^{-5} \ \Omega\text{-cm}^2$). The higher reactivities of Pt and Pd with InGaAs resulted in consistently lower specific
contact resistances due to the dispersion of any interfacial oxides leftover from the ex-situ surface preparation. Barrier heights for the different metal contacts were extracted after fitting theoretical specific contact resistance values with measured values from I-V-T measurements of Pd- and Mo-based contacts to lightly-doped n-InGaAs. A pinned barrier height of 0.24 eV was extracted for these contacts, which closely matched those of Pd contacts to heavily-doped n-InGaAs, and Mo contacts with very stringent surface preparation methods, indicating that the surface treatment was a significant factor affecting contact resistance for metals contacted to heavily-doped epilayers. The morphological and electrical stability of the contacts after annealing at 350°C/1 h was also studied to determine their usefulness under high temperature processing conditions. All contact metallizations showed no significant lateral diffusion and shallow reaction depths. The measured specific contact resistances of the annealed Pd and Pt-based contacts were corrected according to observed reaction depths from the TEM images by taking into account increased sheet resistance under the contact. There was an improvement in specific contact resistance for the Mo-based contacts, while there was over a 60% change for the Pt and Pd based contacts to p-type InGaAs. The low contact resistances and good thermal stability of the Pd-based contacts to heavily-doped InGaAs were attributed to the unique interaction of Pd with InGaAs, leading to the dispersal of an interfacial oxide and the formation of a stable Pd$_x$InGaAs phase.

Because of the difficulty in forming low resistance, shallow ohmic contacts without complex surface cleaning procedures ex situ to InGaAs that is not otherwise very heavily doped, methods of metal/semiconductor interface engineering were explored to lower specific contact resistance. The first method was an attempt to fabricate enhanced topography at the semiconductor surface before contact metallization. Features with dimensions on the order of the depletion width spaced sufficiently apart have been predicted to increase the electric field at the interface and the active surface area of the ohmic contact. Refractory TiB$_2$ thin film masks were fabricated on lightly-doped n-InGaAs using electron beam GLAD. By modifying the thin film deposition process parameters, films of varying intercolumnar spacing and thickness could be deposited. Selective wet etching and RIE of the InGaAs was used to roughen the surface, which was characterized by AFM. The lateral dimensions of the surface features was
quantified by PSD evaluations. Ohmic contacts of Ti/Pt/Au were fabricated on the modified surfaces and correlated with the InGaAs roughness and lateral dimensions. Specific contact resistance was reduced up to 85% when RIE was used to modify the InGaAs surface and features with dimensions 30–50 nm wide and 2–3 nm deep were obtained. Even though the ability to form deeper features based on calibrated etch rates was limited by the GLAD process, the initial epilayer smoothness and the film/substrate etch selectivity, the multi-step GLAD etching process produced InGaAs surfaces that had RMS roughnesses 2 times higher and lateral dimensions almost 2 times larger (depending on GLAD and etching parameters) compared with surfaces etched without the GLAD etch mask. This multi-step etch method using a GLAD film shows potential as a method for introducing controlled nanomorphology at a substrate surface but would need to be further optimized, especially for incorporation in small area dimensions.

Another method of engineering the metal/semiconductor interface was explored by introducing a heavily-doped, regrown InGaAs layer containing Si, at the metal/n-InGaAs interface. Pd/Si/Pd/Ti/Au contacts to lightly-doped n-InGaAs were formed via a two-step annealing process, where a solid-phase regrowth process took place. In the SPR process, a series of thermodynamically driven solid-state reactions occur below the melting points of the layers. The metals, thicknesses and annealing temperatures were optimized so that the lowest specific contact resistance of $9 \times 10^{-8} \, \Omega \cdot \text{cm}^2$ was achieved for Pd/Si SPR contacts to n-InGaAs of $N_D = 1 \times 10^{17} \, \text{cm}^{-3}$. TEM analysis was integral for confirming the morphology in each step of the SPR process and correlating it with the specific contact resistances. I-V-T measurements and Schottky barrier height modeling was used to show that an excess Si doping of $1.0 \times 10^{19} \, \text{cm}^{-3}$ was introduced at the interface as a result of the optimized two-step SPR process. The resulting contacts were also confirmed to be shallow with no lateral diffusion, making them good candidates for integration into devices requiring small dimensions and shallow junctions.

This thesis explored factors affecting current transport in shallow, ohmic contacts to n-InGaAs. The limitations in decreasing contact resistance due to a pinned Fermi level and for ex situ contacts to lightly-doped InGaAs led to efforts to modify the metal/n-InGaAs interface: by developing a nanopatterning method to change the to-
pography, and by introducing excess doping through an optimized SPR process, which resulted in the lowest resistance ohmic contacts to lightly-doped $\text{n-In}_{0.53}\text{Ga}_{0.47}\text{As}$ epi-layers. Advanced characterization techniques, especially TEM, and modeling of specific contact resistances and barrier heights were integral to better understanding the interfacial reactions and current transport in contacts to InGaAs.

### 7.2 Future Work

The electrical and morphological behavior of the contacts studied in this thesis reveals several areas of further work regarding the improvement of low-resistance Ohmic contacts to InGaAs. It is essential to understand the metal-dependent phenomena that was observed for the planar contacts to heavily-doped InGaAs and the significance of the surface cleaning when the dominant mechanism of current transport is FE because it can inform the selection of contact metals, layer thicknesses and surface processing conditions. The case of the Pd-based contact is especially interesting because of its good morphological and electrical stability and low specific contact resistance to both n- and p-InGaAs. In order to determine the presence of defects caused by Pd diffusion into the bulk below the Pd/InGaAs interface, I-V-T measurements of the as-deposited and annealed Pd and Pt contacts to heavily-doped n and p-InGaAs can be performed and compared. The presence of defect-assisted tunneling may reveal different temperature dependancies of the specific contact resistances depending on the energy of the defect state [58]. Recently, very high resolution structural characterization techniques such as aberration-corrected TEM (ac-TEM) [170, 171] and atom probe tomography [172] have been developed. These techniques can be used to directly probe the presence of defects in the semiconductor near the contact interface. The use of different deposition techniques such as sputtering should also be considered, as it was shown that sputtered contacts resulted in slightly lower specific contact resistances, possibly due to the introduction of subsurface defects [49].

The nanopatterning technique developed in this thesis is limited by the substrate roughness as well as the etch selectivity of the metal thin film with the substrate. Other methods such as self assembled monolayers [173, 174], block copolymers [174, 175, 176] and nanosphere lithography [173, 174, 177, 178] have already
been explored as means of patterning sub-50 nm dimensions. The GLAD method could be used in conjunction with these methods to deposit thin films on a prepatterned substrate in order to further decrease pattern sizes by taking advantage of the physical shadowing mechanism. Another means of patterning could be to spin-on metal nanoparticle solutions. Nanoparticle suspensions of Pd, a metal which was explored in this thesis and found to form low-resistance ohmic contacts with InGaAs, are readily available and relatively non-toxic [179, 180, 181]. The organic solutions containing the nanoparticles could then be selectively removed to leave behind the metal nanoparticles.

The contacts formed by SPR to n-InGaAs in this thesis had a very low specific contact resistance, but values on the order of $10^{-9} \ \Omega \cdot \text{cm}^2$ and below may be required for future generations of devices. A continuation of the SPR study on p-InGaAs is desirable in order to better understand the mechanism, and to see if it may be applied for contacts to lightly-doped p-type InGaAs by replacing Si with acceptor dopants such as Zn. Pd/Zn contacts have already been explored on p-InGaAs [136], but their acceptor concentrations were still high with $2 \times 10^{19} \ \text{cm}^{-3}$ and their specific contact resistances were still much higher than the values obtained on p$^+$-InGaAs using Pd/Si/Pd SPR contacts. A doping concentration on the order of $1.4 \times 10^{19} \ \text{cm}^{-3}$ was introduced into the SPR contact to n-InGaAs, but other methods of introducing and activating dopants should be explored, such as plasma doping (PD) [182] and laser annealing [183].

Due to issues with short channel effects and electrostatic control for scaled devices, there is currently a major thrust towards the development of devices with non-planar gate geometries, thus requiring very stringent requirements for the ohmic contact [184]. Fermi-level unpinning is another method that is currently being explored as a means to lower specific contact resistance. Recently, interfacial oxide layers have been investigated for insertion at the metal/n-Si, n-Ge, n-GaAs and n-InGaAs interfaces to form M-I-S contacts in order to modify the effective barrier heights and shift Fermi-level pinning [22, 23, 24]. The “self-cleaning” effect of the atomic layer deposition (ALD) of Al and Hf-oxides (for use as gate dielectric barriers) is interesting in that it removes surface oxides in GaAs and results in Fermi-level unpinning of the interfaces [185]. The same phenomena could be applied for ALD of contact metals such as Pd.
[186, 187], provided the proper precursors are used [185, 188]. ALD is also a useful deposition technique to consider for non-planar geometries because of its conformal nature. In the same vein, different crystallographic facets of the semiconductor should also be taken into account when designing future contact schemes. The Fermi-level unpinning behavior was found to be more desirable on GaAs (111) compared with GaAs (100) with ALD of Al$_2$O$_3$ due to differing bonding structure [184, 189]; this suggests that a better understanding of metal-InGaAs interactions with respect to different faces is needed also.
Appendix A

I-V-T Equations

A.1 Specific Contact Resistance as a Function of Temperature

The specific contact resistance equations as a function of temperature [190] are derived from the typical current density equations describing current transport across a rectifying metal-semiconductor barrier [29]:

\[ J = A^* T^2 \exp \left( -\frac{q\phi_b}{kT} \right) \left[ \exp \left( \frac{qV}{nkT} \right) \right] \]  

(A.1)

for \( V \geq \frac{3kT}{q} \), where \( A^* = \frac{4\pi q m^* k^2}{h^3} \) (Richardson’s constant), \( k = \) Boltzmann’s constant, \( q = \) elementary electron charge and \( m^* = m_e m_0 = \) effective mass (where \( m_e = \) electron effective mass and \( m_0 = \) mass of a free electron). The specific contact resistance is then defined by:

\[ \rho_c = \left( \frac{\partial V}{\partial J} \right)_{V=0} \]  

(A.2)

The specific contact resistance varies as a function of doping concentration, temperature and barrier height and as such different current transport mechanisms may be dominant. The tunneling parameter [29] can be used to determine the range of doping and temperature where each current transport mechanism is valid, and is
expressed below:

\[ E_{00} = \frac{hq}{4\pi} \left( \frac{N_D}{m^*\varepsilon_s} \right)^{1/2} \]  (A.3)

where \( h \) = Planck’s constant, \( N_D \) = total donor concentration and \( \varepsilon_s \) = permittivity of semiconductor.

For thermionic emission \( (E_{00} \ll kT) \), following Equation A.1:

\[ \rho_c = \frac{k}{qA^*T} \exp(q\phi_b/kT) \]  (A.4)

For thermionic-field emission \( (E_{00} \approx kT) \):

\[ J = J_{0TF} \exp(qV/E_0) \]  (A.5)

\[ J_{0TF} = \frac{A^*T}{k} \sqrt{\pi E_{00} q(\phi_b - V - \xi)} \frac{\exp \left( -\frac{q\xi}{kT} - \frac{q}{E_0} (\phi_b - \xi) \right)}{\cosh \left( \frac{E_{00}}{kT} \right)} \]  (A.6)

\[ E_0 = E_{00} \coth(E_{00}/kT) \]  (A.7)

\[ \rho_c = \frac{k^2 \cosh(E_{00}/kT)}{qA^* \pi (q\phi_b + q\xi) E_{00}} \left[ \coth(E_{00}/kT) \right]^{1/2} \exp \left( \frac{q(\phi_b - \xi)}{E_0} + \frac{q\xi}{kT} \right) \]  (A.8)

where \( \xi = E_C - E_F \).

For field emission \( (E_{00} \gg kT) \):

\[ J = J_{0F} \exp \left( qV/E_{00} \right) \]  (A.9)

\[ J_{0F} = \frac{\pi A^*T}{kC_1 \sin(\pi kTC_1)} \exp(-q\phi_b/E_{00}) \]  (A.10)

\[ C_1 = (2E_{00})^{-1} \ln[-4(\phi_b - V)/\xi] \]  (A.11)
\[ \rho_c = \left( \frac{A^* T \pi q}{k \sin(\pi C_1 k T)} \exp\left(-q \phi_b / E_{00}\right) - \frac{A^* q}{C_1 k^2} \exp\left(\left(-q \phi_b / E_{00}\right) + C_1 q \xi\right) \right)^{-1} \] (A.12)

### A.2 Current Transport Modeling

To calculate theoretical \( \rho_c \) values according to \( N_D, \phi_b \) and \( T \), the following considerations were taken. The electron concentration at thermal equilibrium is given by the density of states and the Fermi-Dirac integral [15]:

\[ n = \frac{2}{\sqrt{\pi}} N_c F_{1/2}(\eta_F) = \frac{2}{\sqrt{\pi}} N_c \int_0^\infty \left( \frac{\eta^{1/2}}{1 + \exp^{-\eta}} \right) d\eta \] (A.13)

where \( \eta = (E - E_C)/kT \), \( \eta_F = (E_F - E_C)/kT \) and \( N_c \) is the density of states:

\[ N_c = 2 \left( \frac{2 \pi m^* k T}{\hbar^2} \right)^{3/2} \] (A.14)

In order to calculate the theoretical specific contact resistances for n-InGaAs using Equation A.8 or A.12, the temperature dependence of the \( \xi = E_C - E_F \) term must be accounted for. The difference between the conduction band and Fermi level changes because the Fermi level position varies as a function of temperature and concentration of ionized dopants. The carrier concentration of the n-InGaAs epilayer is taken to be \( n \). For \( n \) at a range of \( T \), \( \xi \) was calculated by Equation A.13. Specifically, \( \eta_F \) values were inputted to evaluate the Fermi-Dirac integral of the 1/2 order (as defined by Blakemore [191]) and implemented using a MATLAB function [192].

For \( \xi < 3kT \), a degenerately-doped semiconductor was assumed. Otherwise, the following procedure was used to calculate the total donor concentration, \( N_D \). The ionized donor concentration, \( N_D^+ \) was then calculated at \( T=300 \) K by relating \( N_D^+ \) to \( n \) by the charge neutrality equation:

\[ n + N_A^- = p + N_D^+ \] (A.15)

where \( n \) and \( p \) are the concentrations of electrons and holes, and \( N_A^- \) and \( N_D^+ \) are the ionized impurity concentrations of acceptors and donors. In the case of n-type
doping, and with \( N_D^+ >> p \) and no compensation, the equation simplifies to:

\[
n \sim p + N_D^+ \approx N_D^+ \quad \text{(A.16)}
\]

thus, the electron concentration is equated to the ionized donor concentration. The ionized donor concentration is related to the total donor concentration by:

\[
N_D^+ = \frac{N_D}{1 + g_D \exp \left( \frac{E_F - E_D}{kT} \right)} \quad \text{(A.17)}
\]

where for n-type doping, \( g_D = 2 \), which is the ground state degeneracy of the donor impurity level [15]. Using the ionization energy, \( E_C - E_D = 0.005 \text{ eV} \), for Si-doped n-In_{0.53}Ga_{0.47}As [148], \( E_F - E_D \) can be determined from the previously calculated \( \xi \) value.

In the degenerately doped case, the following assumption may be applied:

\[
N_D^+ \approx N_D \quad \text{(A.18)}
\]

because as the as \( E_F \) rises close to \( E_D \), the impurity level broadens into an impurity band that merges with the conduction band. Thus, complete ionization of donors may be assumed [193].

\( N_D \) was then used to calculate \( E_{00} \) and subsequently solve the \( \rho_e \) equations as a function of barrier height and temperature.

### A.3 Schottky Barrier Lowering

The effect of image force lowering of the Schottky barrier was also considered when calculating specific contact resistances by applying the model by Sze [15]. The maximum electric field at the metal surface is expressed as

\[
E_m = \sqrt{\frac{2qN_D|\Psi_s|}{\varepsilon_s}} \quad \text{(A.19)}
\]
where $\Psi_s$ is the surface potential and is expressed as

$$|\Psi_s| = \phi_{bn0} - \xi + V_R$$  \hspace{1cm} (A.20)

where $\phi_{bn0}$ is the intrinsic barrier height and $V_R$ is the reverse bias. The change in barrier height due to the image force lowering is expressed as

$$\Delta \phi = \sqrt{\frac{qE_m}{4\pi\varepsilon_s}}$$  \hspace{1cm} (A.21)

and the resulting barrier height at zero bias and thermal equilibrium is then calculated to be

$$\phi_{bn} = \phi_{bn0} - \Delta \phi$$  \hspace{1cm} (A.22)

For the current modeling, the resulting $\phi_{bn}$ was then used to calculate specific contact resistances with respect to intrinsic barrier heights.
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157


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