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ARSENIDE-ANTIMONIDE HETERO-JUNCTION TUNNEL TRANSISTORS FOR LOW POWER LOGIC APPLICATIONS

A Dissertation in

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ABSTRACT

Aggressive supply voltage (V_{CC}) scaling of future transistors without increasing the off-state leakage while maintaining performance remains an important challenge. Hetero-junction Tunnel FETs (HTFETs) with steep switching slope and high drive current at low supply voltage (below 0.35V) have emerged as promising low V_{CC} device option. $GaAs_{1-y}Sb_y$ source and $In_xGa_{1-x}As$ channel form lattice matched arsenide-antimonide staggered hetero-junctions with compositionally tunable effective tunnel barrier height. Unlike homo-junction Tunnel FETs, the effective barrier height of staggered hetero-junctions can be made negligibly small while maintaining large band-gaps in the respective source, channel and drain regions, thus, enabling TFETs to achieve MOSFET like drive currents while maintaining higher on-off ratio.

This dissertation focuses on experimental demonstration of mixed arsenide-antimonide hetero-junction TFETs with nano-pillar tunnel transistor architecture exhibiting MOSFET-like on-current and high on-off ratio for ultra-low power logic applications. Within this dissertation, using experimental demonstration and detailed modeling, following aspects of the n-channel hetero-junction Tunnel FETs will be discussed: a) Material selection and device design; b) Nano-pillar TFET process flow development; c) Hetero-junction TFET growth and materials characterization; and d) Hetero-junction TFET transport study. The dissertation concludes with benchmarking of the performance of arsenide-antimonide n-channel Tunnel FETs with those reported till date, and an address to the feasibility of arsenide-antimonide based complementary Tunnel FET logic for future ultra low power logic applications.

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Chapter 1

Tunnel FET Design for Low Power Applications

1-1 Introduction to Tunnel FETs

Continued miniaturization of the silicon CMOS transistor technology has resulted in an unprecedented increase in single-core and multi-core performance of modern-day microprocessors. However, the exponentially rising transistor count (Figure 1-1) has also increased the overall power consumption, making performance per watt of energy consumption the key figure-of-merit for today's high performance microprocessors [8]. Today, energy efficiency serves as the central tenet of high performance microprocessor technology at the system architecture level as well as the transistor level ushering in the era of energy efficient nano-electronics. Aggressive supply voltage scaling while maintaining the transistor performance is a direct approach towards reducing the energy consumption since it reduces the dynamic power quadratically and the leakage power linearly as shown in equation 1-1[9].

$$P_{total} = P_{active} + P_{passive}$$

$$= \alpha C_{eff} V_{CC}^{\ 2} f + I_{leak} V_{CC} \quad (1\text{-}1)$$

where α represents activity factor, C_{eff} is the system capacitance, f represents clock frequency, V_{CC} represents CMOS supply voltage and I_{leak} is the system leakage current.

However, due to the thermal limit of kT/q on the sub-threshold swing in MOSFETs, the threshold voltage and hence the supply voltage scaling has essentially stopped around V_{CC}=1V (Fig. 1-1 (c)). In order to maintain the on-state performance (Eq. 1-2), aggressive scaling of V_{CC} for quadratic reduction in active power consumption requires aggressive scaling of threshold

voltage (V_{th}). However, for a fixed value of the sub-threshold slope (SS), reduction in V_{th} results in exponential increase in the I_{OFF} (Eq. 1-3).

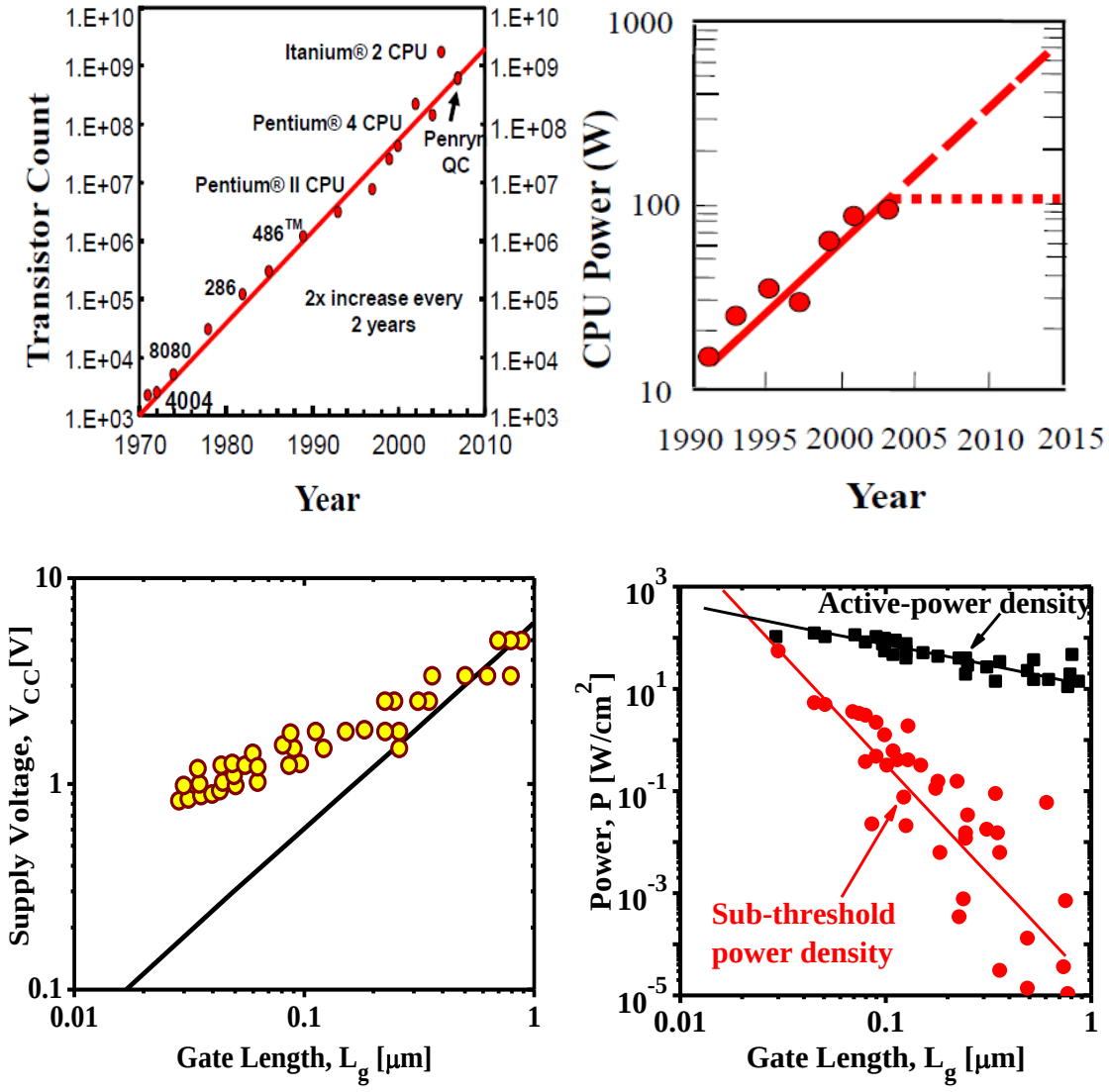

Figure 1-1. (a) 2x increase in the transistor count every 2 years following the well known Moore's law. (b) CPU power consumption already reached 100W around 2005. Aggressive supply voltage (V_{CC}) scaling is required to keep the power consumption within limits while continuing to pack in more and more transistors [8]. (c) VCC scaling stopped around 1V due to lack of threshold voltage scaling. (d) Reduction of threshold voltage scaling over the years has resulted in exponential increase in CMOS off-state leakage and hence sub-threshold power density. Any further reduction in threshold voltage will make uncontrolled increase in static power consumption dominating the total power consumption of the chip [9].

$$I_{on} = wC_{inv}V_{inj}(V_{CC} - V_{th}) \quad (1\text{-}2)$$

$$I_{off} = wI_o 10^{\frac{-Vth}{SS}} \quad (1\text{-}3)$$

where w is related to the device dimensions, C_{inv} is the inversion capacitance, V_{inj} is the source injection velocity, I_o is the targeted off-state current, V_{th} is the threshold voltage and SS is the sub-threshold slope. Due to the scaling of the V_{th} over the past few decades, the sub-threshold power density has increased exponentially and now it is comparable to the active power density as shown in Figure 1-1(d) [9]. Any further reduction in V_{th} without changing the underlying fundamental limit on the SS of the CMOS devices will worsen this situation by resulting in uncontrolled increase in the sub-threshold and the static power density. Thus, emerging switches beyond CMOS are being actively explored which posses switching characteristics that is much steeper than the thermal limit of kT/q in MOS transistors, which can scale the threshold voltage and hence supply voltage significantly while simultaneously achieving MOSFET-like on current on-off ratio at reduced supply voltage [10-13].

Inter-band tunnel field effect transistors (TFETs) with a gate modulated Zener tunnel junction at the source have recently attracted a great deal of interest due to their steep switching property [12-36]. Figure 1-2(a) shows a representative curve of an n-channel TFET I_{DS}-V_{GS} curve compared with that of a similar dimension n-channel MOSFET. TFETs differ from MOSFETs mainly in the way majority carriers get injected into the channel. In MOSFETs, the carrier injection is dependent on the gate modulated source to channel barrier, while in TFETs, carriers get injected into channel through inter-band tunneling from the source. Figure 1-2(b) shows the on-state band-diagram and the difference between n-channel MOSFET and TFET operation. The n-channel TFET operates on the principle of band to band tunneling (BTBT) of electrons across the source to channel tunnel junction under the influence of a gate electric field. The major advantage of the TFETs in comparison with the metal-oxide-semiconductor field-effect

transistors (MOSFETs) is that the reverse biased tunnel junction in the former eliminates the high energy tail present in the Fermi-Dirac distribution of the valence band electrons in the p+ source

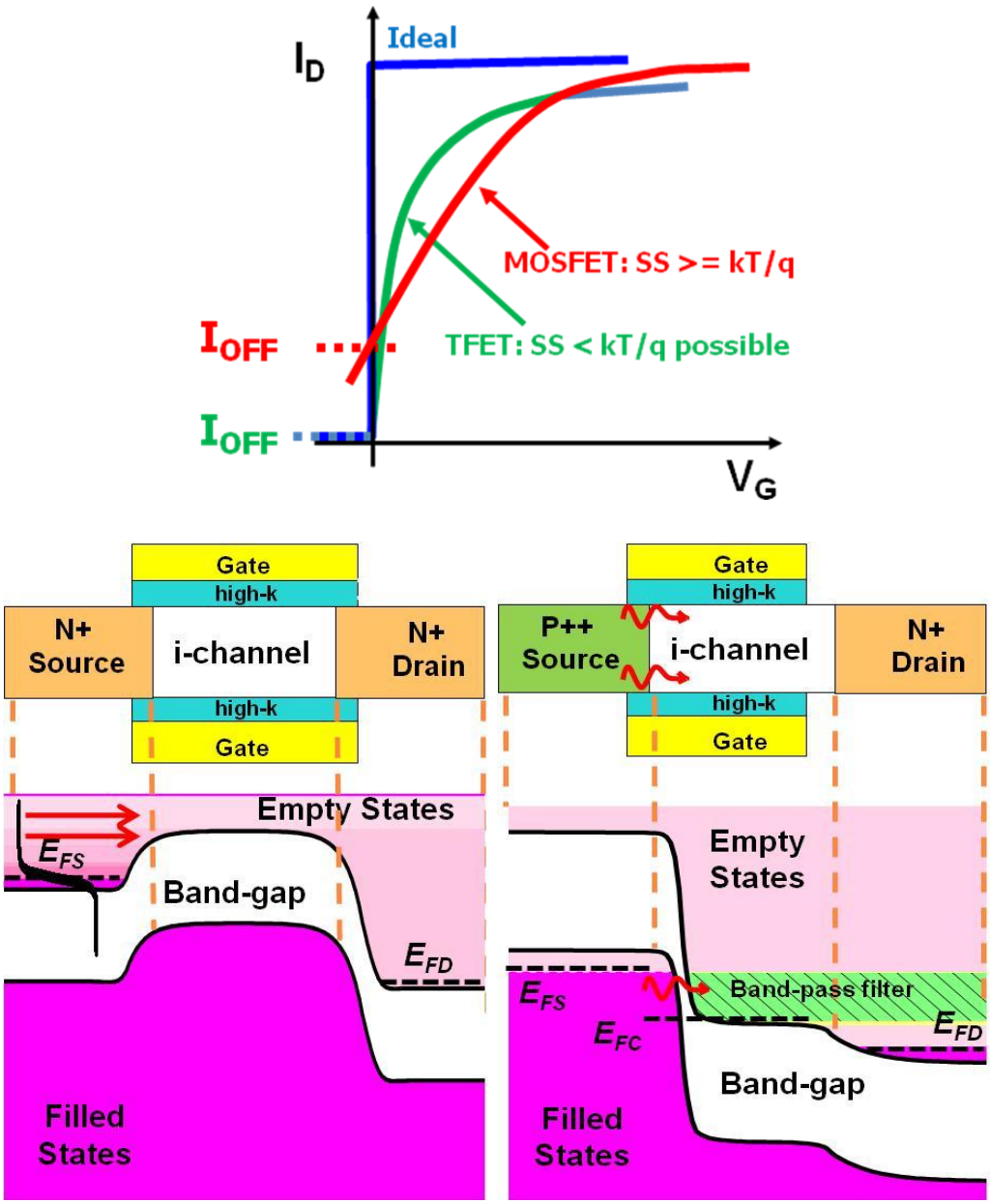

Figure 1-2. (a) Qualitative I_{DS}-V_{GS} curves comparison showing the advantage of using Tunnel FETs over MOSFETs for low power logic applications. (b) Band-diagrams comparing carrier injection mechanism between a MOSFET and a Tunnel FET.

region and allows sub-kT/q sub-threshold slope device operation over a certain gate bias range near the off-state. This allows TFETs to achieve, in principle, much higher I_{ON}-I_{OFF} ratio over a given gate voltage swing compared to the MOSFETs, making the TFET architecture an attractive vehicle to implement low supply voltage (V_{CC}) digital logic circuits. The Tunnel FET schematic of Figure 1-2 (b) represents homo-junction Tunnel FETs. In a homo-junction Tunnel FET, the source, channel and the drain regions are made of the semiconductor. Figure 1-3 shows measured I_{DS}-V_{GS} characteristics of Si [34] and $In_{0.53}Ga_{0.47}As$ [35] homo-junction Tunnel FETs fabricated and reported in literature and compared with 22nm technology Trigate MOSFET [36].

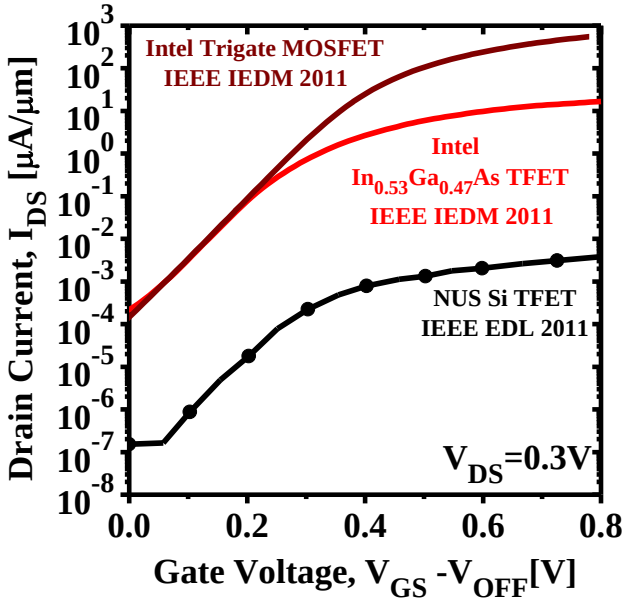

Figure 1-3. Measured I_{DS}-V_{GS} curves of Si [34] and $In_{0.53}Ga_{0.47}As$ [35] homo-junction Tunnel FETs reported. Drive current increases with reducing band-gap, however the on-current is orders in magnitude smaller than the 22nm Trigate Si MOSFET [36] at V_{CC}=0.3V.

The fabricated TFET devices have bulk device geometry and have poor electrostatic control of the gate on the surface channel. However, one trend is very clear. The measured on-current increases with reducing band-gap of the homo-junction Tunnel FET. Si has an indirect band-gap of 1.12eV, while $In_{0.53}Ga_{0.47}As$ has a direct band-gap of 0.74eV. However, the on

current demonstrated till date in the category of homo-junction TFETs is orders of magnitude smaller than that of the Si Trigate MOSFET. Also, note that with decreasing band-gap, the reported off-state leakage is increasing. To replace or substitute MOSFETs for low power logic, both I_{ON} and I_{ON}/I_{OFF} should remain better than MOSFETs for the V_{CC} concerned. This problem and the proposed solution will be discussed in more detail in the following sections.

1-2. Tunnel FET Design and Simulations

1-2.1. Homo-junction TFETs

A simple material system to choose and demonstrate tunneling operation would be a design made of a single semiconductor, doped heavily such that maximum on-state tunneling current can be achieved. Silicon forms the obvious choice because of the presence of high quality native oxide, state of the art foundries and the abundance of SiO_2 (source of elemental Si). The Si TFET demonstrated (Figure 1-3) has bulk device geometry and thick electrical oxide thickness of 4.5nm [33]. It is hence important to scale the device dimensions and see if improvement in device electrostatics as much can bring performance of TFET better than Si MOSFETs at low supply voltages. Figure 1.4 (a-b) show schematic of ultra-thin body TFET device structure and simulated I_{DS}-V_{GS} characteristics for Si homo-junction TFET and compared with corresponding Si MOSFET at V_{DS}=0.5V. TCAD Sentaurus is used to generate the I_{DS}-V_{GS} curves by solving non-local band-to-band generation model self consistently with Poisson's and continuity equation [37]. Effect of quantization due to structural confinement in thin body structures has been considered [38]. Clearly, Si TFET shows SS steeper than 60mV/dec at room temperature. However, the corresponding current levels are too low and the drive current is still orders in magnitude smaller than that of Si MOSFET. This rules out Si TFET as far as any reasonably performing state of the art logic application is concerned. Gate leakage across the physical oxide

thickness of 2.5nm of high-k with ε_r=9.55 was not considered in these simulations. The ultra low off-state leakage of Si homo-junction TFET hence needs to be modified considering practical direct tunneling leakage through the ultra-thin dielectric layer.

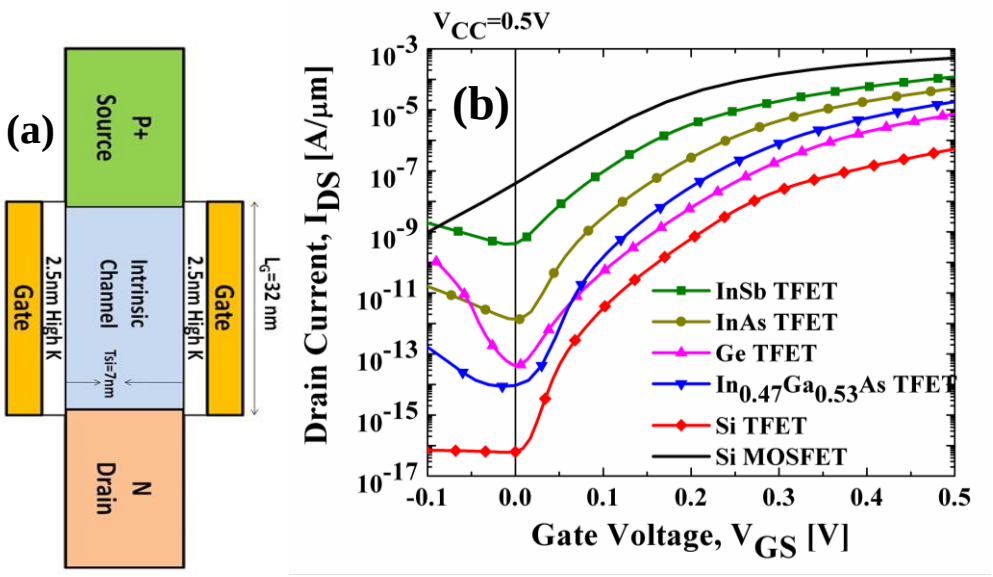

Figure 1-4. (a) Device schematic of an ultra-thin body double gate Tunnel FET (Lg=32nm, T_{oxe}=1nm, Ns=8x10^{19}/cm^3). Numerically simulated I_{DS}-V_{GS} curves for various homo-junction TFET. Si homo-junction TFET show steep switching, however the on-state performance is orders in magnitude smaller than Si MOSFET. Reducing band-gap and hence tunneling barrier improves on-state performance. Due to the reduced tunneling band-gap InSb homo-junction TFET promise MOSFET like on-current, however, the on-off ratio is severely degraded due to exponential increase in ambipolar leakage.

The tunneling probability increases with decrease in the tunneling mass (m_r) and the tunneling barrier height E_{Beff} which is Eg in a homo-junction TFET. The relationship for triangular barrier and W-K-B approximation is shown in Equation 1-4 [44][45][46].

$$T \cong e^{\frac{-4\sqrt{2m_r}E_{Beff}^{1.5}}{3q\hbar F}} e^{\frac{-E_\perp}{\overline{E}}} \tag{1-4}$$

where q is the charge on an electron, F is the average junction field, $E_\perp$ is the tranverse component of the total carrier energy and $\overline{E} = q\hbar F / \sqrt{(2m_r E_{Beff})}$, which determines the impact

of the transverse-energy-state carriers on the tunneling magnitude. The larger the factor $\overline{E}$ is, the less the degradation of tunneling probability by carriers with transverse energy we have. The effect on tunneling by the transverse states is minimized by high electric field, small effective mass, and narrow bandgap.

Figure 1.4 (b) also compares I_{DS}-V_{GS} for various smaller band-gap semiconductors such as Ge, InAs etc. with their material parameters listed in Table 1.1. Clearly, as we move to smaller Eg (E_{Beff}) semiconductor, the drive current increases due to increased tunneling probability and with InSb the I_{ON} is comparable to that of Si MOSFET. However note, on the flip side, the off-state leakage has also increased substantially. The problem with homo-junction TFETs is the uniformity in the band-gap. Due to the reduction in Eg everywhere, parasitic leakage mechanisms such as the Shockley-Read-Hall generation [46][47] within the reverse biased p-i-n diode and the drain side BTBT generation leakage increase exponentially reducing the on-off ratio substantially.

Semiconductor	Eg (eV)	m_e (mo)	m_{lh} (mo)	m_{hh} (mo)	$mr_{e\text{-}lh}$ (mo)	$mr_{e\text{-}hh}$ (mo)	$mr_{e\text{-}hh}/mr_{e\text{-}lh}$
InSb	0.43	0.014	0.015	0.43	0.0072	0.0135	1.93
InAs	0.59	0.023	0.026	0.41	0.012	0.022	1.83
$In_{0.53}Ga_{0.47}As$	0.74	0.041	0.05	0.45	0.0225	0.04	1.78
Ge	0.80	0.067	0.043	0.33	0.0262	0.038	1.45
Si	1.12	0.26	0.16	0.49	0.099	0.17	1.717

Table 1-1. Input parameters for the TCAD simulations of band-to-band generation of carriers using TCAD Sentaurus. Parameters were obtained from Ioffe [39] and Nextnano^3 [37].

We envision Tunnel FETs to outperform MOSFETs for a particular I_{ON} with orders lower I_{OFF}. In order to evaluate if any of these homo-junction TFETs can deliver better I_{ON}/I_{OFF} at any I_{ON} and at any V_{CC}, I_{ON}/I_{OFF} is plotted against I_{ON} for varying supply voltages and shown in Figure

1.2 (a-c). At V_{CC}=0.7V, only Si TFET can deliver higher I_{ON}, however, the corresponding I_{ON} < 20μA/μm, too low to drive any state of the art logic. As V_{CC} is reduced to 0.3V, smaller band-gap

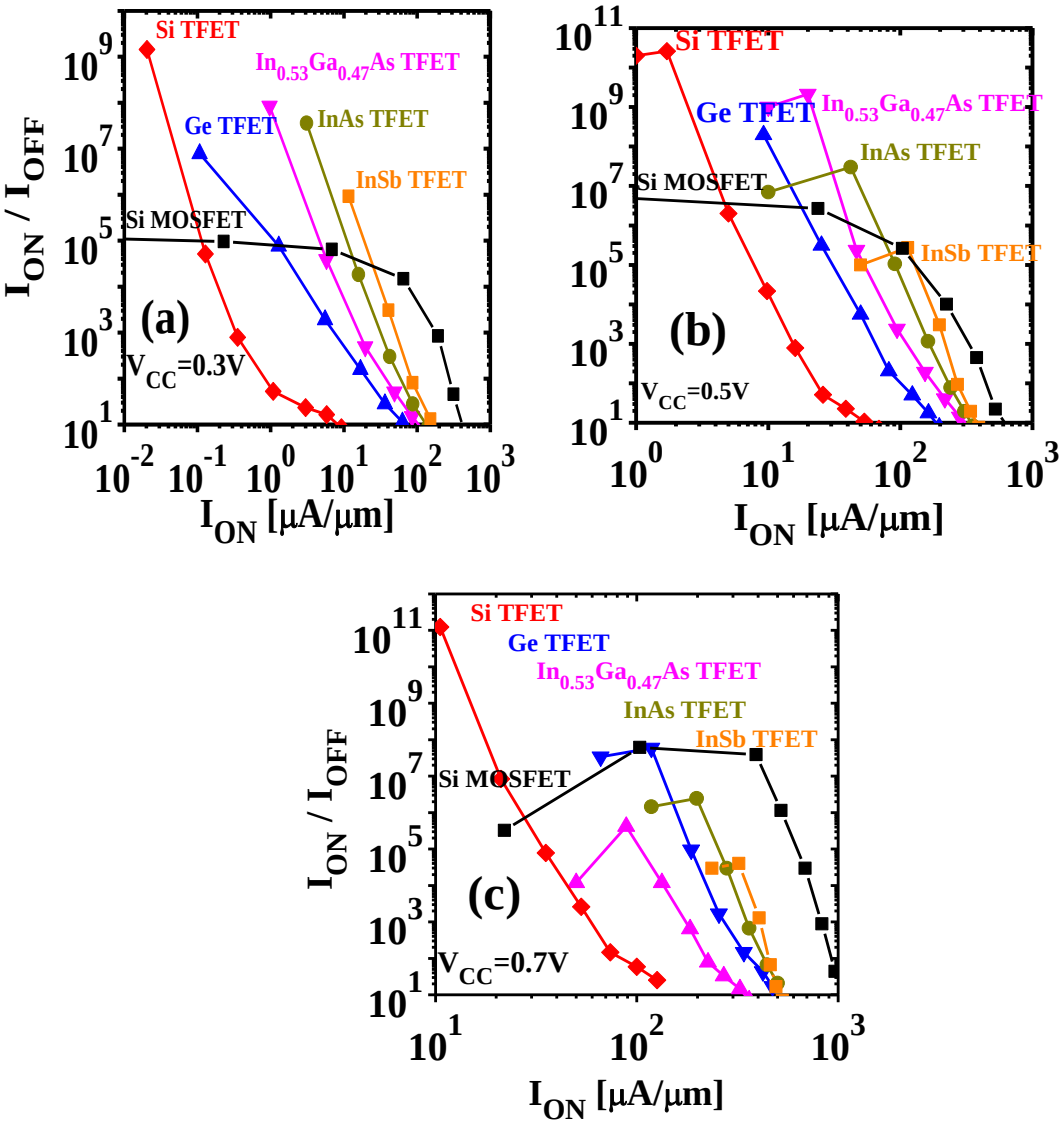

Figure 1-5 (a-c) On-off ratio (I_{ON}/I_{OFF}) plotted against on-current (I_{ON}) calculated from I_{DS}-V_{GS} curves of the homo-junction Tunnel FETs simulated at V_{CC}=0.3V, 0.5V and 0.7V respectively.

semiconductors such as $In_{0.53}Ga_{0.43}As$ and InAs do show higher I_{ON}/I_{OFF}, however the drive current is still in the range of 10-20 μA/μm. The irony with TFETs is that in order to increase I_{ON} we have to reduce the source side tunneling barrier which leads to an un-necessary increase in

parasitic leakage mechanism by nearly the same order as the increase in drive current. Is there a way to just reduce the source side barrier and keep the band-gap large in other portion of the device geometry? The answer is yes and staggered or type II hetero-junction systems form the natural choice.

1-2.2. **Staggered Gap Hetero-junction TFETs**

A. **Materials Options**

It is now clear that simply reducing the band-gap for the homo-junction TFET by choosing alternate materials like Ge, InAs or InSb will not provide performance benefit due to the inherent ambipolar leakage issue. In order to keep the ambipolar leakage low, it is desired to keep the band-gap high at all regions except for the source-channel junction where high tunneling transmission is desired. Recently, it has been theoretically shown and experimentally proven that type II (staggered) band-alignment can provide low effective barrier height (E_{Beff}) at the source-channel tunneling junction while keeping the band-gap of the individual materials high at respective regions [40][41][42]. This means that the drive current and the leakage can be separately optimized for performance, thus creating a design space for a high performance and low power device. With a staggered hetero-junction system (Figure 1-6), the energetic locations

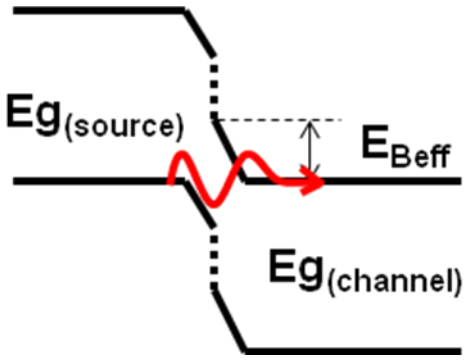

Figure 1-6. Band-diagram of a staggered hetero-junction made of dissimilar source and channel materials. Higher stagger results in reduced E_{Beff}, while the source and channel band-gaps can be relatively large.

of the source valence band edge ($E_{V(source)}$) and the channel conduction band edge ($E_{C(channel)}$) are closer than the respective band-gaps and the effective barrier height (E_{Beff}) is approximately written as [41]:

$$E_{Beff} = E_{V(source)} - E_{C(channel)} \quad (1\text{-}5)$$

Ideally, it is desired to keep E_{Beff} as close to 0eV as possible. Si/SiGe hetero-junctions emerge as the natural choice for realizing Hetero-junction TFETs due to the fact that Si/SiGe hetero-structures are currently being used in commercial CMOS technologies [42]. SiGe is lattice mis-matched to Si and the mismatch increases with increase in Ge composition. Koester et al. have experimentally demonstrated $Si_{0.75}Ge_{0.25}$/Si staggered gap HTFET and shown 2X improvement in drive current with a change in Ge composition from 8% to 25% [42]. However, the conclusion is that further increasing the Ge composition would pose a significant growth challenge owing to the large lattice mismatch and corresponding stringent requirement on the critical thickness of the SiGe source. Hence achieving $E_{Beff} \approx 0$eV is not practically possible.

III-V semiconductors, especially the arsenide-antimonide hetero-junctions provide a wide range of lattice-matched, compositionally tunable effective barrier heights [38][39][43]. Figure 1.4 shows varying band alignments for $GaAs_xSb_{1-x}$ source and $In_yGa_{1-y}As$ channel. Depending on the choice of compositions of In in $In_yGa_{1-y}As$ and Sb in $GaAs_{1-x}Sb_x$, various lattice matched combinations with varying degree of E_{Beff} can be achieved. For example, the combination that is lattice matched to InP intrinsically makes an E_{Beff} =0.5eV [38]. As the % of In in $In_yGa_{1-y}As$ and Sb in $GaAs_xSb_{1-x}$ is increased, the E_{Beff} reduces and for the combination that is lattice matched to InAs, $E_{Beff} \approx 0$eV. Figure 1.4 also shows the band-alignment considering quantization along one direction, i.e. along the ultra-thin body of the tunnel transistor. Since the density of states (DOS) mass of III-V materials is low, especially for the CB, effects of quantization cannot be neglected for scaled TFET devices. Hence it is imperative to check the right material combination for the

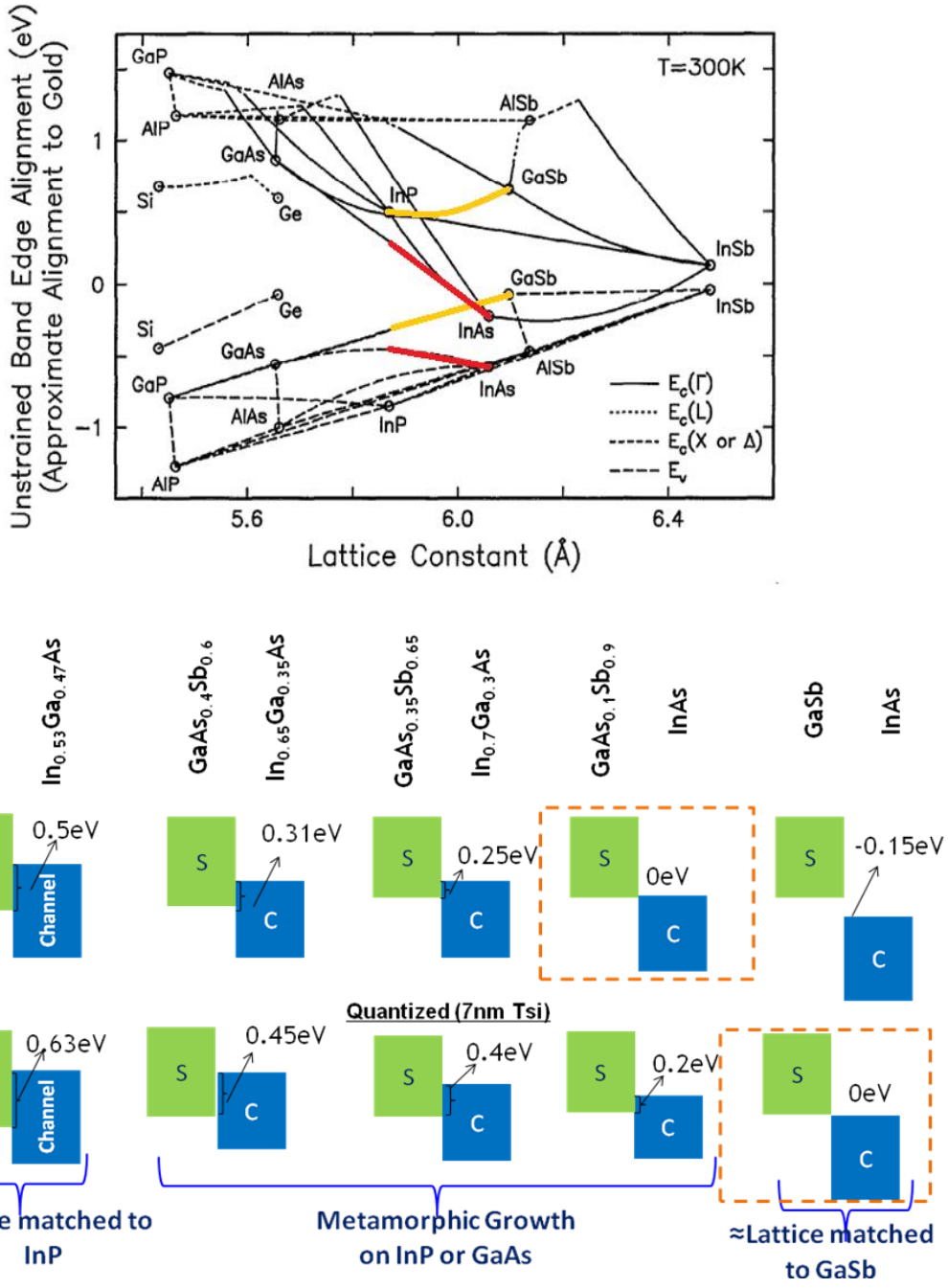

Figure 1-7.(Top) Si, Ge and III-V world map showing energetic positions of the conduction and valence band edges corresponding to the minimum band-gap possible [43]. (Bottom) Extracted band-alignment for GaAsSb source and InGaAs channel lattice matched within themselves [38].

right structure so that the drive current can be maximized, while keeping the off-state leakage low. The effect of quantization and the resulting band-alignments were evaluated using commercial quantum simulator Nextnano^3 [38]. Clearly, the effect of quantization cannot be neglected. For example, bulk $GaAs_{0.1}Sb_{0.9}$/InAs with E_{Beff} =0eV has finite value for the effective barrier height under the effect of quantization. In order to move to a broken gap structure under such a confined geometry we need to consider100% Sb, that is GaSb as shown in the figure.

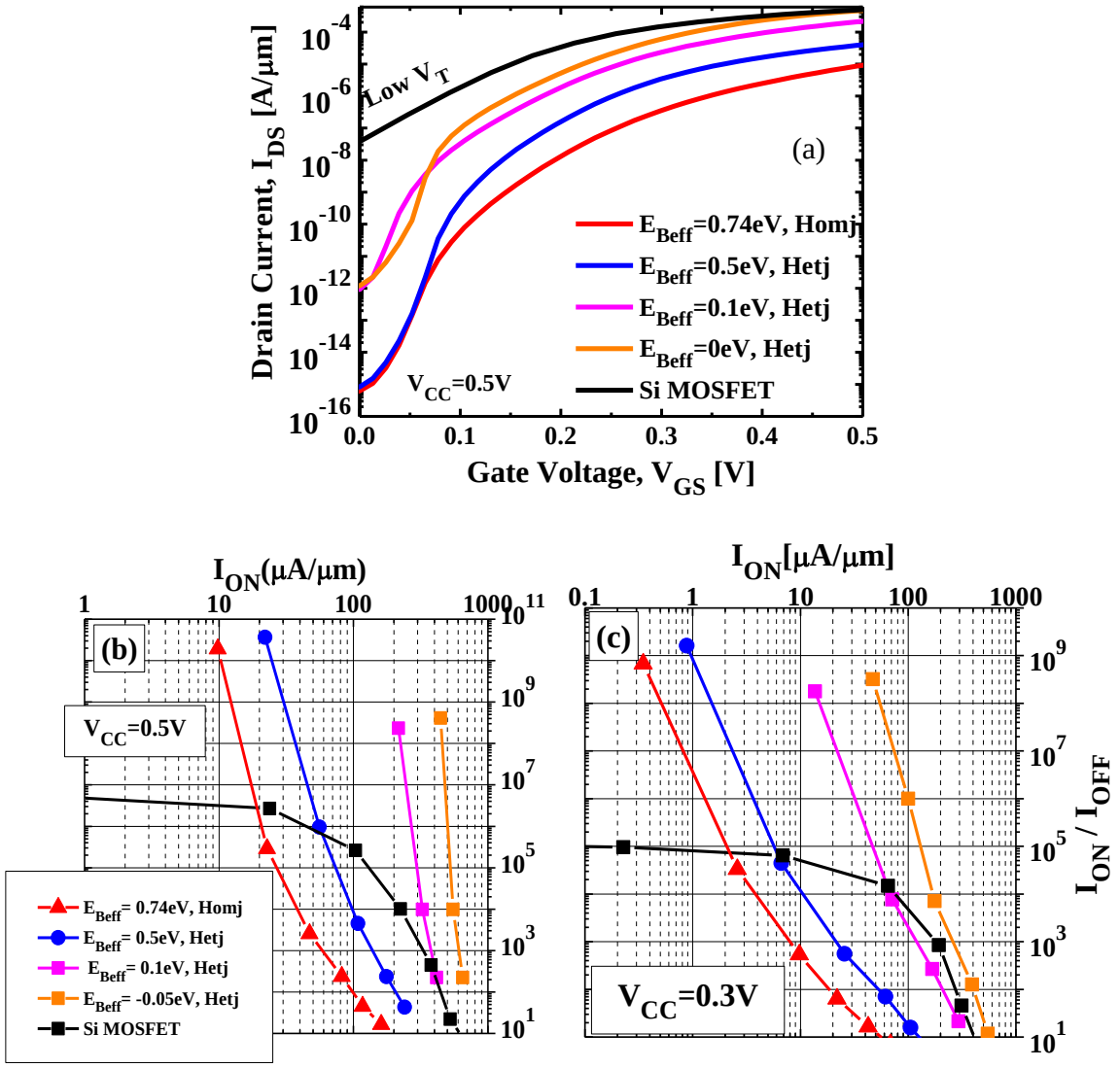

Figure 1-7 (a) I_{DS}-V_{GS} simulated for $In_{0.53}Ga_{0.47}As$ homo-junction TFET, GaAsSb/ $In_{0.53}Ga_{0.47}As$ staggered HTFET and GaSb/InAs broken gap HTFET. (b-c) I_{ON}/I_{OFF} vs I_{ON} plotted at V_{CC}=0.3V and V_{CC} =0.5V. Broken gap HTFETs with UTB-DG device geometry can potentially replace MOSFETs for V_{CC}<=0.5V logic applications.

B. **Device Simulations**

Figure 1-7 (a) shows I_{DS}-V_{GS} characteristics for GaAsSb/InGaAs staggered hetero-junction TFETs for E_{Beff}=0.5eV and E_{Beff}<0eV (L=30nm, T_{oxe}=1nm, T_{body}=7nm and V_{CC}=0.5V). Figure 1-5 (b,c) show I_{ON}/I_{OFF} vs I_{ON} at V_{CC}=0.3V and V_{CC}=0.5V. For comparison, curves for $In_{0.53}Ga_{0.47}As$ homo-junction TFET (E_{Beff} 0.74eV) and Si MOSFET (E_{Beff} =1.12eV) with similar device geometry are also plotted. Clearly, with reducing E_{Beff}, I_{ON} increases. With GaSb/InAs broken gap structure, the drive current is similar to what a MOSFET can deliver with nearly two orders of magnitude advantage over Si MOSFET at V_{CC}=0.3V and I_{ON}=100µA/µm.

C. **Device Demonstration**

Tunnel FETs can replace MOSFETs if they promise to achieve superior performance at

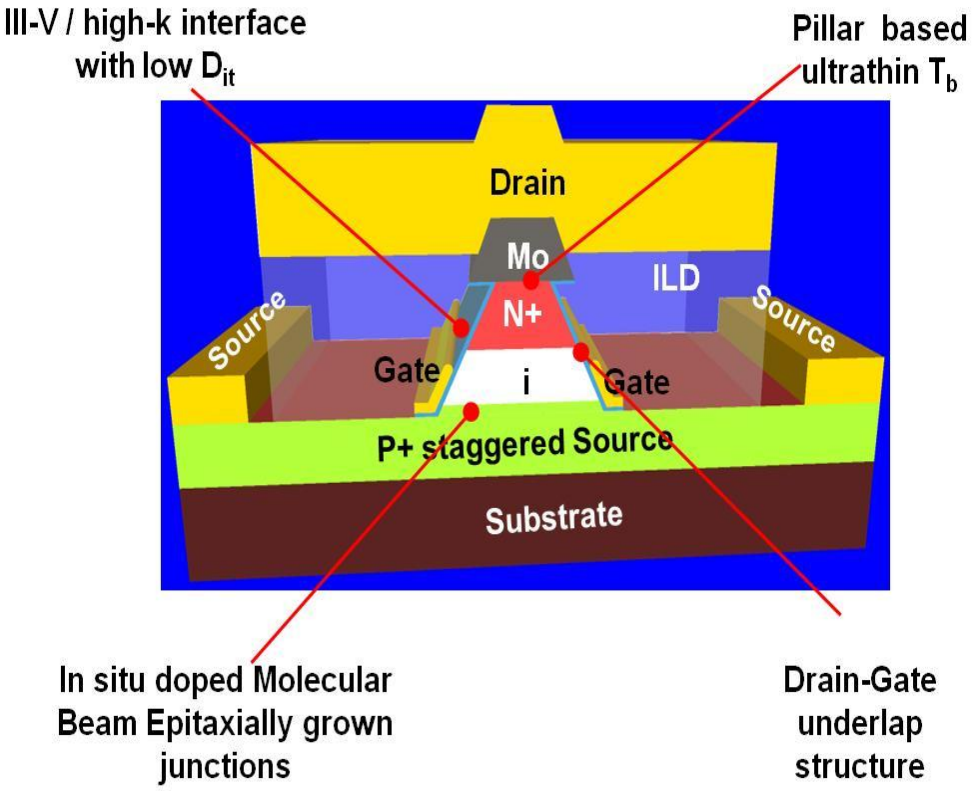

Figure 1-8. Device schematic of the typical non-planar nano-pillar Tunnel transistor fabricated in this dissertation. Key requirements and advantages of the structure in demonstrating high I_{ON} and high I_{ON}/I_{OFF} performance is also described.

scaled supply voltages (V_{CC}≤0.3V) [45]. Since the mechanism of carrier injection is tunneling, we need to know how we can maximize the rate of tunneling without sacrificing the steep switching behavior and the high on-off ratio inherent in a BTBT transistor. Figure 1-8 shows the device schematic of a vertical nano-pillar tunnel transistor. We chose this particular device structure for our experimental demonstration for the following reasons:

Advantages of MBE:

Molecular Beam Epitaxy (MBE) is capable of growing high quality and abrupt hetero-junctions. Abrupt junctions make sure that we achieve the tunnel barrier height we design, the interface is nearly free of defects or Tamm states that can unnecessarily increase the on-off ratio and the junction electric field is maximized due to the abrupt doping profiles. For all the device demonstrations to be discussed in later chapters, the device layers were grown using solid source MBE at IQE Bethlehem, PA [50]. The characterization of the grown materials will be discussed in chapter 2.

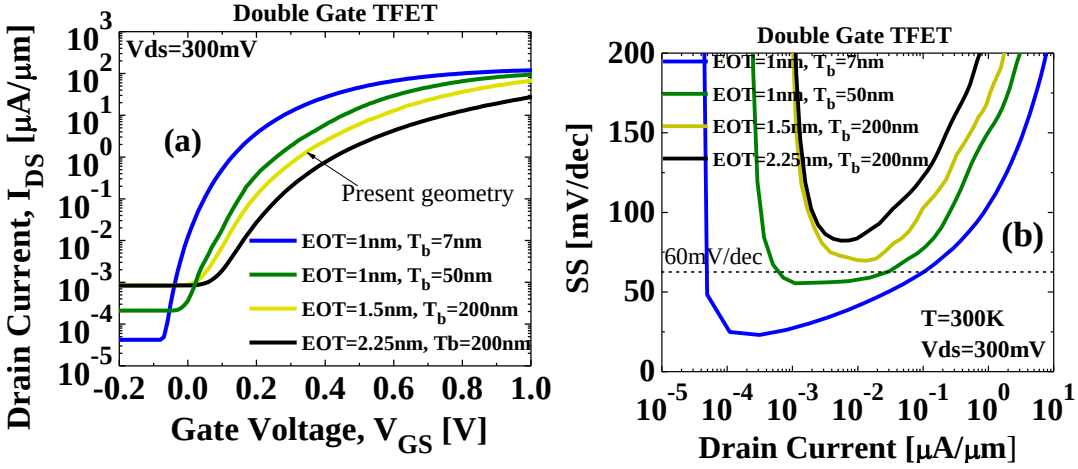

Figure 1-9. (a) Effect of body dimensions on the on-off performance of the $GaAs_{0.35}Sb_{0.65}$/ $In_{0.7}Ga_{0.3}As$ (E_{Beff}=0.25eV) UTB-DG-HTFET. (b) Effect of (T_b)T_{body} and (EOT) T_{oxe} scaling on SS vs I_{DS}. With T_{body}=7nm and T_{oxe}=1nm, SS<60mV/dec for more than two orders change in I_{DS}.

Device Geometry Scaling:

The device structure shown is similar to the FinFET structure of the MOSFETs except for one difference. The channel is horizontal and into the plane of the paper for a MOSFET, while it is vertical for the tunnel FET. With nano-pillar device dimensions, this particular device structure can result in scaled device dimensions while taking advantage of the MBE growth. It is important to note that unless the device structure is extremely scaled, TFETs will not be able to provide significant performance advantage [51][52]. For a broken gap band-alignment, it has been shown that ultra thin body double gate TFET device configuration with T_{body} as small as 5-10nm and T_{oxe}=1nm is required such that I_{ON}/I_{OFF} is maximized for a given I_{ON}[51]. To illustrate the dependence of I_{ON}, I_{OFF} and SS on device dimensions, Figure 1-9 (a) shows numerical I_{DS}-V_{GS} simulated for GaAsSb/InGaAs TFET with E_{Beff}=0.25eV. T_{body} is varied from 200nm to 7nm and T_{oxe} has been scaled from 2.5nm to 1nm. Figure 1-9(b) shows the SS vs I_{DS} curve evaluated from Figure 1-9(a) for each of them. Clearly, I_{ON} and SS improve with T_{oxe} scaling and is expected due to the improvement in device electrostatics. I_{OFF} reduces with T_{body} due to the reduction in parasitic conduction. However, SS is not sub-60mV/dec for large device dimensions. Due to the strong dependence of the SS on V_{GS}, SS smaller than 60mV/dec can only be achieved with T_{body} $\leq$7nm and $T_{oxe}\leq$1nm as shown in 1-9 (b).

D. **Selection of Hetero-junction**

In order to demonstrate the worth of hetero-structures in eliminating drive current limitations in TFETs, growth of a high quality and abrupt hetero-junction is required. GaAsSb/InGaAs lattice matched to InP has an E_{Beff}=0.5eV. Because of the naturally occurring InP binary substrate, the MBE growth is for this particular hetero-junction is matured and nearly avoids growth of substrate induced defects. However, the E_{Beff} is too large to deliver reasonable drive current and performance. The system GaAsSb/InAs also has lattice matched InAs binary substrate, however the band-alignment is broken. The system is highly susceptible to any

imperfection during growth or switching cycle which can lead to high parasitic leakage degrading the device electrostatics. Thus, in this dissertation, intermediate band-alignments with moderate and high staggers have been chosen for demonstration of simultaneous improvement in on current and on-off ratio over homo-junction counterparts. They are $GaAs_{0.6}Sb_{0.4}/In_{0.35}Ga_{0.65}As$ with E_{Beff}=0.31eV and $GaAs_{0.65}Sb_{0.35}/In_{0.3}Ga_{0.6}As$ with E_{Beff}=0.25eV. The materials characterization and device fabrication results will be discussed in the following chapters.

E. **Gate Dielectric Integration**

Unlike SiO_2/Si interface, native oxides on III-Vs are inferior and do not form a device quality hetero-interface. Oxides of elemental III-V act as large scattering centers for channel carriers and result in significant degradation of the on-state mobility and hence the drive current. The scattering centers also accompany high density of interface states. Figure 1-10 (a-b) show measured capacitance voltage (C-V) and conductance voltage (G-V) characteristics at room temperature on n-type $In_{0.53}Ga_{0.47}As$ ($N_D=2x10^{17}/cm^3$) MOS capacitors (MOSCAPs) for the frequency range 75KHz-2MHz. Fifty cycles of Al_2O_3 [55] were deposited at 200^{o}C using plasma enhanced Atomic Layer Deposition technique (PEALD) [57]. Figure 1-10 (c-d) show C-V and G-V characteristics after forming gas anneal at 350^{o}C for 10mins. For both cases of as-measured and annealed C-V, capacitance higher than depletion is observed due to the contribution from band edge and mid-gap interface states (Dit). Figure 1-11(a,b) show the extracted density profile of interface states and the carrier capture time constant as a function of energy inside the band gap of $In_{0.53}Ga_{0.47}As$ using the technique discussed in [56]. The mid-gap density of traps is orders in magnitude higher compared to Si/SiO_2 interface. Since these traps share charge with the channel, they slow down the efficiency of the Fermi-level movement and hence degrade the minimum achievable sub-threshold slope in a MOSFET. In TFETs, apart from this sluggish Fermi level movement, these traps also contribute to trap assisted tunneling in the off-state,

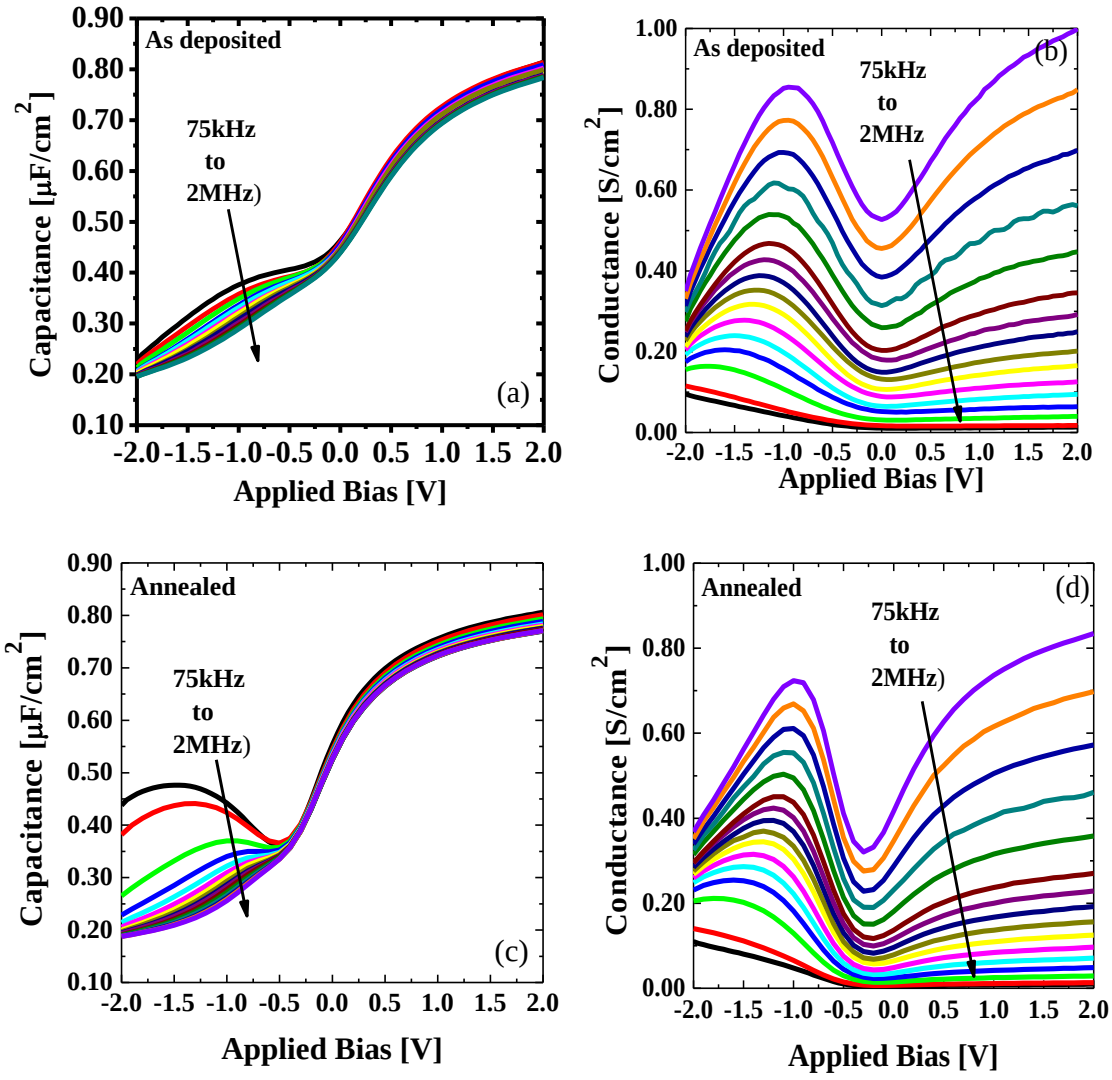

Figure 1-10. (a-d) Capacitance-voltage and conductance-voltage measured on 5nm Al_2O_3/ n-$In_{0.53}Ga_{0.47}As$ MOSCAPs for frequency range: 75kHz-2MHz. Al_2O_3 was deposited at 200°C using Plasma Enhanced ALD technique [57].

creating additional conduction mechanism and thus further degrading the SS. Figure 1-12 (a,b) show measured and modeled I_{DS}-V_{GS} curves for $In_{0.53}Ga_{0.47}As$ homo-junction TFET reported in IEDM 2011 paper by S. Mookerjea et al.[53]. The on-current is nearly temperature independent, however, the SS and the off-state leakage is significantly temperature dependent, with the SS min changing by factor close to change in the kT/q suggesting the existence of trap assisted tunneling

followed by thermionic emission process of Poole-Frenkel type [54]. The Dit profile required to model the SS using simulations has similar mid-gap density profile, while the profile near the conduction band-edge required higher values than measured with MOSCAPs. The difference could be because of the side wall and the wet etch differences between the planar MOSCAPs and non-planar TFET geometry. Simulations show that for $In_{0.53}Ga_{0.47}As$ homj TFET, mid-gap Dit less than at least $10^{12}/cm^2/eV$ is required in order to achieve point SS smaller than 60mV/dec at room temperature. This requirement, however, can vary for materials with different E_{Beff}.

Atomic layer deposition technique can be made effective in depositing high quality physical oxides such as Al_2O_3, HfO_2, ZrO_2 etc. with significantly scaled T_{oxe}. However, in order to take advantage of these ALD deposited oxides, proper pre deposition clean, native oxide etch, surface passivation, pre-deposition and post-deposition anneal need optimization to make sure that the interface quality is good enough to prevent any parasitic conduction diluting the SS.

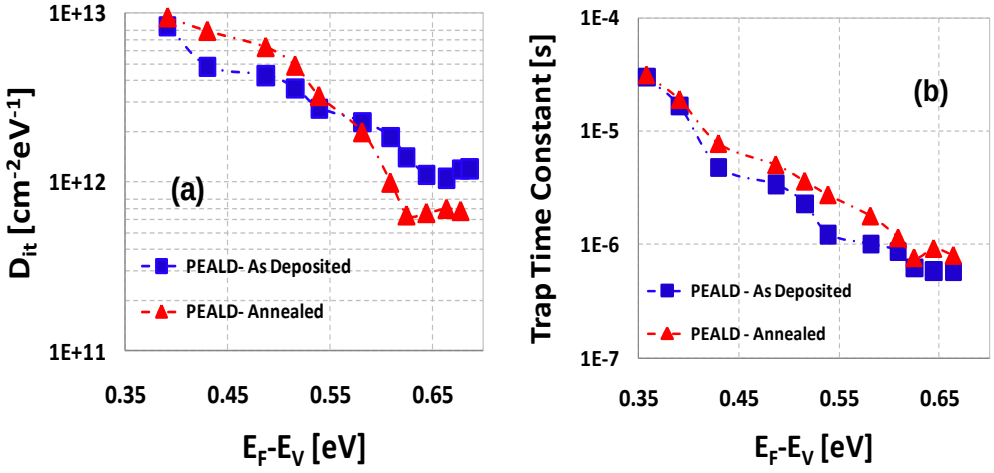

Figure 1-11 (a-b) Dit and trap response time extracted from the measured admittance using self consistent modeling of the measured admittance [56][57].

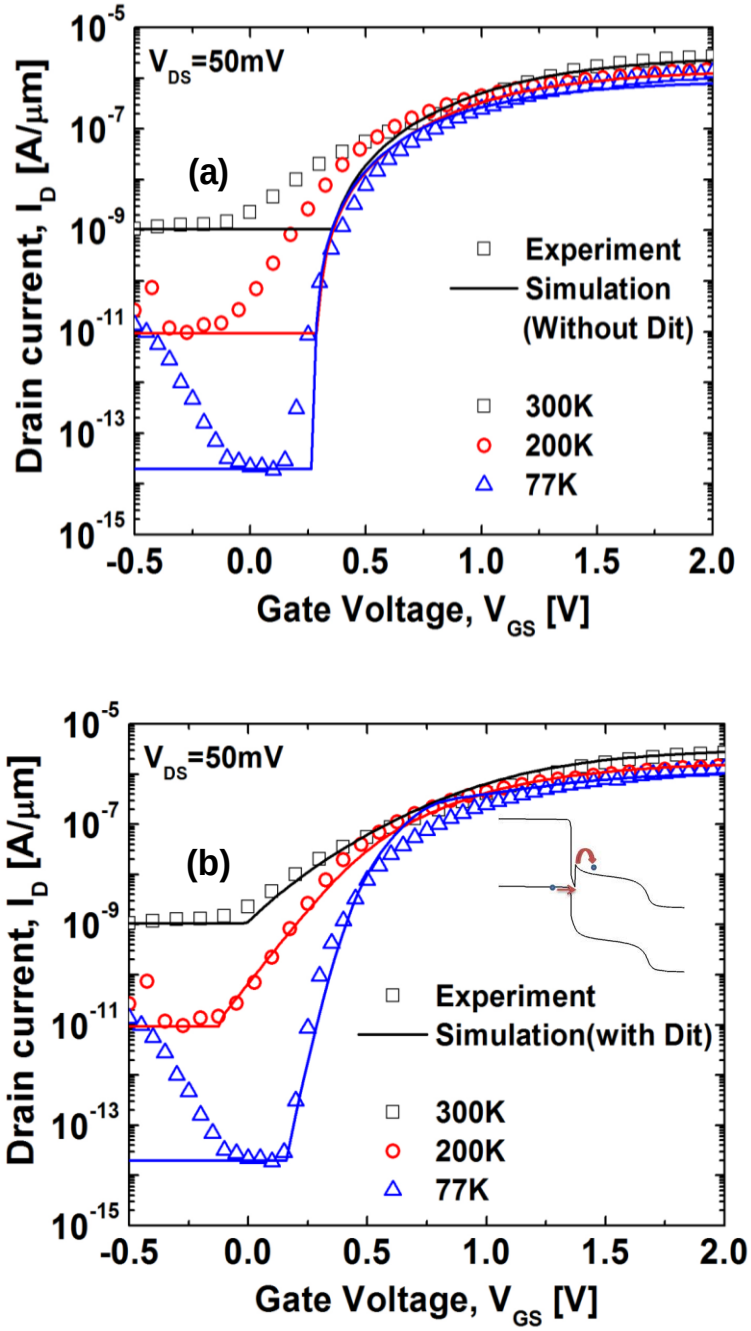

Figure 1-12. (a) Temperature dependent I_{DS}-V_{GS} characteristics of $In_{0.53}Ga_{0.47}As$ homo-junction TFET. Symbols represent measured curves and lines are modeled curves obtained using BTBT model and S-R-H model. (b) Discrepancy within the sub-threshold regime is explained using trap assisted tunneling followed by Poole-Frenkel type thermionic emission process [54].

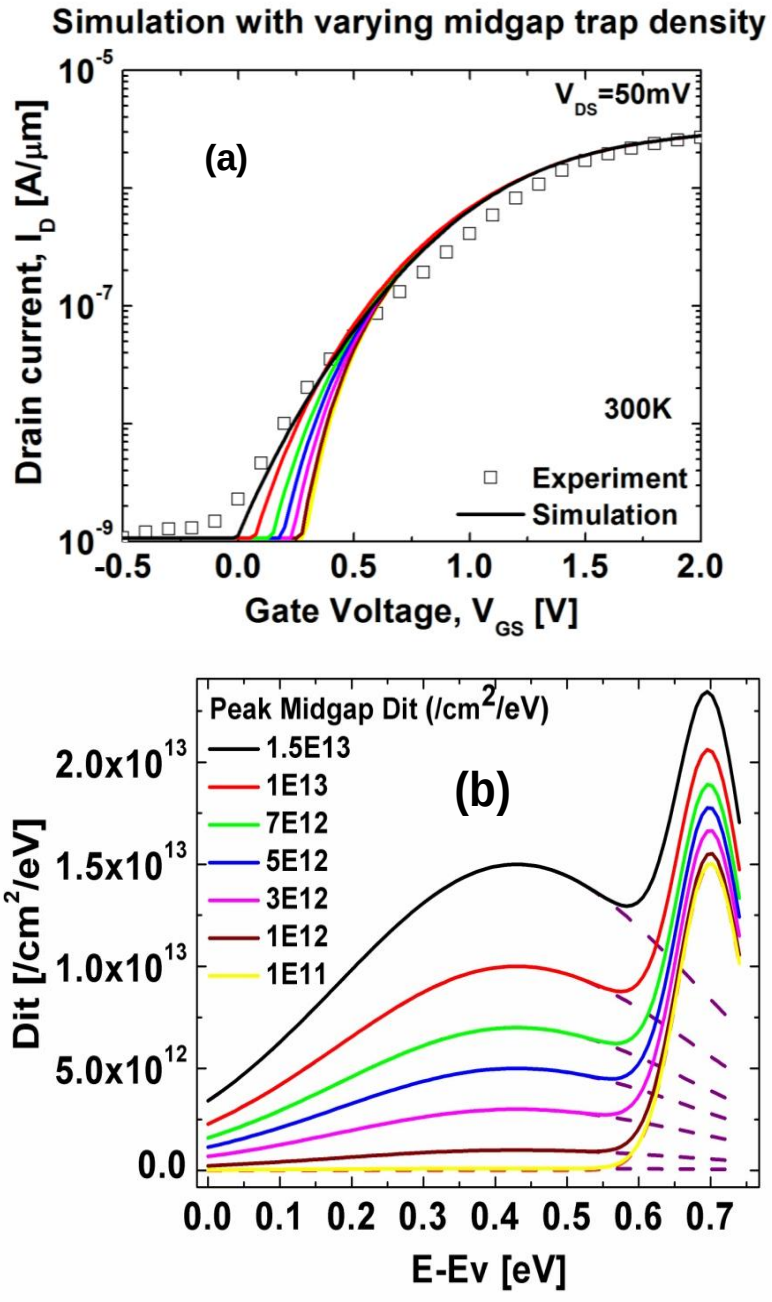

Figure 1-13. (a-b) Effect of reducing mid-gap Dit on the SS. For $In_{0.53}Ga_{0.47}As$ homj TFET, reducing Dit at least below $10^{12}/cm^2/eV$ is crucial in order to observe sub-60mV/dec switching operation at room temperature.

1-3. Conclusion

Achieving high on-currents in the category of homo-junction Tunnel FET trades with significant increase in the off-state leakage and reduction in the on-off ratio mainly due to the uniformity of the band-gap in the source, channel and the drain regions. InSb homo-junction TFET promises MOSFET like on-current, however, due to the low band-gap of InSb, parasitic leakage mechanisms such as the ambipolar leakage is very high and degrades on-off ratio significantly . III-V staggered hetero-junctions, especially lattice matched $GaAs_{1-x}Sb_x/In_yGa_{1-y}As$, enable reduction of the tunneling barrier height locally near the source channel junction, while maintaining large band-gaps in the respective regions. $GaAs_{1-x}Sb_x/In_yGa_{1-y}As$ provide a wide range of lattice matched compositionally tunable effective tunneling barrier height. GaSb/InAs broken gap hetero-junctions promise MOSFET like on-current (I_{ON}>100μA/μm) at $V_{CC}\leq 0.3V$ while maintaining I_{OFF}=5nA/μm promising V_{CC} scaling for future low power logic applications.

Chapter 2

Vertical Nano-pillar TFET Process Development

It was discussed in section 1-2.2 (B) that scaling device dimensions especially the body thickness is essential in realizing enhancement in on-current of a tunnel FET while maintaining high I_{ON}/I_{OFF} ratio. Hetero-junctions, specifically ternary material interfaces of III-Vs, pose great risk of forming defects during their materials growth. Poor quality hetero-interface can potentially generate parasitic leakage paths either through trap assisted tunneling or S-R-H generation mechanism. These are bulk leakage mechanisms, independent of the gate bias. The best way to reduce these parasitic leakage mechanisms is by reducing the T_{body} of the device to ultra-thin dimension ($T_{body} \leq 7$nm) and $T_{oxe} \leq 1$nm.

We have adopted a non-planar TFET process flow that has been completely developed at Penn State nanofabrication facility. The device schematic is shown in Figure 2-1 (a). $In_{0.53}Ga_{0.47}As$ homo-junction TFET was chosen for the process flow optimization due to the relatively matured knowledge of the Atomic Layer Deposition of high-k on $In_{0.53}Ga_{0.47}As$ [58]

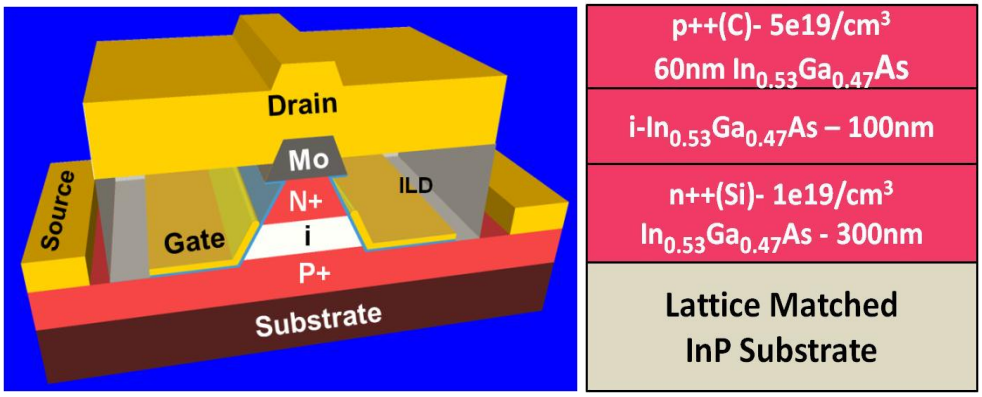

Figure 2-1. (Left) Device Schematic and layer structure. (Right) $In_{0.53}Ga_{0.47}As$ homo-junction TFET Layer structure grown using MBE.

and reasonably large band-gap of 0.74eV due to which high on-off ratio is expected with scaled device dimensions. Growth of $In_{0.53}Ga_{0.47}As$ on InP using MBE is a matured technology now and the density of bulk defects is expected to be low. Thus, it is easier to study the effect of scaling nano-pillar perimeter 2(L+W) on the I_{OFF} and SS of the TFET. Here, L is pillar length into the plane of the paper and W is the width of the pillar along the plane of the paper.

2-1. Vertical Nano-pillar Process Flow

The $In_{0.53}Ga_{0.47}As$ homo-junction TFET wafer was grown at IQE Bethlehem, PA using solid source MBE. Sample of nearly $1x1cm^2$ is cleaved out of the wafer along (110). Step I of the fabrication process involves degreasing of the sample in Acetone, Methanol and IPA. This is then followed by deposition of 300nm of Molybdenum using RF sputtering as shown in schematic of

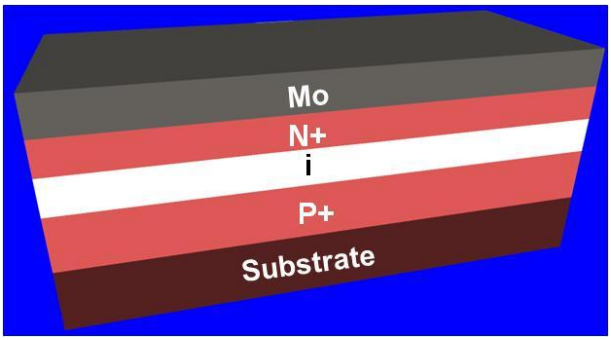

Figure 2-2. Step I- Blanket deposit Molybdenum on pre-cleaned III-V wafer.

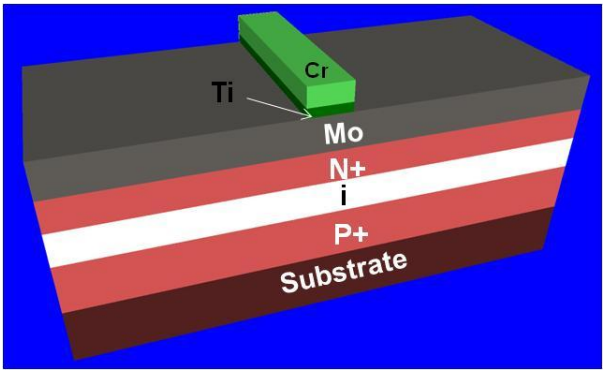

Figure 2-3. Step II- Define Cr/Ti dry etch mask using EBL and Lift-off techniques.

Figure 2. The details of the processing conditions can be referred in the Appendix. In step II, 5µm long pillars and widths varying from 20µm down to 200nm are defined with 30nmTi/70nm Cr using E-beam lithography (EBL) and lift off techniques. The representative schematic is shown in Figure 2-4(a). Step III involves dry etch of Molybdenum and $In_{0.53}Ga_{0.47}As$ using inductively coupled reactive ion etch (ICP-RIE). The gas recipes involve $Cl_2/Ar/SF_6$ chemistry. The etch is stopped close to the P+/I junction. The representative schematic and the scanning electron microscopy (SEM) image of the etched pillar are shown in Figure 2-4 (b).

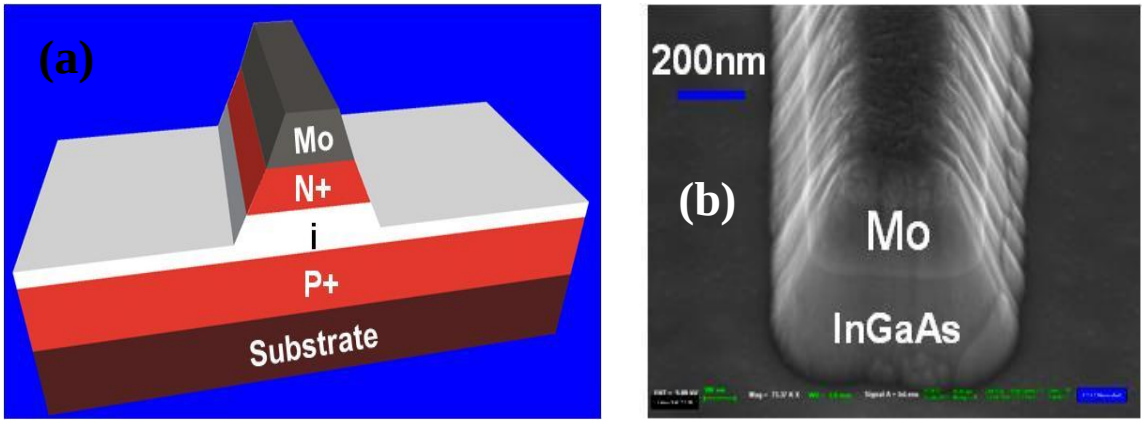

Figure 2-4. Step III- (a) Dry etch Mo and InGaAs using ICP RIE. The remaining Cr/Ti etch mask is removed using dilute HF. (b) SEM showing etched Mo and InGaAs.

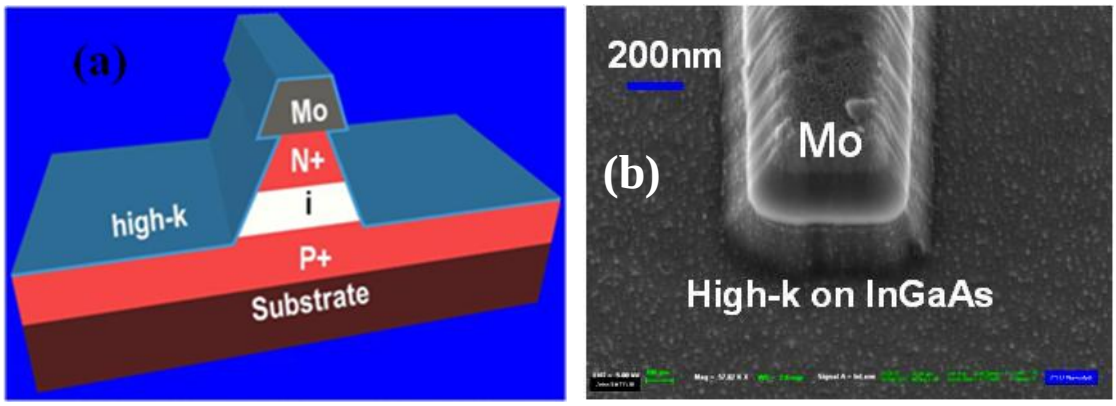

Figure 2-5. Step IV – (a) Wet etch undercut of the pillar using citric acid. Native oxide removal using 1:10 HCl: H_2O and ALD high-k (5nm Al_2O_3) at 250^oC. (b) SEM after wet etch undercut.

In step IV, the dry etch is followed by wet etch undercut using citric acid and hydrogen peroxide mixture. The wet etch undercut serves dual purpose. It removes most of the dry etch induced side wall damage and also it helps in self aligned deposition of the side wall gate at the tunneling junction. This is followed by 50 cycles of Al_2O_3 deposition using Atomic Layer Deposition technique at deposition temperature of 250^{o}C. The representative schematic along with the SEM showing undercut are shown in Figure 2-5 (b). The TEM of the high-k is shown in Figure 2-6.

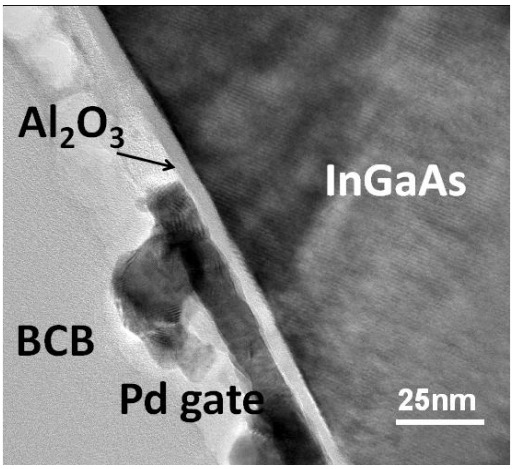

Figure 2-6. TEM showing the side wall of the InGaAs with 5nm Al_2O_3 and 20nm Pd gate metal.

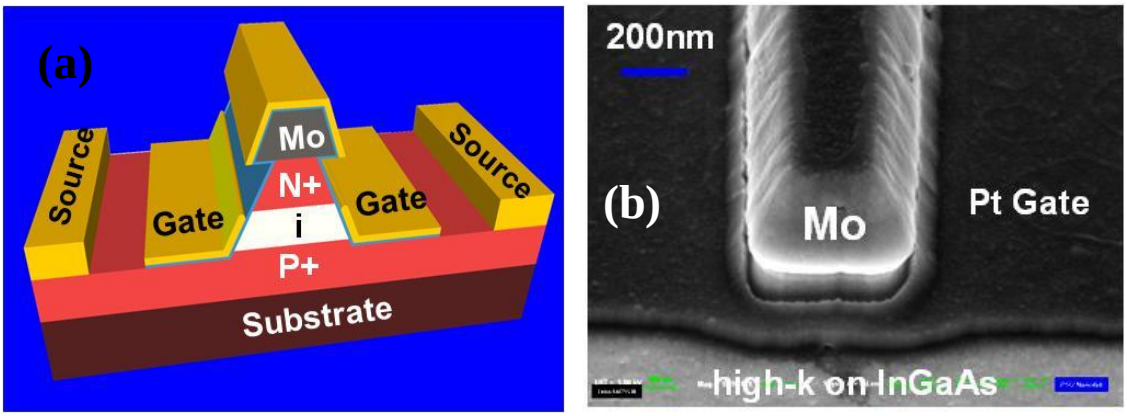

Figure 2-7. Step V- (a) Self aligned gate lift-off taking advantage of the undercut. Source contact definition, high-k removal and Source metal lift-off. (b) SEM showing self aligned Pd gate.

Next, in step V, 20nm Pd is vertically deposited in a self aligned manner on the side wall using EBL and lift-off technique. Because of the undercut, the gate metal on the top and the side-wall is not continuous. This process avoids additional lithography and etch back step which would have been required if the deposited metal was continuous. Figure 2-7 show the representative device schematic and the tilted view SEM image of self aligned gate metal deposited on the side wall. After gate contact definition, source window is defined using EBL and dry etch is used to removed the gate oxide Al_2O_3 and create the P++ source contact. For oxide dry etch, ICP RIE was used with Cl_2/Ar as the etch chemistry. Using the same window defined for the dry etch, Ti/Pd/Au is deposited and lifted-off to form the source contact and source pads.

Step VI is the final step. After source contact formation, Benzo-Chloro Butane (BCB) is spun coated and cured within N_2 ambient at 250^{o}C for 1hr. The thickness of the spun BCB is around 2.4µm while the pillar height is close to 800nm. The BCB is then etched back from 2.4µm to 600nm, 200nm below the Mo surface. The etch back was done in PT 720, a capacitively coupled reactive ion etch chamber with O_2/CF_4 as the gas mixture. The details of the etch recipe is mentioned in the Appendix. Etch back was followed by EBL for the drain pads. After drain pad

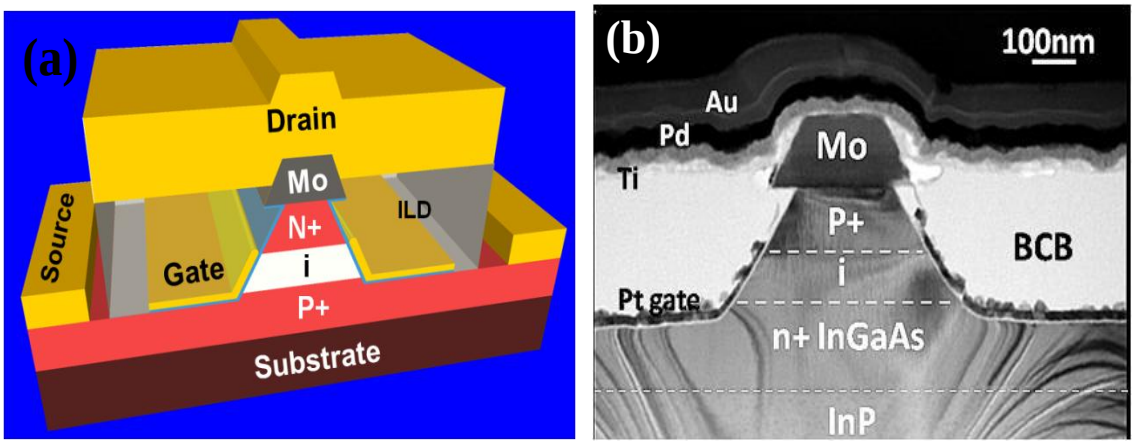

Figure 2-8. Step VI – (a) Planarization with BCB, etch back and Drain pad lift-off. (b) Cross-section TEM image showing 200nm mask defined pillar width, Pd self aligned gate, crystallographic side wall obtained with wet etch and BCB used for planarizing the device.

definition on top of BCB, dry etch was performed to remove Pd and Al_2O_3 on top of Mo using Cl_2/Ar etch chemistry. After the dry etch the sample was immediately loaded into E-beam evaporator for Ti/Pd/Au drain pad deposition. The cross-section schematic and the TEM of the vertical nano-pillar InGaAs homojunction TFET is shown in Figure 2-8.

2-2. Electrical Results

BCB on top of the source and the gate pads were then etched off and the devices were brought to the Cascade probe station for two terminal pin and three terminal electrical measurements. Agilent 4156A semiconductor parameter analyzer (SPA) was used to do the electrical measurements. Figure 2-9 shows two terminal p-i-n curves measured with the gate terminal open. The current density has been normalized with the defined mask area of the

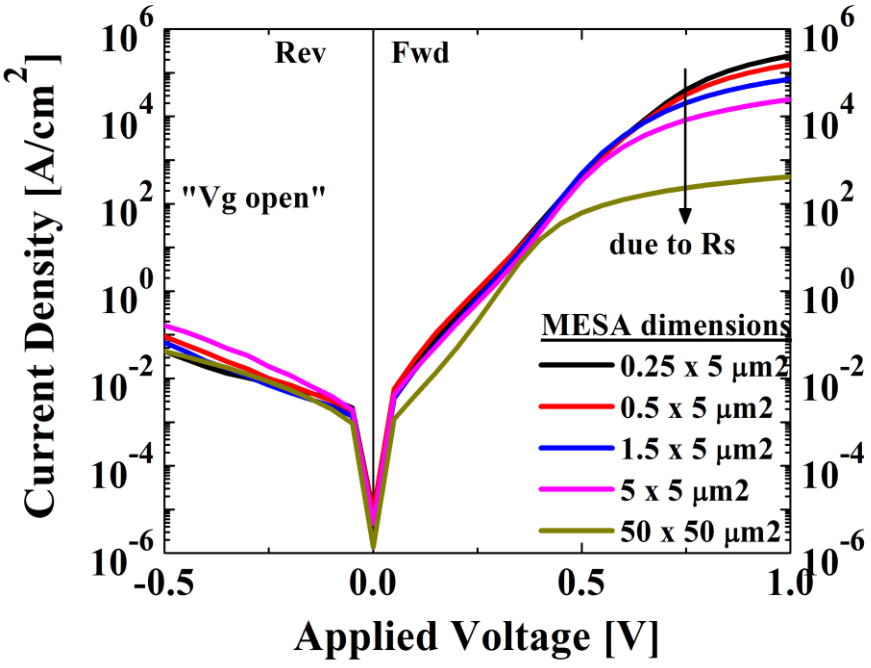

Figure 2-9.Open gate pin curves measured as a function of pillar area. The reverse leakage scales with area signifying bulk properties. Forward sub-threshold slope also fall on top of each other except the forward on-current which is limited by series resistance posed by the measurement set-up and device intrinsic resistances.

devices. The curves are rectifying with maximum on-off ratio of 10^6 between V_{DS}=±1V for the pillar dimensions of 0.25x5μm^2. The reverse side current is small and determined by S-R-H generation recombination mechanism. The reverse leakage current density scales with the volume of the device while the forward side current is limited by the series resistance. Since the reverse leakage scales with the volume of the pin diodes, the off-state leakage/unit length of the pillar, which defines the off-state leakage of a tunnel FET, should scale with the width of the pillar. Figure 2-10 shows the room temperature transfer characteristics (three terminal measurement) of the homo-junction TFET for V_{DS}=1.05V and for different mask defined area of the pin diodes. Clearly, the I_{OFF} at V_{GS}=0V scales with the width of the device. For example for a change from

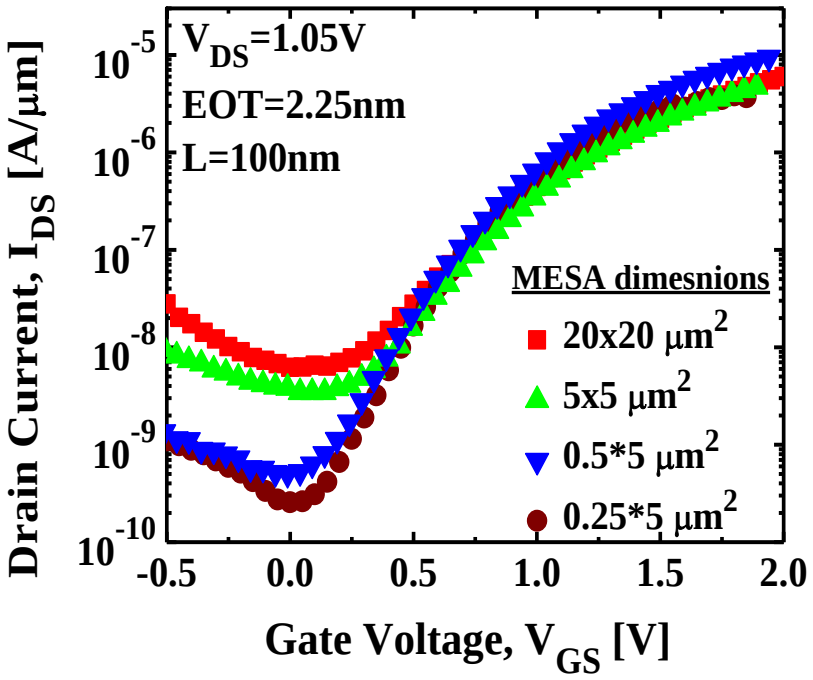

Figure 2-10.Measured I_{DS}-V_{GS} curves as a function pillar area. The on-current scales with the perimeter of the Tunnel FET device signifying gates current, while the off-state scales with area consistent with the pin measurements. Using the nano-pillar TFET process flow minimum pillar width of 250nm was achieved.

20µm to 0.25µm, the I_{OFF} changes from $3x10^{-8}$A/µm to $2x10^{-10}$A/µm, nearly two orders reduction in the off-state leakage consistent with the scaling of the pillar defined area. However, the on-current, at V_{GS}=2V, scales with the perimeter of the device and is constant when normalized with the 2(L+W) as shown in Figure 2-10. This is consistent as the on-current is gate controlled and is a surface phenomenon. The switching slope (SS) however should improve with reduction in I_{OFF} as the SS is a strong function of I_{DS} in Tunnel FET. Figure 2-11 shows SS vs I_{DS} evaluated from I_{DS}-V_{GS} curves plotted in Figure 2-10. Due to the reduction in the off-state leakage, switching slope at smaller drain currents is exposed. As SS is a strong function of I_{DS}, SS improves from a minimum value of 350mV/dec to 200mV/dec due to the reduction in I_{OFF}. Note however that the measured SS is not smaller than 60mV/dec at room temperature. Near the high-k/InGaAs interface, high density of mid-gap and conduction band-edge states are present as was shown in

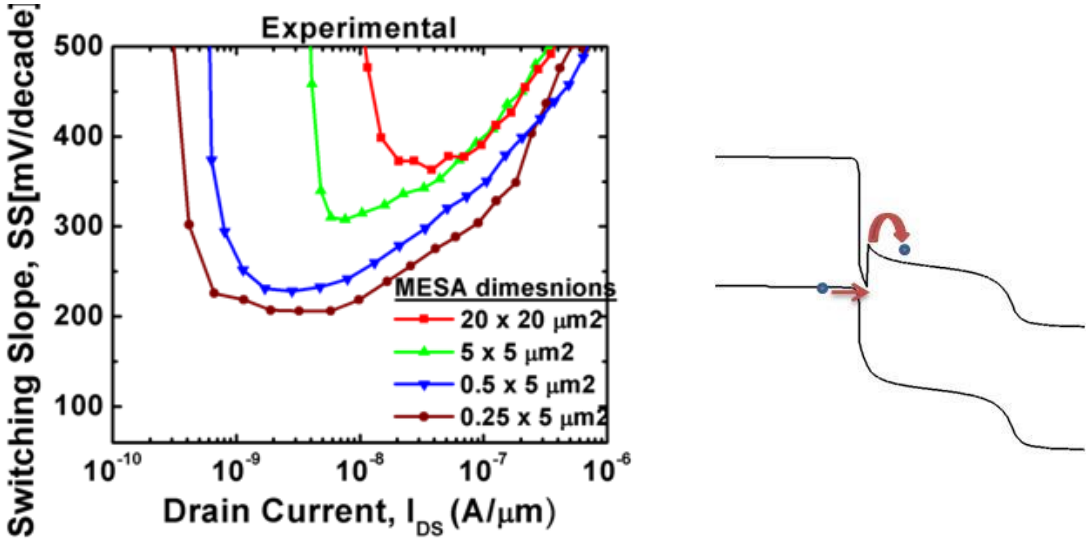

Figure 2-11. (Left) Siwthcing slope vs Ids for different pillar area. Increasing the perimeter to area ratio results in decrease in off-state leakage and hence steeper SS. (Right) SS>60mV/dec at room temperature is a result of trap assisted tunneling + thermionic emission near the higk-tunneling junction.

section 1-2.2 (E). These states slow down the Fermi level movement by participating in the charge balance. Also, in the off state, when the conduction band in the channel is not aligned with

the valence band edge of the source, these traps act as intermediate states that assist in tunneling. The entire process consists of an electron tunneling into one of these intermediate trap state and then thermionically emit into the channel following the Poole-Frenkel dependence of the trap depth on the junction field [54]. This makes SS highly temperature sensitive. As temperature is lowered, the emission process begins to subside. Hence the tunneling to trap process by itself does not exist and the switching slope is entirely limited by pure BTBT process which is what is desired ideally.

Scaling device area also improves the peak to valley current ratio of the negative differential resistance (NDR) observed in the forward side of the gated p-i-n curves. Figure 2-12 shows I_{DS}-V_{DS} curve, plotted in semilog scale, illustrating the dependence of the gated and non-

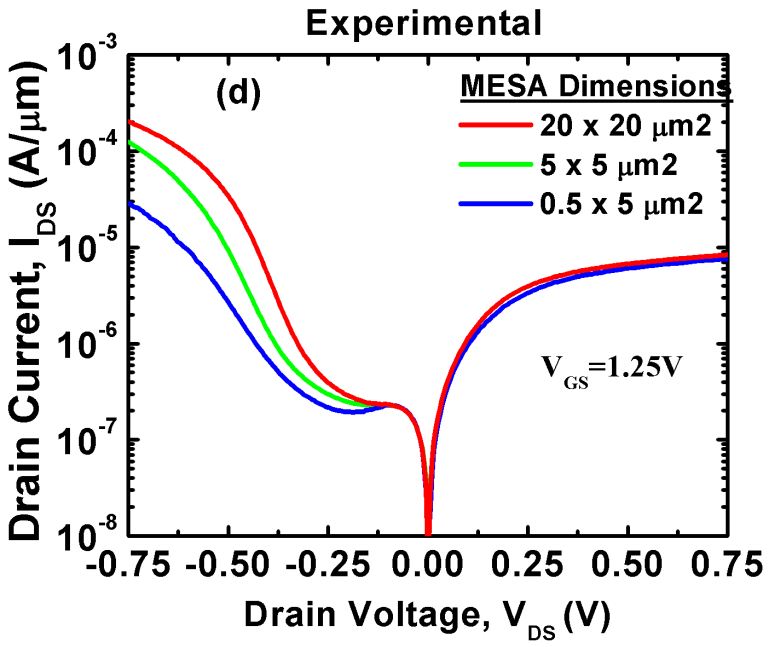

Figure 2-12. Improvement in PVCR as a result of increase in perimeter to area ratio with the nano-pillar device geometry.

gated current on the TFET area. As the area is scaled, the gated current per perimeter is the same, however the valley current which is essentially a mixture of forward side thermionic, SRH

recombination and excess current, do not scale with perimeter rather they scale with the area. For the dimensions compared in Figure 2-10, the area changes significantly compared to the perimeter and hence the PVCR improves as the area is scaled.

2-3. Conclusion

A process flow has been developed which is capable of generating pillars with widths varying from 20µm down to 200nm. For a perimeter normalized current, 40X reduction in the off-state leakage is achieved compared to large pillar TFET devices reported at the IEDM 2010 paper by PennState [59]. The reduction in the off-state leakage is due to the reduction in the bulk parasitic leakage mechanisms such as S-R-H or drain side tunneling. Reduction in I_{OFF} leads to higher I_{ON}/I_{OFF} for the same I_{ON}, steeper switching near I_{OFF} and higher PVCR in the forward side of the gated p-i-n characteristics.

2-4. Implications for Demonstration of Hetero-junction TFETs

The nano-pillar TFET process flow developed for $In_{0.53}Ga_{0.47}As$ Homj TFET can be easily transferred to hetero-junction TFETs. $In_yGa_{1-y}As$ drain and channel layer can be designed to grow on top of $GaAs_{1-x}Sb_x$ source so that the relatively high wet etch undercut property of $In_yGa_{1-y}As$ with citric acid can be exploited to produce the required undercut for self aligned gate deposition. However, as will be shown in the next chapter in the materials growth and characterization sections, not all combinations of $GaAs_{1-x}Sb_x$ / $In_yGa_{1-y}As$ have a naturally occuring lattice matched binary substrate to grow defect free epi-layers. Metamorphic growth using a graded metamorphic buffer such as $In_yAl_{1-y}As$ is required. Metamorphic growth within the MBE requires a lot of growth experience and calibration process. Due to the lack of experienced grower at PennState we chose to grow our wafers at IQE [50].

Chapter 3

Hetero-junction Materials Growth and Characterization

In order to demonstrate the effect of scaling of the effective tunneling barrier height (E_{Beff}) on the on-current and on-off ratio of a tunnel FET, two $In_yGa_{1-y}As$ homo-junction TFETs and two staggered hetero-junction TFETs (HTFETs) using lattice matched combinations of $GaAs_{1-x}Sb_x$ source and $In_yGa_{1-y}As$ channel were designed. Figure 3-1 shows the layer structure and the expected band-alignment for (I) $In_{0.53}Ga_{0.47}As$ homo-junction TFET. Since E_{Beff} = 0.74eV is the largest amongst the four devices considered for comparison, the TFET is termed as 'Large Homj' Design (II) is $GaAs_{0.4}Sb_{0.6}$ source and $In_{0.35}Ga_{0.65}As$ channel staggered HTFET with $E_{Beff} = E_{G(Source)} - \Delta E_C$=0.31eV and (III) $GaAs_{0.35}Sb_{0.65}$ source and $In_{0.7}Ga_{0.3}As$ channel with E_{Beff}=0.25eV. The layer schematics and the band-alignments for the later two structures are shown in Figure 3-2 and 3-3 respectively.

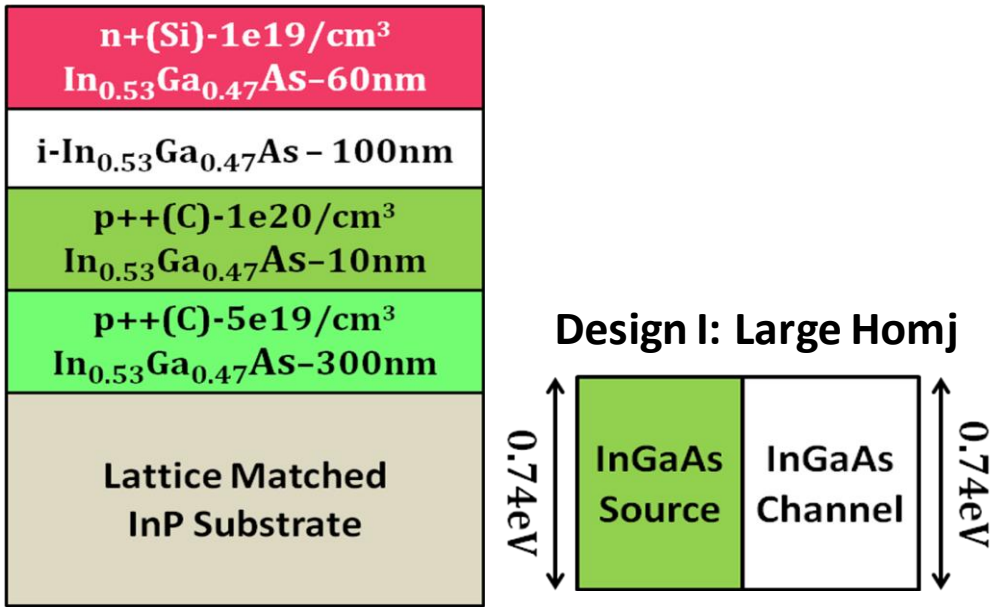

Figure 3-1. $In_{0.53}Ga_{0.47}As$ homo-junction TFET (Large Homj TFET, E_{Beff}=0.74eV) layer structure.

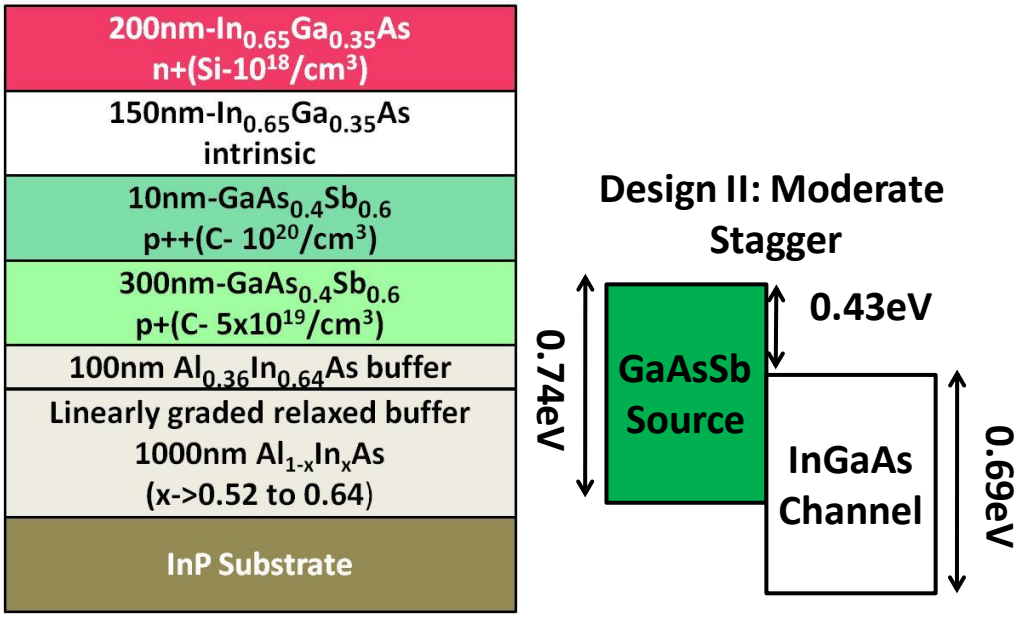

Figure 3-2. $GaAs_{0.4}Sb_{0.6}/In_{0.65}Ga_{0.35}As$ HTFET (Moderate Stagger HTFET, E_{Beff}=0.31eV) layer structure.

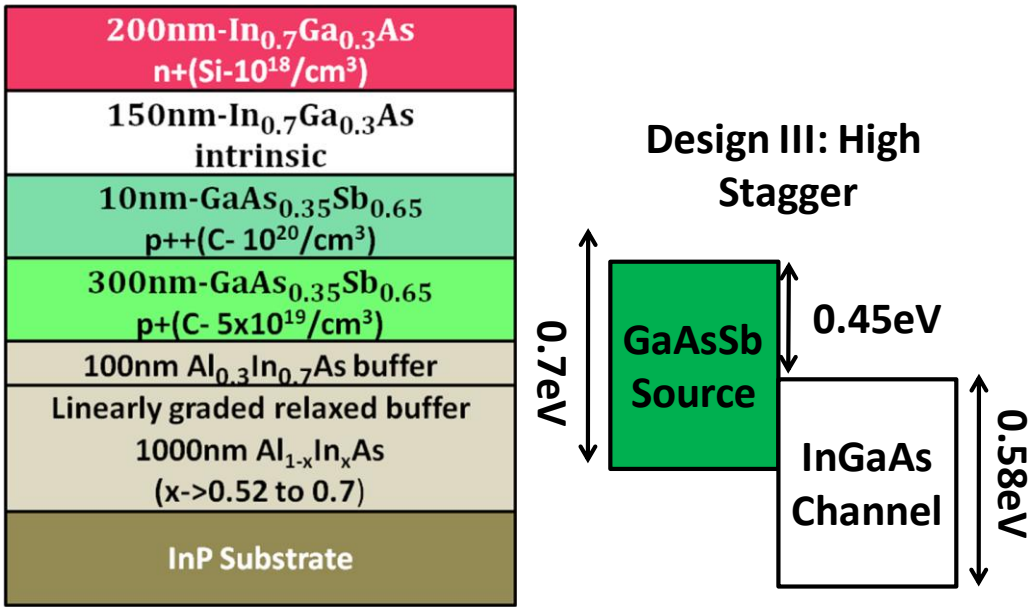

Figure 3-3. (a) $GaAs_{0.35}Sb_{0.65}/In_{0.7}Ga_{0.3}As$ HTFET (High Stagger HTFET, Eb_{eff}=0.25eV) layer structure and (b) band-alignment.

In order to compare the enhancement in drive current over the homo-junction counterpart of the high stagger TFET system, (IV) $In_{0.7}Ga_{0.3}As$ homo-junction TFET was also designed for growth (E_{Beff}=0.58eV). The layer structure and band-gap is shown in Figure 3-4. Due to the progressively reducing E_{Beff}, the IInd design is called "Moderate Stagger" and the IIIrd "High Stagger". Design IV is termed "Small Homj' as the band-gap is smaller than that of Large Homj. The High stagger system is expected to result in the maximum TFET drive current amongst the four since the E_{Beff} is the minimum, however the on-current is not expected to be the absolute best due the finite value of E_{Beff} (0.25eV). E_{Beff} less than 0eV can be achieved with GaAsSb/InAs or GaSb/InAs hetero-junctions. However, as mentioned in section 1-2.2 (D), the aim of this research is to show the worth in moving to staggered hetero-junctions and hence show an improvement in the on-current and on-off ratio simultaneously. As will be shown later within the materials characterization section, switching from an Sb rich to As rich layer is a challenge and any growth issue results in formation of large density of defects or Tamm states making the junction normally on without the application of any applied gate bias [59].

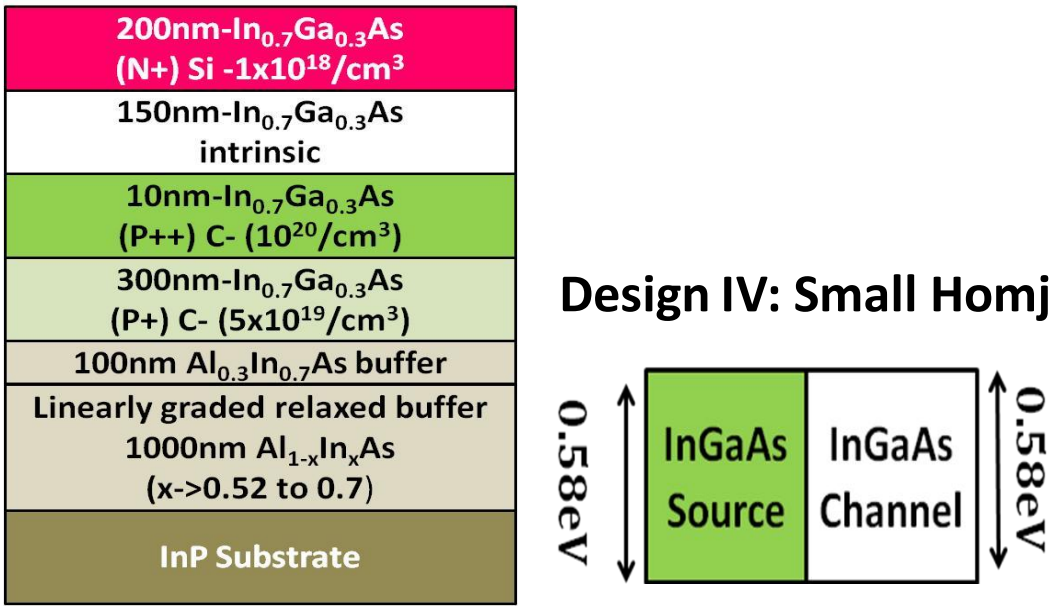

Figure 3-4. $In_{0.7}Ga_{0.3}As$ homo-junction TFET (Small Homj TFET, E_{Beff}=0.58eV) layer structure.

3-1. **Materials Growth and Characterization**

The change of group V fluxes from Sb to As in the mixed anion GaAsSb to mixed cation InGaAs layers can potentially introduce interface intermixing that can lead to uncontrolled layer composition at the interface. While switching from Sb rich source to As rich channel, there is high likelihood of formation of a binary junk, either few mono layers of GaAs or InAs [59]. Strained mono-layers of GaAs is 5.3% lattice mismatched to $In_{0.7}Ga_{0.3}As$, while strained InAs is 1.9% lattice mismatched [38]. While switching if the growth of this binary junk is beyond the critical thickness, then the chances of forming threading dislocations is larger for the GaAs like interface than for InAs like as shown in Figure 3-4 (a,b).

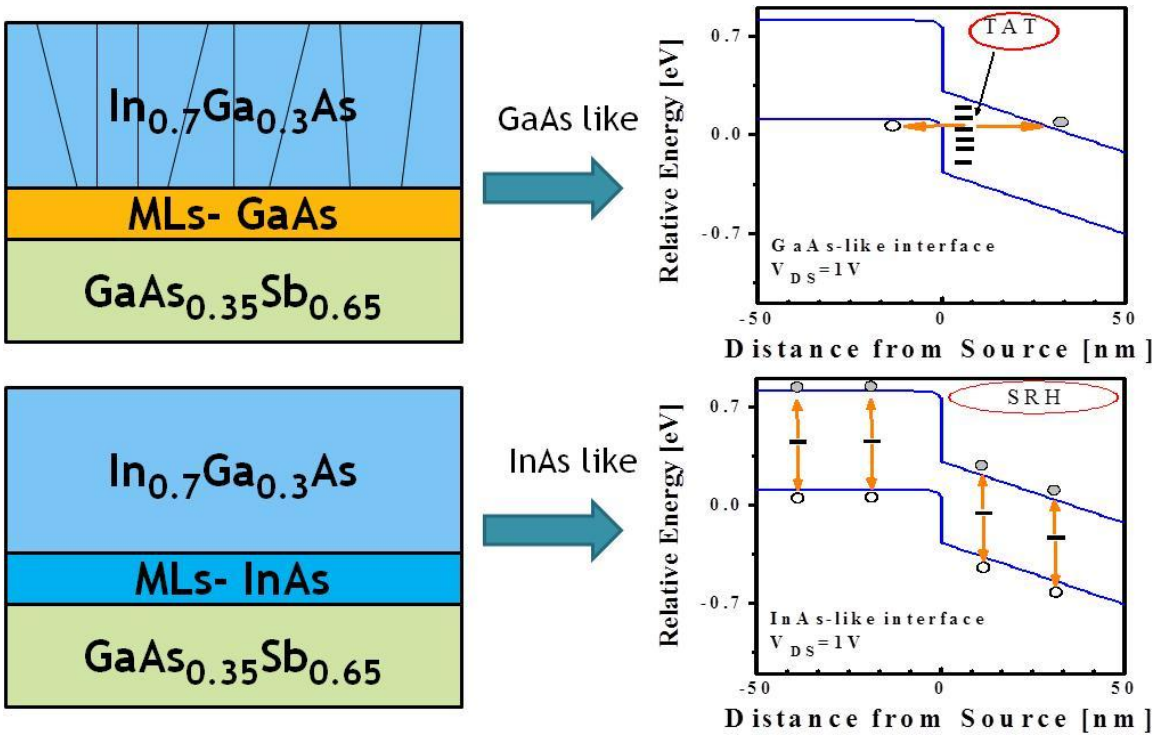

Figure 3-5. Two possible growth scenarios and the resulting quality of GaAsSb/ InGaAs hetero-junction interface. GaAs like interface can result in threading dislocations in the entire InGaAs layer. Large density of interface defects and threading dislocations can result in high off-state leakage due to trap assisted tunneling. InAs like interface on the other hand is more favorable for the growth of nearly dislocation free hetero-junction.

High density of threading dislocations and interface hetero-material intermixing can result in formation of huge amount of interface defects or Tamm states. These states, if present in high density, can result in trap assisted tunneling dominated leakage (Figure 3-5 (c)) opposed to nominal S-R-H generation process if the density is low (Figure 3-5 (d)). Therefore, exploring a proper growth switching sequence and investigating the influence of different atomic termination at the source/channel interface on the mixed As-Sb staggered gap tunnel FET structures is essential.

For illustration, we study this effect of different switching termination on the IIIrd system called High stagger ($GaAs_{0.35}Sb_{0.65}/In_{0.7}Ga_{0.3}As$, E_{Beff}=0.25eV) since this is the system which is expected to deliver maximum drive current amongst the four. Since there is a possibility of formation of GaAs like or InAs like interface while switching from GaAsSb to InGaAs, two different interface terminated wafers were grown. (I) GaAs like interface: In this growth, while switching, the Sb flux was stopped and under As over pressure, the temperature of the Ga cell was ramped up for the growth of InGaAs. (II) InAs like interface: In this growth, while the cell temperature of Ga was ramped up, In was preferentially flown to possibly avoid formation of GaAs junk and form few mono-layers of InAs instead.

The strain relaxation, surface morphology, and defect properties of both kinds of the high stagger TFET structures were characterized using double axis x-ray diffraction (XRD), atomic force microscopy (AFM), and cross-sectional transmission electron microscopy (TEM) respectively. TEM samples were prepared using conventional mechanical thinning procedure followed by Ar ion milling. Reciprocal space maps (RSMs) were obtained using Panalytical X'pert Pro system with Cu Ka1 line x-ray source.

3-2. Reciprocal Space Maps (RSMs)

Both symmetric (004) and asymmetric (115) RSMs were recorded to determine the alloy composition, the lattice mismatch, and the strain relaxation properties. The strain relaxation properties of epitaxial layers can be deduced from the RSMs by relating to the q vectors. In RSMs, the vector q represents the deviation between the reciprocal lattice points (RLPs) of the substrate and epi-layers. There are two components in the q vector, qx and qz, which correspond to the angular splitting ω and 2θ, respectively, in real space. Reciprocal lattice points in RSMs may have different qx and qz positions depending on the degree of relaxation and mis-orientation corresponding to a fully strained (pseudomorphic) substrate or a fully relaxed (metamorphic) buffer layer. For a (115) asymmetric RSM of an ideal, fully relaxed epitaxial layer without tilt, the diffracted intensity from this layer is expected to fall on the fully relaxed line joining the (115) RLP of the substrate and having a 15.8^{o} angle between the (001) and (115) directions. In contrary, a fully strained layer is expected to follow the fully strained line that joins the (115) RLP of the substrate and along the (001) direction.

According to the epi-layer structures shown in Figures 3-3(a), the $In_{0.7}Al_{0.3}As$ uppermost layer of the linearly graded $In_xAl_{1-x}As$ buffer, the $GaAs_{0.35}Sb_{0.65}$ source and the $In_{0.7}Ga_{0.3}As$ channel and drain layers were designed to be internally lattice matched. As a result, the RLPs of each layer should appear at the same peak position in the RSM of these TFET structures. However, due to the residual strain present in these layers, lattice contraction due to heavy C doping [59] and compositional fluctuation during MBE growth, two distinct RLPs along with InP substrate were found in the RSMs of GaAs-like interface structure (Figures 3-6 (a)) and three RLPs in the RSMs of InAs-like interface structure (Figures 3-6 (e)), respectively. In order to certificate RLP of each, wet chemical etching was performed to selectively remove epi-layer one from other. Symmetric (004) RSMs were then successively recorded to assign the RLP of each

layer in these TFET structures. Citric acid/hydrogen peroxide ($C_6H_8O_7$:H_2O_2) at volume ratios of 20:1 and 5:1 were used to selectively etch $In_{0.7}Ga_{0.3}As$ and $GaAs_{0.35}Sb_{0.65}$, respectively. All wet etch experiments were carried out at room temperature. Anhydrous citric acid crystals were dissolved in deionized water (DI H_2O) at the ratio of 1 g $C_6H_8O_7$:1 ml H_2O. The solution was kept more than 12 h prior to wet etch process of TFET structures to ensure complete dissolution and room temperature stability. About 15 min before the wet etch experiment, the above mixed liquid solution (considered as one part of $C_6H_8O_7$) was mixed with 30% hydrogen peroxide (H_2O_2) at the desired volume ratio (x parts $C_6H_8O_7$ to 1 part H_2O_2 by volume). From our measurements, the etch rate for $In_{0.7}Ga_{0.3}As$ using $C_6H_8O_7$:H_2O_2 at volume ratio of 20:1 was 48 nm/min and the selectivity between $In_{0.7}Ga_{0.3}As$ and $GaAs_{0.35}Sb_{0.65}$ layers was found to be ≈50. The InAs like interface TFET structure was etched for 10min to ensure that the $In_{0.7}Ga_{0.3}As$ top layer was completely removed. After symmetric (004) RSM measurement of this etched TFET sample, the same structure was further etched using $C_6H_8O_7$:H_2O_2 at volume ratio of 5:1 for 2 h to remove most of the $GaAs_{0.35}Sb_{0.65}$ layer. The symmetric (004) RSM was performed once again to determine the change of diffraction patterns and assignment of layer peaks. With these measurement results, each layer RLP was precisely assigned. Figure 3-6 (d-f) shows (004) RSMs of InAs-like interface TFET structure (a) before wet etching, (b) etched with $C_6H_8O_7$:H_2O_2 at volume ratio of 20:1 for 10min, and (c) etched with $C_6H_8O_7$:H_2O_2 at volume ratio of 5:1 for another 2 h. All the peak positions and materials compositions were labeled in this figure. Similarly, wet etch process was performed on the GaAs-like TFET structure and Figure 3-6 (a-c) shows the symmetric (004) RSMs of this structure. Unlike InAs-like interface structure, $In_{0.7}Ga_{0.3}As$ and $GaAs_{0.35}Sb_{0.65}$ layers in GaAs like interface structure were merged together due to higher degree of strain relaxation of the $In_{0.7}Ga_{0.3}As$ layer. As a result of removing the top $In_{0.7}Ga_{0.3}As$ cap layer, the RLP position of the remaining $GaAs_{0.35}Sb_{0.65}$ layer was shifted compared with the combined contour of $In_{0.7}Ga_{0.3}As$ and $GaAs_{0.35}Sb_{0.65}$ prior to wet etching.

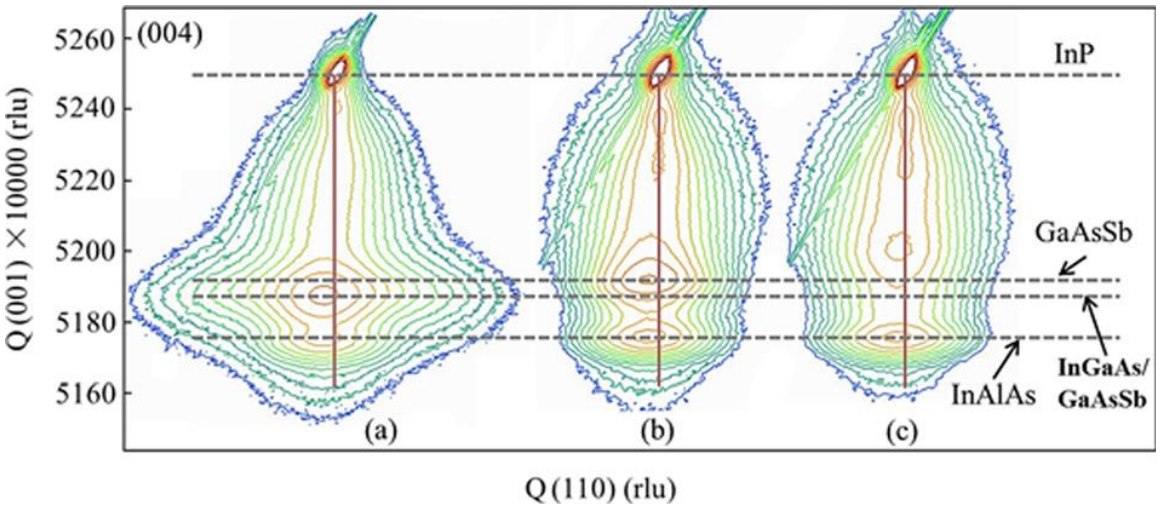

Figure 3-6. (a) Symmetric Reciprocal Space Map of GaAs like interface structure recorded along (004). The first contour is recorded on the as grown structure. (b) The second contour is without the top InGaAs layer. (c) The third contour is without the GaAsSb layer. The peak corresponding to the InGaAs layer is stretched along all directions indicating presence of dislocations.

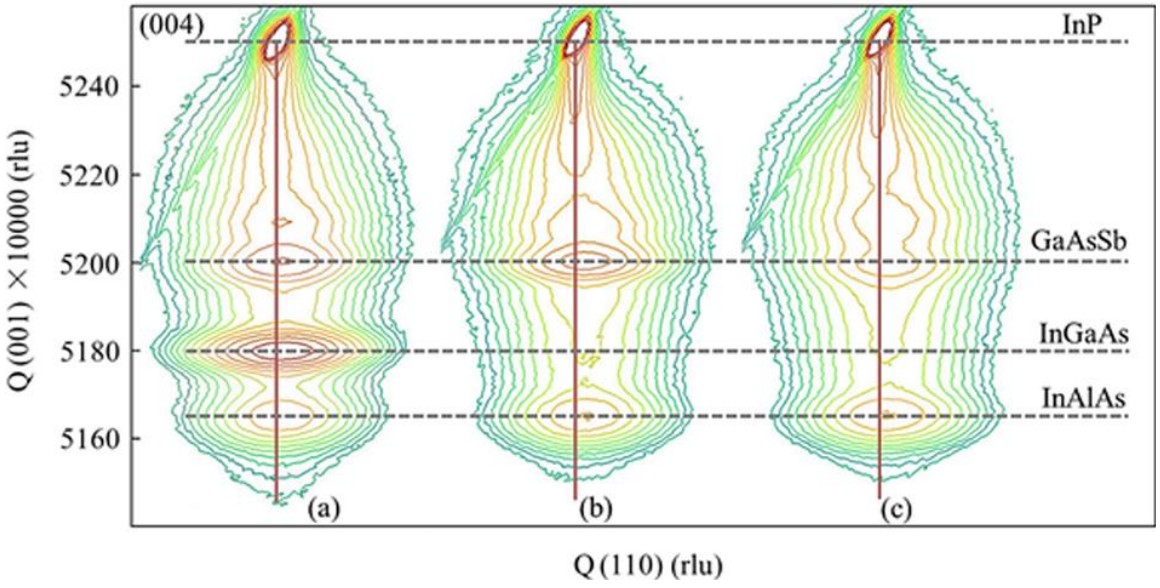

Figure 3-7. (a) Symmetric Reciprocal Space Map of GaAs like interface structure recorded along (004). The first contour is recorded on the as grown structure. The second contour is without the top InGaAs layer. The third contour is without the GaAsSb layer. The peaks corresponding to all layers are distinct and sharper than the GaAs like interface indicating improved growth quality.

3-2.1. GaAs-like interface TFET structure

The relaxation state of the upper part of the linearly graded $In_xAl_{1-x}As$ buffer has a significant role for the internally lattice mismatched active layer in As and Sb based TFET structures. From both (004) and (115) RSMs, the strain relaxation value of the uppermost $In_{0.7}Al_{0.3}As$ layer of the linearly graded buffer with respect to InP substrate was found to be 69% along the [110] direction, which corresponds to a misfit strain of 1.15%. The strain relaxation value obtained from our measurement of the uppermost $In_{0.7}Al_{0.3}As$ layer is consistent with the results obtained by other researchers on the uppermost layer of linear graded $In_xAl_{1-x}As$ buffer. From the asymmetric (115) RSMs of the GaAs-like interface TFET structure as shown in Figure 3-8, the RLP of $GaAs_{0.35}Sb_{0.65}$/ $In_{0.7}Ga_{0.3}As$ layers followed the fully relaxed line (the deep blue dashed line), indicating nearly full relaxation of these two layers with respect to the InP substrate.

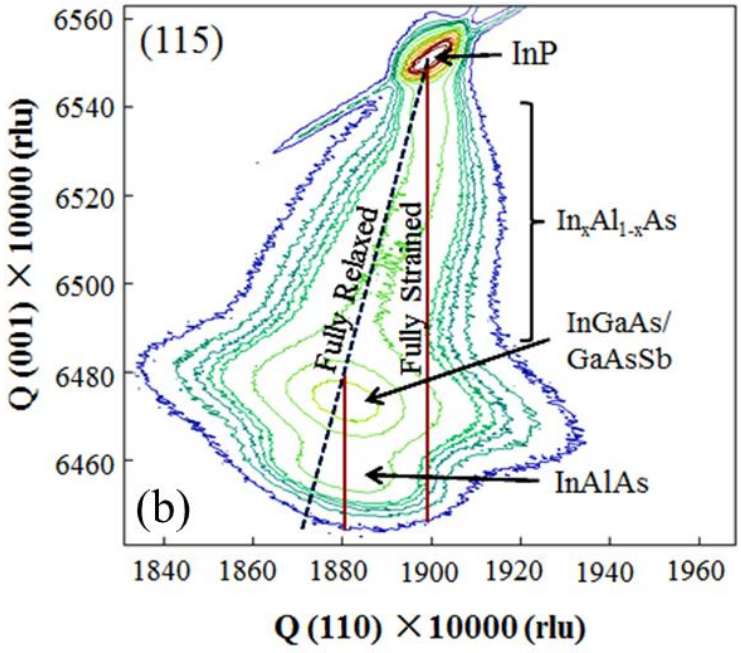

Figure 3-8. Asymmetric (115) RSMs of GaAs-like interface TFET structure using an incident beam along [110] direction.

The percentage of strain relaxation of these two layers with respect to InP was found to be 91%, within the relative experimental error. Since both the epilayers on top of InAlAs virtual substrate follow the fully relaxed line, two inferences can be deduced regarding their growth. Either both of them contain severe dislocations or the top InGaAs layer is full of dislocations resulting in merging and broadening of the two peaks and the location of the combined peak measured close to that of the fully relaxed line. However, when the top InGaAs layer is etched off, the peak position of the GaAsSb can be distinguished and shifts close to the InAlAs virtual substrate. The degree of relaxation of the GaAsSb peak is 80%, which is lower than their combined peak relaxation of 94%, indicating that the InGaAs epilayer grown on GaAsSb is defective due to generation of misfit and threading dislocations.

3-2.2. InAs like interface

Comparing Figure 3-8 with Figures 3-6 (d), a distinct $In_{0.7}Ga_{0.3}As$ RLP was observed in the RSM of the InAs-like interface structure unlike the combined RLPs of both $GaAs_{0.35}Sb_{0.65}$ and $In_{0.7}Ga_{0.3}As$ layers for the GaAs-like interface TFET structure. The out-of-plane and in-plane lattice constants with the incident beam along [110] direction were 5.9481A ° and 5.9168A ° , respectively, corresponding to the strain relaxation value of 76%. This value is less than that of $In_{0.7}Ga_{0.3}As$ layer in the GaAs-like interface structure. The lower value of strain relaxation indicates reduced dislocation density in the $In_{0.7}Ga_{0.3}As$ layer, which could be further supported from the shorter elongation of $In_{0.7}Ga_{0.3}As$ RLP. The RLP maxima from $In_{0.7}Ga_{0.3}As$ layer in the InAs-like interface TFET structure appears in between the fully strained line (red solid line) and the fully relaxed line (blue dashed line) as shown in Figure 3-9. This indicates that the $In_{0.7}Ga_{0.3}As$ layer is pseudomorphic in nature. Although, the in-plane lattice constant of $In_{0.7}Ga_{0.3}As$ layer is higher than the lattice constant of $GaAs_{0.35}Sb_{0.65}$ layer, the small difference in lattice constant does not generate strain relaxation of the $In_{0.7}Ga_{0.3}As$ layer due to the critical layer

thickness consideration. It should also be noted that the apparent change of RLP position of $GaAs_{0.35}Sb_{0.65}$ with respect to the $In_{0.7}Ga_{0.3}As$ could be due to the lattice contraction due to heavy C doping inside the $GaAs_{0.35}Sb_{0.65}$ layer. From the measured in- plane and out-of-plane

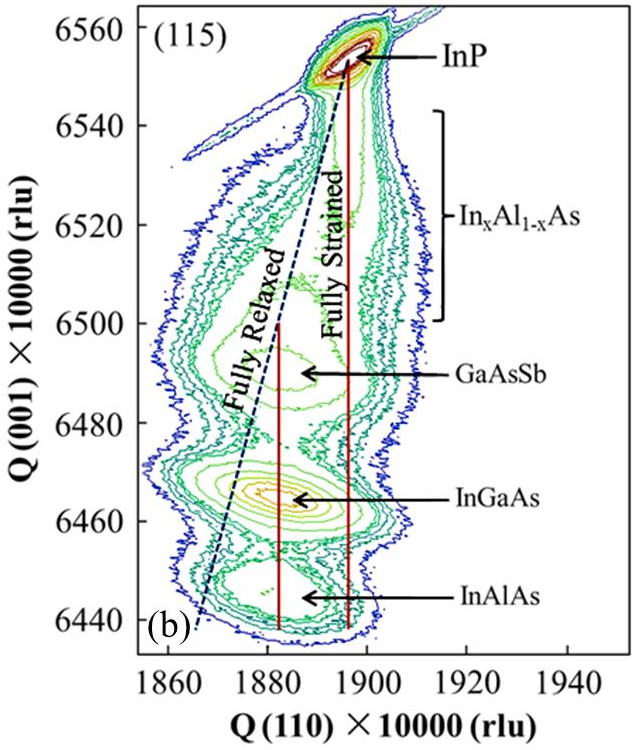

Figure 3-9. Asymmetric (115) RSMs of InAs-like interface TFET structure using an incident beam along (110) direction.

lattice constants, only 4% strain relaxation was expected in the $In_{0.7}Ga_{0.3}As$ layer with respect to the $GaAs_{0.35}Sb_{0.65}$ layer. The pseudomorphic characteristic of the $In_{0.7}Ga_{0.3}As$ layer indicates the lower dislocation density at the $GaAs_{0.35}Sb_{0.65}$ /$In_{0.7}Ga_{0.3}As$ interface or within the $In_{0.7}Ga_{0.3}As$ layer. Therefore, the InAs-like interface TFET structure creates a "virtually" defect-free active region compared to GaAs-like interface TFET structure, which is desirable for improving the performance of TFET devices with lower OFF state p-i-n leakage and higher I_{ON}/I_{OFF} ratio.

3-3. Surface morphology

It is important to characterize the surface morphology (roughness, other possible features) for metamorphic TFET structures due to the expected crosshatch resulting from ideal strain relaxation with minimum concentrations of threading dislocations, as this is an important figure of merit. Surface morphology of the two TFET structures was examined by AFM in contact mode. The 20 μmx20μm AFM micrographs of these two structures and related line profiles in two orthogonal [110] directions is shown in Figure 3-10 (a-d). For InAs like structure, the anticipated two dimensional crosshatch pattern is uniform and well-developed, indicating nearly ideal graded buffer. Crosshatch pattern shows a characteristic undulating morphology with hills and valleys parallel to the intersection of slip planes with the crystal surface [60]. In our case, the undulating surface morphology exhibits ridges and grooves parallel to the [110] direction on the surface. The peak-to-valley height from line profiles in the two orthogonal [110] direction is also included in these figures. The uniform distribution of the crosshatch pattern from [110] directions for the InAs-like interface TFET structure suggests a symmetric relaxation of the linearly graded buffer layer, which is in agreement with the XRD results. The AFM micrograph of the InAs-like interface structure shows a smooth surface morphology with surface rms roughness of 3.17 nm. Compared to the surface morphology of InAs-like interface, the GaAs-like interface structure does not exhibit two-dimensional crosshatch surface morphology. A grainy texture dispersed across the surface was observed from the AFM micrograph of the GaAs-like interface structure. From the line profiles along [110] direction, the peak-to-valley height of GaAs-like interface sample is 3 times higher than the InAs-like interface structure, indicating a significantly poor

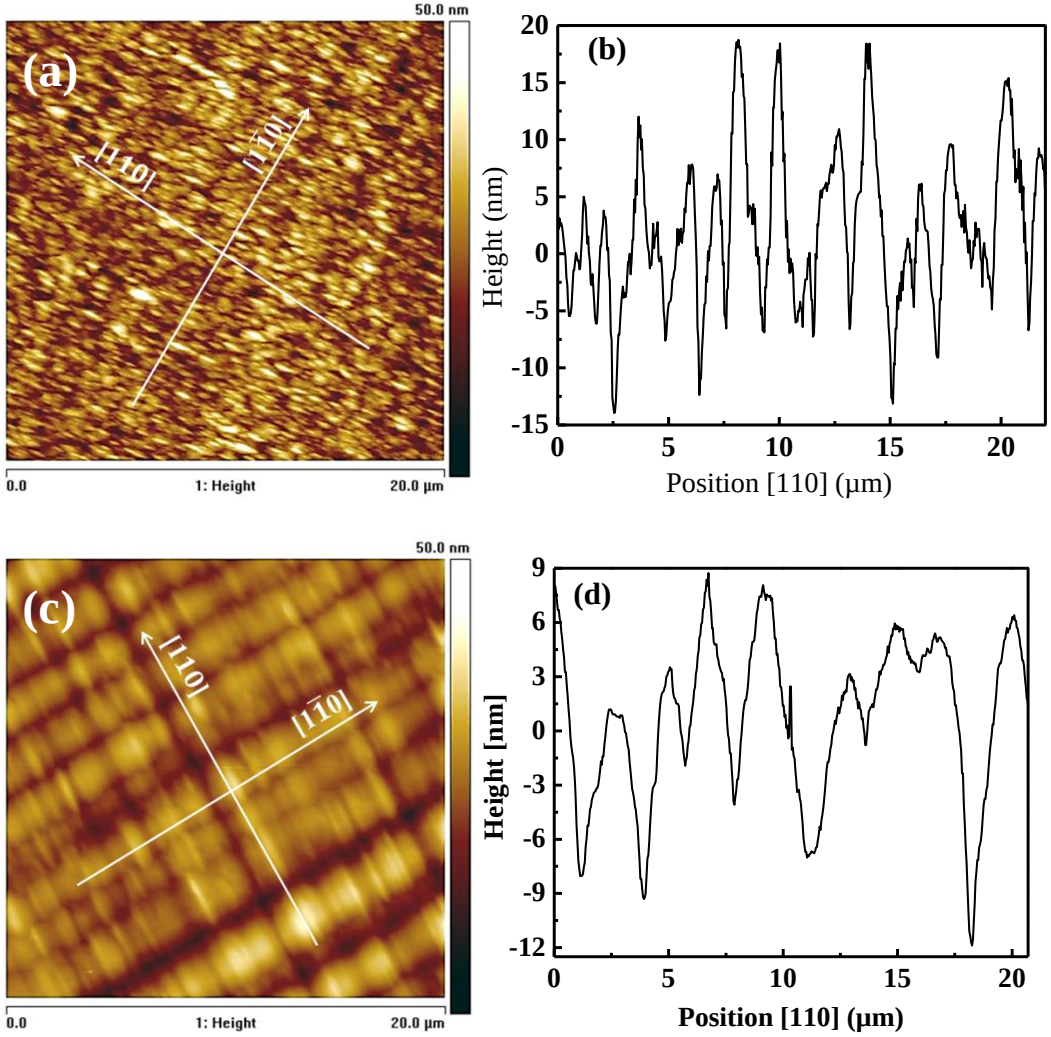

Figure 3-10. 20µm×20µm AFM surface morphology and line profiles in two <110> directions of the (a-b) GaAs and (c-d) InAs-like interface TFET structure. The micrograph show typical cross-hatch pattern with *rms* roughness of 3.17nm for the InAs like interface structure while grainy morphology with rams of 4.46nm for the GaAs like interface structure.

surface quality due to the large amount of dislocation embedded within the TFET structure. The surface rms roughness of the GaAs-like interface sample is 4.46 nm. The rough surface and deterioration of the two-dimensional cross-hatch pattern on the surface of GaAs-like interface structure should be attributed to the higher dislocation density of the $In_{0.7}Ga_{0.3}As$ layer introduced by the GaAs-like interface, which was confirmed by the broadening of the RLP during x-ray

measurement as discussed earlier in this paper. From the AFM micrographs of these two structures, it can be concluded that the InAs-like surface structure shows a much better surface morphology with typical two-dimensional cross-hatch patterns and lower peak-to-valley height corresponding to a reduced rms roughness than those of the GaAs-like interface structure.

3-4. Dislocation and Defects

Further insight into the structural properties of the GaAs-like interface and InAs-like interface TFET structures is provided by cross-sectional TEM analysis. Figures 3-11 (a) and (b) show cross-sectional TEM micrographs of the GaAs-like interface and InAs-like interface structures, respectively. All the layers were labeled in these figures and the $GaAs_{0.35}Sb_{0.65}/In_{0.7}Ga_{0.3}As$ hetero-interface was denoted by an arrow in each micrograph. One can find from these figures that the dislocations due to the substrate mismatch were confined within the the linearly graded $In_xAl_{1-x}As$ buffer layer. The uppermost region of the graded $In_xAl_{1-x}As$ buffer of thickness about 200nm has minimal dislocation and not observed at this scale. As evidenced in the literature that the linearly graded buffer appears to have advantages of spreading the misfit dislocations with depth throughout the layer, it is supposed to leave less residual strain on the top of the buffer layer. Since near to the top of linear grades, where the residual strain is significantly small, no further relaxation will take place, leaving a strained and dislocation-free region at the top of the linearly graded buffer. No threading dislocations are observable in the $GaAs_{0.35}Sb_{0.65}$ layers grown on the linearly graded $In_xAl_{1-x}As$ buffers in both of the two structures, indicating that the $In_xAl_{1-x}As$ linearly graded buffer effectively accommodates the lattice mismatch between the active layer and the InP substrate and thus provides a high-quality virtual substrate for the TFET structures. It can be seen from Figure 3-11 (a) that the $In_{0.7}Ga_{0.3}As$ layer of the GaAs-like interface TFET structure is full of threading dislocations. Threading dislocations were generated from the interface of $GaAs_{0.35}Sb_{0.65}$ and $In_{0.7}Ga_{0.3}As$ and went all the way up until

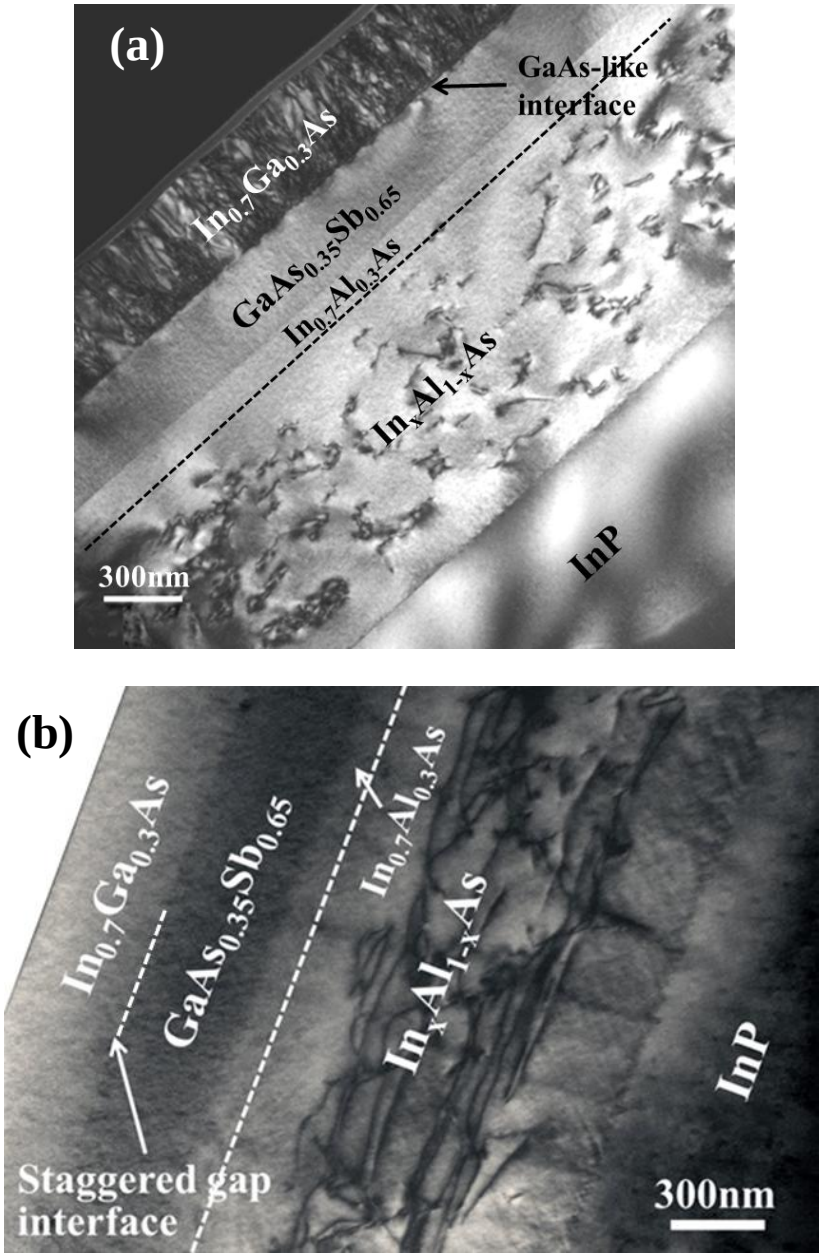

Figure 3-11. Cross-sectional TEM micrograph of the GaAs-like and InAs like interface TFET structures. High threading dislocation density is shown in the $In_{0.7}Ga_{0.3}As$ layer of the GaAs like interface structure due to improper switching conditions.

the end of the structure. The dislocation density in the $In_{0.7}Ga_{0.3}As$ layer was too high to be quantified. As no dislocations were observed from the bottom $GaAs_{0.35}Sb_{0.65}$ layer on which the $In_{0.7}Ga_{0.3}As$ was grown, it was reasonable to conclude that the GaAs-like interface contributed to

the high dislocation density in the $In_{0.7}Ga_{0.3}As$ layer and it is consistent with the XRD analysis discussed above. Moreover, it is also clear that the poor surface morphology of the GaAs-like interface TFET structure from AFM measurement and the elongation of the RLP in RSMs are due to a very high defect density present in the top $In_{0.7}Ga_{0.3}As$ layer, as observed by cross-sectional TEM. On the other hand, no threading dislocations were observed in the top $In_{0.7}Ga_{0.3}As$ layer of the InAs-like interface TFET structure at this magnification, indicating a threading dislocation density (TDD) in this layer on the order of or below $10^7/cm^2$.

3.5. Band-offset Characterization using XPS

XPS measurements provide binding energy information about the core level and the valence electrons emitting from each layer structure. This allows determination of ΔE_V of $In_{0.7}Ga_{0.3}As$ channel relative to $GaAs_{0.35}Sb_{0.65}$ source. XPS spectra were collected from the following three samples: i) 150nm $In_{0.7}Ga_{0.3}As$/310nm $GaAs_{0.35}Sb_{0.65}$, ii) 5nm $In_{0.7}Ga_{0.3}As$/310nm $GaAs_{0.35}Sb_{0.65}$ and iii) 310nm $GaAs_{0.35}Sb_{0.65}$ without the top $In_{0.7}Ga_{0.3}As$ layer for both GaAs interface type as well as InAs interface type. The ΔE_V can be determined using the following equation:

$$\Delta E_v = \left(E^{GaAsSb}_{Sb3d_{5/2}} - E^{GaAsSb}_{VBM}\right) - \left(E^{InGaAs}_{In3\,d_{5/2}} - E^{InGaAs}_{VBM}\right) - \Delta E_{CL} \quad (3\text{-}1)$$

where $E^{GaAsSb}_{Sb3d_{5/2}}$ and $E^{InGaAs}_{In3\,d_{5/2}}$ are CLs of $Sb3d_{5/2}$ and $In3d_{5/2}$ from thick $GaAs_{0.35}Sb_{0.65}$ and thick $In_{0.7}Ga_{0.3}As$ film surfaces, respectively; E_{VBM} is the valence band maximum (VBM) of the corresponding samples and it can be determined by linear extrapolation of the leading edge of valence band (VB) spectra to the base lines in order to account for the finite instrument resolution;

$\Delta E_{CL} = (E_{Sb3d_{5/2}}^{InGaAs/GaAsSb} - E_{In3d_{5/2}}^{InGaAs/GaAsSb})$ is the energy difference between $Sb3d_{5/2}$ and $In3d_{5/2}$ CLs which are measured at the $In_{0.7}Ga_{0.3}As/GaAs_{0.35}Sb_{0.65}$ hetero-interface. Figure 3-12 (a-f) shows the CL and VB spectra from each sample. In order to improve the accuracy of measured binding energy, curve fitting was performed on each CL spectra to distinguish Sb-O and In-O bonds from Sb-Ga and In-As bonds. The Sb-O and In-O bonds were found to be around 530.0eV and 444.9eV, respectively, which were consistent with the reported values [61][62]. It should be noted that different from the $In3d_{5/2}$ CL spectra, which is a combination of In-O and In-As bond peaks, the Sb-O bond is resolved from the $Sb3d_{5/2}$ CL as a separate peak (not shown in Fig. 3-12(a)). As a result, the $Sb3d_{5/2}$ spectra from thick $GaAs_{0.35}Sb_{0.65}$ sample is Lorentzian shape without any curve fitting. The results show that the values of $\left(E_{Sb3d_{5/2}}^{GaAsSb} - E_{VBM}^{GaAsSb}\right)$, $\left(E_{In3d_{5/2}}^{InGaAs} - E_{VBM}^{InGaAs}\right)$ and ΔE_{CL} are 527.707eV, 443.784eV and 83.525eV, respectively. The valence band offset of $In_{0.7}Ga_{0.3}As$ channel relative to $GaAs_{0.35}Sb_{0.65}$ source is 0.398 ± 0.05eV using Eq. (3-1). The uncertainty value of 0.05eV is from the scatter of VB data with respect to the fitting in VBM positions. The conduction band offset (ΔE_c) can be estimated by the following equation:

$$\Delta E_c = E_g^{GaAsSb} + \Delta E_v - E_g^{InGaAs} \quad (3\text{-}2)$$

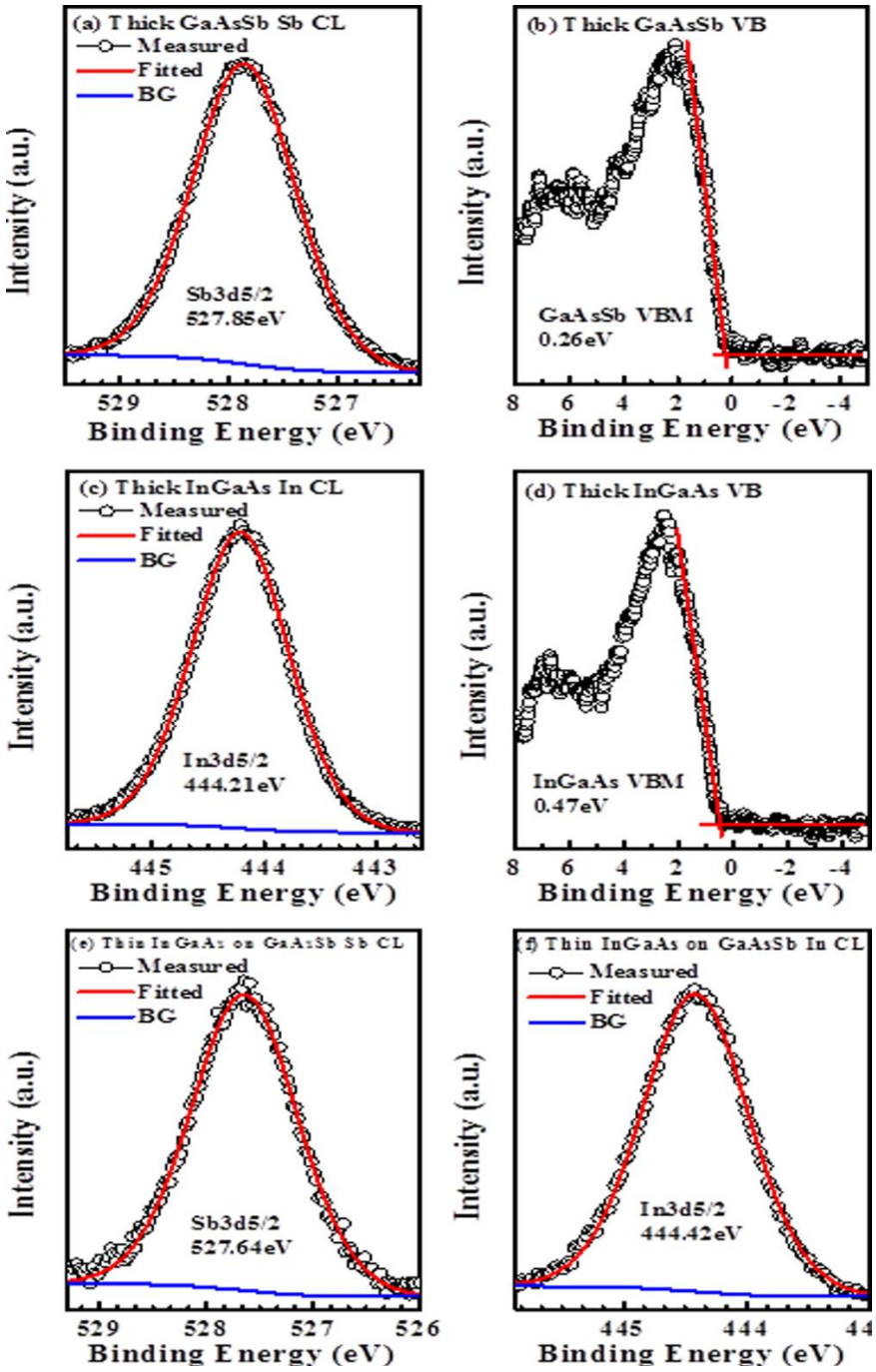

Figure 3-12. XPS spectra of (a) Sb3d5/2 CL and (b) $GaAs_{0.35}Sb_{0.65}$ VB from 310 nm $GaAs_{0.35}Sb_{0.65}$ without the top $In_{0.7}Ga_{0.3}As$ layer; (c) In3d5/2 CL and (d) $In_{0.7}Ga_{0.3}As$ VB from 150nm $In_{0.7}Ga_{0.3}As$ /310 nm $GaAs_{0.35}Sb_{0.65}$; (e) Sb3d5/2 CL and (f) In3d5/2 CL from 5 nm $In_{0.7}Ga_{0.3}As$/310nm $GaAs_{0.35}Sb_{0.65}$ structure measured at the hetero-interface of structure A. CL spectra curves were fitted using a Lorentzian convolution with a Shirley-type background. VBM were determined by linearly fitting the leading edge of the VB spectra to the base line.

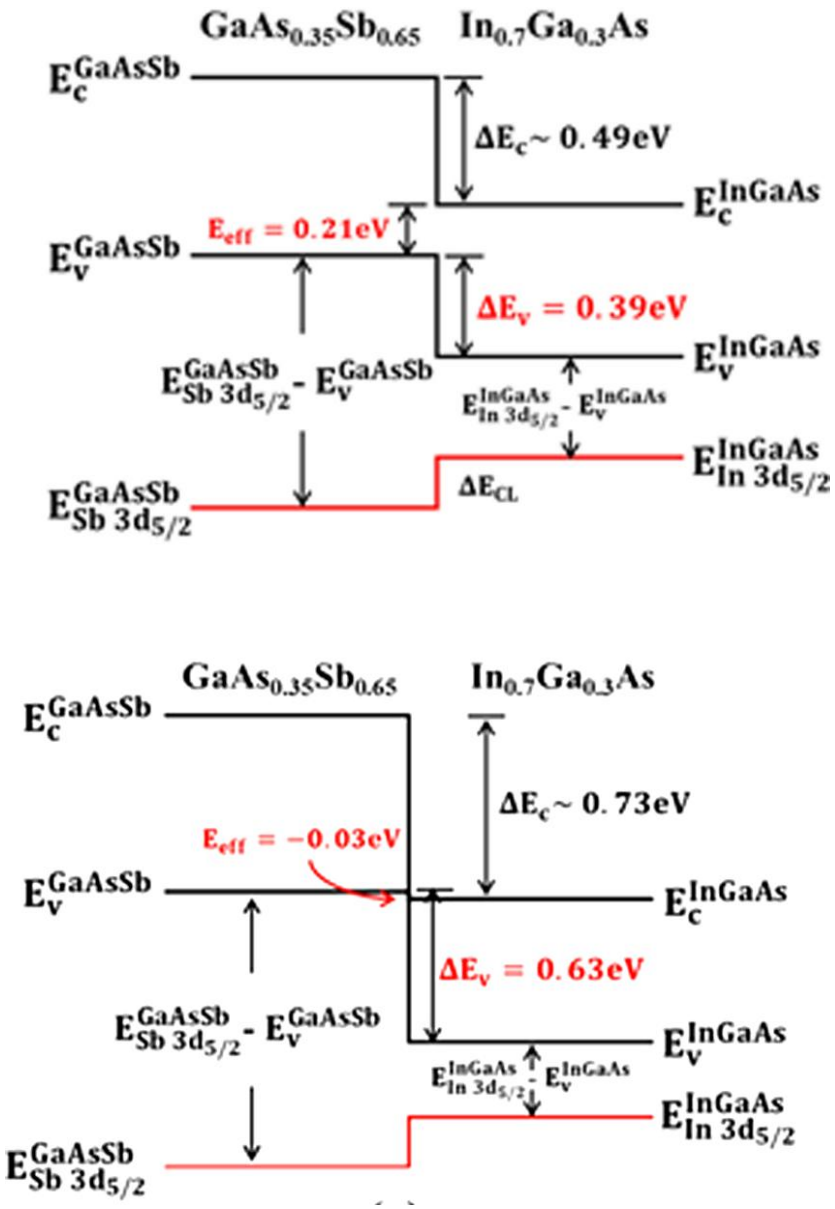

Figure 3-13. Derived band-alignment for the InAs like (top) and GaAs like (bottom) interface TFET structures. Band-gap narrowing due to heavy doping in III-V has been considered. InAs like TFET structures result in E_{Beff}=0.202eV, while GaAs like TFET structure is broken due to presence of high density of gap states.

where E_g^{GaAsSb} and E_g^{InGaAs} are the band gap of heavily doped $GaAs_{0.35}Sb_{0.65}$ and intrinsic $In_{0.7}Ga_{0.3}As$. The bandgap of P^{++} $GaAs_{0.35}Sb_{0.65}$ was found to be 0.703eV by simulation [38], where Jain-Roulston model [63] was used to calculate band-gap-

narrowing effect caused by heavily carbon doping. The bandgap of measured intrinsic $In_{0.7}Ga_{0.3}As$ material is 0.6eV [64]. Using these data, the ΔE_C is calculated to be ~ 0.501eV. Figure 3-13 shows the schematic band alignment diagram of the $GaAs_{0.35}Sb_{0.65}/In_{0.7}Ga_{0.3}As$ hetero-junction based on the present results above. A type-II staggered band lineup is seen to have formed at the source/channel interface of the TFET structure. The effective tunneling barrier height ($Eb_{eff} = E_g^{InGaAs} - \Delta E_v$) is found to be 0.202eV.

3-6. Comparison of OFF state current of TFET devices with InAs-like and GaAs-like interface at source/channel region

In order to assess the impact of the difference between InAs-like and GaAs-like interface on the OFF state leakage current of the HTFET, p-i-n devices were fabricated on both the samples. Room temperature p-i-n curves and the comparison is shown in Figure 3-14 (a). About four orders of magnitude higher leakage current density was observed from the GaAs-like interface structure than the InAs-like at 300 K, indicating different OFF state current mechanisms involved in these TFET structures. In order to gain insight into the mechanism governing them, temperature dependent I-V measurements were performed in the reverse-mode, with temperature ranging from 150K to 300K. The measured and modeled curves for the GaAs like and the InAs like structures are shown in Figure 3-14 (b) and (c) respectively. For modeling, device simulations were performed using TCAD Sentaurus. A list of parameters used for the simulations is provided in Table II. In both the structures, the source (P+) has been heavily doped, hence band-gap narrowing model was activated.

The reverse leakage for the GaAs like interface is four orders of magnitude higher than the InAs like interface and the temperature dependence is weak. High current and weak temperature dependence indicate trap assisted tunneling dominating the (TAT) transport. To

explain why the TAT dominates the OFF state transport of the GaAs-like interface, fixed positive charges representative of interface defects or Tamm states were introduced into the simulation of

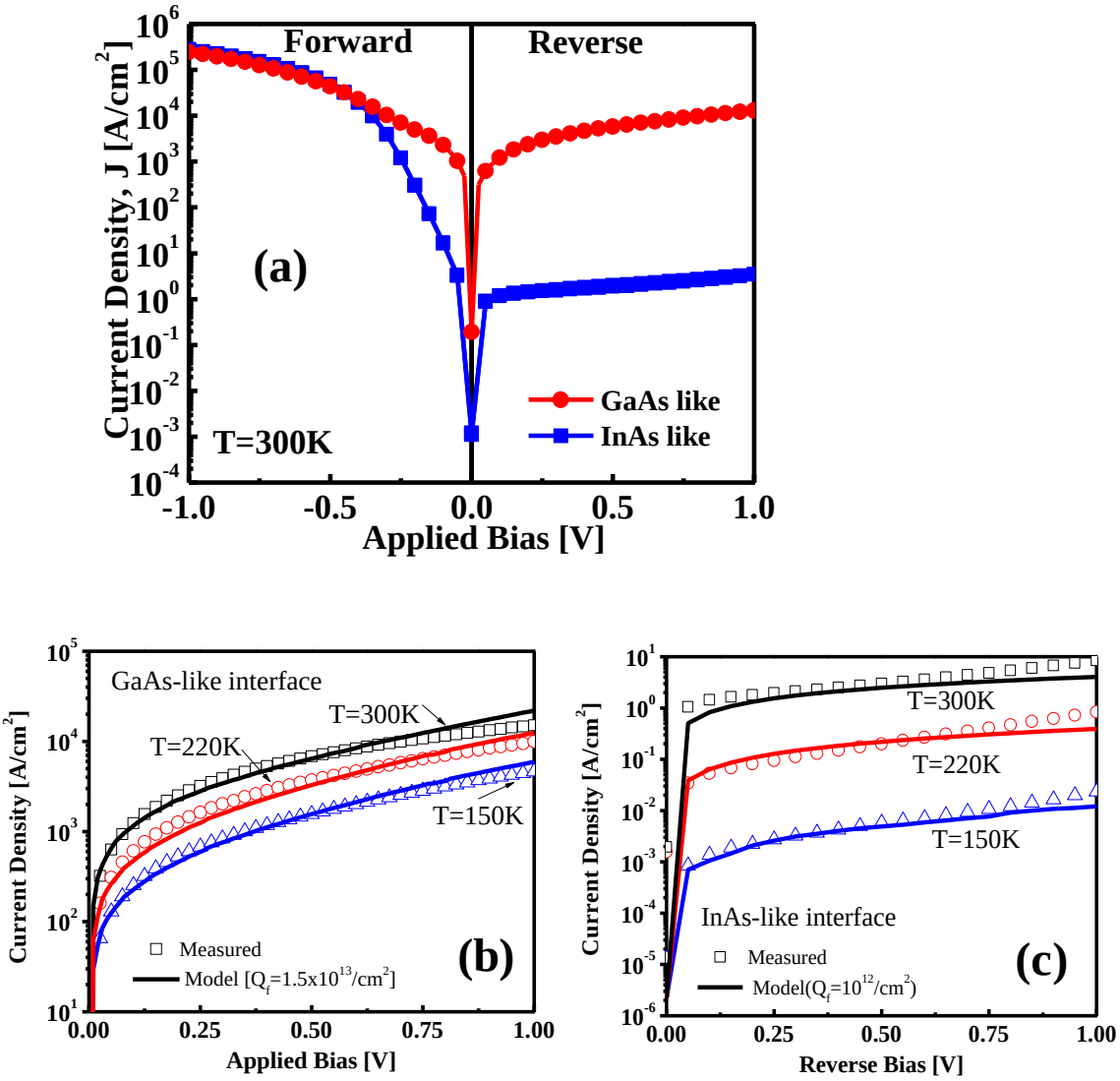

Figure 3-14. (a) Comparison of the ungated pin diode characteristics of the GaAs like and InAs like High Stagger HTFET layers. (b-c) Temperature dependent reverse leakage current density of the GaAs like and InAs like HTFET structures along with modeled curves.

the ideal structure. While fixed positive charge of 10^{12}/cm^2 was required for the InAs like interface, the GaAs like interface required 1.5x10^{13}/cm^2 of fixed charge in order to model the four

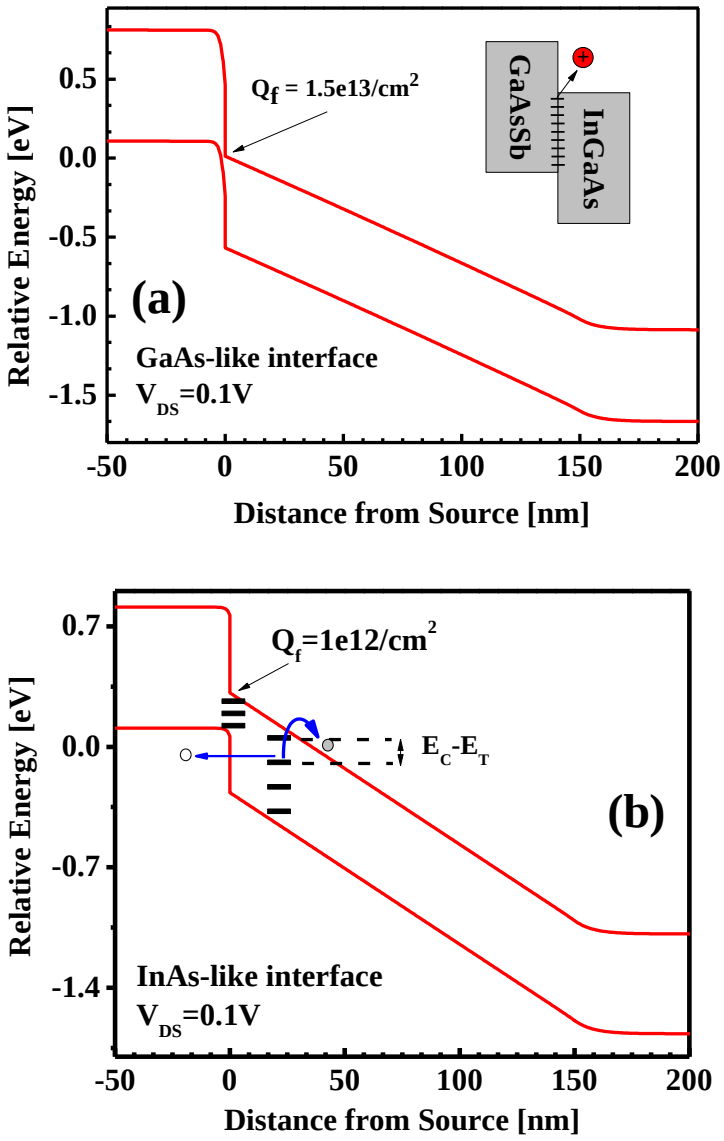

Figure 3-15. (a) Band-diagram showing $1.5x10^{13}/cm^2$ of equivalent fixed charge density required to change the band-alignment from expected staggered hetero-junction to broken gap structure. (a) InAs like structure is expected to have fixed charge density less than $10^{12}/cm^2$.

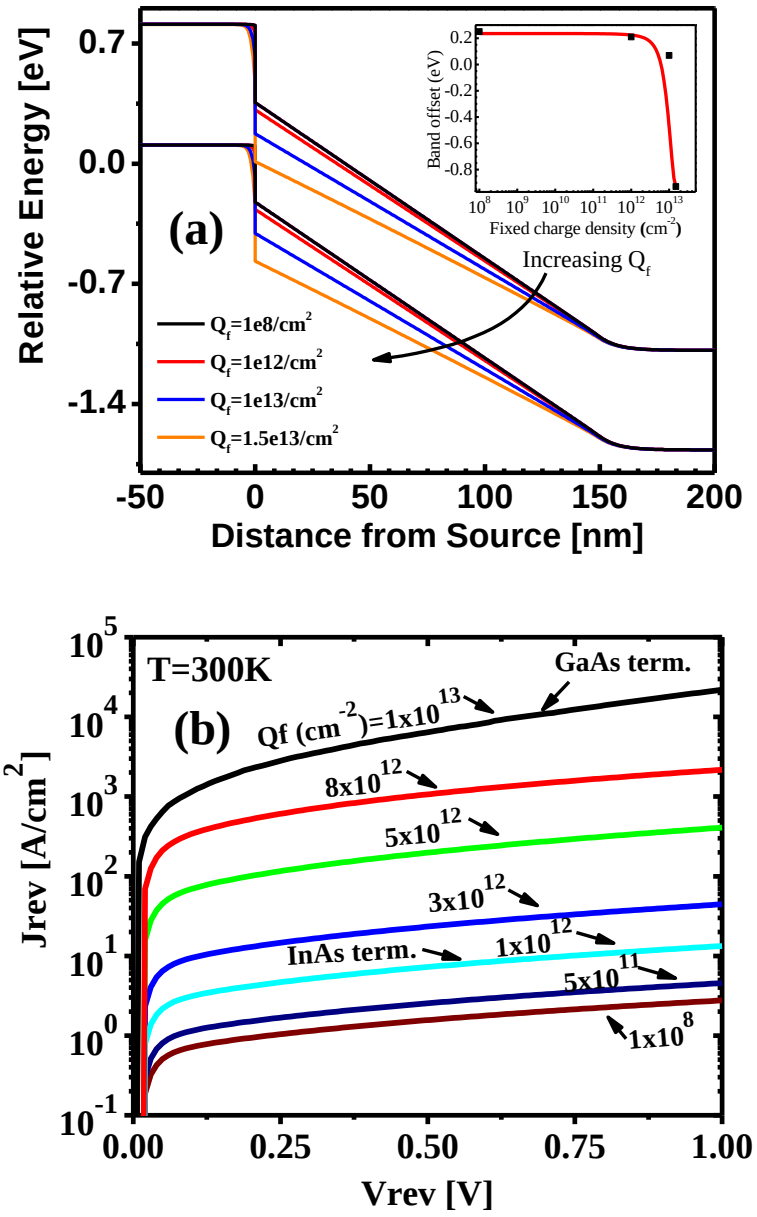

Figure 3-16. (a) Change in band bending as a function of density of fixed charge at the hetero-interface. (b) p-i-n reverse current density as a function of fixed charge density. The reverse leakage changes from trap assisted tunneling to S-R-H generation for densities lower than $5x10^{11}/cm^2$.

orders higher tunneling leakage. Such high value of the fixed charge causes severe band-bending of the channel near the hetero-interface making the junction E_{Beff}≈0eV. Also, such a high density of interface defects is representative of presence of huge density of junk induced defects, dislocations, hetero material intermixing which has already been confirmed from the RSM, AFM and TEM studies. In order to evaluate the dependence of the band-bending and hence the reverse current on the interface fixed charge density, Q_F was varied from $1.5x10^{13}/cm^2$ down to $10^8/cm^2$ (typical for a growth with very low defect density). Clearly, if the interface state density can be brought below $10^{11}/cm^2$, the contribution to the off-state leakage from the Tamm states or interface defects will become much lower compared to the bulk S-R-H generation mechanism.

3-7. Conclusion

In order to show the effect of decreasing effective barrier height on the on-current, Large Homj TFET with E_{Beff}=0.74eV, Small Homj TFET with E_{Beff}=0.58eV, Moderate stagger HTFET with E_{Beff}=0.31eV and High stagger TFET with E_{Beff}=0.25eV were designed for growth using MBE. For staggered HTFET growth, while switching between 'Sb' rich GaAsSb to 'As' rich InGaAs, possibility of intermixing and growth of binary junk like GaAs or InAs is evaluated. GaAs junk originate under 'As' overpressure, while InAs mono layers result from the preferential flow of 'In' during the switching process. For this study, high stagger $GaAs_{0.35}Sb_{0.65}$/ $In_{0.3}Ga_{0.7}As$ wafers with both hetero-interface types were characterized for strain relaxation using reciprocal space maps, surface morphology using Atomic Force Microscopy and confirmation of defects and dislocations using Transmission Electron Microscopy. All the three techniques signified existence of threading dislocations in $In_{0..3}Ga_{0.7}As$ channel and the drain layers for the GaAs like interface compared to the InAs like structure. TEM confirmed the existence of the defects at the interface as well as within the bulk of the $In_{0.3}Ga_{0.7}As$ layer while the virtual InAlAs substrate and the $GaAs_{0.35}Sb_{0.65}$ source layers being free of noticeable dislocations or defects. Finally, the temperature dependent reverse pin diode current density were measured and numerically modeled for both the type of TFET structures. Four orders higher reverse current density and the weak temperature dependence for the GaAs like interface indicated trap assisted tunneling determining the off-state leakage compared while the InAs like interface being dominated by low level S-R-H generation mechanism. The band-offset for the GaAs is nearly broken as confirmed by XPS and modeling, where as for the InAs like the band-offset follows near ideal growth, considering the effect of band-gap narrowing. Thus, InAs terminated hetero-interface $GaAs_{0.35}Sb_{0.65}$/ $In_{0.3}Ga_{0.7}As$ staggered TFET structures are expected to result in higher I_{ON} and higher I_{ON}/I_{OFF} ratio over $In_{0.3}Ga_{0.7}As$ Homj TFET.

Chapter 4

Electrical Characterization and Benchmarking

Four TFET structures were grown and fabricated using the process flow introduced in chapter 2. The layer structures are "Large Homj" TFET, "Moderate Stagger" hetero-junction TFET, "High Stagger" hetero-junction TFET and "Small Homj" TFET. The common device schematic and the corresponding TFET band-alignments are shown in Figure 4-1 and 4-2 (a-d) respectively. Table 4-1 summarizes the expected effective barrier heights (E_{Beff}) for these structures along with experimentally measured value for some of them. In all the structures, the p++ GaAsSb source layer is below the InGaAs channel and the drain layers. GaAsSb etches 30 times slower than InGaAs in citric acid. Since wet etch undercut is required to facilitate self aligned gate metal deposition on the side wall, GaASb on top of InGaAs will undercut slower than InGaAs and will shadow the tunneling junction for self aligned gate deposition. Thus, GaAsSb is designed as the bottom layer. The P+ source layer has been heavily doped to make sure that the electric field is maximized. The N+ drain layer doping is low to make sure that the off-state leakage is not dominated by the ambipolar leakage.

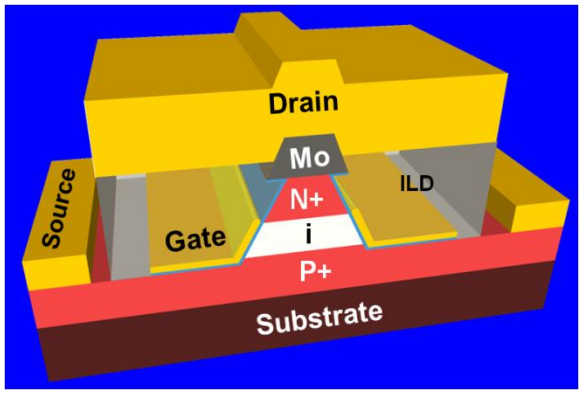

Figure 4-1. Device schematic of the nano-pillar TFET. P+ source is at the bottom while n+ drain at the top. The device is planarized with BCB and the gate is on the side wall.

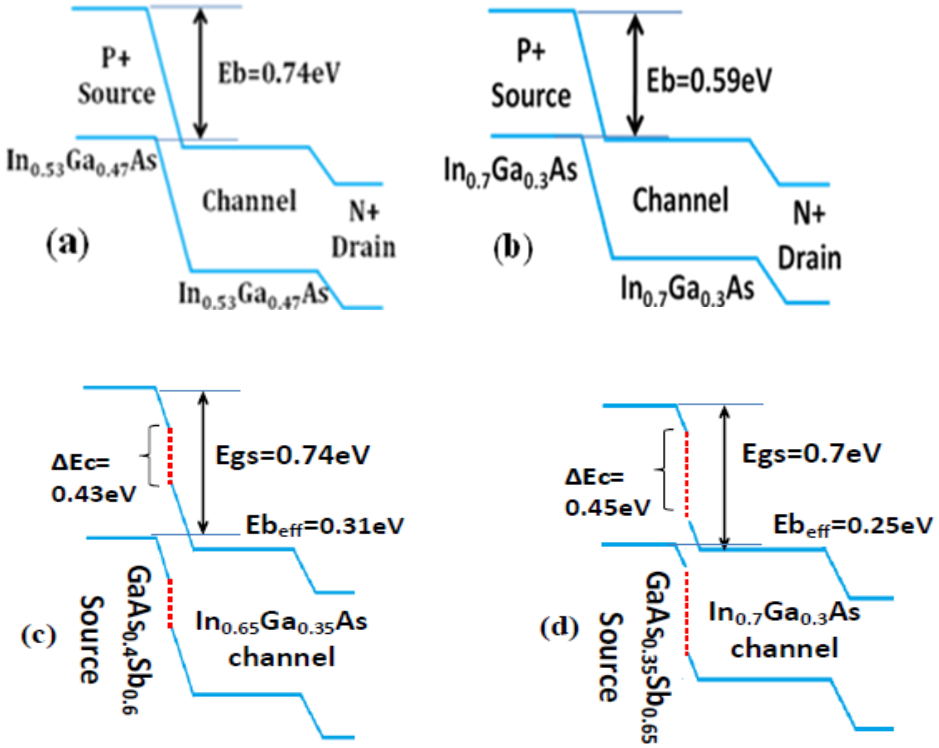

Figure 4-2. Band-alignments for Large Homj TFET, Small Homj TFET, Moderate Stagger HTFET and High Stagger HTFET.

TFET	Expected E_{Beff} (eV)	Measured E_{Beff} (eV)
Large Homj	0.74	0.74
Small Homj	0.58	0.58
Moderate Stagger	0.31	0.3
High Stagger	0.25	0.202

Table 4-1. Summary of TFET effective tunneling barrier heights (E_{Beff}) fabricated in this dissertation.

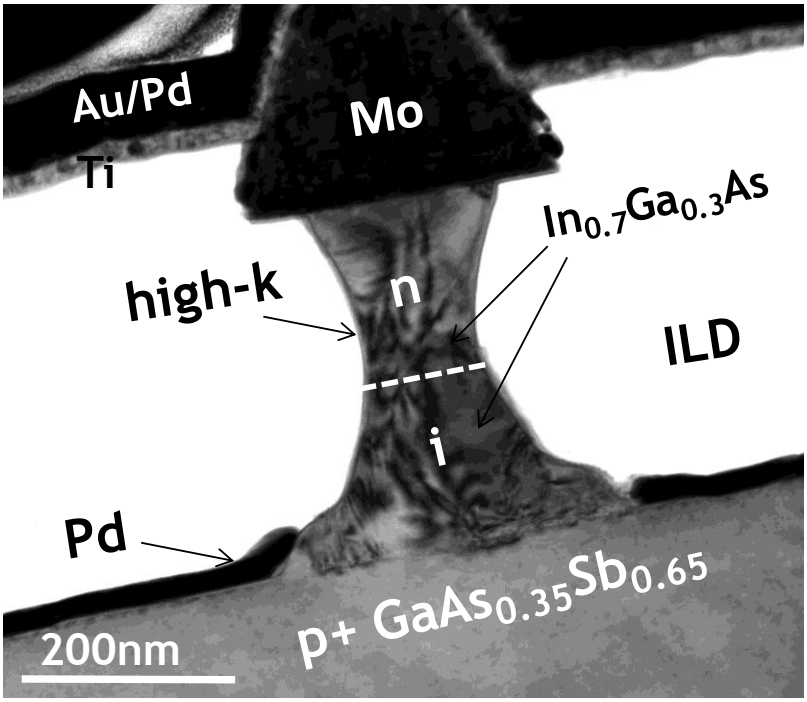

Figure 4-3. GaAs like High Stagger HTFET cross-section TEM

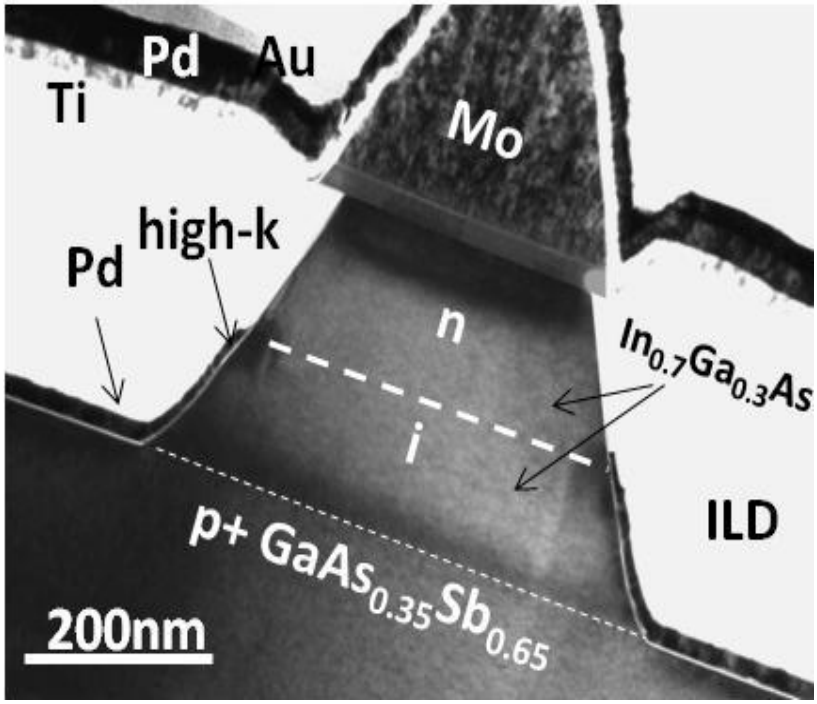

Figure 4-4. InAs like High Stagger HTFET cross-section TEM

Figure 4-3 and 4-4 show cross-section TEM images of the fabricated high stagger hetero-junction TFET structures grown with two different hetero-interface terminations: GaAs like interface and InAs like interface respectively. Threading dislocations can be observed within the InGaAs layer in the GaAs like structure and the shape of the MESA or the pillar is conical. While in the InAs terminated interface, no apparent dislocations in the scale shown is observed. The shape of the pillar after wet etch reveals (111) side wall which is expected after the wet etch. The conical shape of the GaAs like interface could be a result of dislocations bringing in different etch rate and etch profile. The gate and the drain contact structures, BCB planarization, ALD high-k deposition etc. look similar for both of them.

Before we move to the results and comparison of electrical characteristics with respect to the effect of scaling E_{Beff}, it is important to observe the effect of hetero-interface termination on the output and transfer characteristics of the GaAs like and InAs like high stagger hetero-interface TFET structures. Figure 4-5 and 4-6 compare the I_{DS}-V_{GS} and I_{DS}-V_{DS} curves respectively measured at room temperature. Consistent with the difference in the reverse leakage of the p-i-n diodes, the off-state leakage of the InAs like interface is 10^4X smaller than that of the GaAs like interface and is a result of significantly reduced interface defect and Tamm state density. The SS is also steeper due to the reduction in I_{OFF}. I_{DS}-V_{DS} curves of the GaAs terminated interface do not saturate because of the defective InGaAs layer and high I_{OFF}. However, the I_{DS}-V_{DS} curves of the InAs terminated interface saturate very well with improved I_{ON} due to improved junction properties. The peak to valley current ratio (PVCR) in the forward side of the I_{DS}-V_{DS}, i.e., negative V_{DS} side is higher for the InAs terminated interface due to the reduced excess current density. Excess current is trap assisted tunneling current that takes place through gap states present in the tunneling junction. Higher the trap density, higher is the excess current and hence lower is the PVCR.

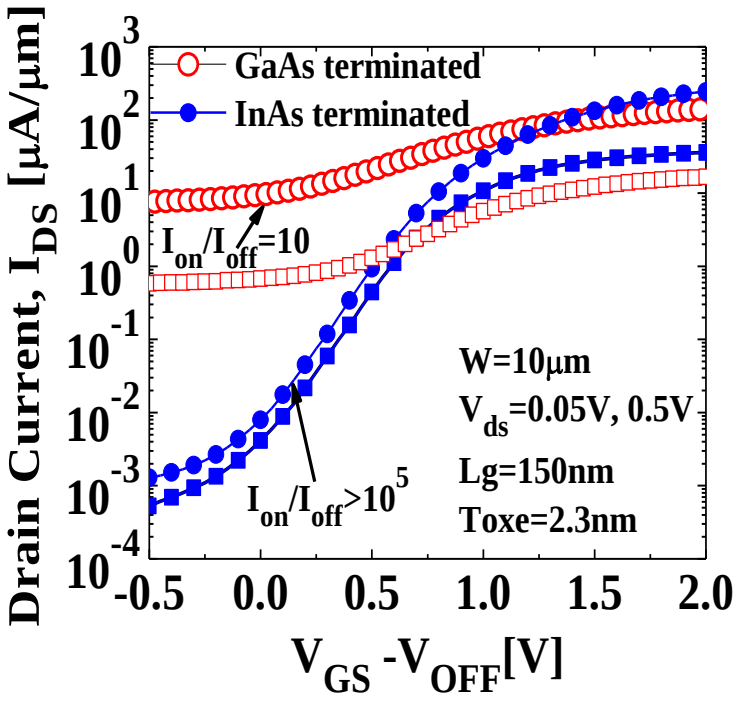

Figure 4-5. Comparison of the measured I_{DS}-V_{GS} characteristics of InAs and GaAs like High Stagger HTFET.

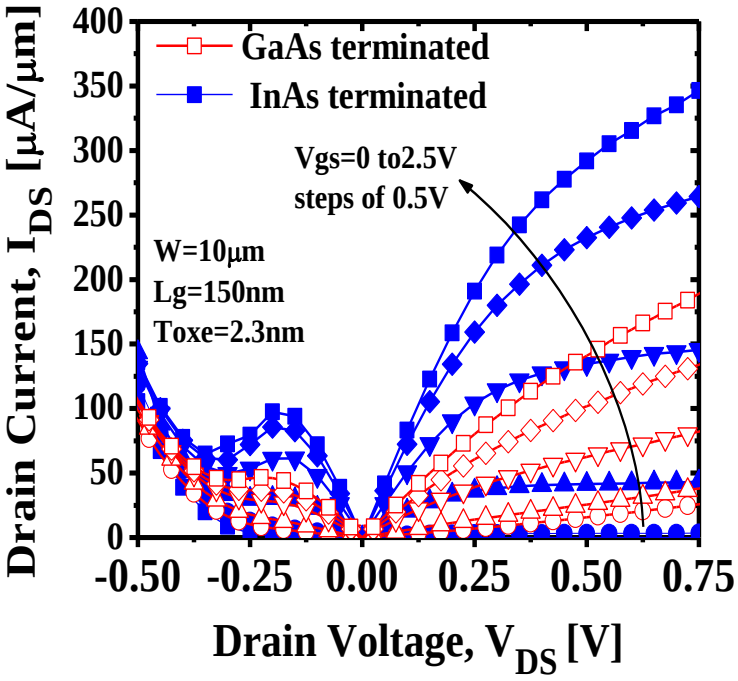

Figure 4-6. Comparison of the measured I_{DS}-V_{DS} characteristics of InAs and GaAs like High Stagger HTFET.

4-1. Electrical Results as a Function of E_{Beff}

In order to study the effect of E_{Beff} scaling on the on-current (I_{ON}), on-off ratio (I_{ON}/I_{OFF}), switching slope (SS) and drain induced barrier thinning (DIBT), Large Homj, Small Homj and Moderate Stagger hetero-junction TFETs were also fabricated. The channel length (L) for the Large Homj is 100nm opposed to 150nm for the remaining three TFETs. The choice of longer channel length for the smaller E_{Beff} system is to prevent any short channel effect and thick T_{oxe} on the I_{OFF}, SS and DIBT of the measured characteristics. Unlike MOSFETs, it has already been proven that the on current in a Tunnel FET is nearly independent of the channel length [65]. Hence, choosing different channel length for different E_{Beff} systems does not make any difference as far as comparison of the DC performance is concerned. Width of the fabricated devices is 10µm, while the measured T_{oxe} from $In_{0.53}Ga_{0.47}As$ MOS capacitors is 2.3nm.

Figure 4-7 compares the transfer characteristics (I_{DS}-V_{GS}) of all the fabricated devices at V_{DS}=0.05V and 0.5V. The curves shift left with reducing E_{Beff}. The early onset of the I_{DS}-V_{GS} is a result of reducing E_{Beff} since in a type II system, increasing stagger and reducing E_{Beff} means lower V_{GS} to turn on the transfer characteristics. The gate leakage is much lower than the off-state leakage of for each of the fabricated devices, signifying that the off-state leakage is determined by S-R-H generation or ambipolar leakage. Figure 4-8 shows calculated inverse of point switching slope vs drain current at room temperature and at V_{DS}=0.05V. SS is non uniform and varies with I_{DS} and V_{GS} which is characteristic of Tunnel FETs. The minimum value of the SS moves to right indicating that for the same point SS, the transmission or the tunneling probability is higher. Ideally, for Tunnel FETs to replace MOSFETs, it is desired to have the min value of the SS below 60mV/dec over significant orders of magnitude change in drain current. In the fabricated devices the SS is greater than 60mV/dec due to two reasons: (a) The fabricated devices do not have a scaled T_{oxe} ($\leq$1nm) and scaled T_{body} ($\leq$7nm). (b) The high-k/channel interface is not

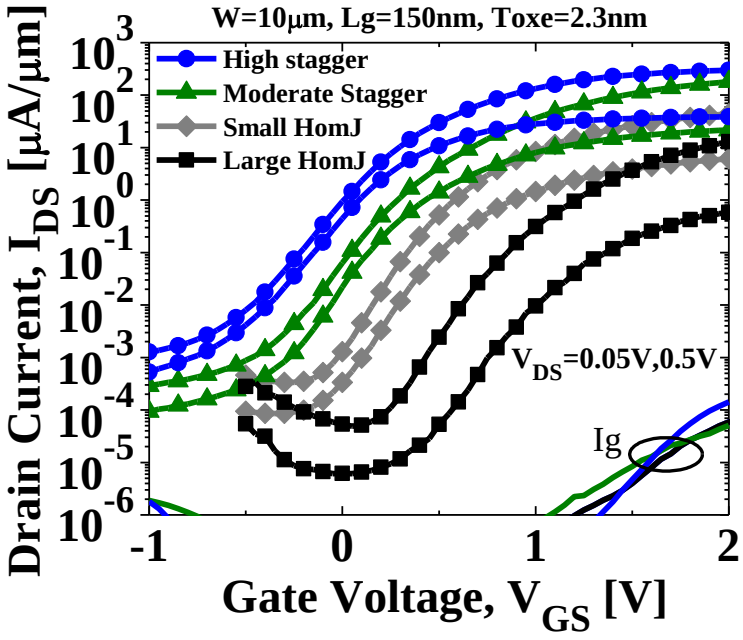

Figure 4-7. Comparison of the measured I_{DS}-V_{GS} characteristics for different E_{Beff} systems.

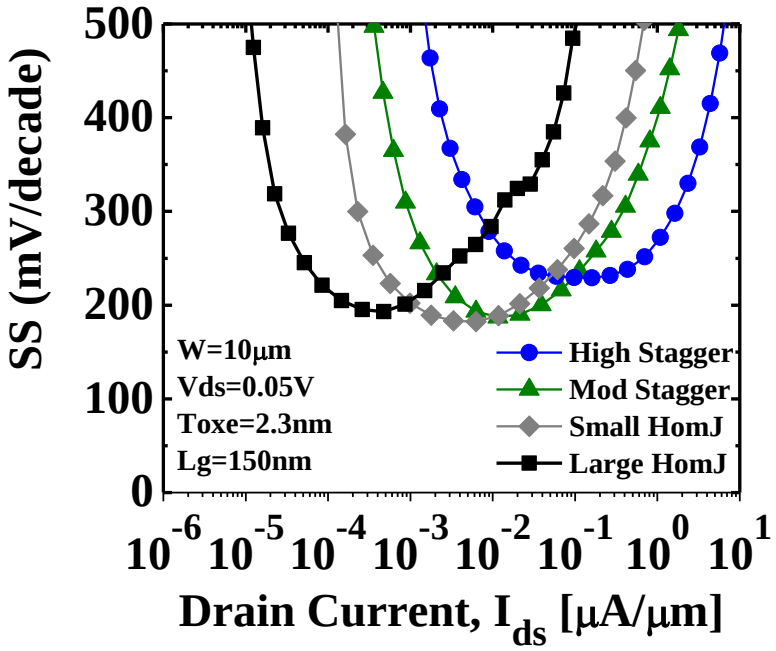

Figure 4-8. Comparison of the calculated SS vs I_{DS} characteristics for different E_{Beff} systems.

optimized as far as reducing Dit is concerned as discussed in section 1-2.2 (E) and will be discussed later in more detail in the pulsed I-V measurement section.

4-1.1. Impact on I_{ON}

Figures 4-9 (a-d) show the measured room temperature output characteristics (I_{DS}-V_{DS}) of the fabricated devices. The applied gate biases mentioned in the plots have been adjusted for the different turn-off voltages observed in the transfer characteristics. This is needed to compare the on-current for the same overdrive. The I_{DS}-V_{DS} for the Large Homj TFET does not saturate because of the large tunnel barrier and thick T_{oxe}. However for the smaller E_{Beff} systems including the small Homj TFET, the I_{DS}-V_{DS} show clear signs of output saturation. Moving from Large Homj TFET to Small Homj TFET, E_{Beff} reduces by 21% and the I_{ON} at V_{GS}=2.5V and V_{DS}=0.5V increases from 24µA/µm to 60µA/µm, a 150% increase. Moving to Moderate Stagger, E_{Beff} reduces by 58% and the on-current increases to 100µA/µm, 319% increase. Finally, for the High Stagger TFET, E_{Beff} reduces by 66% and the I_{ON} increases to 260µA/µm, 983% increase. This demonstration of high on-current using an inter band tunneling junction explains that, fundamentally, Tunnel FETs can deliver MOSFET like on current while maintain high on-off ratio thus eliminating the low on current limitations posed by homo-junction TFETs.

4-1.2. Impact on SS

Due to the large V_{GS} stretch out, however, high overdrive voltages have been used to report the measured BTBT current. Because the I_{DS}-V_{DS} curves saturate even with such high overdrive voltages of V_{GS}-V_{OFF}=2.5V, there is room for reduction of this stretch out using T_{oxe} scaling. Figure 4-10(a) shows measured I_{DS}-V_{GS} characteristics for the high stagger hetero-junction TFET with scaled T_{oxe} of 2nm (0.3nm reduction). Figure 4-10 (b) shows the corresponding point SS vs I_{DS} calculated at V_{DS}=0.3V. Clearly, the SS_{min} and the average SS measured from 5nA/µm to 1µA/µm is lower than for the case with T_{oxe}=2.3nm. Further

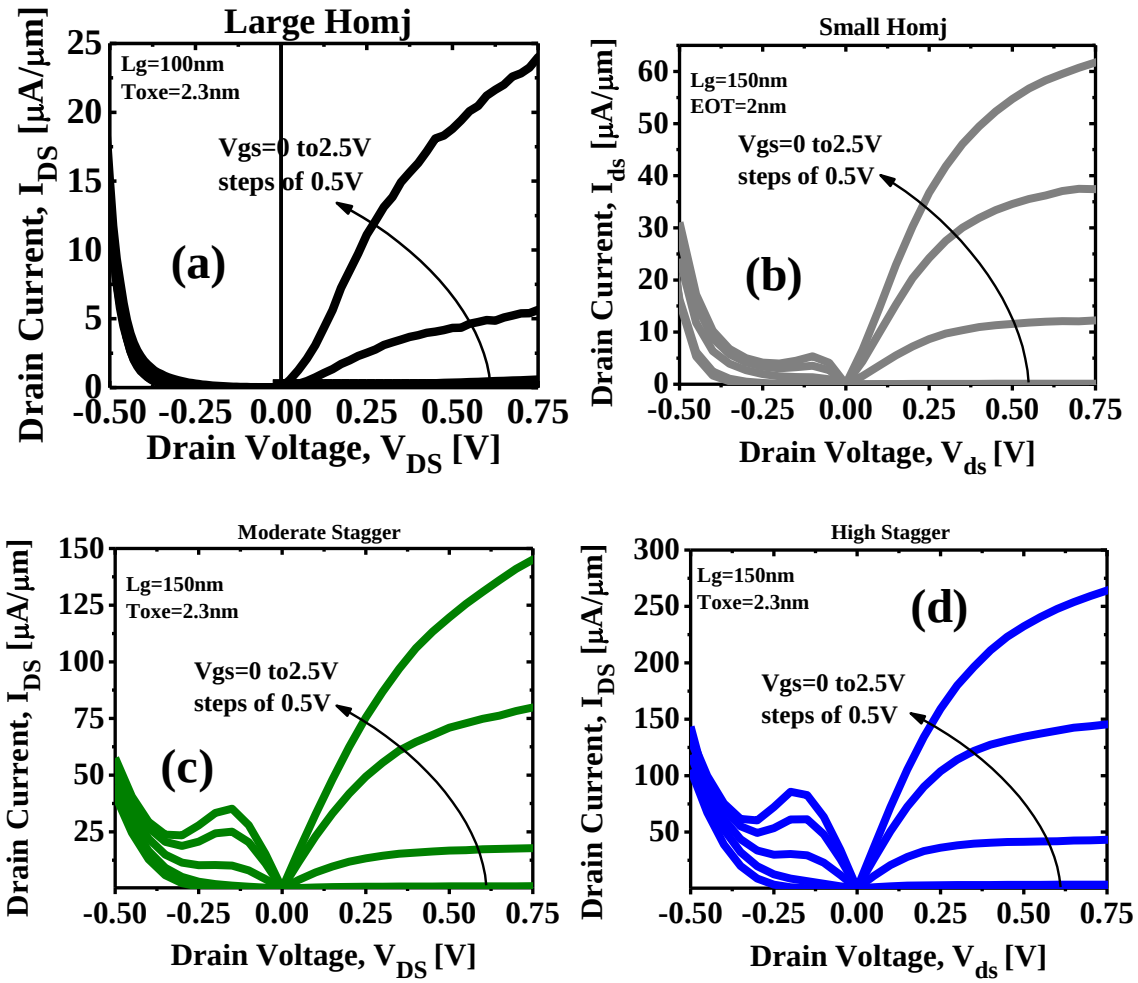

Figure 4-9. (a-d) Measured output characteristics of different E_{Beff} systems.

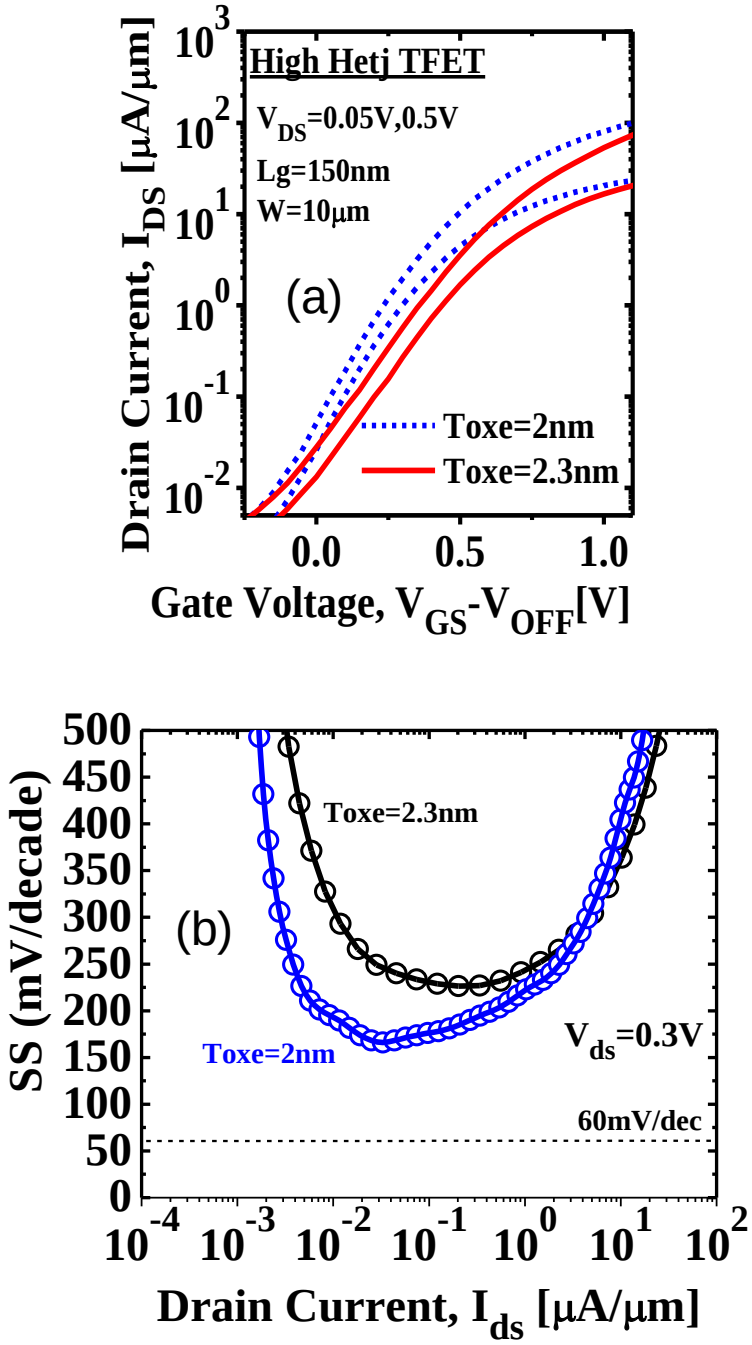

Figure 4-10. (a) Effect of T_{oxe} scaling on the I_{DS}-V_{GS} curve of High stagger HTFET. (b) Change in SS vs I_{DS} characteristics as a result of T_{oxe} scaling.

significant reduction in SS is expected with T_{oxe} scaling down to 1nm, thus reducing the un-intentional V_{GS} stretch out obtained due to poor Fermi-level movement in the presence high Dit. Figure 4-11 summarizes the change in on-current with E_{Beff} and T_{oxe} scaling combined. For I_{OFF}=5nA/μm and V_{GS}-V_{OFF}=1.5V, High stagger Hetj TFET shows I_{ON} of 135μA/μm with I_{ON}/I_{OFF} of 27000, a record value demonstrated till date in the category of Tunnel FETs.

4-1.3. Impact on DIBT

Drain induced barrier thinning (DIBT) is an important metric to quantify the short channel effects in Tunnel FETs. It is analogous to the Drain Induced Barrier Lowering (DIBL) in MOSFETs with the only difference being the carrier injection mechanism. In a short channel MOSFET, V_{DS} impacts the source thermionic barrier by reducing the barrier height, while in a short channel Tunnel FET, V_{DS} impacts the tunnel junction by thinning the barrier width or the tunneling length. The dependence of the short channel effects as a function of channel length (L) and other device geometry (T_{oxe}, T_{body}) are also different and can be referred for details at [75]. For a given tunnel barrier height and common device geometry, Tunnel FETs suffer from lower short channel effects (SCE) than MOSFETs up to a critical channel length L_C below which the SCE in Tunnel FETS become severe and worse than MOSFETs due to increased direct S/D tunneling.

Since the SS of a Tunnel FET is a strong function of V_{GS} and is not a constant, choosing a current level to quantifying DIBT requires some understanding. For the same channel length, tunnel junctions with different barrier heights can result in orders in magnitude difference in on-currents. Hence, while comparing DIBT for different tunneling barrier heights (E_{Beff}), different current levels can be chosen for evaluating DIBT. For example, current levels which lead to minimum DIBT can be chosen or a fraction to the on-current can be chosen such as I_{ON}/100 or

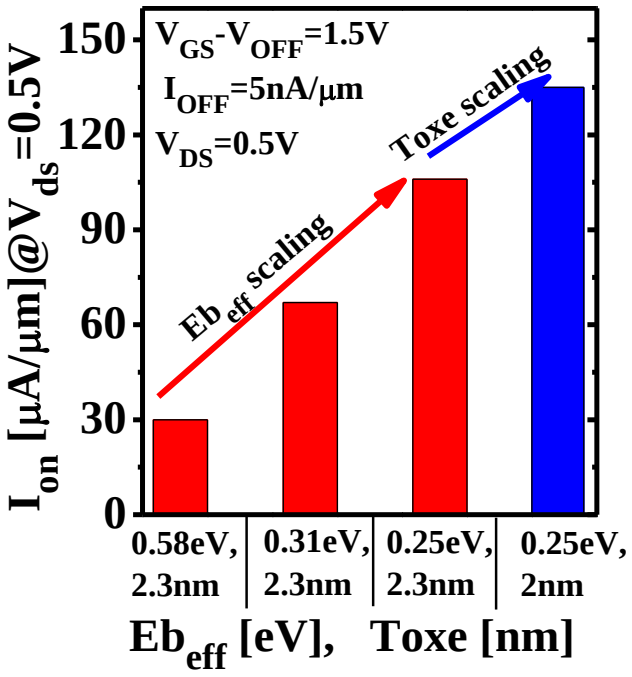

Figure 4-11. Summary of the effect of E_{Beff} and T_{oxe} scaling on the Ion of the fabricated devices.

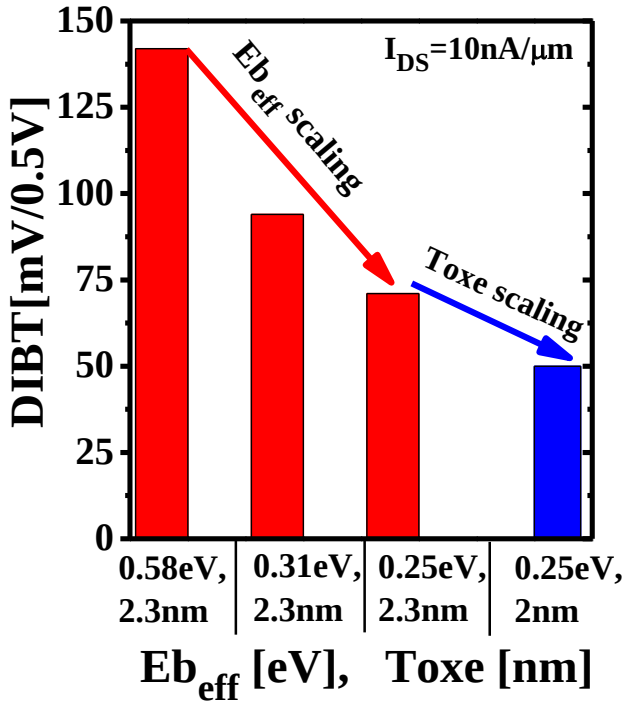

Figure 4-12. Summary of the effect of E_{Beff} and T_{oxe} scaling on the DIBT of the fabricated devices.

I_{ON}/1000 and the rule should be fixed for each of them. Figure 4-12 summarizes DIBT calculated from Figure 4-7 and 4-10 (a) at I_{DS}=10nA/µm and for V_{DS} change from 0.05V to 0.5V.DIBT reduces with decreasing barrier height. This is a very important result as far as short channel effect is concerned. In order to investigate more into this dependence, TCAD simulations of the change in profile of the electron BTBT generation rate close to the source channel tunnel junction is shown in Figure 4-12. Note the peak position of the generation rate for the Small Homj TFET and the High Stagger Hetj TFET at I_{DS}=10nA/µm. The peak position is closer to the source channel tunnel junction for the high stagger indicating that the effective scaling length (λ_{eff}) is smaller for the high stagger and the device is more scalable than the homo-junction counterpart. This also means that with further scaling of the E_{Beff}, even further increase in scalability is expected.

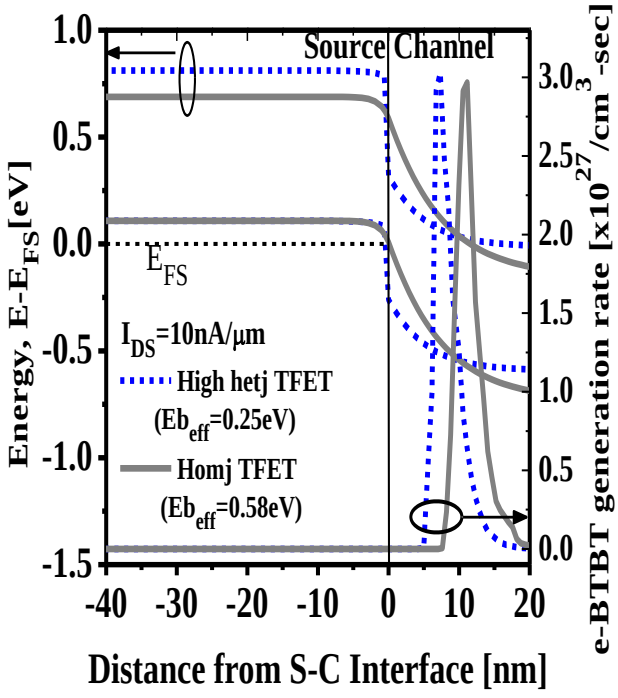

Figure 4-13. electron band to band (e-BTBT) generation rate plotted as a function of the distance from the source channel interface. e-BTBT calculated at I_{DS}=10nA/µm.

4-2. Pulsed I-V on Small Homo-junction TFET

The measured room temperature I_{DS}-V_{GS} of TFETs shown in Figure 4-7 have point switching slope higher than 60mV/dec for all I_{DS}, which is not desired since the reason for choosing Tunnel FET as an alternate low power device is the sub-kT/q steep switching property. As indicated before, device geometry can lead to significant reduction in SS; however there is fundamental fabrication issue in the fabricated devices with respect to the high-k/channel interface. Figure 4-14 shows measured Capacitance Voltage characteristics for $In_{0.53}Ga_{0.47}As$ MOSCAPs with 1nmAl_2O_3/3.5nmHfO_2 as the bi-layer gate oxide. Expected ideal C-V at is also shown for comparison. Clearly, below flat band (FB) voltage, near the depletion region, excess capacitance is observed indicating significant contribution of Cit due to Dit. Since Al_2O_3 forms the interface with InGaAs, Dit profile and density similar to that of Figure 1-10(c) is expected. This density of interface state is very high and it is important to look at the characteristic trap capture-emission time constants of such as trap distribution. Figure 4-16 shows calculated electron capture-emission time constants from mid-gap towards CB edge. The characteristics capture time near mid-gap is of the order of low msec and decrease exponentially to sub-µS values at energy levels close to band-edges. These traps respond to the perturbations in the Fermi-level movement by capture and emission process, thus stretching out the I_{DS}-V_{GS} response. In addition, traps present close to the mid-gap contribute through trap-assisted tunneling followed by thermionic emission leading to excess current and SS dilution in the switching slope regime as shown in Figure 4-16. If the I_{DS}-V_{GS} measurement can be pulsed with a period much faster than the response time of these mid-gap traps, the trap-assisted tunneling and sluggish Fermi-level movement can be avoided. Figure 4-17 shows a simplified block diagram of the pulsed-IV set up used for fast I-V measurements.

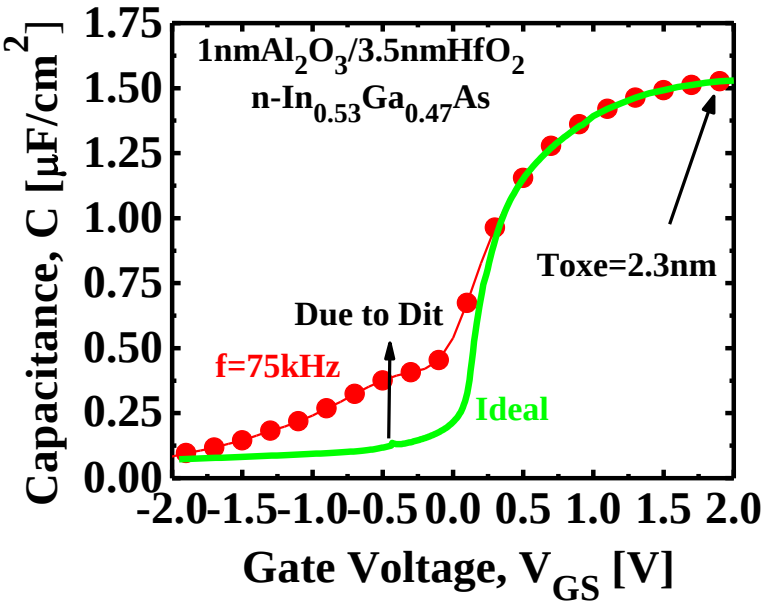

Figure 4-14. Capacitance Voltage characteristics measured for $1nmAl_2O_3/3.5nmHfO_2/n\text{-}In_{0.53}Ga_{0.47}As$ MOSCAPs at f=75 KHz. Also shown ideal CV expected at the measured frequency.

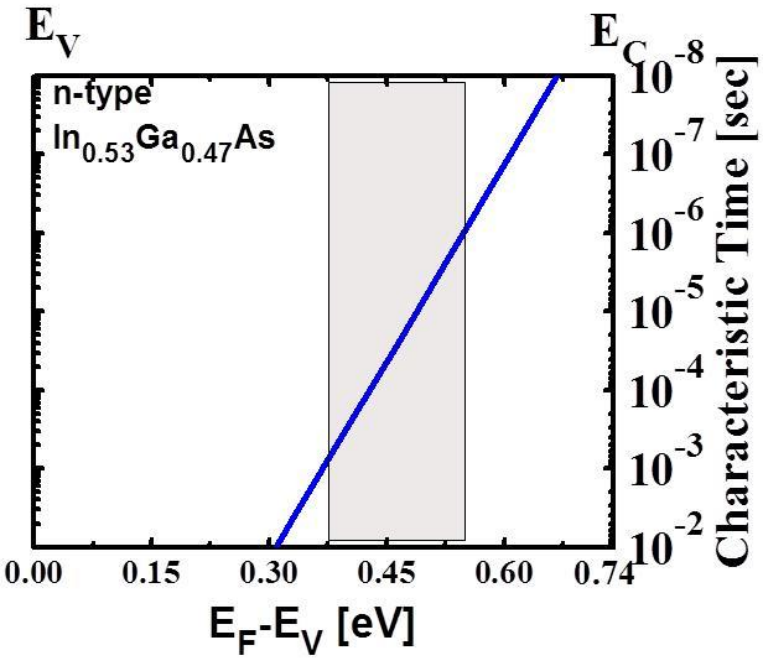

Figure 4-15. Calculated trap characteristic response time for electrons. Trap response time range between 1ms and 1μs.

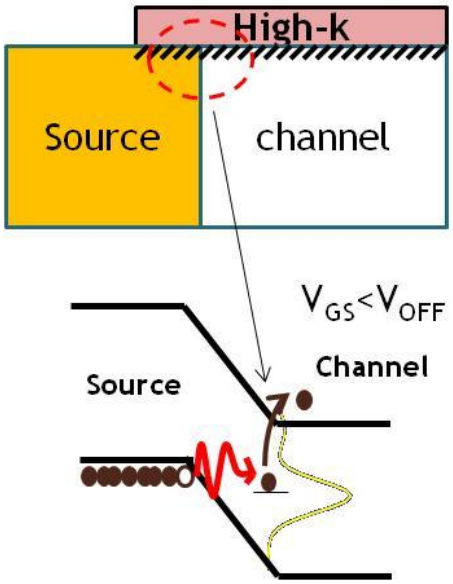

Figure 4-16. Schematic explaining trap assisted tunnel followed by thermionic emission occurring near the high-k/ tunneling junction interface.

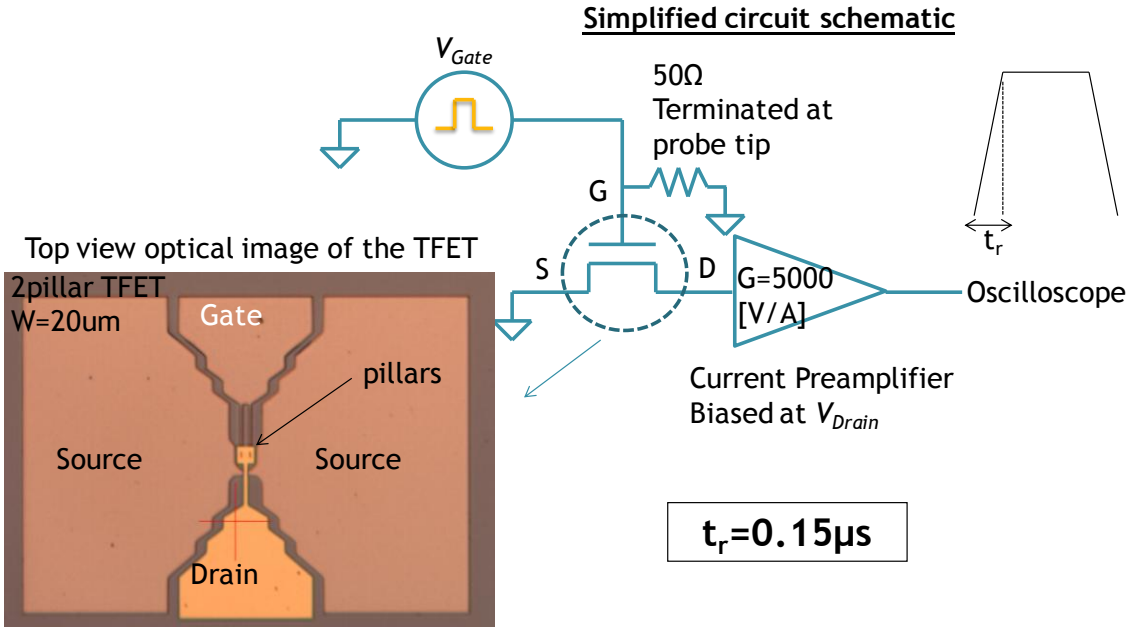

Figure 4-17. Fast IV measurement set up used to avoid slow traps responsible for SS dilution at room temperature. Minimum response time of 0.15µs was reliably recorded. (Bottom left) Snapshot of the device used for Pulsed IV measurements.

Small Homj TFET was used for demonstration of steepening of the SS. The input gate voltage pulses have rise time (t_r) of 10ns and pulse period as low as 0.1µs. A current pre-amplifier was connected between the drain terminal and the drain supply voltage. The pre-amp consists of a two stage trans-impedance amplifier, each stage having an OPAMP as the amplifier with negative feedback through resistors as shown in Figure 4-18. The gain of the first stage OPAMP is 1000 while for the second is 10. In order to transfer maximum power to the second stage, 200ohm matching resistor is inserted between the two gain blocks resulting in net gain of 5000. Agilent 81110 was used as the function generator and the pulsed I-V response were recorder in LeCroy oscilloscope. Using the setup shown in Figure 4-17, the response time of the transient TFET drain current was reliably sampled after 150ns (t_{resp}). Figure 4-19 compares the I_{DS}-V_{GS} between DC and pulsed IV. The pulsed I_{DS}-V_{GS} data show marked steepening of the switching slope with minimum SS of 100mV/decade and matches the theoretical I_{DS}-V_{GS} for Dit ~ $8x10^{11}/cm^2$ as shown in Figure 4-20.

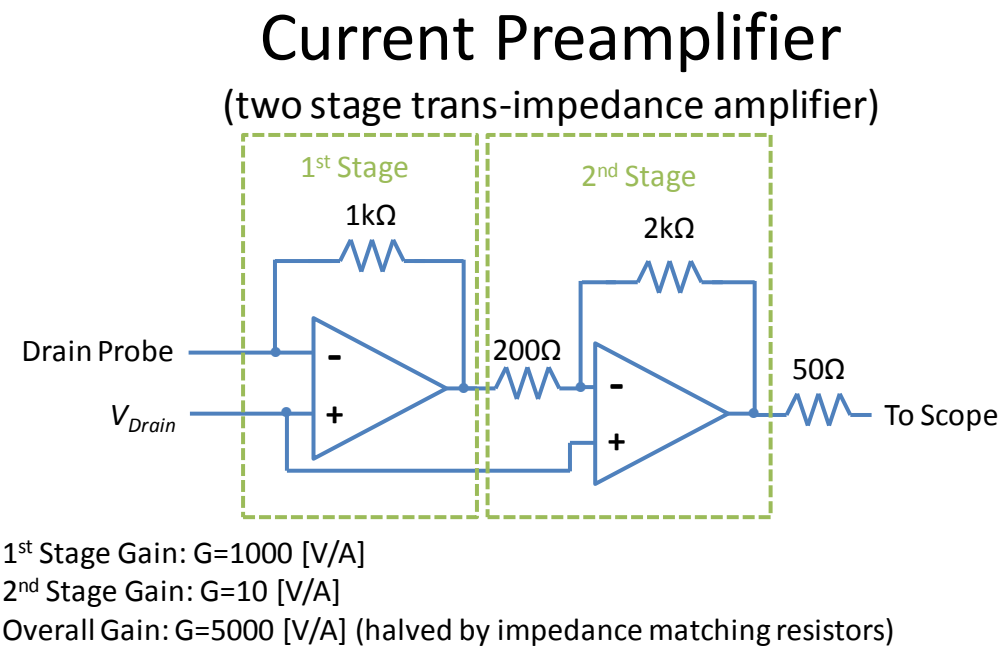

Figure 4-18. Current pre-amplifier used to amplify the measured pulsed drain voltage within the switching slope regime.

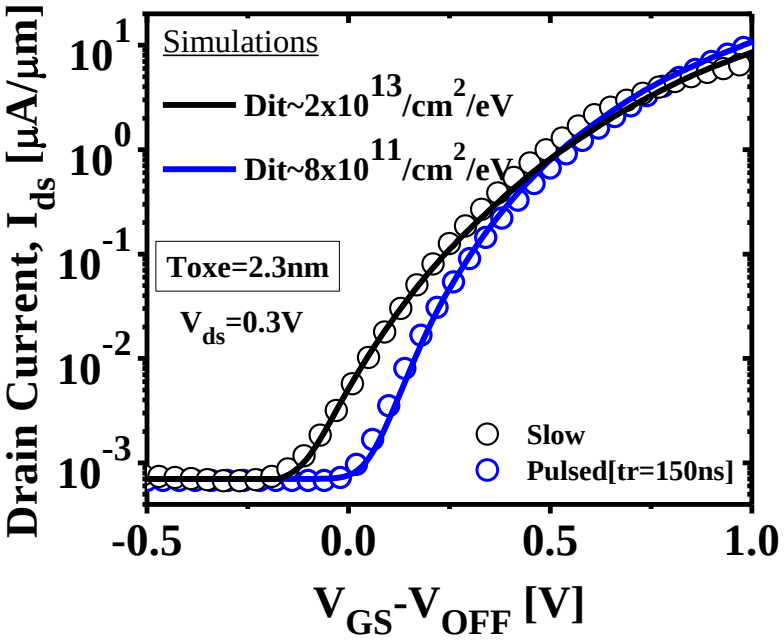

Figure 4-19. Comparison of DC and Pulsed I_{DS}-V_{GS} curves measured at room temperature.

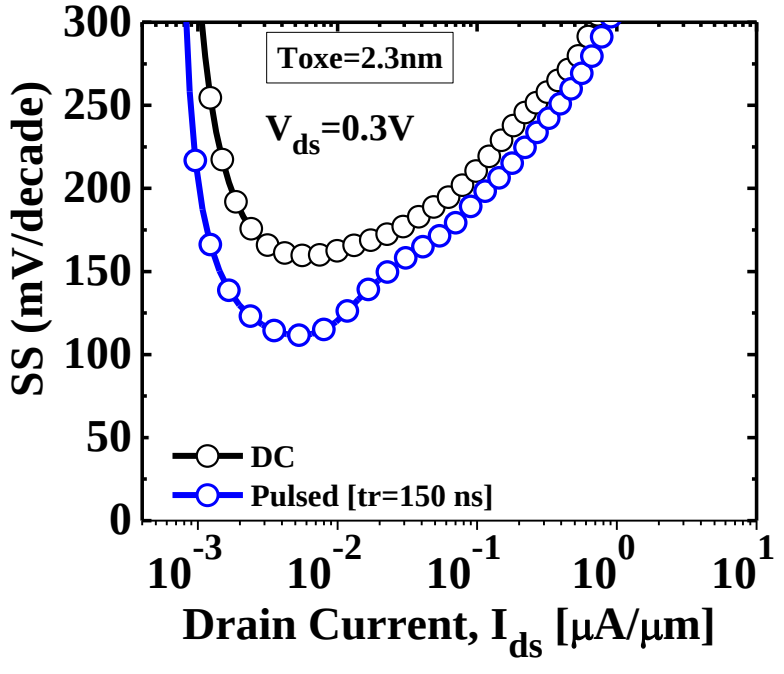

Figure 4-20. Improvement in the switching slope with pulsing. SS_{min} improves from 150mV/dec to 100mV/dec.

4-3. Benchmarking

For low power logic applications, it was shown in Figure 1-7 that broken gap TFETs can deliver superior performance than MOSFETs with drive currents ≥100μA/μm at V_{DS}=0.3V. Hence, in order to benchmark the measured I_{ON} and I_{OFF} in this hetero-junction TFET research, V_{DS}=0.3V has been chosen. Figure 4-21 shows I_{DS}-V_{GS} of the Small Homj, Moderate stagger and High stagger TFETs measured at V_{DS}=0.3V and compared with those reported at V_{DS}≤0.5V [58, 69]. The V_{GS} is adjusted for the offset voltage. If we neglect the stretch out of switching slope regime and focus on the pure BTBT regime, drive current is higher for the fabricated staggered systems measured in this work due to the reduced E_{Beff}. Table 4-2 summarizes the on-current, effective switching slope and I_{ON}/I_{OFF} as a function of E_{Beff}. I_{ON} is measured at V_{GS}-V_{OFF}=1.5V, where V_{OFF} is taken at I_{DS}=5nA/μm. SS_{eff} is calculated as [45]:

$$SS_{eff} = (V_{GS}-V_{OFF})/ (2\log (I_{ON}/I_{OFF}) \quad (4\text{-}1)$$

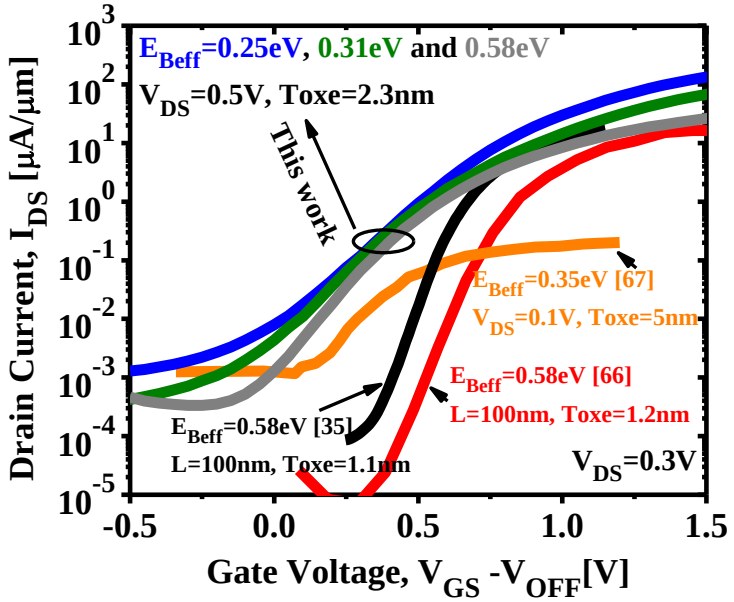

Figure 4-21. Benchmarking of the offset corrected I_{DS}-V_{GS} curve of the High Stagger HTFET against those reported till date [35] [66] [67].

Reference	E_{Beff} (eV)	Lg (nm)	T_{oxe} (nm)	V_{ON}-V_{OFF} (V)	V_{DS} (V)	I_{ON} (µA/µm)	I_{ON}/I_{OFF}	SS_{eff} (mV/dec)
Zhao et. al, EDL,2011 [66]	0.58	100	1.2	1.5	0.5	30	$6x10^3$	200
Dewey et. al IEDM, 2011 [35]	0.74	100	1.1	0.9	0.3	8	$1.6x10^3$	140
Dewey et. al IEDM,2011 [35]	0.58	100	1.1	0.9	0.3	17	$3.4x10^3$	106
Small HomJ (This work)	0.58	150	2.3	1.5	0.5	30	$6x10^3$	200
Mod. HetJ (This work)	0.31	150	2	1.5	0.5	78	$1.5x10^4$	179
High HetJ (This work)	0.25	150	2	1.5	0.5	135	$2.7x10^4$	169

Table 4-2. Benchmarking the record high on-current achieved using High Stagger HTFET compared with those reported till date at I_{OFF}=5nA/µm.

Clearly, high stagger TFETs show record high drive current of 135µA/µm at on-off ratio of $2.7x10^4$ which is also a record in the category of surface tunneling devices reported till date. With further scaling of E_{Beff} to zero gap, further enhancement in drive current is expected at V_{DS}=0.3V.

4-4. Modeling and Projection

With the fast I-V measurements on the Small Homj TFET (Figures 4-19 and 4-20), it is argued that if the higk-k/channel Dit can be reduced below $8x10^{11}/cm^2/eV$, trap assisted tunneling followed by thermionic emission process diluting the SS regime can be avoided enabling pure BTBT to determine the sub-threshold conduction. Since the channel of the Small Homj and the High Stagger hetero-junction TFETs are the same (InGaAs), similar Dit distribution is expected. Figure 4-22 (a) shows modeling of the measured high stagger TFET I_{DS}-V_{GS} curves for T_{oxe} of 2nm and 2.3nm and at V_{DS}=0.3V. Consistent with the modeling of the homo-junction TFET, the SS regime of the hetero-junction TFET can be consistently reproduced using uniform Dit of

10^{13}/cm^2/eV. Figure 4-22(a) also shows the simulation result for the case when Dit ~$8x10^{11}$/cm^2/eV and for T_{oxe}=1nm. Figure 4-22(b) compares the switching slope as a function of I_{DS} and T_{oxe}. Clearly, for T_{oxe}=1nm and mid-gap peak Dit≤$8x10^{11}$/cm^2/eV, high on-current and SS<60mV/dec over more than two orders of magnitude change in I_{DS} is expected.

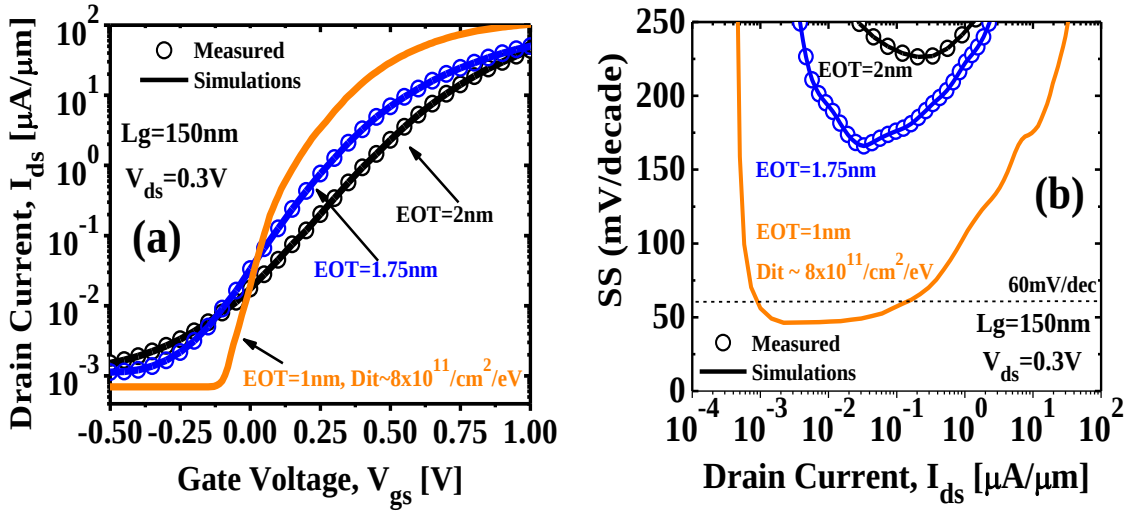

Figure 4-22. (a-b) Measured and modeled I_{DS}-V_{GS} and SS vs I_{DS} curves of the High Stagger HTFET for EOT (T_{oxe}) =2.3nm, 2nm and V_{DS}=0.3V. Projection for T_{oxe}=1nm and mid-gap peak Dit<=$8x10^{11}$/cm^2/eV.

Even with T_{oxe}=1nm, the on-current for the high stagger hetero-junction TFET at V_{CC}=0.3V and I_{OFF}=5nA/µm is only 10µA/µm. Please note that the body thickness of the modeled high stagger TFET device is still large (T_{body}=200nm). Scaling of the T_{body} down to 7nm is expected to result in significant increase the device electrostatics and hence the drive current. Figure 4-23 shows the I_{DS}-V_{GS} characteristics expected for the high stager TFET with T_{body}=7nm. The on-current at V_{CC}=0.3V has now increased 10 µA/µm to 50µA/µm. However, this is equivalent in performance to the recently published 22nm Tri-gate TFET data published from Intel [36]. Hence this is not at all a low power option as far as substitution or a replacement technology is concerned. Further scaling of the E_{Beff} is required. Figure 4-23 also shows the I_{DS}-V_{GS} curve for broken gap TFET with E_{Beff}~0eV. Clearly, this TFET can deliver 100µA/µm of

drive current for $V_{DS} \leq 0.3V$ which is more than an order higher compared to the Tri-gate MOSFET technology. Thus, broken gap Tunnel FETs, with scaled device geometry make tunnel transistors a viable option for future sub 0.3V V_{CC} low power logic technology.

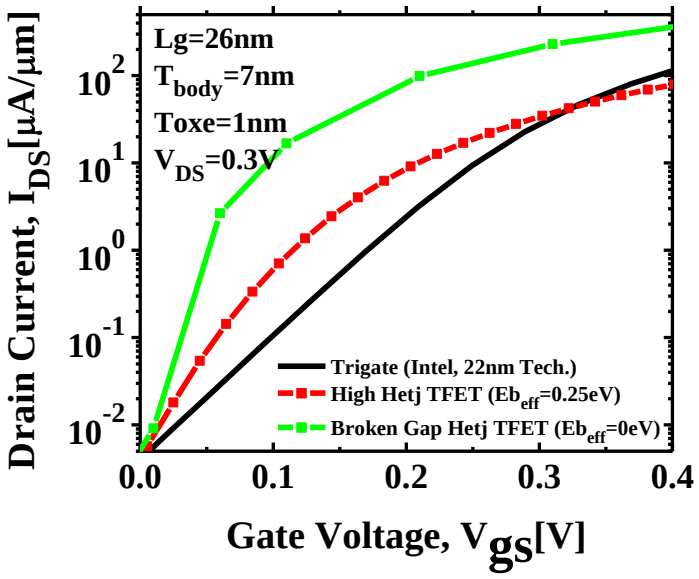

Figure 4-23. Expected I_{DS}-V_{GS} curve for UTB-DG GaSb/InAs broken gap HTFET and compared with Tri-gate MOSFET [36].

4-5. Conclusion

$In_{0.7}Ga_{0.3}As$ homo-junction control, $GaAs_{0.4}Sb_{0.6}$/ $In_{0.65}Ga_{0.35}As$ moderate and $GaAs_{0.35}Sb_{0.65}/In_{0.7}Ga_{0.3}As$ high stagger hetero-junction TFETs are fabricated and the dependence of the I_{ON} and DIBT (short channel effect) on the effective barrier height (E_{Beff}) is systematically studied. By scaling E_{Beff} from 0.58eV to 0.25eV, 253% enhancement in I_{ON} is demonstrated, at V_{DS}=0.5V, arising due to an increased tunneling efficiency. Further, using electrical oxide thickness scaling in conjunction with barrier height engineering, record high I_{ON}=135μA/μm (350% enhancement) along with the highest on-off current ratio $I_{ON}/I_{OFF}=2.7x10^4$ in the category of TFETs is achieved, at V_{DS}=0.5V and V_{GS}-V_{OFF}=1.5V. DIBT is shown to reduce by 65% due to band-to-band generation occurring closer to the source-channel interface, thus improving device electrostatics. Using pulsed I-V technique, traps with capture emission response times of less than 0.1us were reduced and the switching slope is improved from 150mV/dec to 100mV/dec. Further reduction in SS can be achieved with T_{oxe} and T_{body} scaling down to 1nm and 7nm respectively. GaSb/InAs HTFET structures with ultra-thin body dimensions form the ultimate n-channel TFET choice for future low power logic solution.

Chapter 5

Future Work: p-channel As-Sb Tunnel Transistors

Complementary logic has several advantages amongst which low static power dissipation and high noise margin top the list. Since Tunnel FETs are being envisioned as future substitution for MOSFETs in the category of low power logic, a complementary p-channel Tunnel FET solution is inevitable. Unlike MOSFETs, Tunnel FET is an asymmetric device. For n-channel TFETs, the source is designed as heavily doped p+ region, while for p-channel TFETs, source is heavily doped n++ regions as shown in schematic of Figure 5-1. However, the conduction band DOS in III-V semiconductors is very low, hence, heavy n+ doping results in significant Fermi level degeneracy and exposes the tail of the Fermi distributed carriers to BTBT [68].

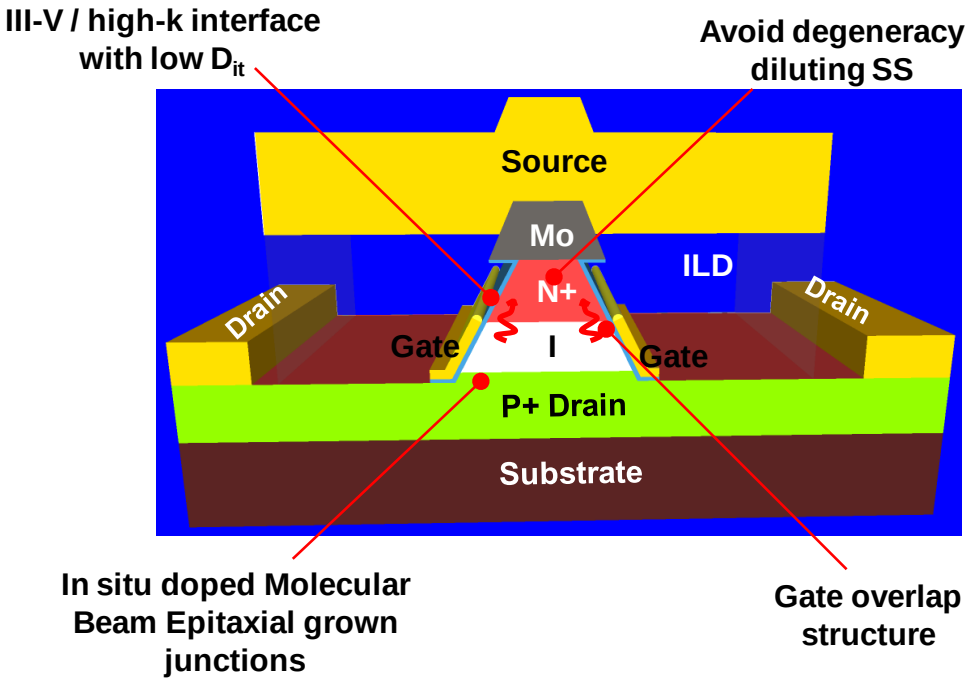

Figure 5-1. Schematic of the p-channel Tunnel FET.

Since this tail is temperature dependent with slope proportional to kT/q, heavy source degeneracy results in SS limited to kT/q as seen in MOSFETs. Figure 5-2 and 5-3 explain this situation. However, high source doping is required to maximize the electric field and hence the drive current. This brings a fundamental trade-off between switching slope and drive current in p-channel III-V HTFET. It is imperative to find innovative solutions towards engineering the density of states in n+ source region of p-channel HTFET while simultaneously engineering the tunnel barrier and the source doping.

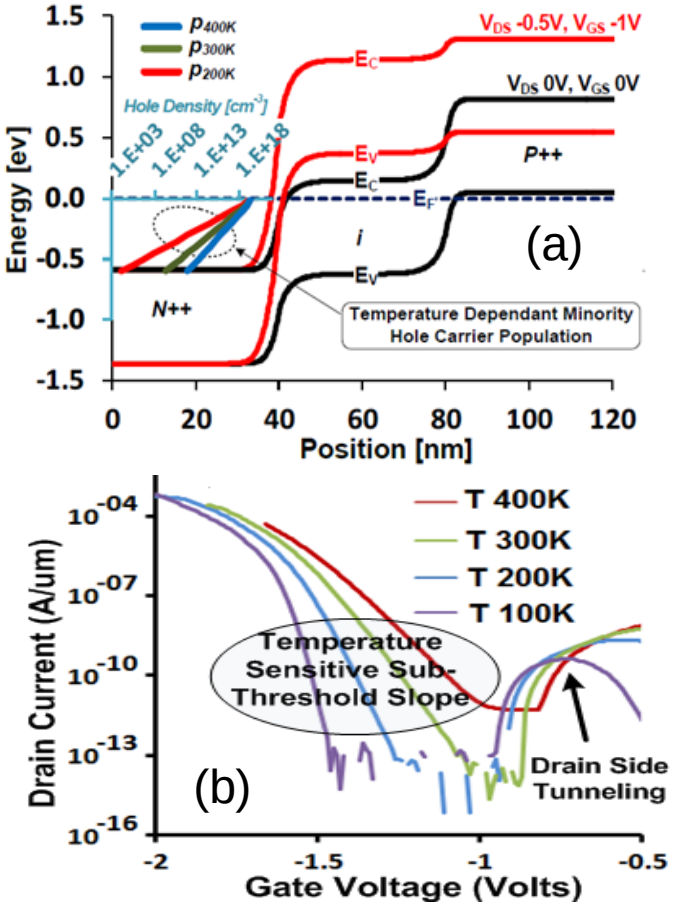

Figure 5-2. (a) GaSb/InAs p-channel Tunnel FET band-diagram explaining the temperature dependent carrier distribution tail completely exposed to tunneling due to heavy degeneracy within the n+ doped InAs source region. (b) Impact of the high source degeneracy on the temperature dependence of the switching slope regime of the p–channel Tunnel FET [68].

5-1. Optimizing Source Doping (Ns)

Figure 5-3 shows I_{DS}-V_{GS} characteristics simulated for p-channel High stagger HTFET and broken gap HTFET with Ns=2x10^{19}/cm^3. L=32nm, T_{oxe}=1nm and T_{body}=7nm. As a guide, 60mV/dec slope is shown using black dotted lines. Clearly, SS for both the TFETs follow the 60mV/dec limit confirming the Fermi degeneracy issue. Please note that the effect of Dit on SS has not been included here for the simplicity of understanding. Bringing down Ns to 5x10^{18}/cm^3 does not avoid the Fermi degeneracy issue, rather the on-current for V_{CC}=0.5V and V_{CC}=0.3V reduces by 8X and 2X with the I_{ON} being less than 10μA/μm. An attempt to further reduce the source doing will result in further degradation of the on-current and hence engineering Ns without changing the DOS of the source material is not a viable solution of p-channel Tunnel FETs.

N-channel TFETs achieve sub-60mV/decade switching slope due the band filtering of the Fermi tail of the carrier distribution by the band-gap. Due to the high DOS of the valence band, Fermi-level is not degenerate even with Ns as high as 8x10^{19}/cm^3. Thus both steep switching and high on-current can be achieved simultaneously. In order to enable p-TFETs achieve the same, the DOS of the conduction band needs to be engineered such that even with heavy doping, the Fermi-level is not significantly degenerate.

Lchannel	32nm
EOT	1nm
Tb	7 nm
Tov	1nm
Tun	1nm
Nd (n+)	vary
Na (p+)	10^{19}/cm^3
Ni-channel	undoped

Table 5-1. p-channel TFET device parameters for TCAD Sentaurus simulations.

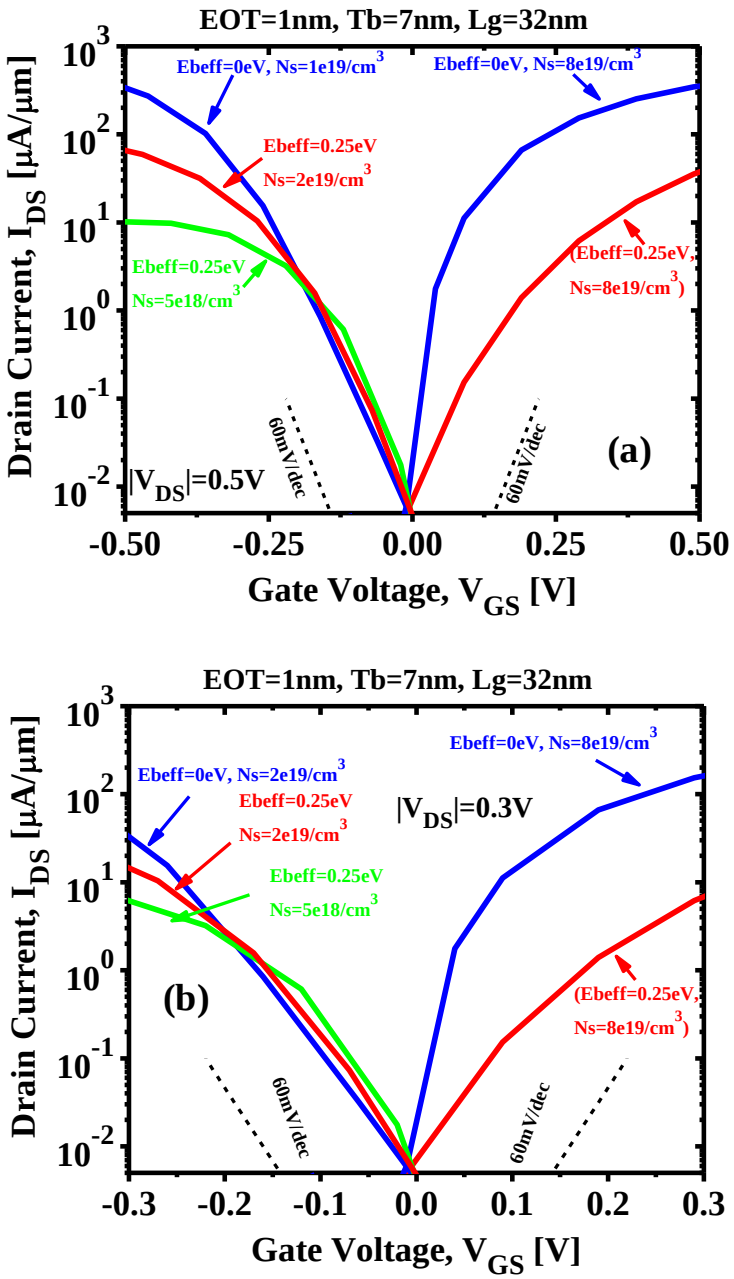

Figure 5-3. (a-b) Simulated I_{DS}-V_{GS} characteristics of the High Stagger and GaSb/InAs broken gap p and n-channel HTFETs for V_{CC}=0.3V and 0.5V respectively. N+ source doping as slow as $5x10^{18}/cm^3$ is not able to remove the degeneracy issue.

5-2. Strain and Quantum engineered "non-classical" p-channel TFET

The fundamental limitation stemming from the limited DOS in the n+ source region of p-channel TFETs challenges us to a broader thinking of DOS engineering utilizing crystal orientation, strain and quantum confinement as key modulating factors. Two categories of DOS engineered p-channel HTFET are: a) Quantum engineered pTFETs and b) Quantum + Strain Engineered pTFETs (see Figure 5-4). Since GaSb/InAs broken gap TFET is expected to result in maximum TFET drive current at $V_{CC} \leq 0.3V$, n++ InAs needs DOS optimization.

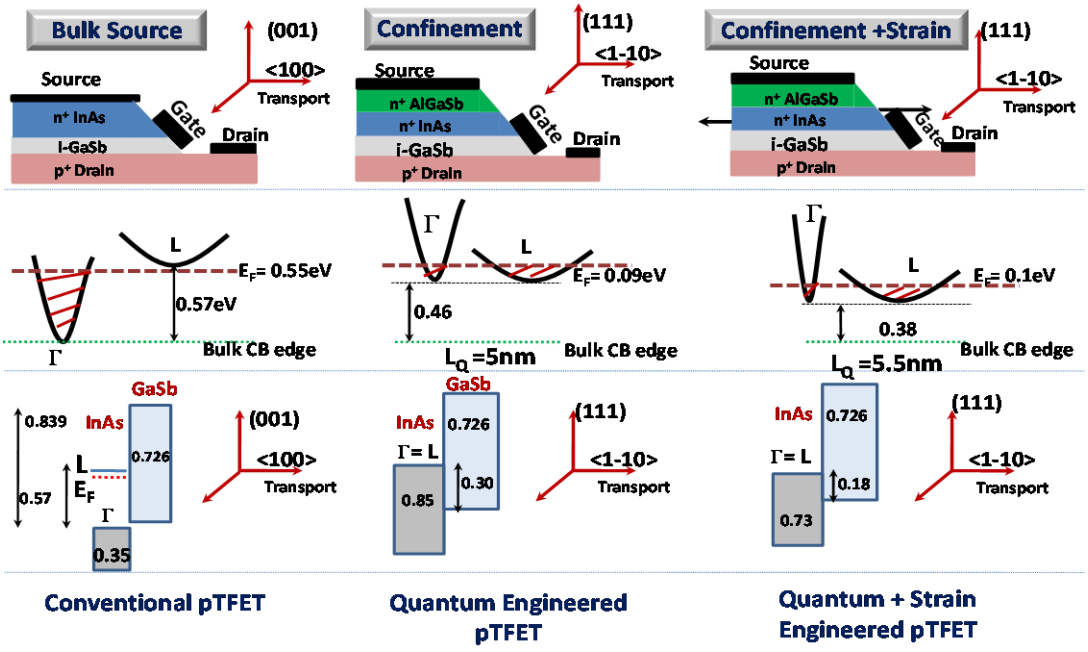

Figure 5-4. Density of States (DOS) engineered pHTFETs: Enhancing the DOS in n+ doped InAs using quantization and uniaxial strain to reduce energetic separation between L and Γ valleys while maintaining high stagger with GaSb; (Left) Unstrained and bulk InAs. (Middle) Unstrained, quantized InAs. (Right) 2% uniaxially (tensile) strained and quantized InAs configurations for high performance, steep slope pHTFETs [38].

In conventional pTFET with n+ doped (100) InAs, high source doping pushes the Fermi level away from conduction band exposing the high energy carrier distribution tail and diluting switching slope. Figure 5-4 shows numerical band structure simulations of (111) InAs using Nextnano[3] [38]. The DOS in (111) InAs source region can be increased by energetically

lowering the L-valley using a combination of quantum confinement and uniaxial strain. This novel approach preserves both the steep switching slope as well as high on-current in future p-channel HTFETs.

Figure 5-4 shows how quantum confinement can elevate the gamma valley (Γ) energetically and re-populate the L-valley with carriers. L-valley has higher DOS and allows higher source doping in the source without exposing the high energy tail of the Fermi distribution of carriers. However, our initial calculations indicate that this could potentially increase the tunnel barrier to 0.3eV and suppress on-current. Strain engineering will be needed to reduce the effective tunnel barrier and increase Ion without compromising the DOS in the source region. Various stressor techniques such as built-in epitaxial strain, capping layer, and metal gate induced strain can be investigated for strained pTFET. Finally, the effect of transition from direct to indirect gap system on the effective tunneling rate needs quantification.

5-3. In-situ Gate Stack

Antimonides and arsenides are extremely sensitive to surface oxidation leading to non-ideal high-k dielectric/III-V interface which affects the TFET switching slope. While the self-cleaning effect of TMA precursor used in Al_2O_3 dielectric deposition has proven beneficial to mitigating oxide formation with arsenides, no such effect has been observed for antimonides. Using a dual chamber ALD/PEALD deposition system, which will allow removal of surface oxide in-situ followed by ALD or PEALD high-k deposition over a wide range of temperature, is desired. This will allow for in-situ surface conditioning and conformal deposition of high-k in etched nana-pillar 3D devices geometries with high device yield.

5-4. Future Work

Complementary p-channel Tunnel FETs need heavily doped n++ source to boost the drive current comparable in performance to the n-channel counterpart. However, low DOS for the CB forms the bottleneck in achieving high Ns in III-V semiconductors. Reducing Ns is not a straightforward solution as it trades between steep SS and high I_{ON}. Bringing satellite valleys closer to the direct gap gamma valley is one way to prevent Fermi-degeneracy. Orientation dependent confinement and strain are possible technique to achieve this however this requires significant modeling and experimental validation to prove to be a robust complementary solution.

Appendix

Detailed Process Flow for Nano-pillar Tunnel FET

The fabrication details for the nano-pillar transistor are described below:

1. **Alignment Markers and Dry Etch Mask Definition**
    a. Degrease the III-V sample with Acetone (10mins), Methanol (5mins) and IPA (5mins).
    b. Rinse with DI water for 1min and blow dry with N_2.
    c. Spin coat with PMMA-MAA EL-6 resist at 2000 rpm for 1min.
    d. Bake@150^{o}C for 3min. Cool the sample for 2mins.
    e. Spin coat PMMA 950 A3 resist at 4000 rpm for 45secs.
    f. Bake @ 180^{o}C for 3 mins. Cool the sample for 2 mins.
    g. Use E-beam lithography (EBL) to write the features. Write features smaller than equal to 5x5µm^2 at dose of 900µC/cm^2 with beam size of 15nm. Write larger features with 420µC/cm^2 using beam size of 220nm.
    h. Develop the patterns using 1:3 MIBK: IPA for 1min and 45 secs followed by 20 secs dip in IPA.
    i. Rinse in DI water for 30secs and blow dry with N_2.
    j. Observe for clean and sharp patterns.
2. **Dry Etch Mask Deposition**

    In this step, pillar hard etch mask will be defined using EBL and Lift-off technique
    a. Load the developed sample into the evaporator
    b. Load Ti and Cr crucibles and wait for vacuum

c. Start depositing once the base pressure comes below 10^{-6} Torr

d. Lift-off the patterns using Remover PG preheated to 60^{o}C.

e. Rinse in IPA, DI water and then blow dry with N_2.

f. Observe under microscope for a clean lift-off.

3. Pillar Definition Using Dry Etch

In this step, pillars will be defined using Ti/Cr as the hard etch mask

a. Paste the sample on a carrier wafer using double sided thermal tape.

b. Clean the back of the carrier wafer before loading into the ICP RIE chamber

c. Load and wait for the lock vacuum to reach below 100mTorr

d. Before running the actual sample for etch, perform chamber clean followed by chamber conditioning with Cl_2 (40sccm), Ar (20sccm) and SF_6 (10sccm). RF1 PWR-250W, RF2 PWR-750W.

e. Etch Molybdenum followed by InGaAs using the same recipe. Break the entire etch into steps till bottom P++ source is reached.

f. Use Profilometer to measure the step height

g. Confirm the P++ source using multimeter.

4. Pillar Wet Etch Undercut and high-k Deposition

In this step, wet etch is performed to remove dry etch damage and produce the undercut needed for self aligned gate contact deposition

a. Rinse the dry etched sample with DI water to remove an Cl_2 residue

b. Create citric acid (100gm+100ml DI water stirred for 40mins and keep overnight) and H_2O_2 solution with 20:1 ratio. Store for 15mins.

c. Etch the sample for 1 min to produce undercut in InGaAs of around 20nm.

d. Rinse with Di water and blow dry with N_2

e. Load the sample into a preconditioned ALD chamber with the hot plate maintained at 250^{o}C

f. Close the lid immediately and bring down the pressure to 0.2Torr

g. Wait for 1 min

h. Treat the surface with 5 Cycles of TMA

i. Pulse 10 cycles of TMA and H_2O to deposit 1nm of Al_2O_3

j. Pulse 35 cycles of TEMAH and H2O in top to deposit 3.5nm of HfO_2.

k. Unload the sample and then cool down for 1min.

5. Self-aligned Gate Contact Definition and Deposition

In this step, Pd gate metal is deposited vertically in a self aligned manner using EBL, evaporation and lift-off technique

a. Spin coat with PMMA-MAA EL-11 resist at 2000 rpm for 1min.

b. Bake@150^{o}C for 3min. Cool the sample for 2mins.

c. Spin coat PMMA 950 A3 resist at 4000 rpm for 45secs.

d. Bake @ 180^{o}C for 3 mins. Cool the sample for 2 mins.

e. Use lithography to write the features. Write larger features with 420μC/cm^2 using beam size of 220nm.

f. Develop the patterns using 1:3 MIBK: IPA for 1min and 45 secs followed by 20 secs dip in IPA.

g. Rinse in DI water for 30secs and blow dry with N_2.

h. Observe for clean and sharp patterns.

i. Load into the evaporator and wait for pressure to reach below 10^{-6}Torr

j. Deposit 20nm Pd gate metal

k. Lift-off with Remover PG preheated at 60^{o}C, rinse with IPA and DI water.

l. Blow dry and observe under microscope for a clean lift-off

6. Source and Gate Pad Definition and Deposition

In this step, source and gate pad windows are created. High-k is removed and the pads are formed using EBL, evaporation and Lift-off techniques

a. Spin coat with PMMA-MAA EL-11 resist at 2000 rpm for 1min.
b. Bake@150^{o}C for 3min. Cool the sample for 2mins.
c. Spin coat PMMA 950 A3 resist at 4000 rpm for 45secs.
d. Bake @ 180^{o}C for 3 mins. Cool the sample for 2 mins.
e. Use lithography to write the features. Write larger features with 420μC/cm^{2} using beam size of 220nm.
f. Develop the patterns using 1:3 MIBK: IPA for 1min and 45 secs followed by 20 secs dip in IPA.
g. Rinse in DI water for 30secs and blow dry with N_2.
h. Observe for clean and sharp patterns.
i. Dry etch the high-k in ICP RIE using Cl_2 (20sccm) and Ar (10 sccm): RF1 Pwr: 75W and RF2 Pwr: 500W, Time: 25secs
j. Load into the evaporator with Ti, Pd and Au crucibles
k. Wait for pressure to reach below 10^{-6} Torr
l. Deposit 20nm Ti, 20nm Pd and 30nm Au.
m. Lift-off the metal with remover PG preheated @ 60^{o}C
n. Rinse in IPA and DI water and then blow dry with N_2.
o. Observe under microscope for clean lift-off.

7. Planarization and Etch back

In this step, the pillars are planarized using BCB and the BCB is etched back till the top of Mo contact for the top contact formation.

a. Spin Coat BCB @ 500rpm for 1min

b. Bake at 140^{o}C for 10mins.

c. Load into an oven with N_2 ambient while the hot plate is preset to 140^{o}C.

d. Gradually raise the temperature from 140^{o}C to 250^{o}C.

e. Cure BCB at 250^{o}C for 2 hr.

f. Unload the cured sample once the temperature is below 150^{o}C

g. Cool the sample and load into the RIE chamber.

h. Etch BCB in O_2 (80sccm) and CF_4 (20sccm), Pressure 200mT, RF-200W (Capactively coupled RIE).

i. Etch in steps until the BCB is below the pillar surface by 150nm. Check the height with Profilometer and or SEM.

8. Drain Pad Definition and Deposition

In this step, drain pads are formed in contact with the Mo on top of the pillars. EBL, E-beam evaporation and Lift-off technique is used.

a. Spin coat with PMMA-MAA EL-11 resist at 2000 rpm for 1min.

b. Bake@150^{o}C for 3min. Cool the sample for 2mins.

c. Spin coat PMMA 950 A3 resist at 4000 rpm for 45secs.

d. Bake @ 180^{o}C for 3 mins. Cool the sample for 2 mins.

e. Use E-beam lithography to write the features. Write larger features with 420μC/cm^2 using beam size of 220nm.

f. Develop the patterns using 1:3 MIBK: IPA for 1min and 45 secs followed by 20 secs dip in IPA.

g. Rinse in DI water for 30secs and blow dry with N_2.

h. Observe for clean and sharp patterns.

i. Remove O_2 plasma induced native oxide with high-k etch recipe for 25 secs.

j. Load into the evaporator with Ti, Pd and Au crucibles.

k. Wait for the pressure to reach below 10^{-6} Torr.

l. Deposit 20nm Ti, 20nm Pd and 60nm Au.

m. Lift-off in Remover PG preheated at 60^{o}C.

n. Rinse in IPA and DI water.

o. Blow dry with N_2 and Observe under microscope for a clean lift-off.

9. Remove unwanted BCB

In this step, unwanted BCB exposed anywhere else is removed using dry etch

a. Load into the dry etch chamber.

b. Etch BCB in O_2 (80sccm) and CF_4 (20sccm), Pressure 200mT, RF-200W (Capactively coupled RIE).

c. Etch for 1min and 30 secs until any remnant BCB on top of source and gate pads are removed.

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VITA

Dheeraj K Mohata

Dheeraj Mohata hails from Bhubaneswar (BBSR), renowned as the city of Temples in East India and the present capital of the state of Odisha. He did his elementary schooling from Maharishi Vidya Mandir and high school from Maharishi College of Natural Law, BBSR. Dheeraj received his B.S. degree in Instrumentation and Electronics Engineering from the College of Engineering and Technology, BBSR, India, in 2006 and then went to pursue Masters degree at the Indian Institute of Technology Kanpur, India. He received his M.S. degree from the department of Electrical Engineering in 2008. He then moved to Pennsylvania State University, University Park, PA and joined the research group of Dr. Suman Datta in 2009 where he worked towards his doctorate degree in the field of Tunneling Transistors for low power logic applications. In 2013 he obtained the Ph.D. degree from the Department of Electrical Engineering at Penn State. After his PhD, he is headed to RFMD where he will be working as Senior Device Engineer in the Device Development group in Greensboro, NC.

During his PhD, Dheeraj published 8 journal and 9 conference papers with 6 first author publications among them. He was awarded the prestigious IBM PhD Fellowship, an intensely competitive program which honors exceptional Ph.D. students worldwide. Recently he was awarded the Melvin P. Bloom Outstanding Doctoral Research Award in Electrical Engineering
The award recognizes outstanding achievement in scholarship and professional accomplishment, and he was honored to be one of the two graduate students within Electrical Engineering at Penn State to receive the award. He can be contacted at his email dkm016@gmail.com.