INVESTIGATING ALTERNATIVE SACRIFICIAL CHANNEL MATERIALS FOR GROW-IN-PLACE ENCAPSULATED SILICON NANOWIRES

A Thesis in
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by
Zakaria Y. Al Balushi

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The thesis of Zakaria Y. Al Balushi was reviewed and approved* by the following:

Stephen J. Fonash  
Bayard D. Kunkle Chair Professor in Engineering Sciences  
Thesis Advisor

Mark W. Horn  
Professor of Engineering Science and Mechanics

Wook Jun Nam  
Research Associate, Center for Nanotechnology Education and Utilization  
Special Signatory

Judith A. Todd  
P. B. Breneman Department Head  
Head of the Department of Engineering Science and Mechanics

*Signatures are on file in the Graduate School
ABSTRACT

Nanowires have become of great interest for many applications in different fields of science and engineering. They have many interesting properties, such as high surface area to volume ratios and tunable electrical properties. These properties make nanowires ideal for integration into electronic and optoelectronic high performance devices. Nanowire-based logic devices are still in an embryonic stage and more research is needed for the integration of nanowire building blocks into CMOS technology. For the potential future of semiconductor nanowires in very-large-scale-integrated VLSI circuits, the challenge of high density alignment and precise placement of nanowires for individual device control must be addressed.

The “Grow-in-Place” approach for encapsulated nanowires can overcome some of the limitation of post-growth integration of these one-dimensional materials by essentially combining growth and integration into a single step. In order to build robust nanowire FETs, precise control over the in-plan growth of the nanowires must be realized. The grow-in-place approach can provide an excellent platform for innovative nanowire based TFTs. This thesis is intended to investigate alternative sacrificial materials to fabricate nanochannels for in-plane growth of encapsulated SiNWs using the grow-in-place approach. The objective is to advance the current grow-in-place approach that has been proposed by the Fonash Research Group. This keen interest in optimizing the approach is important in order to make encapsulated growth of SiNWs commercially feasible and economical for high volumetric device integration of nanowire FETs that will enhance the performance of current CMOS technology.
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CHAPTER 1

Introduction to Semiconductor Nanowires

1.1 Motivation

The future generation of advanced nanowire-based logic devices will potentially lead the pathway to new high-performance functional systems. These systems will complement and possibly replace current planer bulk complementary-metal-oxide-semiconductor CMOS technology. The top-down fabrication approach has continued to be most successful in the microelectronics industry for many years. But given the increasing demand for evermore compact electronic systems and high dense silicon integrated circuits, the top-down fabrication approach used to scale down semiconductor materials and metal/gate-oxide structures to critical dimensions in the nanometer domain has created new challenges on material performance and consequently device operation. Such technological challenges for electronic nanoscale devices includes lithography, etch and surface roughness limitations to random dopant fluctuations within aggressively scaled down material lattice structures.

In addition, CMOS technology relies heavily on the high-performance of integrated silicon-based devices. With the increasing economic constraints associated with current state-of-the-art lithography techniques that are used to fabricate such high-density semiconductor integrated units, a call for an increase in research efforts for alternative fabrication approaches for high-performing nanoscale devices has been intensified. Bottom-up synthesis of nanostructures has been given consideration to be
utilized to produce nanoscale devices due to the simplicity of the approach, the high yield and minimal apparatus requirements\textsuperscript{6}.

The synthesis of semiconductor nanowires through the bottom-up approach has become of great interest for many applications in different fields of science and engineering. They have many interesting properties due to their high surface area to volume ratios and tunable electrical\textsuperscript{7}, optical\textsuperscript{8, 9} and mechanical\textsuperscript{10} properties. These properties make semiconductor nanowires an attractive integration component for high-performance electronic devices such as for the active channel material in accumulation metal-oxide-semiconductor field-effect transistors AMOSFETs\textsuperscript{11}.

Moreover, the integrated CMOS device platform requires the precise addressability and control of individual devices\textsuperscript{12}. Therefore, in order for semiconductor nanowires to become key building blocks for sub-20-nm pitch high volumetric manufacturing HVM, control over various aspects of the nanowire growth, surface roughness and impurity incorporation at the atomic-level is critical. This is important for the fabrication and integration of the next generation of low-power, high-speed nanowire-based logic device.

From the semiconductor industry’s point of view, nanowire-based logic devices are still in an embryonic stage and more research is needed for the integration of nanowire device building blocks into CMOS technology. For the potential future of semiconductor nanowires in very large scale integrated VLSI circuits, the challenge of high density alignment and precise placement of nanowires for individual device control must be addressed. Although there may be ample examples of two- and even three-dimensional high-density nanowire array integration, current opportunities for large scale
introduction and device addressability at the single nanowire level is somewhat limited\textsuperscript{13}. This is due to the difficulty of post-growth integration of individual semiconductor nanowires. The integration approach for nanowire building blocks in this matter is known as the “Grow-and-Place” approach.

More importantly throughout the years, it has been clear that both top-down fabrication and bottom-up synthesis are necessary for the future of nanowire building blocks for CMOS devices\textsuperscript{14}. Therefore, there is a need for nanowire growth to occur in-conjunction with device integration; an approach known as “Grow-in-Place”\textsuperscript{15,16}. This ability to grow silicon nanowires within device architectures using the grow-in-place approach and with near-atomic perfection is the theme of this thesis.

Evidently, the degree to which one can control and modify nanowire growth parameters is not only crucial in obtaining uniform properties at the atomic level, but also reproducible device performances. Aside from the control over the growth mechanism of silicon nanowires, the rational engineering that goes into the fabrication of the device architectures, in which nanowire growth and integration is achieved, plays an influential role in determining final device performance. With engineering optimization and an excellent understanding of template growth of semiconductor nanowires\textsuperscript{17}, the grow-in-place approach can provide an excellent platform for innovative nanowire based Thin Film Transistors TFT that could potentially enhance the VLSI sector. This can only be accomplished if both bottom-up and top-down techniques are used in tandem.

Before embarking into the core focus and results of this thesis, key concepts related semiconductor nanowires will be discussed within this and proceeding chapters. The sections in this chapter and the following will provide the essential background that
is necessary to understand the properties of semiconductor nanowire growth and device integration. Discussion on the fundamental challenges associated with utilizing these one-dimensional building blocks and related impact work of these nanostructures will be provided in detail through this thesis.

1.2 Semiconductor Nanowire Synthesis

Semiconductor nanowires are a class of one-dimensional nanomaterials that exhibit a very high surface-to-volume ratio and fairly small diameters. One-dimensional electronic nanostructure materials can be defined as material systems in which, the mean free path of the charge carries is greater than the available lengths in two spatial dimensions\(^{18}\). This allows the transport properties of the charge carriers to be confined in one-dimension. With the high surface-to-volume ratio of these one-dimensional nanostructures, the interface and surface phenomena in semiconductor nanowires tend to dominate over their bulk effects\(^{19}\). This results in interesting crystal anisotropy within the composed material structure. In addition, the reduced size of these nanostructures play an important role in fundamentally changing the electronic band structure of the semiconductor material from that of the bulk. The radial dimensions of semiconductor nanowires are typically less than 100nm in diameter and are composed of one or several intrinsic or extrinsic semiconductor materials\(^{14}\).

First reports on the growth of semiconductor whisker materials “known today as nanowires” can be dated back to an article published in the late 1950s, where R. G. Treuting and S. M. Arnold reported the successful synthesis of <111> oriented Silicon as
well as $<111>$ and $<112>$ oriented Germanium whisker structures$^{20}$. These whiskers were produced using a vapor deposition technique. Over the years, a variety of inorganic elemental and compound semiconductor stacks have also been successfully grown into one-dimensional nanowire architectures$^{21}$. This ability to grow low dimensional highly anisotropic epitaxial layers has led to various examples of these one-dimensional nanomaterials in sensing$^{22,23}$, electronic$^{24,25,26,27,28,29}$, opto-electronic$^{30,31,32,33}$ and many power generation$^{34,35}$ applications. Table 1-1 provides some examples of advanced material systems where nanowire synthesis has been realized.

Both semiconductor nanowires and carbon nanotubes CNTs have appeared alongside each other as prospective building blocks for nanoscale electronic devices. Yet, unlike the metallic or semiconducting nature of CNTs, the properties of semiconductor nanowires are determined by the semiconductor material system in which they are made from$^{36}$ and not from the number of walls and/or fold orientation like in CNTs. Semiconductor nanowires are more attractive than CNTs because their electrical properties are much easier to control and as long as the surface of these nanowires are passivated, they are consistently semiconducting in devices$^{37}$. Such semiconductor nanowire structures have been customarily realized through both top-down fabrication and bottom-up synthesis approaches. A great deal of effort has been focused on developing and optimizing methods for bottom-up chemical synthesis and in particular the chemical vapor-phase growth of semiconductor nanowires. This is due to facile control of many aspects of the nanowire growth that are important for the rational engineering of new and novel high-performance devices such as the aforementioned applications$^{38}$. 
Much difficulty has hindered the rapid development of nanoscale devices based on these one-dimensional nanomaterials. One of the fundamental limitations in using nanowires as building blocks for different devices and applications is developing well defined structures with homogeneous properties. These difficulties will be discussed in detail in the following sections.

First, a few methods used to fabricate silicon nanowires through the top-down approach will be presented in the next section. This section will then be concluded with an outline of the limitations of the top-down approach in producing nanowire building blocks for electronic device applications and in particular transistor architectures. The proceeding section will then provide the details of chemical vapor-phase growth of semiconductor nanowires. It will be pointed out that chemical vapor-phase growth of semiconductor nanowires is the best choice when nanowire electronic devices are envisaged. This is due to the controllability and versatility of the approach that relates to the resulting morphology and electrical properties.

Table 1-1: Examples of material systems that have been developed into one-dimensional nanowire structures with potential applications that commonly appear in the literature. This table was adapted from Ref\textsuperscript{38}.

<table>
<thead>
<tr>
<th>Nanowire Material System</th>
<th>Potential Application Area</th>
</tr>
</thead>
<tbody>
<tr>
<td>Silicon (Si)</td>
<td>Electronics, Biosensors, Solar cells</td>
</tr>
<tr>
<td>Germanium (Ge)</td>
<td>Electronics, IR detectors</td>
</tr>
<tr>
<td>Gallium nitride (GaN)</td>
<td>High-temperature electronics, Lasers, Sensors</td>
</tr>
<tr>
<td>Boron nitride (BN)</td>
<td>Insulator</td>
</tr>
<tr>
<td>Gallium arsenide (GaAs)</td>
<td>Electronics</td>
</tr>
<tr>
<td>Indium phosphide (InP)</td>
<td>Electronics, Opto-electronics, Lasers</td>
</tr>
<tr>
<td>Zinc selenide (ZnSe)</td>
<td>Photonics</td>
</tr>
<tr>
<td>Indium(III) selenide (In\textsubscript{2}Se\textsubscript{3})</td>
<td>Phase change memory device</td>
</tr>
<tr>
<td>Germanium telluride (GeTe)</td>
<td>Phase change memory device</td>
</tr>
<tr>
<td>Cadmium telluride (CdTe)</td>
<td>Solar cells</td>
</tr>
</tbody>
</table>
Although many of the synthesis and features of nanowires that will be discussed in this thesis applies to many semiconductor material systems, this chapter will primarily focus on discussing the synthesis of silicon nanowires SiNWs and their prominent structural and electrical properties. Understanding the rational design and synthesis that goes into semiconductor nanowires is critical to the work of this thesis, as it is directed towards the deployment and improvement of the grow-in-place approach of SiNWs for transistor device integration.

1.2.1 Top-down Fabrication of Semiconductor Nanowires

For a semiconductor material system such as the silicon diamond cubic crystal structure, atomic bonding is relatively isotropic. In general, to achieve one-dimensional nanostructures, it is required that the symmetry of the crystal structure be broken or confined in two-dimensions during fabrication or growth. The top-down fabrication approach for SiNWs is fundamentally an extension to the well-established fabrication processes that rely heavily on patterning techniques used in the microelectronics industry. These techniques often utilize different lithographic approaches in conjunction with a combination of sophisticated chemical and/or physical etch steps as well as material deposition on planer substrates. Using conventional top-down fabrication approaches, silicon nanostructures can be formed from bulk material.

As will be seen, a particular challenge associated with the top-down approach for fabricating one-dimensional nanostructures is that as structures decrease in size, defects associated with the utilized etch and/ or patterning technique become increasingly
problematic on device performance. In addition, due to the spatial resolution limits of different optical lithographic techniques, patterning surfaces for sub-100nm structures can be rather challenging.

1.2.1.1 Surface Patterning Techniques

There are many methods used to fabricate one-dimensional structures from thin film materials. The improvements of optical masks and chemically amplified resists have been the most significant innovations introduced to enhance the resolution of optical lithography\(^5\),\(^18\). But due to the diffraction and light scattering limitations of optical lithography, sub-100 nm features are challenging to achieve. Therefore, much effort has been centered towards the production of Nano-Imprint Lithography NIL and mask-less lithography techniques such as Electron Beam Lithography EBL, as an alternative approach to pattern sub-100 nm semiconductor nanowire elemental building units from bulk materials\(^40\).

As mentioned above, EBL can be used to obtain highly ordered silicon nanowire features\(^41\). This process begins by defining high resolution patterns using a beam of electrons of a particular spot size, accelerating voltage and dose, on specially designed resist materials. Such resist materials include organic polymers\(^42,43\), inorganic materials\(^44\) as well as self-assembling monolayers SAMs\(^45,46\). For polymeric resist materials, particular reactions or processes are induced upon electron beam exposure. Such reactions include molecular cross-linking, polymerization, molecular chain scission and/or acids/base chemical amplifications\(^47\). A list of common resist materials used in
EBL is illustrated in Table 1-2. These resist materials are conventionally spin coated directly onto planar substrates containing the material in switch pattern transfer is desired.

Table 1-2: Examples of conventional electron beam lithography resist materials with their corresponding tone and dry etch resistance. These resists were chosen because they commonly appear in the literature.

<table>
<thead>
<tr>
<th>Resist Material</th>
<th>Tone</th>
<th>Etch Resistance</th>
</tr>
</thead>
<tbody>
<tr>
<td>PMMA</td>
<td>Positive</td>
<td>Poor</td>
</tr>
<tr>
<td>ZEP Series</td>
<td>Positive</td>
<td>Good</td>
</tr>
<tr>
<td>P(MMA-MAA)</td>
<td>Positive</td>
<td>Poor</td>
</tr>
<tr>
<td>EBR-9</td>
<td>Positive</td>
<td>Poor</td>
</tr>
<tr>
<td>NEB-31</td>
<td>Negative</td>
<td>Good</td>
</tr>
<tr>
<td>HSQ</td>
<td>Negative</td>
<td>Good</td>
</tr>
<tr>
<td>ma-N</td>
<td>Negative</td>
<td>Good</td>
</tr>
<tr>
<td>APEX-E</td>
<td>Positive</td>
<td>Good</td>
</tr>
<tr>
<td>SAL-601</td>
<td>Negative</td>
<td>Fair</td>
</tr>
<tr>
<td>UV-5</td>
<td>Positive</td>
<td>Good</td>
</tr>
</tbody>
</table>

Prior to resist coating, silicon of high crystallinity can be grown or deposited onto planar substrates using Molecular-Beam Epitaxy MBE, Vapor-Phase Epitaxy VPE, Liquid-Phase Epitaxy LPE growth or other material deposition methods prior to resist coating. After material deposition and resist coating is performed, the solvent-rich resist undergoes a post-apply bake, also called a soft-bake or pre-bake, to remove the excess solvent that typically dilutes the electron beam resist. The removal of the solvent results in the reduction of the resist film thickness and improves resist adhesion to the substrate. Also, post-apply bake plays a crucial role in determining the reaction properties of the resist that will be exposed to an electron beam as well as final post-exposure baking and development times. After the post-apply bake, exposing areas of the resist to an electron beam source allows for selective development of patterns. These patterns are used for
nanowire fabrication by chemical or physical etch transfer. The resulting resolution and minimum achievable feature size of the developed patterns depends on the initial electron beam spot size, the resolution and etch resistance of the resist and the post-exposure bake and development conditions. Moreover, the practical resolution of EBL is also determined by proximity effects in the resist material that are resulted from the generation of back scattered electrons from the substrate\textsuperscript{49}. Depending on how insulating the substrate is, metal and other conductive layers are typically deposited on top of the resist to reduce charge build-up. Nobel metals or conductive polymers can be used to fulfill such tasks. These conductive layers are always removed prior to resist development of the electron beam exposed sample.

Similarly, the above mentioned process flow for surface patterning can be reversed. That is, the resist patterns can be defined first with EBL without prior material on the substrate. Through creating well-defined surface patterns with some degree of resist undercut, material deposition using a Physical Vapor Deposition PVD technique - such as thermal or e-beam evaporation- or thin film growth using a Chemical Vapor Deposition CVD process can be performed. After material transfer, a lift-off process is done in common resist removal solvents. This leaves behind precisely positioned patterned nanowire structures of the transferred material on the substrate.

Evidently, EBL can be replaced with NIL or other techniques capable of forming etch or lift-off masks for a variety of materials. With NIL, residual resist material must be removed prior to material transfer. This is achieved by using common oxygen plasma descum processes.
In addition, there have been examples of using polystyrene particles to pattern vertical nanowire structures; an approach known as colloidal lithography. A single layer of monodispersed micron-size particles or nanospheres can be arranged in an array by spin coating from solution. The single layer of particles acts as a mask for the under-layer in which nanowire-like structures will be formed. After partial removal of the particle top layer by plasma ashing, metal is deposited in-between the particles. The deposited metal acts as a catalyst to assist in the wet-etch of the material of the underlying material; a process known as metal-assisted etching. Typically vertical nanowires are achieved using this fabrication route, but other architectures are potentially possible.

Figure 1-1: The provided schematic illustrates a generic process flow for fabricating either vertical or horizontal nanowire structure: A) top-down fabrication process flow utilizing EBL and B) top-down fabrication process flow utilizing NIL.
From Figure 1-1, the aforementioned surface patterning techniques requires further processing of material removal, by either wet chemical etch or physical etch or a combination of the two. The next two sections will discuss in more detail some of the most important etch processes used in top-down fabrication for silicon nanowires.

1.2.1.2 Chemical and Physical Etch

Chemical etch techniques represents one of the most important top-down fabrication routes for the formation of one-dimensional semiconductor nanostructures. It has been demonstrated that direct etch transfer from preliminary pre-defined patterns, which have been lithographed onto the surface of bulk semiconductor materials, can be achieved to feature sizes below 20nm. This can be done through the use of highly selective isotropic and at times anisotropic etchants. Chemical etch involves reactions that attack and remove materials either in the liquid-phase such as in wet etch chemistry processes or in the vapor-phase using chemically active ionized plasma gas species. Such etch techniques require good adhesion with the etched material, making the hardmask or resist the only controlling interface in the process. In the 1960s, it has been found that single crystal silicon exhibits wet etch rates that are not only concentration dependent but also orientation dependent within individual crystal planes. When KOH is used as an etch solution, it has been observed that the etch rate along the \{111\} crystal family planes are much slower than the etch rates in the \{100\} and \{110\} crystal planes. This allows for high aspect ratio structures and v-grooves to be achievable in silicon.
The resulting dry chemical etch process of materials from reactive ionized gas species, is referred to as Reactive Ion Etch RIE. Reactive ion etching of materials is performed routinely in reactors under low pressure conditions. Particular gases are sequentially introduced into the reactor. These gases are ionized typically in the presences of a strong RF powered magnetic field produced in-between conductive plates in Capacitance Coupled Plasma CCP systems or within the coils in Inductive Couple Plasma ICP systems. This results in the generation of plasma in which the ions accelerate towards the substrate and selectively chemically etch the desired material on the sample. If the impinging ions have enough energy through reactor biasing, high physical bombardment onto the sample can occur. This result in the physical etch portion of the RIE which is highly anisotropic. One can control the “selectivity and directionality” and hence the etch rate and profile of the resulting nanowire structure via the RIE process by tailoring the physical bombardment through biasing and collectively tuning the gas concentration in conjunction with the reactor pressure.

1.2.1.3 Advantages of Top-down Approach

There are many examples of top-down fabrication of vertical and planar silicon nanowire structure using a combination of lithographic and etch techniques\textsuperscript{55,56}. The benefit of top-down fabrication of silicon nanowires is its compatibility with standard IC technology. Explicitly, it is possible to produce devices without the need for post-alignment and integration. Other key advantages of the top-down approach includes the ability to use well-established techniques for device contact formation as well as high
achievable doping densities that are required for different device concepts such as the junction-free nanowire transistors\textsuperscript{57}.

Although the top-down approach presents good advantages for forming silicon nanowire building blocks for logic devices, in-particular concerning single device integration and addressability, there are inherit limitations of the approach. This will be discussed in the next section.

1.2.1.4 Limitation of Top-down Approach

The top-down approach to obtain silicon nanowires using EBL with a combination of physical and chemical etch processes has some drawbacks. First, EBL is a serial process and therefore has a low throughput capability that is not suitable for heavy use in HVM of VLSI devices. Though, EBL has been extensively utilized in this research project, the technique itself can be substituted for NIL techniques or other more cost effective lithographic methods. EBL in this thesis serves as a research tool and provides high resolution patterning of sub-100 nm features and was the only lithographic tool capable of such performance that was available at the time. There have been many improvements to writing speeds of EBL. This tool is not intended as a mean for HVM, unless more improvements with EBL are done to reduce its economic cost.

In addition to EBL being a high-cost fabrication technique, further economic costs associated with the top-down approach comes from the high cost of current used silicon-on-insulator SOI wafers. Moreover, producing sub-10 nm nanowire features have proven difficult to achieve using the top-down fabrication approach. This creates a limitation for
high density semiconductor nanowire formation and hinders bandgap engineering in silicon nanowires that will be discussed in later sections.

Moreover, while developments continue to push the resolution of lithography tools for top-down fabrication, conventional etching of nanostructures using anisotropic dry-etch transfer of very small and highly dense surface patterns has proven to be difficult. As mentioned previously, the chemical etch rate of silicon is dependent on the crystal plane of the bulk material. This can produce problems with etch profiles and potential etch uniformity. Other effects that can hinder silicon etching includes; notching due to charge accumulation$^{58}$, micrograss due to residual resist redeposition and more importantly loading effects. The loading effect is a phenomena that produces etch rate variations that are a direct result of differences in pattern density, particularly when scaling to larger wafers$^{59}$. The discussed effects can be detrimental to producing uniform nanowire building blocks for high-performance devices.

From the top-down approaches as discussed in this section, we are able to observe the different techniques and steps required to fabricate such one-dimensional nanostructures. Though top-down fabrication present some advantages, it suffers from a number disadvantages as well. This will be clearer to the reader when comparing top-down to bottom-up vapor-phase synthesis as will be seen in the following sections.
1.2.2 Bottom-up Synthesis of Semiconductor Nanowires

There are many routes for bottom-up synthesis of nanowires of different material systems. The growth process used to synthesize semiconductor nanowires must be able to support preferential growth in one-dimension. Therefore, for semiconductor nanowire synthesis to occur, a reversible condition near equilibrium must be maintained between atoms in the solution, melt or vapor phase and atoms in the solid phase\textsuperscript{60}. These atoms in the solid phase must have high surface or bulk mobility in order to promote one-dimensional crystal growth. Approaches for bottom-up synthesis of SiNWs can be separated into two categories: These categories are liquid-phase synthesis and vapor-phase synthesis techniques.

Liquid-phase synthesis utilize template and template-free growth approaches. Some examples of this technique include hydrothermal nanowire synthesis, electrodeposition and sol-gel processes\textsuperscript{38}. Vapor-phase synthesis of SiNWs has been the primary bottom-up route for growing high crystalline quality nanowires. This is based on the facile control over the growth parameters that are necessary for high-performance nanowire logic-based devices. The following section will provide some insight into vapor-phase growth used to produce semiconductor nanowires.

1.2.2.1 Vapor Phase Catalyzed Growth

There are many bottom-up growth techniques in which vapor-phase synthesis of SiNWs has been achieved. The different vapor-phase techniques merely differ in which the silicon material is supplied for nanowire growth. These two possibilities are either
elemental silicon directly replenished into the nanowire synthesis or silicon supplied indirectly through an intermediate chemical reaction step of gas-phase molecules. The latter case being more attractive for SiNW growth using foreign metal catalytic materials as the growth mediator and is the preferred method in this thesis. These molecules and/or compound materials are often referred to as precursors and are typically oxygen-free.

Some common bottom-up vapor-phase techniques include evaporation, pulsed laser ablation, MBE, reactive atmospheric annealing of source material, arc discharge and chemical vapor deposition CVD\textsuperscript{61}. Semiconductor precursors are generated from solid targets in MBE, through momentum transfer as in pulsed laser ablation and through chemical decomposition in CVD. CVD has not only been the first technique utilized for nanowire synthesis, but has also been the most successful and widely used growth technique for single crystal nanowires which are necessary for transistor devices.

Typically, CVD metal catalytic supported synthesis of SiNWs takes place in a reactor operating low pressure. The growth substrates are placed downstream to the vapor source, in which reactive species deposit into the metal catalyst host. Each vapor-phase technique developed for nanowire growth is fundamentally achieved through different crystal growth mechanisms. These mechanisms include Vapor-Liquid-Solid VLS and Vapor-Solid-Solid VSS growth mechanisms as well as other analogues mechanisms such as Solution-Liquid-Solid SLS, Supercritical Fluid-Solid-Solid SFSS, Supercritical Fluid-Liquid-Solid SFLS and Oxide-Assisted-Growth OAG mechanisms\textsuperscript{61}.

The VLS and VSS nanowire growth mechanisms rely on semiconductor precursors that are in the gas-phase. These precursor “species” of the nanowire material impinge on a liquid phase metal catalyst that has been deliquescing during the growth
process from which directional nanowire growth can proceed. The thermodynamics, driving forces and kinetics of the VLS and VSS growth mechanisms will be discussed in the following sections.

1.2.2.1 Vapor-Liquid-Solid

The VLS mechanism used to grow SiNWs was pioneered in the early 1960s at Bell Telephone Laboratories by R. S. Wagner and W. C. Ellis to fabricate single crystal silicon whiskers, and has been regarded as the most successful method in fabricating large quantities of high quality single crystal semiconductor nanowires\textsuperscript{62}. In their work, metal clusters “referred to as catalysts” were used to enhance the selectivity of the vapor-phase precursors in the catalyst to that of the substrate. This approach is often referred to in the literature as catalyst-assisted VLS growth for semiconductor nanowires. The VLS mechanism represents the core research of this thesis project. This growth mechanism can be applied to a broad range of advance semiconductor material systems.

VLS growth presented here is customarily realized in a low-pressure chemical vapor deposition LPCVD reactor containing gas-phase precursor molecules and dopants. These precursors and dopants must be able to form a eutectic compound within the chosen metal nanocatalyst material. In other terms, the precursor molecules and dopants must be able to crack the surface of the nanocatalyst to thereby supply silicon and dopants into the metal and form an alloy. To better illustrate this process, the binary phase-diagram of Au-Si and a schematic of the growth mechanism is provided in Figure 1-2 (A through C). In the phase diagram, Au is used as the metal nanocatalyst material
and is sometimes referred to as the “seed” or precursor “sink” material. These terms describing the metal cluster will be used interchangeably throughout the chapters.

Figure 1-2: This figure provides an overview of the vapor-phase process for SiNW growth: A) Vapor-Liquid-Solid vertical nanowire growth utilizing a metal nanocatalyst on a supporting nanowire substrate (courtesy of Lauhon Research Group); B) FESEM image of a SiNW synthesized via Au catalyzed VLS growth in a hot-walled LPCVD @ 470 C. This image was taken at 5 kV and B) Phase diagram of Au-Si. Dashed line indicates the eutectic temperature for Au-Si to be 363 C.\textsuperscript{63}
When the LPCVD reactor is heated above the eutectic temperature of the metal nanocatalyst material, the VLS process begins by preferential decomposition of the gaseous precursors and dopants at the vapor-liquid interface, leading to the saturation and formation of a liquid eutectic. Sequential decomposition leads to the formation of a supersaturated metal nanocatalyst. The eutectic point on the phase-diagram in Figure 1-2C represents the supersaturated stage, where liquid nanocatalyst, solid silicon and dopants if present, are all in equilibrium. Once the metal nanocatalyst reaches supersaturation, precipitation and nucleation of the solid, crystalline silicon nanowire out of the supersaturated liquid nanocatalyst occurs. The vertical growth of the silicon nanowire is enhanced with the catalytic -Au-Si- alloy at the tip of the nanowire with the continued incorporation of the gas-phase precursor. Furthermore, the radial dimension of resulting nanowire is proportional to that of the size of the nanocatalyst material. Final lengths of the nanowires are determined by the amount of time the tip-led growth is allowed to proceed. By combining the pressure \( p \) and temperature \( T \) dependence of the SiNW growth, one can estimate the growth velocity \( v \) for Au-catalyzed SiNWs with the following equation, Ref\(^61\):

\[
v \approx 1.7 \times 10^6 \frac{nm}{s \, mbar} \, p \, e^{-\frac{9500 K}{T}}
\]

The equation above combines the temperature and pressure growth rate dependence of Au catalyzed SiNWs from both the work of Schmid H. et al.\(^{64}\) and the work of Lew K. K. et al.\(^{65}\) on nanowire growth via Al templates. This equation to estimate the growth velocity of the SiNWs is applicable to template free growth and could possibly be used to estimate growth velocities for encapsulated SiNWs.
Typically for CVD growth of SiNWs via the VLS process, the most frequent oxygen-free precursors utilized are silane SiH\textsubscript{4}, disilane Si\textsubscript{2}H\textsubscript{6}, dichlorosilane SiH\textsubscript{2}/Cl\textsubscript{2}, and tetrachlorosilane SiCl\textsubscript{4}. During growth, chlorinated silanes can react with H\textsubscript{2} that is typically supplied to the tubular hot-wall reactors for precursor dilution. The reaction can form HCl gas that can effectively etch the substrate and the nanowire base. This however can be a desirable outcome depending on the application. For example, HCl can etch away unwanted oxide material on the substrate or on the side walls of the nanowire.

In addition, though chlorinated silanes are general more chemically stable than non-chlorinated silanes gases\textsuperscript{66}; they require higher growth temperature ranges to participate in nanowire growth via metal seeds. For example SiCl\textsubscript{4} growth temperature ranges between ~800\textdegree{}C to beyond 1000\textdegree{}C, when compared to low temperature growth of nanowires with SiH\textsubscript{4}, with growth ranges of ~350\textdegree{} – 600\textdegree{}C. More importantly, these growth ranges directly depend on the chosen metal catalytic material utilized for the growth. The precursor molecule temperature range dependence is due to the fact that SiNW growth is a thermally activated process; there is a decomposition reaction of the precursor molecule before it can diffuse into the catalyst and participates in the growth. It has been reported by Wagner et al. that the activation energy of Au-catalyzed SiNW growth using SiCl\textsubscript{4} is approximately 1.38 ± 0.06 eV\textsuperscript{67}. Schmid et al. reported reduced activation energy for Au-catalyzed with a SiH\textsubscript{4}\textsuperscript{64}. For growth temperatures ranging between 450\textdegree{} – 600\textdegree{}, a deduced activation energy of 0.82 ± 0.07 eV was observed. This is a direct result of the Arrhenius-type exponential dependence of the SiNW growth to the precursor molecule process temperature.
Moreover, throughout the growth, one can switch between different semiconductor precursors molecules and dopants supplied to the reactor. Due to radial strain relaxation of the one-dimensional geometry of the nanowire, in-situ axial and radial homo- and hetero-structures can be achieved. The ability to dope semiconductor nanowires will be discussed in detail in the upcoming sections.

### 1.2.2.1.2 Vapor-Solid-Solid

The Vapor-Solid-Solid VSS growth mechanism has been observed and extensively reported in the literature for SiNWs. Growth of such nanowires is realized bellow the bulk eutectic temperature of the metal catalyst/semiconductor alloy. When growing nanowires using the VSS mechanism, the metal catalyst stays in the solid phase throughout the growth process, hence the term: Vapor-Solid-Solid. This growth mechanism particularly occurs as a result of the insufficient saturation of the catalyst below the eutectic temperature. Therefore, the phase of the metal nanocatalyst during and after growth is always the same. Growing nanowires via VSS can be relatively slow, when compared to the VLS growth mechanism. Moreover, it is very hard to distinguish between the two growth mechanisms, particularly at growth temperatures close to the eutectic temperature of the metal nanocatalyst.

There are some advantages of VSS growth for SiNWs over VLS that have been reported in the literature. The reduced growth temperature can be beneficial when considering a low-thermal processing budget for the production of logic-devices. Generally, metal nanocatalysts on supported substrates can agglomerate during the
growth process. That is, larger catalysts tend to grow in the expense of smaller diameter catalysts. This phenomenon is referred to as Oswald ripening and is dependent on the diffusion rate in-between adjacent catalyst material. Due to the low VSS growth temperature, nanocatalyst ripening by diffusion can be better managed. This is because the nanocatalysts maintain their solid phase throughout the growth process. This also could potentially help control the diameter distribution of the nanowires throughout their growth.

Furthermore, VSS may yield nanowires of higher crystal quality and of abrupt junction interfaces for nanowire homo- and hetero-structures. This will be further understood, as we progress in the discussion on the solubility behavior of the metal nanocatalysts that are utilized for vapor-phase growth of SiNWs.

### 1.2.2.2 Metal Catalysts for Silicon Nanowire Growth

The most remarkable aspect of VLS nanowire growth is its universality. That is, it can be applied to many semiconductor material systems, utilizing different metal seeds. In VLS nanowire growth, the diameter of the nanowire is controlled via the size of the metal nanocatalyst. During the growth processes the nanocatalyst undergoes morphological and phase changes from its initial state when in contact with the substrate, to that when on the tip of the final length of the nanowire. As mentioned previously, metal nanocatalysts, which are typically supported on substrates, enhance the selectivity of the gas-phase species and allow material solubility for one-dimensional nanowire growth to occur. The main underlying principle for traditional VLS tip-lead nanowire
growth is that the corresponding solubility behavior of the nanocatalyst must be sufficiently reactive to the precursor molecules and dopants that are present in the vapor-phase. One can use thermodynamic and kinetic arguments to understand the catalytic action of metal seed as well as the rules of nucleation and growth for single nanowires. Nucleation from a supersaturated nanocatalyst must be well comprehended in terms of factors that enhance the dissociative adsorption of the gas-phase precursors. To truly understand the catalytic action of the utilized metal seeds for VLS nanowire growth, we must look into the various competing processes that occur during the growth of nanowires in an LPCVD reactor. A schematic in Figure 1-3 below provides the various adsorption and desorption processes that occurs and is as follows: (1) distribution of the gas-phase precursors that are fed into the reactor; (2) adsorption and desorption processes of gas-phase precursors at the nanocatalyst surface; (3) surface diffusion events of the adsorbed gas-phase precursors; (4) bulk diffusion events of the adsorbed gas-phase precursors towards the liquid-solid interface; (5) precipitation of a solid crystalline nanowire at the liquid-solid interface; (6) adatom adsorption and desorption processes along the length of the nanowire; and (7) distribution of adatom diffusion events from the substrate to the nanowire base.

It can be observed that the selective enhancement of the dissolution kinetics through the metal nanocatalysts is effected by the proximity of other competing adsorption and desorption mechanism that occur during the nanowire growth. This is one factor that one must consider when choosing an appropriate catalytic material for SiNW growth via the VLS process as well as appropriate catalyst position and substrate material to reduce silicon deposition onto the substrate.
Moreover, metal nanocatalysts used in VLS process have different melting and solidification behaviors in incorporating precursor molecules and dopants during nanowire growth. Such behaviors can be observed from the analysis of the binary phase diagram between the precursor and the utilized metal seed. Certain impurities within semiconductor materials can act as recombination centers and predominantly affect negatively on the charge-carrier lifetime. The impurities can come directly from the metal nanocatalyst material, from the utilized substrate and from contamination introduced in the environment of the hot-wall reactor. Therefore, incorporation of unintentional

Figure 1-3: The figure shows the different processes that are contributing to the VLS growth of metal catalyzed nanowire. The different competing mechanisms can be observed in this figure. An adaptation from Ref 69 (image courtesy of Lauhon Group).
impurities during growth can be problematic; it can degrade the performance of devices that use these one-dimensional nanostructures as building units.

For example, the recombination rate of the impurity incorporated into silicon during nanowire growth depends on its energetic level positioning within the bandgap of the semiconductor material. The closer it is to the middle of the bandgap of the material, the more effective these impurities can act as deep level recombination centers. Therefore, when growing semiconductor nanowires, one should avoid seed materials that can create deep energetic levels, unless the application calls for such induced recombination centers.

From the discussions carried out in this section, when considering the economics and thermal budget of nanowire growth for device applications, ideally the catalyst should have high solubility of the precursor material, low solubility for the impurity materials that can unintentionally dope the nanowire and a relatively low eutectic temperature. One mean of reducing contamination and impurity concerns is to avoid the presents of any material that might incorporate and create deep level defects in the nanowire during growth. This is particularly important in template assisted growth of nanowires. It can be noted that when the impurity energetic levels are close to the conduction band or the valence band of the semiconductor material, one can use the metal catalyst to “intentionally” dope the material and may be potentially useful for the junction-free transistor concept, where high doping densities are typically required to switch on the TFT device after depleting the charge carriers. Further discussion on nanowire doping is included in the next section.
1.2.2.3 Nanowire Doping and Supperlattice Structures

The solubility behavior of the nanowire metal catalyst provides a gateway for creating nanowire junction interfaces. Such junction interfaces can occur between different doped regions in nanowire homostructures or between different utilized precursor materials in nanowire heterostructures. This is all as a result of the unique one-dimensional geometry of the nanowires. The nanowire geometry is sustainable for radial strain relaxation and permits a wide range of defect-free material combinations that can be introduced into a nanowire lattice structure. That is, the nanowire structure can relive its strain through elastic deformation.

In essence, a semiconductor homojunction or heterojunction is the layering of two materials that are different in composition and/or doping type and density. When these materials come in contact, unique electronic and photonic properties at the junction interface can be observed. Ideally, it can be difficult to combine two different materials to form a junction; they can encompass a non-negligible lattice mismatch. Also, it is often desired that the junction interface be abrupt. In most cases, nanowire junctions are often diffused. By analyzing the solubility behavior of the metal catalyst, as well as the bulk crystal structure and lattice mismatch between junctions of the semiconductor precursor and/or dopant materials, one can appropriately choose material combinations that better suit the particular application of the nanowire.
1.2.2.3.1 Axial Heterostructures and Homostructures

There are different chemical activities that exist for the incorporation of different gas-phase precursors through a given metal catalyst material using the VLS mechanism. For nanowire axial superlattice structures, the chemisorption and physisorption of precursor and dopant materials onto the sidewalls of the nanowires are often suppressed. This allows for the direct absorption of precursor and dopants at the metal catalyst for obtainable vertical crystal growth. The technique used to form axial heterostructures and homostructures is through modulation of the reactant material during nanowire growth. Periodic layers of different semiconducting materials can be achieved using this approach and the number of junction interfaces is defined by the CVD practitioner.

For any solid-state semiconductor device, it is important to have good control of doping over a wide range of concentration for nanowires. In conventional silicon planner devices, ion implantation is usually used to dope the material. This standard approach to dope silicon can lead to the creation of structural defects that are often undesirable. Typically, the species used for in-situ doping of SiNWs through the VLS mechanism are n-type Phosphine and p-type Diborane. Though in-situ doping of SiNWs grow with minimum dopant fluctuations and without any structural defects, the dopant density for axially doped in-situ silicon is limited\(^7\)\(^0\). High dopant densities for nanowires are a prerequisite for high performance devices such as the junction-free field-effect transistors FET. To enable low power consumption and fast switching devices, high dopant concentration in SiNWs is crucial. Radial doping of nanowires has been of increasing
interest to tailor and further improve electrical properties of SiNWs. A reference list of in-situ doping species for silicon nanowire can be found in Table 1-3 bellow\textsuperscript{71}.

Table 1-3: Examples of some successful in-situ doping of SiNWs as illustrated in the literature

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<th>n-type</th>
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</tr>
<tr>
<td>-</td>
<td>AsCl\textsubscript{3}</td>
</tr>
<tr>
<td>-</td>
<td>Al</td>
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1.2.2.3.2 Radial Hetrostructures and Homostrucutres

Moreover, adsorption and desorption processes of gas-phase precursors and dopants can occur on the nanowire surface in addition to catalyst incorporation. Studies have shown evidence that under certain nanowire growth conditions; favorable radial growth via vapor phase deposition on the surface of the nanowire can be achieved. This is known as the vapor-solid VS mechanism. The rates between VLS growth from the precursors and dopants through the metal nanocatalyst and that of the VS radial growth of the nanowire are unequal. The VS growth mechanism can lead to high nonuniform dopant distributions along the length of the nanowire. This is due to base area of nanowire being exposed longer to the gas-phase reactants than that at the top when considering template free nanowire growth on conventional substrates.

Though VS at times can be undesirable during growth and can result to the well-known tapered nanowire structure, radial core-shell homostructures and heterostructures can provide useful applications and potentially enhance nanowire electrical and photonic
properties. Examples of core-shell nanowire structures have been realized by Lauhon et al.\textsuperscript{72} by varying the gas-phase precursor and dopant conditions in the LPCVD environment during the VLS nanowire growth.

1.2.2.4 Nanowire Crystallography and Growth Orientation

The VLS mechanism used to grow SiNWs is a complex growth mechanism that has been heavily investigated by many research groups. When considering silicon nanowires as building blocks for the next generation of TFTs, it is important to consider both the degree of crystallinity and the crystal growth orientation of the nanowire. Epitaxial growth of free standing SiNWs on silicon substrates are typically in most cases single-crystal diamond crystal structures. For the presented encapsulated grow-in-place approach of SiNWs, it is important to determine the degree of crystallinity of the nanowire. This can be achieved by analyzing the nanowire using Raman Spectroscopy, Selected Area Electron Diffraction SAED patterns and/or High Resolution Transmission Electron Microscopy HRTEM images of the silicon nanowire lattice.

There are three growth directions that have been observed for SiNWs grown via the VLS mechanism. The growth directions are $<112>$, $<110>$ and $<111>$\textsuperscript{61}. These growth directions are generally observed independently of the vapor-phase technique utilized to grow the SiNWs via VLS. Nanowires tend to choose a growth direction that is more energetically favorable; it wants to reduce its free energy. For nanowire diameters less than 20 nm, the $<110>$ growth direction is preferred. The $<111>$ growth direction is typically observed for nanowire diameters greater than 50 nm. $<112>$ growth direction is
observed between the transition of the nanowire radial dimension from 20 nm to 50 nm. Faceting at the nanowire surface has also been observed for silicon nanowires and has shown to affect the electrical properties in nanowire devices. For high performance electronic applications, smooth nanowire surfaces are often desirable. Faceted and rough nanowire surfaces can cause surface scattering of charge carriers and create quantum interference that can severely degrade the performance of the electronic device.

Furthermore, over the length of the VLS growth, the nanowire orientation can change. This observed phenomenon can be explained by the tilting effect of the metal nanocatalyst during the growth - when in a supersaturated liquid eutectic droplet phase - from its initial solid phase. In addition, nanowires can change their growth direction and result in what is known as nanowire kinks. Such kinks are undesirable and are influenced directly by growth temperatures and precursor partial pressures within the working LPCVD reactor.

Figure 1-4: The figure illustrates the quantum confinement effect observed by Ma et al. in sub-10nm SiNWs.
1.3 Nanowire Electrical Properties

From the exceptional one-dimensional nanowire geometry, spatial confinement of electrons and holes can be achieved. This allows one-dimensional carrier transport to occur. The quantum size effect has also been observed in silicon nanowires. Ma et al. has shown that the bandgap of SiNWs can be altered by changing the diameter of the nanowires\textsuperscript{74}. From Figure 1-4, an illustration of experimental and calculated data show that the silicon bandgap in the nanowires increased with decreasing nanowire diameter. This observation shows achievable quantum size effect in SiNWs.
CHAPTER 2
Semiconductor Nanowire Device Integration

2.1 Grow-and-Place Approach

Semiconductor nanowires have shown tremendous promise for applications in different areas of electronic, optoelectronic and photonic devices. In order for these applications to become commercially viable, large scale production and integration of nanowires with uniform electrical properties must be achieved. This section will discuss the two step process of nanowire growth and post-growth integration that is universally used today to fabricate nanowire devices.

There are two approaches that are utilized to synthesize SiNWs. They are the “Template-free” synthesis approach and the “Template-assisted” synthesis approach. Although both “Template-free” and the “Template-assisted” nanowire synthesis use the VLS growth process which was discussed in the previous chapter, both growth methodologies -the “Template-free” and the “Template-assisted”- require post-growth integration in order to facilitate in the fabrication of single nanowire devices. An overview of the different pathways for post-growth integration of nanowires will be discussed in this section. The process flow that requires post-growth integration of the nanowires is referred to the “Grow-and-Place” approach. Investigation on the limitations of the “Grow-and-Place” approach will also be discussed in this chapter as well.
2.1.1 Template-Free Growth

Nanowires grown without templates are often supported by a substrate material. This method of growing nanowires requires favorable conditions for VLS tip lead growth over substrate film deposition. The one-dimensional growth direction of the nanowires is not only guided via the size of the metal nanocatalyst but also the crystal orientation and thermal expansion coefficients of the utilized growth substrate as well. These nanowires are harvested after growth by means of ultrasonic agitation in solution, typically a common solvent, after removal of the metal nanocatalyst that is capped at the tip of the nanowire. Typically, selective metal wet etchants are utilized to remove the metal nanocatalyst from the tip and from the side-walls throughout the length of the nanowire prior to post-growth processing.

One key advantage of template-free growth over conventional template assisted growth is the overall surface quality of the nanowire is much better for template-free growth. This is because the material surface energy and atomic smoothness of the boundary of the template assisted growth must be considered in order to produce nanowires with superior surface quality. Furthermore, one of the most important advantages of template-free growth of nanowires is that the growth method does not suffer from the post-growth template removal process. Template assisted growth may pose problems in the performance of devices utilizing these nanowires as building blocks as the template materials can unintentionally introduce impurities and defects into the nanowires. Nerveless, template-free nanowire growth poses poor growth yield, non-uniform dopant distributions as well as tapered nanowire morphologies resulting in low
aspect ratios. Template growth can possibly overcome some of these problems and will be discussed in the next section.

2.1.2 Template Assisted Growth

Templates can provide a mean for guiding nanowire growth and controlling nanowire morphology. Prefabricated templates for VLS nanowire growth have been commonly reported in the literature. Nanochannels fabricated in anodic or anodized alumina membranes AAMs have shown to serve as good templates for VLS metal catalyzed nanowire growth. Side-wall deposition of the precursor material can occur at the inlets and radial length of the nanochannel. But with the utilization of metal nanocatalysts that are strategically placed in the nanochannel, selective deposition inside the channel and particularly at the metal nanocatalyst over the nanochannel surface and inlets can be achieved. This will lead to tip lead nanowire growth confined within the nanochannel geometry.

For SiNW VLS growth in AAM templates, a Au layer is electrodeposited inside the nanochannels via a two-step process: First by electrodepositing Ag inside the channel followed by the electrodeposition of Au. The Ag material is then etched away before nanowire growth and is used to strategically place the Au at a particular position along the length of the nanochannel. Although successful synthesis of sub-100nm diameter nanowires of various materials have been reported, the use AAM templates defeat the possibility of producing intrinsic semiconductor nanowires. With AAM templates, Al can effectively dope the nanowire and particularly SiNWs. Therefore it is important to
choose a template material that will not unintentional introduce impurities and possibly incorporate into the nanowires, creating deep level defects that will hinder the life-time of the minority charge carries. Therefore, the compatibility of the materials used during the VLS growth process is of crucial interest in this thesis project and will be later discussed in the upcoming sections.

2.1.3 Limitations of the Grow-and-Place Approach

There are many challenges that are associated with the grow-and-place approach for the synthesis of SiNWs for FET devices. This section will provide more insight to some of these challenges, in particular, the challenges that can affect device performance that are important to electronic applications of SiNWs.

2.1.3.1 Dimention Control

During VLS nanowire growth, it was pointed out that the diameter of the nanowire is controlled via the size of the metal catalyst. But during the growth process, the metal nanocatalyst can undergo morphological changes. This leads to dimensional changes of the nanowire over the span of the growth process as well as migration of the metal seed onto the side-walls of the nanowire. Moreover, an interesting effect can occur between the nanowire and the supporting substrate interface during VLS growth. This effect is the diameter expansion at the nanowire base where it is attached to the substrate. This is a direct reflection of the interaction between the liquid eutectic metal nanocatalyst
and the precipitated solid crystalline nanowire during growth. The reason for this expansion can be due to Si overgrowth directly on the sidewalls of the nanowires, but more importantly is due to the morphological transition of the metal catalyst from its initial phase. Throughout the growth process, the contact angle between the liquid eutectic nanocatalyst droplet and nanowire precipitate can change over time. Typically this effect is observed in nanowires grown without any supporting template. Therefore, the expansion of the base is a direct result of the vacillating surface tension of the liquid droplet, the solid nanowire and the boundary tension between the liquid-solid interface during growth. This is not the case when templates, such as the AAM templates, are utilized to assist in controlling the nanowire’s dimension and growth.

Another challenge associated when using metal seeds to catalyze nanowire growth is the distribution of nanowire diameters that is obtained from one growth sample to another. This is due to the size dispersion of the metal nanocatalysts themselves, particularly with colloidal Au nanoparticles or Au island formation from annealed Au films. In addition, the position of the nanocatalysts with respect to the laminar gas flow in the CVD system can change from sample to sample. This leads to a variation in nanocatalyst saturation rates from the precursor and/or dopants introduced during nanowire growth. Due to the quantum size effect that has been demonstrated in SiNWs, the bandgap of the nanowire can change with the diameter of the nanowire. Having a variation in nanowire diameter and therefore its bandgap reduces performance reproducibility when considering these nanowires for electronic and optoelectronic applications.
2.1.3.2 Orientation Control

The challenge of controlling the growth orientation of SiNWs has many practical, technological and fundamental scientific implications. The inherit properties of these one-dimensional nanostructures, combine high crystalline quality and great controllability in terms of length and diameter via metal catalyzed growth. These properties have opened up many possibilities of utilizing these structures in electronic and optoelectronic applications. In order to make the most out of the properties of epitaxially grown SiNWs for the manufacturability of nanowire FETs, one must investigate the interfacial surface energies that interplay in the crystallographic orientation of the nanowires.

It has been reported by Lieber and his colleagues that VLS SiNWs grown on SiO$_2$ supporting substrates, preferentially change growth direction from the $<111>$ to the $<110>$ as the diameter of the nanowire was scaled down to 20 nm$^7$. The $<112>$ growth direction was also observed in transition of the nanowire crystal growth direction from $<111>$ to $<110>$. In terms of nanowire FETs for CMOS technology, a single misoriented nanowire from the array can be the difference between a functional or faulty device. The performance of nanowire FET devices is highly tailored by the orientation of the nanowire building block that is utilized as the active channel material. Also, the forming facets on the sidewalls of the nanowire, when template-free nanowire growth is being considered, can affect device performance as well. Nanowires tend to grow in the direction that minimizes its total free energy, until a critical diameter of the nanowire is reached$^7$. Thereafter, the free surface energy of the nanowire facets begins to dictate the
growth direction of the nanowire and can lead to different electrical and optical properties of the nanowire than that of nanowires with larger diameters.

It has been reported that nanowire grown in the \(<112>\) direction for very small diameters inherits an indirect band structure that cannot be utilized for FETs and AMOSFET devices\textsuperscript{77}. It is important to have good control over the crystallography of the nanowire by investigating the surface energies and surface roughness of the supporting template materials or substrates.

2.1.3.3 Integration Control

Semiconductor nanowires have shown tremendous promise for the many applications aforementioned throughout the sections. In order for such conventionally grown nanowires to adequately become commercially feasible for large scale production and integratable into active CMOS components, post growth harvesting of these nanowires must be achieved. There are limitations of post-growth integration on device yield, especially when scaling to larger substrates. Furthermore, post-growth integration can possibly introduce unintentional impurities and damage to the nanowires during the integration process. Such improprieties can be detrimental to the performance of metal contacts that are placed post nanowire integration. This section will illustrate some of the most successful methods used to integrate nanowires into device. The majority of the devices that have been fabricated using such aggressive integration approaches were done at the proof-of-concept level. Nevertheless, it is important to investigate these approaches
in order to understand why there is greater emphasis on the grow-in-place approach over the grow-and-place approach that was discussed in the previous section.

2.1.3.3.1 Electric Fields

In recent years, high yield integration of semiconductor nanowires has been a subject of great interest. Many research efforts have sought the use of electric fields to manipulate and assemble polarizable one-dimensional nanomaterials and in particular semiconductor nanowires. This approach is commonly referred to in the literature as dielectrophoretic assembly\(^\text{78}\). Nonuniform electric fields have tremendous promise in selectively controlling nanowire separation, motion and assembly. Such electric fields are induced from electrically biased predefine electrodes. Typically these electrode structures are designed using a series of fabrication processes that include lithography, deposition and etch. Therefore much effort goes into play with optimizing the design of these electrodes. In order to achieve site specific device assembly goals of the nanowire building blocks, the dielectric properties of the suspension solution (such as the conductivity and permittivity) and the supporting substrate must be precisely tailored and controlled. By controlling such properties, the nanowires can interact and align with the minimum energy configuration of the applied varying electric field\(^\text{79}\).
Furthermore, other factors that influence the spatially varying electric field profile and hence the assembly and integration of the nanowires includes nanowire dimensions, surface functionalization and nanowire density in the solution used to post-growth release the nanostructures by means of ultra-sonication. Recently, T. Mayer and her colleagues have studied the deterministic assembly of functional nanostructures using nonuniform electric fields and demonstrated nanowires assembly for FET devices\textsuperscript{80}. Aside from the complexity of the integration approach, obtaining high yield integration of nanowires using nonuniform electric fields on large substrates requires high monodisparity and material homogeneity of the utilized nanowires. This is often challenging to achieve when considering nanowires grown without supporting templates to guide VLS growth.

\textbf{2.1.3.3.2 Fluidic Channel Assisted Alignment}

In addition to manipulating polarizable nanomaterials, such as semiconductor nanowires via electric fields, an extensive amount of research efforts has been done in
recent years on micro- and nano- fluidic assembly of nanostructures. Typically fluidic channels are fabricated using innovative soft lithography approaches (i.e. poly-dimethylsiloxane PDMS stamps) as well as the common aforementioned fabrication approaches discussed in the previous chapter. Fluids that are confined within such channels establish a uniform shear force that can be utilized for nanostructure alignment. The application of this approach has been demonstrated extensively in the literature.\textsuperscript{81}

Nanostructures, such as nanowires are pumped into these nanofluidic channels that have been designed to precisely control the fluid dynamics inside the channel where assembly takes place. Ultimately, these nanowires adhere to the surface with an adapted orientation that is typically parallel to the fluid flow.\textsuperscript{79} But utilizing fluidic channels in FET devices to align nanowires has its own set of challenges. First, the stability of the nanowires in the solutions used to disperse and assemble these nanowires can leave residual material after solution removal at assembled sites. These residual materials can potentially be detrimental to the device performance that utilizes these nanowires as building blocks. Moreover, the stability of the nanowires after solution removal can present some other difficulties. Due to surface tension and electrostatic interaction of the nanowires with the solution during drying, nanowires can buckle or delaminate from their assembled sites. This can affect the yield of devices utilizing these nanowires as well as device performance. Furthermore, device reproducibility can be a problem when using this approach to assemble nanowires for FETs.

In addition, the scalability of the approach to large substrates with single nanowire control and assembly precision can be challenging with fluidic assisted assembly. Also when considering the fabrication of FETs on flexible materials, utilizing
fluid channels to assist in the assembly nanowires for devices may not be feasible. Nevertheless, fluidic channel assisted alignment of nanowires presents its advantages due to the fact that the field of nanofluidics has been well developed in the past years due to advances in fluid dynamic modeling.

2.1.3.3 Direct Contact Printing

Another approach that has been gaining interest in integrates nanowires for device fabrication is assembly driven through electrostatic interactions. Because of the inherent polarizability of semiconductor nanowires as discussed previously, nanowires can be assembled onto surfaces that have been functionalized to adapt a specific electrical charge. Surface functionalization can be done by using defined self-assembled...

Figure 2-2: An illustration of a general assembly process flow for direct contact printing of nanowires.
monolayers SAMs designed to adhere to the polarized nanowire structures. Typically, a master mask is fabricated using conventional lithographic approaches. These master masks are used to mold PDMS stamps for direct contact printing on desired surfaces. After curing of the PDMS mold, a desiccator is used to deposit a monolayer of the functional molecule onto the surface of the mold via vapor deposition. These molecules have a functional head and tail, where one end adheres to the desired substrate once the mold is in direct contact, and the other to the nanowires. After SAM stamping on to the desired substrate, nanowires are usually spun casted onto the substrate. These nanowires will adhere to functional sites and the rest will be washed away after dispersing the substrate into DI water. Direct printing allows for selective patterning of the nanowire. An example of a SAM material that is common used is 3-aminopropyltriethoxysilane (APTES).82

Although the discussed assembly approaches can be simple to implement and has the potential to scale to large substrates, orientation control at the single nanowire level is hard to achieve. This is because the alignment of these nanowires using the aforementioned approaches is imperiled to dynamic, adhesion and thermal fluctuations of the process. As mentioned in the previous chapter, in order to make use of nanowires in HVM, integration of nanowires at the single device level is critical to device performance and reproducibility.
2.2 Grow-in-Place Approach

Semiconductor nanowires have shown tremendous promise for application in different areas of electronic and optoelectronic high performance devices. In order for these applications to become commercially viable in the near future, large scale production and integration of nanowires with uniform electrical properties must be achieved. We have discussed previously some of the implications that can occur from post-growth assembly and integration of nanowires into feasible devices. These implications can lead to undesirable effects that can degrade the performance of devices using these nanowires as building blocks. In order to achieve large scale integration of nanowires, particularly on large substrates, it is very important to have good control over the nanowire growth process at the atomic level. To truly maintain control over the nanowire growth process, as well as to have the ability precisely position and integrate these one-dimensional structures into active device, traditional integration routes must be abandoned and new innovative ideas must be formulated.

A concept that has been proposed by the Fonash research group to resolve the many issues with integrating VLS grown SiNWs into devices has been realized using a one-step process. This process combines the growth of nanowires into prefabricated device architectures such FETs. This approach is known as Grow-in-Place. Essentially, nanochannels are used to guide nanowire growth via the VLS mechanism mediated from a single metal catalytic source. These nanochannels can be part of the overall architecture of the FET device as will be discussed later. Although we are focused on grow-in-place of nanowires for FETs, this approach can be applied to nanowire sensor devices and other
nanowire device applications. This Section will discuss the thought process behind the design component of the proposed encapsulating guides that has been proposed by the Fonash research group as well as other related work from the literature.

2.2.1 Discussion of Related Work

Guided grow-in-place of nanowires can overcome some of the limitation of post-growth integration of these nanostructures by essentially combining growth and integration into a single step. In order to build robust nanowire FETs, many researchers have been coming up with different ways to precisely control the growth of in-plane nanowires. A strategy proposed by Linwei Yu et al. showed a reliable way of growing self-aligned SiNWs, via an in-plane solid-liquid-solid growth method using a PECVD system\textsuperscript{16, 83, 83b}.

Figure 2-3: The figure illustrates the solid-liquid-solid growth mechanism of the grow-in-place approach adapted from Ref\textsuperscript{16}.

Prefabricated templates with a simple bottom-gate configuration allows for two dimensional array ordering of single nanowires. This is done by using a thin film of
hydrogenate amorphous silicon a-Si:H, at the edge of a sidewall structure. This a-Si:H layer supplies precursor material to an indium catalyst droplet through the solid-liquid-solid growth mode. The absorption and diffusion of the a-Si:H into the catalyst interface, leads the in-plane motion of the catalyst through precipitation of a solid crystalline nanowire out of the supersaturated indium droplet. This unique approach relies on the surface energetics as the driving force for directional nanowire growth. Such a driving force is established from the difference between the Gibbs free energy of the a-Si:H layer and c-Si nanowire$^8$. Linwei Yu et al. showed effective control over the nanowire diameter as well as an overall low defect density in single crystal nanowires. In addition, the author demonstrated working FET devices with comparable current-voltage characteristics to that of planer silicon transistor structures. Though this approach has shown some potential as a device integration approach for SiNW building blocks, it presents some drawbacks. First, indium is a catalyst that forms a eutectic with very low silicon concentrations (<0.01 at.%). Therefore the growth rate of indium catalyzed SiNWs is very slow. Moreover, indium can cause strong p-type doping in SiNWs and can be undesirable for electronic devices using these SiNWs as active components or interconnects. Finally, uniformity issues with the nanowire throughout its radial length are apparent from the author’s results. This can have some effects on the electrical characteristics of high performance devices utilizing these SiNWs.

Similar to the previous discussed grow-in-place approach, David Tsivion et al. reported VLS growth of GaN Au-catalyzed in-plane nanowires on different crystal planes of sapphire substrates$^8$. David Tsivion et al. showed that the resulting facets and
crystallographic orientation of the nanowires was highly depended on each surface ordination and miscut of the utilized substrates. This is depicted in Figure 2-4, where the growth characteristics of the nanowires is related to the epitaxial relationships and the graphoepitaxial effects that guide the nanowire growth over the legs and groove of the sapphire substrates. The resulting nanowires showed good crystallinity with few observable structural defects. But one key aspect that the approach lacks is single nanowire growth uniformity as well as nanowire length homogeneity. Controllability over nanowire growth length for single device addressability is the only way these nanostructures can be commercially feasible.

The Fonash research group has been the first to demonstrate the ability to grow encapsulated in-plane SiNWs to overcome many difficulties that were discussed in the two previous grow-in-place examples. Though other research groups have shown similar examples to the idea that will be discussed in the next section, nanowires with good crystallographic orientation with low structural defects for high performance FET devices has not been previously reported. This is because the extent of stress induced defect in the nanowires from the material of the channel used to encapsulate the SiNW during VLS growth has not been considered by other research groups.
2.2.2 Discussion of Current Approach

To sustain uniform growth of SiNWs, as well as to have the ability to precisely position and integrate these low-dimensional nanostructures for commercially manufacturable nanowire FET devices, a new grow-in-place approach has been proposed to assemble self-aligned nanowires. This is achieved through the in-situ encapsulated VLS growth of SiNWs in predefine nanochannel structures. These nanochannels will
ultimately be part of device architectures such as the AMOSFETs that was previously discussed in chapter 1. The predefined nanochannels templates that are being proposed is intended to guide nanowire growth via the VLS mechanism mediated from a single metal reservoir. This reservoir not only serves in the VLS catalectic action but also as a potential integrated electrical contact on one end of the SiNW. This will be further elaborated in the upcoming sections.

2.2.2.1 Previous Design

Previously, a nanowire template has been proposed for encapsulated growth of SiNWs. This was a progression from the first attempt in developing the grow-in-place concept, where the approach grew in-plane extruded nanowires from preexisting fabricated templates as first demonstrated by Yinghui Shan et al. in 2008. As depicted from Figure 2-5, the process flow for the fabrication of the first grow-in-place approach for SiNWs started with defining a sub-100nm Au line using electron beam lithography followed by metal deposition and a lift of process. Not only does the Au line act as the sacrificial channel material but also as the catalyst for VLS nanowire growth. After partial capping of the Au line, wet etching of the sacrificial metal to form an empty nanochannel was done. This left a Au slug in the middle the nanochannel for the growth and extrusion of the SiNW from out of the channel inlets during VLS growth in the LPCVD, utilizing SiH₄ as the precursor. One of the inherit problems with extruded growth of SiNWs is the control of the growth direction of the nanowire as it is extruded.
from the capping layer. This result has led to the expansion of the capping layer and hence the introduction of in-plane encapsulated SiNW growth was introduced.

![Diagram](image)

**Figure 2-5:** The process flow for extruded nanowire growth adapted from Ref\(^{15}\). A) Defining Au line using e-beam lithography followed by PVD Au deposition and lift-off. B) Partial capping of Au line using photolithography. C) Partial etch-back of the Au line. D) Extruded growth of a SiNW in the LPCVD system.

Chris Winter was first to show the successful growth of encapsulated SiNWs from similar structure shown in Figure 2-5. In his design, that capping layer was SiO\(_2\) deposited by Plasma Enhanced Atomic Layer Deposition (PEALD)\(^{86}\). He showed narrow Stokes line width from his Raman Spectroscopy data, indicating good crystalline SiNWs. Though the approach showed some promising results for encapsulated nanowire growth, the design was not feasible for HVM. First, controlling the extent of etch back of the Au sacrificial via wet etch chemistry can be difficult. Variations in final nanocatalyst size can lead to a variation in catalyst saturation rates of the precursor atoms introduced during VLS nanowire growth. Due to the quantum size effect that has been demonstrated in SiNWs, the bandgap of the nanowire could potentially change with the size of the
nanowire, if the growth is not graphoepitaxtital, where the nanowire is not defined by the channel. Having a variation in nanowire diameter and therefore its bandgap, reduces performance reproducibility when using these nanowires for electronic and optoelectronic devices.

Furthermore, utilizing Au as a sacrificial material is not commercially feasible due to the increasing material cost. Moreover, residual Au left in the nanochannel can incorporate and create deep levels in the SiNWs. Such deep levels can have detrimental effects on the minority carrier lifetime. Therefore, alternative sacrificial materials to form the nanochannels for encapsulated nanowire growth are highly desired. This is in order to make the grow-in-place approach manufacturable and commercially feasible.

2.3 Research Objectives

This thesis is intended to investigate alternative materials as well as fabrication routes to construct templates for in-plane encapsulated growth of SiNWs. The objective is to advance the previous grow-in-place approach that has been previously proposed. The keen interest in optimizing the approach is important in order to make encapsulated growth of SiNWs commercially feasible and economical for high volumetric device integration of nanowire FETs and therefore enhancing current CMOS technology. Growing nanowires from ultrathin metal catalyst reservoir structures is of focus here. This is because the reservoirs not only serve as a metal catalyst source for multiple self-aligned growth of SiNWs but also as a potential electrical contact for devices. In addition, investigation into the material growth and deposition used to fabricate the
nanochannel templates, for high quality SiNWs is being considered here. This will be discussed in detail in the next chapter.
CHAPTER 3

Design Optimization for Grow-in-Place Approach

3.1 Nanowire Catalyst

In VLS growth of semiconductor nanowires, different elemental and alloy\(^{87}\) metal catalysts can be used. The catalyst material, shape and size highly dictates the desired geometry and resulting properties of the nanowires and hence the performance of these nanowires in active device regions. Therefore, when considering the use of SiNWs as the active switching component in FET devices, we must first consider the role of the catalyst material in producing in-plane high crystalline quality nanowires with reduced structural defects. In addition, it has been discussed in the first chapter that each metal catalyst has different melting and solidification behaviors in incorporating precursors and gas phase dopants during nanowire growth. These behaviors can be understood by analyzing potential-molar phase diagrams of the catalyst material and precursor. Therefore, selective solubility of semiconductor material at the catalyst interface is an important factor when choosing an appropriate catalyst material for the proposed grow-in-place approach. This will be further discussed in this section.

3.1.1 Catalyst Material

As discussed in Chapter 1, the ideal catalyst for VLS nanowire growth must have the following characteristics:
(1) Selective Solubility: This is an important factor when choosing a candidate catalyst material for semiconductor VLS nanowire growth. Ideally, the chosen material should have high solubility of the desired semiconductor precursor and well controlled solubility of dopants, in order to create abrupt junctions during nanowire growth. More importantly, the chosen material should have low solubility of impurity materials that are not only present in the growth reactor, but also the supporting platform used for the encapsulated growth of SiNWs. This is important in order to avoid unintentional doping of the nanowires during growth. (2) Catalyst doping: When growing semiconductor nanowires, one should not choose materials that can create deep energetic levels within the nanowire material, unless the application calls for such induced recombination centers. (3) Low eutectic temperature: Growing nanowire from catalysts with a high eutectic temperature can create thermal budget constraints on the growth and integration process. Typically, catalysts with a low eutectic temperature are often desired.

Other important characteristics of the chosen catalyst material include, (4) Non silicide forming catalyst: For high performance electrical devices such as FETs, growth from silicide forming catalysts can be very complex. Such catalysts exhibit multiple silicide phases and many eutectics. In addition, nanowires grown via the VSS mechanism with silicide forming catalyst often show poor crystal quality\(^{88}\). (5) Low vapor pressure materials. (6) Chemically inert. Au is widely used as the primary catalyst for the growth of many semiconductor nanowires. The challenge of using Au as a catalyst is that it is hard to form abrupt junction interfaces when creating nanowire homo- and heterostructures. The diffuse junction interface is due to the high solubility and low depletion rate of the incorporated material from the supersaturated eutectic Au catalyst when
switching the precursor or dopants to form a semiconductor junction. This phenomenon is referred to in the literature as the “reservoir effect”. Because the performance of p-n junctions are determined by the abruptness of the transition between the p-type and n-type regions, the reservoir effect creates constraints on the performance of devices made using these one-dimensional nanostructures as building blocks.

Nevertheless, Au has been primarily used as a catalyst material to grow SiNWs using the VLS mechanism. Au is favorable for growing nanowires because it is chemically inert, it possesses a low eutectic growth temperature and has a relatively high solubility of the group IV semiconductor material.

3.1.2 Catalyst Shape

The shape of the catalyst in the encapsulated templates that will be discussed in this thesis is defined by the channel in which the grow-in-place approach takes place. In substrate supported VLS growth of SiNWs, the catalyst is in a liquid state as it reaches the eutectic temperature with silicon. As illustrated in Figure 2-5, the first demonstration of the grow-in-place approach utilized a slug shape of Au to catalyze nanowire growth. This slug was positioned in the channel through partial etch back of the sacrificial Au line used to form the empty channel for the extruded growth of an in-plane nanowire. The Au slug configuration was adapted by Chris Winter for encapsulated growth of SiNWs as well. The problem with using a Au slug to catalyze the growth of the nanowire as discussed previously, is that the chemical wet etch process is hard to control and can be difficult to achieve slug dimension uniformity from one device to another.
The concept of utilizing a Au thin strip or line catalyst structure, crossing the middle of the nanochannel or situated at one end of the nanochannel inlet is introduced here. Utilizing a thin strip of Au not only avoids using wet etch chemistry to position the Au, but allows the use of lithography techniques that are commonly used in CMOS technology. Therefore, the catalyst can be precisely positioned and the volume of the Au can be accurately controlled. In the process that will be presented here, the Au catalyst structure will be placed perpendicular to the channel direction. This is done, to see if indeed nanowires can catalyze from lines and or strips of Au that are microns in length. This is for the potential future purpose of utilizing these lines and or strips as electrical contacts if alternative catalyst materials can be utilized.

### 3.1.3 Catalyst Volume

In VLS nanowire growth on supported substrates, the diameter of the nanowire is controlled via the size of the metal catalyst and can be described using the following expression:

\[
R = r \sqrt{\frac{1}{1 - \left(\frac{\sigma_{ls}}{\sigma_l}\right)^2}}
\]

- \(R\) is the radius of the metal catalyst
- \(r\) is the radius of the NW
- \(\sigma_{ls}\) is the interface tension of the liquid/solid interface
- \(\sigma_l\) is the surface tension of the liquid catalyst

To catalyze sub-100nm nanowires, only a small amount of Au is needed to initiate VLS growth. But with the growth of nanowires encapsulated within nanochannel structures, it is necessary to find the optimum volume of Au in order to successfully catalyze the growth of in-plane nanowire via the VLS mechanism. Also, having too much
Au material may hinder the saturation rate to form a Si-Au liquid eutectic, making the precipitation from the eutectic Au-Si alloy almost impossible.

3.1.3.1 Previous Work on Bulk Catalyzed Growth

In previous undergraduate work, nanowire growth from large Au reservoirs was attempted to investigate the growth of SiNW from large bulk material. The sacrificial material used in the channel was chromium. The chromium sacrificial was selectively

Figure 3-1: This figure illustrates the grow-in-place approach that was proposed for encapsulated nanowire growth from large Au reservoirs, using chromium as the sacrificial channel material. A) shows the final design of the supporting template used for in-plane growth of SiNWs. B) Carl Zeiss FESEM image of the fabricated device that will be used for VLS growth of SiNWs encapsulated in the nanochannel. C) An illustration of the growth of potential nanowires from the Au reservoir. D) FESEM image of a potential SiNW inside the channel. The image show very poor overall growth quality.
etched away to form the nanochannel using wet etch chemistry. Figure 3-1 illustrates the device used for the grow-in-place approach for in-plane encapsulated SiNWs. As depicted from the figure, that surface roughness of the nanochannel, which was formed after the removal of the metal sacrificial material, was very rough. This resulted in very poor quality nanowires as seen in Figure 3-1D. From this result, it has been found that chemical wet etch to form the nanochannel for nanowire growth is not a good route to pursue. This is because it affects the inner surface of the nanochannel that will then ultimately affect the quality of the nanowires grown within these nanostructures. In addition, residual material can be left on the sidewall of the nanochannel and potentially incorporate into the nanowires during growth. This can create shallow or deep impurity levels and defects that can degrade the quality and performance of these low-dimensional nanostructures that will be used in different electronic applications.

3.1.3 Optimum Catalyst Design

For the optimum catalyst design, a small line or strip of Au will be considered as the catalyst for the growth of the SiNWs. This catalyst will be defined by electron beam lithography, followed by thermal Au deposition and a lift-off process. The dimension for the catalyst structure will be 3-5um long, 50nm wide and 20-30nm think. Moreover, the configuration of the Au catalyst strip will either be positioned perpendicularly at one end of the nanochannel inlet or crossing perpendicularly at middle of the nanochannel. With the later configuration, it is possible to have VLS growth in two directions within the single nanochannel. This growth phenomena was observed by Shan et al.\textsuperscript{15} in extruded
growth of SiNWs from a slug of Au, that was positioned strategically in the middle of the capped nanochannel.

Some of the important aspects of the nanochannel that must be considered will be discussed in the next section. This includes material selection and surface roughness requirements that could potentially affect the overall quality of the nanowire that will be grown within these nanochannel device structures.

3.2 Nanowire Nanochannel

The process for creating the nanochannel that will allow for encapsulated growth of the SiNWs is done in multiple steps. Electron beam lithography will be the essential lithographic tool that will be used to design sub 100nm line features that will ultimately define the nanochannel. But in order to create a nanochannel device structure for in-plane VLS growth of SiNWs, an appropriate sacrificial material must be chosen. This will be discussed in detail in the next sections.

3.2.1 Nanochannel Roughness Requirements

When choosing a sacrificial material to define the nanochannel geometry, it is important to consider the surface roughness properties of the material. This is because such sacrificial materials will be encapsulated with a capping layer material that can epitaxially tailor the roughness from the surface in which it is either deposited or grown on. Therefore, choosing a sacrificial material, were the surface roughness properties can
be potentially tailored, is advantageous for our process. To better tailor the surface roughness properties of the sacrificial material, polymers have been taken into consideration for as alternative sacrificial material in creating the nanochannels. This is because the surface roughness properties can be controlled through polymer reflow at the glass transition temperature of the sacrificial material.

### 3.2.2 Sacrificial Material

Different polymeric sacrificial materials have been considered as potential candidates for the fabrication of the nanochannels for in-plane growth of SiNWs. With the use of polymers, not only is it possible to change the surface roughness properties via polymer reflow, but also thin polymer films can be easily spin coated on the substrates and removed without harsh wet etch chemistries. Three polymer materials have been considered for the fabrication of our nanochannel devices. These polymers are categorized based on the method used to remove the sacrificial material from the nanochannel at the end of the fabrication process.

#### 3.2.2.1 Water Soluble Polyacrylic Acid

There are many water soluble sacrificial polymers that have been investigated for the fabrication of nanochannels. In order to make great use of water soluble polymers as sacrificial materials, it is important that the polymer is compatible with the fabrication and development processes that will be utilized to create the templates in which the
encapsulated nanowire growth will take place. Properties such as glass transition temperatures, developer compatibility, etch rate and surface roughness were taken into consideration. Polyacrylic acid PAA has shown to be best choice for our fabrication process. Table 3-1 illustrates some of the important properties of PAA:

Table 3-1: Some important properties of 50 kDa PAA pH level 7.5 that was purchased from Polysciences (Warrington, PA):

<table>
<thead>
<tr>
<th>Property</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$T_g$</td>
<td>106 °C</td>
</tr>
<tr>
<td>RMS Roughness</td>
<td>0.28nm</td>
</tr>
<tr>
<td>Etchant</td>
<td>Only in H$_2$O</td>
</tr>
<tr>
<td>Etch Rate</td>
<td>750um/min</td>
</tr>
<tr>
<td>Molecular Weight</td>
<td>50 kDa</td>
</tr>
</tbody>
</table>

3.2.2.2 Thermal Decomposable Polynorbornene

Our second approach to create nanochannels is to remove the sacrificial polymer through thermal decomposition. Most polymers thermally decompose at high temperatures. But one problem associated with decomposing polymers in oxygen free atmospheres at elevated temperatures is that the removal process leaves behind residual material. Such residual material can hinder the growth of high quality nanowires within the encapsulate nanochannel structure. Many polymers have been investigates and it has been found that the Polynorbornene PNB, not only provides a low thermal decomposition temperature that will reduce the overall thermal budget of the process, but also does not leave residual material nor release toxic volatile products during the decomposition process. Therefore, we have acquired a specific grade of PNB sacrificial material from Promerus, LLC (Subsidiary of Sumitomo Bakelite Co. Ltd.) that fits our processing
requirements to create the nanochannels for the encapsulate growth of SiNWs. Promerus is currently developing several grades of sacrificial materials that thermally decompose into gases that can easily be vented from a processing furnace. As a result, ASR-5600 PNB grade was obtained to use as a sacrificial material for the nanochannels. Some of the properties of the sacrificial material are elaborated in Table 3-2:

Table 3-2: Properties of ASR-5600 PNB grade from Promerus, LLC. The sacrificial material is still under development:

<table>
<thead>
<tr>
<th>Property</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$T_g$</td>
<td>300 °C</td>
</tr>
<tr>
<td>Decomposition T</td>
<td>400-425 °C</td>
</tr>
<tr>
<td>Etches with</td>
<td>Acetone or N-Methyl Pyrrolidinone</td>
</tr>
<tr>
<td>Swells in</td>
<td>IPA</td>
</tr>
</tbody>
</table>

3.2.2.3 Organic Solvent Soluble ZEP520A

The final approach to fabricate the nanochannels for the grow-in-place of SiNWs will directly utilize the e-beam definable resist as the sacrificial material. To pattern both the PAA water soluble and thermal decomposable PNB polymers, ZEP520A will be utilized to define the nanochannels etch transfer profiles using e-beam lithography. Dry etch transfer into the sacrificial polymer material is than processed after resist development. Due to the high solubility of ZEP520A in N-Methyl Pyrrolidinone, a sacrificial ZEP520A line can be defined by exposing a reverse pattern using the electron beam, leaving behind the sacrificial line after resist development. After capping and fully encapsulating the sacrificial line, ZEP520A can be removed from the nanochannel with a combination of deep-UV exposure and N-Methyl Pyrrolidinone rinse, leaving an empty
channel for in-plane VLS growth of SiNWs. Using ZEP520A as the sacrificial material not only reduces the need for post lithography etch transfer, but also N-Methyl Pyrrolidinone is not a harsh organic remover. Therefore, it has a low detrimental effect on the surface roughness of the nanochannel during sacrificial material removal.

3.2.3 Nanochannel Capping Layer

To grow encapsulated SiNWs using the VLS growth mechanism, it is important to consider the materials selection in the fabrication process used in the proposed optimum design. Throughout our discussion of nanowire growth via the VLS mechanism, unintentional impurity incorporation can occur during the growth process. Impurity incorporation can occur from the metal catalyst during nanowire growth and from other materials that can be present in the LPCVD reactor. Since the nanowires will be grown within nanochannel structures, impurity incorporation from the capping layer can also potentially occur. Many materials have shown the ability to create both shallow and deep energetic levels in silicon. These energetic levels can act as traps and recombination centers, degrading the performance of devices using the semiconductor nanowires. Consequently for the template design, it is critical to choose materials that will not incorporate into the SiNW or if incorporated will not create deep level defects that can act as recombination centers. Figure 3-2 shows the different impurities that can incorporate into silicon and their relative energetic level positions from the middle of the semiconductor bandgap. Therefore, for the manufacturing process of the nanochannels, there are two particular oxide materials that are being considered for the capping layer.
The two oxide materials are SiO$_2$ and HfO$_2$. These materials were chosen because they do not create unfavorable energetic levels in silicon.

Figure 3-2: A study by Schmidt et al.$^7$ has shown the different impurities that can incorporate into SiNWs and their relative energetic level position from the middle of the silicon bandgap.

Moreover, the second important criterion concerning the capping layer is the quality of the deposited material. For the encapsulating nanowire device, Atomic Layer Depositions ALD is used to deposit the capping layer. This is because the technique provides atomic precision in the deposited material, as well as atomic smoothness at the surface layer. Since the ultimate goal is to grow SiNWs within gate-oxide devices for FETs, ALD is a good approach for depositing high-k gate-oxide materials. The effect of using ALD to encapsulate the sacrificial polymer material will be investigated. PVD will also be utilized to deposit the capping layer for comparison purposes. In the next chapters, the design and results for the three chosen sacrificial polymer materials will be discussed.
CHAPTER 4

Nanochannel Fabrication Using Polymeric Materials

4.1 Water Soluble Polyacrylic Acid

Polyacrylic acid PAA has been of interest as a potential sacrificial material candidate. This is due to its many advantageous properties for manufacturing nanochannels for in-plane growth of SiNWs in FET architectures. These advantages include high etch rate and no detrimental effects on the inner surface roughness of the nanochannels. The DI water used to remove the sacrificial material is highly compatible with CMOS fabrication processes. The fabrication efforts to pattern the water soluble PAA polymer will be investigated. The process flow and results from the fabrication will be illustrated as well. Moreover, it is important to note that the tools used in the fabrication process and their operations are generally described merely for the reader’s understanding. All the fabrication processes were done at the Penn State Nanofabrication Facility. The polyacrylic acid PAA solution preparation will be discussed first in the next section.

4.1.1 Sacrificial Material Preparation

Preparation approach for the PAA sacrificial material was adapted from Vincent Linder et al.\textsuperscript{91} and was adjusted to fit our processing needs. PAA (MW = 50 kDa) was purchased from Polysciences (Warrington, PA). The solution was prepared by mixing the 25\% (w/v) solution of obtained PAA with droplets of 1:1 diluted NaOH, in a beaker with
a magnetic stir bar, mixing at approximately 200 rpm until a pH level of 7.5 was reached. Multiple pH test strips were used to find the correlated pH level of the solution. Neutralization of the solution is critical as it promotes the adhesion of the polymer onto desired surfaces. The neutralized solution was then diluted in DI water with a 9:1 DI water + PAA dilution while increasing the mixing speed to 500 rpm for 2 min. The stirring speed was then set to 1100 rpm and left undisturbed to stir for 1 hour at room temperature.

4.1.2 Sacrificial Material Patterning

To prepare the utilized substrates, 1 um of SiO₂ was thermally grown on RCA cleaned Si (100) prime wafers. The wafers were cleaned in two steps. First, SC1 standard organic clean of wafers in 5:1:1 solution of DI water + NH₄OH-28% + H₂O₂-30% was done for 5 min at 75-80 °C. This was followed by DI water rinse for 3 min. Immediately after the organic clean, SC1 native oxide strip was performed in a 1:30 solution of HF-49% + DI water in a propylene beaker for 15 sec, followed by a 30 sec DI water rinse. Next, SC2 ionic contamination clean was performed on the wafers in a 6:1:1 solution of DI water + H₂O₂-30% + HCl-37% for 10 min at 75-80 °C. This was then followed by DI water rinse for 6 min and N₂ dry. Finally, the wafers were then de-hydrate baked for 5 min at 150 °C.

After 1 um thermal oxide growth, 15 nm of HfO₂ was deposited by Cambridge Savannah™ 200 Atomic Layer Deposition ALD system at 110 °C. The deposition recipe used a 0.15sec pulse of Hf(NMe₂)₄ precursor with 0.015 H₂O pulse at a deposition rate of
~0.9 Å/Cycle (total of 167 cycles). Since the device platforms are meant for TFT devices, utilizing a high-k dielectric such as HfO₂, is of great interest since it is currently replacing thermal grown SiO₂ as the gate-oxide material of choice for high performance FETs.

Before, fabricating actual devices for in-place growth of SiNWs via the growth-in-place approach, it is necessary to see if it is possible to pattern sub-100 nm lines of the PAA sacrificial material utilizing a combination of electron beam lithography followed by reactive ion etching. The first fabrication step to pattern test devices is illustrated in Figure 4-1:

![Figure 4-1](image)

**Figure 4-1:** A) First, 15 nm HfO₂ deposited using ALD with deposition temperature 110 C; Second, O₂ Plasma surface modification, followed by spin coating PAA: (PAA + NaOH + H₂O), pH 7.5, 2.5% (w/v) at 4000 rpm/sec with 2 min bake @ 150 C; Third, 15nm HfO₂ deposited using ALD with deposition temperature 110 C. B) Show an FESEM image of the 100 nm cross section of the spin coated PAA on HfO₂. C) Illustrates the FESEM cross section of the HfO₂/PAA/HfO₂ sandwiched layers. The bright white layer represents the PAA sacrificial material.

After HfO₂ deposition, the surface of the substrate was modified by oxygen plasma to promote the adhesion of the PAA film onto the substrate HfO₂ surface. The M4L high pressure etch tool was utilized for this process with 200W RF power, 600 mT
pressure, 150 sccm of O\textsubscript{2} and 50 sccm of He for 30 sec. PAA was then spin coated onto the substrates using the following spin recipe:

Table 4-1: Spin coat recipe for 80 nm PAA on HfO\textsubscript{2}

<table>
<thead>
<tr>
<th>Step</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.</td>
<td>Static disperse PAA completely wetting the substrate.</td>
</tr>
<tr>
<td>2.</td>
<td>Spin at 500 rpm with 1000 rpm/sec acceleration for 10 s.</td>
</tr>
<tr>
<td>3.</td>
<td>Spin at 4000 rpm with 10000 rpm/sec acceleration for 60 s.</td>
</tr>
<tr>
<td>4.</td>
<td>Bake at 150 °C for 2 min and keep in dry area.</td>
</tr>
</tbody>
</table>

The thickness of the PAA material was confirmed by using both KLA-Tencore P-16+ stylus profilometer as well as the Nanometrics 8000X SE (a Woollam spectroscopic ellipsometer system with a reflection spectrophotometer). Both instruments indicated an approximate PAA thin film thickness of ~81.67 nm. After spin coating the polymer, 15 nm of HfO\textsubscript{2} at 110 °C was deposited using the same recipe as the first HfO\textsubscript{2} layer. This second layer of HfO\textsubscript{2} provides protection of the PAA layer, particularly for areas in which will be pattern though lithography and etch. The resulting PAA line will be utilized as the sacrificial material for forming the nanochannels. Moreover, the HfO\textsubscript{2} Capping layer acts as a hard mask for the etch that will follow the lithography process.

After HfO\textsubscript{2} deposition, M4L oxygen plasma was used to promote the adhesion of the e-beam resist onto the top HfO\textsubscript{2} layer using the standard recipe described previously: 200W RF power, 600 mT pressure 150 sccm of O\textsubscript{2}, 50 sccm of He for 30 sec. ZEP520A was used as the resist material, because of the non-water solvents that are used during the resist development process. In addition, ZEP520A has a very good etch resistance in combination with high resolution lithography capabilities. The spin recipe used for ZEP520 is illustrated in Table 4-2. Following the ZEP520A coating, 15 nm of Au was
thermally evaporated onto the substrate using the Semicore Evaporator from a tungsten boat with low substrate rotation. The thin layer of Au acts as a conducting layer for electron beam lithography and is necessary for high-resolution patterning.

Table 4-2: Spin coat recipe for 391 nm of ZEP520A. Thickness confirmed with the Nanometrics 8000X SE.

<p>| | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>1)</td>
<td>Static dispense ZEP520A wetting 2/3 of substrate.</td>
</tr>
<tr>
<td>2)</td>
<td>Spin at 500 rpm with 1000 rpm/sec for 10 s.</td>
</tr>
<tr>
<td>3)</td>
<td>Spin at 4000 rpm with 10000 rpm/sec for 60 s.</td>
</tr>
<tr>
<td>4)</td>
<td>Bake at 180 °C for 3 min.</td>
</tr>
</tbody>
</table>

Different 40 nm resolution line widths and markers were written onto the resist by exposing it to an electron beam using the Leica EBPG5-HR e-beam writer. A 44 nm beam spot size (2.03nA measured beam current at the Faraday cup), 400 um aperture at 100 kV beam energy with a range of electron beam dose between 120-500 uC/cm² was utilized for the patterns. After exposure, the conductive Au layer was removed using TFA gold etchant from Transene by dispersing the substrate in the etchant for 40s at 25 °C followed by a DI water rinse. Following Au layer removal, the substrate was developed in 99% n-Amyl acetate CH₃COO(CH₂)₄CH₃ for 3 min, then 8:1 MIBK+IPA for 30 sec for high-resolution and then followed by 30 sec IPA rinse. The sample was then analyzed using FESEM and optical microscopy. Figure 4-2 shows some FESEM images taken at different pattern locations.

From Figure 4-2, cracking of the ZEP520A resist material is apparent. The resolution and quality of the unexposed resist lines as depicted in Figure 4-2A shows high roughness as well as some resist scrumming. But with further investigation of the patterns in Figure 4-2D, it has come to a conclusion that the cracking in ZEP520A with the
appearance of 7-20 nm dot like structures, particularly at the PAA layer, are an indication of material swelling in the PAA layer. This swelling resulted in circular like dots, which was also be observed in ALD HfO$_2$ exposed layers as apparent in Figure 4-2C and D. This has been concluded because the dots observed in Figure 4-2D did not go away, even with higher electron dose exposure and O$_2$ de-scramming.

Figure 4-2: Illustrates top-down FESEM images of the pattern ZEP520A resist on top of the HfO$_2$ hard mask. A) and B) were pattern with 160 uC/cm$^2$ at 100 kV and C) were pattern with 170 uC/cm$^2$ at 100 kV.
Moreover, it can be concluded that the H$_2$O precursor used in pulse step of the ALD process is potentially swelling the polymer layer and conceivably incorporating the Hf(NMe$_2$)$_4$ precursor within the PAA sacrificial material or at least resulting in very poor quality oxide deposition. This has led to the formation of the 7-20 nm dots observed in Figure 4-2 and was investigated further by taking cross sections FESEM image of exposed regions of the material stack to the electron beam. An FESEM cross section image of the HfO$_2$/PAA/HfO$_2$/ZEP520A layer stack on the Si/SiO$_2$ substrate is illustrated in Figure 4-3.

![Image](image.png)

**Figure 4-3:** A) an Illustration of an exposed cross section of the HfO$_2$/PAA/HfO$_2$/ZEP520A layers on SiO$_2$. The area was exposed to electron beam dose of 360 uC/cm$^2$ at 100 kV beam energy. B) Shows crosslinking in the PAA layer, in-between the two HfO$_2$ layers. C) Shows crosslinking in the ZEP520A layer.

As would be expected, the cross section FESEM image of the ZEP520A layer in Figure 4-3C shows crosslinking in the resist material. This is because the area has been exposed to an electron dose. What is more interesting is the crosslinking of the PAA layer as depicted in Figure 4-3C. As illustrate from the figure, ~5-15 nm spheres are apparent in the PAA layer. This indicates that there has been a change to the characteristics of
sacrificial polymer material upon exposure to the electron dose. This result is similar to what has been reported by Uwe Lappan et al., where he observed intermolecular crosslinking of PAA dissolved in water upon irradiation with high-energy electrons. What he observed was the formation of macroscopic gels depending on the pH level of the aqueous solution. He concluded that the PAA gels were formed by the electrostatic repulsive forces when the PAA macromolecules are negatively charged in low ionic strength solutions (pH levels 2-4). Changes to the polymer may modify its properties from what was initially desired from the sacrificial material. In the next section, the etch transfer of the PAA polymer from the developed ZEP520A resist will be investigated.

4.1.3 Sacrificial Material Etch Results

Two etch studies have been performed on the PAA sacrificial material. First, PAA was spin coated onto a blank silicon wafer and was etched directly using the PT Versalock Dual ICP etch system with the following recipe: 50 mT, RF1 chuck bias 50W, RF2 coil bias 100W, 45 sccm O₂ and 10 sccm Ar for 60 sec. Figure 4-4 illustrates the post etch FESEM results of the PAA top layer as well as a cross section view of the resist.
In Figure 4-4A, the characteristics of the PAA layer changes as the dry etch of the sacrificial material proceeds. Nanospheres are being produced during the RIE process and poor etch uniformity is apparent as well. These nanospheres show high etch resistance and do not disappear even after all PAA film has been etched away. The second etch study of the PAA sacrificial material was performed by patterning ZEP520A lines on a PAA/HfO₂ layer stack using electron beam lithography. As discussed in the previous section, PAA crosslinking was found upon the exposure of the stack layers to a 360 uC/cm² electron beam dose with 100 kV beam energy.
In, Figure 4-5, 200 nm gaps were patterned with ZEP520A at a dose of 340 uC/cm$^2$. Figure 4-5A, shows the exposed PAA layer with ZEP520A left on both sides prior to any dry etch of the material. The PT 720 CCP was used for this etch study and the following recipe was utilized: 300W, 10mT and 45sccm of CF$_4$. The fluorine gas was chosen for the etch study because it had been reported in the literature to be the best etch chemistry for PAA thin films and in particular the residual nanospheres that appear during the etch process$^{93}$. From the results in Figure 4-5, the etch resistance of PAA had increased to the point where etch uniformity had become difficult to achieve. Moreover,
with increasing etch time, the nanosphere formation from the PAA layer became evidently more apparent.

Figure 4-6: The FESEM images illustrate etch uniformity issues with PAA. The green arrow shows where residual PAA material is left after 130s etch under the same condition in Fig 4-5.

From these results, it can be concluded that patterning the PAA sacrificial material using a combination of electron beam lithography and dry etch transfer is not feasible for our process. This is because, the characteristics and particularly the dry etch characteristics of the PAA sacrificial material changes with exposure to the electron beam. As a result, nanosphere structures formed during electron beam exposure as well as during reactive ion etching. The subsequent issue with etch uniformity is more evident in the FESEM images illustrated in Figure 4-6.

4.2 Thermal Decomposable Polynorbornene

This section will investigate the use of thermally decomposable polynorbornene as a sacrificial material to fabricate nanochannels for the in-plane growth of SiNWs. This
polymeric sacrificial material was acquired from Promerus, LLC (Subsidiary of Sumitomo Bakelite Co. Ltd.). Promerus spin coated 70nm of ASR-5600 grade polynorbornene on provided pre-patterned Si (100) 4inch prime wafers. These wafers contained 1um of thermally grown SiO$_2$. Lithography alignment markers as well as the Au catalyst structures that will be utilized for VLS nanowire growth were patterned on to the 1um of thermally grown SiO$_2$ layer before sending the samples Promerus, LLC for material coating.

4.2.1 Defining Gold Catalyst

These Au catalyst lines were defined by electron beam lithography. First, ZEP520A was spin coated on the Si/SiO$_2$ wafers using the recipe depicted in Table 4-2, followed by 15nm Au (e-beam conductive layer) was thermally deposited using the Kurt J Lesker Lab-18 evaporator. Immediately following Au deposition, 3um long by 50nm wide lines were aligned and exposed onto the wafer, where the alignment of the line structures was achieved by using fixed global markers that have been generated onto the surface previously using e-beam lithography and liftoff. The Vistec EBPG5200 e-beam was used to for all of the lithography process that will be discussed in this section.

The writing parameters used for the Au catalyst structure were as follow: 380 uC/cm$^2$ electron dose, 5nm resolution, 7nm beam spot size (500 pA current), 400um aperture at 100 kV beam energy. Following exposure, the conductive Au layer was removed using TFA gold etchant from Transene by dispersing the substrate in the etchant for 40s at 25 °C followed by a DI water rinse. After Au layer removal, the substrate was
developed in 99% n-Amyl acetate CH₃COO(CH₂)₄CH₃ for 3 min, then 8:1 MIBK+IPA for 30 sec for high-resolution and followed by 30 sec IPA rinse.

After development, resist descum was performed in the M4L using the following parameters: 200W RF power, 400 mT pressure 100 sccm of O₂, 30 sccm of He for 60 sec. Succeeding the descum process, 2 nm Ti adhesion layer and 25 nm of Au was deposited on to the pattern surface using thermal evaporation in the Semicor evaporator. Resist liftoff was performed in Nano Remover PG overnight and was than heated to 50 °C for 1hr before final DI water rinse.

4.2.2 Sacrificial Material Patterning

The schematics in Figure 4-7 illustrate the process flow for patterning the ASR-5600 sacrificial material with e-beam lithography. After patterning the Au lines and spin coating the ASR-5600 sacrificial material shown in Figure 4-7 A and B, the next step in the fabrication process is to define the sacrificial material in order to fabricate the nanochannels for in-plane growth of SiNWs. To do this, we first deposit 50 nm of Al using electron beam evaporation in the Semicore evaporator. The Al layer not only serves as a hard mask, but as a sacrificial material to effectively remove the ZEP520A e-beam resist after the etch process, by removing the Al layer in CD-26 (TMAH). This is because; the goal is to utilize the ASR-5600 exclusively as the sacrificial material. After Al deposition, HMDS was applied to the substrate to promote resist adhesion using the following recipe: 1000 rpm for 15 sec followed by 60 sec bake at 100 °C. Thereafter, 500nm of ZEP520A was spin coated onto the substrate using a similar recipe in Table4-2,
except the spin speed was reduced from 4000 rpm to 2900 rpm. Thermal evaporation of 15nm Au was performed to serve as the conductive layer for e-beam lithography.

Defining the PNB sacrificial material was done in two steps. The first step allows for the partially defining the 100nm line of PNB sacrificial material while fastening both ends to the substrate. This step is necessary in order to stabilize the ZEP520A resist structure after development during the etch process due to the high aspect ratio of the resist. It has been found that ZEP520A provides the best etch selectivity for our process.

Figure 4-7: This figure illustrates the process flow for fabricating nanochannels for the grow-in-place approach at the device cross section shown in the figure.
when compared to negative tone e-beam resist materials. Therefore, two 100um by 5um patterns with 100nm spacing between them were exposed to an electron beam. The beam writing parameters used is as follow: 183 uC/cm² electron dose, 5nm resolution, 7nm beam spot size (500 pA current), 400 um aperture at 100 kV beam energy. The first written layer (A) is illustrated on the device schematic in Figure 4-8.

Figure 4-8: CAD layout of the over design of the device that will be utilized for the grow-in-place approach.

Following Au layer removal, the substrate was developed in 99% n-Amyl acetate CH₃COO(CH₂)₄CH₃ for 2.5 min, then 8:1 MIBK+IPA for 30 sec for high-resolution and then followed by 30 sec IPA rinse (Figure 4-7C).

The resulting ZEP520A structure that will be utilized for the dry etch transfer into the PNB sacrificial material is affix at both ends for structural stability during the etch process. Moreover, because the patterns that are being written are very large at both sides of the ZEP520A line, electrons that are in proximity to the unexposed resist resulted in
electron back-scattering and bleeding into undesired areas of the ZEP520A line that was intended to be left unexposed to the electron beam. Figure 4-9A illustrates this result in the 100 nm ZEP520A line. As one would expect, the base of the ZEP520A line becomes overexposed, because the electron dose spreads away from its intended location, allowing undesired areas to be exposed. This leads to structural collapsing of the ZEP520A line.

![Figure 4-9: The effect of the proximity electron corrector PEC on the profile of the ZEP520A line. A) Without PEC. B) With PEC](image)

To assist in correcting the scattering of the electrons, a proximity electron corrector PEC was utilized in the Layout Beamer fracturing software. The PEC was applied using the alpha (electrons forward scattering in the resist), beta (electrons backscatter from off substrate) and eta parameters of silicon as indicated in Table 4-3. The resulting ZEP520A structure after applying PEC to the fractured design is illustrated in Figure 4-9B. Good structural stability of the ZEP520A line is illustrated and stands ready reactive ion etching transfer into the PNB material.
Table 4-3: Proximity electron correction parameters for ~500 nm ZEP520A on Silicon provided by Electron Beam Facility at the Nanoscale Research Center, Georgia Institute of Technology.

<table>
<thead>
<tr>
<th>Alpha</th>
<th>Beta</th>
<th>Eta</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.0070 um</td>
<td>35.0498 um</td>
<td>0.5962</td>
</tr>
</tbody>
</table>

4.2.3 Sacrificial Material Etch Results

The reactive ion etch process was performed using the PT Versalock dual ICP etch system with backside wafer helium cooling. Schematic D-F represents the three step dry etch process to define the PNB sacrificial material. First, the Al hardmask was etched using the following recipe: 5mT chamber pressure, RF1 chuck bias 150W, RF2 coil bias 500W, 30 sccm BCl₃ and 10 sccm Ar for three 25sec segments with a purge loop in-between each segment. The resulting etch rate of Al was ~40 nm.min⁻¹. Second, the PNB sacrificial material was etched using the following recipe: 50mT chamber pressure, RF1 chuck bias 50W, RF2 coil bias 100W, 45 sccm O₂ and 10 sccm Ar for two 60sec + one 30sec segments. The resulting etch rate of the PNB was ~28 nm.min⁻¹. Finally, an over etch into SiO₂ was performed to make sure that no residual PNB sacrificial material was left un-etched. The following recipe was used: 5mT chamber pressure, RF1 chuck bias 10W, RF2 coil bias 300W, 30 sccm CHF₃ and 10 sccm CF₄ for 30sec. The resulting etch rate of SiO₂ layer was ~30 nm.min⁻¹ and was highly anisotropic. The reason behind etching in short segments was to reduce heating of the resist, to reduce redeposition of Al by products (micrograss) and to increase anisotropicity of the etch profile. The results from the etch process are illustrated in the taken FESEM images in Figure 4-10. After the
dry etch process, the substrate was left in CD-26 for 10 hours to remove the Al layer and consequently any residual ZEP520A left on top of the Al layer (Figure 4-7G).

Figure 4-10: RIE process for sacrificial PNB material. A) BCl\textsubscript{3} etch of Al layer. B) O\textsubscript{2}/Ar etch of PNB layer. C) CF\textsubscript{4} and CHF\textsubscript{3} etch of SiO\textsubscript{2} layer. D) Over etch into the SiO\textsubscript{2} layer.

Following removal of the Al layer in CD-26, 440 nm of SiO\textsubscript{2} was deposited onto the patterned substrate by e-beam evaporation with the Kurt Lesker Lab-18 evaporator with substrate rotation. Next, 500 nm of ZEP520A was spin coated onto the substrate using a similar recipe in Table 4-2, except the spin speed was reduced from 4000 rpm to 2900 rpm. Thermal evaporation of 15 nm Au was performed to serve as the conductive layer for e-beam lithography using the Kurt Lesker Lab-18 evaporator. Layer (B) in Figure 4-8 is then defined with electron beam lithography, overlapping the first layer (A) by 200 nm. This overlap created the opening to the inlets of the nanochannel, in which
the PNB material will thermally decompose from. The e-beam write for this layer used the following parameters: 250 uC/cm² electron dose, 5nm resolution, 7nm beam spot size (500 pA current), 400um aperture at 100 kV beam energy. The resist was then developed after removal of the Au layer using gold TFA wet etch chemistry. Resist development was performed in in 99% n-Amyl acetate CH₃COO[CH₂]₄CH₃ for 3 min, then 8:1 MIBK+IPA for 30 sec for high-resolution and then followed by 30 sec IPA rinse. A descum process was then performed using the M4L with the following recipe: 500mT pressure, 150 sccm O₂, 50 sccm He, 100W power for 2 min.

Succeeding the descum process, etch into SiO₂ layer, to create the nanochannel opening, was performed using the PT Versalock Dual Etch ICP with the following recipe: 5mT, RF1 150W chuck power, RF2 700W coil power, 50 sccm CF₄ for two 60sec + one 45sec segments. The etch rate of the SiO₂ layer was 160 nm.min⁻¹. Next, residual ZEP520A was removed by ashing in the M4L. Both the KLA-Tencore P-16+ stylus profilometer as well as the Nanometrics 8000X SE was used to confirm the removal of the residual ZEP520A.

4.2.4 Sacrificial Material Removal Results

The next step in the fabrication process is the removal of the sacrificial PNB material from the nanochannel by thermal decomposition. A tube furnace was utilized for the annealing of the samples. 8cc/min of ultrahigh purity N₂ was flown into the tube surface throughout the annealing process. In Table 4-4 the annealing recipe used to thermally decompose the PNB sacrificial material is presented. Removal of the sacrificial material
from the nanochannel was confirmed using FESEM and Olympus FV1000 Fluorescent Confocal Microscopy.

Table 4-4: Annealing recipe for PNB sacrificial material removal in ultrahigh purity N2 atmosphere.

<table>
<thead>
<tr>
<th>Step</th>
<th>Temperature</th>
<th>Time</th>
<th>Rate</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.</td>
<td>350 °C</td>
<td>5 min</td>
<td>5 °C/min</td>
</tr>
<tr>
<td>2.</td>
<td>500 °C</td>
<td>10 hours</td>
<td>1 °C/min</td>
</tr>
<tr>
<td>3.</td>
<td>500 °C</td>
<td>10 hours</td>
<td>1 °C/min</td>
</tr>
<tr>
<td>4.</td>
<td>25 °C</td>
<td>10 hours</td>
<td>1 °C/min</td>
</tr>
</tbody>
</table>

The fluorescent stain 4',6-diamidino-2-phenylindole DAPI was used for the experiment by directly dispersing the fabricated nanochannel device sample into a 10:1 dilution of DAPI for 5 min. The fluorescent material was drawn into the nanochannel through capillary forces. The sample was then rinsed in DI water for 5 min to wash away any residual DAPI from the background of the device. Therefore, this left the fluorescent material only confined in the nanochannels.

Figure 4-11 illustrates the results from the experiment. From the figure, clear formation of the nanochannel is illustrated from the confocal microscopy image. In Figure 4-11B, DAPI has successfully incorporated in to the empty nanochannel that has clearly formed from the FESEM images in Figure 4-11C-D. An interesting result from the annealing process is the diffusion of the Au catalyst structure into SiO2. Because the diffusion of Au into the oxide, SiO2 may not be the best capping material for the process of fabricating nanochannels using the thermally decomposable PNB sacrificial material. The diffusion issue of Au could be solved by using a barrier to inhibit the diffusion process or by optimizing the annealing recipe. Therefore, the devices fabricated from this experiment cannot be used for in-plane growth of SiNWs.
Figure 4-11: Results from the thermal decomposition experiments for sacrificial PNB material removal. A) Nanochannel device before annealing experiment. B) Post annealing of device in N₂ rich atmosphere. The fluorescence confocal image shows successful formation of the nanochannel through the observation of the fluorescence stain inside the nanochannel. C) Illustration of the empty nanochannel leading to the successful removal of the PNB material through thermal decomposition. The circle indicates the Au catalyst structure diffusing into the oxide material. D) Clear indication of the nanochannel inlet.
4.3 Organic Solvent Soluble ZEP520A

In this section, ZEP520A will be used as the sacrificial material to fabricate the nanochannels for in-plane growth of SiNWs. The interest in using ZEP520A as a sacrificial material is because, the sacrificial pattern can be defined directly with the electron beam and therefore, reducing the amount of post lithography etch processing. Moreover, ZEP520A can be easily removed from the nanochannel using Acetone, Nano Remover PG, Dimethylacetamide DMAC or N-methyl-2-pyroridone NMP, without any resist residue when compared to negative tone e-beam resists. In addition, ZEP520A can be removed with a combination of deep-UV exposure and solvent wet etch as well. But more importantly, the resist requires only a small amount of electron dose to design high resolution features. The next section will discuss the fabrication process of the nanochannels utilizing ZEP520A as the sacrificial material.

4.3.1 Sacrificial Material Patterning

A 3:1 anisole + ZEP520A dilution was prepared before spin coating the resist on patterned wafers containing alignment markers and Au catalyst structures. The overall process flow for the nanochannel device fabrication is illustrated in Figure 4-12. As can be seen from this nanochannel device structure, the Au catalyst structure is placed at one end of the nanochannel and only one inlet will be design for the nanochannel devices. The Au catalyst structures were fabricated by electron beam lithography followed by Au deposition and lift off. The Au catalyst fabrication process is exact to what was discussed in section 4.2.1, except, the Au catalysts structures were patterned on Si (100) prime 3inch
wafers with 15nm of HfO$_2$ deposited by ALD at 110 °C (Figure 4-12A). The surface of the substrate was modified by oxygen plasma to promote the adhesion of the resist material onto the HfO$_2$ surface. The M4L was utilized for this process with: 200W RF power, 600 mT pressure 150 sccm of O$_2$, 50 sccm of He for 60 sec. A 55nm thin film of 3:1 ZEP520A was spin coated onto the substrate using the recipe described in Table 4-5 (Figure 4-12B). Next, 15nm of Au was evaporated onto the substrate using thermal evaporation in the Semicore evaporator.

Figure 4-12: The figure illustrates the nanochannel fabrication process utilizing ZEP520A as the sacrificial material to form the nanochannel. There will only be one inlet for the nanochannel as opposed to two in the PNB sacrificial material previous nanochannel device design.
Succeeding the deposition of the 15nm Au conductive layer through thermal evaporation, the ZEP520A sacrificial line was defined through exposure of the resist in a way that allowed only a line of ZEP520A to be left after exposing the line boundary. As opposed to the design utilized to fabricate the nanochannels for the PNB sacrificial material as discussed in the previous section, both ends of the ZEP520A sacrificial line are not affixed to the substrate. This is because there are no post-development etch processes that are needed to define the sacrificial material. Figure 4-13 illustrates the fractured design that is utilized for writing the different layers with the electron beam. The Vistec EBPG5200 e-beam was used for the lithography process. The ZEP520A sacrificial line e-beam write parameters are: 170 uC/cm² electron dose, 5 nm resolution, 7nm beam spot size (500 pA current), 400um aperture at 100 kV beam energy. Succeeding conductive Au layer removal in TFA gold etchant, the substrate was developed in 99% n-Amyl acetate CH₃COO[CH₂]₅CH₃ for 3 min, then 8:1 MIBK+IPA for 30 sec for high-resolution and then followed by a 30 sec IPA rinse (Figure 4-12C).

The ZEP520A line was characterized by optical microscopy, FESEM and AFM for surface roughness measurements. Figure 4-14 illustrates some images of the ZEP520A

Table 4-5: Spin coat recipe for 55nm 3:1 anisole + ZEP520A. Thickness confirmed with the KLA-Tencore P-16+ stylus profilometer.

<table>
<thead>
<tr>
<th>Step</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1)</td>
<td>Static dispense ZEP520A wetting entire surface.</td>
</tr>
<tr>
<td>2)</td>
<td>Spin at 500 rpm with 1000 rpm/sec for 10 sec.</td>
</tr>
<tr>
<td>3)</td>
<td>Spin at 2000 rpm with 10000 rpm/sec for 70 sec.</td>
</tr>
<tr>
<td>4)</td>
<td>Bake at 180 °C for 3 min.</td>
</tr>
</tbody>
</table>

1) Static dispense ZEP520A wetting entire surface.
2) Spin at 500 rpm with 1000 rpm/sec for 10 sec.
3) Spin at 2000 rpm with 10000 rpm/sec for 70 sec.
4) Bake at 180 °C for 3 min.
A 50x50 nm area along the ZEP520A line was analyzed from a 5x5 μm scan taken with PeakForce QNM mode on the Bruker icon AFM for ZEP520A roughness properties. The resulting surface roughness of the 55nm ZEP520A line height was: $R_q = 2.75$ nm (root mean squared), $R_a = 2.31$nm (arithmetic average), $R_{\text{max}} = 12.5$ nm (maximum roughness). Although no experiments on improving the surface roughness of the sacrificial material was investigated in this thesis project, it is possible to potentially reduce the surface roughness of the ZEP520A line through controlled reflow of the resist at its glass transition temperature $T_g = 105$ °C.

**Figure 4-13:** The figure illustrates the nanochannel fabrication process utilizing ZEP520A as the sacrificial material to form the nanochannel. There will only be one inlet for the nanochannel as opposed to two in the PNB sacrificial material previous nanochannel device design.
Nevertheless, the roughness values are acceptable for proof of concept and for the fabrication of the nanochannels for the grow-in-place of SiNWs.

Next, the capping layer was deposited on to the substrate as depicted in the schematic in Figure 4-12D. Two samples were prepared with the HfO₂ capping layer. The first sample with 25 nm of HfO₂ of deposited with ALD at 110 °C, followed by 160 nm of SiO₂ deposited using e-beam evaporation in the Semicore evaporator with sample rotation. The second sample was prepared with 25 nm of HfO₂ deposited by e-beam evaporation, followed by 260 nm of SiO₂ deposited using e-beam evaporation both in the Kurt Lesker Lab-18 evaporator with sample rotation. Succeeding capping layer deposition, the samples were left in Nano Remover PG overnight at room temperature.

Figure 4-14: A) FESEM image of the ZEP520A line. B) Dark Field optical microscope image of the ZEP520A line aligned onto the Au catalyst structure. C) SPM image of ZEP520A line using PeakForce mode on the Bruker icon AFM.
for the liftoff process to proceed. Deposition of SiO$_2$ in the two samples was done to insure complete encapsulation of the sacrificial ZEP520A line structure. Successful liftoff of the resist that was left in the background was achieved, leaving only the ZEP520A sacrificial line and the Au catalyst structure encapsulated within the oxide capping layers.

Afterward, 500nm of ZEP520A was spin onto the substrate using a similar recipe in Table 4-2, except the spin speed was reduced from 4000 rpm to 2900 rpm. Thermal evaporation of 15nm Au was performed to serve as the conductive layer for e-beam lithography. The next lithography step was performed in order to create an etch window for the dry etch process. This window is to create the nanochannel inlet in the two samples that were prepared with differently deposited capping layers. The following beam write parameters were used for the lithography step: 380 uC/cm$^2$ electron dose, 100nm resolution, 110nm beam spot size (40 nA current), 400um aperture at 100 kV beam energy. Succeeding conductive Au layer removal, the substrate was developed in 99% n-Amyl acetate CH$_3$COO[CH$_2$]$_4$CH$_3$ for 3 min, then 8:1 MIBK+IPA for 30 sec for high-resolution and then followed by 30 sec IPA rinse and an O$_2$ descum in the M4IL as follow: 500mT pressure, 150 sccm O$_2$, 50 sccm He, 100W power for 2 min.

Post e-beam lithography, reactive ion etching into the SiO$_2$ and HfO$_2$ layers was performed using the PT Versalock Dual Etch ICP. First, 160nm of SiO$_2$ was etched using the following recipe: 5mT chamber pressure, RF1 chuck bias 10W, RF2 coil bias 300W, 30 sccm CHF$_3$ and 10 sccm CF$_4$ for 520 sec. The HfO$_2$ layer was then etched using the following recipe: 5mT chamber pressure, RF1 chuck bias 20W, RF2 coil bias 600W, 25 sccm BCl$_3$, 5 sccm Cl$_2$ for 48 sec. The resulting recipe over etched into the oxide capping layer in order to insure that the inlet of the nanochannel was fully exposed.
4.3.2 Sacrificial Material Removal Results

The ZEP520A line that is serving as the sacrificial material to form the nanochannel is removed through a combination of deep-UV exposure followed by removal in a solvent solution. First, ZEP520A is slightly decomposed inside the nanochannel using 185nm + 254nm deep-UV irradiation for 5 min. After exposure, the samples were left in NMP overnight and then rinsed in acetone, IPA and DI water each for 1 min. Next, the samples were left in Nano Remover PG at 60 °C for 5 hours to ensure removal of residual ZEP520A material from the nanochannel. This was followed by an acetone, IPA and DI water rinse each for 1 min and then a N₂ dry. Finally, the wafers were then de-hydrate baked for 5 min at 150 °C on a hotplate.

Through optical microscopy, successful formation of the nanochannel was observed in the sample where HfO₂ was deposited using e-beam evaporation. This was done by observing the color change of the nanochannel, before and after resist removal from the nanochannel structure. As for the sample with the ALD deposited HfO₂ capping layer, no clear color change was observed, even after repeating the sacrificial material removal process multiple times. Therefore, we found that it would be necessary to further investigate the sample with the ALD deposited layer by taking a Focus Ion Beam FIB cross-section at the nanochannel and analyzing the sample under the FESEM. The FEI Company Quanta 200 3D Dual Beam FIB was used for this experiment after sputtering a thin layer of Au and a thick layer of tungsten on to the sample using the gas injection system GIS. Following ion milling, the sample was analyzed under the FESEM and the resulting images are illustrated in Figure 4-15.
The results form Figure 4-15 showed that the ZEP520A sacrificial layer was left encapsulated within the nanochannel. It may be concluded that the ALD process can potentially incorporate precursor material during the pulse process, changing the structure and properties of the ZEP520A material inside the nanochannel. Similar results have been reported in the literature, where Al₂O₃ deposited by ALD has shown to incorporate into the surface of PMMA⁹⁴. Such material incorporation into the ZEP520A sacrificial material made the removal of the resist from the nanochannel difficult. Nevertheless, the sample with e-beam evaporated HfO₂ showed potential for in-plane growth of SiNWs. This will be discussed in the next chapter.

Figure 4-15: Both A and B are FESEM images of the FIB cross-sections of the sample where HfO₂ was deposited by ALD. The sample illustrated has done through the multiple steps to remove the ZEP520A from the nanochannel. No channel formation observed.
Results and Discussion Growth of Nanowires

5.1 Encapsulated Silicon Nanowire Growth Results

This section will provide information on the attempted growth of SiNWs within the nanochannel device that were fabricated using ZEP520A as the nanochannel sacrificial material and e-beam evaporated HfO$_2$ and SiO$_2$ as the capping material layers. First, 5x5 cm samples were clean via ultra-sonication in Acetone for 10 min, IPA for 10 min and then finally rinsed in DI water and N$_2$ dried. Nanowire growth via the encapsulated grow-in-place template was carried out in a hot-walled quartz tube low pressure chemical vapor deposition LPCVD system. An image of the tubular LPCVD reactor that was utilized is depicted in Figure 5-1.

Figure 5-1: Atomate hot-walled LPCVD system. Processing occurs in the quartz tube.
The samples were then placed in the LPCVD tube reactor and the temperature was raised to the growth temperature of 475 °C under the flow of N₂. Nanowire growth was then carried out at a total reactor pressure of 13T with SiH₄ flow rate of 100 sccm for one hour. The complete ramp and growth process of the SiNWs in the LPCVD is illustrated in the schematic Figure 5-2. After growth, the samples were left in the LPCVD system until the walls of the furnace cooled down to below < 100 °C.

![LPCVD SiNW Growth Process](image)

Figure 5-2: Atomate hot-walled LPCVD heating and gas flow process used for the encapsulated growth of SiNWs with SiH₄ as the precursor.

Both FESEM and optical microscopy were used to confirm the encapsulated growth of SiNWs. Typically a color change is observed with dark field optical...
microscopy when nanowire growth occurs inside the nanochannel. This is a quick and easy way to confirm successful growth of nanowires from an LPCVD run. From the optical images illustrated in Figure 4-3, a color change can be seen along the partial length of the nanowire. It can also be observed with the optical microscope, that nanowires have grown out of oxide capping layer at the Au catalyst structure. Further investigation of the growth results was done using the FESEM. From the FESEM images in Figure 5-3, not only is it clear that nanowire growth has occurred within the nanochannel material, but also some nanowire growth leaving the inlet of the nanochannel was also observed. Evidently, it is difficult from these results to determine the growth rate of the nanowires, due to the fact that there was a large growth length variation of the nanowires from one nanochannel device to another. Results has shown that the encapsulated SiNW growth length range between 20 um to 35 um with some SiNWs leaving the nanochannel inlet.

Moreover, reproducibility of the SiNW growth has been an issue for later LPCVD runs. Some growths lead to large amount of silicon deposition onto the surface of the devices, inhibiting the VLS growth of the nanowires in the nanochannel. In addition, some nanochannel devices showed silicon deposition at the inlet of the nanochannel, leading to the blockage of the inlets over time during the growth process. Because of the sidewall deposition of silicon at the inlet, saturation of the Au catalyst to achieve SiNW growth in the nanochannel did not occur in some devices. Nevertheless, the sidewall deposition can be suppressed by tweaking tube reactor conditions. Since this thesis is not concern with optimizing the CVD process, the samples what have shown successful
growth of SiNWs were further characterized with Transmission electron Microscopy TEM. This will be discussed in the next section.

Figure 5-3: A) Dark field image of encapsulated SiNW. B) and C) are FESEM images of a SiNW growing inside the nanochannel and leaving the nanochannel inlet. In addition, the FESEM images show growth of random nanowire above the Au catalyst surface, from out of the capping layer.
5.2 FIB HRTEM Sample Preparation

Successful grown SiNWs were further characterized using higher resolution TEM. A thin TEM slice of the nanochannel cross-section, where the SiNW is encapsulated, was prepared with a focus ion beam using the Quanta 200 3D Dual Beam FIB. The nanochannel cross-section was taken 8um away from the Au catalyst structure. This was to ensure that the TEM sample slice would be of silicon material and not Au. Creating the TEM slice began with sputtering a thin conductive layer of Au. This followed by the deposition of Tungsten and Platinum with the GIS. The ion milling process was then preform at different angles of the sample that will allow the Omni probe to then be used to manipulate and pull the slice off from its position in the sample. Finally, the slice was mounted onto a TEM grid and the ion beam was used to thin the sample out until it was transparent (<100nm). Figure 5-4 illustrates some of the SEM images from the FIB TEM sample prep.

Figure 5-4: A) Ion milling to define slice area. B) Release of slice from sample. C) Mounted slice onto TEM grid, followed by thinning the slice with the FIB.
5.3 Encapsulated Silicon Nanowire HRTEM Characterization

The prepared TEM sample was analyzed using the Jeol 2010F Field Emission-TEM at 200kV. First, the SiNW cross-section was located and analyzed by EDS for elemental confirmation. From the EDS results, the material encapsulated within the nanochannel structure was indeed silicon. This was concluded from the clear silicon peak observed at the core of the nanochannel cross-section. In addition to the silicon energy peak, a small Au peak was observed as well. When the EDS spot was placed on the edge of the nanochannel, only the Hf capping material energy peaks were observed. Therefore, the EDS results concluded the presence of a p-type silicon material encapsulated within HfO$_x$. Figure 5-5 illustrates the EDS results confirming the elemental observation of the nanochannel cross-section. But in-order to confirm that the silicon material is a single crystal nanowire, HRTEM images of the sample cross-section was analyzed at different tilt angels.

HRTEM images were obtained to asset the crystallographic orientation of the silicon material encapsulated within the cross-section. Further thinning of the sample was performed in the FIB, before retaking the HRTEM images. Figure 5-6 illustrates high resolution images of the nanochannel cross-section. From the images, single crystal silicon was confirmed. The only defect that is present in the HRTEM image is the observed SiNW twin. Because EDS was performed on the sample before taking higher resolution images, slight damage to the nanochannel cross-section can be observed. The EDS damage is not part of the SiNW crystallographic structure and should be ignored when analyzing the provided HRTEM images. The d-spacing from the evident crystal
planes were measured to be 3.130Å which is equivalent to the [111] calculated direction of 3.136Å. Figure 5-7 illustrates the crystal direction from the corresponding d-spacing. From the HRTEM images, the dimension of the nanowire was 36nm x 49nm. Moreover, correlated twin defects are often observed in SiNWs, particularly in nanowires of small diameters. The source of such defects and its effect on device operation is something that should be investigated in future works.

Figure 5-5: A) TEM image of sample cross-section. B) EDS analysis for cross-section core. Result show silicon material with Au impurities. D) EDS at the edge of the channel cross-section, confirming the presence of only Hafnium.
In addition, there is no clear crystallographic relationship between the capping layer material and the SiNW from the Si/HfO$_2$ boundary. Both HRTEM images as well as detraction patterns show that there is no epitaxial relationship between the silicon substrate and the HfO$_2$ layer deposited using ALD. The diffraction pattern for the silicon substrate and the substrate/HfO$_2$ boundary is illustrated in Figure 5-7B-C. This result shows that it may be possible to fabricated nanowire devices using the grow-in-place approach on different surfaces and confined materials, if the surface energetics of the material allows for high quality growth of SiNWs. However, HfO$_2$, deposited by e-beam
evaporation for our devices, has shown to be a good material starting point for the encapsulated growth of single crystal nanowires.

Furthermore, it is necessary to perform electrical measurements on the nanowires in order to fully relate their electrical properties to their growth inside these existing nanochannels. This will be the only way to fully obtain the functionality of the low dimensional semiconductor materials for high performance devices such as FETs. Electrical measurements were not performed in this thesis as it is out of the scope of the project. Nevertheless, the electrical device fabrication is essentially an extension to the nanochannel fabrication process that has been discussed in the previous chapter.

Figure 5-7: A) HRTEM of the crystal plane direction for the corresponding measured lattice d-spacing. B) Diffraction of the silicon (100) substrate. C) Diffraction pattern between the silicon substrate and the HfO$_2$ layer deposited by ALD. No crystallographic apparent relationship.
CHAPTER 6

Summery and Future Work

The alternative sacrificial materials that have been investigated in this thesis have brought up some interesting points to be considered when using electron beam lithography to define the sacrificial material structure. Because the chosen materials are polymeric in nature, it is important to study the crosslinking properties of the polymers before integrating the sacrificial material into device platforms. As shown from the use of the PAA material, strong crosslinking of the polymer was observed upon exposure to the electron beam. This resulted into the increase in dry etch resistance and decreased dry etch uniformity due to the formation of nanospherical structures. As a future work, understanding the degree of intermolecular crosslinking of polymers with electron beam exposure and its effect on the characteristics of the material may help better understand how to better make use of such polymer in processes containing such lithography techniques.

Moreover, results showed successful fabrication of nanochannels using both the PNB thermal decomposable as well as the solvent soluble ZEP520A sacrificial materials. Interestingly, the annealing process used to thermally decompose the PNB material from out of the nanochannel caused the diffusion of the Au catalyst into oxide material. Therefore, more work in investigating the role of the capping layer in controlling catalyst material diffusion as well as its surface energetic role in assisting in the growth of single crystal SiNWs with reduced defects must be performed. Although, the SiNW growth results from the nanochannel fabricated using ZEP520A as the sacrificial material to form
the nanochannel was promising, PVD deposited metal-oxides is a poor technique to be used for gate-oxide deposition and cannot directly provide a platform for FET devices. Therefore, to make full use of the grow-in-place approach for FET device fabrication, further investigation into the use of the capping layer as the gate-oxide material must be achieved.

Figure 6-1: Ultimate goal of the grow-in-place approach is to utilize the capping layer as the gate-oxide and the catalyst as an electrical contact
REFERENCES


