CHARACTERIZATION OF MULTI-FIN QUANTUM WELL STRUCTURES USING PHOTOCONDUCTANCE DECAY TECHNIQUE

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by

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ABSTRACT

The era of traditional ‘Moore’s Law’ scaling of transistors encountered a roadblock with problems like short channel effects and subthreshold leakage current increasingly plaguing the MOS devices. As a result the industry began to show a shift towards non-conventional approaches such as three-dimensional (non planar) device architecture. Electrical characterization techniques are used for probing electronic properties of the material systems, which serve as means of predicting their behavior in the final device. The conventional electrical characterization techniques could no longer be successfully and reliably used to characterize the ‘Fin’ structures with added complexities like vertical sidewall orientation and extremely confined geometry.

This work suggests adapting and evaluating the Photo-Conductance Decay (PCD) minority carrier lifetime measurement technique for specific needs of fin-shaped semiconductor material systems. In this work, multi-fin non-gated III-V test structures were used, wherein each fin is comprised of heterogeneously integrated multi-layer MBE grown In$_{0.7}$Ga$_{0.3}$As quantum well structures. Fin width was varied across the sample, thus leading to progressively more and more number of fins within the same area.

The PCD tool, built around a standard probe station, is a simple tool which allowed calculation of minority carrier lifetime from the extracted PCD curves. The results obtained confirmed the viability of the suggested PCD approach for multi-fin 3D structure characterization. The PCD curves depicted the fin surface and sidewall quality. Poorly formed fins gave a lower minority carrier lifetime, whereas lifetime shown by good quality fins was significantly higher. This work is also concerned with the effect of several surface passivation techniques on the minority carrier lifetime of III-V material systems.
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Chapter 1

INTRODUCTION

The semiconductor industry started over 50 years ago when semiconductor fabrication began to be considered a viable business. Today it is an industry worth more than 250 billion dollars. In order to meet the benchmarks set by The International Technology Roadmap for Semiconductors (ITRS) organization, the linear dimensions of MOS transistor have been reduced by 50 percent every 3 years, for the past 40 years. Since the late 1990’s, the Silicon-on-Insulator (SOI) type of transistors have become increasingly popular because of the growing concern about transistor off-state leakage, CMOS latch-up and parasitic capacitances. SOI transistors in their various forms have allowed for significant performance improvement and helped infuse new functionality into cutting-edge nanoscale devices [1].

As the transistor dimensions shrink, Short Channel Effects (SCE) [4], especially Drain Induced Barrier Lowering (DIBL), start plaguing the MOSFET. Thus for all practical purposes, shrinking the dimensions of the classical bulk MOSFET beyond 20 nm becomes very challenging. To continuously achieve transistor scaling while increasing current drive and achieving better control over short channel effects, the classical single gate planar structure of transistors has evolved into a three-dimensional multi-gate ‘Fin’ structure (FinFETs), wherein a fin-shaped body is surrounded by the gate dielectric and gate metal on three sides. Figure 1.1 shows an example of a fin transistor.
In addition to silicon FinFETs, research has also been carried out in the field of III-V FinFETs, wherein the channel consists of a III-V material [4]. These compound semiconductor materials could lend significant performance improvement to high speed low power applications. III-V materials possess excellent carrier transport properties such as very high electron mobility and low electron effective mass. As a result, extensive research is being carried out in the field of non-planar III-V devices, in an effort to achieve superior scalability and performance.

Electrical characterization of semiconductor material systems is broadly used for the purpose of determining either bulk or surface electronic properties, and also in process monitoring and diagnostics applications. Characterization reveals electronic properties of the material system, and this directly reflects their performance in the final device configuration. The issue gets complicated, however, when the aforementioned unconventional three-dimensional structures need to be electrically characterized.

This thesis proposes and explores an approach which adapts Photoconductance Decay (PCD) minority carrier measurement methodology to the specific needs of 3D, fin-shaped
semiconductor material systems. Chapter 2 compiles the necessary background information and reviews current literature on the subject. It covers transistor architecture considerations, compound semiconductor (III-V) properties, electrical characterization techniques and PCD measurement technique. Chapter 3 highlights the main objectives of the thesis and also discusses scope of this work. Chapter 4 describes the measurement setup, experimental procedure and details about minority carrier lifetime calculation. A brief description of preparation of samples used in the experiments is also included. Chapter 5 contains experimental results and related discussions. Chapter 6 summarizes the work and provides a conclusion based on the results obtained in this work.
Chapter 2

BACKGROUND

2.1 Developments in Transistor Architecture

A brief history of transistor architecture shows evolution from classical, planar, single gate devices, into three-dimensional multi-gate devices (which include double-gate, triple-gate and quadruple-gate) [6].

2.1.1 Planar Architecture

In the early 1990’s, Partially Depleted (PD) SOI MOSFETs were being widely used for special applications like high temperature electronics. However, the device operation was limited to supply voltages below 1 V. At this time, Fully Depleted (FD) SOI MOSFETs came into spotlight because of their improved electrostatic coupling between gate and channel. This led to an improved sub-threshold slope, better linearity of the device, and increased current drive. These advantages ensured the entry of FDSOI devices into various applications including low power, low voltage and RF circuits.

2.1.2 Three Dimensional Architecture

At a time when short channel effects, especially DIBL, began to hinder the scalability of a planar MOSFET, novel structures with non-planar architecture began to gain importance
among researchers. Non-planar ‘Fin’ structure devices show excellent sub-threshold slope on account of reduced DIBL, and also have better scalability compared to its planar counterpart. Superior channel control suppresses leakage currents leading to improved turn-off behavior. Further, ON-current is enhanced (multiplied) due to additional channels. Fin structures could also eliminate the need for channel doping and thus solve the problem of dopant fluctuations which nano-scale planar devices face. Higher stack heights allowed by Fin transistors enable additional area reduction. Several variations of the non-planar SOI multi gate MOSFET such as Tri-gate, Omega gate, pie gate and Gate-all-around have been explored in an attempt to achieve continual performance improvement of transistors [3],[5].

*Double gate SOI MOSFET*

T. Sekigawa and Y. Hayashi were the first to publish an article on the non planar double gate MOS transistor in 1984. Their work showed that it was possible to achieve significant reduction in short channel effects by using a fully depleted SOI device sandwiched between two gates connected to the same potential [7]. This reduction in short channel effects is achieved on account of reduced Drain Induced Barrier Lowering (DIBL). Lesser influence of the drain field on the channel improves the gate control over channel, thus reducing DIBL. Double gate MOSFETs consist of a fully depleted SOI ‘fin’ with the gate wrapped around the fin on two sides. Other variations of the double gate MOSFET include the Gate-All-Around (GAA) structure, wherein the gate is wrapped around three sides of the fin.
**Triple Gate MOSFET**

Triple gate MOSFETs are implemented either as a quantum wire or as the ‘Trigate’ MOSFET [8] which involves a narrow, thin silicon fin with gate around three sides. To further improve performance by means of improving electrostatic integrity, a variation of triple gate MOSFET called the ‘Pi-Gate MOSFET’ was developed. This device has its fin sidewalls extending into the buried oxide, giving it a shape similar to the greek letter ‘pi’. Pi-Gate MOSFET is simpler to fabricate than the Gate-All-Around (GAA) device, and yet possesses similar electrical characteristics. Another variation is the ‘Omega FinFET’ which has a close resemblance to the GAA device. It shows superior scalability similar to the GAA MOSFET, and also has easier manufacturing process like the FinFET. It has sidewalls similar to FinFET, a top gate like the Ultrathin Body (UTB) MOSFET, with gate extensions under the silicon body. The gate extension plays a crucial part in reducing DIBL because it shields the electric field lines from the drain and reduces control of the drain field on the channel.

**Surrounding-gate (quadruple-gate) SOI MOSFET**

Surrounding Gate or Quadruple Gate MOSFET was first fabricated by wrapping a gate electrode around a vertical silicon pillar. Theoretically this device offers the best electrostatic integrity and the best gate control over the channel [3]. Several variations like Multi-Bridge Channel MOSFET (MBCFET) and the Twin-Silicon-Nanowire MOSFET (TSNWFE) have been studied in an effort to increase the current drive per unit area.
2.1.3 Challenges Associated with Non-planar Structure

Even though 3D seems the way to go in order to continuously enable transistor scaling, several challenges are faced by these non-planar structures. Ultra-fine structures of the fin (active area) and the gate require optical lithography with some pattern reduction techniques. However, to achieve very small resolution (< 20 nm), optical lithography is replaced by SEM based electron beam lithography, which is costly and has a low throughput. Specific details about
process integration of 20 nm e-beam lithography and patterning of nanostructures are mentioned in reference [9].

Moreover, there are additional fabrication challenges such as using suitable etch processes with low surface damage. The quality of the sidewalls of fins is thus one of the major problems. The sidewalls usually contain large pits as a result of patterning steps and dry etching processes. The interface trap density of side walls of Fin structures is observed to be about 2.5 times higher than that of top walls [10]. Since the sidewalls act as ‘additional channels’ for carrier flow, their quality is of utmost importance in determining device performance and current drive. Techniques such as hydrogen annealing are being studied to improve quality of fin sidewalls [11].

2.2 Material Considerations for Transistors

2.2.1 Elemental Semiconductors

Ever since the first transistor was made in 1954, silicon has dominated the semiconductor industry as the material of choice for devices. The era of silicon scaling (known as ‘traditional scaling’) has lasted for approximately 40 years. Silicon is the most abundant element in nature, after oxygen. Its abundance, coupled with its unique ability to form high quality native oxide (silicon dioxide) have been some of the main reasons for silicon to remain the single most widely used material in the semiconductor industry for many years. Also, the fabrication technology for silicon is relatively cheaper and well established all these years, making it difficult for any other
material to become a serious contender to silicon in MOSFET technology in the immediate future.

For deeply scaled MOSFET applications, silicon faces challenges such as low drive current, short-channel effects and the sub-threshold leakage. In order to minimize these, approaches like shallow junctions, and ultra-thin gate dielectrics have to be used. These in turn interfere with the goals of achieving high carrier mobility and steep sub-threshold slope. As a solution to the problem of carrier mobility, germanium has been considered as a viable option since the late 1980s. Germanium possesses lower melting point compared to silicon, which opens up the possibility of using processes with lower thermal budget. Lower temperature processing also makes integration of metal gates easier, since metal gates otherwise do not support high temperature processing. Germanium possesses a relatively lower electron transverse mass and hole effective mass [12]. The high hole mobility is important from the viewpoint of PMOS transistors. It leads to a higher source injection velocity, thus improving drive current. It was at the 90 nm technology node that a new technological innovation, ‘uniaxial strain’ for mobility enhancement, was introduced. This innovation demanded use of silicon-germanium, to introduce uniaxial compressive strain in the PMOS channel, thus imparting drastic mobility improvements.

However, germanium has its set of disadvantages and challenges. Germanium needs to be heterogeneously integrated with silicon, and many researchers have an opinion that it could not be successfully used as the lone material for fabricating integrated circuits. Germanium passivation is another challenge, and so is reducing the high band-to-band tunneling leakage currents.
2.2.2 III-V Semiconductors

Compound semiconductor III-V materials possess very high electron mobility and low electron effective mass. This leads to a high injection velocity and thus a very high intrinsic speed of III-V devices. They offer increased performance with reduced power consumption. Good progress has been made in the development of III-V narrow band-gap quantum-well field-effect transistors (QWFETs) for high speed low power logic applications, as stated in reference [13]. The major advantage of such devices is that they can be operated under very low supply voltage, thus leading to low power dissipation, and can still achieve very high speed.

Various III-V materials possess unique advantages in terms of device performance and applications. Devices incorporating more indium usually show better high-frequency performance. InSb is a promising material, possessing the highest electron mobility and electron saturation velocity among all the known semiconductors. An InSb quantum well FET demonstrating an enhanced performance was first demonstrated in 2004, and has been described in reference [13]. Also, since the past few years, gallium nitride High Electron Mobility Transistors (HEMT) have been considered and studied as a very good option in high power applications. Hybrid FinFETs (HFinFET) consisting of a combination of High Electron Mobility Transistors (HEMT) and FinFETs have also been fabricated, and found to possess excellent scalability and performance [14].

Several emerging materials like carbon nanotubes and nanowires show promise for use in future high mobility transistors. However, III-V materials are more practical as far as patterning is concerned, because they do not face problems of precise alignment and positioning like nanotubes and nanowires [15].
Problems associated with III-V devices

In case of planar MOSFETs, III-V devices face a faster degradation in Short Channel Effects than silicon devices. This is primarily because of the narrow bandgap and higher dielectric constant of the III-V material. Boosting the on-current and achieving good off-state control was in general a big hurdle for planar III-V devices. To some extent the 3-D fin structure serves as a solution for this problem. It improves on and off state performance, and thus 3-D structure proves to be crucial in case of III-V devices. However, FinFET-like structure for compound semiconductors is relatively more difficult to fabricate because, unlike silicon technology, dry-etching for these materials is considered to be more difficult to control. This leads to the issue of surface damage during dry etching for III-V structures. Another critical aspect of III-V domain is that most researchers believe that III-V nanoelectronics will not replace silicon in the near future. It would in fact have to be integrated on to silicon.

Passivation Techniques for III-V Materials

Semiconductor surfaces contain dangling bonds, which are chemically and electrically active and can lead to instability of the material. To saturate and deactivate these bonds and render them inactive, the surface needs to be passivated with particular elements that assure chemical stability of the surface [16].

This thesis contains a brief study of surface passivation techniques of planar and non-planar compound semiconductor (III-V) structures; specifically, antimonides, arsenides,
phosphides and nitrides. It also gives a set of techniques to etch away native oxides from the surface of III-V semiconductor structures (Appendix A).

2.3 Electrical Characterization of Semiconductors:

2.3.1 Significance of material characterization

Electrical characterization is a means to probe and reveal electrical characteristics such as current-voltage relationship, resistivity, and minority carrier generation and recombination lifetimes. It is usually preferred to use techniques which could be easily applied to standard and routine test structures, and do not necessitate development of special test structures for the purpose of characterization.

2.3.2 Widely used electrical characterization techniques

Some of the common semiconductor characterization techniques that are being used successfully for the past few decades are: Atomic Force Microscopy (AFM), Scanning Tunneling Microscopy (STM), Photo-Conductance Decay (PCD), Scanning Electron Microscopy (SEM), Transmission Electron Microscopy (TEM), X-ray Photoelectron Spectroscopy (XPS). Reference [17] gives a detailed description of most of these techniques.
2.3.3 Characterization of three-dimensional structures

The above mentioned techniques could be applied successfully to devices and structures which are planar. However, characterization of 3 D structures has been a challenge, due to the added complexity involved in their structure, fabrication, processing and operation. Several attempts are being made to establish characterization techniques and to devise new metrics to gauge the quality of FinFET sidewall surface. The vertical orientation of the sidewalls makes it difficult to characterize their roughness and quality. Researchers have tried to modify the existing techniques to make them applicable to non-planar structures. However, an effective solution in the form of a simple, reproducible, non-destructive, relatively inexpensive and reliable technique to characterize non-planar structures is yet to be established.

Several issues arise on account of the extremely confined vertical and horizontal material systems involved in non planar, especially, ‘multi fin’ type of structures. Also, the ultra-thin epitaxial layers involved are very much susceptible to damage if some of the popular techniques are used to characterize them. For instance, the highly energetic Scanning Electron Microscopy (SEM) beam of electrons or Focused Ion Beam (FIB) gallium ions could rupture the ultra thin epitaxial films involved in fin structures. It could also induce charging effects on the very thin active layer of the device [18]. FIB technique could lead to gallium ion implantation causing induced shifts in the threshold voltage characteristics of the device. There have been efforts to characterize III-V fin structures using High Resolution X-Ray Diffraction (HR-XRD) and Raman Spectroscopy. However, expensive setup, sample heating, vacuum requirement, low throughput are some of the major problems these techniques face, and the complexity and very high aspect ratio of fins makes it more challenging. Gate patterning for fin devices is a difficult
process, and hence the characterization techniques which could be used on un-gated samples (prior to gate deposition) could prove to be very important.

Atomic Force Microscopy (AFM) is a powerful technique to characterize surface roughness. However, when applied to fin or non-planar structures, several modifications are essential because of the vertical orientation of fin sidewalls and nanoscale dimensions of fins. Measuring roughness of the inaccessible regions at the bottom of fin sidewalls is a serious challenge.

A number of modifications to the conventional technique have been tried, such as tilting the sample at a specific angle to make these regions accessible, or using different shaped tips to obtain high resolution in the lateral direction. Another approach involves cleaving the fin sample along the fin length and then polishing the sample edge using FIB technique, to approach the fin sidewall. However, most of these modifications and adaptations are very complicated and require sophisticated equipment.

Reference [19] explains an effective method for measuring fin sidewall roughness by conventional AFM technique. The fins are released by immersing in buffered HF solution to remove the buried oxide on which the fins stand. As a result of the release, the fin sidewalls are presented to the AFM probe tip in a direction parallel to the substrate, and can thus be characterized by conventional AFM probe tip. Figure 2.2 a) shows the original Si fins, and Figure 2.2 b) shows the fins after they are released. This method is quite effective; however it requires extensive sample preparation, and is not truly ‘non-destructive’ because it involves etching and releasing the fins. Also, the method has been tried on Si fins, but there have been no successful attempt yet to use it for III-V fin characterization.
Photoconductance Decay (PCD) Technique:

Photoconductance Decay method is one of the most widely used techniques to measure minority carrier lifetime of semiconductor materials. When a semiconductor material is illuminated with photons having energy more than the bandgap of the material, excess carriers are generated in the material. As a result, the sample conductivity increases, since its resistance decreases. If the light pulse is now abruptly shut off, then the conductivity slowly returns to its equilibrium value following an exponential decay with time. However, in practice, the decay is not purely exponential, due to the presence of traps and recombination centers in the material. The decay time constant depends on the lifetime of minority carriers. Due to the presence of traps and recombination centers, the decay represents two distinct lifetimes, the near surface and the bulk lifetime as shown in Figure 2.3.
2.4.1 Photo-carrier Generation and Recombination

The phenomenon of photoconductivity involves absorption of electromagnetic radiation by charge carriers, and a resultant change in the conductivity of the material. The newly generated carriers are said to be ‘photo-carriers’. Under steady-state illumination, a balance between electron and hole generation and recombination gives the following relation (equation 1) between the generated excess minority carrier density and the photocurrent density.

\[ J_{ph} = \Delta n \frac{qd}{\tau_{eff}} \]  

where \( \Delta n \) = concentration of excess electrons/holes, \( d \) = sample thickness,

\( \tau_{eff} \) = minority carrier lifetime

Excess carrier densities give rise to photoconductivity in the sample which is given as:

\[ \sigma_{ph} = q \Delta n (\mu_n + \mu_p) \]  

Figure 2.3: \( \log_{10} \) (PCD voltage) vs time curve shows 2 distinct slopes which can be used to separately calculate surface and bulk lifetime.
where $\mu_n$ and $\mu_p$ represent electron and hole mobility respectively.

Photoconductivity is also observed in doped materials when impurity atoms absorb photons of energy slightly less than the bandgap. Also, photons with energy much less than the bandgap can create free charge carriers by ionization of impurity atoms in doped semiconductors [20].

The distinction between traps and recombination centers is crucial since it has a direct impact on electrical properties of the semiconductor. Capturing centers are a result of impurities and defects present in the semiconductor. They can capture electrons (or holes), and how long the electron (or hole) stays in the ‘captured’ state will determine whether the center is a ‘trap’ or a ‘recombination center’. If the electron (or hole) stays in the captured state for a certain mean lifetime, and is then thermally ejected, then the capturing center is regarded as a trap. On the other hand, if a hole (or electron) is captured by the same capturing center before the electron (or hole) could be ejected, then the electron and hole would recombine. In that case, the capturing center is regarded as a recombination center [21]. Traps preferentially eliminate one type of carrier, whereas recombination centers simultaneously annihilate an electron and a hole.

The annihilation of excess electrons and holes takes place through different recombination mechanisms. Indirect semiconductors show non-radiative recombination via deep recombination centers in the forbidden gap. The energy release of excess carriers occurs through emission of phonons. Small bandgap semiconductors like InSb, and also degenerate semiconductors predominantly show Auger band-to-band recombination, which is a three particle process. As shown in Figure 2.4 ii), annihilation of an electron-hole pair takes place by electron-electron collision, and transfer of energy to the third particle (the electron). Similarly, Figure 2.4 i) shows annihilation of electron-hole pair by hole-hole collision, and energy transfer
to a third particle (the hole). The non-radiative Shockley-Read-Hall (SRH) recombination takes place via deep trap states within the forbidden energy gap. The trap could either be empty or filled, and can accordingly capture an electron or a hole. Figure 2.4 i) a) shows capture of a conduction band electron by an empty trap. Figure 2.4 i) b) shows emission of an electron by a filled trap. Similarly, Figure 2.4 i) c) shows capture of a hole by a filled trap and Figure 2.4 i) d) shows emission of a hole from an empty trap to the valence band.

Figure 2.4 i): Shockley–Read–Hall Recombination  Figure 2.4 ii): Band-to-band Auger Recombination

2.4.2 Minority Carrier Lifetime

Minority carrier lifetime depends largely on the concentration of defects and impurities in the material. As a result, it provides crucial information regarding the quality of the
A semiconductor for device applications. Lifetime of surface carriers could help to determine the quality of the surface. A higher lifetime indicates lesser traps and good quality surface. On the other hand, low lifetime values point towards high defect density or number of traps, and thus tells us that the surface quality is poor.

From equation 1 and equation 2, the minority carrier lifetime in terms of photocurrent and sample conductance is given as:

$$\tau_{\text{eff}} = \frac{\sigma_{\text{ph}} d}{J_{\text{ph}}(\mu_n + \mu_p)}$$

As shown in Figure 2.3, minority carrier lifetime depends upon the decay constant of the photoconductance decay curve. The initial slope of the curve corresponds to the near-surface lifetime of the carriers. This lifetime value gives information about the condition of the surface. The second slope of the PCD curve gives the bulk lifetime value, which is useful in studying properties in the bulk of the material.

### 2.4.3 PCD measurement Techniques

There are two common ways to implement the Photoconductance Decay (PCD) technique for minority carrier lifetime measurement [22]. The first method involves detection of change in photoconductivity based on microwave power reflection (Citarella et al 2002). This method involves an expensive setup. The second method requires formation of two Ohmic contacts on the surface of the sample, the contacts being separated by a few millimeters.
constant current is passed through the contacts, and the resulting change in photoconductivity is expressed in terms of change in voltage drop (or current) across the sample. This work involves the use of the second method (contact method) for PCD measurement in all the experiments conducted. The details about the experimental setup will be covered in chapter 4 (Experimental Setup).
Chapter 3

Scope and Objectives

The considerations in the previous chapters suggest that the industry is heading towards a future which would be increasingly dominated by complex, non-planar structures and material systems. Three-dimensional ‘Fin’ structures especially create the need for novel characterization techniques, which could respond to the challenges put forth by the emerging complex structures and material systems. The scope of this work involves investigation of electrical characterization methods for three-dimensional structures (FinFETs). Also, as the device geometries become more and more confined, the behavior and properties of surface of the device play a crucial role in determining the device electrical characteristics. Taking into account the significance of the surface properties, this thesis also explores the surface passivation techniques for several III-V material systems.

As the fin width of FinFET device gets smaller, conduction in sidewalls becomes more and more significant as compared to conduction in top surface of the fin. This is why sidewall surface quality and passivation becomes extremely crucial for narrow fin width devices.

The main objective of this work is to adapt and evaluate Photoconductance Decay (PCD) technique to measure minority carrier lifetime, and thus characterize multi-fin III-V material systems. The technique shows reproducible results when tested on a multi-fin III-V quantum well sample, containing structures with varying fin width and fin density. The ultimate goal of this work is to use this technique to monitor the outcome of fin patterning and etch processes and to study the effect of surface passivation techniques on the fin surface and sidewalls.
Chapter 4  
Experimental Procedure

4.1 Sample fabrication details:

The wafer used for the sample was a multi-layer III-V wafer. The sample was an ungated Multi-Fin Quantum Well Field Effect Transistor, as shown in Figure 4.1. The exact details of the sample fabrication are covered in reference [23]. This reference mentions the gated sample, however, PCD measurements were performed on the ungated sample. The sample consisted of a strained, high mobility $\text{In}_{0.7}\text{Ga}_{0.3}\text{As}$ quantum well channel surrounded by higher bandgap $\text{In}_{0.52}\text{Al}_{0.48}\text{As}$ buffer layers. InP was used as the substrate and high-k dielectric layer was deposited on top.

![Figure 4.1: Layer structure of wafer used for the fin sample [23]](image)
The fins were patterned using reactive ion etching (RIE) and e-beam lithography. The sample fabrication flow is briefly explained in Figure 4.2, with all the major fabrication steps included. The wafer was cleaned by boiling in acetone and isopropyl alcohol, followed by defining the source, drain and the alignment markers by electron beam lithography. This was followed by oxygen descumming and a BCl$_3$/Ar etch. The source-drain contact Ni(10nm)/Ge(30nm)/Au(80nm) was then formed by evaporation and lift-off, followed by contact annealing. Deep vertical isolation trenches of high aspect ratio were then defined by electron beam lithography, then the fins were patterned using Reactive Ion Etching and e beam lithography. The high-k dielectric was deposited at the end by Atomic Layer Deposition technique. Reference [23] gives a more detailed and complete description.

Figure 4.2: Sample fabrication process flow for the multi-fin quantum well sample
Figure 4.3 shows the sample as seen under the microscope. The entire sample is divided into four identical sets ‘A’, ‘B’, ‘C’ and ‘D’ shown in Figure 4.3 (a). This repetition gave a chance to check for reproducibility and reliability of results. Each set is an array of fin structures. Figure 4.3(b) shows a magnified version of array ‘B’, and then Figure 4.3(c) shows a further magnification of one of the fin structures present in the array. Each fin structure consists of a particular number of fins, with each fin possessing a particular fin width. Some nested dummy fins are also included to facilitate fin patterning using electron beam lithography.

![Figure 4.3: Sample view showing sets A,B,C,D and enlarged set B showing array of fins](image)

![Figure 4.4: Fin array showing variation in fin width and number of fins](image)

Figure 4.4 shows the layout of array B. Column 1 of this array consists of planar structures. Columns 2 onwards contain fin structures. As we go across the columns two to nine, the number of fins per structure and the width of each fin varies. The rightmost column has the narrowest fins, and the maximum number of fins packed within the same area. The variation
across rows is in the fin length. The effect of this parameter is not taken into consideration in the experiments for this work.

<table>
<thead>
<tr>
<th>Column Number</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
<th>5</th>
<th>6</th>
<th>7</th>
<th>8</th>
<th>9</th>
</tr>
</thead>
<tbody>
<tr>
<td>Fin width</td>
<td>Planar</td>
<td>1 um</td>
<td>500 nm</td>
<td>400 nm</td>
<td>300 nm</td>
<td>200 nm</td>
<td>150 nm</td>
<td>120 nm</td>
<td>80 nm</td>
</tr>
<tr>
<td>Number of fins</td>
<td>Planar</td>
<td>7</td>
<td>10</td>
<td>10</td>
<td>12</td>
<td>14</td>
<td>15</td>
<td>16</td>
<td>16</td>
</tr>
</tbody>
</table>

Table 4.1: Fin Width and Number of Fins in a Fin Array for the In$_{0.7}$Ga$_{0.3}$As Quantum Well Sample

### 4.2 Experimental Setup

The PCD measurements were performed using the tool [24] built around a typical probe station. The schematic of the measurement setup is shown in Figure 4.5. The sample is connected in series with a load resistance, the value of which can be determined experimentally. Two tungsten probes with tip diameter 0.25 mm are placed 3 mm apart on the sample with the help of vertical, horizontal and lateral sensitivity knobs to establish temporary Ohmic contact. A power supply (Keithley 236 source-measure unit) provides voltage to the probes through the load resistance (500kΩ potentiometer) whose value can be experimentally determined. The ideal value of the potentiometer is equal to the sample resistance. A 658 nm laser is with 30 mW output power used in order to obtain shallow absorption depths such that the PCD signal corresponds to surface of the fins, and not the bulk. A pulse generator (HP8131A) supplies
pulses to the laser. Light from the laser is shone on the sample, which generates photo-carriers. The laser is positioned using sensitivity knobs such that the light falls exactly between the two probes, and minimum light falls on the probes. A pulse generator HP8131A supplies voltage to the laser. The laser is easily replaceable with other wavelength lasers. The photocurrent is displayed on the source-measure unit and the oscilloscope displays PCD curves for the minority carriers in the sample. These PCD curves are a plot of voltage versus time. The voltage decay curve is a result of change in conductivity of the sample due to the laser light. The laser pulse period, duty cycle and the voltage provided by the voltage supply could be changed as per requirement. In the experiments conducted for this work, a laser pulse period of 200us, duty cycle of 10% and voltage of 5V were used to carry out the measurements. The data (photo-voltage values) is collected by means of an interface between the oscilloscope and a computer.

Figure 4.5: Schematic representation of PCD measurement setup
A visual basic program [24] allows the user to select the value of applied voltage, and collects the data. The minority carrier lifetime value for the sample can be calculated using the visual basic data and some plotting software. The visual basic program itself also calculates lifetime, however, it does so only for a specific set of values of the pulse time period and the time scale on the oscilloscope. The calculations for this work were carried out using a Matlab code [25] which provides more flexibility in terms of the pulse period and oscilloscope time scale.

4.4 Measurement Procedure

The PCD measurement technique used in this work was initially tested on planar silicon wafers and then on doped GaSb wafers to observe the photoconductance decay curves of the minority carriers [25]. The results showed that the technique is useful to study the near-surface region. Thereafter, non-planar multi-fin quantum well III-V samples (containing specific test structures) were used in the measurement setup. For each structure on the sample, the dark current and also the photocurrent after shining a laser of suitable wavelength were measured. The laser beam illuminated the entire area (all the fins) of the structure being tested. Thus the emerging signal could be assumed to have originated from all fins equally. The oscilloscope displayed the PCD curves (change in voltage with respect to time), which were then used to calculate the surface minority carrier lifetime. A visual basic code developed in ref [24] was used to acquire time resolved data from the oscilloscope. The code also extracts raw data and saves it in a text file so that it could be used for plotting and analysis purposes.
The carrier lifetime can be calculated from the PCD curve as shown in Figure 4.6. The peak and 0.8*peak points on the curve are used as a reference for the near-surface lifetime slope calculation. The lifetime is given as time taken by the PCD voltage to fall from peak value to (1/e)*peak value, on the corresponding (near-surface) slope.

Figure 4.6: Calculation of minority carrier lifetime from the PCD curve
Chapter 5

RESULTS AND DISCUSSION

The PCD near-surface characterization method and its application in studying the effect of surface passivation on planar semiconductor sample surface (Si, Ge, GaAs) had been studied in ref [24]. Ref [25] includes a comparative study of near-surface PCD and microwave PCD method. It also includes a study of semiconductor-dielectric interface (for Si/SiO\textsubscript{2}, Si/ Al\textsubscript{2}O\textsubscript{3}, Si/ Ta\textsubscript{2}O\textsubscript{5}, GaSb/ Al\textsubscript{2}O\textsubscript{3}) using near-surface PCD method. This work attempts to take forward this characterization method to adapt it to three-dimensional semiconductor material systems.

Preliminary results were obtained from experiments conducted on InGaAs quantum well fin samples, the description of which is included in section 4.1. These results suggest that the method is viable and gives meaningful PCD results.

If the PCD minority carrier method has to be used to characterize the near-surface region, and not the bulk region, then the pulse width of the illuminating laser should be relatively short (a few us). This would minimize the effect of carrier diffusion into the bulk. As a result, the lifetime obtained would be dominated by surface properties instead of bulk properties. However, using very short illumination pulse leads to a low signal to noise ratio. Due to high noise level, the lifetime cannot be reliably and reproducibly calculated. The laser used for this work had a 658 nm wavelength, 30 mW output power and pulse period of 200 us. The duty cycle was 10%, and hence the pulse width was 20 us.
5.1 Dark current and photo-current variation with change in fin width

The sample used consisted of planar structures and fin structures with varying fin width. The dark current measured on applying a voltage of 5 Volt to the sample varied depending upon the fin width, and quality of fin formation. Most of the structures showed higher dark current for fin width above 300 nm and below 1 um. Narrow fins showed low dark current on account of poor fin formation and thus poor sidewall quality. The dark current for planar structures was in between that for wide fin and narrow fin structures.

Figure 5.1 shows dark current variation for an array of fins from the sample. This particular structure showed high dark current (13-16 µA) for fin width between 300nm and 800nm. Minimum dark current (48 nA) was observed for the least fin width (80 nm), indicating poor fin formation quality. Planar structure showed dark current of about 6-7 µA. Current flows through the volume of the fins, and hence fin sidewall and top surface quality affects current.
Photocurrent also varied with a similar trend, but with larger values because of increase in conductivity due to the laser illumination. Average photocurrent values for the sample varied from 25-30 µA for wide fins, to less than 50 nA for very narrow fins. Figure 5.2 shows photocurrent variation for the same array of fins, as in Figure 5.1. For this array, the photocurrent for planar structure was observed to be around 9 µA.
5.2 Effect of fin width variation on minority carrier lifetime value

The sample consisted of structures with varying fin width (and thus, varying number of fins packed within the same area). It also contained planar structures, to facilitate comparison between planar and non planar structures. The minority carrier lifetime values obtained from experiments and calculations reflected the quality of fin formation. Fins with greater width were found to possess higher lifetime values than the narrower fins. The structures with a large number of narrow fins packed within the area, showed very low lifetime values and thus indicated poor fin formation. Also, the wider fin structures showed a more significant bulk component in the PCD curve, whereas narrower fins show lesser bulk and dominant surface contribution in the PCD curve. A possible explanation for the reduced lifetime values for narrower fins is that the narrower the fin, the more challenging is the fin patterning.
process. As a result, the dry etching, e-beam lithography and fin patterning makes the fin sidewall surface quality worse. Higher lifetime values (comparable to planar structure) for wider fins showed good quality of the fins. Narrow fins showed much lesser dark current, photocurrent and lifetime values as compared to wider fins. Figure 5.3 shows PCD plots with $\log_{10}(\text{PCD voltage})$ with respect to time (µs) for fin structures with fin width 500 nm (10 fins), 300 nm (12 fins), 150 nm (15 fins) and 80 nm (16 fins). The lifetime value decreased progressively from the 500 nm wide fin to the 80 nm narrow fin, from 9.5 µs to 4.5 µs.

![Figure 5.3: Plot showing PCD curves for different fin widths and number of fins. Corresponding lifetime values are also shown](image)

Figure 5.4 shows another set of PCD curves from a different fin array on the sample. The widest fin structure with 500 nm fin width showed a high lifetime, around 10.8 µs, and the narrowest one with a fin width of 80 nm showed a lifetime value of around 3.6 µs.
Figure 5.4: Plot showing PCD curves for different fin widths and number of fins. Corresponding lifetime values are also shown.

Figure 5.5: Plot showing decrease in minority carrier lifetime with increase in Fin width for 80nm, 150nm, 300nm and 500nm Fins.
5.3 Effect of Additional Processing (Lamp Exposure) on Dark Current, Photo-current and Lifetime values

This work is also concerned with the effect of some additional processing steps on the lifetime value. A set of experiments were designed to carry out processing steps on the fin sample, and then re-measure the minority carrier lifetime value using the PCD tool.

The first experiment involved removal organic impurities from the surface of the fins, by lamp exposure. The sample was subjected to Rapid Thermal Cleaning by lamp exposure in ambient air at 200°C for 30 seconds. The sample was then measured using the PCD tool. The fin structures now showed a change in dark current and photocurrent. These values increased by approximately 10 percent of their initial values. However, the increase in minority carrier lifetime value was not very conclusive because it was only about 2-3 percent of the initial value. Also, this increase is not conclusive enough because the standard deviation of the lifetime value measurements was almost equal to or greater than the increase in lifetime. Figure 5.6 shows the PCD curve of the structure tested before and after lamp cleaning.
Even though the lamp cleaning results were not conclusive enough, this does not suggest that the PCD tool was incapable of detecting the change in fin surface and sidewall quality. In fact, the processing method was not effective enough to improve the quality of fins substantially. The increase in current values simply indicated that the contacts might have gotten annealed, thus causing an increase in current.

5.4 Generation of carriers in the Multi-fin Structure

Since the fins contain multiple layers of different materials, it is crucial to study the carrier generation within the fins that the incident laser illumination causes. The incident laser beam uniformly illuminates all fins between the contacts, of the fin structure under
consideration, as shown in figure 5.7. Each layer in the fins absorbs specific amount of light depending upon the thickness of the layer, bandgap and absorption coefficient of the material and the incident light wavelength and intensity. Carrier generation in each layer depends on the internal quantum efficiency and thus the responsivity of the material at the incident wavelength.

Figure 5.7: Schematic showing laser beam illuminating all fins uniformly

To ensure that majority of the carrier generation takes place in the fins, and not in the substrate, the ideal fin geometry should be such that the exposed area of the fins including the top surface and sidewalls should be much greater than the exposed area of the substrate. If the substrate is transparent to the incident wavelength, then this issue would not arise because in that case, the substrate will not have any carrier generation. In the case of samples used for this work, the InP substrate is not transparent to the incident 658 nm wavelength and hence shows some carrier generation. To ensure that the PCD signal received is mainly originating from the fins, we need to calculate and ensure that carrier generation in the layers of the fins is dominant as
compared to carrier generation in the exposed substrate consisting of the In\textsubscript{0.52}Al\textsubscript{0.48}As buffer layer and the InP layer. Figure 5.8 shows a three-dimensional schematic of the multilayer fin, indicating the fin layers and the substrate layers. The Figure shows gated sample, but this work used the ungated sample.

![Figure 5.8: Three-dimensional schematic of the multilayer fin structure (gated sample) [23]](image)

The photon flux (radiative power) emerging from a layer of thickness ‘x’ when the incident photon flux is Io (W/cm\(^2\)) is given by Beer-Lambert Law as:

\[
I(x) = I_0 (1-R) e^{-\alpha x}
\]

(3)

where \(\alpha\) = absorption coefficient of the material,

\(R\) = normal incidence reflectivity of the material at incident wavelength
For the experiments carried out in this work, the incident laser light wavelength was 658 nm, corresponding to photon energy of 1.88 eV.

Assuming cylindrical radiant pattern from the laser (Figure 5.9), the incident photon intensity can be calculated. Calculations are mentioned in Appendix B.

![Figure 5.9: Illumination cylinder produced by the laser](image)

The photon flux emerging from each layer, after a part of it has been absorbed within the layer, can be calculated using equation (3). Detailed calculations have been mentioned in Appendix B.
<table>
<thead>
<tr>
<th>Layer</th>
<th>Bandgap (eV)</th>
<th>Thickness (nm)</th>
<th>Absorption Coefficient (α) at 1.88 eV</th>
<th>Penetration Depth at 1.88 eV</th>
<th>Percentage of total light absorbed</th>
</tr>
</thead>
<tbody>
<tr>
<td>High-k dielectric (Al₂O₃)</td>
<td>5.95</td>
<td>10</td>
<td>(no absorption)</td>
<td>(no absorption)</td>
<td>0 %</td>
</tr>
<tr>
<td>InP</td>
<td>1.34</td>
<td>2</td>
<td>6*10⁴ cm⁻¹</td>
<td>166.67 nm</td>
<td>1.2 %</td>
</tr>
<tr>
<td>The first In₀.₅₂Al₀.₄₈As layer</td>
<td>1.47</td>
<td>2</td>
<td>7*10⁴ cm⁻¹</td>
<td>143 nm</td>
<td>1.4 %</td>
</tr>
<tr>
<td>In₀.₇Ga₀.₃As Quantum Well layer</td>
<td>0.60</td>
<td>14</td>
<td>10⁵ cm⁻¹</td>
<td>100 nm</td>
<td>13 %</td>
</tr>
<tr>
<td>Delta doped In₀.₅₂Al₀.₄₈As layer</td>
<td>1.47</td>
<td>33</td>
<td>7*10⁴ cm⁻¹</td>
<td>143 nm</td>
<td>17.4 %</td>
</tr>
</tbody>
</table>

Table 5.1: Absorption of incident light in the different layers of the sample
Figure 5.10: Absorption coefficient of InP with respect to incident wavelength [26]

Figure 5.11: Absorption coefficient of In$_{1-x}$Ga$_x$As with respect to incident wavelength [26]
The generation of photocarriers due to the absorbed photons depends on the Internal Quantum Efficiency (\( \eta \)) and thus the responsivity of the layer materials at incident wavelength of 658 nm.

\[
\eta = \frac{\text{Number of photoelectrons created per second}}{\text{Number of incident photons per second}}
\]

\[
\eta = \frac{(hc/e\lambda)}{R(\lambda)}
\]

where \( R(\lambda) \) = Responsivity of the material at wavelength ‘\( \lambda \)’

Responsivity of InAlAs at wavelength of 658 nm is approximately 0.03 A/W, which can be obtained from Figure 5.11.

Figure 5.12: Responsivity of InAlAs with respect to incident wavelength [27]
Responsivity of InGaAs at 658 nm incident light is approximately equal to 0.2 A/W from Figure 5.12.

Figure 5.13: Responsivity of InGaAs with respect to incident wavelength [28]
To ensure that the PCD signal originates mainly from the quantum well and majority of the photocarriers generated originate from the quantum well, we need to calculate approximate number of photocarriers generated in the two layers with the maximum absorption of light. The amount of light absorbed is maximum in the InAlAs layer, followed by the quantum well InGaAs layer. However, InGaAs has much higher internal quantum efficiency and thus more photo-carriers are generated per second in this layer.

From eqn (4),

Internal Quantum efficiency ($\eta$) of InGaAs layer = 37.8 %

Internal Quantum efficiency ($\eta$) of InAlAs layer = 5.7 %

From the calculations in Appendix B,

Number of photoelectrons generated per second in InGaAs layer = $5 \times 10^{15}$

Number of photoelectrons generated per second in InAlAs layer = $9.6 \times 10^{14}$

Since the number of carriers generated in the quantum well is almost an order of magnitude greater than that generated in the InAlAs layer, we can conclude that the PCD signal mainly emerges from the quantum well.
Chapter 6

SUMMARY AND CONCLUSION

6.1 Summary

The thesis gives an introduction of non planar or ‘fin’ structures and electrical characterization techniques. It also mentions challenges associated with characterization of three-dimensional structures and the disadvantages of using some of the commonly used planar structure techniques to characterize non planar structures. The main objective of this work is to adapt and evaluate the Photoconductance Decay technique to characterize non planar or fin structures. The experimental setup and sample details for this work are described. The main results showing PCD curves for fin structures with varying fin width are included. These results indicate that the PCD tool can provide a viable method for electrical characterization of III-V fin structures. The lifetime is calculated using a Matlab code mentioned in reference [25]. Appendix B includes the calculations showing carrier generation in the various material layers of the fin sample. This work is also concerned with passivation of fin sidewalls, and the effect of passivation techniques on the lifetime value. Appendix A includes a table containing some of the main passivation techniques being used for surface passivation of III-V devices (specifically arsenides and antimonides). One of the preliminary surface processing techniques, the lamp cleaning method, was carried out on the fin sample. Future work includes further processing in terms of passivation of the fin sidewalls by sulfidizing or by plasma nitridation.
The results obtained and calculations carried out in this work suggest that the near-surface PCD measurement tool gives results that confirm the viability of this technique for fin structure characterization. This technique provides a non-destructive, simple, reproducible technique for fin characterization without the need for an expensive setup or formation of the MOS device.

### 6.2 Future Work

*Challenges and disadvantages associated with the method:*

The ideal wavelength to be used for the sample layer structure used in this work should be such that the carriers are generated only in the quantum well layer, and not in the buffer layers and the substrate material. In order to achieve sufficient near surface carrier generation and to minimize carrier generation in the bulk, a short wavelength high power laser is required. The ideal laser to be used would be one with wavelength around 1.2 µm, with a high power, above 30 mW.

For feature sizes below optical resolution limits, the results given by the PCD tool would be unreliable. Also, for some samples, like fins with very poor quality, the carrier lifetimes obtained could be very low. If the lifetime is lower than the standard deviation of the PCD tool, the results would not be reliable.
Considerations for future work include surface passivation of fins to reduce trap density and surface state density, and to improve the quality of fin sidewalls and top surface. Sulfur passivation of fin sidewalls can be carried out using ammonium sulfide solution or plasma nitridation can be carried out by exposing the fins to nitrogen plasma.

Tunable laser could be used to generate carriers in specific layers of a multi-layered fin structure, depending on the wavelength absorbed for the various layers. The carrier generation in the fin structure can be modeled using Monte Carlo simulations or Sentaurus device modeling EM wave solver. An ultra-violet laser could be used to calculate minority carrier lifetime in wide bandgap semiconductors, like GaN or AlGaN/GaN heterostructures. Some curve fitting operations of the obtained PCD curves could also be carried out.
## Appendix A

Table 6.1: Passivation Techniques for planar III-V devices

<table>
<thead>
<tr>
<th>Cleaning/Passivation Technique (Materials used)</th>
<th>Application (Semiconductor Materials and Devices)</th>
<th>Results/Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>Passivation by $\text{Si}_x\text{N}_y$, $\text{SiO}_2$, Polyimide, and Ammonium Sulfide [29]</td>
<td>$\text{InAs/GaSb SuperLattice Infrared}$ detectors</td>
<td>Deposition of $\text{Si}_x\text{N}_y$, $\text{SiO}_2$ at low temperature ($&lt;$300°C) is needed to avoid high surface leakage currents</td>
</tr>
<tr>
<td>Cleaning by wet etch with $\text{H}_3\text{PO}_4$, $\text{H}_2\text{O}_2$, and DI water, followed by a finishing etch of $\text{H}_2\text{SO}_4$, $\text{H}_2\text{O}_2$, and DI water [30]</td>
<td>$\text{InAs Photodiodes}$</td>
<td>Reduction in Reverse Leakage Current</td>
</tr>
<tr>
<td>Cleaning by Atomic Hydrogen (H*) [31]</td>
<td>Polar III-V materials, specifically: InAs (001,111A) InSb (001), GaSb (001) surfaces</td>
<td>Clean, well-ordered surface obtained. Supply of Sb4 flux from Knudsen Cell is needed in case of InSb, to avoid surface decomposition</td>
</tr>
<tr>
<td>Passivation by Argon-ion beam etching method [32]</td>
<td>Smoothes out surface roughness in InP, InAs, and InSb devices</td>
<td>Approximately 70-80% reduction in RMS roughness observed by Atomic Force Microscopy</td>
</tr>
<tr>
<td>Ammonium Sulfide Passivation: Samples soaked in ((\text{NH}_4)_2\text{S}:) H(_2\text{O}(1:4)) soln at 50(^\circ)C for 10 min. Then dried with dry nitrogen gas [33]</td>
<td>Improves surface properties of InAs/GaSb superlattices</td>
<td>Removes native oxides with minimal surface etching, then forms covalently bonded sulfur layer</td>
</tr>
<tr>
<td>---</td>
<td>---</td>
<td>---</td>
</tr>
<tr>
<td>Orientation-dependent Sulfide Passivation: Sulfidizing in 1 M Na(_2)S aqueous solution [34]</td>
<td>Improve Photoluminescence properties of InAs</td>
<td>Reduction in surface states by one order of magnitude, increase in photoluminescence intensity. Removes native oxides and elemental arsenic</td>
</tr>
<tr>
<td>Silicon Interface-Control Layer (ICL) based passivation technique [35]</td>
<td>To reduce III-V semiconductor surface state density in quantum wire transistors (GaAs, InGaAs)</td>
<td>Large reduction of Fermi level pinning, and anomalous side-gating is suppressed</td>
</tr>
<tr>
<td>Interface Passivation Technology to achieve good quality gate stacks on III-V materials [12]</td>
<td>To improve interface quality and reduce interface and bulk oxide trap charges</td>
<td>Surface treatment using SiH(_4), NH(_3), and PH(_3), followed by CF(_4) plasma treatment. Low interface trap density is achieved</td>
</tr>
<tr>
<td>Silane-Ammonia Surface Passivation Technology [36]</td>
<td>Passivation of High Mobility $\text{In}<em>{0.55}\text{Ga}</em>{0.47}\text{As}$ MOSFETs</td>
<td>Vacuum anneal at 520$^\circ$C to desorb native oxide, then $\text{SiH}_4 + \text{NH}_3$ treatment at 400$^\circ$C for 60 s under pressure of 5 torr to reduce interface state density</td>
</tr>
</tbody>
</table>
Appendix B

Calculations for carrier generation in the various layers of the fin sample:

Beer-Lambert Law (equation 3) gives the radiant intensity \( \text{W/cm}^2 \) at a distance \( x \) from the surface in terms of the incident intensity, reflectivity and absorption coefficient of the material:

\[
I(x) = I_0 e^{-\alpha x}
\]

The laser beam diameter is about 3 mm. Assuming cylindrical pattern of emerging light from laser (Figure 5.7), and assuming 1 cm separation between the beginning of the laser beam and the sample surface, we can calculate the incident photon intensity.

The incident photon intensity = Incident optical power/Area

Area = Area of illumination cylinder with diameter 3 mm and height 1 cm

Area = 9.57 cm\(^2\)

Incident photon intensity = 30 mW/9.57 cm\(^2\)

\[ I_0 = 3.13 \times 10^{-3} \text{ W/cm}^2 \]

Using the amount of light absorbed in each layer, we need to calculate the number of photocarriers generated by the absorbed photons in the layer.

Number of photoelectrons generated per second = Internal Quantum efficiency \(*\) Number of incident photons absorbed per second

Incident energy per second = Laser incident power (30 mW)
Number of incident photons per second = 0.03 * (λ/hc) \sim 10^{17} \text{ photons per second}

Number of incident photons absorbed per second = Percentage of incident light absorbed \times 10^{17} \text{ photons}

A detailed analysis of light entering each layer of the fins follows:

The incident light first encounters the high-k dielectric layer on the fins.

**High-k dielectric (Al}_2\text{O}_3\text{ layer:}\)**

Bandgap = 5.95 eV

Thickness of layer = 10 nm

Reflectance at normal incidence = 8% [37]

Since incident photon energy is much less than bandgap, no light is absorbed in the high-k dielectric layer. The layer is transparent to the 658 nm laser light. However, there is an 8% reflection from the surface, assuming normal incidence of light.

Hence, 92% of initial incident light passes through this layer and reaches the next layer (InP).

**InP layer:**

Bandgap = 1.34 eV

Thickness of the layer = 2 nm

Reflectance at normal incidence = 30% [38]

Absorption coefficient (α) of InP at 1.88 eV incident light = 6\times10^4 \text{ cm}^{-1} \text{ (from Figure 5.10)}
Penetration depth in InP layer = $1/\alpha = 166.67$ nm

Since the penetration depth of the incident light inside InP is quite large, very less light is absorbed in the thin 2 nm layer.

From eqn 3, $I(x)/I_0 = 0.699$

69.9 percent of light that is incident on this layer passes through it to the next layer, and only about 1% light is absorbed, the rest is reflected.

1 photon out of initial 100 photons are absorbed in this layer.

Since the light absorbed is very less, we would not calculate number of photons generated in this layer.

64.4% of initial light reaches the next layer.

**The first In$_{0.52}$Al$_{0.48}$As layer:**

Band gap = 1.47 eV [39]

Thickness of the layer = 2 nm

Reflectance at normal incidence = 37% (Very little information about optical coefficients is available for InAlAs alloys, hence the value of reflectivity has been estimated from that for InAs and AlAs materials) [40]

Absorption coefficient ($\alpha$) of In$_{0.52}$Al$_{0.48}$As at 1.88 eV incident light = $7*10^4$ cm$^{-1}$ [39]

Penetration depth in In$_{0.52}$Al$_{0.48}$As layer = $1/\alpha = 143$ nm

Very less light is absorbed by this ultrathin layer.
From eqn 3, $I(x)/I_0 = 0.62$

62 percent of light that is incident on this layer passes through it and reaches the quantum well layer.

About 40 percent of the initial light reaches the next (quantum well) layer.

1 photon out of initial 100 photons are absorbed in this layer.

Again, we would not calculate carrier generation in this ultra-thin layer.

**In$_{0.7}$Ga$_{0.3}$As Quantum Well layer:**

Band gap = 0.6 eV

Thickness of the layer = 14 nm

Reflectance at normal incidence = 32% [41]

Absorption coefficient ($\alpha$) of In$_{0.7}$Ga$_{0.3}$As at 1.88 eV incident light = $1*10^5$ cm$^{-1}$ (Figure 5.11)

Penetration depth in In$_{0.7}$Ga$_{0.3}$As layer = $1/\alpha = 100$ nm

From eqn 3, $I(x)/I_0 = 0.59$

59 percent of light that is incident on this layer passes through it without being absorbed.

23.6 percent of the initial light passes through this layer and reaches the next layer.

About 17 percent of incident light is absorbed in the quantum well layer, which is higher than all layers above it.

If 100 photons were incident on the sample, then 17 of them would be absorbed in the quantum well layer.
We would calculate number of photocarriers generated in this layer.

Number of photoelectrons generated per second = Internal Quantum efficiency * Number of photons absorbed in the layer

(Figure 5.13 is used to obtain responsivity which is then used to calculate internal quantum efficiency of In$_{0.7}$Ga$_{0.3}$As).

Number of photoelectrons generated per second = $0.378 \times 0.17 \times 10^{17} = 6.4 \times 10^{15}$ photons/sec

**Delta doped In$_{0.52}$Al$_{0.48}$As layer:**

Thickness of the layer = 33 nm

Reflectance at normal incidence = 37%

Only 8.7% of the initial light reaches this layer, after reflection.

Absorption coefficient ($\alpha$) of In$_{0.52}$Al$_{0.48}$As at 1.88 eV incident light = $7 \times 10^4$ cm$^{-1}$

Penetration depth in In$_{0.52}$Al$_{0.48}$As layer = $1/\alpha = 143$ nm

From eqn 3, $I(x)/I_0 = 0.5$

50 percent of light that is incident on this layer passes through it without being absorbed.

11.8 percent of the initial light reaches the next layer.

If 100 photons were incident on the sample, then about 11.8 of them would be absorbed in this layer.

Number of photoelectrons generated per second = Internal Quantum efficiency * Number of photons absorbed in the layer
(Figure 5.12 gives responsivity, which is used to obtain internal quantum efficiency of $\text{In}_{0.52}\text{Al}_{0.48}\text{As}$).

Number of photoelectrons generated per second $= 0.057 \times 0.118 \times 10^{17} = 6.7 \times 10^{14}$ photons/sec

**400 nm In$_{0.52}$Al$_{0.48}$As layer buffer layer:**

Assuming that all the remaining (after reflection from this layer) is absorbed in this buffer layer, because the thickness is greater than penetration depth of light in the material:

Number of photoelectrons generated per second $= 0.057 \times 0.11 \times 10^{17} = 6.24 \times 10^{14}$ photons/sec

However, considering reflections from sidewalls of fins, negligible light would reach the substrate.

This estimate shows that maximum photocarrier generation occurs in the In$_{0.7}$Ga$_{0.3}$As quantum well layer, and thus the PCD signal emerges mainly from the fin, and not from the substrate.
Appendix C

PCD near-surface measurement tool setup

Figure 6.1: PCD near-surface measurement tool setup [25]
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