HIGH CURRENT DENSITY STABILITY OF
OHMIC CONTACTS TO SILICON CARBIDE

A Dissertation in
Materials Science and Engineering

by

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ABSTRACT

The materials properties of SiC, such as wide bandgap, high breakdown electric field, and good thermal conductivity, make it an appealing option for high temperature and high power applications. The replacement of Si devices with SiC components could lead to a reduction in device size, weight, complexity, and cooling requirements along with an increase in device efficiency. One area of concern under high temperature or high current operation is the stability of the ohmic contacts. Ohmic contact degradation can cause an increase in parasitic resistance, which can diminish device performance. While contact studies have primarily focused on the high temperature stability of ohmic contacts to SiC, different failure mechanisms may arise under high current density stressing due to the influence of electromigration. In addition, preferential degradation may occur at the anode or cathode due to the directionality of current flow, known as a polarity effect.

The failure mechanisms of ohmic contacts to p-type SiC under high current density stressing are explored. Complementary materials characterization techniques were used to analyze contact degradation, particularly the use of cross-sections prepared by focused ion beam for imaging using field emission scanning electron microscopy and elemental analysis using Auger electron spectroscopy. Initially the degradation of commonly studied Ni and Al-based contacts was investigated under continuous DC current. The contact metallization included a bond pad consisting of a TiW diffusion barrier and thick Au overlayer. The Ni contacts were found to degrade due to the growth of voids within the ohmic contact layer, which were initially produced during the high temperature Ni/SiC ohmic contact anneal. The Al-based contacts degraded due to the
movement of Al from the ohmic contact layer to the surface of the Au bond pad, and the
movement of Au into the ohmic contact layer from the bond pad. The inequality of Al
and Au fluxes generated voiding within the ohmic contact layer causing a large increase
in contact resistance.

A bottom to top approach was used to develop a more robust contact structure
based on the failure mechanisms of the Ni and Al-based contacts. Contacts utilizing a Pd
layer contacting the SiC were found to provide a lower specific contact resistance ($\rho_c$)
and improved stability under current stressing. A Pd/Ti contact was introduced that when
annealed under a N$_2$ atmosphere produced a robust TiN layer at the surface of the contact.
The $\rho_c$ of the Pd/Ti contact was (4.7±1.7)x10$^{-6}$ $\Omega \text{ cm}^2$, compared to the Ni and Al-based
contacts, all of which had a $\rho_c$ of greater than 10$^{-5}$ $\Omega \text{ cm}^2$. The Pd/Ti contacts were able
to withstand higher currents than the Ni or Al-based contacts under continuous DC
current stressing. The degradation mechanism of the Pd/Ti contacts depended on
whether the current was pulsed or continuous. Under continuous DC stressing, Au from
the bond pad diffused through the TiW barrier and into the ohmic contact region leading
to severe intermixing and voiding. Under pulsed DC stressing, voiding at the Au/TiW
interface occurred caused by the electromigration of Au. The different degradation
mechanisms were related to the temperature during stressing, as the temperature of the
continuous DC stressed contacts exceeded 649 °C at failure, while the peak temperature
of the pulsed DC contacts was between 316 °C and 371 °C, using 5 $\mu$s pulses and a 10%
duty cycle.

Finally, the lowest $\rho_c$, (1.4±0.6)x10$^{-6}$ $\Omega \text{ cm}^2$, was attained with a Pd/Ti/Pt contact,
which also possessed a very smooth surface morphology, especially compared to the
conventional Ti/Al contact. The Pd/Ti/Pt contacts were also shown to be more stable under continuous DC lateral current stressing than the Ti/Al contacts. A polarity effect on temperature was observed during stressing with the temperature of the cathode being higher than the anode, likely due to carrier recombination at the cathode for the p-type material. The increased temperature caused preferential degradation of the cathode of both the Pd/Ti/Pt and Ti/Al contacts. Under continuous DC stressing, degradation of the Pd/Ti/Pt contacts was characterized by voiding and intermixing at the leading edge of the cathode. The temperature of the Pd/Ti/Pt contacts during stressing was reduced under pulsed DC current, and voiding was observed between the Au bond pad and the ohmic contact. Mechanical stresses and thermal cycling were suspected to have produced the voiding under pulsed DC stressing.
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Finally I am not sure where I would be without my family.
Chapter 1

Introduction

1.1 Introduction

In the semiconductor industry, silicon (Si) has played the dominant role as the material of choice for most applications. There are, however, areas where the intrinsic capabilities of Si can be surpassed, particularly in the areas high temperature and high power needs. A potential candidate for such a replacement material is the wide bandgap semiconductor silicon carbide (SiC). Electroluminescence from SiC was first shown by Round in 1907 [1], but it was not until the late 1980’s when Cree, Inc., was founded and introduced the first blue LED [2] that SiC research garnered significant attention. Table 1 lists some important material properties of some semiconductors of interest. Numerical values can vary slightly depending on the reference, and the values used in this table were tabulated by Mishra et al. [3]. Since SiC has many polytypes, or crystal structures, the 4H structure is listed, which is currently the most technologically important structure as well as the material studied here. The intrinsic carrier concentration, \( n_i \), of a material is dependent on the bandgap, \( E_g \), and temperature, \( T \), through \( n_i \propto \exp(-E_g/T) \). The higher bandgap allows a material to have a lower \( n_i \) at a given temperature. A low \( n_i \) is very important for high power/temperature applications as thermally generated carriers can degrade device performance. The critical or breakdown electrical field, \( E_{BD} \), is another important parameter for high power operation as it describes the maximum field across the material before breakdown occurs. For a higher \( E_{BD} \), a thinner and higher doped voltage-blocking layer can be used for a given voltage requirement, which can reduce the on-resistance of the device [4]. High saturation
velocity, $v_s$, and mobility, $\mu$, are needed for high speed, high frequency devices. Thermal conductivity, $\kappa$, is important for heat dissipation during device operation.

**Table 1-1:** Material properties and figures of merit (normalized to Si) of select semiconductors [3,5,6,8].

<table>
<thead>
<tr>
<th></th>
<th>Si</th>
<th>GaAs</th>
<th>4H-SiC</th>
<th>GaN</th>
<th>Diamond</th>
</tr>
</thead>
<tbody>
<tr>
<td>$E_g$ (eV)</td>
<td>1.1</td>
<td>1.42</td>
<td>3.26</td>
<td>3.39</td>
<td>5.45</td>
</tr>
<tr>
<td>$n_i$ (cm$^{-3}$) (300 K)</td>
<td>1.5x10$^{10}$</td>
<td>1.5x10$^6$</td>
<td>8.2x10$^{-9}$</td>
<td>1.9x10$^{-10}$</td>
<td>1.6x10$^{-27}$</td>
</tr>
<tr>
<td>$\varepsilon_r$</td>
<td>11.8</td>
<td>13.1</td>
<td>10</td>
<td>9</td>
<td>5.5</td>
</tr>
<tr>
<td>$\mu_n$ (cm$^2$/V s)</td>
<td>1350</td>
<td>8500</td>
<td>700</td>
<td>1200 (Bulk)</td>
<td>1900</td>
</tr>
<tr>
<td>$v_s$ (10$^7$ cm/s)</td>
<td>1.0</td>
<td>1.0</td>
<td>2.0</td>
<td>2.5</td>
<td>2.7</td>
</tr>
<tr>
<td>$E_{BD}$ (MV/cm)</td>
<td>0.3</td>
<td>0.4</td>
<td>3.0</td>
<td>3.3</td>
<td>5.6</td>
</tr>
<tr>
<td>$\kappa$ (W/cm K)</td>
<td>1.5</td>
<td>0.43</td>
<td>4.5</td>
<td>1.3</td>
<td>20</td>
</tr>
<tr>
<td>JFOM $E_{BD}v_s/2\pi$</td>
<td>1</td>
<td>1.3</td>
<td>20</td>
<td>28</td>
<td>50</td>
</tr>
<tr>
<td>BFOM $\varepsilon_r\mu E_{BD}^3$</td>
<td>1</td>
<td>17</td>
<td>440</td>
<td>900 (Bulk)</td>
<td>4300</td>
</tr>
<tr>
<td>CFOM $\kappa\varepsilon_r\mu v_s E_{BD}^2$</td>
<td>1</td>
<td>4</td>
<td>260</td>
<td>180 (Bulk)</td>
<td>8200</td>
</tr>
</tbody>
</table>

Another way to compare semiconductors for device applications is through figures of merit (FOM). Three different FOMs are listed in Table 1-1. Johnson’s FOM (JFOM) [5] describes the power handling and high frequency potential of a device. Baliga’s FOM (BFOM) [6], where $\varepsilon_r$ is the dielectric constant, is more appropriately used for power devices under low frequency operation [7]. Finally the combined FOM (CFOM) [8] characterizes high frequency/power/temperature operations. From Table 1-1, it is easy to discern that the wide bandgap semiconductors on the right side, SiC, gallium nitride (GaN), and diamond, dominate Si and gallium arsenide (GaAs) in these respects. While diamond certainly has the best properties listed, growth and doping of the material are huge hurdles that need to be overcome [9]. GaN is another great candidate for high power applications, particularly at high frequencies, due to the
formation of a high electron mobility two-dimensional electron gas (2DEG) that can be produced at the interface between GaN and other III-N compounds. The phenomenon is being exploited for high electron mobility transistors (HEMT). HEMTs have high carrier concentrations and high mobilities, which allow for a low channel resistance and high current density [3]. This is of great technological importance for high frequency operations. The shortcomings of GaN are the lack of bulk GaN material (GaN is typically grown on SiC or sapphire substrates) and difficulty with p-type doping.

One advantage that SiC enjoys over GaN and diamond are the availability of bulk substrates and doping capabilities. Recently, in August, 2010, Cree, Inc., announced 150 mm SiC substrates [2], which will further decrease the cost per device. Even with the availability of 150 mm wafers looming, the cost of SiC wafers is still great compared to Si. Despite the higher costs of SiC, the advantages in material properties and FOMs SiC enjoys over Si makes it an attractive alternative, particularly when comparing $E_g$, $E_{BD}$, $v_s$, and $\kappa$ (3x larger than GaN), all of which are reflected in the FOMs listed in Table 1-1. These properties will allow SiC devices to be smaller than Si counterparts as well as lessen the cooling requirements needed for operation, which take up additional space. In addition, SiC components will be able to be used in environments not possible with Si devices. The ability to grow SiO$_2$ on SiC is another advantage of SiC [10]. The use of SiC devices is described in the next section.

1.2 SiC Applications

The previous section illustrated the many SiC material properties that makes it attractive for high power, high temperature devices. Neudeck et al. describes the need
for wide bandgap materials for high temperature environments discussed below and listed in Table 1-2 [11]. Such applications and industries include automotive, turbine engines, spacecraft, high temperature industrial processing, and deep-well oil drilling. The limit for Si device operation is set at around 200 °C. While silicon-on-insulator technology (SOI) is appropriate for low-power operation up to 300 °C, high power applications can create excess heating in the high current on-state, during switching when dynamic power dissipation occurs, and in the off-state power from leakage currents. In addition, lateral SOI devices may suffer from worsened thermal management due to the buried oxide insulator. The need for added cooling systems with included overhead, such as longer wires, more connectors, and extra plumbing increase costs, size and weight, and complexity, which can increase reliability concerns. The ability to use wide bandgap materials directly in high temperature environments, such as engines, can increase efficiency and safety. NASA has recently demonstrated SiC junction field effect transistors (JFET) operable at 500 °C in air for up to 10,000 h [12]. Realization of high temperature operation will also hinge on packaging concerns.
Table 1-2: Possible high temperature applications for wide bandgap semiconductors [11].

<table>
<thead>
<tr>
<th></th>
<th>Peak Ambient Temperature (°C)</th>
<th>Chip Power (kW)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Automotive</td>
<td></td>
<td></td>
</tr>
<tr>
<td>On-cylinder and exhaust pipe</td>
<td>600</td>
<td>&lt; 1</td>
</tr>
<tr>
<td>Electric suspension and brakes</td>
<td>250</td>
<td>&gt; 10</td>
</tr>
<tr>
<td>Electric/hybrid vehicle</td>
<td>150</td>
<td>&gt; 10</td>
</tr>
<tr>
<td>Turbine engine</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Sensory and control</td>
<td>600</td>
<td>&lt; 1</td>
</tr>
<tr>
<td>Electric actuation</td>
<td>150</td>
<td>&gt; 10</td>
</tr>
<tr>
<td>Electric actuation</td>
<td>600</td>
<td>&gt; 10</td>
</tr>
<tr>
<td>Spacecraft</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Power management</td>
<td>150</td>
<td>&gt;1</td>
</tr>
<tr>
<td>Power management</td>
<td>300</td>
<td>&gt;10</td>
</tr>
<tr>
<td>Venus and Mercury exploration</td>
<td>550</td>
<td>~1</td>
</tr>
<tr>
<td>Industrial high temperature processing</td>
<td>600</td>
<td>&lt; 1</td>
</tr>
<tr>
<td>Deep-well drilling</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Oil and gas</td>
<td>300</td>
<td>&lt; 1</td>
</tr>
<tr>
<td>Geothermal</td>
<td>600</td>
<td>&lt; 1</td>
</tr>
</tbody>
</table>

With energy use in the United States being estimated at $10^{14}$ BTUs [13], more efficient device technology is necessary for reduced power consumption. The high-power electronics market is estimated at $16$ billion and increasing at a rate of $10\%$ per year [14]. Figure 1-1 illustrates the voltage/current ratings for power applications and the blocking voltages of Si and SiC power devices [4,13]. Most power device usage is in a range of a few hundred or thousand volts at one to several hundred amps, as shown in Figure 1-1a, where SiC devices can be beneficial (Figure 1-1b), and if a 5\% improvement of efficiency is assumed for SiC devices over Si devices, then approximately $50$ billion can be saved annually in the US, not including the additional savings from reduced cooling expenses [14]. Recent simulations show that the replacement of a Si inverter with a SiC inverter can improve fuel economy in a conventional hybrid electric vehicle.
(HEV) by 14.7% and a plug-in HEV by 18.1% [15]. Some areas of high power electronics where SiC can be advantageous are power conversion and pulsed power applications [16]. Bipolar devices such as bipolar junction transistors (BJT), insulated gate bipolar transistors (IGBT), and gate turn-off thyristors (GTO) may provide the high voltage blocking (> 6.5 kV) and current capacity (> 1 kA) with low on-resistance needed for applications such as heavy duty traction motor drives, power distribution systems, electric guns, and fault current limiters [17]. Unipolar devices such as Schottky diodes and field effect transistors may be more ideal for lower voltages and higher switching speeds [4].

![Figure 1-1: (a) Voltage/current ratings for some power applications [13] and (b) blocking voltage ratings for Si and SiC devices [4]. Reprinted with permission from [13], Copyright 2008, IEEE. Reprinted with permission from [4], Copyright 2010, IEEE.]
1.3 Contact Reliability

Although the previous two sections have outlined the advantages of SiC in terms of material properties over Si and potential applications and benefits of replacing Si in high temperature and high power applications, there are many other factors that must be considered before SiC implementation. One such necessity is the stability of metal/semiconductor contacts. Ideally, metal/semiconductor contacts are classified as either Schottky or ohmic. Schottky contacts exhibit nonlinear current-voltage (I-V) characteristics with a low leakage current in the reverse bias and a large current in the forward bias. Linear I-V characteristics are indicative of an ohmic contact, which is usually engineered to have a low resistance. Both contacts are important in devices, but ohmic contacts will be the focus of this study. Ohmic contacts allow current to flow through a device. A low voltage drop, or contact resistance, is required across the contacts in order to take advantage of the intrinsic properties of the device, and if unstable or too high, the additional parasitic resistance from contacts can degrade the device performance.

The metal/semiconductor interface controls the properties of the ohmic contacts. For high temperature and high power operation of SiC devices, this interface, and thus the contact resistance and device functionality, can be compromised. Under high temperature operation, failure mechanisms such as oxidation and reactions can affect the contact resistance. Long term stability of ohmic contacts under high temperature annealing, between 350 °C and 650 °C for tens to thousands of hours, have been the focus for many studies already [18-26]. Annealing environments include air [18,19,21-24], inert gas such as N₂ [20], and vacuum [25,26]. While these studies provide insight into
the possible failure mechanisms of contacts to SiC under high temperature operation, high power devices may require large current densities through the contacts. In addition to thermal concerns from Joule, or resistive, heating, high current densities also introduce reliability issues related to electromigration, or the movement of atoms due to the momentum transfer from conducting electrons [27]. Studies into contact damage of Si devices were spurred by the increase in current density due to scaling of integrated circuits [28-36]. These studies illustrate how diffusion and reactions can occur between the semiconductor and the contact metallization or between the metals in the contact. Failure due to an increase in parasitic contact resistance causing thermal runaway, the creation of voids generating an open circuit, or junction shorting producing an unacceptable leakage current were observed. These mechanisms were not observed under thermal annealing alone, and in some cases preferential degradation occurred at the anode or cathode [28-30,32-35]. Unlike Si, high current densities from the scaling of SiC devices to sub-micron dimensions may not be an area of concern, but high currents may be present in high power devices, especially under pulsed power operations which can require fast rise-times on the order of 10 kA/µs [16] and operation currents of ~20 kA/cm² [17], with a single device being demonstrated at 12.8 kA/cm² [37]. A scanning electron microscope (SEM) image showing failure of a SiC GTO at the edge of the anode due to current crowding is shown in Figure 1-2 [16].
1.4 Focus

The goal of this study was to explore the degradation mechanisms of ohmic contacts to SiC under high current densities and to develop and optimize more robust ohmic contacts with improved contact resistance. Additionally, failure modes of contacts under continuous DC and pulsed DC stress, using both vertical and lateral current flow, will be investigated, as any of these stressing situations are possible depending on device configuration. Initial work focused on developing a suitable testing structure based on the available material and on the failure of commonly studied contacts in order to develop a baseline for contact stability, as well as understand any shortcomings of the contacts with regards to high current density stability. Contact failure was assessed through a combination of both electrical and materials characterization. Further contact improvement and optimization was based on the initial studies as well as published studies. Ultimately this dissertation sought to establish a procedure for the testing of
contacts under high current densities as well as guidelines for improving the stability of contacts, not only to SiC, but also to other material systems.

1.5 References


Chapter 2

Literature Review

2.1 Introduction

This chapter will present the necessary background and cite examples in order to better understand the goals described in the previous chapter and the results and discussions in subsequent chapters. As mentioned, the focus of this study is to investigate failure mechanisms of contacts to SiC under high current density and develop more stable, lower resistance contacts. First, some general concepts of ohmic contact formation and carrier transport mechanisms will be introduced in Section 2.2, followed by the examination of contacts to SiC in Section 2.3, which will focus on the contacts or similar contacts to those used in this study. Section 2.4 and 2.5 will concentrate on the degradation of ohmic contacts, with contacts to SiC being the focus of the high temperature degradation section, and the high current density degradation section centering around contacts to Si due to the lack of SiC related studies. Emphasis will be placed on electromigration and polarity effects when reviewing high current density stressing. Finally the main aspects of the entire literature review will be revisited in the final section.

2.2 Metal/Semiconductor Contacts

In order to investigate the degradation and improvement of ohmic contacts, it is imperative to understand the various concepts behind metal/semiconductor junctions. The following subsections will discuss the theories behind the barrier formation created at metal/semiconductor interfaces as well as the carrier transport mechanisms occurring
at the contact. These ideas will help in the comprehension of producing an ohmic contact.

2.2.1 Metal/Semiconductor Interfaces

There are many models that predict what phenomena occur when a metal and semiconductor come into contact, some of which are detailed in a book by Rhoderick and Williams [1], which is followed here. One of the most straightforward ideas is the from the Schottky-Mott theory. Figure 2-1a illustrates the band structure of a metal and an n-type semiconductor far away from contact. From the figure, \( E_c \), \( E_v \), \( E_{\text{vac}} \), and \( E_F \) are the conduction band edge of the semiconductor, valence band edge of the semiconductor, vacuum energy, and Fermi level of the metal and semiconductor, respectively, while \( \phi_m \) and \( \phi_s \) are the work functions of the metal and semiconductor, respectively, and \( \chi_s \) is the electron affinity of the semiconductor. It is assumed that both the metal and semiconductor are free of surface states and the semiconductor is non-degenerately doped.
Figure 2-1: Metal/semiconductor contact formation using Schottky-Mott rules when (a) materials are far away from each other and (b) materials are in contact.

When the metal and semiconductor are brought in contact to equilibrium, shown in Figure 2-1b, charge must be transferred so that the Fermi energies align and flatten, causing the conduction and valence bands of the semiconductor to bend. For an n-type semiconductor, electrons are transferred to the metal near the metal/semiconductor interface as indicated by the increased difference between $E_F$ and $E_c$ in the semiconductor. This region is known as the depletion region and is positively charged because of the ionized donor atoms left behind by the transferred electrons. From Figure 2-1b, an energy barrier for electron transport can be given by

$$\phi_b = \phi_m - \chi_s,$$  \hspace{1cm} [2.1]

where $\phi_b$ is the Schottky barrier. For a non-degenerate p-type semiconductor, a similar treatment can be performed to show that the barrier for hole conduction is given by

$$\phi_b = E_g + \chi_s - \phi_m,$$  \hspace{1cm} [2.2]
where $E_g$ is the bandgap energy of the semiconductor. From equations 2.1 and 2.2, known as the Schottky-Mott limit, the barrier could be tailored for a given semiconductor by selecting a metal with the desired work function. This would allow for the formation of either an ohmic or Schottky contact. Both ohmic and rectifying cases for n-type and p-type semiconductors following Schottky-Mott rules are shown in Figure 2-2.

**Figure 2-2:** Examples of rectifying and ohmic contacts for n-type and p-type semiconductors using the Schottky-Mott theory.

From a device engineering standpoint, the Schottky-Mott theory would allow for a broad range of metal/semiconductor contact properties by just selecting the appropriate metal for the desired electrical characteristics. However, experimentally this is not always the case, and in fact $\phi_b$ sometimes has little or no dependence on $\phi_m$ [2]. One
explanation for this lack of dependence is given by the Bardeen model, which describes the metal and semiconductor as having a thin insulating layer between them, with the semiconductor/insulator interface containing a distribution of energy states. The interface states are described by a charge neutrality level, $\phi_0$, and the insulator is thin enough for electron tunneling. Using an n-type semiconductor as an example, charge neutrality requires that the negative charge on the metal surface must be balanced by the net positive charge in the semiconductor due to uncompensated donors. If interface states are present, charge neutrality must include any charge from these states. For example, if $\phi_0$ is positioned above $E_F$, then the charge on the interface states is positive, so the positive charge in the depletion region must decrease to keep the neutrality condition. This will in turn decrease the band bending because of a decreased depletion region, thus lowering $\phi_b$. The opposite would occur if $\phi_0$ is below $E_F$. The Bardeen model illustrates how $E_F$ can be positioned around the same energy at the metal/semiconductor interface regardless of the metal work function due to interface states, which has been deemed “Fermi level pinning.” The barrier height can be approximated by

$$\phi_b = E_g - \phi_0,$$

which is referred to as the Bardeen limit.

There are various other views on the exact phenomena leading to barrier height pinning. One such treatment proposes metal-induced gap states (MIGS) [3,4], which replace intrinsic electron states on the semiconductor surface. Under the MIGS theory, the tails of electron wave functions from the metal conduction band tunnel into the bandgap of the semiconductor for a few Angstroms, creating the MIGS, which pins the Fermi energy. Another possible derivation from the Schottky-Mott limit is defect
formation at the semiconductor surface without an insulating layer. Defects can include vacancies, interstitials, antisites, or other point defects. These can arise due to the deposition process from energetic metal atoms [5], diffusion of metals into the semiconductor or vice versa, or reactions that occur between the metal and semiconductor. These defects can create acceptor or donor-like states, which can lead to changes in the effective barrier height. Finally, reaction products at the interface can have a different work function than that of the metal, altering the barrier height. It is difficult to determine the barrier height for any given metal/semiconductor system a priori, so experiments must be performed to verify a barrier height.

### 2.2.2 Carrier Transport Mechanisms

From the previous subsection, it can be seen that a barrier to carrier transport can occur between a metal and a semiconductor. A good ohmic contact can be produced by reducing or eliminating the barrier, through proper selection of a metal with an appropriate work function in the Schottky-Mott limit, or if $E_F$ is pinned near or in either the conduction or valence band of an n- or p-type semiconductor, respectively. In the absence of barrier height engineering, a good ohmic contact can still be produced through barrier width modulation [6]. For an n-type semiconductor, the width of the depletion region ($W_d$) is given by [7]

$$W_d = \sqrt{\frac{2\varepsilon_s (V_0 \pm V_{app})}{qN_D}}, \quad [2.4]$$

where $\varepsilon_s$ is the permittivity of the semiconductor, $V_0$ is the built-in potential due to band bending, $V_{app}$ is the applied voltage, $q$ is the charge of an electron, and $N_D$ is the doping density. The important relationship is that $W_d$ is proportional to $1/(N_D)^{1/2}$, and therefore,
gets smaller as $N_D$ increases. A smaller barrier width can lead to enhanced electron tunneling, which improves carrier transport. Carrier transport can fall under one of three regimes: thermionic emission (TE), thermionic-field emission (TFE), or field emission (FE). Figure 1-3 illustrates how each of these mechanisms operate in an n-type semiconductor.

![Diagram of electron energy levels for thermionic emission, thermionic-field emission, and field emission.](image)

**Figure 2-3:** Three possible scenarios for carrier transport. Doping density increases from left to right as $E_F$ gets closer to $E_c$ and $W_d$ decreases.

In the case of TE, the electrons are thermally excited over of the barrier. As $N_D$ increases and $W_d$ decreases, thermally excited electrons are able to tunnel through the barrier as it thins towards the top, where the TFE regime becomes important. At even higher $N_D$, $W_d$ becomes so narrow that electrons can tunnel directly through it and the FE regime dominates. It is possible to estimate which regime is controlling carrier transport by comparing the characteristic energy for tunneling, $E_{00}$, to thermal energy $kT$, where $k$ is Boltzmann’s constant and $T$ is temperature, and $E_{00}$ is given by [6],

$$E_{00} = \frac{qh}{4\pi} \sqrt{\frac{N_D}{e\mu_{\text{tun}}}}, \quad [2.5]$$
where $h$ is Planck’s constant and $m_{\text{tun}}^*$ is a tunneling effective mass that is material. If $kT \gg E_{00}$ then TE dominates, if $kT \approx E_{00}$ then TFE dominates, and if $kT \ll E_{00}$, FE dominates.

Other mechanisms for carrier transport are possible, which can create a good ohmic contact. One such transport mechanism is via interface states and defects [8], as mentioned in Section 2.2.1. If these defects or states are electrically active and located appropriately within the bandgap, then they can act as traps. Traps can increase the likelihood of FE and TFE by decreasing the distance a carrier has to traverse across the barrier. Another possibility is that traps can become centers for generation/recombination within the depletion region, increasing transport across the barrier.

2.3 Contacts to SiC

While ohmic contacts to SiC have been studied for decades, the mechanisms behind contact formation are still under debate [9]. The previous section illustrated how defects and interface states can control the metal/semiconductor interface properties, like barrier height. These defects and states can depend on the processing steps taken to form the contact as well as intrinsically from the growth of the semiconductor itself. This can make it difficult to come to a consensus about pinning effects; however, it appears that the 4H polytype has some dependence of barrier height on metal work function, more so for n-type than p-type [10]. The pinning of barrier height on p-type 4H-SiC was suggested to be due to hole traps, which could explain the difference in the barrier height dependence on metal work function of n- and p-type SiC [11]. Evidence for native defect control, such as point defects and dislocations, of barrier heights for 4H-SiC, rather than
metal-specific states, has been shown [12]. These types of defects can diffuse at the high temperatures used for ohmic contact formation or form due to metal/semiconductor reactions. For ohmic contact formation, high temperature annealing, on the order of 1000 °C, is typically employed to induce reactions between the metal(s) and SiC. The high temperature annealing in conjunction with a heavily doped SiC layer is preferred for low contact resistance [13]. This section will describe the metallizations used and possible reasons for ohmic formation for both n-type and p-type SiC. Although numerous metal combinations and annealing conditions have been studied, this section will focus on metallizations relevant to this dissertation.

2.3.1 Contacts to n-type SiC

Nickel ohmic contacts are probably the most well studied contacts to n-SiC. An early study of a Ni/6H-SiC system displayed a low specific contact resistance, $\rho_c$, of less than $5 \times 10^{-6} \text{ } \Omega \text{ } \text{cm}^2$ after annealing at 950 °C for 2 min in vacuum [14]. Rutherford backscattering spectrometry (RBS) was used in that study to analyze the reaction products, which were interpreted to be Ni$_2$Si with C distributed within the silicide layer. A later study also investigated Ni/6H-SiC as well as Ni/Si multilayer contacts on 6H-SiC, where both systems were annealed at 950 °C for 10 min in N$_2$ [15]. Transmission electron microscopy (TEM) and energy dispersive x-ray spectroscopy (EDS) was used to characterize the reaction products and interface. For the Ni-only contacts, a shift of the metal/semiconductor interface into the SiC was found and Ni$_2$Si with C incorporation was again detected, but the TEM analysis was also able to discern Kirkendall voiding in the area of the original interface. For the annealed Ni/Si multilayer contacts, the contact
became Ni$_2$Si and a smaller amount of C and voiding was present compared to the Ni-only contacts. The voiding and C was limited to the original metal/semiconductor interface, demonstrating less reaction between the Ni/Si layers and SiC compared to the Ni-only contact.

Further characterization was performed on the Ni/4H-SiC system by TEM and x-ray diffraction (XRD) [16,17]. From XRD [16], only Ni and SiC were detected after annealing at 400 °C while Ni$_2$Si and Ni$_{31}$Si$_{12}$ were present after annealing at 600 °C. Both XRD and TEM [17] detected Ni$_2$Si and Ni$_{31}$Si$_{12}$ formation after annealing at 800 °C, with Ni$_{31}$Si$_{12}$ at the contact surface and both a C layer and Ni$_2$Si at the contact interface. After annealing at 950 °C, NiSi was found at the interface along with C, with the rest of the contact containing Ni$_2$Si with C at the surface, which is consistent with the Ni-Si-C phase diagram [18]. Although reactions occurred in these studies at temperatures as low as 600 °C, ohmic contact formation did not occur until 900 to 950 °C, illustrating that silicide formation itself does not cause the Schottky to ohmic transition. One explanation given for ohmic contact formation was that the outdiffusion of C at the higher temperatures created C vacancies, which act as donors [19], decreasing the barrier width.

Further support for C vacancies as the mechanism for ohmic contact formation was introduced by removing the Ni/SiC reaction products after the ohmic contact anneal, followed by depositing a metal where the contact had been etched [20,21]. The electrical characteristics of the contact using the second metal were similar to the original annealed Ni contact, revealing that the silicides or C were not directly responsible for the ohmic transition. In contrast, deep level transient spectroscopy did not show the presence of
defects at the expected level corresponding to C vacancies [22]. The high temperature reaction could cause other defects to occur, which control carrier transport across the interface through defect-assisted tunneling, as mentioned in the previous section.

Regardless of the formation mechanism of Ni contacts, the voiding and C inclusions can become a reliability issue under high power and high temperature operation since stresses can cause the contact to delaminate and make wire bonding for device packaging challenging [23]. The addition of carbide forming elements such as Cr [24] or Ti [25] can reduce voiding and excess C formation.

2.3.2 Contacts to p-type SiC

While Ni is the most studied contact for n-type SiC, the Ti/Al contact is highly investigated for p-type contacts. There are, however, some cases of Ni employment for p-type contacts. Annealed Ni has been used as a contact to highly doped p-type SiC [26,27], further illustrating that defects other than C vacancies may control the electrical properties of the contacts. The addition of Ni to the Ti/Al structure used for contacts to p-type SiC has been investigated for simultaneous ohmic contact formation to n- and p-type SiC as well as to lower the required annealing temperature of contacts to p-SiC [28,29]. The remainder of this subsection will focus on Ti/Al contacts as well as Pd-based contacts, which are relevant to this study.

An early report of Ti/Al contact formation, after annealing at 1000 °C, yielded poor reproducibility and pitting into the SiC layer [30]. The high Al fraction used in that study, 90 wt.% Al, was later found to be the cause of the pits [31,32] as lowering the Al fraction to 70 wt.% reduced pitting and a reduction to 60 wt.% eliminated pitting for
contacts annealed at 1000 °C in vacuum [31]. The higher pit density was associated with a lower contact resistance, with no spiking being characteristic of non-ohmic contacts [30-32]. An optimal Al fraction for both good morphology and low contact resistance was found to be around 70 wt.% Al [30,31].

Further study into the ohmic mechanism led to the hypothesis that lattice matched Ti$_3$SiC$_2$ [33] at the interface, created by the high temperature ohmic contact anneal, could reduce the barrier height, after both the pitting and doping of the SiC by Al were determined as not the primary factors for ohmic formation [34]. Support for Ti$_3$SiC$_2$ formation creating the ohmic contact was augmented by attempting to form Ti/Al ohmic contacts to n-SiC using the same conditions as was used to make ohmic contacts to similarly doped p-SiC [35]. The contacts to n-SiC were not ohmic, although the reacted interfacial microstructure was the same as in the p-type material. The Ti$_3$SiC$_2$, a reaction product from annealing the Ti/Al (50/190 nm or 70 wt.% Al) contacts at 1000 °C for 2 min, was thought to be a p-type semiconductor. Assuming the Ti$_3$SiC$_2$ is a p-type semiconductor, then it is possible that two smaller energy barriers are created, one at the p-SiC/Ti$_3$SiC$_2$ interface and one at the Ti$_3$SiC$_2$/metal interface. The reduction in barrier height from the Ti$_3$SiC$_2$ formation was estimated to be about 1 eV. In a separate study, a 70 wt.% Al contact was annealed at 1000 °C, creating the Ti$_3$SiC$_2$ layer at the metal/semiconductor interface, and interfacial defect states were found via depth-resolved cathodoluminescence [36]. These defects could act as trap centers for increased tunneling and could play a strong role in current transport since the maximum barrier height in that work was measured to be about 1.3 eV, which is large for an ohmic contact. It is thought that the role of Al, which melts at 660 °C, in the Ti/Al contacts annealed to
1000 °C is to stabilize the reaction within the SiC+ Ti$_3$SiC$_2$+liquid region, which occurs in the SiC-Al-Ti phase diagram at 1000 °C [37], creating Ti$_3$SiC$_2$ as a reaction product [36].

Another contact scheme of interest for this dissertation is Pd-based contacts. The high work function of Pd, 5.12 eV, could be beneficial for the formation of an ohmic contact to the wide bandgap SiC, assuming a Schottky-Mott relationship based on equation 2.2. As Pd resides in the same column as Ni in the periodic table, similar reactions with SiC could be expected. Both XRD and RBS were used to study the reaction products between Pd and SiC [38]. Reaction between Pd and SiC started at 500 °C with the formation of Pd$_3$Si. At 700 °C, both Pd$_3$Si and Pd$_2$Si were detected, while at 800 °C and above, only Pd$_2$Si was found. After annealing Pd and 6H-SiC for 85 h at 750 °C, Pd$_2$Si, Pd$_3$Si, and Pd$_2$Si+C were observed, with the C inclusions being consistent with the Ni/SiC reaction discussed in Section 2.3.1 [39].

Annealed Pd contacts were found to be ohmic to p-SiC after annealing at 600 °C to 700 °C for many minutes [40,41]. The loss of rectifying properties of a Pd/SiC Schottky diode was also observed after annealing at 600 °C [42]. The lowest contact resistance was obtained after annealing at 700 °C. The reactions at those temperatures were studied by x-ray photoelectron spectroscopy (XPS) depth profiling, Auger electron spectroscopy (AES) depth profiling, RBS, and XRD. The Pd$_3$Si phase was found after annealing at 600 °C, while Pd$_3$Si, C, and Pd$_2$Si (found at the metal/SiC interface) were observed after annealing at 700 °C, all of which is consistent with Reference 38. The Pd contact annealed at 700 °C was rough compared to the as-deposited case, with a
root-mean-squared (RMS) roughness of 110 nm after annealing compared to 8 nm as-deposited, measured by atomic force microscopy (AFM) [40].

Composite contacts consisting of Pd/Ti/Pd/Au and Pd/Au were also investigated [43,44]. An optimal annealing temperature for the Pd/Au (100/100 nm) and Pd/Ti/Pd/Au (10/20/70/100 nm) contacts was 850 °C and 900 °C, respectively, both higher than the optimal annealing temperature of Pd-only contacts at 700 °C. Although annealed at a higher temperature, the additional elements reduced the agglomeration and surface roughening that occurred with the Pd-only contacts. The Pd/Ti/Pd/Au contacts exhibited the lowest contact resistance and best thermal stability, measured after 100 h at 700 °C in N₂. The annealed Pd/Ti/Pd/Au contacts had an RMS roughness of 75 nm, compared to the 110 nm RMS roughness for annealed Pd-only contacts. The reacted Pd/Ti/Pd/Au contact consisted of Pd₂Si near the interface and TiC, Pd₃Si, and Au throughout the rest of the contact. There was no apparent excess C, like in the annealed Pd-only contact, as the Ti layer was able to consume the C created from the Pd/SiC reaction and form TiC. This is a similar strategy as the one mentioned in Section 2.3.1, where carbide-forming elements were added to Ni contacts to reduce voiding and C inclusions.

2.4 High Temperature Degradation of Contacts to SiC

The potential high temperature applications of SiC were assessed in Section 1.2. In order for SiC-based devices to be used at high temperatures, the contact resistance must not degrade over time. Contact stability testing varies depending on the study, with the temperature and annealing environment differing. A typical ohmic contact study will anneal the contact at a high temperature for some amount of time in an inert atmosphere.
Annealing in inert atmosphere will determine if any further reaction will occur that will adversely affect the contact resistance. Some examples of stable contacts include the Pd/Ti/Pd/Au contact to p-type SiC [44], described in Section 2.3.2, which was stable after 100 h at 700 °C in N₂ and a Ni/WSi/Ti/Pt contact to n-type SiC annealed at 1000 °C, which displayed good thermal stability after 100 h at 650 °C in N₂ [45]. Both these contacts were said to show good stability due to complete reaction of the contact components. Sometimes contacts are tested at very high temperature for a shorter period of time. A W-Ni metallization annealed at 1000 °C to make contacts to both n- and p-type SiC were tested at 900 °C for 1 h in Ar, showing good stability [46].

Although inert atmosphere annealing will identify additional reactions that might diminish a contact’s stability, contact metallizations may be exposed to oxidizing environments under high temperature operation, such as air. The addition of oxygen to the annealing atmosphere can oxidize the metallization, or cause elements to diffuse to the surface to oxidize. This type of degradation would not be observed using an inert aging environment. An early study of high temperature stability in air was performed using Ti/TiN/Pt (50/50/100 nm) contacts to n-type SiC annealed at 1000 °C in Ar [47]. The contacts exhibited good stability after 65 h at 650 °C in air. While Pt had diffused into the TiN layer, O diffusion was suppressed allowing the contact to remain stable over time.

The TiN layer was replaced by a TaSi₂ layer and good stability was displayed by Ti/TaSi₂/Pt contacts to n-type SiC, first annealed for 30 min at 600 °C in N₂, after 1000 h at 600 °C in air [48]. In that study, it was determined that the thickness of the Pt layer compared to the other layers was vital to the long-term stability of the contact. For a
Ti/TaSi$_2$/Pt (100/200/300 nm) contact, during annealing in air, excess Pt diffused towards the metal/SiC interface, reducing Ti$_5$Si$_3$ that had formed during the initial anneal in N$_2$. By reducing Ti$_5$Si$_3$ to form PtSi$_x$, the free Ti was able to diffuse towards the surface of the contact to oxidize. The Ti agglomerated below the contact surface creating blistering and cracking allowing a fast diffusion path for O to the metal/SiC interface. By increasing the TaSi$_2$ thickness to 400 nm and holding the Pt thickness at 300 nm (increasing the ratio of TaSi$_2$ to Pt), the Pt and subsequent Ti diffusion was not observed, and thus no blistering occurred. Eventually a Ti/TaSi$_2$/Pt (100/400/200 nm) contact was tested that exhibited good thermal stability after 1000 h in air at 600 °C. A thin PtSi$_x$ layer at the surface, which possesses a very slow rate of oxidation, was thought to control oxidation of the contact structure and improve stability. These contacts were eventually employed in devices that were operable after 10,000 h at 500 °C in air [49].

A TaSi$_2$/Pt bilayer was also used in Ni contacts to n-type SiC for high temperature gas sensor application [50,51]. In both studies, a 100 nm Ni layer was first deposited and annealed at 950 °C in Ar. Then a 50 nm TaSi$_2$ layer and a 150 nm Pt capping layer were deposited. These contacts failed after 36 h at 600 °C in air, but were still ohmic after 1000 h at 300 °C in air. Oxidation of the TaSi$_2$ was determined to be the cause of failure. By using a thicker TaSi$_2$/Pt bilayer (400/200 nm), similar to the Ti/TaSi$_2$/Pt described earlier [48], the contacts remained ohmic after 312 h at 600 °C in air. While Ni and Pt had diffused within the contact, a thin oxide layer at the surface of the contact was thought to have diminished the oxidation of the rest of the contact, as postulated for the Ti/TaSi$_2$/Pt contact [48].
Contact reliability is not only measured by the stability of electrical properties, but also the mechanical properties, such as adhesion, since devices may be packaged using wire bonding and contacts could delaminate, causing failure. The use of a Ta-Ru-N diffusion barrier for Ni and Al/Ni contacts to p-type SiC aged at 350 °C in air was examined for electrical and mechanical stability [27,52]. In one study, the contact metallization consisted of Ni or Al/Ni ohmic contacts, a 200 nm Ta-Ru-N diffusion barrier, and a Pt/Sn/Au (100/25/200 nm) cap [27]. The composition of the Ta-Ru-N barrier layer was varied from Ta-rich to Ru-rich. Contacts utilizing the Ru-rich diffusion barrier displayed good stability up to 2000 h at 350 °C in air. It was shown by AES depth profiling that O reacted with the Ru-rich barriers, even though N was lost in the process, which protected the ohmic contact below. Since N was lost during ageing, Ta-Ru barriers were tested on the Ni and Al/Ni contacts, this time with a 5 nm Ta or Ru adhesion layer between the barrier and a 700 nm Au capping layer on top [52]. While the Ru-rich Ta-Ru-N barriers again provided good stability after 2000 h of ageing at 350 °C in air, the contacts peeled after mechanical testing. The Ru-rich Ta-Ru barriers not only provided electrically stable contacts, but also mechanically stable contacts after 2000 h of ageing.

2.5 Current Induced Contact Degradation

The previous section described cases of thermal degradation studies of ohmic contacts to SiC, illustrating that the ohmic contact metallization must be carefully controlled and that layer thickness and composition can have enormous effects on the contact stability. Continued reactions or oxidation of the contacts can cause failure.
Under high current densities, Joule, or resistive, heating can cause similar contact degradation as thermal ageing. Additionally, high current densities can produce failure from electromigration, or the physical transport of atoms due to momentum transfer from electrons under high current density [53]. Atomic movement could cause voiding or reactions to occur, degrading a contact. The ability of contacts to be reliable under high current densities is important for power applications. This section will first describe electromigration and then discuss current induced failure of contacts to Si, which became significant as devices continued to scale. An important aspect of contact failure from high current densities is that electrons are flowing into the semiconductor through the cathode and out of the semiconductor through the anode. This difference in electron flow through the metal/semiconductor interface can generate polarity effects, meaning one contact can preferentially degrade compared to the other. Polarity effects in contacts to Si will be the main focus of Section 2.5.2.

2.5.1 Electromigration

Under an applied electric field, thermally activated atoms, vibrating in the lattice, will be acted upon by two forces [54]. The electric field will apply a force on the positive ion in one direction. In the opposite direction, electrons colliding, or scattering, with the metal ions will impart momentum, with the direction of force in the direction of the electron flow. The force on a metal ion from the applied field is typically small, due to electron shielding, so the force from the momentum exchange between the electrons and ions, sometimes referred to as the electron wind, dominates. The total atomic flux, $J_{\text{flux}}$, due to electromigration and chemical potential gradients can be expressed as [55],
\[ J_{\text{flux}} = -D \left( \frac{\partial C}{\partial x} - \frac{Z^* eE}{kT} C \right), \]  

where \( D \) is the diffusivity, \( C \) is the atomic concentration, \( k \) is Boltzmann’s constant, \( T \) is temperature, \( Z^* \) is the effective charge number, \( e \) the charge of an electron, and \( E \) is the electric field.

Typically electromigration is associated with interconnect failure, Al or Cu lines, in integrated circuits. Failure is usually characterized by voids or extrusions in the line, caused by a flux divergence, when the incoming flux of atoms or vacancies is not equal to the outgoing flux [56]. If the vacancy or atomic flux were constant, failure would not occur. Interfaces and triple points in grain boundaries are common areas where divergence can occur. Reliability of interconnects is often predicted after accelerated testing and is described in terms of median time to failure, MTTF, which is the time at which 50% of the samples have failed. Samples are typically tested at various temperatures at the same current density, producing different MTTF values. The data is fit using Black’s equation, [54]

\[ MTTF = \frac{A e^{E_A/kT}}{J^2}, \]

where \( A \) is a constant, \( J \) is the current density, and \( E_A \) is the activation energy for the failure mechanism. The \( J^2 \) term is more universally written as \( J^n \), where \( n \) is another constant [57], and can vary depending on the failure mechanism.

Stress [58] and temperature gradients [59] can also contribute to electromigration induced failure. A build up vacancies can cause a tensile stress in the film, while an accumulation of atoms can create compressive stress. These stresses can exacerbate or even decelerate failure, by creating a backflow of atoms [60]. Thermal gradients can
occur at areas where film adhesion is poor or between materials with vastly different thermal conductivities, such as metal/insulator and metal/semiconductor interfaces. In higher temperature areas, the movement of atoms is accelerated, while at lower temperature the movement is slowed. The thermal gradients can also create a flux divergence, creating voids or extrusions.

Although the bulk of the literature employs continuous direct-current (DC) stressing for electromigration testing, many applications use pulsed DC currents. Figure 2-4 shows a pulsed DC current waveform. A current is pulsed during the on-time, $t_{on}$, with no current during the off-time, $t_{off}$, where $t_{on} + t_{off}$ is the period, $T$, and $1/T$ is the frequency. The $t_{on}/T$ ratio is termed the duty cycle and is given in a percentage, which describes the amount of on-time per period. Pulsed DC can affect electromigration failure in a few ways [61]. The duty cycle and frequency can influence the amount of damage and possible repair of damage depending on the length of $t_{on}$. The frequency and duty cycle could also affect the absolute and change in temperature of the structure, depending on the ability to dissipate Joule heating. The general dependence of MTTF on duty cycle and frequency has been difficult to determine because of the diversity in testing structures and conditions. However, lifetime enhancement is typically observed for decreased duty cycles [62], while frequency may have less of an effect.
Figure 2-4: Pulsed DC current vs. time.

2.5.2 Degradation of Contacts to Silicon

The schematic in Figure 2-5 shows a possible example of electron flow through a simplified device. In this case, electrons flow through a metallic interconnect and the cathode, into an n-type layer isolated on a p-type substrate. The electrons flow out of the n-type layer through the anode into another interconnect. As shown, the electrons travel through numerous interfaces, such as the contact/interconnect and semiconductor/contact interfaces, and as the previous sections mentioned, interfaces are possible areas where flux divergence of atoms or vacancies can become an issue. Additionally, the direction of the flow of electrons, whether it be from semiconductor into metal or vice versa, can lead to preferential or accelerated degradation of either the anode or cathode. This is called a polarity effect, a phenomenon that is prevalent in contact failure under high current densities. Also, under the lateral current flow, current crowding at the corners of interconnects or the leading edges of contacts, the right edge of the cathode or left edge of the anode as shown in the figure, is another concern. Current crowding increases the
local current density, which can in turn create a thermal gradient from localized Joule heating or increase the effects of electromigration.

![Diagram of electron flow in a device](image)

**Figure 2-5:** Example of electron flow in a device.

One example illustrating a polarity effect and current crowding can be found for Al-1%Si contacts to Si [63]. The experimental setup is similar to that shown in Figure 2-5, with Al-1%Si contacts to an n⁺-Si channel on a p-type substrate. The contacts were 3x3 µm² and were stressed at above $10^5$ A/cm² at a temperature of 250 °C or below. At higher temperatures and stressing currents, Si from leading edge of the anode migrated into the Al-1%Si films while Al diffused in the opposite direction, creating pits and causing an increase in leakage current across the n⁺/p junction. Numerical simulations showed that the leading 0.5 µm edge of the contact carried about 90% of the contact, making the current density in that area closer to $6\times10^5$ A/cm² instead of around $10^5$ A/cm². At the cathode, Si from the Al-1%Si film had migrated to the Al-1%Si/n⁺-Si interface. A small concentration of Si, in this case 1%, is typically added to Al contacts in order to reduce “pitting” or “spiking,” which typically occurs during thermal annealing when Si diffuses into Al, due to the small solid solubility of Si in Al, and the subsequent
filling of Si voids by Al [64]. No pitting occurred in this study under thermal annealing alone, demonstrating that additional failure mechanisms can occur from current stressing. Electromigration of Si in the Al-1%Si film at the contact interface allowed Si from the n⁺-Si to migrate into the film. At lower current densities and temperatures, Al migration away from the contact interface at the anode caused an increase in resistance. The Al at the anode is under two opposing forces, electromigration away from the interface, a lower activation energy process, and diffusion into pits created by the electromigration of Si into the Al-1%Si film, a higher activation energy process. In this case the stressing conditions greatly affect the failure mode of this contact structure.

Leakage failure in the Al-1%Si/n⁺-Si contact example in the previous paragraph was alleviated through the use of a W barrier, modifying the failure mechanism to Al electromigration away from the W/Al-1%Si interface. The use of a barrier is common in contact structures in order to reduce mixing between the different layers or the semiconductor and typically consists of noble or near-noble metals, refractory metals, intermetallic alloys, or transition metal silicides [65]. The use of a barrier is again seen in the case of Al/CoSi₂ contacts to n⁺-Si [66]. The contact structure is again similar to the schematic in Figure 2-5 with Al-0.5%Cu interconnects and CoSi₂ contacts to an n⁻-Si channel on a p-type substrate. The contacts were stressed above 8x10⁵ A/cm² at temperature between 150 °C and 220 °C. Figure 2-6a shows SEM micrographs of stressed Al/CoSi₂/n⁺-Si contacts after selectively etching away the Al interconnect. While the cathode appears unchanged compared to an unstressed contact, the anode shows Si precipitates at the contact surface. The leakage current increases in this case due to Al pitting as described earlier. The introduction of a TiN diffusion barrier slowed
this failure mechanism and increased the MTTF of the structure by an order of magnitude.

Figure 2-6: Examples of polarity effects in the failure of contacts to Si. Metallizations include (a) Al/CoSi2/n⁺-Si [66] and (b) Ni/n⁺-Si and (c) Ni/p⁺-Si [67]. Reprinted with permission from [66], Copyright 1984, American Institute of Physics. Reprinted with permission from [67], Copyright 1997, American Institute of Physics.

The study of Ni and Ni/Ni₂Si contacts to both n- and p-type Si exhibited another interesting polarity effect, where not only was there preferential degradation at the cathode or anode, but also the doping type altered which contact degraded first [67,68]. Contacts were stressed at 275 °C and 5x10⁵ A/cm². For Ni on n⁺-Si, shown in Figure
failure occurred at the anode where electromigration moved Ni away from the contact interface leaving voids. The increase in current density after voiding caused an increase in Joule heating, which created a reaction between Ni and Si to form nickel silicides. Since nickel silicides are more resistive than pure Ni, increased Joule heating occurred, accelerating the resistive change. When $p^+\text{-Si}$ was the contacted epilayer, as shown in Figure 2-6c, the Ni contacts instead failed at the cathode. It is thought that this failure is due to electron-hole recombination causing a large amount of Joule heating. As more resistive nickel silicides form due to the increase in temperature, the amount of Joule heating increases, creating a positive feedback loop. When $\text{Ni}_2\text{Si}$ was added between the Ni and $p^+\text{-Si}$, the cathode failed faster than the pure Ni contact, and it was thought that the increased Joule heating effect of the silicide was the cause for the decreased time to failure. For Ni/$\text{Ni}_2\text{Si}$ contacts to $n^+\text{-Si}$, the failure also occurred at the cathode and was explained by the electromigration of Ni into the Si from the $\text{Ni}_2\text{Si}$, which was replaced by Ni from the bond pad. The Ni from the $\text{Ni}_2\text{Si}$ reacted with the Si, increasing the contact resistance and causing thermal runaway. The preferential failure of the Ni/$\text{Ni}_2\text{Si}/n^+\text{-Si}$ contacts at the cathode and the Ni/$n^+\text{-Si}$ contacts at the anode illustrates the effect slightly different contact metallizations have on the failure mechanism.

2.6 Summary of Literature Review

Chapter 2 of this dissertation has described ohmic contact theory, the formation of ohmic contacts to SiC, and the degradation of contacts under thermal and current stressing. Good ohmic contacts can be formed by controlling the barrier height at the
metal/semiconductor interface, promoting tunneling via a highly doped contacting layer, or through other defects that can increase tunneling [1]. Ohmic contacts to SiC, both n- and p-type, are typically produced after high temperature annealing. The reactions between the metal(s) and SiC may create defects that can increase doping near the contact interface [20] or could increase tunneling through the barrier [36]. In Section 2.4, the thermal stability of contacts to SiC in air was shown to be dependent on the thickness and composition of the layers [27,47,48,50-52]. Finally, polarity effects were illustrated in the failure of contacts to Si under high current density, causing preferential failure of the anode or cathode [63,64,66-68]. The current stressing produced failure mechanisms not observed under thermal stressing alone.

2.7 References


Chapter 3

Experimental Methodology

3.1 Introduction

This chapter will detail the fabrication and characterization techniques of the samples used to optimize as well as stress ohmic contacts under high current densities. Section 3.2 will introduce the material used and the cleaning procedures. The next section will discuss the structures and techniques employed for measuring contact resistance. The fabrication of the structure used for stressing the contacts will be discussed in Section 3.4 followed by details of electrical stressing and materials characterization in Section 3.5 and 3.6, respectively. Sample fabrication was performed mostly in the PSU Nanofabrication facility and labs belonging to Dr. Mohney’s group. Electrical characterization was done mostly in Dr. Flemish’s lab. As photolithography equipment and procedures have changed over the time, the most recent processes are recorded in this dissertation. All photolithography performed in this dissertation was contact photolithography. The fabrication procedure for the contact stressing structures in Section 3.4 may be altered for different metallizations introduced in subsequent chapters, and those variations will be discussed within the appropriate chapter.

3.2 Material

A SiC PiN diode structure was the material provided for this study, and the layers are shown in Figure 3-1. Different epilayers were grown on a 3” research grade n-type 4H substrate cut 8° off (0001) and doped to $1 \times 10^{18}$ cm$^{-3}$ to produce the diode arrangement. On top of the substrate, a 10 µm n drift layer was grown with a donor
density of $2 \times 10^{14} \text{ cm}^{-3}$, followed by a 2.5 µm p$^+$ injection layer doped at $8 \times 10^{18} \text{ cm}^{-3}$ and a 0.5 µm p$^{++}$ capping layer doped to $1 \times 10^{20} \text{ cm}^{-3}$. Nitrogen and aluminum were used as the donors and acceptors, respectively. One advantage PiN diodes have over a Schottky diode is a lower forward voltage ($V_F$) at blocking voltages over 2 kV; however, stacking fault propagation in the n$^-$ drift layer under current stressing can cause an increase in $V_F$ over time [1,2]. The drift layer in this study was kept thin, compared to the 100 µm drift layer for power devices of interest, in order to mitigate this effect.

**Figure 3-1:** Layers of SiC PiN diode structure (not to scale).

All samples were cleaned using a modified RCA clean [3]. The clean consisted of the following chemical treatments:

1. Deionized (DI) H$_2$O:H$_2$O$_2$:NH$_4$OH (5:1:1) at 80 °C for 10 min
2. 10:1 buffered oxide etch (BOE) for 30 s
3. DI H$_2$O:H$_2$O$_2$:HCl (5:1:1) at 80 °C for 10 min
4. DI H$_2$O rinse after each step and blow dry with N$_2$ at the end
Samples were cleaned with solvents at various points throughout processing and will be termed DEGREASING:

1. Acetone for 5 min (ultrasonic agitation optional)
2. Isopropanol (IPA) for 5 min
3. DI H₂O for 5 min and dry with N₂

The ultrasonic agitation during the acetone step is used for reducing the number of particulates on the surface of the sample. Ultrasonic agitation is not recommended for samples that have photoresist or metals since delamination of the films can occur. After annealing the metal contacts, ultrasonic agitation could be used if a reaction occurs between the metal and semiconductor that increases the mechanical stability of the contact.

3.3 Contact Resistance Structures

Before stressing the ohmic contacts under high current densities, the contacts first were optimized in order provide a low initial contact resistance. In order to compare contacts, a normalized value termed specific contact resistance, \( \rho_c \), is used. This value takes into account the active area of the contact and has units of ohms*area\(^2\), so for a larger contact area, the total resistance from the metal/semiconductor interface becomes smaller. The primary test structure used to measure \( \rho_c \) for the optimization process is the circular transfer length method (CTLM) [4] test structure. The transfer length method (TLM) [5] test structure is another structure that can be used, but requires an extra processing step compared to the CTLM structure. The TLM is used in this study to compare extracted values of \( \rho_c \) from the different test structures on the same processed
sample. In order to measure $\rho_c$ before and after high current density stressing to observe electrical changes of the contact, a test structure employing the four circular contacts method (FCCM) [6] is used. The FCCM allows for small contacts, which can provide high current densities under stressing. The three methods to measure contact resistance will be described in this section.

### 3.3.1 Circular Transfer Length Method

The CTLM test structure [4] typically requires only one processing step to fabricate, compared to two steps required by the TLM. The CTLM test structure is shown in Figure 3-2 and consists of circular metal pads and a metal field separated with a gap of semiconductor. The CTLM structure consists of gaps of varying sizes. A current is applied between the circular pad and the metal field, both assumed to be equipotential surfaces. Resistance from the metal, the semiconductor, and the contacts accounts for the total voltage drop for the applied current. Assuming the metal adds negligible resistance compared to the semiconductor and contact, the voltage drop can be shown to be

$$
\Delta V = \frac{IR_{\text{SH}}}{2\pi} \left[ \ln\left( \frac{r_i}{r_0} \right) + \frac{L_T}{r_0} \frac{I_0(r_0/L_T)}{I_1(r_0/L_T)} + \frac{L_T}{r_i} \frac{K_0(r_i/L_T)}{K_1(r_i/L_T)} \right],
$$

where $I$ is the applied current, $R_{\text{SH}}$ is the sheet resistance of the semiconductor, $L_T$ is the transfer length, and $r_1$ and $r_0$ are defined in Figure 3-2, $r_0$ being constant. The functions $I_0$, $I_1$, $K_0$, and $K_1$ are modified Bessel functions. Under lateral current flow, $L_T$ describes the measure of current crowding at the leading edge of a contact, such as the outer edge of the circular metal pad in Figure 3-2, and is related to $R_{\text{SH}}$ and $\rho_c$ through

$$
L_T = \sqrt{\frac{\rho_c}{R_{\text{SH}}}}.
$$
The values of $R_{SH}$ and $L_T$ can be extracted from equation 3.1 by plotting the total resistance, $\Delta V/I$, for each gap, $r_1-r_0$, in the CTLM set and using $R_{SH}$ and $L_T$ as the fitting variables. The value of $\rho_c$ can then be found from equation 3.2.

**Figure 3-2:** Schematic of CTLM test structure.

Each CTLM test structure used for ohmic contact optimization had ten gaps with a size of 20, 18, 16, 14, 12, 10, 8, 6, 4, and 3 $\mu$m and an inner pad radius, $r_0$, of 40 $\mu$m. The CTLM structure included on the samples containing the current stressing structures had gaps of 20, 16, 12, 8, and 4 $\mu$m and $r_0$ was 50 $\mu$m. All gaps were measured in a scanning electron microscope (SEM). Measuring the gaps is a vital procedure since photolithography may not produce the same size gaps as the mask defines. Small deviations from the ideal gap size can cause large errors in $\rho_c$. An additional error in $\rho_c$ can stem from significant series resistance from the metal [7,8]. This effect can be observed by moving the voltage-sensing probe on the metal field. If the change in the total resistance measured across a gap is significant then the metal resistance could be adding error to the extracted $\rho_c$. In this study, some CTLM structures were repatterned.
and a 100 nm Au film was deposited directly on the existing annealed contact to mitigate the effect of metal resistance. The additional metal deposition will be noted when utilized.

The CTLM tests were performed on a Keithley 4200 SCS and Karl Suss probe station with optical microscope. Two probes were placed inside the circular metal pad, and two were placed on the metal field, typically a few µm’s from the other side of the gap being measured. One probe inside the circular pad was the current source (using SMU1), while the other probe was the voltage-sensing probe. Ground (using GND) source and sense probes were used on the metal field. Sense probes are high impedance probes that can accurately measure the voltage on the metal, reducing the effects of additional resistance at the probe/metal interface and in the cables. Current was sourced from -10 mA to 10 mA in 0.1 mA steps for a total of 201 data points per gap. An insulating piece of alumina was placed between the sample and the metallic probe station stage in order to avoid any grounding effects through the sample that might affect the lateral measurement.

For linear current-voltage (I-V) plots, Microsoft Excel was used to fit a line to the middle 101 points, and the total resistance for that gap was found through the inverse slope. The resistance values and corresponding gaps, measured in the SEM, were entered into an Excel spreadsheet. Excel can calculate Bessel functions, and the error between the value calculated by Excel and the value calculated by a series expansion of \( I_0(1) \) is less than \( 3 \times 10^{-6} \)% after 5 terms of the series expansion [9]. The Excel solver function was used to minimize the sum of the errors, first squared, by varying \( R_{SH} \) and \( L_T \). The solver function utilizes the Newton method with central derivatives, and therefore an
initial guess is required. Both $R_{SH}$ and $L_T$ are constrained to be positive numbers. The correlation coefficient $R^2$ is used to measure how well the function is fit to the data. A value of $R^2$ greater than 0.999 is typical. Typically 5 CTLM sets were measured with the standard deviation reported as the error.

One photolithography step is used to fabricate the CTLM structures, in which photoresist is used to mask the areas of the CTLM structure where the gaps in the metal are located. After the photolithography step, the metal is deposited and then the resist is removed, a process called lift-off, leaving the structure shown in Figure 3-2. All photolithography in this study was performed at the PSU Nanofab facility. Some CTLM structures were formed simultaneously with the contact stressing structures described in Section 3.4. Fabrication of samples with only CTLM structures is described here. The following photolithography procedure is used for metal lift-off on a bare SiC substrate:

1. Degrease with ultrasonic agitation
2. Dehydration bake at 175 °C (blow off with $N_2$ before placing on hot plate)
3. Coat with hexamethyldisilazane (HMDS), a photoresist adhesion promoter, and spin dry at 4000 rpm for 15 s
4. Bake at 112 °C for 15 s on hot plate
5. Coat with MicroChem LOR5A and spin at 7000 rpm for 45 s
6. Bake at 175 °C for 10 min on hot plate
7. Coat with Microposit SPR 3012 and spin at 7000 rpm for 45 s
8. Bake at 95 °C for 60 s on hot plate
9. Align and expose with a Karl Suss MA/BA6 contact aligner for an exposure time of 7.0 s

10. Develop with MicroChem CD-26 developer (tetramethylammoniumhydroxide or TMAH) for 60 s followed by DI H₂O rinse and blow dry with N₂

11. Inspect samples in optical microscope

12. Descum sample with O₂ plasma to remove residual photoresist in exposed areas

The O₂ descum is done in a Metroline M4L plasma etcher. The parameters used were an O₂ flow of 200 sccm, a pressure of 1000 mTorr, an RF power of 200 W, and a time of 2 min. The procedure is termed as O₂ DESCUM.

All metal deposition for ohmic contacts was performed in a Denton DC magnetron sputtering system. A turbomolecular pump, assisted by a liquid N₂ cold trap, was used to pump the chamber to a base pressure below 10⁻⁷ Torr, as read by a Penning gauge. The chamber was allowed to pump down overnight or for more than 5 h during the day, until liquid N₂ was added to the cold trap, typically with the chamber at less than 5x10⁻⁶ Torr. Semiconductor grade Ar (99.9995% pure) was used as the process gas. The operating pressure was 5 mTorr as read by a capacitance manometer, with the flow rate of the Ar controlled by a needle valve. The sample stage was rotated to provide good uniformity, and a calibrated DTM-100 quartz crystal monitor measured the film thickness. Prior to loading into the chamber, the samples were soaked in 10:1 buffered oxide etch (BOE), a solution containing water and a 10:1 volume ratio of 40% NH₄F and
49% HF in water. The BOE treatment time was 2 min, followed by a DI H₂O rinse and blow dry with N₂.

Metal lift-off was done by following procedure termed LIFT-OFF:

1. Soak samples in Remover PG (N-methyl-2-pyrrolidinone) heated to 60 °C in a beaker on a hot plate for at least 30 min (beaker should be loosely covered so Remover PG does not evaporate entirely)
2. Place heated Remover PG beaker into ultrasonic bath for 2 s (optional and could cause film delamination)
3. Rinse thoroughly using IPA rinse bottle into separate beaker
4. Rinse thoroughly using DI H₂O rinse bottle into separate beaker and dry with N₂
5. Inspect in optical microscope for good lift-off of features
6. Repeat if necessary with shorter soak time for step 1

After lift-off, the CTLM structure can be measured as described above.

As-deposited contacts to SiC are typically not ohmic so I-V curves are used for comparison with annealed samples or between as-deposited samples of different metallizations. As mentioned in Section 2.3, high temperature annealing is usually required for forming ohmic contacts to SiC. Here, the contact annealing was performed in an AG Associates Heatpulse 610 rapid thermal annealing (RTA) furnace. The RTA furnace uses tungsten-halogen lamps to quickly heat the sample within a quartz chamber. An inert gas flows through the chamber during annealing to reduce oxidation of the metals. Either Ar or N₂, both ultra-high purity (UHP) grade (99.999%), was flowed at 3 slm during the annealing, with a 10 min purge at 3 slm after loading the sample and prior
to annealing. The UHP grade gas was first flowed through a gettering furnace consisting of a quartz tube with titanium sponge that when heated, at 600 °C for Ar and 500 °C for N₂, will react with any residual O₂ in the gas, purifying it even further. The ramp rate for annealing was usually 75 °C/s. Samples were placed on a Si carrier wafer that sits in the quartz tube and either an attached thermocouple or a calibrated pyrometer inside the RTA provided temperature control. The sample was allowed to cool inside the tube for approximately 8 min as chilled H₂O cooled the quartz tube.

### 3.3.2 Transfer Length Method

The TLM [5] is used in this study to compare extracted ρᵥ values with the CTLM and FCCM. The TLM requires a contact formation and isolation step to form a structure similar to that shown in Figure 3-3. The TLM structure consists of a rectangular section of isolated semiconductor, created by etching a mesa in this study. Rectangular metal pads are deposited, with gaps of varying sizes in between, similar to the CTLM structure. The total resistance, \( R_T \), measured between adjacent pads can be approximated by

\[
R_{T,i} = \frac{R_{SH}}{Z} (d_i + 2L_T), \tag{3.3}
\]

where \( d_i \) is the gap size, \( Z \) is the metal pad width, and it is assumed that the pad length is greater than 1.5\( L_T \), which is typically is not an issue. A linear fit is performed of a plot of \( R_T \) vs. \( d_i \), and \( R_{SH} \) can be found from the slope of the line multiplied by \( Z \), and -2\( L_T \) is the x-intercept. The value of \( \rho_c \) can then be found from equation 3.2, assuming \( R_{SH} \) under the contact is the same as in between the contacts.
The dimensions of the TLM structure used in this study were 100 µm for Z and 3, 6, 9, 12, and 15 µm for the gaps, all of which were measured in an SEM. Similar to the CTLM described in Section 3.3.1, a Keithley 4200 and probe station were used for the I-V measurements. Current was sourced between adjacent pads from -10 mA to 10 mA in 0.1 mA steps for 201 data points. A source and sense probe was used on each pad (using SMU1 and GND). Again, an alumina piece was used to insulate the sample from the probe station stage. The I-V curve, if linear, was fit to the middle 101 points using Excel, $R_T$ being the inverse slope. The $R_T$ value and corresponding measured gap were input into Excel, and Excel’s linear regression command was used to find the slope and x-intercept along with an $R^2$ value. The values of $R_{SH}$, $L_T$, and $\rho_c$ were determined from the derivation above. The TLM structures were fabricated simultaneously along with the current stressing structures, so the mesa isolation and ohmic contact formation steps would be the same as those described for the contact stressing structure in Section 3.4.

**Figure 3-3:** Schematic of TLM structure.
3.3.3 Four Circular Contacts Method

The FCCM [6] is based on the four-point probe method used for determining the sheet resistance of a thin film [10]. A schematic of the structure is shown in Figure 3-4. The structure consists of an isolated semiconductor, mesa isolated via etching in this study, with four evenly spaced circular contacts. The contacts are spaced a distance, s1, and are centered with respect to side length D. The two outer contacts, J and K, have the same distance between the center of the contact and the outer edge of the semiconductor layer with respect to side length C. First, \( R_{SH} \) of the semiconductor is calculated through [10]

\[
V_{12} = \frac{I_{JK} \cdot R_{SH}}{\pi} \left( \frac{\pi}{d} + \ln \left[ 1 - \exp \left( -\frac{4\pi}{d} \right) \right] - \ln \left[ 1 - \exp \left( -\frac{2\pi}{d} \right) \right] + \sum_{m=1}^{\infty} a_{m} \right),
\]

where

\[
a_{m} = \frac{\exp \left[ -\frac{2\pi(\alpha - 2)m}{d} \right] \left[ 1 - \exp \left( -\frac{6\pi m}{d} \right) \right] \left[ 1 - \exp \left( -\frac{2\pi m}{d} \right) \right]}{m \left[ 1 + \exp \left( -\frac{2\pi\alpha m}{d} \right) \right]},
\]

and d is D/s1 and \( \alpha \) is C/s1. Contacts 1 and 2 should be small to reduce any effects of current shunting through the metal contact. A current is applied through contacts J and K, \( I_{JK} \), and the voltage drop is measured across contacts 1 and 2, \( V_{12} \), allowing \( R_{SH} \) to be extracted from equation 3.4.
Figure 3-4: FCCM structure with geometry labeled for equation 3.4.

Once $R_{SH}$ is determined, the voltage drop between any two points along a line centered with respect to side $D$, as shown in Figure 3-5, can be calculated. The radius of the outer contacts $J$ and $K$ may have a different radius than contacts 1 and 2. Points $A$ and $B$ in Figure 3-5 are at the edge of the metal/semiconductor interface along the center line and are separated by a distance $s_2$. The voltage drop across $A$ and $B$, $V_{AB}$, is given by

$$V_{AB} = \frac{I_{JR} R_{SH}}{\pi} \left( \frac{\pi}{d} + \ln \left[ 1 - \exp \left( -\frac{2\pi (r + 1)}{d} \right) \right] - \ln \left[ 1 - \exp \left( -\frac{2\pi r}{d} \right) \right] + \sum_{m=1}^{\infty} a_m \right), \quad [3.6]$$

where

$$a_m = \frac{\exp \left[ -\frac{2\pi (\alpha - r)m}{d} \right] \left[ \exp \left( \frac{2\pi m}{d} \right) - \exp \left( -\frac{4\pi rm}{d} \right) \right] \left[ 1 - \exp \left( -\frac{2\pi m}{d} \right) \right]}{m \left[ 1 + \exp \left( -\frac{2\pi \alpha m}{d} \right) \right]}, \quad [3.7]$$

and $d$ is $D/s_2$, $r$ is $R/s_2$, and $\alpha$ is $C/s_2$, and it is assumed that $D$, $s_2$, and $C$ are much larger than $R$. It is also assumed that current distributed through $J$ and $K$ is through an area that
is small compared to the area of J and K. This assumption is realized by having a small L_T compared to R.

![FCCM structure with geometry labeled for equation 3.6.](image)

**Figure 3-5**: FCCM structure with geometry labeled for equation 3.6.

After calculating $V_{AB}$, a resistor network, shown in Figure 3-6, can be used to model the contributions to the total voltage drop across J and K, $V_{JK}$. The network contains resistance contributions from the outer contacts, $R_{C,J}$ and $R_{C,K}$, and probe resistance, $R_{P,J}$ and $R_{P,K}$, and the voltage drop across the semiconductor, $V_{AB}$. If $R_{C,J}$ and $R_{C,K}$ are assumed to be the same, then $R_{C,J} = R_{C,K} = R_C$, and $R_C$ can be determined from the resistor network in Figure 3-6 by

$$R_C = \left[\frac{V_{JK} - V_{AB} - (R_{P,J} + R_{P,K})I_{JK}}{2I_{JK}}\right], \quad [3.8]$$

where $R_C$ is in ohms. The probe resistance can be eliminated if a second measurement is performed where the voltage sensing and current sourcing probes are both located on contacts J and K.
After determining $R_C$, $\rho_c$ can be found if it is assumed that the current is distributed evenly around the circumference of contacts J and K with a constant $L_T$. The value of $\rho_c$ can be extracted from

$$R_C = \frac{R_{SH} I_0(kR)}{2\pi k R I_1(kR)},$$

where $I_1$ and $I_0$ are modified Bessel functions, $k^2 = R_{SH}/\rho_c$, and $1/k = L_T$. The Keithley 4200 and probe station were used for the I-V measurements. A current, $I_{jk}$, of 0.10 mA was sourced between contacts J and K (using SMU3 and SMU4), while two voltage sensing probes (using SMU1 and SMU2) were placed on pads 1 and 2, measuring $V_{12}$. The current was sourced for 20 s with 5 values of $V_{12}$ measured and averaged. The current was kept low to avoid degrading the contacts. An identical measurement was performed with the voltage sensing probes on pads J and K for determining $V_{jk}$. Again, an alumina piece was used to insulate the sample from the probe station stage. All geometric values along with $V_{jk}$, $V_{12}$, and $I_{jk}$ were entered into an Excel spreadsheet to calculate $R_{SH}$ and $R_C$. The solver function in Excel, detailed in Section 3.3.1, was used to...
determine $\rho_c$ by finding $k$ from equation 3.9. The FCCM structures were incorporated into a structure that allowed for current stressing of the contacts as well as measuring the change in $\rho_c$.

The fabrication of the FCCM structures will be discussed in the next section when the current stressing structure fabrication is presented. Initially two mesa sizes were used, 1000 x 300 $\mu$m$^2$ and 1500 x 400 $\mu$m$^2$. It was found that the $\rho_c$ measurements and effects of contact stressing were independent of mesa size for the two sizes listed, so the smaller mesa size was preferred due to its smaller footprint on the sample. The distance between contacts, $s_1$, was 200 $\mu$m for the smaller mesa and 300 $\mu$m for the larger mesa. The inner contact radius, pads 1 and 2, was 10 $\mu$m in every case and the outer contact radius, pads J and K, was initially 10, 20, 40, or 60 $\mu$m, and 5 $\mu$m radius contacts were added for lateral stressing described in Chapter 6. As will be described in Chapter 4, only the 10 $\mu$m radius outer contacts provided an accurate measurement of $\rho_c$ and allowed for high enough current densities under vertical current flow to cause contact failure in an appropriate amount of time.

3.4 Current Stressing Structure for Contacts

Given the SiC material provided for this study was grown in a PiN diode arrangement, high current densities could be produced vertically through the structure at low voltages. Figures 3-7 and 3-8 show the final structure. The FCCM structure is incorporated into the p-type layers of the PiN diode. In order to stress the contacts under high current densities, the contacts must be small, which can make probing difficult. To facilitate probing, larger bond pads were fabricated on top of the contacts with a silicon
nitride (SiN\textsubscript{x}) layer insulating the bond pads from the SiC surface, as detailed in the inset in Figure 3-8. The addition of a bond pad also mimics the possible metallization used in a packaged device. A backside metallization is needed to order to generate current through the device vertically. The general fabrication of the device starts with mesa isolation first, then ohmic contact formation on both the front (p-type) and back (n-type) of the structure, followed by SiN\textsubscript{x} deposition and via etching, and finally bond pad formation and completing the backside metallization. Contact photolithography masks labeled “FCCM 01,” “FCCM 02,” or “FCCM 03” were used for the fabrication. Each 5”x5” mask contains patterns for each of the four photolithography steps, “ISO,” “OHM,” “NV1,” and “M1A.” Each mask has slightly different geometry or contacts added for lateral stressing. This section will describe each fabrication step in more detail. Alterations to the fabrication procedure will be discussed in the appropriate chapter.

**Figure 3-7:** Illustration of the current stressing structure utilizing the FCCM.
Figure 3-8: Simplified side-view of current stressing structure. Inset shows contact metallization in greater detail.

3.4.1 Mesa Isolation

Both the FCCM and TLM structures require mesa isolation. Because of the strong chemical bonding in SiC, etching is usually done using plasma etching with a fluorine containing plasma chemistry and a hard etch mask, such as indium tin oxide (ITO) [11]. The photolithography process used for metal lift-off described in Section 3.3.1 was utilized for defining the mesa geometry using the “ISO” pattern on the mask. The ITO (90 wt% indium oxide) etch mask was deposited using sputtering at approximately 1 Å/s to a thickness of 200 nm. The ITO was sputtered with target shutter closed, as to not deposit on the sample, for at least 5 min in order to clean the target. This process is called presputtering. The voltage during sputtering was typically around 485 V and the current was around 175 mA.

After metal lift-off, etching was performed in either an Applied Materials Decoupled Plasma System (DPS) etcher or a Tegal 6540 Cluster Etching System. Both
tools required the use of a Si carrier wafer, and small samples could be attached to the wafer using thermal tape, which loses adhesion when heated above 126 °C, allowing the sample to be unattached from the carrier wafer. The samples were cooled during etching using flowing He along the backside of the Si carrier wafers. For the DPS etch tool, CF$_4$ and O$_2$ were flowed at 50 and 25 sccm, respectively, at an operating pressure of 6 mTorr. The coil power was set to 700 W at 2 MHz while the chuck power was set to 50 W at 13.56 MHz, giving a DC bias of around -70 V. A typical etch rate was around 97 nm/min and samples were etch for 35 min, ensuring that both p-type layers were etched through entirely. The etch selectivity between SiC and ITO was about 36:1. The DPS tool was used for the Ni and Al-based contact study described in Chapter 4.

For the Tegal etch tool, SF$_6$ and O$_2$ were flowed at 30 and 10 sccm, respectively, at an operating pressure of 5 mTorr. The power on the chuck was set to 30 W at 13.56 MHz. The etch rate of SiC was around 230 nm/min and the etch time was 15 min, using three 5 min etches with 5 min between each etch to allow for cooling. The etch selectivity was about 19:1. The Tegal tool was used for the Pd-based contact studies described in Chapters 5 and 6. A KLA-Tencor 500 profilometer was used to measure etch depths and calculate etch rate and selectivity. Additionally, a digital multimeter was also used to check for a large change in resistance between the mesas after etching to ensure isolation. The ITO was removed using DI H$_2$O:HCl (5:1) for 2 min followed by a DI H$_2$O rinse and drying with N$_2$. 


3.4.2 Ohmic Contact Formation

For contact stressing, ohmic contacts are required on both the front and back of the structure for vertical current flow. Contacts were first made to the lower doped n-type substrate. The p-type side was first coated with photoresist for protection. The sample was then subjected to a 2 min 10:1 BOE soak, DI H₂O rinse, and dried with N₂. A blanket layer of 150 nm of Ni (99.99% target) was deposited at approximately 2.4 Å/s at an operating pressure of 5 mTorr. The Ni target was presputtered for at least 5 min. A typical current and voltage during sputtering was 335 mA and 385 V, respectively, although these parameters changed depending on the thickness of the target to keep a consistent deposition rate. The protective photoresist was stripped using the lift-off procedure and the samples were placed p-type side up on the Si carrier wafer in the RTA furnace. Samples were annealed at 1000 °C for 60 s with a ramp rate of 75 °C/s under flowing Ar. Because the contacts were made to a thick, rough substrate, $\rho_c$ could not be calculated; however, CTLM measurements showed that the contacts provided linear I-V curves. Additionally, by covering the entire n-type side with the contact, a large area contact was created which can help in providing a low contact resistance.

For the p-type side, ohmic contacts were needed for the CTLM, TLM, and current stressing structures. The same lift-off photolithography process used for the mesa isolation step could not be used here since the resist stack was nominally only 1.7 µm (LOR5A is approximately 500 nm and SPR 3012 is approximately 1.2 µm) and the mesa height is over 3 µm. It was found that areas on top of the mesas, near the edges, would not be covered with resist using the LOR5A/SPR 3012 resist process. The following
process, using the “OHM” pattern on the mask, was used instead, utilizing Shipley 1827 (~2.7 µm):

1. Degrease with ultrasonic agitation
2. Dehydration bake at 175 °C (blow off with N₂ before placing on hot plate)
3. Coat with HMDS and spin dry at 4000 rpm for 15 s
4. Bake at 112 °C for 15 s on hot plate
5. Coat with MicroChem LOR5A and spin at 7000 rpm for 45 s
6. Bake at 175 °C for 10 min on hot plate
7. Coat with Shipley 1827 and spin at 5000 rpm for 45 s
8. Bake at 115 °C for 60 s on hot plate
9. Align and expose with a Karl Suss MA/BA6 contact aligner for an exposure time of 10.0 s
10. Develop with MicroChem CD-26 developer for 60 s followed by DI H₂O rinse and blow dry with N₂
11. Inspect samples in optical microscope
12. Descum sample with O₂ plasma

Various metallizations were used in this study and each will be described in the appropriate chapter. After metal deposition, metal lift-off was performed and the contacts were annealed in the RTA furnace. Both TLM and CTLM test structures that were fabricated simultaneously with the current stressing structures were measured after this step to ensure acceptable values of $\rho_c$ before continuing the process.
3.4.3 Silicon Nitride Deposition and Via Etch

Due to potential issues of probing the small contacts used in the current stressing structure, larger bond pads were needed. A layer of SiN\textsubscript{x} was used to insulate the bond pad from the SiC surface. Vias etched through the SiN\textsubscript{x} layer were used to allow the bond pads to contact the circular contacts on the p-type side for current stressing. Vias were also etched above the CTLM and TLM structures that were fabricated on the same sample. The SiN\textsubscript{x} was deposited by plasma enhanced chemical vapor deposition (PECVD) due to the low temperatures allowed by process.

A blanket layer of 100 nm of SiN\textsubscript{x} was deposited on the p-type side of the samples using an Applied Materials P-5000 PECVD Cluster Tool. Prior to loading into the chamber, the p-type side of the samples underwent an O\textsubscript{2} descum, as described in Section 3.3.1, in order to improve the adhesion of the SiN\textsubscript{x} layer. An 8” Si carrier wafer was required for processing the sample in the cluster tool. The chamber was cleaned for at least 3 min with a high power plasma treatment (800 W), using O\textsubscript{2} and C\textsubscript{2}F\textsubscript{6} plasma chemistry, before loading the samples. The deposition was performed at a pressure of 2.7 Torr with N\textsubscript{2}, NH\textsubscript{3}, and SiH\textsubscript{4} gas flows set at 1000, 100, and 10 sccm, respectively, and the chuck power was set to 150 W. The process was run for 2 min before loading the samples into the chamber in order to season the chamber for good reproducibility. The deposition parameters gave a rate of approximately 11 Å/s. The refractive index ranged from 1.84 to 1.85. Thickness and refractive index of the SiN\textsubscript{x} were measured using a Gaertner ellipsometer on Si test pieces placed next to the SiC samples during deposition. Process parameters were selected to produce a SiN\textsubscript{x} layer with a high breakdown field [12].
After the blanket layer of SiN$_x$ was deposited, vias above the metal contacts were needed for all test structures. For the contact stressing structures, the SiN$_x$ was made to overlap the contacts by 1 µm in order to ensure the band pads did not contact the SiC directly. Patterned photoresist was used as an etch mask. The following process, using the “NV1” pattern on the mask, was used for the SiN$_x$ via photolithography:

1. Degrease with ultrasonic agitation
2. Dehydration bake at 112 °C (blow off with N$_2$ before placing on hot plate)
3. Coat with HMDS and spin dry at 4000 rpm for 15 s
4. Bake at 112 °C for 15 s on hot plate
5. Coat with Microposit SPR 3012 and spin at 7000 rpm for 45 s
6. Bake at 95 °C for 60 s on hot plate
7. Align and expose with a Karl Suss MA/BA6 contact aligner for an exposure time of 7.0 s
8. Develop with MicroChem CD-26 developer for 45 to 60 s followed by DI H$_2$O rinse and blow dry with N$_2$
9. Inspect samples in optical microscope
10. Descum sample with O$_2$ plasma

The SiN$_x$ was dry etched in a PlasmTherm 720 that utilizes parallel plate configuration. Samples were placed on an anodized aluminum carrier wafer. A chamber clean (“CHMBRCLN” recipe), using oxygen and fluorine-based chemistry, was performed prior to etching. The etching recipe was run for 2 min following the chamber clean in order to season the chamber for good reproducibility. Two recipes were used for
the via formation. The first recipe consisted of CF$_4$ and O$_2$ flowed at 22.5 and 2.5 sccm, respectively, at 50 mTorr for 30 s. The radio frequency (RF) power was 50 W and the corresponding DC bias was typically between -100 to -150 V. This recipe was used for the Ni and Al-based contact study described in Chapter 4.

The second recipe used was found to reduce the DC bias during etching. This recipe used SF$_6$ and O$_2$ flowed at 22.5 and 2.5 sccm, respectively, at 50 mTorr for 1 min. The power was reduced from the previous recipe to 25 W, diminishing the DC bias to around -10 to -15 V. This recipe was used for Pd-based contact studies described in Chapters 5 and 6. The samples were inspected in an optical microscope after etching to make certain all exposed SiN$_x$ was etched. The photoresist was removed using acetone, IPA, DI H$_2$O, and the sample was dried with N$_2$.

### 3.4.4 Bond Pad Formation

For the bond pads, a thick layer of Au was needed to facilitate the high current stressing and mimic a packaged device. An overview of the bond pad formation follows. A blanket seed layer for electroplating was first deposited, and then photolithography was used to define the bond pad size and placement. The bond pads were formed by electroplating Au into the areas not covered by photoresist. After photoresist removal, the unplated areas were etched away leaving the bond pads and SiN$_x$ covering the SiC.

The seed layer was deposited using DC magnetron sputtering. The blanket seed layer was deposited on both sides of the samples, p-type side first. The n-type side required Au in order to make good contact with the probe stage for vertical stressing. The seed layer typically consisted of 10 nm of Ti (99.995% target) deposited at
approximately 1.6 Å/s, 60 nm of TiW (90 wt.% W target, 99.99%) deposited at approximately 1.6 Å/s, and 100 nm of Au (99.99% target) deposited at approximately 2.4 Å/s. The Ti and TiW targets were presputtered for 5 min each while the Au target was presputtered for 2 min. The Ti layer was used for adhesion, the TiW layer was used as a diffusion barrier [13], and the Au layer was used a base layer for plating.

The p-type side was patterned to form the bond pads using photoresist. A top-view of the final structure with the bond pads is shown in Figure 3-9. Circular pads with a radius of 75 μm were formed for the modified FCCM current stressing structures. Bond pads were also formed directly above the contacts in the CTLM and TLM structures fabricated simultaneously with the current stressing structures. Structures used for vertical stressing, mostly in Chapter 4, have extended bond pads on the outer contacts to facilitate easier probing, as shown in Figure 3-9. The following process, using the “M1A” pattern on the mask, was used for bond pad formation:

1. Degrease with ultrasonic agitation
2. Dehydration bake at 115 °C (blow off with N₂ before placing on hot plate)
3. Coat with Shipley 1827 and spin at 4000 rpm for 45 s
4. Bake at 115 °C for 60 s on hot plate
5. Align and expose with a Karl Suss MA/BA6 contact aligner for an exposure time of 15.0 s
6. Develop with MicroChem CD-26 developer for 45 to 60 s followed by DI H₂O rinse and blow dry with N₂
7. Inspect samples in optical microscope
8. Descum sample with O₂ plasma

Figure 3-9: Top-view of current stressing structure with measurements for bond pads (not to scale).

The bond pads were then formed by Au electroplating using Techni Gold ES Au electroplating bath by Technic, Inc. The solution was poured into a 1 L plastic measuring cup. A titanium anode plate was placed on one side of the cup, and the sample was immersed under the plating solution by attaching it to a metal bar sitting on top of the cup by using a Cu wire and alligator clip. The sample was approximately 4” from the anode plate with the p-type side facing the plate. A schematic of the electroplating setup is shown in Figure 3-10. An Agilent 8114A pulse generator was used to supply a pulsed current. The current density used was approximately 1 mA/cm² (0.6 to 1.5 mA depending the sample size). A positive bias was applied to the anode plate at a frequency of 10 Hz and duty cycle of 0.5 (50 ms on, 50 ms off). A 3 kΩ resistor was placed between the sample and ground. A high series resistance was needed in order to source the small current required for plating. An Agilent DSO3202A oscilloscope was used to
measure the voltage across the circuit and across the 3 kΩ resistor, which was used to
monitor the current. The current could be adjusted by changing the output impedance on
the pulse generator and reading the voltage across the 3 kΩ resistor. The impedance was
started at 3 kΩ and varied to obtain the desired current. Samples were plated for at least
45 min to a thickness greater than 1.5 µm. The Au thickness was measured using a
Tencor profilometer. Both sides of the sample were plated simultaneously.

**Figure 3-10:** Schematic of electroplating setup.

After removing the photoresist with acetone, IPA, DI H₂O and drying with N₂, the
unplated seed layer was removed. Two processes were used for seed layer removal. The
first process was a dry and wet etching process, used for the samples fabricated with Ni
contacts. First, the 100 nm Au layer was etched in the PlasmaTherm 720 described
previously. Both the plated Au and Au seed layer were etched, so the bond pad thickness
decreased along with the 100 nm Au seed, although the etched was timed in order to
minimize the plated Au loss. The process gases were Cl\textsubscript{2}, CF\textsubscript{4}, and O\textsubscript{2} flowed at 15, 10,
and 5 sccm, respectively, at a chamber pressure of 10 mTorr. The RF power was 100 W
Corresponding to a DC bias of around -270 V for an etch time of 20 min. Samples were
then placed in Transene GE-8148 Au etch for 5 s to remove any redeposited Au from dry
etching, followed by rinsing in DI H\textsubscript{2}O and drying with N\textsubscript{2}. The TiW was etched using
H\textsubscript{2}O\textsubscript{2} (30%) at room temperature for 3 min while the Ti was etched using 5:1:1 DI
H\textsubscript{2}O:NH\textsubscript{4}OH:H\textsubscript{2}O\textsubscript{2} at room temperature for about 10 to 20 s. The Au bond pads served
as an etch mask in this case, and the wet etchants did not attack the Au. Samples were
inspected in an optical microscope to ensure the seed layer was etched entirely.

The second process used all wet etching and was used to fabricate the rest of the
samples. For the Au, the Transene GE-8148 was used to etch the entire 100 nm Au seed.
Again, some of the plated Au bond pad was also etched since it was used as the etch
mask, but a 20 s etching time allowed the 100 nm Au seed to be etched while minimizing
the amount of Au etched from the bond pads. The TiW and Ti were etched as described
in the previous paragraph. Wet etching the Au also decreased the thickness of the plated
Au on the backside of the samples, although the thickness for the backside was less
critical.

3.5 Current Stressing

For continuous DC stressing, the Keithley 4200 SCS and probe station were used.
A schematic of the electrical measurements used for vertical stressing is shown in Figure
3-11. The samples were placed on the conductive probe station stage and vacuum was
used to ensure good contact between the back of the sample and the stage. The stage was
grounded and a current sourcing probe and voltage sensing probe were placed on the
contact of interest. After $\rho_c$ was extracted using the FCCM, one outer contact was
initially stressed, and it was assumed that the stressing would not affect the contact
resistance of the other contacts. This assumption was later justified as the Joule heating
during testing was found to be localized to the contact being stressed. Initially stressing
one outer contact allowed for the change in $\rho_c$ due to current stressing to be calculated by
modifying equation 3.8 to get

$$ R_{C,d} \text{ (post - stressed)} = \frac{V_{JK} - V_{AB}}{I_{JK}} - R_{C,K}, $$

[3.10]

where $R_{C,K}$ is assumed to be the pre-stressed value of $R_C$ and the probe resistance is
neglected by making a second measurement with the voltage sensing probes on the outer
contacts. Under vertical stressing, the 10 $\mu$m radius contacts were used while 5 $\mu$m
radius contacts were used for lateral stressing. The procedure for lateral stressing will be
discussed further in Chapter 6.
Figure 3-11: Schematic of fabricated device showing the setup for the electrical testing used to extract $\rho_c$ from the FCCM and to stress the contacts vertically.

For vertical continuous DC stressing, the anode contacts were typically stressed for 1 h in air at room temperature. The diode structure limited current stressing to the forward direction. A 10 V compliance was set for vertical stressing. Examples of I-V vs. time plots are shown in Figure 3-12. Electrically stable contacts exhibited very little change in voltage for the set current as shown in Figure 3-12a. Under vertical stressing, failure was characterized when the voltage suddenly increased rapidly to the 10 V compliance, along with a concurrent large drop in stressing current as shown in Figure 3-12b. For some contacts under vertical stressing, a threshold current during the 1 h test was defined where the contact would be considered to have failed at or above that current. Below the threshold current, the contacts were electrically stable. At least 6 contacts were stressed at each current.
Figure 3-12: Example of an I-V vs. time plot of (a) an electrically stable contact and (b) a failed contact.

A schematic of the setup used for vertical pulsed DC stressing is shown in Figure 3-13. Like continuous DC stressing, vacuum was used to hold the sample against the probe station stage. The same Agilent pulse generator and oscilloscope used for Au electroplating, described in Section 3.4.4, were used for pulsed DC stressing. An RF choke, Radio Shack Snap-on RF Choke, was placed between the pulse generator and probe. Four loops of 22 gauge wire was wrapped around the choke, which reduced signal ringing and overshoot. The oscilloscope monitors the voltage across the circuit and a 10 Ω resistor, which used to monitor the current. The test was driven by a computer using code written in Labview. The Labview program holds the current constant by checking the voltage across the 10 Ω resistor and changing the output impedance of the pulse generator to obtain the desired current, kept within 5% of the set current. A 10 V compliance was used for vertical stressing. The test ended when the compliance was reached. The duty cycle of the pulsed stressing was 10% and the on-time was 5 µs.

Pulsed DC lateral stressing is described in Chapter 6.
3.6 Materials Characterization

In order to analyze contact failure and develop and optimize ohmic contacts, materials characterization was required in addition to electrical characterization. Both imaging and elemental analysis are needed to understand the causes behind contact degradation and ohmic contact formation. In addition to profilometry and ellipsometry for processing verification, the main materials characterization techniques used include scanning and transmission electron microscopy and Auger electron spectroscopy (AES). In order to image the small diameter contacts after current stressing, cross-sections of select contacts were produced by focused ion beam (FIB). This section will describe each technique in greater detail.

**Figure 3-13:** Setup for vertical pulsed DC stressing.
3.6.1 Focused Ion Beam

The ability to image cross-sections of stressed contacts is a valuable technique that allows for expedient information collecting for the failure analysis of stressed contacts. Traditional cleaving or cutting is not practical for small, specific areas such as the small diameter contacts used in this study. This issue can be resolved using a FIB-sectioning technique. An FEI Quanta 200 3D dual beam FIB was used in this study for this purpose. The FIB uses a 30 kV Ga ion beam for milling and also has an electron beam for imaging. In order to create a clean cross-section suitable for imaging, a protective layer was needed. An illustration of the cross sectioning of a contact is shown in Figure 3-14 and an example of a completed cross-section is shown in Figure 3-15. The sample was first tilted 52° inside the chamber so that the ion beam was normal to the sample surface, and the contact of interest was found by imaging with the electron beam. The ion beam current was set to 3 nA and a 4 µm long by 20 µm wide W layer was deposited until the surface was covered. The deposition time was about 5 min and typically only a few hundred nanometers of W was needed. Next, a 10 µm long by 20 µm wide window was milled adjacent to the W layer. A 7 nA beam current was typically used for fast milling. The large window is required for subsequent imaging in the electron microscope. A few minutes is needed to mill through the entire metallization and into the SiC, typically about 4 min. The electron beam was used to image the sample at various intervals during the milling and after each milling step. Next a 1 µm long by 20 µm wide area was milled directly adjacent to the W layer. Beam currents of 1.0, 0.5, and 0.3 nA were used to polish the cross-section surface for 1 min each. The
cross-section should be checked after each milling step before moving to the next current in order to monitor its quality.

**Figure 3-14:** Top-view illustration of cross sectioning using FIB (not to scale).

**Figure 3-15:** Micrograph of a FIB-cut cross-section of a contact. Sample tilted to 30° and image is not rescaled to account for the tilt.
3.6.2 Scanning Electron Microscopy

Scanning electron microscopy (SEM) is an essential technique for imaging and measuring dimensions for process development and investigations into contact formation and degradation. A few SEM’s were utilized for this work, all of which were used for process development and verification. An FEI Philips XL-20 was used to measure the dimensions (gap sizes) for the contact resistance structures and image the surface of contacts. For measuring the gap sizes the sample was tilted to 0°. An FEI Quanta 200 Environmental SEM (ESEM), which includes an energy dispersive x-ray spectroscopy (EDS) detector, was used for some elemental examinations of the surface of the Au bond pads, although the technique probes material on the order of a micron below the surface. This issue was mitigated due to the thick, greater than 1.5 µm, Au bond pads. The comparative analysis of stressed and unstressed contacts allowed for some elemental information to be acquired. Finally, a LEO 1530 field emission SEM (FESEM) was used for imaging the FIB-cut cross-sections and the surface of some contacts. The samples were tilted 30° in the FESEM so that the cross-sections could be viewed and micrographs were typically rescaled in ImageJ to account for the altered scales for the x and y dimensions.

3.6.3 Auger Electron Spectroscopy

Auger electron spectroscopy (AES) is a surface sensitive technique used for elemental determination, as elements have signature Auger electron energies. Information is collected from the top 5 to 10 nm. A PHI 670 field emission scanning
Auger microprobe was used for collecting elemental information from the surface of samples and producing elemental depth profiles of contacts by sputtering with a 3 kV Ar ion beam. A 10 kV, 10 nA electron beam was used to create the Auger electrons. Information for depth profiles was taken from an approximately 25 µm by 20 µm area (5000x magnification). The sample was tilted 30° into the ion gun and the sample was not rotated. Auger spectra for the elements of interest were collected after 18 s of Ar sputtering. Surface scans of FIB-cut cross-sections were performed using spot analysis, while surface scans of the top of the Au bond pad of stressed contacts were taken from inside the contact perimeter. PHI Multipak software was used to provide semi-quantitative analysis of the depth profiles [14].

3.6.4 Transmission Electron Microscopy

Transmission electron microscopy (TEM) provides high resolution imaging and elemental information. Thin cross-sections, typically less than 100 nm, are needed for this technique. Cross-sections were prepared by Evans Analytical Group using a FIB sectioning procedure, and a JEOL EM-2010F field emission TEM using a 200 kV beam was used for analysis, performed by Dr. Trevor Clark, Materials Research Institute, Penn State University. Elemental mapping was achieved via EDS in scanning TEM mode.

3.6.5 Surface Temperature Indicators

Under high density current stressing, Joule heating can cause an increase in temperature. That temperature can be an important clue for determining the degradation mechanism of stressed contacts. Tempilaq temperature indicator solution by Tempil and
Omegamarker temperature crayons by Omega Engineering, Inc., were used to approximate the temperature of the surface of the contacts during stressing. The crayon was rubbed onto the surface, or the solution was applied and allowed to dry. The entire surface of the contact stressing structure was covered in order to observe the temperature profile above and around the contacts. The indicator melts when the rated temperature is reached, accurate to within 1%, and melting was observed via an optical microscope during stressing, as shown in Figure 3-16.

![Image: Optical microscope image of temperature indicator melting above current stressed contact.]

**Figure 3-16:** Optical microscope image of temperature indicator melting above current stressed contact.

### 3.7 References


Chapter 4

Initial Contact Studies and FCCM Simulations

4.1 Introduction

As described in Chapter 2, Ni and Ti/Al contacts are probably two of the most widely studied contacts to SiC. The highly doped p-type cap used in the PiN diode structure allows for Ni, typically used for contacting n-type material, to be studied using the test structure described in Chapter 3. By initially investigating these contact schemes, a baseline for contact stability can be found and future metallizations with improved stability can be designed to overcome potential weaknesses associated with the Ni and Ti/Al contacts. The typical approach for the contact studies consists of first finding an optimal ohmic contact annealing temperature, followed by fabricating the current stressing structures, electrical stressing and characterization, and finally materials characterization. All the contacts in this chapter were stressed vertically under continuous DC current. Section 4.3 will describe simulations used to clarify a discrepancy between the values of $\rho_c$ extracted from the FCCM for different contact radii compared to $\rho_c$ extracted from TLM and CTLM structures. The results in this chapter are also presented elsewhere [1,2].

4.2 Experimental Details

Before fabricating the contact stressing structures, the ohmic contact annealing temperature must be optimized to provide the lowest $\rho_c$ for a given metallization. Optimization is usually performed through cumulative annealing, a process where the contact is deposited and annealed at increasing temperatures for the same amount of time.
at each temperature. The value of $\rho_c$ is extracted after the contact deposition and after each annealing step. A separate unannealed contact is then annealed at the temperature providing the lowest $\rho_c$ during the cumulative anneal to ensure a low value. It is possible that annealing at lower temperatures before the optimal annealing temperature may affect the reaction products during the anneal, affecting the value of $\rho_c$. For cumulative annealing, CTLM structures were used, typically with four or five CTLM sets measured and the standard deviation being the error. Fabrication and electrical measurements for the CTLM structures can be found in Section 3.3.1.

The Ni contacts were deposited to a thickness of 100 nm, while the Ti/Al contacts consisted of 25 nm of Ti deposited first, followed by 95 nm of Al. The thickness of Ti and Al were chosen to give a 70 wt.% Al contact, which was found to be an optimal Al fraction as described in the literature review in Section 2.3.2. Both metallizations were sputtered in the Denton sputtering system using DC magnetron sputtering at 5 mTorr, as described previously. All targets were presputtered for 5 min. The Ni (99.99% target), Ti (99.995% target), and Al (99.9995% target) were deposited at approximately 2.4, 1.6, and 1.5 Å/s, respectively. Before loading into the deposition chamber, all samples were subjected to a 2 min 10:1 BOE treatment, DI H$_2$O rinse, and dried with N$_2$. All annealing was performed in the RTA furnace under 3 slm of flowing Ar. The annealing time was 60 s with a ramp rate of 75 °C/s. The annealing temperatures ranged from 700 °C to 950 °C.

The results from the cumulative annealing experiments are shown in Figures 4-1 and 4-2 for the Ni and Ti/Al contacts, respectively. Both the Ni and Ti/Al contacts had nonlinear I-V curves in the as-deposited state and became linear at 700 °C. For the Ni
contacts, 800 °C was found to give the lowest value of $\rho_c$ at $(2.5\pm0.4)\times10^{-5} \ \Omega \ \text{cm}^2$, and a contact annealed directly at the temperature had a $\rho_c$ close to that of $(1.9\pm0.4)\times10^{-5} \ \Omega \ \text{cm}^2$. The optimal annealing temperature for the Ti/Al contacts was higher, 850 °C, with a slightly higher value of $\rho_c$ at $(4.0\pm0.3)\times10^{-5} \ \Omega \ \text{cm}^2$, and $(2.3\pm0.3)\times10^{-5} \ \Omega \ \text{cm}^2$ was found for Ti/Al contacts annealed directly at 850 °C. The Ti/Al contacts were ohmic at 950 °C but the value of $\rho_c$ could not be extracted as the resistance values did not fit well to the CTLM equation. This could be due to oxidation of the Al layer after continual annealing with air exposure after each step for measuring the contact resistance.

![Graph showing values of $\rho_c$ for cumulatively annealed Ni contacts.](image)

**Figure 4-1:** Values of $\rho_c$ for cumulatively annealed Ni contacts.
The optimized Ni (800 °C anneal) and Ti/Al (850 °C anneal) contacts were used in the contact stressing structures. Additionally a W/Al contact scheme, 20 nm of W (99.95% target) followed by 95 nm of Al, was also used. It was found that, like the Ti/Al contacts, annealing at 850 °C for 60 s under flowing Ar provided a low value of $\rho_c$. The addition of W to Al-based contacts has been reported [3,4]. As described in Chapter 3, there was some variation in processing the contact stressing structures over the time of this study. The variations will be clarified here. Photolithography for the contact stressing structures using the Ni contacts was performed using the “FCCM 01” mask. It consisted of two mesa sizes, 1000 x 300 $\mu$m$^2$ and 1500 x 400 $\mu$m$^2$, and outer contacts ranging from 10 to 60 $\mu$m in radius (all inner contacts were 10 $\mu$m in radius). The contact stressing structures employing the Al-based contacts were fabricated using the “FCCM 02” mask, consisting of 1000 x 300 $\mu$m$^2$ mesas with 10 or 5 $\mu$m radius contacts (all contacts on each mesa were either 5 or 10 $\mu$m in radius). Mesa isolation was
completed for all structures using the Applied Materials DPS etch tool, and vias in the SiN$_x$ were etched using the CF$_4$ plasma chemistry. A Ti/TiW/Au (10/60/100 nm) seed layer was used for the Ti/Al contacts, while a W/TiW/Au (10/60/100 nm) seed layer was used for the Ni and W/Al contacts. The seed layer removal from the bond pad formation for the Ni contacts was done through a combination of wet and dry etching, while only wet etching was used for the Al-based contacts. The thin W layer was etched using the same H$_2$O$_2$ etch described for the TiW layer in Section 3.4.4.

All contacts in this chapter were stressed vertically under continuous DC current for 1 h in air using a 10 V compliance. Only the 10 µm radius contacts were used for current stressing as it provided high enough current densities for an observed change after 1 h. Currents ranged from 400 mA to 750 mA or 1.3x10$^5$ to 2.4x10$^5$ A/cm$^2$ for the 10 µm radius contacts. These current densities are much higher than would be normally used in an actual device, particularly under continuous DC current; however, interesting failure mechanisms occurred in an appropriate amount of time, which was useful for developing more stable contacts.

### 4.3 FCCM Simulations

Pre-stressed values of $\rho_c$ for the Ni contacts measured from the FCCM structures exhibited a dependence on outer contact radius as shown in Table 4-1, which includes values extracted from CTLM and TLM structures fabricated on the same samples. While the extracted values of $R_{SH}$ are consistent among all the test structures, only the FCCM structures using the 10 µm radius contacts give a $\rho_c$ value close to values measured from the TLM and CTLM structures, which are in agreement. There was no dependence of $\rho_c$
or $R_{SH}$ on mesa size or contact spacing for the two FCCM geometries used for the Ni contacts.

**Table 4-1**: Comparison of $\rho_c$ and $R_{SH}$ measured from the CTLM, TLM, and FCCM structures.

<table>
<thead>
<tr>
<th>Radius ($\mu$m)</th>
<th>$\rho_c$ ($\Omega \text{ cm}^2$)</th>
<th>$R_{SH}$ ($\Omega / \square$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>CTLM</td>
<td>$(2.1 \pm 1.0) \times 10^{-5}$</td>
<td>331 ± 50</td>
</tr>
<tr>
<td>TLM</td>
<td>$(3.0 \pm 1.7) \times 10^{-5}$</td>
<td>308 ± 30</td>
</tr>
<tr>
<td>FCCM 10</td>
<td>$(3.6 \pm 1.0) \times 10^{-5}$</td>
<td>322 ± 9</td>
</tr>
<tr>
<td>20</td>
<td>$(8.6 \pm 1.6) \times 10^{-5}$</td>
<td>330 ± 3</td>
</tr>
<tr>
<td>40</td>
<td>$(4.8 \pm 1.2) \times 10^{-4}$</td>
<td>330 ± 3</td>
</tr>
<tr>
<td>60</td>
<td>$(1.3 \pm 0.1) \times 10^{-3}$</td>
<td>331 ± 2</td>
</tr>
</tbody>
</table>

To investigate the apparent dependence of $\rho_c$ of contact size, Sentaurus Structure Editor and Device by Synopsys, Inc., version Z-2007.03 [5], were used to generate a similar FCCM structure and model the electrical characteristics. Structure Editor was used to produce a SiC layer with dimensions of 1000 $\mu$m x 300 $\mu$m as shown in Figure 4-3. The thickness of the layer was 0.5 $\mu$m, the same as the heavily doped p-type capping layer in the PiN diode structure. Previous simulations, based on those described here, showed that an order of magnitude more current flows through that layer compared to the more lightly doped p-type injection layer under lateral current flow. Two metal cylinders with a height of 1 $\mu$m and varied radii were placed in contact with the SiC layer where they would be located on the experimental FCCM structures, centered about side D with the center of each cylinder 200 $\mu$m from side D. The resistivity of Au was used
for the contacts as all the experimental contacts had the thick plated Au layer on top. The entire top of each metal cylinder was defined as an equipotential surface for the simulation.

![Figure 4-3: FCCM structure created in Structure Editor.](image)

Sentaurus Device was used to provide the simulated I-V characteristics of the structure. The simulations were run with a constant bias of 0.06 V applied to one contact with the other contact at 0 V. This voltage was similar to that measured in the experimental FCCM structures for a 0.1 mA current. The simulations utilized the materials parameters for SiC from the Sentaurus Device materials library, and the simulation was performed by self-consistently solving Poisson’s equation and the electron and hole continuity equation using drift-diffusion physics. The contact radius was varied from 10 to 60 µm to compare with experimental data. A value of $\rho_c$ was input into the simulation through the “DistResistance” command, which models the contact/semiconductor interface as a distributed resistance in units of $\Omega \text{ cm}^2$, like $\rho_c$, so that each mesh point at the interface acts as a resistor. An example of a command file can be found in the appendix. The values of $\rho_c$ input into the simulation ranged from $10^{-2}$ to $10^{-7} \Omega \text{ cm}^2$. Both $R_{SH}$ and $\rho_c$ were calculated from the FCCM equations described in Section 3.3.3 using the simulated current, $I_{JK}$, for a voltage drop across the outer contacts.
of 0.06 V, $V_{JK}$. The simulated voltage drop across the inner contacts, $V_{12}$, was found by using Sentaurus Tecplot, a post-processing program that can plot the simulated variables, such as potential or current density, as a function of position. The simulated potential drop across the surface of the semiconductor where the inner contacts would be (600,150 µm and 400,150 µm for C,D) was measured in Tecplot. The doping density of the semiconductor was varied until $R_{SH}$ calculated from the simulations was close to the experimental values from Table 4-1. The final doping density was $4.2 \times 10^{18} \text{cm}^{-3}$, p-type as defined in Structure Editor, giving a simulated $R_{SH}$ value of 321 $\Omega/\square$.

Results from the simulations are plotted in Figure 4-4. The ratio of $\rho_c$ calculated from the simulation results to the input $\rho_c$ was used to quantify the accuracy of the $\rho_c$ value extracted from the simulation. In this case, a value of 1 for the ratio would be exact. The simulated results show the same trend as the experimental results from Table 4-1, that for a given value of $\rho_c$, as the contact radius increases, the measured value of $\rho_c$ increases, deviating farther from the true $\rho_c$ value. Additionally, the deviation of the measured value from the actual value increases as the input $\rho_c$ value decreases. The results show that smaller contacts should be used in order to make a more accurate measurement of $\rho_c$, and that the test structure allows for a more accurate measurement for higher values of $\rho_c$, although this fact might not be known before making an experimental measurement. All values of $R_{SH}$ extracted from the simulations were within less than 1% of 321 $\Omega/\square$, showing that there is no dependence of the measured $R_{SH}$ based on the geometries used here.
Figure 4-4: Ratio of values of $\rho_c$ extracted from simulations to the input $\rho_c$ for various contact sizes and input $\rho_c$ values.

Equation 3.9, used to extract $\rho_c$ in the FCCM, assumes that the current is evenly distributed around the circumference of the contacts with a constant $L_T$. The simulated current density contours in Figure 4-5 show that this is not the case for larger contacts, with the 60 $\mu$m radius contacts shown in the figure. The current crowds the side of the 60 $\mu$m radius contacts directly across from the other outside contact. The current crowding worsens as $\rho_c$ decreases as shown for the 60 $\mu$m contact with an input $\rho_c$ value of $10^{-6}$ $\Omega \text{ cm}^2$. The current density appears to be similar around the entire circumference of the 10 $\mu$m radius contacts. The current flow into the 60 $\mu$m contact would not be accurately described by equation 3.9, likely accounting for the large deviation in extracted $\rho_c$ values from the simulations and experiments. This type of current crowding is also evident for the 20 and 40 $\mu$m radius contacts, particularly as the input $\rho_c$ decreases. The accuracy of the FCCM method is likely defined by the contact and mesa size. For the 1000 x 300
µm$^2$ mesa used here, the 10 µm radius contacts give an acceptable $\rho_c$ measurement, although larger contact sizes might be useful for larger mesa sizes.

Figure 4-5: Current density plots for simulated FCCM structures. The metal contacts were removed and a black oval is used to show where the contact was on the 10 µm radius contact structures. The scale bar is applicable to all four simulations.

The y-axis of the plot in Figure 4-4 can be used as a correction factor for the experimental values of $\rho_c$ from Table 4-1, as it describes the ratio of the measured to actual value of $\rho_c$ based on the simulations. By using the average $\rho_c$ from the CTLM and TLM measurements as the true value, 2.6x10$^{-5}$ Ω cm$^2$, a correction factor for each contact radius can be found by running a simulation using 2.6x10$^{-5}$ Ω cm$^2$ as the input value. The correction factors are 1.2, 3.4, 16, and 42 for the 10, 20, 40, and 60 µm radius contacts, respectively. Table 4-2 contains the corrected experimental $\rho_c$ values, which now all closely match the values measured from the TLM and CTLM. This further illustrates that the simulations provide accurate information about the FCCM structure.
Table 4-2: Corrected values of $\rho_c$ from Table 4-1 using the FCCM simulation results.

<table>
<thead>
<tr>
<th></th>
<th>CTLM</th>
<th>TLM</th>
<th>FCCM 10 µm</th>
<th>FCCM 20 µm</th>
<th>FCCM 40 µm</th>
<th>FCCM 60 µm</th>
</tr>
</thead>
<tbody>
<tr>
<td>$\rho_c$ measured</td>
<td>2.1x10^{-5}</td>
<td>3.0x10^{-5}</td>
<td>3.6x10^{-5}</td>
<td>8.6x10^{-5}</td>
<td>4.8x10^{-4}</td>
<td>1.3x10^{-3}</td>
</tr>
<tr>
<td>$\rho_c$ &quot;corrected&quot;</td>
<td>2.1x10^{-5}</td>
<td>3.0x10^{-5}</td>
<td>3.0x10^{-6}</td>
<td>2.5x10^{-6}</td>
<td>3.0x10^{-6}</td>
<td>3.1x10^{-5}</td>
</tr>
</tbody>
</table>

4.4 Nickel Contacts

As described in the previous section, the 10 µm radius contacts provided an accurate measurement of $\rho_c$ based on comparisons with the TLM, CTLM, and simulations. Due to the accuracy of the $\rho_c$ measurement and the ability to create very high current densities for stress, only the 10 µm radius contacts were used for stressing. A pre-stressed $\rho_c$ of $(3.6\pm1.0)x10^{-5} \, \Omega \, \text{cm}^2$ was used, averaged from a minimum of 24 different FCCM structures, with the standard deviation as the error. The remainder of this section will describe the electrical and materials characterization of the contacts leading to the failure mechanism under current stressing.

4.4.1 Electrical Characterization

Table 4-3 shows examples of the time to degradation, defined as the time until the voltage reaches the 10 V compliance, and the change in $\rho_c$ for various currents. As described in Section 3.5, failure occurred when the voltage increased rapidly to the 10 V compliance and the current decreased rapidly to typically less than half of the initial applied current. Entries in Table 4-3 marked with “>1” under time to degradation denote an electrically stable contact where the voltage did not change and the applied current was the same throughout the test. An “instantaneous” label denotes degradation occurred as soon as the current was applied. There was large variability in the time and current
needed to cause degradation. A total of 24 contacts were stressed. Approximately 15% of the contacts tested were electrically stable after 1 h and about half failed instantly or within the first 30 s. Failed contacts exhibited a large change in $\rho_c$, about an order of magnitude or more, while electrically stable contacts showed a smaller change, keeping within one standard deviation of the average. The $R_{SH}$ of the semiconductor showed very little change in all cases.

**Table 4-3:** Examples of variation in current needed to cause failure and time to degradation.

<table>
<thead>
<tr>
<th>Stressed Current (mA)</th>
<th>Time to Degradation (min)</th>
<th>Change in $\rho_c$</th>
</tr>
</thead>
<tbody>
<tr>
<td>400</td>
<td>&gt; 1 h</td>
<td>51%</td>
</tr>
<tr>
<td>400</td>
<td>&gt; 1 h</td>
<td>9%</td>
</tr>
<tr>
<td>400</td>
<td>0.25</td>
<td>460%</td>
</tr>
<tr>
<td>400</td>
<td>10</td>
<td>650%</td>
</tr>
<tr>
<td>500</td>
<td>&gt; 1 h</td>
<td>-50%</td>
</tr>
<tr>
<td>500</td>
<td>instantaneous</td>
<td>510%</td>
</tr>
<tr>
<td>500</td>
<td>1.0</td>
<td>4100%</td>
</tr>
<tr>
<td>500</td>
<td>23</td>
<td>2300%</td>
</tr>
<tr>
<td>600</td>
<td>instantaneous</td>
<td>410%</td>
</tr>
<tr>
<td>600</td>
<td>0.10</td>
<td>2600%</td>
</tr>
<tr>
<td>600</td>
<td>10</td>
<td>12000%</td>
</tr>
<tr>
<td>750</td>
<td>instantaneous</td>
<td>2400%</td>
</tr>
<tr>
<td>750</td>
<td>instantaneous</td>
<td>500%</td>
</tr>
<tr>
<td>750</td>
<td>25</td>
<td>4600%</td>
</tr>
<tr>
<td>750</td>
<td>36</td>
<td>5700%</td>
</tr>
</tbody>
</table>

**4.4.2 Plan-view and Cross-sectional SEM**

The surface of failed contacts became darker in contrast as observed by an optical microscope during stressing. The change in contrast occurred as soon as failure occurred. The FESEM micrograph in Figure 4-6 shows a significant change in surface morphology of the Au pad above the failed contact. The surface appears dome-like with cracking in
the Au. Cross-sections of unstressed and failed Ni contacts are shown in Figure 4-7.

Voiding in the contact is already apparent in the unstressed contact shown in Figure 4-7a. The voiding is much more significant for the failed contact in Figure 4-7b.

![Figure 4-6: FESEM micrograph of the surface of the Au pad above a failed Ni contact.](image)

![Figure 4-7: Cross-section of (a) an unstressed and (b) a failed Ni contact.](image)
4.4.3 AES of Selectively Etched Contact

In order to determine if the voiding was occurring in the Ni/SiC reaction layer, metals were selectively etched by using a series of wet etchants. The seed layer was removed by wet etching described in Section 3.4.4 and Section 4.2 (Transene Au etch for Au and H₂O₂ for both the TiW and W layers). The SiNx layer was etched in 10:1 DI H₂O:HF solution for 45 s. A micrograph of an etched failed contact from the AES instrument is shown in Figure 4-8. The contact contains areas of light and dark contrast. The dark areas of contrast covering most of the contact displayed a relatively low Ni-to-Si signal compared to the lighter areas near the edges, which corresponded to a higher Ni-to-Si signal. Unstressed contacts showed uniform contrast across the entire contact area with a high Ni-to-Si signal after undergoing the same etching conditions. Dr. Bangzhi Liu, Penn State Materials Research Institute, performed the AES analysis presented in this section.

Figure 4-8: SEM image of a failed contact after selectively etching all layers except the Ni/SiC reaction layer.
4.4.4 Degradation Mechanism

The voiding in the unstressed contact, Figure 4-7a, is consistent with the literature presented in Section 2.3.1, where the high temperature Ni/SiC reaction needed for ohmic contact formation can produce NiSi, carbon segregation, and Kirkendall voiding within the Ni/SiC reaction region. The current stressing caused void growth, Figure 4-7b, changing the surface morphology and causing the cracking in the Au layer shown in Figure 4-6. The AES surface scans of the selectively etched failed contact illustrated that some Ni was still present in all of the areas of the contact, more so at the edges. The voiding in the Ni/SiC reaction region could cause some of the reaction region to become unattached, which could easily be washed away during the wet etching, leaving only part of the reaction layer behind. The large void growth would reduce the active area of the contact, causing an increase in applied voltage to sustain the stressing current. The decrease in area would increase localized current densities and heating, likely exacerbating the growth of voids. Rapid void growth is consistent with the sudden increase in voltage to the 10 V compliance observed during stressing. The variability in time and current needed to cause failure might be explained by a variation in initial void size and density across the contacts created by the high temperature Ni/SiC ohmic contact anneal.

4.5 Al-based Contacts

The pre-stressed $\rho_c$ values for the Al-based contacts, shown in Table 4-4, are slightly higher than the pre-stressed values for the Ni contacts described in the previous section, as measured by the 10 µm radius FCCM structures. The Ti/Al contacts had an
average $\rho_c$ of $(4.8 \pm 1.6) \times 10^{-5} \, \Omega \, \text{cm}^2$ while W/Al contacts had an average $\rho_c$ of $(6.8 \pm 1.0) \times 10^{-5} \, \Omega \, \text{cm}^2$. The values are an average of at least 25 FCCM structures with the standard deviation as the error. The rest of this section will be presented similarly to the previous section on Ni contacts, presenting electrical and materials characterization results leading to an explanation of the failure mechanism.

**Table 4-4:** Pre-stressed values of $\rho_c$ and $R_{SH}$ as measured by the FCCM, 1 h threshold current for degradation, and average change in $\rho_c$ for stressed contacts.

<table>
<thead>
<tr>
<th>Contact</th>
<th>$\rho_c$ (Ω cm$^2$)</th>
<th>$R_{SH}$ (Ω)</th>
<th>Threshold Current (mA)</th>
<th>$\Delta \rho_c$ (stable)</th>
<th>$\Delta \rho_c$ (failed)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ti/Al</td>
<td>$(4.8 \pm 1.6) \times 10^{-5}$</td>
<td>338 ± 4</td>
<td>700</td>
<td>-10%</td>
<td>2000%</td>
</tr>
<tr>
<td>W/Al</td>
<td>$(6.8 \pm 1.0) \times 10^{-5}$</td>
<td>328 ± 15</td>
<td>650</td>
<td>-20%</td>
<td>3500%</td>
</tr>
</tbody>
</table>

**4.5.1 Electrical Characterization**

Unlike the Ni contacts, a 1 h threshold current for degradation for vertical stressing was observed for both the Ti/Al and W/Al contacts, 700 and 650 mA, respectively, as shown in Table 4-4. At or above these currents, the contacts would always fail within the 1 h test, with the voltage increasing rapidly to the 10 V compliance and the current reducing, as described previously. The failed contacts, stressed at or above the threshold current, displayed a large increase in $\rho_c$ and the current decreased typically to less than half of the original applied current. As the current was increased above the threshold current, generally the contacts would fail more rapidly. For the Ti/Al contacts, the average time to when the voltage increased to the 10 V compliance was approximately 40 and 10 min for 700 and 750 mA, respectively. For the W/Al contacts, the average time to failure was approximately 15, 10, and 2 min for 650, 700, and 750 mA, respectively. At currents below the threshold current, the current would remain
constant for the 1 h test, typically with a small decrease in voltage. The average $\rho_c$ decreased slightly for these electrically stable contacts.

4.5.2 Cross-sectional FESEM

FESEM micrographs illustrating examples of an unstressed, electrically stable, and failed contact for each contact structure are shown in Figure 4-9. The images of the unstressed contacts (Figures 4-9a and d) reveal an ohmic contact reaction region, TiW barrier, and thick layer of plated Au. For electrically stable contacts (Figures 4-9b and e), those stressed below the 1 h threshold current, smaller voids appear in the plated Au as well as a few within the ohmic contact layer. In addition, brighter areas of contrast are now observed within the ohmic contact region, as indicated within the black ovals added to the figure. These brighter areas could signify a chemical change within the layer; however, neither the chemical change nor the voiding caused an increase in $\rho_c$ or voltage during the test. For failed contacts (Figures 4-9c and f), the bright areas are again observed in the ohmic contact region, although the area appears reduced compared to the electrically stable contacts. The amount of voiding, particularly in the ohmic contact region, is increased for the failed contacts compared to the electrically stable contacts. Increased voiding can also be seen within the Au layer. While the images shown in Figure 4-9 were taken from the inner areas of the contacts, no preferential degradation was observed between the inner areas and periphery of the contacts for all the sectioned contacts imaged. The small overlap between the contacts and the SiNx layer as well as the extended Au bond pads should help reduce oxidation or reactions from the periphery of the contact.
**Figure 4-9:** Cross-section of an unstressed (a) Ti/Al and (d) W/Al, an electrically stable (b) Ti/Al and (e) W/Al, and a failed (c) Ti/Al and (f) W/Al contact imaged by FESEM. The black ovals indicate areas of brighter contrast within the ohmic contact region after current stressing.

### 4.5.3 TEM Characterization

To determine the chemical changes within the contact structure, cross-sectional TEM and EDS mapping were performed by Dr. Trevor Clark, Penn State Materials Research Institute. The TEM micrographs, labeled with the elemental information obtained through EDS mapping, are shown in Figure 4-10. The bright areas of contrast within the ohmic contact region of the electrically stable contacts, Figures 4-10a and c, are identified as Au or Au-containing regions. These Au-containing regions are most likely the bright areas discovered in the cross-sections examined by FESEM (Figures 4-9b and e). Additionally, Al and O was found at the surface of the Au bond pad, which
was also observed by EDS performed in an SEM. For unstressed contacts, only a strong Au signal was observed from EDS performed in an SEM. The movement of Au into the ohmic contact region and Al to the surface indicates TiW barrier failure. The Au in the ohmic contact region can account for some of the voiding in the plated Au layer; however, the extent of voiding in the plated Au in some of the stressed contacts, particularly the failed contacts, cannot by explained by only thermally-induced diffusion of Au into the ohmic contact region, and electromigration of Au from the Au layer to the surface must be considered.

The TEM micrographs of the failed contacts, shown in Figures 4-10b and d, again illustrate more extensive voiding, similar to the FESEM imaged cross-sections in Figures 4-9c and f. Voiding occurred within the ohmic contact region, the plated Au layer, and at the Au/TiW interface. Similar to the electrically stable contacts, Au appears in the ohmic contact region, although to a lesser extent, and Al was found at the surface using EDS in both the TEM and SEM.
4.5.4 Thermally Stressed Contacts

Due to all the elemental movement occurring within the contacts, an approximate temperature during stressing was measured using the temperature indicator solutions/markers described in Section 3.6.5. For the Ti/Al contacts under the highest stressing current, 750 mA, the 593 °C rated indicator melted directly above the contact. The area of the melted indicator increased to about the size of the 10 µm radius contact, indicating that the thermal effects are somewhat localized to the contact area itself. The presence of localized heating verified that by current stressing one contact, other contacts...
would likely not be degraded. At 750 mA, the 649 °C rated indicator did not melt, establishing the temperature of the surface of the failed contacts to be between 593 °C and 649 °C.

To determine the extent that thermal effects have on the degradation mechanism, Ti/Al contacts that did not undergo current stressing were cumulatively annealed in air for 1 h at increasing temperatures up to 650 °C. The average value of $\rho_c$, as measured by the FCCM, after each anneal is plotted in Figure 4-11. Very little change in $\rho_c$ was measured up to 600 °C, and only a 60% increase was measured after 650 °C. This increase is small compared to the order of magnitude or more increase measured for the contacts that failed under current stressing. The fact that annealing alone did not cause the large increase in $\rho_c$ indicated that diffusion caused by Joule heating was not the sole cause of degradation.

![Graph](image)

**Figure 4-11:** Values of $\rho_c$ for Ti/Al contacts cumulatively annealed in air for 1 h. The contacts had not previously undergone current stressing.
The Ti/Al contacts that had been annealed in air at 600 °C were then current stressed at the same currents described previously. The previously annealed contacts failed at currents below the 1 h threshold current listed in Table 4-4, demonstrating that the annealing had caused some damage to the contact structure, although not enough to replicate the failure produced under current stressing. Cross-sections of thermally stressed and current stressed Ti/Al contacts that had previously been annealed at 600 °C are shown in Figure 4-12. The thermally stressed contacts shown in Figures 4-12a and b, annealed at 600 °C and 650 °C, respectively, appear similar to the electrically stable Ti/Al contacts shown in Figure 4-9b, with brighter areas of contrast appearing the ohmic contact layers, which were found to be Au-containing regions by TEM as described earlier. Like the current stressed samples, EDS was performed in an SEM on the surface of the Au bond pads for contacts thermally stressed at 600 °C and 650 °C. Both Al and O signals were apparent on the Au bond pad above the thermally stressed contacts. This again signals movement of both Al and Au across the TiW barrier layer, which occurred in this case from thermal stressing alone.

The electrically stable, previously thermally annealed contact, shown in Figure 4-12c, also has a similar appearance to the thermally stressed contacts and the electrically stable Ti/Al contact from Figure 4-9b, with Au and Al movement across the barrier. The thermally stressed contact that had failed after current stressing, shown in Figure 4-12d, appears similar to the failed contact shown in Figure 4-9c. More extensive voiding is observed in the ohmic contacts layer along with less area of brighter contrast or Au-containing regions compared to the electrically stable or thermally stressed contacts.
**Figure 4-12:** Cross-sectional FESEM micrographs of Ti/Al contacts annealed in air at (a) 600 °C and (b) 650 °C for 1 h without having undergone current stressing. Ti/Al contacts annealed for 1 h at 600 °C followed by current stressing that subsequently were (c) electrically stable and (d) failed. The vertical features spanning the full height of the micrographs are artifacts from FIB sample preparation.

### 4.5.5 Degradation Mechanism

It is clear from the materials characterization that Al-based contact failure, caused by stressing the contact at or above the threshold current, is associated with the extensive voiding in the ohmic contact layer since atomic movement across the barrier was observed for all stressing conditions, current stressing and thermal stressing. An increase in temperature from Joule heating, up to 650 °C, was shown to cause Al to diffuse to the surface of the Au, likely to oxidize, and Au to diffuse to the ohmic contact layer. The movement of Al and Au is consistent with results presented by Oparowski *et al.* [6],
where Al and Au diffusion was observed in a Au/TiW/Al/SiO$_2$/Si stack after annealing at only 300 °C for 1 h in air. The addition of an electrical current must play an important role in the ultimate failure mechanism as the thermal annealing did not cause an electrical change to the contact structure.

Focusing on only the Al and Au species, the most mobile species in this case, the total flux of atoms depends on the flux due to the chemical potential gradient and the flux caused by electromigration [7]. From thermally stressing the contacts, the direction of the flux due to the chemical potential gradient is toward the SiC for Au and toward the surface for Al. As shown in Figure 4-13, electrons are flowing from the metal/semiconductor interface toward the surface, and since Au and Al generally have a negative effective charge, Z* [8], it is expected that the flux of both species should be toward the surface from electromigration. In cases where the contacts remained electrically stable, when stressed below the 1 h threshold current or under thermal stressing at 650 °C and lower, a nearly equal flux of Al leaving and Au entering the ohmic contact region could occur, as illustrated in Figure 4-13b. The nearly equal fluxes of Al and Au would reduce the amount of voiding within the ohmic contact layer.

At or above the threshold current, extensive voiding in the ohmic contact region occurs, which could be attributed to an unequal flux of Au entering and Al leaving the ohmic contact region due to electromigration, as shown in Figure 4-13c. Once voiding begins in the ohmic contact layer, localized current densities will increase causing an increase in Joule heating and electromigration effects. This type of feedback effect is consistent with the rapid failure of the Al-based contacts, where the voltage increases rapidly to the 10 V compliance and the current is immediately reduced. As both Al-based
contacts failed similarly, the Ti and W in the ohmic contact appeared to not have an effect on the degradation mechanism. Since the Ti/Al contacts had a slightly higher threshold current than the W/Al contacts and their $\rho_c$ values were similar, it is possible that the chemical driving force for Au diffusion into the ohmic contact layer is higher for the Ti/Al contacts, as Au can readily react with Al and Ti while there is no significant solid solubility between Au and W [9]. The higher Au chemical potential gradient would help cancel the effects of Al and/or Au electromigration.

**Figure 4-13:** Illustration of an (a) unstressed, (b) low current stressed, and (c) high current stressed Al-based contact.
4.6 Summary

This chapter has presented the initial studies into the stability of Ni and Al-based contacts to SiC under high current densities. The contacts were vertically stressed for 1 h under continuous DC current densities above $10^5$ A/cm$^2$. The current stressing structure utilizing the FCCM for measuring $\rho_c$ before and after stressing was shown to provide an acceptable measurement of $\rho_c$ when 10 $\mu$m radius contacts were used, as confirmed by comparison with values measured by CTLM and TLM and through simulations.

For Ni contacts, growth of voids in the Ni/SiC reaction layer, created during the high temperature ohmic contact anneal, caused contact failure. The void growth reduced the active area of the contact, creating an increase in current density, accelerating failure. This type of failure is consistent with the rapid increase in voltage to the 10 V compliance and a subsequent drop in stressing current observed during stressing. The variation in the time and current needed to cause failure suggests nonuniform void formation among the contacts across the samples.

The Al-based contacts had a slightly higher value of $\rho_c$ compared to the Ni contacts. In the case of the Al-based contacts, a threshold current for the 1 h test was observed. At or above the threshold current, the contacts would always fail with the voltage increasing to the 10 V compliance and the current decreasing. The $\rho_c$ increased an order of magnitude or more for failed contacts. For contacts stressed below the threshold current (electrically stable contacts) the current was stable for the entire 1 h test with the voltage slightly decreasing. The $\rho_c$ decreased slightly on average for the electrically stable contacts. The temperature of the surface of the Au bond pad above the failed contacts under the highest stressing condition was found to be between 593 $^\circ$C and
649 °C. Diffusion caused by Joule heating was not the sole cause of degradation, as thermally stressing contacts to 650 °C for 1 h in air did not cause ρc to increase as much as the increase exhibited by the failed current stressed contacts. Under both thermal and current stressing, the TiW barrier failed as evidenced from Au moving into the ohmic contact region and Al from the ohmic contact region moving to the surface of the Au bond pad. Under thermal stressing or current stressing below the threshold current, the fluxes of Au and Al due to electromigration and the chemical potential gradient are relatively equal. Above the threshold current, there is an inequality in the fluxes and the flux of Al exiting the ohmic contact region becomes greater than the flux of Au entering the ohmic contact region, creating voids. The flux inequality is caused by the increased flux of Al or decreased flux of Au caused by electromigration. Like the Ni contacts, the void creation reduces the active area of the contacts, increasing the effects of electromigration and Joule heating, accelerating the degradation.

4.7 References


Chapter 5

Pd/Ti Contacts and Pulsed DC Stressing

5.1 Introduction

The previous chapter described the failure of Ni and Al-based contacts under high current densities. For the Ni contacts, the high temperature ohmic contact anneal created voids within the ohmic contact layer as a byproduct from the reaction between Ni and SiC. The growth of the voids under current stressing degraded the ohmic contact. In addition to voiding, C segregation is another reaction product from the Ni/SiC ohmic anneal, which can weaken the mechanical stability of the contact by forming a C layer within or on top of the contact. For the Al-based contacts, the unequal fluxes of Al and Au through the TiW barrier caused voiding within the ohmic contact layer and ultimately failure. The Al was driven by a combination of thermal diffusion and electromigration to the surface of the Au bond pad. Due to the low melting point of Al and its propensity to react with other metals at low temperature, such as Au [1], the use of Al in contacts to SiC for high temperature or high power applications may not be ideal. Regions containing Al and Au were observed for stressed Ti/Al contacts in Section 4.5.3.

This chapter will focus on the development and testing of a contact that not only has increased stability under current stressing, but also provides a lower $\rho_c$. The process used to develop this contact is based on a bottom to top approach, where single layer contacts were first tested to garner a low $\rho_c$, and then the rest of the metallization was developed for increased stability. It will be shown in this chapter that Pd-only contacts provide a low $\rho_c$ to the p-type SiC used in this study. As described in Section 2.3.2, like Ni, Pd does not form a carbide phase, so excess C and voiding are potential pitfalls. To
mitigate this effect, the addition of a carbide forming metal to the contact scheme is required, which has been demonstrated for Ni contacts through the addition of Cr or Ti, as mentioned in Section 2.3.1, and for Pd contacts through a Pd/Ti/Pd/Au metallization described in Section 2.3.2. In this study, a Ti layer was deposited on top of Pd to react with the excess C. A thin Pd layer was deposited first in order to control the electrical properties of the contact and to limit the excess C produced during the anneal.

In addition to metal/metal and metal/semiconductor reactions occurring during the high temperature ohmic contact anneal, reactions could occur between the contact and the annealing atmosphere. While Ar was used in Chapter 4 as the process gas in the RTA furnace, N\textsubscript{2} is also commonly employed. With the Ti layer exposed to atmosphere during the annealing, a TiN layer could be formed by annealing the Pd/Ti contact in N\textsubscript{2}. The TiN could increase the stability of the contact as TiN has a high melting point, around 2950 °C, low electrical resistivity, and has been used as a diffusion barrier for contacts to Si [2-8]. Formation of the TiN barrier layer for contacts to Si has been implemented through sputtering [5,6] and annealing in a nitrogen-containing atmosphere to create a TiSi\textsubscript{2}/TiN bilayer [2-4, 8], where the TiSi\textsubscript{2} layer is the ohmic contact. Issues with sputtered TiN include a columnar grain structure, creating fast pathways for diffusion through the barrier, and potentially large stresses, which can cause cracking or peeling of the film [6]. The deposition parameters, such as pressure, percent N\textsubscript{2}, and power, for the sputtered TiN must be optimized for good barrier properties. The process is simplified by creating the TiN layer via thermal annealing. The thermally processed TiN films have been shown to have more of a fine-grained structure [2] and to have little effect on the film stress in the TiSi\textsubscript{2}/TiN bilayer [8].
A single high temperature anneal has been used to create the TiSi$_2$/TiN bilayer to Si; however, a two-step anneal, consisting of a low and then a high temperature step, has also been utilized, which can create a thicker TiN layer and cause the reaction depth of the Ti into the Si to be reduced [3,4]. The low temperature first step allows the Ti to be saturated with N to the solubility limit while no significant reaction occurs between the Ti and Si. The higher temperature anneal creates the ohmic contact and the TiN layer. For the Pd/Ti contacts to SiC, this type of annealing method could increase the TiN thickness as well as limit the interaction of the Ti with the Pd and SiC. Ideally the Ti would not react with the SiC directly and only tie up excess C from the Pd/SiC reaction and with N to form TiN. This would allow PdSi$_x$, as described in Section 2.3.2, to be formed at the metal/semiconductor interface, controlling the electrical properties like a Pd-only contact.

This chapter focuses on the stability of Pd/Ti contacts under both continuous DC and pulsed DC vertical current stress. As mentioned in Section 1.3, high current densities for device operation will likely be in the form of pulsed DC currents. Depending on the frequency and duty cycle, the pulsed DC operation may lead to lower temperatures than continuous DC, possibly resulting in a different failure mechanism for the contact. The continuous DC current stability of the Pd/Ti contacts will be compared to the Ti/Al contacts discussed in the previous chapter. The Pd/Ti contacts will also utilize the TiW barrier and plated Au pad so a more direct comparison can be made. Like the previous chapter, the experimental details will be discussed first, including the optimization of the Pd/Ti contact. The next sections will describe the electrical and materials characterization of the unstressed, continuous DC stressed, and pulsed DC stressed Pd/Ti contacts followed by the failure mechanisms. It will be shown that the failure mechanism
changes depending on if the Pd/Ti contact is stressed under pulsed or continuous DC current. The results from this chapter are also presented elsewhere [9].

5.2 Experimental Details

This section will describe the procedure used to develop the Pd/Ti contact scheme, using a cumulative annealing approach and comparing different metals. Electrical and materials characterization of the contacts will be presented. Finally the process used for fabricating the current stressing structures using the Pd/Ti contacts is explained. The process is modified compared to the process used for the Ni and Al-based contacts in the previous chapter.

5.2.1 Pd/Ti Contact Development

Similar to the Chapter 4, a cumulative annealing approach was used to achieve a single layer metal contact with a low $\rho_c$. Four metals were chosen, Ni, Pd, Pt, and Ti. Although Ni had been studied previously, the material used in this chapter was from a different SiC PiN diode wafer, so the Ni contacts were investigated again in order to make a fair comparison, since any variation in the heavily doped p-type capping layer might not make the extracted $\rho_c$ of the contacts comparable between wafers. The Ni, Pd, and Pt contacts were all deposited to a thickness of 100 nm while the Ti contacts were deposited to 150 nm. The Ni (99.99% target), Pd (99.95% target), Pt (99.99% target), and Ti (99.995% target) were deposited at approximately 2.5, 2.2, 0.9, and 1.6 Å/s, respectively, using DC magnetron sputtering. The Ni and Ti targets were presputtered for 5 min while the Pd and Pt targets were presputtered for 3 min. Before loading into
the deposition chamber, all samples were subjected to a 2 min 10:1 BOE treatment, DI H₂O rinse, and dried with N₂. All annealing was performed in the RTA furnace under 3 slm of flowing Ar. The annealing time was 60 s with a ramp rate of 75 °C/s. The annealing temperatures ranged from 500 °C to 900 °C.

The results from the cumulative annealing experiments are shown in Figure 5-1. The values of ρc were extracted from the CTLM, typically averaged from 4 to 5 sets with the standard deviation as the error. The Ti contacts exhibited the highest value of ρc, with its lowest value from the cumulative anneal at (1.8±0.1)x10⁻⁴ Ω cm² for an annealing temperature of 600 °C. The Ni contacts had similar ρc values as those in the previous chapter, with the lowest value of ρc of (1.7±0.5)x10⁻⁵ Ω cm² at 800 °C, near the value of (2.5±0.4)x10⁻⁵ Ω cm² measured at 800 °C for the cumulatively annealed Ni contacts in the last chapter. Similar values of ρc were produced by the Pd and Pt contacts, both high work function metals from the same column in the periodic table. The lowest value of ρc for the Pt contacts was (6.8±1.6)x10⁻⁶ Ω cm² at 800 °C, while the Pd contacts had a value of ρc of (5.6±2.2)x10⁻⁶ Ω cm² at 850 °C. The Pd contacts had a similar value of ρc of (6.3±0.8)x10⁻⁶ Ω cm² at 700 °C, and the Pt contacts had a value of ρc of (7.5±1.5)x10⁻⁶ Ω cm² at 850 °C.
Figure 5-1: Values of $\rho_c$ for cumulatively annealed Pt, Pd, Ni, and Ti contacts.

It was clear from the cumulative annealing experiments that both Pt and Pd can provide a low value of $\rho_c$. As neither form stable carbides, a second metal would need to be added to the contact metallization in order to mitigate potential C segregation and void formation during the high temperature ohmic anneal. As described in Section 5.1, the increased contact stability proposed here is based on using a thin metal layer contacting the SiC to control the electrical properties, followed by a Ti layer to react with excess C and form a TiN layer on top by reacting with N during annealing via a two-step annealing process. A Pt/Ti and Pd/Ti contact was fabricated to find which scheme provided the lowest $\rho_c$. The contacts consisted of either 10 nm of Pd or Pt, deposited at approximately 0.9 and 0.8 Å/s, respectively, followed by 100 nm of Ti, deposited at approximately 1.6 Å/s. Samples underwent BOE pretreatment as described previously. The low temperature annealing step of the two-step process was chosen to be 400 °C under 3 slm
N\textsubscript{2} so little or no reaction would occur between the Pd or Pt and SiC [10,11]. At 400 °C, it was reported that 90 s was enough time to saturate a 100 nm Ti layer with N [3]. The second step of the anneal was at 850 °C for 60 s, which gave similar values of \( \rho \) for both the Pd-only and Pt-only contacts during the cumulative anneal and should produce a TiN top layer. The ramp rate of both steps was 75 °C/s.

After annealing, the gaps were measured via SEM. The samples were repatterned with the CTLM patterns, and a 100 nm Au layer was deposited directly on top of the annealed contacts. The Au layer was necessary as the metal layer was contributing to the total resistance in the I-V measurements. The annealed Pt/Ti contact had a \( \rho \) of (8.9±1.4)x10\textsuperscript{-6} Ω cm\textsuperscript{2} while the Pd/Ti contact had a \( \rho \) of (5.3±0.9)x10\textsuperscript{-6} Ω cm\textsuperscript{2}. The Pd/Ti contacts were chosen due to the lower \( \rho \) as well as good repeatability as \( \rho \) was (4.7±1.7)x10\textsuperscript{-6} Ω cm\textsuperscript{2} for 7 separately fabricated samples with 4 to 5 CTLM sets averaged per sample. These values are close to the Pd-only contact annealed at 850 °C during the cumulative anneal, with a \( \rho \) of (5.6±2.2)x10\textsuperscript{-6} Ω cm\textsuperscript{2}. The formation of a TiN layer was observed at the surface by a golden appearance, typical of stoichiometric TiN films. A Ti only contact annealed under the same two-step anneal had a \( \rho \) of (4.4±0.5)x10\textsuperscript{-4} Ω cm\textsuperscript{2}, substantiating that the Pd/SiC reaction appeared to be controlling the electrical properties of the Pd/Ti contact. The \( \rho \) of the Pd/Ti contacts is lower than the \( \rho \) reported by Kolaklieva et al. [12] for Pd/Ti/Pd/Au (10/20/70/100 nm) contacts to p-type SiC, described in Section 2.3.2. The \( \rho \) for the Pd/Ti/Pd/Au contacts was 2.8x10\textsuperscript{-5} Ω cm\textsuperscript{2} for a doping concentration of 3x10\textsuperscript{19} cm\textsuperscript{-3} to 5x10\textsuperscript{19} cm\textsuperscript{-3}. The higher doping concentration of the p-type capping layer used in this study could account for the lower \( \rho \) measured here.
5.2.2 AES Depth Profiles

Figure 5-2 shows AES depth profiles of an as-deposited and annealed, 400/850 °C, Pd/Ti (10/100 nm) contact. The O signal tracking the Ti signal in the as-deposited profile in Figure 5-2a is likely from background O within the analytical chamber. Sputter-cleaned Ti will readily adsorb any residual O from within the chamber. The profile for the annealed contact, shown in Figure 5-2b, illustrates that Pd has remained near the SiC interface, suggesting PdSi$_x$ formation, which controls the electrical properties of the contact. Due to the overlap of the N and Ti peaks around 390 eV and that N only has one major peak, the contributions from those elements cannot easily be deconvoluted, so they are plotted together on the depth profile using the 390 eV peak. In addition to the peak at 390 eV, Ti has another major peak at approximately 420 eV. The peak-to-peak heights of a differentiated spectrum at 390 eV and 420 eV have a certain ratio for pure Ti, and if N contributes to the total peak height at 390 eV, then this ratio will be changed. The ratio of the peak-to-peak heights of the differentiated spectra at 390 eV and 420 eV increases in the annealed sample compared with the as-deposited sample, indicative of incorporation of N as could occur with a chemical change typical of TiN [13]. Again, the golden appearance of the contact after annealing is characteristic of TiN. The O signal that appears with the Ti+N signal could be from the adsorption of residual gas in the analytical chamber or the annealing step.
5.2.3 Current Stressing Structure Fabrication

During integration of the Pd/Ti contacts into the current stressing structure, it was found that the small contacts would occasionally oxidize after the ohmic contact anneal, which did not occur while processing the CTLM structures. Oxidation was apparent by a colored tint to the contacts, typically red or purple, instead of the golden color of the top TiN layer typically observed from the CTLM structures. Larger areas of metallization (CTLM and TLM structures) on the contact stressing samples also did not oxidize after the ohmic contact anneal. Since other areas of metallization on the same sample did not oxidize, it was determined that the RTA furnace or the metal deposition was not the source of oxygen in the top layer of Ti.

To mitigate the effect of oxidation of the small contacts, the processing steps for the contact stressing structure was modified. The final contact metallization is shown in the inset in Figure 5-3. The first step of the process was the blanket Ni ohmic contacts to

**Figure 5-2:** AES depth profile of (a) an as-deposited and (b) a two-step annealed Pd/Ti contact.
the backside of the device, as described in Section 3.4.2. Mesa isolation was shifted to
the final step to minimize any potential changes to the SiC surface from the ITO
deposition and removal with HCl. Instead of forming small 10 μm radius contacts via
lift-off photolithography, a blanket layer of SiNx was first deposited and then 10 μm
radius vias were defined and etched through the SiNx to the SiC surface. The Pd/Ti
contacts could be deposited to a much greater size on top of the vias, with only the
metallization in the vias making contact to the SiC, and all other metallization isolated
from the SiC surface using the insulating SiNx. The SiNx deposition and
photolithography is described in Section 3.4.3, with the “OHM” part of the mask,
“FCCM 03,” used as the pattern for via definition, allowing the contacts to be the same
size as in the Al-based contacts in the last chapter. The vias were 10 or 5 μm in radius
for contact definition to the SiC, although the contact metal will be larger in radius. In
this case, 500 nm of SiNx was deposited to ensure that the Pd/Ti layer on top of the SiNx
remain isolated from the SiC after the ohmic contact anneal. The SF₆/O₂ plasma
chemistry, described in Section 3.4.3, was used to etch the vias, as the low DC bias
helped reduce any damage at the SiC surface. The etch time was 80 s.
Figure 5-3: Schematic of current stressing structure. The inset shows the Pd/Ti contact metallization in greater detail.

After etching the SiN\textsubscript{x} and removing the photoresist, the ohmic contacts were ready to be defined. The photolithography process used for lift-off for the CTLM structures and the mesa isolation step, described in Section 3.3.1, was used for this step. The “M1A” pattern was used to create 75 µm radius contact pads above the etched vias. The samples were subjected to 10:1 BOE for only 30 s in this case, as the BOE attacks the SiN\textsubscript{x}, followed by a DI H\textsubscript{2}O rinse and N\textsubscript{2} dry, before loading into the sputtering chamber. The Pd/Ti (10/100 nm) contacts were deposited and annealed using the two-step process described in this section. All areas of metallization appeared golden after annealing.

The bond pads were formed next, directly above the Pd/Ti contacts, again using the “M1A” pattern on the mask. The bond pad formation is described in Section 3.4.4, with a Ti/TiW/Au (10/60/100 nm) seed layer used for the Pd/Ti contacts. The all wet etching process illustrated in that section was used to remove the seed layer. The final plated Au thickness was approximately 1.8 µm. Lastly, the 1000 x 300 µm\textsuperscript{2} mesas were
formed. The photolithography process from Section 3.4.2 was used with the “ISO” pattern from the mask to define the mesa size using the ITO etch mask. The mesas were formed by etching through the SiNx and p-type SiC layers using the Tegal etch tool as described in Section 3.4.1, using a fluorine-based etch chemistry.

Like in the previous chapter, all contacts were vertically stressed. For continuous DC stressing, contacts were stressed for 1 h or more using a 10 V compliance. Under pulsed DC stressing, described in Section 3.5, the contacts were stressed for 10 h or more using a 5 µs pulse, 10% duty cycle, and 10 V compliance. The 10 µm radius contacts were stressed up to 900 mA under continuous DC and 1 A under pulsed DC currents, corresponding to 2.9x10^5 A/cm^2 and 3.2x10^5 A/cm^2, respectively.

5.3 Pre-stressed Contacts

Table 5-1 compares ρc and RSH for the Pd/Ti contacts and Ti/Al contacts from Chapter 4. The ρc for the Pd/Ti contacts, as measured by the 10 µm radius FCCM, was (1.6±0.9)x10^5 Ω cm^2, higher than the (4.7±1.7)x10^6 Ω cm^2 measured from samples with only CTLM structures using the same PiN wafer. The CTLM-only samples did not undergo SiNx deposition and etching or the high temperature backside Ni ohmic anneal. The extra processing steps could have affected the surface of the p-type layer prior to metallization. The large discrepancy in ρc cannot be explained by the differences between the FCCM and CTLM test structures, as the 10 µm radius contacts should still allow for an accurate measurement of ρc around 5x10^6 Ω cm^2, as shown from the simulation results presented in Figure 4-4. The higher value of ρc measured for the Pd/Ti contacts in the current stressing structure is still lower than all the contacts previously
used, including the Ni and Ti/Al contacts with a measured \( \rho_c \) from the 10 \( \mu \text{m} \) radius FCCM of (3.6\( \pm \)1.0)\( \times \)10\(^{-5} \) \( \Omega \) cm\(^2\) and (4.8\( \pm \)1.6)\( \times \)10\(^{-5} \) \( \Omega \) cm\(^2\), respectively.

**Table 5-1:** Pre-stressed values of \( \rho_c \) and \( R_{SH} \) as measured by the FCCM for Pd/Ti contacts and Ti/Al contacts from Chapter 4 for comparison. Also listed are the 1 h threshold current for continuous DC stressing and the change in \( \rho_c \) for electrically stable and failed contacts.

<table>
<thead>
<tr>
<th>Contact</th>
<th>( \rho_c ) (( \Omega ) cm(^2))</th>
<th>( R_s ) (( \Omega )/sq)</th>
<th>1 h continuous DC threshold current (mA)</th>
<th>( \Delta \rho_c ) (no failure)</th>
<th>( \Delta \rho_c ) (failure)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pd/Ti</td>
<td>(1.6( \pm )0.9) ( \times )10(^{-5} )</td>
<td>327( \pm )3</td>
<td>900</td>
<td>-15%</td>
<td>97000%</td>
</tr>
<tr>
<td>Ti/Al</td>
<td>(4.8( \pm )1.6) ( \times )10(^{-5} )</td>
<td>338( \pm )4</td>
<td>700</td>
<td>-10%</td>
<td>2000%</td>
</tr>
</tbody>
</table>

**5.4 Continuous DC Stressing**

The continuous DC stressed Pd/Ti contacts will be compared to the continuous DC stressed Ti/Al contacts, which had the highest 1 h threshold current from the previous chapter. The increased stability of the Pd/Ti contacts compared to the Ti/Al contacts, both possessing a TiW barrier and thick plated Au layer as part of the metallization scheme, will be illustrated in this section.

**5.4.1 Electrical Characterization**

Just like the Ti/Al contacts, the Pd/Ti contacts also exhibited a threshold current for the 1 h continuous DC current stressing test, where the contacts would always fail at the threshold current and remain electrically stable below that current. The change in \( \rho_c \) for failed and electrically stable contacts as well as the 1 h continuous DC threshold current for the Pd/Ti and Ti/Al contacts from Chapter 4 are shown in Table 5-1. The 1 h threshold current for continuous DC stressing is 29% higher for the Pd/Ti contacts compared to the Ti/Al contacts, illustrating an increase in stability. For failed contacts,
the measured voltage would suddenly increase rapidly to the 10 V compliance, along
with a subsequent drop in current, typically to less than half the original stressing current.
At least 6 contacts were stressed at each current. For contacts stressed below the
threshold current (electrically stable contacts), the $\rho_c$ slightly decreased on average and
the measured voltage did not drift more than ±0.1 V. Contacts stressed at the threshold
current, 900 mA, failed on average approximately 20 min into the test.

5.4.2 Cross-sectional FESEM

The Pd/Ti and previously presented Ti/Al contacts are compared in Figure 5-4,
which shows FESEM micrographs of FIB-cut cross-sections before and after stressing.
For the unstressed contacts, Figure 5-4a for Ti/Al and Figure 5-4d for Pd/Ti, the ohmic
contact region, TiW barrier, and Au overlayer can be easily identified. The brighter area
of contrast near the metal/SiC interface for the Pd/Ti contact is suspected to be the PdSi$_x$
layer created during the ohmic contact anneal, which likely controls the electrical
characteristics of the contact. A significant difference is depicted for electrically stable
contacts, Figure 5-4b for Ti/Al and Figure 5-4e for Pd/Ti. For the Ti/Al contacts, bright
areas of contrast, found to be Au-containing regions in the previous chapter, were always
found within the ohmic contact layer. In the Pd/Ti case, the ohmic contact region appears
to be unchanged. In addition to being more electrically stable compared to the Ti/Al
contacts, the Pd/Ti contacts also appear to have increased chemical stability. Some small
voiding is apparent in the plated Au layer in both structures.

Both the failed Ti/Al and Pd/Ti contacts, Figures 5-4c and 5-4f, respectively, have
similar features. Brighter areas of contrast now appear within the ohmic contact region in
both contact structures. Again, these brighter areas were found to be Au-containing for the Ti/Al contacts in the previous chapter. Large voiding appears in the ohmic contact region of both structures, along with voiding in the Au bond pad. The temperature of the surface of failed Pd/Ti contacts, stressed at 900 mA, exceeded 649 °C based on the temperature indicator solution. This temperature is higher than the Ti/Al contacts, which was found to be between 593 °C and 649 °C at the highest stressing condition, of 750 mA.

Figure 5-4: FESEM imaged cross-section of an unstressed (a) Ti/Al and (d) Pd/Ti, an electrically stable (b) Ti/Al and (e) Pd/Ti, and a failed (c) Ti/Al and (f) Pd/Ti contact after continuous DC stressing. The ovals highlight areas of brighter contrast within the ohmic contact region after current stressing.
5.4.3 AES Surface Scans

The bright areas of contrast in the current stressed Ti/Al contacts (Figures 5-4b and 5-4c) were found to be Au-containing regions via TEM analysis, described in the previous chapter. In order to analyze the bright areas in the failed Pd/Ti contact (Figure 5-4f), AES surface scans were performed on the FIB-cut cross-sections. The AES surface scans reduced sample preparation time and cost compared to TEM analysis. Samples were placed on a 30° tilted holder, and then tilted another 15° inside the AES chamber (45° total tilt) in order to view and probe the cross-sections. Point scans were performed on the larger bright areas, on the order of a few hundred nm, as shown in Figure 5-5. The AES scans confirmed that the bright areas were Au-containing for the Pd/Ti contacts as well. The AES scans also detected Si, which forms a low temperature eutectic with Au at approximately 363 °C [14]. In addition to Si, O and C were also detected, likely due to surface contamination, as well as Ga, stemming from FIB sample preparation. No obvious change was evident from comparing surface scans of the Au bond pad above unstressed and stressed contacts.
Figure 5-5: AES surface scan of a cross-section probing a bright area of contrast in a failed Pd/Ti contact. The image of the cross-section is from the FESEM.

5.5 Pulsed DC Stressing

The Pd/Ti contacts were able to sustain a higher stressing current during the 10 h (1 h on-time) test under pulsed DC stressing, up to 950 mA. The short term pulsing (5 µs) and small duty cycle (10%) were used in an attempt to reduce the effects of Joule heating, so much higher current operation was expected. Like the failed continuous DC stressed contacts, a sudden increase in voltage occurred when the contacts failed. FESEM micrographs of cross-sections of an electrically stable and a failed contact are shown in Figure 5-6. The electrically stable contact in Figure 5-6a shows the ohmic contact layer intact, although significant voiding occurred in the plated Au, near the Au/TiW interface. The voiding was not substantial enough to cause electrical degradation of the contact over the 10 h test. More severe voiding is illustrated for the
failed contact in Figure 5-6b. The vertical lines and the apparent roughening of the metal/SiC interface are artifacts from the FIB sample preparation due to the roughening of the contact surface from void formation. Like the electrically stable case, the ohmic contact region appears to be unchanged. The temperature of the Au directly above the contact under 900 mA pulsed current was found to be between 316 °C and 371 °C, significantly cooler than under continuous DC stress where temperatures exceeded 649 °C.

![Figure 5-6: FESEM imaged cross-section of (a) an electrically stable and (b) a failed Pd/Ti contact after pulsed DC stressing. The vertical lines and the apparent roughening of the metal/SiC interface are artifacts from the FIB sample preparation.](image)

To investigate whether contacts under continuous DC stress would exhibit similar voiding, a contact was stressed at 800 mA, 100 mA below the 1 h continuous DC threshold current. After 10 h of continuous DC stressing at 800 mA, the contact remained electrically stable with the voltage decreasing slightly over the 10 h test. The cross-section in Figure 5-7a illustrates that there is no apparent degradation of the ohmic contact region or significant voiding near the Au/TiW interface for the 10 h stressed
contact. There are some small voids in the plated Au layer. The contact is similar in appearance to the electrically stable contact stressed for 1 h in Figure 5-4e. The temperature of the surface was found to be between 593 °C and 649 °C for continuous DC stressing at 800 mA, the same temperature range the current stressed Ti/Al contacts were found to fail, at a current of 750 mA. Increasing the continuous DC current to 850 mA, 50 mA below the 1 h threshold current, a Pd/Ti contact failed in less than 2 h, with the cross-section shown in Figure 5-7b, which is similar to the cross-section of the failed contact in Figure 5-4f. The ohmic contact region contains voids and Au-containing regions. Failure below the 1 h threshold current suggests that longer stressing times may result in a decrease in the threshold current for that specific time period, i.e. a 2 h continuous DC threshold current may be 850 mA instead of 900 mA, the 1 h threshold current.

Since a continuous DC current of 850 mA caused failure in fewer than 2 h, a Pd/Ti contact was stressed under a pulsed DC current to investigate if failure would occur under long term stressing. The contact failed under pulsed DC stressing in under 46 h (more than 4.5 h on-time) and is shown in Figure 5-7c, with the vertical lines and apparent roughening of the metal/SiC interface being artifacts from FIB sample preparation. Voiding near the TiW/Au interface, observed more readily in the inset, is again featured. Although not as severe as the voiding in Figure 5-6b, the thin void must expand to a significant area to cause electrical failure.
Figure 5-7: Cross-section of (a) a stable Pd/Ti contact after 10 h of continuous DC stressing below the 1 h threshold current, (b) a failed Pd/Ti contact after continuous DC stressing below the 1 h threshold current for more than 1 h, and (c) a failed Pd/Ti contact after more than 45 h of pulsed DC stressing. The vertical lines and apparent roughening of the metal/SiC interface in (c) are artifacts from FIB sample preparation.

5.6 Current Density Simulation

Since electrons are moving away from the metal/SiC interface, the voiding occurring in the Au under pulsed DC stressing could be from electromigration. Although the contacts were stressed vertically, the electrons must also move laterally through the Au to the probe providing the positive potential on the surface of the Au bond pad. The probe is typically placed to one side of the contact on the 75 µm radius Au pad.

Simulations were performed using Sentaurus Structure Editor and Device to investigate any current crowding and determine the current density throughout the contact. The simulated current density contours of a contact stressed at 850 mA are shown in Figure 5-8. The simulated structure consisted of a 1000 x 300 x 3 µm p-type SiC layer, doped to $4.2 \times 10^{18}$ cm$^{-3}$, similar to the simulations presented in the previous chapter. A 10 µm radius metal cylinder, 200 nm in height, was used to represent the ohmic contact, and
placed in contact with the SiC where an outer contact would be in the current stressing structure. Centered above the 10 µm radius cylinder, a 75 µm radius metal cylinder with a height of 1.8 µm was used to represent the Au bond pad. The electrical resistivity of Au was used for both the contact and bond pad.

The entire backside of the p-type layer was grounded, while a positive potential was placed to one side of the contact on the surface of the Au bond pad. The positive potential was represented by a 7 µm radius circle on top of the Au pad, the same size as the probe tips used for stressing. The center of the positive potential was placed 40 µm away from the center of the bond pad/contact. A contact resistance of $10^{-5}$ Ω cm$^2$ was input into the simulation. The simulation was performed by self-consistently solving Poisson’s equation and the electron and hole continuity equation using drift-diffusion physics. The simulation forced a current of 850 mA between the positive potential on the surface of the Au pad and the grounded backside of the p-type SiC layer.

The current density plot at the bottom of Figure 5-8 shows current crowding in the bond pad at the edge of the contact and near the probe. A slice along the dashed line in the figure was made and the edge of the contact was magnified, as shown at the top of Figure 5-8. This area is expected to have the highest current crowding. The simulation shows that the Au at the edge of the contact in the direction of the probe experiences current densities of approximately $9 \times 10^5$ A/cm$^2$, three times the nominal current density of $3 \times 10^5$ A/cm$^2$, under vertical current stressing at 850 mA.
Figure 5-8: Simulation of current density for Pd/Ti contacts stressed at 850 mA with the voltage probe placed away from the contact on the Au bond pad.

5.7 Degradation Mechanisms

The failure of the Pd/Ti contacts under both pulsed and continuous DC current stressing appears to be related to the movement of Au. Like the Al-based contacts in the previous chapter, both thermal and electromigration effects must be taken into account. The flux of Au is toward the SiC due to the chemical potential gradient, deduced from the previous chapter and from Au appearing in the ohmic contact region of contacts that failed under continuous DC stressing, which reached very high temperatures. Since electrons are moving away from the metal/SiC interface, the movement of Au due to electromigration should be toward the surface, both laterally and vertically as illustrated from the simulations in Section 5.6. The dissimilar failure modes of the continuous DC
and pulsed DC stressed contacts under similar current densities, but very different temperatures suggest two thermally activated processes are at work.

Under pulsed DC stressing, electromigration of Au away the Au/TiW interface creates voiding, causing failure. This observation from the present study is consistent with Kilgore et al., who found electromigration induced void growth originating from the interface between sputtered TiW and Au, used as a seed layer for Au electroplated lines, which occurred from continuous DC stressing at $2 \times 10^6$ A/cm$^2$ and a temperature of 340 °C to 391 °C [15]. These are similar conditions to those experienced by the Au bond pad under pulsed DC stressing here, around $9 \times 10^5$ A/cm$^2$ at a temperature between 316 °C and 371 °C. Once voiding starts at the edge of the contact, the current crowding increases around the void, causing the void to grow toward the center of the contact. The temperature under pulsed DC stressing was around $0.5T_m$ of Au, where $T_m$ is the melting point.

Under continuous DC stressing, diffusion of Au through the TiW barrier into the ohmic contact layer is the dominant process. Voiding is created during this process, decreasing the active area of the contact, like in the failed Al-based contacts. The temperature during continuous DC stressing exceeds $0.7T_m$ of Au. The higher temperature during continuous DC stressing is consistent with a higher activation energy process such as grain boundary diffusion in TiW, while the lower temperatures during pulsed DC stressing are consistent with a lower activation energy process, such as Au electromigration along the Au/TiW interface and through Au grain boundaries. At continuous DC stressing below the threshold current, neither of these mechanisms dominate, so no failure occurs.
5.8 Summary

This chapter presented the development and testing of a Pd/Ti contact, which exhibited a lower $\rho_c$ and increased stability compared to the Ni and Al-based contacts presented in the previous chapter. By employing a bottom to top approach to design a more stable contact, it was found that Pd-only contacts possessed a low $\rho_c$ to the p-type SiC used here. Although the Pd/SiC reaction can suffer from C segregation and voiding, like the Ni/SiC reaction, by depositing a thin, 10 nm, Pd layer first, followed by a 100 nm Ti layer, it was reasoned that voiding and excess C could be limited by the minimal reaction between Pd and SiC and the addition of Ti would react with any C produced from the Pd/SiC reaction. A two-step annealing process in N$_2$, 400 °C for 90 s followed by 850 °C for 60 s, was utilized to create a thick TiN layer on top of the contact and minimize the reaction between Ti and Pd or SiC. Similar $\rho_c$ values were obtained for Pd-only contacts annealed at 850 °C and Pd/Ti contacts annealed using the two-step process, $(5.6\pm2.2)\times10^{-6}$ Ω cm$^2$ and $(4.7\pm1.7)\times10^{-6}$ Ω cm$^2$ for the Pd and Pd/Ti contacts, respectively. AES depth profiles showed that the Pd stays near the metal/SiC interface after annealing.

The Pd/Ti contacts showed increased stability over the Ti/Al contacts, with an increase in the 1 h continuous DC threshold current for the Pd/Ti contacts of 29% compared to the Ti/Al contacts. Like the Ti/Al contacts, the Pd/Ti metallization included a TiW barrier layer and plated Au bond pad. In addition, below the threshold current, the Pd/Ti contacts not only exhibited electrical stability but also chemical stability as the ohmic contact region appeared unchanged, compared to the Al and Au movement across
the TiW barrier that occurred in the Ti/Al contacts. For Pd/Ti contacts that failed under continuous DC stress, the surface of the contact exceeded 649 °C, causing the movement of Au into the ohmic contact layer and severe intermixing and voiding to occur, degrading the contact.

The Pd/Ti contacts were also subjected to pulsed DC stressing, which reduced the temperature of the contacts to between 316 °C and 371 °C. Under pulsed DC stressing, failure occurred due to voids created by electromigration of Au originating at the Au/TiW interface. Through simulations, it was found that current crowding at the edge of the contact created current densities surpassing $9 \times 10^5$ A/cm$^2$. Although the current densities for both continuous and pulsed DC stressing were similar, the higher temperature from continuous DC stressing caused the diffusion of Au through the TiW barrier to be dominant, consistent with a higher activation energy process. The lower temperatures during pulsed DC stressing caused electromigration of Au along the Au/TiW interface and through the Au grain boundaries to dominate, consistent with a lower activation energy process. This shows that failure mechanisms can differ depending on the stressing conditions used, i.e., pulsed vs. continuous DC current.

5.9 References


Chapter 6

Pd/Ti/P Contacts and Polarity Effects

6.1 Introduction

The previous two chapters described the degradation mechanisms of Ni, Al-based, and Pd/Ti contacts under high current density stressing. The contacts were stressed with current flowing vertically through the PiN diode structure. While the high current densities could be produced at low bias, the current was limited to one direction, so only the anode contacts could be studied. As illustrated in Section 2.5.2, preferential failure could occur at either the anode or cathode, even though the current flowing through each contact is the same. The direction of carriers will influence the movement of atoms due to electromigration, which can affect the degradation mechanism. Additionally, recombination of carriers at an interface can increase localized heating at the contact. This chapter will examine the degradation of contacts to p-type SiC under lateral current flow, allowing for the observation of polarity effects for contact degradation.

In the previous chapter, Pd/Ti contacts exhibited a lower $\rho_c$ and better stability under current stressing compared to commonly studied Ti/Al contacts. The 10 µm radius Pd/Ti contacts were stable under very extreme conditions, 1 h at currents up to 900 mA with a temperature exceeding 649 °C. The electrically stable Pd/Ti contacts were also chemically stable as the ohmic contact layer appeared intact with no observed movement across the TiW barrier layer. One drawback with the Pd/Ti contacts was the susceptibility of the top Ti layer to oxidation, particularly with the small contacts used for current stressing. Typically a capping layer is added to the top of a contact metallization, where the capping layer possesses low electrical resistivity and resistance to oxidation.
While Au is often used, Pt may serve as a more robust alternative due to its higher melting point, 1769 °C for Pt as opposed to 1064 °C for Au. In addition, Pt has been used successfully as a capping layer for contacts to SiC in long-term high temperature studies, as described in Section 2.4. The Ti/TaSi₂/Pt contacts to n-type SiC, presented by Okojie et al., provided excellent thermal stability for 1000 h at 600 °C in air [1]. A Pt layer was added to the Pd/Ti metallization to mitigate oxidation of the Ti layer.

This chapter will first focus on the optimization of the Pd/Ti/Pt contacts, including electrical and materials characterization. Annealing temperature and environment, as well as Pt layer thickness, will be examined. The optimized Pd/Ti/Pt contact will be shown to have a lower \( \rho_c \), a lower ohmic contact annealing temperature, and smoother surface morphology than any of the previously presented contacts. The Pd/Ti/Pt contacts will then be subjected to lateral current stressing to determine if any polarity effects exist for the contacts to p-type SiC. In addition, Ti/Al contacts will also be stressed laterally for comparison. Both contact metallizations will have the electroplated Au bond pad, although only the Ti/Al will use the TiW barrier as Pt has been shown to be effective as a diffusion barrier for Ti/Pt/Au contacts to diamond, annealed for 120 min in vacuum up to 900 °C [2]. The Pd/Ti/Pt contacts will demonstrate improved stability over the Ti/Al metallization, and a polarity effect for contact degradation will be revealed through materials characterization. The fabrication of the structure for lateral stressing will also be discussed.
6.2 Pd/Ti/Pt Contact Optimization

This section will discuss the optimization of the Pd/Ti/Pt contacts to p-type SiC. A cumulative annealing approach will again be used to find an optimal annealing temperature, and the effects of Pt layer thickness and annealing temperature on the surface morphology will be discussed along with the annealing environment, Ar or N₂. Both Auger depth profiles and surface scans will be used to characterize the contacts. The characteristics of the Pd/Ti/Pt contacts will be compared to Pt/Ti/Pt and Ti/Al contacts. The optimized Pd/Ti/Pt contacts will be shown to be thermally stable at 900 °C in an inert gas atmosphere, retaining a low ρₑ and fairly smooth surface morphology.

6.2.1 Electrical Characterization

As in the previous chapters, initial contact optimization was performed utilizing a cumulative annealing approach using CTLM test structures for measuring ρₑ. All samples were subjected to a 2 min 10:1 BOE soak, DI H₂O rinse, and dried with N₂ before loading into the sputtering chamber. Initially the thickness of the Pd, Ti, and Pt layers was 10, 50, and 150 nm, respectively. The layers were deposited at approximately 1.2, 1.6, and 1.6 Å/s, respectively, and the purity of each target was mentioned in previous chapters. The Pd and Pt targets were presputtered for 3 min each while the Ti target was presputtered for 5 min. The contacts were cumulatively annealed in the RTA furnace under flowing N₂ between 600 °C and 850 °C for 60 s at a ramp rate of 75 °C/s. Four to five CTLM structures were measured after each annealing step with the standard deviation as the error. No Au layer was added before the ρₑ measurement, so measured values of ρₑ could be higher than the actual value of ρₑ, as discussed in Section 3.3.1.
The results for cumulative annealing of the Pd/Ti/Pt (10/50/150 nm) contact are shown in Figure 6-1. The lowest value of $\rho_c$, $(3.3\pm0.4)\times10^{-6} \ \Omega \text{cm}^2$, was obtained at 700 °C. The $\rho_c$ increased slightly to $(4.3\pm0.4)\times10^{-6} \ \Omega \text{cm}^2$ at the highest annealing temperature of 850 °C. Because of the low values of $\rho_c$ obtained with this metallization, there is potential for the metal to add significant resistance to the CTLM I-V curves, particularly since the metal may have intermixed, possibly increasing the metal sheet resistance. Slight changes in total resistance values for CTLM gaps were observed by moving the voltage sensing probe on the metal field of the CTLM structure. Additional resistance from the metal could add error to the extracted $\rho_c$ value, as described in Section 3.3.1.

Because of the possibility of error in $\rho_c$ due to resistance from the metal, a Pd/Ti/Pt (10/50/150 nm) contact was deposited and annealed directly to 700 °C for 60 s under flowing N$_2$, since that annealing condition provided the lowest $\rho_c$ from the cumulative anneal. The CTLM gaps were measured via SEM and then the sample was repatterned and 100 nm of Au was added to the metallization to reduce the metal sheet resistance. The $\rho_c$ of the contact was $(1.1\pm0.1)\times10^{-6} \ \Omega \text{cm}^2$, the lowest value of $\rho_c$ measured so far in this study, also at the lowest ohmic contact annealing temperature, as the Ni contacts from Chapter 4 were annealed at 800 °C. The Pd/Ti/Pt contacts were found to be repeatable as the average $\rho_c$ for 3 separately fabricated samples with 4 to 5 CTLM structures measured per sample was $(1.4\pm0.6)\times10^{-6} \ \Omega \text{cm}^2$. A Pd/Ti/Pt contact was also annealed at 700 °C in Ar to observe if the N$_2$ atmosphere was influencing the contact during annealing. The Pd/Ti/Pt contact annealed in Ar had a $\rho_c$ of $(1.2\pm0.3)\times10^{-6} \ \Omega \text{cm}^2$, verifying that the electrical characteristics of the contact remained the same for
both a N₂ and Ar annealing environment. Since a different wafer was used for the experiments in this chapter compared to the previous two chapters, the Pd/Ti contact described in the Chapter 4 was measured on the same wafer as the Pd/Ti/Pt contact for direct comparison. The $\rho_c$ of the two-step annealed Pd/Ti contact was $(3.8\pm1.1)\times10^{-6}$ Ω cm², slightly lower than the value of $(4.7\pm1.7)\times10^{-6}$ Ω cm² from the last chapter, but within error. A 100 nm Au layer was also added to the Pd/Ti contact after annealing and before measuring $\rho_c$.

![Figure 6-1: Values of $\rho_c$ for cumulatively annealed Pd/Ti/Pt (10/50/150 nm) contacts. Contacts were annealed for 60 s at each temperature. CTLM measurements were made without an extra Au layer added after annealing, potentially increasing the measured $\rho_c$ value from the actual value.](image)

As the Pd/Ti/Pt contacts had a lower $\rho_c$ than the Pd/Ti contact, and similar values of $\rho_c$ were provided by both Pd-only and Pt-only contacts, as described in Section 5.2.1, the cumulative annealing experiment was repeated with a Pt/Ti/Pt (10/50/150 nm) stack. The Pt/Ti/Pt contacts were annealed under flowing N₂. Again, since no Au was added
prior to measuring $\rho_c$ using the CTLM structures, the metal sheet resistance could affect the extracted $\rho_c$ value. The lowest value of $\rho_c$ was $(2.5 \pm 0.4) \times 10^{-6} \ \Omega \ \text{cm}^2$ at 750 °C, as shown in Figure 6-2. The $\rho_c$ increased to $(5.2 \pm 0.3) \times 10^{-6} \ \Omega \ \text{cm}^2$ at 800 °C. A Pt/Ti/Pt contact annealed directly to 750 °C, with a 100 nm Au layer added prior to the CTLM measurements, had a $\rho_c$ of $(3.0 \pm 1.0) \times 10^{-6} \ \Omega \ \text{cm}^2$, slightly higher than the Pd/Ti/Pt (10/50/150 nm) contact annealed at 700 °C.

![Graph showing $\rho_c$ vs. Temperature](image)

**Figure 6-2:** Values of $\rho_c$ for cumulatively annealed Pt/Ti/Pt (10/50/150 nm) contacts. Contacts were annealed for 60 s at each temperature. CTLM measurements were made without an extra Au layer added after annealing, potentially increasing the measured $\rho_c$ value from the actual value.

### 6.2.2 Surface Morphology

The SEM images in Figure 6-3 show the surface morphologies of various Pd/Ti/Pt contacts as well as a Pt/Ti/Pt and Ti/Al contact. All contacts were made on the same wafer. The Pd/Ti/Pt (10/50/150 nm) contacts annealed at 700 °C, which possessed a low $\rho_c$, are shown in Figures 6-3a and 6-3b for a contact annealed in $N_2$ and Ar, respectively.
In addition to the low $\rho_c$ value, the Pd/Ti/Pt (10/50/150 nm) contacts also have a smooth surface morphology. Like the electrical characteristics, the annealing environment, N$_2$ or Ar, does not appear to have affected the surface morphology of the Pd/Ti/Pt (10/50/150 nm) contacts annealed at 700 °C. As discussed in the previous chapter, the $\rho_c$ measured for Pd-based contacts studied here, especially for the Pd/Ti/Pt (10/50/150 nm) contact annealed at 700 °C, is lower than the value measured by Kolaklieva et al. [3] for Pd/Ti/Pd/Au (10/20/70/100 nm) contacts to p-type SiC, although the p-type layer is more heavily doped in this study, (3-5)×10$^{19}$ cm$^{-3}$ versus 1×10$^{20}$ cm$^{-3}$ used here. The Pd/Ti/Pt contacts not only have an order of magnitude lower $\rho_c$ than the reported Pd/Ti/Pd/Au contacts, but also a 200 °C less optimal annealing temperature, 900 °C versus 700 °C used here, and much improved surface morphology. The reported Pd/Ti/Pd/Au contacts had a surface roughness of 75 nm and exhibited rougher areas in some parts of the contacts due to dendrite-like formation, with a roughness of 125 nm.

It was found that the Pt layer thickness had an effect on the surface morphology for the Pd/Ti/Pt contacts. Increasing the Pt thickness to 250 nm, keeping the Pd and Ti thicknesses the same at 10 and 50 nm, respectively, caused agglomeration at the surface after annealing directly to 700 °C for 60 s in N$_2$, as shown in Figure 6-3c. Despite the agglomeration, the $\rho_c$ remained within error of the Pd/Ti/Pt (10/50/150 nm) contacts at (8.8±1.9)×10$^{-7}$ Ω cm$^2$. Agglomeration was also observed for Pd/Ti/Pt (10/50/150 nm) contacts annealed directly to 850 °C for 60 s in N$_2$, as shown Figure 6-3d, and the $\rho_c$ increased slightly to (2.9±0.3)×10$^{-6}$ Ω cm$^2$. A Pt/Ti/Pt (10/50/150 nm) contact, annealed under the optimal conditions of 750 °C for 60 s in N$_2$, appeared roughened in some areas of the contact, as shown in Figure 6-3e, but was mostly smooth.
Conventional Ti/Al contacts were also made using a 70 wt.% Al composition as in previous chapters. The thickness of the Ti and Al were 50 and 190 nm, respectively, twice the thickness used previously, so that the total thickness was closer to the Pd/Ti/Pt (10/50/150 nm) contacts. For annealing conditions of 800 °C for 60 s in Ar, 50 °C lower than previous chapters, the $\rho_c$ was $(1.9\pm0.4) \times 10^{-5} \ \Omega \ cm^2$, similar to the $\rho_c$ of $(2.3\pm0.3) \times 10^{-5} \ \Omega \ cm^2$ measured via CTLM for the Ti/Al (25/95 nm) contacts annealed at 850 °C for 60 s in Chapter 4. The surface of the annealed Ti/Al contact, shown in Figure 6-3f, is much rougher than the optimized Pd/Ti/Pt (10/50/150 nm) contact in Figure 6-3a and has an order of magnitude higher $\rho_c$. The high temperature annealing of the Ti/Al contacts, greater than the melting point of Al, causes the Al top layer to melt, roughening the contact and potentially causing the loss of edge acuity in the patterned features, which could potentially cause performance and reliability issues for devices.
Figure 6-3: SEM images of the surface of various contacts. The metallization, annealing conditions, and $\rho_c$ are listed for the contact in each image. All contacts were annealed for 60 s.

6.2.3 AES Surface Scans and Depth Profiles

AES depth profiles are shown in Figure 6-4a for an as-deposited Pd/Ti/Pt (10/50/150 nm) contact and Figure 6-4b for a Pd/Ti/Pt (10/50/150 nm) contact annealed at 700 °C. The O signal tracking the Ti in the as-deposited profile is likely background O in the analytical chamber, adsorbed by the Ti surface after sputtering. The O signal disappears in the annealed profile as the Ti has likely reacted with other elements before depth profiling. The Ti signal is found throughout the Pt layer and near the metal/SiC.
interface, possibly forming Ti-Pt intermetallics, TiSi\textsubscript{x}, or TiC\textsubscript{x} after annealing. The annealed profile also shows that Pt has diffused to the metal/SiC interface along with Pd, likely forming PtSi\textsubscript{x} and PdSi\textsubscript{x}. The high work functions of these silicides could be beneficial for contacts to p-type material. A Si signal is also apparent at the surface of the annealed contact along with Pt, as well as O and C that are likely surface contaminants.

**Figure 6-4:** AES depth profile of an (a) as-deposited and (b) annealed Pd/Ti/Pt (10/50/150 nm) contact. The Pd/Ti/Pt contact was annealed at 700 °C for 60 s in N\textsubscript{2}.

AES surface scans were performed on the surface of a Pd/Ti/Pt (10/50/150 nm) contact annealed at 850 °C, Figure 6-5, and a Pd/Ti/Pt (10/50/250 nm) contact annealed at
700 °C, Figure 6-6, to investigate the agglomeration at the surface. The agglomerates for the Pd/Ti/Pt (10/50/150 nm) contact annealed at 850 °C contain Pd and Pt, illustrating that the higher annealing temperature caused Pd to go to the surface and mix with Pt, causing agglomeration. No significant amount of Pd was detected in areas between agglomerates. For the Pd/Ti/Pt (10/50/250 nm) contact annealed at 700 °C, the agglomerates contained mostly Pt and no Pd. The thicker Pt layer appears to leave unreacted Pt after annealing, causing Pt agglomeration. Silicon was detected in all areas of the contacts. The Pt thickness, or ratio of thickness to that of other layers, greatly influenced the thermal stability of the Ti/TaSi$_2$/Pt ohmic contacts on n-type SiC studied by Okojie et al. [1].

Figure 6-5: AES surface scan of a Pd/Ti/Pt (10/50/150 nm) contact annealed at 850 °C.
6.2.4 High Temperature Stability

It was found that the optimized Pd/Ti/Pt (10/50/150 nm) contact, annealed at 700 °C for 60 s in N₂, showed good thermal stability when annealed at 900 °C for 15 min in N₂ in the RTA furnace. The ρ_c increased slightly from (1.9±0.6)x10⁻⁶ Ω cm² to (3.0±1.0)x10⁻⁶ Ω cm² after the anneal. A Pd/Ti (10/100 nm) contact, annealed under the optimized conditions presented in Chapter 5 (400 °C for 90 s, then 850 °C for 60 s), was further annealed for 15 min in N₂ for comparison. The ρ_c increased from (3.8±1.1)x10⁻⁶ Ω cm² to (9.0±1.3)x10⁻⁶ Ω cm², a larger increase than for the Pd/Ti/Pt contacts. A 100 nm layer of Au was added to all contacts after the 900 °C anneal, prior to the CTLM measurements.

The surfaces of both the Pd/Ti/Pt (10/50/150 nm) contact, annealed at 700 °C, and the Pd/Ti (10/100 nm) contact, annealed at 400/850 °C, before and after the 900 °C, 15 min anneal, are shown in Figure 6-7. Some small agglomerates appear at the surface of the Pd/Ti/Pt contact after the 900 °C anneal, as shown in Figure 6-7c. The agglomerates are small compared to the agglomeration observed for the Pd/Ti/Pt (10/50/150 nm)
contact annealed directly to 850 °C for 60 s (Figures 6-3d and 6-5). It is suspected that
the reactions that occurred after first annealing the Pd/Ti/Pt (10/50/150 nm) contact at
700 °C stabilized the metallization, reducing Pt agglomeration or Pd from diffusing to the
surface to agglomerate during the 900 °C anneal. AES surface scans reveal that the small
agglomerates contain Pt while the other areas show Ti diffusion to the surface. Again, Si
was detected at the surface of all areas of the contact. The Pd/Ti contact also roughened
after the 900 °C anneal, as shown in Figure 6-7d. Some discoloration of the contact was
evident, possibly from oxidation of the top TiN layer.

![Image](image.png)

**Figure 6-7:** Surface of a (a) Pd/Ti/Pt (10/50/150 nm) contact annealed at 700 °C, (c) then
annealed at 900 °C for 15 min in N₂. Surface of a (b) Pd/Ti (10/100 nm) contact annealed
at 400/850 °C, (d) then annealed at 900 °C for 15 min in N₂.

### 6.3 Structure for Lateral Current Stressing

As contacts in the previous chapters underwent vertical current stressing, the
current stressing structure required modification so contacts could undergo lateral current
stressing. The fabrication was simplified to three main steps: ohmic contact formation to p-type SiC, SiN_x deposition and via etch, and bond pad formation. The structure did not facilitate the measurement of $\rho_c$ before or after current stressing, but since ohmic contact formation to p-type SiC was the first step, the contacts should have a similar $\rho_c$ as the contacts measured using the CTLM presented previously in this chapter. Contact degradation was deduced from a total increase in resistance during stressing and from materials characterization. This section will describe the fabrication of the structure for lateral current stressing, the current stressing conditions, and present simulations illustrating the current density and current crowding during stressing. Both the optimized Pd/Ti/Pt (10/50/150 nm) contacts, annealed at 700 °C for 60 s in N_2, and the Ti/Al (50/190 nm) contacts, annealed at 800 °C for 60 s in Ar, were used for the lateral stressing experiments to observe potential polarity effects.

### 6.3.1 Fabrication

Figure 6-8 shows a schematic of the structure for lateral current stressing. After the cleaning procedure described in Section 3.2, the contacts to the p-type layer made using the photoresist process from Section 3.3.1, using the “OHM” part of the “FCCM 03” mask. The circular contacts were either 5 or 10 µm in radius, but only the 5 µm contacts were used for current stressing. The 5 µm radius contacts were in pairs, 20 µm apart edge-to-edge. As mentioned previously, the optimized Pd/Ti/Pt (10/50/150 nm) contacts, annealed at 700 °C for 60 s in N_2, and Ti/Al (50/190 nm) contacts, annealed at 800 °C for 60 s in Ar, were used for current stressing. All samples were subjected to a 2
min 10:1 BOE soak, rinsed with DI H$_2$O, and dried with N$_2$ before loading into the deposition chamber.

**Figure 6-8:** Side-view schematic of the structure for lateral current stressing. The inset shows a top-view of the structure. The dotted lines in the inset indicate where cross-sections for SEM imaging were produced via FIB.

After ohmic contact formation, a blanket layer of 100 nm of Si$_N_x$ was deposited to the p-type side via PECVD. The deposition, photolithography, and etching procedures are described in Section 3.4.3. The Si$_N_x$ vias were defined using the “NV1” pattern on the “FCCM 03” mask. The SF$_6$/O$_2$ plasma chemistry described in Section 3.4.3 was used for Si$_N_x$ etching, with an etch time of 60 s. The Si$_N_x$ overlapped the metal contacts by 1 µm to ensure electrical isolation between the bond pads and the SiC surface, as shown in Figure 6-8. The bond pads were formed last. A blanket seed layer consisting of Ti/TiW/Au (10/60/100 nm) for the Ti/Al contacts and Ti/Au (10/100 nm) for the Pd/Ti/Pt contacts was used. The photolithography and plating conditions were the same as described in Section 3.4.4; however, no seed layer was deposited on the n-type side, so
Au was plated on only the p-type side. The bond pads were defined using the “M1A” pattern on the “FCCM 03” mask. The seed layer was removed using the wet etching process described in Section 3.4.4. The Au was electroplated to a thickness of greater than 2 µm. The 75 µm radius bond pads had a 5 µm overlap between the edge of the bond pad and the contact, as shown in Figure 6-8.

6.3.2 Lateral Current Stressing

The structure for lateral current stressing did not incorporate the FCCM test structure, so $\rho_c$ was not measured for the contacts. Electrically, contacts were monitored for degradation by the change in total resistance during stressing. For continuous DC stressing, the Keithley 4200 SCS and probe station were used, similar to vertical stressing. The sample was placed on a thin piece of alumina to electrically isolate the sample from the stage. Source and sense probes were placed on each adjacent contact. The 5 µm radius contacts were stressed in ambient at 200 mA for 20 h under continuous DC current with a 22 V compliance. The compliance for lateral stressing was higher than for vertical stressing due to the higher series resistance from the SiC under lateral current flow. Unlike vertical continuous DC stressing, the voltage increased gradually for degraded contacts under lateral DC stressing, so no rapid voltage and current changes were observed.

Under pulsed DC stressing, the setup was similar to that of vertical pulsed DC stressing, described in Section 3.5 and shown in Figure 3-13. Again, the sample was placed on a thin piece of alumina for electrical isolation from the stage. Instead of the stage being grounded, like in Figure 3-13, a probe was used to ground the adjacent
contact for stressing. The contacts were stressed at 200 mA using 5 \( \mu \)s pulses and a 10% duty cycle for 200 h (20 h on-time). A 22 V compliance was set and stressing was performed in ambient.

### 6.3.3 Simulation of Current Density under Lateral Stressing

Although both the Pd/Ti/Pt and Ti/Al contacts were stressed under the same current, the \( \rho_c \) of the Pd/Ti/Pt contacts was an order of magnitude lower than the Ti/Al contacts, and thus will have a smaller transfer length (described in Section 3.3.1). Due to the possibility of asymmetric current flow through the circular contacts, with current crowding likely at the leading edge, which is the edge nearest to the adjacent contact, the active area of the contacts cannot simply be calculated using the transfer length that applies for the CTLM measurements (in which circularly symmetric current flows through the contacts).

To assess the current density and effects of current crowding, simulations of the current stressing structure were used. Like in the previous chapters, Sentaurus Structure and Device by Synopsys, Inc., were used for the simulations. A schematic of the structure used for the simulations is shown in Figure 6-9. The structure utilizes symmetric current flow about the axis through the center of the two contacts, so only half a structure is needed for the simulation, which increases the density of mesh points that can be used. Like in Section 4.3, the p-type SiC layer had a thickness of 0.5 \( \mu \)m, representing the capping layer in which most of the current flows laterally, and was doped to \( 4.2 \times 10^{18} \) cm\(^{-3} \). The SiC layer was 2500 \( \mu \)m x 1250 \( \mu \)m (2500 \( \mu \)m for a full structure). Two 5 \( \mu \)m radius cylinders, 200 nm in height, were placed 20 \( \mu \)m apart at the
center of the full SiC layer, to represent the contacts. A 75 μm radius cylinder, 2 μm in height, was placed above the contacts to represent the bond pads. The electrical resistivity of Au was used for the contacts and bond pads. The $\rho_c$ was input into the simulations to match that of the Pd/Ti/Pt and Ti/Al contacts, $1.1 \times 10^{-6} \, \Omega \, \text{cm}^2$ and $1.9 \times 10^{-5} \, \Omega \, \text{cm}^2$, respectively. A current of 100 mA was used for the simulation, as only half the structure was simulated.

![Diagram of the simulation structure](image)

**Figure 6-9:** Structure used to simulate lateral current flow.

The simulated current densities are shown in Figure 6-10, which shows a cross-section of the contacts along the axis through the center of both contacts. A higher current density occurs at the leading edge of both contacts, although some current enters the contacts from all sides. The highest current density and the current crowding effects for the contact with a $\rho_c$ of $1.9 \times 10^{-5} \, \Omega \, \text{cm}^2$, Figure 6-10a, is less than that of the contact with $\rho_c$ of $1.1 \times 10^{-6} \, \Omega \, \text{cm}^2$, Figure 6-10b, as suspected. From the simulations, the maximum initial current density for the Ti/Al and Pd/Ti/Pt contacts are approximately
9x10^5 A/cm² and 1.3x10^6 A/cm², respectively. Current densities/paths may be altered during stressing depending on voiding or a change in transfer length of the contact.

Figure 6-10: Simulation of current density for a \( \rho_c \) of (a) 1.9x10^{-5} \( \Omega \) cm² and (b) 1.1x10^{-6} \( \Omega \) cm².

6.4 Continuous DC Lateral Stressing

The Pd/Ti/Pt and Ti/Al contacts will be compared in this section using electrical and materials characterization, including FESEM of FIB-cut cross-sections and AES scans of the surface of the Au above the contacts. A polarity effect will be shown for the contacts, due to a difference in temperature between the anode and cathode. Also, Pd/Ti contacts were stressed to compare degradation mechanisms between lateral and vertical stressing and between the Pd/Ti/Pt and Pd/Ti contacts. The Pd/Ti samples from Chapter 5 also contained pairs of 5 \( \mu \)m radius contacts that could be used for lateral stressing.
Only a few Pd/Ti contacts were laterally stressed, and no Pd/Ti contacts underwent pulsed DC stressing.

6.4.1 Electrical Characterization and Temperature During Stressing

For 200 mA continuous DC stressing, a starting voltage of 19.8±0.7 V was measured for the Pd/Ti/Pt contacts and 20.8±0.5 V for the Ti/Al contacts. Electrically, the Pd/Ti/Pt contacts were stable for the 20 h test, with an average increase in total resistance of less than 1% after 8 h and 2.5% after 20 h. The Ti/Al contacts reached the 22 V compliance and the stressing current decreased after an average of 9.6 h. The contacts exhibited a 31% increase in total resistance after 20 h, although a larger increase would be expected if the current was held the same throughout the test instead of decreasing after the voltage compliance was reached. The Pd/Ti contacts showed an average increase of 1% in total resistance over the 20 h test and the average starting voltage was 20.3 V. The surface temperatures were similar for all the metallizations; however, the temperature for the anode and cathode were different. For the anode, a surface temperature between 510 °C and 593 °C was determined, while the cathode surface temperature was found to be between 593 °C and 649 °C. It was proposed by Huang et al. [4], as mentioned in Section 2.5.2, that Ni and Ni2Si contacts to p-type Si failed predominantly at the cathode due to increased Joule heating from the electron-hole recombination occurring, which releases energy.
6.4.2 Cross-sectional FESEM

As shown in Figure 6-8, the cross-sections were made along the axis through the center of the concurrently stressed contacts, and the entire contact was sectioned and observed in the microscope. The FESEM micrographs in Figure 6-11 compare an unstressed Pd/Ti/Pt contact with an anode and cathode stressed for different times. The edge of the unstressed contact in Figure 6-11a shows the SiNx overlap between the ohmic contact and the Au bond pad. The winged feature at the edge of the contact is due to the sputtering/lift-off process and is not expected to affect the electrical properties of the contact or the current stressing since it does not make contact with the SiC. After 8 h of stressing, some darker areas appear in the ohmic contact layer at the leading edge of the cathode, shown in Figure 6-11b, possibly signifying intermixing or voiding. The anode (not shown), looks similar to the unstressed contact in appearance after 8 h of stressing. After 20 h, very little damage is evident at the leading edge of the anode, shown in Figure 6-11c, while Figure 6-11d illustrates severe degradation at the leading edge of the cathode, which includes some voiding and possible intermixing. Approximately 1.5 μm of the leading edge of the cathode appears damaged, whereas the remainder of the contact, in all cases, has similar appearance to the unstressed contact.
Figure 6-11: FESEM cross-sectional images of Pd/Ti/Pt contacts. The images are an (a) unstressed, (b) 8 h stressed cathode, (c) 20 h stressed anode, and (d) 20 h stressed cathode after continuous DC current stressing. The winged feature at the edge of the contact is due to the sputtering/lift-off process.

Cross-sections of an unstressed and stressed Ti/Al contacts are shown in Figure 6-12. All metal layers are observed in the unstressed Ti/Al contact in Figure 6-12a (similar the unstressed Ti/Al contact in Figure 4-9). In contrast to the Pd/Ti/Pt case, the 20 h stressed Ti/Al contacts, both the anode (Figure 6-12b) and cathode (Figure 6-12c), appear degraded along the entire length of the contact, with no obvious preferential degradation at the leading edge. The bright areas in the ohmic contact region are similar to those found for stressed Ti/Al contacts in Chapter 4 (Figures 4-9b and 4-9c), which
were discovered to be Au-containing regions. Void formation within the ohmic contact region is also observed for both the anode and cathode.

**Figure 6-12:** FESEM cross-sectional images of Ti/Al contacts. The images are of an (a) unstressed, (b) 20 h stressed anode, and (c) 20 h stressed cathode after continuous DC current stressing.

FESEM micrographs of an unstressed and stressed Pd/Ti contacts are shown in Figure 6-13. The unstressed contact in Figure 6-13a shows the ohmic contact region, TiW barrier, and Au bond pad (similar to Figure 5-4d). Like the Pd/Ti/Pt contact, very little damage is observed in the Pd/Ti anode after 20 h of stressing, as shown in Figure 6-13b. Some voiding and possible intermixing is observed in Figure 6-13c at the leading edge of the cathode after 20 h of stressing. The voiding appears to be near the TiW/ohmic contact interface. There also appears to be a reduction in the bright layer near the metal/SiC interface at the leading edge of the cathode, presumed to be Pd-containing from comparisons to the unstressed contact in Figure 6-13a, shown on the left side of Figure 6-13c. No bright Au-containing areas were observed in the Pd/Ti contact, like the failed Pd/Ti contact presented in Chapter 5 (Figure 5-4f).
Figure 6-13: FESEM cross-sectional images of Pd/Ti contacts. The images are of an (a) unstressed, (b) 20 h stressed anode, and (c) 20 h stressed cathode after continuous DC current stressing.

6.4.3 AES Surface Scans

AES surface scans of the Au bond pad above the contacts further illustrate the polarity effect observed under continuous DC stressing. After 8 h of stressing, Si was detected at the surface of the cathode of a Pd/Ti/Pt contact, but not the anode, as shown in Figure 6-14a. After 20 h, shown in Figure 6-14b, the Au signal on the surface of the cathode becomes significantly reduced compared to the unstressed case and the Si signal becomes comparatively larger. A small Si signal is detected on the surface of the anode after 20 h.
For the Ti/Al contacts, Al was detected after 4 h of stressing at the surface of the Au, as shown in Figure 6-15a, but not at the surface of the anode. After 20 h, the Au signal at the surface of the cathode is greatly reduced, while the Al signal increases, as shown in Figure 6-15b. In addition, Si was also detected at the surface of the cathode after 20 h. After 20 h, Al was revealed at the surface of the anode along with a small Si signal. The bright areas of contrast in the ohmic contact region of the stressed Ti/Al contacts, shown in Figures 6-12b and 6-12c, were confirmed to be Au-containing via surface scans of the FIB-cut cross-sections using AES. A small Si signal was detected at the surface of Pd/Ti contacts after 20 h of stressing, for both the anode and cathode.
Figure 6-15: AES spectra of the surface of the Au bond pad above a Ti/Al contact after (a) 4 h and (b) 20 h of continuous DC current stressing.

6.5 Pulsed DC Lateral Stressing

Under pulsed DC stressing using 200 mA, 5 µs pulses, and a 10% duty cycle, no electrical degradation during the 200 h (20 h on-time) test was evident for both the Ti/Al and Pd/Ti/Pt contacts. Although electrical degradation was not detected, physical changes in the contact were observed after 200 h of stressing and will be presented in this section. The temperature of the surface of both the anode and cathode of both contact schemes was reduced compared to the continuous DC stressed contacts to between 204 °C and 232 °C. The reduced temperature is due to the short-term pulses and small duty cycle. The polarity effect due to different temperatures of the anode and cathode during stressing is not apparent under pulsing. At this lower temperature range, the difference in temperature may not be large, or the temperature difference may fall into a range that cannot be discerned by the temperature indicators.

Cross-sections of the pulsed DC stressed Pd/Ti/Pt contacts, imaged in the FESEM, are shown in Figure 6-16. Unlike the continuous DC stressed contacts, both
anode and cathode have a similar appearance, with some voiding near the leading edge of the contact. The voiding appears to be between the Au bond pad and the top of the ohmic contact and the SiN$_x$ isolation layer. The voiding starts approximately 3.5 µm into the contact from the leading edge and extends all the way to the edge of the bond pad. No additional damage to the ohmic contact layer was observed nor was any Si detected at the surface of the contacts via AES prior to sectioning, unlike in the continuous DC stressed case where Si was detected at the surface after stressing.

![Cross-section of a pulsed DC stressed Pd/Ti/Pt](image)

**Figure 6-16:** Cross-section of a pulsed DC stressed Pd/Ti/Pt (a) cathode and (b) anode.

In contrast to the Pd/Ti/Pt contacts, the cross-sectional FESEM images of the pulsed DC stressed Ti/Al contacts in Figure 6-17 exhibit similar characteristics to the continuous DC stressed Ti/Al contacts, with areas of brighter features in the ohmic contact layer, which were found to contain Au. The bright feature in the cathode, Figure 6-17a, appears right at the leading edge, while the bright feature in the anode, Figure 6-17b, is a few microns from the leading edge of the contact. Some small voiding is also apparent in the ohmic contact layer at the metal/SiC interface at the leading edge of the anode. Also near the bright features, a thin bright layer appears next to the metal/SiC
interface, possibly Au preferentially reacting with elements in that region. The features above the bright area in the cathode, Figure 6-17c, could be small voids resulting from the Au that diffused into the ohmic contact. Neither the cathode nor anode displayed any Al or Si signal from AES surface scans of the Au bond pads above the contacts prior to sectioning.

![Cross-section of a pulsed DC stressed Ti/Al (a) cathode and (b) anode. Higher magnification images are shown for the (c) cathode and (d) anode.](image)

**Figure 6-17:** Cross-section of a pulsed DC stressed Ti/Al (a) cathode and (b) anode. Higher magnification images are shown for the (c) cathode and (d) anode.

### 6.6 Degradation Mechanisms

A clear polarity effect was observed for the continuous DC stressed contacts, with the cathodes degrading preferentially. This polarity effect likely stems from the difference in temperature between the anode and cathode during stressing, which could be attributed to carrier recombination increasing the temperature at the cathode of the
p-type material. For the Pd/Ti/Pt contacts, intermixing and voiding was apparent at the leading edge of the cathode after 20 h of stressing, along with Si diffusion to the surface of the Au bond pad, which possibly forms an oxide due to stressing in ambient. The Si was likely from the ohmic contact layer, as Si was found at the surface of the annealed Pd/Ti/Pt ohmic contact, described in Section 6.2.3. Much less damage occurred at the anode, probably due to the lower temperature. Any increase in resistance during stressing was likely caused by the damage at the cathode.

For the Ti/Al contacts under continuous DC stressing, a similar failure phenomena as described in Chapter 4 occurred, with Au from the bond pad diffusing into the ohmic contact layer and Al from the ohmic contact layer going to the surface. An inequality of fluxes can cause voiding, reducing the active area of the contact and increasing the resistance. While the cross-sections of both the anode and cathode appeared similar, the AES scans showed a larger Al signal at the surface of the cathode compared to the anode after both 4 and 20 h.

The Pd/Ti contacts that were stressed under a lateral continuous DC current also developed preferential degradation at the cathode, with some voiding and possible intermixing. Some Si was detected at the surface of the bond pads after 20 h of stressing, possibly from the ohmic contact. The Pd/Ti contacts probably had the least amount of visible damage, and the increase in total resistance was only about 1% after 20 h of stressing.

 Preferential failure of the anode or cathode was not evident under pulsed DC stressing for either the Pd/Ti/Pt or Ti/Al contacts. For the Pd/Ti/Pt contacts, voiding occurred between the Au bond pad and the ohmic contact and SiN$_x$ layer. Since both the
anode and cathode exhibit similar void formation, electromigration of Au away from the interface is probably not an important factor since electrons move away from the metal/SiC interface at the anode and toward the metal/SiC interface at the cathode, making the anode more susceptible to voiding from electromigration. A more likely possibility is that the Au bond pad has delaminated because of mechanical stresses caused by the mismatch of coefficients of thermal expansion (CTE) of the materials in the test structure and thermal cycling from current pulsing, in which the contacts were pulsed over $10^{10}$ times during the 200 h test. The 10% duty cycle (45 µs off-time per period) could allow the contacts to cool significantly between the 5 µs pulses, especially since SiC has good thermal conductivity [5]. The CTE of Pt, Ti, Au, and Si$_3$N$_4$ are approximately 9.1, 8.4, 14.3, and $3.0 \times 10^{-6}$/°C, respectively, at 20 °C [6]. There is a large mismatch in CTE between Si$_3$N$_4$ and the metals, particularly Au. Furthermore, the highest temperature during stressing should be at the leading edge of the contact due to current crowding, so it is not surprising that voiding occurred at the location that probably exhibited the greatest temperature excursions during pulsed testing. Since the temperature of both the anode and cathode were similar, the stresses should also be similar, so no polarity effect would be expected or was observed.

For the pulsed DC stressed Ti/Al contacts, Au diffused into the ohmic contact layer in some parts of the contact, in contrast to the continuous DC stressed Ti/Al contacts where Au diffusion and voiding was prevalent along the entire length of the contact. The bright feature appearing right at the leading edge of the cathode could be attributed to increased Joule heating from current crowding. The bright feature a few microns from the leading edge in the anode might be explained by a defect or weak area
in the TiW barrier, allowing an easier path for Au diffusion. The Au diffusion did not affect the overall resistance during stressing, and no Al was found at the surface of either the anode or cathode.

6.7 Summary

This chapter detailed the development of Pd/Ti/Pt contacts and the investigation of polarity effects on the degradation of contacts under lateral current stressing. The Pd/Ti/Pt (10/50/150 nm) contacts, annealed at 700 °C, provided a much lower $\rho_c$, $(1.4\pm0.6)\times10^{-6} \ \Omega \ \text{cm}^2$, compared to conventional Ti/Al contacts, $(1.9\pm0.4)\times10^{-5} \ \Omega \ \text{cm}^2$, and even the Pd/Ti contacts presented in the previous chapter, $(4.7\pm1.7)\times10^{-5} \ \Omega \ \text{cm}^2$. The optimized Pd/Ti/Pt contact also possessed good surface morphology and required a lower ohmic contact annealing temperature compared to the Ti/Al contacts. The surface morphology depended on the Pt thickness and annealing temperature, with a thicker Pt layer or higher annealing temperature causing agglomeration at the surface. The surface of the optimized Pd/Ti/Pt contact remained fairly smooth and $\rho_c$ increased by 58%, compared to a 137% increase for Pd/Ti contacts, after annealing at 900 °C for 15 min in N₂.

The Pd/Ti/Pt contacts were shown to be more stable under lateral stress compared to Ti/Al contacts after stressing 5 µm radius contacts at 200 mA continuous DC current for 20 h. The total resistance during stressing increased by only 2.5% for the Pd/Ti/Pt contacts after 20 h, while the Ti/Al contacts showed a 31% increase. The most severe damage for the Pd/Ti/Pt contacts appeared at the leading edge of the cathode, illustrating a polarity effect. The polarity effect could be explained by the higher temperature of the
surface of the cathode, between 593 °C and 649 °C, likely stemming from carrier recombination. Silicon was detected at the surface of the Pd/Ti/Pt contacts, with a larger signal coming from the cathode. Severe intermixing and voiding at the cathode edge caused the increase in total resistance for the Pd/Ti/Pt contacts. In contrast to the Pd/Ti/Pt contacts, the Ti/Al contacts appeared to be degraded along the entire length of both the anode and cathode. The temperature of the Ti/Al contacts was the same as the Pd/Ti/Pt contacts, with the cathode having a higher temperature than the anode. The movement of Al and Au, as presented in previous chapters, was again the degradation mechanism for the Ti/Al contacts. A larger Al signal was detected at the surface of the cathode compared to the anode, suggesting expedited degradation of the cathode. Pd/Ti contacts, described in the last chapter, were also stressed, and the damage at the cathode appeared less severe than for the Pd/Ti/Pt contacts, with only a 1% increase in total resistance after 20 h, although some voiding and possible intermixing had occurred.

For pulsed DC stressing for 200 h using a 200 mA current with 5 µs pulses and a 10% duty cycle, both the Pd/Ti/Pt and Ti/Al contact metallizations remained electrically stable. The temperature of the surface of the contacts was reduced to less than 232 °C during stressing. While evidence of Au diffusion into the ohmic contact layer of the Ti/Al contacts was observed, the Pd/Ti/Pt ohmic contact layer remained unchanged. The only degradation in the complete test structure for the Pd/Ti/Pt contacts was voiding between the Au bond pad and the ohmic contact and SiNx layers. The voiding was suspected to have occurred due to mechanical stress caused by the mismatch of CTE of the materials in the test structure and thermal cycling from the pulsed testing.
6.8 References


Chapter 7

Summary and Future Work

7.1 Summary

The materials properties of SiC make it an attractive choice for high temperature and high power applications. The replacement of Si components with SiC-based semiconductor devices could lead to the reduction in size, weight, complexity, and cooling requirements and an increase in efficiency, which could in turn save money and have a positive environmental impact. An area of concern for the use of SiC devices in extreme conditions is the stability of ohmic contacts, which provide a connection between the device and the rest of the circuit. Ohmic contact instability can cause an increase in parasitic series resistance, which could lead to degradation in device performance or failure. While the stability of contacts to SiC have been investigated under high temperatures, little has been reported on the stability of contacts under high current densities. Along with effects of Joule heating, electromigration of material at the contacts can influence contact degradation. Since carriers can flow from the semiconductor to the metal and vice versa, preferential degradation of the anode or cathode can occur, referred to as a polarity effect. The objective of this work has been to explore the degradation of ohmic contacts to SiC under high current density stressing. Differing failure mechanisms were found depending on whether current was stressed continuously or by pulsing, and a polarity effect was observed under continuous DC stressing. In addition to current stressing, more robust contacts were developed that possessed a lower $\rho_c$ compared to conventional Ni and Ti/Al contacts. A combination of
electrical and materials characterization, particularly the use of FIB-cut cross-sections for imaging via FESEM and AES surface analysis, were used to analyze contact degradation.

A structure for current stressing was introduced, taking advantage of the available SiC PiN diode material. Contacts to p-type SiC could be stressed vertically while $\rho_c$ could be measured before and after stressing using the FCCM. Current stressing studies were limited to the anode in this configuration. Simulations were performed to investigate the accuracy of the FCCM. It was shown that smaller circular contacts provided a more accurate measurement of $\rho_c$ for a given mesa size. Initial studies of high current density stability were performed using the well-studied Ni and Ti/Al contacts at continuous DC current densities of greater than $10^5$ A/cm$^2$ for 10 $\mu$m radius contacts. The metallization structure included a TiW barrier layer and a thick electroplated Au bond pad, which were fabricated after the ohmic contact anneal. The Ni contacts degraded due to the growth of voids in the ohmic contact layer. The voids were initially produced as a reaction product during the high temperature Ni/SiC contact anneal.

Al-based contacts were found to be more electrically stable than the Ni contacts based on the Ni contacts failing at a lower current than the Al-based contacts during the 1 h test. The Al-based contacts degraded due to the movement of Al from the ohmic contact layer to the surface of the Au bond pad, and the movement of Au from the bond pad into the ohmic contact layer. Below a defined threshold current for 1 h of continuous DC stressing, the $\rho_c$ of the Al-based contacts did not change appreciably and they were deemed electrically stable, while stressing at the threshold current and above, the $\rho_c$ increased by an order of magnitude or more. For electrically stable contacts, the fluxes of Al and Au through the TiW barrier were relatively equal. Failed contacts incurred
voiding within the ohmic contact layer, likely causing the increase in \( \rho_c \). The voiding was caused by the inequality of Al and Au fluxes from the effects of electromigration. Thermally stressed Al-based contact structures also displayed the movement of Al and Au, although the \( \rho_c \) of contact structures annealed at 650 °C in air for 1 h did not increase as significantly as current stressed contacts, where the temperature of the surface of the contact under the maximum stressing current was found to be between 593 °C and 649 °C. Minimal voiding in the ohmic contact layer occurred under thermal stressing.

A bottom to top approach was then used to develop a more robust contact structure, taking into account the failure mechanisms of the Ni and Al-based contacts, which included voids produced during the ohmic contact anneal and Al movement and reactions within the contact metallization. A Pd/Ti (10/100 nm) contact was introduced that when annealed using a two-step process in \( \text{N}_2 \), 400 °C for 90 s followed by 850 °C for 60 s, provided a \( \rho_c \) of \((4.7 \pm 1.7) \times 10^{-6} \, \Omega \, \text{cm}^2\), compared to the Ni and Ti/Al contacts which both had a \( \rho_c \) of greater than \( 10^{-5} \, \Omega \, \text{cm}^2\). The contact scheme took advantage of the low \( \rho_c \) provided by a Pd-only contact and a Ti layer to react with C, which should reduce void formation that can occur when a contact scheme reacts with only Si, such as a Pd-only or Ni-only contact. The Ti layer reacting with C should also increase the mechanical stability of the contact. Annealing in \( \text{N}_2 \) produced a robust TiN layer at the contact surface.

A 29% increase in the 1 h threshold current for failure under continuous DC current was found for the Pd/Ti contacts compared to the Ti/Al contacts, both having a TiW barrier and Au overlayer. Pd/Ti contacts stressed right below the 1 h threshold current were not only electrically stable, but also chemically stable as the ohmic contact
layer appeared unchanged. The temperature of the surface of failed Pd/Ti contacts exceeded 649 °C, causing the movement of Au into the ohmic contact region leading to severe intermixing and voiding. Under pulsed DC stressing using 5 µs pulses and a 10% duty cycle, the temperature during stressing was reduced to between 316 °C and 371 °C. Under pulsed DC stressing, the Pd/Ti contacts degraded due to voids created by electromigration of Au originating at the Au/TiW interface. Although the current densities were similar for both continuous and pulsed DC stressing, the temperature during stressing caused the differing degradation mechanisms. Diffusion of Au through the TiW barrier occurred at the higher temperatures caused by continuous DC stressing, consistent with a higher activation energy process, while electromigration of Au along the Au/TiW interface and through the Au grain boundaries dominated under the lower temperatures provided by pulsed DC stressing, consistent with a lower activation energy process.

The Pd/Ti contacts were susceptible to oxidation because of the top layer of Ti, so a Pd/Ti/Pt (10/50/150 nm) contact was introduced, which provided the lowest value of ρc measured in this study, (1.4±0.6)x10⁻⁶ Ω cm², at a lower ohmic contact annealing temperature, 700 °C, which was at least 100 °C lower than any of the other contact metallizations used here. The optimized Pd/Ti/Pt contacts also possessed very smooth surface morphology, especially compared to the conventional Ti/Al contacts. Pd/Ti/Pt metallizations that were annealed at a higher temperature (850 °C) or had a thicker Pt layer (250 nm) possessed a rougher surface morphology after annealing characterized by agglomeration at the surface, even though the electrical characteristics were similar to the
optimized Pd/Ti/Pt contact. The Pd/Ti/Pt contacts to p-type SiC were stressed laterally in order to observe any polarity effects.

The Pd/Ti/Pt contacts, as well as the Pd/Ti contacts, were shown to be more stable under continuous DC lateral stressing compared to Ti/Al contacts. The total resistance of the Pd/Ti/Pt contacts increased only by 2.5% while the total resistance of the Ti/Al contacts increased by 31% after 20 h of stressing 5 µm radius contacts using a 200 mA current. A polarity effect on temperature was observed during stressing with the temperature of the cathode measured to be between 593 °C and 649 °C and the anode between 510 °C and 593 °C, likely stemming from carrier recombination at the cathode on the p-type material. Severe intermixing and voiding at the leading edge of the cathode caused degradation of the Pd/Ti/Pt contacts, whereas little damage occurred at the anode due to the temperature differential. In contrast, the Ti/Al contacts appeared degraded along the entire anode and cathode, with Au and Al movement causing degradation, as observed for the vertically stressed Ti/Al contacts. For the Ti/Al contacts, AES surface scans showed a higher Al signal on top of the cathode compared to the anode, illustrating more rapid degradation at the cathode. Pd/Ti contacts were also stressed laterally and appeared to be the most stable with only a 1% increase in total resistance after 20 h of stressing. The damage at the leading edge of the Pd/Ti cathode appeared less than the damage observed in the Pd/Ti/Pt cathode, although voiding and possible intermixing occurred.

For pulsed DC lateral stressing using 200 mA, 5 µs pulses, and a 10% duty cycle, both the Ti/Al and Pd/Ti/Pt contacts remained electrically stable after 200 h as the temperature was reduced to below 232 °C during stressing. Although the Ti/Al contacts
suffered from Au diffusion into the ohmic contact layer, the Pd/Ti/Pt ohmic contact layer appeared to be intact. Unlike under continuous DC stressing, the pulsed DC stressing caused voiding in the contact structure for the Pd/Ti/Pt contact metallization, which occurred between the Au bond pad and the ohmic contact and SiNx layers. Because the voiding was observed for the both the anode and cathode, electromigration of Au was likely not the cause of voiding due to the opposite direction of electron flow for the anode and cathode, meaning that electromigration of Au away from the Au/contact interface would likely happen only at the anode. The voiding was suspected to have occurred due to the mismatch of CTE of the materials in the test structure leading to mechanical stresses and thermal cycling from the pulsed testing.

7.2 Future Work

While low resistance, stable Pd-based contacts to p-type SiC were developed in this work, a detailed analysis of the ohmic contact formation mechanism would be beneficial in further ohmic contact development, especially an analysis of the Pd/Ti/Pt contact which provided a low $\rho_c$ at a low annealing temperature. Materials characterization utilizing TEM analysis techniques would be ideal to study the phase formation at the metal/SiC interface, since phase identification and phase location within the metallization structure cannot easily be discerned through AES depth profiles. Additionally, techniques that could detect point defect formation at the metal/SiC interface would be advantageous in discerning the ohmic contact formation mechanism, as any metal/semiconductor reaction could produce defects, which may be important for low $\rho_c$ contact formation. Defect states produced during the Ni/SiC and Ti/Al/SiC ohmic
contact anneal were discussed in the literature review in Chapter 2, and similar interface states could be formed during the Pd-based ohmic contact anneal.

A limitation in this study was that only contacts to p-type SiC were examined due to material constraints. The degradation of contacts to n-type SiC would be interesting since the polarity effect may be different, as indicated by reported studies of the degradation of contacts to Si in the literature. The cathode preferentially degraded for contacts to p-type SiC, likely due to the increase in temperature at the cathode compared to the anode from carrier recombination at the cathode. This type of recombination would not occur in contacts to n-type material since electrons are the majority carrier. An ohmic contact that could be made to both n-type and p-type SiC under the same annealing conditions, with similar electrical properties, would provide a fair comparison and be useful for devices where simultaneous formation of contacts to both n- and p-type SiC would simplify processing.

Finally, long-term current and temperature stressing of the Pd-based contacts compared to conventional Ti/Al and Ni contacts would be valuable. Stressing under less elevated conditions would provide more thorough information for long-term reliability and allow for lifetime predictions of the contacts.
Appendix

Example of Command File for Sentaurus Device for FCCM Simulations

Electrode {
    { Name="contacta" Voltage=0}
    { Name="contactb" Voltage=0}
}

File {
    * Input files
    Grid    = "fccm_msh.grd"
    Doping    = "fccm_msh.dat"
    Parameter = "models_SiC.par"

    * Output files
    Current = "fccm.plt"
    Plot    = "fccm.tdr"
    Output  = "fccm.log"
}

Physics{
    EffectiveIntrinsicDensity( OldSlotboom )
    Mobility ( 
        DopingDep
        HighFieldSaturation
    )
    Recombination( 
        SRH
        Auger
    )
}

Physics(
    MaterialInterface = "SiliconCarbide/Gold"){
    DistResistance=1e-5
}

Plot{
    *--Density and Currents, etc
    eDensity hDensity
    TotalCurrent/Vector eCurrent/Vector hCurrent/Vector
eMobility hMobility
eVelocity hVelocity
eQuasiFermi hQuasiFermi

*--Temperature
eTemperature Temperature * hTemperature

*--Fields and charges
ElectricField/Vector Potential SpaceCharge

*--Doping Profiles
Doping DonorConcentration AcceptorConcentration

*--Generation/Recombination
SRH Band2Band * Auger
AvalancheGeneration eAvalancheGeneration hAvalancheGeneration

*--Driving forces
eGradQuasiFermi/Vector hGradQuasiFermi/Vector
eEparallel hEparallel eENormal hENormal

*--Band structure/Composition
BandGap
BandGapNarrowing
Affinity
ConductionBand ValenceBand
eQuantumPotential

Math {
  Digits=7
  ErrRef(electron) = 1E-12
  ErrRef(hole) = 1E-12
  RHSmin=1e-30
  RHSmax=1e30
  CDensityMin=1e-30
  Notdamped=20
  Iterations=15
  RecBoxIntegr
}

Solve {
  *-Build-up of initial solution
  NewCurrentFile="init"
Coupled (Iterations=100) {Poisson}
Coupled {Poisson Electron Hole}
Plot (FilePrefix="fccm_zero_Bias")

*IdVd curve
NewCurrent="fccm_0p06_Bias"
Quasistationary (   
    Goal {Name="contacta" Voltage=0.06}   
    Minstep=1.0 MaxStep=1.0
) {Coupled {Poisson Electron Hole} }
Plot (FilePrefix="fccm_0p06_Bias")
}
VITA

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Select Publications


