The Pennsylvania State University

The Graduate School

Department of Electrical Engineering

# DESIGN, FABRICATION AND CHARACTERIZATION OF ANTIMONIDE MOS TRANSISTORS

A Dissertation in

Electrical Engineering

by

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# ABSTRACT

Future transistor scaling will require enhancement in device electrostatics (multigate), channel transport enhancement (beyond strained Silicon) and reduction in parasitics (contact, junction engineering etc.). Due to the high electron mobility and hole mobility (using strain), antimony (Sb) based III-V materials are of strong interest as channel material for low power all-antimonide complementary metal-oxide-semiconductor (CMOS) digital logic. Sb-based MOSFETs can operate at high speed and very low supply voltage, which promises to dramatically lower the power dissipation in future high-speed logic circuits.

This dissertation will describe compound semiconductor based transistor architecture which integrates mixed anion $InAs_xSb_{1-x}$ quantum-wells (QW) exhibiting very high electron mobility, for ultra-low power logic applications. I will discuss the following aspects of the n-channel Sb MOSFETs using experimental data and detailed modeling: a) material selection and device design; b) strategy for integrating a high-k dielectric using a composite barrier scheme; c) equivalent oxide thickness scalability including quantum capacitance; and d) transport properties in long and short channel Sb NMOSFETs. The dissertation concludes with benchmarking the performance of Sb NMOSFETs with other III-V devices, and address the feasibility of Sb NMOSFETs for enhancement mode (normally OFF) logic transistors operating with ultra low energy dissipation.

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# Chapter 1

## Antimonide NMOSFET Device Design for Ultra-low Power Logic Applications

A transistor is essentially a "*switch*" which controls the flow of current between two terminals, using a "*gate*" that acts as a valve. The goal is to make this switch work at very high speed with very low power dissipation. Scaling the dimensions of transistors has led to exponential increase in density and switching speed, and a similar decrease in the switching energy [1]. The supply voltage of the transistor has been scaled in a similar proportion as the dimensions to reduce the power dissipation in the transistors as the number of transistors per chip increased exponentially. The processor power continued to rise even with scaling the supply voltage due to increased die size and fast frequency scaling [2]. As the total power dissipated in the microprocessor reached 100W (Figure 1-1), the frequency and die scaling were stopped. MOSFETs entered a "power constrained scaling" phase where the power dissipation was limited to 100W per chip [3]. To integrate more functions or to pack more transistors into the microprocessor, the supply voltage was required to be scaled. Since the threshold voltage and the sub-threshold slope of the transistor did not scale with the supply voltage [4], the leakage power density continued to increase as the supply voltage was scaled. Scaling the supply voltage without scaling the threshold voltage would lead to reduced switching speed and slower performance, which is not desired. Innovations in the past decade (high-κ metal gate, strain and tri-gate architectures) have improved the performance of the transistors in the past decade and helped scale the supply voltage moderately (from ~1.2V for planar 65nm to ~0.9V for 22nm tri-gate transistors) [4].

Future transistor scaling will require enhancement in device electrostatics (multigate), channel transport enhancement (beyond strained Silicon) and reduction in parasitics (contact, junction engineering etc.). Near threshold voltage operation can improve the energy efficiency of computing as shown in Figure 1-2, and can help scale the supply voltage [5]. Introducing a new material which has a higher carrier velocity than silicon would help to aggressively scale the supply voltage to around 0.5V, while maintaining the same or better performance levels as Si at high gate overdrive. III-V semiconductors comprising of elements from group III and V of the periodic table have extra-ordinary mobility (which translates to enhanced carrier velocities for short channel MOSFETs) compared to silicon and can help achieve near threshold voltage operation. Figure 1-3 shows the electron and hole mobility of various III-V compound semiconductors [1]. Antimonide based semiconductors are very attractive since they have high electron as well as high hole mobility.

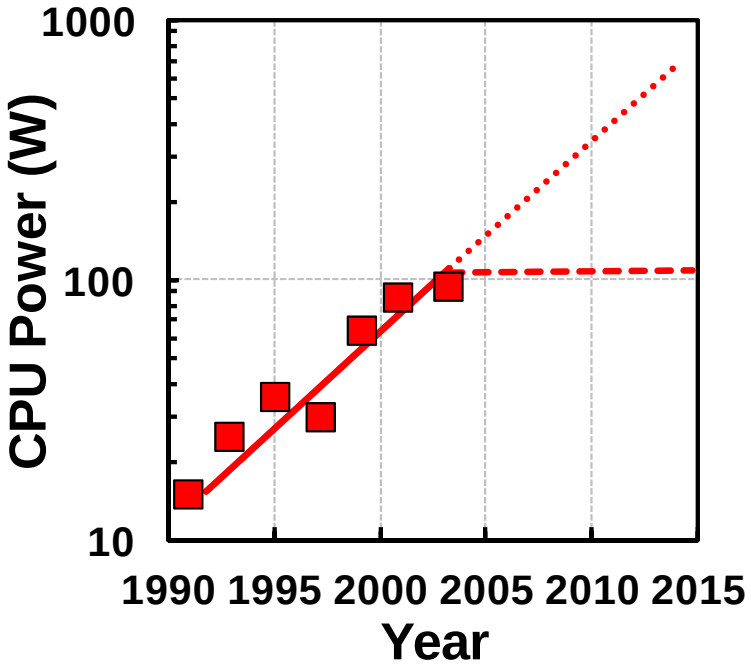



Figure 1-1. Power dissipation in CPU for various technologies as a function of the year of introduction (Source: Intel [3])

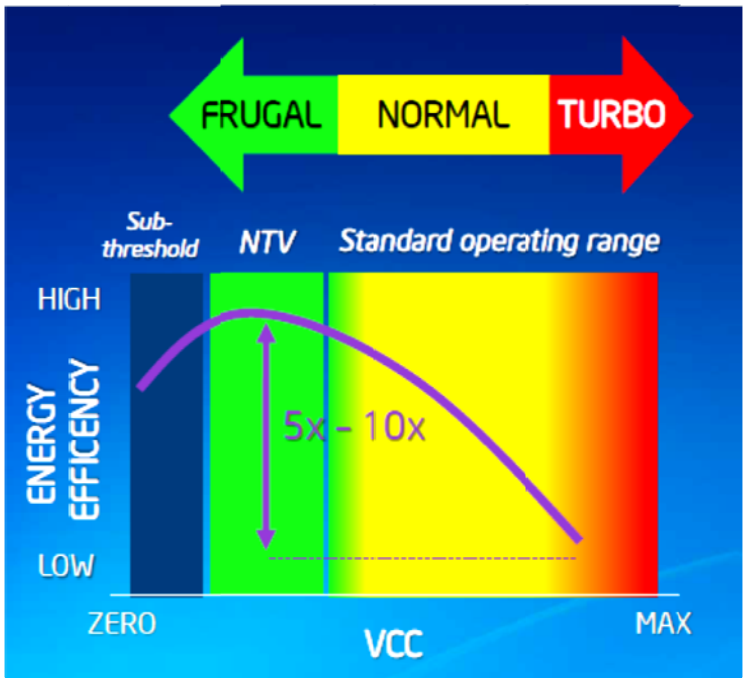



Figure 1-2. Transistor operating voltage range showing energy efficient computation for near threshold voltage operation. (Source: Intel Labs ISSCC [5])

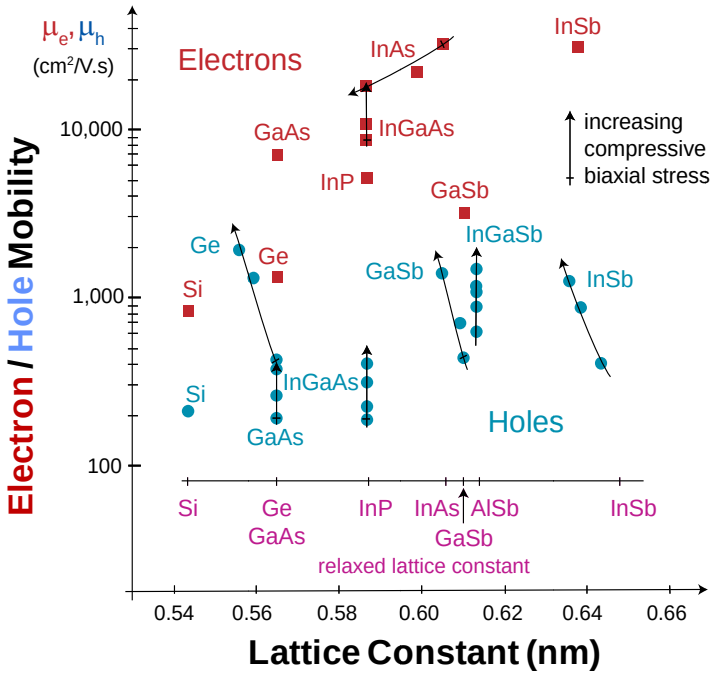



Figure 1-3. Electron and hole mobility of various III-V compound semiconductors (Source: del Alamo MIT [1]). Antimonides are very attractive since they have high electron as well as high hole mobility

## I. Motivation: Unified Material System with High Electron and Hole Mobility

Due to their unique material properties, antimony (Sb) based III-V materials (materials comprised of elements from group III and V of periodic table) are of strong interest as channel material for low power all-antimonide complementary metal-oxide-semiconductor (CMOS) digital logic. Sb-based MOSFETs (Metal-Oxide-Semiconductor Field Effect Transistors) can operate at high speed and very low supply voltage, which promises to dramatically lower the power dissipation in future high-speed logic circuits. Antimonide based materials have high electron as well as high hole mobility [6][7]. Figure 1-4 shows the electron mobility of InAsSb QW heterostructure along with that of Si NMOSFET. For inversion carrier density of the order of 3-4x$10^{12}$/$cm^2$, InAsSb QW layers have a mobility of about ~ 13000 $cm^2$/Vs, which is ~60x higher than that of Si NMOS inversion layers. This can give rise to a substantial improvement in drive current for InAsSb based devices which can help scale supply voltage to about 0.5V. Similarly if we compare the hole mobility of InGaSb quantum well heterostructure with that of Si PMOS, we see that for a hole density of about 2x $10^{12}$/$cm^2$, the InGaSb QW layers have ~7x higher hole mobility compared to Si PMOS inversion layers.

The antimonide NMOS and PMOS have similar lattice constants and they have a unified buffer which makes them very interesting. If we can integrate In AsSb QW NMOSFET and InGaSb QW MOSFET, we can envision a III-V complementary logic operating at low supply voltage. Figure 1-5 shows a schematic of Sb NMOS and PMOS integration for complementary logic operation.

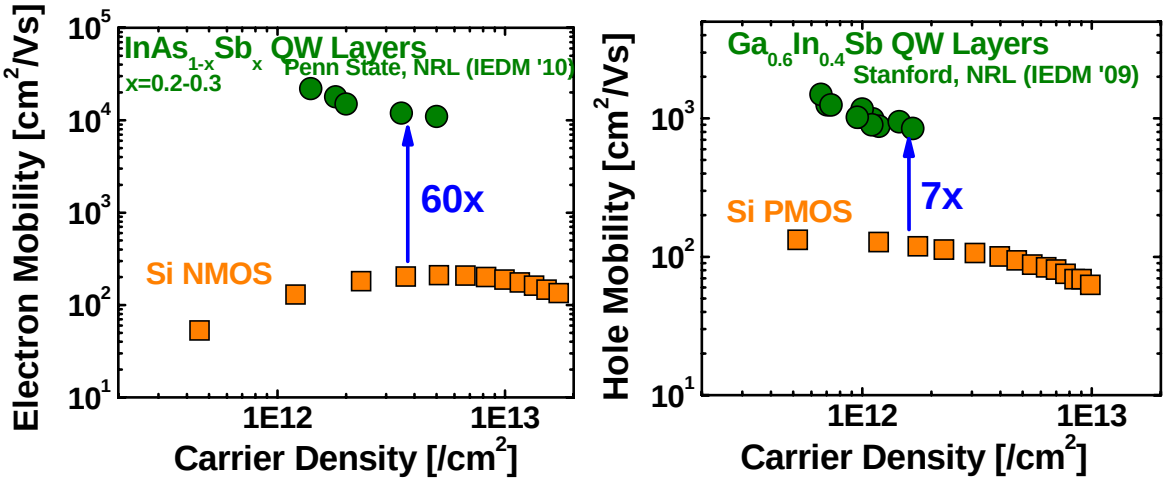



Figure 1-4. Electron mobility of InAsSb QW heterostructure layers compared to that of Si NMOS inversion mobility and the hole mobility of InGaSb QW layers compared to that of Si PMOS inversion layers

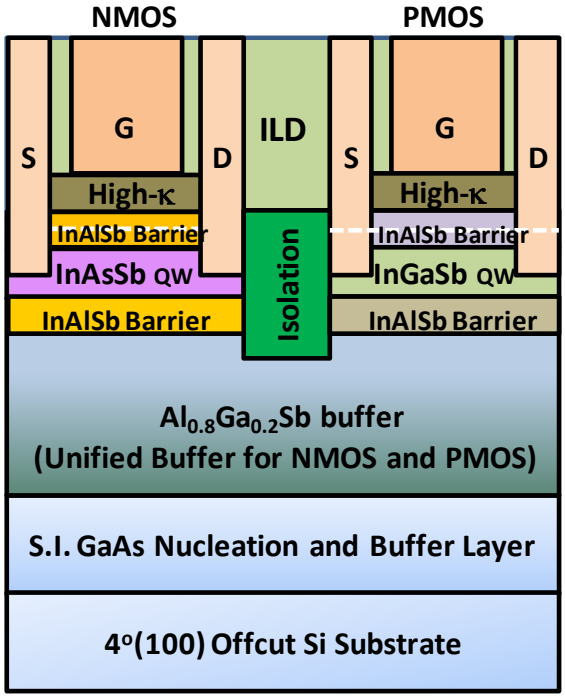



Figure 1-5. Schematic showing integration of InAsSb NMOS and InGaSb PMOS for III-V complementary logic operation

## II. Device Architecture of Sb QW MOSFET for Ultra-low $V_{DD}$ Logic

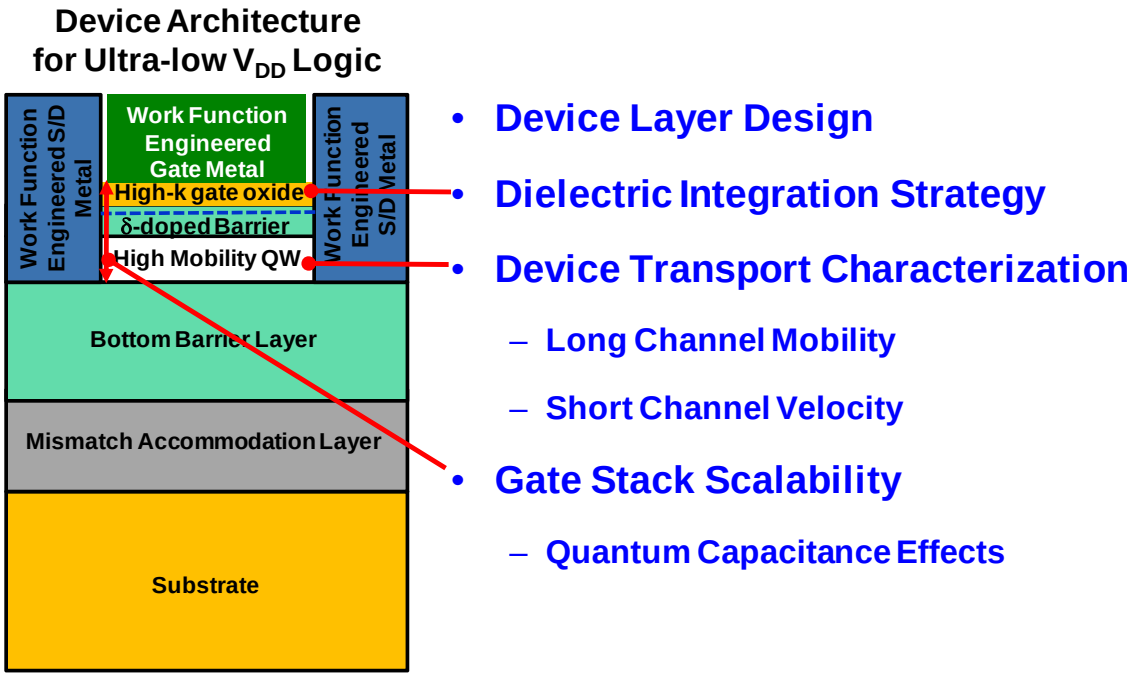



Figure 1-6. TEM micrographs of the $InAs_{0.8}Sb_{0.2}$ QWFET stack grown on GaAs by MBE and the defect free active device layers

Figure 1-6 shows a schematic of the quantum well MOSFET device architecture for ultra-low supply voltage operation. The high mobility quantum well is confined within an insulating barrier layer. The quantum well is remote doped using a delta-doping layer in the barrier to provide low resistance access regions for source drain contact. The device has a high quality high-k dielectric integrated on top of the barrier layer to reduce gate leakage, and a work function engineered gate metal to target threshold voltage.

In this dissertation, I address the feasibility of Arsenide-Antimonide channel materials to enable high-performance low-power logic computing. There are three main challenges which are key to demonstrating high performance transistors operating at low supply voltage, – (1) A good quality interface between the channel material and the gate oxide, which determines the standby

power dissipation in the device, (2) High drive current (current passed by the device when it is switched ON) which determines the switching speed of the device, and (3) Enhancement mode operation (device conducts only with the application of a gate voltage and is otherwise OFF), which is required for CMOS logic circuits.

This dissertation is organized as follows. In this chapter I, I will discuss about the device layer design for Sb NMOSFETs followed by the strategy for integrating a good quality high-k dielectric in chapter II. Device fabrication and characterization details are explained in chapter III. Chapter III concludes with benchmarking the device figures of merit of the Sb NMOS, particularly the long channel mobility and short channel effective velocity, with that of the standard strained silicon NMOS. Enhancement mode device characteristics are presented in chapter III. In chapter IV, I will discuss the quantum capacitance and band non parabolicity measurements and address the effects of quantum capacitance on gate stack scalability and performance of these devices. I will conclude this dissertation with the future works section in Chapter V. My research works show that antimonide transistors are really promising for high-performance low-power logic applications, if the key issues on gate stack quality and external resistance are addressed. For these devices to compete with the state-of-the-art Silicon tri-gate devices, the device architecture has to evolve from a planar to three-dimensional fashion, or a gate wrap-around structure

## III. Device Layer Design and Characterization

The device layer design for InAsSb quantum well MOSFET is shown in Figure 1-7. The device is metamorphically grown on GaAs since there is no lattice matched substrate for InAsSb. The quantum well is undoped and the $Al_{0.9}ln_{0.1}Sb$ barrier layer has been delta-doped with Te to provide carriers to the access regions. The device layers are grown by Dr. Brian Bennett at Naval

Research Lab, Washington DC. Figure 1-8 shows the TEM micrographs of the $InAs_{0.8}Sb_{0.2}$ QWFET stack grown on GaAs by MBE and the defect free active device layers There is ~9% lattice mismatch between the channel and the GaAsb substrate, which is accommodated as defects in the bottom buffer layer as seen from the cross-section TEM picture.

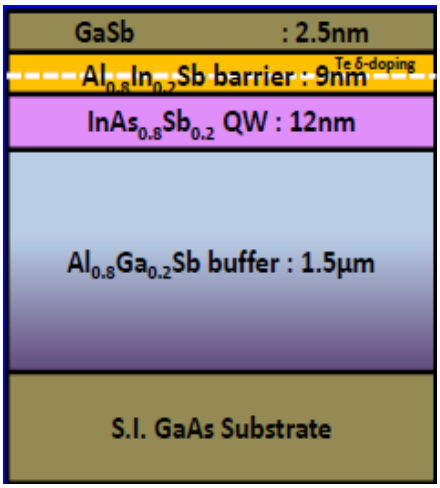



Figure 1-7. Schematic of the Sb QW MOSFET device layers

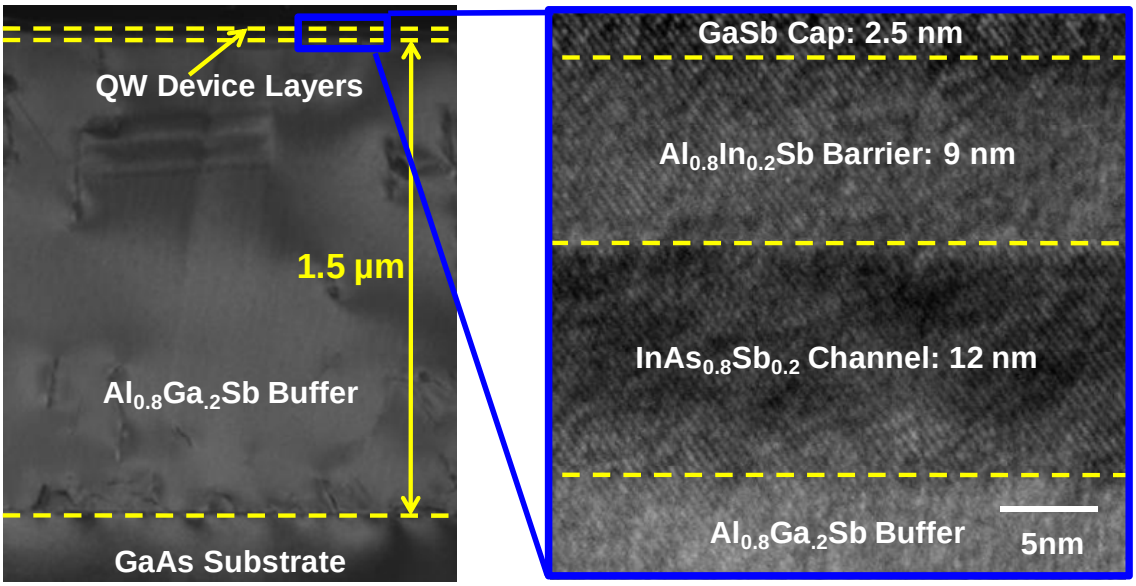



Figure 1-8. TEM micrographs of the $InAs_{0.8}Sb_{0.2}$ QWFET stack grown on GaAs by MBE and the defect free active device layers

The InAlSb barrier layer can have oxidation problems while depositing high-k dielectric. So I have introduced a thin layer of GaSb on the top to make a good interface with the dielectric. Incorporation of GaSb layer is a key difference that separates the Sb MOSFET structure from the previous HEMT works on antimonide systems [7]. The energy band diagram of the device in Figure 1-9 shows that the carriers are efficiently confined within the quantum well and that there is no carrier spill over to the barrier.

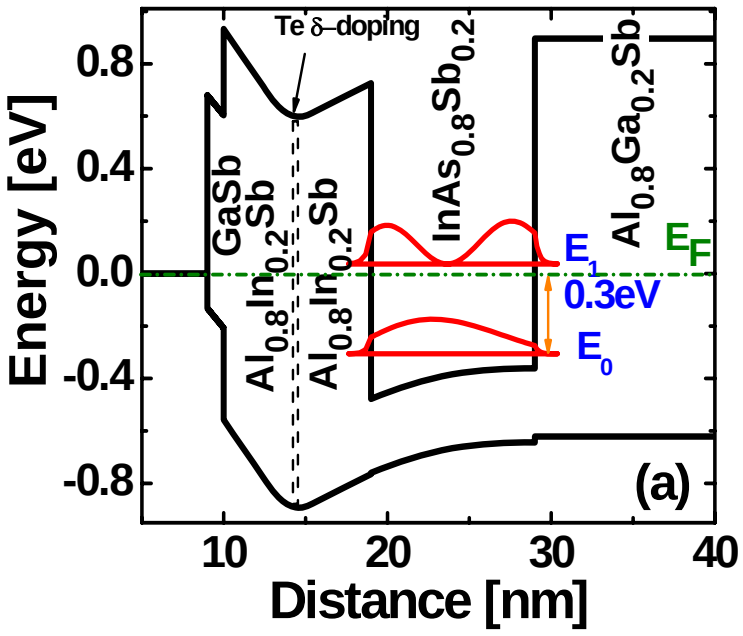



Figure 1-9. Energy band diagram of the InAsSb QWFET device layers showing carriers confined effectively in the QW with no carrier spill over to the barrier layer

As this structure is metamorphically grown on GaAs, it is important to see if there is any parallel conduction in the device layers due to defects at the material interface. So I studied the quantitative mobility spectrum analysis [8] of this device as a function of temperature to identify if the transport it confined to the Sb QW itself. In QMSA, the conductivity tensor of a Hall device is studied as a function of magnetic field. The sheet resistance and the hall resistance obtained from Hall measurements are converted to the conductivity tensor. By numerically solving the

conductivity tensor as a function of magnetic field, we can identify if there is multi-carrier transport in the device. Figure 1-10 shows the quantitative mobility spectrum analysis (QMSA) for the QW heterostructure obtained using magneto conductance measurements at various temperatures and under varying magnetic field. There is a large conductivity ratio between the majority carrier (electrons) and the minority carrier (holes) at all temperatures. The single dominant conductivity peak due to electrons indicates that there is no parasitic or parallel conduction through the barrier or the metamorphic buffer layers.

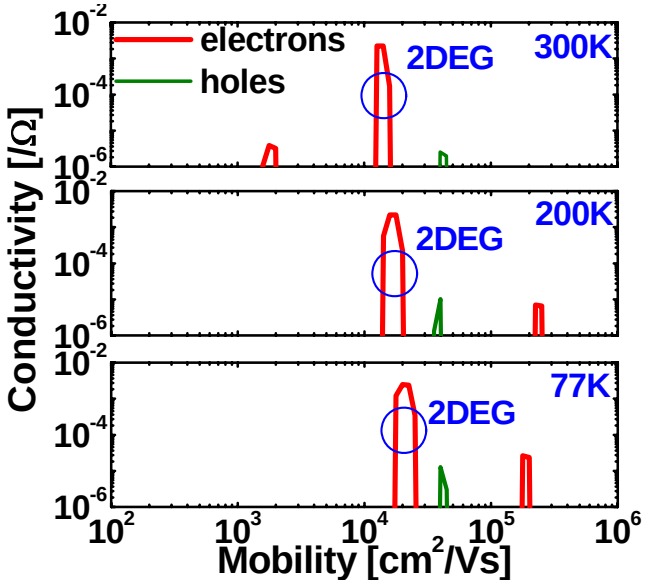



Figure 1-10. Quantitative mobility spectrum analysis (QMSA) for the QW heterostructure obtained using magneto-conductance measurements at various temperatures and under varying magnetic field

The as grown device layers exhibit an electron mobility of 13,000 $cm^2/Vs$ at 300K at carrier density of $2.2x10^{12}$ $/cm^2$. Figure 1-11 shows the measured and modeled Hall mobility as a function of temperature. The Hall mobility was modeled using various scattering mechanisms including acoustic deformation potential scattering, polar optical phonon scattering, remote ionized impurity scattering, alloy disorder scattering, interface roughness scattering, and coulomb scattering due to charge trapped at the barrier and channel interface. As can be seen from the

temperature dependence of the Hall mobility, the low temperature mobility is limited by interface charge scattering. This charge could be at the hetero interface of the InAlSb and InAsSb layers due to Tamm States arising from AlAs and InSb phase formation while growing an abrupt interface between the QW and barrier layer [9]. Figure 1-12 (a) shows the various parameters used in the modeling of scattering mechanisms, and Figure 1-12 (b) shows the percentage contribution of various scattering mechanisms toward 1/μ at room temperature. Coulomb scattering due to interface limits the electron mobility at room temperature.

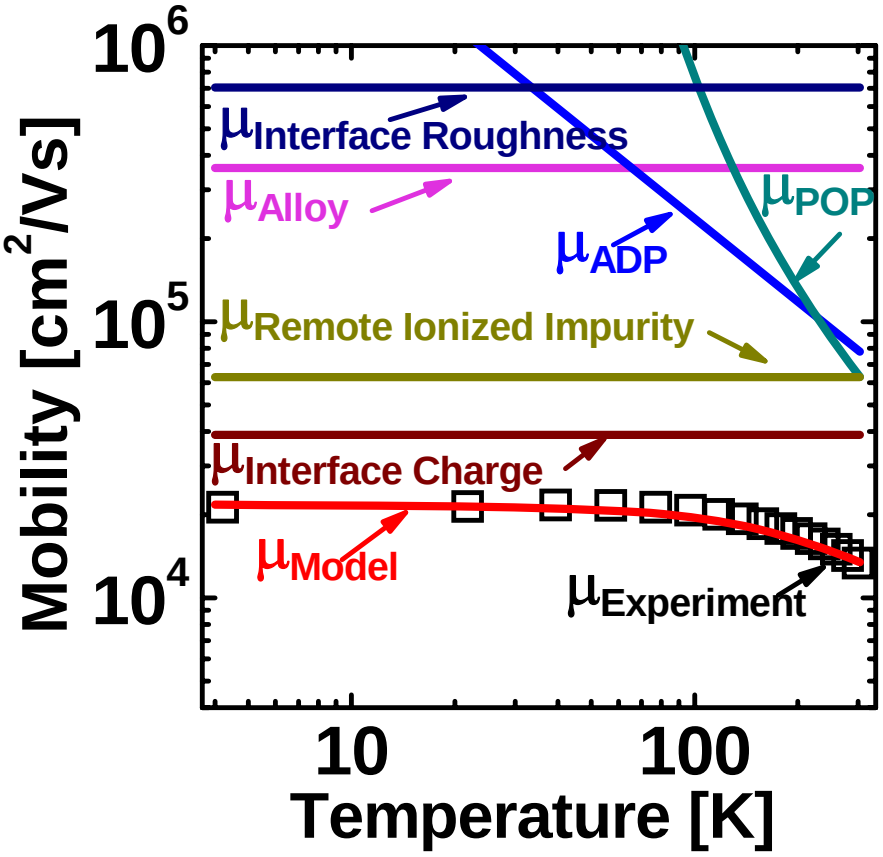
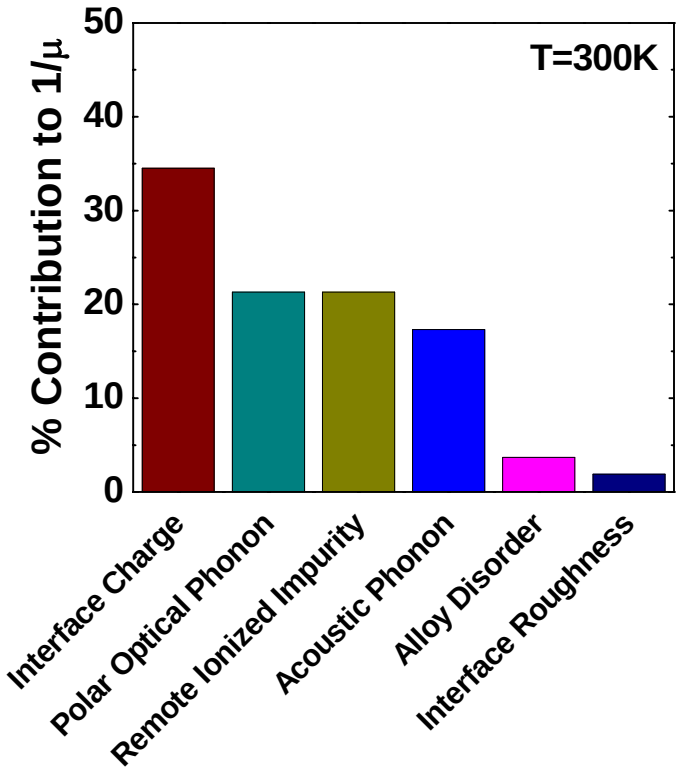



Figure 1-11. Hall mobility of the Sb QW device layer as a function of temperature from 4K-300K

| Parameter | Value |
|---|---|
| Acoustic Deformation Potential | 4.8 eV |
| Polar Optical Phonon Energy | 27.8 meV |
| Alloy Disorder Potential | 0.3eV |
| Interface Charge | $6x10^{11}/cm^2$ |
| Mean height of Roughness | 6.2Å($T_{QW}$=12nm), 6.8Å($T_{QW}$=7.5nm) |
| Correlation Length | 20nm |
| Remote Ionized Impurity | $1.8x10^{12}/cm^2$ |

(a)




(b)

Figure 1-12. (a) Parameters used for modeling the different scattering mechanisms (b) Percentage contribution of different scattering mechanisms to the 1/μ at room temperature showing the mobility is limited by Coulomb scattering due to interface charge

In summary, the Sb quantum well device layers have very high mobility and no parallel conduction, suitable for fabricating MOSFETs. A good quality dielectric is required to be integrated on these device layers to scale the device, which is discussed in the next chapter.

# Chapter 2

# Dielectric Integration Strategy

## I. Introduction

Integrating a high quality dielectric is key to demonstrating a scalable antimonide (Sb) quantum well (QW) MOSFET architecture for high performance low-power logic applications. The Sb QW MOSFET has $Al_yIn_{1-y}Sb$ as the barrier layer which is highly reactive. This has been one of the major obstacles in the development of antimonide based FETs. The aluminum containing barrier layer oxidizes very rapidly on exposure to air. The $Al_yIn_{1-y}Sb$ material increases in volume on oxidizing which would then lead to cracking and further oxidation of the entire epitaxial layer [10]. This oxidation of $Al_yIn_{1-y}Sb$ was observed by many researchers who worked on InAs-AlSb HEMTs [11][12][13]. Further the oxidation of InAlSb would leave behind oxides of aluminum (Al) and antimony (Sb), as well as metallic antimony at the surface. On forming an MOS (metal-oxide-semiconductor) gate stack on the $Al_yIn_{1-y}Sb$ barrier layer for making the Sb MOSFET, the native oxides ( of Al and Sb) and the metallic Sb species would give rise to interface traps, which then screen the gate potential from modulating the channel potential. If this happens, the charge in the Sb QW channel (or the Fermi level in the channel) cannot be modulated with the gate potential and this is called Fermi level pinning. I found out experimentally that an ultra-thin GaSb surface layer which caps the InAlSb barrier layer is more favorable toward high-κ dielectric integration than $Al_yIn_{1-y}Sb$ top barrier layer for the Sb MOSFET, as it avoids Al at the interface and the associated surface oxidation. Figure 2-1 shows the effect of surface passivation treatment with HCl (surface treatment prior to dielectric integration) on the Sb QW samples with and without the GaSb cap. The sample without GaSb cap

where the InAlSb surface was exposed to HCl showed pits uniformly throughout the sample due to oxidation of InAlSb, whereas the sample with the GaSb cap layer exhibited a smooth surface after HCl treatment. In this chapter, the electrical characteristics of high-k/GaSb semiconductor interface are carefully examined to evaluate its potential to be integrated on the Sb MOSFET.

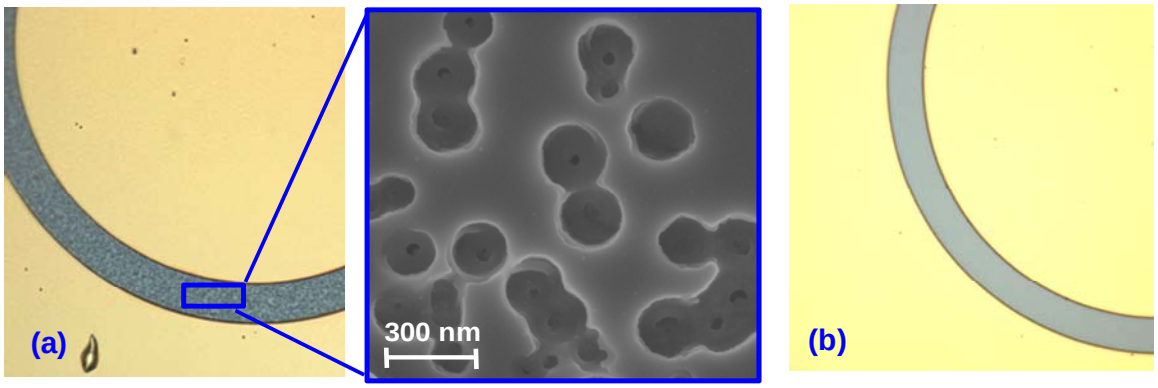



Figure 2-1. Optical micrograph of device layers after HCl surface treatment step on, (a) sample without GaSb cap (top InAlSb barrier layer is exposed to HCl), and (b) sample with GaSb cap

GaSb has a highly reactive surface and on exposure to air it will form a native oxide layer composed of $Ga_2O_3$ and $Sb_2O_3$ ($2GaSb + 3O_2 \rightarrow Ga_2O_3 + Sb_2O_3$). The $Sb_2O_3$ can further react with the GaSb surface forming elemental Sb and $Ga_2O_3$ ($Sb_2O_3 + 2GaSb \rightarrow Ga_2O_3 + 4Sb$) [14][15]. Chemical treatments based on HCl are effective in removing native oxides on GaSb [15][16]. I studied the effects of HCl treatment on the capacitance-voltage characteristics (C-V) and the surface chemistry of n-type and p-type GaSb (100) MOS capacitors with $Al_2O_3$ dielectric fabricated using both Atomic Layer Deposition (ALD) and Plasma Enhanced ALD (PEALD) techniques. PEALD was employed to reduce the thermal budget of dielectric deposition, particularly important for antimonide based semiconductors. In this chapter, I demonstrate an unpinned Fermi level in GaSb

MOS system with a high-κ PEALD $Al_2O_3$ dielectric, using temperature resolved admittance spectroscopy and monochromatic X-ray photoelectron spectroscopy (XPS) analysis.

## II. GaSb MOS Capacitor Fabrication

### ALD vs Plasma Enhanced ALD

Atomic layer deposition (ALD) has widely been used to form high quality dielectrics for the gate stack of MOS transistors. In the ALD process, the substrate is exposed to a metal organic compound for a certain period of time. The metal organic adsorbs to the surface of the substrate uniformly. This step is followed by an inert gas purge step which will evacuate the chamber of any unreacted precursor. A second precursor or reactant is now purged for a short period of time which then reacts with the adsorbed metal organic species on the surface forming a high quality conformal thin film on the surface. To form a high quality thin film during the reaction between the metal organic and the reactant, the temperature of the substrate is kept high. Typically higher temperatures are preferred for film growth. However very high temperatures would lead to desorption of the metal organic species already adsorbed on to the substrate. A suitable temperature of growth is preferred which gives rise to a good quality dense film while maintaining a conformal coating of metal organic.

In the case of antimonide semiconductors, it is desired to reduce the temperature of dielectric deposition to prevent the oxidation of GaSb to $Ga_2O_3$ and metallic Sb [16]. Figure 2-2 shows compares the conventional ALD process with a new Plasma Enhanced ALD (PEALD) process in which the inert gas purge is replaced with a weak oxidant gas like $CO_2$, which acts as the oxidant when the plasma is pulsed. Since the reaction is plasma assisted it helps to lower the

deposition temperature. More details on the PEALD process can be obtained in [17]. A schematic representation of the sequence of steps in the ALD and PEALD processes is shown in Figure 2-3.

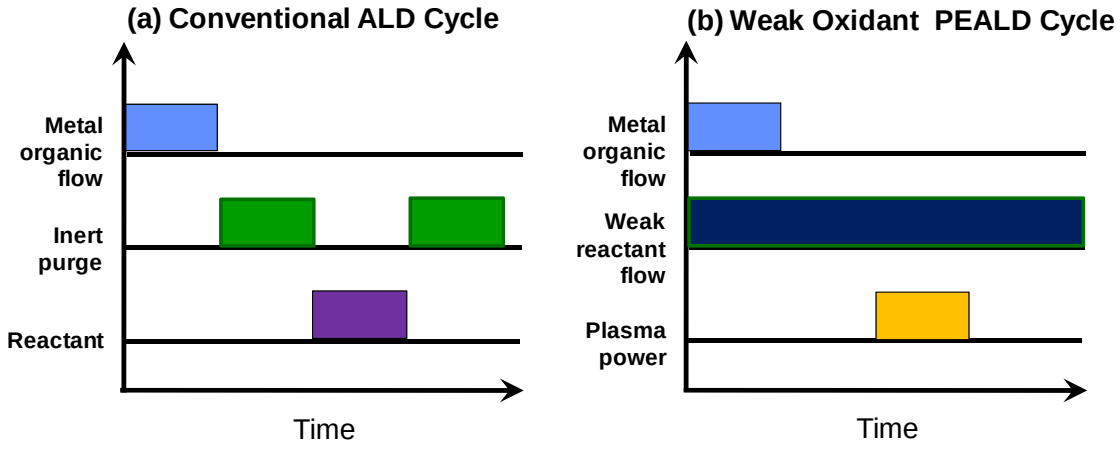



Figure 2-2. Schematic of (a) conventional ALD process with a strong reactant, and (b) Weak oxidant PEALD process with a pulsed plasma sequence to form the oxide

## III. Results and Discussion

### C-V/G-V Characterization of GaSb MOS Capacitors

Both n-type and p-type GaSb (100) MOS capacitors were fabricated with high-κ $Al_2O_3$ gate dielectric. The samples were degreased in acetone and ethanol for 5 min each and rinsed in isopropyl alcohol (IPA). The degrease step was followed by a dip in concentrated HCl (HCl : $H_2O$ = 1:2) for 5 min to remove surface oxides followed by an IPA rinse. GaSb MOS capacitors were fabricated with $Al_2O_3$ deposited by ALD at 300$^oC$ from trimethylaluminum (TMA) and water or by PEALD at 200$^oC$ from TMA and $CO_2$. Pt/Au gate metallization was done using electron beam evaporation after defining gate patterns using optical lithography. Pd/Au backside

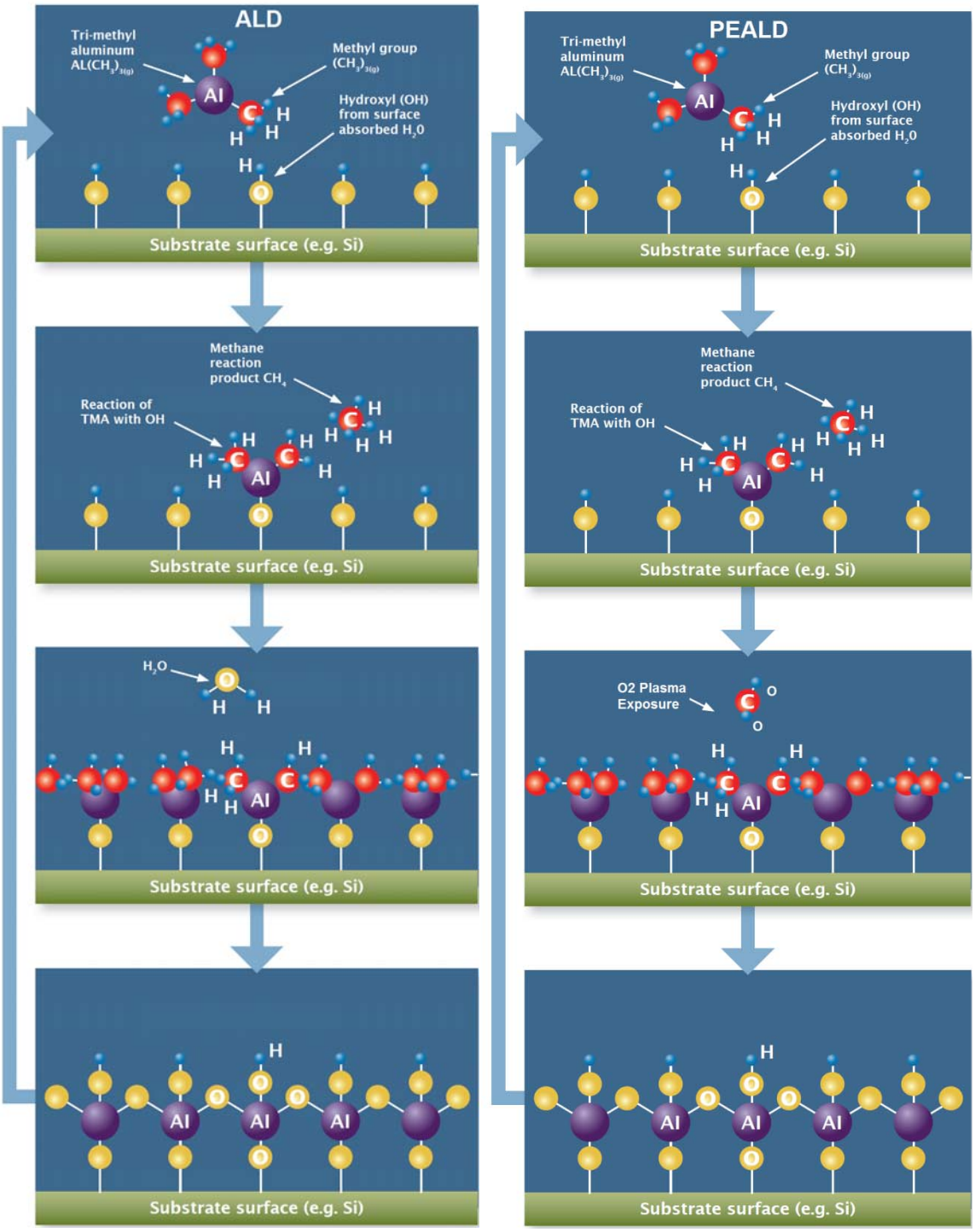



Figure 2-3. Schematic illustration of the thin film deposition process using ALD and PEALD (Source: Cambridge Nanotech Corporate Brochure June 2010.)

ohmic contacts were deposited using electron beam evaporation. No post deposition anneal was done for any of the samples.

Capacitance voltage (*C-V*) and conductance voltage (*G-V*) measurements were obtained with HP 4285A precision *LCR* meter. Figure 2-4 shows the C-V measurements on ALD $Al_2O_3$/n-GaSb and PEALD $Al_2O_3$/n-GaSb MOS capacitors. The ALD sample shows weakly pinned C-V characteristics with very fast interface trap density ($D_{it}$) response whereas PEALD sample demonstrates good Fermi level modulation. The accumulation side of *C-V* characteristics for the PEALD sample shows the effect of high $D_{it}$ near conduction band and the negative bias regime shows the effect of inversion response along with a low $D_{it}$ response. The accumulation side of the admittance data is analyzed using the standard depletion/accumulation model [18] and the inversion side using the model introduced in [19]. The circuit model in inversion accounts for the supply of minority carriers through bulk thermal generation and diffusion across the space charge layer along with interface state contribution, which enables accurate modeling of the admittance data in inversion. Figure 2-5 shows *C-V* characteristics of the ALD $Al_2O_3$/p-GaSb and PEALD $Al_2O_3$/p-GaSb samples with HCl treatment for different temperature. The ALD sample shows strongly pinned *C-V* characteristics with both accumulation and inversion regimes completely dominated by interface states. For the PEALD sample, there is minimal dispersion of capacitance in accumulation due to less $D_{it}$ near the valence band whereas the inversion response shows contributions from minority carriers as well as high $D_{it}$ near the conduction band. The 200K *C-V* shows a clear Fermi level movement from accumulation to depletion for the PEALD sample whereas ALD sample exhibits pinned *C-V* characteristics.

*C-V* measurements for the n-type (p-type) MOS capacitors were done at 300K and 250K (300K and 200K). The reason is that the backside contact (Pd/Au) on GaSb is ohmic for holes whereas it forms a Schottky barrier for electrons (~ 0.6 eV Schottky barrier height for electrons due to the Fermi stabilization energy in GaSb being ~0.1eV from valence band as mentioned in

[20]. This Schottky barrier gives rise to higher contact resistance for electrons at lower temperatures, which causes frequency dispersion in the accumulation capacitance of the n-type MOSCAPS.

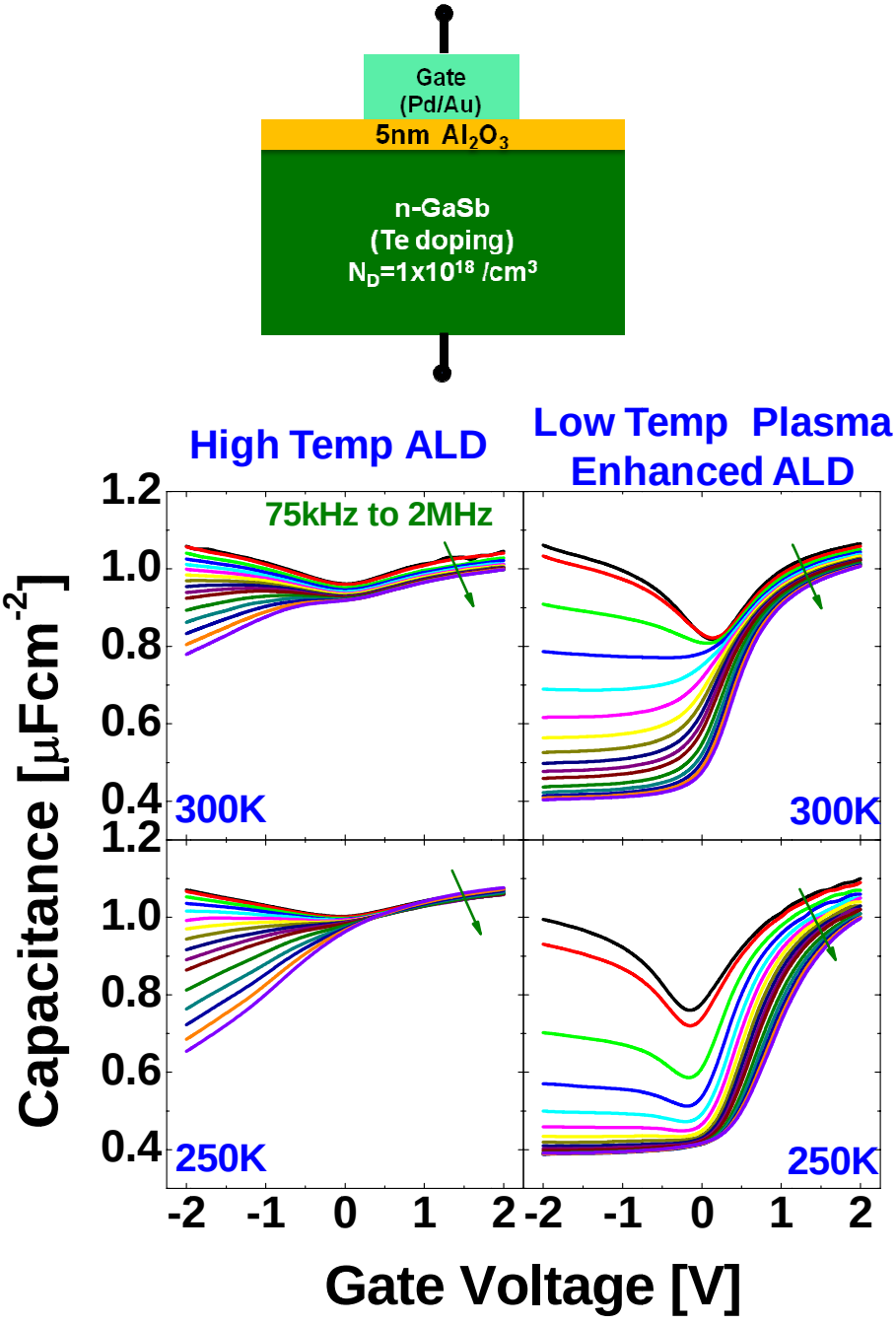



Figure 2-4. *C-V* characteristics as a function of frequency of n-type ALD and PEALD MOS capacitors with HCl treatment. Measurement temperature is indicated in the figure.

For the p-type devices this is not a problem as the contacts are ohmic for holes, and the measurement can be done at very low temperature. Hence, to avoid parasitic series resistance in the measurement, the above measurement temperatures were employed

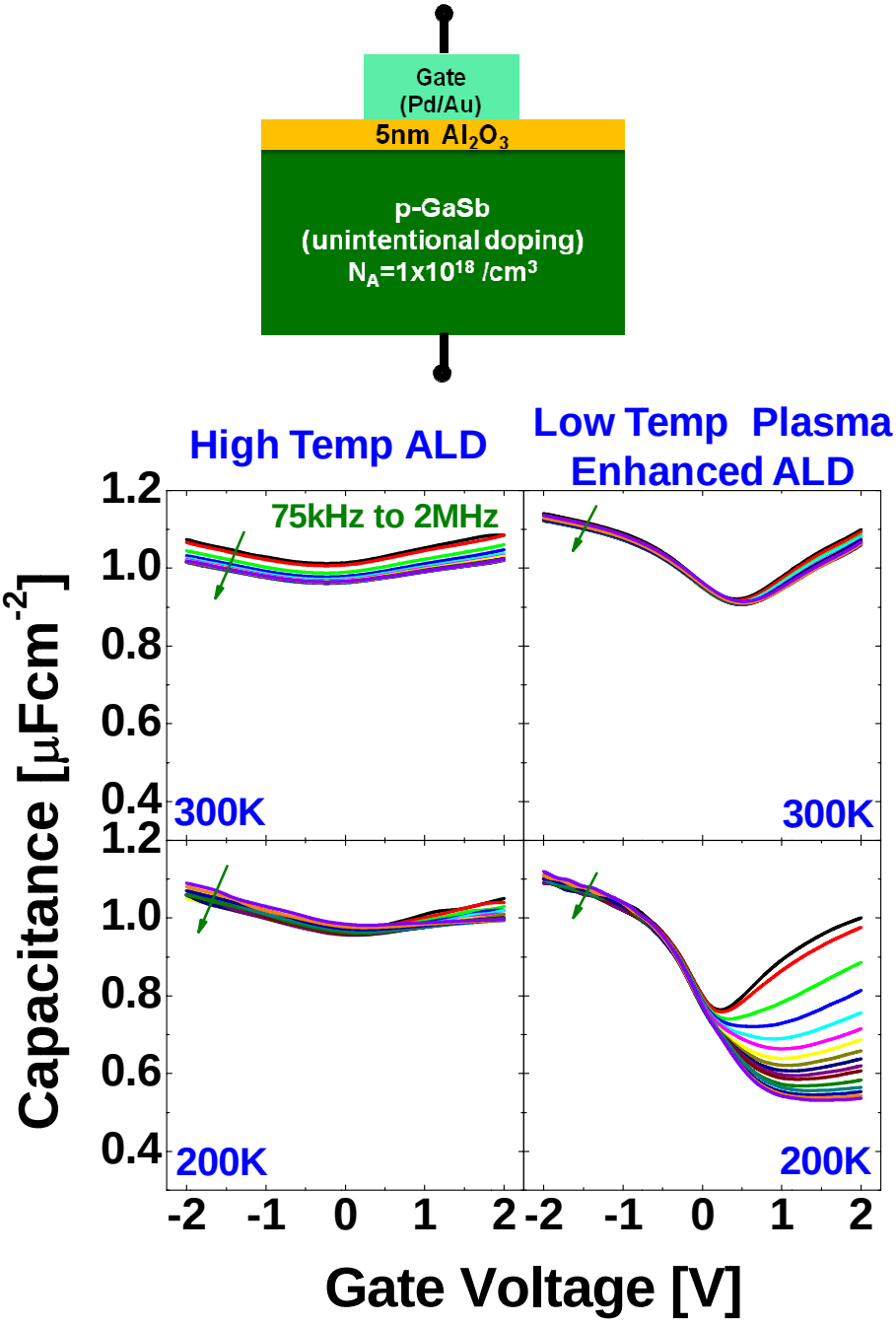



Figure 2-5. *C-V* characteristics as a function of frequency of p-type ALD and PEALD samples with HCl treatment. Measurement temperature is indicated in the figure.

Figure 2-6 shows the conductance contour map ($G/\omega$) of n-type and p-type PEALD samples as a function of gate voltage and small-signal frequency. The V-shaped trajectory of the peak value of conductance, $(G/\omega)_{peak}$, along the frequency axis shows that the Fermi level moves freely on either side of the midgap of GaSb. PEALD $Al_2O_3$/GaSb samples demonstrate an unpinned Fermi level at the interface, even though the Fermi stabilization energy for GaSb is 0.1eV from valence band [20].

$$\tau_e = \left(N_c \sigma v_t\right)^{-1} \exp(\Delta E / kT)$$

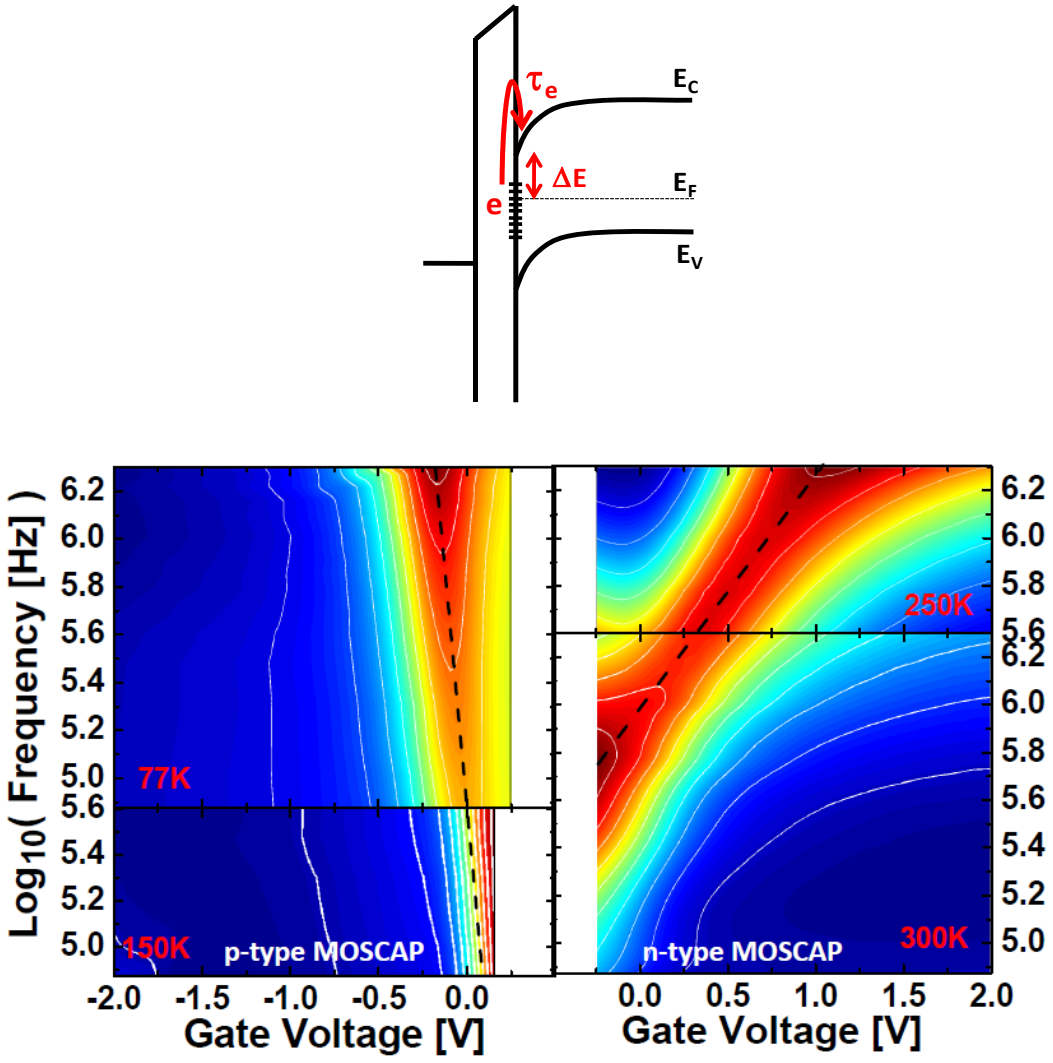



Figure 2-6. Conductance ($G/\omega$) contours of n-type and p-type GaSb MOSCAPs with PEALD $Al_2O_3$ showing good Fermi level modulation towards valence and conduction band sides.

The extracted capture cross section values are $9\times10^{-15}$ $cm^2$ for traps near valence band and $8\times10^{-19}$ $cm^2$ for traps near conduction band, indicating that the traps near the valence band are faster than those near the conduction band. Hence, the conductance plots were done at lower temperature for the p-type samples where the conductance peaks were visible. The capture cross section values are consistent with [21], where irradiated p-type GaSb showed acceptor type traps near the valence band with higher capture cross-section.

**Interface Chemical Analysis with X-ray Photoelectron Spectroscopy (XPS)**

Figure 2-7 shows the monochromatic XPS analysis of the Sb 4*d* region for the ALD and PEALD samples with HCl treatment. XPS measurements were done in collaboration with Dr. Bob Wallace's group at UTD and more details on the XPS measurement system can be found in [22]. All PEALD and ALD samples show presence of Ga-oxides. The ALD samples show no detectable Sb-oxides where as the PEALD samples have significant Sb-oxides. As mentioned before, $Sb_2O_3$ reacts with GaSb forming $Ga_2O_3$ and elemental Sb: $Sb_2O_3 + 2GaSb \rightarrow Ga_2O_3 + 4Sb$ [15]. The kinetics of this reaction is enhanced at higher temperatures>200$^oC$ [23]. Enhanced thermal desorption of Sb-oxides are also anticipated at such temperatures [24]. The ALD, which was done at 300$^oC$, could therefore result in significant formation of elemental Sb, thereby reducing the available $Sb_2O_3$. In contrast, the PEALD was done at 200$^oC$ where the reduction is significantly suppressed. The 4*d* orbital binding energy of elemental Sb (Sb-Sb) is similar to that for GaSb. Hence, due to the $Al_2O_3$ thickness, it is difficult to conclude whether the PEALD samples are free from elemental Sb. It is possible that the Fermi level, $E_F$, unpinning for PEALD samples is due to the absence of elemental Sb at the $Al_2O_3$/GaSb interface. Further, the absence of water in PEALD, coupled with low thermal budget, leads to a better quality interface.

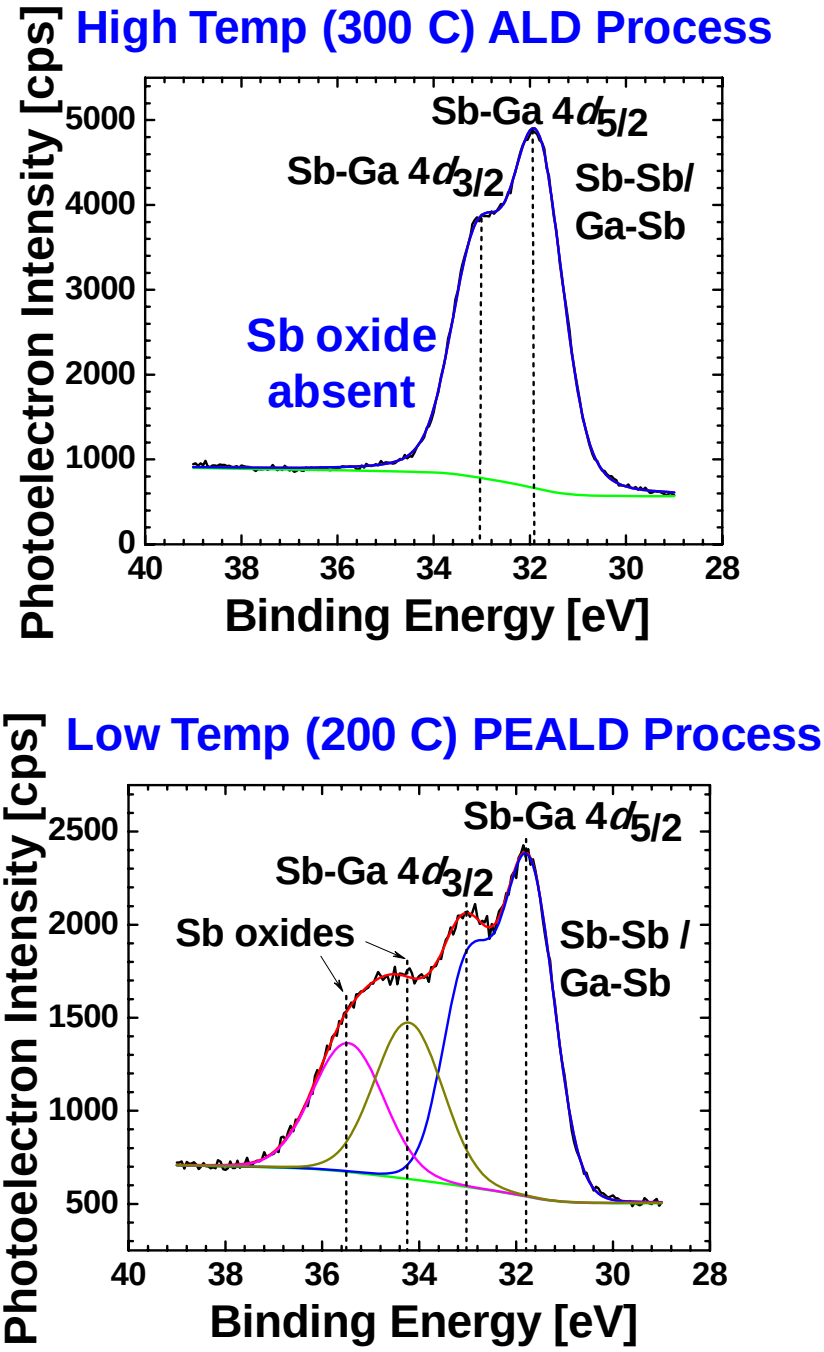



Figure 2-7. XPS data comparing the concentration of $Sb_2O_3$ in ALD and PEALD samples. Reduction of $Sb_2O_3$ in the (higher temperature) ALD samples is evident.

Finally, F was detected in all samples by XPS and is attributed to reactor O-ring decomposition. The role of F remains a topic of investigation.

**Fermi Level Unpinning of GaSb MOS Capacitors**

Figure 2-8 shows the $D_{it}$ extracted from multi-temperature *C-V / G-V* analysis of the n-type and p-type GaSb MOSCAPs using the admittance modeling technique mentioned in [18]. Band diagrams showing the positions of Fermi level at the GaSb interface for the range of operation of the Sb QW MOSFET is also shown in Figure 2-8. For the range of operation of the Sb QW MOSFET, the Fermi level at the GaSb interface sweeps from the valence band towards midgap where the $D_{it}$ is relatively low.

Figure 2-9 shows the Fermi level movement efficiency of the ALD and PEALD samples. Fermi level movement efficiency is defined as the ratio of the change in the Fermi level at the oxide-semiconductor interface in the presence of $D_{it}$ to the change in Fermi level without $D_{it}$, for a unit applied gate voltage. Mathematically, it can be represented as:

$$\mathrm{E_F\ movement\ efficiency} = \frac{(\delta\psi_s / \delta V_g)with\ D_{it}}{(\delta\psi_s / \delta V_g)ideal}\% = \frac{1 + C_{dep}/C_{ox}}{1 + (C_{dep} + C_{it})/C_{ox}}\% \qquad (1)$$

The PEALD sample with HCl pretreatment shows a 90% $E_F$ movement efficiency near the valence band. This makes it suitable for integration with Sb QW MOSFET, where the Fermi level sweeps near the valence band of GaSb.

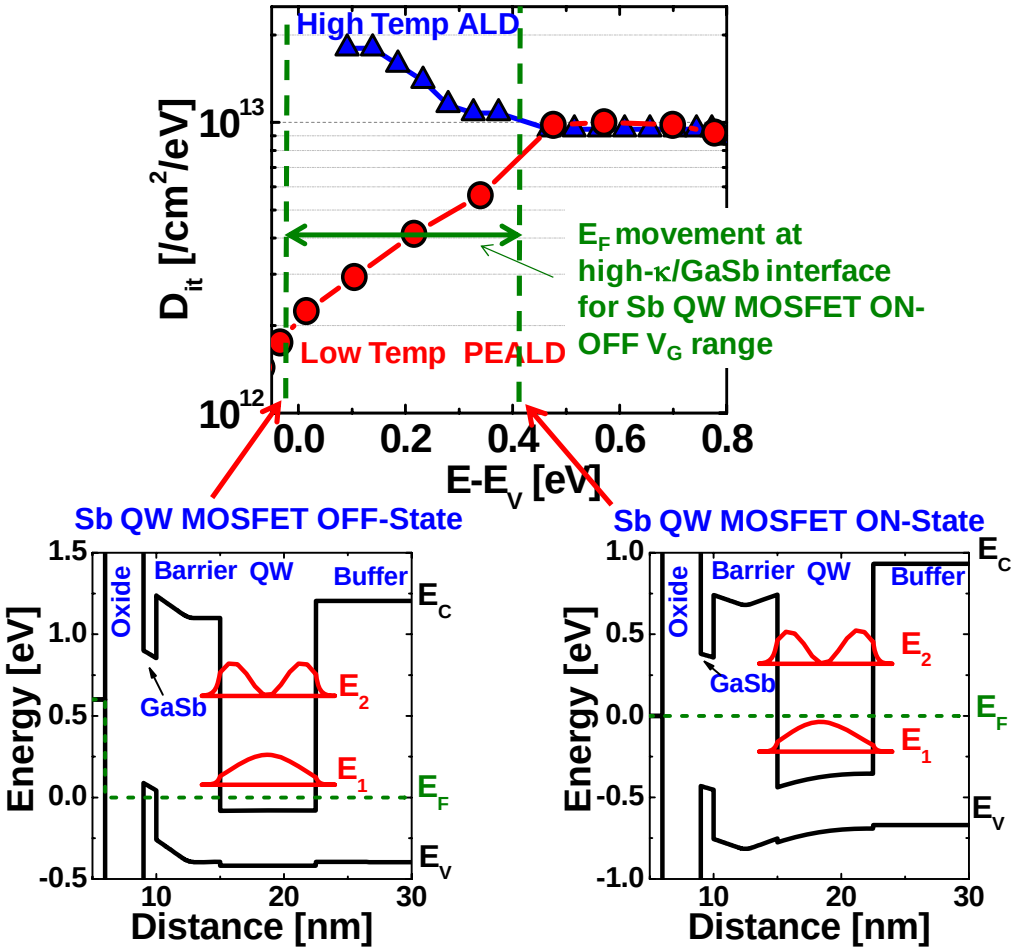



Figure 2-8. Extracted $D_{it}$ from multi-temperature *C-V/G-V* analysis of n and p type GaSb MOSCAPs showing low $D_{it}$ near $E_V$ for PEALD $Al_2O_3$/GaSb interface. Fermi level movement at the GaSb interface for the range of operation of the Sb QW MOSFET is also shown.

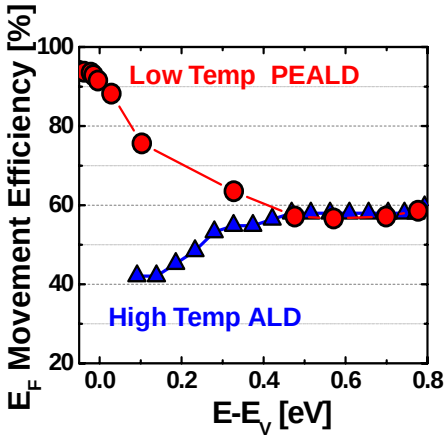



Figure 2-9. Fermi level movement efficiency of GaSb MOSCAPs with ALD and PEALD $Al_2O_3$

I have also studied the *C-V* characteristics of GaSb samples with ALD $Al_2O_3$ deposited at a lower temperature (250°C). A bilayer oxide stack with 1nm $Al_2O_3$ and 5.5nm $HfO_2$ was investigated. The bilayer stack was introduced to enable gate stack scaling. The *C-V* characteristics as shown in Figure 2-10 exhibited much better gate modulation (i.e. higher $C_{max}/C_{min}$ ratio) compared to the 300°C ALD sample, and is comparable to the *C-V* characteristics of the low temperature PEALD $Al_2O_3$ process (200 °C). This is due to the reduced amount of elemental Sb formation at 250°C. The $D_{it}$ extracted from multi-temperature *C-V/G-V* analysis is shown in Figure 2-11. The 250°C ALD sample has comparable $D_{it}$ profile as the 200°C PEALD process, but has slightly higher $D_{it}$ than the PEALD process. I also speculate that the oxide anions in the plasma during the PEALD process may more efficiently oxidize the elemental Sb back to $Sb_2O_3$. I have investigated lower temperature ALD process ($Al_2O_3$ at 200°C), which exhibited unpinned *C-V* characteristics (not shown here) similar to the ALD 250°C process, however the gate leakage currents in those devices where higher. This could be due to non-uniform nucleation of the metal organic during the ALD growth process.

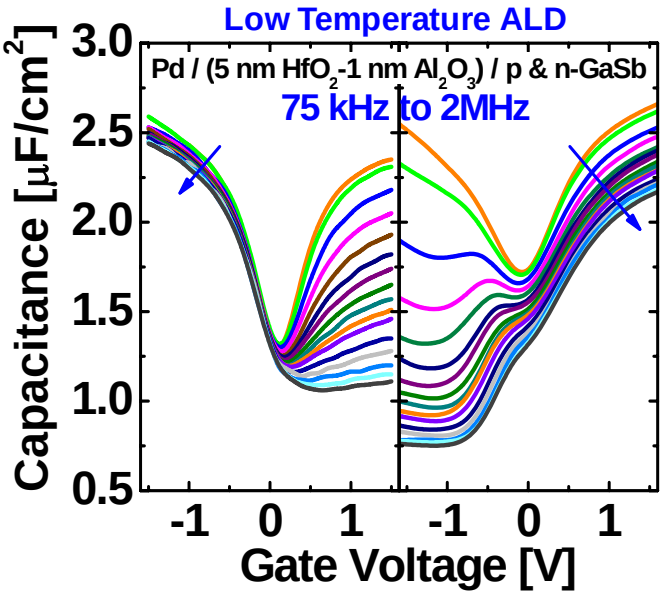



Figure 2-10. *C-V* of n and p type GaSb MOS capacitors with 1nm $Al_2O_3$ - 5.5 nm $HfO_2$ dielectric stack deposited using low temperature (250 C) ALD process

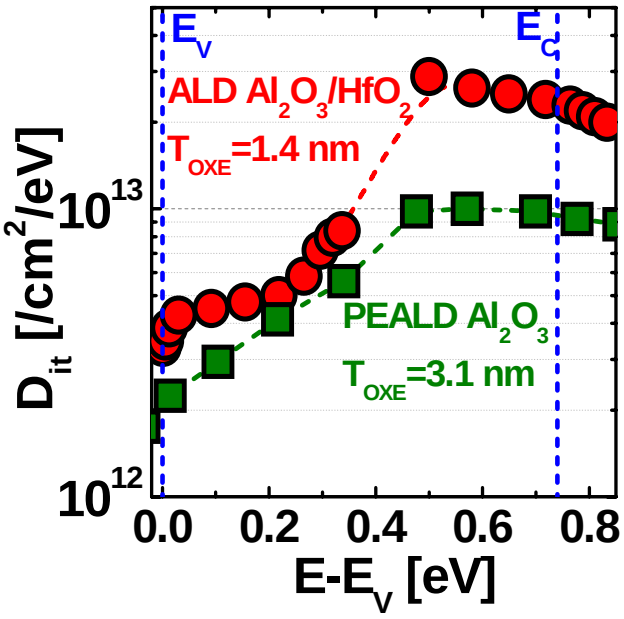



Figure 2-11. Extracted $D_{it}$ from multi-temperature C-V/G-V analysis of n-type and p-type GaSb MOSCAPs showing low $D_{it}$ near valence band for both low temperature ALD and low temperature PEALD process.

**Band Alignment of GaSb with $Al_2O_3$**

XPS measurements were used to determine the conduction and valence band offsets of $Al_2O_3$ with GaSb. These measurements were done in collaboration with Mozhe Eiseberg's group at Technion Institute, and are mentioned in detail in [25]. The bandgap of $Al_2O_3$ was first determined from the O 1s core level spectrum. The energy loss of O 1s photoelectrons for thick 20 nm $Al_2O_3$ film is shown in Figure 2-12. The energy loss region is shown in the inset where the difference between the middle of the peak and the beginning of the energy loss region (shown in inset of Figure 2-12) gives the bandgap energy. The obtained energy bandgap value is 6.5 eV which is consistent with literature. The valence band offset of $Al_2O_3$ relative to GaSb is obtained from the difference in energy between the valence band spectra of $Al_2O_3$ and GaSb as shown in Figure 2-13. The obtained valence band offset is 3.4 eV±0.2 eV. The conduction band offset is now calculated from the band alignment noting that $\Delta E_C + \Delta E_C + E_{g,GaSb} = Eg, AlO_3$. The obtained

$\Delta E_C$ was 2.4±0.1 eV. A schematic of the band alignment of $Al_2O_3$ with GaSb is shown in Figure 2-14.

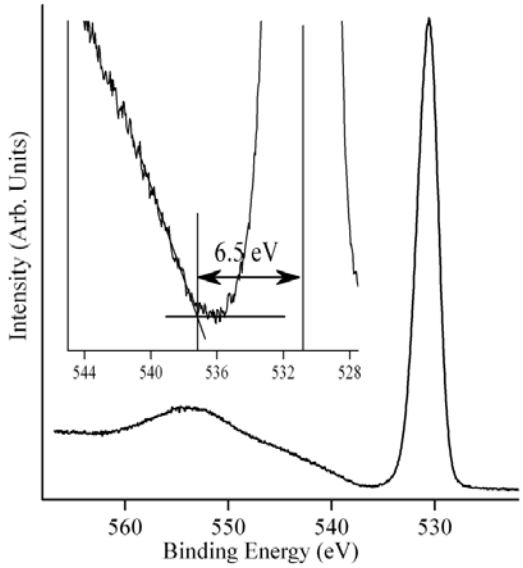



Figure 2-12. O 1s energy-loss spectrum for 20 nm $Al_2O_3$ film. The inset is a magnified region of the energy loss spectrum.

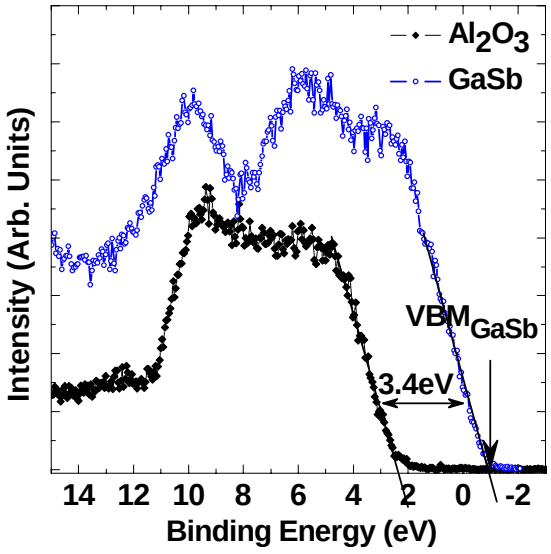



Figure 2-13. Valence band spectra of $Al_2O_3$ and GaSb (More details of the band offset determination procedure is reported in [25].

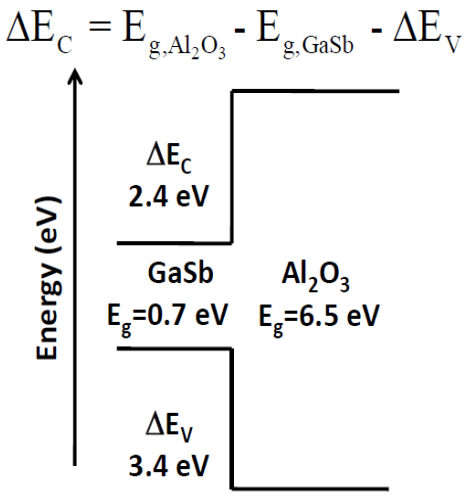



Figure 2-14. Schematic band alignment of $Al_2O_3$ with GaSb

GaSb/$A_2O_3$ interface has a symmetric conduction and valence band alignment reduces both electron and hole leakage. Figure 2-15 shows the leakage current density as a function of gate voltage for GaSb MOS capacitors with $Al_2O_3$, which gives very low gate leakage for all ranges of applied bias.

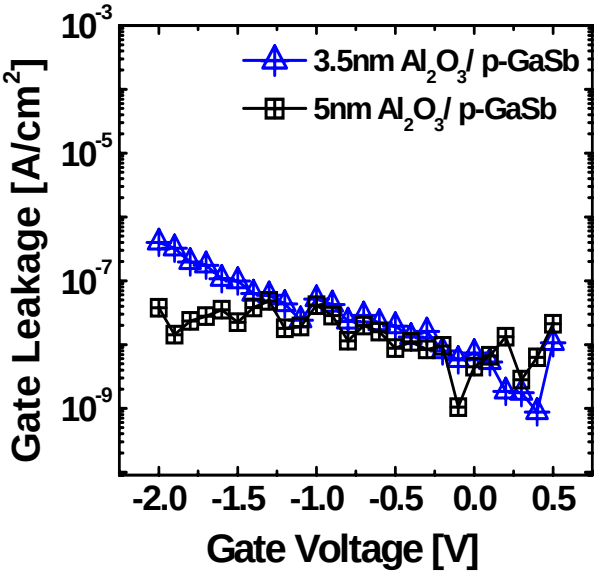



Figure 2-15. Gate leakage of GaSb MOS capacitors with $Al_2O_3$

## IV. Conclusions

In summary, I have demonstrated GaSb MOS capacitors (p-type and n-type) with unpinned Fermi level using PEALD $Al_2O_3$ by minimizing elemental Sb at the GaSb/$Al_2O_3$ interface. The reduction of $Sb_2O_3$ to metallic Sb is suppressed with PEALD due to lower deposition temperature, which is confirmed by XPS analysis. The $D_{it}$ is low near the valence band which makes GaSb-PEALD $Al_2O_3$ a good interface for composite barrier design with $Al_yIn_{1-y}Sb$ and $Al_yGa_{1-y}Sb$ barrier layers in mixed-anion QW MOSFETs for ultra-low power logic applications. Further, the GaSb/$Al_2O_3$ interface has a symmetric band alignment which reduces both electron and hole leakage.

# Chapter 3

# Antimonide MOSFET Fabrication and Characterization

## I. Introduction

$InAs_xSb_{1-x}$ quantum-well (QW) heterostructure with high electron mobility integrated with high hole mobility strained $In_xGa_{1-x}Sb$ QW, can potentially enable III-V CMOS and share the same metamorphic buffer on Silicon (Figure 3-1) [26]. With the exception of recent $In_{0.7}Ga_{0.3}As$ QWFET with high-κ gate stack [27], nearly all QWFETs, reported to date, use Schottky gate and suffer from high gate leakage. For further scaling, a gate stack is needed for integration with $InAs_ySb_{1-y}$ QWFET, with low EOT and $J_{OX}$, good interface properties and high carrier mobility in the channel. Here, I integrate a composite high-κ gate stack ($Al_2O_3$-$HfO_2$-GaSb) with $InAs_{0.8}Sb_{0.2}$ QWFET, resulting in high performance transistors operating at 0.5V $V_{DS}$. In this chapter, I report $InAs_{0.8}Sb_{0.2}$ NMOSFETs with integrated high-κ dielectric, which exhibit record high long channel electron mobility, short channel electron velocity and high-frequency small-signal performance, for the first time. The effects of interface trap density ($D_{it}$) which degrades the DC drive current and transconductance ($g_m$) is studied in detail using pulsed I-V and radio frequency (RF) measurements.

This chapter describes the fabrication flow of the $InAs_{0.8}Sb_{0.2}$ NMOSFETs with integrated high-κ dielectric followed by the long channel and short channel device characterization. The chapter concludes with enhancement mode Sb MOSFET design which is required for logic operation and identifies the key improvement areas required for performance enhancement in these devices.

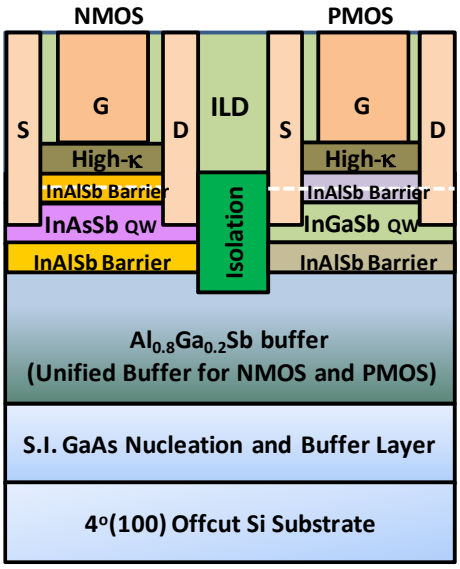



Figure 3-1. Schematic of Sb CMOS with common buffer technology, highlights the vision of low power, high speed Sb CMOS

## II. Device Fabrication

Figure 3-2 shows the schematic of the process flow for fabricating the Sb nMOSFET. Pd/Pt/Au metal stack was alloyed to form embedded contacts making direct ohmic contact with the QW [28]. Device isolation was done using $Cl_2$/Ar based reactive ion etching (RIE) followed by deposition of 1 nm $Al_2O_3$ – 10 nm $HfO_2$ bi-layer oxide stack employing low temperature ALD process. The device layers were treated in dilute HCl (1HCl: $20H_2O$) for 20 sec prior to gate dielectric deposition. The devices received a 15 min post deposition anneal (PDA) at 200C in forming gas ambient to densify the dielectric and reduce the interface and bulk defects. Pd/Au gate metal was defined using e-beam lithography and lift off process. Devices with gate lengths from 20 μm to 150 nm were fabricated. Figure 3-3 shows the schematic of $InAs_{0.8}Sb_{0.2}$ nMOSFET with 1 nm $Al_2O_3$/10 nm $HfO_2$ high-κ gate dielectric and a tilted view SEM of a device with 150 nm $L_G$ and source-to-drain separation of 500 nm.

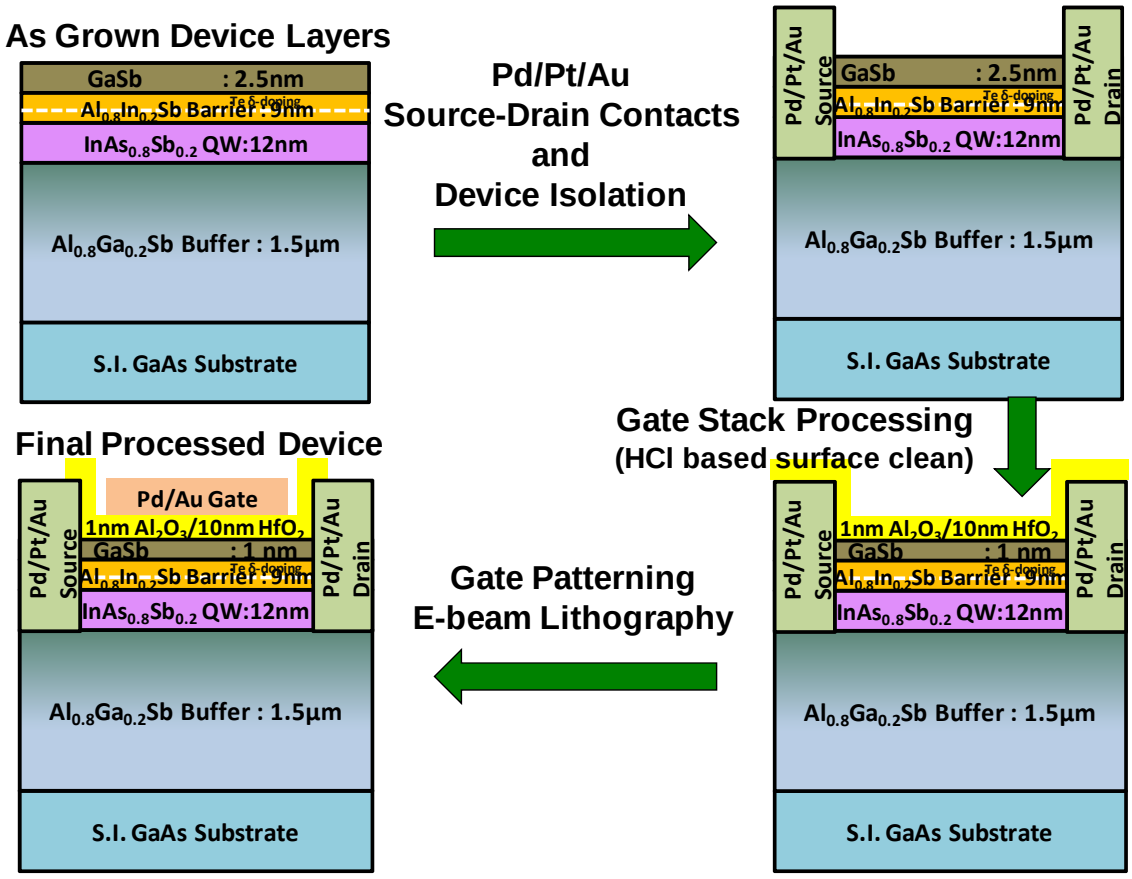



Figure 3-2. Schematic showing the process flow for fabricating the Sb NMOSFET

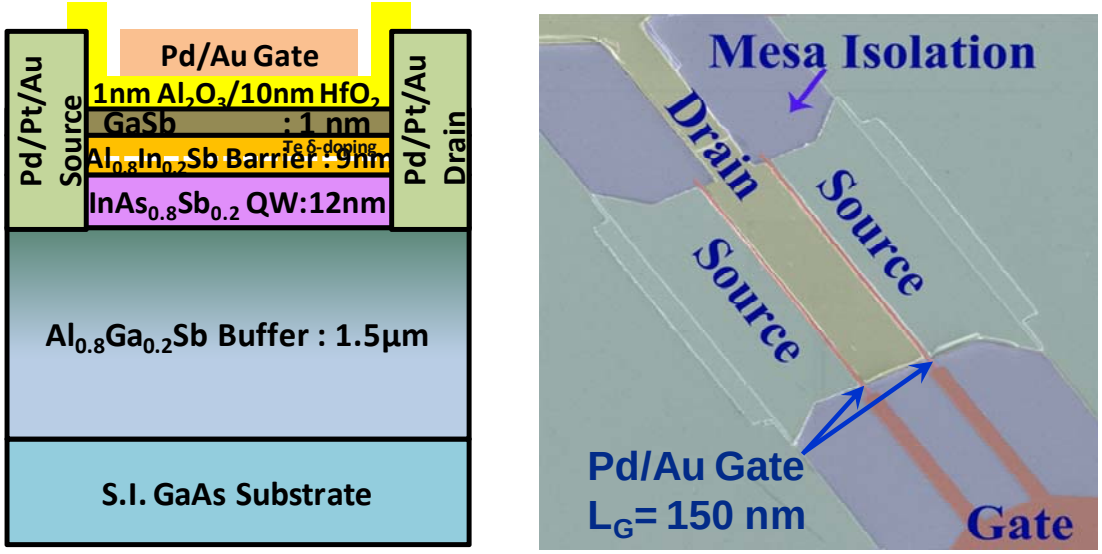



Figure 3-3. Schematic of the Sb NMOS with 1nm$Al_2O_3$/10nm $HfO_2$ dielectric, and tilted view SEM image of the fabricated device with 150nm $L_G$ and 500nm source-to-drain spacing

## III. Results and Discussion

### Development of a Scaled Gate Stack for Antimonide MOSFETs

A high quality gate stack is needed for integration with $InAs_xSb_{1-x}$ QW, with low EOT and $J_{OX}$, excellent interface properties and high carrier mobility in the channel. I use an ultra-thin (1nm) GaSb cap layer on top of the upper barrier for dielectric integration, to prevent oxidation of the $In_{0.2}Al_{0.8}Sb$ barrier layer. Using ALD $Al_2O_3/HfO_2$ bilayer dielectric on n and p type GaSb, I demonstrated MOSCAPs with unpinned Fermi level across gap and scaled EOT (Figure 3-4). The extracted $D_{it}$ is low towards valence band of GaSb which results in good nMOS turn off, while the high $D_{it}$ from midgap to conduction band can affect drive current.

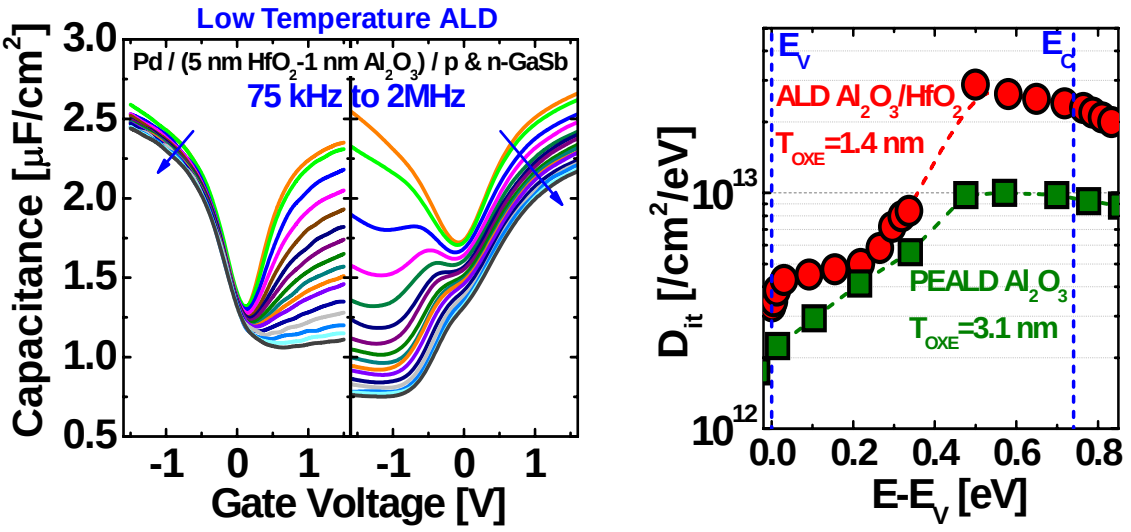



Figure 3-4. *C-V* of n and p type GaSb MOS capacitors with 1nm $Al_2O_3$ - 5.5 nm $HfO_2$ dielectric stack deposited using low temperature (250 °C) ALD process, and the Extracted $D_{it}$ from multi-temperature *C-V/G-V* analysis of n-type and p-type GaSb MOSCAPs

### DC Characterization

Figure 3-5 and Figure 3-6 show the transfer and output characteristics of Sb nMOSFETs with 5 μm, 450 nm and 150 nm gate lengths. The long channel devices exhibit good $I_{ON}$-$I_{OFF}$ ratio

and excellent saturation in the output characteristics. Contact resistance limits the drive current and degrades the output saturation for the 150 nm $L_G$ device which has an $I_{DSAT}$ of 450 µA/µm at $V_{DS}$ of 0.75 V. The sub-threshold characteristics and short channel effects degrade as $L_G$ is scaled, due to the non-optimized barrier and oxide thickness and the thick quantum well structure (EOT=4.5nm). Scaling of the device (oxide and the quantum well) is required to maintain electrostatic integrity of the devices.

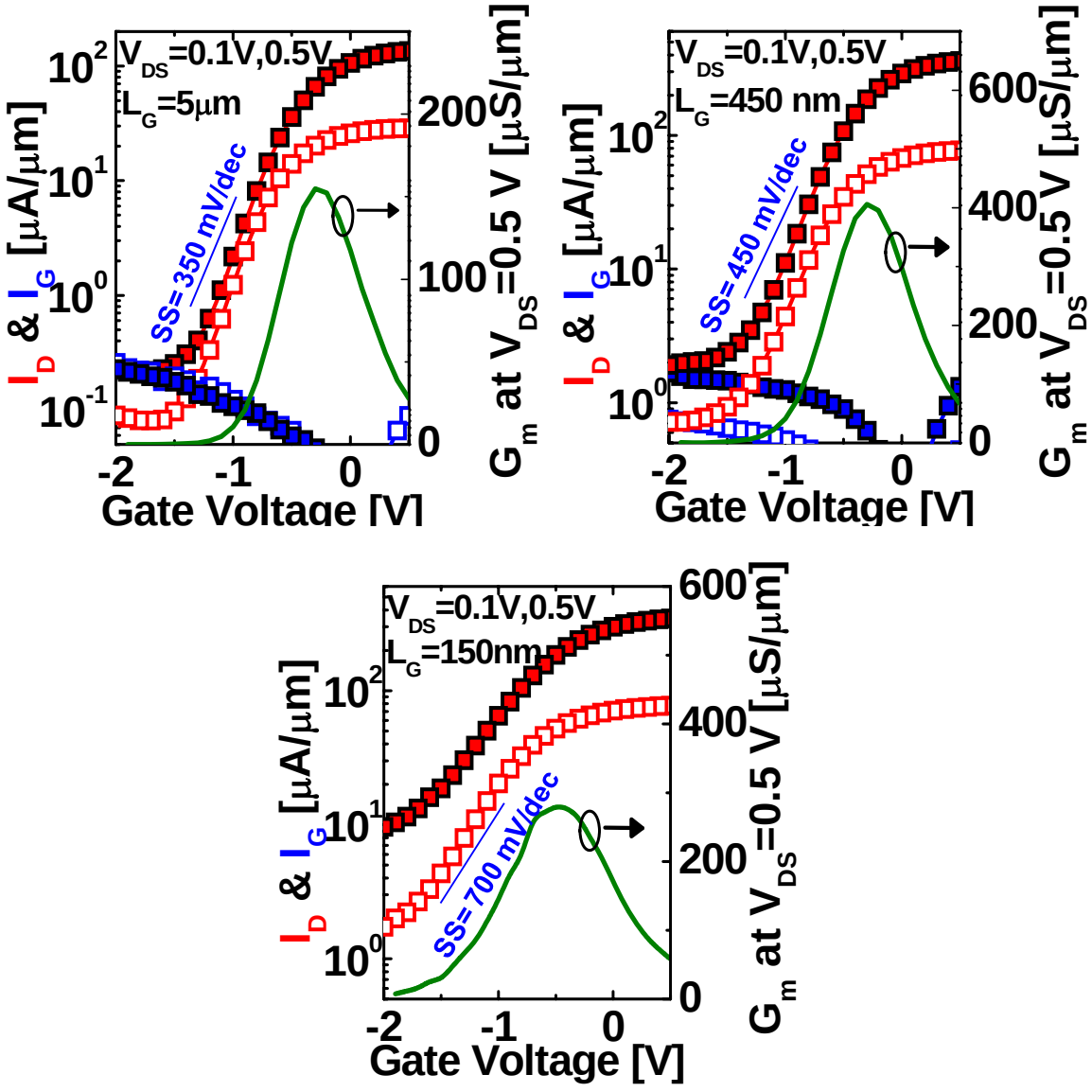



Figure 3-5. Transfer characteristics of Sb nMOSFETs with 150nm, 450nm and 5µm gate lengths

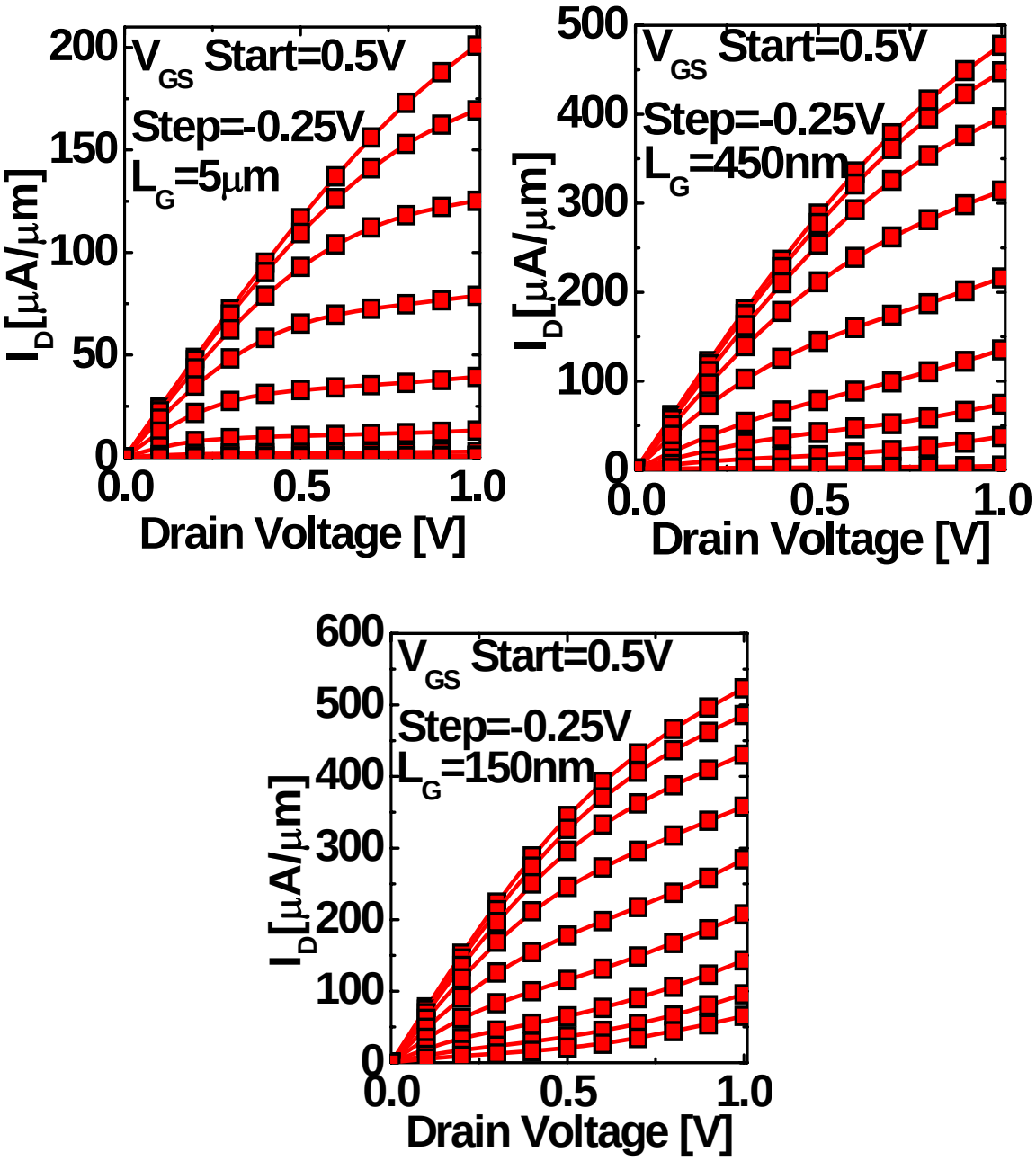



Figure 3-6. Output characteristics of Sb nMOSFETs with 150nm, 450nm and 5μm gate lengths

**Long Channel Device Characterization**

Figure 3-7 shows the electron drift mobility extracted from the output conductance and measured *C-V* characteristics. Here, I report a record high effective electron mobility of 6,000 $cm^2/Vs$ at $2x10^{12}$ $/cm^2$ of $N_s$, which is 15x higher than Si NMOS inversion layer mobility and 3x higher than that of InGaAs NMOS [29]. The Sb NMOSFET electron mobility is 2.2x lower than the Hall mobility (13,500 $cm^2/Vs$ at a carrier density of $2.2x10^{12}$ $/cm^2$) for the as-grown device layers without dielectric. This could be due to the overestimation of channel charge from split *C-V* measurements due to interface traps ($D_{it}$), as well as due to scattering from remote phonons in the high-κ dielectric or surface charge at the oxide-GaSb interface [30]. Figure 3-7Figure 3-8 (a) shows the measured and simulated split *C-V* characteristics of $L_G$=20μm device. The stretch-out in the measured *C-V* compared to the simulated *C-V* is due to interface traps ($D_{it}$). The procedure to obtain an ideal *C-V* including the quantum capacitance of the Sb QW will be explained in detail in the next chapter.

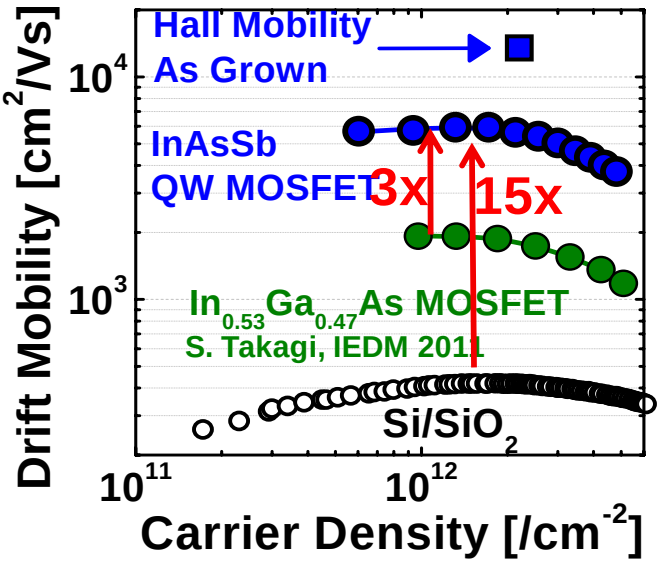
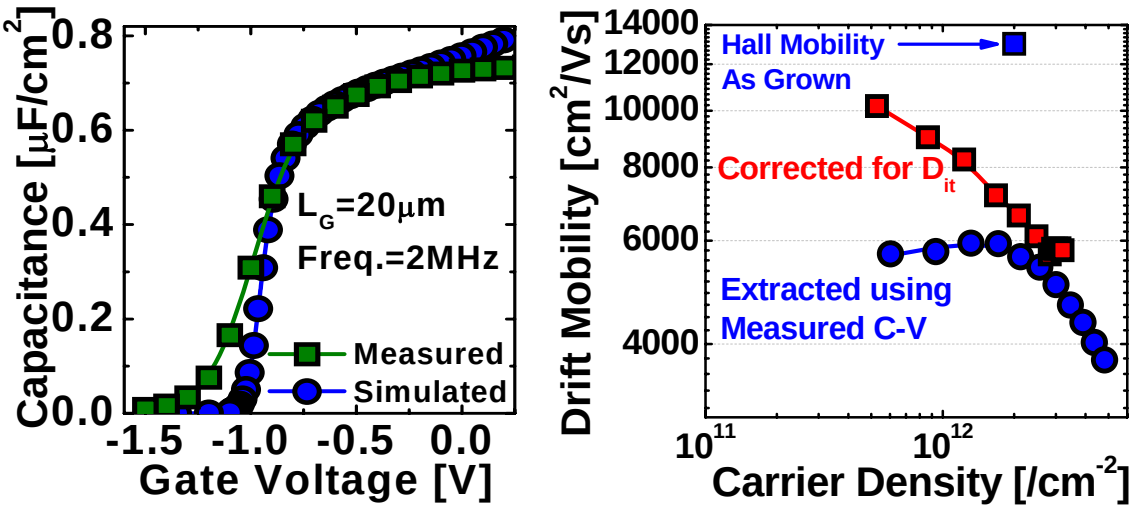



Figure 3-7. Extracted drift mobility vs $N_s$ showing record high mobility




(a) (b)

Figure 3-8. (a) Measured and modeled split C-V characteristics, and (b) Drift mobility extracted using measured *C-V* characteristics and the corrected mobility accounting for stretch-out due to $D_{it}$

By mapping the measured high frequency *C-V* with the simulated *C-V*, the real charge density in the channel can be obtained which is devoid of any interface trapped charge [31]. Using this, a corrected mobility is obtained as a function of charge density. Figure 3-8 (b) shows the as measured mobility and the mobility curve corrected for interface trapped charge. The corrected mobility is ~20% higher than the measured drift mobility at a charge density of $2x10^{12}$ /cm$^2$. However this is still 1.8x lower than the Hall mobility of as grown device layers. I think that this is due to scattering from remote phonons in the high-κ dielectric or surface charge at the oxide-GaSb interface.

The charge trapping effect of $D_{it}$ is further investigated in detail using pulsed IV and RF measurements. A schematic explaining the traps at the oxide GaSb interface capturing electrons from the gate leakage current is shown in Figure 3-9. The source for the trapped charge comes from the gate leakage current or through the Schottky emission of carriers from the source-drain contacts to the surface GaSb layer (the reacted Pd/Pt/Au contact makes a Schottky barrier with

the GaSb surface layer). The estimated trap response time is in the range of 0.5 to 2 μs. This means that if the gate voltage is pulsed with a pulse-width in the range of ~1 μs, it will prevent most of the interface states from trapping charge at the interface. This will give rise to enhanced carrier density in the channel and an enhancement in current. I chose 2 μs pulse widths for our experiments due to system and cable limitations in obtaining narrower pulse widths.

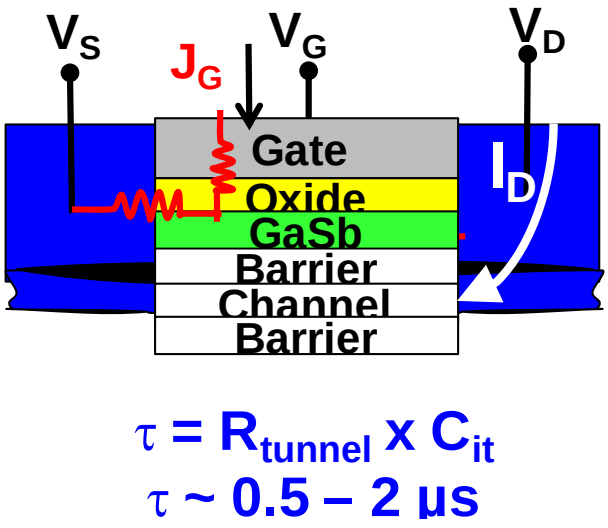



Figure 3-9. Schematic showing traps at the oxide GaSb interface capturing electrons from the gate leakage current. Estimated trap response time is in the range of 0.5 to 2μs.

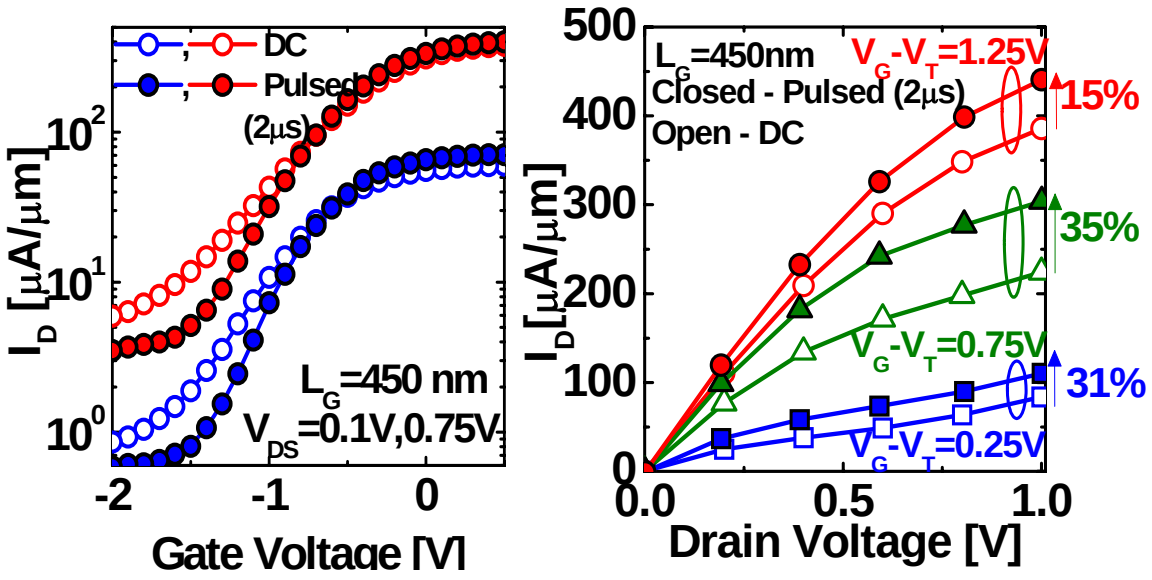
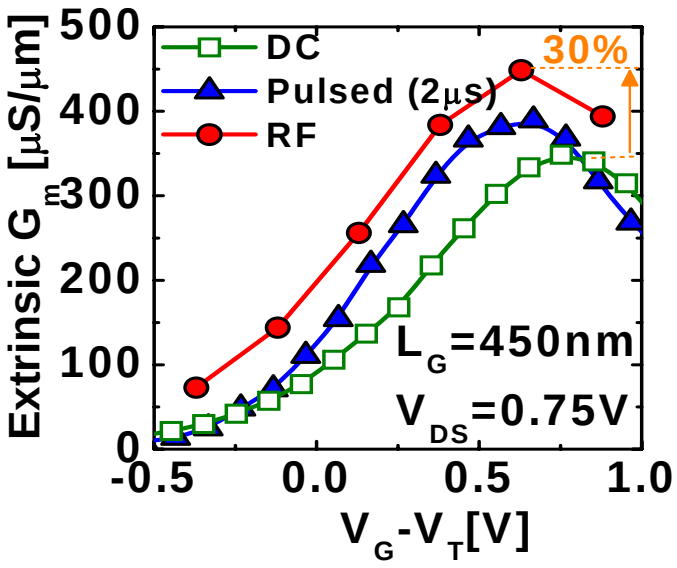



Figure 3-10. Pulsed IV characteristics showing significant enhancement in $I_{ON}$ and $I_{ON}/I_{OFF}$ over DC

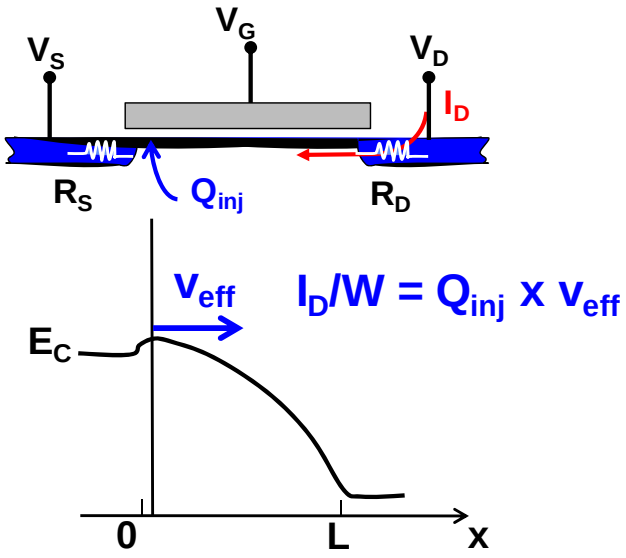
Figure 3-10 show the output and transfer characteristics of the 450nm $L_G$ device using DC and pulsed measurements. The pulsed $I_D$-$V_D$ data shows significant improvement (by 35% at 0.75V gate overdrive) in $I_{ON}$ and $I_{ON}$-$I_{OFF}$ ratio compared to the DC. Figure 3-11 shows extrinsic $g_m$ comparing DC, pulsed IV and RF measurements. Peak extrinsic RF $g_m$ improves by 30% compared to DC $G_m$ for a gate overdrive of 0.6V. This improvement is due to reduced charge trapping in the dielectric at very high frequencies. This confirms that overestimation of charge from split *C-V* leads to ~30% reduction in FET mobility compared to Hall mobility at $N_s$=2x10$^{12}$ /cm$^2$ as obtained in Figure 3-8 (b) from mapping measured and simulated *C-V* curves.




$$RF\ g_m = \mathrm{Re}[Y_{21}]\big|_{\omega^2=0}$$

Figure 3-11. Extrinsic RF $g_m$ showing 30% enhancement over DC $g_m$ due to less charge trapping in RF.

**Short Channel Device Characterization**




$$\frac{1}{v_{eff}} = \frac{1}{v_T} + \frac{1}{\mu_{eff} E(0^+)}$$

$$v_T = \sqrt{\frac{2k_B T}{\pi m^*}}$$

Figure 3-12.Effective injection velocity of electrons at the top of the barrier determines current in a short channel MOSFET

For short channel devices, electron velocity at the top of the source barrier determines the current [32]. Figure 3-12 shows a schematic explaining the virtual source barrier, which is the top of the conduction band near the source end. The source barrier blocks all back scattered electrons beyond a certain distance from the top of the barrier and all electrons passing the barrier and this distance should eventually reach the drain end and contribute to the total drain current. The injection velocity ($v_{inj}$) of carriers at the top of the barrier is an important metric in evaluating the performance of short channel devices. The extraction of $v_{inj}$ requires knowledge of the device gate capacitance which is obtained from RF measurements.

RF characterization allows extraction of the intrinsic device metrics ($C_{gs}$, $C_{gd}$, $g_m$, $g_{ds}$, $v_{eff}$, and $f_t$) and the parasitic resistive and capacitive elements limiting the short channel device performance. The 2 port scattering parameters (S-parameters) of the device under test and the open and short dummy structures are measured. S-parameters of the device are obtained after the

open-short de-embedding to remove the parasitic resistance and capacitance. From the de-embedded S-parameters of the device $C_{gs}$, $C_{gd,}$ $g_m$, $g_{ds}$ are obtained using equations (1) – (4). More details on parameter extraction can be found in [33].

$$C_{gs} = \left(\mathrm{Im}[Y_{11}] + \mathrm{Im}[Y_{12}]\right)/\omega \quad (1)$$

$$C_{gd} = -\mathrm{Im}[Y_{12}]/\omega \quad (2)$$

$$g_m = \mathrm{Re}[Y21]\big|_{\omega 2=0} \quad (3)$$

$$g_{ds} = \mathrm{Re}[Y22]\big|_{\omega 2=0} \quad (4)$$

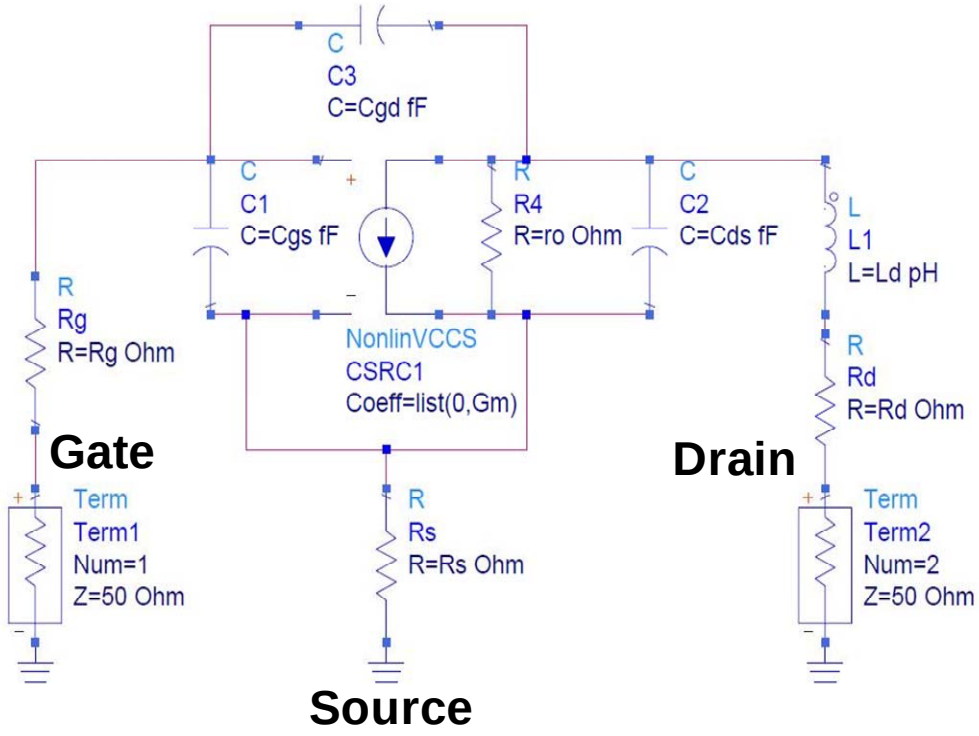
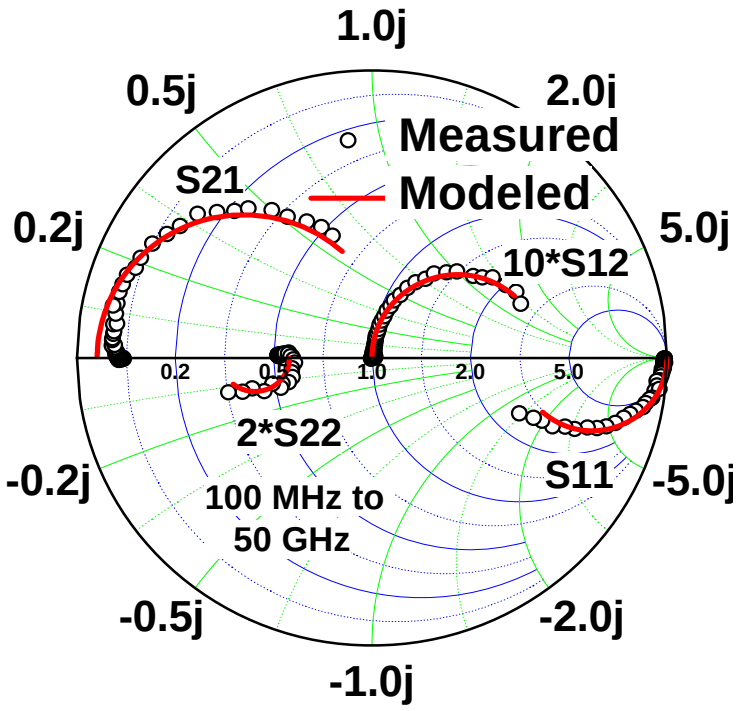



Figure 3-13. A simplified MOSFET small signal equivalent circuit which was used to model the measured s-parameters of Sb NMOSFET

The de-embedded S-parameters of the device are modeled using a simplified small signal equivalent circuit model of MOSFET shown in Figure 3-13 to extract the intrinsic device parameters. The modeling exercise is done using the Agilent Advanced Design System (ADS) software and The evaluated $C_{gs}$, $C_{gd,}$, $g_m$, and $g_{ds}$ from (1) – (4) were used as starting values for the

optimization procedure. Figure 3-14 shows the measured and modeled scattering parameters of the 150 nm $L_G$ device from 100 MHz to 50 GHz and the extracted circuit elements. Excellent agreement between the measured and simulated S-parameters confirms the extracted circuit element values. Figure 3-15 shows the measured and modeled small signal current gain, $|h_{21}|$, vs frequency for $L_G$=150 nm, 300 nm and 450 nm. The devices have cut-off frequencies of 120 GHz, 55 GHz and 27 GHz, respectively. Figure 3-16 benchmarks cur-off frequency of the Sb MOSFETs with Si NMOSFETs. For comparable gate lengths, $f_t$ of Sb nMOSFET is 2x that of of Si NMOSFET.




| Device $L_G$ (nm) | 150 | 300 |
|---|---|---|
| Measured fT(GHz) | 120 | 56 |
| Simulated fT (GHz) | 120 | 55 |
| **Circuit Element** | **Extracted Value** | |
| gm (µS/µm) | 1030 | 820 |
| gd (µS/µm) | 1262 | 459 |
| Cgs (fF/µm) | 0.53 | 1.2 |
| Cgd (fF/µm) | 0.11 | 0.22 |
| Rs (Ω. µm) | 594 | 594 |
| Rd (Ω. µm) | 660 | 594 |

Figure 3-14. Measured and modeled S-parameters of the 150nm $L_G$ Sb NMOS at $V_G$-$V_T$= 0.6V and $V_{DS}$=0.75V, and the extracted circuit elements from the small signal model

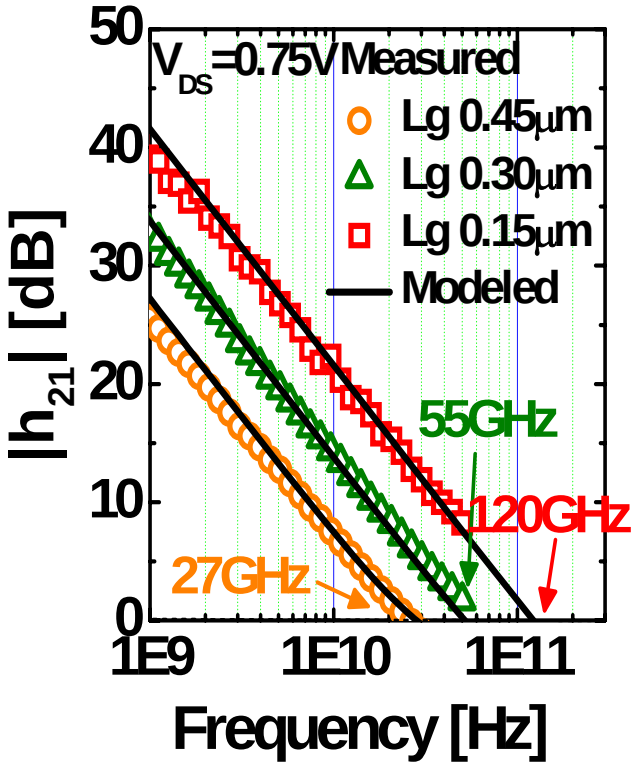



Figure 3-15. Measured and modeled $|h_{21}|$ showing current gain cut-off frequency ($f_t$) of 120 GHz , 55 GHz, 27 GHz for Sb NMOSFETs with 150 nm, 300 nm and 450 nm gate lengths

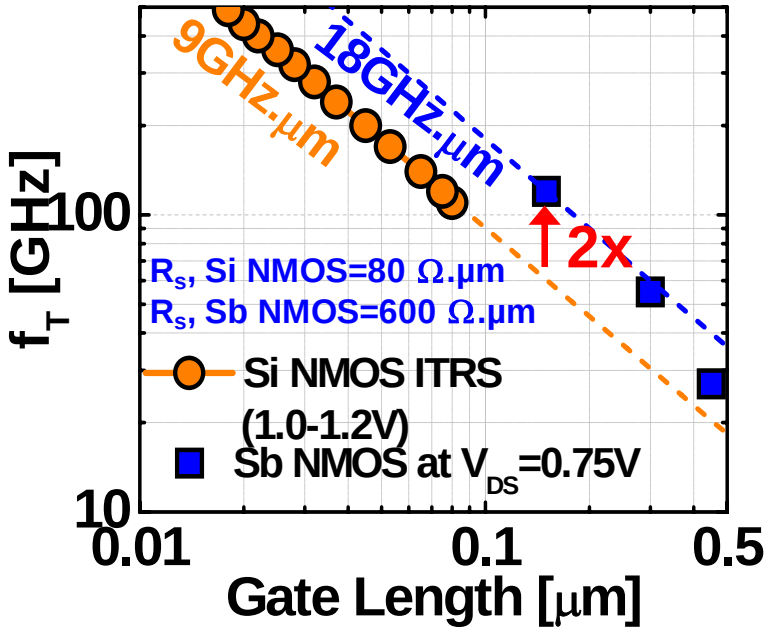



Figure 3-16. Cut-off frequency ($f_t$) vs gate length for Sb compared to Si NMOSFETs. The measured $f_T$,and $f_T x\, L_G$ are the highest reported in literature among III-V MOSFETs.

From the extracted parameters from small signal modeling, I evaluated the source side injection velocity ($v_{eff}$) of these devices as $g_m$/slope($C_{gs}$ vs $L_G$). Figure 3-17 benchmarks the $v_{eff}$ of the Sb NMOS devices with state-of-the-art Si and III-V NMOS. The $v_{eff}$ is 4x that of Si NMOS [34] and 1.5x that of InGaAs NMOS [27]. The 150 nm $L_G$ Sb NMOS exhibits a $v_{eff}$ of 2.7x$10^7$ cm/s and $f_T$-$L_G$ product of 18 GHz.μm, which are the highest reported for III-V MOSFETs till date.

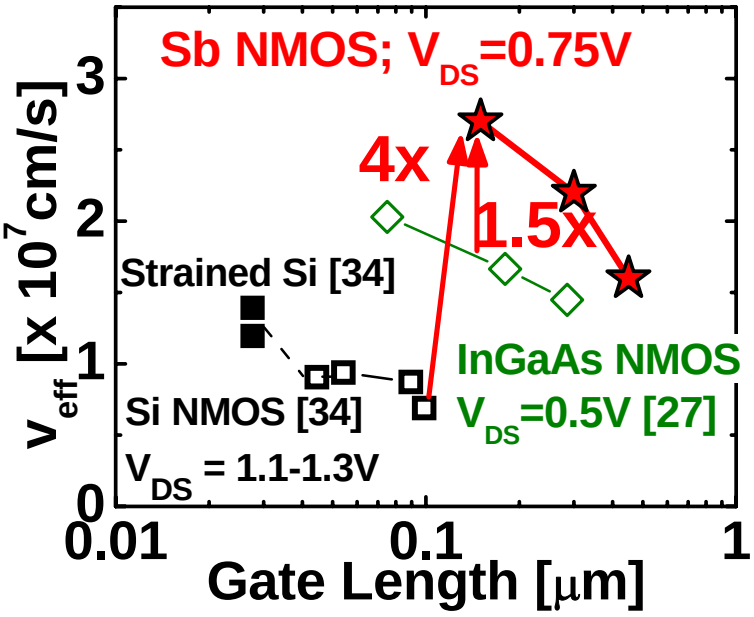



Figure 3-17. Extracted source injection velocity as a function of gate length for Sb NMOSFET

**Enhancement Mode Operation**

While above mentioned devices operate in depletion mode (normally ON) due to thick EOT, enhancement mode (normally OFF) operation is required for logic applications. In this section, I discuss on the design, fabrication and characterization of enhancement mode Sb NMOSFETs. As the quantum well is scaled, the subband energy levels in the quantum well will move up in energy which gives rise to higher threshold voltage operation. Scaling of the barrier

layer will also reduce potential drop in the barrier layer, which further leads to enhancement mode operation. Figure 3-18 shows the schematic of two devices with thick barrier (10nm) / thick QW(12nm) and thin barrier (5nm) / thin QW(7.5nm). As observed experimentally in the previous section, the thick barrier / thick QW device is a depletion mode (D-mode) device. The electron density in the quantum well as a function of gate voltage is shown in Figure 3-19 for the thick barrier (10nm) / thick QW(12nm) and the thin barrier (5nm) / thin QW(7.5nm) cases. This was obtained by solving Poisson and Schrodinger equations self-consistently using nextnano simulator. The graph shows that the thin barrier / thin QW device is an enhancement mode (E-mode) device. The only structural difference between the D-mode and the E-mode device, other than the thickness of the barrier and QW, is that the E-mode devices have InAs cap layer which prevents the depletion of carriers in the access region. Under the gate the InAs layer is etched prior to oxide deposition.

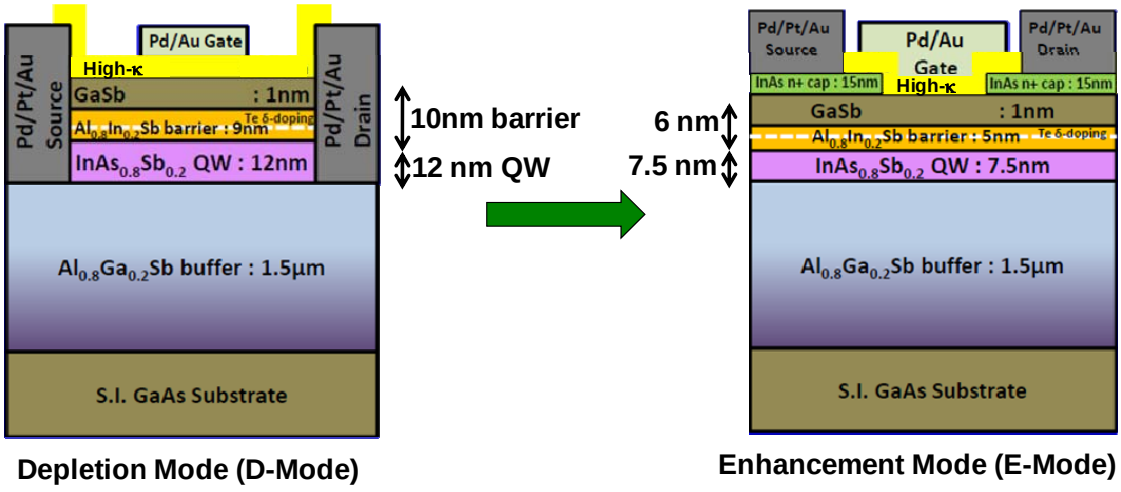



Figure 3-18. Schematic of the enhancement mode device structure with scaled barrier and quantum well

Figure 3-19 also shows the band diagrams in the OFF-state of the D-mode and E-mode devices. For the D-mode device, as the device is turned off, the barrier layer starts accumulating

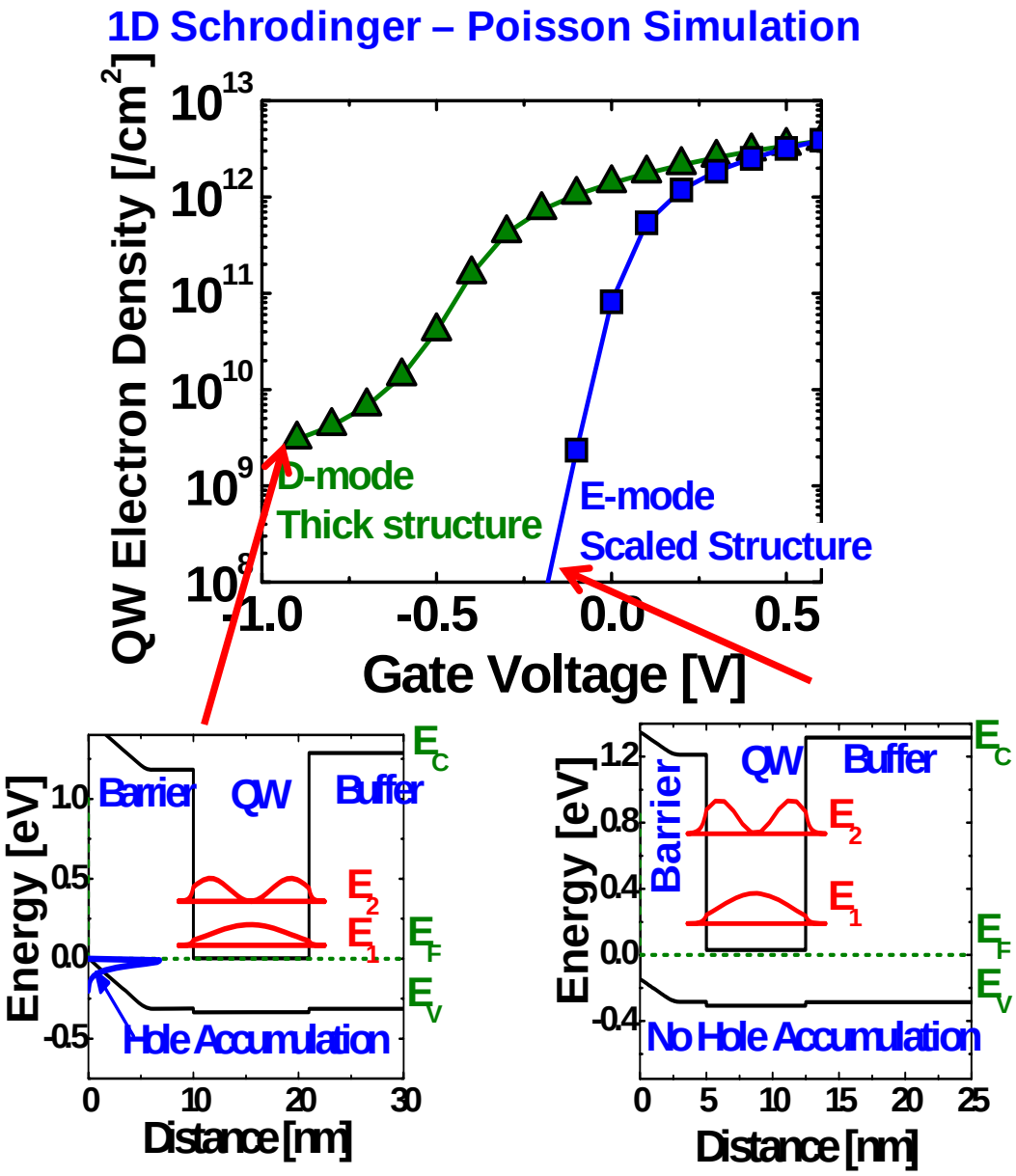



Figure 3-19. 1D Schrodinger-Poisson simulation showing enhanced electrostatic coupling of the gate to the quantum well. Band diagram in the OFF-state for the D-mode and E-mode shows less potential drop in barrier for scaled E-mode. This avoids hole accumulation in the barrier layer in the OFF-state of E-mode device and reduces $I_{OFF}$.

holes. This hole accumulation in the barrier layers screens the gate potential from further depleting the QW. This limits the OFF- state leakage for the D-mode devices. For the E-mode device, the scaling of QW increases the threshold voltage of the device which partly reduces the

hole accumulation in the barrier. Further, scaling the barrier layer reduces the potential drop in the barrier and hence the Fermi level in the barrier layer is not close to the valence band of barrier layer during device turn off, as shown in Figure 3-19 . This avoids hole accumulation for the E-mode devices. As a result of the enhanced electrostatic coupling of the gate to the QW, the E-mode device has better $I_{ON}/ I_{OFF}$ compared to that of the D-mode device.

The fabrication flow for the E-mode device is very similar to that of the D-mode device, except that prior to oxide deposition the InAs layer is etched under that gate using a citric acid based etch (citric acid mixed with hydrogen peroxide in 1:1 ratio). To study the enhancement mode operation of the device, I systematically scale the device structure. D-mode (thick oxide and QW), near E-mode (scaled oxide) and E-mode (scaled oxide and QW) Sb MOSFETs were demonstrated using scaled gate stack and quantum-well thicknesses. Figure 3-20 shows the transfer characteristics of long channel ($L_G$=5 μm) and short channel ($L_G$=150 nm) Sb nMOSFETs for the three devices. Improvement in device electrostatics is demonstrated with lowest sub-threshold slope of 150 mV/decade for the E-mode Sb MOSFETs. The $I_{ON}$-$I_{OFF}$ ratio improves with scaling the EOT as expected for Schrodinger-Poission simulations in Figure 3-19. Figure 3-21 shows the output characteristics of the three devices for a gate length of 150 nm, which shows improvement in the saturation with scaling oxide and QW. Maximum $I_{DSAT}$ of 450 μA/μm is obtained for 150 nm $L_G$ device (D-Mode) at 0.75 V $V_{DS}$ due to electron drift mobility of 6,000 $cm^2/Vs$ at $2x10^{12}$ $/cm^2$ of $N_s$. $R_{EXT}$ due to ungated access region limits the short channel device performance.

Figure 3-22 (a) shows the measured and modeled small signal current gain, $|h_{21}|$, vs frequency for D-mode, Near E-mode, and E-mode devices with $L_G$=150 nm. The devices have cut-off frequencies of 120 GHz, 90 GHz and 21 GHz, respectively. Increase in $R_{EXT}$ due to ungated access region limits the frequency response of the E-mode devices. From the extracted

parameters from small signal modeling, the source side injection velocity ($v_{eff}$) of these devices were evaluated as $g_m/slope(C_{gs}\ vs\ L_G)$. Figure 3-22 (b) benchmarks the $v_{eff}$ the Sb NMOS devices

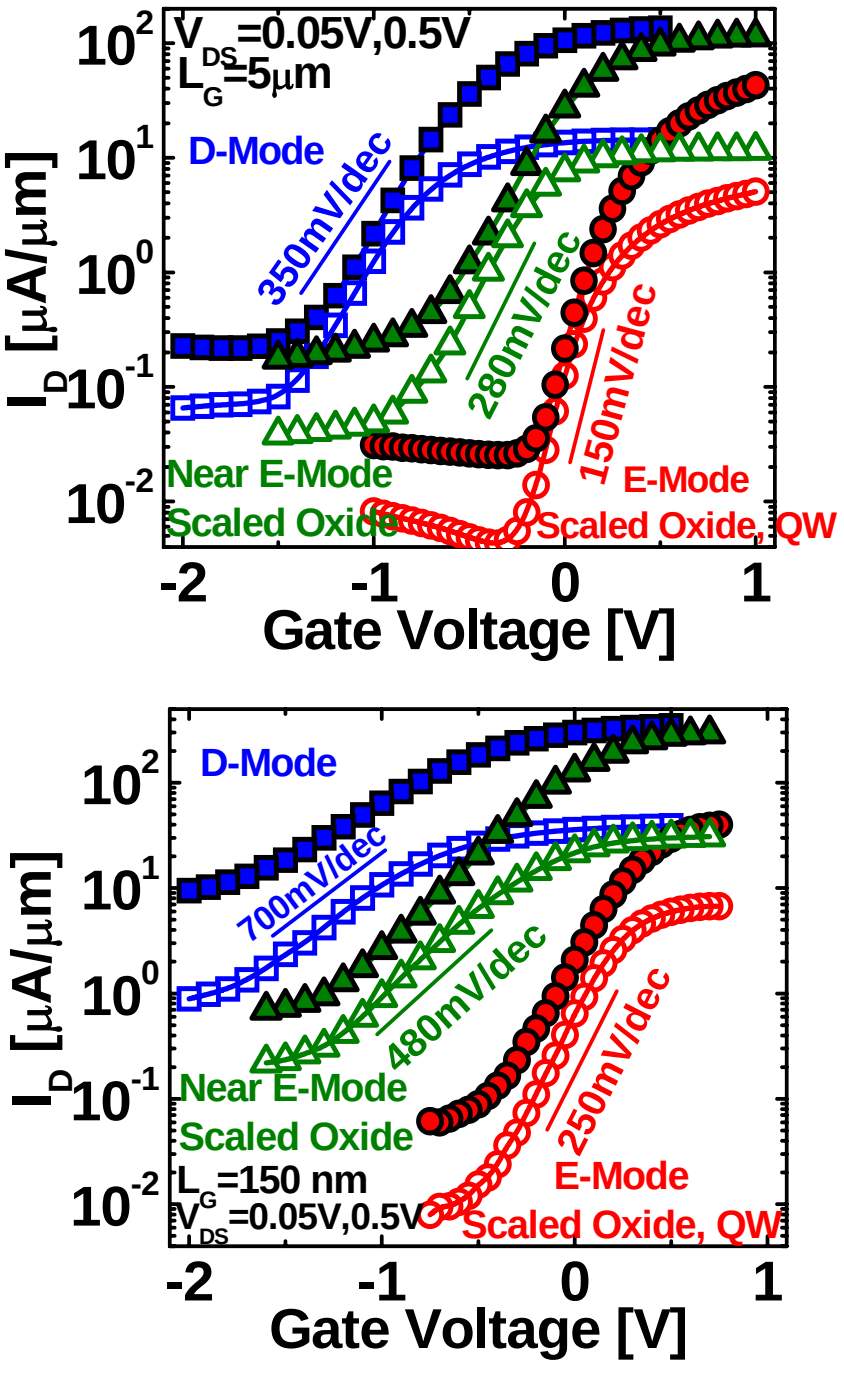



Figure 3-20. Transfer characteristics of long channel ($L_G$=5 μm) and short channel ($L_G$=150 nm) Sb nMOSFETs for D-mode (thick oxide and QW), near E-mode (scaled oxide) and E-mode (scaled oxide and QW) device structures

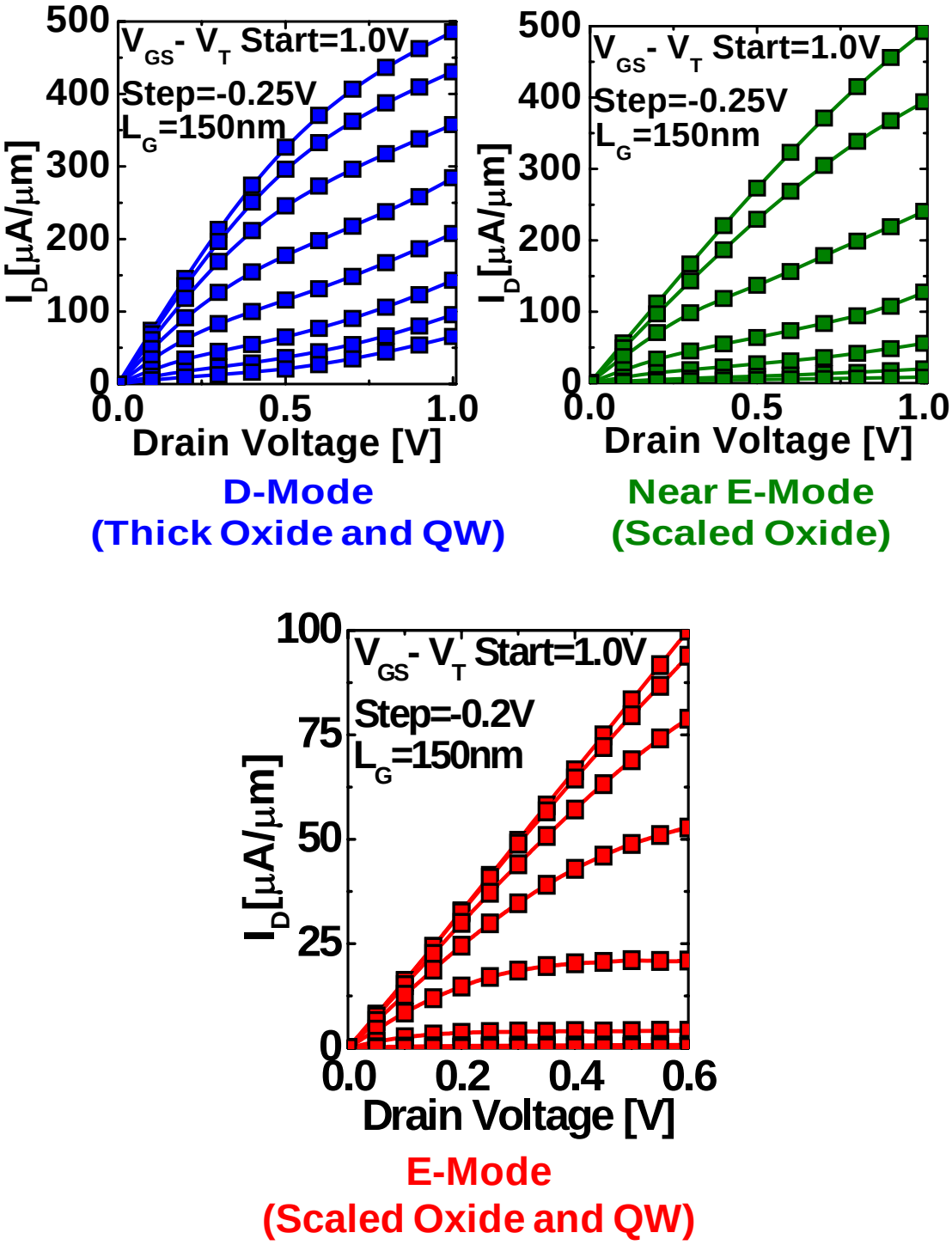
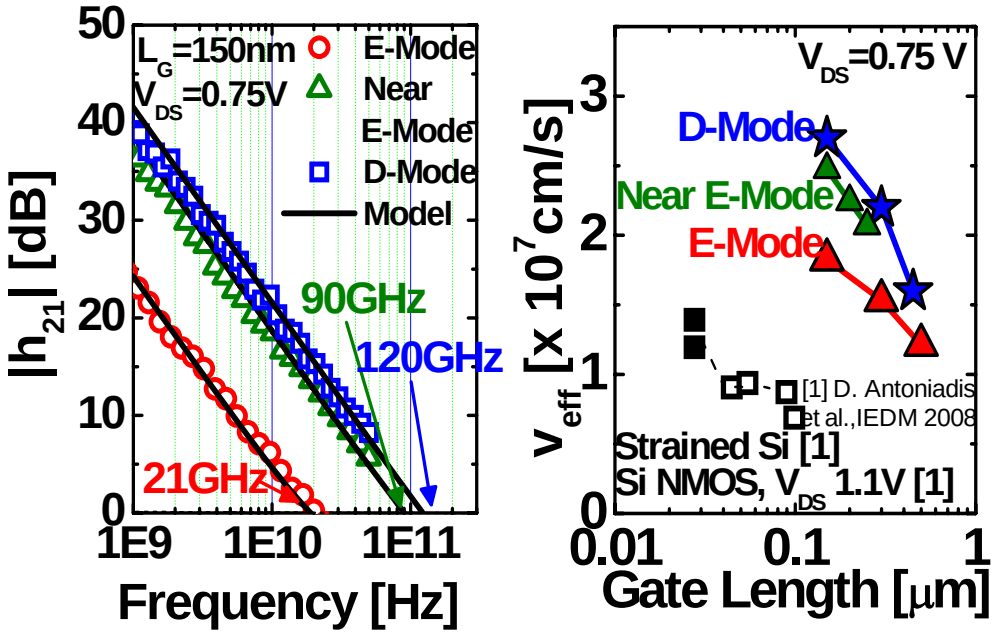



Figure 3-21. Output characteristics of short channel ($L_G$=150 nm) Sb nMOSFETs for D-mode (thick oxide and QW), near E-mode (scaled oxide), and E-mode (scaled oxide and QW) device structures

with state-of-the-art Si. The short channel D-mode Sb NMOSFET ($L_G$ = 150 nm) exhibits a cut-off frequency ($f_T$) of 120 GHz, $f_T$ - $L_G$ product of 18 GHz.µm and source side injection velocity ($v_{eff}$) of 2.7x10$^7$ cm/s, at drain bias ($V_{DS}$) of 0.75 V and gate overdrive of 0.6V. The measured $f_T$ and $f_T$ x $L_G$ are 2 x higher, and $v_{eff}$ is 4x higher than Si NMOS (1.0-1.2 V $V_{DD}$) at similar $L_G$, and are among the highest values reported for III-V MOSFETs. For the Near E-mode and E-mode devices the extracted $v_{eff}$ is lower than that of the D-mode device. This is due to the lower drift mobility of these devices compared to the D-mode device. I find that decreasing the oxide thickness reduces the drift mobility of the Sb NMOSFETs possibly due to scattering from surface charge in the oxide limiting the transport. This lower mobility with scaling the oxide results in lower $v_{eff}$ for the Near E-mode device compared to the D-mode device.




(a) (b)

Figure 3-22. (a) Current gain vs frequency, and (b) Source injection velocity as a function of gate length for D-Mode, Near E-mode and E-Mode Sb NMOSFET.

For the E-mode device, the mobility of the as grown device layer itself was lower than that of the D-mode device layers (13,500 cm$^2$/Vs Hall mobility for the D-mode device vs 5,500

$cm^2/Vs$ for the E-mode device layers). Hence the $v_{eff}$ for the E-mode devices are lower than D-mode and near E-mode devices. Figure 3-23 shows the peak extrinsic RF $g_m$ for the D-mode, Near E-mode, and the E-mode devices mapped as a function of the sub-threshold slope. The near E-mode device has a peak extrinsic $g_m$ of 700 µS/µm, which is higher than the DC $g_m$ (520 µS/µm) by nearly ~35% due to the effect of interface traps. For the near E-mode device, improvement in the $C_{ox}$ improves the *SS* and $g_m$ compared to that of the D-mode device. For the E-mode device, increased $C_{ox}$ compared to the near E-mode device improves the *SS*, but the extrinsic $g_m$ is degraded due to increased access resistance, as the access regions are depleted of carriers.

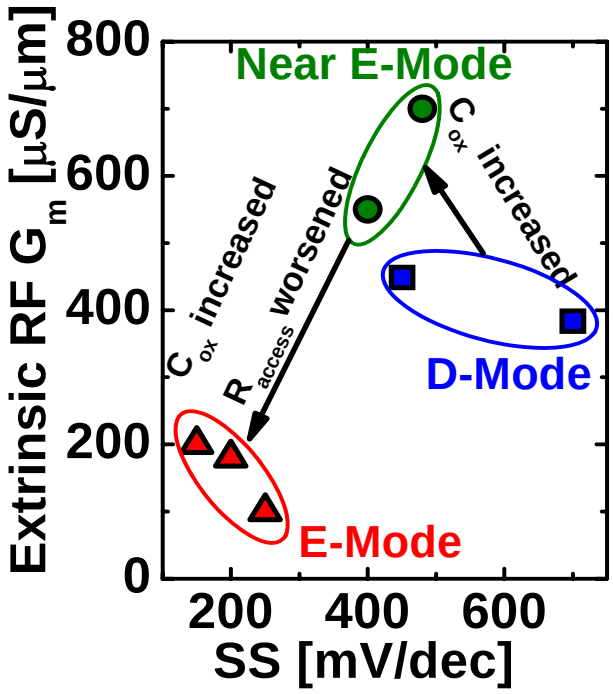



Figure 3-23. Peak extrinsic RF $g_m$ for D-mode, near E-mode and E-mode devices vs sub-threshold slope

## IV. Conclusions

Antimonide (Sb) quantum well (QW) MOSFETs are demonstrated with integrated high-κ dielectric (1nm$Al_2O_3$-10nm $HfO_2$). The long channel Sb NMOS exhibits effective electron mobility of 6,000 $cm^2$/Vs at high field (2 x $10^{12}$ /$cm^2$ of charge density ($N_s$)), which is the highest reported value for any III-V MOSFET. The short channel Sb NMOSFET ($L_G$ = 150nm) exhibits a cut-off frequency ($f_T$) of 120GHz, $f_T$ - $L_G$ product of 18GHz.μm and source side injection velocity ($v_{eff}$) of 2.7x$10^7$ cm/s, at drain bias ($V_{DS}$) of 0.75V and gate overdrive of 0.6V. The measured $f_T$ and $f_T x\ L_G$ are 2 x higher, and $v_{eff}$ is 4x higher than Si NMOS (1.0-1.2V $V_{DD}$) at similar $L_G$, and are the highest values reported till date for any III-V MOSFET. D-mode, near E-mode, and E-mode Sb NMOSFETs were demonstrated for the first time by systematically scaling the oxide and the quantum well (QW) structure.

# Chapter 4

# Quantum Capacitance and Gate Capacitance Scalability of Sb NMOSFETs

## I. Introduction

Mixed anion $InAs_ySb_{1-y}$ quantum-wells (QW) with high electron mobility are candidates for direct integration with high hole mobility $In_xGa_{1-x}Sb$ QW for ultra-low power complementary applications [35][36]. In chapter 3, the transport characteristics of long channel and short channel Sb nMOSFETs were studied in detail. Short channel Sb nMOSFETs (150 nm $L_G$ device) exhibit electron velocity of about $2.7x10^7$ cm/s which is 4x higher than Si MOSFETs of comparable $L_G$. However, the ON current of the (short channel) device depends not only on the electron velocity, but also on the electron density at the top of the barrier. As a direct consequence of the low effective mass for electrons in the Γ-valley, $InAs_ySb_{1-y}$ QW-MOSFETs can suffer from the so-called density of states (DOS) bottleneck which may limit the effective ON-current, and adversely affect switching in fixed load capacitance dominated digital circuits [37]. The capacitance associated with the QW in $InAs_ySb_{1-y}$ QW-MOSFET depends on the 2D DOS (quantum capacitance, $C_Q$) as well as the electron wave function distribution (centroid capacitance, $C_{cent}$) in the quantum well [38]. Even though the low effective mass limits the $C_Q$, quantization and non-parabolicity enhances the $C_Q$ and the $C_{cent}$ of the $InAs_{0.8}Sb_{0.2}$ quantum-well [39]. Incorporation of a gate dielectric within the $InAs_ySb_{1-y}$ QW-MOSFET together with finite capacitance, $C_{barrier}$, arising from the upper semiconductor barrier layer further increases the equivalent oxide thickness (EOT) in a QW-MOSFET. Hence, it is imperative to understand how the different components of capacitance ($C_Q$, $C_{cent}$, $C_{barrier}$ and $C_{ox}$) affect the overall gate capacitance and scalability of this device.

In this chapter, I present a physics-based analytical model to analyze the experimental gate capacitance ($C_g$) versus gate voltage ($V_g$) data for an $InAs_{0.8}Sb_{0.2}$ QW-MOSFET with a composite high-κ gate stack (10 nm $HfO_2$ -1 nm $Al_2O_3$ - 1nm GaSb), and to extract systematically the quantum capacitance of the channel including the non-parabolicity effect, as well as the centroid capacitance associated with the spread of the electron wave function in the QW. The significance of this work lies in the fact that accurate quantification of the quantum capacitance in high mobility channel MOSFETs is critical to future device scaling. A small-signal equivalent circuit model is utilized to correct the measured gate capacitance data from the impact of the interface state density, $D_{it}$. In a previous work done by Jin et al. [40], the quantum capacitance of a Schottky gated InAs QWFET was analyzed, but without considering the effect of non-parabolicity in the band structure and the impact of interface states. Jin et al. used a single effective mass, higher than the Γ-valley mass of bulk InAs, to account for the increase in $C_Q$ due to quantization and non-parabolicity. In this work, I incorporate the non-parabolicity in the $InAs_{0.8}Sb_{0.2}$ band structure using the non-parabolicity factor, $\alpha$, which captures the energy dependence of both the two-dimensional DOS and the effective mass. The effective mass obtained from the capacitance modeling was further verified using Shubnikov-de Haas (SdH) magnetotransport measurements at low temperature (2-15K) and high magnetic field (0-9T). I also present an EOT scalability study, which shows that, for $InAs_{0.8}Sb_{0.2}$ QW-MOSFET with thin dielectric (0.7nm EOT) and barrier (0.45nm EOT), the oxide and barrier capacitance has similar contribution to the gate capacitance (53% of $1/C_g$) as that from the quantum capacitance, $C_Q$ (39% of $1/C_g$) and the centroid capacitance, $C_{cent}$ (8% of $1/C_g$), for a gate overdrive of 0.35V (~two-third of $V_{DD}$=0.5V).

## II. Experimental $C_g$-$V_g$ Measurements and Correcting for $D_{it}$

Figure 4-1 shows the schematic of the fabricated $InAs_{0.8}Sb_{0.2}$ QW-MOSFET with 1nm GaSb and 1nm $Al_2O_3$ / 10 nm $HfO_2$ dielectric which forms a composite gate stack on top of the barrier. The fabrication details of the transistor are reported elsewhere [41]. A thin layer of GaSb (1nm) is used as an interfacial layer with the high-κ dielectric to reduce the interface state density [42]. Figure 4-2 shows the experimentally measured split capacitance –voltage characteristics ($C_g$-$V_g$ ) and conductance – voltage characteristics ($G$-$V_g$) of $InAs_{0.8}Sb_{0.2}$ QW-MOSFET at 300K. The capacitance and conductance exhibit frequency dispersion due to effects of interface states. The frequency independent device capacitance needs to be extracted from this data to study the gate capacitance scalability of Sb NMOS. For this, I employed the equivalent circuit model procedure to correct the $C_g$-$V_g$ data of the effects of frequency dispersion due to $D_{it}$. This method is explained in detail in my paper [43], and briefly mentioned below.

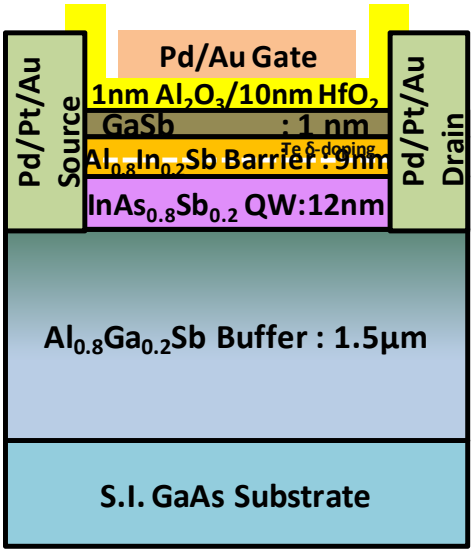



Figure 4-1. Schematic of the $InAs_{0.8}Sb_{0.2}$ QW-MOSFET with composite high-k dielectric (10 nm nm $HfO_2$ – 1 nm $Al_2O_3$ – 1 nm GaSb)

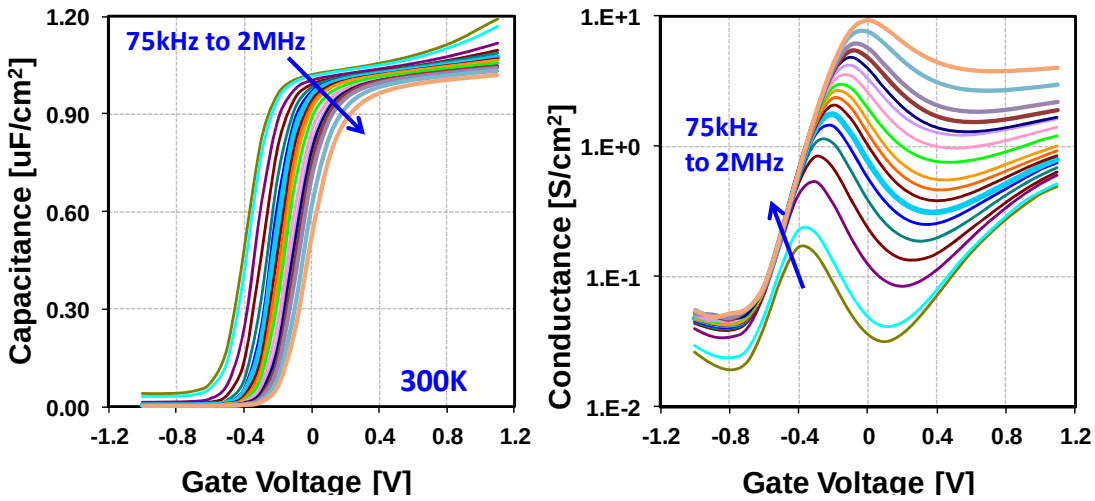



Figure 4-2. Measured split capacitance ($C_g$-$V_g$) and conductance ($G$-$V_g$) characteristics of $InAs_{0.8}Sb_{0.2}$ QW-MOSFET at 300K

**Fundamentals of Interface States Characterization**

As we saw in chapter 2, GaSb and high-κ dielectric interfaces are known to possess interface defects. Although the exact origin of the defects is still under debate there is evidence that compound semiconductors exhibit interface states that arise from the native defects, such as Ga or Sb dangling bonds as well as Ga–Ga or Sb–Sb like-atom bonds created by unwanted oxidation during the process of gate dielectric formation. These defects can give rise to a distribution of electronic states exist within the band gap of the semiconductor, and also extend into the conduction and valence bands [44][45]. The presence of interface states near the band edges leads to fast trap response as the Fermi level approaches and enters the conduction band in the inversion regime. Many recent publications of III–V MOSFETs have reported split C-V measurements and the resultant mobility calculated from those measurements [46][47][48]. Frequency dispersion due to $C_{it}$ as well as lumped and distributed resistance effects in the inversion regime has strongly influenced the $C_g$ vs $V_g$ *(or C-V)* curves resulting in incorrect mobility calculations.

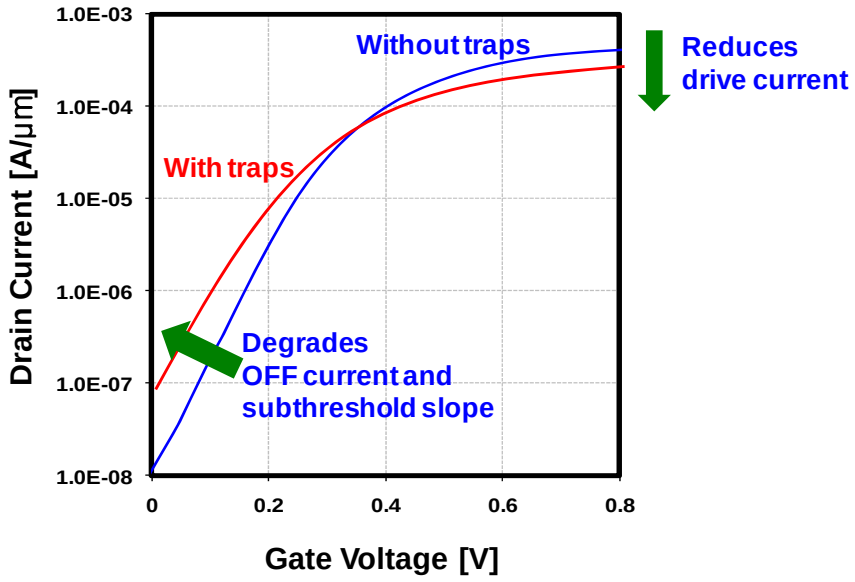



Figure 4-3. Transfer characteristics of an nMOSFET showing the impact of $D_{it}$. Charging of traps gives rise to poor sub-threshold slope, degraded OFF state leakage and poor ON current.

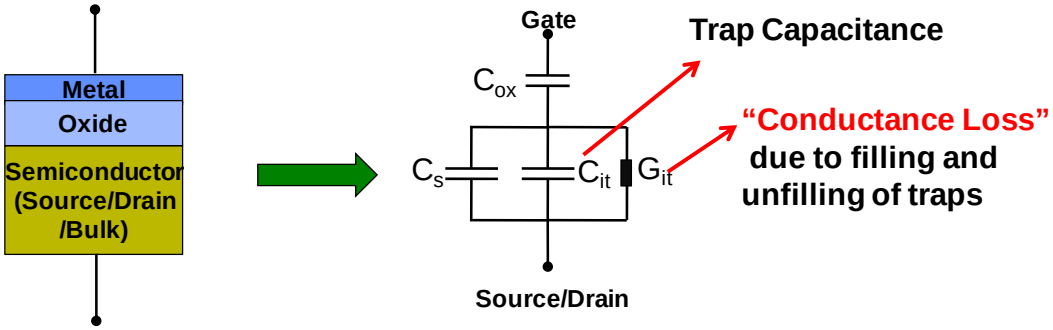



Figure 4-4. Equivalent ciruit model of a MOS capacitor with $D_{it}$ at the oxide-semiconductor interface

Figure 4-3 shows the impact of $D_{it}$ on the transfer characteristics of an NMOSFET. Charging of traps gives rise to poor sub-threshold slope, degraded OFF state leakage and poor ON current. The interface states get charged and discharged as the Fermi level sweeps at the interface. This charging and discharging of $D_{it}$ gives rise to a dynamic capacitance ($C_{it}$) which changes as a function of the frequency at which the Fermi level moves at the interface. In addition, there will be an energy loss associated with the trap charging/discharging cycle if the

frequency response of the traps lags behind the frequency of the applied gate bias. This energy loss is called the conductance loss ($G_{it}$). Figure 4-4 shows the equivalent small signal circuit model of a MOS capacitor with $D_{it}$ at the oxide-semiconductor interface.

The conductance method was proposed by Nicollian and Brews to characterize $D_{it}$ at the oxide-semiconductor interface [49]. $D_{it}$ extraction using this method is illustrated in Figure 4-5. The conductance response of the traps ($G_p/\omega$) is plotted a function of the frequency of the AC signal ($\omega$). At very low frequencies, when all traps respond to the AC signal, there is no loss. Similarly, at very high frequencies, none of the traps follow the AC signal and hence no conductance loss. At intermediate AC frequencies where the traps are in resonance with the AC signal, the conductance will go through a maximum. From the value of this peak conductance, the $D_{it}$ is estimated. However, this method assumes that the entire conductance loss is due to $D_{it}$.

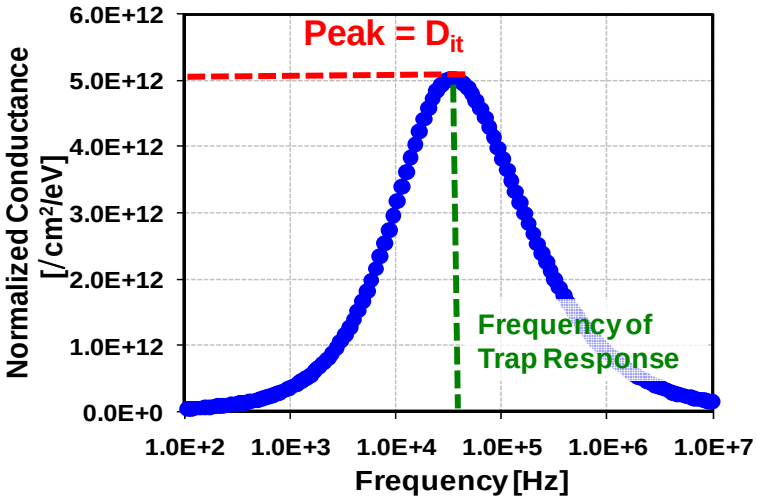



Figure 4-5. $D_{it}$ extraction using conductance method proposed by Nicollian and Brews [49]

In reality, conductance loss in a MOSFET can come from additional dissipating factors like the series resistance due to contact and channel resistance as well as due to gate leakage. Figure 4-6

shows the modified equivalent circuit model including the effects of series resistance and gate leakage.

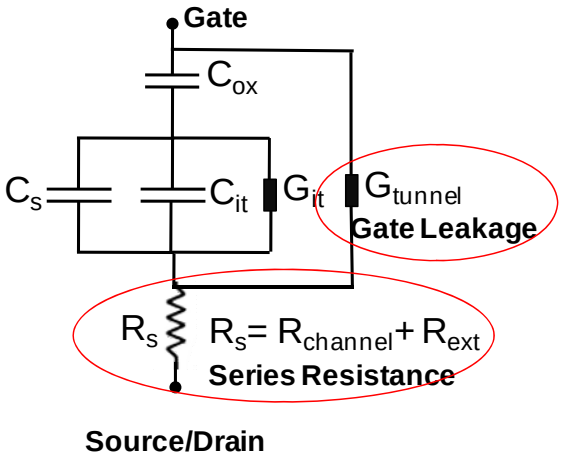



Figure 4-6. Equivalent circuit model for a MOSFET including the effects of series resistance ($R_{series}$) and gate leakage ($G_{tunnel}$) along with $D_{it}$

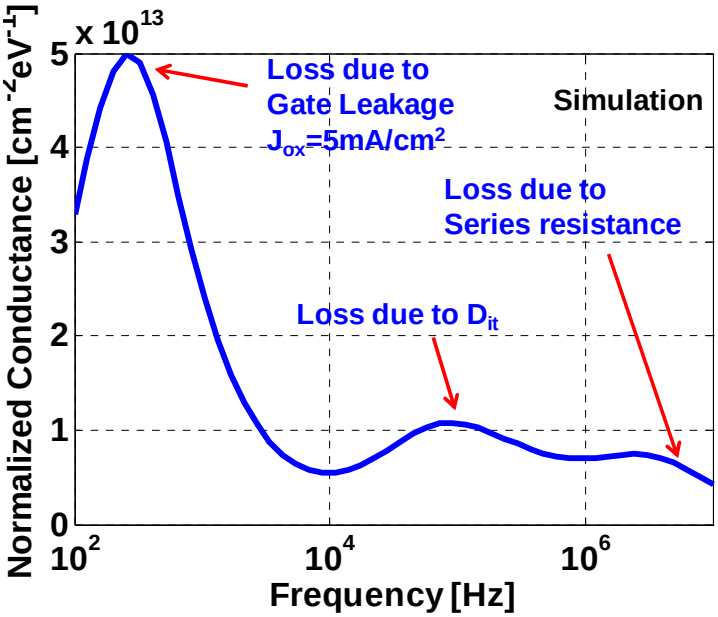



Figure 4-7. Normalized conductance as a function of frequency showing conductance peaks due to $D_{it}$, gate leakage and series resistance.

Figure 4-7 shows the normalized conductance as a function of frequency showing conductance peaks due to $D_{it}$, gate leakage and series resistance. The peak at low frequency is due to gate leakage, which shifts toward higher frequencies with increased gate leakage. For thin oxides with high gate leakage, the gate leakage peak shifts to higher frequencies and overlap with the peak due to $D_{it}$ (in the mid frequency range). The peak at high frequencies is due to series resistance which shifts to the left with increased series resistance. This peak also overlaps with the peak due to $D_{it}$ (in the mid frequency range) making it difficult to rely on the conventional conductance method for $D_{it}$ extraction. Figure 4-8 shows the normalized conductance as a function of frequency showing effects of increased gate leakage and series resistance for high $D_{it}$ ($1x10^{13}$ /cm$^2$/eV) case, and Figure 4-9 shows the case for low $D_{it}$ ($1x10^{13}$ /cm$^2$/eV).

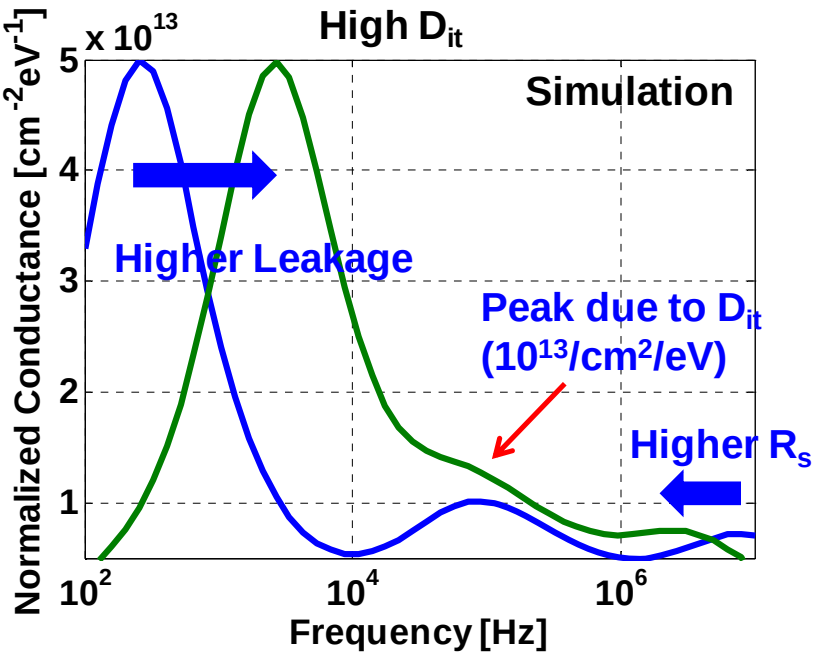



Figure 4-8. Normalized conductance as a function of frequency showing effects of increased gate leakage and series resistance for high $D_{it}$ ($1x10^{13}$ /cm$^2$/eV) case

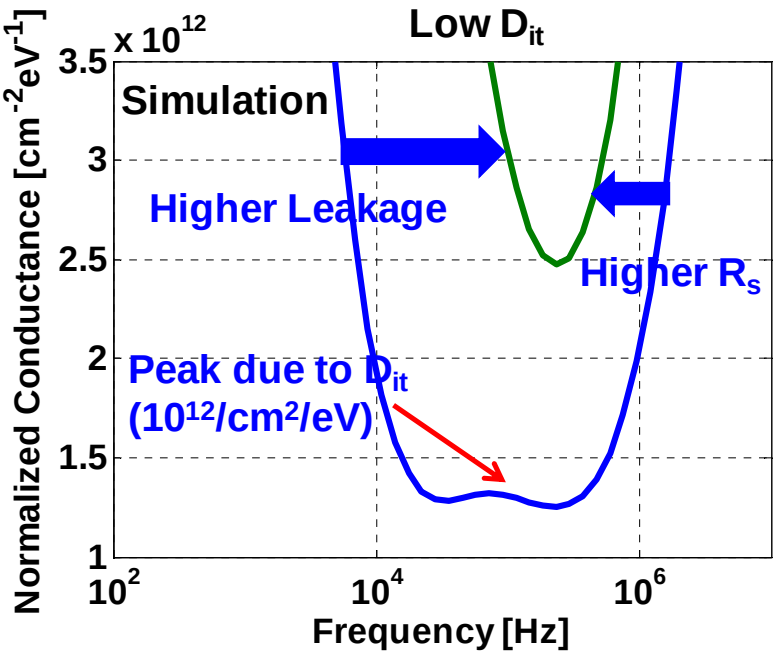



Figure 4-9. Normalized conductance as a function of frequency showing effects of increased gate leakage and series resistance for high $D_{it}$ (1x10$^{13}$ /cm$^2$/eV) case

From this, it is clear that the conductance method for $D_{it}$ extraction works well for thick oxides (> 60 Å) and high $D_{it}$ (> 5x10$^{12}$ /cm$^2$/eV). For the case of thin oxides (< 40 Å) and low $D_{it}$ (< 1x10$^{12}$ /cm$^2$/eV), significant influence of parasitics (gate leakage and series resistance) exist in the conductance method and hence cannot be applied.

Another limitation of the conductance method is that it requires multi-temperature measurements to extract the $D_{it}$ over the entire band gap of the semiconductor. Figure 4-10 shows the characteristic frequency response of traps as a function of energetic location in the band gap. Since the conductance method requires that the trap response frequency falls within the measurement frequency range to extract the $D_{it}$ at a particular energy level, multi-temperature measurements are required to change the frequency response of traps and scan the entire band gap.

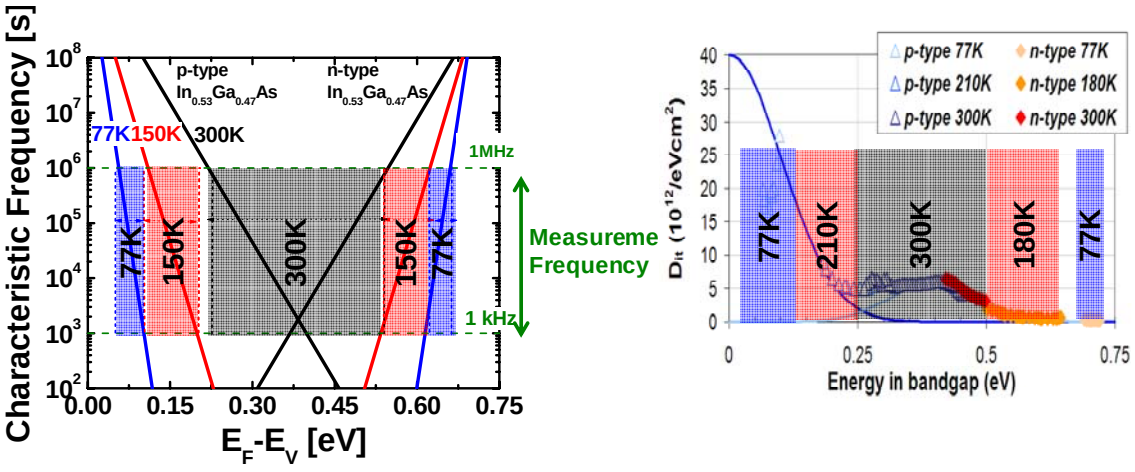



Figure 4-10. Characteristics frequency of trap response as a function of position in the band gap. $D_{it}$ extraction using conductance method requires multi-temperature measurements to scan the band gap. A typical $D_{it}$ profile of $In_{0.53}Ga_{0.47}As$ semiconductor with $Al_2O_3$ gate dielectric obtained using conductance analysis is shown on the right with the different measurement temperatures indicated along the band gap [50].

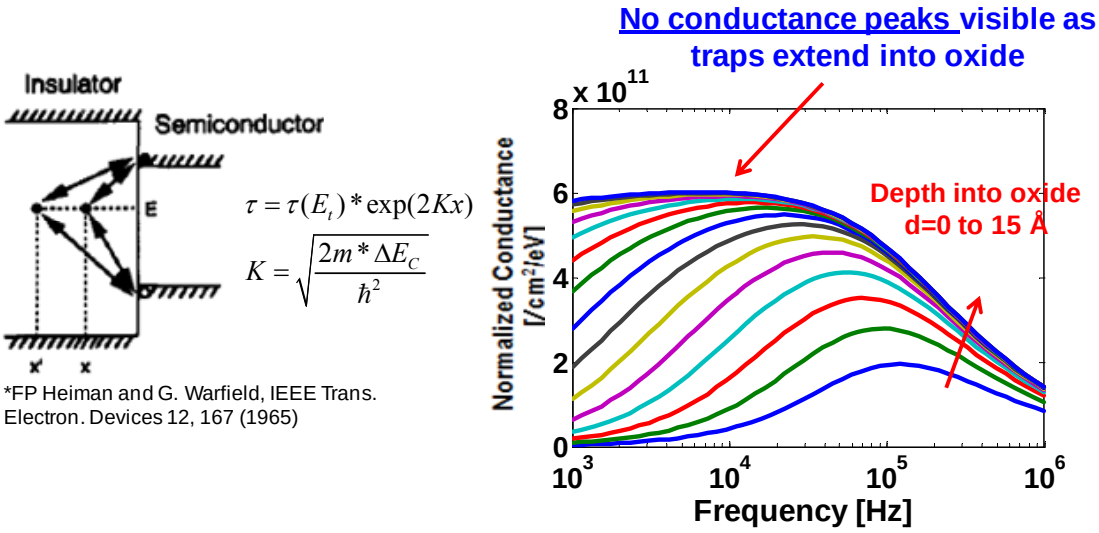
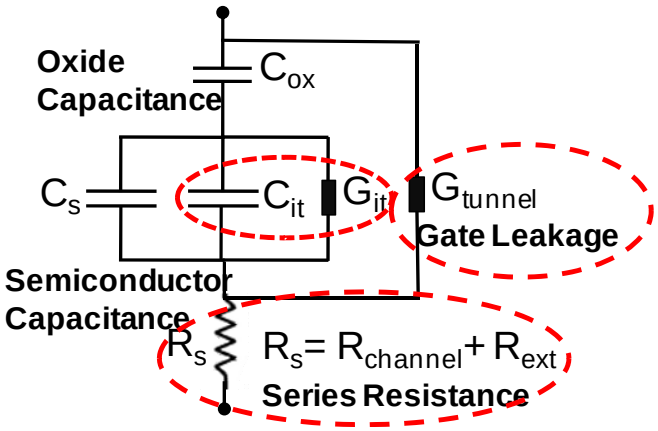



Figure 4-11. Normalized conductance as a function of frequency for traps which extend physically into the oxide.

Depending on the nature of the interface defects, traps need not be exactly at the interface of the oxide and semiconductor. It can physically extend into the oxide by as much as 1 nm to 2 nm [51], and these so called border traps deep inside the oxide need to exchange carriers with the semiconductor to attain equilibrium. As the depth of the traps increase, the response time of the

traps also increase. Figure 4-11 shows the conductance response of the traps as a function of depth extending into the oxide. At depths > 5 Å, the conductance peaks are no longer visible and the normalization procedure in the conductance method cannot be applied.

**Equivalent Circuit Modeling for $D_{it}$ Characterization**




$$Solve \sum_{frequency} \left[ Y_{Measured} - Y_{simulated}(D_{it}, \tau, C_s, G_{tunnel}, R_s) \right] = 0$$

Figure 4-12. Equivalent circuit model for self-consistently solving the measured capacitance and conductance

In this section, I will outline a novel technique that self consistently solves the capacitance-voltage (*C-V)* and conductance-voltage (*G-V*) measurement data as a function of gate bias and small signal AC frequency to uniquely determine the $D_{it}$ response as well as the true inversion carrier response for a given voltage. This technique enables us to extract the true inversion capacitance which is frequency independent ($C_{inv}$) as a function of gate bias in the inversion regime. The model shown in Figure 4-12 incorporates several features which are currently absent in the previous methods for extracting $D_{it}$. The method addresses the limitations

of the conductance method in extracting $D_{it}$ for thin oxide devices with high gate leakage and high series resistance, by including series resistance and gate leakage in the circuit model. The effect of border traps is included in the model by defining the time constant of the border traps using WKB approximation [51]. Unlike the conductance method we do not need to locate the conductance peak, and hence we can quantitatively extract the $D_{it}$ over a wide range of energy at room temperature even though the precise location of the conductance peak, $(G_{it}/\omega)_{peak}$, is outside the measurement frequency range.

The measured $C_g$-$V_g$ and $G$-$V_g$ data were self-consistently modeled using the equivalent circuit model which accounts for the admittance contribution from the interface states at the $Al_2O_3$-GaSb interface. Figure 4-13 shows an excellent agreement between the measured $C_g$-$V_g$ and $G$-$V_g$ curves at 300K for the Sb QW MSOFET, and the modeled data using the method. Figure 4-14 shows the $D_{it}$ extracted from the modeling as a function of gate voltage. Using the extracted values of trap response, the $C_g$-$V_g$ is corrected for $D_{it}$ using the circuit model shown in Figure 4-15. Figure 4-15 also shows the $C_g$-$V_g$ curves corrected for $D_{it}$ along with the measured $C_g$-$V_g$ characteristics at 300K. The extracted frequency independent device capacitance (*the true C-V*) helps us understand the density of states and quantum capacitance of the Sb quantum well MOSFET using the analytical modeling procedure explained in the next section.

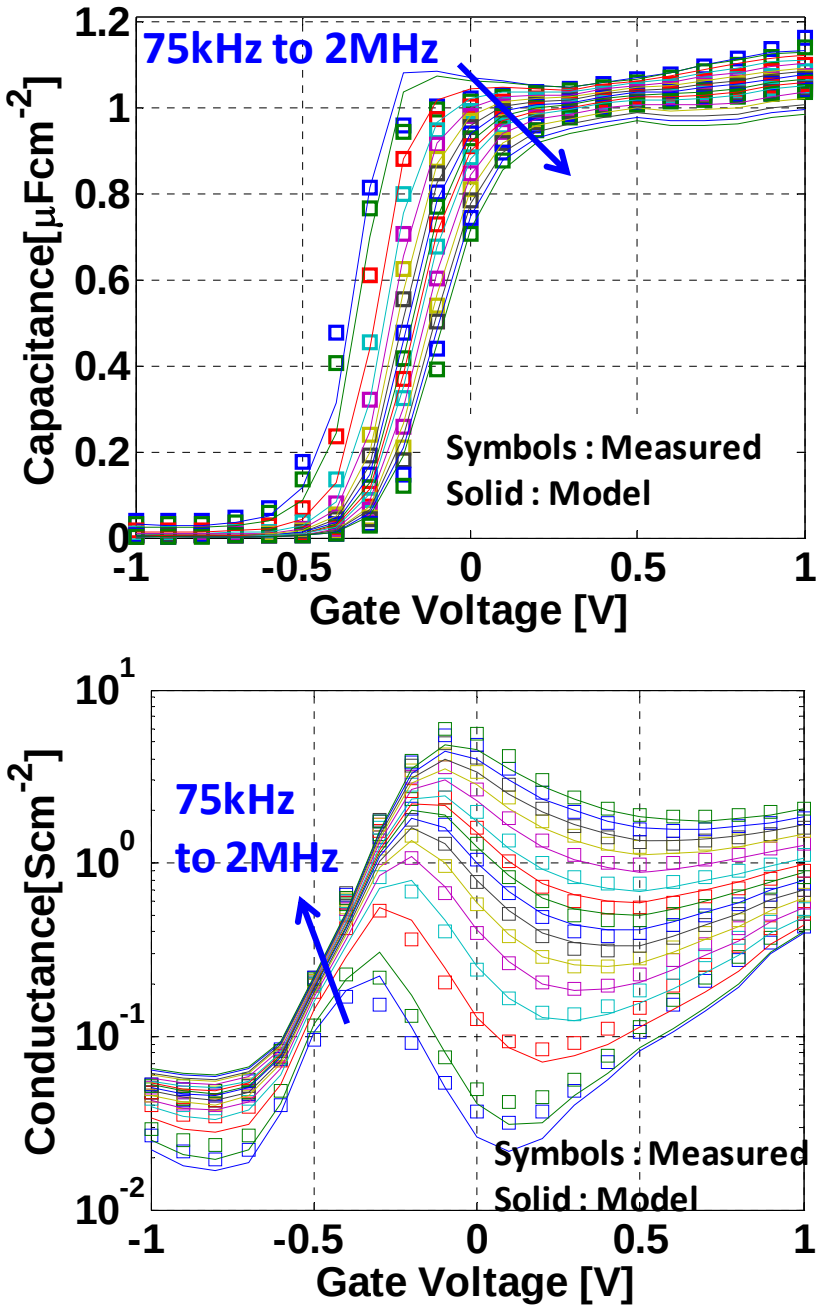



Figure 4-13. Self consistent solving of capacitance and conductance data at 300K using the equivalent circuit model, showing excellent fit between measured and modeled data

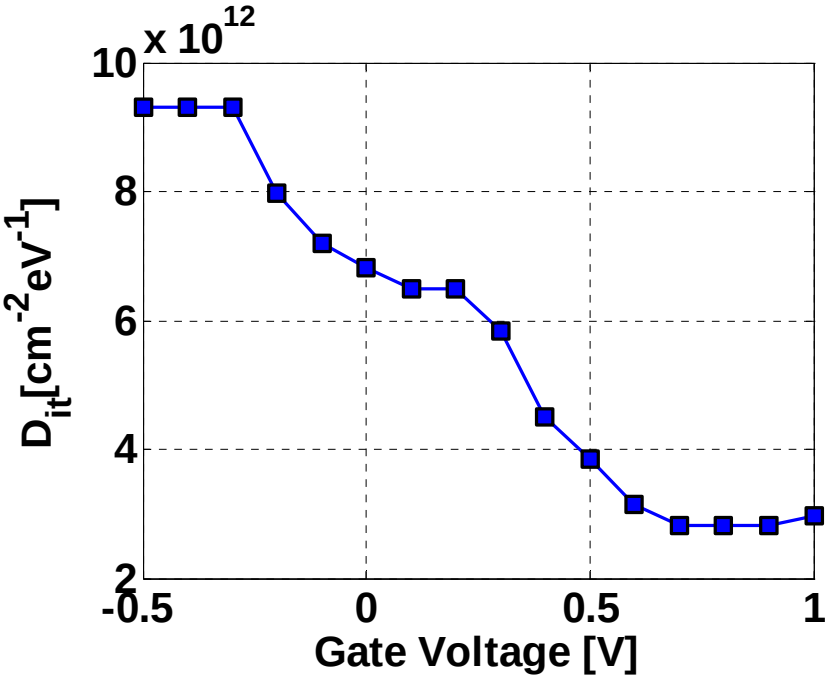



Figure 4-14. Extracted $D_{it}$ as a function of gate voltage

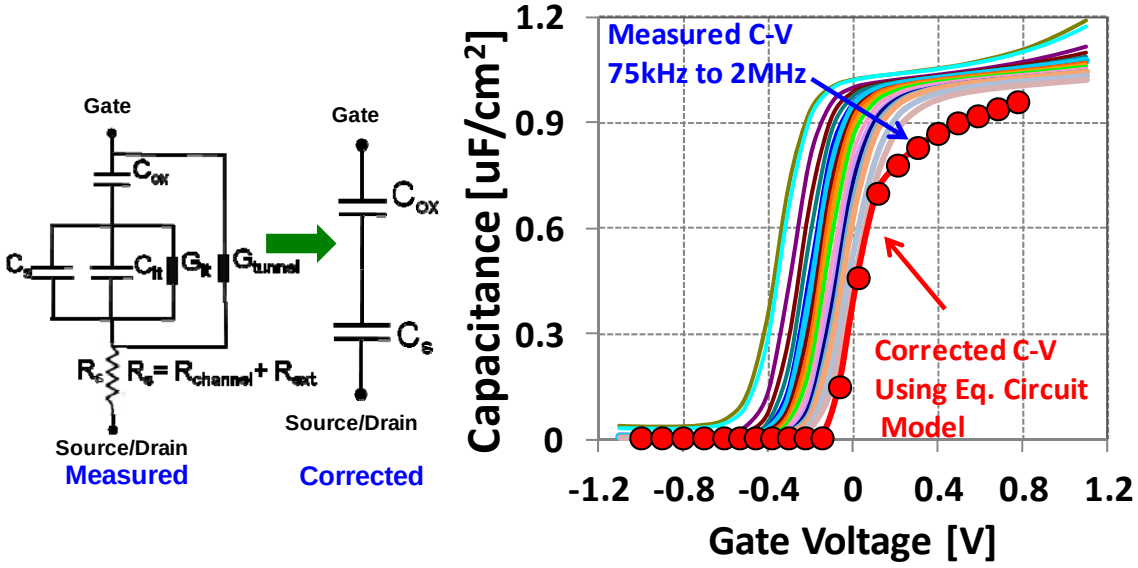



Figure 4-15. $C_g$-$V_g$ curves corrected for $D_{it}$ along with the measured $C_g$-$V_g$ characteristics

## III. Analytical Modeling of Gate Capacitance of QW-MOSFET Including Non-parabolicity

The capacitance of the $InAs_{0.8}Sb_{0.2}$ QW ($C_S$) can be expressed as a series combination of the quantum capacitance ($C_Q$) which is related to the two-dimensional (2D) DOS in the QW, and the centroid capacitance ($C_{cent}$) which is related to the change in the subband energy levels in the QW due to the sheet charge density in the QW (which is related to the charge distribution in the QW), as given by (1) - (8). Here $N_{S,i}$ stands for charge density in the *i-th* subband, $\Psi_{S,QW}$ stands for the quantum well potential, $C_{Q,i}$ stands for quantum capacitance of the *i-th* subband, $C_{cent,i}$ stands for centroid capacitance of the *i-th* subband, $E_i$-$E_C$ stands for the position of the *i-th* subband with respect to bottom of the conduction band in the QW, $E_F$-$E_i$ stands for the Fermi level position with respect to the *i-th* subband and *f(E)* is the Fermi-Dirac distribution function.

$$C_S = \frac{\partial(-Q_S)}{\partial \psi_{S,QW}} = \sum_i q \frac{\partial N_{S,i}}{\partial \psi_{S,QW}} \tag{1}$$

$$N_S = \sum_i N_{S,i} = \sum_i \int_{E_i}^{\infty} DOS_{2D}(E) f(E) dE \tag{2}$$

$$q\partial \psi_{S,QW} = \partial(E_F - E_C) = \partial(E_F - E_i) + \partial(E_i - E_C) \tag{3}$$

$$C_S = \sum_i q^2 \frac{\partial N_{S,i}}{\partial(E_F - E_i) + \partial(E_i - E_C)} \tag{4}$$

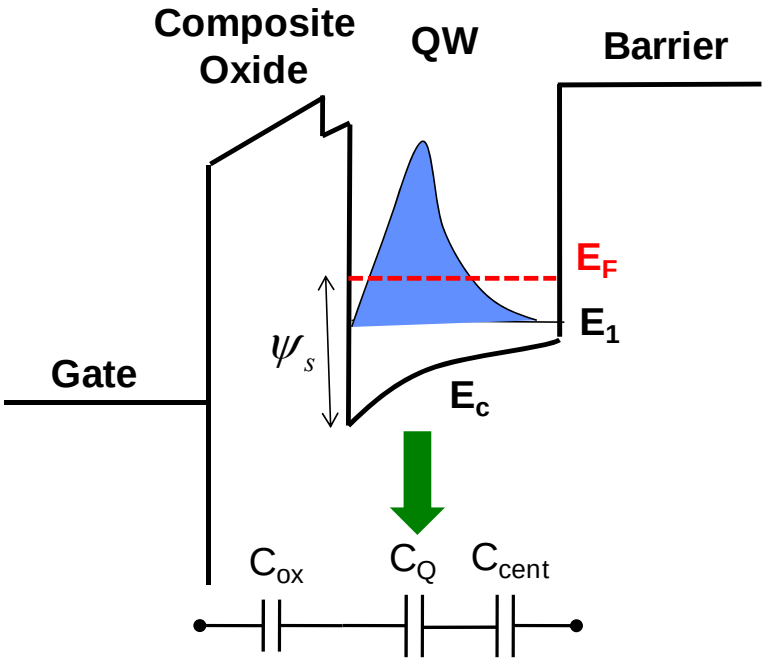



Figure 4-16. Schematic of electron distribution in the Sb QW MOSFET. The semiconductor capacitance depends on the density of states (quantum capacitance, $C_Q$) as well as the change in sub-bands with field in the quantum well (centroid capacitance $C_{cent}$, which is associated with the distribution of electrons in the QW)

$$C_S = \sum_i q^2 \frac{\partial N_{S,i}}{\partial(E_F - E_i)} \frac{\partial(E_F - E_i)}{\partial(E_F - E_i) + \partial(E_i - E_C)} \tag{5}$$

$$C_S = \sum_i C_{S,i} \tag{6}$$

$$\frac{1}{C_{S,i}} = \frac{1}{C_{Q,i}} + \frac{1}{C_{Q,i}} \frac{\partial(E_i - E_C)}{\partial(E_F - E_i)} = \frac{1}{C_{Q,i}} + \frac{1}{C_{cent,i}} \tag{7}$$

$$C_{Q,i} = q^2 \frac{\partial N_{S,i}}{\partial(E_F - E_i)}; \quad C_{cent,i} = C_{Q,i} \frac{\partial(E_F - E_i)}{\partial(E_i - E_C)} \tag{8}$$

The non-parabolicity of the $InAs_{0.8}Sb_{0.2}$ QW band structure is included in the model by modifying the effective mass and 2D DOS using the non-parabolicity factor $\alpha$ as in (9) and (10),

where $m_\Gamma$ is the effective mass at the bottom of the Γ-valley, and $E$ is the total energy with respect to the bottom of the Γ-valley [52].

$$m^* = \frac{\hbar^2 k}{\partial E / \partial k} = m_\Gamma (1 + 2\alpha E) \tag{9}$$

$$DOS_{2D} = \frac{m^*}{\pi \hbar^2} = \frac{m_\Gamma (1 + 2\alpha E)}{\pi \hbar^2} \tag{10}$$

Figure 4-17 shows the equivalent circuit model showing the different components of the gate capacitance. The extraction of $C_{cent}$ requires solving Schroedinger and Poisson equations self-consistently to evaluate the subband energy levels ($E_i$-$E_C$) as a function of charge density. I have performed Nextnano [53] simulations to obtain $E_i$-$E_C$ as a function of $E_F$-$E_i$. Using the quantum well capacitance evaluated from (6), the gate capacitance is obtained using (11), where $C_{barrier}$ and $C_{ox}$ are the barrier and oxide capacitance respectively.

$$\frac{1}{C_g} = \frac{1}{C_{ox}} + \frac{1}{C_{barrier}} + \frac{1}{C_S} \tag{11}$$

The gate capacitance obtained in (11) is a function of the potential ($\Psi_{S,QW}$) in the QW. The applied gate potential is calculated from $\Psi_{S,QW}$ using the equivalent circuit model shown in Figure 4-17.

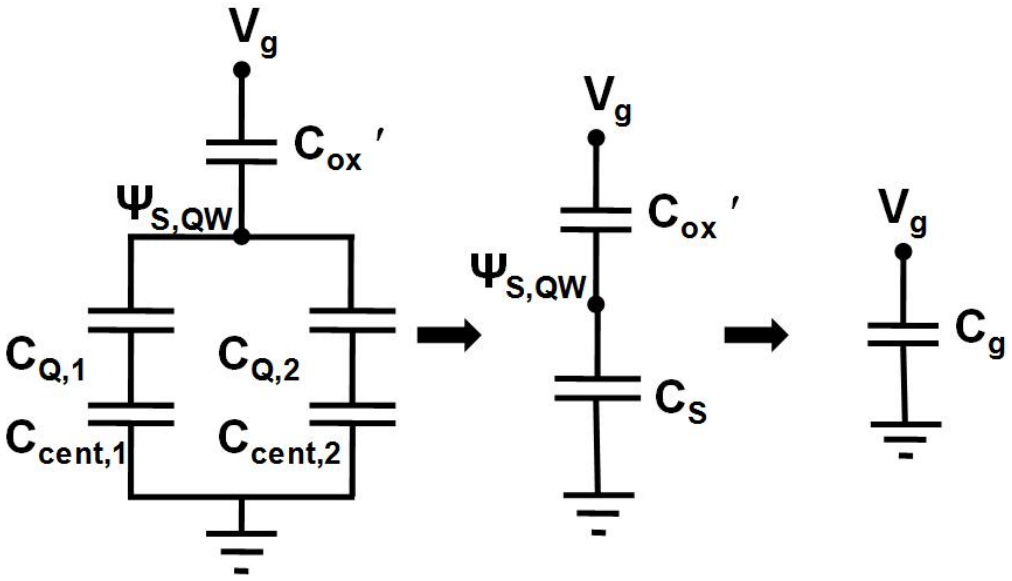



Figure 4-17. Equivalent circuit model of a QW-MOSFET showing the different components of gate capacitance. $C_{Q,i}$ stands for quantum capacitance of the *i-th* subband, $C_{cent,i}$ stands for centroid capacitance of the *i-th* subband, $C_{ox}'$ stands for the series combination of oxide and barrier capacitance and $\Psi_{S,QW}$ stands for the quantum well potential. Only two subbands are considered in the model

Figure 4-18 shows analytical modeling of gate capacitance of $InAs_{0.8}Sb_{0.2}$ QW-MOSFET with the numerical simulations (Nextnano). Effective mass at the bottom of Γ-valley is taken to be $0.018m_0$ for $InAs_{0.8}Sb_{0.2}$ [54]. The analytical model shows excellent agreement with the numerical simulation. This validation was first done for a parabolic band structure case ($\alpha$=0). The subband positions for evaluating the centroid capacitance were numerically obtained as a function of the Fermi level from Nextnano simulations for all the cases considered in this paper. Now, I incorporate the non-parabolicity of the band structure in our analytical calculations to model and analyze the experimental $C_g$-$V_g$ data obtained from the $InAs_{0.8}Sb_{0.2}$ QW-MOSFET after $D_{it}$ correction. Figure 4-19 (a) and (b) show the experimental $C_g$-$V_g$ data corrected for $D_{it}$ at 300K along with the analytical model. The effect of varying $\alpha$ on the different components of gate capacitance is also shown in Figure 4-19. For single effective mass approximation ($\alpha$=0), the quantum capacitance will not change with gate bias as the Fermi level moves above the first

subband in the QW. This is due to the constant density of states in the QW, and $C_Q$ reaches the quantum capacitance limit. As the Fermi level enters the second subband the capacitance starts to rise again as shown in Figure 4-19. This gives rise to a kink in the CV characteristics. Band parabolicity factor ($\alpha$ ) strongly influences the gate capacitance. Increasing $\alpha$ gives rise to increasing $C_Q$ even after the Fermi level moves above the first subband. Hence, the $C_Q$ and the $C_{cent}$ will keep increasing with gate bias. Best fit to the experimental data was obtained with $\alpha$ =2.5$eV^{-1}$ at 300K. Figure 4-20 shows the different components of the gate capacitance for the 300K $C_g$-$V_g$ data.

Similar analysis was done at multiple temperatures (77 K and 150 K) on different sets of devices to confirm the extracted effective mass and non-parabolicity. Details on these results can be found in [54].

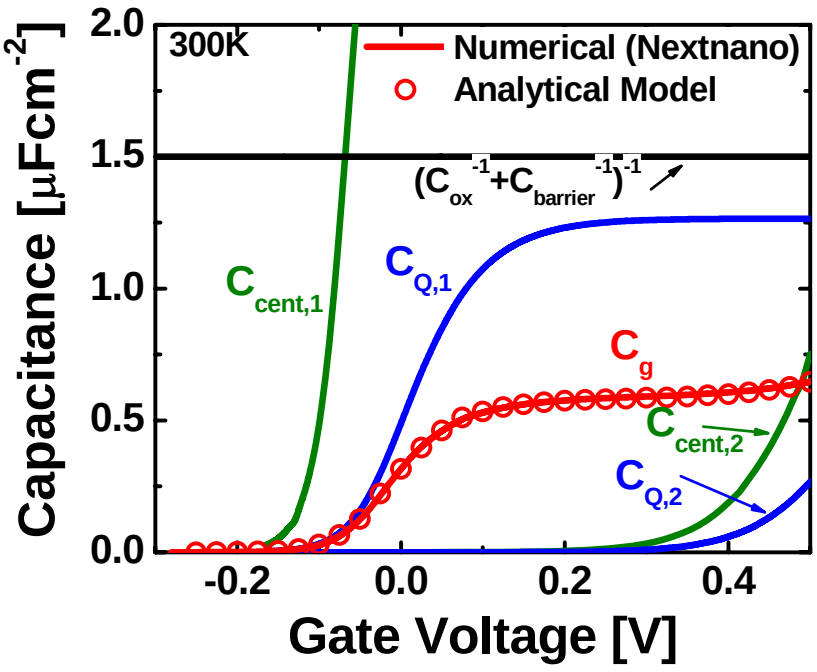



Figure 4-18. Analytical modeling of gate capacitance of $InAs_{0.8}Sb_{0.2}$ QW-MOSFET compared with numerical simulations (Nextnano)

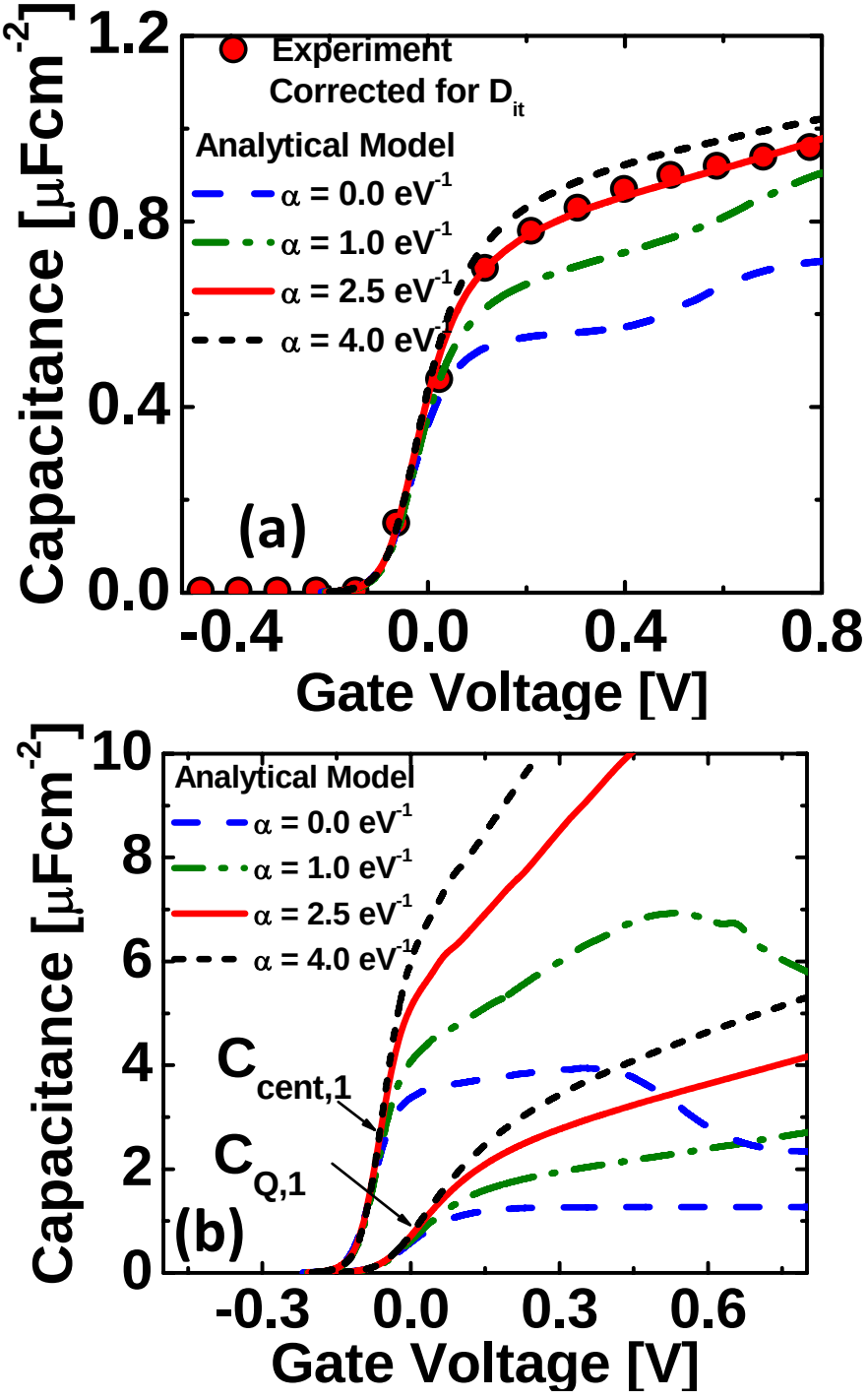



Figure 4-19. Effect of varying $\alpha$ on (a) the gate capacitance at 300K, and (b) the quantum and centroid capacitance at 300K. The kink visible in the CV curves in (a) for $\alpha$=0 and 1, is due to capacitance contributions from the second sub-band. Capacitance components of the second sub band are not shown in (b) for clarity. The drop in centroid capacitance for $\alpha$=0 and 1 in (b) is also due to second subband population. Best fit to the experimental data was obtained with $\alpha = 2.5 eV^{-1}$

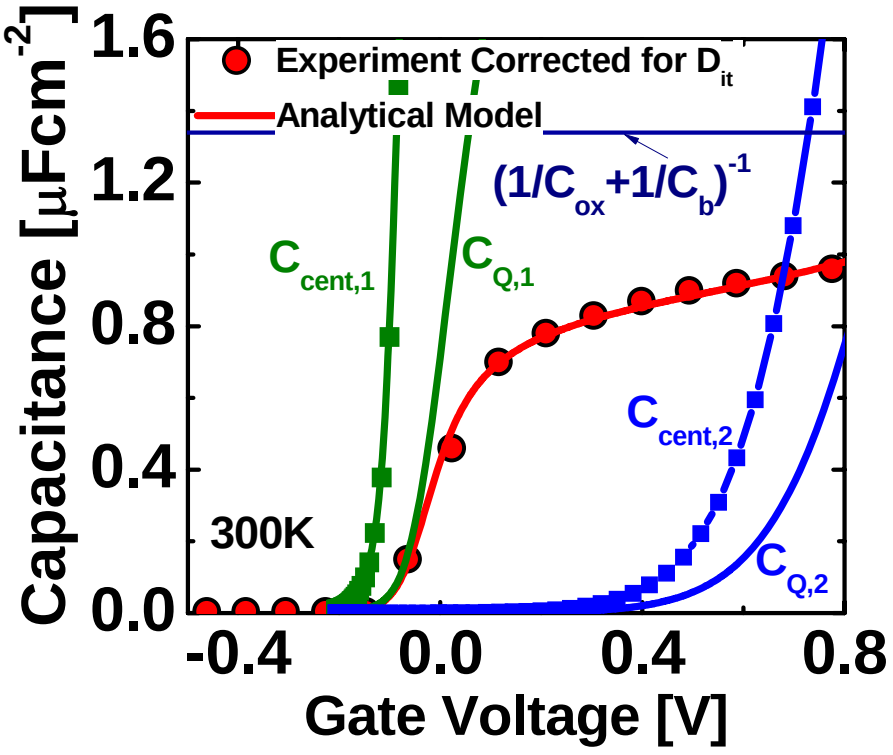



Figure 4-20. Components of the gate capacitance for the 300K $C_g$-$V_g$ data.

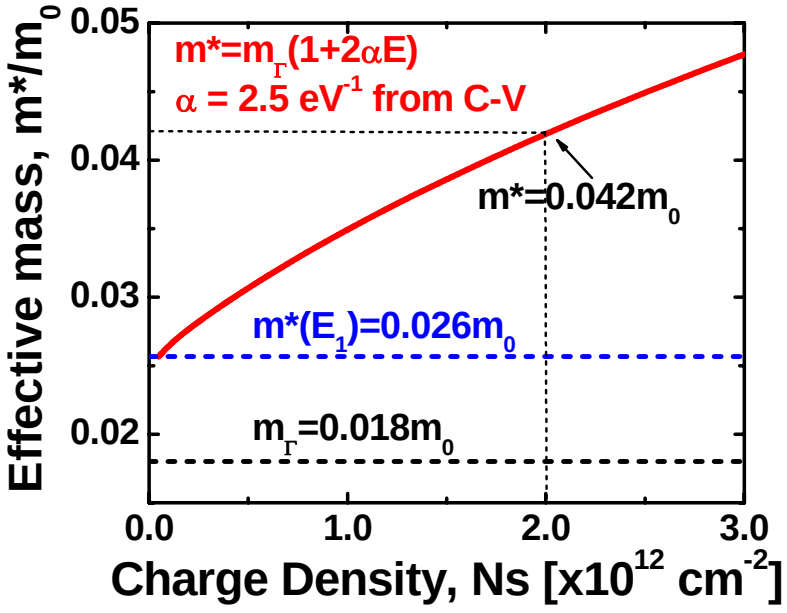



Figure 4-21. Effective mass extracted from the $C_g$-$V_g$ analysis as a function of charge density in the QW

Figure 4-21 shows the effective mass extracted from the $C_g$-$V_g$ analysis as a function of charge density in the QW. For a charge density of $2.0\text{x}10^{12} cm^{-2}$, the extracted effective mass is $0.042m_0$, which is 2.33 times higher than $m_\Gamma$ ($0.018m_0$) due to quantization and non-parabolicity**.** The non-parabolicity factor extracted from $C_g$-$V_g$ analysis ($\alpha = 2.5eV^{-1}$) is similar to that for InAs/AlSb QW heterostructure ($\alpha = 2.5eV^{-1}$) reported from cyclotron resonance measurements [56].

## IV. Shubnikov-de Haas Analysis for Effective Mass Extraction

The effective mass obtained from the capacitance modeling was verified using Shubnikov-de Haas (SdH) magnetotransport measurements on an $InAs_{0.8}Sb_{0.2}$ QW heterostructure (without dielectric) at low temperatures (2-15K) and high magnetic fields (0-9 tesla). The magnetotransport measurements, in standard four probe DC configuration, were carried out using Quantum Design Model 6000 Physical Property Measurement System (PPMS), with a base temperature of 1.8 K and magnetic field in the range of 0-9 tesla. Figure 4-22 (a) and (b) show the measured sheet resistance ($R_{XX}$) and Hall resistance ($R_{XY}$) of the device from 0-9 tesla. Inset of the figures show the configurations to measure $R_{XX}$ and $R_{XY}$. SdH oscillations are observed in $R_{XX}$ at magnetic fields below 8 tesla. At fields above 8 tesla, quantum Hall plateaus appear in $R_{XY}$ and $R_{XX}$ tends to zero resistance. The magnetic field and temperature dependence of sheet resistance can be expressed as [57][58][59],

$$\frac{\Delta\rho_{XX}}{\rho_0} = R_S \frac{4\chi}{\sinh\chi} \exp\left(\frac{-\pi}{\omega_c \tau_q}\right) \cos\left(2\pi \frac{E_F}{\hbar\omega_c} + \phi\right) \qquad (12)$$

where $\rho_0$ is the sheet resistance at zero $B$, $\tau_q$ is quantum lifetime, $\chi = 2\pi^2 kT / \hbar\omega_c$, and $\omega_c = eB / m^*$ is the cyclotron frequency. The prefactor $R_s$ is associated with Zeeman splitting, and is assumed to be independent of the magnetic field in the following analysis [57]. While extracting the effective mass from SdH oscillations, the background magnetoresistance was corrected as follows. The envelope of maxima (minima) of the $\rho_{XX}$ oscillations was evaluated from the peak (valley) in the $\rho_{XX}$ as a function of $B$. The average of the two envelopes gave the background magnetoresistance which was subtracted from the measured $\rho_{XX}$.

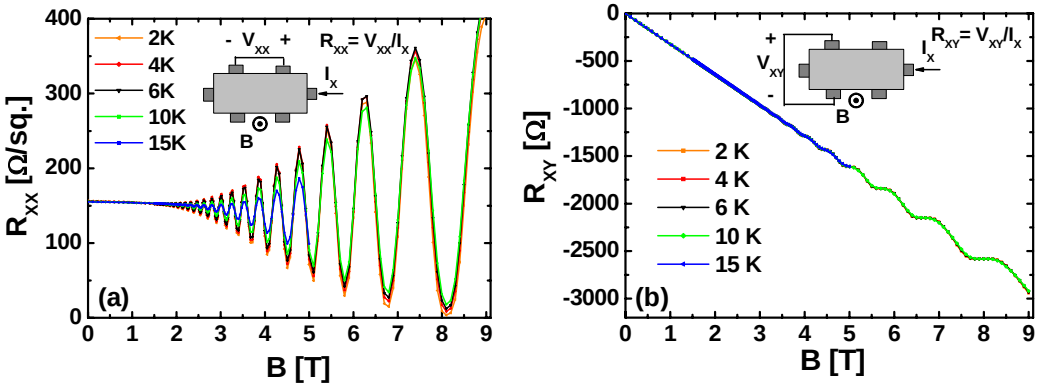



Figure 4-22. Measured sheet resistance ($R_{XX}$) and (b) Hall resistance ($R_{XY}$) of the $InAs_{0.8}Sb_{0.2}$ QW-heterostructure from 0-9 tesla. Insets in the figures show the configurations employed to measure $R_{XX}$ and $R_{XY}$

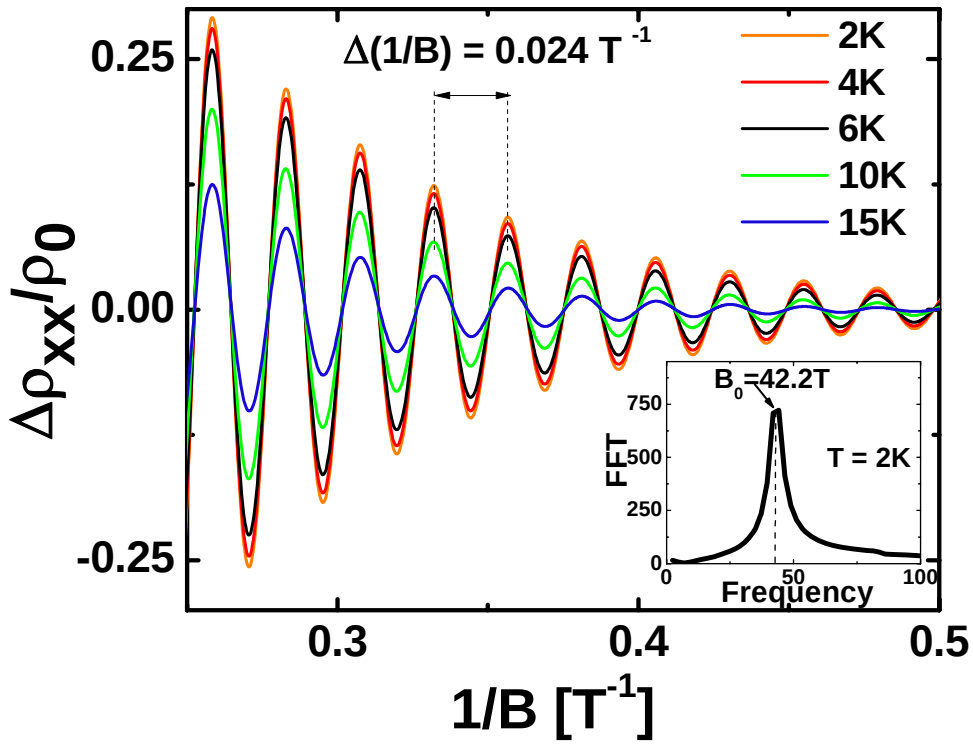



Figure 4-23. Periodic SdH oscillations in $\Delta\rho_{XX}/\rho_0$ (after removing the background contribution) as a function of *1/B*. Fast Fourier Transform (FFT) of $\Delta\rho_{XX}/\rho_0$ vs *1/B* is shown in the inset

Figure 4-23 shows the periodic SdH oscillations in $\Delta\rho_{XX}/\rho_0$ (after removing the background contribution) as a function of *1/B*. FFT of $\Delta\rho_{XX}/\rho_0$ vs *1/B* is shown in the inset of Figure 4-23. There is a well resolved peak at the fundamental oscillation period $B_0$=42.2 *T*. From the period of oscillation, *Δ(1/B)* =0.024 $T^{-1}$, the sheet carrier density can be obtained as $N_S = 2q/h\Delta(1/B) = 2.01x10^{12}\,cm^{-2}$. The carrier density obtained from period of SdH oscillations is independent of the device dimensions or QW thickness.

The analytical procedure to extract the effective mass is as follows. From (12), a plot of $Ln\left(\Delta\rho_{XX}/\rho_0\right)$ *vs* $Ln\left(\chi/\sinh\chi\right)$ gives a straight line with slope=1. $Ln\left(\Delta\rho_{XX}/\rho_0\right)$ is from the experimentally measured magnetoresistance data as a function of temperature, and $Ln\left(\chi/\sinh\chi\right)$ is calculated as a function of temperature using $m^*$ as an adjustable parameter. The correct value of $m^*$ gives a slope of 1 for the graph. Figure 4-24 shows the extraction procedure at $B$=2.54 $T$ and $B$=3.01 $T$. The extracted effective mass from the analysis is $0.043m_0$ at a sheet carrier density of $2.01x10^{12}cm^{-2}$ (from the period of SdH oscillations). The effective mass extracted from the *C-V* analysis in the previous section is very well in agreement with the SdH analysis. Figure 4-25 shows the Dingle plot [60] of $Ln\left(\frac{\Delta\rho_{XX}}{\rho_0}\frac{\sinh\chi}{4\chi}\right)$ *vs* $1/B$ using $m^*$=$0.043m_0$, which gives a universal straight line for all temperatures as given by (12). The slope of the line is $-\pi m^*/q\tau_q$ which yields a quantum lifetime of $\tau_q = 0.065ps$. The assumption that $R_s$ is independent of magnetic field is justified from Figure 4-24 and Figure 4-25 which give good straight lines as expected from (12). The ratio of transport time $\tau = 0.5ps$ obtained from quantum well electron mobility at 2K, to the quantum scattering time is ~7.5. This indicates that the dominant scattering mechanism in the $InAs_{0.8}Sb_{0.2}$ QW-heterostructure (without dielectric) at low temperatures is due to ionized impurities in the $In_{0.2}Al_{0.8}Sb$ barrier or interface charge at the barrier-QW interface, as observed in the case of GaAs/$Al_xGa_{1-x}As$ QW-heterostructure [61].

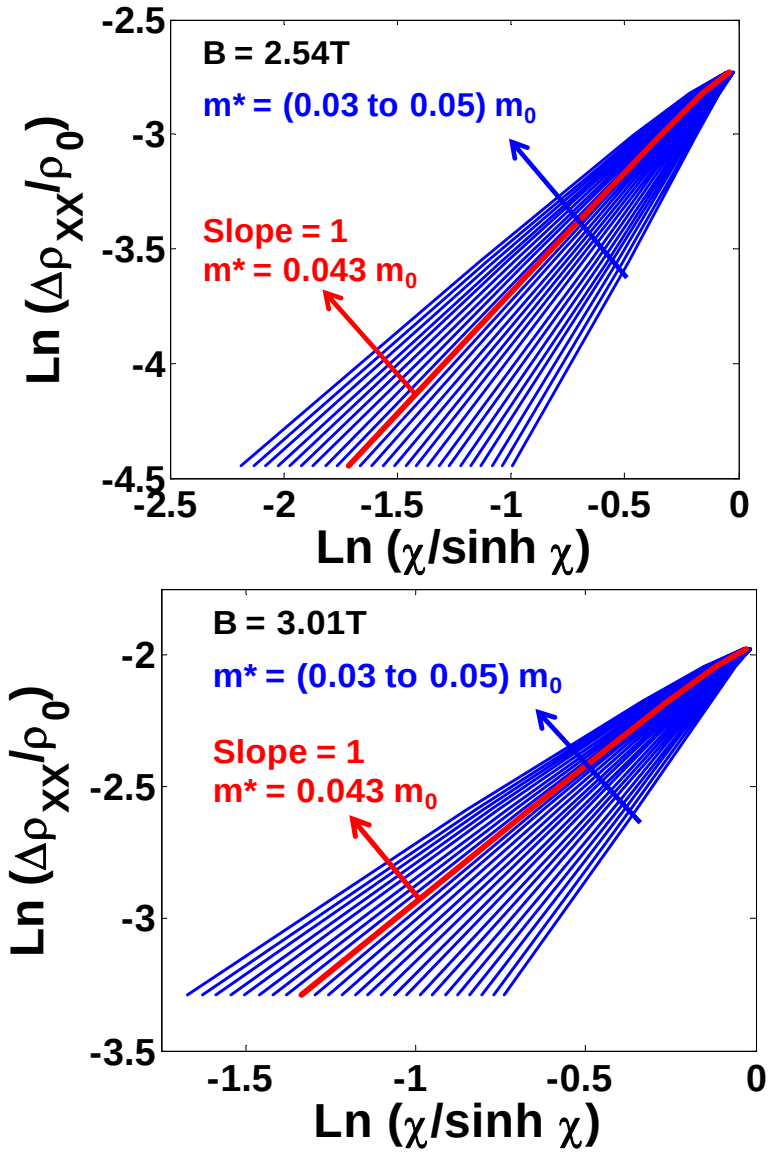



Figure 4-24. Plot of $Ln\left(\Delta\rho_{XX}/\rho_0\right)$ *vs* $Ln\left(\chi/\sinh\chi\right)$ for (a) $B$=2.54$T$, and (b) $B$=3.01$T$ to extract effective mass. Correct value of effective mass gives a slope of 1 for the graph

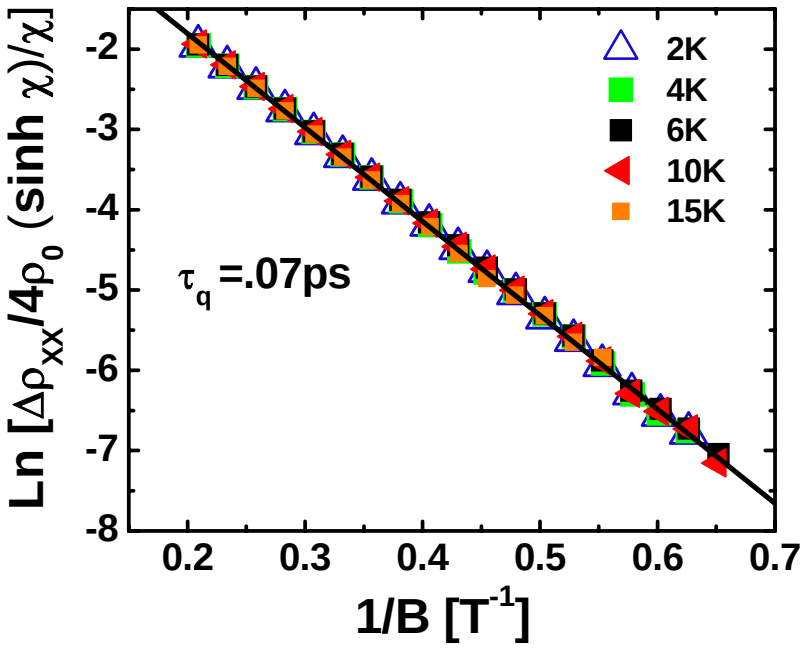



Figure 4-25. Dingle plot used to extract quantum lifetime

## V. Gate Capacitance Scaling Projection

In this section, I provide a quantitative estimate of the various factors determining gate capacitance scaling in future arsenide-antimonide QW-MOSFETs. As shown in the previous sections, both the quantization and the non-parabolicity increase the effective mass in the QW which increases the quantum capacitance, $C_Q$, and the centroid capacitance, $C_{cent}$. As we scale the gate length of future generation QW-MOSFETs, we need to scale the thickness of the semiconductor barrier and the quantum-well, to maintain acceptable short channel effects. Thinner quantum wells will exhibit higher $C_{cent}$ due to less change in the sub-band energy levels with Fermi level position [62], and higher $C_Q$ as well due to increased density of states at higher energy, for a given sheet carrier density, $N_s$, in the QW.

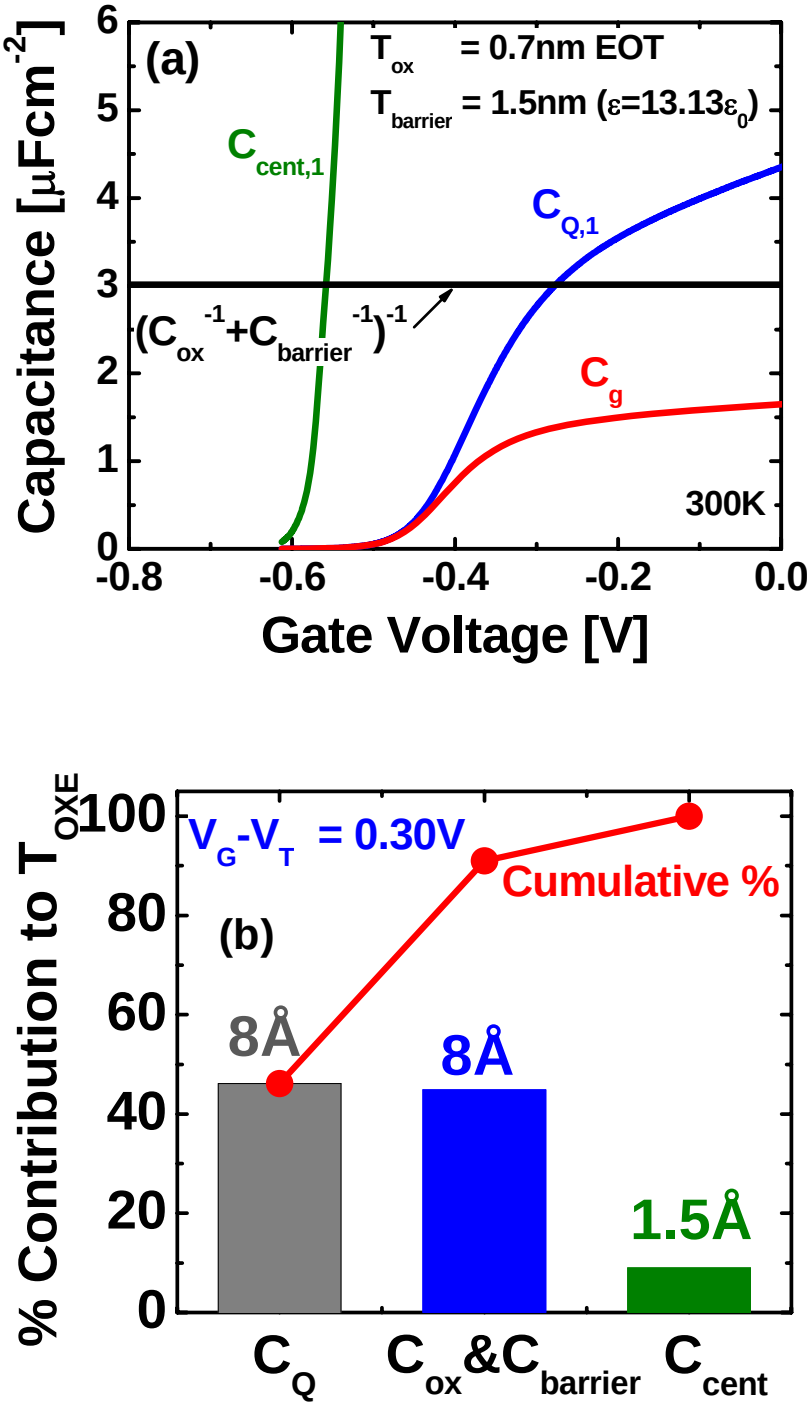



Figure 4-26. (a) Components of the gate capacitance of $InAs_{0.8}Sb_{0.2}$ QW-MOSFET with a scaled dielectric and barrier, and (b) Percentage contribution of various components of gate capacitance to $1/C_g$

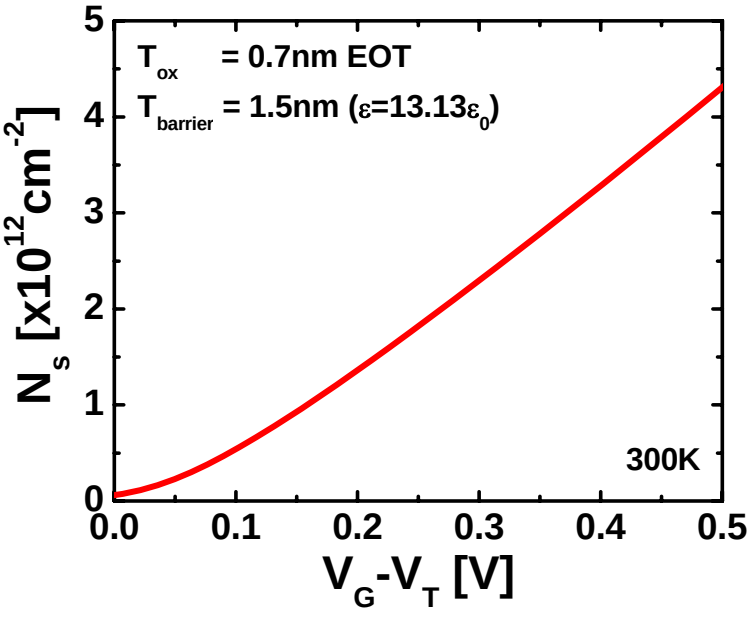



Figure 4-27. Sheet charge density in the quantum well as a function of gate overdrive for $InAs_{0.8}Sb_{0.2}$ QW-MOSFET with a scaled oxide and barrier. The threshold voltage is defined at the gate bias for which $N_s = 5x10^{10}\ cm^{-2}$

Figure 4-26 (a) and (b) show the various components of the gate capacitance of $InAs_{0.8}Sb_{0.2}$ QW-MOSFET, with 5nm thick quantum well, 1.5nm thick $In_{0.2}Al_{0.8}Sb$ barrier (0.45nm EOT) and a thin high-κ dielectric (0.7nm EOT) on top of the barrier. For a gate overdrive of 0.35V (~two-third of $V_{DD}$=0.5V), the oxide and barrier capacitance together contribute to about half (53%) of $1/C_g$, whereas the quantum and centroid capacitance contribute to the remaining half, with $C_Q$ (39% of $1/C_g$) being more limiting factor than $C_{cent}$ (8% of $1/C_g$).. The charge density in the QW for 0.35V gate overdrive is ~ $3.5x10^{12}cm^{-2}$ [Figure 4-27]. This implies that the oxide and barrier capacitance are as significant as quantum capacitance for gate capacitance scaling in MOS-QWFETs in the arsenide-antimonide material system.

Table 4-1. Table comparing the capacitance components of Sb nMOSFET with the scaled gate stack and that of 40nm $L_G$ strained Si. The composite barrier of Sb nMOSFET is same has the same EOT as that of the high-κ/SiON gate stack of the strained Si MOSFET.

| | $V_G$-$V_T$ | $C_G$ [μF/cm²] | Composite Oxide, $T_{OX}$ | Channel Layer, $T_{OXE}$ | Total $T_{OXE}$ | $N_s$ [/cm²] | $v_{eff}$ [cm/s] |
|---|---|---|---|---|---|---|---|
| 40nm $L_G$ Strained Si (G. Dewey et al., IEDM 2009) | 0.3 V | 2.45 | 8 Å (High-κ / SiON) | 6 Å | 14 Å | $4.5x10^{12}$ | $0.75x10^{7}$ |
| InAsSb QW $T_{QW}$=5nm Simulation | 0.3 V | 1.97 | 8 Å | 9.5 Å $C_Q$ =8Å $C_{cent}$=1.5Å | 17.5Å | $3.5x10^{12}$ | $2.7x10^{7}$ |

Table 4-1 compares the capacitance components of Sb nMOSFET with the scaled gate stack and that of 40 nm $L_G$ strained Si. The composite barrier of Sb nMOSFET is same has the same EOT as that of the high-κ/SiON gate stack of the strained Si MOSFET. For gate overdrive of 0.3 V, the electrical oxide thickness of inversion layer for Sb NMOSFET is 3.5 Å more than that of the Si NMOS. As a result the carrier density is 1.28x lower than that of Si NMOS. However, the enhancement in carrier velocity (3.6x) makes up for the less charge in the Sb MOSFET and hence the drive current for the Sb NMOSFET will be better than the Si NMOSFET at low $V_{DD}$.. Hence at low $V_{DD}$, low DOS mass problem is less of an issue due to enhanced quantization and non-parabolicity of the Sb QW MOSFET.

## VI. Conclusions

In this chapter, I presented a physics-based analytical model to extract the quantum capacitance and non-parabolicity factor in $InAs_{0.8}Sb_{0.2}$ QW-MOSFET. The effective mass extracted from $C_g$-$V_g$ analysis is validated through SdH measurements at low temperatures (2K-15K) and high magnetic fields (0-9T). Effective mass of $0.043m_0$ was obtained at $N_s$=$2.0x10^{12}$

$cm^{-2}$ (from SdH as well as $C_g$-$V_g$ analysis), which is 2.33 times higher than the Γ-valley mass of bulk $InAs_{0.8}Sb_{0.2}$. Non-parabolicity factor of 2.5 $eV^{-1}$ was obtained from $C_g$-$V_g$ modeling. The sheet carrier density as a function of temperature from Hall measurements was self-consistently modeled using the $m^*$, $\alpha$ and the Fermi level position from $C_g$-$V_g$ analysis. Gate capacitance scaling study of $InAs_{0.8}Sb_{0.2}$ QW-MOSFET, with 5nm thick quantum well, 1.5nm $In_{0.2}Al_{0.8}Sb$ barrier (0.45nm EOT) and a thin high-κ oxide (0.7nm EOT) shows that the oxide and barrier capacitance limits the gate capacitance (53% of $1/C_g$), more than the $C_Q$ (39% of $1/C_g$) and the $C_{cent}$ (8% of $1/C_g$), for a gate overdrive of 0.35V (~two-third of $V_{DD}$=0.5V).

In summary, low DOS mass problem is less of an issue at low $V_{DD}$ due to enhanced quantization and non-parabolicity of the Sb QW MOSFET. The enhancement in carrier velocity makes up for the less charge in the Sb MOSFET and hence the drive current for the Sb NMOSFET will be better than the Si NMOSFET at low $V_{DD}$.

# Chapter 5

# Future Works: P-channel Antimonide MOSFETs

## I. Summary on N-channel Antimonide MOSFETs

In the previous chapters, I have discussed the design, fabrication and characterization of Antimonide (Sb) quantum well (QW) MOSFETs with integrated high-κ dielectric (1nm$Al_2O_3$-10nm $HfO_2$). The long channel Sb NMOS exhibits effective electron mobility of 6,000 $cm^2/Vs$ at high field (2 x $10^{12}$ /$cm^2$ of charge density ($N_s$)), which is the highest reported value for any III-V MOSFET. The short channel Sb NMOSFET ($L_G$ = 150nm) exhibits a cut-off frequency ($f_T$) of 120GHz, $f_T$ - $L_G$ product of 18GHz.μm and source side injection velocity ($v_{eff}$) of 2.7x$10^7$ cm/s, at drain bias ($V_{DS}$) of 0.75V and gate overdrive of 0.6V. The measured $f_T$ and $f_T x\ L_G$ are 2 x higher, and $v_{eff}$ is 4x higher than Si NMOS (1.0-1.2V $V_{DD}$) at similar $L_G$, and are the highest for any III-V MOSFET. I also measured quantum capacitance and band non-parabolicity factor of Sb NMOSFETs and concluded that channel "DOS bottleneck" is not an issue for gate stack scalability, for low $V_{DD}$ application. Based on the experimentally measured $v_{eff}$ and charge density, we can estimate the drive current for Sb QW MOSFET with gate lengths smaller than 15nm. For smaller $L_G$ devices, the QW is expected to be very thin (~5 nm) to control short channel effects. The carrier velocity in these devices is expected be ~ 2.7x$10^7$ cm/s based on the measurements explained in chapter 3, assuming that the velocity does not degrade much as the QW is thinned. The carrier densities in the Sb QW for the 15nm $L_G$ device will be of ~3.5x$10^{12}$ /$cm^2$ for gate overdrive of ~0.33V for a $V_{DD}$ of 0.5V, based on the experimental analysis in chapter 4. Now assuming an external source resistance of ~ 80 Ω.μm (similar to that of state-of-the art Si), we can expect the drive current to be ~1 mA/ μm at 0.5V $V_{DD}$.

The key challenges to be addressed in obtaining this performance figure of merit are, maintaining high effective velocity for thin QW channels (< 5nm thickness), obtaining a reasonable external resistance at the required footprint and acceptable short channel effects. As we saw in the previous chapters, high external resistance ($R_S$>500 Ω.μm) high $D_{it}$ for the gate stack (5x10$^{12}$ to 1x10$^{13}$ /cm$^2$/eV) are the main show stoppers for these devices. These issues need to be studied in detail for the Sb QW MOSFETs. Antimonide transistors are really promising for high-performance low-power logic applications, if the above issues are addressed. For these devices to compete with the state-of-the-art Silicon tri-gate devices, the device architecture has to evolve from a planar to three-dimensional fashion, or a gate wrap-around structure.

## II. P-channel Antimonide MOSFETs

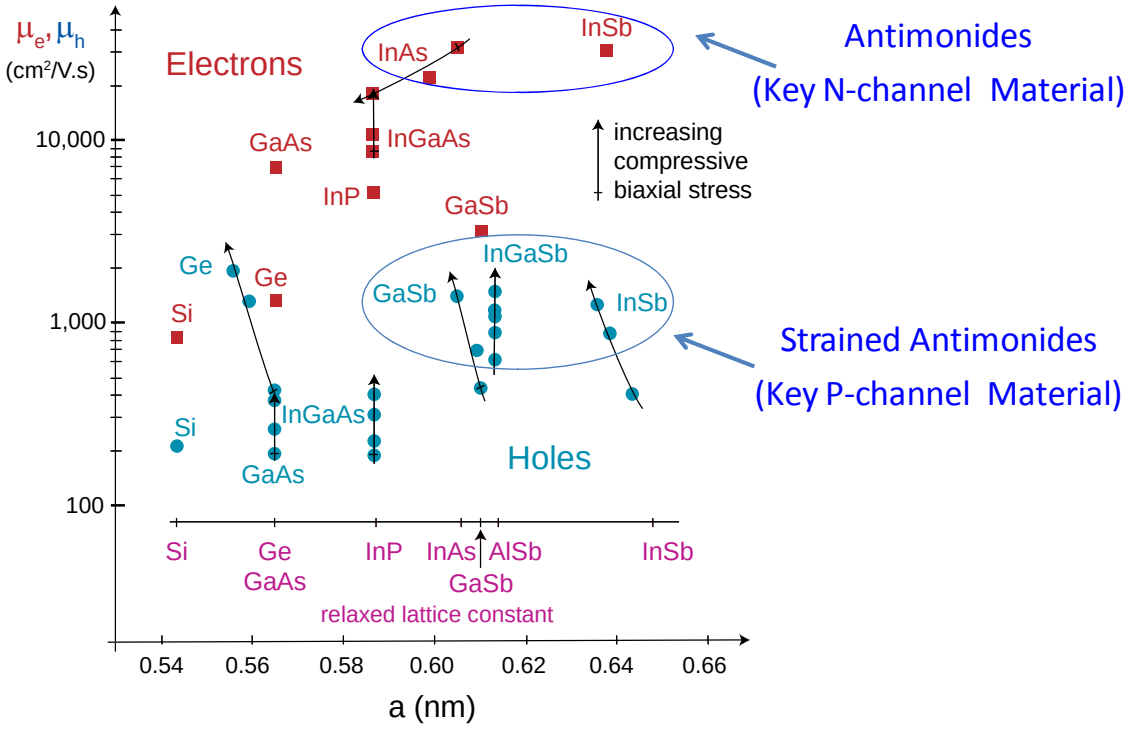



Figure 5-1. Electron and hole mobility of various III-V compound semiconductors [63]. Antimonides are very attractive since they have high electron as well as high hole mobility.

For logic operation, high channel III-V pMOS devices need to be integrated with the Sb NMOS. Figure 5-1 shows the electron and hole mobility of various III-V compound semiconductors [63]. Antimonides are very attractive p-channel solutions since they have high electron as well as high hole mobility. Ge, InSb and InGaSb based materials have the highest hole mobility. However it is preferred to have antimonide based p-channel devices than Ge p-channel devices for ease of integration with an Sb NMOSFET device.

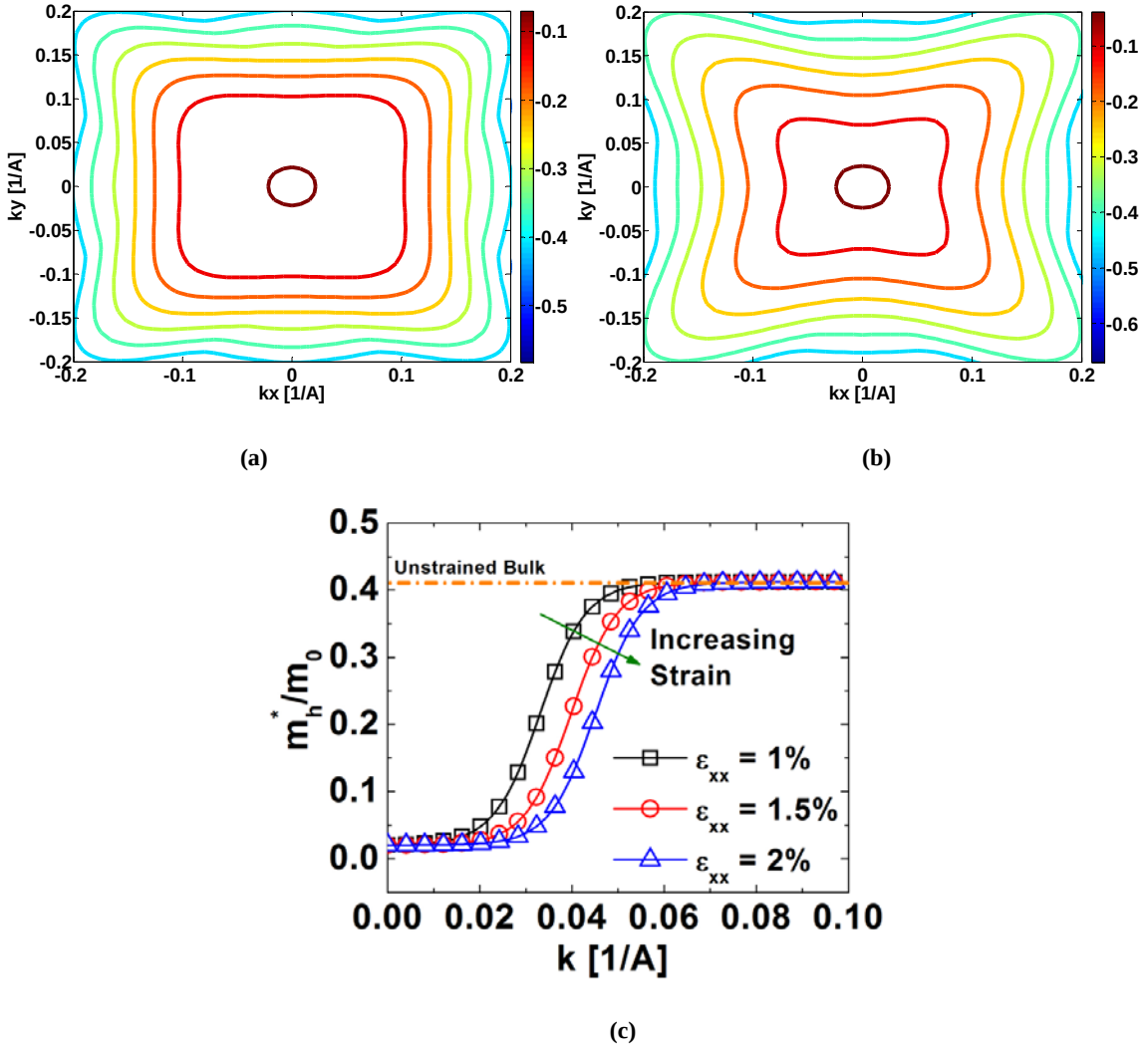



Figure 5-2. **(a)** Constant energy surfaces of the valence band of bulk InSb (unstrained) **(b)** Constant energy surfaces of the valence band of bulk InSb at 2% compressive strain **(c)** 6-band k.p simulation of in-plane effective hole mass as a function of energy for different compressive strain levels in InSb. For a given energy, higher compressive strain results in lower effective hole mass.

Currently we are investigating strained InSb p-channel quantum well MOSFETs to complement the n-channel InAsSb MOSFETs. Another factor for choosing InSb p-channel over the InGaSb p-channel devices is that it could potentially enable NMOS device fabrication on the same material system itself. Figure 5-2 (a) shows the constant energy surfaces of the valence band of bulk InSb at different strain levels (unstrained and 2% compressive strain).

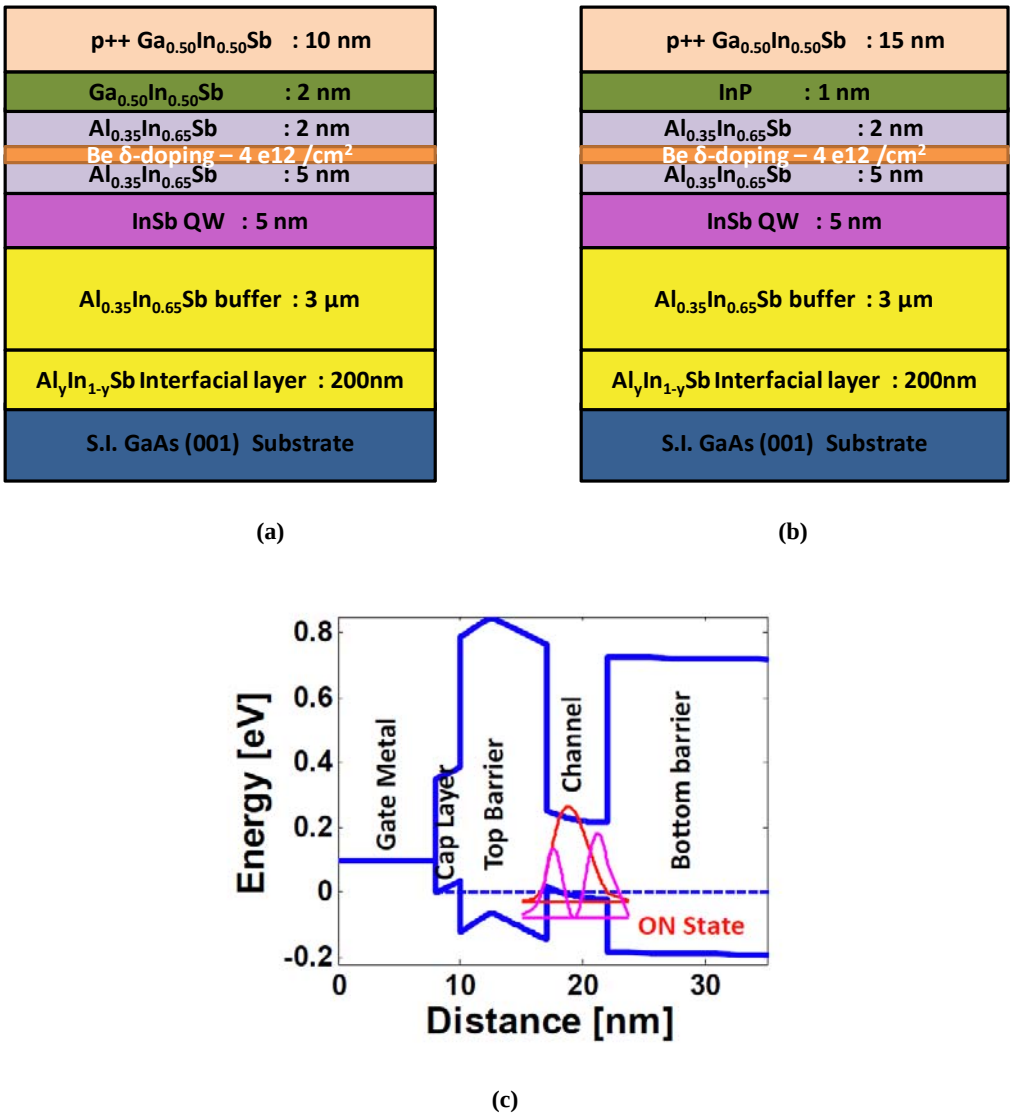
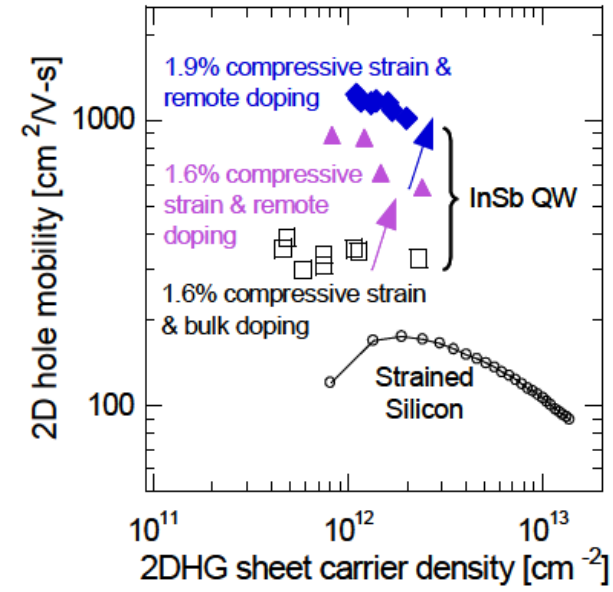
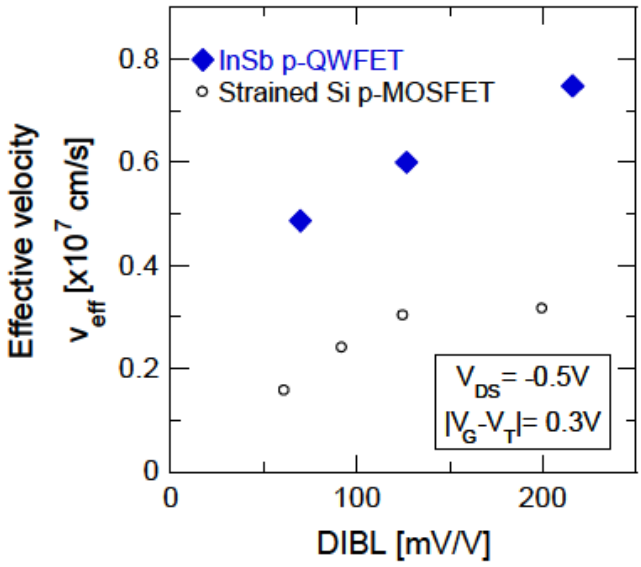



Figure 5-3. **(a-b)** Schematic of the p-channel InSb quantum well heterostructure with $Ga_{0.5}In_{0.5}Sb$ or InP cap layer. The quantum well is 2% compressively strained. The $Ga_{0.5}In_{0.5}Sb$ or InP cap layer is used for obtaining a high quality interface with the high-κ dielectric **(c)** Energy band diagram of the quantum well heterostructure under the gate (without the dielectric) showing good confinement of holes in the InSb channel.




**(a)**




**(b)**

Figure 5-4. (a) Hole mobility vs. sheet carrier density measurements for InSb QW showing mobility improvement with increasing compressive strain and remote doping. (b) Effective hole velocity (veff) vs. DIBL comparing InSb p-channel compressively strained QWFETs to strained Si p-channel MOSFETs at $V_{DS}$= -0.5V and $|V_G-V_T|$=0.3V. (Source: Intel, IEDM 2008 [64])

I have designed quantum well layer structures with 1.9% compressive strain on the InSb quantum well. Figure 5-3 (a-b) shows the schematic of the layer structure. The $Al_{0.35}In_{0.65}Sb$ barrier layer is δ-doped with Be to provide holes to the access region of the transistor. A thin 2nm $Ga_{0.5}In_{0.5}Sb$ layer or InP layer is used for dielectric integration. Figure 5-4 shows the expected hole mobility of the as grown device layers and the hole velocity of the Sb pMOSFET. This data is obtained from [64] where a similar p-channel structure has been studied but without high-κ dielectric. The measured Hall mobility of our structures is 765 $cm^2/Vs$ at a hole density of 3.6 x $10^{12}$ $/cm^2$. This data agree with the expected Hall mobility vs sheet carrier density data from [64] shown in Figure 5-4. Another key difference between our structure and the structure in [64] is that we have cap layers of InGaSb and InP for dielectric integration. However we expect that the transport properties of the InSb QW will be similar for both structures. The devices exhibit 5x higher hole mobility and more than 2x higher short channel velocity compared to strained Si, showing promise for high performance p-channel MOSFETs.

## III. Future works

Gate stack quality and external resistance and key issues that need to be addressed for both n and p channel antimonide devices. For these devices to compete with the state-of-the-art Silicon tri-gate devices, the device architecture has to evolve from a planar to three-dimensional fashion, or a gate wrap-around structure. The scalability of antimonide devices needs to be addressed by fabricating and characterizing non-planar multi-gate transistors. Antimonide transistors are really promising for high-performance low-power logic applications, if the above issues are addressed.

## Appendix: Process Flow for Antimonide QW MOSFET Fabrication

The fabrication details of the antimonide transistors are explained in detail below.

1. **Alignment Marker Deposition**

   - Clean sample using Acetone (1 min)/ IPA (1min) / DI water rinse (10s)/ $N_2$ dry
   - Spin coat the sample
   - PMMA-MAA EL 11 (D09/20/60) – bake @150C for 3 min
   - PMMA 950 A3 (D09/40/45) – bake @180C for 3min
   - Write alignment marker patterns using electron beam lithography at a dose of 400μC/cm$^2$ and a beam size of 200nm
   - Develop the pattern using MIBK: IPA (1:1) - 1min, IPA 15s, DI water rinse and $N_2$ dry
   - Observe the patterns under microscope
   - Oxygen descum process for 20s using Plasmatherm 720 tool (Recipe: 45sccm $O_2$, 100 W at 100 mTorr base pressure)
   - Dip for 30s in 6:1 BOE to remove native oxides
   - Deposit metal stack (20 nm Pd/ 30 nm Ti/ 100 nm Au)
   - Lift-off in PG Remover for 30 min
   - Observe under microscope to verify that lift-off is clean

2. **Source Pad Deposition**

The source pad and drain pad depositions are done in two different steps to get the source and drain as close as 300nm. Patterning the source and drain together in one step will cause the patterns to merge during e-beam lithography step.

- Clean sample using Acetone (1 min)/ IPA (1min) / DI water rinse (10s)/ $N_2$ dry
- Spin coat the sample
- PMMA-MAA EL 11 (D09/20/60) – bake @150C for 3 min
- PMMA 950 A3 (D09/40/45) – bake @180C for 3min
- Write source pad patterns using electron beam lithography at a dose of 330μC/cm$^2$ and a beam size of 100nm. Align the source pads to the markers.
- Develop the pattern using MIBK: IPA (1:1) - 1min, IPA 15s, DI water rinse and $N_2$ dry
- Observe the patterns under microscope
- Oxygen descum process for 20s using Plasmatherm 720 tool (Recipe: 45sccm $O_2$, 100 W at 100 mTorr base pressure)
- Dip for 30s in 6:1 BOE to remove native oxides
- Deposit metal stack (15 nm Pd/ 15 nm Pt/ 120 nm Au)
    - Pt deposition rate needs to be lower than 0.2Å/s, otherwise the resist will develop cracks due to the stress generated on the Pt film
- Lift-off in PG Remover for 30 min
- Observe under microscope to verify that lift-off is clean

**3. SEM Imaging of Source Pad**

This step is required only once for calibrating the mask design.

- Take SEM images to find out the gap between the two source-pads in the RF devices. If the pads widen during e-beam lithography, then the drain pads need to be adjusted in the mask to correct for the widening of source pads. Otherwise the devices with small source-drain spacing (<300nm) will merge.

**4. Drain Pad Deposition**

- Clean sample using Acetone (1 min)/ IPA (1min) / DI water rinse (10s)/ $N_2$ dry
- Spin coat the sample
- PMMA-MAA EL 11 (D09/20/60) – bake @150C for 3 min
- PMMA 950 A3 (D09/40/45) – bake @180C for 3min
- Write drain pad patterns using electron beam lithography at a dose of 330μC/cm$^2$ and a beam size of 100nm. Align the drain pads to the markers
- Develop the pattern using MIBK: IPA (1:1) - 1min, IPA 15s, DI rinse and $N_2$ dry
- Observe the patterns under microscope
- Oxygen descum process for 20s using Plasmatherm 720 tool (Recipe: 45sccm $O_2$, 100 W at 100 mTorr base pressure)
- Dip for 30s in 6:1 BOE to remove native oxides
- Deposit metal stack (15 nm Pd/ 15 nm Pt/ 120 nm Au)
    - Pt deposition rate needs to be lower than 0.2Å/s, otherwise the resist will develop cracks due to the stress generated on the Pt film
- Lift-off in PG Remover for 30 min
- Observe under microscope to verify that lift-off is clean

**5. SEM Imaging of Source to Drain Spacing**

This step is required only once for calibrating the mask design.

- Take SEM images to find out the gap between the source and drain pads. The mask design needs to be calibrated with the required source to drain spacing.

**6. Device Isolation Lithography**

- Clean sample using Acetone (1 min)/ IPA (1min) / DI water rinse (10s)/ $N_2$ dry
- Spin coat the sample

- PMMA-MAA EL 11 (D09/20/60) – bake @150C for 3 min
- PMMA 950 A3 (D09/40/45) – bake @180C for 3min
- Write isolation patterns using electron beam lithography at a dose of 330μC/cm$^2$ and a beam size of 100nm. Align the pattern with the markers
- Develop the pattern using MIBK: IPA (1:1) - 1min, IPA 15s, DI water rinse and $N_2$ dry
- Observe the patterns under microscope

**7. Device Isolation using Reactive Ion Etching**

- Isolate the device regions using Reacting Ion Etching in the Versalock plasma etching tool. The recipe details are given below.
    - Recipe name: PM1 AlSbn
    - Gas Flow: Ar 30 sccm ($Cl_2$ could be used, however the etch rate increases very much, and has large variability. Using just Ar gas gives slow and consistent etch rate)
    - Power: RF1 100 W, RF2 500 W.
    - Pressure 2 mTorr
    - Time to etch 100 nm ~75s

The etch rate needs to be calibrated on test samples. Typically about 60 nm to 100 nm of etch depth is required to isolate the devices. Too low of etch depth leads to poor isolation between devices and will have parallel conduction from source to drain. Too deep of an isolation will cause issues with gate patterning as the gate finger needs to climb over the mesa region to contact the device. Typical time to etch 100 nm is about 70 s – 80 s. Tool baseline changes can affect this etch rate and it is recommended to run a test piece prior to etching the device.

- Measure the electrical isolation between TLM pads on the mesa floor

    - Leakage between TLM pads on the mesa floor or between two isolated devices should be less than 100 nA at 1 V
- After etching, the device, lift-off the sample in PG Remover for 30 min
- If the resist does not clear off completely, oxygen descum in PT720 for 30 s to 1 min is required (Recipe: 45sccm $O_2$, 100 W at 100 mTorr base pressure)
- Observe the sample under microscope to verify that resist has been removed completely.

**8. Oxide Deposition**

Oxide deposition is done using Atomic Layer Deposition (ALD) tool in Nanofab or in the Plasma Enhanced Atomic Layer Deposition (PEALD) tool in Dr. Jackson's group

- Run the ALD $Al_2O_3$ recipe to deposit ~10nm of $Al_2O_3$ to coat the chamber
- Surface Preparation: Acetone, 30s, IPA 30s, HCl (1:20) for 10s, DI water rinse
    - DI water rinse needs to be done very well to clear off HCl from between pads which will otherwise lead to pitting the sample
    - Minimize the time between surface preparation and loading the sample to the ALD chamber
- Deposit 10cy $Al_2O_3$ + 100cy $HfO_2$ (10cy TMA prepulse) for 1 nm $Al_2O_3$ / 10 nm $HfO_2$ bilayer oxide stack. The cycles can be changed according to the required thickness of oxides
    - The ALD chamber will be at 250 C during the deposition with $N_2$ gas flowing during the deposition process. This will anneal the source drain contacts, and hence no separate annealing is required for the contacts.

**9. Rapid Thermal Annealing (RTA) of Oxide**

RTA will densify the oxide and reduce the gate leakage as well as passivate the interface states. RTA is done at 200C for 15 min in forming gas.

**10. Gate Pad and Finger Deposition**

- Clean the sample using DI water rinse (10s)/ $N_2$ dry
- Spin coat the sample
- PMMA-MAA EL 5.5 (D09/20/60) – bake @150C for 3 min
    - EL 5.5 gives better resolution to print small gate fingers
- PMMA 950 A3 (D09/40/45) – bake @180C for 3min
- Write gate pad patterns using electron beam lithography at a dose of 330μC/cm$^2$ and a beam size of 100nm. Align the gate to marker.
- Write gate finger patterns at a dose of 750μC/cm$^2$ and a beam size of 10 nm. Align the gate to marker.
- Develop the pattern using MIBK: IPA (1:1) - 1min, IPA 15s, DI water rinse and $N_2$ dry
- Observe the patterns under microscope
- Oxygen descum process for 10s using Plasmatherm 720 tool (Recipe: 45sccm $O_2$, 100 W at 100 mTorr base pressure)
- Deposit metal stack (20 nm Pd/ 80 nm Au)
    - The gate metal needs to be thicker than the mesa isolation depth so that the gate finger does not break as it climbs the mesa (The gate pad is in the mesa isolated region and the finger goes up the mesa and gates the device region).

- Too thick of metal deposition (>140 nm thick) using the EL 5.5 bottom resist could lead to lift off issues. In that case, tape lift-off process is preferred. In the tape lift-off process, a piece of scotch tape is pasted on to the top of the metal film (press firmly on corners of the sample and not on the device region). Slowly lifting the tape along the direction of gate fingers will remove the metal film from outside the device region. The resist can now be removed using Acetone or PG Remover.

- Lift-off in PG Remover for 30 min
- Rinse very gently with DI water and also dry with $N_2$ gun very gently, which could otherwise damage the gate fingers
- Observe under microscope to verify that lift-off is clean

Gate pattering is typically the last step in the fabrication process. In some cases, if the devices are not well isolated due to less mesa depth, the devices need to be re-isolated by following steps 6 and 7. The mask then needs to be adjusted such that the alignment error between the first and second isolation is accommodated in the mask during the re-isolation.

The devices are now ready for AC, DC and RF characterization.

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# VITA

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