The Pennsylvania State University

The Graduate School

Graduate Program in Materials Science and Engineering

CHARACTERIZATION OF LASER FIRED CONTACTS, LASER DOPED EMITTERS, AND FIXED CHARGE PASSIVATION FOR IMPROVED SILICON SOLAR CELLS

A Thesis in

Materials Science and Engineering

by

Brittany Lynn Hedrick

Submitted in Partial Fulfillment
of the Requirements
for the Degree of

Master of Science

August 2011

The thesis of Brittany Lynn Hedrick was reviewed and approved* by the following:

Suzanne E. Mohney
Professor of Materials Science and Engineering
Thesis Co-advisor

Joseph R. Flemish
Professor of Materials Science and Engineering
Thesis Co-advisor

S. Ashok
Professor of Engineering Science

T. DebRoy
Professor of Materials Science and Engineering

Joan M. Redwing
Professor of Materials Science and Engineering
Chair, Intercollege Materials Science and Engineering Graduate Degree Program

*Signatures are on file in the Graduate School

ABSTRACT

With the introduction of laser processing into silicon solar cell manufacturing, characterization and understanding of laser-material interactions and laser fired device performance is critical. To assess laser doping of the front-side emitters and laser firing of the rear-side contacts of silicon solar cells, several experiments were carried out to create and characterize laser fired contacts (LFCs) and laser doped emitters (LDEs). Additionally, an investigation of fixed charge layers for increased surface passivation performance was performed.

A cross-sectioning and selective plating method was developed to characterize the molten region of LFCs created with varying laser firing conditions. Delineation of the geometry and penetration depth of an LFC, within the silicon, was possible with this method, and the once-molten, laser fired region was measured to depths of tens of microns in the silicon substrate. Investigation of surface topography, diameter, and electrical performance of LFCs was carried out in previous work by Brennan DeCesar, and is briefly reviewed herein. Simulations of LFCs were performed by modeling devices of different diameter and doping densities to replicate trends in experimental resistance data, and to identify the concentration of Al in the fired contact region. Resistances simulated for LFCs modeled with doping densities above $1x10^{18}/cm^3$ matched best with experimental data, and the resistance of the contacts is dominated by spreading resistance from the heavily doped region (formed through laser firing) into the rest of the wafer.

Laser doped emitters were also fabricated and characterized through electrical characterization and cross-sectioning and junction delineation techniques. Doping of the emitters using phosphorus-doped amorphous silicon films, incorporated in the passivation layers, was found to be promising. Depths of LDEs within the silicon were much shallower than those of LFCs, due to the shorter pulse duration used in laser processing (μs rather than ms).

Passivation of silicon through the introduction of negative fixed charge was investigated using alumina (Al_2O_3) and hafnia (HfO_2) films deposited by atomic layer deposition (ALD). Layered structures with SiO_x capping films deposited by plasma enhanced chemical vapor deposition (PECVD) were also investigated. Passivation quality was characterized by measuring effective carrier lifetime using microwave photoconductive decay. The longest lifetimes achieved were over 1.5 ms, measured on a sample passivated with 10 nm Al_2O_3 and 100 nm SiO_x after a 5 min 350°C anneal. Fixed charge density was calculated through flat band voltage shifts in C-V measurements made using a mercury probe. Both the Al_2O_3 and HfO_2 samples exhibited negative fixed charge densities. Samples passivated with thin Al_2O_3 layers were found to have the largest negative fixed charge densities, up to $1x10^{13}/cm^2$. Additionally, the creation of an inversion layer due to fixed charge in passivation films deposited on high resistivity silicon substrates was investigated using contactless conductivity measurements and changes in sheet resistance. The presence of an inversion layer was detected by a decrease in sheet resistance and correlated to an increase in effective carrier lifetime for those samples annealed for 5 min at 450°C in a tube furnace, 450°C in a RTA, and 350°C on a hot plate.

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

GLOSSARY OF TERMS

AC – alternating current

$Al(CH_3)_3$ – trimethylaluminum, precursor for alumina ALD growth

Al_2O_3 – aluminum oxide or alumina

ALD – atomic layer deposition

ARC – anti-reflection coating, for reduced reflection at a solar cell's surface

a-Si:H – amorphous silicon, hydrogenated

a-$Si_{1-x}C_x$ – amorphous silicon carbide

a-SiC_x – amorphous silicon carbide

a-SiN_x:H–amorphous silicon nitride, hydrogenated

BOE – buffered oxide etch, consisting of hydrofluoric acid and ammonium fluoride and DI water

BSF – back surface field created at the rear side of a cell due to Al metallization

C_{ox} – capacitance of an oxide

C-V measurement – capacitance-voltage measurement

CVD – chemical vapor deposition

CZ – Czochralski, silicon growth technique

DI water – de-ionized water

e-beam deposition – electron-beam deposition

EBIC – electron beam induced current

FESEM – field emission scanning electron microscopy

FF – fill factor

FSF-IBC – front surface field interdigitated back contact back junction cell

FZ – float zone, silicon growth technique

H_2 – hydrogen gas

H_2O – water

HfO_2 –hafnium oxide or hafnia

HIT cell – Sanyo's high efficiency cell, the "heterojunction with intrinsic thin layer" device

HP – hot plate, used for annealing

I_o – saturation current, a measure of recombination in the scr

I-V measurement – current-voltage measurement

J_{sc}– short circuit current

LBIC – light beam induced current measurement

LCP – laser chemical processing

LCR meter – impedance, capacitance, resistance meter

LDEs – laser doped emitters

LFCs – laser fired contacts

LGBC – laser grooved buried contacts

LIMPID – laser induced melting of a pre-deposited impurity doping

L-SNMS – laser secondary neutral mass spectroscopy

m – slope of the qnr and scr regions on a log(I)-V plot

n+ a-Si:H – phosphorus doped a-Si:H

N_2 – nitrogen gas

N_2O – nitrous oxide gas

Nd:YAG laser – neodymium-doped yttrium aluminium garnet laser

Nd:YVO_4 laser – neodymium-doped yttrium orthovanadate laser

PECVD – plasma enhanced chemical vapor deposition

PERC – passivated emitter and rear cell

PERL – passivated emitter and rear locally diffused cell

PERT – passivated emitter rear totally diffused cell

PH_3 – phosphine gas

Q_f – fixed charge density

qnr – quasi neutral region, the p and n-type regions of a diode, away from the junction

r_s – series resistance

RTA – rapid thermal anneal or annealing furnace

scr – space charge region, the region of band bending in a diode

SEM – scanning electron microscopy

SiH_4 – silane gas

SIMS – secondary ion mass spectroscopy

SiN_x – silcon nitride deposited by PECVD

SiO_2 – silicon dioxide, thermally grown silicon oxide

SiO_x – silicon oxide as deposited by PECVD

SOD – spin on dopant

SRV – surface recombination velocity

TCAD – technology computer-aided design

TEM – transmission electron microscopy

TF– tube furnace, used for annealing

UV LED – ultraviolet light emitting diode

V_{FB} – flat band voltage, the voltage at the transistion point between accumulation and depletion

V_{oc} – open circuit voltage

μ-PCD – microwave photoconductive decay

φ_{MS} – metal-semiconductor work function difference

η – conversion efficiency

ACKNOWLEDGEMENTS

First, I would like to thank Dave Carlson, Lian Zhou, and the other scientists of BP Solar for their guidance and support of this research. Second, I would like to acknowledge the students with whom I worked on this research project: Brennan DeCesar, for his initial work with LFCs, and Jillian Woolridge, for her continued work on LDEs. Third, I would like to thank my advisors: Suzanne Mohney, for her guidance and expertise, Joe Flemish, for his guidance in the design of experiments and help in the fab, and Ted Reutzel, for his challenging questions and attention to detail. Fourth, I would like to thank all the students in Suzanne's lab group, for their friendship, insight, and support. Finally, I would like to thank all of my friends and family, for their love and encouragement; most of all my parents and my fiancé Wesley. Hebrews 12:1-3.

Chapter 1

Introduction

Device Components

Developed in 1954 by researchers at Bell Telephone, the first solar cell for commercial use was fabricated with an efficiency of 6% (1). The cell was based on a diffused p-n junction, fabricated in silicon, that successfully separated charge carriers generated by the absorption of solar radiation (1) (2). From that structure the basic solar cell design was born. In its simplest form a solar cell is intended to maximize the conversion of incident solar energy into electrical energy (2), and to do so any design requires three necessary components: a semiconducting substrate, a p-n junction, and metal/semiconductor contacts. The band gap in a semiconductor allows for certain wavelengths of electromagnetic radiation to be absorbed; those materials used in solar cells are selected to absorb wavelengths corresponding to the solar spectrum. The substrate comprises the active regions of the solar cell where photon absorption takes place and electron and hole charge carriers are generated (3). A homogeneous or heterogeneous p-n junction, or "charge separation engine", is required so that photogenerated charge carriers can be separated for current collection. Homogeneous junctions are formed in silicon by doping a region of the bulk n-type (p-type) substrate to be p-type (n-type). Heterogeneous junctions are formed by growing or depositing a different semiconductor material of a different dopant type and bandgap on top of silicon (3) (4). The space charge region (SCR) that forms in the p-n junction serves to separate electrons and holes absorbed in the bulk of the material, making them available for collection (3) (4). The metal/semiconductor contacts of the cell serve to collect the separated photogenerated carriers from the device, and maintain current flow to the external load on the

cell. These three components, or variations of them, will be found in any solar cell structure. Working together they allow the device to operate.

The basic structure of a bulk silicon solar cell is pictured in Figure 1-1. It features a base layer of silicon for light absorption, a rear-side, full area contact for carrier collection, and a front-side emitter region contacted by thin metal finger contacts, to allow incident light into the cell and create a front contact. The front surface the metal grid (as opposed to a full area, blanket metal contact) is necessary to reduce shading and limit optical losses, but it still provides adequate contact area to minimize resistive losses (5). The junction is present on the front surface of the cell in order to more efficiently collect the large number of carriers that are photogenerated where light is first incident on the cell. Surface treatments, such as texturing and the application of an anti-reflection coating, improve light trapping and decrease reflection of impinging radiation. Surface treatments are just one means of engineering to improve device efficiency.

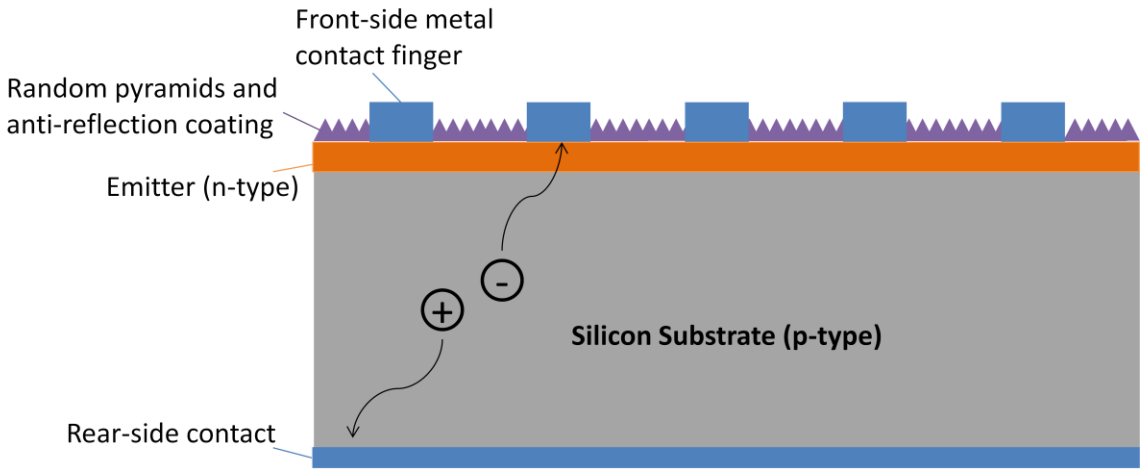


Figure 1-1: Schematic of a standard solar cell adapted from (2).

The cell in Figure 1-1 utilizes a p-type silicon wafer as the base material, and an n-type doped emitter region. Cells can also be manufactured on n-type wafers with p-type doped emitters. The quality of the cell and its performance is dependent upon the doping of the base

layer along with structural and process variables including front contact spacing, minority carrier lifetime, and surface recombination velocities of the front and rear-side contacts and surfaces (2).

Intrinsic performance of a solar cell hinges on material quality. Values inherent to the material such as carrier mobility and carrier lifetime will govern the maximum efficiency that a solar cell can achieve. A perfect single crystal would yield the best performance, but in the interest of cost savings, aspects of cell design are sometimes cleverly engineered and manufactured in order to obtain as much performance as possible out of less expensive, lower quality materials. Innovative engineering will be required to obtain (1) effective charge separation at the emitter (p-n junctions), (2) efficient carrier collection at the contacts, and (3) excellent front and rear surface passivation.

Selective Emitters

In a solar cell, light is absorbed in the bulk material and electron and hole charge carriers are generated. Separation of those photogenerated charges takes place in the space charge region of a p-n junction, built into the solar cell at the interface of the emitter layer and the bulk substrate. Nomenclature surrounding solar cells typically terms the "emitter" as the layer deposited on the substrate to form the junction, but sometimes refers to emitter characteristics in reference to the performance of the p-n junction (6). In the experimental section, use of the term "emitter" will refer to the doped region on the front side of a cell and the p-n junction thus created. A good quality emitter-base junction essentially acts as a diode, allowing current flow in one direction and separating carriers out of the cell for collection. Emitter junctions need to be rectifying, with little series resistance, low saturation current, and minimal leakage current. To form the front side emitter in a solar cell, a homogenous or heterogeneous p-n junction can be created. A homogeneous junction is formed by heavily doping the front surface of a p-type (n-

type) cell to be n-type (p-type). A heterogeneous junction is formed by depositing a p-type (n-type) layer of another semiconducting material onto an n-type (p-type) substrate material (3) (4). In conventional solar cell designs the emitter region is heavily doped over the entire front surface (7) (8). Doping is performed through high temperature furnace diffusion to drive an n-type dopant, such as phosphorus (p-type dopant, i.e., boron), present in a phosphorus containing environment or a phosphosilicate glass, into the p-type (n-type) substrate material (7) (8). The high temperature drive-in step is necessary for doping to occur, but can have undesirable effects on yield due to wafer warping and fracture that can occur (8). Furnace diffusion results in uniform doping across the entire front surface, with no selectivity between the active regions of the material and the regions to be metallized (7). The heavy doping in the active window region decreases the short wavelength response of the cell and leads to a reduction in cell efficiency (7) (9).

Continued efforts to manufacture high-efficiency cells necessitated a switch to selective emitters, which feature heavily doped contact areas underneath the metallized region and a light doping in the window regions (active regions) between front metal fingers (9) (10). Heavy doping under metal contacts ensures ohmic contact formation and reduced contact resistance, and light doping of the active regions of a cell reduces recombination and improves spectral response (11) . Selective emitters are formed through either photolithographic patterning and an “etch back” process, or screen printing and patterning of a dopant paste or metallization paste with the dopant mixed in (10). The heavily doped regions under the metallization have to be carefully patterned for alignment of the metal fingers that are subsequently patterned over the doped region using screen printing, or in high-efficiency cells photolithographic patterning and electron-beam or physical vapor deposition.

Rear-Side Contacts

Photogenerated majority carriers are collected out of the cell at the rear-side contacts. The contacts need to be low resistance and ohmic to ensure that carriers are collected and to avoid degradation of cell efficiency. Higher resistance contacts hinder the travel of holes (for a p-type cell) through the contact and increase resistive loss. Rear-side contacts can be formed over the full area of the rear or in local areas, depending on the cell structure. Screen printing of the rear side contact is commonly performed due to its low cost (12). Using an aluminum paste, full area contacts are printed and then fired to drive out organics and solvents in the paste. Finally the contact is further annealed to ensure contact of the Al metal with the silicon substrate (7) (12). The aluminum layer aids in the reduction of recombination at the rear surface by generation of a back surface field (BSF), which inhibits the movement of minority carriers to the rear-side surface. The presence of Al, a p-type dopant in Si, generates a p-p+ junction at the rear, from which the localized electric field results (7) (13). While screen printing is inexpensive and repeatable it is undesirable to expose the device to the high temperature firing step required to cure the paste and anneal the contacts. The performance of passivation layers degrades with high temperature firing, and as wafers in production become thinner, the contact printing process and extreme heat treatment required for screen printing can cause wafer warping and breakage (8). In high-efficiency solar cells local rear-side Al contacts are made by photolithographic definition. The contacts must be spaced a certain distance apart in a large array; contact spacing depends on the carrier mobility in the substrate and their diffusion lengths. Contact regions are photolithographically defined and etched through the rear passivation layer, making openings for local metal contact to the active region of the device (12). A blanket layer of aluminum is typically used as the contact metal, deposited through e-beam deposition, thermal evaporation, or sputtering.

Surface Passivation

Surface passivation is critical to solar cell performance because it is at the surface where photo-generated carriers can be most readily lost through recombination (9) (14) (15). In the bulk, electrons and holes exist for a characteristic time before they recombine; referred to as the bulk lifetime, the value is much longer than the near-surface lifetime of the carriers. At the termination of the crystalline silicon lattice, bulk properties of silicon no longer apply and the order and predictability of the lattice is abruptly truncated, leaving dangling bonds, surface states, and numerous defects, which have a large impact on cell efficiency and device performance due to carrier recombination. A large fraction of the photogenerated carriers are generated in the near-surface region as light impinges on the cell, but when electron and hole pairs are generated in the bulk of the cell they must travel to the device contacts to be collected (9). Once in the vicinity of the contacts at the cell surface the carriers have an increased chance of recombination. Electrons and holes are attracted to defect induced traps and surface states instead of the contacts if surface passivation is not in place to mitigate the defects.

Passivation and annealing are crucial to reducing carrier recombination and prolonging carrier lifetime. By tying up dangling bonds and reducing the number of defects, device efficiency is increased and carrier collection improved. The passivation layers used must be robust under constant light exposure in outdoor environments, and transparent (on the front side of the cell), to allow light penetration into the cell without absorbing much of the solar spectrum (15). Many materials can be used along with different deposition methods and subsequent heat treatments for passivation. In many solar cells, amorphous silicon (a-Si:H) layers or silicon oxide (SiO_x) layers are used for passivation (14). Amorphous silicon layers can degrade over time, with light exposure and heating, due to the breakdown of the silicon-hydrogen in the film (15). The deterioration happens over the course of tens of years, but once it occurs the passivation qualities

of the film are lost. Amorphous silicon is deposited using plasma enhanced chemical vapor deposition (PECVD). Silicon oxide doubles as an anti-reflection coating (ARC) and a passivation layer. As an ARC it provides enhanced light trapping and light absorption. Silicon dioxide (SiO_2) can be grown through thermal oxidation, or SiO_x can be deposited using PECVD. Dual layers of a-Si:H and SiO_x can be used to maximize the benefits of each material and prolong the longevity of the passivation quality. Silicon nitride (SiN_x) is another common material used to provide surface passivation (14). Similar to SiO_x, SiN_x acts as an ARC, and is deposited through PECVD. Recently amorphous silicon carbide (a-SiC_x) has been found to provide suitable passivation of silicon by researchers at Fraunhofer ISE (14) (16) (17).

Fixed charge passivation relies on charge in the deposited passivation layer to repel carriers from the surface, in addition to passivation through satisfying dangling bonds and surface states. The main mechanism for passivation is that of field effect passivation; by shielding carriers from the surface, they are never near enough to surface defects to have the opportunity to recombine (15) (18). Negative fixed charge in the passivation film is critical for providing passivation of the surface. Alumina (Al_2O_3) has been reported to have large densities of fixed charge (15) (18), and several groups have demonstrated its use in high-efficiency solar cells. Atomic layer deposition (ALD) and plasma assisted ALD or chemical vapor deposition (CVD) are useful in deposition of Al_2O_3 passivation layers (15) (19) (20). Film thickness, passivation layer structure, and annealing treatments are important variables in optimizing passivation for increasing carrier lifetime at the surface. Fixed charge passivation potentially could replace conventional passivation materials if proven robust and capable of reducing carrier recombination.

Solar Cell Design Improvements and Modern Structures

In recent years there has been a push to thinner solar cells not only as a result of materials cost, but also due to the performance limitations associated with thicker base materials. If the base layer is excessively thick the photogenerated carriers have more opportunities to recombine within the material before they can be collected at a contact (2). Subsequent generations of solar cells, building upon the bulk crystalline cell, feature device designs and manufacturing techniques to improve performance and cost savings. Thinning the silicon used in the cell is one method to cut costs, but advancements in cell design typically require more expensive manufacturing processes, which are justified only by device performance improvements or cost savings elsewhere (5). To achieve higher conversion efficiencies and reduce manufacturing costs is a challenging combination but ultimately what manufacturers must do.

Recently, structures including the "heterojunction with intrinsic thin layer" (HIT) cell by Sanyo, and rear surface point-contact cells by SunPower, have been commercially manufactured. Sanyo and SunPower have demonstrated cells in production that achieve efficiencies upwards of 20%, with the HIT cell (23%) and rear point contact cell (22.7%), respectively (16) (21). Two additional cell structures that have the potential to defray manufacturing costs and improve device performance are the passivated emitter and rear cell (PERC) and the front surface field interdigitated back contact, back junction cell (FSF-IBC) (14) (22). Coupled with laser manufacturing, the PERC and FSF-IBC structures could lead to significant advancements in cell performance and efficiency (23) (24).

The PERC family of cells has achieved some of the highest efficiencies reported. As early as 1990 they were demonstrated with an energy conversion efficiency of 23.1% (25). Shown in Figure 1-2, the passivated emitter and rear locally diffused (PERL) cell features passivation at both the front and rear surfaces along with rear-side diffused p+ regions that serve

to reduce recombination losses at the contacts (2). PERL cells and passivated emitter rear totally diffused (PERT) cells have been demonstrated by researchers at the University of New South Wales with efficiencies of more than 24% (25). Both are types of PERC cells, featuring localized rear contacts made through the passivating dielectrics.

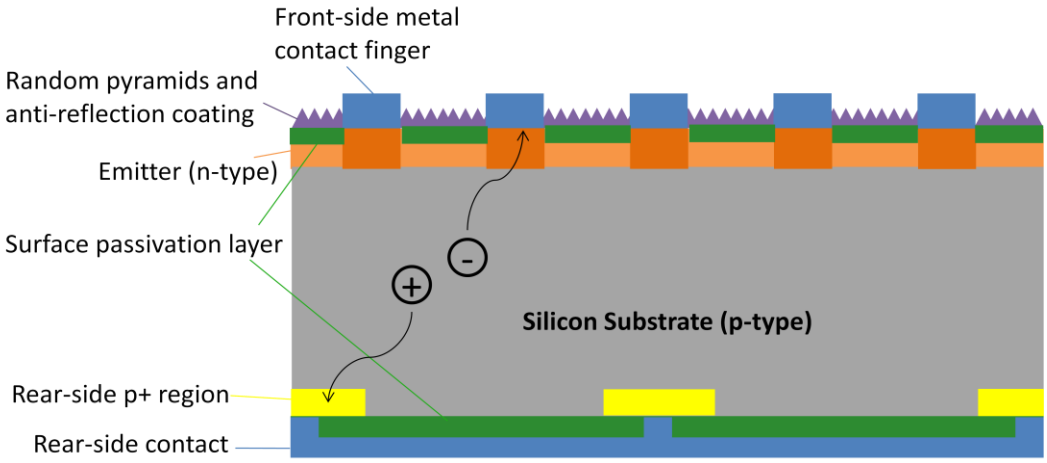


Figure 1-2: Passivated emitter and rear locally diffused cell (PERL) adapted from (2).

Creating a heavily doping the region under the contacts makes collection of majority carriers more efficient by the formation of a p-p+ junction and a local back surface field (13). In a PERC cell, the local rear-side contacts can be formed through laser firing, creating highly doped regions like those in a PERL cell, resulting in a BSF due to incorporation of Al into the laser fired contact. Laser firing of PERC cells reduces manufacturing steps and makes them more manufacturable while maintaining high efficiency. The Fraunhofer Institute for Solar Energy Systems has demonstrated PERC cells achieving efficiencies from 20.2 to 22.4% (16) (24) (26).

To reduce costs lower quality multi-crystalline silicon is often substituted for single crystalline silicon. The mc-Si has shorter minority carrier diffusion lengths and shorter carrier lifetimes, which limit the distance that the photogenerated carriers can travel to reach a contact. The lower quality material dictates the use of a front-side emitter and contact grid to ensure carriers can be collected at the front surface, in the vicinity where they are generated (5).

Unfortunately, the use of front side metal fingers causes shading loss of the active silicon, reducing the area available for photon absorption, leading to a reduction in cell efficiency. An innovative cell design to completely prevent shading loss is the front surface field, interdigitated back contact, back junction cell (FSF-IBC) shown in Figure 1-3. Interdigitating both contacts for collection of electrons and holes (shown as the n+ BSF and the p+emitter) on the rear-side of the cell leaves no metallization in the front side to shadow the active region of the cell (5).

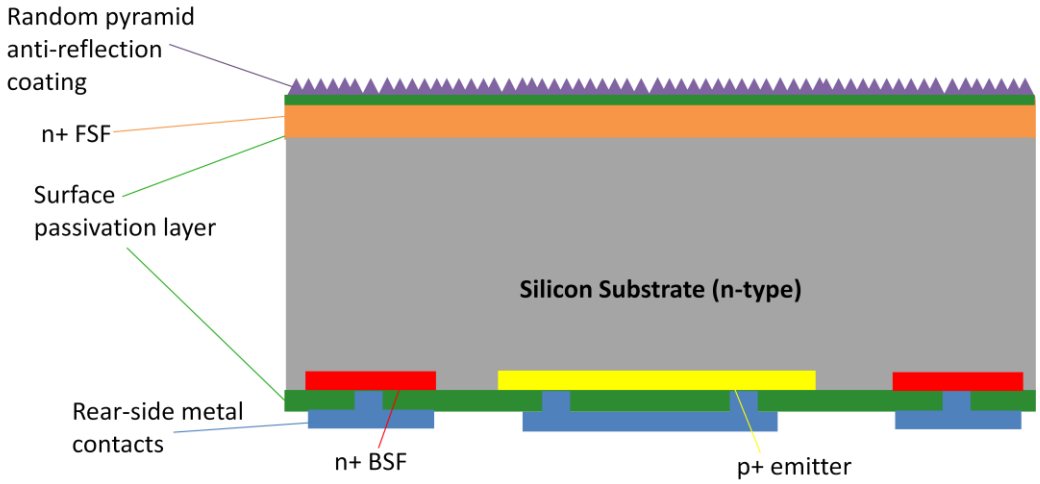


Figure 1-3: Front surface field, interdigitated back contact, back junction cell (FSF-IBC) adapted from (2).

An n-type substrate is used due to the higher carrier mobilities it features. Higher quality substrates must be used in IBC cells because carriers generated at the front surface must travel from the front surface to the collecting contacts and emitters at the rear-side of the cell (9); therefore, it is critical that minority carrier lifetime and bulk diffusion lengths are very long.

As cells become thinner, the quality of the substrate plays an increased role in performance. Since the active region is thinner, the use of a high quality substrate is critical to maintaining device performance (9). Additionally, with the removal of the bulk thickness, carrier collection at the rear of the cell becomes more prevalent, making the FSF-IBC design more attractive (5).

With increased carrier collection at the rear side, cell performance can be severely limited if recombination at the rear surface and contacts occurs. Passivation at the front and rear surfaces become increasingly important in thinner cells, as well as FSF-IBC cells. In a FSF-IBC cell, excellent surface passivation is important in order to prevent carrier recombination at the front side surface since there are no contacts present to collect them (9). Passivation of the rear surface is important as well since the presence of both contacts means a large concentration of electrons and holes will be in the same area. Recombination at the contacts and front surface must be combatted using field effects (high doping density to create BSFs) and chemical passivation layers (5).

Solar Cell Structure and Laser Firing

The introduction of laser processing to photovoltaic manufacturing has the potential to be very advantageous for solar cell manufacturability. Laser firing makes possible the formation of front and rear-side contacts in a few steps, rather than the numerous photolithography, development, etching, and metallization steps or the high temperature screen printing steps previously required (24). The formation of front and rear-side contacts through laser firing is one potential method of reducing manufacturing cost while maintaining device performance and improving processing throughput; however, careful control of laser processing conditions must be implemented to ensure that device performance is maintained. It is imperative to understand how lasers processing can be used beneficially for improvement of device performance and implementation in manufacturing.

Laser fired contacts (LFCs) rely on a laser to selectively heat and melt regions of the rear Al contact layer through the rear-side passivation layers to create a localized rear-side contact into the underlying silicon substrate. In a PERC type cell this process creates contacts along with a

localized back surface field (BSFs) created by the incorporation of Al into the molten silicon and subsequent solidification. The BSF positively impacts the recombination dynamics at the rear-side contact given that the LFC does not introduce excessive damage to the region around it (16). The primary concern with replacing rear-side solar cell contacts with LFCs is that structural damage can occur due to the large amount of energy imparted by the laser to a very small volume over an exceedingly short time. Excessive laser energy can result in damage to the surrounding substrate and passivation layers, making careful selection of laser processing parameters critical. Conditions for forming LFCs must be only energetic enough to melt and mix the aluminum and silicon in the locally fired contact region; ablation, drilling, or a large heat affected zone are undesirable (27). With careful selection and control of the laser processing parameters, LFCs can be implemented into solar cells structures and can improve cell performance and manufacturing throughput.

The doping of locally diffused front side emitters is also possible with the proper implementation of laser firing. So-called laser doped emitters (LDEs) can be fabricated by selectively firing the laser in regions to be metallized. By firing through a dopant layer, a high concentration of the dopant is incorporated into the molten silicon substrate at points selectively melted with a laser (10). Using a laser to dope the emitter has the potential to degrade device performance if the laser processing parameters are excessively energetic. Excessive laser energy can induce defects into the crystalline structure that can act as recombination centers and reduce the number of carriers available for collection (28). In particular, series resistance, saturation current, and leakage current may be affected, and if any one of these parameters is increased, it detracts from the emitter's performance. The diode ideality factor also suffers with increased recombination; therefore, it is critical to perform laser doping with mild processing conditions that do not damage the silicon, but are energetic enough only for adequate doping of the contact, through the passivation layers.

The passivated emitter and rear cell (PERC) and front surface field interdigitated-back contact (FSF-IBC) cell are particularly well suited for the implementation of laser firing in solar manufacturing. In PERC cells, laser firing has been used to fire rear-side ohmic contacts though passivation layers, incorporating Al into the melted laser fired region of the silicon, forming cells with efficiencies greater than 20% (16) (24) (26). With improved understanding of laser-material interactions and LFE and LDE performance, a fully laser processed cell could be commercially manufactured in the near future.

Motivation

For solar energy to achieve grid parity, methods to increasing cell efficiency and manufacturability, while minimizing cost, need to be developed. Combining innovative cell structures, like the PERC and FSF-IBC, with advanced processing methods, like laser processing, is one strategy that holds promise in improving solar cell's manufacturability. Laser processing of rear-side contacts and front-side doped emitters, along with the introduction of new passivation techniques, can greatly improve performance of both PERC and FSF-IBC cells, providing efficiency enhancement and eliminating the traditional processing steps for patterning or screen printing emitters and contacts. Using the appropriate processing conditions, laser firing the rear-side contacts and laser doping the front-side emitters of crystalline silicon PERC solar cells could be adapted to a low-cost, high-volume manufacturing scenario.

Experiments and Goals

In order to evaluate the feasibility of laser firing a solar cell and to assess the quality of the resulting contacts and emitters, several experiments have been performed. LFCs were

fabricated and characterized through cross-sectioning, junction delineation, and simulations of resistance measurements. Two lasers, a ytterbium-doped 1070 nm single mode fiber laser and a Nd:YVO_4 355 nm frequency tripled Q-switched laser, were utilized to evaluate laser processing parameters. Evaluation of contact geometry within the silicon was carried out using a newly developed technique of cross-sectioning and junction delineation of laser doped features. Device simulations were also performed to estimate the dopant density of the LFCs and to fit experimental current-voltage (I-V) data.

Laser doped emitters were fabricated and evaluated through I-V measurements, cross-sectioning, and junction delineation. Line emitters are generally studied in the literature, but herein we study individual spot emitters. Fabrication of the LDEs was performed with three different lasers; a ytterbium-doped 1070 nm single mode fiber laser, a Nd:YVO_4 355 nm frequency tripled solid state Q-switched laser, and a Nd:YAG 1064 nm Q-Switched laser. Diode characteristics were evaluated for each LDE by comparing diode ideality factors, saturation currents, and leakage currents. Cross-sectioning and junction delineation were performed to determine emitter depth and width within the substrate.

In passivation layer experiments, alumina (Al_2O_3) and hafnia (HfO_2) films prepared by atomic layer deposited (ALD) were investigated as a means of providing fixed charge passivation. Films of varying thickness, and multi-layer structures incorporating plasma-enhanced chemical vapor deposited (PECVD) silicon oxide (SiO_x), were studied with different annealing treatments. Each passivation structure given a different annealing treatment was evaluated through measurement of effective carrier lifetime, calculated fixed charge densities, and sheet resistance changes in special high resistivity wafers, indicating the presence of an inversion layer. Microwave photoconductive decay was used to measure effective carrier lifetime, capacitance-voltage (C-V) measurements were used to calculate fixed charge densities, and a contactless conductivity probe was used to measure sheet resistance.

In evaluating these devices and passivation layers, the goal was to identify a means to fabricate a fully laser processed, high efficiency cell. Each structure is critical to the device performance and by optimizing each—the contacts, emitters, and passivation—a high efficiency cell may be manufactured affordably through laser processing.

Chapter 2

Laser Fired Contacts

Literature Review

Laser processing has made possible the formation of rear-side ohmic contacts without the use of multi-step photolithography patterning processes previously used in high efficiency solar cells. Instead of opening the rear side dielectric passivation through patterning and etching, and then metalizing the rear contacts, a laser can be used to fire through both the metal and dielectric passivation layers to incorporate the metal into the silicon substrate. Laser fired contacts (LFCs) are also suitable for replacing rear-side contact patterning by screen printing, which requires deposition of a metal paste and a high temperature firing step to create the contact. The elimination of extra processing steps and high temperature steps, along with the potential for compatibility in high efficiency device production has made research in laser processing widely popular. The ability to create laser fired contacts (LFCs) and apply them to solar cell devices has been demonstrated by many research groups (24) (26) (29) (30) (31). The best efficiencies reported have been greater than 18%, with the highest reported being 21.3% and recently 22.4% (14) (16) (24). Devices performance is evaluated by examining solar cell characteristics, including open circuit voltage, V_{oc}, short circuit current, J_{sc}, fill factor, FF, and conversion efficiency, η. However, deeper understanding of the contacts themselves requires further characterization, and groups have used several techniques to do so. The work of Zastrow et al. (23) involved secondary ion mass spectroscopy (SIMS) and transmission electron microscopy (TEM) characterization. LFCs were fired with a pulsed Nd:YAG laser and had diameters between 80 and 100 μm. The group found concentrations of Al on the order of ~$10^{19}cm^{-3}$ at the center of

the LFC, which was incorporated within the contact to a depth of 1µm (23). Grohe et al. (22) performed laser secondary neutral mass spectroscopy (L-SNMS) as well as electron beam induced current (EBIC) measurements on LFCs fired with a Q-switched Nd:YAG laser. The EBIC and L-SNMS measurements indicated that Al was incorporated with Si in the center region of each contact (22). Additional EBIC measurements on the cross-section of a cleaved LFC confirmed incorporation of the Al within the contact to a depth of ~1µm (22). Kray and Glunz investigated the morphology of LFCs and reported the effects of contact pitch on surface recombination velocity (SRV) analytically and experimentally (32). Surface recombination velocity was determined based on bulk carrier lifetime and near surface carrier lifetime. Light beam induced current (LBIC) measurements, scanning electron microscopy (SEM) images, and EBIC measurements were taken on LFCs to determine the presence of Al in the inner region and measure contact diameter. When performing SEM/EBIC scans on a cross-sectioned LFC fired on n-type silicon, they found Al present within the volume of their contacts as well (32). They report a SRV of 35 cm/s with a contact pitch of 1000µm (32). All these techniques are useful for tracing the presence of Al incorporated into the contacts and prove the ability to create LFCs; however, little has been disseminated with regards to the appropriate laser processing conditions to use.

A majority of the LFCs examined in previous work were fired with 1064 nm lasers with nanosecond pulse durations; in research carried out by past students on this project, an investigation to identify processing conditions for 1070 nm and 355 nm lasers was performed (27). Through evaluation of contact resistance, SEM observations, and post-processing effective carrier lifetime measurements, processing conditions of LFCs fabricated with a gated pulse ytterbium-doped 1070 nm single mode fiber laser and with a Nd:YVO_4 355 nm frequency tripled Q-switched solid-state laser were evaluated for use in manufacturing. Samples investigated were passivated with either 10 nm of amorphous silicon (a-Si:H) and 100 nm of silicon oxide (SiO_x)

deposited by plasma-enhanced chemical vapor deposition (PECVD), or 80 nm of a-Si:H deposited by PECVD and metallized with a 0.5 μm Al layer deposited on both sides using electron-beam (e-beam) deposition (27). All wafers used for resistance experiments and surface morphology studies were ~275 μm thick (100) p-type float zone (FZ) silicon wafers with a resistivity between 1-5 Ω-cm. LFCs fabricated with each laser were evaluated using SEM imaging to assess visible changes to the contact morphology as a function of laser processing parameters. For the 1070 nm laser, using high power (> 45 W) and long pulse durations (> 14 ms) resulted in large diameter contacts (> 50 μm), and at the largest powers and pulse durations (50 W, 19 ms) degradation of the surrounding area occurred due to a large heat affected zone (27). When low power and short pulse durations were used (< 30 W, and 14 ms), the contacts were much smaller in diameter (< 20 μm) and damage to the surrounding substrate was minimal (27). For the 355 nm laser, using high energies (> 50 μJ) and multiple pulses per shot (> 1 pulse) created large contacts and ablated a significant amount of material to the point of laser drilling. Those contacts fired at lower energies (< 50 μJ) and single pulses did not penetrate the substrate deeply but still exhibited ablation (27). Following SEM investigation resistance measurements were taken on LFCs fired with each laser to understand the effect of laser processing conditions on the electrical performance. Resistances measured on LFCs fired with the IPG 1070 nm single mode fiber laser correlated inversely with size. The resistance decreased with increased LFC diameter, implying that processing with larger powers and longer pulse duration led to larger contacts with smaller resistances. For the AVIA 355 nm laser, no trends or correlations between resistance and processing conditions were apparent. It was concluded that further investigation of less energetic pulses would be needed to further evaluate the usefulness of the AVIA 355 nm solid state Q-switched laser in LFC manufacturing. Carrier lifetime mapping provided insight into the consequences of laser firing on the effective carrier lifetime. It was demonstrated that appropriate laser firing conditions (30 W and 6.5 ms, 30 W and 21.5 ms, and

50 W and 4 ms) could be selected to avoid significant degradation of the effective carrier lifetime (27). The lifetime in regions surrounding LFCs processed with the IPG 1070 nm did not degrade after laser processing, but lifetime in regions surrounding LFCs fired with the AVIA 355nm laser did. A 10 min 275°C anneal was required post processing to re-measure lifetime.

Having gained an understanding of laser processing conditions useful for LFC creation in this previous work, additional experimentation was needed to understand the laser-material interaction. The work herein sought to study the effects of laser processing conditions on Al incorporation and concentration in the contact, and the resulting geometry of the contact within the silicon substrate.

LFC Simulation and Cross-sectioning Goals

Based on the experiments performed by DeCesar (27), additional experiments were performed along with simulations, to understand LFC geometry and doping. Cross-sectioning and junction delineation were performed to investigate contact depth within the silicon. A technique was developed to delineate the geometry of the melt region. Simulations using Sentaurus (33) device simulator were carried out to estimate the doping density of the laser fired contacts and fit the experimental trend of reduced contact resistance with increased LFC diameter. LFCs were modeled and resistance measurements were simulated in an attempt to match experimental resistance measurements taken by DeCesar.

Cross-sectioning and Junction Delineation

Sample Fabrication

In order to create a p-n junction upon laser firing a p-type Al contact, samples for cross-sectioning and junction delineation were fabricated on ~500 μm thick (100) n-type Czochralski-grown (CZ) silicon wafers with a resistivity of 0.5-1 Ω-cm. The n-type samples were passivated with either 80 nm of PECVD grown a-Si:H or 10 nm of PECVD grown a-Si:H and 100 nm of PECVD grown SiO_x, and metallized with 0.5 μm of Al deposited on both sides by e-beam deposition.

The same ytterbium-doped 1070 nm continuous wave, gated pulse, single mode fiber laser used in previous work was used in fabrication of samples that were cross-sectioned. The 355 nm laser was not investigated due to the poor results previously seen in LFC resistance measurements. Dense arrays of LFCs were fired to increase the likelihood of cross-sectioning multiple contacts on a single sample. Center to center spacing of the LFCs in the array was equal to approximately twice their measured diameter.

Processing Procedures

Following laser processing, samples were sectioned using a diamond saw for precise control of sample size and orientation. A piece of the sectioned array was super-glued on its face to another silicon piece to protect the edges to be polished from rounding off. The glued sample was mounted onto a polishing stub. The procedure is detailed in Figure 2-1.

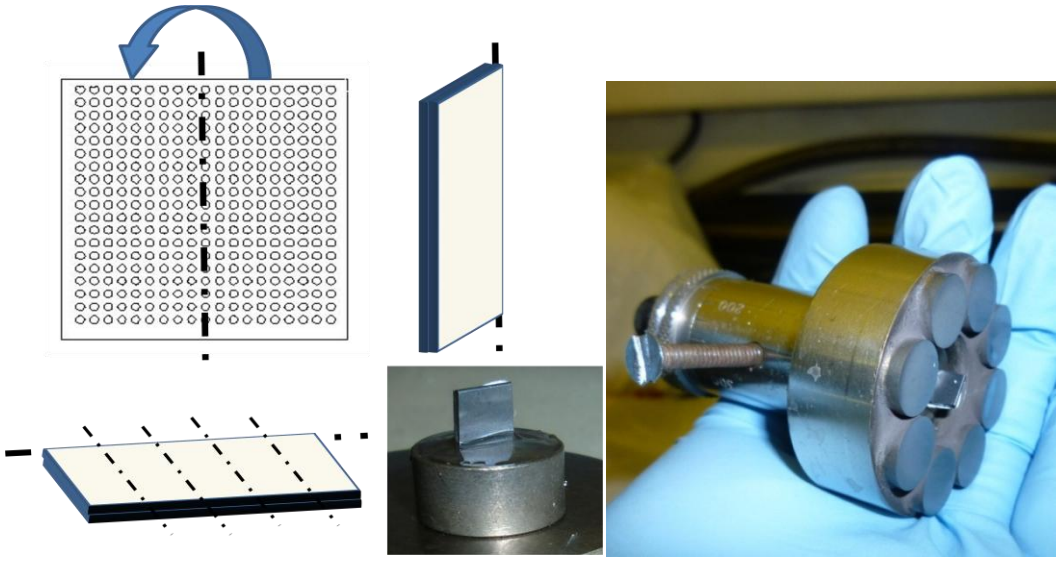


Figure 2-1: Dense array and sample preparation for polishing.

By polishing the sample with increasingly finer grits of silicon carbide polishing disks, the sample was gradually ground down and scratches in the surface were polished out. The disks were mounted on a rotating polishing wheel, seen in Figure 2-2, and a steady stream of water was run across them while they spun. Polishing the samples with the LFC array at a slight angle, indicated in Figure 2-2 by θ, increased the likelihood of cross-sectioning more than one LFC.

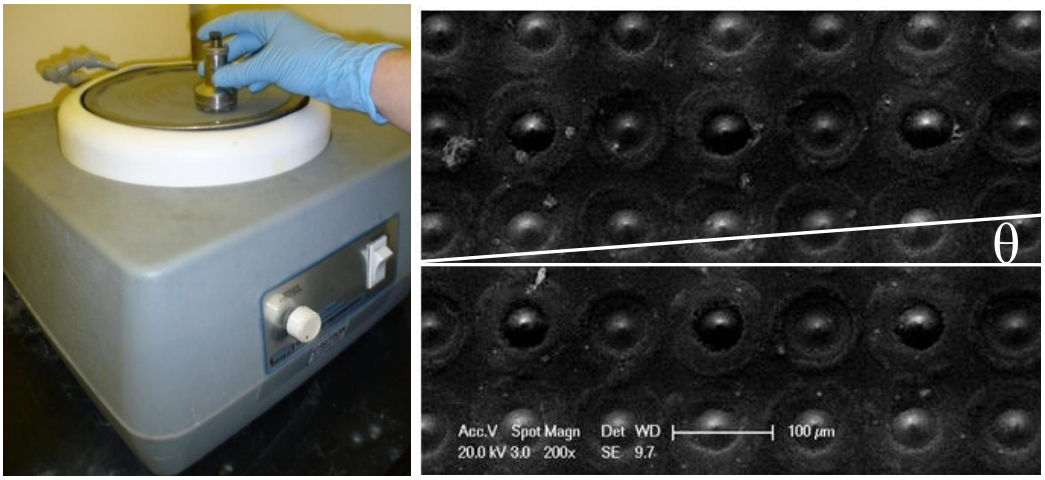


Figure 2-2: Polishing wheel and angle at which the sample is polished.

Throughout the grinding process, the surface was examined under a light microscope to assess the location of the cross-section within the LFC array. The approximate middle of an LFC, where the laser should have melted the silicon to a maximum depth, was reached when the characteristic peaks, at the center of an LFC on the surface, were apparent in cross-section. Once a successful cross-section was made, a final polishing pad was used, and afterwards the sample was rinsed in a de-ionized (DI) water bath and dried with N_2 gas.

Techni Gold 25, an electroless plating solution made by Technic, Inc., was used to delineate the p-n junction of the LFCs in a manner similar to that reported for delineating p-n junctions in silicon nanowires (34). Aluminum is a p-type dopant that has solubility on the order of 10^{19} cm^{-3} in silicon (35) (36). On an n-type wafer the incorporation of Al forms a p-n junction at each laser fired contact, making selective plating possible. Eichfeld et al. successfully demonstrate the selectivity of Technic Gold 25 on very small geometries, delineating n-type sections of 1.4 µm to 0.12 µm lengths on alternating n- and p-type segments of silicon nanowires only 150 nm in diameter (34). Under illumination, gold in the solution selectively plates on the n-type region of the silicon. The n-type region acts as a cathode, due to electrons generated, and the p-type region functions as an anode, remaining free of nucleated gold, due to holes generated.

Cross-sectioned samples were immersed in the plating solution and illuminated with a 50 W halogen lamp for 6 to 8 min at room temperature. Once removed from the solution, the samples were rinsed with DI water and dried with nitrogen gas. Imaging the samples in the field emission scanning electron microscope (FESEM) clearly showed the p-type regions created from laser firing, and provided evidence of the presence and incorporation of Al within the laser fired region, seen in Figure 2-3.

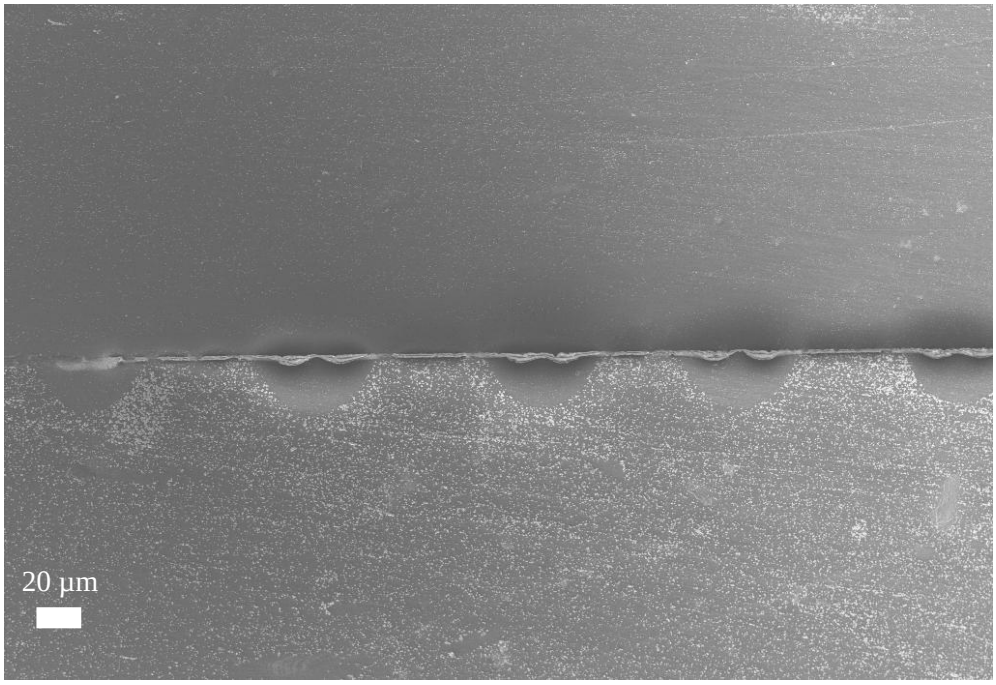


Figure 2-3: Successful cross-section of a row of LFCs and junction delineation between the p-type melt regions and the n-type substrate, sample passivated with a-Si:H/SiO_x.

Results and Discussion

Four different samples were cross-sectioned and plated after being processed with the IPG 1070 nm laser. Shown in Table 2-1, two sets of processing conditions were fired onto each type of passivated substrate. The processing conditions, 45 W and 4 ms along with 22 W and 19 ms, were selected to compare the dimensions of the resulting LFCs on each passivation structure. At the higher 45 W power there was not a significant difference in the dimensions of LFCs fired on either substrate, indicating that the structure of the passivation layers did not impact LFC formation. At the lower 22 W power, the LFC fired on the a-Si:H passivation structure is slightly larger than the LFC fired on the a-Si:H/SiO_x layer. The difference is slight, but indicates that the presence of the SiO_x layer may impact LFC formation at lower powers.

Table 2-1: Dimensions of cross-sectioned profiles within the substrate.

Sample	Passivation	Power	Duration	LFC Width	LFC Depth
n-type	a-Si:H	5 W	4 ms	57 µm	25 µm
n-type	a-Si:H/SiO_2	45 W	4 ms	60 µm	28 µm
n-type	a-Si:H	22 W	19 ms	45 µm	21 µm
n-type	a-Si:H/SiO_2	22 W	19 ms	42 µm	16 µm

Samples with the 45 W pulse had much larger melt regions than those fired with 22 W, which would be expected. Both sets of processing conditions adequately incorporated aluminum in silicon as evidenced by successful plating of samples. If Al had not been incorporated, there would not have been a noticeable contrast in the plating between n- and p-type regions. It is surmised that the geometry of the p-type region represents the once-molten solidified region, and originates from the melting and mixing of aluminum and silicon during the laser pulse. Solid state diffusion would be negligible given the length of the pulse durations. Aluminum was incorporated within the silicon to depths from 16 to 28 µm, which was much deeper than previously reported (22) (23). Any effect a depletion region may have had on the dimensions has been neglected. Based on the assumed doping concentrations of $1x10^{16}/cm^3$ for phosphorus in the n-type substrate (from ρ = 0.5-1 Ω-cm) and $2x10^{19}/cm^3$ for Al in the p-type once-molten region (taken from (35)), the depletion width would be less than 0.4 µm wide.

The characteristic morphology of LFCs fired with the 1070 nm single mode fiber laser exhibited a peak in the center of a recessed area. LFCs fired at 4 ms and 45 W are seen in Figure 2-4. The figure shows the diameter of the molten region, the diameter of the heat affected zone, and the center peak of the once-molten region. The diameter of the LFC, measured as the visible width of the molten region, is approximately 45 µm.

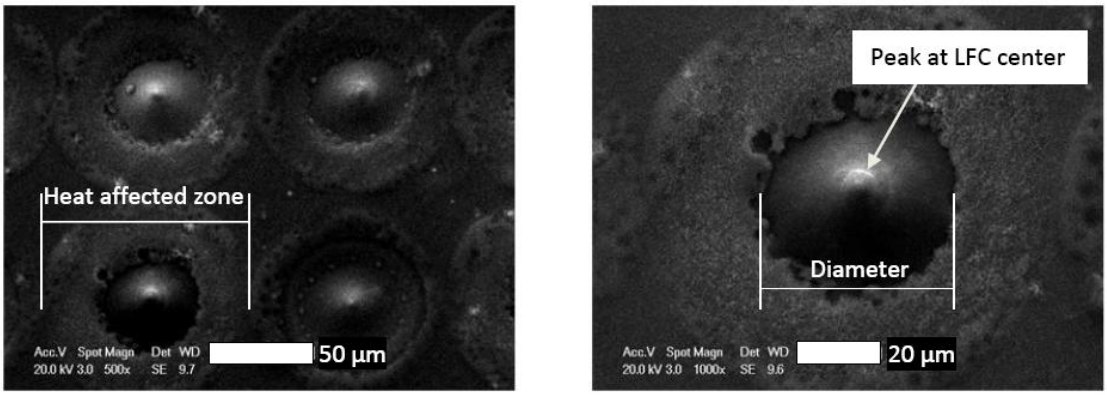


Figure 2-4: Sample fired at 45 W and 4 ms showing typical morphology of LFCs fired with the IPG 1070 nm single mode fiber laser.

As seen in cross-sectioning, the width of the once molten region is somewhat wider than what is visible at the surface. Figure 2-5 shows the extent of the p-type region for different laser parameters on each type of sample. Both were fired using the IPG 1070 nm single mode fiber laser. The LFC in image (a) was fired at 22 W and 19 ms on an n-type wafer passivated with a-Si:H. The LFC in image (b) fired at 45 W and 4 ms on an n-type wafer passivated with the a-Si:H/SiO_x dual stack. In image (b), the characteristic peak seen in the top view of the LFCs in Figure 2-4 is evident in the cross-section.

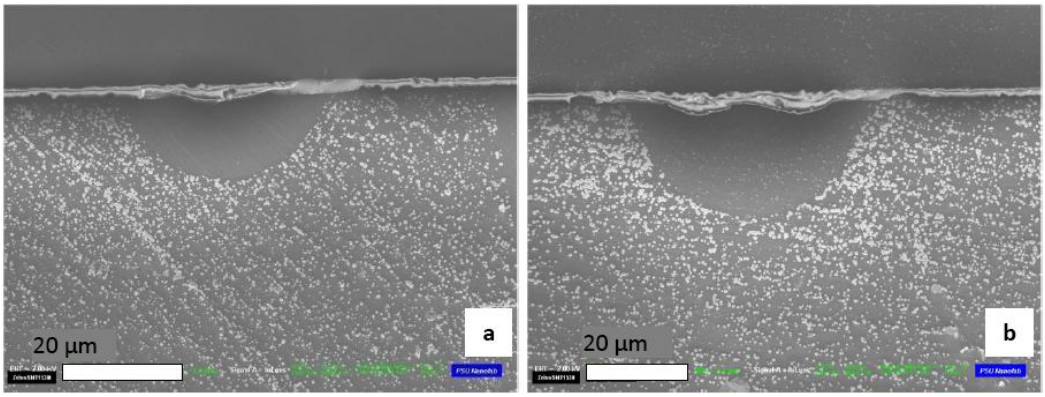


Figure 2-5: Cross-sections after junction delineation of an LFC (a) fired at 22 W and 19 ms, passivated with a-Si:H, and an LFC in image (b) fired at 45 W and 4 ms, passivated with a-Si:H/SiO_x.

LFC Simulation

Device Modeling and Simulation

To further understand the effects of laser processing parameters on the contact resistance and to determine if experimental measurements could be predicted, LFC simulations were performed using SENTAURUS TCAD by Synopsys, Inc. (33) with the assistance of Brian Downey.

Based on the results of cross-sectioning, the LFC device was modeled as a doped hemispherical region embedded at the surface of a silicon substrate. The model was created based on sample geometry, with a wafer thickness of 275μm and length and width of 700 μm on a side. Taking advantage of symmetry, current transport in only one quarter of the contact was simulated, and the total resistance of each LFC was found by dividing the simulated resistance by 4.

In order to simulate the boron doped substrate used in experiments, which was measured to have a resistivity of approximately 2 Ω-cm, the modeled substrate was doped p-type with a boron acceptor concentration of $7x10^{15}$ cm^{-3}. Simulations were performed using different doping densities for the contact region to best match the actual doping density of the contact by comparing simulations to experimental measurements. Many papers report aluminum concentrations in silicon similar to the solid solubility limit of $2x10^{19}/cm^3$, as given by Trumbore in 1960 for a film grown at 800°C (35) (36). However, solubilities from $3x10^{19}$ up to $10^{20}/cm^3$ have been suggested for films deposited and annealed at temperatures from 400-500°C (37) (38) (39). Doping densities up to $1x10^{20}/cm^3$ were modeled to compare with the experimental data.

The device was simulated by applying a dc bias to the top surface area of the LFC region from 0 to 2 V with the entire back side of the substrate at ground. The metal/semiconductor

contact resistance was neglected in the simulation due to the assumption that Al metal contacts a highly doped p+ region leading to a low specific contact resistance. Those reported in the literature justify this assumption. Hara et al. reported a contact resistivity of $4x10^{-6}\Omega$-cm^2 for an Al sintered contact at 450°C on p+ silicon with a surface dopant concentration of $1x10^{19}$ cm^{-3} (40). Furthermore, Schwartz reported a contact resistivity of $3.6x10^{-6}$ Ω-cm^2 for laser annealed Al contacts to poly-Si (41). A contact resistivity of $4x10^{-6}$ Ω-cm^2 corresponds to a contact resistance of 0.2 Ω for a 25μm radius contact. Such a resistance is much less than the total resistance measured (~100 Ω) and can be neglected. The generated I-V plot produced from the simulation was used to determine the total resistance of each different diameter contact.

Simulation Results

Simulation of contacts with radii from 10 μm to 40 μm were performed with fixed LFC doping densities of $1x10^{16}$, $1x10^{18}$, $2x10^{19}$ and $1x10^{20}/cm^3$. The results are shown in Figure 2-6, where simulated resistance values as a function of radius and doping are plotted and compared to experimental data.

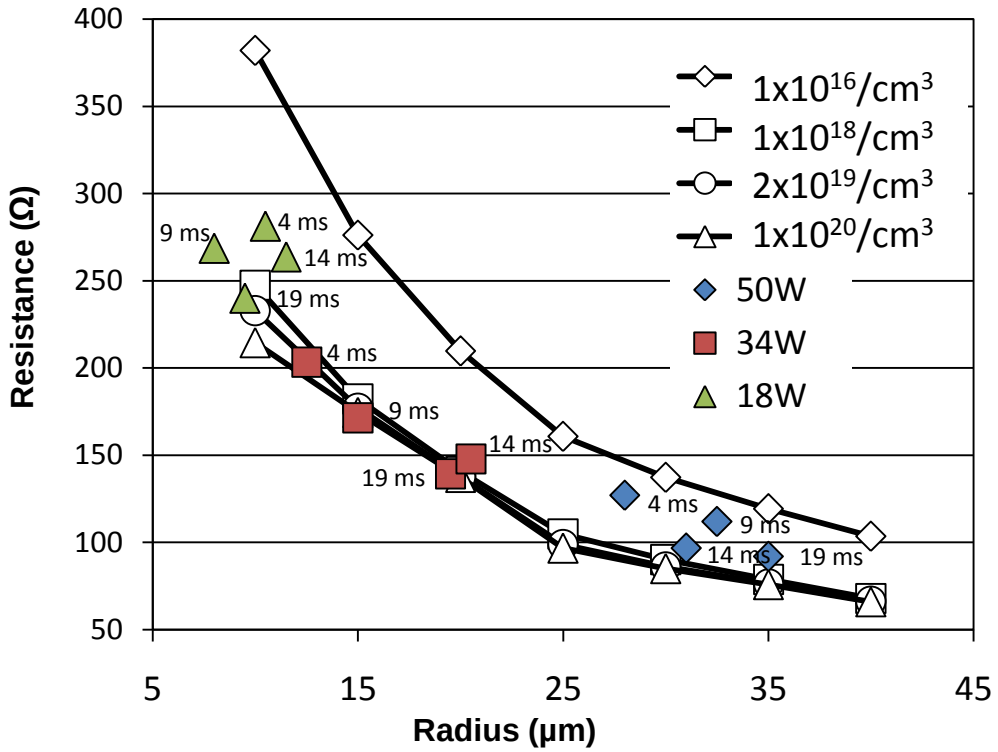


Figure 2-6: Simulated resistance values and experimental resistance values for LFCs.

The simulated total resistance values match well with the experimental data when assuming a doping density of $1x10^{18}$ to $1x10^{20}/cm^3$ for the LFC region. The experimental resistances for LFCs fired at 34 W match particularly well with the simulated resistances. For a LFC fired at 34 W and 19 ms with a diameter of 19.5 μm the measured resistance was 139 Ω. The simulated resistances of a 20 μm radius LFC with doping from $1x10^{18}$ to $1x10^{20}$ cm^{-3} were 141 to 137 Ω, matching within $\pm$2 Ω. For a LFC fired at 50 W and 19 ms with a radius of 35 μm the measured resistance was 92 Ω. The simulated resistances of a 35 μm radius LFC with doping of $1x10^{18}$ to $1x10^{20}/cm^3$ were 79 to 76 Ω, a 14% to 17% difference from the measured value. The measured resistance is likely higher than the simulated resistance because of the damage inherent in LFCs fired at larger powers. For a LFC fired at 18 W and 19 ms with a radius of 9.5 μm the measured resistance was 240 Ω. The simulated resistances of a 10 μm radius LFC with doping from $1x10^{18}$ to $1x10^{20}/cm^3$ were 248 to 215 Ω, a 3% to 10% difference from the measured value.

For contacts with smaller radii, the doping density of the LFC region has a greater impact on the overall resistance, while contacts with larger radii are less affected by a change in simulated doping density. For the larger radii LFCs simulated with high doping densities, the resistance values begin to coincide despite changes in doping density, because the spreading resistance from the hemispherical p+ region into the substrate dominates the overall resistance.

Simulations have shown that the trend seen in experimental resistance measurements, of increased resistance for smaller diameter contacts. Resistances simulated for LFCs modeled with doping densities greater than $1x10^{18}/cm^{-3}$ matched well, and spreading resistance was found to dominate resistance measurements of larger radii contacts.

Chapter 3

Laser Doped Emitters

Literature Review

The advent of laser processing in solar cell manufacturing has led to a wide range of innovative laser-doping techniques for the fabrication of front side emitters (6) (10) (42) (43) (44). In particular, the ability of a laser to locally heat specific regions makes it an ideal tool for doping selective emitters (6) (42) (43) (44). These emitters are located underneath the front side metallization and must have a high doping density to ensure ohmic contact characteristics (6) (11) (44). Lasers are used primarily in two ways: to create either laser-assisted selective emitters or laser doped emitters (LDEs). In the former process, a laser is used to ablate dielectric layers in order to create openings for subsequent doping of the exposed silicon. Doping is performed through conventional furnace diffusion in a subsequent process step (10). In the formation of LDEs, a laser is used to dope select regions (6) (10) (44) (45). Wet or dry processing can be used, the difference being the method of dopant source incorporation into the process (10). In wet processing the dopant material is introduced onto the surface through a liquid stream or in a bath (10) (11). In dry processing the dopant material can be introduced onto the surface through either a gas atmosphere or a dopant containing layer (10). Dopant source layers under investigation in much of the literature include: pure dopant layers (6) (45), spun on dopant layers (42) (44), or even doped amorphous silicon carbide films (16). After introduction of the dopant source to the surface a laser is used to induce doping and dopant activation by melting the substrate, allowing for liquid diffusion of the dopant (6) (10) (11) (42) (44) (45).

Once the selective emitter is laser doped, metal fingers must be patterned over the laser doped regions. Previously metallization was performed either by photolithographic patterning

and subsequent metal deposition (in high efficiency cells), or by careful alignment of a screen printed metal pattern and a high temperature firing step (typical in commercial cells) (12). Photolithographic metal patterning is very expensive but provides well defined, high purity metal contacts. Screen printing is cheap and repeatable but exhibits poor line definition and high resistance lines. The high doping achieved with selective laser doped emitters makes them suitable for electroplating when patterned first with a seed layer (46) (47). Electroplating itself is inexpensive, easily scalable to manufacturing, and provides high purity metallization, but the need for a seed layer when metalizing front side emitter fingers requires an additional deposition step that is undesirable. Selective electroplating techniques are being developed that do not require the use of a seed layer (48), and electroless plating by illumination may also be possible, but neither have been implemented in production. In current research, investigation of metallization processes commonly goes hand in hand with investigation of emitter doping techniques.

In work by Kray and McIntosh the formation and performance of selective emitters prepared by laser chemical processing (LCP) was studied (11). A chemical stream directed by a nozzle was used to introduce the liquid dopant material to the cell surface only on regions that were to be laser doped. Deposition of the liquid dopant was followed directly by a scanning laser that melted the selected regions, inducing liquid state diffusion of the dopant into the underlying silicon through the front passivation layers (10) (11). The front side emitters were defined by laser doping and selective heating/melting rather than by photolithographic definition and high temperature diffusion doping in a furnace (11). Kray and McIntosh investigated the I-V characteristics of the LCP grooves and determined the recombination current density (saturation current density) associated with them was at most 8.5×10^{-13} A/cm^2 (11). In manufacturing test cells, they achieved efficiencies from 14.6 to 20.4% across planar and textured substrates, demonstrating the compatibility of LCP with manufacturing high-efficiency solar cells (11).

An additional investigation of LCP and metallization by aerosol jet printing (AJP) was reported by Drew et al. (47). They successfully implemented LCP to create selective emitters, and used AJP to write a silver seed layer over the laser doped regions. The Ag seed layer was then thickened by light induced plating to create a silver metal contact finger 45 to 55 µm wide and 9 µm thick (47). They used laser fluences in the range of 0.5 to 1.5 J/cm^2 to create the emitters but noted a decrease in cell performance when processing with fluences in the range of 1.1 to 1.4 J/cm^2. They attributed performance loss to laser induced damage resulting from higher fluences (47). In studying morphology of the LCP area, they observed that a rough surface was formed rather than a deep groove. Lower fluences made possible the formation of a molten region of silicon in which the dopant material could diffuse and solidify, without material loss through ablation. Higher fluences were attributed to silicon evaporation and removal material from the substrate, forming grooves and material damage rather than doping (47).

A concept recently demonstrated at Fraunhoffer ISE, by Suwito et al., used a doped a-$Si_{1-x}C_x$ layer to act as both a passivation layer and dopant source (16). Their so-called "passdop" layer demonstrated the capability of a dopant source layer to additionally provide surface passivation. Upon laser firing through the layer, melting and liquid dopant diffusion occurred (16). Since the layer doubles as a passivation layer, the removal of an extraneous dopant source layer was not needed. While they used the layer to create rear-side contacts, a similar process commonly referred to as laser induced melting of a pre-deposited impurity doping (LIMPID) (10) (49) is used for doping front-side emitters by firing through a dopant source film.

Esturo-Breton et al. fabricated cells with efficiencies of 14.2% by doping selective emitters through a spin on dopant (SOD) layer. A phosphorus containing SOD was deposited and cured producing a 400 nm thick dopant source layer. Selective LDEs were processed using a 15 ns pulsed frequency doubled Nd:YVO_4 laser with a 532 nm wavelength (44). The frequency of the laser was kept under 100 kHz and the power used was less than 1 W. The shape of the laser beam in the study was elongated into a line. Energy distribution across the beam remained

Gaussian, but it was 5μm wide in the y-direction and 200 μm wide in the x-direction. To investigate the concentration and distribution of phosphorus atoms laterally and in the depth of the emitter, secondary ion mass spectroscopy (SIMS) and electron beam induced current (EBIC) measurements were taken. Through SIMS it was determined that laser doping created a heavily doped, shallow emitter, and that the depth of the emitter (250 to 625 nm) increased with pulse energy density (from 2.5 to 4.5 J/cm^2) (44). Phosphorus concentrations at the surface were 10^{20}/cm^3 and were on the order of 10^{18}/cm^3 at the depth of 250 nm for the LDE fired at 2.5 J/cm^2. Through transmission electron microscopy (TEM) of the LDE fired at 2.5 J/cm^2 it was observed that the once-molten silicon re-crystallized free of defects; none were apparent in TEM micrographs (44). In evaluating I-V measurements Esturo-Breton et al. observed a "double diode behavior," which they attributed to non-uniform lateral distribution of dopants across the doped emitter. They present a two diode model, to match their experimental measurements, in which a heavily doped diode contributed most of the current at high positive voltages and a lightly doped diode contributed at low positive voltages (44). Each diode had an associated series resistance and saturation current; those in the highly doped diode were less than those in the lightly doped diode. The authors attribute the reduced resistance and saturation current seen at higher voltages to the highly doped diode, and increased current flow enabled by the larger area associated with it. The ideality factors associated with the lightly doped diode that dominated at low voltage and the highly doped diode that dominated at high voltage were 2.15 and 3.05, respectively. The model of an emitter is more commonly discussed in terms of a quasi neutral region and space charge region associated with one diode (50), but the model presented by Esturo-Breton et al. fit their experimental data well.

Using a 355 nm wavelength laser, Ogane et al. evaluate the formation of LDEs and the effects of laser power on doping depth and concentration. The laser used was a Nd: YAG laser with pulse durations of 15 ns and output power from 0.30 W to 0.55 W (0.51 to 0.93 J/cm^2). Comparing both phosphorus and boron SODs, they fabricated emitters on p-type wafers and

examined the doping of both n+ and p+ emitters, respectively (8). By controlling the power of the laser they were able to alter the depth of the doped emitter region. SIMS measurements indicated that shallower emitters were formed with less powerful laser shots. For a 0.30 W pulse the depth of the emitter, with a concentration of $10^{18}/cm^3$, was approximately 70 nm, whereas for a 0.55 W pulse the depth of the emitter, to a concentration of $10^{18}/cm^3$, was approximately 230 nm. The highest doping concentrations in the very near surface (within 0.3 μm) were $10^{20}/cm^3$ to $10^{21}/cm^3$ for phosphorus and $10^{19}/cm^3$ to $10^{20}/cm^3$ for boron (8). At low powers they found that the performance was limited due to inadequate doping, and at higher powers ablation of the silicon occurred and surface recombination increased, degrading performance. The best results were obtained for cells doped with powers between 0.45 and 0.5 W, but the maximum cell efficiency obtained was 8%. In I-V measurements of the p-n junctions formed by laser doping, an increase in series resistance and leakage current was apparent as compared to junctions created through thermal diffusion. (8). The authors cite crystalline disorder, doping inhomogeneity, and incorporation of carbon or oxygen impurities as sources for reduced performance.

Eisele et al., at the University of Stuttgart, demonstrated the LIMPID procedure to create a "full area" laser doped silicon cell with 18.9 % efficiency (6). The predeposited dopant layer consists of a 60 nm sputter deposited phosphorus film. An 532 nm Nd:YAG laser with a pulse duration 65 ns was used to dope the entire emitter layer on the front surface. The laser pulse melted the surface to a depth of 1 μm, enabling liquid diffusion of the phosphorus dopant (6). In this case, a full area emitter was fabricated instead of selective emitters. The authors did not address any performance loss due to decreased spectral response typically associated with high doping over the entire emitter surface. The cell that achieved 18.9% was of a passivated emitter and rear cell (PERC) type, with SiO_2 passivation at the front and rear surfaces. The cell achieved a very low saturation current density of 88 fA/cm^2 and a short circuit current density (J_{sc}) of 35 mA/cm^2. The authors state that, theoretically, an open circuit voltage (V_{oc}) of 694 mV and J_{sc} of 40 mA/cm^2 could be attained if front surface texture and improvement of the rear side contacts

were implemented. With such improvements they projected an efficiency of 21 % to be possible (6). Given the low J_{sc} and high V_{oc} attainable, Eisele et al. claimed that laser doping did not lead to any lattice defects, and any degradation in cell performance did not result from laser processing the emitter (6). They identified recombination at the rear side contact to be the main source of performance loss in the cell.

On the other hand, Ametowobla et al. attempted to identify the effects of laser doping on device performance by laser irradiating samples with and without a dopant layer on the surface, and highlighted several factors that must be controlled to ensure device performance. They hypothesized initially that discrepancies between theoretically attainable V_{oc} values and those measured in actual cells were due to recombination in the doped emitters due to laser processing (28). By examining saturation current densities and SIMS profiles, they identified two factors that degraded device performance. The first was the choice of dopant precursor. Through evaluation of different doping precursors it was discovered that the choice of dopant source greatly influenced recombination in the emitter. If ultrapure doping precursors were not used, impurities in the precursors were incorporated into the doped emitter and led to increased saturation current densities. The second factor was the laser irradiation on the sample. When irradiating "pre-diffused" emitters without a dopant layer in place an increase in recombination was noted. Defects inherent to the laser firing process occurred, resulting in more recombination, increasing the saturation current density from 25 fA/cm^2 to 45 fA/cm^2 (28). SIMS measurements on the samples laser irradiated without the dopant layer indicated that laser firing caused the incorporation of oxygen, carbon, and nitrogen into the silicon (28). They concluded that, while the increase in recombination was minimal, laser doping led to increased recombination in the LDEs, and laser doping conditions along with the selection of dopant precursor will impact saturation current.

Hameiri et al. (42) studied the effects of different laser processing parameters on the properties of laser doped solar cells, with a solid dopant layer deposited by a spin on process.

The dopant layer was applied on top of a dielectric film that was used for passivation, anti-reflection, and a mask for selective metallization after laser processing. The Nd:YVO_4 532 nm diode pumped, Q-switched laser induced diffusion of dopants in the liquid phase by melting the substrate and removing the dielectric passivation film, creating a selective emitter and self-aligned pattern for subsequent metallization all at once (42). Analyzing the laser doped regions through cross-sectioning, electron beam induced current (EBIC) measurements, and secondary ion mass spectrometry (SIMS) profiling gave insight into the influence of different laser parameters on doping and emitter formation. Different laser diode currents from 14.1 A to 30.2 A were studied, and using EBIC they examined the formation of p-n junctions in the laser doped regions (42). At currents of 26.8 A and higher, ablation of material and laser drilling became an issue. Junction formation was possible but resulted in poor efficiencies under 17% (42). In cases where the diode current was not sufficient to melt the pyramids of the textured front surface, doping still occurred and junctions were formed. The best efficiency achieved was 18.6%, measured on samples fabricated with diode currents of 14.1 A and 16.8 A.

To be implemented in manufacturing, LDE processing should feature as few steps as possible and eliminate the need for high temperature furnace diffusion. Laser assisted selective emitter formation is currently used in manufacturing to create laser grooved buried contacts (LGBC). Commercially, cells with the technology have achieved efficiencies of up to 20% (9) (10) (51). LGBCs rely on laser ablation to create deep trenches (10) (51). Once opened, the laser grooves are subject to high temperature furnace diffusion to induce doping, and subsequent metal plating to fill the grooves. Many proposed laser doping techniques eliminate the need for furnace diffusion, but require removal of the dopant layer after laser doping—an extra step that should also be avoided if possible. The so-called “passdop” layer implemented by Suwito et al. (16) is of interest in LDE processing because the dopant layer does not need to be removed, but is an integral part of the passivation structure. Herein we investigate the adaption of such a layer,

using doped a-Si:H passivation/dopant structures, in the creation of selective laser doped emitters (LDEs).

LDE Experiments

Background

To examine the manufacturability of LDEs for solar devices, an evaluation of different laser processing conditions was performed with two different solid dopant sources combined with different passivation layers. The experiments performed provided insight into laser-material interactions and the effects of processing parameters on different dopant and passivation structures.

Antimony was investigated as a dopant source, e-beam deposited as a pure layer between two layers of silicon, on top of passivation layers to be doped through. The sandwich structure of Sb between silicon was implemented to reduce volatilization of the Sb when laser processed, due to its low vapor pressure and evaporation temperature. The silicon and Sb layers were all 50 nm thick deposited by e-beam evaporation. The passivation layers used with the Sb dopant samples were either a layer of 80 nm a-Si:H, or layers of 10 nm a-Si:H and 100 nm of SiO_x, deposited using PECVD. The a-Si:H films were deposited by flowing silane (SiH_4) and hydrogen (H_2) at rates of 30 sccm and 300 sccm, respectively, into the PECVD reactor. Deposition was performed at 120°C at a pressure of 2 Torr with a power of 25 W. The SiO_x films were deposited using N_2O, SiH_4, and an N_2 purge gas, with flow rates of 1800 sccm, 18 sccm, and 1800 sccm, respectively. Deposition was performed at 250°C at a pressure of 3.5 Torr with a power of 100 W.

In parallel, phosphorus was investigated as a dopant source. The P was incorporated into the passivation layers in an n+a-Si:H film deposited using PECVD. The phosphorus dopant

source was integrated into a doped a-Si:H films (n+ a-Si:H) by introducing phosphine (PH_3) gas in addition to the SiH_4 and H_2 gases during deposition of the passivation stacks. The two different passivation structures were either layers of 10 nm a-Si:H, 20 nm n+ a-Si:H, and 100 nm SiO_x, or layers of 10 nm a-Si:H and 100 nm n+ a-Si:H. To deposit the n+ a-Si:H the respective flow rates of PH_3, SiH_4 and H_2 were 15 sccm, 30 sccm, and 285 sccm. Deposition was performed at 200°C at a pressure of 2 Torr with a power of 50 W. The recipes for the a-Si:H films and the SiO_x films were the same as previously described. The time of each deposition was dependent on the required layer thickness. The passivation and dopant layers for each sample can be seen in Figure 3-1.

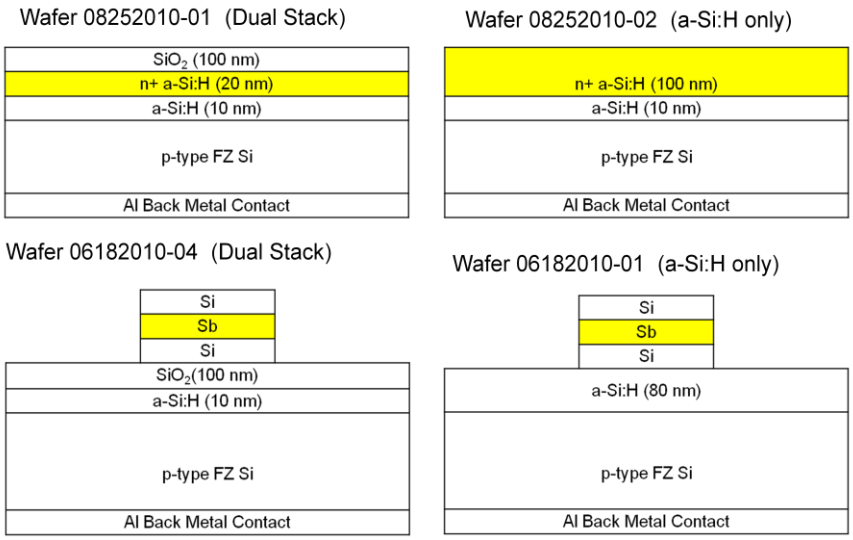


Figure 3-1: Passivation and dopant structures.

After the deposition of passivation and dopant layers, laser doping on each sample was performed using one of three lasers: a yitterbium doped 1070 nm continuous wave, single mode fiber laser; a Nd:YVO_4 355 nm pulsed 30 ns frequency tripled Q-switched laser; and a Nd:YAG 1064 nm, 4 ns Q-switched laser. Experiments were performed with each laser to determine if LDEs could be created, and to ascertain the range of appropriate processing parameters for each sample type. Power and gated pulse duration were varied for the 1070 nm continuous wave laser.

Frequency and number of pulses were varied for the 355 nm, pulsed 30 ns laser. Energy per pulse was varied for the 1064 nm, 4 ns laser. Processing conditions were varied along the x- and y-axes of each sample to create an array of different processing conditions, shown in Figure 3-2. Each processing condition was shot nine times on one pad of the sample to create nine identical emitters.

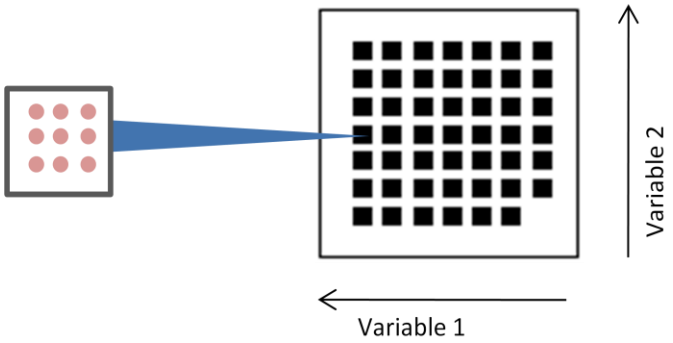


Figure 3-2: Image of a LDE array sample.

Ranges of processing variables for each laser and sample are shown in Table 3-1. Note that for the 1064 nm laser only one variable was altered along the y-axis of the sample. For the 1070 nm laser processed on the n+ a-Si:H samples, the variable of power was increased to a range of 34 W to 100 W due to the increased thickness of the samples' passivation and dopant layers. The P dopant layers were more resilient than the Sb dopant layers and required higher laser powers to affect the sample surface. On the Sb doped samples powers of only 15 W to 45 W were tested.

Table 3-1: Sample processing conditions.

Passivation	Dopant	Laser	Variable 1 (x-axis)	Variable 2 (y-axis)
80 nm a-Si:H	Sb	355 nm	1 pulse to 7 pulses	41 µJ/pulse to 155 µJ/pulse
10 nm a-Si:H/ 100 nm SiO_x	Sb	355 nm	1 pulse to 7 pulses	41 µJ/pulse to 155 µJ/pulse
80 nm a-Si:H	Sb	1070 nm	50µs to 350 µs	15.2 W to 45 W
10 nm a-Si:H/ 100 nm SiO_x	Sb	1070 nm	50µs to 350 µs	15.2 W to 45 W
80 nm a-Si:H	Sb	1064 nm	-	285 µJ/pulse to 35 µJ/pulse
10 nm a-Si:H/ 100 nm SiO_x	Sb	1064 nm	-	285 µJ/pulse to 35 µJ/pulse
10 nm a-Si:H/ 100 nm n+ a-Si:H	P	355 nm	1 pulse to 7 pulses	41 µJ/pulse to 155 µJ/pulse
10 nm a-Si:H/ 20 nm n+ a-Si:H/ 100 nm SiO_x	P	355 nm	1 pulse to 7 pulses	41 µJ/pulse to 155 µJ/pulse
10 nm a-Si:H/ 100 nm n+ a-Si:H	P	1070 nm	50µs to 350 µs	34 W to 100 W
10 nm a-Si:H/ 20 nm n+ a-Si:H/ 100 nm SiO_x	P	1070 nm	50µs to 350 µs	34 W to 100 W
10 nm a-Si:H/ 100 nm n+ a-Si:H	P	1064 nm	-	35 µJ/pulse to 285 µJ/pulse
10 nm a-Si:H/ 20 nm n+ a-Si:H/ 100 nm SiO_x	P	1064 nm	-	35 µJ/pulse to 285 µJ/pulse

Characterization

Each LDE processed on a particular sample was characterized using SEM and electrically evaluated by taking I-V measurements. The results of each investigation were used to determine the appropriate wavelengths and laser processing conditions to create LDEs, and to identify a passivation and dopant structure suitable for laser doping. An attempt to down select the best laser processing parameters for LDE formation was performed by the comparison of LDE I-V measurements. The depth and geometry of LDEs was correlated to laser processing parameters through cross-section and junction delineation. Successful junction delineation provided support for laser doping and emitter creation, in addition to the I-V measurements taken.

I-V Measurements

When measuring current during a voltage sweep on an ideal diode, contributions from two regions of the diode are apparent. At low voltages, the current is primarily from recombination in the space charge region (scr) of the diode, and the diode ideality factor is approximately 2. At higher voltages, greater than the turn on voltage of ~0.4 V, the current is largely due to recombination in the quasi neutral region (qnr). The ideality factor of the qnr should be equal to 1 in an ideal diode. The equation for current in a diode is shown in Equation 1, where $I_{o,scr}$ and $I_{o,qnr}$ are the saturation currents in the scr and qnr, and n_{scr} and n_{qnr} are the ideality factors in the scr and qnr. Series resistance is given by r_s.

$$I = I_{o,scr}\left(e^{\frac{q(V-Ir_S)}{nkT}} - 1\right) + I_{o,qnr}\left(e^{\frac{q(V-Ir_S)}{nkT}} - 1\right) \quad (1)$$

In Equation 1, V is voltage, I is current, q is the charge on an electron, k is the Boltzmann constant, and T is temperature (50).

A I-V measurement of a diode with contributions from the scr and the qnr is shown in Figure 3-3, after that presented in reference (50). The data is plotted with a log scale of current. Contributions from the scr and qnr are indicated on the figure.

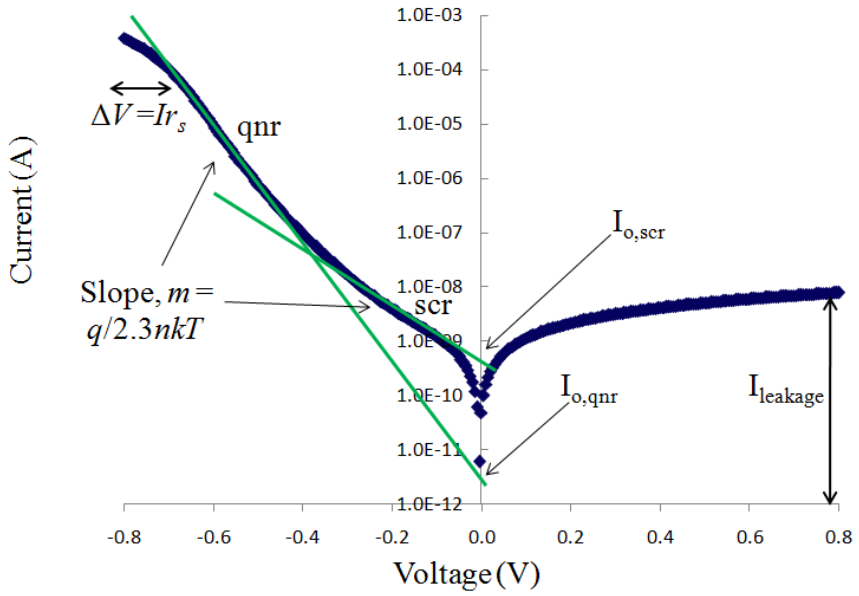


Figure 3-3: I-V curve for a diode with series resistance, schematic after (50).

The ideality factors and saturation currents of each region can be obtained from the curve to provide metrics to gauge the quality of the diode. The ideality factor, *n*, can be extracted from the slope, *m*, of each region, according to Equation 2.

$$m = \frac{q}{\ln(10)nkT} \tag{2}$$

The saturation current, I_o, is found by extrapolating the linear portion of each region to V= 0 V and is given by the intercept value. Very low saturation currents result from minimal recombination in the diode, indicating a high quality device. Leakage current of the diode is given by the maximum current value measured in reverse bias. Low leakage current and low series resistance are desirable. Series resistance is determined from the leveling off of current at higher voltages, according to Equation 3, where I is the current approached, r_s is the series resistance, and ΔV is the change in voltage.

$$\Delta V = Ir_s \tag{3}$$

For each sample, I-V measurements were taken for LDEs prepared with different laser processing parameters. Measurements were performed on a Suss probe station through a Keithley 4200 semiconductor characterization system. Out of the nine LDEs processed per pad,

only one was measured. Statistically this is a small data set to draw conclusions from; however, as a preliminary investigation I-V measurements were useful in assessing the formation of LDEs given the wide range of variables under comparison. For LDEs on which I-V measurements could be taken, the shape of the I-V curves was assessed qualitatively. Understanding that the severity of series resistance, and magnitude of leakage current, can be determined from the shape of the I-V curve, measurements were easily compared at a glance. This first pass allowed for initial identification of LDEs doped with processing conditions that warranted further in depth investigation. I-V measurements selected could then be quantitatively compared by extrapolating ideality factors, saturation currents, and series resistance from the curves.

Antimony Doped Samples

The antimony dopant samples on each passivation structure were processed with a Nd:YVO_4 355 nm pulsed 30 ns frequency tripled Q-switched laser; a yitterbium doped 1070 nm continuous wave gated pulse single mode fiber laser; and a Nd:YAG 1064 nm, 4 ns Q-Switched laser. Regardless of wavelength and pulse duration, the antimony dopant structure exhibited flaking and peeling; however, despite poor resilience of the dopant layer structure, I-V measurements were attempted on each sample. I-V measurements were only obtained on samples irradiated with the 355 nm, 30 ns laser.

Figure 3-4 shows the I-V curves measured for LDEs processed with the 355 nm laser on the Sb dopant stack on top of the a-Si:H passivated sample. Taking a qualitative look at the I-V curves it is clear that there is a large series resistance in many of the LDEs, limiting current at higher voltages. Leakage current is also very large ranging from $1x10^{-9}$ A to $1x10^{-6}$ A. The two slope regions of current contributions from the qnr and scr are not apparent in most of the curves. The majority of processing conditions do not appear useful for the creation of low leakage, low

series resistance diodes. Although diodes were created by doping with Sb, the poor integrity of the dopant source structure makes it unsuitable for use in manufacturing.

Figure 3-5 shows the I-V curves measured for LDEs processed with the 355 nm laser on the Sb dopant stack on top of the a-Si:H/SiO_x passivated sample. A qualitative look at the I-V curves reveals that with the a-Si:H/SiO_x passivation, current at forward bias is further reduced and series resistance is even greater than in LDEs processed on the a-Si:H passivated sample. Leakage current is reduced on the a-Si:H/SiO_x passivated sample as compared to the a-Si:H passivated sample, with values on the order of $1x10^{-8}$ A. The SiO_x layer appears to play a role in the current reduction in both forward and reverse bias. Paths for current flow other than through the diode are blocked by the insulating layer thereby reducing leakage. Despite lower leakage current, the low currents achieved in forward bias, and the high series resistance thereby indicated, make these LDEs unsuitable for further investigation.

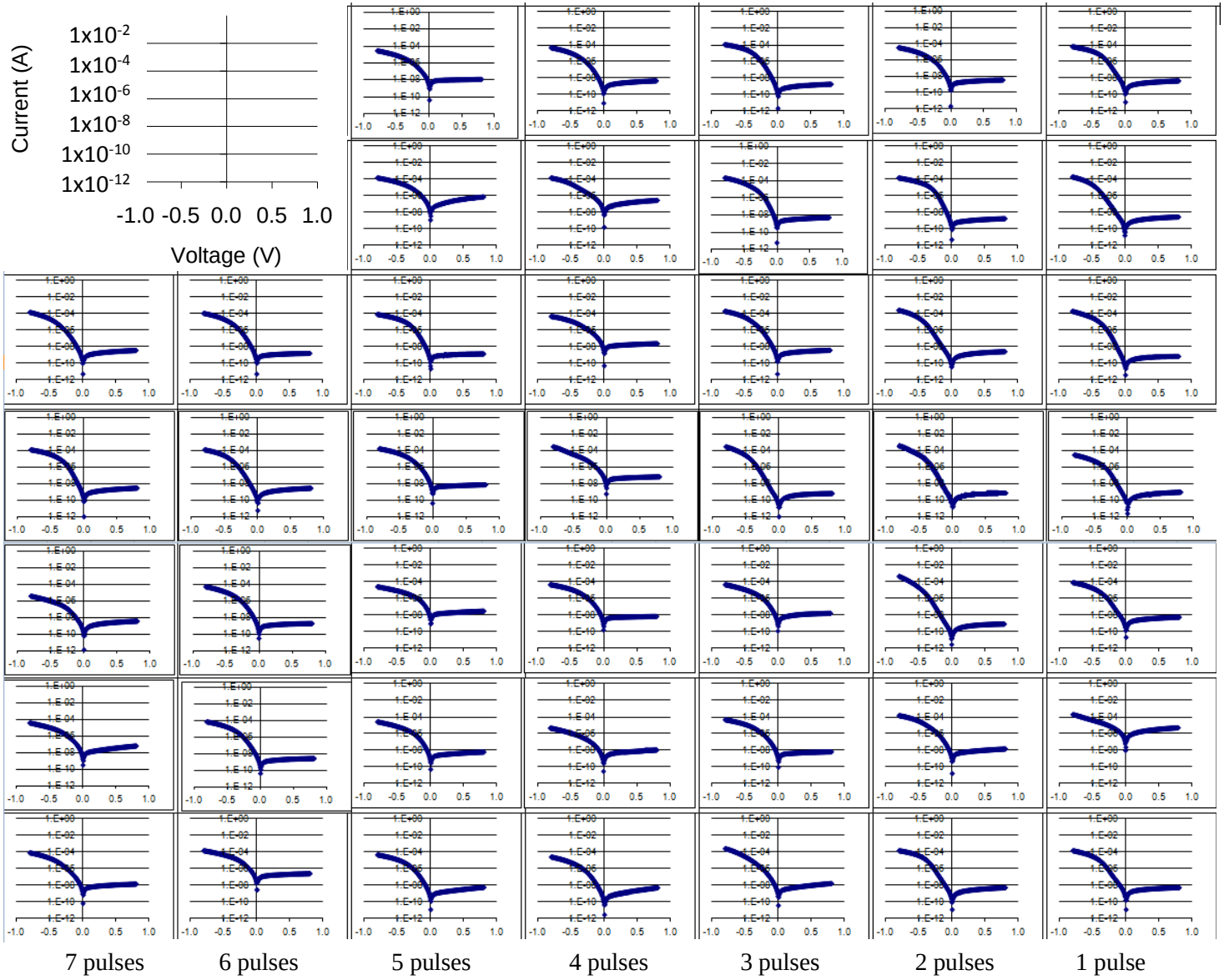


Figure 3-4: I-V curves for LDEs on a-Si:H passivated Sb sample, 355 nm laser.

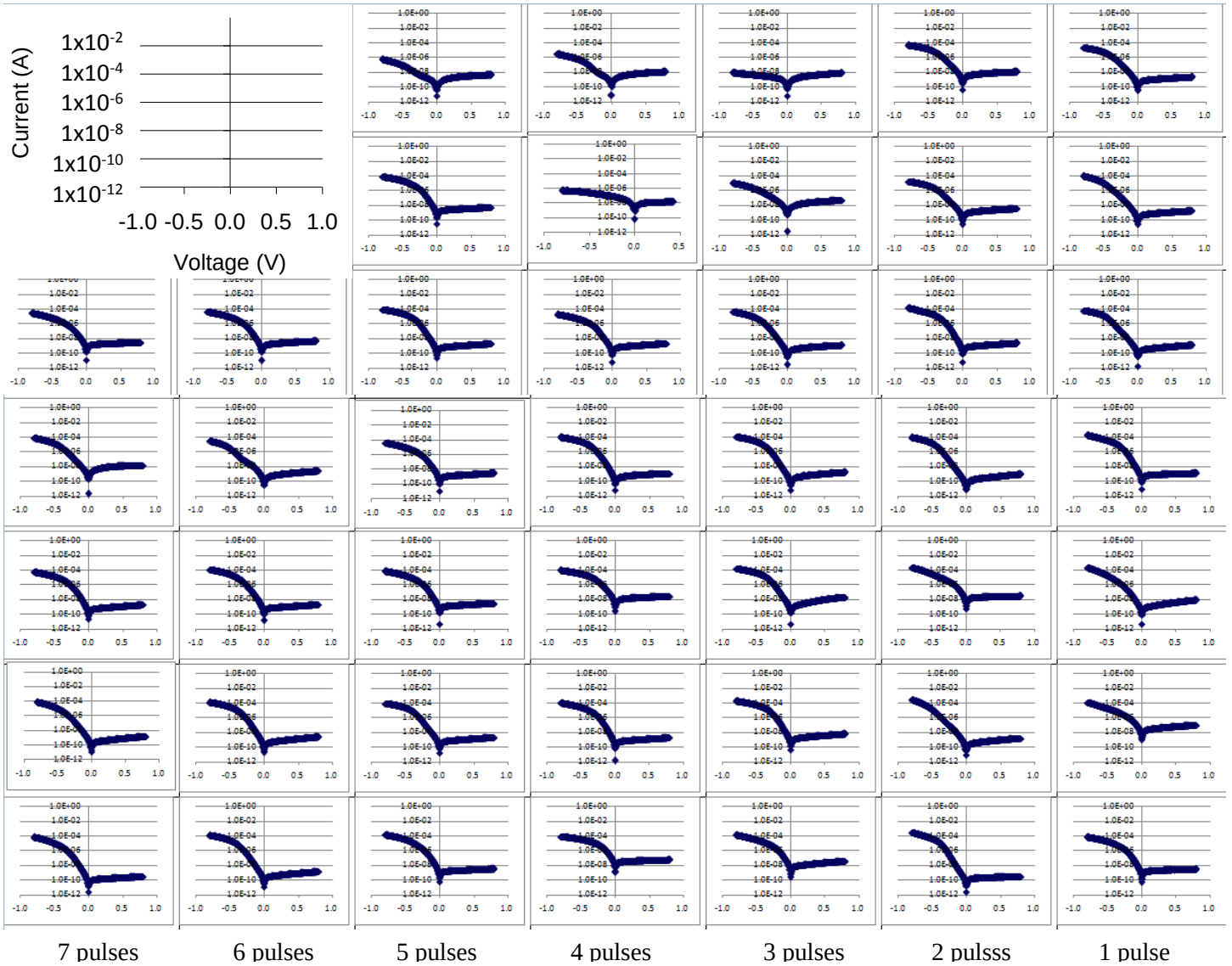


Figure 3-5: I-V curves for LDEs on a-Si:H/SiO_x passivated Sb sample, 355 nm laser.

The SEM images taken for the LDEs doped with the 355 nm laser on the Sb dopant stack on top of the a-Si:H passivated sample, shown in Figure 3-6, reveal the extent of delamination that occurs with laser processing. The appearance of the LDEs in part supports the results of the I-V measurements; poor diode results correlate to higher energies and number of pulses (more ablation and delamination).

The SEM images for the Sb doped a-Si:H/SiO_x passivated sample, in Figure 3-7, exhibit delamination and ablation as well. Penetration into the substrate for these samples appears to be shallower, likely due to the presence of the SiO_x film in the passivation stack, but the Sb dopant layers still deteriorate.

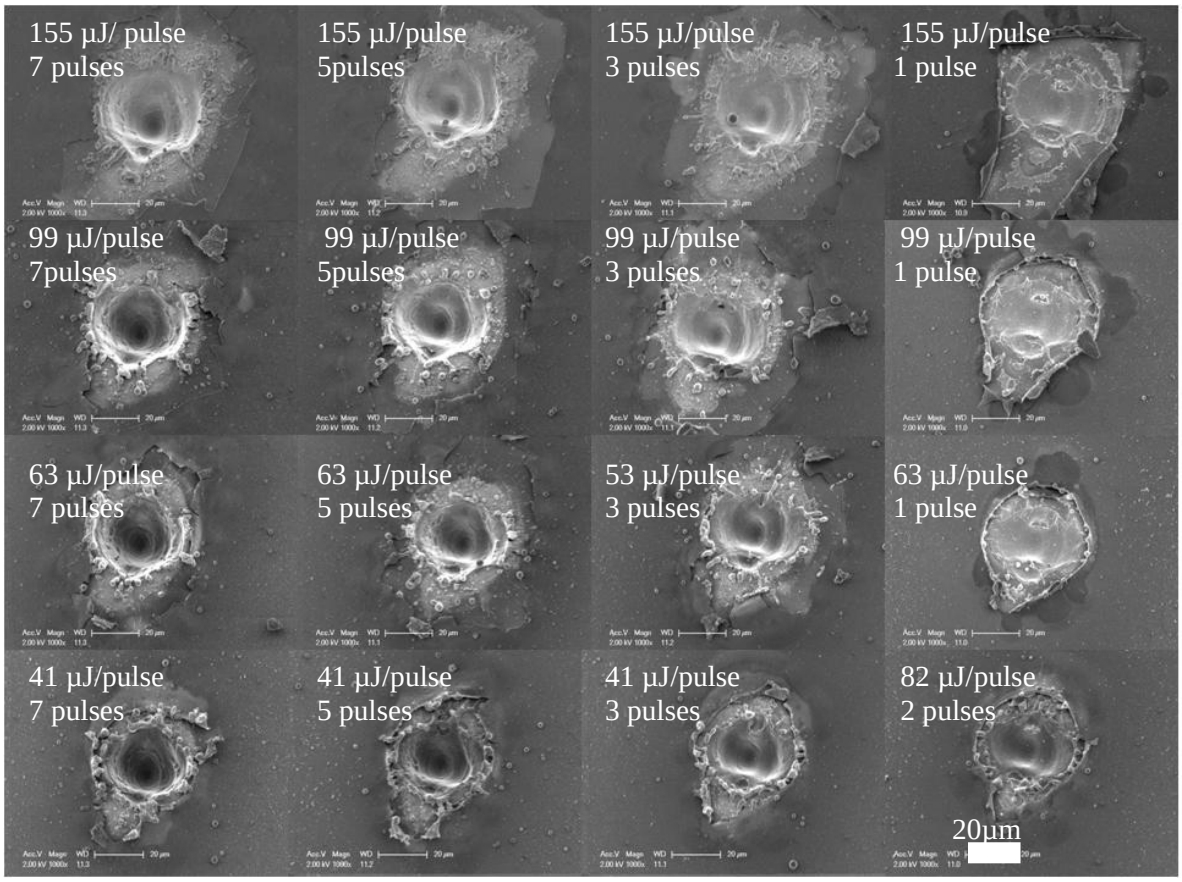


Figure 3-6: SEM images of LDEs on a-Si:H passivated Sb sample, 355 nm laser.

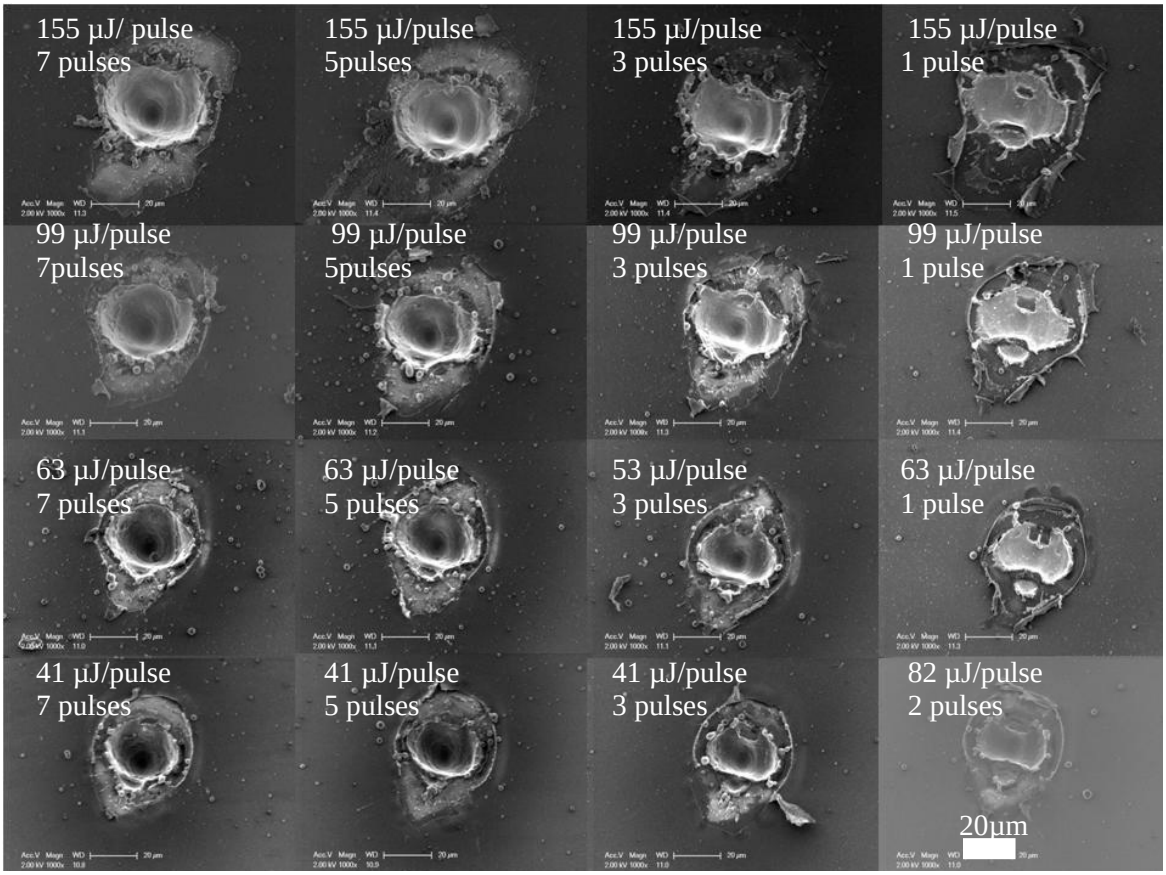


Figure 3-7: SEM images of LDEs on a-Si:H/SiO_x passivated Sb sample, 355 nm laser.

I-V measurements for LDEs processed with the 1070 nm laser could not be measured on Sb doped samples with either passivation stack. The 1070 nm wavelength is less absorbed in the silicon than the 355 nm wavelength, but the longer µs pulses of the laser likely volatilized the Sb dopant source before any melting and liquid diffusion can take place. Spots exhibit little ablation, but delamination of the Sb dopant structure is apparent. Figure 3-8 and Figure 3-9 show SEM images of laser processed spots on the a-Si:H passivated sample, and the a-Si:H/SiO_x passivated sample, respectively.

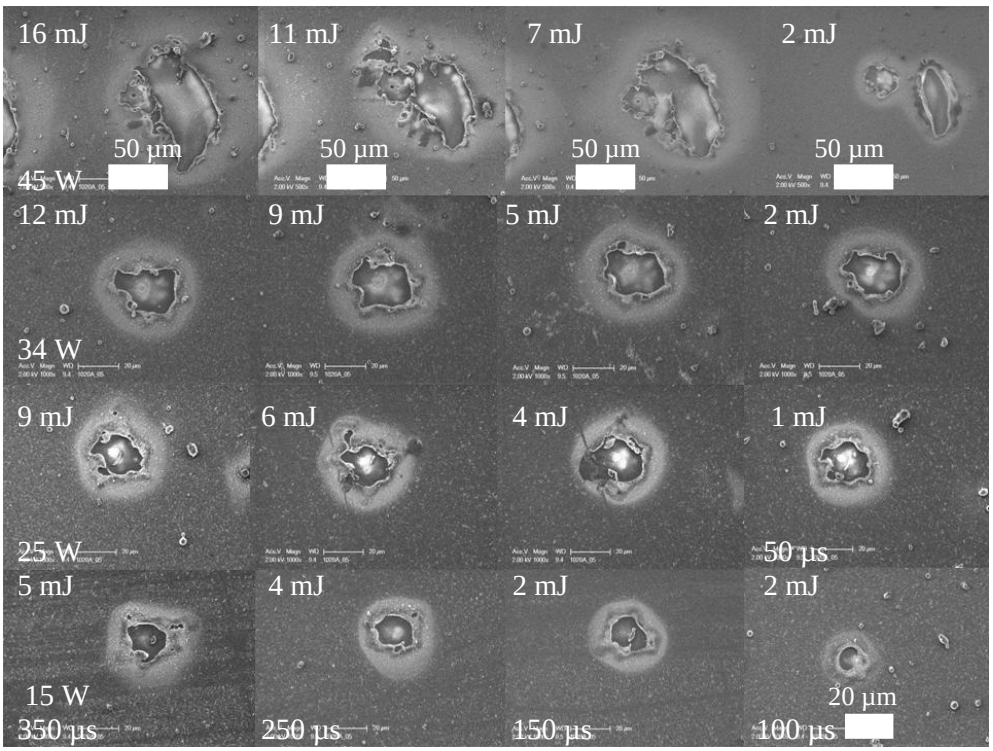


Figure 3-8: SEM images of LDEs on a-Si:H passivated Sb sample, 1070 nm laser. The 20 nm scale marker applies to all micrographs not otherwise labeled.

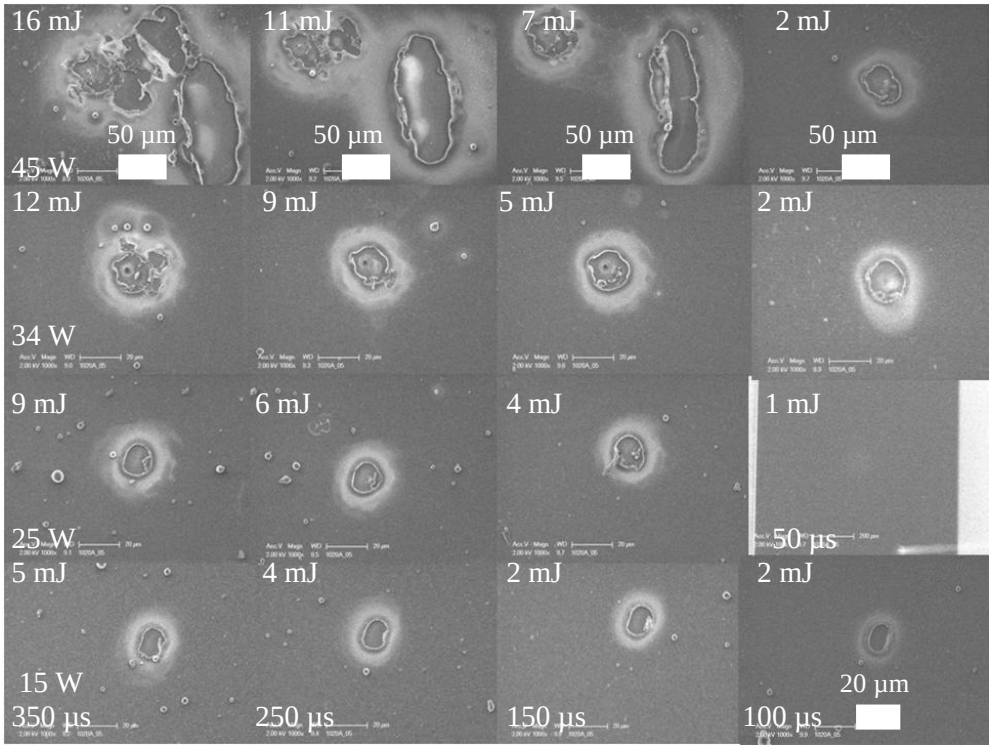
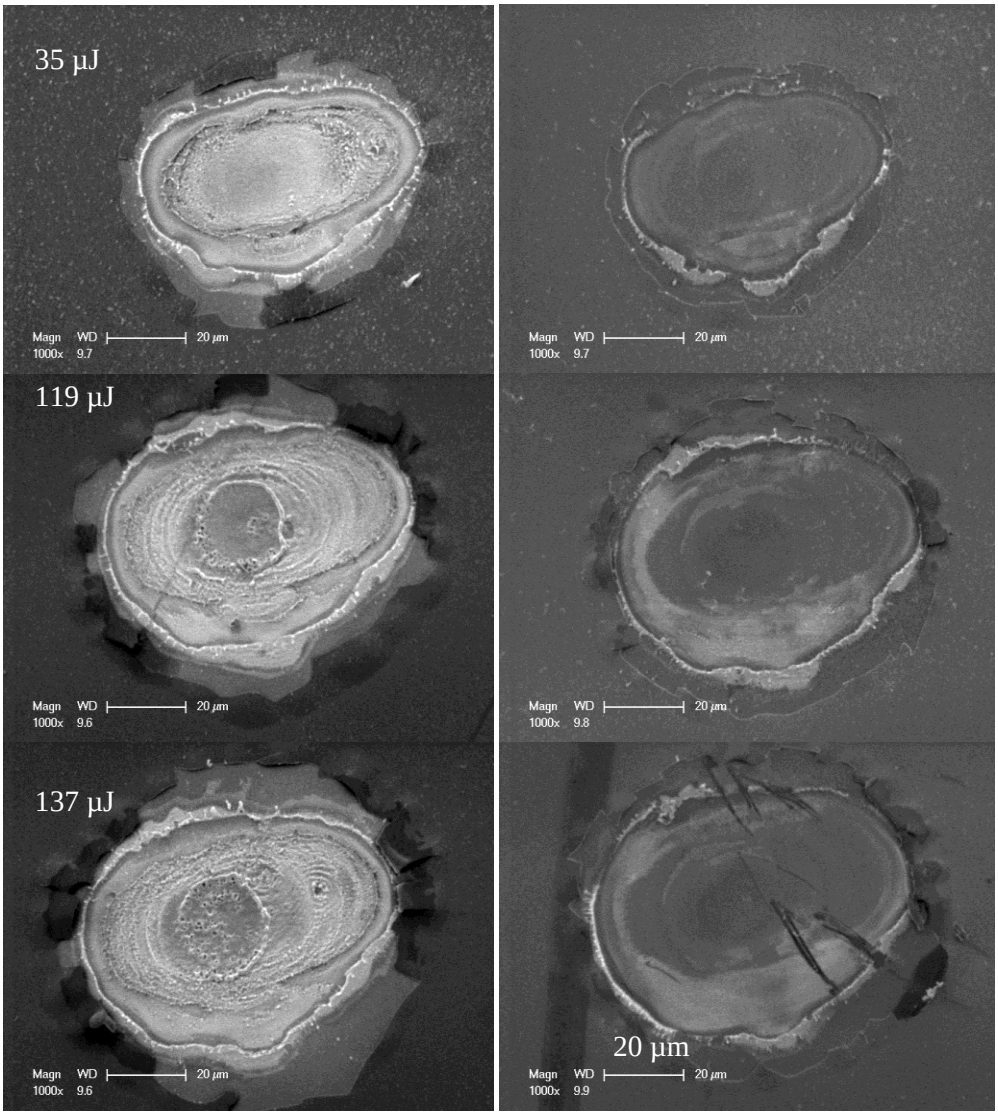


Figure 3-9: SEM images of LDEs on a-Si:H/SiO_x passivated Sb sample, 1070 nm laser. The 20 nm scale marker applies to all micrographs not otherwise labeled.

I-V measurements for LDEs processed with the 1064 nm, 4 ns laser could not be measured on Sb doped samples with either passivation stack. Delamination is apparent in the SEM images of select laser processed spots processed on the a-Si:H and the a-Si:H/SiO_x passivated samples shown in Figure 3-10.



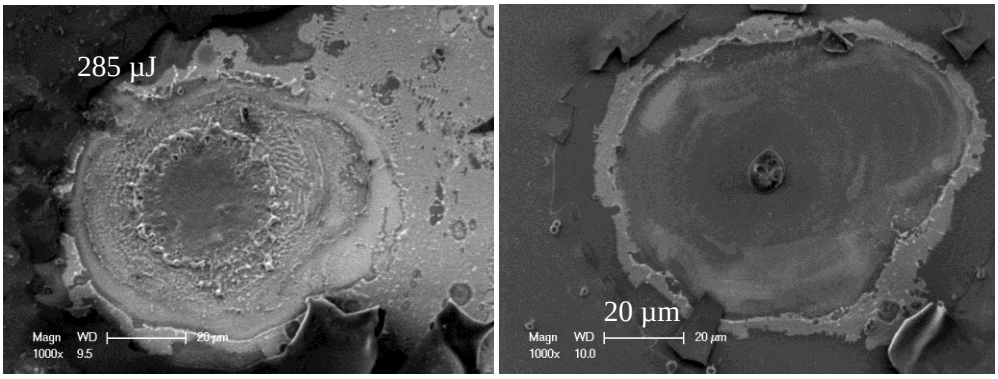


Figure 3-10: SEM images of processed spots on Sb doped (left) a-Si:H passivated sample and (right) a-Si:H/SiO_x passivated sample, 1064 nm laser.

Our inability to fabricate viable LDEs on the Sb dopant structures with the 1070 nm laser and 1064 nm laser, and the extensive delamination and volatilization that result from processing do not lend the structure to further investigation for use in manufacturing.

Phosphorus Doped Samples

The two phosphorus dopant structures were processed with a Nd:YVO_4 355 nm, pulsed 30 ns frequency tripled Q-switched laser; a yitterbium doped 1070 nm continuous wave, gated pulse single mode fiber laser; and a Nd:YAG 1064 nm, 4 ns Q-Switched laser. The sample structures featured passivation/dopant layers of 10 nm a-Si:H, 20 nm n+ a-Si:H, and 100 nm SiO_x, or layers of 10 nm a-Si:H and 100 nm n+ a-Si:H. Phosphorus was incorporated into the layers referred to as n+ a-Si:H. Diode characteristics were successfully measured on each sample processed with the different lasers, and several LDEs were identified for further quantitative analysis.

The I-V curves in Figure 3-11 were taken for LDEs on the a-Si:H/n+ a-Si:H passivated sample processed with the 355 nm, 30 ns laser. Looking at the curves qualitatively, series resistance becomes a problem on those samples doped with multiple pulses per shot, which is apparent by the leveling off of current with increasing negative bias. Leakage current for the

LDEs with minimal series resistance are on the order of $1x10^{-8}$ A. LDEs with leakage current values larger than $1x10^{-8}$ A do not merit further investigation. Those that will be investigated further are outlined in green. Some of the curves measured appear to exhibit the two slope regions characteristic of current contributions from the qnr and scr. Many of the LDEs that warrant further study were processed with fewer pulses per pulse and lower energies per pulse.

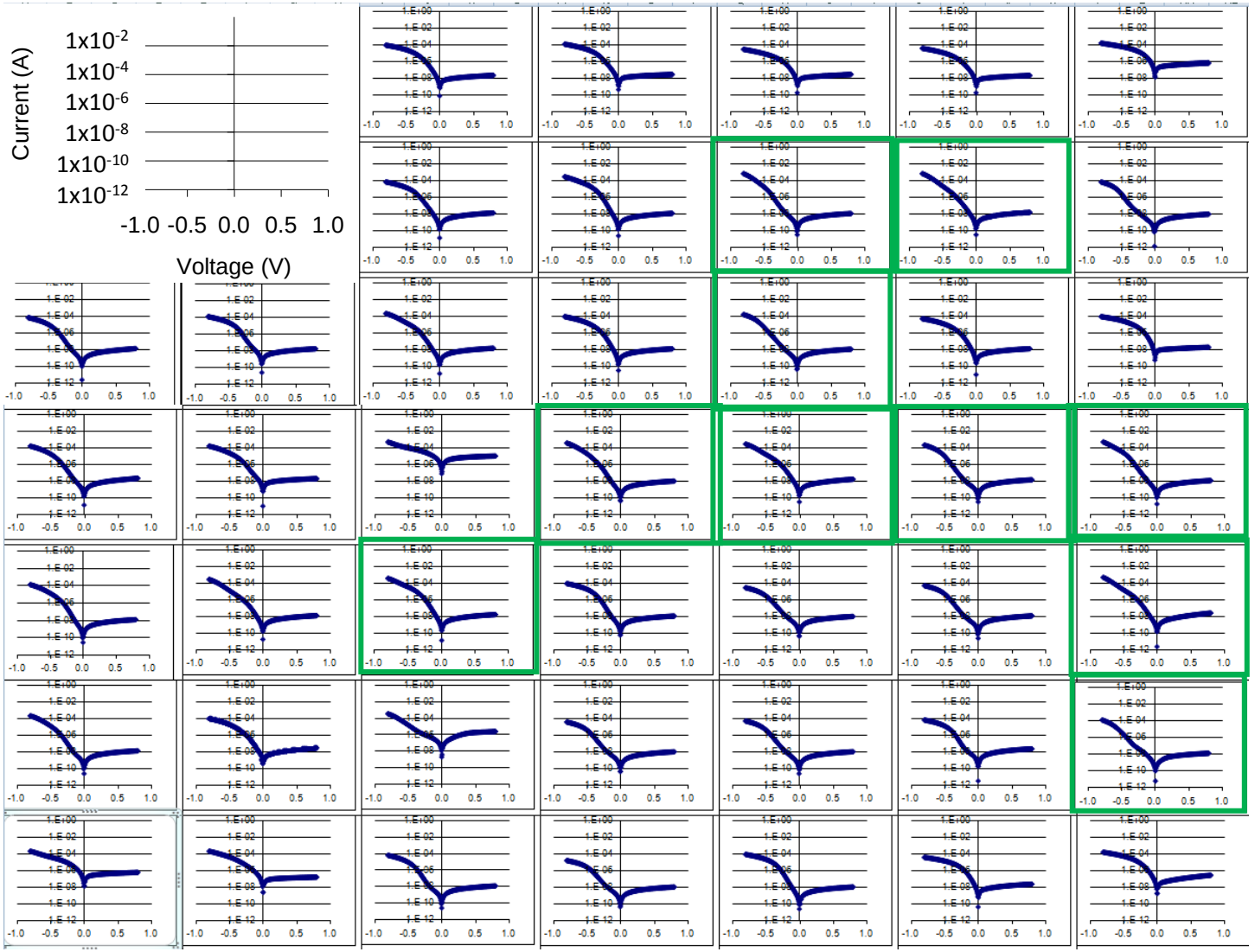


Figure 3-11: I-V curves for LDEs on a-Si:H/n+ a-Si:H passivated sample, 355 nm laser.

Scanning electron microscope images of the LDEs created on the a-Si:H/n+a-Si:H passivated sample with the 355 nm laser are shown in Figure 3-12. With increased number of pulses ablation and drilling of the silicon become apparent. The amount of energy per pulse correlates to the diameter of the laser processed spot and the number of pulses per shot correlates to the depth of the spot into the silicon. Material ablation is apparent for each LDE, but those processed at higher energies and more pulses per shot exhibit the most. Unlike the Sb doped samples, delamination and flaking of the dopant and passivation layers are not apparent; the doped a-Si:H/n+a-Si:H is compatible with the materials system and adheres well. Volatilization of the dopant is not a concern since the P dopant was incorporated into the n+a-Si:H layer.

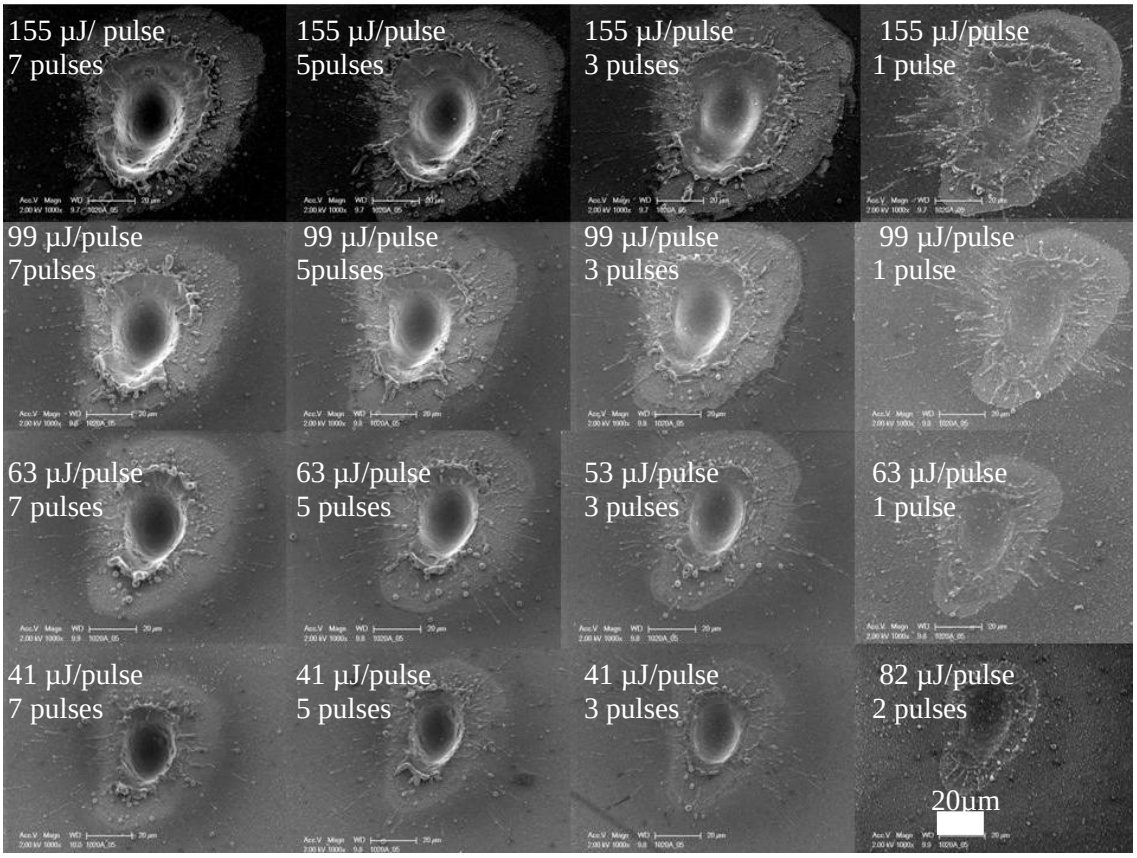


Figure 3-12: SEM images of LDEs on a-Si:H/n+a-Si:H passivated sample, 355 nm laser.

Figure 3-13 shows the I-V curves measured for LDEs processed with the 355 nm laser on the a-Si:H/n+a-Si:H/SiO_x passivated sample. A qualitative look at these curves shows a very

large series resistance exists in these LDEs, greater than that seen in the I-V measurements of LDEs created on the n+a-Si:H/a-Si:H passivated sample. Leakage current varies for LDEs across the sample, but values as low as $1x10^{-9}$ A are achieved. The SiO_x layer plays a role in current reduction in both forward and reverse bias, blocking current paths that would otherwise be open with a non-insulating top most layer. Despite lower leakage current in some of the I-V measurements for LDEs processed with the 355 nm laser, the high series resistance seen in the measurements makes the LDEs unsuitable for use in solar cells, and from this sample set none will be examined further.

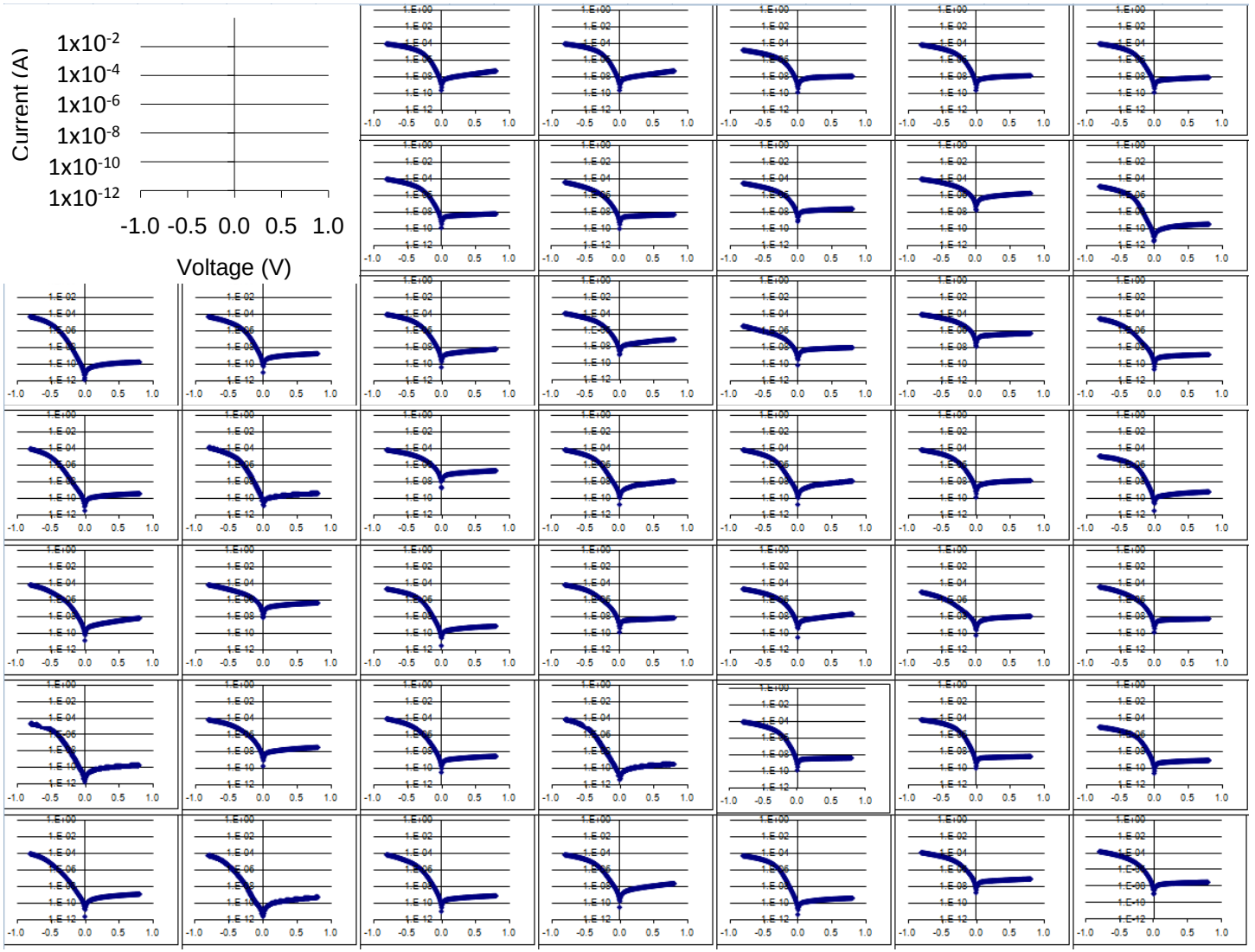


Figure 3-13: I-V curves for LDEs on a-Si:H/SiO_x passivated sample, 355 nm laser.

SEM images taken of the LDEs created on the a-Si:H/n+a-Si:H/SiO_X passivated sample are shown in Figure 3-14. The laser processed spots are smaller in diameter than those created on the a-Si:H/n+a-Si:H passivated sample due to the SiO_x layer. Despite the robust SiO_x layer, ablation and drilling of the Si occur. The short 30 ns pulses and the absorption of the 355 nm wavelength in silicon lead to the ablation observed. In this particular passivation structure the dopant source layer is only 20 nm thick, whereas with the a-Si:H/n+a-Si:H passivation structure the dopant source layer was 100 nm thick. Any ablation and removal of material on this sample will lead to less doping of P in the silicon. The thin dopant source layer will be expelled rather than incorporated into the substrate, which could make formation of highly doped emitters difficult.

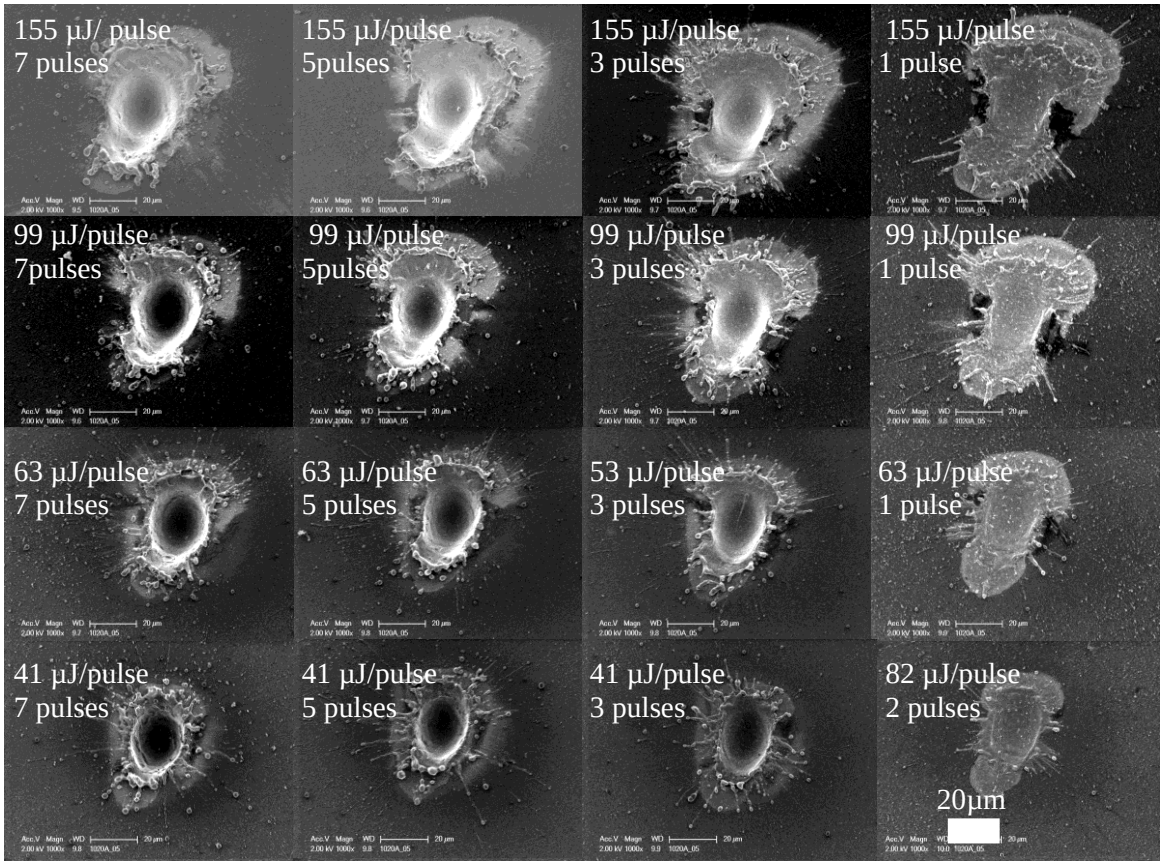


Figure 3-14: SEM images of LDEs on a-Si:H/n+a-Si:H/SiO_x passivated sample, 355 nm laser.

I-V curves for LDEs processed with the 1070 nm µs laser on the a-Si:H/n+a-Si:H passivated sample are shown in Figure 3-15. The majority of curves taken on LDEs for this sample show low series resistance and many look promising for use in a cell, indicating a wide range of processing conditions suitable for manufacturing with this passivation structure. Leakage current is on the order of $1x10^{-8}$ A for the majority of measured LDEs. Measurements were not possible on pads shot with lower powers and lower durations because laser processed spots were not visible. The large powers used to create LDEs were necessitated by the thickness of the n+a-Si:H passivation/dopant structures. Those LDEs suitable for further investigation are highlighted in green.

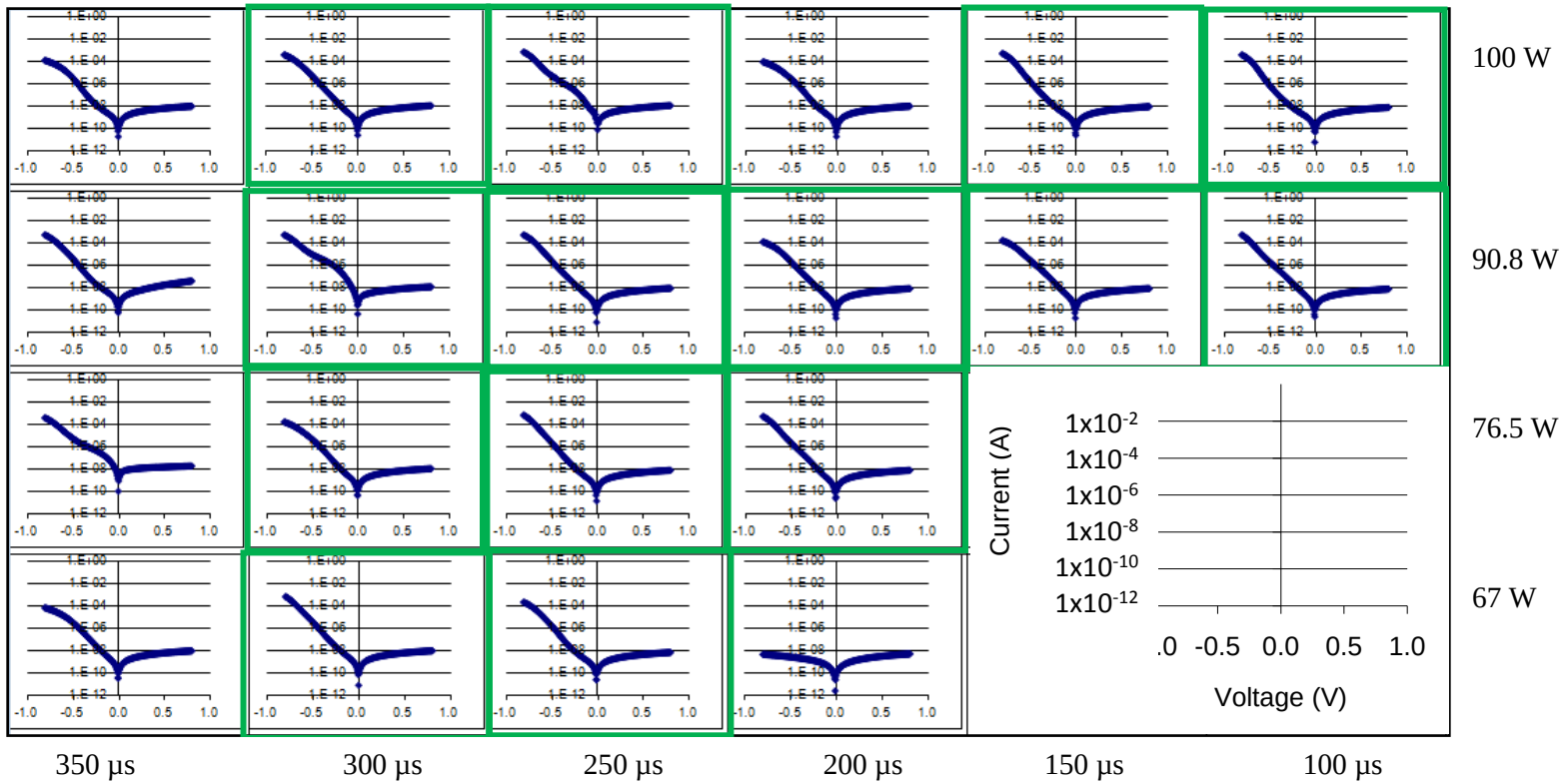


Figure 3-15: I-V curves for LDEs on a-Si:H/n+a-Si:H passivated sample, 1070 nm laser.

Images of the LDEs created on the a-Si:H/n+a-SiH passivated sample created with the 1070 nm laser are shown in Figure 3-16. The visible diameter of the LDEs ranges from approximately 10 to 20 µm. Without sufficient power or pulse duration the laser has no impact on the sample surface and an LDE is not created. The shape of the LDEs is similar to the LFCs fired with the 1070 nm laser, although in this case the center peaks of the processed spots are slightly off center. Their irregular shape could be the result of a poorly focused laser beam.

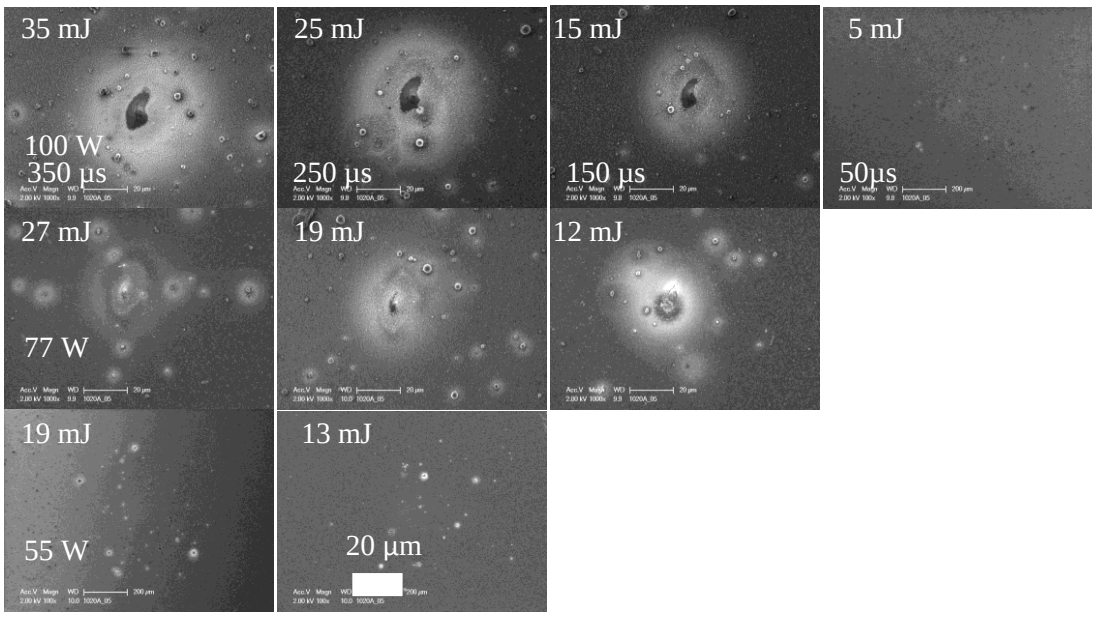


Figure 3-16: SEM images of LDEs on a-Si:H/n+a-Si:H passivated sample, 1070 nm laser.

I-V curves of LDEs fabricated on the a-Si:H/n+a-Si:H/SiO_x passivated sample are shown in Figure 3-17. Series resistance is apparent in LDEs processed at high powers, but at lower powers and pulse durations it is minimal. The lowest leakage currents yet attained were measured on LDEs formed on this sample, with the best on the order of $1x10^{-11}$A. The low leakage is a result of the SiO_x passivation overlay and the minimal damage caused by the laser. Several promising laser conditions were apparent on this sample structure. The I-V curves were some of the best attained in the entire experiment, with low series resistance and low leakage current. Those highlighted in green will be examined later. Without sufficient power or pulse duration the laser did not affect the surface and no LDE were present to be measure. Higher

powers and longer pulse durations were require to create LDEs on the robust a-Si:H/n+a-Si:H/SiO_x passivation structure.

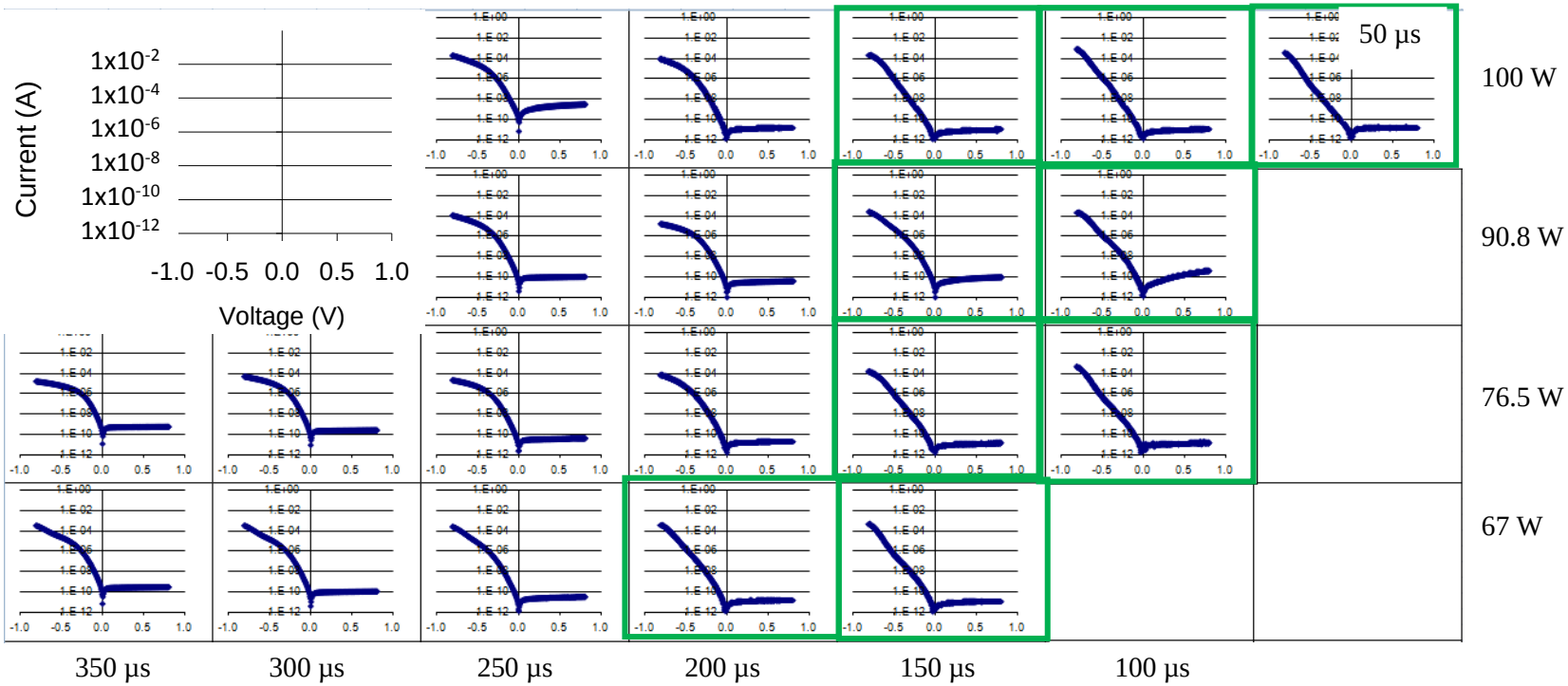


Figure 3-17: I-V curves for LDEs on a-Si:H/n+a-Si:H/SiO_x passivated sample, 1070 nm laser.

Images for the LDEs created on the a-Si:H/n+a-Si:H/SiO_x sample are shown in Figure 3-18. They have exceedingly small diameters on the order of 10-15 µm, and below a certain fluence threshold no laser processed spot was visible. That threshold varies depending on the power used, but ranges between 12 and 25 kJ/cm^2. LDEs that are visible appear to cause very little surface damage. There is no ablation or expulsion of material apparent with use of the 1070 nm wavelength and µs duration pulse length. Based on I-V characteristics and SEM observations, LDEs created on the a-Si:H/n+ a-Si:H/SiO_x sample with the 1070 nm laser show the most promise for use in a solar cell.

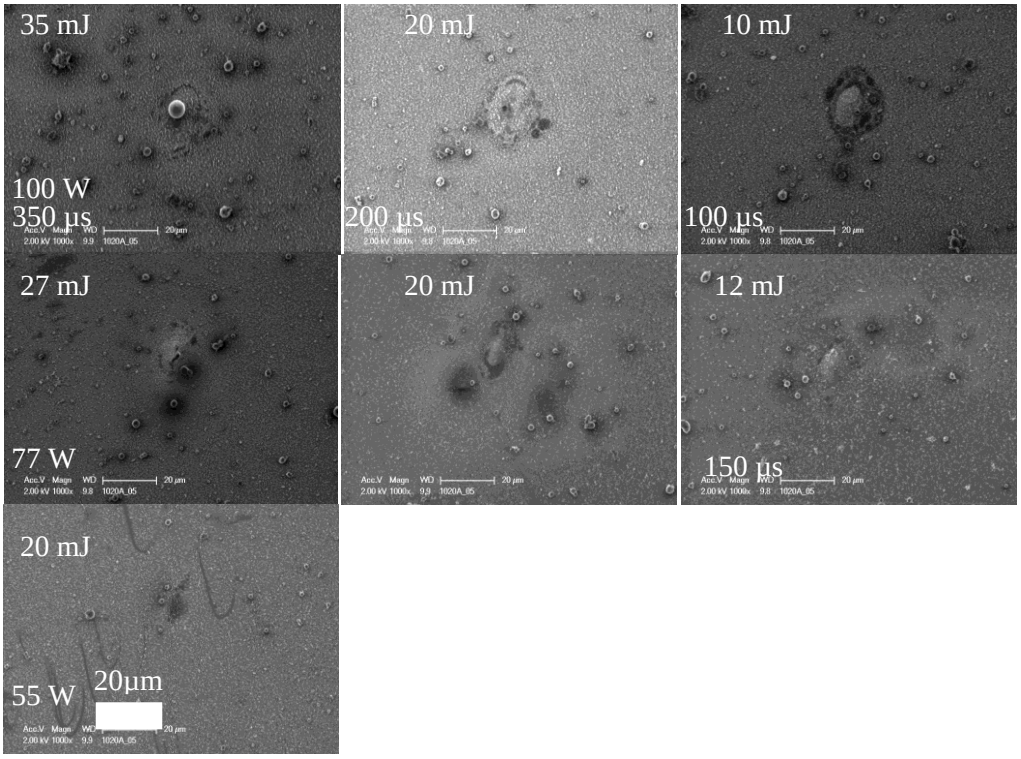


Figure 3-18: SEM images of LDEs on a-Si:H/n+a-Si:H/SiO_x passivated sample, 1070 nm laser.

I-V measurements of the LDEs made with the 1064 nm, 4 ns pulse laser on the a-Si:H/n+a-Si:H passivated sample are shown in Figure 3-19. The I-V characteristics of each LDE, except that created with 285 µJ/pulse, show low series resistance and low leakage currents on the

order of $1x10^{-8}$ A. The laser processed spots do not exhibit drilling, or as much ablation, as those processed with the 355 nm 30 ns laser, but neither are they as mild as the spots created with the 1070 nm microsecond laser. Some ablation is apparent. Unlike the 355 nm wavelength laser, the 1064 nm wavelength laser is not as readily absorbed in silicon. However, since the pulse duration is so short, a large amount of energy imparted in such a brief time causes ablation. The resulting morphologies and I-V measurements indicated that the 1064 nm laser has a wide range of pulse energies at which it can potentially create LDEs for a solar cell.

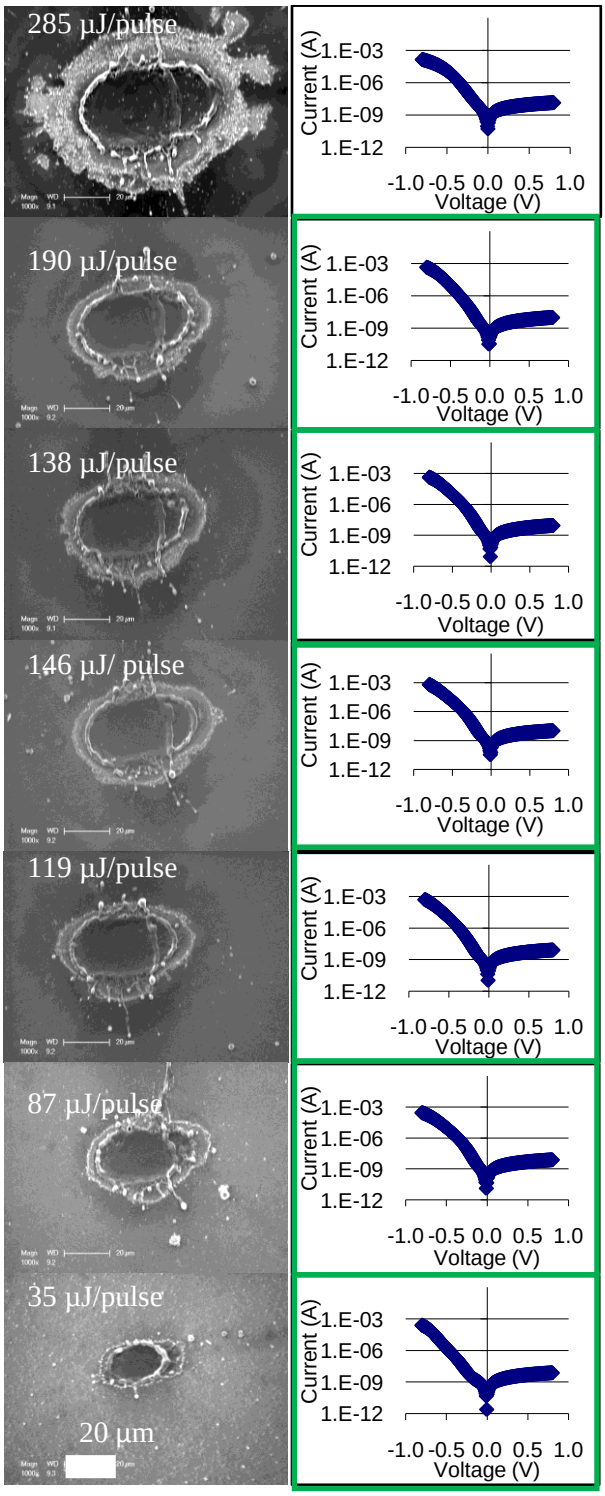


Figure 3-19: SEM images and I-V measurements of LDEs on a-Si:H/n+ a-Si:H sample, 1064 nm laser.

Images and I-V curves for the a-Si:H/n+ a-Si:H/SiO_x sample are shown in Figure 3-20. The leakage current is reduced in these LDEs due to the SiO_x layer, and in several cases forward bias current is reduced as well and series resistance dominates the measurement. There are a few conditions that hold promise for manufacturing LDEs in cells, and they will be investigated further in the next section. Notably those processing conditions of interest are the lower energy pulses.

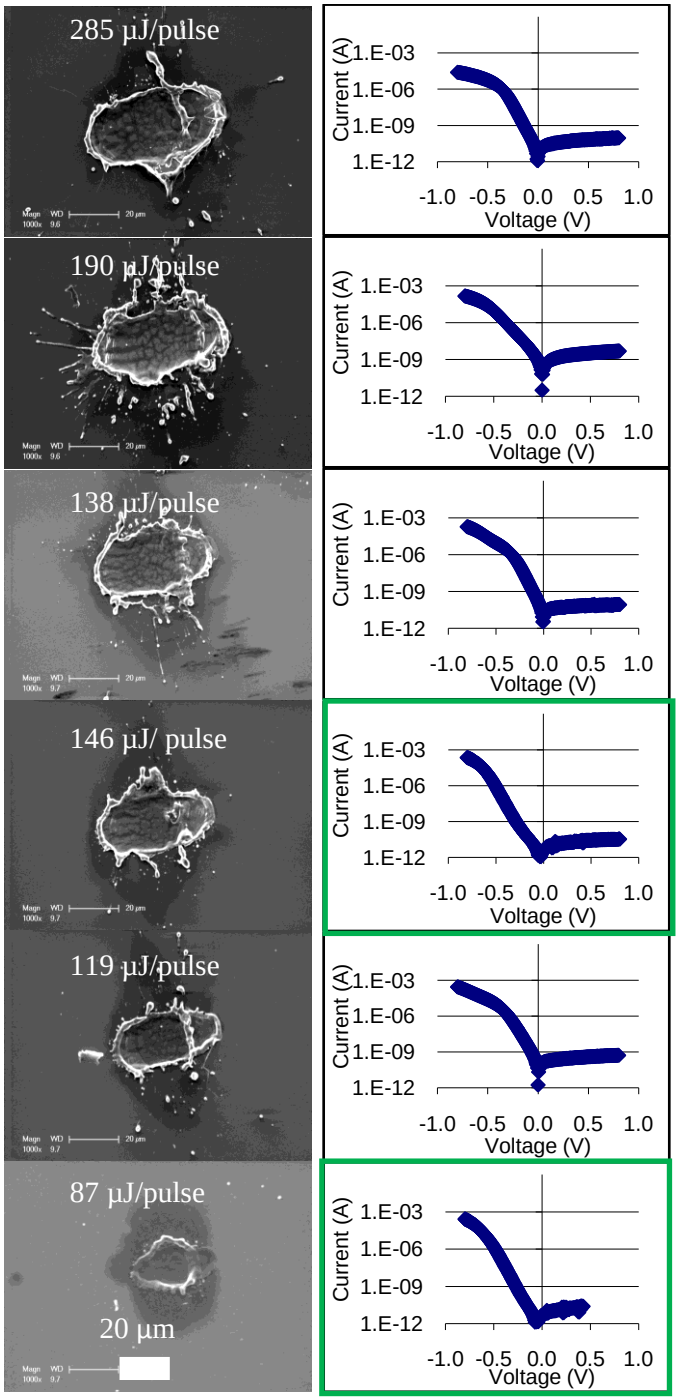


Figure 3-20: SEM images and I-V measurements of LDEs on a-Si:H/n+ a-Si:H/SiO_x sample, 1064 nm laser.

Curve Comparison

Further comparison of the specific I-V curves selected earlier provided insight into suitable LDE laser processing conditions. I-V measurements do not give a comprehensive picture of device performance and only with the evaluation of parameters in a diagnostic cell can we fully evaluate all the factors that contribute to performance in a cell. While the I-V measurements may not be characteristic of each LDE created with certain laser processing conditions, in our preliminary investigation it is useful to compare the I-V measurements and determine the laser processing conditions that yielded LDEs with the best diode characteristics.

Comparing the previously selected curves together, only those with the best "turn on" characteristics were selected for further examination. As shown in Table 3-2, the 1070 nm and 1064 nm lasers were useful in the formation of a majority of these LDEs. Those selected are shown in an I-V plot, and additionally shown on a log(I)-V plot in Figure 3-21. Markers have been added to indicate slopes with ideality factors equal to 1 and 2 on the log(I)-V plot.

Featuring low series resistance and leakage currents on the order of $1x10^{-8}$A, the a-Si:H/n+a-Si:H structure yielded LDEs for a majority of the laser processing conditions to which it was exposed. The LDEs formed on the a-Si:H/SiO_x passivation structure were formed with fewer processing conditions; however, those that were fabricated had the lowest leakage currents observed, on the order of $1x10^{-11}$ A. LDEs were more difficult to fabricate on the a-Si:H/n+aSi:H/SiO_x sample as compared to the a-Si:H/n+a-Si:H sample because of the laser interaction with the robust SiO_x layer in the former.

Table 3-2: LDE parameters plotted in Figure 3-21.

Laser	LDE Parameter	Passivation	Fluence
1064 nm	35 µJ/pulse	a-Si:H	11.1 J/ cm^2
1064 nm	119 µJ/pulse	a-Si:H	37.9 J/ cm^2
1064 nm	146 µJ/pulse	a-Si:H	46.5 J/ cm^2
1064 nm	190 µJ/pulse	a-Si:H	60.5 J/ cm^2
1070 nm	100 W, 250 µs	a-Si:H	31.8kJ/ cm^2
1070 nm	77 W, 250 µs	a-Si:H	24.3 kJ/ cm^2
1070 nm	67 W, 300µs	a-Si:H	25.6 kJ/ cm^2
1070 nm	100 W, 100 µs	a-Si:H/SiO_x	12.7 kJ/ cm^2
355 nm	124.3 µJ/pulse (3 pulses)	a-Si:H	57.7 J/ cm^2
355 nm	124.3 µJ/pulse (2 pulses)	a-Si:H	35.16 J/cm^2

Note: a-Si:H represents 10 nm a-Si:H/ 100 nm n+ a-Si:H passivation and a-Si:H/SiO_x represents 10 nm a-Si:H/ 20 nm n+ a-Si:H/ 100 nm SiO_x passivation

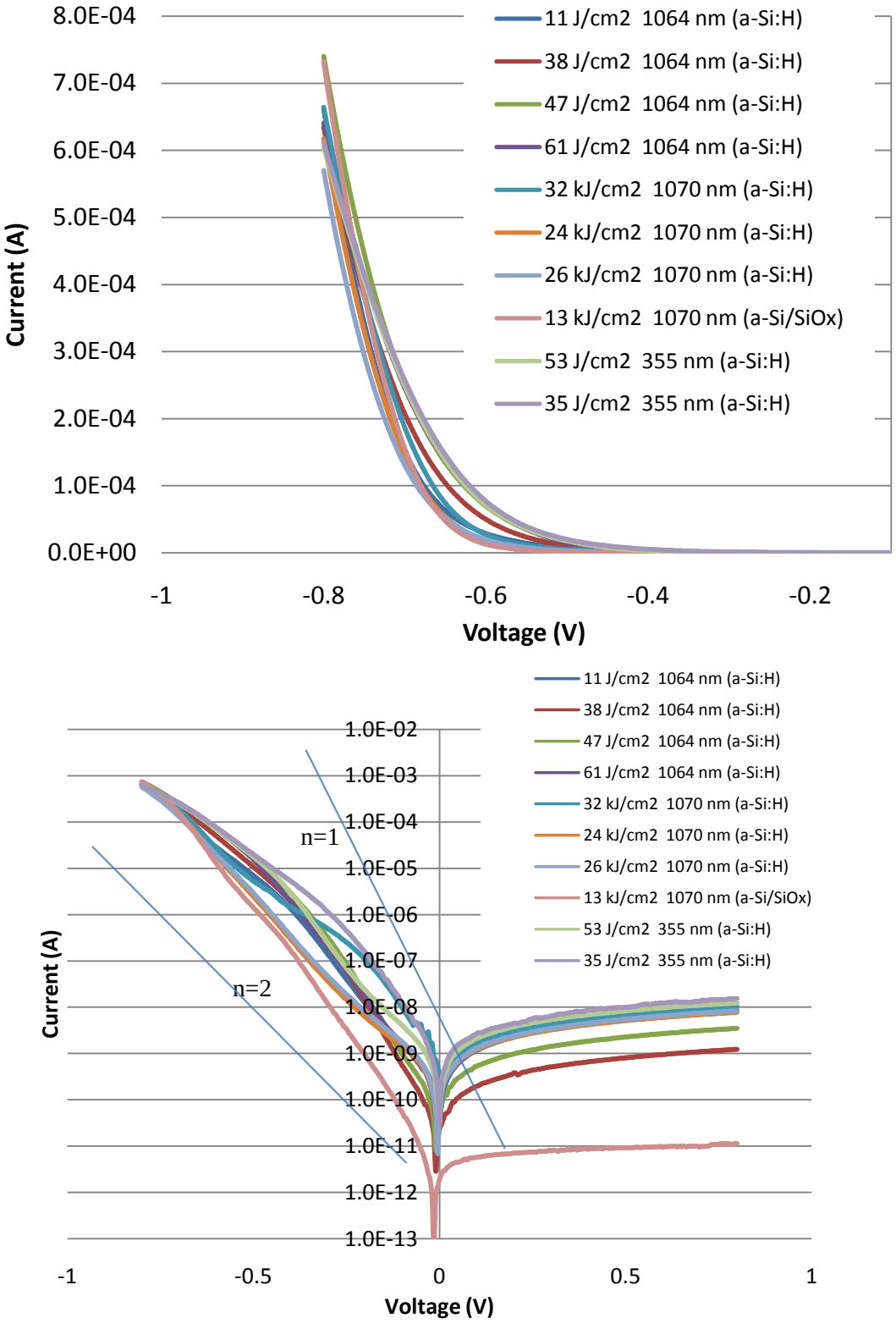


Figure 3-21: I-V and log(I)-V plots of the best diode characteristics.

Examining the curves in Figure 3-21, the LDE processed at 47 J/cm^2 on the a-Si:H passivation layer with 1064 nm laser, and the LDE processed at 13 kJ/cm^2 on the dual stack passivation layer with the 1070 nm laser, achieved the largest currents at forward bias. Looking at the log (I)-V plot it appears that the series resistance of each of the LDEs selected is approximately the same; however, the ideality factors and saturation and leakage currents vary greatly. Most of the LDEs have ideality factors (η_{qnr}) somewhere between 1 and 2.

Given the wide range of fluences used across each laser to produce functional LDEs one would not expect each LDE's I-V characteristics to be similar. To more closely evaluate the diode characteristics of each, fitting of the measured I-V curves was performed by manipulating values for $I_{o,scr}$, $I_{o,qnr}$, n_{scr}, n_{qnr} and r_s in Equation 1, the equation for current in a diode.

The majority of the I-V curves on the log(I)-V plot are very dissimilar, due to varying fluences, pulse durations, and wavelengths used to create them. Two particular LDEs formed with 1070 nm laser feature similar fluences and are of interest to compare. Both LDEs were created with fluences of ~25kJ/cm^2 on the a-Si:H/n+a-Si:H passivation structure. Shown in Figure 3-22, the I-V measurements of the LDEs, processed at 77 W and 250 µs and 67 W and 300 µs are very similar. The LDE processed with 77 W and 250 µs had a leakage of 8.2x10^{-8} A, a saturation current of 3.0x10^{-11} A, a series resistance of 90 Ω, and an ideality factor of 1.6. The LDE processed with 67 W and 300µs had a leakage of 8.2x10^{-8} A, a saturation current of 7.0x10^{-11} A, a series resistance of 100 Ω, and an ideality factor of 1.7.

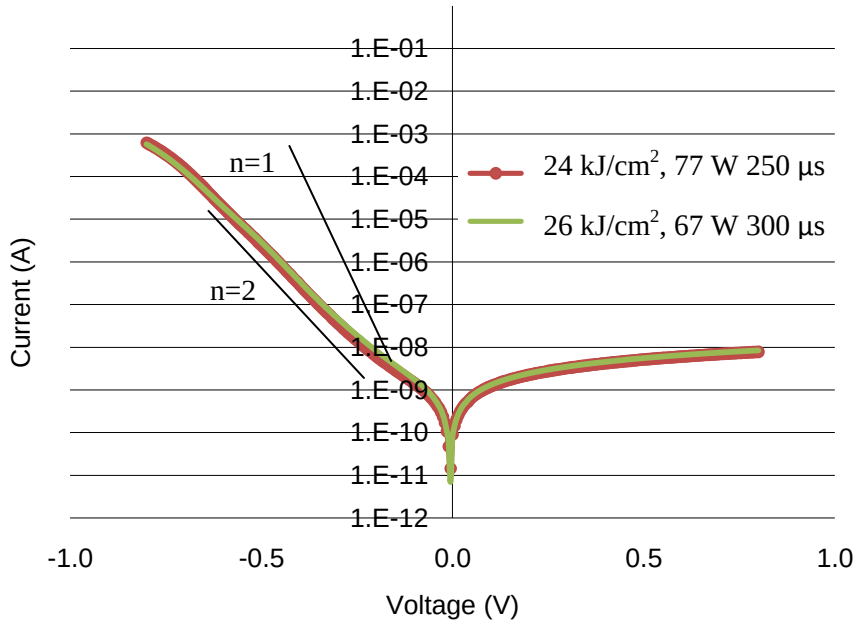


Figure 3-22: Curves for similar LDEs.

One curve in particular, measured for the LDE processed with the 1070 nm laser at 100 W and 100 µs on the P doped a-Si:H/n+ a-Si:H/SiO_x structure, showed the best I-V characteristics. It exhibited a very low leakage current of $1.1x10^{-11}$ A, a saturation current of $6x10^{-13}$ A, a series resistance of 100 Ω, and an ideality factor of 1.3 (the closest to 1 out of all measurements). Given that the diameter of the LDE is approximately 20 µm, the leakage current density is approximately $3.5x10^{-6}$ A/cm^2. The saturation current density is approximately $2x10^{-7}$ A/cm^2 (or approximately $4x10^{-8}$ A/cm^2 considering the junction area revealed in cross section). This value is large compared to reports of $8.5x10^{-13}$ A/cm^2 for laser chemically processed emitters (11) and $8.8x10^{-14}$ A/cm^2, which is the lowest theoretical saturation current density for an LDE (6). The fluence calculated for the creation of this LDE was 12.7 kJ/cm^2, again a large value compared to those reported in literature (0.5-1.5 J/cm^2).

From these evaluations the emitters fabricated are not of a quality that would lend them to use in solar cell manufacturing. While we were able to demonstrate laser doping, the

saturation ($2x10^{-7}$ A/cm^2) and leakage currents ($3.5x10^{-6}$ A/cm^2) of our LDEs were much higher than those in the literature (11).

Future experiments will seek to further understand the formation of laser doped emitters and the critical aspects of their laser processing. One place to start is with the reduction of laser fluences used in LDE formation. Compared to those reported in the literature the values utilized herein are exceedingly large. The thickness of the passivation/dopant structures necessitated the large energies that we used, and in the future passivation and doping layers that are better suited to gentler laser fluences must be fabricated. Thinner layers should make the use of less energy possible. Once appropriate passivation/dopant structures are developed, in conjunction with milder laser processing parameters, better quality LDEs should be attainable. Processing improvements will lead to reduced laser damage and carrier recombination, easily observed in I-V measurements by lower saturation currents, minimal leakage current, and ideality factors closer to 1. In the future, diagnostic cells will also be used to understand the impact of emitter performance on the overall cell. Of the lasers examined, the 1070 nm and 1064 nm lasers were used with numerous processing conditions to create LDEs. The 355 nm laser exhibited ablation when forming LDEs and may not be suitable for further investigation if thinner dopant/passivation structures are used.

Metallization

In an attempt to conclusively measure I-V curves for each LDE without uncertainty in the measurements, metallization of the contacts became an additional area of experimentation. Due to the large radius of the probe tip in comparison to the LDE diameter, and the surface topography of each laser processed region, exact placement of the probe on a specific area of the LDE was very difficult, as pictured in Figure 3-23. Metalizing the LDE sample would allow for

uniform contact to the device with only a minimal addition of contact resistance, assuming an ohmic metal contact could be made to the top surface of the rectifying LDE.

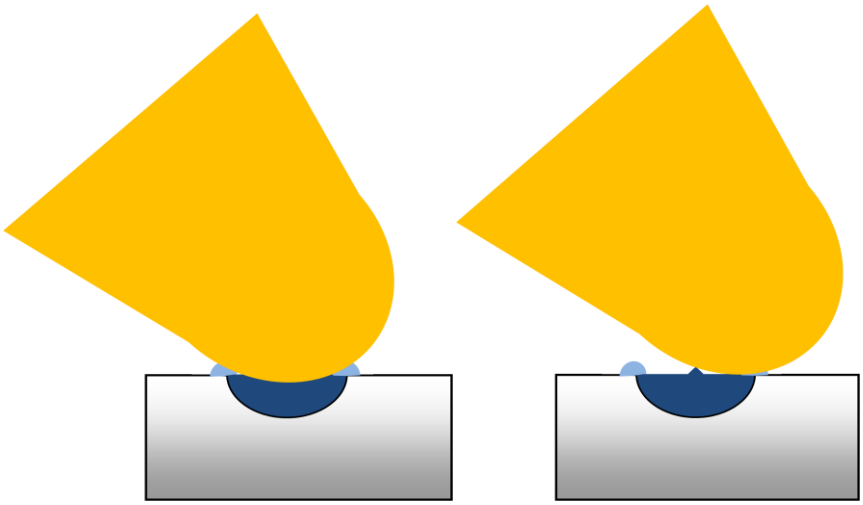


Figure 3-23: Possible locations of probe tip contacting the LDE when taking I-V measurements.

When considering the passivation structures in our experiments it is important to note that depositing metal onto an a-Si:H film would effectively short out measurement of the LDE. It is critical that there be an insulating layer between the metal film and the underlying passivation stacks so that only the I-V characteristics of the LDE are measured. On samples with the SiO_x overlayer contact would be made only to the LDE. Figure 3-24 highlights the problem for the case the case of nickel deposition and silicide formation.

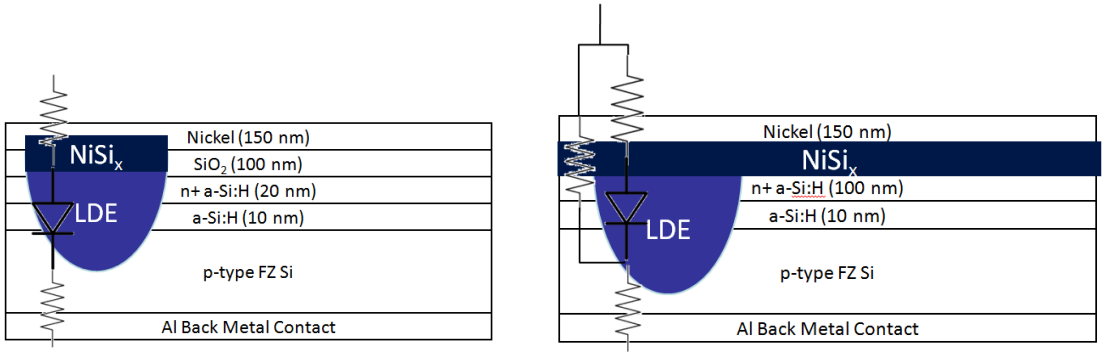


Figure 3-24: Importance of a SiO_x barrier layer for selective metallization of LDEs.

Blanket metallization poses an additional problem in that each LDE will be contacted and any measurements would represent the current contributions of all of the LDEs rather than just one. Selective or patterned metallization would be required to measure accurately the I-V characteristics of only one LDE, ensuring that only the laser doped region was metallized.

The first approach taken to metallize the samples was to pattern and e-beam deposit nickel over each pad, understanding that e-beam deposition would contact all the LDEs in each array and I-V measurements would include their contributions. Only samples with a SiO_x layer were used to ensure contact to only the LDEs. Prior to deposition the samples were etched in a dilute solution of 50:50 DI water to buffered oxide etch (1:10 BOE). Etching was very brief (3 to 6 s) to ensure that the passivation oxide was not removed entirely. Nickel was deposited to a thickness of 150 nm in an Axxis e-beam deposition system. Liftoff was performed using Microchem Remover PG and samples were then annealed at 450°C in an RTA for 15 min in an attempt to form NiSi.

After annealing it became apparent that tensile stresses existed in the deposited Ni film. Shown in Figure 3-25, cracking and peeling of the film occurred on several of the metallized pads. E-beam deposition has been known to introduce stresses in metal films as they are deposited, but another likely cause of the stress was the excessive thickness of the metal layer, 150 nm. In the future, sputter deposition would allow for control of stresses in the metal film through the manipulation of chamber pressure, and a thinner film may be used. Lessons from this first metallization attempt gave insight into what needs to occur in future work.

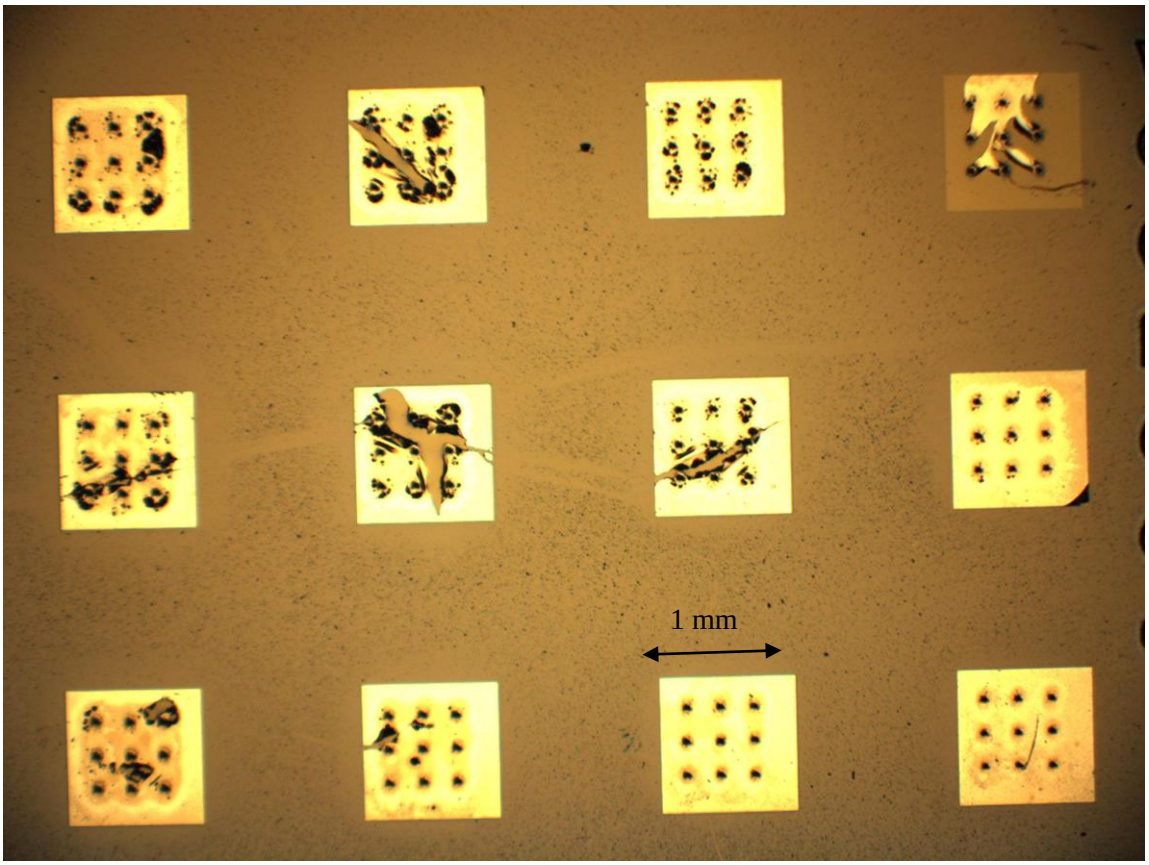


Figure 3-25: Tensile stresses evidenced in Ni films by peeling.

I-V measurements were taken on the sample to study the changes in the curves due to blanket metallization. The probe tip was placed in various locations on the metal pad to ensure that probe location did not impact the current measurement. The probe was placed on the metal pad (offset from the LDE) and directly on a metallized LDE. The curves acquired in both sweeps were the same, indicating that metallization removed measurement variability due to probe placement. When comparing the I-V curves taken before on the bare LDE with those taken after metallization, it became clear that the magnitude of current measured had increased. The increase in current was expected since a single LDE was no longer being measured, but all nine. The current increase is not a sum of each diodes individual contribution and cannot be directly predicted; the most conductive diode will dominate the measurement with additional contribution

from the other LDEs. Figure 3-26 highlights the current increase in the post metallization measurement.

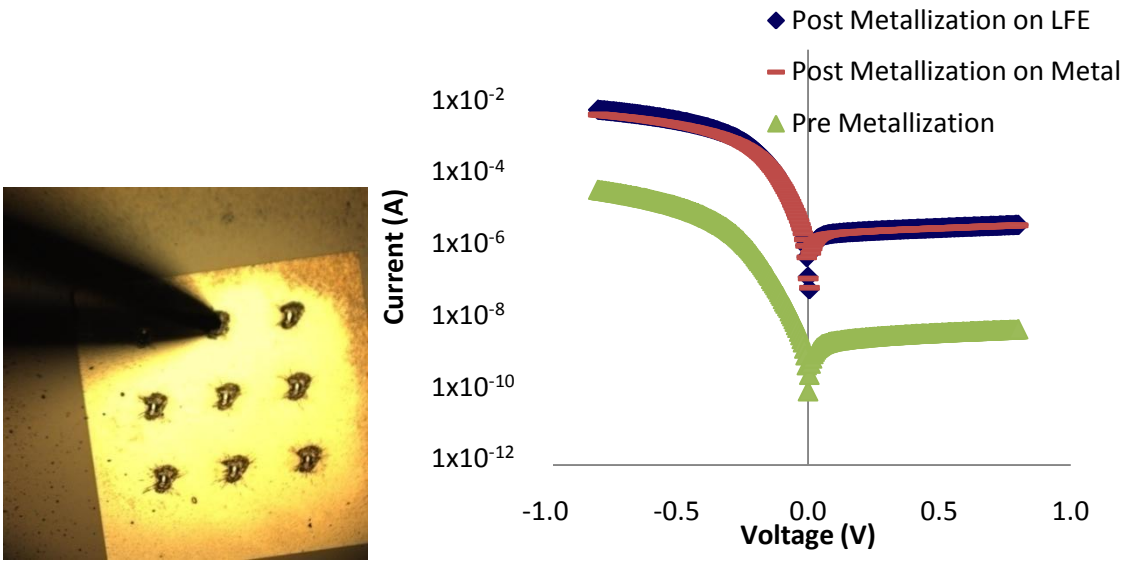


Figure 3-26: Pre and post metallization I-V measurements on a pad processed with the 355 nm laser (155 µJ).

Cross-sectioning and Junction Delineation

To determine LDE depth within the substrate cross-sectioning was employed. Dense arrays of LDEs were created with select processing conditions drawn from I-V measurement results. The process used herein was identical to the procedure used for LFC cross-sectioning and junction delineation, but the sample structure is different. The wafer substrate for these samples was p-type, so that laser doping of the n-type emitter would be highlighted. Plating should occur on the laser doped region rather than the substrate.

For the 1070 nm laser the first LDE sample analyzed was created with processing conditions of 100 W and 100µs on the a-Si:H/n+ a-Si:H substrate. The dense array prior to sample preparation and the subsequently polished and plated cross-section are shown in Figure 3-27.

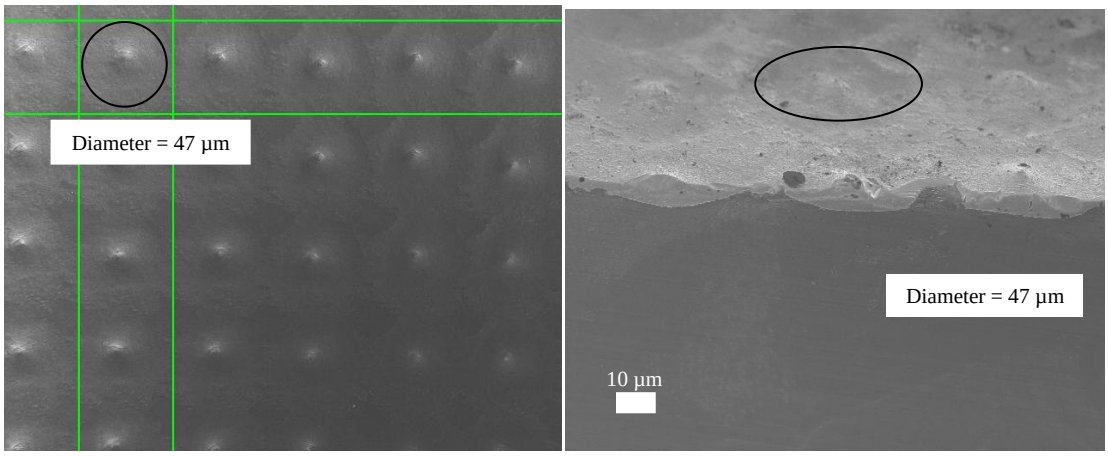


Figure 3-27: Dense array of LDEs processed at 100W and 100 µs on a-Si:H/n+ a-Si:H sample using a 1070 nm laser.

Initial assessment of the LDE cross-section shows that the doped emitters are much shallower than the LFCs fired with the 1070 nm laser, with depths of 11 µm. Pulse durations for the LDEs are much shorter than those used to fire LFCs, although the powers are comparable. The short duration of the laser pulse and the different wafer structure used to dope LDEs result in the large difference in geometry and aspect ratio. The approximate width of the LDEs processed at 100 W and 100 µs was 45 nm, and the approximate penetration depth was 11 nm.

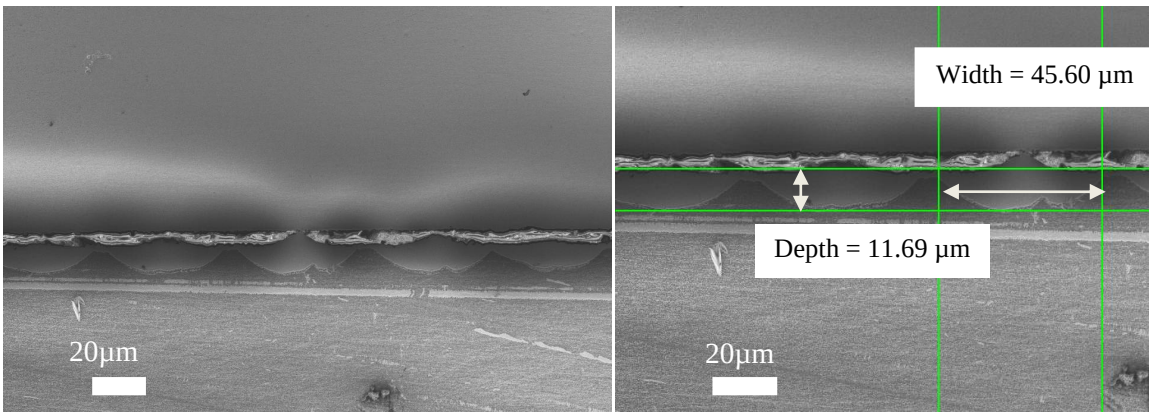


Figure 3-28: Cross-section of LDEs processed with a 1070 nm laser at 100 W and 100 µs.

Cross-sectioning was attempted on a sample processed with the 355 nm laser with 1 pulse at 124.3 µJ. The 355 nm wavelength of the laser is strongly absorbed in the very near surface of the sample; with only a 30 ns pulse duration there is not a deeply doped region apparent. From the cross-sectioning and plating of this sample it was confirmed that the doping occurs in only a very shallow region. Further samples with different processing conditions will be examined in future work. Images of the cross section attempt for the single 124.3 µJ pulse sample are show in Figure 3-29.

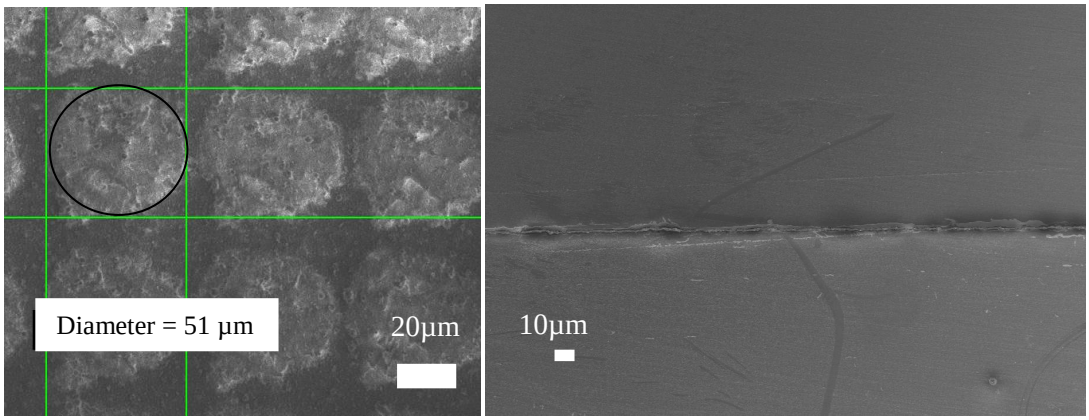


Figure 3-29: Cross-sectioned LDE sample processed with 1 pulse at 124.3 µJ/pulse with the 355 nm laser.

Results and Discussion

Through SEM investigation and I-V measurements it was quickly determined that the Sb dopant structure on both the a-Si:H and a-Si:H/SiO_x passivated samples was not a robust structure suitable for laser doping a selective emitter. Delamination and peeling of the e-beamed evaporated Si/Sb/Si structures occurred prior to laser firing, and when processed with each laser further delamination and volatilization occurred. Diodes were only formed on Sb samples processed with the 355 nm laser, but the I-V characteristics and excessive delamination apparent did not make them suitable for further investigation.

Diodes were formed, using each laser, on both of the P doped a-Si:H/n+ a-Si-H and a-Si:H/n+ a-Si:H/SiO_x passivated sample structures. LDEs processed with the 1070 nm and 1064 nm lasers exhibited the least ablation, whereas the 355 nm laser caused ablation across all the LDEs created with it. In I-V measurements it was clear for LDEs processed with the 355 nm laser on the a-Si:H/n+ a-Si:H/SiO_x passivated sample it was difficult to form diodes with low series resistance. Ablation of the thin dopant layer with the passivation stack likely led to less doping of the P within the substrate. LDEs processed with the 1070 nm, μs laser exhibited low series resistance, but were formed only when shot with the highest powers and longest durations. At lower power and pulse duration no change to the substrate was apparent. Leakage currents of LDEs created with the 1070 nm laser were lower on the a-Si:H/n+ a-Si:H/SiO_x passivated sample than those created on the a-Si:H/n+ a-Si-H passivated sample. The insulating SiO_x layer limits current transport to only the LDE and any parallel paths that would be possible through the a-Si:H/n+ a-Si-H layer are blocked. LDEs doped using the 1064 nm laser showed similar I-V characteristics to those doped with the 1070 nm laser but exhibited larger diameters and some ablation. Leakage currents were lower on the a-Si:H/n+ a-Si:H/SiO_x passivated sample than those created on the a-Si:H/n+ a-Si-H passivated sample, and also the LDEs created on the Si:H/SiO_x passivated sample were slightly smaller and showed less ablation splatter. The fluences used to fabricate LDEs were much larger than those in the literature; values of 10s of J/cm^2 were reached for the 1064 nm and 355 nm lasers, and values of 10s of kJ/cm^2 were reached for the 1070 nm laser (under 1.0 J/cm^2 used in (11)). Only because of the robustness of the passivation and dopant stack layers were such large values required. A much thinner structure would require lower fluences.

The leakage and saturation current of those LDEs selected for further investigation were much higher than those reported in the literature. Ideality values ranged between 1 and 2, with the best estimated to be 1.3 for the LDE doped with the 1070 nm laser with 100 W and 100 μs on

the P doped a-Si:H/n+ a-Si:H/SiO_x structure. The leakage current of that sample was of $1.1x10^{-11}$ A, and the saturation current was of $6x10^{-13}$ A. The resulting saturation current density was approximately $2x10^{-7}$ A/cm^2 (or approximately $4x10^{-8}$ A/cm^2 considering the junction area revealed in cross section). Series resistance in most of the select LDEs was less than 200 Ω.

E-beam deposition of Ni to form nickel silicide was possible, but several difficulties were encountered during processing. Blanket metallization eliminated the ability to selectively measure just one LDE. Additionally, e-beam evaporation of Ni to the thickness of 150 nm caused excessive stress in the films, and upon annealing they peeled and delaminated due to the tensile forces within them. It was clear that a thin oxide barrier layer would be necessary to metallize the samples to ensure measurement of only the LDEs and eliminate other possible current paths. Future work will include sputter deposition of a thinner Ni film onto a passivation structure capped with a SiO_x film.

Cross-sectioning and junction delineation was again used to identify the regions where doping had occurred beneath the laser processed regions. The n-type doped regions were selectively plated and dimensions of the depth and width of the LDEs were obtained. For those LDEs processed at 100 W and 100 μs with the 1070 nm laser, their penetration depth was ~11 nm and their width was ~45 nm. The sample cross-sectioned for the 355 nm laser showed some plated regions; however, they were not definitive enough to determine the maximum width or depth. Additional samples will be cross-sectioned in the future to better correlate dopant depth and penetration to laser processing parameters.

In summary, LDEs have been fabricated, and a particular dopant and passivation structure was identified for future experimentation. LDEs were created on the P doped n+ a-Si:H samples with each laser, while the Sb doped samples were not resilient enough to withstand laser firing with the longer wavelength lasers and LDEs were not measureable. It should be possible to fabricate LDEs suitable for a solar cell with further refinement of processing parameters and

passivation layer thicknesses. Evaluation of diagnostic cells will also be possible with the development of a more robust metallization technique.

Chapter 4

Passivation

Literature Review

Recent investigations into surface passivation have highlighted aluminum oxide (Al_2O_3) as a promising alternative to conventional passivation layers used in solar cell manufacturing. Unlike hydrogenated amorphous silicon (a-Si:H), silicon nitride (SiN_x) and silicon oxide (SiO_2 or SiO_x) layers, which create surface passivation through the reduction of dangling bonds, Al_2O_3 and similar metal oxides afford fixed charge passivation, which reduces recombination at the surface through field effects. On an n-type wafer, sufficient negative fixed charge creates an inversion layer and shields majority carriers from the surface; on a p-type wafer negative fixed charge creates an accumulation layer and shields minority carriers from the surface, thus preventing their recombination at surface states (18). Fixed charge passivation is very robust both thermally and under light soak, making it advantageous over passivation achieved with a-Si:H layers, which degrade over time due to the loss of hydrogen in the film at moderate temperatures (greater than ~150°C) (52) (53). Rather than a physical means of dangling bond passivation to reduce surface recombination, Al_2O_3 provides field effect passivation to force electrons away from the surface and prevent recombination.

Hydrogenated amorphous silicon and SiO_x layers are commonly deposited using PECVD and can be deposited quickly on large areas. Hydrogenated amorphous silicon can be grown at low temperatures, around 150°C, and can provide passivation with a low surface recombination velocity on the order of 10 cm/s (53). Unfortunately, the passivation provided by the film degrades when exposed to higher temperatures and over time, due to loss of hydrogen from the

film (53). Thermally growing silicon oxide, SiO_2, provides a more robust, chemically inert passivation, which can result in long effective carrier lifetimes, in the ms range, and low SRVs, from 1 to 40 cm/s depending on the wafer type (54). Thermal oxidation, however, requires exposing silicon to high temperatures around 1000°C (19) (54). Aluminum oxide and hafnium oxide (HfO_2), investigated herein for fixed charge passivation, are typically deposited using atomic layer deposition (ALD) at low temperatures in the range of 100 to 200°C (19). Record SRVs achieved for Al_2O_3 have been as low as 3 cm/s (15).

Atomic layer deposition relies on specific gaseous precursors, which complete self-limiting reactions, to form the desired metal oxide (55). The precursors are introduced in alternating pulses into a low pressure reaction chamber to grow one layer of the reaction product at a time; one pulse of each precursor completes one cycle. For the growth of Al_2O_3, typical precursors are trimethylaluminum ($Al(CH_3)_3$) and water vapor (H_2O) (55). Oxygen plasma in plasma assisted ALD, or ozone, can also be used with $Al(CH_3)_3$ (18) (19) (20). The reactions that take place during each pulse are as shown below (55). Hydrogen terminated bonds at the silicon surface are required to start the reaction, which then proceeds one layer at a time with each cycle.

$$Si\text{-}O\text{-}H_{(s)} + Al(CH_3)_{3(g)} \rightarrow :Si\text{-}O\text{-}Al(CH_3)_{2(s)} + CH_{4(g)}$$

$$:Si\text{-}O\text{-}Al(CH_3)_{2(s)} + 2\ H_2O_{(g)} \rightarrow :Si\text{-}O\text{-}Al(OH)_{2(s)} + 2\ CH_{4(g)}$$

Several groups have demonstrated excellent passivation of silicon using ALD Al_2O_3 and stacked structures of Al_2O_3 and another dielectric. Schmidt et al. investigated both Al_2O_3 and Al_2O_3/SiO_x passivation layers for rear side passivation of a p-type PERC cell (19). Efficiencies of 20.0% and 20.6% were confirmed for 130 nm ALD Al_2O_3 and 30 nm ALD Al_2O_3/200 nm PECVD SiO_x rear passivation stacks, respectively. The rear side contacts were made through standard photolithographic patterning and etching steps. After contact formation the entire cell was subjected to a 10 min 500°C front oxidation step and a final 1 min 300°C anneal (19). Surface recombination velocities of 90 ± 20 cm/s and 70 ± 20 cm/s were measured for the 130 nm

alumina layer and the 30 nm Al_2O_3/200 nm SiO_x layers, respectively (19). Benick et al. fabricated n-type PERL solar cells with efficiencies of 22.5±0.7% using Al_2O_3 for front surface passivation of the highly doped p-type emitter (56). A 30 nm Al_2O_3 front surface passivation layer was deposited by plasma-assisted ALD followed by plasma-assisted CVD of a 40 nm SiN_x ARC. The best efficiency achieved was 23.2% (56). Suwito et al. fabricated a similar PERL-like cell, with a 10nm Al_2O_3 front side passivation layer and SiN_x anti-reflection coating, and achieved an efficiency of 22.4% (16).

Saint-Cast et al. demonstrated solar cells with efficiencies ranging from 21.2 to 21.5% passivated with both Al_2O_3 and Al_2O_3/SiO_x layers. Al_2O_3 layers were depositing using both ALD and PECVD (20). Stacked passivation layers studied included 7 nm ALD Al_2O_3/90 nm PECVD SiO_x, 20 nm ALD Al_2O_3/80 nm PECVD SiO_x, and 30 nm PECVD AlO_x/70 nm PECVD SiO_x; however, a sample passivated with 100 nm PECVD AlO_x cell exhibited the highest efficiency of 21.5% and lowest SRV of 8 cm/s. Across the different passivation structures, surface recombination velocities ranged from approximately 8 to 108 cm/s. From their findings the authors concluded that Al_2O_3 passivation layers were comparable to a-Si:H and SiO_2 for solar cell passivation, becoming the third suitable material for use in manufacturing (20).

Hoex et al., in a study on Al_2O_3 passivation of p-type silicon, attributed the excellent passivation of Al_2O_3 to a large negative fixed charge density that repelled minority carriers (electrons in a p-type material) away from the surface, thereby reducing the recombination rate of carriers at the surface (18). They claimed a fixed charge density of $-1x10^{13}$ q/cm^2 in a 30 nm Al_2O_3 plasma-ALD film after a 30 min 425°C anneal in a N_2 ambient. The SRVs reported were measured for Al_2O_3 passivated samples, in comparison with samples passivated with SiO_2, a-Si:H and a-SiN_x:H films. Surface recombination velocities were calculated based on the effective carrier and bulk carrier lifetimes of each sample, and were reported to be in the range of ~100-200 cm/s for the Al_2O_3 films (18). In other work by Hoex et al. SRVs of 2 cm/s and 13 cm/s were

obtained on n- and p-type silicon wafers passivated with 7 to 30 nm Al_2O_3 films, annealed at 425°C in a N_2 ambient in a rapid thermal annealing (RTA) furnace (15). Even layers as thin as 7 nm were reported to exhibit SRVs as low as 5 cm/s on n-type silicon. Effective carrier lifetimes as high as 1.2 ms were measured on p-type silicon passivated with 30 nm Al_2O_3, and a maximum lifetime of 6.6 ms was measured on n-type silicon passivated with 26 nm Al_2O_3, although negative fixed charge is not the mechanism by which n-type silicon is passivated, as it would create an inversion layer. Hoex et al. claimed that such values were comparable to the longest lifetimes obtained for "alnealed" SiO_2, a-SiN_x:H, as well as a-Si:H films typically used in solar cell passivation (15). ("Alnealing" involves annealing a passivation layer after having deposited an Al film on top prior to heat treatment. After the annealed Al film is removed, there is a noted improvement of the passivation quality of the silicon derivative films (19).) Hoex et al. attribute the high lifetimes and low SRVs obtained with the Al_2O_3 passivation films to a built-in, negative, fixed charge density of ~10^{13} cm^{-2}, responsible for inducing field effect passivation in the p-type samples (15). The large negative fixed charge density was calculated from flat band voltage shifts seen in C-V measurements, which they did not report.

Benick et al. examined the thermal stability of Al_2O_3 on p-type silicon. Two sets of samples were passivated with 27 nm of plasma-assisted ALD Al_2O_3 on 0.1, 0.5, and 1.0 Ω-cm FZ p-type silicon. One set was deposited at 170°C, and the other at 230°C. After deposition, individual samples were cleaved in order to receive different annealing treatments. Anneals were performed in forming gas at either 440°C or 500°C (52). A maximum lifetime of 3.3 ms was achieved on the 1.0 Ω-cm sample annealed at 440°C in forming gas. Samples were additionally subjected to temperatures up to 850°C for 3 seconds, and while some degradation occurred, passivation quality was still high (52). In an additional study by Schmidt et al., thinner Al_2O_3 layers were studied for passivation integrity and robustness when subjected to high temperatures (57). After annealing at 425°C in for 15 min, they measured a lifetime of 550 μs (22 cm/s) for a

3.6 nm film, and a lifetime of 1 ms for a 20 nm film on a 1.5 Ω-cm wafer. Similarly, they achieved lifetimes of 8 ms (1.8 cm/s) for a 3.6 nm film, and 10 ms (1.4 cm/s) for a 20 nm film on 200 Ω-cm wafers. However, after firing at 830°C the passivation degraded, and in the case of the ultra thin 3.6 nm Al_2O_3 layer the lifetime was reduced to 50 µs. Thermal stability of thin Al_2O_3 passivation layers was improved with the deposition of a PECVD SiN_x capping layer (57). The initial lifetime of a 3.6 nm Al_2O_3/75 nm SiN_x sample was 700 µs before firing and dropped less severely to 300 µs after firing. Maintaining passivation of the substrate after firing was attributed to the deposition of the SiN_x layer and the hydrogen it introduced. The authors claim that hydrogen present in the SiN_x provided passivation by diffusing to the Al_2O_3/Si interface where it satisfied dangling bonds.

Little investigation into HfO_2 as a passivation layer for silicon has been performed. One report by Wang et al. found that HfO_2 provided negative fixed charge passivation similar to Al_2O_3 (58). They deposited Al_2O_3 and HfO_2 films on two n-type silicon samples using ALD for 150 cycles at 200°C. No additional annealing was performed. By studying C-V characteristics and V_{FB} shifts they found negative fixed charge in the bulk of the films. They measured as deposited effective carrier lifetimes of 302 µs and 347 µs for the Al_2O_3 and HfO_2 passivated samples, using µ-PCD. The lifetime values correlated to maximum SRVs of 84.5 cm/s and 73.4 cm/s, respectively (58). Interestingly, they report that for each dielectric an increase in the film thickness leads to lower SRVs.

For use in solar cells, ALD and PECVD deposited Al_2O_3 hold much promise as a passivation layer that could surpass the long term integrity and robustness of a-Si:H and SiO_x films. Many groups have demonstrated its capabilities in test cells but little work has been done to understand in detail the fixed charge passivation and how to optimize it. An investigation of the factors that contribute to fixed charge passivation is performed herein to determine the best material systems and layers for cell passivation. Both Al_2O_3 and HfO_2 are considered. The work

herein attempts to determine the effect of film thickness, annealing treatments, fixed charge density, SiO_x capping layers, and multi-layers structures on passivation quality. Passivation was evaluated through effective carrier lifetime measurements, C-V measurements, fixed charge density calculations, and sheet resistance measurements. Single layer films of Al_2O_3 are studied in conjunction with Al_2O_3/SiO_x layered films to better understand the passivation mechanisms of each.

Passivation Experiments

A series of experiments were designed to study performance of Al_2O_3 and HfO_2 layers, Al_2O_3/SiO_x and HfO_2/SiO_x layers on the passivation of crystalline silicon wafers, and to investigate the potential of fixed charge passivation for use in high efficiency solar cells. On an n-type wafer, sufficient negative fixed charge creates an inversion layer thus shielding majority carriers from the surface; on a p-type wafer, negative fixed charge creates an accumulation layer thus shielding minority carriers from the surface. In either case, the presence of fixed charge in the passivation layer serves to shield one type of carrier from the surface of the silicon, thereby providing passivation and reducing surface recombination.

Figure 4-1: Cambridge Savannah^{TM} 200 ALD system and the AMAT P-5000 cluster tool.

Alumina (Al_2O_3) and hafnia (HfO_2) layers were deposited using atomic layer deposition (ALD) in a Cambridge Savannah™ 200 system shown in Figure 4-1. In later experiments SiO_x capping layers were deposited using an Applied Materials P-5000 four chamber cluster tool. While ALD has often been ignored as a large scale production tool, progress is being made to increase the rate and scale of ALD by developing a spatial technique to separate deposition steps (59). In conventional ALD the cycle time remains a limiting factor; however, thin films (< 10 nm) can be deposited rapidly, and would suffice as long as a thinner film is adequate for passivation. Additionally, passivation layers similar to those grown by ALD can be deposited in PECVD systems, and although we did not have the capability to compare PECVD and ALD films directly, other groups have found passivation quality of the films to be similar (20).

Three sets of experiments were performed. The first investigated the passivation of silicon by layers of Al_2O_3 and HfO_2 with increasing thicknesses from 4 nm to 35 nm, and is presented in the section "Film Thickness Experiment: Al_2O_3 and HfO_2 Layers". The second compared passivation by single Al_2O_3 layers to that of Al_2O_3 capped with SiO_x layers, and is presented in the section "Multi-Layer Passivation Experiment: Al_2O_3/SiO_x and HfO_2/SiO_x Layers". The third was an investigation into maximizing fixed charge density in Al_2O_3 and Al_2O_3/SiO_x layers with the goal of creating an induced inversion layer in a highly resistive test silicon substrate, and is presented in the section "Inversion Layer Experiment: Al_2O_3 and Al_2O_3/SiO_x Layers".

Film Thickness Experiment: Al_2O_3 and HfO_2 Layers

The first experiment carried out was designed to correlate the passivation of silicon by ALD films of Al_2O_3 and HfO_2 with different film thicknesses and annealing treatments. Effective carrier lifetime measurements and C-V measurements were used to evaluate the changes in surface passivation and determine the presence and quantity of fixed charge in the passivation layers. Two sets of samples were created, the first passivated with Al_2O_3 films with thicknesses of 8, 12, 20, and 35 nm, and the second passivated with HfO_2 films with thicknesses of 9, 13, 22, and 38 nm. The films were deposited in the Cambridge ALD tool at 200°C. For the deposition of Al_2O_3, the first precursor, water, was pulsed for 0.015 s followed by a wait time of 8 s, after which the trimethylaluminum precursor was pulsed for 0.015 s followed by an 8 s wait time. Deposition and run time details are given Tables 4-1 and 4-2 for each film deposited.

Table 4-1: Al_2O_3 deposition details.

Al_2O_3 Sample	Cycles	Film Thickness	Deposition Temperature	Deposition Time
A1	80	8 nm	200°C	22 min
A2	120	12 nm	200°C	33 min
A3	200	20 nm	200°C	54 min
A4	350	35 nm	200°C	98 min

Table 4-2: HfO_2 deposition details.

HfO_2 Sample	Cycles	Film Thickness	Deposition Temperature	Deposition Time
H1	80	9 nm	200°C	32 min
H2	120	13 nm	200°C	45 min
H3	200	22 nm	200°C	69 min
H4	350	38 nm	200°C	122 min

Thicker films take much longer to deposit given the increased number of cycles required. Despite any superior passivation quality potentially achieved with a 35 nm film, a deposition time of 98 min may not be realistic in a manufacturing setting. Other groups, however, have demonstrated high-efficiency solar cells passivated with similar thickness Al_2O_3 layers, warranting the comparison.

After deposition, two different annealing treatments were performed to improve the films and drive out organics or impurities. The first anneal was carried out at 250°C for 5 min on a Temptronic vacuum chuck, and the second at 350°C for 5 min on a Thermolyne hot plate, both shown in Figure 4-2. Annealing temperatures were confirmed with a thermocouple during heat treatment, and were performed in ambient air.

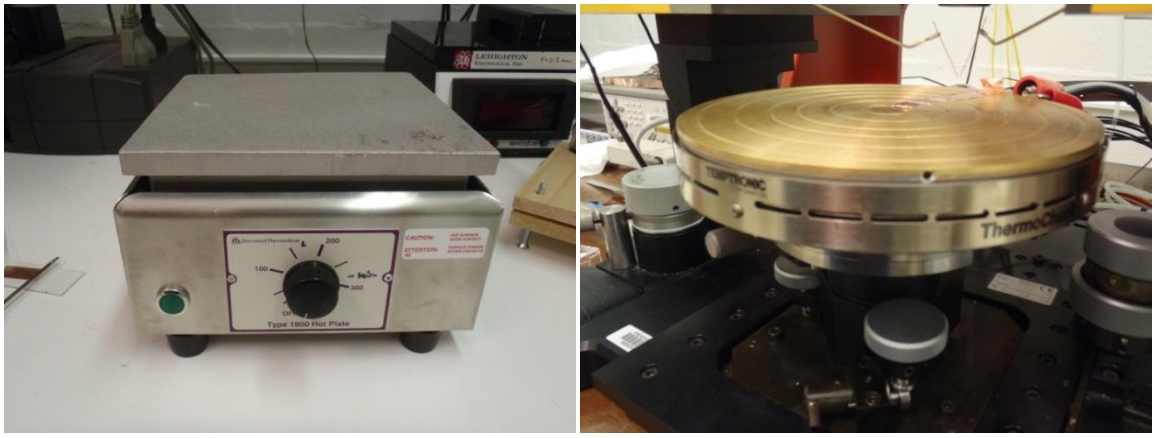


Figure 4-2: Barnstead Thermolyne hot plate and Temptronic ThermoChuck vacuum chuck.

Lifetime Measurements

Effective carrier lifetime was measured for each sample before and after annealing treatments to observe any change in minority carrier lifetime and determine any improvement in surface passivation. Measurements were performed using a microwave photoconductive decay (μ-PCD) tool built in house. A description of the measurement process can be found in Appendix

A. A microwave antenna was used to transmit microwaves to the sample and then measure the reflected microwave power from the sample, while the sample was illuminated on the opposite side with a UV LED. The UV wavelength excited carriers (electron-hole pairs) within the bulk of the silicon and near the surface. Once excited the carriers exist for a characteristic time before they recombine. That time is the effective carrier lifetime, and can be prolonged by adequate surface passivation. Longer effective carrier lifetimes indicate better passivation and reduced carrier recombination at the surface. The length of the carrier lifetime can be extrapolated from the decay of microwave power captured by the antenna, since photoconductivity and reflectivity are linked. An example of a reflected power curve measured on an annealed sample (P-A10S100-4_450a_RTA) and the μ-PCD set up used is shown in Figure 4-3.

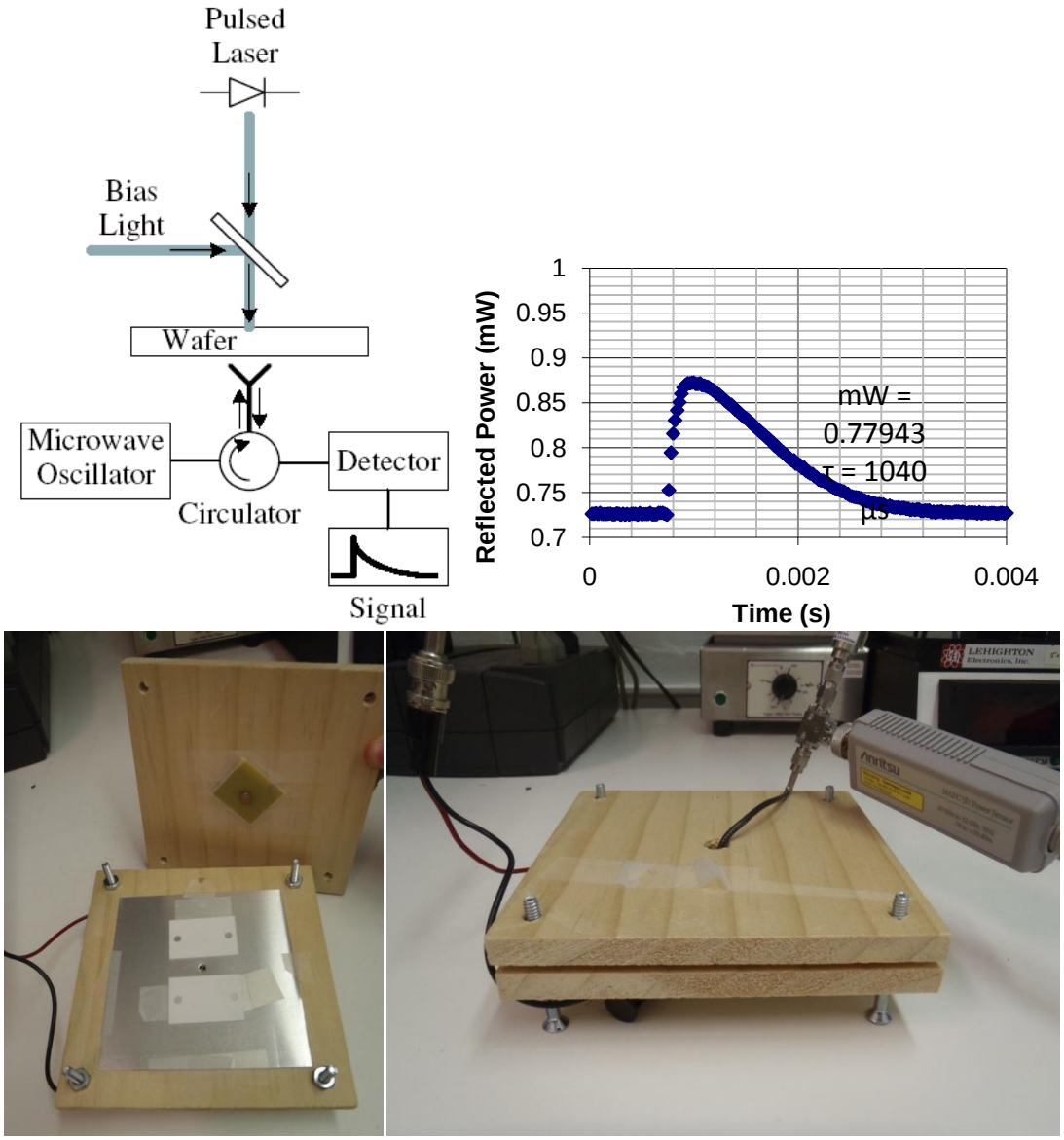


Figure 4-3: Microwave photoconductive decay, effective carrier lifetime measurement set up (50).

Average effective carrier lifetime values for the Al_2O_3 and HfO_2 passivated samples are shown in Table 4-3 and Table 4-4. Measurements were taken as deposited, after a 5 min 250°C anneal, and after a 5 min 350°C anneal.

Table 4-3: Effective carrier lifetime for Al_2O_3 passivated samples.

Al_2O_3 Sample	Film Thickness	As Deposited	Post 250°C	Post 350°C
A1	8 nm	370 µs	312 µs	1012 µs
A2	12 nm	420 µs	618 µs	1030 µs
A3	20 nm	510 µs	817 µs	1722 µs
A4	35 nm	594 µs	480 µs	440 µs

Table 4-4: Effective carrier lifetime for HfO_2 passivated samples.

HfO_2 Sample	Film Thickness	As Deposited	Post 250°C	Post 350°C
H1	9 nm	365 µs	765 µs	859 µs
H2	13 nm	356 µs	775 µs	1070 µs
H3	22 nm	480 µs	793 µs	760 µs
H4	38 nm	656 µs	1063 µs	296 µs

Effective carrier lifetimes for samples passivated with both the Al_2O_3 and HfO_2 films, as deposited, appear to increase with increasing film thickness. Certain samples exhibited a trend of increased effective carrier lifetime with increased annealing temperature, highlighted in Figure 4-4, particularly the 12 nm and 20 nm Al_2O_3 passivated samples, and the 9 nm and 13 nm HfO_2 passivated samples. The 5 min 350°C hot plate anneal was more effective than the 250°C vacuum chuck anneal for these samples, and this treatment sufficiently activated the fixed charge in the film leading to increased effective carrier lifetimes and reduced surface recombination. Samples passivated with the thinner films exhibited very long lifetimes, greater than 1 ms for the sample passivated with the thinnest 8 nm Al_2O_3 film, and up to 1.7 ms for the sample passivated with 20 nm Al_2O_3 sample. It is interesting to note, however, that samples passivated with the thickest Al_2O_3 and HfO_2 films did not improve with the 5 min 350°C anneal.

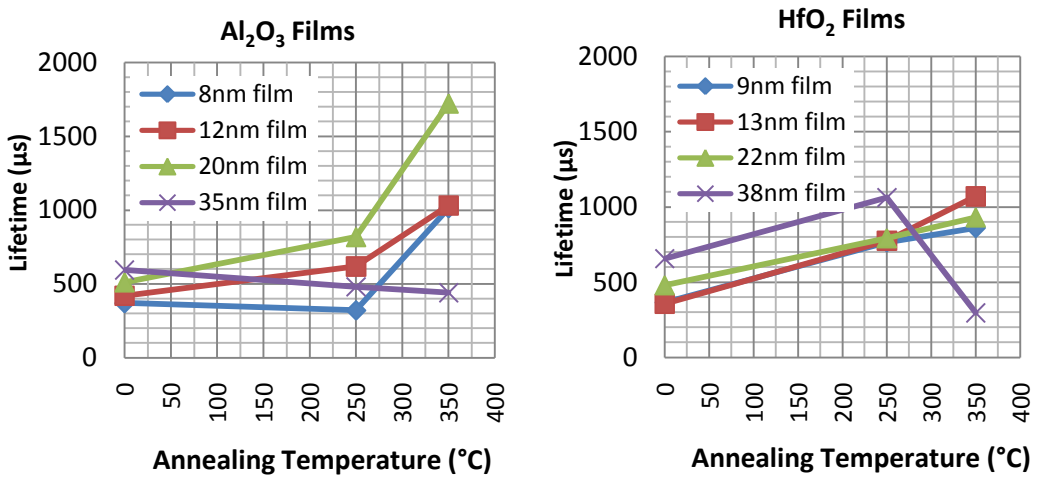


Figure 4-4: Effective carrier lifetime and annealing temperature.

C-V Measurements

Capacitance-voltage (C-V) measurements were performed to determine the fixed charge densities of the passivation films before and after each annealing treatment. A Leighton 2017B mercury probe, shown in Figure 4-5, was used with an Agilent 4284A LCR meter to measure capacitance while applying a DC voltage sweep and 1 MHz AC signal. Contact was made to the passivated surface of the wafer with the mercury probe, and voltage was applied with the LCR meter while capacitance was simultaneously measured.

Figure 4-5: Agilent4284A LCR meter Leighton 2017B mercury probe.

Two contacts, one small area and one large area, were made to the front side of the passivated silicon wafer. The smaller contact was used to make the capacitance measurement and had an area of approximately 0.002 cm^2. The fixed charge density, Q_f, can be determined from the difference in the flat band voltage (ΔV_{FB}) from one measurement to another according to Equation 4

$$Q_f = \frac{-C_{ox}(\Delta V_{FB} + \varphi_{MS})}{Aq}, \tag{4}$$

where C_{ox} is the capacitance of the oxide in accumulation, φ_{MS} is the metal-semiconductor work function, A is the contact area, and q is the charge on an electron. The metal-semiconductor work function difference is the main source of uncertainty in the calculation (50). For our purposes the value of φ_{MS} has been assumed to be +0.5 eV for a p-type silicon substrate, and −0.5 eV for an n-type silicon substrate. Shown in Figure 4-6, when φ_{MS} is assumed to be zero, the ideal C-V curve transitions from accumulation to depletion at V= 0 V.

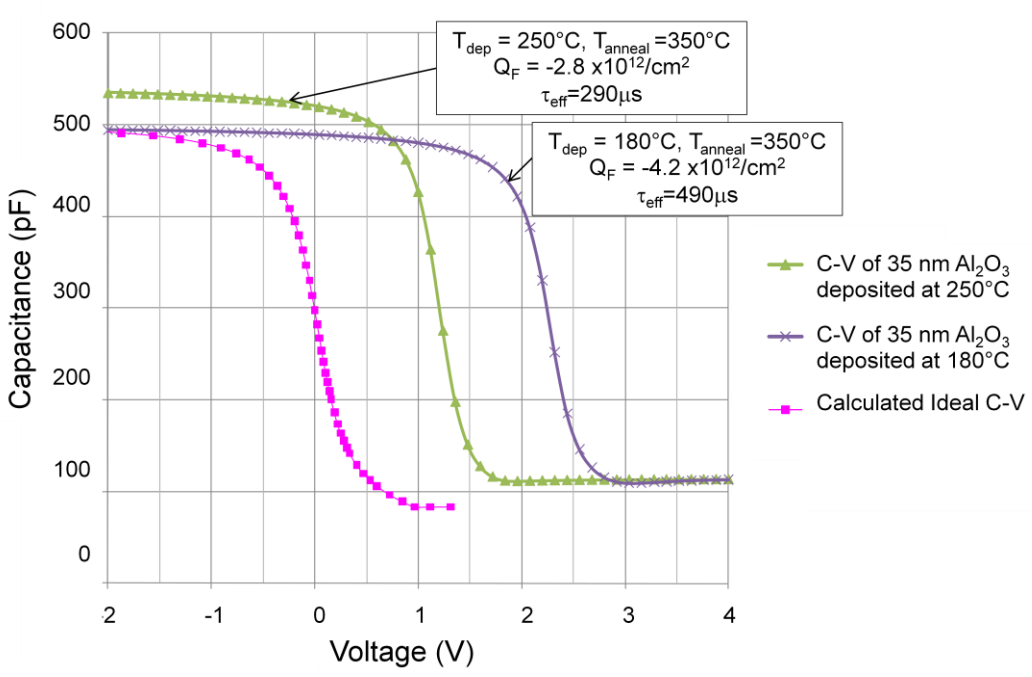


Figure 4-6: Shift in V_{FB} due to the metal-semiconductor work function difference and fixed charge in the film.

Further shift in V_{FB} can be attributed to fixed charge in the dielectric film near the dielectric/silicon interface, as shown by the additional curves for samples passivated with Al_2O_3 films. A V_{FB} shift to the left indicates positive fixed charge in the film, as a more negative voltage would be required to induce accumulation in the near surface of the substrate (for a p-type semiconductor) in the presence of positive charge. A V_{FB} shift to the right indicates negative fixed charge in the film, as a more positive voltage would be required to drive holes in the near surface of the substrate away from the negative fixed charge in the film and into depletion (for a p-type semiconductor).

In addition to fixed charge density, C-V measurements provide information about interface states in the film. A C-V curve appears stretched out if there is a large density of interface traps. The traps prolong the transition from accumulation to depletion, making the curve less abrupt. Annealing the passivation layer often heals traps or drives out the impurities that cause them, which leads to a lateral compression of the C-V curves.

Electrically active interfacial traps at the interface of the silicon and dielectric layer can also be detected in C-V measurements. These charges are apparent when comparing C-V curves taken with alternate polarity voltage sweeps, from positive bias to negative bias and from negative bias to positive bias. Due to their ability to charge and discharge based on the applied potential, the traps can shift V_{FB} depending on the direction of the voltage sweep. Figure 4-7 shows the hysteresis in the C-V curve caused by these interface trapped charges. With higher temperature annealing treatments these defects can often be mitigated, greatly reducing the hysteresis in the C-V curves.

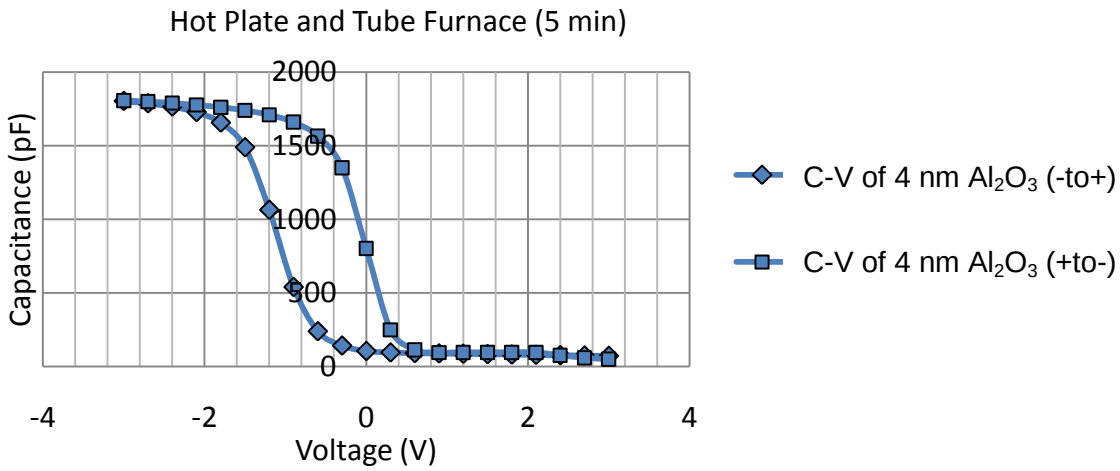


Figure 4-7: C-V measurement hysteresis.

The curves obtained with the mercury probe for the Al_2O_3 passivated samples are seen in Figure 4-8. C-V measurements were taken on each sample as deposited, after the 5 min 250°C anneal, and after a 5 min 350°C anneal. A large degree of hysteresis is evident in the C-V curves of the samples as deposited, but is reduced with the subsequent annealing treatments. Hysteresis is mitigated with the 250°C anneal and further with the 350°C anneal, indicating improvement, and giving evidence to the healing of interface traps.

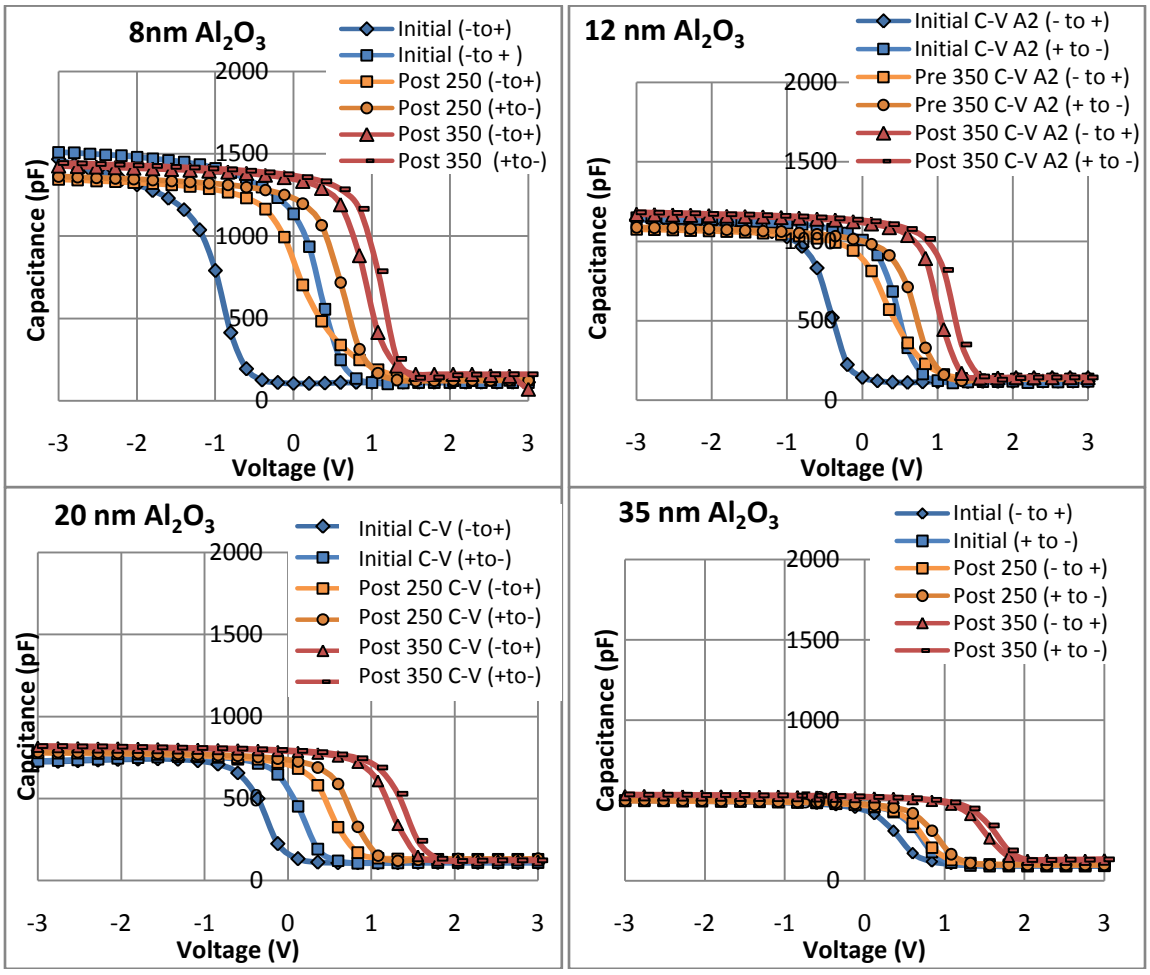


Figure 4-8: C-V curves for the Al_2O_3 passivated samples.

Looking at the samples with 8 nm to 35 nm of passivation, the maximum capacitance decreases for the thicker films, according to the inverse relationship between capacitance and film thickness shown in Equation 5

$$C = \frac{\varepsilon_o \, kA}{t}, \tag{5}$$

Where ε_0 is the permittivity of free space, k is the relative permittivity of the dielectric, A is the area of the film used in the measurement, and t is the film thickness.

Examining the V_{FB} shifts in each sample, a shift to more positive voltages is apparent (to the right) for each sample with increased annealing temperature. The shift to positive voltages indicates the presence of negative fixed charge. While the shifts appear greater for samples with thicker Al_2O_3 films, the corresponding decrease in capacitance leads to similar values of fixed charge in each sample. The greatest amount of fixed charge was achieved in the 8 nm Al_2O_3 passivated sample with the 5 min 350°C hot plate anneal, with a fixed charge density of $-7.1x10^{12}/cm^2$. Table 4-5 gives the values of fixed charge calculated for each film as deposited and after being annealed at 350°C.

Table 4-5: Fixed charge density in Al_2O_3 passivation films.

Al_2O_3 Sample	Film Thickness	Fixed Charge Density As Deposited	Fixed Charge Density Post 350°C
A1	8 nm	$-9.4x10^{11}/cm^2$	$-7.1x10^{12}/cm^2$
A2	12 nm	$-1.1x10^{12}/cm^2$	$-5.9x10^{12}/cm^2$
A3	20 nm	$-9.7x10^{11}/cm^2$	$-4.6x10^{12}/cm^2$
A4	35 nm	$-1.7x10^{12}/cm^2$	$-3.4x10^{12}/cm^2$

To ensure the integrity of the passivation layers over time, C-V measurements were taken on the 8 nm Al_2O_3 passivated sample three months after the 350°C anneal was performed. The V_{FB} shift was maintained and the C-V curves, shown in Figure 4-9, closely matched those taken originally. The repeatability of the measurements indicated that the passivation quality remained stable over the three month period.

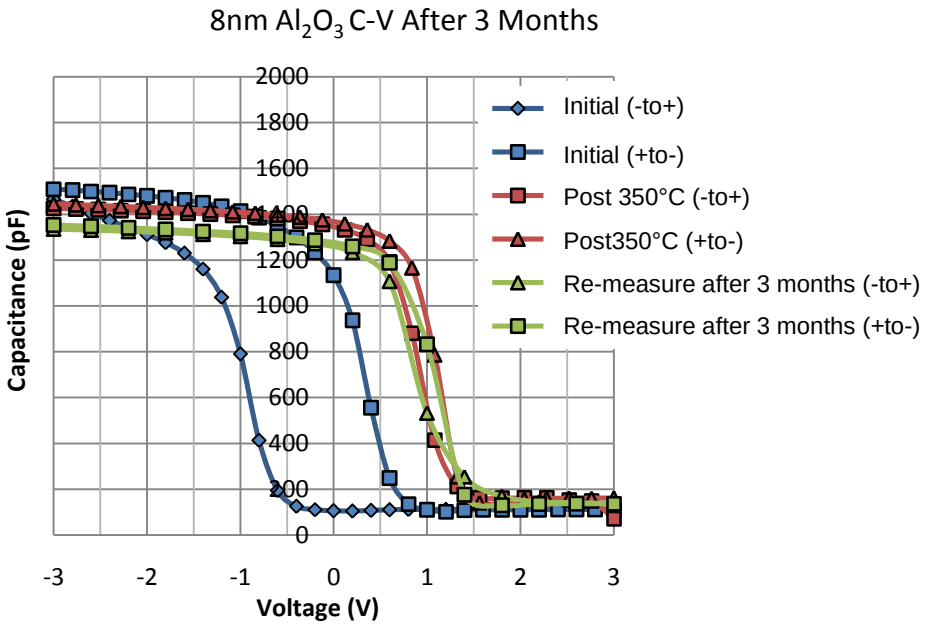


Figure 4-9: C-V curves of the 8 nm Al_2O_3 passivated sample after the 350°C anneal and three months later.

The C-V curves obtained with the mercury probe for the HfO_2 passivated samples are shown in Figure 4-10. The HfO_2 passivated samples exhibited characteristics similar to the Al_2O_3 passivated samples, showing reduced hysteresis and increased V_{FB} shifts with higher annealing temperatures. C-V curves were not taken for all of the samples as deposited, but shifts in V_{FB} were apparent for each when comparing the C-V curves of the 5 min 250°C anneal and the 5 min 350°C anneal. Similar to the Al_2O_3 samples, the largest fixed charge densities were calculated in films annealed for 5 min at 350°C.

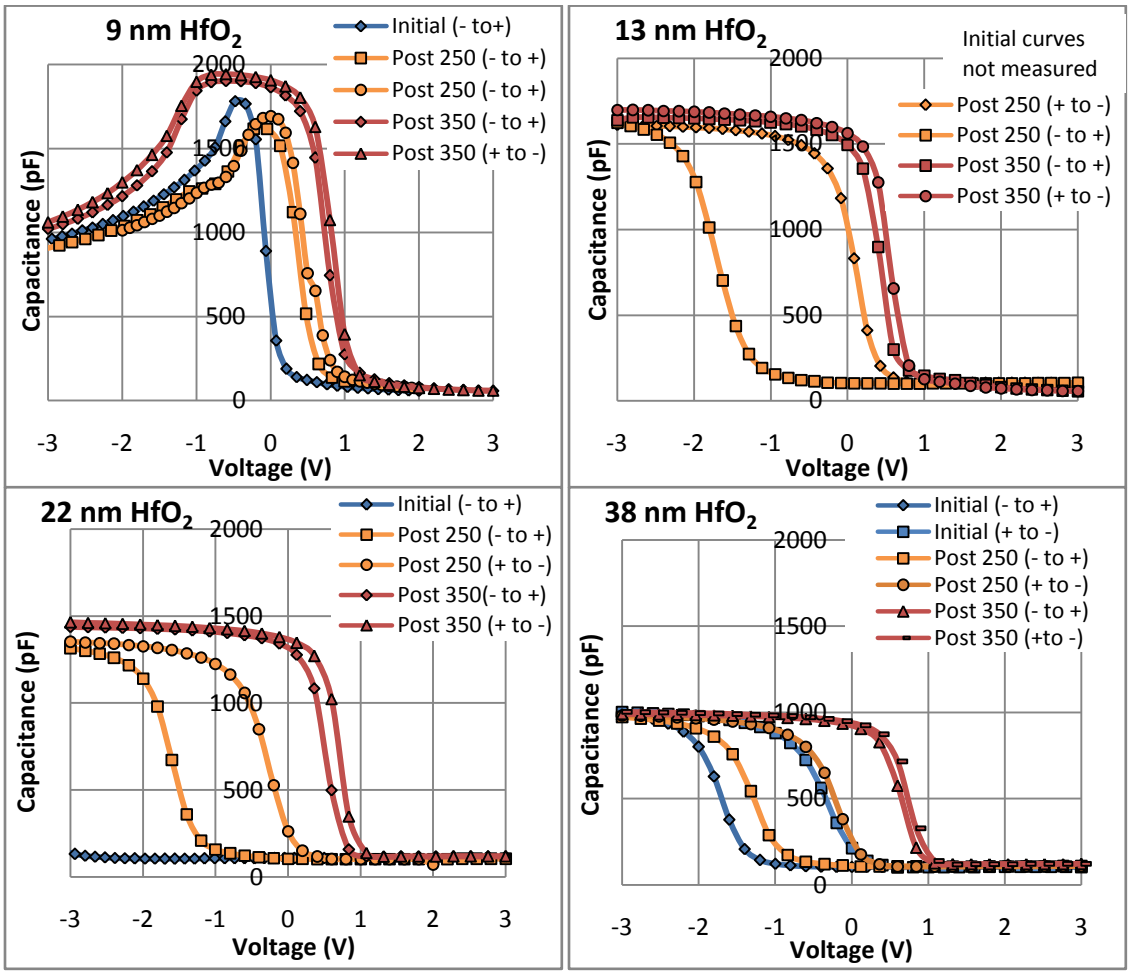


Figure 4-10: C-V curves for the HfO_2 passivated samples.

The fixed charge densities for each HfO_2 passivated sample are seen in Table 4-6. Interestingly, the fixed charge densities are very similar to those measured in the Al_2O_3 passivation films. The 9 nm HfO_2 film exhibited the largest fixed charge density of $-7.8x10^{12}/cm^2$. Due to time constraints and the longer effective carrier lifetimes exhibited by samples passivated with Al_2O_3, HfO_2 was not studied in further in the inversion layer experiment.

Table 4-6: Fixed charge density in HfO_2 passivation films.

HfO_2 Sample	Film Thickness	Fixed Charge Density Post 350°C
H1	9 nm	$-7.8 \times 10^{12}/cm^2$
H2	13 nm	$-5.3 \times 10^{12}/cm^2$
H3	22 nm	$-4.8 \times 10^{12}/cm^2$
H4	38 nm	$-3.4 \times 10^{12}/cm^2$

Results and Discussion

From the initial investigation of film thickness and annealing treatments, it was apparent that annealing treatments are critical for improving film quality and passivation. Lifetime increased with the temperature of the annealing treatments up to 350°C (except for the thicker passivation films) indicating reduced carrier recombination at the surface. The longest lifetime of 1.7 ms was achieved for the sample passivated with 20 nm of Al_2O_3 and annealed for 5 min at 350°C on the hot plate. Lifetimes over a millisecond were achieved on samples passivated with 8 nm Al_2O_3, 12 nm Al_2O_3, and 13 nm HfO_2 when annealed for 5 min at 350°C on the hot plate. The 38 nm HfO_2 sample annealed at 250°C on the vacuum chuck also exhibited a lifetime over a millisecond.

The 35 nm Al_2O_3 and 38 nm HfO_2 passivated samples had reduced lifetimes after annealing for 5 min at 350°C on the hot plate. It is not apparent why the thicker passivation films reacted poorly to the higher temperature annealing treatment.

Flatband voltage shifts apparent in C-V measurements increased to more positive voltages with higher temperature annealing treatments. The shifts indicated the presence of negative fixed charge in the passivation films. Improvement in the measured hysteresis was noted with increasing temperature annealing treatments. The increased V_{FB} and reduction in

hysteresis suggested the improvement of film quality with each anneal. The changes in the C-V curves indicated that a majority of interface states and trapped charges were removed with the 5 min 350°C anneal on the hot plate. Additionally, the V_{FB} shifts of the films were maintained over time as seen with re-measurement of the C-V curves after three months, showing that the integrity of the passivation was maintained.

For each sample fixed charge density was maximized with the 5 min 350°C anneal. Fixed charge density did not increase with increasing film thickness, and the largest fixed charge densities were found in the thinner films; $-7.1 \times 10^{12}/cm^2$ in the 8 nm Al_2O_3 passivated sample and $-7.8 \times 10^{12}/cm^2$ in the 9 nm HfO_2 passivated sample. The fixed charge passivation was stable over time as indicated by the maintained V_{FB} shifts in the C-V measurements after 3 months.

Multi-Layer Passivation Experiment: Al_2O_3/SiO_x and HfO_2/SiO_x Layers

In the second passivation experiment, an investigation of thin Al_2O_3 films capped with SiO_x was performed. It was assumed that adequate passivation could be possible with a thin film of Al_2O_3 or HfO_2, as seen in the previous experiment, capped with a layer of SiO_x, and that fixed charge could be maximized in the passivation structure based on the idea that the fixed charge exists at the interfaces of the dielectric. In the previous experiment the best lifetimes were achieved for samples passivated with Al_2O_3 layers 8 to 20 nm thick, and the largest fixed charge density was measured in the thinnest passivation layers, further supporting the investigation of very thin Al_2O_3 passivation films capped with SiO_x.

Prior to designing a full experiment to investigate the effects of an SiO_x capping layer on passivation, a brief study was performed using the 8 nm Al_2O_3 and 9 nm HfO_2 passivated samples from the previous experiment. Each sample was capped, on one side, with 50 nm of SiO_x deposited using PECVD. C-V measurements and effective carrier lifetime measurements were

taken on the samples as deposited, after a 5 min 250°C anneal, and after a 5 min 350°C anneal, both in air.

The lifetime results for the SiO_x capped samples are shown in Table 4-7. With the exception of the 8 nm Al_2O_3/50 nm SiO_x sample annealed at 350°C, effective carrier lifetimes were larger on the SiO_x capped samples than those passivated with only the ALD films. Lifetime measurements were taken one month after the samples were capped to see if passivation quality was maintained, and interestingly the effective carrier lifetime increased over 200 µs for reasons unknown.

Table 4-7: Lifetime of thin film ALD samples capped with SiO_x.

Sample	Film Thicknesses	As Deposited	Post 250°C	Post 350°C	After 1 Month
A1	8 nm Al_2O_3/50 nm SiOx	406 µs	627 µs	747 µs	1000 µs
H1	9 nm HfO_2/50 nm SiOx	615 µs	923 µs	1040 µs	1306 µs

The C-V curves for the SiO_x capped samples are shown in Figure 4-11. V_{FB} shifts were apparent with increased annealing treatment, as was a reduction of hysteresis in the measurements. C-V measurements taken one month and two months after the 350°C anneal showed further V_{FB} shifts indicating further improvement in the film and increased negative fixed charge density.

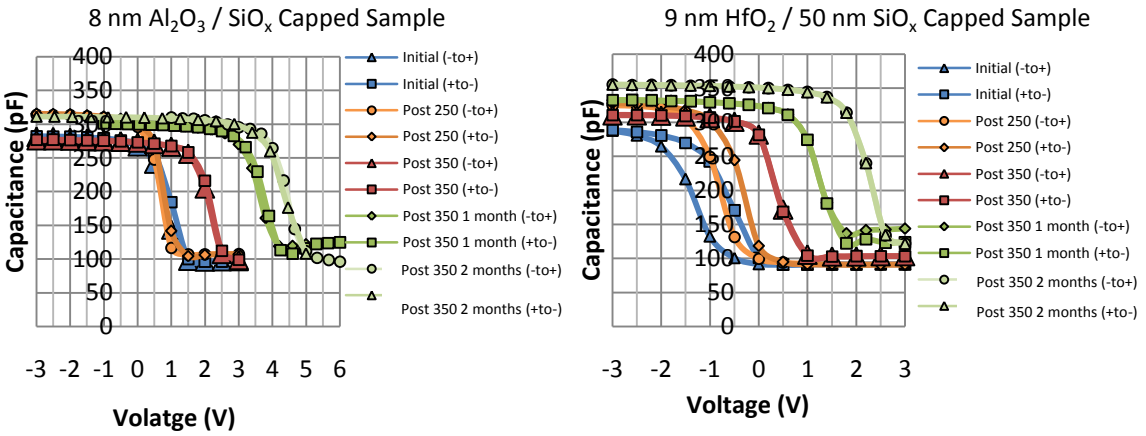


Figure 4-11: C-V curves for 8 nm Al_2O_3 and 9 nm HfO_2 samples capped with 50 nm SiO_x.

Given the interesting results obtained in the initial investigation of SiO_x capping layers, a full experiment was designed to compare the passivation quality of Al_2O_3 passivated samples and Al_2O_3/SiO_x passivated samples. In the interest of minimizing deposition time further, a thin 4 nm layer of Al_2O_3 was investigated. Samples were fabricated on 275 µm thick, dual side polished, (100) 1-5 Ω-cm, p-type FZ silicon wafers with the passivation layers shown in Figure 4-12. The 4 nm layers of Al_2O_3 were deposited by ALD, and the 50 nm capping layers of SiO_x were deposited by PECVD.

50 nm SiO_x layer
4 nm Al_2O_3 layer
p-type Si wafer
4 nm Al_2O_3 layer
50 nm SiO_x layer

4 nm Al_2O_3 layer
p-type Si wafer
4 nm Al_2O_3 layer

Figure 4-12: Cross sectional diagram of the passivation layer stack up.

C-V measurements were performed with the mercury probe and LCR meter, and effective carrier lifetime measurements were performed by microwave photoconductive decay on the samples as deposited, after a 5 min 250°C vacuum chuck anneal, and after a 5 min 350°C hot plate anneal.

Lifetime Measurements

The initial lifetimes for the thin film samples were very low and did not improve with the 250°C anneal. The 350°C anneal yielded a moderate increase in effective carrier lifetime, providing the longest lifetime of 373 µs on the 4 nm Al_2O_3/50 nm SiO_x passivated sample.

Table 4-8: Lifetime of the 4 nm Al_2O_3 and 4 nm Al_2O_3/50 nm SiO_x passivated samples.

Sample Passivation	Initial Lifetime	Post 250°C Lifetime	Post 350°C Lifetime
4 nm Al_2O_3	108 µs	75 µs	178 µs
4 nm Al_2O_3 / 50 nm SiO_x	108 µs	63 µs	373 µs

C-V Measurements

Studying the shift of V_{FB} with each progressive heat treatment showed that the 350°C annealing treatment maximized fixed charge in each passivation film. Neither V_{FB} shifted significantly with the 250°C anneal. The largest V_{FB} shift of 3.5 V was achieved with the 350°C anneal of the 4 nm Al_2O_3/50 nm SiO_x passivated sample. Measuring the sample one week after the 350°C anneal showed improvement in the V_{FB} shift, and measuring it again after two months showed a further V_{FB} shift but reintroduction of hysteresis in the measurement, shown in Figure 4-13. The development of hysteresis in the measurements was apparent only in the thin 4 nm Al_2O_3/50 nm SiO_x passivated sample.

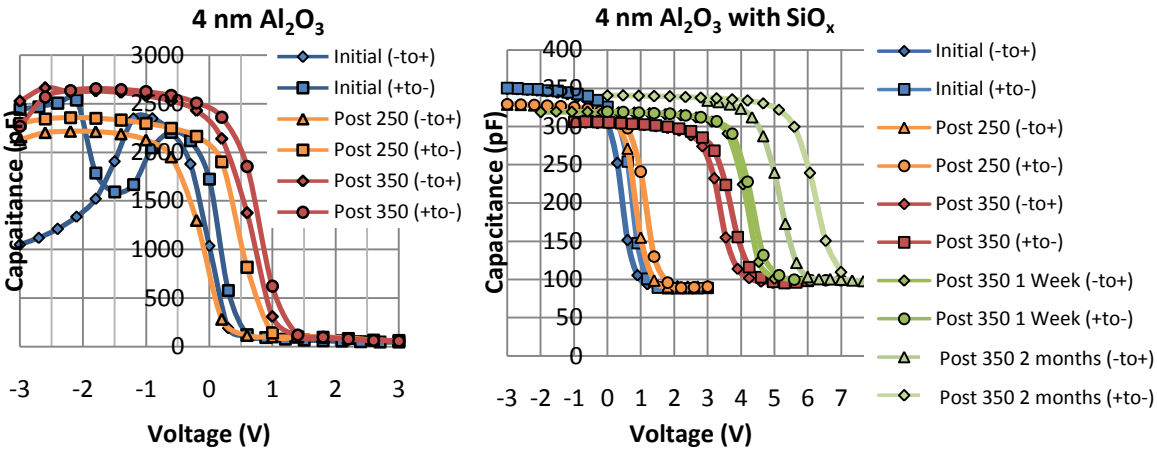


Figure 4-13: C-V measurements for 4 nm Al_2O_3 and 4 nm Al_2O_3/50 nm SiO_x passivated samples.

Fixed charge densities for the 4 nm Al_2O_3/50 nm SiO_x passivated samples are given in Table 4-9. The fixed charge density increased over time and was modest for such a thin film.

Table 4-9: Fixed charge density values for the SiO_x capped samples.

Sample	Fixed Charge Density Post 350°C Anneal	Fixed Charge Density After 1 Week	Fixed Charge Density After 2 Months
4 nm Al_2O_3/50 nm SiO_x	-4.0x10^{12}/cm^2	-4.8x10^{12}/cm^2	-5.9x10^{12}/cm^2
8 nm Al_2O_3/50 nm SiO_x	-2.3 x10^{12}/cm^2	-3.9 x10^{12}/cm^2	-4.4 x10^{12}/cm^2
9 nm Al_2O_3 50 nm SiO_x	-9.2 x10^{11}/cm^2	-1.9 x10^{12}/cm^2	-3.0 x10^{12}/cm^2

Results and Discussion

Investigating capped samples and very thin film Al_2O_3 samples has shown that adequate passivation can be achieved with SiO_x capped films. However, Al_2O_3 films of thicknesses greater than 4 nm were required to achieve effective carrier lifetimes comparable to those used in solar cells. A lifetime of 373 µs was achieved on the 4 nm Al_2O_3/50 nm SiO_x passivated samples.

Longer lifetimes, of 747 µs and 1040 µs, were achieved on the 8 nm Al_2O_3/50 nm SiO_x and 9 nm HfO_2/50 nm SiO_x passivated samples, respectively.

As with the previous films, these passivation layers required an annealing treatment to improve lifetime and maximize fixed charge density. The largest V_{FB} shifts were achieved with the 5 min 350°C anneal, and hysteresis in the C-V measurements was also alleviated. The corresponding fixed charge density of the 4 nm Al_2O_3/50 nm SiO_x passivated sample was $-4.0x10^{12}/cm^2$, and the fixed charge density of the 8 nm Al_2O_3/50 nm SiO_x passivated sample was $-2.3x10^{12}/cm^2$.

The most interesting discovery made during this experiment was the improvement of the capped layers' lifetime and V_{FB} shift over time. When re-measured after weeks and months, effective carrier lifetimes were longer and V_{FB} shifts were greater. The fixed charge densities of each film increased, and were calculated to be $-5.9x10^{12}/cm^2$ and $-4.4x10^{12}/cm^2$ for the 4 nm Al_2O_3/50 nm SiO_x and the 8 nm Al_2O_3/50 nm SiO_x passivated sample, respectively. In both cases the new fixed charge density was approximately $-2x10^{12}/cm^2$ greater. The films in this work were in the dark for the better part of their storage between measurements, so the improvement cannot be attributed to charging under illumination. The improvement in the films merits further investigation, but was encouraging since some conventional passivation films degrade over time and under illumination. Other groups have not reported such improvements, and if the improvement in the Al_2O_3/SiO_x passivation is stable, it could have important implications on the selection of passivation layers in high efficiency cells.

Inversion Layer Experiment: Al_2O_3 and Al_2O_3/SiO_x Layers

In the third experiment, several different layer structures were fabricated to determine the magnitude of fixed charge attainable by introducing multiple interfaces within the passivation structure. Additionally, we sought to determine if the presence of fixed charge in the passivation layer could induce an inversion layer in the near surface of the silicon substrate. Along with effective carrier lifetime and C-V measurements, contactless sheet resistance measurements were taken. A reduction in sheet resistance would suggest increased conductivity near the surface, and indicate the creation of an inversion layer (in an n-type sample) due to the presence of negative fixed charge in the passivation layer. Samples for sheet resistance measurements were fabricated on high resistivity ($\rho \geq 10000$) nominally n-type FZ (100) wafers to ensure that any change in measurement would be indicative of an inversion layer, and not affected by carriers in a low resistance substrate. Samples for lifetime measurements were fabricated on p-type (ρ = 1-5 Ω-cm) FZ (100) wafers, and samples for C-V measurements were fabricated on both p-type and n-type (ρ = 0.5-1 Ω-cm) CZ (100) wafers. The passivation layer structures fabricated are seen in Figure 4-14.

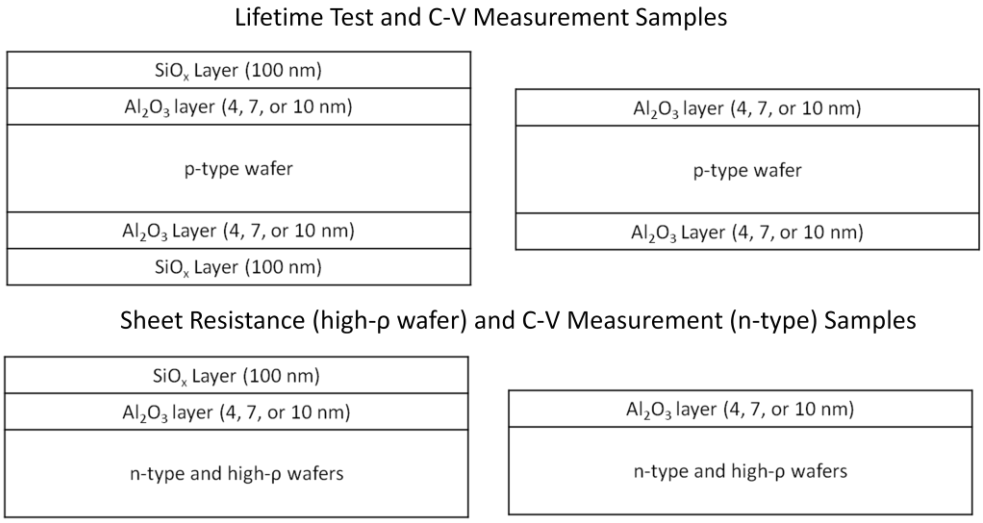


Figure 4-14: Passivation layers on different substrates for lifetime and C-V measurements and sheet resistance measurements.

Different thicknesses of Al_2O_3 passivation layers were investigated based on results from prior experiments; 4 nm, 7 nm, and 10 nm films were deposited by ALD. One set of samples was capped with 100 nm of SiO_x deposited by PECVD. Hafnia passivation layers were not studied since previous experiments showed Al_2O_3 layers provided superior passivation. An additional sample structure was fabricated in an attempt to maximize fixed charge density, based on the assumption that fixed charge exists at the interfaces of Al_2O_3 layers. Shown in Figure 4-15, the "stack" sample consisted of alternating Al_2O_3 and SiO_x layers. A 4 nm Al_2O_3 layer was deposited first, as it has been shown to have the largest fixed charge density, followed by a thin 4 nm SiO_x layer, a thicker 7 nm Al_2O_3 layer, and finally a 50 nm SiO_x layer. Different variations of this structure are of interest for future work.

SiO_x Layer (50 nm)
Al_2O_3 layer (7 nm)
SiO_x Layer (4 nm)
Al_2O_3 layer (4 nm)
p-type wafer
Al_2O_3 Layer (4 nm)
SiO_x Layer (4 nm)
Al_2O_3 layer (7 nm)
SiO_x Layer (50 nm)

Figure 4-15: Stack passivation layer sample.

After deposition of the different passivation structures, wafers were cleaved and individual pieces were subject to particular annealing treatments. Annealing was performed at three different temperatures, 250°C, 350°C, and 450°C, on either a vacuum chuck, a hot plate, in an rapid thermal anneal (RTA) furnace, or in a tube furnace for 5 min, to better understand the effect of different annealing conditions. The vacuum chuck, hot plate, and tube furnace anneals

were done in air (compressed dry air flowed through the tube furnace at 1 sL/min), and the RTA anneals were in an argon environment (2 to 3 sL/min). Table 4-10 details the different annealing treatments.

Table 4-10: Annealing conditions studied.

Temperature	Vacuum Chuck 5 minutes	Hot Plate 5 min	Tube Furnace 5 min	RTA 5 min
250°C	X	-	-	X
350°C	-	X	-	X
450°C	-	-	X	X

Rapid thermal annealing is commonly used in the microelectronics industry to quickly reach an elevated temperature that will effectively anneal dielectric layers. Typical durations are 1-2 min; however, in this work all annealing processes lasted 5 min for consistency. Additional investigations would be required to determine the optimal time for each annealing process.

Lifetime Measurements

Effective carrier lifetime measurements were taken for each sample as deposited and after each annealing treatment. Measurements were taken using the µ-PCD set-up as in previous experiments. Table 4-11 details the measurements for each sample.

Table 4-11: Effective carrier lifetime measurements for samples across different annealing treatments.

Sample	Layers	Initial	250°C Hot Plate 5 min	250°C RTA 5 min	350°C Hot Plate 5 min	350°C RTA 5 min	450°C Tube Furnace 5 min	450°C RTA 5 min
P-A4	4 nm Al_2O_3	108 µs	53 µs	80 µs	385 µs	33 µs	138 µs	128 µs
P-A7	7 nm Al_2O_3	166 µs	193 µs	315 µs	1249 µs	323 µs	620 µs	243 µs
P-A10	10 nm Al_2O_3	218 µs	203 µs	233 µs	1125 µs	638 µs	755 µs	250 µs
P-A4S100	4 nm Al_2O_3 100 nm SiO_x	120 µs	98 µs	65 µs	531 µs	169 µs	485 µs	365 µs
P-A7S100	7 nm Al_2O_3 100 nm SiO_x	205 µs	295 µs	255 µs	1249 µs	360 µs	595 µs	670 µs
P-A10S100	10 nm Al_2O_3 100 nm SiO_x	308 µs	540 µs	455 µs	1563 µs	510 µs	1538 µs	980 µs
Stack sample	Stack	225 µs	305 µs	300 µs	435 µs	490 µs	638 µs	515 µs

The lower temperature, 250°C annealing treatments did not improve surface passivation. The greatest improvement in lifetime was achieved with the 350°C hot plate anneal, which can be seen graphically in Figure 4-16. For a few samples the 450°C tube furnace anneal and 450°C RTA anneal improved carrier lifetime, but not to the same extent as the 350°C hot plate anneal.

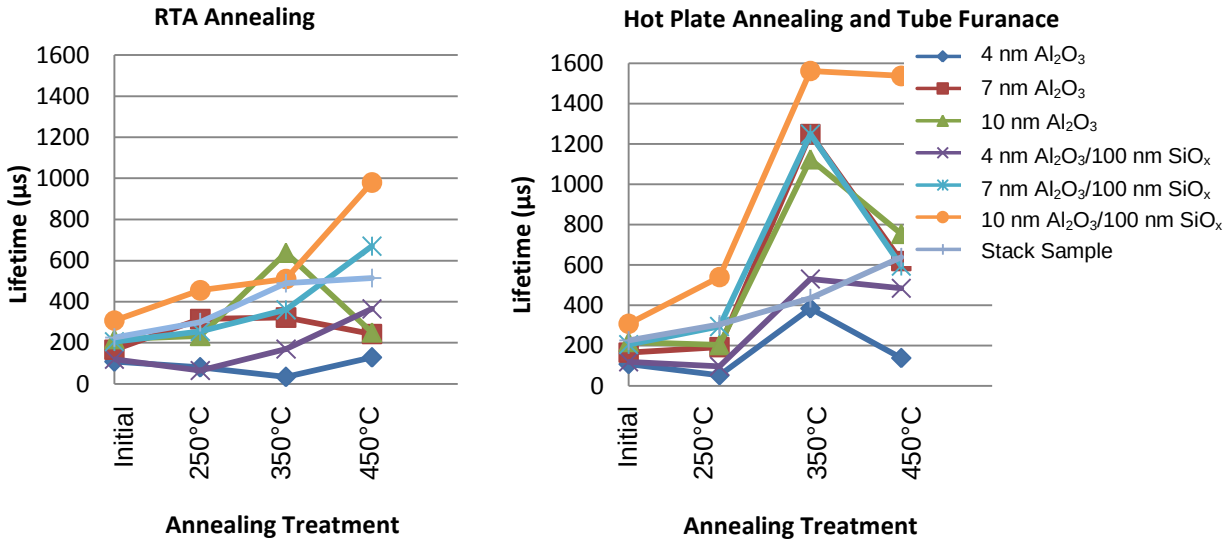


Figure 4-16: Effective carrier lifetime vs. annealing treatment: (a) RTA annealing (b) hot plate annealing.

From the graphs in Figure 4-16 it is it is clear that the 350°C hot plate anneal was the most effective, followed by the 450°C RTA anneal and the 450°C tube furnace anneal. The longest lifetime, 1.5 ms, was measured on the 10 nm Al_2O_3/100 nm SiO_x passivated sample annealed at 350°C on the hot plate. Long lifetimes of 980 µs and 1538 µs were measured on samples passivated with the same structure annealed for 5 min at 450°C in the RTA and at 450°C in the tube furnace. Annealed for 5 min at 350°C on the hot plate, the 7 nm Al_2O_3 passivated sample and the 7 nm Al_2O_3/100 nm SiO_x sample both exhibited lifetimes of 1.2 ms, and the 10 nm Al_2O_3 passivated sample provided a lifetime of 1.1 ms. The 4 nm Al_2O_3 and 4 nm Al_2O_3/100 nm SiO_x passivated samples did not reach the longer lifetimes of those passivated with thicker films but did show improvement with the 350°C hot plate anneal and the 450°C RTA and tube

furnace anneals. It is clear that a temperature higher than 250°C is required for annealing to improve film quality and reduce surface recombination.

Interestingly, the lifetime of the stack sample did not improve appreciably with any of the annealing treatments. This may be due to exposure to ambient air in between growth of the ALD films and the PECVD films, or possibly the presence of positive fixed charge in the SiO_x film that negates the negative fixed charge in the Al_2O_3 film (60).

C-V Measurements

C-V measurements were taken on each sample in order to calculate fixed charge densities. For samples passivated with single layers of Al_2O_3, measurement trends and values were similar to those presented in the previous section on C-V measurements in the "Film Thickness Experiment: Al_2O_3 and HfO_2 Layers" section. The largest fixed charge density of all films studied was measured in the 4 nm Al_2O_3 film annealed for 5 min at 350°C on the hot plate, with a density of $-1x10^{-13}/cm^2$. The C-V curves for the single Al_2O_3 layer samples can be found in Appendix C for further reference.

The C-V curves in the following figures were taken on p-type samples passivated with the Al_2O_3/100 nm SiO_x layers. In previous samples with single layers of Al_2O_3, V_{FB} shifts increased with both the 5 min 250°C anneal and the 5 min 350°C anneal. For several of the capped samples, V_{FB} increased only with the 5 min 350°C, and no improvement was observed with the lower temperature anneal. In a few samples a V_{FB} shift to more negative voltages was observed in response to the 5 min 250°C anneal. Shifts to the left indicated positive fixed charge in the film, but after a 350°C anneal the V_{FB} shifted to more positive voltages, indicating negative fixed charge. The 5 min 250°C anneal might not have been sufficient to "activate" the negative fixed charge in the film, or perhaps the positive fixed charge density in the SiO_x film was larger

than the negative fixed charge density and caused the negative shift in V_{FB}. It is important to note that the drastic shifts in V_{FB}, while they do indicate an increase in fixed charge, are partly due to the increased voltage required to make the C-V measurement through the thick SiO_x layer. For the most part the introduction of the SiO_x capping layer decreased the overall negative fixed charge density.

The C-V measurements in Figure 4-17 were taken on the 4 nm Al_2O_3/100 nm SiO_x samples annealed in the RTA furnace. The V_{FB} voltage shift achieved with the 450°C RTA anneal was approximately 8.5 V and corresponded to a fixed charge density calculated to be $-4.1x10^{12}/cm^2$ and a lifetime value of 365 µs. With the 350°C RTA anneal the V_{FB} shifted right to 4 V (indicating negative fixed charge), and the measured effective carrier lifetime increased to 169 µs. For the 250°C RTA anneal, V_{FB} shifted to the left (indicating the presence of positive fixed charge), and the measured lifetime, 65 µs, was reduced from the initially measured 120 µs lifetime.

Sample	Passivation Layer	Initial	250°C RTA 5 min	350°C RTA 5 min	450°C RTA 5 min
P-A4S100	4 nm Al_2O_3 100 nm SiO_x	120 µs	65 µs	169 µs	365 µs

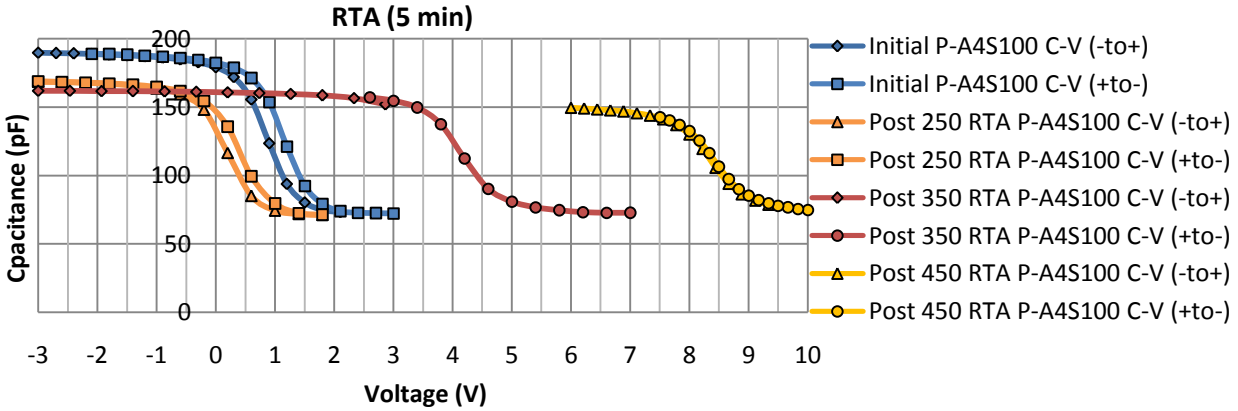


Figure 4-17: C-V measurements for RTA annealed 4 nm Al_2O_3/100 nm SiO_x passivated samples.

The C-V measurements for 4 nm Al_2O_3/100 nm SiO_x samples annealed on the hot plate and tube furnace are seen in Figure 4-18. The largest V_{FB} voltage shift occurred with the 450°C

tube furnace anneal, which was only slightly improved over the 350°C hot plate anneal, and was approximately 6 V. The shift correlated to a fixed charge density calculated to be -3.5x10^{12}/cm^2 and correlated to a lifetime of 495 µs. The 350°C hot plate anneal induced a V_{FB} shift of 5.5V and the measured effective carrier lifetime increased to 531 µs.

Sample	Passivation Layer	Initial	250°C Hot Plate 5 min	350°C Hot Plate 5 min	450°C Tube Furnace 5 min
P-A4S100	4 nm Al_2O_3 100 nm SiO_x	120 µs	98 µs	531 µs	485 µs

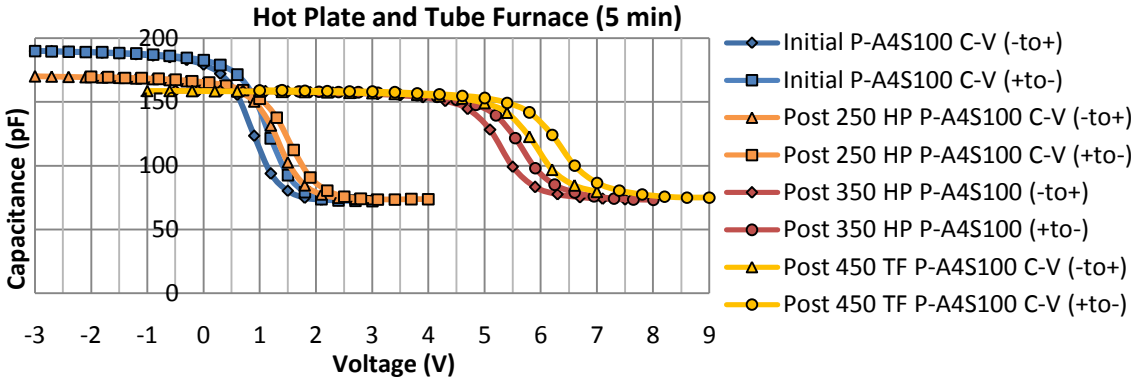


Figure 4-18: C-V measurements for the HP and TF annealed 4 nm Al_2O_3/100 nm SiO_x samples.

The C-V measurements in Figure 4-19 were taken on the 7 nm Al_2O_3/100 nm SiO_x samples annealed in the RTA furnace. The V_{FB} voltage shift achieved with the 450°C RTA anneal was the greatest, approximately 6 V. The shift corresponded to a fixed charge density of -4.1x10^{12}/cm^2 and a lifetime of 670 µs.

Sample	Passivation Layer	Initial	250°C RTA 5 min	350°C RTA 5 min	450°C RTA 5 min
P-A7S100	7 nm Al_2O_3 100 nm SiO_x	205 µs	255 µs	360 µs	670 µs

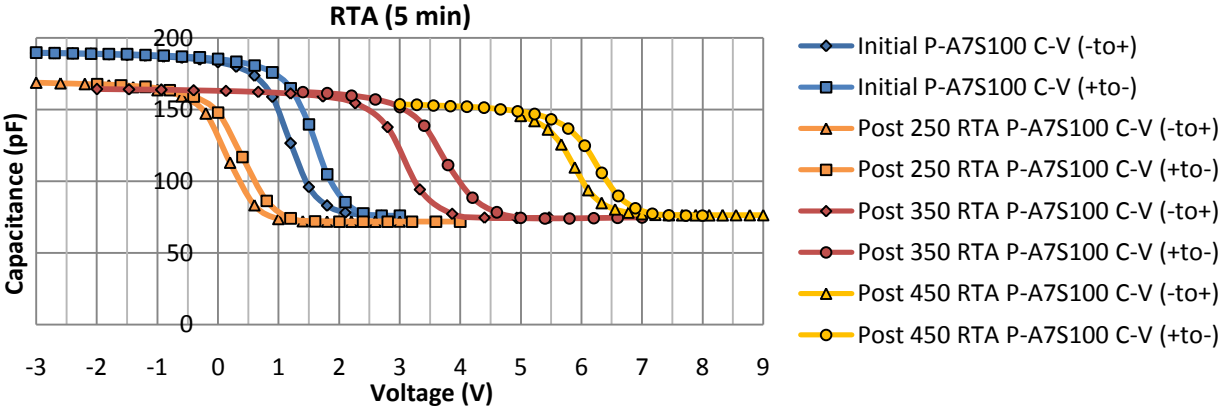


Figure 4-19: C-V measurements of the RTA annealed 7 nm Al_2O_3/100 nm SiO_x samples.

C-V measurements for 7 nm Al_2O_3/100 nm SiO_x samples annealed on the hot plate and tube furnace are seen in Figure 4-20. The largest V_{FB} voltage shift occurred with the 350°C hot plate anneal, which in this case provided better results than the 450°C tube furnace anneal. The V_{FB} for the 350°C hot plate anneal was approximately 4.5 V, which correlated to a fixed charge density calculated to be $-2.6 \times 10^{12}/cm^2$ and a lifetime of 1249 µs. The C-V measurement taken after 450°C tube furnace anneal was stretched out significantly compared to the other curves measured. The V_{FB} of 3.4 V corresponded to a lifetime of only 595 µs, much less than the 1.2 ms lifetime measured on the sample annealed at 350°C on the hot plate.

Sample	Passivation Layer	Initial	250°C Hot Plate 5 min	350°C Hot Plate 5 min	450°C Tube Furnace 5 min
P-A7S100	7 nm Al_2O_3 100 nm SiO	205 µs	295 µs	1249 µs	595 µs

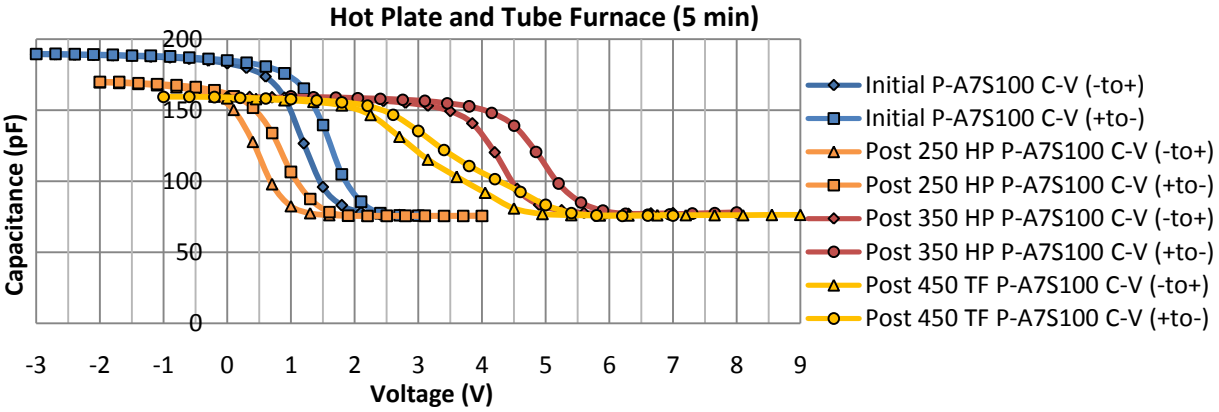


Figure 4-20: C-V measurements for HP and TF annealed 7 nm Al_2O_3/100 nm SiO_x samples.

The C-V measurements in Figure 4-21 were taken on the 10 nm Al_2O_3/100 nm SiO_x samples annealed in the RTA furnace. The largest V_{FB} shift occurred with the 450°C RTA anneal and was approximately 4.1 V, which corresponded to a fixed charge density of $-2.2 \times 10^{12}/cm^2$ and a lifetime of 980 µs.

Sample	Passivation Layer	Initial	250°C RTA 5 min	350°C RTA 5 min	450°C RTA 5 min
P-A10S100	10 nm Al_2O_3 100 nm SiO_x	308 µs	455 µs	510 µs	980 µs

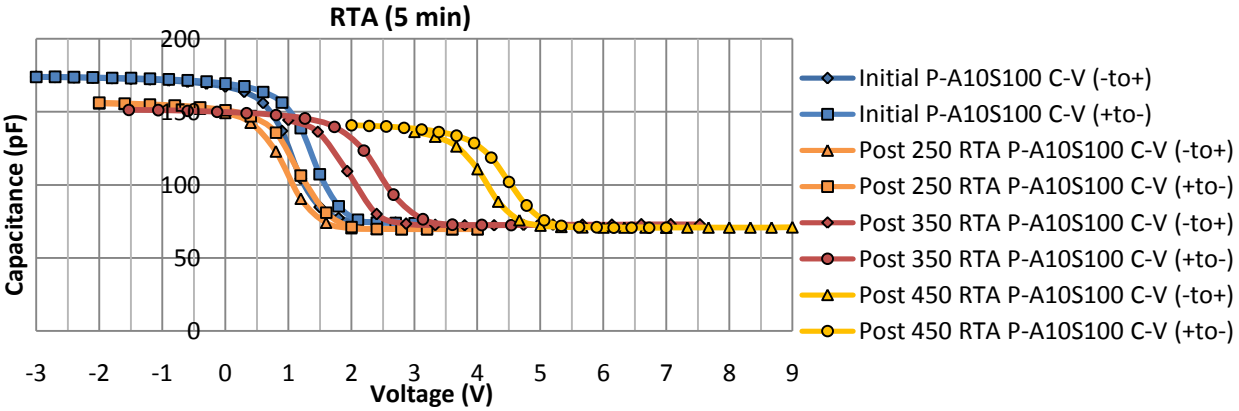


Figure 4-21: C-V measurements for RTA annealed 10 nm Al_2O_3/100 nm SiO_x samples.

C-V measurements for 10 nm Al_2O_3/100 nm SiO_x samples annealed on the hot plate and tube furnace are shown in Figure 4-22. Both the 350°C hot plate anneal and the 450°C tube furnace anneal significantly improved effective carrier lifetime, resulting in the highest lifetimes measured in this experiment. The largest V_{FB} voltage shift of 4.4V occurred with the 450°C tube furnace anneal, and correlated to a fixed charge density calculated to be -2.4x10^{12}/cm^2 and a lifetime of 1538 µs. The 350°C hot plate anneal led to a V_{FB} shift of 2.6 V and corresponded to an effective carrier lifetime measurement of 1.5 ms.

Sample	Passivation Layer	Initial	250°C Hot Plate 5 min	350°C Hot Plate 5 min	450°C Tube Furnace 5 min
P-A10S100	10 nm Al_2O_3 100 nm SiO_x	308 µs	540 µs	1563 µs	1538 µs

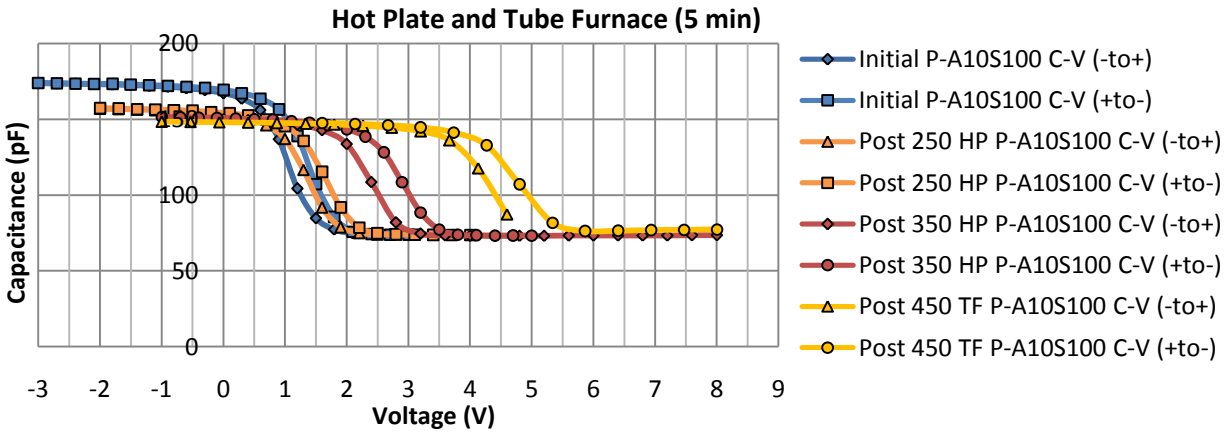


Figure 4-22: C-V measurement for HP and TF annealed 10 nm Al_2O_3/100 nm SiO_x samples.

The C-V measurements for the stack samples annealed in the RTA furnace are shown in Figure 4-23. The stack sample consisted of 4 nm Al_2O_3/4 nm SiO_x/7 nm Al_2O_3/50 nm SiO_x passivation layers on a p-type substrate. Multiple Al_2O_3/SiO_x layers were deposited in an attempt to maximize fixed charge, assuming that it resides at the Al_2O_3 interfaces. The largest V_{FB} shift occurred with the 450°C RTA anneal to approximately 9.7 V. The shift in V_{FB} corresponded to a fixed charge density of -4.1x10^{12}/cm^2 and a lifetime of 515 µs. Shifts in V_{FB} correlate somewhat with effective carrier lifetime measurements, but the drastic shifts in V_{FB} do not correspond to

large increases in lifetime. The increased thickness of the sample forces the use of higher voltages when taking the measurements. The fixed charge density was not increased by increasing the number of Al_2O_3 interfaces by using SiO_x layers in the structure.

Sample	Passivation Layer	Initial	250°C RTA 5 min	350°C RTA 5 min	450°C RTA 5 min
Stack	Stack	225 µs	300 µs	490 µs	515 µs

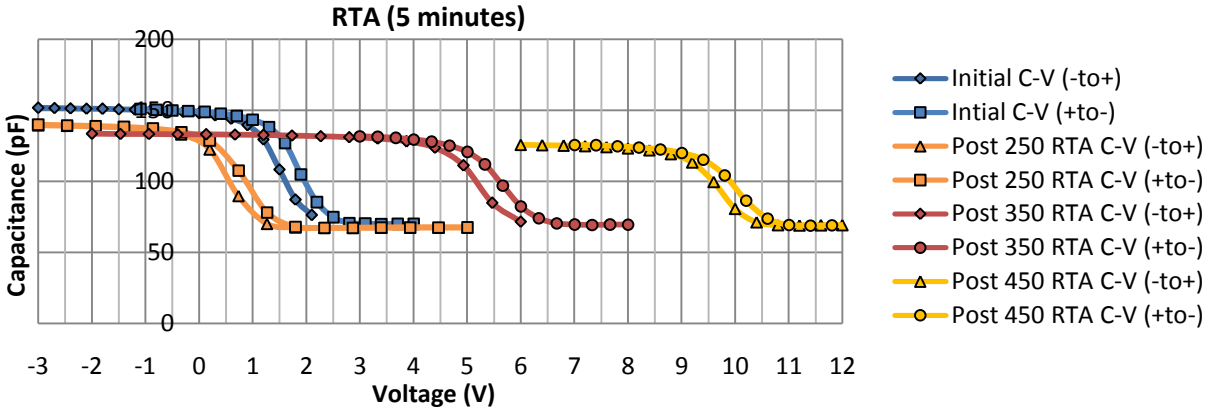


Figure 4-23: C-V measurements for RTA annealed 4 nm Al_2O_3/4 nm SiO_x/7 nm Al_2O_3/50 nm SiO_x samples.

C-V measurements for stack samples annealed on the hot plate and tube furnace are seen in Figure 4-24. The largest V_{FB} voltage shift, of 8.3 V, occurred with the 450°C tube furnace anneal, and corresponded to a fixed charge density calculated to be $-3.6 \times 10^{12}/cm^2$ and a lifetime 638 µs.

Sample	Passivation Layer	Initial	250°C Hot Plate 5 min	350°C Hot Plate 5 min	450°C Tube Furnace 5 min
Stack sample	Stack	225 µs	305 µs	435 µs	638 µs

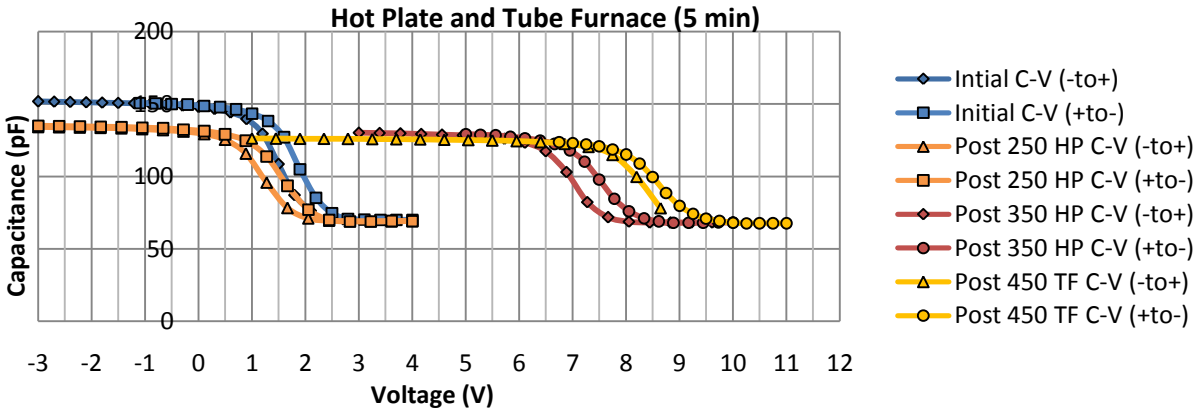


Figure 4-24: C-V measurements for HP and TF annealed 4 nm Al_2O_3/4 nm SiO_x/7 nm Al_2O_3/50 nm SiO_x samples.

Upon examining the fixed charge values calculated for each sample there does not appear to be a strong correlation between fixed charge density and film thickness. The values given in Table 4-12 were calculated for samples fabricated on both p and n-type substrates. C-V curves of the n-type samples can be found in Appendix B. The thinner films have slightly more fixed charge, but all of the values are of the same order of magnitude. There was not an increase in fixed charge density for the multi-layer stack sample.

Table 4-12: Maximum fixed charge densities.

Sample	Passivation Layer	Max Fixed Charge p-Type Substrate	Max Fixed Charge n-Type Substrate
P-A4	4 nm Al_2O_3	-1.1x10^{13}/cm^2	-8.1 x10^{12}/cm^2
P-A7	7 nm Al_2O_3	-9.6x10^{12}/cm^2	-7.2 x10^{12}/cm^2
P-A10	10 nm Al_2O_3	-9.3 x10^{12}/cm^2	-7.2 x10^{12}/cm^2
P-A4S100	4 nm Al_2O_3 100 nm SiO_x	-4.1 x10^{12}/cm^2	-4.8 x10^{12}/cm^2
P-A7S100	7 nm Al_2O_3 100 nm SiO_x	-3.2 x10^{12}/cm^2	-2.7 x10^{12}/cm^2
P-A10S100	10 nm Al_2O_3 100 nm SiO_x	-2.4 x10^{12}/cm^2	-4.2 x10^{12}/cm^2
Stack sample	Stack	-4.1 x10^{12}/cm^2	N/A

For many of the annealed samples the measured effective carrier lifetime values correlated with V_{FB} shifts seen in the C-V measurements. The largest V_{FB} shifts typically occurred with the highest temperature anneals, as did the longest lifetime values. The 350°C hot plate anneal and the 450°C tube furnace anneal yielded some of the longest lifetimes, 1.5 ms for the 10 nm Al_2O_3/100 nm SiO_x sample. The stack sample did not achieve a lifetime better that 638 μs, and fixed charge density did not increase with the number of layer interfaces.

Sheet Resistance Results

After samples had been annealed, sheet resistances of the films deposited on high resistivity wafers were measured using a Lehighton 1605 contactless conductivity probe. The system measures sheet resistance through the detection of eddy currents in a material induced by a drive coil (50). Samples were placed onto a mylar carrier and slid into the microwave circuit, and the reflection induced by conductivity in the sample was detected. A copper disk was inserted into the circuit prior to sample measurement, and being completely conductive, allowed for calibration of the tool.

The measurements taken for each passivated sample are shown in the following figures. Sheet resistance is plotted against annealing condition, which are ordered not by increasing temperature but by increasing effectiveness, as determined by improvements in lifetime and C-V measurements. Effective carrier lifetime (of passivated p-type samples measured in the last experiment) is plotted on a second vertical axis against annealing treatments as well. Reduction in sheet resistance indicates the presence of an inversion layer in the high resistivity silicon induced by negative fixed charge in the passivation film.

The graphs in Figure 4-25 show sheet resistance and effective carrier lifetime plotted against annealing treatments for the 4 nm Al_2O_3 passivated samples and the 4 nm Al_2O_3/100 nm

SiO_x passivated samples. It is apparent that sheet resistance of the samples tends to decrease as the annealing treatments improve the passivation layers, as indicated by increased lifetimes. For the most part decreased sheet resistance correlates to improved carrier lifetime further supporting the presence of an inversion layer induced by the fixed charge in the passivation film.

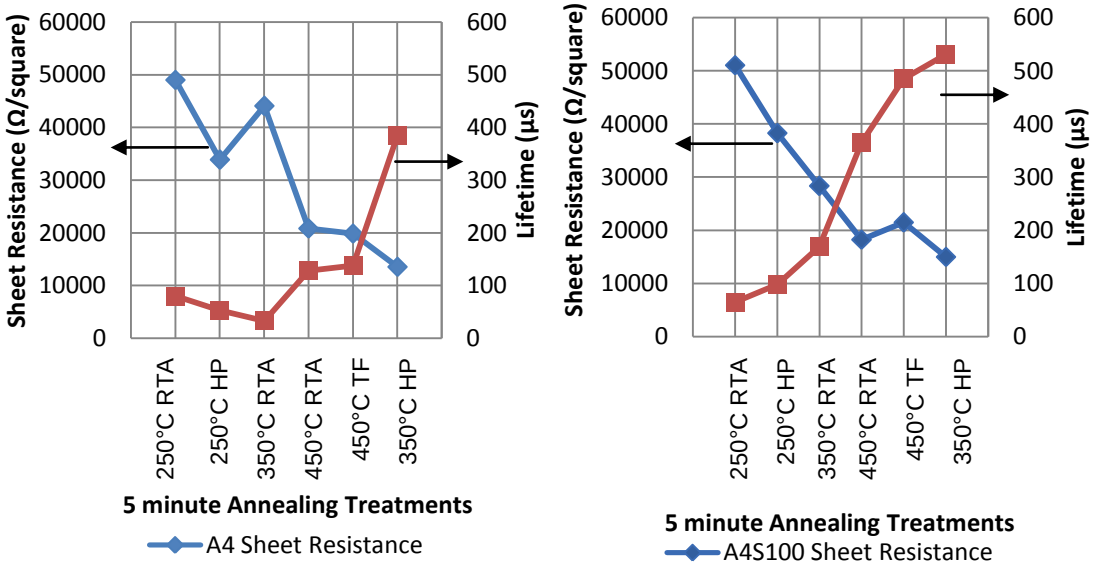


Figure 4-25: Sheet resistance and effective carrier lifetime vs. annealing treatments for 4 nm Al_2O_3 passivated sample and 4 nm Al_2O_3 / 100 nm SiO_x passivated samples.

Sheet resistance of the 4 nm Al_2O_3 passivated samples decreased from 49000 Ω/□, measured on the 250°C RTA annealed sample, to 13600 Ω/□ measured on the 350°C hot plate annealed sample. Sheet resistances of the 4 nm Al_2O_3/100 nm SiO_x passivated samples reached values similar to those of the 4 nm Al_2O_3 passivated samples despite differences in the passivation layer structure. Sheet resistance decreased from 51000 Ω/□ for the 250°C RTA annealed sample, to 15000 Ω/□ for the 350°C hot plate annealed sample. The reduced values in sheet resistance measured for each sample indicates the presence of an inversion layer induced by negative fixed charge in the passivation films.

The graphs in Figure 4-26 show sheet resistance and effective carrier lifetime plotted against annealing treatments for the 7 nm Al_2O_3 passivated samples and the 7 nm Al_2O_3/100 nm SiO_x passivated samples. Again sheet resistance decreased with annealing, and lifetime increased.

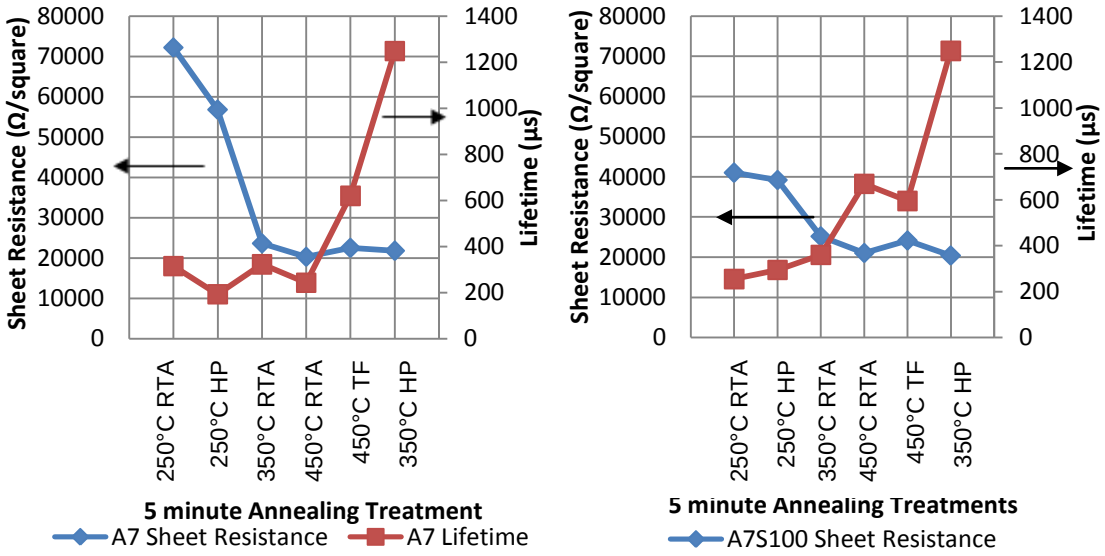


Figure 4-26: Sheet resistance and effective carrier lifetime vs. annealing treatments for 7 nm Al_2O_3 passivated sample and 7 nm Al_2O_3 / 100 nm SiO_x passivated samples.

The sheet resistance of the 7 nm Al_2O_3 passivated samples decreased from 72200 Ω/□, to 21800 Ω/□ with the 5 min 350°C hot plate anneal. The 7 nm Al_2O_3/100 nm SiO_x passivated sample had a much lower initial sheet resistance of 41000 Ω/□ amd decreased to 20400 Ω/□ with the 5 min 350°C hot plate anneal. The reduction in sheet resistance indicates the presence of an inversion layer in the high resistivity silicon induced by negative fixed charge in both the 7 nm Al_2O_3 and the 7 nm Al_2O_3/100 nm SiO_x passivation films.

The graphs in Figure 4-27 show sheet resistance and effective carrier lifetime plotted against annealing treatments for the 10 nm Al_2O_3 passivated samples and the 10 nm Al_2O_3/100 nm SiO_x passivated samples. The trend of sheet resistance decreasing with improved

lifetime and annealing treatment is apparent for the 10 nm Al_2O_3 passivated samples but is not clear for the 10 nm Al_2O_3/100 nm SiO_x passivated samples.

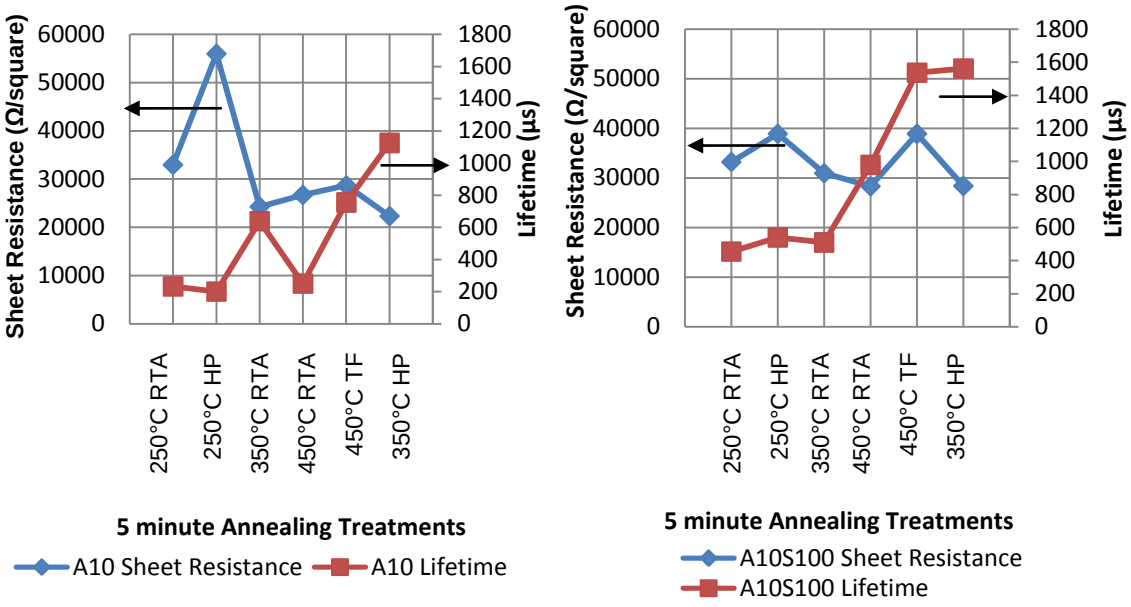


Figure 4-27: Sheet resistance and effective carrier lifetime vs. annealing treatments for 10 nm Al_2O_3 passivated sample and 10 nm Al_2O_3 / 100 nm SiO_x passivated samples.

Sheet resistance of the 10 nm Al_2O_3 passivated samples decreased from 33000 Ω/□, measured for the 250°C RTA annealed sample, to 22400 Ω/□, measured for the 350°C hot plate annealed sample. The reduction in sheet resistance is indicative of an inversion layer in the high resistivity silicon. Sheet resistances of the 10 nm Al_2O_3/100 nm SiO_x passivated samples were relatively stable across the annealing treatments. While sheet resistance was not reduced with annealing, the lifetime does improve significantly (1.5 ms) indicating that passivation of the substrate was achieved. With a value of 33300 Ω/□ for the 250°C RTA annealed sample, and 28400 Ω/□ for the 350°C hot plate annealed sample, the insignificant change in sheet resistance suggests that the passivation maybe afforded by other means. For the 10 nm Al_2O_3/100 nm SiO_x passivated sample the fixed charge in the passivation film does not appear to be large enough to induce an inversion layer.

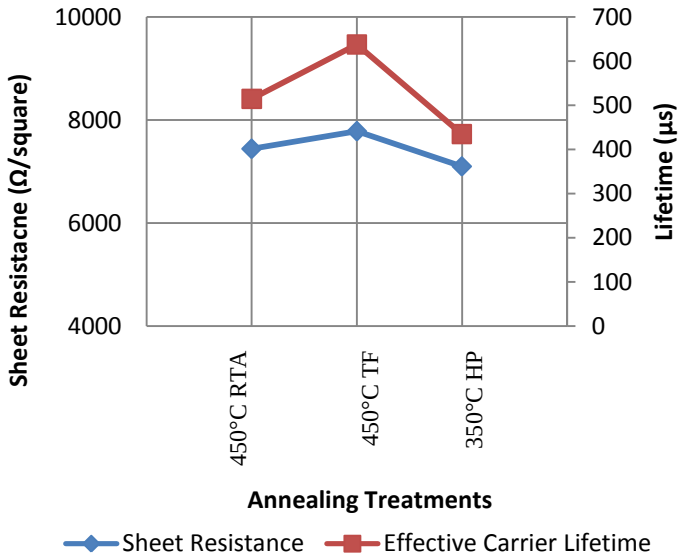


Figure 4-28: Sheet resistance and effective carrier lifetime vs. annealing treatments for samples passivated with the stack structure.

Sheet resistance of the 4 nm Al_2O_3/4 nm SiO_x/7 nm Al_2O_3/50 nm SiO_x passivated sample, in Figure 4-28 did not vary significantly with annealing conditions. The sample was treated with select annealing treatments, the 5 min 450°C RTA anneal, the 5 min 450°C tube furnace anneal, and the 5 min 350°C hot plate anneal. The sheet resistance measured for each annealed sample was on the order of 7000 Ω/□, and the effective carrier lifetimes were on the order of 500 µs. The lowest sheet resistance was 7100 Ω/□, measured for the 350°C hot plate annealed sample, corresponding to a lifetime of 435 µs. It is intersting to note that, while sheet resistances measured on the stack passivated samples were the lowest out of all the samples, the lifetimes achieved were some of the shortest.

Results and Discussion

In the investigation of the presence of an inversion layer induced by fixed charge density, annealing treatments were found to be critical to optimizing film quality, maximizing lifetime,

and reducing sheet resistance. Effective carrier lifetime measurements and C-V measurements were performed to study the effects of the different annealing treatments. The best lifetimes of over 1 ms were generally achived on samples annealed for 5 min at 350°C on the hot plate, and in some cases on samples annealed for 5 min at 450°C in the tube furnace. RTA annealing did not improve film quality to the degree that the hot plate and tube furnace anneals did. The longest lifetimes of 1.5 ms were acheived on the 10 nm Al_2O_3/100 nm SiO_x sample annealed on the hot plate for 5 min at 350°C and in the tube furnace for 5 min at 450°C. Samples passivated with thicker Al_2O_3 layers achieved the longest lifetimes.

C-V measurements were used to calculate fixed charge densities in the films. The largest densities ($-1x10^{13}/cm^2$) were calculated in films that had been annealed for 5 min at 450°C in the tube furnace, and in some cases on samples annealed for 5 min at 350°C on the hot plate. The largest fixed charge density was calculated in the 4nm Al_2O_3 film, but was not significantly greater than those calculated in the 7 nm and 10 nm films. Samples with SiO_x capping layers had reduced fixed charge densities compared to samples without capping layers. Effective carrier lifetime did not correlate to fixed charge density for the samples as some of the longest lifetimes were achieved on samples passivated with Al_2O_3/SiO_x layers, which exhibited reduced negative fixed charge densities.

Sheet resistance measurements were performed to investigate the presence of an inversion layer induced into a high resistivity silicon substrate by negative fixed charge density in the passivation films. It was generally observed that sheet resistance decreased with increasingly effective annealing treatments, and an increased effective lifetime correlated with reduced sheet resistance. The lowest sheet resistance attained was 7100 Ω/□, and was measured on the 4 nm Al_2O_3/4 nm SiO_x/7 nm Al_2O_3/50 nm SiO_x passivated sample annealed at 350°C on the hot plate. Lifetime measured on that sample was 435 μs. The second lowest sheet resistance attained was 13600 Ω/□, was measured on the 4 nm Al_2O_3 passivated sample annealed at 350°C on the hot

plate, which was also found to have the largest fixed charge density. Lifetime measured on that sample was 385 μs. The sheet resistances were not very low, but the reduction in sheet resistance, and longer lifetimes associated with annealing, indicated a field effect induced by the the annealed passivation layers, and the presence of an inversion layer.

Consitent with the works reported in the literature review, we have shown that Al_2O_3 provides passivation of p-type silicon as indicated by long effective carrier lifetimes and C-V mesurements. We achieved negative fixed charge densities similar to those reported by Hoex et al. ($1x10^{13}/cm^2$) and similar lifetimes on the order of a millisecond. Annealing treatments on a hot plate for 5 min at 350°C and for 5 min in a tube furnace at 450°C were suitable for attaining long lifetimes and large fixed charge densities in the Al_2O_3 and Al_2O_3/SiO_x passivation films. In investigating the presence of an inversion layer we have added further evidence for negative fixed charge being the mechanism of passivation of silicon by thin Al_2O_3 films. Additionally, we have shown that HfO_2 films provided suitable passivation of p-type silicon, and further experimentation could prove the films to be a viable alternative to Al_2O_3.

Chapter 5

Conclusions and Future Work

Conclusions

Laser fired contacts (LFCs) and laser doped emitters (LDEs) were prepared, and junction formation was studied using materials and electrical characterization. Additionally, fixed charge passivation of silicon was examined using thin layers of alumina (Al_2O_3) deposited by atomic layer deposited (ALD) with and without a layer of silicon oxide (SiO_x) deposited by plasma enhanced chemical vapor deposited (PECVD).

In Chapter 2 LFCs were further investigated to determine contact geometry and evaluate penetration into the silicon substrate, and I-V curves were simulated to estimate the doping density of Al within the contact. Through a new cross-sectioning and junction delineation technique the LFC was revealed to be nearly hemispherical beneath the surface of the laser fired region for those LFCs fired with the IPG Photonics single mode fiber 1070 nm laser. Selective plating of Au on an n-type substrate with LFCs indicated that the Al metal was incorporated into the once molten region and p-type doping was present to depths greater than 20 µm. LFCs fired with 45 W pulses had larger contact volumes than those fired with 22 W pulses. The corresponding dimensions were approximately 60 µm wide by 28 µm deep (for that fired at 45 W and 4 ms) and 45 µm wide by 21 µm deep (for that fired with 22 W and 19 ms), indicating that power had a large impact on the size and penetration of the LFC melt pool into the substrate. Simulations were used to model LFCs and to recreate the trend apparent in experimental measurements of decreasing resistance for larger diameter contacts. Assuming fixed dopant densities for the LFC region experimental resistances were best matched by LFCs modeled with a

dopant density between $1x10^{18}/cm^3$ and $1x10^{20}/cm^3$, on the order of the solubility limit of aluminum and silicon. Additionally, it was determined that the resistance measured was that of the spreading resistance from the highly doped, laser processed region into the lightly doped p-type substrate.

In Chapter 3 fabrication of LDEs was attempted on silicon wafers deposited with four different passivation and dopant structures. From SEM imaging and I-V measurements, it was apparent that the passivation structures with Sb dopant layers were not suitable due to flaking, delamination, and volatilization of the Sb dopant layer. The passivation layers that incorporated P as a dopant in n+ a-Si:H films were suitable for LDE formation with each laser: the 1070 nm microsecond laser, the 1064 nm 4 ns laser, and the 355 nm 30 ns laser. The 1070 nm laser and 1064 nm lasers successfully doped LDEs for the largest number of conditions tested, and the resulting LDEs exhibited the least ablation and substrate damage. The 355 nm laser was used to successfully form LDEs, but only with select conditions. The LDEs exhibited ablation and drilling, and series resistance was apparent in all of the I-V measurements taken for each sample regardless of passivation structure. Samples passivated with 10 nm a-Si:H/20 nm n+a-Si:H/100 nm SiO_x doped with each laser exhibited LDEs with larger series resistances than samples passivated with 10 nm a-Si:H/100 nm n+a-Si:H. Although the best I-V characteristics were seen in LDEs doped on the 10 nm a-Si:H/100 nm n+a-Si:H passivated samples, a SiO_x layer would be required for LFE metallization. The SiO_x layer would ensure that an insulating barrier layer existed between the conducting a-Si:H on the substrate and the deposited metal. LDEs doped with the 1070 nm and 1064 nm lasers showed the most promise. Those fabricated with the 1070 nm laser exhibited deeply doped regions evident in cross-sectioning and junction delineation, to depths of 11 µm (100 W, 100 µs pulse), confirming the successful creation of an LDEs and incorporation of the phosphorus dopant.

In Chapter 4 fixed charge passivation was demonstrated with Al_2O_3 and Al_2O_3/SiO_x passivated samples, annealed under appropriate conditions, on p-type silicon wafers. Experiments were performed to assess the density of fixed charge in Al_2O_3 layers, determine the best annealing treatments to maximize fixed charge, and improve film quality to achieve the longest lifetimes. In the initial investigation of the impact of film thickness on fixed charge density, it was demonstrated that fixed charge is maximized in thinner films of Al_2O_3 and is reduced as films increase in thickness. Al_2O_3 and HfO_2 films were studied ranging in thickness from 8 to 35 nm and 9 to 38 nm, respectively. Samples were subjected to 5 min vacuum chuck/hot plate annealing treatments at 250°C and 350°C, and generally improved with higher temperature annealing. In the thinner samples annealed at 350°C for 5 min, long lifetimes, over 1 ms, were attained by fixed charge passivation (8 to 12 nm), as thinner films had the largest fixed charge densities. Despite reduced fixed charge densities in the thicker passivation films, long lifetimes (> 1 ms) were measured as well, indicating suitable passivation by a means other than fixed charge passivation. While investigating the presence of fixed charge at interfaces in SiO_x capped Al_2O_3 samples, it was discovered that deposition of SiO_x reduced fixed charge in the passivation layer, but passivation quality was maintained with suitable annealing treatment and even improved over the course of weeks and months. Fabricated through a combination of ALD and PEVCD, Al_2O_3/SiO_x passivated samples were subjected to 5 min vacuum chuck/hot plate annealing treatments at 250°C and 350°C, and measured for lifetime and V_{FB} shifts. The longest lifetime achieved in the experiment was 1.5 ms, on a 10 nm Al_2O_3/100 nm SiO_x passivated film annealed at 350°C on a hot plate for 5 min. Samples prepared on high resistivity ($\rho \geq 10000$ Ω-cm) silicon wafers exhibited a reduction in sheet resistance that correlated to an increase in effective carrier lifetime, which often increased with annealing. The reduction in sheet resistance was most apparent in thin Al_2O_3 passivation layers, which were found to contain the most fixed charge. The physical mechanism responsible for reduction in sheet resistance is

the creation of an inversion layer in the high resistivity (nominally n-type) substrate, due to the presence of fixed negative charge. The repulsion of negative charge carriers from the surface reduces recombination. In a p-type sample, minority carriers are shielded by the creation of an accumulation layer near the surface of the silicon. The fixed charge in the Al_2O_3 contributed to passivation of the silicon substrate and improved both effective carrier lifetime and sheet resistance.

Future Work

Throughout the experiments performed it was apparent that additional studies would be valuable to completely evaluate the fabrication of LDEs for use in solar cells. Further refinement of the passivation/dopant structure would be useful in order to perform doping at lower laser powers and create shallower emitters. Additionally, a structure with suitable dopant layer thickness with a top SiO_x barrier layer will be required to ensure successful metallization of the LDEs. Sputter deposition of thinner nickel films has been highlighted as a useful technique for future LDE metallization. A selective electroplating technique could also serve as a useful method for device metallization. The use of a green 532 nm nanosecond laser would be interesting to study in comparison to those lasers previously examined.

Future investigation into fixed charge passivation would be of interest on additional HfO_2 passivation layers and multi-stack passivation structures. Examination and optimization of HfO_2 passivation films could prove the material to be an alternative passivation film to Al_2O_3. Alternate stack structures incorporating more layers of thin Al_2O_3 in between SiO_x layers would be of interest in studying maximum fixed charge density attainable. Having studied only one stacked structure, comparison of others would be valuable to determine if reduction of fixed

charge in a multi-layer stack was a typical result. The ability to deposit Al_2O_3 and SiO_x in the same system would also be advantageous for passivation of future samples.

As the project continues, work on LDEs will continue with the goal of fabricating diagnostic cells. Ideally the structure will incorporate fixed charge passivation, LDEs, and LFCs in a fully laser processed cell with high efficiency.

Bibliography

1. Chapin DM, Fuller CS, Pearson GL. A new silicon p-n junction photocell for converting solar radiation into electrical power. J Appl Phys 1954;25(5):676-7.
2. Muller K, Borges R. Simulation in photovoltaics: From solar cells to full-scale arrays. Solar Industry Magazine 2010;1(10).
3. Fonash SJ. Solar cell device physics. 2nd ed. Burlington, MA: Academic Press/Elsevier; 2010.
4. Kasap SO, Capper P, editors. Springer handbook of electronic and photonic materials. New York, NY: Springer; 2006.
5. Kerschaver EV, Beaucarne G. Back-contact solar cells: A review. Prog Photovoltaics Res Appl 2006;14(2):107-23.
6. Eisele SJ, Roder TC, Kohler JR, Werner JH. 18.9% efficient full area laser doped silicon solar cell. Appl Phys Lette 2009;95(13):133501.
7. PV CDROM [Internet]; Available at http://pveducation.org/pvcdrom. [cited January 2011].
8. Ogane A, Hirata K, Horiuchi K, Nishihara Y, Takahashi Y, Kitiyanan A, Fuyuki T. Laser-doping technique using ultraviolet laser for shallow doping in crystalline silicon solar cell fabrication. Jpn J Appl Phys 2009;48(7):071201.
9. Glunz SW. New concepts for high-efficiency silicon solar cells. Solar Energy Mater Solar Cells 2006;90(18-19):3276-84.
10. Colville F. Laser-assisted selective emitters and the role of laser doping. Photovoltaics International [Internet]. Available from http://legacy.pv-tech.org/technical_papers/browse/_c/edition_5/P0/.
11. Kray D, McIntosh KR. Analysis of selective phosphorous laser doping in high-efficiency solar cells. IEEE Transactions on Electron Devices 2009;56(8):1645-50.

12. Hilali MM, Rohatgi A, To B. A review and understanding of screen-printed contacts and Selective–Emitter formation. 14th Workshop on Crystalline Silicon Solar Cells and Modules. Winter Park, Colorado; August 2004.
13. von Roos O. A simple theory of back-surface-field (BSF) solar cells. J Appl Phys 1979;50(8):5371-4.
14. Hofmann M, Janz S, Schmidt C, Kambor S, Suwito D, Kohn N, Rentsch J, Preu R, Glunz SW. Recent developments in rear-surface passivation at fraunhofer ISE. Solar Energy Mater Solar Cells 2009;93(6-7):1074-8.
15. Hoex B, Heil SBS, Langereis E, van de Sanden MCM, Kessels WMM. Ultralow surface recombination of c-si substrates passivated by plasma-assisted atomic layer deposited Al_2O_3. Appl Phys Lett 2006;89(4):042112.
16. Suwito D, Jäger U, Benick J, Janz S, Hermle M, Glunz SW. Industrially feasible rear passivation and contacting scheme for high-efficiency n-type solar cells yielding a of 700 mV. IEEE Transactions on Electron Devices 2010;57(8):2032-6.
17. Janz S, Riepe S, Hofmann M, Reber S, Glunz S. Phosphorus-doped SiC as an excellent p-type si surface passivation layer. Appl Phys Lett 2006;88(13):133516.
18. Hoex B, Schmidt J, Bock R, Altermatt PP, van de Sanden MCM, Kessels WMM. Excellent passivation of highly doped p-type si surfaces by the negative-charge-dielectric Al_2O_3. Appl Phys Lett 2007;91(11):112107.
19. Schmidt J, Merkle A, Brendel R, Hoex B, de Sanden MCMv, Kessels WMM. Surface passivation of high-efficiency silicon solar cells by atomic-layer-deposited Al2O3. Prog Photovoltaics Res Appl 2008;16(6):461-6.
20. Saint-Cast P, Benick J, Kania D, Weiss L, Hofmann M, Rentsch J, Preu R, Glunz SW. High-efficiency c-si solar cells passivated with ALD and PECVD aluminum oxide. IEEE Electron Device Letters 2010;31(7):695-7.

21. Maruyama E, Terakawa A, Taguchi M, Yoshimine Y, Ide D, Baba T, Shima M, Sakata H, Tanaka M. Sanyo's challenges to the development of high-efficiency HIT solar cells and the expansion of HIT business. Conference record of the IEEE 4th World Conference on Photovoltaic Energy Conversion; 2006; (2): 1455-60.
22. Grohe A, Schneiderlochner E, Hermle M, Preu R, Glunz SW, Willeke G, Walz S.Characterization of laser-fired contacts processed on wafers with different resistivity. Proceedings of the 3rd World Conference on Photovoltaic energy conversion 2003;(2):1032-5.
23. Zastrow U, Houben L, Meertens D, Grohe A, Brammer T, Schneiderlöchner E. Characterization of laser-fired contacts in PERC solar cells: SIMS and TEM analysis applying advanced preparation techniques. Appl Surf Sci 2006;252(19):7082-5.
24. Schneiderlöchner E, Preu R, Lüdemann R, Glunz SW. Laser-fired rear contacts for crystalline silicon solar cells. Prog Photovoltaics Res Appl 2002;10(1):29-34.
25. Zhao J, Wang A, Altermatt PP, Wenham SR, Green MA. 24% efficient perl silicon solar cell: Recent improvements in high efficiency silicon cell research. Solar Energy Mater Solar Cells 1996;41-42:87-99.
26. Brendle W, Nguyen VX, Grohe A, Schneiderlöchner E, Rau U, Palfinger G, Werner JH. 20·5% efficient silicon solar cell with a low temperature rear side process using laser-fired contacts. Prog Photovoltaics Res Appl 2006;14(7):653-62.
27. DeCesar B. Investigation of process parameter optimization of laser-fired back contact silicon solar cells. The Pennsylvania State University Graduate School 2010.
28. Ametowobla M, Kohler JR, Esturo-Breton A, Werner JH. Improved laser doping for silicon solar cells. 22nd European Photovoltaic Solar Energy Conference. Milan, Italy; September 2007.

29. Tucci M, Talgorn E, Serenelli L, Salza E, Izzi M, Mangiapane P. Laser fired back contact for silicon solar cells. Thin Solid Films 2008;516(20):6767-70.

30. Preu R, Schneiderlochner E, Grohe A, Glunz SW, Willeke G. Laser-fired contacts - transfer of a simple high efficiency process scheme to industrial production. Conference Record of the Twenty-Ninth IEEE Photovoltaic Specialists Conference; 2002. 130-3.

31. Schultz O, Glunz SW, Willeke GP. Multicrystalline silicon solar cells exceeding 20% efficiency. Prog Photovoltaics Res Appl 2004;12(7):553-8.

32. Kray D, Glunz S. Investigation of laser-fired rear-side recombination properties using an analytical model. Prog Photovoltaics Res Appl 2006;14(3):195-201.

33. Synopsys Inc. TCAD Sentaurus Device User's Manual [computer program]. Mountain View, CA: 2007.

34. Eichfeld CM, Wood C, Liu B, Eichfeld SM, Redwing JM, Mohney SE. Selective plating for junction delineation in silicon nanowires. Nano Letters 2007;7(9):2642-4.

35. Trumbore FA. Solid solubilities of impurity elements in germanium and silicon. Bell Syst Tech J 1960;39:205-33.

36. Krause O, Ryssel H, Pichler P. Determination of aluminum diffusion parameters in silicon. J Appl Phys 2002;91(9):5645-9.

37. Ke Y, Weng X, Redwing JM, Eichfeld CM, Swisher TR, Mohney SE, Habib YM. Fabrication and electrical properties of si nanowires synthesized by al catalyzed vapor-liquid-solid growth. Nano Letters 2009;9(12):4494-9.

38. Civale Y, Nanver LK, Schellevis H. Selective solid-phase silicon epitaxy of p^+ aluminum-doped contacts for nanoscale devices. IEEE Transactions on Nanotechnology 2007;6(2):196-200.

39. Civale Y, Nanver LK, Alberici SG, Gammon A, Kelly I. Accurate SIMS doping profiling of aluminum-doped solid-phase epitaxy silicon islands. Electrochem Solid-State Lett 2008;11(4):H74-6.

40. Hara T, Suzuki H, Furukawa M, Amemiya K. Contact resistance of Al/Si ohmic electrodes formed by rapid lamp sintering. Jpn J Appl Phys 1983;22(Part 2, No. 6):L340-2.

41. Schwartz GC, editor. Handbook of semiconductor interconnection technology. 2nd ed. CRC Press; 2006. 167.

42. Hameiri Z, Mai L, Puzzer T, Wenham SR. Influence of laser power on the properties of laser doped solar cells. Solar Energy Mater Solar Cells 2011 4;95(4):1085-94.

43. Röder T, Esturo-Breton A, Eisele S, Wagner C, Köhler JR, Werner JH. Fill factor of laser doped textured silicon solar cells. 23rd European Photovoltaic Solar Energy Conference and Exhibition. Valencia, Spain; September 2008; 1740-2.

44. Esturo-Breton A, Ametowobla M, Köhler JR, Werner J H. Laser doping for crystalline silicon solar cell emitters. Proc. 20th European Photovoltaic Solar Energy Conference. Munich, Germany; 2005; 851-4.

45. Köhler JR, Eisele S. Influence of precursor layer ablation on laser doping of silicon. Prog Photovoltaics Res Appl 2010;18(5):334-9.

46. Glunz SW, Mette A, Alemán M, Richter PL, Filipovic A, Willeke G. New concepts for the front side metallization of silicon solar cells. 21st European Photovoltaic Solar Energy Conference and Exhibition. Dresden, Germany; 2006.

47. Drew K, Hopman S, Hörteis M, Glunz SW, Granek F. Combining laser chemical processing and aerosol jet printing: A laboratory scale feasibility study. Prog Photovoltaics Res Appl 2011;19(3):253-9.

48. Wenham SR, Green MA, inventors. Self aligning method for forming a selective emitter and metallization in a solar cell - Patent 6429037. August 6, 2002.

49. Tian Z, Salama IA, Quick NR, Kar A. Effects of different laser sources and doping methods used to dope silicon carbide. Acta Materialia 2005;53(9):2835-44.

50. Schroder D. Semiconductor material and device characterization. 3rd ed. Hoboken, NJ: Wiley-Interscience;2006.

51. Schultz O, Glunz SW, Warta W, Preu R, Grohe A, Köber M, Willeke GP, Russel R, Fernandez J, Morilla C, Bueno R, Vincuería I. High-efficiency solar cells with laser-grooved buried contact front and laser-fired rear for industrial production. 21st European Photovoltaic Solar Energy Conference. Dresden, Germany; September 2006 .

52. Benick J, Richter A, Hermle M, Glunz SW. Thermal stability of the Al_2O_3 passivation on p-type silicon surfaces for solar cell applications. Physica Status Solidi:Rapid Research Letters 2009;3(7-8):233-5.

53. Dauwe S, Schmidt J, Hezel R. Very low surface recombination velocities on p- and n-type silicon wafers passivated with hydrogenated amorphous silicon films. Conference Record of the Twenty-Ninth IEEE Photovoltaic specialists conference 2002; 1246-9.

54. Kerr MJ, Cuevas A. Very low bulk and surface recombination in oxidized silicon wafers. Semicond Sci Technol 2002;17(1):35-8.

55. Widjaja Y, Musgrave CB. Quantum chemical study of the mechanism of aluminum oxide atomic layer deposition. Applied Physics Letters 2002;80(18):3304-6.

56. Benick J, Hoex B, van de Sanden MCM, Kessels WMM, Schultz O, Glunz SW. High efficiency n-type Si solar cells on Al_2O_3-passivated boron emitters. Applied Physics Letters 2008; 92(25):253504-3.

57. Schmidt J, Veith B, Brendel R. Effective surface passivation of crystalline silicon using ultrathin Al2O3 films and Al_2O_3/SiN_x stacks. Physica Status Solidi: Rapid Research Letters 2009;3(9):287-9.

58. Wang J, Farokh-Baroughi M, Shanmugam M, Samadzadeh-Tarighat R, Sivoththaman S, Paul S. Passivation of silicon surfaces using atomic layer deposited metal oxides. Materials Research Society Symposium Proceedings 2009; 1153 (A07-17).

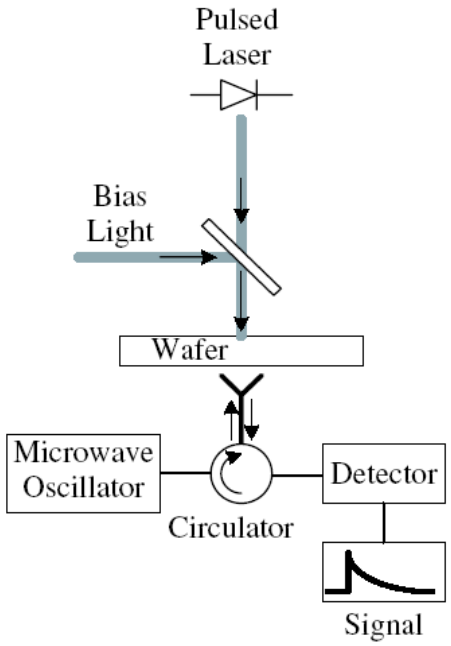
59. Poodt P, Lankhorst A, Roozeboom F, Tiba V, Spee K, Maas D, Vermeer A, Elam J, Bent S, De Gendt S, Delabie A, Londergan A, Roozeboom F, Van der Straten O. Atomic layer deposition of alumina layers for solar cell passivation. Meet. Abstr. - Electrochem. Soc. 2010;1002(20): 1438.

60. König D, Rennau M, Henker M, Ebest G. Evidence of a high density of fixed negative charges in an insulation layer compound on silicon. Thin Solid Films 2001;385(1-2):126-31.

Appendix A

Effective Carrier Lifetime Measurements

The basic μ-PCD system set up in our lab consists of a UV LED, modulated by an Agilent 8114A Pulse Generator, used to illuminate a sample whose effective carrier lifetime decay is sensed by an antenna connected to an Anritsu MA2473D Microwave Sensor and an Anritsu ML2488A Power Meter, which measure the signal and interface with the computer to capture it. The Microwave Oscillator/Detector is controlled with an HP 8350B Sweep Oscillator. A schematic of the setup is shown in the image below (50).



Measurement Proceedure

1. Log into the 2B Steidle account on the computer. Password: xxxxxxxxx
2. Open the folder C:\Documents and Settings\2B Steidle\Desktop\ML248XA_V2
    a. The folder is on the desktop, labled ML248XA_V2

3. The program required later in step 9 is titled fileselect, do not open it at this time
4. Turn on the Agilent 8114A Pulse generator
    a. Push the large white square button on the lower left front to do so
5. Turn on the hp 8305B Sweep Oscillator
    a. Flip the white switch on the lower left front labeled “LINE” to do so
    b. Set the Frequency to continuous wave by pressing the “CW” button
        i. It is the second button from the left, in between “START” and “CF” on the frequency panel
6. Turn on the Anritsu ML2488A Power Meter
    a. Press the white ellipse shaped button on the lower left front labeled “On/Standby” to do so
7. Set up the Agilent pulse generator to produce the signal that will power the UVLED. **Note:** The pulse parameters will need to be altered based on your samples.
    a. To start, set the Period to 500 µs
        i. Use the cursor arrows to navigate on the screen, so that the value next to “Per” is highlighted.
            1. It will be in the upper left most part of the screen. If it says “Freq” instead of “Per”, highlight “Freq” and adjust the knob labled “Modify” until “Per” appears
        ii. Change the value to 500 µs by pressing the buttons “5” “0” “0” “micro” on the DATA ENTRY key pad
    b. Set the Delay to 0.00 ns
        i. Use the cursor arrows to navigate on the screen, so that the value next to “Delay” is highlighted.

1. “Delay” is listed directly underneath “Per” on the screen. If it says “Delay%” or “Phase” instead of “Delay”, highlight the label and adjust the “Modify” knob until “Delay” appears

ii. Change the value to 0.00 ns by pressing the buttons “0” “.” “0” “0” “nano” on the DATA ENTRY key pad. It should be set to this value already.

c. Set the Width to 150 µs

i. Use the cursor arrows to navigate on the screen, so that the value next to “Width” is highlighted.

1. “Width” is listed directly underneath “Delay” on the screen. If it says “DutyCycle” or “TrialDel” instead of “Width”, highlight the label and adjust the “Modify” knob until “Width” appears

ii. Change the value to 150 µs by pressing the buttons “1” “5” “0” “micro” on the DATA ENTRY key pad.

d. Set the “50Ω into” value to 2 Ω

i. Use the cursor arrows to navigate on the screen, so that the value next to “50Ω into” is highlighted.

1. “50Ω into” is listed directly underneath “Width” on the screen. If it says “HIZ” instead of “50Ω into”, highlight the label and adjust the “Modify” knob until “50Ω into” appears

ii. Change the value to 2 Ω by pressing the buttons “2” “ENTER” on the DATA ENTRY key pad. You may have to come back and reset this to another value depending on the signal.

e. Let the output “Out” switched to OFF until the remaining settings are selected

f. “Inh” should be OFF and the signal should be rising

g. Set the baseline “Baselne” to 0 V and the amplitude “Amplitd” to 2 V

i. Use the cursor arrows to navigate on the screen, so that the value next to “Baselne” is highlighted.

1. “Baselne” and “Amplitd” are listed directly underneath “Inh” on the screen, to the right of “Delay” and “Width”. If it says “High” and “Low” instead highlight the labels and adjust the “Modify” knob until “Baselne” and “Amplitd” appear

ii. Change the “Baselne” value to 0 V by pressing the buttons “0” “ENTER” on the DATA ENTRY key pad. You may have adjust the units to V by highlighting them and using the “modify” knob.

Change the “Amplitd” value to 2 V by pressing the buttons “2” “ENTER” on the DATA ENTRY key pad. You may have adjust the units to V by highlighting them and using the “Modify” knob.

Note: If an error message is displayed, navigate to the “LIMITS” menu by selecting the grey square key under the “LIMITS” tab on the screen. Adjust the “Lev-Limits” of “High-V” , “Low-V”, “High-A” , and “Low-A” in the range of + 2V, -2V, +300mA, -300mA, respectfully, or in the range where the error is alleviated.

h. Set the shape of the pulse to be “Positive”

i. Use the cursor arrows to navigate on the screen, so that the shape is hightlighed

1. The shape value is located directly under “Amplitd”

ii. Use the “Modify” knob so that a positive shape is displayed and the label “Positive” apears

8. Set up the Anritsu ML2488A Power Meter

a. Select the grey button next to the “More” tab on the screen, located on the bottom right.
b. Select the grey button next to the “Scaling” tab on the screen, located second from the top.
c. Select the grey button next to the “Autoscale” tab on the screen, located third from the top.
    i. A line should now be present on the screen, and it should wiggle. If it is jumping around and is not a line, make sure the Sweep Oscillator is set to “CW”.
d. Select the grey button labeled “Channel” to navigate back to the main screen.
e. Select the grey button next to the “Trigger” tab on the screen, second from the top on the right.
f. Select the grey button next to “Set Cap Time…” on the screen located second from the top on the right.
g. Set the Capture time to match the “Per” value set on the Pulse generator.

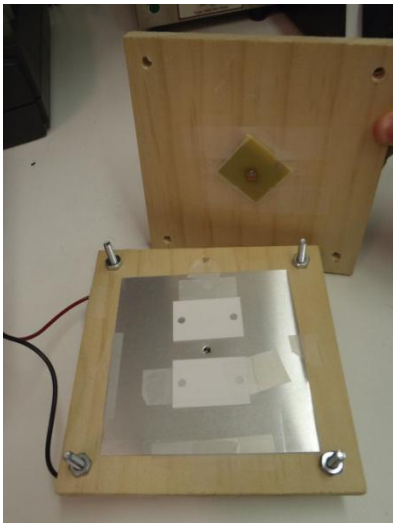
    Note: THIS IS EXTREMELY IMPORTANT AND WILL AFFECT YOUR MEASUREMENT UNITS. IF NOT CORRECT YOU WILL BE REPORTING FALSE VALUES.

    i. First hit “Sel” on the key pad followed by “5” “0” “0”
    ii. Set the units to μs by pressing the grey button on the right next to the “μs” tab on the screen, it should be second from the top.
h. Select the “Channel” button to navigate back to the main screen.

Note: at any time during the measurement you may have to go in and select “Autoscale” to view the waveform on the Power Meter screen. Refer to step 8a-

8d. Additionally if you change the period output by the Pulse Generator change the value on the Power Meter and restart the measurement. Refer to step 8e-8h.

9. Remove the top panel of the measurement fixture, and place a sample above the LED on the test stand, and replace the top panel, which houses the microwave antenna, on top of it. Adjust the spacers (the nuts on the screw feet) so that the antenna is nearly touching the surface.



10. Now turn the output of the Agilent Pulse Generator to "ON"
    a. Use the cursor arrows to navigate to "Out" and use the "Modify" knob to switch the output from "OFF" to "ON"
11. Autoscale the screen on the Anritsu Power Meter
    a. Select the grey button next to the "More" tab on the screen, located on the bottom right.
    b. Select the grey button next to the "Scaling" tab on the screen, located second from the top.
    c. Select the grey button next to the "Autoscale" tab on the screen, located third from the top. A waveform should be present if there is any carrier decay being

measured. You will now need to adjust the period "Per" on the Pulse Generator and the "Set Capture Time" on the Power Meter, to get the cleanest signal. You may also have to adjust the "50Ω into" resistance value.

12. Adjust the "Per" on the Pulse Generator and the "Set Capture Time" on the Power Meter, to get the cleanest signal. If the wave form does not decay to zero before the next pulse starts you will need to lengthen the period and capture time
    a. On the Pulse Generator increase the Period to 1000 µs (or whatever period you desire)
        i. Use the cursor arrows to navigate on the screen, so that the value next to "Per" is highlighted.
        ii. Change the value to 1000 µs by pressing the buttons "1" "0" "0" "0" "micro" on the DATA ENTRY key pad
    b. On the Power Meter change the "Set Capture Time" to match the period of the Pulse generator
        i. Select the grey button labeled "Channel" if needed to navigate back to the main screen.
        ii. Select the grey button next to the "Trigger" tab on the screen, second from the top on the right.
        iii. Select the grey button next to "Set Cap Time…" on the screen located second from the top on the right.
        iv. Set the Capture time to match the "Per" value set on the Pulse generator.

            Note: THIS IS EXTREMELY IMPORTANT AND WILL AFFECT YOUR MEASUREMENT UNITS. IF NOT CORRECT YOU WILL BE REPORTING FALSE VALUES.

v. First hit “Sel” on the key pad followed by “1” “0” “0” “0” (or whatever the period value is set to on the Pulse Generator)

vi. Set the units to µs by pressing the grey button on the right next to the “µs” tab on the screen, it should be second from the top. (set the value to match the Pulse Generator period)

c. Select the “Channel” button to navigate back to the main screen. You may want to autoscale the waveform is needed.

d. Continue adjusting the period and capture time on each tool until the decay signal is not overlapping. Once it is clean and clearly decays to zero before the start of the next signal you can capture the signal using the computer software.

13. Capture the image on the Power Meter Software

a. Open the fileselect application in the folder C:\Documents and Settings\2B Steidle\Desktop\ML248XA_V2

b. In the left hand menu select “ML248XA Application Programs”

i. In sub menu that appears select “Power Meter”

c. In the following window that opens select “Load from Power Meter”

Note: if an error window reports that the software cannot read the Power Meter or it is not connected, make sure that the meter is connected by the GPIB-USB-PS data line (it is a big blue connection), at the rear to both the computer and Pulse Generator.

i. A window will open that looks like the screen of the power meter. Nothing will be happening on either screen at this point.

d. MAKE SURE THE VALUE IN THE LOWER RIGHT CORNER OF THE WINDOW REFLECTS THE VALUE OF THE PERIOD ON THE PULSE GENERATOR.

i. If it does not, close the window and set the capture time on the Power Meter to the correct value

e. Given that the capture time value is correct, go to the PulseMod menu at the top of the window and select Start.

i. If the waveform does not appear on the computer screen, close the window, autoscale the signal on the power meter and load from the power meter again.

1. In the left hand menu select “ML248XA Application Programs”. In sub menu that appears select “Power Meter”
2. In the following window that opens select “Load from Power Meter”

ii. If the wave form does appear you now fine tune the frequency and power of the Sweep Oscillator and the “50Ω into” value on the Pulse Generator to get the best signal

1. On the Sweep Oscillator:
    a. Increase the frequency by adjusting the knob above the “CW” button, on the left panel, labeled “Frequency”
    b. Adjust the power up and down, to center the waveform on the screen, by adjusting the knob on the far right panel, labeled “Power”
2. On the Pulse Generator:
    a. Chance the resistance of the “50Ω into” value to 2 Ω or some other value, until the signal looks good.

f. Once you have a clean signal capture the full shape of it in the window.

i. Hit the “File” menu at the appropriate moment to freeze the signal and then select to “Save”

ii. Save the file in an appropriate folder with a consistent naming scheme for each sample measured. This will make it easier for the Excel Macro to evaluate the data all at one time. Consider having all your files start with the same number or letter, and save them all in the same folder.

14. Measure additional samples and save data.
15. Turn off all equipment
16. Analyze data
    a. Open Microsoft Excel and open the file “Lifetime macro” located in the folder C:\Documents and Settings\Flemish\Desktop\Flemish PCD\Lifetime Code
    b. One open click any cell and enter the keystrokes Alt and F8 to edit the code
        i. Select “Open_file” and click the “Edit” button
        ii. In the region that says ‘Enter the directory path where the files of interest are: Directory = “ C:\...” ’ enter the file location where you saved your files to be analyzed
        iii. Return to the main spread sheet once you have edited the code
    c. Enter the first letter of your file’s name in the E1 cell next to the cell with “filename=”
    d. Select Alt and F8 again and select “Open_files” and then click the “Run” button
        i. A window will report the number of files in that folder with that filename, click “OK”
        ii. Your files will open into one large workbook, select the leftmost tab in that spreadsheet

e. Select Alt and F8 again and select " 'Lifetime macro.xls'!AddSummarySheet" and click "Run"
    i. A summary sheet will be added to the workbook
    ii. Go back to your first file tab to the right of the summary sheet
f. Select Alt and F8 again and select 'Lifetime macro.xls'!Analyze" and click "Run"
    i. The Macro will run and typically ends with a Run-time error. Simply select the "End" button
    ii. In the Summary tab of the workbook each calculated lifetime value will be reported for each sample
g. Save the summary or rename it according to the samples you have measured

17. Log off the computer but do not shut it down.

Appendix B

C-V Measurements on n-Type Wafers

All samples were annealed for 5 min in ambient air. The 250°C anneal was performed on a vacuum chuck and the 350°C anneal was performed on a hot plate. The wafers were n-type 0.5-1 Ω-cm FZ silicon wafers (100) silicon.

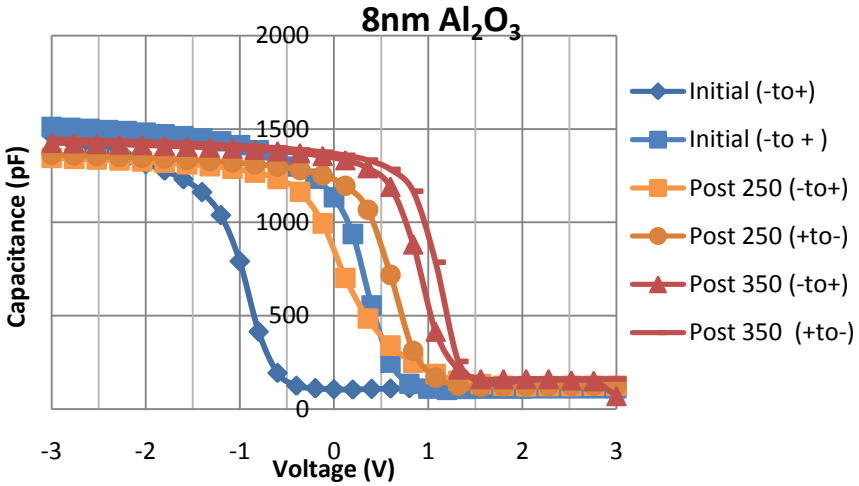


Figure B-1: C-V measurements of the 8 nm Al_2O_3 passivated sample

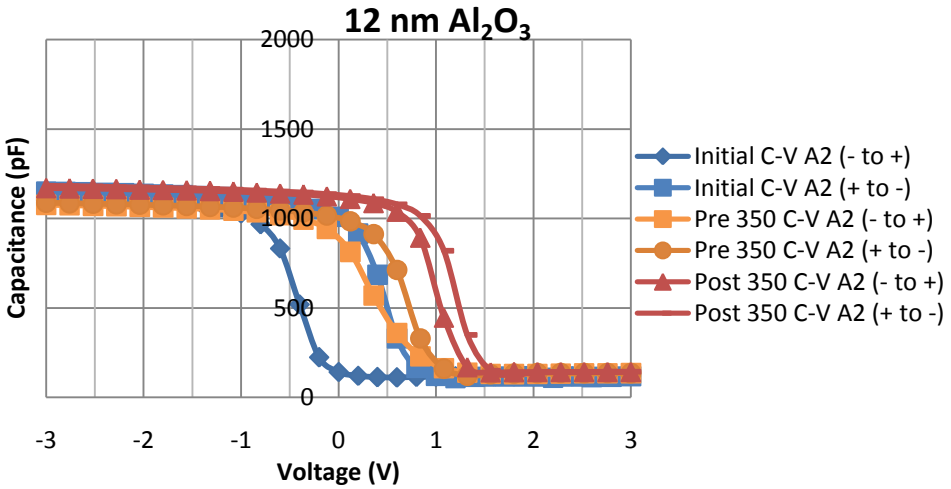


Figure B-2: C-V measurements of the 12 nm Al_2O_3 passivated sample

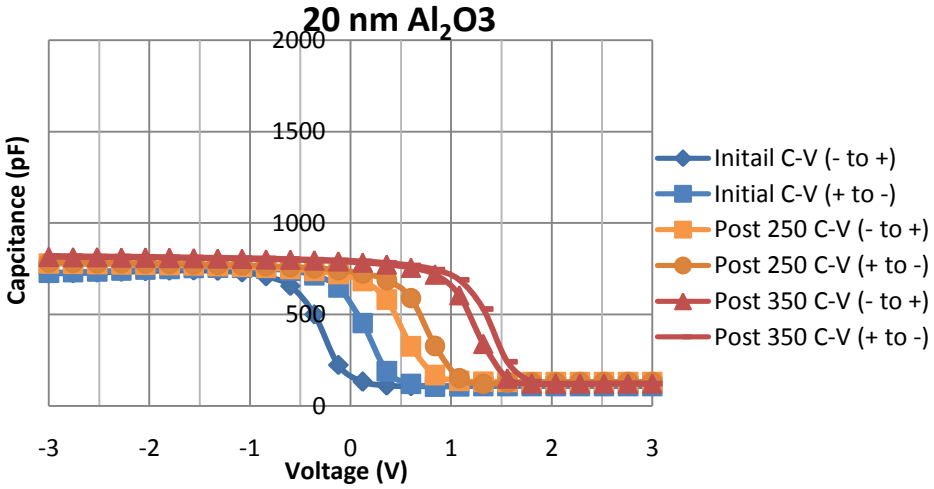


Figure B-3: C-V measurements of the 20 nm Al_2O_3 passivated sample

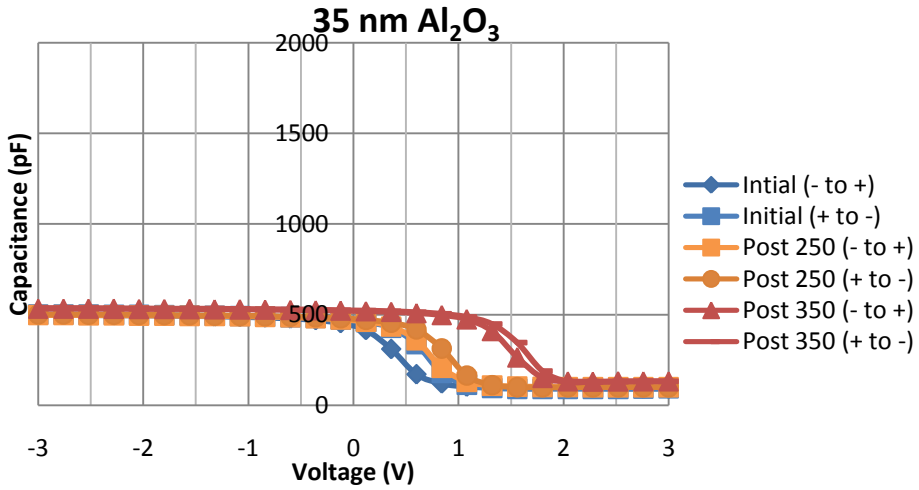


Figure B-4: C-V measurements of the 35 nm Al_2O_3 passivated sample

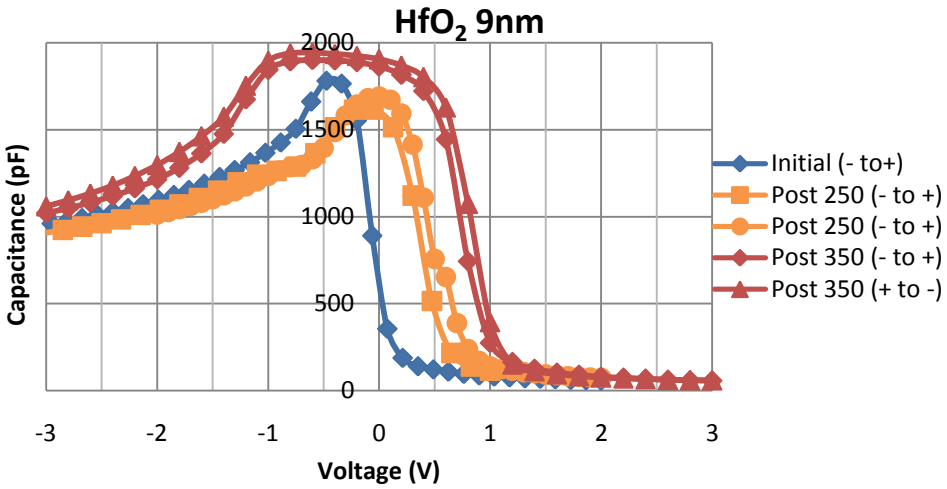


Figure B-5: C-V measurements of the 9 nm HfO_2 passivated sample

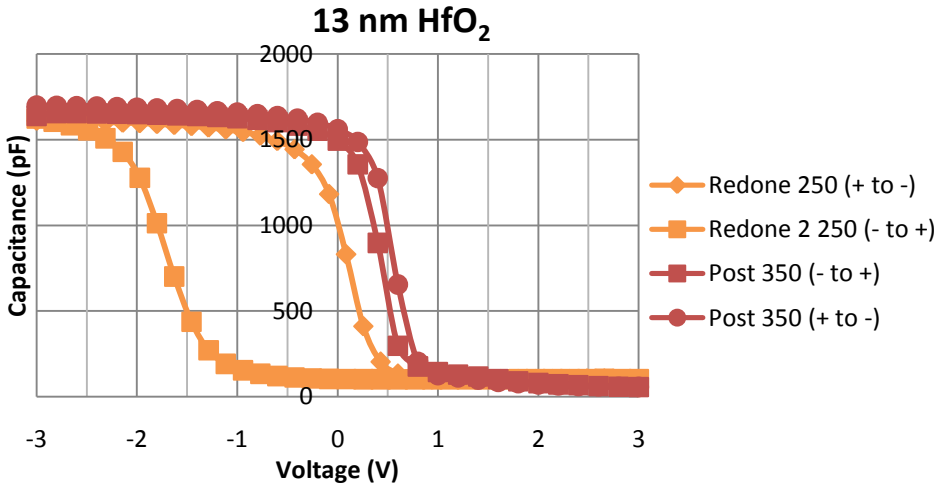


Figure B-6: C-V measurements of the 13 nm HfO_2 passivated sample

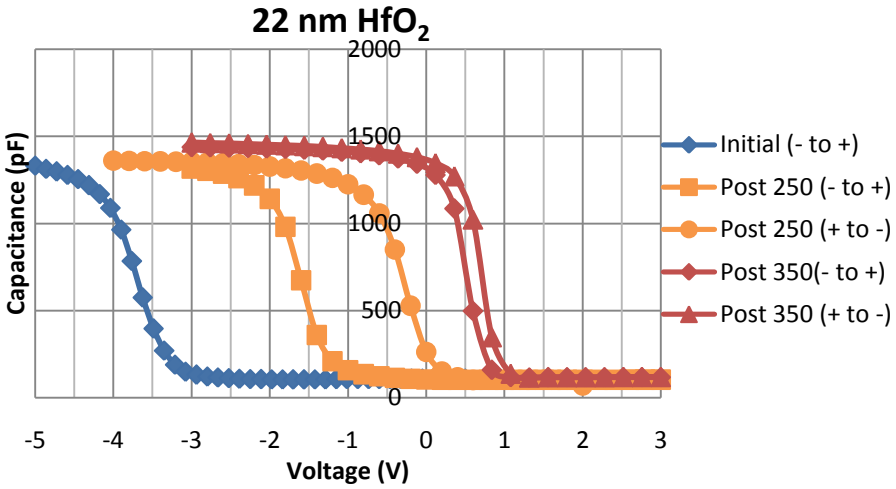
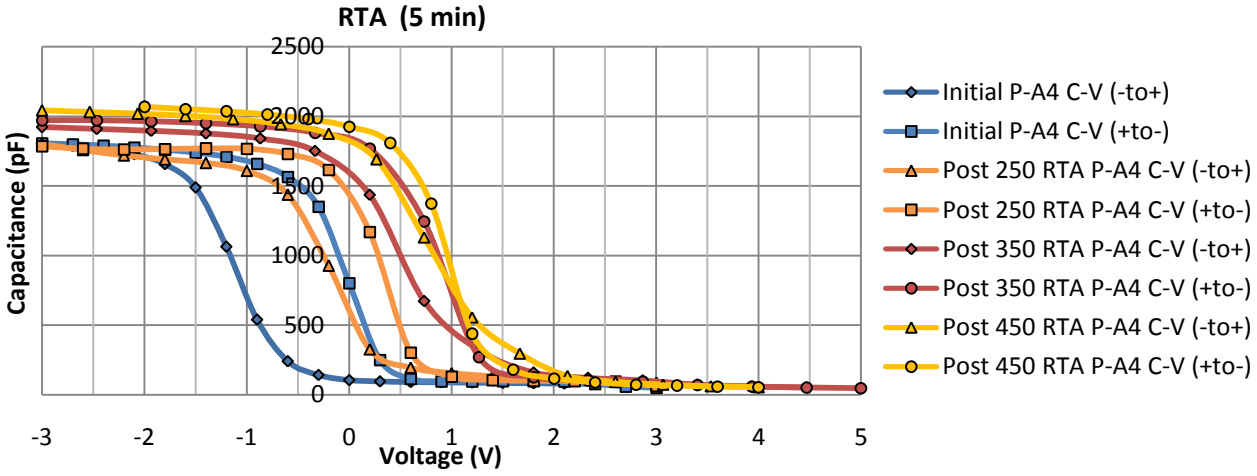


Figure B-7: C-V measurements of the 22 nm HfO_2 passivated sample

Appendix C

C-V Measurements from the Inversion Layer Experiment

Samples were annealed at temperatures of 250°C, 350°C, and 450°C for 5 min. The 250°C anneal was performed in either the RTA or on a vacuum chuck. The 350°C anneal was performed on either the RTA or the hot plate. The 450°C anneal was performed on either the RTA or the tube furnace. All annealing treatments were performed in air except for those in the RTA which were performed in argon. The wafers were 1 to 5 Ω-cm resistivity p-type FZ silicon wafers (100) silicon with boron as the dopant.



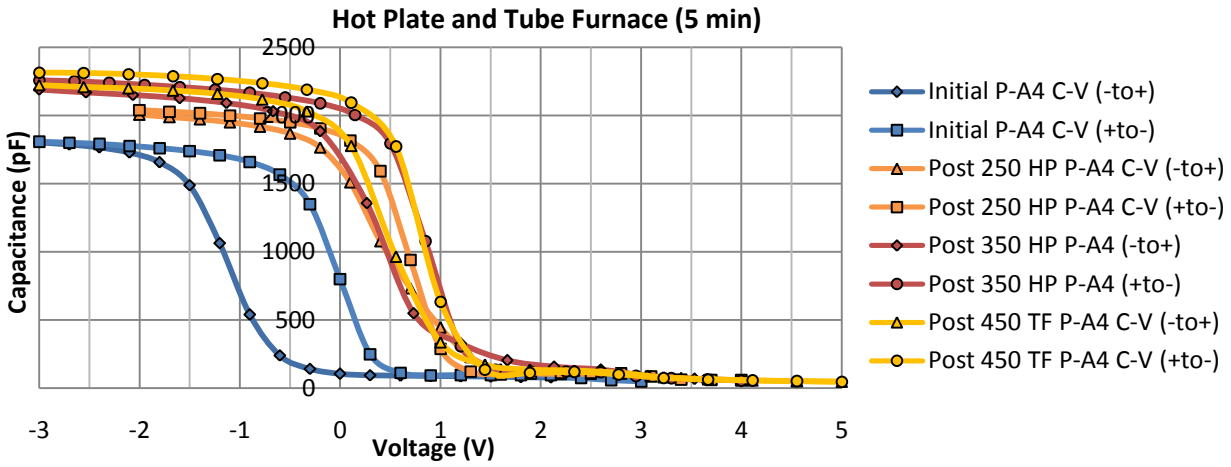


Figure C-1: C-V measurements of the 4 nm Al_2O_3 passivated samples.

The curves in Figure C-1 were taken for the 4 nm Al_2O_3 passivated samples. Curves in the top graph were taken on samples annealed in the RTA, curves in the bottom graph were taken on samples annealed on the hot plate (HP) or tube furnace (TF). The initial curves showed a large degree of hysteresis, indicative of interface traps. With annealing the hysteresis was reduced and became negligible with treatments at 350°C and 450°C for 5 min. Flat band voltage shifts for the 4 nm Al_2O_3 passivated sample were near 1 V with these annealing treatments. Fixed charge for the sample annealed at 450°C in the RTA was calculated to be $-8.9 \times 10^{12}/cm^2$, and fixed charge for the sample annealed at 350°C on the hot plate was calculated to be $-1.0 \times 10^{13}/cm^2$.

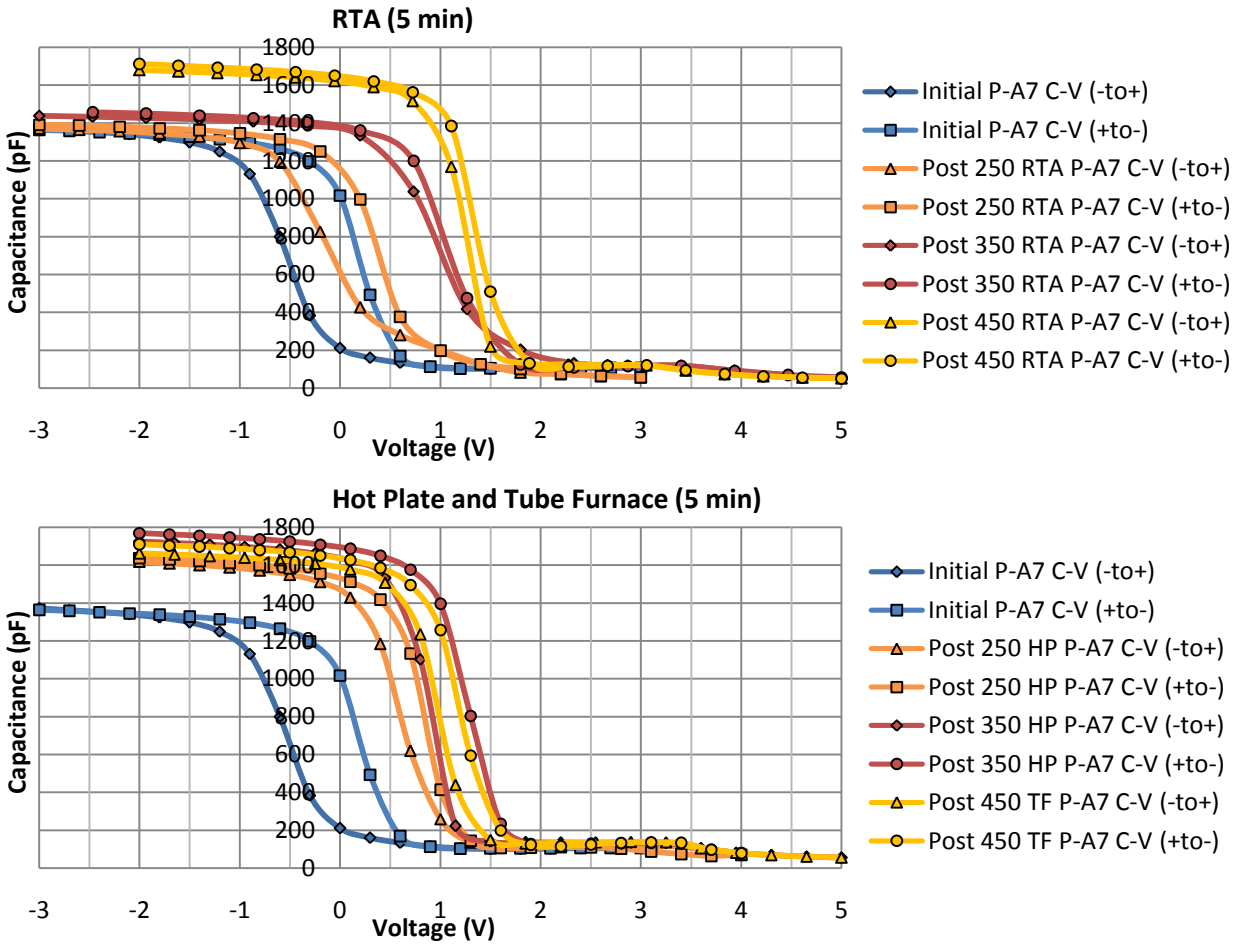


Figure C-2: C-V measurements 7 nm Al_2O_3 passivated sample.

In Figure C-2, the initial curves for the 7 nm Al_2O_3 passivated sample showed a large degree of hysteresis as well, but with annealing the hysteresis was reduced. The V_{FB} shifts for the 7 nm Al_2O_3 passivated sample were near 1.3 V with the 350°C and 450°C annealing treatments. Fixed charge density for the sample annealed at 450°C in the RTA was calculated to be $-9.6 \times 10^{12}/cm^2$, and fixed charge density for the sample annealed at 350°C on the hot plate was calculated to be $-8.8 \times 10^{12}/cm^2$. These values were of the same order of magnitude as the fixed charge densities of the 4 nm Al_2O_3 passivated sample, with no appreciable difference despite the increase in film thickness.

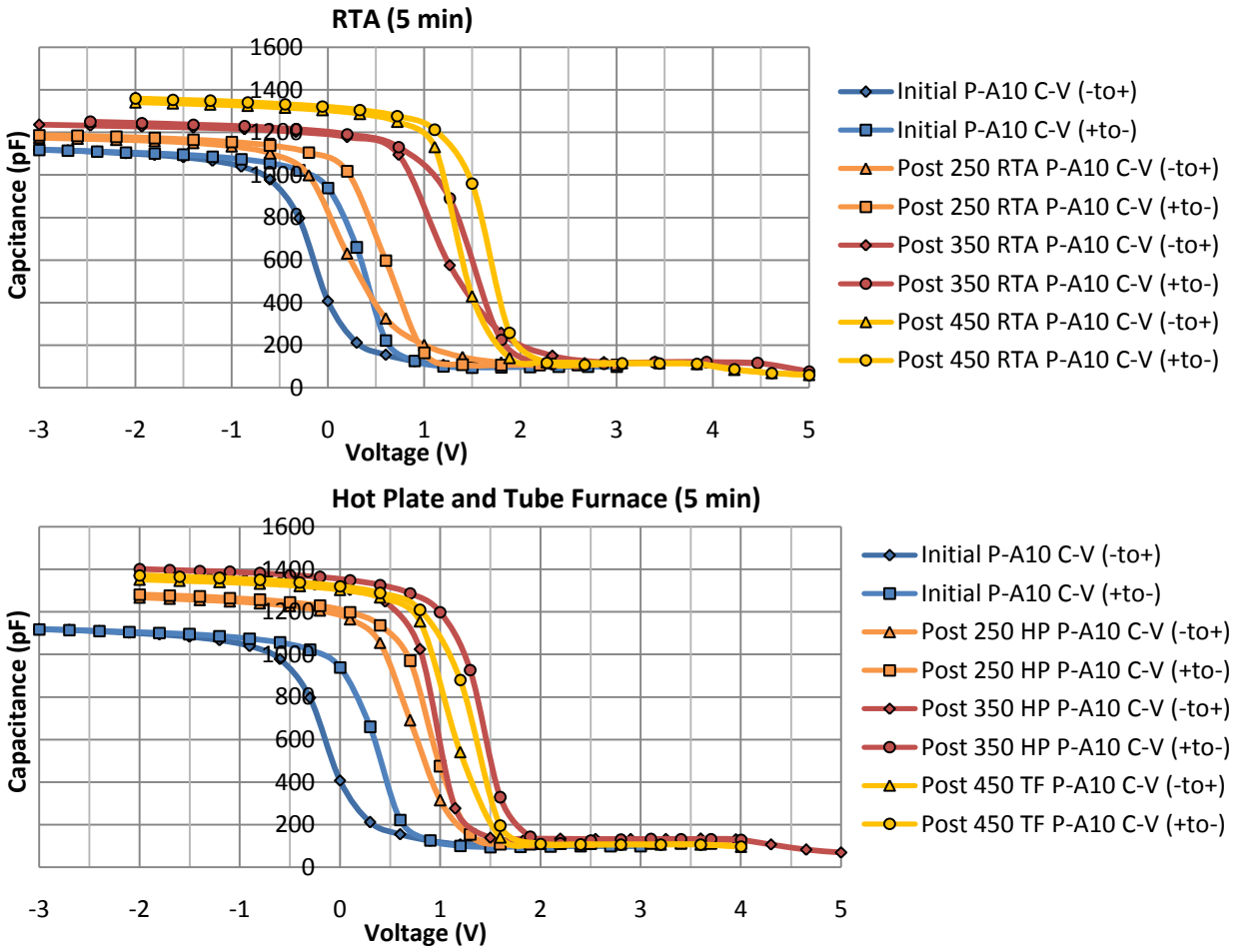


Figure C-3: C-V measurements of the 10 nm Al_2O_3 passivated sample.

In the initial curves for the 10 nm Al_2O_3 passivated sample in Figure C-3, there was a slight degree of hysteresis, but less than what was seen in the thinner Al_2O_3 passivated samples. With annealing the hysteresis was reduced but was not completely eliminated. The V_{FB} shifts for the 10 nm Al_2O_3 passivated sample were near 1.5 V with the 350°C and 450°C annealing treatments. Fixed charge density for the sample annealed at 450°C in the RTA was calculated to be $-9.3 \times 10^{12}/cm^2$, and fixed charge density for the sample annealed at 350°C on the hot plate was calculated to be $-8.1 \times 10^{12}/cm^2$. Again there was no appreciable difference in fixed charge density despite the increase in film thickness.