INTEGRATION AND CHARACTERIZATION OF SILICON NANOWIRE FIELD EFFECT DEVICES

A Thesis in

Electrical Engineering

by

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ABSTRACT

The ability to engineer materials at the nanoscale utilizing a combination of controlled nanomaterial synthesis and self-assembly methods offers the potential to create new electronic devices with improved performance and functionality. Semiconductor nanowires (NWs) provide an ability to utilize the fundamental electronic building blocks that have been developed over a half-century of semiconductor technology and flexibility to integrate a wide choice of materials on a silicon platform. Moreover, semiconductor NWs could be used as an excellent model system for answering fundamental questions related to semiconductor device process integration and electrical transport at the nanoscale. In this thesis, my work on integration and characterization of silicon nanowire (SiNW) field effect (FET) devices is presented. This work provides a basis for understanding process integration and electrical transport in ultra-scaled devices.

First, we describe the synthesis of SiNWs using an Au-catalyzed vapor-liquid-solid (VLS) growth technique. Transmission electron microscopy (TEM) studies indicate that the SiNWs have single crystal cores that are sheathed with a 2-3 nm thin amorphous native oxide. We developed a general integration process to electrically address individual SiNWs in a global-back-gated test structure with four top-side electrodes. The electrical measurement results of four-point resistance and gate-dependent conductance demonstrate that trimethylboron and phosphine can be used as a source of boron and phosphorus for in-situ p- and n-type doping of SiNWs during VLS growth, respectively.

Second, we utilized thermal oxidation of SiNWs to form Si core/SiO₂ shell NW for fabricating top-gated SiNW FET devices. Structural characterization on thermally-
oxidized SiNWs shows that the interface between the Si core and SiO₂ shell is smooth and the SiO₂ shell is uniform along the length of the NW. The field effect measurements show that thermally-grown SiO₂ shell is suitable for use as the gate dielectric in the top-gated SiNW FET device structure, which has better device properties and stronger gate modulation than the global-back-gated test structure. Furthermore, the large hysteresis commonly observed in the subthreshold properties of the global-back-gated test structure is significantly suppressed in the top-gated FET structure. Both p- and n-channel top-gated SiNW FET devices were demonstrated, which facilitates fabrication of complementary SiNW FETs.

Third, we successfully synthesized axially-doped n⁺-p⁻-n⁺ SiNWs by sequential introduction of n- and p-type dopant gases during VLS. TEM studies show that the length of each segment is well controlled and the transition between n⁺ and p⁻ is sharp. The characteristics of FETs fabricated using these SiNWs resemble conventional n-channel MOSFETs, which indicates inversion-mode operation with dominant electron transport. Control samples with different S/D configurations fabricated using a global-back-gated FET structure confirm that there is no deleterious n-type overcoating along the p⁻ segment. These results demonstrate the potential to use SiNWs for future nanoelectronic device application or as a model system by engineering the doping profile during VLS growth and taking advantage of various gating structures.
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Chapter 1

Introduction

1.1 Motivation

Recently there has been increasing research interest in nano science and technology. According to the National Nanotechnology Initiative\(^1\), nano science and technology can be defined as “research and technology development at the atomic, molecular or macromolecule levels, in the length scale of approximately 1-100 nanometer range, to provide a fundamental understanding of phenomena and materials at the nanoscale and to create and use structures, devices and systems that have novel properties and functions because of their small and/or intermediate size”. In this broad field, silicon nanowires (SiNWs) are of particular interest because they are a possible candidate for future nanoelectronic devices and circuits\(^2\) and also can be used as an excellent model system for answering fundamental questions related to the scaling effects on semiconductor device integration process and electrical transport.

Conventional silicon electronics has been dominated by top-down manufacturing methods since 1960\(^3\), where micro- to nanometer-scale features are patterned on bulk Si substrates by lithography to form functional devices. The bottom-up approach represents an exciting alternative to the top-down method. Here, functional structures are assembled from chemically synthesized nanoscale building blocks such as carbon nanotubes (CNTs)\(^4\) and semiconductor nanowires (NWs)\(^5,6\). CNTs have been studied extensively because of their potential as molecular devices and quantum wires. Single walled CNTs
can exhibit either metallic or semiconducting behavior depending on diameter and helicity. However, the inability to control whether CNTs are metallic or semiconducting makes fabrication of specific devices largely a random event.

In contrast to CNTs, SiNWs can be synthesized predictably using the vapor-liquid-solid (VLS) growth method in single crystal form with all key properties controlled, which includes chemical composition, diameter and length, and doping/electronic properties. Moreover, the VLS growth technique facilitates the synthesis of NWs with diameter as small as 2 nm, well into the range where interesting behavior such as quantum confinement is expected. Moreover, axial homo- and hetero-structures can be formed by modulating dopants and alloy composition during VLS synthesis of NWs, and radial junctions by combining VLS with well-controlled epitaxial growth techniques to form core-shell structures. In addition to well-controlled properties, SiNWs provide the ability to utilize the knowledge of semiconductor technology that has been developed over the last half-century. Thus, SiNWs represent one of best-defined and controlled class of nanoscale building blocks, which correspondingly enables a wide-range of devices and integration strategies to be studied.

Prof. Charles M. Lieber and his co-workers at Harvard University demonstrated for the first time the intentional doping of SiNWs and electrical properties of global-back-gated SiNW field effect device (FETs) in 2000. Later, in 2001, this group determined a peak value of the field effect mobility of their SiNW FETs of $\mu_n \sim 1300$ cm$^2$/Vs. The reason for this high value is unexpected and not clearly understood. In the past five years, research on SiNWs has been accelerating and many SiNW-based devices have been demonstrated. For example, SiNWs have been assembled into nanometer scale
FETs\textsuperscript{11,12}, p-n diodes\textsuperscript{9,13}, light emitting diodes\textsuperscript{9}, bipolar junction transistors\textsuperscript{10},
complementary inverters\textsuperscript{11}, and even computational circuits that were used to carry out
basic digital calculations\textsuperscript{14}.

Even with the considerable progress in SiNW synthesis, device integration and
applications that has taken place in the last six years, most of the transport measurements
and analyses of SiNWs have been largely rudimentary, and our understanding of
fundamental issues, including field effect mobility and the effect of surface states,
impurities, orientation, and interfaces on device parameters remain elusive. For example,
the large hysteresis in subthreshold properties observed commonly in global-back-gated
SiNW FETs changes the device parameters dramatically as the gate sweep rate and
direction are varied, which makes it impossible to extract accurate device properties. The
large variation in on-state current from device-to-device that could be caused by factors
such as surface states and wire diameter must to be solved to facilitate practical device
applications. Moreover, SiNW transistors are typically fabricated by placing two metal
contacts on the ends of a SiNW. Such devices may function as so-called Schottky-barrier
(SB) transistors, which is commonly observed in CNT FETs.\textsuperscript{15} Here the transistor action
comes from field induced modulation of the tunneling through the SB at the source
contact, and little or no information about the field effect mobility of the channel can be
extracted.

It is critically important to develop diagnostic NW device structures that will
allow accurate measurement of device properties that are dominated by the SiNW
channel instead of the contacts. Ultimately, these studies will illuminate fundamental
scaling laws for NW synthesis, device integration, and device physics from the bulk to quantum’s regimes.

The aim of my thesis work is to develop an improved understanding of the electrical properties of intentionally-doped SiNWs and associated field effect devices. This research is a first step towards answering fundamental questions related to the effect of scaling on SiNW device process integration and electrical transport. The work presented in the thesis can be divided into three main categories:

1) The VLS synthesis, structural, and electrical properties of as-grown intentionally-doped SiNWs.

2) Dry thermal oxidation of SiNWs and top-gated uniformly-doped SiNW FETs.

3) The VLS synthesis and structural properties of as-grown axially-doped SiNWs and top or wrap-around gated axially-doped $n^+\cdot p^-\cdot n^+$ SiNWs.

1.2 Overview of the thesis

In chapter 2, the synthesis of SiNWs via a metal-catalyzed VLS growth mechanism is described. The diameter and length of the SiNWs are determined by the size of the Au catalyst and growth time, respectively. Intentional doping of SiNWs was achieved by introducing dopant gases such as trimethylboron (TMB) as p-type and phosphine (PH$_3$) as n-type dopants. High resolution transmission electron microscopy (TEM) studies demonstrate that the SiNWs have a single crystal with ~ 2nm thick amorphous native oxide layer on the surface. As-grown SiNWs were integrated into a global-back-gated four-point test structure using a bottom-up assembly approach for four-point resistivity and gate dependent conductance measurements to investigate the dopant
incorporation efficiency and doping type, respectively. Furthermore, Secondary Ion Mass Spectroscopy (SIMS) analysis was used to study the chemically active dopant concentration, which further confirms the conclusions from electrical test results. The source of p-type background doping in nominally-undoped SiNWs and the effect of growth substrates on dopant incorporation efficiency are discussed as well.

In chapter 3, dry thermal oxidation of as-grown uniformly-doped SiNWs was studied to provide a high-quality SiO₂ shell for passivating the SiNW surface and to serve as the gate dielectric of top-gated SiNW FETs. The structural properties of thermally-grown Si/SiO₂ core/shell NWs and SiNW oxidation kinetics are discussed and compared with the results from bulk Si. Using uniformly-doped thermally-oxidized SiNWs, top-gated FET devices are fabricated with enhanced device characteristics, including significantly reduced hysteresis and smaller subthreshold slope when compared with the global-back-gate SiNW test structure. Electrical properties of thermally-oxidized SiNWs such as oxide breakdown field strength and interface charge state density are estimated and discussed.

In chapter 4, the VLS synthesis of axially-doped SiNWs is presented. As-grown axially-doped SiNWs are examined by TEM, which indicates that the SiNWs have a single crystal structure with a thin native oxide on the surface. Moreover, the length and surface morphology of each segment in axially-doped SiNWs are well controlled. Electrical measurements on top-gated FET devices using thermally-oxidized axially-doped n⁺-p⁻-n⁺ SiNWs show excellent field effect device properties with inversion-mode operation. The electrical measurement results suggest that the axially-doped n⁺-p⁻-n⁺ SiNW FETs are suitable for extracting accurate device properties such as field effect
mobility because device properties are dominated by inversion of the channel rather than modulation of a SB contact. Electrical measurements on a series of control samples fabricated with different S/D configurations in a global-back-gated test structure confirms that the second n⁺-segment can be grown without any deleterious overcoating of the p⁻ channel segment during VLS.

Chapter 5 provides summary of this thesis work and overview of future work.

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Chapter 2

*In-situ* Doping and Resistivity of Silicon Nanowires

2.1 Introduction

As discussed in chapter 1, silicon nanowires (SiNWs) grown by Vapor-Liquid-Solid (VLS) technique are not only be a candidate for use as building blocks in future nanoelectronics applications,\(^1,2\) but also as an excellent model system for answering fundamental questions related to the effects of scaling in semiconductor device fabrication, integration and electrical transport. In order to achieve these goals, it is important to control the conductivity of the SiNWs through intentional *in-situ* doping during VLS growth because different doping types and concentrations are required for more sophisticated device designs. For example, a high doping concentration is desired for making ohmic contacts to SiNWs. However, lower doping concentrations are required for the channel of SiNW field effect devices (FETs) to ensure strong gate modulation of the device. Therefore, we conducted a series of studies to investigate *in-situ* doping of SiNWs during VLS growth.\(^3,4\)

This chapter describes the synthesis and characterization of intentionally-doped SiNWs. Section 2.2 provides a brief overview of VLS growth technique used to synthesize SiNWs with *in-situ* doping by introducing trimethylboron (TMB) or diborane (B\(_2\)H\(_6\)) as the p-type dopant gas and phosphine (PH\(_3\)) as the n-type dopant gas. Two different substrates including Anodic Aluminum oxide (AAO) membranes and silicon (Si) wafers coated with a 1 µm thick SiO\(_2\) layer were used as the SiNW growth platform.
Section 2.3 shows the mask layout design and fabrication process of the electrical test structure used to measure four-point resistance and doping type of the SiNWs. It also describes the NW assembly and integration process. The four-point resistance and gate dependent conductance of uniformly-doped n- and p-type SiNWs are presented in sections 2.4 and 2.5 along with discussions. Finally, Section 2.6 summarizes the key contributions in this chapter.

VLS synthesis of SiNWs used in this study was performed by Dr. Kok-Keong Lew. Transmission electron microscopy (TEM) analysis was performed by Dr. Ling Pan and Dr. Bangzhi Liu.

2.2 VLS Synthesis of SiNWs

2.2.1 Overview of VLS technique

The synthesis of SiNWs has been studied extensively. The most common approach used to synthesize SiNWs relies on the VLS mechanism, which was pioneered by Wagner and Ellis in the 1960s. In VLS growth of SiNWs, a metal such as gold (Au) is used as a catalyst to nucleate NW growth from a Si-containing vapor such as silane (SiH₄). Au and Si form a liquid alloy at temperature greater than their eutectic temperature of 363°C, which, upon super-saturation, nucleates the growth of a SiNW. When SiH₄ is used as a source gas, the growth temperature is usually between 360 and 500°C.

The typical VLS growth process can be summarized in the following four steps: (1) mass transport of Si source gases from the gas phase to the Au catalyst surface; (2) reaction of source gases on the Au surface; (3) diffusion of Si through the Au-Si eutectic
liquid phase; (4) crystallization of Si from the super-saturated Au-Si eutectic liquid. Gold is considered to serve a dual role in VLS growth: first, it catalyzes the decomposition of the SiH₄ source gas to form Si atoms, and then the Au-Si liquid alloy acts as a perfect sink for the Si atoms.

### 2.2.2 Substrates for VLS synthesis of SiNWs

Initially AAO membranes with nominal pore diameters of 80 nm⁸ as shown in the scanning electron microscopy (SEM) image of Figure 2.1 (a) were selected as a platform for VLS growth of SiNWs because they can be used to produce well aligned SiNW arrays. A 5 μm long segment of silver (Ag) was electrodeposited into the pores, followed by a 0.25 μm segment of Au as shown in Figure 2.1 (b). The Ag segment was then removed by etching in 8.0 M nitric acid (HNO₃), leaving only the thin Au segment near the top of the membrane to serve as the catalyst for VLS growth. The membrane was cleaned with distilled water in an ultrasonic bath and dried under ambient conditions.

Si wafers coated with a 1 μm thick SiO₂ layer were also selected to serve as a platform for VLS growth of SiNWs. Here Au nanoparticles and Au thin films were used as catalysts to nucleate SiNW growth. We carried out preliminary studies of SiNW growth at 450-500°C using SiH₄ as the source gas and 10 nm Au nanoparticles (Ted Pella, Inc.) dispersed onto Si substrates that were coated with poly-L-lysine. However, the samples usually had low densities of as-grown SiNWs because a low density of Au nanoparticles was required to avoid particle clustering. Moreover, there was considerable variation in NW length particularly after they are removed from the substrate by mechanical agitation. Therefore, in this thesis work, Au thin films were used for VLS synthesis of SiNWs unless otherwise specified. This was accomplished by sputter
deposition of a 3 nm Au thin film followed by annealing at 500°C, which results in the formation of small Au islands as shown in Figure 2.1 (c). It is important to note that the size distribution of Au islands is relatively large, which is reflected in similarly large distribution in the diameter of the as-grown SiNWs.

(a)

(b)
Figure 2.1 (a) Top view and (b) cross-sectional SEM images of AAO membrane. ~ 0.25 µm long electrodeposited Au segment was used as catalyst to grow high density aligned SiNW arrays. (c) A top view SEM image of SiO₂ substrate with sputtered Au thin film as catalyst. Small Au islands with large size distribution are formed after high temperature process.

2.2.3 Experiment setup for SiNW synthesis by VLS

VLS growth of SiNWs was carried out in an isothermal quartz tube reactor at 500°C with a total reactor pressure of 12 Torr using a 10% mixture of SiH₄ in H₂ as the source gas and either TMB (200 ppm in H₂) or B₂H₆ (100 ppm in H₂) as the p-type dopant gas and PH₃ (100ppm in H₂) as the n-type dopant gas. The total gas flow rate was held constant at 100 sccm⁹. The dopant to silane gas ratio [TMB:SiH₄] or [B₂H₆:SiH₄] and [PH₃:SiH₄] were varied from 4.0×10⁻⁶ to 1.6×10⁻² and 2×10⁻⁵ to 2×10⁻³ by changing the inlet gas flow rates of the dopant gas (TMB or B₂H₆ or PH₃) to SiH₄.

2.2.4 Structural properties of as-grown SiNWs

Low magnification SEM images of SiNWs grown out of AAO membranes and on SiO₂ substrates are shown in Figure 2.2 (a) and (b), respectively. As observed, Au tip is
Figure 2.2 Top view SEM images of SiNWs grown (a) out of AAO membrane and (b) on a SiO₂ substrate. The density of SiNWs is high for both types of substrates. Present on top of each SiNW and the majority of the NWs are straight, single wires. A small percentage of SiNWs are branched, which could be because they touch other SiNWs during the growth. Furthermore, the surface of the NWs is smooth and the density is relatively high, which is essential for obtaining high alignment yield during NW assembly and integration. The diameter of as-grown SiNWs ranges from 60 to 100 nm.
This variability can vary the device properties of SiNW field effect devices significantly because of large surface/volume ratio in SiNW case.

Transmission electron microscopy (TEM) was used to characterize the structural properties of the as-grown SiNWs. The SiNWs were released from the substrates after VLS synthesis by mechanical sonication in an isopropyl alcohol (IPA) solution. A suspension containing individual SiNWs was dropped onto lacey carbon grids for TEM analysis, which was conducted using a JEOL 2010F field-emission TEM (FE-TEM) operated at 200 kV. Typical TEM micrographs of nominally-undoped, B$_2$H$_6$-doped ([B$_2$H$_6$:SiH$_4$] = 1.4×10^{-2}), TMB-doped ([TMB:SiH$_4$] = 1.6×10^{-2}) and PH$_3$-doped ([PH$_3$:SiH$_4$] = 2×10^{-3}) SiNWs grown out of the AAO membranes are shown in Figure 2.3.

As shown in Figure 2.3 (a), the nominally-undoped SiNWs are single crystal with a $<112>$ dominant growth direction and are covered by a thin ~ 2nm native oxide layer. A typical B$_2$H$_6$-doped SiNW with [B$_2$H$_6$:SiH$_4$]=1.4×10^{-2} shown in Figure 2.3 (b) consisted of a crystalline Si core, approximately 30 nm in diameter and an amorphous Si shell approximately 35 nm thick. While this radial growth can be used to form i-Si/p-Si core-shell structures, it is undesired for the fabrication of uniformly boron (B) -doped NWs. In contrast, the majority of the TMB-doped SiNWs were found to be either single- or bi-crystalline. As shown in Figure 2.3 (c), a representative TMB-doped SiNW is ~ 50 nm in diameter and single crystalline with a $<112>$ growth direction and is covered by a thin ~ 2 nm native oxide layer similar to that observed in nominally-undoped SiNWs.
Figure 2.3 TEM images of (a) nominally-undoped, (b) B_2H_6-doped ([B_2H_6:SiH_4] = 2×10^{-2}), (c) TMB-doped ([TMB:SiH_4] = 2×10^{-2}) and (d) PH_3-doped ([PH_3:SiH_4] = 2×10^{-3}) SiNWs grown out of AAO membranes. The SiNWs are single crystal with a thin 2-3 nm native SiO_x layer covering the surface. The high diborane-doped ([B_2H_6:SiH_4] = 2×10^{-2}) SiNWs have an amorphous Si shell that surrounds the single crystal Si core.
The different NW structures obtained with B$_2$H$_6$ and TMB can be explained by comparing the thermal stability and reactivity of the two sources with SiH$_4$. B$_2$H$_6$ in the gas phase decomposes at relatively low temperature forming monoborane (BH$_3$). The B-B bond dissociation energy of B$_2$H$_6$ is approximately 27 Kcal/mol. Furthermore, B$_2$H$_6$ is known to react with SiH$_4$ leading to an increase in the Si growth rate for B$_2$H$_6$-doped films. The increase in Si thin film deposition rate is believed to be responsible for the formation of the amorphous Si outer layer on the B$_2$H$_6$-doped NWs, and further studies are underway to investigate this effect. TMB decomposes via the sequential loss of methyl group (CH$_3$). The B-C bond dissociation energy in TMB is approximately 87 kcal/mol, leading to an increased thermal stability for TMB compared to B$_2$H$_6$. Thus, we believe that the reduced reactivity of TMB enables the growth of highly B-doped SiNWs without a thick amorphous Si coating.

In comparison, the majority of the phosphorus (P) -doped SiNWs were found to be single crystal with a $\langle 112 \rangle$ growth direction as shown in Figure 2.3 (d). A smaller fraction were bicrystals with a [112] growth axis that contained a twin boundary separating two parallel NW segments, similar to that observed in nominally-undoped and TMB-doped SiNWs. The PH$_3$-doped ([PH$_3$:SiH$_4$] = 2×10$^{-3}$) SiNWs exhibited slightly increased surface roughness, compared to nominally-undoped or TMB-doped SiNWs. A thin layer of native silicon oxide (SiO$_x$) was present on the surface of all of the P-doped SiNWs.

The growth direction of SiNW can be controlled by the crystal orientation of the substrate. For example, Si (111) wafers can be used in VLS growth and to give rise to a dominant growth orientation of $\langle 111 \rangle$. However, for NWs grown without using a
crystalline substrate, such as the AAO membrane, a range of growth orientations was observed such as \( <112> \), \( <111> \) and \( <110> \). In addition, bicrystal SiNWs with a (111) twin plane were also reported with a dominant growth orientation of either \( <110> \) or \( <112> \). The variation of the growth directions of SiNWs could be an important factor for many studies such as oxidation rate and field effect mobility especially for sub-10 nm SiNWs. Recent work by Jim Mattzela and Chad Eichfeld demonstrated a new TEM workbench structure that provides a one-to-one correlation between device characteristics and detailed structural information (e.g., diameter, orientation, interfacial roughness, etc.) collected on the same NW. This is accomplished by performing high-resolution TEM on individual NW devices that are integrated directly onto an electron transparent window. Finally, it should be noted that the \( <100> \) growth orientation is not observed commonly in VLS growth of SiNWs because NWs preferentially grow in the direction that minimizes their surface free energy.

TEM studies on SiNWs grown on SiO\(_2\) substrate show similar structural properties as those shown for SiNWs grown out of the AAO membrane. Thus, these images will not be repeated here.

These results demonstrate that the use of TMB and PH\(_3\) as a source of boron and phosphorus for in-situ p- and n-type doping produces as-grown SiNWs on both AAO membrane and SiO\(_2\) substrate with single crystal structure covered by a ~2 nm native oxide SiO\(_x\) layer. Thus, these SiNWs can be used to fabricate devices that require control over p- and n-type doping along the axial direction. Moreover, field effect device application can be realized and used as an excellent model system to investigate the scaling effect of semiconductor devices.
2.3 Electrical test structure

Individual SiNWs were characterized electrically by integrating them into a global-back-gated four-point test structure that includes four topside electrodes as shown in Figure 2.4. Four-point resistance and gate-dependent conductance measurements were carried out on nominally-undoped, uniformly TMB-doped and PH₃-doped SiNWs grown out of AAO membranes and on SiO₂ substrates with a nominal 80 nm diameter to study the doping incorporation efficiency of TMB and PH₃ dopant gases. The outer electrodes were used to force a constant current through the SiNW while the inner electrodes labeled source (S) and drain (D) in Figure 2.4 were used as high impedance voltage probes for four-point resistance measurements, which will be discussed in detail in section 2.4. The inner S/D electrodes and global back gate were used for gate-dependent conductance measurements to determine the doping type of SiNWs, which will be discussed in detail in section 2.5.

![Figure 2.4](image)

Figure 2.4 Simplified 3-D schematic representation of a four-point back-gated test structure used to characterize the four-point resistivity and doping type of the SiNWs.
2.3.1 Nanowire preparation and assembly

The SiNWs were grown to a nominal length of 15 µm using both types of substrates. In the case of AAO substrates, this involved growing 20 µm NWs such that the first 15 µm protruded from the tops of the pores. Those grown from the SiO₂ substrates were grown to a length of 15 µm. The SiNWs were released from the growth substrate by mechanical agitation in an ultrasonic bath and suspended in IPA.

Electrofluidic assembly was used to position individual SiNW between pairs of large-area electrodes as illustrated in Figure 2.5.¹⁸ By applying an AC voltage across the bottom pair of interdigitated electrodes, which are electrically isolated from the top electrodes, an AC electric field can be formed between two top electrodes through the capacitive coupling. The non-uniform AC electric fields induce long and short-range forces to direct NWs self-assembly onto the patterned array. Specifically, long-range dielectrophoretic forces cause NWs to move in the direction of highest field strength, while final positioning is done by the short-range electric field forces. The alignment yield depends on the excitation frequency, polarizability of medium, and conductivity of the NWs. For example, NWs with higher conductivity align more easily because of their higher polarizability. This alignment process is self-limiting because once one NW is positioned between two electrodes the electric field drops to almost zero across that pair of electrodes. Therefore, only one NW will be captured between each pair of electrodes, which is necessary for electrical characterization of individual SiNWs. The SEM image in Figure 2.6 shows one NW captured between two electrodes. Furthermore, post-processing can be done after NW alignment to electrically address individual NWs. Finally, this assembly technique facilitates parallel integration of NWs on the same
substrate, which allows characterization of large numbers of NW devices (>100) that are all subjected to the same processing steps. This makes it possible to compile statistically significant data sets that address the inherent variability in the as-grown SiNWs, which is critically important for understanding electrical properties of SiNW devices.

**Figure 2.5** 3-D illustration of the electrifluidic NW assembly technique. The non-uniform AC electric fields induce long and short-range forces to direct NWs self-assembly onto patterned electrodes.
Figure 2.6 A SEM image showing a single NW captured between two large area electrodes that are used to electrically address the NW.

2.3.2 Test structure fabrication

Three optical and one electron-beam mask layers are used to fabricate the four-point test structure as shown in Figure 2.7 (a) – (d). The first mask layer shown in Figure 2.7 (a) is comprised of pairs of interdigitated electrodes that are connected to large area probe contacts at the northwest and southeast corners of the layout. When an AC voltage is applied across these two contact pads, an AC electric field is generated between each pair of top electrodes, which facilitates simultaneous NW alignment on large arrays of electrodes as discussed in section 2.3.1. Before fabricating the top electrodes, an interlevel dielectric layer is deposited to provide electrical isolation between the bottom and top electrodes during NW assembly and measurement. Figure 2.7 (b) shows the second mask level that is designed to remove the portion of the interlevel dielectric layer not required for isolation. The third mask level shown in Figure 2.7 (c) is used to define the top electrodes that provide the electric field for nanowire assembly and also serve as large area contacts for electrical probing. The final mask shown in Figure 2.7 (d) is designed to define the four top-side electrodes using electron-beam lithography. This
completes the test structure used to perform four-point resistance and gate-dependent conductance measurements.⁴
Figure 2.7 Mask layouts of one single cell including (a) bottom electrode layer, (b) dielectric removal layer and (c) top electrode layer with a zoomed-in layout of a single device. (d) Layout of four-point features defined by electron-beam lithography after nanowire assembly. (e) Cross-sectional schematic of the global-back-gated four-point test structure.

Samples were fabricated by integrating SiNWs onto n^{++}-Si substrates (ρ~0.001 Ω-cm) coated on the topside with 100 nm of silicon dioxide (SiO₂) grown by dry thermal oxidation and the backside with 20/80 nm of Ti/Au deposited by thermal evaporation, which served as the gate dielectric and electrode respectively as illustrated in Figure 2.7 (e). After the thermal evaporation Ti(30nm)/Au(60nm) to form the lower electrode using
the layout shown in Figure 2.7 (a), a 100nm thick layer of Si$_3$N$_4$ was deposited by plasma enhanced chemical vapor deposition (PECVD) to provide isolation between the top and bottom electrodes. The Si$_3$N$_4$ in areas not protected by the pattern shown in Figure 2.7 (b) was removed by wet etching using buffered oxide etch (BOE). The top electrode layer was defined using the layout shown in Figure 2.7 (c) and Ti(30nm)/Au(70nm) was deposited by thermal evaporation. Finally, after electrofluidic assembly of the SiNWs, four topside electrodes were patterned using electron-beam lithography using the layout shown in Figure 2.7 (d) followed by lift-off of Ti(100 nm)/Au(100 nm) deposited by thermal evaporation. A thick metal layer is used for the top side four electrodes because good step coverage is required to make good contact to SiNWs. Moreover, as mentioned in structural properties of as-grown SiNWs of section 2.2, a thin native oxide is present on the SiNW surface. Therefore, in order to make intimate contact to SiNWs, BOE, which can provide hydrogen-terminated surface to prevent re-oxidation for a short period, was used to remove this native oxide layer immediately before loading the sample into the thermal evaporator for the final metallization.

All post-growth thermal treatment (e.g., contact anneal) was avoided to minimize unintentional and intentional impurity diffusion and activation that would make direct comparison of the as-grown SiNWs difficult.

2.3.3 Electron-beam lithography

Electron-beam lithography was used to define most of the features in the test structure following NW assembly because it provides the ability to define nano-scale features and also the flexibility to customize layouts without redesigning new mask reticles. A double layer electron-beam resist was used in this work, which consists of a
top 3% 950K PMMA in anisole layer and a bottom 11% MAA(8.5)-MMA in ethyl lactate (co-polymer) layer, as shown in Figure 2.8. A 10 nm Au layer was incorporated to dissipate the charge accumulated on the sample surface during electron beam exposure to increase the resolution and reduce the proximity effect. After exposure, the Au layer was removed using Au etchant type TFA (Transcene, Inc.). The pattern was then developed in MIBK:IPA=1:1 for 60s, which results in the overhang structure as illustrated in Figure 2.8. This overhang profile provides clean lift-off for metal thickness up to 350nm, which makes it possible to achieve good step coverage even for NWs with larger diameters.

**Figure 2.8** Cross-sectional schematic of the double layer Co-polymer/PMMA e-beam resist structure. The overhang profile achieved after development provides clean lift-off for metal thickness up to 350 nm.

### 2.3.4 Finished test structure

A top-view FE-SEM image of a fully fabricated test structure is shown in Figure 2.9 (a). A SiNW is aligned between the two large-area electrodes. Four additional electrodes defined by electron-beam lithography are also shown in this image. The global
Figure 2.9 (a) Top view and (b) cross-sectional FE-SEM images of fabricated global-back-gated four-point test structure. The spacing was varied from 1.6 to 2.6 µm between the two internal electrodes (S/D) and from 4 to 8 µm between the two external electrodes. Approximately ~ 75% of the surface of SiNWs is contacted by the metal with good step coverage.

The back gate is on the back side of n$$^+$$+ Si wafer and not shown in this FE-SEM image. The spacing was varied from 1.6 to 2.6 µm between the two internal electrodes (S/D) and from 4 to 8 µm between the two external electrodes to accommodate SiNWs with
different lengths. Focused ion beam (FIB) cross-sections were also used to prepare a sample of the finished test structure for cross-sectional TEM analysis. This was used to investigate the morphology of the interface between SiNW and contact metal and the step coverage of the contact metal. A typical cross-sectional TEM image is shown in Figure 2.9 (b), which indicates that the interface between the SiNW and the contact metal is smooth and ~ 75% of the SiNW surface is contacted by the metal with good step coverage. This observation is important because the percentage of the coverage must be considered during the theoretical calculations of contact resistivity and gate capacitance in top gated SiNW field effect device. This percentage can be further increased to 100% using a wrap-around gate structure, which will be discussed in detail in chapter 3.

2.4 Nanowire resistivity

Electrical characterization was performed on more than ten SiNWs grown at each [B$_2$H$_6$:SiH$_4$], [TMB:SiH$_4$] and [PH$_3$:SiH$_4$] gas flow ratio to account for variations in properties that can be introduced by differences such as SiNW diameter. Moreover, all electrical data was collected in a chamber purged with nitrogen (N$_2$) to minimize the deleterious effects of adsorbed moisture on the SiNW surfaces, which can have a significant impact on the measurement reproducibility and stability, particularly for nominally-undoped and lightly-doped SiNWs.

2.4.1 Two-point current-voltage measurement

Two point current-voltage (IV) measurements were conducted between two internal electrodes (S/D) as indicated in Figure 2.10 (a). Typical results on TMB-doped, B$_2$H$_6$-doped, PH$_3$-doped and nominally-undoped SiNWs grown out of the AAO
membranes are plotted in Figure 2.10 (b) and (c). As plotted in Figure 2.10 (b), the IV curves are linear and symmetric for both positive and negative biases for heavily-doped SiNWs. However, for lightly doped SiNWs, such as nominally-undoped and [\(\text{PH}_3:\text{SiH}_4\)=2×10^{-5}] doped SiNWs shown in Figure 2.10 (c), the IV curves are nonlinear and asymmetric, which suggests that the current of these SiNWs is dominated by the Schottky barrier at metal/SiNW contacts. Variations in current of up to a factor of three are observed for different devices fabricated from the same growth run due to differences in wire diameter and contact resistance. The resistance extracted from the two-point IV curves includes contributions due to NW and contact resistance. Similar results are observed for SiNWs grown on SiO$_2$ substrate. Therefore, in order to obtain the SiNW resistance, we used four-point resistance measurement technique to isolate the contact resistance from the SiNW resistance where the differential voltage $\Delta V$ developed across the two internal voltage probes was divided by the current forced between the two external electrodes.\(^3\)
Figure 2.10 (a) Two-point IV measurement configuration using HP4156B semiconductor analyzer. The IV curves were measured between the two internal electrodes. (b) The IV curves for highly TMB-doped ([TMB:SiH₄]=2×10⁻²), B₂H₆-doped ([B₂H₆:SiH₄]=2×10⁻³), PH₃-doped ([PH₃:SiH₄]=2×10⁻³) and PH₃-doped ([PH₃:SiH₄]=2×10⁻⁴) SiNWs are linear and symmetric for both positive and negative biases. (c) The IV curves for nominally-undoped and PH₃-doped ([PH₃:SiH₄]=2×10⁻⁵) SiNWs are nonlinear and asymmetric.
2.4.2 Four-point resistance measurement

The four-point resistance measurement technique is illustrated in the simplified circuit schematic presented in Figure 2.11 (a). When a constant current is applied through the device under test (DUT), only the voltage drop across the DUT will be measured when the impedance (R_{vp}) of the electrometer is much higher than the DUT resistance (R_{DUT}). The R_{DUT} is then calculated by dividing the applied current by the differential voltage. The measurement setup is illustrated in Figure 2.11 (b), which consists of one HP4156B semiconductor analyzer and two Keithley 6517 electrometers. Signal and measurement unit 1 (SMU1) and 2 (SMU2) of the HP4156B are used to apply constant current through the two external electrodes while voltage measurement unit 1 (VMU1) and 2 (VMU2) units of the HP4156B are used to measure the differential voltage drop between two internal electrodes by cascading two Keithley 6517 electrometers. The Keithley 6517 provides very high input impedance (>10^{15}\,\Omega), which is critically important for four-point measurements on nominally-undoped and lightly doped SiNWs.

A typical four-point measurement result is plotted in Figure 2.12 and shows the differential voltage vs. sampling time for different forced currents. The spacing between each curve is uniform, which indicates that the four-point resistance does not change as the forced current changes. This is in contrast to what was observed in two-point IV measurements of the nominally-undoped and lightly-doped SiNWs shown in Figure 2.10 (c). This confirms that the contact resistance is separated from the SiNW resistance in this measurement.
Figure 2.11 (a) Simplified circuit representation of four point resistance measurement. $R_{VP}$ represents the input impedance of the voltage meter. $R_{DUT}$ represents the resistance of device under test. $R_{C}$ represents the contact resistance. $I_{SRC}$ is the current source while $V_{MEAS}$ is the voltage meter. (b) Measurement configuration using one HP4156B semiconductor analyzer and two Keithley 6517 electrometers with high input impedance ($>10^{15}\Omega$).
Figure 2.12 A typical four-point measurement result, which suggests that the contact resistance is separated from the SiNW resistance.

2.4.3 Summary of four-point resistivity

A plot of SiNW resistivity and carrier type as a function of dopant to SiH₄ gas ratio for SiNW grown out of AAO membranes is shown in Figure 2.13. Nanowire resistivity ($\rho_{\text{SiNW}}$) was determined from the resistance of the SiNW ($R_{\text{SiNW}}$) from the relationship $\rho_{\text{SiNW}}=R_{\text{SiNW}} \times A/L$, where $A$ is the area and $L$ is the length, using the length and diameter measured by FE-SEM. $\rho_{\text{SiNW}}$ was found to be $0.25 \pm 0.12$, $2.1 \pm 1.6$, $1.9 \pm 1.6$, $0.08 \pm 0.06$, $0.035 \pm 0.02$ and $0.006 \pm 0.003$ Ω·cm for SiNWs doped with [TMB:SiH₄] = $2 \times 10^{-2}$, nominally-undoped and [PH₃:SiH₄] = $2 \times 10^{-5}$, $7 \times 10^{-5}$, $2 \times 10^{-4}$, $2 \times 10^{-3}$, respectively. The error bars represent the distribution of resistivities calculated from four-point resistance data collected on more than ten SiNWs at each dopant to SiH₄ gas ratio. The carrier type was determined from the gate dependent conductance measurements that will be discussed in detail in section 2.5. Four-point resistivity of
B₂H₆-doped SiNWs is not shown in Figure 2.13 since their single crystal Si core and amorphous Si shell structure is not desired for device applications. These values of ρ_{SiNW} neglect the effects of surface depletion or accumulation on the actual cross-sectional area responsible for conduction and the voltage probe contact barriers on channel potential. Thus, larger measurement inaccuracies are expected for nominally-undoped and lightly-doped SiNWs than the more heavily doped wires. Nevertheless, a clear trend of decreasing ρ_{SiNW} is noted for increasing [PH₃/TMB::SiH₄], which shows that phosphorus and boron are effectively incorporated into the SiNWs from PH₃ and TMB gas sources during VLS growth.

![Figure 2.13](image)

**Figure 2.13** Summary of four-point resistivity with error bars for SiNWs with different dopant to SiH₄ gas ratios grown out of AAO membranes. The error bars represent the distribution of resistivities calculated from four-point resistance data collected on more than ten SiNWs at each gas flow ratio. The carrier type was determined from gate-dependent conductance measurements where squares and triangles are used to denote p- and n-type SiNWs, respectively. All measurements were conducted in a N₂ purged chamber for 8+ hours.
Secondary ion mass spectrometry (SIMS) was used to measure the total concentration of phosphorus and boron that was incorporated into the SiNWs during VLS growth using 3 KeV Cs\(^+\) and O\(^{2+}\) primary ion beams, respectively. The measurement was performed by S. W. Novak (Evans East, Inc.) directly on high density arrays of 20\(\mu\)m long intentionally doped SiNWs that protruded from AAO membrane after the Au catalyst was removed from the tips of the SiNWs by wet etching. The SIMS signal was converted to concentration (cm\(^{-3}\)) using ion implanted standards for boron and phosphorus in silicon. In the case of phosphorus detection, mass interference from Si-H species at a mass to charge ratio of 31 was subtracted from the total signal to obtain the phosphorus concentration. The lower detection limits (LDL) of both boron and phosphorus measured using nominally-undoped SiNW samples were on the order of 1\(\times\)10\(^{17}\) to 1\(\times\)10\(^{18}\) cm\(^{-3}\). This relatively high LDL is most likely due to background contamination resulting from the high surface area of the NW samples. As shown in Figure 2.14, the measured phosphorus concentrations were approximately 2\(\times\)10\(^{18}\), 2\(\times\)10\(^{19}\) and 1\(\times\)10\(^{20}\) cm\(^{-3}\) for [PH\(_3\):SiH\(_4\)] = 2\(\times\)10\(^{-5}\), 2\(\times\)10\(^{-4}\), and 2\(\times\)10\(^{-3}\), and the boron concentrations were 1\(\times\)10\(^{18}\) and 4\(\times\)10\(^{19}\) cm\(^{-3}\) for [TMB:SiH\(_4\)] = 1\(\times\)10\(^{-3}\) and 2\(\times\)10\(^{-2}\). These SIMS results show that both the phosphorus and boron concentrations increase in direct proportion to the [PH\(_3\)/TMB:SiH\(_4\)] over the entire range of inlet gas flow ratios investigated. In addition, the incorporation efficiency of phosphorus from PH\(_3\) is at least an order of magnitude greater than that of boron from TMB for these gas flow ratios as indicated in Figure 2.14.
It should be noted that the measured NW resistivities are substantially higher than would be expected at similar acceptor concentrations in bulk Si. There are several potential explanations for this difference. The boron concentrations in the NWs were determined by SIMS using bulk Si boron calibration standards which may not accurately extrapolate to high surface area NW samples. Incorporation of Au impurities within the SiNW during VLS growth may lead to an increase in resistivity due to compensation from deep donors. Alternatively, a reduction in hole mobility in the NWs due to enhanced surface scattering would also give rise to increased resistivity.

Both four-point resistivity and SIMS data indicate that a much higher inlet gas flow ratio of TMB as compared to PH$_3$ is required to achieve similar p- and n-type SiNW resistivities. In particular, [TMB:SiH$_4$] = 2$\times$10$^{-2}$ gives $\rho_{\text{SiNW}}$ = 0.25 (±0.12) while [PH$_3$:SiH$_4$] = 7$\times$10$^{-5}$ gives $\rho_{\text{SiNW}}$ = 0.08 (±0.06). This can most likely be attributed to the
lower incorporation efficiency of boron from TMB than phosphorus from PH₃ that was deduced from SIMS measurements of dopant concentration. Prior work has shown that the bond dissociation energy is in the range of 76.4 to 88.5 kcal/mol²⁰,²¹ for P-H bonds in PH₃ and 86.8 kcal/mol for B-C bonds in TMB. Thus, the slightly higher bond dissociation energy of TMB would result in a higher thermal stability, and hence lower incorporation efficiency of TMB compared to PH₃. In addition, the introduction of unintentional impurities such as carbon or gold that form additional energy levels within the bandgap of silicon could also contribute to the increased resistivity of the TMB-doped SiNWs.

Several observations regarding incorporation of electrically-active boron and phosphorus dopants during SiNW VLS growth are evident from the data of Figure 2.13. First, the values of four-point resistivity determined for lightly phosphorus-doped SiNWs (i.e., [PH₃:SiH₄] < 7×10⁻⁵) are not inversely proportional to [PH₃:SiH₄] as would be expected from the SIMS data in Figure 2.14. In particular, the median resistivity of SiNWs grown at the lowest inlet gas flow ratio of [PH₃:SiH₄] = 2×10⁻⁵ was nearly equal to that of the nominally-undoped SiNWs. A further increase in [PH₃:SiH₄] from 2×10⁻⁵ to 7×10⁻⁵ was accompanied by an initial large decrease in resistivity (factor of ~27), at which point the resistivity began to decrease more slowly (factor of ~7 per decade increase in [PH₃:SiH₄]) and in direct proportion to the increase in phosphorus concentration. As will be discussed in section 2.5, gate-dependent conductance measurements indicate that SiNWs grown using [PH₃:SiH₄] = 2×10⁻⁵ have a p-type background, and that [PH₃:SiH₄] greater than 2×10⁻⁵ are required to convert the NWs from p- to n-type. Thus, the comparable values of resistivity obtained for nominally-
undoped and \([\text{PH}_3\text{:SiH}_4] = 2 \times 10^{-5}\) can be explained by the p-type background compensating the incorporated phosphorus in SiNWs with \([\text{PH}_3\text{:SiH}_4] = 2 \times 10^{-5}\). After a sufficient amount of phosphorus is introduced to overcome the p-type background, the resistivity begins to decrease in direct proportion to the increase in phosphorus concentration, which occurs for \([\text{PH}_3\text{:SiH}_4] > 7 \times 10^{-5}\). Potential sources of the p-type background in the nominally-undoped SiNWs will be discussed in section 2.5. The larger decrease in resistivity for \([\text{PH}_3\text{:SiH}_4]\) between \(2 \times 10^{-5}\) and \(7 \times 10^{-5}\) could, at least in part, be explained by surface effects that were not considered in determining SiNW resistivity. One such effect is surface depletion that would result in an overestimate of resistivity, which is more pronounced for nominally-undoped and lightly-doped SiNWs such as those grown with \([\text{PH}_3\text{:SiH}_4] < 7 \times 10^{-5}\).

2.5 Global back gate dependent conductance measurement

As mentioned in section 2.4.3, gate dependent conductance measurements were used to determine the carrier type of each SiNW at different dopant (e.g., TMB/PH\(_3\)) to SiH\(_4\) gas flow ratios. This was achieved by measuring the IV curve between two internal electrodes as S/D while varying the global back gate voltage as illustrated in Figure 2.4. For p-type SiNWs, the current increases as the gate voltage decreases, which is consistent with depletion mode operation of a p-channel field effect device (FET). Moreover, for n-type SiNWs, the current increases as the gate voltage increases, which is consistent with depletion mode operation of an n-channel FET. It is important to note that the actual transport mechanism of these global-back-gated uniformly doped SiNW FET structures
includes not only the channel depletion but also the Schottky barrier modulation as will be discussed in the next section.

### 2.5.1 Transport mechanism

As demonstrated previously in carbon nanotube (CNT) studies\(^2\), the global-back-gated field effect device test structures are operated by field induced modulation of Schottky barrier at source contact because the Schottky barrier between the contact metal and the SiNW is often not negligible, especially for nominally-undoped and lightly-doped SiNWs. In the “ON” state, the back-gated device operates by hole tunneling through the Schottky barrier because the effective width of the barrier is lowered by the gate voltage.

![Band diagrams of On- and Off-state operation of global-back-gated nominally-undoped SiNW FET devices.](image)

**Figure 2.15** Band diagrams of On- and Off-state operation of global-back-gated nominally-undoped SiNW FET devices.
as illustrated by the band diagram in Figure 2.15. In the “OFF” state, the device turns off because most of holes can not tunnel effectively through the Schottky barrier whose width is increased significantly by the gate voltage. In addition to Schottky barrier modulation, depletion of SiNW channel also can contribute to the field effect properties. This effect may dominate back-gated heavily-doped SiNW FETs because the width of the Schottky barrier is usually thin, which allows the carriers tunnel through the barrier more easily.

2.5.2 Carrier type of as-grown SiNWs

The drain-to-source current ($I_{DS}$) vs. drain-to-source voltage ($V_{DS}$) for different gate-to-source voltage ($V_{GS}$) (i.e., output characteristics) of nominally-undoped and TMB-doped ([TMB:SiH$_4$] = 2×10$^{-2}$) SiNWs are plotted in Figure 2.16. The nominally-undoped SiNWs show a decrease in $I_{DS}$ as $V_{GS}$ is increased from $V_{GS} = 0$ to the pinch-off voltage of $V_{GS} \sim 5$V as shown in Figure 2.16 (a). These results are consistent with depletion mode operation of a SiNW FET with p-type background concentration. Possible sources of these unintentional acceptors are discussed in page 44. In comparison, in Figure 2.16 (b) the TMB-doped SiNWs have an $I_{DS}$ that is a factor of twenty to forty times larger than the nominally-undoped SiNWs at $V_{GS} = 0$V, and have smaller modulation of $I_{DS}$ with increasing $V_{GS}$. These NWs do not show pinch-off for gate voltages as large as $V_{GS} = 40$V due to the heavier p-type doping and the relatively thick gate oxide. These gate dependent IV measurements further substantiate the SIMS and resistivity measurements, which indicate that boron is being incorporated into the SiNWs during VLS synthesis.
Figure 2.16 Output properties of global-back-gated (a) nominally-undoped and (b) TMB-doped ([TMB:SiH₄] = 2×10⁻²) SiNW FET devices. The topmost curve in both plots was measured at zero $V_{GS}$. The voltage step is 1V for (a) and 5V for (b).

Output characteristics of SiNWs grown using [PH₃:SiH₄] = 2×10⁻⁵, 7×10⁻⁵ and 2×10⁻⁴ are plotted in Figure 2.17 (a) - (c). A decrease in $I_{DS}$ as $V_{GS}$ is increased from $V_{GS} = 0$ to the pinch-off voltage of $V_{GS} \sim +5$V is observed for SiNWs grown using [PH₃:SiH₄] = 2×10⁻⁵. In contrast, a more negative $V_{GS}$ is required to cause a reduction in $I_{DS}$ for SiNWs grown using [PH₃:SiH₄] = 7×10⁻⁵, 2×10⁻⁴, and 2×10⁻³. These results are
consistent with a conversion from p- to n-type conduction at a [PH3:SiH4] between 2×10⁻⁵ and 7×10⁻⁵. In addition, the values of $I_{DS}$ measured at $V_{GS} = 0$ as well as the pinch-off voltages for [PH3:SiH4] = 7×10⁻⁵, 2×10⁻⁴, and 2×10⁻³ are considerably larger than those grown using [PH3:SiH4] = 2×10⁻⁵. This is due to the higher carrier concentration of the n-type SiNWs, which results in a reduction in the width of the S/D Schottky barrier. These show that phosphorus is being incorporated into the SiNWs during VLS growth using PH₃. However, it should be noted that the electrically-active p- and n-type carrier concentrations can not be established from the measured values of four-point resistance because the actual mobility of the SiNWs is expected to be significantly different from that of bulk silicon and can not be accurately determined using this test structure.
Figure 2.17 Output characteristics of global back-gated SiNWs grown using [PH₃:SiH₄] = 2×10⁻⁵ (a), 7×10⁻⁵ (b), and 2×10⁻⁴ (c). The topmost curve is $V_{GS} = 0$V in all plots. The voltage step is $V_{GS} = +1$V in (a), $V_{GS} = -5$V in (b), and $V_{GS} = -10$V in (c).

The output characteristics and resistivity data demonstrate that the nominally-undoped SiNWs grown using the AAO membranes have a significant p-type background carrier concentration that must be compensated by the addition of phosphorus during VLS growth to produce n-type SiNWs. In these studies, a [PH₃:SiH₄] greater than 2×10⁻⁵
was required to achieve n-type conduction. The unintentional acceptors incorporated in the wires likely originate from either the AAO membranes or the electrodeposited gold that were used for VLS growth. The AAO membranes used in this study were fabricated by partial anodization of aluminum (Al) foil followed by wet etching of the remaining Al to form a free-standing membrane. It is possible that residual amounts of Al\(^{23}\), a shallow acceptor in Si, remained within the membrane following anodization and were incorporated into the wires during VLS growth. However, it was not possible to use SIMS to detect Al in the SiNW samples directly due to the large Al background signal from the alumina membrane that was present during the measurement. Alternatively, oxygen is also a shallow acceptor in Si\(^{24}\) and could be incorporated in the NWs during growth from H\(_2\)O absorbed within the membrane pores. Further studies are underway to identify and reduce the unintentional acceptor concentration in the SiNWs.

### 2.5.3 Substrate effect on doping efficiency

Four-point resistivity as a function of dopant to SiH\(_4\) gas flow ratio for SiNWs grown on SiO\(_2\) substrates was also investigated and is plotted in Figure 2.18. As shown in Figure 2.18, the nominally-undoped SiNWs grown from SiO\(_2\) substrates have a much higher resistivity of ~ \(10^5\) Ω-cm than those grown out of AAO membranes. Furthermore, in contrast to NWs grown from AAO membranes, the PH\(_3\)-doped ([PH\(_3\):SiH\(_4\)] = 2×10\(^{-5}\)) SiNWs grown on SiO\(_2\) substrate have n-type rather than p-type properties because of sufficient compensation to the p-type background doping from PH\(_3\) dopants. These results suggest that these NWs have a lower p-type background doping concentration, which could be due to the impurities from AAO membrane or the electrodeposited Au catalyst incorporated into SiNWs during VLS growth. In addition to smaller p-type background...
doping, the SiO$_2$ substrate with thin Au film as catalyst for VLS growth is relatively easy to fabricate compared with the AAO membrane. Thus, SiNWs grown from SiO$_2$ substrates are used for the rest of the thesis work unless otherwise specified. Finally, it is important to note that nominally-undoped SiNWs grown on SiO$_2$ substrates behave p-type properties indicating very low p-type background doping which could be due to the incorporation of Au catalyst into the SiNWs during VLS.

![Figure 2.18](image)

**Figure 2.18** Summary of four-point resistivity as a function of dopant to SiH$_4$ gas ratio for SiNWs grown on SiO$_2$ substrate.

### 2.5.4 Gate dependent four-point resistance measurement

As mentioned in section 2.5.1, the device operation mechanism of back-gated SiNW FET structures is due to a combination of field induced depletion of the SiNW channel and gate modulation of Schottky barrier at S/D contacts. Gate dependent four-point resistance measurements were conducted to study the effect of field induced modulation of the Schottky barrier during the back-gated field effect measurement. As
shown in Figure 2.19 (a), the four-point resistance of nominally-undoped SiNWs increases as the gate voltage increases (e.g., depletion width increases as the gate voltage increases), which is consistent with depletion mode operation of p-channel FETs and substantiates that the SiNWs are p-type. As shown in Figure 2.19 (b), the resistance of

![Figure 2.19](image-url)

**Figure 2.19** Four-point resistance as a function of global back gate voltage for (a) nominally-undoped and (b) [PH$_3$:SiH$_4$]=7×10$^{-5}$ doped SiNWs, which indicates that the depletion width of SiNWs changes when the global back gate voltage is changed.
PH$_3$-doped ([PH$_3$:SiH$_4$] = 7×10$^{-5}$) doped SiNWs increases as the gate voltage decreases (e.g., depletion width increases as the gate voltage decreases) which is consistent with depletion mode operation of n-channel FETs and confirms that the SiNWs are n-type.

2.6 Summary

In summary, SiNWs have been grown successfully by Au-catalyzed VLS and integrated into a global-back-gated four-point test structure to investigate the dopant incorporation efficiency. Structural analysis by TEM shows that the intentionally-doped SiNWs are predominately single crystal with a ~ 2 nm native SiO$_x$ covering the NW surface even at high doping concentrations. Four masks were designed to fabricate a back-gated four point test structure that facilitates NW alignment on a large array of electrodes in order to compile statistically significant data sets. Four-point resistance and gate-dependent conductance measurements demonstrate that TMB and PH$_3$ can be used as a source of boron and phosphorus for in-situ p- and n-type doping of SiNWs. The SiNW resistivity decreased by approximately three orders of magnitude as the [PH$_3$:SiH$_4$] was increased from 0 to 2×10$^{-3}$, which is significantly larger than the decrease determined for comparable gas flow ratios of TMB. Gate-dependent conductance measurements indicate that a [PH$_3$:SiH$_4$] greater than 2×10$^{-5}$ is required to compensate the unintentional p-type background doping and transition from p- to n-type conduction for SiNWs grown out of AAO membranes. However, the nominally-undoped SiNWs grown on SiO$_2$ substrates have much higher resistivity, which suggests lower p-type background doping concentration. Moreover, P-doped ([PH$_3$:SiH$_4$] = 2×10$^{-5}$) SiNWs grown on SiO$_2$ substrate show n-type properties in contrast to SiNWs grown using the same PH$_3$ to SiH$_4$ gas flow.
ratio using AAO membrane. These results suggest that the impurities from AAO membrane are incorporated into SiNWs during VLS growth, which is not desired for many applications such as FETs. Finally, the nominally-undoped SiNWs grown on SiO₂ substrate still show very low p-type background doping that could be due to the incorporation of Au impurities during VLS growth.

2.7 Bibliography

16 C. Eichfeld, J. Mattzela, S. E. Mohney and T. S. Mayer, unpublished results
Chapter 3

Thermal Oxidation and Top-gated Field Effect Devices

3.1 Introduction

Most of the previously reported nanowire (NW) field effect transistors (FETs) that were fabricated using unpassivated silicon nanowires (SiNWs) used the global-back-gated (GBG) test structure described in chapter 2. These devices typically exhibited poor gate modulation, high subthreshold slope, and large hysteresis in their subthreshold characteristics (e.g., drain-to-source current ($I_{DS}$) vs. gate-to-source voltage ($V_{GS}$) @ fixed drain-to-source voltage ($V_{DS}$)). An example of a back-gated FET using unpassivated SiNWs fabricated at Penn State University is shown in Figure 3.1. As observed, the On/Off ratio ($I_{On/Off}$), the on-state current ($I_{On}$) and the subthreshold slope ($S$) are $10^4$, 7 nA and 1.2 V/dec, respectively. Moreover, $I_{DS}$ vs. $V_{GS}$ varies with the gate voltage sweep direction and rate, which makes it impossible to extract accurate device properties such as threshold voltages ($V_{th}$) and field effect mobility ($\mu_{eff}$). This large hysteresis is most likely due to interface trap states between the SiNW and the underlying gate dielectric layer or surface states on the unpassivated SiNWs, which is most significant for small diameter SiNWs because of their larger surface/volume ratio. In order to overcome this problem, dry thermal oxidation was used here to produce a high quality oxide layer for passivating the SiNW surface, and to serve as the gate dielectric layer in top-gated (TG) SiNW FET devices. This thermally-grown oxide layer was chosen to serve as the top gate dielectric layer instead of high-$k$ material such as HfO$_2$ because it is well known that the thermally-
grown oxide forms excellent interface in planar Si with an average interface charge state density ($\sim 10^{11} \text{ cm}^{-2}\text{eV}^{-1}$). Moreover, dry rather than wet oxidation was chosen because it provides the highest quality Si/SiO$_2$ interface in planar Si.

![Graph](image)

**Figure 3.1** Subthreshold characteristics of global-back-gated unpassivated nominally-undoped SiNW FETs. Large hysteresis is observed when the gate sweep rate and direction change. The arrows show the gate sweep direction.

This chapter describes the dry thermal oxidation process of as-grown uniformly-doped SiNWs and the structural properties of resulting Si/SiO$_2$ core/shell NWs. It will also discuss the fabrication and electrical characterization of top-gated thermally-oxidized SiNW FETs. In section 3.2, samples oxidized at various oxidation temperatures and times were analyzed and compared with planar Si substrates to better understand the oxidation kinetics of SiNWs. Promising device characteristics, including significantly reduced hysteresis and better subthreshold slope compared with global-back-gated SiNW FETs, are obtained with these top-gated SiNW FET devices as discussed in section 3.3.
Electrical properties such as breakdown field strength and interface charge state density of the SiO₂ gate dielectric and SiO₂/Si interface are discussed as well. Moreover, a wrap-around gate structure fabricated by integrating a local back gate with the top gate structure was analyzed and showed further improved device properties.

SiNWs used in this study were synthesized by Dr. Kok-Keong Lew and Sarah Dilts using SiO₂ substrates coated with Au thin films. Transmission electron microscopy (TEM) analysis was performed by Dr. Bangzhi Liu.

### 3.2 Thermal oxidation of silicon nanowires

After the SiNW were synthesized by VLS as described in Chapter 2, the thermal oxidation of SiNWs was carried out by loading the substrate into a dry oxidation tube furnace. Before oxidation, the as-grown SiNW were placed in Au etchant type TFA (Transcene, Inc.) to remove the Au tips from the SiNW after a native oxide removal in buffered oxide etch (BOE). This native oxide layer, which covers the surface of SiNWs and the Au tip as shown in section 2.2 of chapter 2, must be removed to ensure that the Au tip is etched completely before oxidation. Au is not desired for device applications because Au can not only form deep level impurity states in Si, but it can also contaminate the oxidation furnace. Following Au tip removal, the well-known “standard” cleaning procedure (RCA) commonly used in planar Si substrates was applied to prepare the sample for dry thermal oxidation. The RCA clean is based on a two-step oxidation and reduction treatment using hydrogen peroxide solutions. The first solution (called SC-1) is a high-pH solution consisting of 5 H₂O:1 H₂O₂:1 NH₄OH in which the sample is placed at 70-80°C for 10 minutes. It is important to note that NH₄OH etches Si and this solution
can produce microroughening of the Si. The second solution (called SC-2) is a low-pH solution consisting of 6 H₂O:1 H₂O₂:1 HCl in which the sample is placed at 70-80°C for 10 minutes. RCA clean is very effective in removing contaminants from Si wafers and has been the mainstay of the industry for planar Si since 1970.⁸

In this study, the oxidation temperature was varied from 700°C to 900°C and the oxidation time was varied from 20 minutes to 12 hours. No HF treatment was performed after the RCA clean because it is known that non-purified HF is a source of metallic contamination⁵. The flow rate of trichloroethane/oxygen (TCA/O₂) mixture gas was maintained at 0.1 l/min during the oxidation. TCA was introduced during oxidation to serves as a source of Cl that reacts with many metal ions before and during oxidation. This has been shown to effectively reduce the interface charge state density in planar Si substrates⁵. A schematic of the oxidation furnace used in this study is shown in Figure 3.2. Ultra high purity argon (Ar) was used as purging gas during the temperature ramp up and down period. Finally, the oxidized SiNWs were released from the SiO₂ substrate by mechanical agitation and suspended in isopropyl alcohol (IPA) solution for further characterization.

### 3.2.1 Structural characterization

Transmission electron microscopy (TEM) was used to investigate the structural properties of the thermally-oxidized SiNWs. This included the Si core diameter, SiO₂ shell thickness, crystallinity and surface morphology. All of the images were collected in a JEOL 2010F high resolution field-emission TEM (HR-FETEM) operating at 200 kV. Figure 3.3 (a) and (b) show TEM images of representative nominally-undoped SiNWs
Figure 3.2 A schematic of the furnace used for dry thermal oxidation of SiNWs.

oxidized at 700°C for 4 hours with TCA flowing. These are the same conditions that were used to oxidize SiNWs for initial SiNW FET device fabrication. The schematic insets are used to illustrate the configuration of the NWs during TEM. Specifically, the oxidized SiNW shown in Figure 3.3 (a) is a plan-view image collected by dropping as-grown SiNWs onto lacey carbon grids. The sample shown in Figure 3.3 (b) is a cross-sectional image collected on a SiNW that was sectioned using a focused ion beam (FIB). Note that Ni was deposited on the surface of the NW for FIB sample preparation. The black color represents the Si core, while the green color represents the SiO2 shell. The contrast between the Si core and the SiO2 shell allows direct measurement of the oxide thickness and the Si core diameter and assessment of the interfacial roughness.

The SiNWs that were studied had an average diameter of 80 nm. Figure 3.3 (a) shows that the oxide thickness is ~ 9 nm and the interface between the SiO2 shell and the Si core is smooth and uniform. This indicates that the SiNW surface is not roughened considerably by the RCA clean and oxidation processes. Growth of the SiNW shown in Figure 3.3 (b) was along the <112> direction, and the long, flat regions at the SiO2/Si
interface viewed in cross section are \{111\} planes. \{220\} planes are also observed in the cross-sectional TEM image. Even though the cross section of the Si core shows that different crystallographic orientations are exposed on the surface of the NW, the SiO\textsubscript{2} shell is relatively uniform in thickness around the perimeter of the Si core with \(\sim 1\) nm variation which could imply that the variation in the rate of SiNW oxidation of different crystallographic faces is small\textsuperscript{9}. This is important for the study of SiNW oxidation kinetics because not all of the NWs could be imaged along the same orientation due to limitations in how far the TEM specimen holder could be tilted.

Device applications require a uniform SiO\textsubscript{2} shell along the entire length of SiNW because non-uniform SiO\textsubscript{2} shells could cause unwanted effects in FET device properties such as early oxide breakdown and variations in gate capacitance. Therefore, we conducted detailed TEM analysis on several SiNWs to investigate the uniformity of this SiO\textsubscript{2} shell along the length of the NW. Five TEM images taken on different segments of one SiNW oxidized at 700\degree C for 4 hours with an average length of 14 \(\mu\text{m}\) are shown in Figure 3.4. As indicated in the TEM images, the SiO\textsubscript{2} shell grown by the thermal oxidation is uniform and \(\sim 9\) nm in thickness. Moreover, the interface between the SiO\textsubscript{2} shell and Si core is smooth along the entire length of the SiNW.

TEM analysis on SiNWs oxidized at all other conditions investigated in this study shows similar uniformity and smoothness along the entire length of single crystal Si core. These data demonstrate that the thermal oxidation on SiNWs produces Si core/SiO\textsubscript{2} shell NW with structural properties that are suitable for electronic device applications.
Figure 3.3 (a) Top-view and (b) cross-sectional TEM images of nominally-undoped SiNWs oxidized at 700°C for 4 hours with TCA flowing. These images indicate that NWs have single crystal Si core with a uniform SiO₂ shell. Ni metal was used for focus ion beam (FIB) to prepare the sample for cross-sectional TEM analysis.
3.2.3 Oxidation kinetics

A series of oxidation experiments were conducted to investigate the oxidation kinetics of SiNWs including (1) SiO\textsubscript{2} shell thickness vs. oxidation time for 700 and 900°C with TCA introduced during oxidation, and (2) SiO\textsubscript{2} shell thickness vs. SiNW starting diameter for oxidation at 700 and 900°C for 2 and 4 hours with and without TCA. Planar lightly-doped Si (100) substrates were selected as control samples for comparison.

Figure 3.5 shows a plot of the SiO\textsubscript{2} shell thickness vs. oxidation time for two different temperatures, 700°C and 900°C, with TCA flowing during oxidation for SiNWs with starting diameters ranging from 30 to 80 nm. The starting diameter of all SiNWs in the plot was determined based on volume conservation, given by

\[ a_o^2 = \frac{b^2}{2.25} + \frac{1.25}{2.25}a^2 \]  

where \( a_o \) is the starting radius of SiNWs, \( b \) is the total radius after oxidation, \( a \) is the silicon core radius after oxidation. \( a \) and \( b \) can be obtained from TEM images of SiNWs after oxidation. For each oxidation condition, more than 10 SiNWs were analyzed by TEM. Because of the large diameter distribution of as-grown SiNWs, five starting diameter ranges, [30-39 nm], [40-49 nm], [50-59 nm], [60-69 nm] and [70-79 nm] were selected for both temperatures to show the dependence of SiO\textsubscript{2} shell thickness on the starting diameter. Solid symbols represent the data point for SiNWs oxidized at 900°C, while hollow symbols represent the data for SiNWs at 700°C. Results of planar Si substrates\textsuperscript{5} oxidized at these temperatures without the introduction of TCA during oxidation are plotted here using solid lines for comparison. The red, blue, and black lines denote data for planar Si (001) substrates oxidized at 700°C, (001) substrates oxidized at
900°C and (111) substrates oxidized at 900°C, respectively. Three clear trends are observed from these data.

Figure 3.4 TEM images taken at different positions along the same SiNW to examine the uniformity of the SiO$_2$ shell along the entire length of oxidized SiNW. The total length of the SiNW is ~ 14 μm. The Si core is shown in black color while the SiO$_2$ shell is shown in green color. The oxidation condition is 700°C for 4 hours with TCA flowing.
Figure 3.5 Oxide thickness as a function of oxidation time for different oxidation temperatures with TCA flowing. The starting diameter (nm) in the legend was calculated based on equation 3.1 using the SiNW dimensions obtained from TEM. Solid symbols represent the data for SiNWs oxidized at 900°C, while hollow symbols represent the data for SiNWs at 700°C. Red, blue and black lines denote previously reported data for planar Si (001) substrates oxidized at 700°C, (001) substrates oxidized at 900°C and (111) substrates oxidized at 900°C, respectively.

First, as shown in Figure 3.5, the average oxidation rate of the SiNWs oxidized at 900°C is approximately constant at ~ 36 nm/h for oxidation times less than 2 hours. The oxidation rate then decreases from ~ 15 to 10 nm/hr for oxidation times exceeding 2 hours. While these data also show that SiNWs with larger starting diameter have higher
oxidation rates at a given oxidation temperature, the same general trend in oxidation rate vs. oxidation time was observed for all of the SiNWs diameters studied. A similar, although less pronounced, trend was also observed for 700°C. In contrast, the average oxidation rate maintains relatively constant for planar Si substrates for all oxidation conditions investigated. According to Deal and Grove’s work\textsuperscript{10}, the oxidation rate on planar Si surfaces is limited by either the interfacial reaction rate or diffusion through the formed oxide layer. In our case, the oxidation rate of both SiNWs and planar Si substrates is limited by the interfacial reaction instead of oxidant diffusion because the oxide thickness for all conditions investigated is considerably less than that for which oxidant diffusion is dominant. The results of planar Si substrates are consistent with the oxidation model dominated by the interfacial reaction rate (e.g., linear relationship).\textsuperscript{10} However, it is well known that the interfacial reaction rate is also impacted by stresses introduced by different substrate geometries. It has been shown that an increase in normal compressive stress can decrease the interfacial reaction rate\textsuperscript{11} as explained by a simple equation,

\[ r \propto k_s \propto e^{-\sigma_s}, \sigma_s \propto \frac{1}{a^2} - \frac{1}{b^2} \]  

[3.2]

where \( r \) is the oxidation rate, \( k_s \) is the interfacial reaction rate, \( \sigma_s \) is the compressive stress, \( a \) is the radius of the Si core and \( b \) is the radius of the oxidized SiNW. For example, in the SiNW samples, the average oxidation rate was reduced from \( \sim 2.0 \) to 0.8 nm/h for 2 and 12h long oxidations at 700°C, and from \( \sim 14 \) to 10 nm/h for 2 and 4h long oxidations at 900°C. This reduction in oxidation rate can be explained by an increase in the normal compressive stress \( k_s \) on the SiNW with the increasing oxide thickness \((b-a)\).
Second, higher oxidation temperatures result in higher oxidation rates in SiNWs as plotted in Figure 3.5, which is consistent with planar Si substrates. For example, the average oxidation rate increased from ~ 2.5 nm/h at 700°C to 10 nm/h at 900°C for the SiNWs with starting diameter range [70-79 nm] after the same 4 hour oxidation.

Third, the SiO$_2$ shell thickness depends greatly on the starting diameter of SiNWs after a certain oxide shell thickness is exceeded for a given SiNW starting diameter. For example, the SiO$_2$ shell thickness varied from 23 to 40 nm (variation percentage ~ 23% which is the standard deviation divided by the median) on SiNWs oxidized at 900°C for 4 hours, which correspond to oxidation conditions that give the thickest oxide shells. Further inspection of these data shows that the thinnest oxide shells are found on the smallest diameter SiNWs (e.g., lowest oxidation rate), and thickest on the largest diameter SiNWs (e.g., largest oxidation rate). In contrast, the SiO$_2$ shell thickness is ~ 9±2 nm and only slightly dependent on the starting diameter for SiNWs oxidized at 700°C for 4 hours. It is important to note that even for the higher 900°C oxidation temperature, the variation is still small for thin SiO$_2$ shell thickness (e.g., short oxidation time). For example, the SiO$_2$ shell thickness is ~ 11±1 nm (variation percentage ~ 9%) and nearly independent of the starting diameter for SiNWs oxidized at 900°C for 20 min. These data can be explained by considering the increase in SiNW compressive stress with increasing SiO$_2$ shell thickness, which underscores the importance of accounting for the SiNW stress on the oxidation rate. The variation in SiO$_2$ shell thickness makes it difficult to obtain consistent device properties across large number of devices. Thus, for the initial field effect device studies, SiNWs were oxidized at 700°C for 4 hours to minimize the variation in oxidation shell thickness for different SiNW diameters at higher
temperatures. Such low temperatures have been show to produce inferior oxide quality, which will be the subject of future studies.

The effect of TCA on oxidation rate was investigated as well. A comparison of planar lightly-doped Si (100) control samples and SiNWs with diameter of 40 to 180 nm oxidized at 700°C for 4 h and 900°C for 2 h in the same tube furnace are shown in Figure 3.6. Figure 3.6 (a) shows that the average oxidation rate of samples oxidized with TCA flowing increases by approximately a factor of two from ~ 0.5 to 1.2 nm/h for the 700°C and from ~ 15 to 22 nm/h for the 900°C planar control samples. It has been suggested that the increase in planar Si substrate is due to TCA weakening the Si-Si dangling bonds and increasing the interfacial reaction rate. Figure 3.6 (b) shows a plot of the thickness of SiO2 shell vs. the starting diameter of SiNWs oxidized at 700°C and 900°C with and without TCA flowing. Results from planar Si substrates are shown as dashed lines in this plot for comparison. These data show that the introduction of TCA also enhances the oxidation rate of SiNWs. However, the increase of average oxidation rate for SiNWs oxidized without and with TCA flowing is not as significant as that of the planar Si substrates especially for 700°C oxidation temperature. For example, the average oxidation rate increases from ~ 1.7 to 2 nm/h at 700°C for a starting SiNW diameter of 40 nm and from ~ 6.8 to 8.2 nm/h at 900°C for a starting SiNW diameter of 75nm oxidized without TCA and with TCA flowing, respectively. The difference observed between the planar control samples and SiNWs could also be related to the change in interfacial reaction rate due to the compressive stress introduced during SiNW oxidation. Further studies must be conducted to investigate fully this effect. However, these results further
Figure 3.6 Oxide thickness as a function of temperature with and without TCA flowing for (a) planar Si wafers and (b) silicon nanowires.
emphasize that the stress induced during SiNW oxidation plays an important role in SiNW oxidation kinetics.

### 3.3 Top-gated thermally-oxidized uniformly-doped SiNW field effect device

Figure 3.7 shows a schematic diagram of the top-gated device structure fabricated using thermally-oxidized uniformly-doped Si/SiO$_2$ core/shell NWs. The source (S) and drain (D) electrodes contact the two ends of the uniformly-doped SiNW. The top gate is patterned on top of the thermally-grown SiO$_2$ shell that serves as the gate dielectric layer. A global back gate is also included in this device structure because it can be used to “electrostatically” dope the S and D as will be discussed in section 3.3.5. The mask layer design and detailed fabrication process are discussed in section 3.3.1. Electrical characterization was performed on more than twenty top-gated thermally-oxidized uniformly-doped SiNW FET devices at each dopant to silane (SiH$_4$) gas flow ratio (e.g., [TMB:SiH$_4$] = 2×10$^{-2}$, nominally-undoped, [PH$_3$:SiH$_4$] = 2×10$^{-5}$, 2×10$^{-4}$ and 2×10$^{-3}$).

**Figure 3.7** A 3-D schematic representation of the top-gated device structure fabricated using Si/SiO$_2$ core/shell NWs.
3.3.1 The mask layout design and fabrication process

The mask layout for the top-gated SiNW FET structure is slightly different from those used in the global-back-gated four-point test structure described in chapter 2. The mask layout used for nanowire alignment is shown in Figure 3.8 (a). Here, the 10×10 array of alignment electrodes is connected together with the large area probe pads. This design not only provides good SiNW alignment yield, but also simplifies the fabrication process significantly. The layout shown in Figure 3.8 (b) was used to define the S/D electrodes using electron-beam lithography. The spacing between S/D electrodes ranges from 6 to 8 µm. The layer shown in Figure 3.8 (c) was then used to electrically isolate the 10×10 array of electrodes by etching away the unwanted connecting electrodes. The layout of the top gate layer shown in Figure 3.8 (d) was used to define the top gate structure on the aligned SiNWs. The length of top gate varies from 1 to 3 µm. Finally, wrap-around gate devices were made by adding a local back gate on the bottom electrode layer and then overlapping the local back gate with the top gate. This additional layer was added in the 10th column of the array.

Top-gated uniformly-doped oxidized SiNW FETs were fabricated by integrating SiNWs onto n++-Si substrates (~ 0.001Ω-cm) coated on the topside with 100 nm of LPCVD grown silicon nitride (Si₃N₄) and the backside with 20/80 nm of Ti/Au, which served as the global back gate dielectric and electrode, respectively. Individual SiNWs were positioned between the pairs of large-area electrodes pre-patterned on the LPCVD Si₃N₄ layer with the layout shown in Figure 3.8 (a) using electrofluidic assembly as described in chapter 2. BOE 10:1 was used to remove the SiO₂ shell in the electron-beam lithographically defined S/D regions for intimate contacts prior to metalizing the S/D
regions using thermally evaporated Ti (100nm)/Au (100nm). The top gate was then formed by lifting off thermally-evaporated Ti (80nm)/Au (40nm) without removing the oxide layer, which served as the gate dielectric layer.
Figure 3.8 Mask layout for the fabrication of top-gated SiNW FETs. (a) Bottom layer used for SiNW alignment. (b) Electron-beam lithography layout to define the source and drain electrodes. (c) Isolation layer to isolate each device by etching away the unwanted electrodes. (d) Top gate layer to define the gate metal.

A top-view FE-SEM image of the finished top-gated device structure is shown in figure 3.9. This shows that the S/D contacts defined by electron-beam lithography contact a single SiNW that is aligned between two large area electrodes. The 1.5 μm wide top gate covers the middle segment of the SiNW and is 1 μm from the S/D contacts. The S/D spacing for all SiNW FETs on the mask varied from 6 to 8 μm, and the top gate length from 1 to 3 μm. The global back gate is on the back side of n++ Si wafer and is not shown in this FE-SEM image.
3.3.2 Electrical characterization

Figure 3.10 shows the subthreshold characteristics measured at zero back gate voltage for top-gated FETs fabricated using nominally-undoped SiNWs oxidized at 700°C for 4 hours. As determined by TEM, the SiO₂ shell thickness is ~ 9 nm for SiNWs oxidized at these oxidation conditions. In these SiNW FETs, the $I_{DS}$ decreases as $V_{GS}$ increases, which is consistent with depletion mode operation of a SiNW FET device with p-type background doping as discussed in chapter 2. The On-Off ratio $I_{On/Off}$, on-state current $I_{ON}$, and subthreshold slope $S$ are $\sim 10^4$, 40pA, and 0.3 V/dec, respectively. The subthreshold slope is much smaller than that (\sim 1.2V/dec) of the back-gated device with \sim 100 nm SiO₂ gate dielectric (see section 3.1) because of the improved electrostatic gating in the top-gate/thin SiO₂ shell SiNW FET.
Figure 3.10 Subthreshold characteristic of nominally-undoped thermally-oxidized SiNW FETs. No hysteresis is observed as the top gate (TG) voltage sweep rate or direction is varied.

The hysteresis observed in back-gated unpassivated SiNW FETs is suppressed in the top-gated oxidized SiNW FET as shown in Figure 3.10. In particular, characteristics measured during positive and negative sweep directions overlay and are also independent of the gate sweep rate. This can be attributed to the elimination of interface charges between global back gate and native oxide of SiNW and a significantly reduced interface trap state density at the SiO\textsubscript{2}/Si interface produced by dry thermal oxidation as compared to the interface between the SiNW and native oxide. Electrical characterization on non-oxidized and oxidized SiNWs in a back-gated FET structure also shows reduced hysteresis in latter case, which confirms that the interface trap state density at the SiO\textsubscript{2}/Si interface is reduced by dry thermal oxidation.

In contrast to the global-back-gated SiNW FET\textsuperscript{4}, the electrical characteristics of top-gated oxidized SiNW FETs are dominated by carrier depletion in the channel region.
because the S/D electrodes are not under direct control of the top gate. The band diagrams of the “ON” and “OFF” states are shown in Figure 3.11. However, the $I_{DS}$ of nominally-undoped SiNW FETs is still limited by an injection barrier (e.g., high parasitic resistance) at the S/D contacts to the lightly-doped NWs. In these devices, $I_{ON}$ is $\sim 10^{-10}$ A and much lower than that of heavily-doped NWs ($\sim 10^{-6}$ A). This makes extraction of the field effect mobility inaccurate even though the hysteresis in subthreshold measurements was eliminated.

![Band diagram of the “On” and “Off” states in top-gated thermally-oxidized SiNW FETs.](image)

**Figure 3.11** Band diagram of the “On” and “Off” states in top-gated thermally-oxidized SiNW FETs.

### 3.3.3 Electrical properties of thermally-grown SiO$_2$ gate dielectric

The leakage current of the SiO$_2$ gate dielectric was measured by applying voltage between the gate and drain electrodes and measuring current between them. As shown in Figure 3.12, the gate leakage current increases gradually with the applied gate voltage until oxide breakdown at $V_{GD} \sim 9$ V, which is defined as the intercept of the linear fit of abruptly increasing part of the IV curve to the x-axis as shown in Figure 3.12. The oxide breakdown field strength is estimated from the breakdown voltage of many devices and

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1 $V_{GD}$: gate-to-drain voltage
using the nominal oxide thickness of 10 nm to be 9.0±0.6 MV/cm, which is comparable to the oxide breakdown strength reported in planar Si devices\(^5\).

![IV curve measured between the source and top gate electrodes, which provides the leakage current through the SiO\(_2\) shell. The SiO\(_2\) breakdown voltage is \(\sim 9\) V.]

The interface charge state density \(D_{it}\) of the SiO\(_2\)/Si interface was estimated using the expression of subthreshold slope developed for planar Si devices\(^{14}\), given by

\[
S = \frac{KT}{q} \ln(10)(1 + \frac{C_D + C_{it}}{C_{ox}}) \tag{3.3}
\]

where \(C_D\) is the depletion capacitance, \(C_{it}\) is the interface charge capacitance and \(C_{ox}\) is the gate capacitance. Here, \(C_{ox}\) is calculated using the capacitance equation for a coaxial structure,

\[
C_{ox} = 0.75 \times 2\pi \varepsilon \varepsilon_0 L / \ln(b/a) \tag{3.4}
\]
where \( b \) is the radius of the SiNW including SiO\(_2\) shell and \( a \) is the radius of the Si core. A factor of 0.75 is included in equation 3.4 to account for the fact that only 75\% of the SiNW surface is covered by the top gate as shown in the cross-sectional TEM image of section 2.2. Using values of \( b \) and \( a \) determined by FE-SEM, the value of \( C_{ox} \) is calculated to be \( \sim 3.2 \) fF. \( C_D \) is estimated using a simple parallel plate capacitance equation,

\[
C_D = 0.75 \times \frac{2\pi \varepsilon \varepsilon_0 L}{d}
\]

where \( a \) is the radius of the Si core and \( d \) is the depletion width of the SiNW, which is dependent on factors such as applied gate voltage and doping of SiNW. Assuming a depletion width of 10 nm in nominally-undoped SiNWs with a diameter of 60 nm, \( C_D \) is calculated to be 1.5 fF.

Based on the equations above and the subthreshold slope, \( C_{it} \) is calculated to be 9 fF and much larger than \( C_D \) due to the large subthreshold slope (e.g., 0.3 V/dec) in the top-gated SiNW FET. The interface charge state density is then calculated to be \( 4.2 \times 10^{12} \) cm\(^{-2}\)eV\(^{-1}\) based on the equation given by

\[
Q_{it} = C_{it} / (A \times e)
\]

where \( A \) is the total area of the interface and \( e \) is the unit electron charge 1.6\times10^{-19}. This value is about a factor of two larger than that of planar [111] Si substrates \( (3 \times 10^{12} \) cm\(^{-2}\)eV\(^{-1}\) oxidized at 700\(^\circ\)C for 4 hours\(^5\), which could be due to different orientations of SiNW surface. This can be further improved by increasing the oxidation temperature and adding post-oxidation processes such as Ar and forming gas (H\(_2/N_2\)) annealing\(^5\).
3.3.4 Effect of TCA on electrical properties of top-gated SiNW FETs

As discussed in section 3.2, TCA was introduced during oxidation as a source of Cl. The Cl may be used to clean the furnace tube of metal contaminants prior to oxidation or may actually be used during the oxidation to react with many unwanted metal ions and produce gas phase byproducts. Electrical characterization of top-gated FETs fabricated using SiNWs oxidized without TCA flowing during oxidation at 700°C for 4 hours was also performed, and the subthreshold measurement results are plotted in Figure 3.13. As noted, the $I_{DS}$ vs. $V_{GS}$ curve shifts as the sweep direction of gate voltage is changed, which shows that the hysteresis is greater in the top-gated FETs using SiNWs oxidized without TCA flowing as compared with those oxidized with TCA flowing. Moreover, the subthreshold slope is increased to ~ 0.6 V/dec, which indicates this interface has higher

![Figure 3.13](image_url)

**Figure 3.13** Subthreshold characteristics of top-gated nominally-undoped SiNWs oxidized without TCA flowing at 700°C for 4 hours, which shows larger hysteresis. The arrows indicate the gate sweep direction.
charge state density. These observations indicate that TCA or similar Cl containing source should be used to reduce the interface charge state density during the dry thermal oxidation of SiNWs.

3.3.5 Electrostatic S/D doping

The global back gate in the top-gated SiNW FET device can be used to “electrostatically” dope the S/D and increase $I_{DS}$. This is achieved by suppressing the Schottky barrier between the S/D and SiNW, which allows carriers to tunnel through the barrier more easily as discussed in chapter 2. In Figure 3.14, by applying a constant global back gate voltage -10V applied during the measurements, the $I_{On/Off}$ is increased by two orders of magnitude from $10^3$ to $10^5$ and $I_{On}$ is increased from 50 pA to 80 nA. The subthreshold slope does not change because the global back gate does not alter the

![Image](image)

**Figure 3.14** The top and bottom curves were measured with a global back gate voltage -10V and 0V applied during the subthreshold measurement. This demonstrates that the global back gate can be used to “electrostatically” dope the S/D and increase $I_{On}$. 
interface charge state density at the SiO$_2$/Si interface. While this can be used to improve $I_{on}$, this is not practical for integrated devices. Moreover, this FET device structure can not be used extract accurate field mobility using electrostatic doping because the S/D current is still limited by the Schottky barrier. Finally, it is important to note that inversion mode operation of SiNW FETs can not be achieved by electrostatic doping.

### 3.3.6 Wrap-around gate structure

The device properties such as the subthreshold slope can be further improved by overlapping a local back gate with the top gate to form wrap-around gate structure. In the wrap-around gate structure, the gate surrounds fully the oxidized SiNW, which increases the gate capacitance by 25% according to equation 3.3. Figure 3.15 (a) and (b) show the subthreshold and output characteristics of nominally-undoped thermally-oxidized SiNWs in a wrap-around gate structure. The subthreshold slope is reduced to $\sim 0.2$ V/dec in Figure 3.15 (a) and as compared to $\sim 0.3$ V/dec in the top-gated SiNW FET structure. Moreover, in output characteristics, the saturation behavior is only observed for the negative bias $V_{DS}$ as shown in Figure 3.14 (b), which is consistent with depletion mode operation of p-channel FETs.
Figure 3.15 (a) The subthreshold and (b) output characteristics of oxidized nominally undoped SiNW FETs in a wrap-around gate structure. In (a), the curve was measured at fixed $V_{DS}$ 1V. For both (a) and (b), a global back gate voltage (-10 V) was applied constantly during the measurements. The subthreshold slope is reduced to $\sim$ 0.2 V/dec in the wrap-around gate device structure.
3.3.6 n- and p-type depletion mode silicon nanowire FETs

Top-gated FETs were fabricated using p- and n-type SiNWs oxidized at 700°C for 4 hours and characterized as shown in Figure 3.16 (a) and (b). Figure 3.16 (a) shows the subthreshold characteristics of SiNW FETs fabricated using lightly-doped n-type ([PH₃:SiH₄] = 2×10⁻⁵) and nominally-undoped SiNWs, which have a p-type background doping as indicated previously. For P-doped ([PH₃:SiH₄] = 2×10⁻⁵) SiNWs, the current increases as the gate voltage increases, which is consistent with the depletion mode operation of an n-type SiNW FET. The $I_{ON}$ of this FET is slightly higher than nominally-undoped SiNWs due to the higher doping. However, both types of SiNWs still have low $I_{ON}$ in the range of 1 to 10 nA because of the high parasitic contact resistances. In contrast, Figure 3.16 (b) shows the subthreshold characteristics of heavily-doped p-type ([TMB:SiH₄] = 2×10⁻²) and n-doped ([PH₃:SiH₄]=2×10⁻³) SiNWs plotted on a linear scale. These FETs have significantly higher $I_{ON}$ of ~ 1 µA and poor gate modulation (e.g., small $I_{On/Off}$ ratio) due to their higher carrier concentration that results in improved contacts between S/D electrodes and the SiNW (e.g., thinner Schottky barrier).

These results indicate that both p- and n-type top-gated thermally-oxidized SiNW FETs can be fabricated using in-situ doping by VLS. However, high $I_{ON}$ can not be achieved in lightly-doped SiNW FETs, while excellent gate modulation can not be achieved in heavily-doped SiNW FETs. To overcome these limitations in uniformly-doped SiNW FETs, n⁺-p⁻-n⁺ axially-doped SiNW was used to fabricate FETs in chapter 4. This structure is analogous to conventional doped source/drain (S/D) metal-oxide-semiconductor FETs (MOSFETs). Here, n⁺-doped SiNWs (e.g., [PH₃:SiH₄] = 2×10⁻³) segments are selected as the S/D contact regions to improve $I_{ON}$, while p⁻ doped SiNW
segments (e.g., nominally-undoped) are selected as the channel to achieve excellent gate modulation.\(^{15}\)

**Figure 3.16** (a) Subthreshold characteristics of oxidized nominally undoped and PH\(_3\)-doped ([PH\(_3\):SiH\(_4\)]=2x10\(^{-5}\)) SiNWs. (b) The subthreshold characteristics of oxidized TMB-doped ([TMB:SiH\(_4\)]=2x10\(^{-2}\)) and PH\(_3\)-doped ([PH\(_3\):SiH\(_4\)]=2x10\(^{-3}\)) SiNWs. For both (a) and (b), the \(V_{DS}\) was fixed at 1V and no global back gate was applied during the measurements.
3.4 Summary

In summary, the structural and electrical properties of thermally-grown SiO₂ are suitable for use as the gate dielectric in the top-gated SiNW FET device structure. TEM analysis on thermally-oxidized SiNWs indicates that the interface between the Si core and SiO₂ shell is smooth and uniform for all oxidation conditions and [PH₃/TMB:SiH₄] gas ratios investigated. Experiments conducted to investigate the oxidation kinetics of SiNWs show that the oxidation rate of SiNWs is limited by the interfacial reaction rate and the compressive stress induced during the oxidation. Moreover, the oxidation rate depends strongly on the SiNW starting diameter for oxidation conditions that result in thick oxide shells (e.g., > 20 nm). The enhancement of TCA on the oxidation rate of SiNWs is not as significant as that of planar Si substrates. These observations confirm the importance in accounting for stress and SiNW starting diameter in the SiNW oxidation kinetics.

Electrical characterization on SiNWs oxidized at 700°C for 4 hours reveals a breakdown field strength and interface trap density of the SiO₂ shell are 9.0±0.6 MV/cm and ~ 4.2×10¹² cm⁻²eV⁻¹, respectively. These values are similar to the best values reported in planar Si oxidized at same conditions, and can be further improved by higher oxidation temperature and post-oxidation processing. The significant hysteresis observed commonly in the global-back-gated structure is eliminated in the top-gated structure mainly due to both the passivation effect provided by the SiO₂ shell and reduced interface trap density in the top gate structure, which is the first step toward extracting accurate device properties such as $V_{th}$ and $\mu_{eff}$. A reduced subthreshold slope (0.3 V/dec) is shown in the top gate structure compared with the global back gate structure, which can be
further improved to 0.2 V/dec by the wrap-around gate structure. Both p- and n-channel top-gated SiNW FET devices have been demonstrated in this chapter. However, the trade-off between high $I_{ON}$ and high $I_{on/off}$ is hard to achieve using uniformly-doped SiNWs. To overcome these problems, axially-doped n+-p-n+ top-gated SiNW FETs were investigated and will be discussed in chapter 4.

3.5 Bibliography

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Chapter 4

Axially-Doped Silicon Nanowire Field Effect Devices

4.1 Introduction

As discussed in chapter 3, uniformly-doped p⁻ (nominally-undoped), n⁻ ([PH₃:SiH₄] = 2×10⁻⁵) and n⁺ ([PH₃:SiH₄]=2×10⁻³) thermally-oxidized SiNWs were integrated into a top-gated FET structure as illustrated in Figure 4.1 (a). The subthreshold characteristics for this device are superimposed and plotted in Figure 4.1 (b). For top-gated thermally-oxidized nominally-undoped SiNW FETs¹ ² the On/Off ratio $I_{On/Off}$, on-state current $I_{ON}$ and subthreshold slope $S$ are ~ 10⁴, 40 pA and 0.3 V/dec, respectively. For top-gated thermally-oxidized PH₃-doped n⁻ and n⁺ SiNW FETs the $I_{ON}$ is higher than nominally-undoped SiNWs due to the higher doping level. The lightly PH₃-doped n⁻ ([PH₃:SiH₄] = 2×10⁻⁵) SiNW FETs show similar device properties as nominally-undoped SiNW FETs, which indicates that the current of lightly-doped SiNW FETs is limited by the high parasitic resistance due to the non-ohmic S/D contacts. However, for highly PH₃-doped n⁺ ([PH₃:SiH₄] = 2×10⁻³) SiNWs in the same gate structure, the $I_{On/Off}$ and $I_{ON}$ are ~ 5 and 1 µA, respectively. Moreover, the four-point resistivity of uniformly-doped n⁺, n⁻ and p⁻ SiNWs grown using the same dopant to SiH₄ inlet gas flow ratios were ~ 1×10⁻³, 8×10² and 5×10⁴ Ω-cm, respectively, which further suggests much higher doping concentration of ([PH₃:SiH₄] = 2×10⁻³ doped SiNWs than nominally-undoped and ([PH₃:SiH₄] = 2×10⁻⁵ doped SiNWs.
Figure 4.1 (a) 3D schematic of top-gated uniformly doped oxidized SiNW FET structure. (b) The subthreshold characteristics of top-gated thermally-oxidized nominally-undoped, n' ([PH₃:SiH₄]=2×10⁻⁵) and n'+([PH₃:SiH₄]=2×10⁻³) uniformly-doped SiNW FETs. The nominal length of SiNWs is 14µm.

In order to obtain strong gate modulation and $I_{ON}$ simultaneously, axially-doped n⁺-p⁻-n⁺ SiNWs were grown by VLS in which the n⁺ segments at the NW tips were used to reduce the S/D contact resistance and increase $I_{ON}$. Strong gate modulation was obtained using the top gate to modulate the p⁻ segment. This device structure is similar to
the conventional planar Si-MOSFET and can be referred to as a “doped S/D SiNW FET”.
Here, a planar Si-MOSFET structure is demonstrated using axially-doped SiNWs, which
facilitates inversion mode operation and provides enhanced device performance.

These doped S/D SiNW FETs can be used as an excellent model system to
investigate the electron transport in inversion channel as the SiNWs are scaled in
diameter. In particular, three distinct regimes of transport can be studied using the same
NW material system as demonstrated in the schematic of Figure 4.2. In the first regime,
the SiNW FET should have behavior corresponding to a bulk semiconductor device,
where electrons are confined in the triangular well of the inversion layer. As the diameter
is scaled to ~ 10 nm, the inversion layer should penetrate the entire SiNW channel.
Finally, in the third regime, quantum confinement effects should become important
because of quantization in the x-y plane (i.e., cross-section) of the SiNW. This is
expected for SiNW diameters less than 3 – 5 nm.³

![Figure 4.2 Schematic and corresponding band diagram of the cross-section of SiNWs](image)

This chapter describes the VLS synthesis, structural properties, device fabrication
and electrical properties of top-gated FETs using axially-doped thermally-oxidized n⁺-p⁻-
n$^+$ SiNWs. Control samples with different S/D configurations in a global-back-gated test structure were fabricated as well to confirm that the axially-doped SiNW FETs operate by inverting the p$^-$ channel.

Transmission electron microscopy (TEM) analysis was performed by Dr. Bangzhi Liu. The VLS synthesis of axially-doped SiNWs was done by Sarah Dilts.

### 4.2 Synthesis of axially-doped SiNWs by VLS

The SiNWs used in these studies were synthesized by VLS growth technique as described in chapter 2. Axially-doped n$^+$-p$^-$-n$^+$ SiNWs with n$^+$ and p$^-$ segment lengths of ~ 6 and 1 µm were grown by sequential introduction of phosphine (PH$_3$) during VLS growth as illustrated in Figure 4.3. The PH$_3$ to SiH$_4$ gas ratio $2 \times 10^{-3}$ ([PH$_3$:SiH$_4$] = $2 \times 10^{-3}$), which is the highest ratio we investigated, was chosen for the n$^+$ regions to improve the contact to the S/D regions and facilitate the electron transport through the channel. The nominally-undoped SiNW, which exhibits p-type properties with light doping concentration, was chosen for p$^-$ region because it can be readily modulated by the top gate. The diameter of as-grown SiNWs ranged from 60 to 100nm.

![Figure 4.3 Dopant gas sequence during VLS growth for axially-doped SiNWs.](image-url)
4.3 Structural characterization of axially-doped SiNWs

Transmission electron microscopy (TEM) was used to investigate the structural properties of as-grown n⁺-p⁻-n⁺ SiNWs, including the diameter, crystallinity, and surface morphology. As shown in Figure 4.4, the axially-doped SiNWs are single crystal with ~2 nm native oxide on the surface and a dominant growth direction of [112], which is similar to that observed for the uniformly-doped SiNWs².

![Figure 4.4](image)

**Figure 4.4** A typical high resolution TEM image of as-grown axially-doped SiNWs.

The SiNWs were imaged at various points along their length and representative micrographs of a SiNW taken at different magnifications are shown in Figure 4.5. The transition from n⁺ to p⁻ and from p⁻ to n⁺ segments can be clearly identified from Figure 4.5 by noting changes in the diameter and surface roughness of the SiNW, which occurs over a transition length of ~3 nm. The diameter of p⁻ segment is 2% smaller than that of n⁺ segment, which could be due to the effect of phosphorus (P) on the wetting properties of the Au-Si alloy during VLS. Specifically, the change in diameter indicates that the
contact angle of the Au-Si liquid alloy to the SiNW changes when phosphorus is added or removed. This could also explain the slightly increased surface roughness of n\(^+\) segments compared with nominally-undoped segment, which was observed previously on uniformly-doped n\(^+\) SiNWs\(^2\). The TEM studies also showed no visible evidence of a radial overcoating of the p\(^-\) segment or topmost n\(^+\) segment of the SiNW. This is significant because it was reported previously that the introduction of different dopant gases can result in the deposition of amorphous or crystalline epitaxial layers on the surface of the SiNW segments\(^4\). Hence, a series of electrical control samples with different S/D configurations were fabricated and studied to confirm these conclusions. Finally, the length of each doped SiNW segment is consistent with the values expected from VLS growth calibration, which demonstrates our ability to successfully control the growth of axially-doped SiNWs.

As described in chapter 3, the as-grown axially-doped SiNW substrate was soaked in Au etchant solution TFA (Transcene, Inc.) for 3 hours to remove the Au tips after removing the surface native oxide using buffered oxide etch (BOE)\(^5\). Following Au tip removal, the standard cleaning procedure (RCA) was used to prepare the sample for dry thermal oxidation, which was carried out in a quartz furnace tube at 700\(^\circ\)C for 4 hours with trichloroethane (TCA) flowing.

Figure 4.6 (a) and (b) show representative thermally-oxidized axially-doped n\(^+\)-p\(^-\)-n\(^+\) SiNWs. Detailed TEM studies on more than twenty NWs show that the interface between the p\(^-\) SiNW segment and the ~8nm thick SiO\(_2\) shell is smooth and the oxide shell is uniform along the entire length of the p\(^-\) channel region. The oxide thickness is nearly the same as that measured on uniformly-doped SiNWs oxidized using the same
Figure 4.5 Structural characterization of axially-doped n\(^{+}\) ([PH\(_3\):SiH\(_4\)]\(=2\times10^{-3}\), L\(\sim7\)\(\mu\)m) - p\(^{-}\) (nominally-undoped, L\(\sim1\)\(\mu\)m)-n\(^{-}\) ([PH\(_3\):SiH\(_4\)]\(=2\times10^{-3}\), L\(\sim6\)\(\mu\)m) SiNWs. (Top) Schematic and low magnification TEM image of a typical n\(^{+}\)-p\(^{-}\)-n\(^{+}\) SiNW. (Middle) High magnification TEM image recorded in regions designated by the red box on the top TEM image. (Bottom) High resolution TEM images taken at the left n\(^{+}\), center p\(^{-}\) and right n\(^{+}\) segments in regions indicated by the white boxes on the middle TEM image.
conditions. The slightly increased surface roughness in n⁺ S/D regions is not expected to impact the device performance. These data demonstrate that the thermal oxidation of axially-doped SiNWs produces Si/SiO₂ core/shell NWs with smooth interface and well controlled oxide thickness.

4.4 Device structure and fabrication process

As illustrated in the schematic diagram Figure 4.7 (a), top-gated thermally-oxidized axially-doped n⁺-p⁻-n⁺ SiNW FETs were fabricated by integrating SiNWs onto n++-Si substrates (ρ ~ 0.001 Ω-cm) coated on the topside with 100 nm of LPCVD grown silicon nitride (Si₃N₄) and the backside with 20/80 nm of Ti/Au, which served as the global back gate dielectric and electrode, respectively. Prior to S/D metallization, which is thermally evaporated Ti(100nm)/Au(100nm), BOE 10:1 was used to remove the oxide shell in electron-beam lithographically (EBL) defined S/D regions using a timed etch. Non-self-aligned 4µm-long top gates comprised of Ti(100nm)/Au(100nm) defined by EBL were then deposited on top of the short p⁻ NW segment on top of the thermally-grown SiO₂ shell, which served as the top gate dielectric. A field emission scanning electron microscopy (FE-SEM) image of the finished device structure is shown in Figure 4.7 (b). Electrical characterization was performed on more than twenty SiNW FETs to account for variations in properties that could be introduced by differences such as SiNW alignment position, diameter, and gate metal coverage.
Figure 4.6 Structural properties of thermally-oxidized axially-doped SiNWs. (a) A TEM image of the p’ segment of the axially-doped n⁺-p’-n⁺ SiNWs thermally-oxidized at 700°C for 4 hours in dry oxygen ambient with TCA flowing. The nominal SiNW diameter following thermal oxidation is 60nm and SiO₂ thickness is 8nm. (b) High resolution TEM image recorded on the same SiNW showing the single crystal structure and smooth Si/SiO₂ interface.
Figure 4.7 (a) Simplified 3-D schematic representation and (b) FESEM image of the wrap-around and global back-gated thermally-oxidized n⁺-p⁻-n⁺ SiNW FET device structure. Wrap-around gates were formed by defining a local back gate before the NW integration. The top gate length is 4 µm and the LPCVD Si₃N₄ thickness on the n⁺⁺ Si substrate is 100 nm.
4.5 Axially-doped oxidized n^+-p^-n^+ SiNW FETs

4.5.1 Device properties

As determined from the subthreshold characteristics shown in figure 4.8 (a), the wrap-around gated thermally-oxidized n^+-p^-n^+ SiNW FETs had on-state current $I_{on}$ of ~1.3 µA @ $(V_{GS}-V_{th})$=1.2V, on-off ratio $I_{on/off}$ of $\sim 10^7$, threshold voltage $V_{th}$ of ~1V, subthreshold slope $S$ of $\sim 0.25$ V/decade, and transconductance $g_m$ of ~1.3 µS. The subthreshold (Figure 4.8 (a)) and output (Figure 4.8 (b)) characteristics of these SiNW FETs are consistent with the conventional n-channel inversion-mode MOSFET with $I_{on}$ and $g_m$ that are much higher than uniformly-undoped SiNW FETs (depletion mode operation with $I_{on} \sim 10$ nA and $g_m \sim 10$ nS). Since the p^- segment is under direct control of the top gate, the n^+-p^-n^+ SiNW FETs operate in inversion mode with dominant electron transport instead of hole in depletion mode. More detailed studies of $I_{on}$ dependence on the channel length are required to compare the channel resistance with S/D resistance and confirm this device structure is suitable for parameter extraction because the resistivity of each segment is a function of the gate bias. Nevertheless, the realization of SiNW-FET that operates in the inversion mode is a significant advance because it provides a convenient way to understand scaling effects in Si MOSFETs. This is particularly important to the scaling study of FIN field effect devices (FINFET) because they scale in diameter as well, while the scaling study of conventional Si-MOSFETs in planar structures mainly focuses on scaling in channel length.
Figure 4.8 The (a) subthreshold and (b) output characteristics of wrap-around gated thermally-oxidized n⁺-p⁻-n⁺ SiNW FETs that operate in the inversion mode.

4.5.2 Control samples with different S/D configurations

As discussed in section 4.3, there is the possibility of an n-type radial overcoating on the p⁻ segment due to the VLS growth process. Therefore, two different global-back-gated test structures were fabricated to confirm that this was not the case. Figure 4.9
shows these two test structures with S/D placed on p- or n+ regions of n+-p--n+ SiNWs. FESEM images of the finished test structures are shown in Figure 4.9 (a) and (b) as well.

The first configuration that is shown in Figure 4.9 (a) adds an additional source electrode between the drain electrode and the top gate. In this test structure, the contact to the n+ region can be tested by measuring the I-V characteristics between the electrodes labeled source and drain in figure 4.9 (a). Moreover, the subthreshold properties of this n+ NW segment can be characterized by applying back-gate potential, which can provide qualitative information regarding the doping density of the n+ segment. The top-gate covers the p- region of the SiNW FET. Thus, the axially-doped n+-p-p+ SiNW FET can be characterized by applying a potential between one of the electrodes contacting the SiNW on the left hand side and the source electrode on the right hand side of the gate. This measurement is identical to those done on the SiNW FETs as shown in Figure 4.7.

The second configuration shown in Figure 4.9 (b) and (c) incorporates two sets of source and drain electrodes and a global back gate. The first set of electrodes contact the n+ segments at the two ends of the SiNW, which is similar to the S/D configuration in top-gated axially-doped SiNW FETs excluding the top gate. These electrodes are labeled source and drain in Figure 4.9 (b). The second set of electrodes is in contact with the p- segment of the SiNW as shown in Figure 4.9 (c). This test structure resembles the back-gated nominally-undoped SiNW test structure discussed in the beginning of this chapter. Thus, this second set of electrodes can be used to confirm that the inversion stems from p- segment rather than a radial layer of n-type Si that coats the surface of the p- segment.
Figure 4.9 (a), (b) and (c) show different S/D configurations in a global back-gated device structure. (d) The subthreshold characteristics of global-back-gated n⁺-p⁻-n⁺ SiNW FETs with S/D configurations corresponding to (a), (b) and (c). In part (d), the S/D configuration labeled (a) is that of the back-gated n⁺-SiNW segment.

Figure 4.9 (d) shows the subthreshold characteristics of the global back-gated device structures with the S/D configurations corresponding to Figure 4.9 (a), (b) and (c). The subthreshold properties of S/D configurations (a) and (c) show that the FETs operate by depleting the p-channel and n-channel, respectively. In other words, for S/D configuration shown in Figure 4.9 (a), the current increases as $V_{GS}$ increases and the FET can not be completely turned off, which confirms that n⁺ segment is heavily doped. Moreover, the high on-state current confirms that the contacts are nearly ohmic or form a low barrier for injection of electrons into the channel of the FET. As described previously, the FET of Figure 4.9 (c) turns off with positive $V_{GS}$, which is consistent with depletion mode operation of p-channel FET. Thus, these electrical test results confirm that the surface of the p⁻ segment of the SiNW is not coated with an n⁻ Si layer. Finally,
the subthreshold plot of S/D configuration in Figure 4.9 (b) is similar to that of the top-gated axially-doped SiNW FET, which further indicates the device functions by inverting the p⁺ segment rather than by depleting the segment.

**4.5.3 Global-back-gated FETs using as-grown axially-doped SiNWs**

There also may be a concern that high temperature oxidation could cause dopant diffusion or redistribution along the NW and change the doping profile significantly. Therefore, as-grown axially-doped n⁺-p⁻-n⁺ SiNWs (non-oxidized) were integrated into a global-back-gated FET structure to investigate this effect. The device structure is illustrated in Figure 4.10 (a), which is essentially the same as the back-gated uniformly-doped SiNW test structure discussed in chapter 2. A typical subthreshold plot measured on back-gated as-grown (e.g., nonoxidized) axially-doped n⁺-p⁻-n⁺ SiNW FETs is shown in Figure 4.10 (b). Comparing these results with the top gated devices show in Figure 4.8 indicates that these SiNW FETs also operate by inverting the p⁻ SiNW segment with applied gate potential. However, a significantly higher applied gate voltage [-20V, 20V] is required because of the thicker gate oxide (~100nm) and global back gate configuration. This shows that the n⁺-p⁻-n⁺ SiNW devices circumvent the limitations of uniformly doped SiNW FETs whereby current injection into the channel is limited by the Schottky barrier between the contact metal and S/D. These results suggest that high temperature oxidation does not cause any large-scale dopant diffusion or redistribution.
Figure 4.10 (a) 3D schematic of global-back-gated non-oxidized axially-doped SiNW FET structure. (b) The subthreshold characteristics showing that high temperature oxidation does not cause large-scale dopant redistribution.

4.5.4 Statistical results

Measurements of more than ten 1µm long p’ channel SiNW FETs with diameters ranging from 66 nm to 83 nm showed good uniformity in $I_{on} @ (V_{GS}-V_{th}) = 1.5$ V and $V_{DS} = 1$ V) after normalizing device properties for variations in SiNW diameter and gate
dielectric thickness measured by FESEM. These data are plotted in Figure 4.11. Normalized $I_{on}$ shows less than a factor of two difference across all of the devices that were measured. The device-to-device consistency is substantially better than previous results collected on uniformly-doped SiNW FETs, which could be due to the improved S/D contacts and stability from the passivation provided by the thermally-grown oxide and the top or wrap-around gate structure. These improved properties and reproducibility are critically important for further studies of SiNW FETs, and provides an opportunity to extract accurate values of carrier mobility by studying SiNW FETs with varying channel length. This study is necessary because the channel resistance must be much higher than the S/D resistance and dominate the device operation to facilitate the device parameter extraction.

![Figure 4.11](image)

**Figure 4.11** On-state current per µm (width, divided by SiNW FET circumference) and normalized with variation of gate capacitance due to variation in oxide thickness.
4.6 Summary

In summary, we synthesized axially-doped n⁺-p⁻-n⁺ SiNWs with well-defined structural properties. The SiNWs were integrated into top-gated or wrap-around gated FET device structures using a thermally-grown oxide shell as the gate dielectric. Electrical measurements on conducted on the SiNW FETs show excellent device properties, and that the devices operate by inverting the p⁻ channel of the FET. Control samples using different S/D configurations in a global-back-gated test structure confirm that there is no n⁻ radial overcoating along the p⁻ segment and VLS growth and high temperature oxidation do not cause any large-scale dopant redistribution. This work demonstrates the potential for using SiNWs as a model system to investigate scaling on electrical transport in Si MOSFETs, especially for FINFET device structures.

4.7 Bibliography

Chapter 5

Summary and Future Work

5.1 Summary of the thesis work

This thesis described several significant advances in the integration and characterization of silicon nanowire (SiNW) field effect transistors (FETs), which will enable more detailed studies of NW scaling on device properties such as field effect mobility. First, a general integration process was developed to electrically address individual SiNWs, which is generally applicable to other group V, III-V, II-VI semiconductor NW building blocks. By applying this integration process in a global-back-gated SiNW test structure, the electrical properties of SiNWs such as four-point resistance and doping type were studied. Measurements of four-point resistance and gate-dependent conductance confirmed that the p- and n-type doping concentration of SiNWs grown using a Au-catalyzed vapor liquid solid (VLS) technique can be controlled by varying the inlet gas flow ratio of trimethylboron (TMB) or phosphine (PH₃) to silane (SiH₄). Moreover, gate-dependent conductance measurements indicate a p-type background doping in nominally-undoped SiNWs which can be decreased by using SiO₂ substrates. Large hysteresis was observed in the subthreshold properties of these global-back-gated test structures especially for lightly-doped SiNWs partly due to the unpassivated SiNW surface and the nature of the back gate structure.

Second, in order to eliminate the hysteresis observed in the global-back-gated SiNW test structure and obtain stable device operation, dry thermal oxidation of SiNWs
was used to passivate the SiNW surface and serve as the gate dielectric layer for top-gated SiNW FETs. A series of oxidation experiments were conducted to study oxidation kinetics of as grown SiNWs on SiO$_2$ substrates with an average 80 nm starting diameter by comparing the oxidation rate of SiNWs with that of planar Si substrates at temperatures ranging from 700 to 900$^\circ$C for various of oxidation time. Experimental results show that the oxidation rate of SiNWs is limited by the interfacial reaction rate and the compressive stress induced during the oxidation. Moreover, the oxidation rate depends strongly on the SiNW starting diameter for oxidation conditions that result in thick oxide shells (e.g., > 20 nm). These results suggest that the stress induced during SiNW oxidation plays an important role in determining the oxidation rate of the SiNW.

The electrical properties of the thermally-grown SiO$_2$ shell such as oxide breakdown field strength and interface charge state density were investigated as well and calculated to be $\sim 9.0\pm0.6$ MV/cm and $4.2\times10^{12}$ cm$^{-2}$eV$^{-1}$, respectively. These results are comparable to the best values reported in planar Si substrates oxidized at the same conditions. By using these uniformly-doped thermally-oxidized SiNWs, top-gated p- and n-type SiNW FETs were fabricated. The thermal oxide in conjunction with the top gate eliminated hysteresis in the subthreshold characteristics, and resulted in improved device characteristics such as smaller subthreshold slope as compared to the global-back-gated SiNW test structure. However, high on-state current $I_{on}$ can not be achieved in lightly-doped SiNW FETs because of high contact resistance while high On/Off ratio $I_{On/Off}$ can not be achieved in heavily-doped SiNW FETs because of weak gate modulation.

Finally, to overcome the trade-off between high $I_{on}$ and high $I_{On/Off}$, a conventional doped source/drain FET was fabricated using axially-doped n$^+$-p$^-$-n$^+$ thermally-oxidized
SiNWs. Electrical measurements of these devices show excellent field effect properties such as high $I_{on} \sim 20 \mu A/\mu m$, small subthreshold slope $S \sim 0.25 \ V/\text{dec}$ and high $I_{on/Off} \sim 10^6$. Most importantly, these SiNW FETs operate by inversion of the lightly doped p-channel, which is identical to operation of conventional doped source/drain (S/D) Si metal oxide semiconductor field effect transistor (MOSFET)\(^1\). In addition, excellent device-to-device reproducibility was observed for these SiNW FETs, which is important for collecting statistically significant data necessary for accurate parameter extraction. This is important for future studies of SiNW FETs, which will focus on the effect of diameter scaling on their electrical transport properties.

### 5.2 Future work

Most of the results presented in this thesis use SiNWs with a mean diameter of 60 nm. Future work will focus on small diameter SiNWs ($< 10 \ nm$) because this length scale is required to probe the 1-dimensional (1D) regime where interesting and potentially important transport effects may occur. For example, 1D transport has been predicted to increase electron mobility in NWs due to the suppression of scattering by the reduced phase space of 1D systems\(^2\). More recently, however, it was suggested that 1D mobility would decrease because the increased electron-phonon coupling in a 1D system offsets the reduction of phase space\(^3\). Thus, it is clear that the theoretical understanding of transport in 1D systems is still uncertain, with several issues still being debated. Other interesting behaviors such as quantum confinement, coulomb blockade and ballistic transport may be observed as well.
As a first step toward investigating electrical transport in ultra-scaled NWs, sub-10 nm diameter SiNWs grown using 10-nm diameter Au nanoparticles as described in chapter 2 were synthesized. TEM analysis indicates that the resulting NWs are ~ 10-nm in diameter, and are single crystal with very thin native oxide layer on the surface as shown in Figure 5.1 (a). These results are similar to those observed on large-diameter SiNWs discussed throughout this thesis. These nominally-undoped small diameter SiNWs were integrated into a global-back-gated test structure using the process discussed in chapter 3 as demonstrated in the inset of field emission SEM (FE-SEM) image of Figure 5.1 (b). It should be noted that the etch time required to remove the native oxide on the surface of these small diameter SiNWs needs to be controlled carefully to avoid etching the entire NW. The initial subthreshold measurements results given in Figure 5.1 (b) indicate that these SiNW FETs can be effectively modulated with $I_{on} \sim 1$ nA, $S \sim 0.7$ V/dec and $I_{on/off} \sim 10^2$. The preliminary experiments shown here are currently being extended to axially-doped SiNWs as described in chapter 4 to further enhance their FET properties. Finally, more careful studies of the dependence of SiNW FET properties on channel length and accurate measurements of gate capacitance must be completed to extract accurate values of field effect mobility as a function of SiNW diameter.
Figure 5.1 (a) A typical TEM image of as-grown small diameter SiNWs using Au nanoparticles. The diameter of the SiNW is ~8 nm. (b) The subthreshold characteristics of nominally-undoped sub-10 nm SiNW FETs in a global-back-gated four-point test structure as shown in the inset.
5.3 Bibliography

VITA

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Yanfeng Wang was born on December 2nd, 1976 in Liaoning province, China. He attended the Eighth High School of City Anshan in 1992 and graduated in 1995. He was then admitted to Tsinghua University, Beijing, China. In July 1999, he graduated with a Bachelor of Science degree in Applied Physics from Tsinghua University and was awarded as honor undergraduate student.

In September 1999, he enrolled in the master program of Microelectronics Institute, The Chinese Academy of Sciences, Beijing, China. His master thesis includes designing and fabricating 2.5Gb/s monolithic tranimpedance amplifier using InGaP/GaAs heterojunction bipolar transistors under the guidance of Professor Dexin Wu. He received a Master of Engineering degree in Microelectronics and Solid-State Circuits from The Chinese Academy of Sciences and was awarded as distinguish graduate in July of 2002.

After completing his master degree, he joined Professor Theresa S. Mayer’s group in Department of Electrical Engineering, The Pennsylvania State University, USA to pursue his Ph.D.. His research interests and scientific contributions mainly focused on integration and characterization of silicon nanowire field effect devices.

He is a student member of both The Institute of Electrical and Electronics Engineers (IEEE) and Material Research Society (MRS). He has authored and co-authored more than eight journal papers and has given seven conference presentations.