SILICON NANOWIRE GROWTH AND TRANSISTOR FABRICATION BY
SELF-ASSEMBLING “GROW-IN-PLACE” APPROACH

A Thesis in
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ABSTRACT

Nanowires have attracted much attention recently owing to their ability to serve as critical building blocks for emerging nanotechnologies. Silicon nanowires (SiNWs) are particularly promising because of the central role of silicon in semiconductor industry. SiNWs would allow device fabrication with high density and their high surface to volume ratio offers high sensitivity. In addition, the possible quantum confinement in SiNWs may further enhance device performances and open windows for exploiting fundamental properties. Intense researches have been carried out in SiNW growth and device fabrication. However, there are still challenges in SiNW growth controls, such as size, number, shape, position, orientation, and inter-wire spacings. To make devices from these SiNWs, post-growth processing steps are needed, such as SiNW collecting, picking, positioning, aligning, and assembling. Due to the extremely small size of SiNWs, there are also challenges in SiNW device fabrication.

To solve these challenges in both SiNW growth control and device fabrication, we introduced a novel self-assembling “grow-in-place” approach. Our approach combined vapor-liquid-solid (VLS) nanowire growth mechanism and pre-fabricated nanochannel template. The VLS growth mechanism offers the ability of controlling nanowire size and shape by nanochannel templates. The pre-fabricated nanochannel template guides nanowire growth and offers good SiNW growth control. SiNWs and silicon nanoribbons (SiNRs) with different sizes have been successfully grown in our nanochannel templates. Characterizations on their size, shape, composition, and crystallinity of the SiNW/Rs have confirmed that our “grow-in-place” approach offers
good controls on crystalline SiNW/Rs size, shape, number, orientation, position, and inter-wire spacing. So our approach solved the challenges in SiNW growth control.

Our grow-in-place approach also solved the challenges in SiNW device fabrication. We introduced two versions of nanochannel templates. The first one is the encapsulated/long nanochannel template. The nanochannels in these templates are long and SiNW/Rs grow inside these nanochannels. The grown SiNW/Rs are totally confined by the nanochannels, which offer total and precise control on SiNW growth. The electrodes can be built-in to the templates before SiNW growth. The growing SiNWs are self-positioned, self-assembled, and self-contacted with the built-in electrodes. After SiNW growth, SiNW devices are ready, without any post-growth processing and fabrication steps. The second one is the extruded/short nanochannel template. The nanochannels in these templates are short, only “nurse” the initial growth of SiNWs, and guide SiNW growth out of nanochannels. SiNWs are fixed by the extruded/short nanochannels for easy device fabrications. So there are no post-growth device fabrication difficulties. SiNW transistors have been successfully fabricated from our grow-in-place SiNWs. The transistors showed high performances with on/off ratio of $10^6$ and subthreshold slope of 130 mV/dec. In addition, a new accumulation type transistor model and configuration were proposed to build device model and extract carrier mobility.

As a summary, our novel “grown-in-place” approach allows us to produce self-assembled and self-positioned crystalline SiNW/R devices directly from a silicon precursor gas (e.g., SiH$_4$), without any intervening silicon material formation or collection, positioning, assembling steps. Our approach offers a way to make size controllable, position-controllable, contacted nanowires in an environmentally safe way.
and to assemble the nanowires into rational device geometries. These templates can be an integral component of the final devices and can provide contacts, interconnects, and passivation/encapsulation. The approach results in self-assembly of the SiNW/Rs into interconnected devices without any “pick-and-place” or printing steps, thereby avoiding the most serious problems encountered in process control, assembly, contacting, and integration of SiNW/Rs for IC applications. The approach we have developed is also environmentally safe since the fabricated nanowires are always confined and only the exact number needed is fabricated. In addition, the application of our approach is not limited in SiNW growth control and transistor fabrication. Nanowires from other materials, such as Ge and ZnO₂, and other devices, such as sensors, could also be developed from our grow-in-place approach.
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To My Parents and My Wife
Chapter 1

Introduction

1.1 Overview of one dimensional nanostructures

One-dimensional (1-D) nanostructures such as metallic and semiconducting nanotubes and nanowires have attracted much attention recently owing to their innate submicron feature size, to the potential for exploiting unique fundamental properties, and to their ability to serve as critical building blocks for emerging nanotechnologies [1]. Nanotube researches mainly focus on single wall or multi-wall carbon nanotubes (CNTs) [2][3][4]. Nanowires researches cover various nanowires from different materials, such as silicon nanowires (SiNWs) [5][6], germanium nanowires (GeNWs) [7][8], gallium nitride (GaN) nanowires [9][10], indium phosphide (InP) nanowires[11][12] and zinc oxide (ZnO2) nanowires [13][14].

Carbon nanotubes were discovered in the early 1990s and many efforts have been made to synthesize nanotubes and make devices by employing different methods. Interesting fundamental features have been found from carbon nanotubes, such as ballistic conduction at room temperature [2], the existence of coherent states extending over hundreds of nanometers [3], and Luttinger liquid behavior [4][15]. These CNT researches have also demonstrated the potential for CNT devices such as field effect transistors [16][17][18]. However, there are critical limitations of CNTs. First, the properties of CNTs, such as metallic or semiconducting, depend sensitively on CNTs’
diameters and helicity [19][20]. The growth of semiconducting nanotubes relies on chance observation [21]. It is not possible to control the growth of metallic or semiconducting nanotubes. Second, doping of the semiconducting CNTs is potentially critical for nanotube device applications. It is not possible to control the doping of the semiconducting CNTs. Semiconductor nanowires, however, can overcome these limitations of CNTs. These nanowires will remain semiconducting independent of diameters, and moreover, the doping of these nanowires can be well controlled by taking advantage of the vast knowledge from the semiconductor industry. In addition, the diverse axial nanowire heterostructures [22] and radial heterostructures [23] can be made from nanowires, which is another important advantage over CNTs. Nanowires from different materials have been heavily researched, including SiNWs, GeNWs, GaN nanowires and ZnO2 nanowires for different properties and applications.

Fig. 1-1 shows a nanowire example of dopant-free GaN/AlN/AlGaN radial nanowire heterostructures [24][25]. The GaN/AlN/AlGaN nanowire heterostructure consists of an intrinsic GaN nanowire core and undoped AlN and AlGaN shells as shown in Fig. 1-1a. The AlN and AlGaN shells were sequentially deposited around the GaN core by controlling the deposition condition to favor the homogenous deposition. The epitaxial AlN served as the interlayer to reduce alloy scattering from the AlGaN outer shell and to provide a larger conduction band discontinuity for better electron confinement [25]. In this heterostructure, the electron gas was confined at the GaN side of the heterostructure interface (Fig. 1-1b). The achieving of electron gases enables high performance nanoelectronics and to explore the fundamental properties of 1-D electron gases [26]. The radial nanowire heterostructures also offer opportunities for nanowire
optoelectronics applications with proper materials and doping for the core and shells. The radial core-shell nanowire heterostructures with efficient injection, radiative recombination, and tunable emission wavelength, present a great candidate for nanoLEDs and point a promising way to multicolor nanowire injection laser in the future \[27\].

![Image](image1.png)

Figure 1-1: GaN/AlN/AlGaN radial heterostructure nanowire. (a) Cross-sectional, high-angle annular dark-field scanning TEM image of a GaN/AlN/AlGaN radial nanowire heterostructure; scale bar is 50 nm. (b) Band diagram of a dopant-free GaN/AlN/AlGaN NW illustrating the formation of an electron gas (red region) at the core-shell interface confined by the epitaxial AlN/AlGaN shells.

Nanowires from different materials have been heavily researched. Among the possible nanowire materials, much of this attention has focused on SiNWs due to the central role of silicon in semiconductor industry. SiNWs in this thesis include silicon nanowires with nanometer in diameter and silicon nanoribbons (SiNRs) with nanometer in height.

1.2 Silicon nanowires

SiNWs are particularly attractive and promising due to the central role of silicon in the semiconductor industry, which would allow Si nanowires to be implemented using
existing technologies and equipments. The inherently small size of SiNWs allows device fabrication with extremely high density and the high surface to volume ratio offers high sensitivity. SiNWs also offer an ideal basis to study the effects of quantum confinement and its possible applications because the bulk properties of silicon are well understood [28]. The carrier types and concentrations in crystalline SiNWs could be controlled by doping, as in bulk Si [21]. In addition, at nanoscale, the motion of carriers in SiNWs could be confined, causing a possible transformation of the electronic band structure from indirect band gap to direct band gap [29][30], so SiNWs may emit visible light. More importantly, if such nanowires can be ordered and assembled into an appropriate architectural environment, then a host of nanoelectronic applications can be envisioned. It has been suggested that SiNWs might be used for developing 1-D high-performance field effect transistors [31][32] and bio/chemical sensors [33][34] with extremely low power consumption [35]. SiNWs can also be used to make single-electron transistors (SETs) [36][37]. They, therefore, can be used to determine the relationship between wire sizes and the electrical characteristics of SETs, which can significantly shorten the development time required to make SET practical devices.

1.3 SiNW applications

SiNW field effect transistors (FETs) are one of the most important SiNW applications, providing natural scaling and the potential for integration at the highest densities without additional complexity [38]. The field effect is the base of many device applications and the FETs’ dependency of conductance on gate voltages makes sensing
possible for single SiNW [39]. Studies of SiNWs have shown that nanowire devices can behave as excellent FETs with carrier mobilities in the SiNW devices comparable to or exceeding the best achievable values in planar silicon [33][40]. The high performances were believed partly due to the perfection of the “synthesized” nanostructures, the low dimensionality of nanowires, and other under-researched effects [41]. The “synthesized” SiNWs were grown through bottom-up approaches from elemental sources, instead of the fabricated nanowires formed by lithography or etching of the uniform silicon wafers. SiNW FETs with an on/off current ratio varying by many orders of magnitude for small changes in gate voltages have been demonstrated. These SiNW FETs can be used to assemble devices and circuits for an integrated computing system [31]. In addition, when the nanowire diameter is smaller than 5nm [42][45], the possible quantum confinement of carriers in SiNWs would further enhance the device performance and open windows for exploiting fundamental properties.

Among SiNW applications, SiNW sensing is another important application. SiNWs have extremely high surface to volume ratio which offers very high sensitivity. The diameter of SiNWs can be comparable to the sizes of biological and chemical species being sensed, and thus intuitively represents excellent primary sensing structures for producing signals that ultimately interface with macroscopic instruments [39]. Devices based on nanowires are emerging as a powerful and general class of ultra-sensitive, electrical sensors for the direct detection of biological and chemical species, such as PH sensors [31], protein sensors [39], DNA sensors [43], and even single virus sensors [44]. These sensors can function using simple conductance changes to sense and in this case are referred to as resistive-type sensors. Alternatively, they can be more complex and the
The underlying mechanism of these different nanowire sensors can be the field effect that can be amplified by using field effect transistors [33]. For FETs, the conductance between source and drain is controlled (switched on and off) by a third gate electrode capacitively coupled through a thin dielectric layer [46]. The dependency of conductance on gate voltages makes sensing possible for SiNW FETs. These type structures can function by having charges take place at the gate or in a solution playing the role of the gate. The electrical charges on or at the gate region resulting from the binding of charged biological or chemical species is analogous to applying a voltage to a gate electrode and introduces the change of the conductance of the FETs.

Fig. 1-2 shows a protein SiNW sensor [33][39]. Proteins are typically charged in aqueous solution. The SiNW can be modified with appropriate receptors (e.g., biotin for the case of streptavidin) and this receptor-modified SiNW can selectively bind with specific proteins (Fig. 1-2 A) and introduces the change of conductance (Fig. 1-2 B). The change of conductance can tell us the existence of specific proteins. If the SiNW is not modified by appropriate receptors, there will be no conductance change as shown in Fig. 1-2 C. This sensor offers a direct, label-free, real-time, and high sensitive protein detection tool.
Binding of bio or chemical agents to the surface of a nanowire FET is analogous to applying a gate voltage [39]. The binding can lead to the depletion or accumulation of carriers and subsequent changes of the nanowire conductance. With the extremely high surface to volume ratio and high performance nanowire FETs, nanowire offers high sensitivity on cancer molecule and even a single virus. Researchers have successfully demonstrated the detection of single cancer molecule [47] and single virus by using silicon nanowires. The nanowire sensors offer real-time, high sensitive detection of disease marker proteins at the femtomolar level [47]. The nanowire FET sensors can be readily integrated into electrically addressable sensor arrays and offer potential for powerful sensors. Nanowire FET sensors may greatly improve healthcare in the future. Most recently, researchers reported the detection, stimulation, and inhibition of neuronal signals with high-density nanowire transistor arrays [48] by using hybrid structures. The
hybrid structures consisted of arrays of nanowire field-effect transistors integrated with the individual axons and dendrites of live mammalian neurons. In the structures, each nanoscale junction was used for spatially resolved, sensitive detection, stimulation, and/or inhibition of neuronal signal propagation. Arrays of such nanowire-neuron junctions enabled simultaneous measurement of the rate, amplitude, and shape of signals propagating along individual axons and dendrites [48].

Radial composition and doping modulation in nanowire structures are other advantages of nanowires over carbon nanotubes and top-down lithography and offer more applications. These radial nanowire heterostructures may further enhance device performance and/or enabling new functions through controlled nanowire syntheses. Taking the undoped epitaxial Ge/Si core/shell structure as an example, a one-dimensional hole gas system has been demonstrated in the Ge nanowire core [49]. There is valence band offset at the Ge core and Si shell heterostructure interface as shown in Fig. 1-3. The band offset induces the potential confinement at the heterostructure interface and free holes accumulate in the quantum wall formed in the Ge channel when the Fermi level lies below the valence band edge of the Ge core. The unique transport characteristics of these heterostructures may make them excellent building blocks for the high performance nanowire field effect transistors and alternative for the conventional metal oxide field effect transistors. Researches on these heterostructures have shown that the scaled transconductance and on-current values are greater than state-of-the-art MOSFETs and the highest obtained values on nanowire FETs [49]. This research demonstrated the device performance enhancement through band-structure engineering for creating carrier gas by making nanowire radical heterostructures.
From the discussions above, nanowires especially SiNWs offer promising building blocks for applications. Researches have been carried out in both SiNW growth and device fabrication.

1.4 Thesis organization

The organization of this thesis is as follows:

Chapter 1 introduces 1-D nanostructures, SiNWs and their applications.

Chapter 2 introduces SiNW fabrication, challenges in SiNW growth control, and difficulties in device fabrication.

Chapter 3 introduces our novel self-assembling “grow-in-place” approach, describes our nanochannel template fabrication process, and demonstrates the controlled growth of SiNWs.

Chapter 4 introduces nanowire transistor structures, SiNW transistor fabrication in encapsulated/long nanochannel templates, and characterizations.

Chapter 5 introduces our extruded/short nanochannel template guided “grow-in-place” approach; describes extruded/short nanochannel template fabrication, SiNW
growth, and transistor fabrication; presents transistor characterizations, device model, and mobility analysis.

Chapter 6 summary and future work
References


Chapter 2

Silicon nanowire fabrication and challenges

2.1 Introduction

In recent years, many efforts have been made to fabricate or synthesize SiNWs and SiNRs (SiNW/Rs) by employing different methods. To-date SiNW/R fabrication or syntheses have two main categories, top-down fabrication and bottom-up fabrication.

2.1.1 Top-down approach and device fabrication

Top-down SiNW/R fabrication approaches took intense use of patterning and etching [1][2]. Dr. John A. Rogers’s group in University of Illinois at Urbana-Champaign (UIUC) has been doing researches on top-down silicon micro-/nano- 1-D structures and device fabrications [2][3][4]. These 1-D structures include micro-/nano- ribbons with nanometer height and micrometer width. Fig. 2-1(a-b) shows their fabrication processes [2][3].

Their way of making silicon 1-D structures has been taking use of silicon-on-insulator (SOI) wafers. The silicon film on the insulator is about 100nm thick. They used photolithography to define the silicon film and dry etch the silicon film to expose the buried silicon oxide underneath. The concentrated HF was used to etch the buried oxide and free the 1-D silicon structures. Their structures were actually silicon ribbons with
micrometer width and nanometer height (~100nm). Fig. 2-1c shows a scanning electron microscopy image of these silicon ribbons. To make devices from these silicon ribbons, they used two approaches as shown in Fig. 2-1a-b. The first one was the solution manipulation. In this approach, their silicon ribbons were etched, freed, and collected into solution. The silicon ribbons were then aligned by solution manipulation and devices were made from these aligned silicon ribbons. The second approach was dry transfer. In this approach, they used the HF etchant to etch the buried oxide. Comparing with the first approach, they controlled the etching time and did not totally free the silicon ribbons. A flat piece of polysdimethyisiloxaned (PDMS) was brought into conformal contact with the top surface of the wafer and then carefully peeled back to pickup the interconnected array of ribbons (Fig. 2-1b). The silicon ribbons attached on this PDMS can be transferred to other substrates, such as the polysethyleneteraphtalated (PET). To transfer these silicon ribbons onto this substrate, a spin cast dielectric layer of epoxy was spun on the PET at 3000rpm for 30s. The PDMS with silicon ribbons was then stamped onto the PET film. Because the bonding forces between the silicon ribbons and the soft epoxy layer was stronger than that between the photoresist and the PDMS stamp. The PDMS could be peeled off and left the silicon ribbons to the epoxy. This process finished the silicon ribbon transfer to the PET polymer substrate. This silicon ribbons fabrication and transfer offered silicon ribbon device fabrication on diverse substrates, especially flexible substrates. However, for these top-down approaches, there are several big disadvantages. The first one is that the using of SOI substrates made the device fabrication very expensive. There was only one layer of Si on the buried oxide of SOI, so the SOI substrate was only for one time use. In addition, the silicon etching was also a waste of
materials and further raised the cost for device fabrication. Second, the silicon etching might leave rough side walls to the silicon ribbons. Third, this approach is hard for small size of SiNR or SiNW fabrication, transfer, and device fabrication. They used photolithography, which only gave micro-scale resolution. Other methods, such as electron-beam lithography or nano-imprinting could be used to define the nanoscale patterns, but there would be challenges in nanowire transfer and post-transfer device fabrication, including nanowire positioning, aligning, assembling, source/drain and gate patterning, due to the small size.

Figure 2-1: Top-down silicon ribbon structure fabrication. [2][3]
2.1.2 Bottom-up approaches

In the bottom-up approaches, SiNWs have been grown or synthesized, instead of patterning and etching in the top-down approaches. A great advantage of synthetic SiNWs is that they inherently grow in nanometer size, without the need of complicated processes, such as lithography and etching. The bottom-up approaches offer single crystal SiNWs with good size control [5]. The composition and doping could be controlled during SiNW growth and the grown SiNW surfaces are smooth [6][7][8]. To date, SiNWs have been successfully prepared through different ways, such as thermal evaporation [9][10], laser ablation [11][12], and chemical vapor deposition (CVD) [13][14][15]. Most of these methods are based on the vapor-liquid-solid (VLS) nanowire growth mechanism which was first introduced by R. S. Wagner et al and applied to Si [16][17].

In the VLS nanowire growth mechanism as shown in Fig. 2-2, metal droplets (or slugs) such as, for example, Au and Fe in the case of Si, are generally used as the mediating/catalyst solvent. Gold is used often in the case of silicon because Au and Si can form molten eutectic alloy droplets (in liquid state) (Fig. 2-2A) at relatively low temperature (363 °C). Such a liquid alloy acts as a preferred sink or catalyst for arriving Si vapor, plasma, or gas precursor atoms, radicals or molecules present in a controlled ambient. The liquid alloy/sink absorbs Si and reaches super saturation. This liquid alloy/sink then excretes the solid Si nanowire. In the case of the Au/Si system, the arriving Si precursor from the vapor causes the Au eutectic liquid droplet to become supersaturated with Si, and the Si precipitates out at a solid-liquid interface (Fig. 2-2B).
The Si in the vapor phase continues to diffuse into the liquid alloy droplet while precipitating and bonding to the solid Si at the liquid–solid interface. By a continuation of this process, the standard SiNW VLS approach results in an alloy droplet, which becomes displaced from the substrate and ‘rides’ atop the growing whisker/wire (Fig. 2-2C). The result is the growth of Si whiskers or nanowires (Fig. 2-2D). The advantage of VLS growth method is that the cross sectional size (e.g. diameter for SiNW) and position of the SiNW can be pre-determined by the size and the position of the catalyst. In addition, the catalyst is in liquid state during nanowire growth by VLS methods, which offers the possibility of controlling the catalyst size and shape, subsequently the SiNW size and shape by templates.

Figure 2-2: Schematic of VLS SiNW growth.

Fig. 2-3 shows the experimental apparatus of growing SiNWs by the thermal evaporation approach [10]. The apparatus is composed by furnace (1), quartz tube (2),
quartz cover (3), ceramic boat (4), silicon vapor source (5) (e.g., pure silicon powder or bare silicon substrate), and catalyst-patterned silicon substrate (6). In this approach, catalyst particles or very thin catalyst film (e.g., Au or Fe as catalyst) can be applied onto the substrate and put into the ceramic boat (6). Silicon powder or just bare silicon wafer material as the silicon vapor source can be placed besides the substrate in the ceramic boat (5). At the temperature over 1000°C, the silicon powder or bare silicon can be vaporized and the vapor can be carried by the flowing Ar to the substrate for nanowire growth. This method is simple and direct; however, the required temperature is too high to be compatible with the existing processing in semiconductor industry. The high temperature may also cause a very serious diffusion of catalyst metal into both the grown SiNWs and substrate. If silicon powder is used, the silicon powder can also contaminate the substrate and the SiNWs grown on it. More importantly, the SiNW size and position can not be precisely controlled because the catalyst size and location are very hard to control, especially under high temperature.

Figure 2-3: Schematic of thermal evaporation apparatus.

Fig. 2-4a shows experimental apparatus of growing SiNW by laser ablation approach [11]. This apparatus is composed by a laser source (1), lens (2), a target containing silicon element and catalyst component (e.g. Si\textsubscript{0.9}Fe\textsubscript{0.1}) (3), a furnace (4), a
cold finger (5) for collecting grown nanowires, and flowing gas inlet/outlet (6). The
target can be put inside a quartz furnace tube in which the temperature and pressure can
be controlled. The laser beam generated from the laser source (1) is focused by lens (2)
on the target (3) and creates a hot, dense vapor of Si and Fe species for the case of
Si\(_{0.9}\)Fe\(_{0.1}\) target (see Fig. 2-4b). This hot, dense vapor can condense into small clusters
during collisions between the Si vapor, Fe vapor and flowing gas or by introducing
temperature gradient. The furnace temperature should be controlled to maintain over Si-
Fe nanocluster (“ball”) eutectic temperature (around 1200\(^\circ\)C) to keep this system in liquid
state. Fig. 2-4b shows a possible SiNW growth mechanism from this laser ablation
technique. Nanowires begin to grow after the Fe-Si liquid “balls” become supersaturated
in Si and continue to grow as more silicon enters the “balls”. The grown nanowires are
carried by flowing gas and collected by the cold finger (5). The Si-Fe “balls” solidify
when reach the cold finger and the nanowire growth terminates. For this approach,
nanowires grow from Si-Fe clusters in vapor and the size of the nanowires is defined by
the size of Si-Fe clusters. However, the size of the clusters can not be precisely controlled
and the size distribution may not be uniform because the catalyzing clusters are formed in
the vapor instead of the pre-patterned catalyst. In addition, the nanowires grown from this
approach are collected by the cold figure; the position of the nanowires can not be
precisely controlled as it can in approaches where the nanowire growth occurs where the
catalyst has been pre-located. So, this approach can not take the full advantages of VLS
mechanism of controlling size and position. It is also possible that the silicon vapor
which is not absorbed by Si-Fe clusters to form SiNW can be finally collected on the cold
finger and contaminate the SiNW batch.
For CVD approaches, precursor gases such as silane (SiH₄) can be used as the silicon source gas. The precursor gas (e.g., SiH₄) can decompose into Si and H₂, and Si can deposit out in specific ambient such as in H₂ under controlled pressure and temperature. The deposition can be a homogenous deposition without any selection or priority on the substrate, or heterogeneous deposition occurring at selected or preferred position established by a catalyst. These two processes coexist and compete with each other to varying degrees depending on deposition conditions such as temperature, pressure or catalyst. We can lower the pressure and temperature to reduce the homogenous deposition component; we can also introduce an effective catalyst such as gold to enhance the heterogeneous deposition at catalyst positions. The common catalyst process for Si is again a VLS process. In this case, the precursor gas decomposition occurs at the catalyst and Si is selectively produced on the surface of catalyst. At temperature above the eutectic temperature, the Si can be absorbed and diffuses into the
catalyst to form eutectic alloy (in liquid state). After the eutectic alloy gets supersaturated with Si, the silicon will deposit out and produce a silicon nanowire at the catalyst position.

Among the above-mentioned growth techniques, the CVD, especially low pressure chemical vapor deposition (LPCVD) VLS process has special benefits: it allows one to more easily control the nucleation sites as well as the growth process. The growth rate can be controlled well by controlling the pressure, temperature, gas flowing rate, and gas composition. By controlling these conditions, we can also minimize the contamination of silicon by minimizing the homogenous deposition comparing with thermal deposition and laser ablation method. In the approaches of this thesis, we mainly use LPCVD of diluted silane to prepare silicon nanowires in conjunction with the VLS process. Under low pressure, the silane gas has longer mean free path and can enter the deep channels we will be using allowing silicon nanowires to grow inside pre-fabricated nanochannel templates.

2.2 Challenges in SiNW growth control and device fabrication

The realization of the full potential of SiNWs demands the ability to accurately control the size, shape, number, position, orientation, and inter spacings of SiNWs and to assembly these nanowires into complex, electrically contacted structures and devices [18]. Until now, making devices from SiNWs usually involves a two-step synthesizing-and-then-positioning (“grow-and-place”) procedure for most approaches. For SiNW synthesis, precisely controlling the size, number, position, orientation, and inter spacings
of these synthesized nanowires have been practical problems. For most current SiNW growth methods, a huge number of SiNWs are usually grown or synthesized on the same substrate in messy conditions. There are still big challenges in SiNW growth control. After SiNW growth or synthesis, post-growth processing steps are needed to make SiNW devices from these nanowires. Due to the extremely small size of these SiNWs, there are significant challenges and obstacles in device fabrication, such as SiNWs handling, maneuvering, positioning, aligning, and assembling to form a complete system and to enable current flow between nanoscale and microscale structures. There are some techniques for handling, aligning and assembling SiNWs and making devices from these aligned SiNWs such as “surface patterning fluidic alignment” [19] and “electric-field assembly” [20] methods.

The surface patterning fluidic alignment techniques include fluid flow induced orientation technique [19], and Langmuir-Blodgett technique [21]. For these techniques, SiNWs grown on the substrate are first collected into solution by methods, such as scratching or ultrasonic vibration. Then the SiNWs in the solutions can be aligned by solution manipulations of surface patterning fluidic alignment techniques. Finally, devices could be made on these aligned SiNWs. Fig. 2-5 shows the schematic alignment procedure of the fluid flow induced nanowire orientation technique. In this technique, the synthesized nanowires were harvested and dispersed into a solution (Fig. 2-5a). The nanowires were aligned by passing the suspension solution of the nanowires through fluidic channel structures [19] (Fig. 2-5b), and then the electrodes were patterned by lithography and metal deposition after the microscopic search [22]. Fig. 2-5c shows a nanowire thin film transistor (TFT) fabricated on the aligned SiNW array.
Fig. 2-6 shows the schematic procedure of Langmuir-Blodgett technique [21]. By compressing the Langmuir-Blodgett trough, the nanowires in a monolayer of surfactant at the air-water interface were aligned to a specified pitch (Fig. 2-6a). Then the aligned nanowires were transferred to the surface of a substrate to make a uniform parallel array (Fig. 2-6b). Crossed nanowire structures could be made in the similar way by perpendicularly transferring second nanowire layer to the first layer (Fig. 2-6c).
In these techniques discussed above, SiNWs were formed on a growth substrate, harvested, sorted for size and length, positioned, aligned, fabricated into transistors, and contacted. Besides the difficulties in SiNW growth control and device fabrication, obtaining acceptable inter-device packing for practical applications was difficult too. A previous attempt to circumvent these grow-and-place steps is found in the “patterned growth” [23][24][25] approach. First proposed as a carbon nanotube growth-positioning approach [24], it has been used also for GeNWs [25]. Fig. 2-7 shows this patterned growth method. In this method, the catalyst islands were first defined by electron-beam lithography, catalyst solution patterning, and CVD nanotube growth. First, electron-beam lithography was carried out to open square holes in the e-beam resist PMMA as shown in Fig. 2-7a. Second, the catalyst solution was spun on and heat dried (Fig. 2-7b). The e-beam PMMA was then lift-off leaving the patterned catalyst islands (Fig. 2-7c). Finally, nanowires in a monolayer of surfactant were compressed on a Langmuir-Blodgett trough to a specified pitch and get aligned. The aligned nanowires can be transferred to the surface of a substrate to make a parallel array. Crossed nanowire structures can be formed by similar steps and perpendicularly transferring the second aligned nanowire film to the first aligned nanowire film.

Figure 2-6: Schematic of nanowire alignment by Langmuir-Blodgett technique.
CVD nanotube growth of methane at 1000 °C was carried out to grow nanotubes (Fig. 2-7d). An atomic force microscopy (AFM) image shows the nanotubes grown from the patterned islands (Fig. 2-7e). From this image, nanotubes grew from the patterned islands and some connected islands. The patterned growth approach gave some control on nanotube position for relatively easy device fabrication. There were fewer post-growth alignment and device fabrication difficulties. However, making devices from this approach involved three steps of electron-beam lithography, including alignment marker patterning, catalyst islands patterning and contact definitions. Multiple electron-beam writings and alignments excluded the mass manufacturability. In addition, the patterned growth method did not give any control over the number, direction, or inter-wire spacing of the nanotubes and nanowires produced.

Figure 2-7: Patterned growth approach. (a)–(c) Process flow for fabricating catalytic islands, (d) CVD nanotube growth. (e) Typical large-scale (scale bar: 2mm) phase image recorded by tapping mode AFM, showing carbon nanotubes grown from the patterned islands and bridging between islands.
To make SiNW devices, a few or even just a single SiNW is usually needed. However, the assembling techniques mentioned above usually just work for assembling a large number of SiNWs and even getting aligned nanowire films, such as with the Langmuir-Blodgett technique. It is really hard to pick a single SiNW or a few of them with the right size and length, align and assemble them into rational structures and devices. So there are still big challenges in assembling a single SiNW or a number of them into rational device geometries with desired positioning, contacting, orientation, inter-spacing, and to enable current flow between nanoscale and microscale structures. Also in addition to the positioning problems, there has been the potential health and safety issue of controlling the escape of nanowires into the environment [26]. To date, it remains challenges to grow size-controllable, position-controllable, and orientation-controllable, contacted nanowires whose environment confinement is assured. These problems can seriously restrict the future of SiNW applications.

Our objectives are to solve these problems by introducing a novel self-assembling “grow-in-place” approach. Our approach combines pre-fabricated nanochannel template structures, LPCVD nanowire growth, and VLS nanowire growth mechanism. The nanochannel template in our approach will guide and confine SiNW growth. By precisely defining the nanochannels, we can subsequently give good control on SiNW growth, such size, number, position, orientation, and inter-spacing of SiNWs. In addition, the grown SiNWs are fixed and confined by the nanochannel template, which allows SiNW growth to be precisely positioned, self-aligned, and self-assembled for easy device fabrication. Through our combination of templating, LPCVD, and VLS mechanism, we have nanowires growing only where we want them inside the nanochannels without the need
of nanowire releasing, picking and assembling. Our nanochannel template can be actually a part of the final device and the fabrication processing is compatible with conventional technologies of semiconductor industry. Contacts and doping sources could be built in to the nanochannel template as need for applications at hand. Or the contacts could be patterned and built after nanowire growth for optimizations, such as catalyst cleaning and surface passivation. So our grow-in-place approach solves the challenges in both SiNW growth control and device fabrication. Our approach is also environmentally benign with grown SiNWs always fixed and confined by nanochannel template. Only exact number of SiNWs needed is grown in the place where SiNWs are needed.

After demonstrating above nanowire growth control, it will be the further objective to make devices from our well controlled nanowires. Taking SiNW transistors as demonstrations, SiNW transistors will be fabricated and characterization will be discussed.
References


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Chapter 3

Controlled SiNW growth by “grow-in-place” approach

3.1 Introduction

Our novel “grown-in-place” approach to SiNW controlled growth uses a silicon precursor gas (e.g., SiH₄) to directly produce self-assembled/self-positioned, contacted crystalline SiNW/Rs without any intervening silicon material formation, collecting, positioning, or assembling steps. Our approach combines the LPCVD vapor-liquid-solid (VLS) growth mechanism and lithographically pre-fabricated, permanent, nanochannel growth templates to control the size, number, shape, orientation, position and inter-spacing of the SiNW/Rs. These templates are an integral component of the final devices and may provide contacts, interconnects, and passivation/encapsulation. The approach results in self-assembly of the SiNW/Rs into interconnected devices without any “pick-and-place” or printing steps, thereby avoiding the most serious problems encountered in SiNW/R growth control, assembly, contacting, and integration for IC applications. The approach we have developed is also environmentally safe since the fabricated nanowires are always confined and only the exact number needed is fabricated. Characterizations have been carried out to determine the size, shape, composition, and crystallinity of the “grown-in-place” SiNW/Rs. As an initial demonstration of our approach for device fabrication, we have fabricated SiNW/R resistors with built-in electrical contacts and did conductivity measurements.
3.2 SiNW growth in disposable alumina membrane

A different approach, nanowire growth in disposable templates instead of permanent nanochannel templates, has been undertaken by a number of groups. One of these is Dr. Joan Redwing’s group at Penn State. The work of Dr. Redwing’s group uses commercially available alumina templates to confine nanowire growth, and produces nanowires that are used after being freed by template dissolution.

Fig. 3-1 shows the schematic of nanowire growth in alumina membrane [1]. Commercially available anodic alumina membranes with a nominal pore diameter of 200 nm and thickness of 60 µm were used as templates in this study [2]. Fig. 3-1a shows the schematic cross section of the alumina membrane pore structure. To place catalyst Au into the pores, Ag layer was first evaporated to the backside of the alumina membrane as an electrode for electrodeposition (Fig. 3-1b), then a segment of Ag was electrodeposited into the pores followed by a thin (0.2–1.2 µm) segment of Au as shown in Fig. 3-1c. The Ag was then removed by etching in 8.0 M HNO₃, leaving only the thin Au segments near the center of the pores in the membrane (Fig. 3-1d). SiNWs can grow from these Au segments inside the pores with SiH₄ as the precursor gas inside a LPCVD system (Fig. 3-1e). After LPCVD VLS SiNW growth, the SiNWs inside the pores can be released by wet etching of alumina (Fig. 3-1f). Dr. Redwing’s group has demonstrated the fabrication of SiNWs using the combination of this disposable-template directed synthesis and VLS growth (Fig. 3-1g-h) [1][3]. The gold slugs inside the alumina membrane pores were catalyst for nanowire growth and the pores confined the nanowire growth. The use of the alumina membranes as the templates provides control over nanowire diameter while also
enabling the production of single crystal material [1][2][3]. The pores in the above alumina membrane approach offer some control on nanowire diameters. However, there are disadvantages to this and other similar dissolved/etched-away template approaches:

1. Usually the disposable templates which were employed in their approaches were commercially available anodic alumina membranes. The pore sizes in the membranes were relatively large and might not be precisely controlled. The pores might not be very straight and their size may not be precisely uniform. As a result, the size of the SiNWs produced inside these pores was also relatively large and not precisely

Figure 3-1: Schematic of SiNW growth in alumina membrane and SEM pictures
controlled, and the SiNW surfaces may not be precisely smooth. The large size precludes the opportunity for nanoscale phenomena such as quantum confinement.

2. To initiate SiNW growth in these pores, several electrodeposition steps were used to place gold slugs into the pores. To achieve this, Ag was first electrodeposited, then the Au was electrodeposited and finally the Ag was etched away. All of these steps used electroplating, which introduced environmental issues such as solution disposal and incompatibility with on-chip fabrication.

3. The alumina templates were disposed of (etched away) in their approach and could not be integrated with device assembly. After completing nanowire formation, the template must be etched away to free and then use the nanowires. Positioning, aligning, contacting, and assembling steps are still needed to make devices from these released SiNWs. It was very difficult to separate, move, electrically contact, if needed, align and assemble these freed nanowires into complex structures and devices. The positioning, aligning and assembling of these released nanowires remain challenges.

4. This process was not compatible with on-chip fabrication and assembly, and required post synthesis assembly of nanostructures to form more complicated devices.

5. The approach had the inherent issue of nanowire confinement during the nanowire growth from the alumina membranes, nanowire releasing, positioning, and contacting steps. These also raised the potential for uncontrolled nanowire release into the environment.
3.3 Controlled nanowire growth by grow-in-place approach

Our grow-in-place approach solves all the problems, gives good nanowire growth control, and offers easy nanowire device fabrication. Our approach combines VLS LPCVD nanowire growth, and pre-fabricated integrated/permanent nanochannel template for creating nano-structures such as nanowires of nanoscale diameters and nanoribbons of nanoscale thicknesses. The size, number, orientation, position, inter-spacing, and contacting of the nanochannel templates can be precisely controlled, resulting in the same control of the nanowires grown inside these pre-fabricated nanochannel templates. In addition only the exact number of nanowires needed is fabricated and they are always confined. We can make the nanochannel template where nanowires are needed and this template can be part of the final structure, so the nanowires are “grow-in-place” and no action is needed after the growth of nanowires - there is no separating, picking, positioning, aligning, and assembling. In our approach, the nanochannels in our templates need not be straight nanochannels. They can have branches, if advantageous to have branching nano-structures, and can have varying cross-sections. As will be discussed, contacts may be built-in if desired. Thus completed devices such as diodes, transistors, sensors, and transducers could be fabricated, contacted, and arrayed as nanowire or nanoribbon fabrication is completed. Most importantly, the template is not removed but is a part of the structure and nanowire confinement is complete.
3.3.1 Nanochannel template fabrication

The fabrication of nanochannel template structures has been significantly researched in our group [4][5][6]. The nanochannel templates have been fabricated by the combined use of electron-beam lithography and a sacrificial material etching technique. The use of electron-beam lithography allows nanoscale control of the nanochannel size (width and length), number, inter-nanochannel separation, and nanochannel orientation [6]. It also allows us to make nanochannels where they are needed. These nanochannels become the templates for nanowire or nanoribbon formation in this technique with the addition of the VLS mediator. The creation of the nanochannels dictates the nanowire or nanoribbon dimension, number, separation, and orientation. The position of the nanochannels also dictates the nanowire position. Contacts and doping sources can also be built into the nanochannel templates by simple photolithography.

The nanochannel templates can be fabricated on silicon substrate or glass substrate in similar way. Here silicon substrate is taken as an example for the nanochannel template fabrication. The overall process flow is shown in Fig. 3-2. First, open trenches of desired size (width and length), number, orientation, and position were patterned by electron-beam direct writing on an electron-beam resist film such as PMMA (3% 950K MW). The resist was on a silicon oxide layer that was grown thermally on a silicon substrate (or on bare glass if glass substrate was used). Second, titanium (1.5 nm) was e-gun evaporated as the adhesion layer and then gold was thermally evaporated to a desired thickness (e.g., 20 nm) defining the height of the nanochannels and thereby the height of the SiNWs to be grown. Subsequently, the resist film was lifted off to reveal the
gold lines on the substrate (Fig. 3-2a). Third, a silicon nitride capping layer was deposited over the substrate, patterned by photolithography, and selectively dry etched to open the nanochannel inlets (Fig. 3-2b). Finally, the gold lines buried under silicon nitride were controllably and partially removed by wet etching to form the nanochannels and also to leave short Au segments in the middle of the nanochannels (Fig. 3-2c). The Au lines serve as both sacrificial metal to define the nanochannels and catalyst metal for silicon nanowire growth. Fig. 3-2d shows the schematic of the nanochannel template after SiNW growth.

Figure 3-2: Process flow for nanochannel template fabrication and SiNW/R growth. (a) Sacrificial/catalyst metal (Au) lines defined by electron-beam lithography and lift-off. (b) Deposition and patterning of the capping layer. (c) Partial etching of the sacrificial metal to form the nanochannels with catalyst in the middle. (d) SiNW/R growth by the VLS mechanism.
3.3.2 SiNW growth in nanochannel templates

During the fabrication of nanochannel templates, we use a sacrificial material (e.g., Au for SiNWs) that is to be removed to create the open nanochannel template (see Fig. 3-2). However, one of the novel parts of our research is that the Au serves both as sacrificial metal for forming the nanochannels and the catalyst for VLS silicon nanowire growth. To accomplish this dual use of the Au, we need to etch away the gold sacrificial lines except for positioned Au catalyst slugs. The etching process begins from both ends of the gold nano-lines and progresses toward each opposite end. We can control the etching time and leave very small gold slugs in the nanochannels (Fig. 3-3a-b). These gold slugs serve as mediator/catalyst according to the VLS nanowire growth mechanism. SiNWs will grow in both directions from the center of the gold slugs. Fig. 3-3c-d show the schematic of SiNWs grown in the nanochannel template.

For this process, a standard Au etchant (type TFA from Transene Company, Inc.) was employed with 100 rpm stirring at room temperature. A typical etching rate for the 200 nm by 20 nm nanochannels was 1.6 \( \mu \text{m/min} \), while the etching rate was observed to decrease with decreasing nanochannel width (e.g., 1.3 \( \mu \text{m/min} \) for a 50 nm wide channels). The etching was stopped by immersion in DI water. A relatively short (e.g., 2-10 \( \mu \text{m} \)) length of Au (slugs) was retained (i.e., was not etched away) in the middle of the nanochannels to serve as the VLS catalyst for the SiNW growth (Fig. 3-3a-b). In some cases electrical contacts could be built into the nanochannels by contact metal depositions onto the sacrificial Au lines prior to nitride deposition and to Au etching [4]. In this way, we made a series of template nanochannels, 100 \( \mu \text{m} \) long and 20 nm high with different
widths from 20 to 200 nm, each accommodating an Au slug catalyst in the middle. For ease of observation and characterization, the nanochannels of each size (width) were fabricated and closely arranged in sets of five. VLS growth resulting in SiNWs was then carried out in a LPCVD reactor at 500 °C and 13 torr, using a 5% SiH₄ diluted in H₂ with a total flow rate of 100 sccm [1][2][5] (Fig. 3-3c). Because the nanochannels confined the Au catalyst and subsequently the nanowires grown inside, the growing nanowires would follow the size and the shape of the nanochannels. This results SiNWs in 20nm wide by 20nm high nanochannels and SiNRs in other nanochannels such as 200nm wide by 20nm high nanochannels.

Figure 3-3: Schematic representation of the catalyst slugs and grown SiNWs inside a nanochannel template. (a) Controlled and partial etching of the sacrificial metal to form the nanochannels with catalyst in the middle. (b) Top view of the gold slugs inside the nanochannels. (c) SiNW/R growth in LPCVD by VLS mechanism. (d) Top view of SiNWs grown inside nanochannels.
3.4 SiNW characterization and discussion

After SiNW/Rs have been grown in the nanochannel template, characterizations can be carried out on these SiNW/Rs to determine their size, shape, composition, crystallinity, and conductivity.

3.4.1 Optical microscope characterization

As we introduced before, we made a series of nanochannels, 100 µm long and 20 nm high with different widths from 20nm to 200nm (from right to left in Fig. 3-4) and closely arranged in sets of five for the nanochannels of each size. This configuration allowed us to check them under the optical microscope. Optical microscope images of our grow-in-place SiNW/Rs of various sizes self-assembled by VLS inside our permanent nanochannel templates are shown in Fig. 3-4. These images were taken through the nitride capping/encapsulation layer. We have found that, when the Au catalyst slugs in nanochannels were long (e.g., longer than about 10 µm in length), then SiNW/Rs grew at each end of the Au slugs (gold is seen as the brighter shade located in the middle of each channel) as shown in Fig. 3-4a. For this case, Si absorption and diffusion coexist and compete with each other. The top ends of an Au slug get supersaturated before Si can diffuse to the center. The silicon cannot saturate the whole gold slug, but locally saturates the tips of the gold slug. The result is two SiNWs or SiNRs, each growing from its own cap of the gold slug. These grow in the nanochannels with one SiNW on each side of a central Au slug seen in Fig. 3-4a. When the gold slug is shorter (e.g., 2 µm), the whole Au slug becomes saturated with Si and is split into two
caps. In this case there is only one growing nanowire and it has a cap located at each end. This leaves no central Au region, as seen in Fig. 3-4b.

3.4.2 AFM and FESEM characterizations for size and shape

We studied the size and shape of our SiNW/Rs with atomic force microscopy (AFM) and field emission scanning electron microscopy (FESEM). AFM is very helpful and accurate for height determinations of our grown-in-place SiNW/Rs, while it is less accurate in measuring widths due to the AFM tip angle (20°) and radius (15 nm) effects. Using a combination of AFM (Digital Instruments Dimension 3100) height
measurements and FESEM (Leo 1530) width measurements, the size and shape of our SiNW/Rs were determined. To perform AFM and FESEM, we had to remove the capping layer. This was done by using photolithography and etching. The former was needed to allow selective etching of only half of the capping layer, ensuring that the remaining half remained to immobilize the SiNW/Rs. Subsequently, FESEM and AFM were used to characterize the exposed SiNW/Rs. Fig. 3-5 shows the FESEM and AFM results.

Fig. 3-5a shows the FESEM overview image of the SiNW/R groupings from 200 to 20 nm in width (left to right) after capping layer removal. As in Fig. 3-5a, the brighter regions are gold slugs and the SiNW/Rs look darker. The Au slugs in narrower nanochannels are seen to be slightly longer. This may be attributed to the slower etching rate of the Au sacrificial/catalyst material due to the restricted diffusion of reactants and products during the wet etching process. Fig. 3-5 b and c show the 200 and 20 nm width SiNR and SiNW groups, respectively, in high magnification. From this FESEM work, the width for these ribbons and wires was measured to be 250 and 35 nm, respectively. Fig. 3-5 d and e depict the AFM height profiles for the 200 and 20 nm width ribbon and wire groups, respectively. As is seen, the height of the ribbons/wires is about 25 nm and is independent of the width, as desired, which was defined by the same Au deposition. Hence, both nanoribbons and wires of carefully controlled cross sectional dimensions are obtainable by our approach.
Figure 3-5: (a) FESEM image of SiNW/R group series having widths from 200nm (left) to 20nm (right). (b) FESEM image of a 200 nm width nanoribbon group. (c) FESEM image of a 20 nm width nanowire group. (d) AFM height profile of a 200 nm width SiNR group. (e) AFM height profile of a 20 nm width SiNW group. (f) AFM height profile of a single wire in the 200 nm width nanoribbon group.
The 3-D AFM image shown in Fig. 3-6 for the 200nm by 20nm SiNR group further confirms our nanochannel template control on SiNR size, number, shape, inter-spacing, position, and orientation. We believe that, since the growth front is liquid in the VLS method, it fills in the complete cross sections of the nanochannels during growth, thereby ensuring that the precipitating Si inherits the exact shape of the nanochannel volume. For the same reason, the interface between the grown Si and the built-in contacts should also be very conformal, minimizing the contact resistance as is observed and discussed below.

Figure 3-6: 3-D AFM image for 200nm by 20nm SiNR group.

3.4.3 Augur spectrum characterization for composition

The chemical compositions of the SiNW/Rs produced by our “grown-in-place” approach were also studied. This was accomplished by using a PHI 670 scanning Auger electron spectroscopy (AES) system. AES is a powerful surface characterization method for the study of chemical and compositional properties of materials. Because the basic
Auger technique samples a depth of typically 0.5 to 5 nm and the Auger scanning windows are small enough (smaller than 5 nm by 5 nm), AES can be used to characterize our nanowires/nanoribbons (around 25 nm thick from AFM results, 35 nm to 250 nm wide and 100 µm long) without the influence from the substrate and the signals were all from the nanowire/nanoribbon parts instead of the substrate. The base oxide layer (see Fig. 3-3 a) also assured that there was no influence on the AES measurements from the Si substrate. Fig. 3-7 (a) and (b) show the Auger spectra for the Au catalyst (brighter parts in Fig. 3-5 a) and SiNW/R (darker parts in Fig. 3-5 a and b) regions of the 200nm by 20nm nanoribbon. As seen in Fig. 3-7(a), the Au catalyst regions depict the presence of mainly gold (three characteristic peaks at 1771ev, 2022ev, and 2107ev) and silicon (two characteristic peaks at around 96ev, and 1621ev multiple peaks). This result confirms the diffusion of Si into the Au slugs rendering them Si-Au alloys. The Auger data from the Au regions (Fig. 3-7a) also showed weak peaks at ~275ev and ~510ev, which are characteristic of C and O. These two elements have probably originated from sample-handling surface contamination, since we were able to reduce their Auger signal by ion sputtering cleaning. On the other hand, as seen in Fig. 3-7(b) the Si regions (i.e., the nanoribbons) of 200nm by 20nm nanoribbon exhibit only the two silicon characteristic peaks and no Au characteristic peaks at all. Thus, the SiNRs consist of Si, at least to the detection limit of AES. Fig. 3-7(c) and (d) show the typical AES spectra for the brighter (i.e., Au slug) and darker (i.e., SiNW) regions for the 20nm by 20nm SiNWs. As seen, these are similar to those obtained for the 200 nm width nanoribbon group. These results confirm the grown nanowires and nanoribbons are SiNW/Rs and they are also consistent with microscope and FESEM results.
3.4.4 Raman characterization for crystallinity

The crystallinity of the SiNW/Rs was investigated by Raman spectroscopy. Raman spectra were collected by a double stage Dilor XY spectrometer equipped with a confocal microscope (Olympus BH-2) and a Princeton Instruments model LN/CCD-1024 TKB detector. The laser excitation of 514.5 nm and 6 mW was focused in the
backscattering geometry using an Olympus MSPlan 100×, 0.95 NA microscope objective to a spot size of approximately 2 μm. To optically isolate the underlying Si substrate, an additional process step was introduced into Fig. 3-2 for the samples used for Raman. This consisted of coating a reflective and opaque nickel layer (200 nm) on the silicon substrate prior to the fabrication of the channel templates as shown in Fig. 3-8.

![Figure 3-8: Nanochannel template with reflective layer for Raman characterization.](image)

This nickel layer was inserted and sandwiched between the substrate and oxide (Fig. 3-2a) before the oxide deposition. Fig. 3-9 shows the Raman shift spectra for our various width SiNW/Rs as well as for a <111> single crystal Si wafer for comparison. The Raman peak located within 518-521 cm⁻¹ for our SiNW/Rs is assigned to the first order optical phonon (at the Brillouin zone center) scattering in a Si lattice and identifies our SiNW/Rs as crystalline. However, this peak is slightly downshifted and asymmetrically broadened when compared to that in bulk single crystalline Si, as it can be seen in Fig. 3-9. In agreement with Piscanec et al.,[7] we attribute this downshift and asymmetric broadening of the Raman peak to intense local heating by the laser excitation and not to quantum confinement effects. As the “control” data of Fig. 3-9 show, no Raman peak was obtained when the laser beam was focused outside nanochannel regions.
(i.e., on the silicon nitride capping layer). This ensures that the Raman signals from nanowire groups are not attributable to the underlying Si wafer or any residual Si deposit on the capping layer.

3.4.5 IV measurement for conductivity

To demonstrate the potential of our grow-in-place approach for the self-assembling of interconnected devices and circuits, simple nanowire/ribbon resistor structures were fabricated by building electrical contacts inside the nanochannel templates prior to nanowire VLS growth in the template as shown in Fig. 3-10. To make

Figure 3-9: Raman spectra obtained for a single crystal silicon wafer, various size SiNW/Rs (widths from 30 to 200 nm), and the control region (as described in the text).
the nanochannel template with build-in contacts, the Au lines were first patterned by electron-beam lithography as shown in Fig. 3-2a. Second, the photoresist LOR5A/SPR3012 can be spun on. The build-in contacts were patterned on these photoresists by photolithography followed by metal depositions (1.5nm Ti as adhesion layer and 80nm Pt as electrode metal by e-guy evaporations). After lift-off, the structure shown in Fig. 3-10a was obtained. Third, the capping layer, such as silicon nitride, was deposited and patterned by photolithography. After capping layer etching, the structure shown in Fig. 3-10b was obtained. Finally, the Au lines was controlled etched and the nanochannels were formed. The short Au slugs served as catalyst and SiNW/Rs were grown by VLS LPCVD. After nanowire growth, the SiNW/Rs grown inside the nanochannel template with build-in contacts (Fig. 3-10c) were ready for IV testing.

Figure 3-10: Fabrication process and nanowire VLS growth in nanochannel template with build-in contacts. (a) Contact patterning. (b) Capping layer deposition and patterning. (c) Catalyst controlled etching and SiNW growth
Fig. 3-11 shows the current-voltage (I-V) characteristics of a single 200 nm wide, 20 nm high SiNR obtained using such built-in contacts with 20 µm (●) and 40 µm (▲) spacings. The build-in contacts were made from high work function metal Pt. These data, which are seen to scale with contact spacings, show the SiNR has a conductivity of $2 \times 10^{-4}$ S/cm and that contact resistance is not an issue. The SiNR conductivity value implies our grow-in-place approach is capable of achieving low Au doping. These same measurements were performed for 20 nm high nanowires with widths as narrow as 30 nm. We obtained linear I-V behavior in all these cases.

Figure 3-11: I-V characteristics of a single 200 nm wide, 20 nm high nanochannel without the SiNR (empty, 20 µm contact spacing) (■) and with a grown SiNR using contacts with 20 µm (●) and 40 µm (▲) spacings.

Also seen in Fig. 3-11, the I-V characteristics of an empty nanochannel (prior to growth) (■) in these measurements showed only noise of the measurement system and no I dependence on V. Therefore, the currents measured from our SiNWs/SiNRs are not
attributable to any leakage through the walls of our nanochannels or to noise, but they actually arise from the transport through the SiNW/Rs.

We also tried different contact materials, such as low work function metal Zr (4.05ev) as contacts and compared with those from high work function metal Pt (5.65ev) [8]. Fig. 3-12 shows the current-voltage (I-V) characteristics of a single 200 nm wide, 20 nm high SiNR obtained using such template with built-in contacts. As seen in Fig. 3-12, the I-V characteristics (black plot) of an empty nanochannel (prior to SiNW growth) (■) in these measurements showed only noise of the measurement system and no I dependence on V. The I-V diagram (green plot) for the Pt contact case (▲) shows linear behavior and electrically demonstrates the existence of SiNR inside the nanochannel. As discussed above, the SiNW has a conductivity of 2 × 10⁻⁴ S/cm and the SiNW conductivity value implies our grow-in-place process is capable of achieving low Au impurity levels. The scaling of current with contact spacings in Fig. 3-11 also indicated that contact resistance was not an issue for Pt case. The linear relation of I-V for high work function metal Pt indicates that the SiNW is p-type in background possibly due to the existence of Au in the SiNW [9]. The current in the I-V diagram (red plot) for the Zr contact case (●) is much smaller than that of Pt case and is closer to that of the empty nanochannel case. For the low work function Zr contact case, Zr contacts and SiNW formed Schottky-type contacts suppressing the current flow between the two Zr contacts due to the Schottky barrier. This provides the possibility of making Schottky field effect transistors by using low work function metals such as Zr.
3.5 Summary

Our research has demonstrated for the first time that it is possible to go directly from a silicon precursor gas (e.g., SiH₄) to self-assembled, self-positioned, and contacted crystalline SiNW/R devices without any intervening silicon material formation or collecting/positioning/assembling steps. Our approach offers good control on SiNW/Rs size, shape, number, position, orientation, and inter-spacings, without any post-growth fabrication difficulties.

The approach we have developed is also environmentally safe since the fabricated nanowires are always confined and only the exact number needed is fabricated. The growth nanochannels are horizontally arrayed and become a permanent part of the device.
structure. We show that the nanochannel templates can enable the VLS growth of nanowires and nanoribbons with predetermined locations and orientations and with desired sizes, shapes, number, and inter-spacings. In addition, contacts and interconnects, as well as device encapsulation/passivation, can be built into the templates. We believe this grow-in-place approach points the way to a manufacturable, high-throughput, and environmentally safe methodology for fabricating nanowire/ribbon devices which self-assemble and self-position into integrated circuits.

In the discussions above, the electron-beam lithography was used to define the nanochannels. Other methods, such as nano-imprinting, immersion lithography can also be used. Alternative catalysts, such as Ti can be used as the sacrificial layer and serve as the catalyst for silicon nanowire growth. In addition, SiNWs were grown by our grow-in-place approach and served as the demonstration. However, nanowires or nanotubes from other materials, such as Ge, ZnO$_2$, or Si/Ge junction structure, could also be controlled grown through this approach.

Device fabrication will be carried out from our grow-in-place approach. Transistor fabrication will be taken as an example to demonstrate our grow-in-place approach of device fabrication. In the next chapter, SiNW transistor structures, fabrication, and characterization will be introduced and discussed.
References


Chapter 4

SiNW transistors in encapsulated nanochannel templates

4.1 Introduction

With the scaling limit of conventional silicon devices in sight, there is rapidly growing interest in nanotube and nanowire devices with one-dimensional (1-D) channels [1][2]. Nanowire and nanotube devices have been intensely researched and high performance devices have been demonstrated [3][4][5][6]. Among possible nanowire and nanotube devices, SiNW devices are particularly promising due to the central role of silicon in semiconductor industry. The bulk properties of silicon have been well understood and the carrier type and concentration could be well controlled [7][8][9]. The SiNW device fabrication would allow the using of existing semiconductor technologies, equipments, and knowledge. Different transistor structures and fabrication have been developed for making nanowire transistors. In this chapter, nanowire and nanotube transistor structures will be introduced, followed by transistor fabrication from our grow-in-place SiNWs grown in our encapsulated/long nanochannel templates. These SiNW transistors will be characterized and discussed.
4.2 SiNW transistor structures

Nanowire and nanotube transistors have been intensely researched and difference transistor structures have been developed. These transistor structures include back-gate structure [3][10][11], top-gate structure[12][13][15], and top-back gate combination structure [14][16][17].

4.2.1 Back-gate transistor structure

Due to the extremely small size of nanowires and difficulties in gate alignments, most nanowire devices were made using back-gate geometry. Fig. 4-1 shows one example of these structures [3]. To make this structure, silicon wafer covered with insulation layer (e.g., thermally grown SiO2) could be used as the substrate. Silicon wafer serves as the back-gate electrode and the insulation layer serves as dielectric layer for transistors. High conductive silicon wafers are preferred for better performance. There are several ways of making devices from silicon nanowires. (1), nanowires are grown by VLS LPCVD and collected as nanowire powder or harvested into solution. The nanowires could be simply dropped (nanowire powder) or spun (nanowire solution) onto the substrate, followed by SEM searching, electron-beam lithography to define the source/drain contact regions, metal deposition and lift-off. (2), nanowires are first grown and then harvested into solution. The nanowires could be aligned to desired orientation by alignment methods introduced in chapter 2, such as solution manipulations. After the alignment, the source and drain contacts could be patterned by electron-beam lithography, metal deposition and lift-off.
The main advantage of this transistor structure is that it offers relatively easy transistor fabrication. There is no need of dielectric layer deposition or gate electrode alignments and patterning. The silicon substrate “global” back-gate also offers the ability to modify the Schottky barrier between contact electrodes and nanowires [11][18], so Schottky effect transistors could be fabricated from this structure. However, since the nanowires are only lying on the SiO$_2$ coated silicon substrate, the nanowire and dielectric layer interface quality is not high and this may strongly affect the device performance. The thick silicon substrate also offers low gate efficiency. In addition, the SEM searching and electron-beam lithography may damage the insulation/dielectric layer, bring leakage problems, and offer low throughput.
4.2.2 Top gate transistor structure

To solve the low interface quality problems and low gate efficiency in the back-gate structure devices, top-gate designs were introduced and researched [12][13][15]. In these approaches, nanowires are first grown by such as the typical VLS LPCVD nanowire growth. These nanowires are collected, positioned, and aligned. Source/drain electrodes are then defined by such as electron-beam lithography. These steps and the obtained structures are very similar with the back-gate structure, but the substrate is not serving as the gate electrode, so different substrates can be used, especially insulating substrates and flexible substrates, such as glasses or plastics. After these steps, dielectric layer is formed and the gate electrode is aligned and patterned, usually by electron-beam lithography. There are typical two ways of defining the dielectric layer and making top gate structure.

The first one [12][13][14] is through dielectric layer definition and deposition, followed by top gate electrode deposition as shown in Fig. 4-2. The dielectric layer is usually high k dielectric layer, such as zirconium oxide and hafnium oxide. The dielectric layers could be deposited by atomic layer deposition (ALD) and cover the nanowire between the source and drain electrodes. The gate electrode is then deposited on the dielectric layer.
The second one is the core-shell structure with nanowire as core and dielectric layer as shell [16][19][20], in which dielectric layer shell surrounds the nanowire. Fig. 4-3 shows a top-gate core-shell SiNW transistor structure [16]. To make this structure, the core nanowire is first synthesized by the standard VLS nanowire growth. Then the SiNW can be controlled thermally oxidized to form an oxide shell structure around the core nanowire. This method particularly works well for silicon nanowire, since the silicon oxide around the SiNW core through thermal oxidation offers high quality oxide and interface [21]. The oxidation also helps to passivate the SiNW surface and reduce the surface defects.

Figure 4-2: Top-gate SiNW transistor structure. (a) Schematic cross-section view. (b) SEM top view. [12]

(a) (b)

Figure 4-3: A top-gate core-shell SiNW transistor. (a) 3-D schematic representation, (b) FESEM top view of SiNW field effect transistor. [16]
To make devices from these core-shell nanowires, the core-shell nanowires are located or aligned on the substrate usually through SEM searching or electric field alignment. Gate electrodes are patterned usually by electron-beam lithography and metal depositions on the core-shell nanowire. Following the gate definition, the source and drain regions are opened and electrode metals are then deposited and life off. These source/drain electrodes are also usually defined by electron-beam lithography. This structure offers the advantage of using thermal oxide with high interface quality. However, the gate can only cover part of the nanowire between source and drain regions. The contact resistances and the SiNW slugs between the source/drain and gate electrodes which are in series with the channel region can affect transistor device performance. In addition, nanowire alignments and multiple e-beam alignments make this approach complicated and time consuming.

4.2.3 Top-gate and back-gate combination structure

The top-gate structure introduced above also offers the top-gate and back-gate combination ability. As shown in Fig. 4-3a, the top-gate nanowire transistor structure can be fabricated on a high conductive silicon substrate coated with thermal grown silicon oxide or LPCVD deposited silicon nitride [16]. The high conductive silicon substrate could be used as back-gate electrode and the silicon oxide or nitride could serve as the dielectric layer for the back-gate electrode. The global back-gate can help to enhance the device performance by electrostatics doping the regions between source/drain and gate electrodes or help to modulate the Schottky barriers between the source/drain electrodes
and nanowire. With the combination of the top gate and back gate, this structure offers the flexibility of researching the top-gate and back-gate effects.

Another structure of top/back-gate combination is top-gate transistor with the back-gate electrode buried underneath top-gate electrode as shown in Fig. 4-5. Comparing with structure introduced above, the top-gate electrode metal blocks the effect of the back-gate voltages on the transistor channel region. So the back-gate electrode does not affect the channel region. This structure was first introduced on CNT transistors [17]. Before this new transistor configuration was introduced, most conventional CNT field effect transistors took use of simple back-gate structure shown in the Fig. 4-4, which was very similar to the back-gate nanowire transistor structure. This simple back-gate transistor structure was realized by using back-gate, top contact geometry and remarkable progress has been made to improve the performance of CNT FETs [22][23]. However, those devices showed either contact interface effect or ambipolar behavior [24].

![Figure 4-4: Conventional back-gate carbon nanotube transistor structure](image)

To solve those problems, Dr. Phaedon Avouris group in IBM proposed a novel device concept and the structure is shown in Fig. 4-5. In this new structure, there is an additional Al gate electrode sandwiched between the nanotube and back-gate silicon oxide. To fabricate the structure, the Al electrode was first deposited on the silicon
substrate covered with 10nm SiO$_2$. The Al electrode was then oxidized in moisturized oxygen to form a thin Al$_2$O$_3$ as Al gate electrode dielectric layer. The Al gate electrode and the Al$_2$O$_3$ layer are denoted as B in Fig. 4-5. In this structure, the Al electrode serves as the primary gate which controls the electrostatics and switches the nanotube bulk channel in the region B; the silicon back-gate control the Schottky barriers at the nanotube/metal contacts.

This concept shown in Fig. 4-5 offers electrostatic and chemical doping profiles along the nanotube. Based on the novel device concept, they fabricated high performance carbon nanotube transistors exhibiting pure n- and p- type behaviors. By tuning the Si
back-gate and Al gate voltages, the combination of the electrostatic and chemical doping along the channel enables n/i/n or p/i/p doping profile and offers excellent off-state performance and the smallest inverse subthreshold slope. This novel structure offers (i) an n/i/n or p/i/p doping profile that only allows for either electron or hole transport, and (ii) a unique step-like band bending that suppresses the band-to-band tunneling in CNFETs.

4.3 Transistor fabrication in encapsulated/long nanochannel templates

As discussed in previous chapter, the encapsulated/long nanochannel template in our grow-in-place approach confines the nanowires during the nanowire VLS growth and gives control of nanowire size, shape, number, position, orientation, and inter-spacing. The electrode contacts can be built-into the capping layer of the nanochannel template. This capacity makes grown nanowires self-positioned, self-assembled, and self-contacted into the integrated circuit. Back-gate, top-gate, and their combination structures can be fabricated from these SiNWs grown inside our encapsulated/long nanochannel template.

The global back-gate transistor from our encapsulated/long nanochannel template is shown in Fig. 4-6. This structure and the corresponding fabrication are similar to the resistor structure and the fabrication discussed in last chapter shown in Fig. 3-10. The whole back-gate transistor structure can be pre-fabricated before SiNW growth. The built-in electrodes can serve as the source/drain electrodes and the silicon substrate can serve as the gate electrode for the back-gate transistor or the back/top-gate combination structures. The thermally grown silicon oxide or LPCVD coated silicon nitride on the
silicon substrate can serve as the dielectric layer for the back-gate transistor. Finally, SiNW growth can be carried out in this transistor template with VLS LPCVD growth. During the nanowire growth in the LPCVD system through VLS mechanism, the nanowire will grow inside the nanochannel with liquid tips or growing fronts. The liquid growth tips or fronts make the nanowire follow the nanochannel shape and accumulate the nanochannel. When the nanowire grows underneath the electrodes, the nanowire will form good contact with the electrodes. By controlling the growth time, nanowire will grow inside nanochannel and reach certain length. The grown SiNW will connect the electrodes. The nanochannel guides the nanowire growth and gives good control of nanowire size, shape, number, position and orientation. As a result, the SiNW shown in Fig. 4-6 is self-positioned, self-aligned, self-assembled, and self-contacted into the integrated circuit structure.

Figure 4-6: Schematic representation of a single SiNW inside nanochannel template with built-in contacts. The structure can serve as back-gate transistor by using silicon substrate as the global back-gate electrode.
The top-gate structure can also be fabricated from the encapsulated/long nanochannel templates. The top-gate electrodes can be implemented on the structure shown in Fig. 4-6 and can be fabricated through photolithography on the capping layer. The capping layer, such as silicon nitride, can serve as the dielectric layer for the top-gate electrodes. The top view of the finished top-gate transistors built from the encapsulated/long nanochannel template is shown in Fig. 4-7. As shown in this figure, the source/drain contacts are built-into and buried underneath the capping layer. The capping layer serves as the dielectric layer for the top-gate transistors. The top-gate electrodes can be fabricated before or after SiNW growth on the capping layer. The gate electrodes can be defined by photolithography, metal deposition, and lift-off. This same configuration also offers the back-gate and top-gate combination capacity. We can use the high conductive silicon wafer coated with silicon oxide or nitride as the substrate. The top gate structure shown in Fig. 4-7 can be built on this substrate and the silicon substrate can serve as the back-gate electrode. It allows us to apply the back-gate biases as well as the top-gate voltages.

Figure 4-7: Top view of top-gate transistor building from encapsulated/long nanochannel template.
As a summary for transistor fabrication, the encapsulated/long nanochannel template offers good SiNW growth control, fixes, and confines the SiNWs. The built-in electrodes provide source and drain electrode contacts. The gate electrode can simply be the silicon substrate without any alignment for the back-gate transistor configuration; the gate electrodes can also be patterned by photolithography on the capping layer with the capping layer as the dielectric layer. Our transistor fabrication from this template offers the ability of SiNW transistor fabrication directly from silicon precursor gas by one single step of LPCVD nanowire growth. There are no post-growth fabrication steps for transistor fabrication, which remove the SiNW device fabrication difficulties for most current methods, such as nanowire collecting, picking, positioning, aligning, assembling, and contacting. We have successfully made back-gate, top-gate and combination SiNW transistors by both electron-beam direct writing and laser direct writing. Electrical measurements were carried out on these transistors and compared.

4.4 Characterizations and challenges

As discussed above, our “grow-in-place” approach through encapsulated/long nanochannel template offers good SiNW growth control and easy device fabrication. We have successfully made back-gate and top-gate SiNW transistors. However, these both back-gate and top-gate SiNW transistors made from electron-beam lithography did not give good transistor performance. There were current leakages through dielectric layers of either the silicon oxide or silicon nitride.
Fig. 4-8 shows output characteristics for a back-gate transistor with the structure as shown in Fig. 4-6, made from the encapsulated/long nanochannel template. From the results, the leakage currents through gate electrode $I_G$ are almost equal to the drain currents $I_D$, indicating that there were strong leakage currents through the drain electrode and the back-gate electrode of silicon substrate. So there was few or no control of the gate voltages over the transistor channel.

Figure 4-8: Output characteristics for an example back-gate transistor made from encapsulated/long nanochannel template with $V_G = 3\text{v}$. These plots show leakage through drain and back-gate electrode of silicon substrate.

These leakages may be caused by the high energy electron beam damages of the electron-beam lithography during the nanochannel template fabrication. For the nanochannel template fabrication, the electron-beam lithography was used to define the nanochannel trenches. The high energy electrons (50KeV or 100KeV) in the electron-beam direct writing might damage the regions of dielectric layer under the nanochannels.
The damage sites in the dielectric layer may also enhance the diffusion of Au during the 500 °C SiNW growth. In addition to the damages, the rough inner-surface of the nanochannel, Au residuals, and lack of surface passivation also depress the device performance.

To confirm the electron-beam damages and the corresponding effects on transistor performance, control experiment was carried out. The control experiment and the corresponding nanochannel fabrication were carried out by replacing the electron-beam direct writing and removing the corresponding damages to the dielectric layer by laser direct writing, while kept all other fabrication steps the same. The laser direct writing used 442nm HeCd laser to define the nanochannels without any damage to the dielectric layer of SiO₂ or Si₃N₄ on the silicon substrate. During the channel template fabrication, the laser direct writing system of Heidelberg DWL66 laser system was used to define the nanochannels. The 442nm HeCd laser source in the laser system offers 500nm to 600nm resolution depending on the resists, exposure, and developing parameters. The laser direct writing resolution is much lower than electron-beam writing, but it at least gives some comparisons and tells if the electron-beam damages were a big problem for nanowire FETs made by electron-beam direct writing.

The laser direct writing was used to make nanochannel template with 550nm wide and 45nm high. Same with the previous device fabrication, electrode contacts were built in and LPCVD SiNW growth was carried out to grow SiNWs inside the nanochannels. This nanochannel template results SiNRs of about 550nm wide and 45nm high. With the built-in contacts serving as the source/drain electrodes and the substrate serving as the gate electrode, the fabrication results in single-SiNR transistor. The structure of this
transistor is exactly the same with the structure shown in Fig. 4-6, but it was made from the laser direct writing and lithography, instead of electron-beam writing. The SiNR is larger but there were no damages on the silicon oxide dielectric layer comparing with the electron-beam direct writing. This transistor is a good reference to research the high energy electron damages during electron-beam lithography.

The transistor characterizations for this transistor made from laser direct writing were carried out by using the Agilent 4156 Precision Semiconductor Parameter Analyzer. Fig. 4-9a shows the drain current (I_D) versus drain–source bias voltage (V_DS) (output characteristics) for our nominally undoped back-gate SiNR transistor at different values of the gate voltages (V_G). The family of the I_D-V_DS plots shows that the I_D negatively increases with the negative increase of V_G from 40v to -60v (from top to down in -5v step). These indicate that the SiNR transistor is p-channel field effect transistor. Fig. 4-9b shows a plot of I_D versus V_G (transfer characteristic) with V_D fixed at -20V. In this figure, the black curve is the linear plot of I_D Versus V_G (the scale is the left I_D axis) and the red curve is the corresponding semi-Log scale plot of the I_D versus V_G (the scale is the right I_D axis). From the log scale (red) plot, the device only offers the on/off ratio of 10^2.

From these characterizations, this SiNR transistor shows some degree of transistor performance, but the performance is not good. This poor performance may come from Au residues, rough surface, thick dielectric layer, or lack of surface passivation. More work is needed to optimize device fabrication and enhance device performance. However, this is not the concern in this stage, but to research the leakage.
The gate leakage currents $I_G$ were measured at the same time during the transistor characterizations. The plots of gate leakage currents $I_G$ versus $V_{DS}$ for different $V_G$ are shown in the figure. The leakage currents decrease as $V_G$ increases.

Figure 4-9: Laser SiNR back-gate transistor characterization. (a) Output characteristics, $I_D$ versus $V_{DS}$ diagrams with $V_G$ from 40v to -60v in -5v steps from top to bottom. (b) Transfer characteristics, $I_D$ versus $V_G$ diagrams with $V_D$ fixed on -20V. Pt serves as the source/drain electrodes. The silicon substrate serves as the back-gate electrode and the 200nm silicon oxide serves as the dielectric layer.

The gate leakage currents $I_G$ were measured at the same time during the transistor characterizations. The plots of gate leakage currents $I_G$ versus $V_{DS}$ for different $V_G$ are
shown in Fig. 4-10. Comparing with those plots in Fig. 4-9, the leakage currents $I_G$ are at least 100 times smaller than the corresponding $I_{DS}$ in Fig. 4-9. The leakage currents are in $10^{-10}$ A range with gate voltages up to -60V. From these results and comparisons, the leakage through dielectric layer is not a problem for the back-gate transistor made by laser direct writing from our encapsulated/long nanochannel template.

![Figure 4-10: Leakage current $I_G$ versus $V_{DS}$ with different gate voltages $V_G$ for back-gate transistor made by laser direct writing.](image)

From these results, discussions, and comparisons above between transistors made by electron-beam and laser direct writings, we can confirm that the electron-beam direct wiring for the encapsulated/long nanochannel template fabrication did damage the dielectric layer for the back-gate transistor.

For the top-gate structure shown in Fig. 4-7, there were also gate leakages through dielectric layer of the capping layer. The capping layer for the encapsulated/long nanochannel template was silicon nitride deposited from ECR PECVD. The capping
layer quality may be not very high. In addition, the SiNW growth at 500°C may also enhance the diffusion of Au catalyst into the capping layer.

As a summary for current back-gate and top-gate transistor fabrication from our encapsulated/long nanochannel templates, the major problem that hinders the device performance is the gate leakage. Other possible factors, such as surface roughness and passivation, Au residues, and contacting quality, may also influence device performance. Improvements are needed to enhance the device performance.

4.5 Solution and improvement

As we discussed above, there are several factors that hinder the device performance. The major one is the gate leakage, caused by the electron-beam damages for the back-gate structure and the low quality capping layer for the top-gate structure. There are also other improvements, such as Au removing, surface passivation, and doping.

The first solution is the improvement of our current encapsulated/long nanochannel templates without changing the structure design. The electron-beam lithography could be replaced by other non-damage techniques, such as nano-imprinting or immersion lithography. These techniques may remove the damages to the dielectric layer for back-gate transistors. For top-gate transistors, high quality dielectric layers, such as high k ZrO_2 or HfO_2 deposited by atomic layer deposition, could be used as the capping layer. These high quality dielectric layers may remove the leakage problem through the capping layer for the top-gate SiNW transistors. The combination of non-
damage back-gate definition and high quality capping layer also offers the ability of fabricating high quality top/back-gate combination transistors. In addition, the capping layer could be partially removed to expose the SiNWs. Then improvements, such as Au residue removing and surface passivation could be carried out before device fabrication.

The second approach is nanochannel structure modification. A new extruded/short nanochannel-guided “grow-in-place” approach will be introduced in details in the next chapter. This approach is a modification to our approach of transistor fabrication from encapsulated/long nanochannel templates discussed in this chapter. In the new approach, we shorten the length of our nanochannels. So the extruded/short nanochannels only nurse the initial SiNW growth inside the channels and guide the SiNW growth extruded outside the nanochannels. The grown SiNWs are confined and fixed by the extruded/short nanochannels. SiNW transistors can be fabricated in the SiNWs outside the nanochannels without processing difficulties. Since the SiNW parts for device fabrication are outside the nanochannels, we can do Au etching, cleaning, and surface passivation. We can controlled oxidize the SiNW to form high quality SiO₂ shell around the SiNW core to serve as the dielectric layer. In addition, it allows us to pattern fresh electrodes to the SiNWs. This new nanochannel structure keeps the advantages of our “grow-in-place” approach, while avoids the problems and enhances transistor performance. This new approach, device fabrication, and characterizations will be presented in the next chapter.
References


Chapter 5

SiNW transistors in extruded nanochannel templates

5.1 Introduction

In last chapters, SiNWs were controlled grown in our encapsulated/long nanochannel templates. The SiNWs were totally confined and encapsulated by the long nanochannels. The contacts were built-in to the nanochannel templates and SiNWs were self-contacted after growth. The advantages of these encapsulated/long nanochannels were that they offered full and precise controls on nanowire size, number, shape, orientation, position, and inter-spacing. There were no post-growth processes, which removed the problems and difficulties in nanowire positioning, aligning, contacting, and assembling. Transistors with back-gate and top-gate geometries have been fabricated in our encapsulated/long nanochannel templates with built-in contact electrodes. The back-gate transistors took use of the silicon substrate as the gate electrode and the oxide or nitride coated on the substrate as the dielectric layer. The top-gate transistors took use of the capping layer as the dielectric layer and the metal electrodes on the capping layer as the gate electrodes. However, there were several drawbacks in the encapsulated/long nanochannel grow-in-place approach for transistor fabrication. As discussed in the last chapter, first, there were damages to the nanochannel floors from the electron-beam writing. Second, the quality of capping layer from the deposited oxide or nitride was relative low for being dielectric layer after SiNW LPCVD growth at 500°C. Third, the
nanochannels were not perfectly smooth and there were gold residues inside the nanochannels. So the SiNW surface quality might be not high. The lack of surface passivation depressed the device performance. To take the advantages of our “grow-in-place” approach while avoid these problems and enhance the transistor performance, in this chapter, we introduce a novel extruded/short nanochannel template guided “grow-in-place” approach.

As comparing with our encapsulated/long nanochannel template, this extruded/short nanochannel template takes use of the nanochannels with shorter length. The extruded/short nanochannels only “nurse” the initial growth of the SiNWs and guide the SiNWs growth extruded out of the nanochannels. The extruded/short nanochannels give control on SiNW size, number, position and orientation. The nanochannels fix the SiNWs offering easy device fabrication. Transistors have been fabricated in the extruded part of SiNWs outside the nanochannels. The advantages of this extruded/short nanochannel template approach are that, the electron-beam direct writing is only carried out and restricted in the much shorter nanochannel regions. There are no damages to the regions where the devices are making. Second, the extruded SiNWs can be controlled oxidized, which offers the advantage of using the high quality silicon oxide shell as the dielectric layer for transistor fabrication. Third, Au removing, standard cleaning, and surface passivation can be carried out for the SiNWs outside the nanochannels. The SiNW surfaces of the extruded parts are much smoother and cleaner. This extruded/short nanochannel guided approach offers these advantages and solves the problems in the encapsulated/long nanochannel templates, while keeps our grow-in-place advantages.
The nanowire transistors can be easily made from these well-controlled “grow-in-place” nanowires grown in our extruded/short nanochannel templates, without any “pick-and-place” or printing difficulties; i.e., there are no nanowire or even finished transistor collecting, picking, handling, assembling and integrating steps in fabricating the resulting transistors. In addition, our nanowire transistor fabrication approach is mass-manufacturable and environmentally benign since only the exact number of nanowires needed is fabricated and the fabricated nanowires are always fixed by the guiding nanochannels. In this chapter, we will make top-gate core-shell transistors by combing our extruded/short nanochannel guided grow-in-place approach and top-gate core-shell FET structure geometry. Transistor characteristics and device model will be presented. Initial research on ion-implantation will also be introduced.

5.2 Extruded/short nanochannel template fabrication

Fig. 5-1 schematically shows our extruded/short nanochannel template fabrication and the guided nanowire growth process. Comparing with our encapsulated/long nanochannel template, the major change is the shrinking of capping layer length. In the encapsulated/long capping layer case, the device parts of the nanowires were totally confined inside the capping layer which was 100µm long, however, for this extruded/short capping layer case, the capping layer is shrunk to only 3µm.

To guide SiNW growth in our extruded/short nanochannel “grow-in-place” approach, the nursing/guiding extruded/short nanochannel template was first fabricated as shown in Fig. 5-1a-d. Similar to our encapsulated/long nanochannel template fabrication,
our nursing/guiding extruded/short nanochannel template can be made from different techniques, such as electron-beam lithography or nano-imprinting. Here we used electron-beam lithography for our template fabrication to be consistent with our previous template fabrication. The making processes were similar with our previous reported structures [1][2] and those in chapter 2, the integrated nanochannel templates basic to the grow-in-place approach were fabricated by electron-beam lithography and a controllable sacrificial metal line etching technique in this demonstration. The use of electron-beam lithography allows nanoscale control of the nanochannel dimension, number, orientation, and inter-channel separation [3], which eventually transform into precise control of nanowire dimensions, orientation, position, and inter-spacing [1]. The sacrificial metal, in this demonstration, was gold for catalyzing SiNW growth. It functioned as both the sacrificial material defining the enclosed nanochannels and as the catalyst for VLS silicon nanowire growth.

The overall process flow for our extruded/short nanochannel guiding nanochannel template is shown in Fig. 5-1. First, open trenches (one is shown) of desired size, number, inter-spacing, orientation, and position were patterned by electron-beam direct writing on a resist film (e.g., PMMA) on a substrate (glass or silicon substrate coated with oxide). Alignment markers were also defined at the same time for following capping layer and electrode contact photolithographic definitions. Second, titanium (1.5 nm) was e-gun evaporated as an adhesion layer and then gold was thermally evaporated to a desired nanometer thickness thereby defining the height of the nanochannel (Fig. 5-1a). Subsequently, the resist film was lifted off to reveal the gold line positioned and spaced, as desired, on the substrate (Fig. 5-1b). The electron-beam writing and Au deposition
defined the Au line dimension. Third, a capping layer (e.g., silicon oxide) with the designed width (e.g., 3 µm) was patterned by photolithography, SiO₂ deposition and lift-off (Fig. 5-1c). Finally, the gold line, including the region buried under capping layer, was controllably removed by wet etching to form the nanochannel devoid of Au except for a short slug of Au for catalyzing the VLS SiNW growth process, as depicted in Fig 5-1d. For this gold removal process, a diluted Au etchant (type TFA from Transene Company, Inc.) was employed at room temperature and the etching was stopped by

Figure 5-1: Schematic showing the process flow for fabricating extruded/short nanochannel template and growing SiNW in our “grow-in-place” approach. (a) Sacrificial/catalyst metal definition and deposition. (b) Sacrificial/catalyst line after lift-off. (c) Capping layer formation by lithographic patterning, deposition, and lift-off. (d) Partial etching of the sacrificial metal to form the nanochannels with catalyst in the middle. (e) LPCVD SiNW growth and extrusion out of nanochannel by the VLS mechanism. (f) SiNW ready for device fabrication.
immersion in DI water. The small slug of Au (e.g., sub 1 µm) retained for its catalyst role was located in the middle of the otherwise empty nanochannel to serve as the VLS catalyst for the SiNW growth (Fig. 5-1d).

5.3 SiNW growth in extruded/short nanochannel template

In our extruded/short nanochannel approach, we combined our “grow-in-place” nanowire growth \[1][2] and top-gate FET geometry to make a single-SiNW FET. The nanochannel template was modified and the nanochannel length was reduced to 3µm. VLS growth resulting in unintentionally-doped SiNWs was then carried out in a LPCVD reactor at 500 °C and 13 Torr, using a 5% SiH\(_4\) diluted in H\(_2\) with a total flow rate of 100 sccm \[1][4]. The nanochannel template shown in Fig. 5-1d nursed and guided the nanowire growth. By controlling the growth time, the SiNW grew out of (extruded) the nursing nanochannel (Fig. 5-1e) at growth rate of about 1 µm/min and reached certain length (e.g., 15 µm) to permit easy four contact, or gate and source/drain contact photolithographic definition, depending on whether four probe structures for resistivity-contact resistance studies or transistors were being fabricated.

During SiNW growth, the extruded/short nanochannel basically served as the nursing and guiding nanochannels for the nanowire growth. The extruded/short nanochannel nursed and confined the nanowire in the early stage of the nanowire growth through VLS growth mechanism. The initial nanowire growth inside the extruded/short nanochannel defined the nanowire size, number, position, and growth orientation and gave good growth controls. By controlling the LPCVD growth time, the nanowire would
grow and extrude out of the extruded/short nanochannel. Same with our SiNW growth in the encapsulated/long nanochannels, our extruded/short nanochannel “grow-in-place” approach also offers the ability of synthesizing SiNWs by using a silicon precursor gas (e.g., SiH₄) to directly synthesize self-positioned/self-assembled crystalline SiNW without any intervening silicon material formation, collection, positioning and assembling steps. The grown SiNWs were fixed by the nanochannel and our nanowire transistors could be easily made from these well-controlled “grow-in-place” SiNWs, without any “pick-and-place” or printing difficulties; i.e., there are no nanowire or even finished transistor collecting, picking, handling, assembling and integrating steps in fabricating the resulting transistors. In addition, our nanowire transistors fabrication approach is mass-manufacturable and environmentally benign [5] since the fabricated nanowires are always fixed by the nursing/guiding nanochannels and only the exact number of nanowires needed is fabricated. As our first demonstration, we used unintentionally doped SiNWs to demonstrate our approach for transistor fabrication. In the future, nanowire device performance may be further optimized by proper intentional doping, and structure design. In addition, our nanowire devices can be made on different substrates, such as silicon substrate and glass. As a tougher demonstration, nanowire transistors would be made on glass substrates. Making such transistor structures on other substrates, such as silicon substrate, will be the similar, or easier.

After the nanowire growth, the residual gold catalyst was completely removed by rinsing the whole sample into gold etchant following by DI water cleaning. The SiNWs were then subjected to a modified standard cleaning. After these processes, the nanowire as shown in Fig. 5-1f was ready for device fabrication in its position. Four point probe
contact structure and top gate FET structure have been fabricated on these SiNWs to research on the nanowire resistivity ($\rho_s$), contact resistance ($R_c$), and transistor performance.

Fig. 5-2 shows filed emission scanning electron microscope (FESEM) images of SiNWs grown from different cross-sectional sized nanochannels in this extruded/short nanochannel “grow-in-place” approach on both glass substrate and silicon substrate. Fig. 5-2a shows SiNW of 150nm in diameter and Fig. 5-2b shows SiNW of 80nm in diameter, both on glass substrate. Fig. 5-2c shows SiNW of 80nm in diameter on silicon substrate coated with thermal grown silicon oxide. The FESEM images clearly show that SiNWs grew and extruded from the extruded/short nanochannels. The pre-fabricated nanochannels defined the SiNW size, number, position, and growth orientation.

Figure 5-2: FESEM images of SiNWs produced by the “grow-in-place” approach. Extrusion out of “nursing” nanochannel is evident. (a) 150nm width SiNW on glass substrate, (b) 80nm width SiNW on glass substrate, and (c) 80nm width SiNW on Si substrate.
By using alignment markers and with the grown SiNW fixed by the nanochannel, a four-point probe structure or transistor can be easily fabricated from these well controlled, self-positioned/self-assembled “grow-in-place” nanowires by standard photolithography.

5.4 Four point probe structure fabrication and measurements

To measure SiNW conductivity and contact resistance between SiNW and contact electrodes, four point probe measurement structure was used and fabricated. To make the four point probe measurement structure, the four contact probes 1-4 were defined with electrode contacts width of 1.5 µm and spacing of 1.5µm as shown in Fig. 5-3.

Figure 5-3: Four point probe measurement structure. (a) 3-D Schematic of the four point probe measurement structure. (b) top-view FESEM picture of the structure. The SiNW diameter is 80nm. The structure was defined by photolithography, with probe electrode width 1.5µm and spacing of 1.5µm. The electrode metal was Ti. The scale bar is 1 µm.
The four probe contact structure (Fig. 5-3a) was made by a simple photolithography. To do that, our grow-in-place SiNW was first Au-removed and cleaned. Photoresists LOR5A/SPR1805 were then spun on, exposed, and developed. After native oxide removal, Ti (300nm)/Au(40nm) were deposited by e-gun depositions and lift-off. The testing structure top view is shown in the FESEM image in Fig. 5-3b and SiNW diameter is 80 nm (r_s = 40nm).

The four point probe measurement was carried out on this testing structure and Fig. 5-4 shows the diagrams of the measurements. The linear and symmetric diagrams indicate that Ti probe electrodes form good ohmic contact with the SiNW [6], by forming a stable conducting silicide with low Schottky barrier height [7][8] on our SiNW. The red line is the V2-3-I diagram between Probe 2 and Probe 3 (see Fig. 5-3b). The slope gives the SiNW resistance R_s2-3 between Probe 2 and Probe 3, R_s2-3 = 4.26 × 10^7 Ohm. From this resistance, the SiNW resistivity \( \rho_s = 14.3 \text{ ohm-com} \) and conductivity \( c_s = 0.07 \text{ S/cm} \) can be obtained by equation \( R_{s2-3} = \frac{\rho_s L_{2-3}}{\pi r_s^2} \), where \( L_{2-3} = 1.5 \mu\text{m} \) is the spacing between Probe 2 and Probe 3. The black line is corresponding to the V1-4-I between Probe 1 and Probe 4. The slope gives the total resistance of \( R_t = 2.39 \times 10^8 \text{ ohm} \) between Probe 1 and Probe 4, which includes SiNW resistance between Probe 1 and Probe 4 and contact resistances \( R_c \). If we assume that the SiNW resistance between Probe 1 and Probe 4 as \( R_{s1-4} = \frac{\rho_s L_{1-4}}{\pi r_s^2} \) where \( L_{1-4} = 7.5 \mu\text{m} \) is the SiNW length between Probe 1 and Probe 4, the contact resistance \( R_c \) can be obtained from the total resistance equation \( R_t = 2R_c + R_{s1-4} \). From the calculation, the contact resistance is \( R_c = 1.3 \times 10^7 \text{ Ohm} \). However, this value \( R_c \) is an approximate value and can only used as reference for discussion. There are errors in the assumption of \( R_{s1-4} \), because nanowire resistance is large and a significant
portion of the current may be transported through the middle contacts (current shunting), Probe 2 and Probe 3, rather than the SiNW underneath them [9]. If current shuntings through probe 2 and probe 3 were counted into the calculation, the contact resistance is $3.02 \times 10^7$ Ohm, which is in the same order with the last value. Thermal annealing may help to reduce the contact resistance [8] and improve the contact quality.

![Graph](image)

Figure 5-4: Four point probe measurement diagram. The current $I_{14}$ was forced between Probe 1 and Probe 4 while the voltage drops $V_{14}$ and $V_{23}$ were measured.

## 5.5 Core-shell top-gate SiNW FET fabrication

The top-gate SiNW transistor fabrication combines the core-shell top-gate transistor structure geometry and our extruded/short nanochannel grow-in-place approach. Core-shell top-gate SiNW FETs are schematically shown in Fig. 5-5a and this figure also indicates possible mass-manufacturability. The top-view FESEM image of one final single-SiNW FET structure is shown in Fig. 5-5b.
To make the top-gate core-shell SiNW transistor structure, the dielectric layer of SiO$_2$ was first obtained through controlled SiNW dry thermal oxidation \cite{10,11}. The fabrication started from the sample with our grow-in-place SiNW shown in Fig. 5-6a. Au etching and modified standard cleaning were first carried out before oxidation to remove the Au residues and to clean the SiNW. Then the sample was put into furnace for controlled oxidation at 700 °C for 4 hour \cite{10,12} with O$_2$ flow at 3 L/min. The oxidation resulted a Si/SiO$_2$ core-shell structure \cite{12,13,14,15} with about 10 nm thermal silicon oxide shell around SiNW core. The thermal oxide is shown as the red shell around the green SiNW core in the Fig. 5-6b. The thermal oxidation also helped to passivate the SiNW surface and reduce surface state density of the SiNWs. After oxidation,
source/drain and gate contacts were patterned by simple photolithography. The gate contacts were patterned by photolithographic patterning, Ti (400nm)/Au (50nm) deposition, and lift-off as shown in Fig. 5-6b. The thermal oxide around the SiNW under the gate region would serve as dielectric layer for the SiNW FET transistors.

To define the source and drain contacts, photo resists (LOR5A/SPR3012) were first spun on and the source and drain regions were opened by photolithography. These photoresists served both as silicon oxide etching resists and source/drain contact defining resists. After silicon oxide around the silicon nanowire in the source/drain regions was etched as shown in Fig. 5-6c, the contact metals (400nm Ti/50nm Au) for source/drain
electrodes were deposited and lift off. Fig. 5-6d shows the final schematic diagram of FET transistor structure.

Fig. 5-7a shows a FESEM image of our grow-in-place SiNW before transistor fabrication and Fig. 5-7b shows the corresponding finished transistor testing structure. These images confirmed that top-gate core-shell transistor structure was successfully fabricated from our well controlled grow-in-place SiNW in extruded/short nanochannel template. From our FESEM testing, the diameter of the testing SiNW with oxide around it is 80nm. So our SiNW diameter is around 60nm with 10nm oxide shell around it. We did not do the transmission electron microscopy (TEM) characterization due to the very limit number of SiNWs and the difficulty of making TEM sample from them. However, TEM pictures on SiNW oxidation can be referenced on other groups and showed very good interface quality [10].

Figure 5-7: SiNW transistor (a) grow-in-place SiNW before transistor fabrication. (b) the corresponding SiNW transistor after gate and source/drain patterning.
The transistor performance characterizations were carried out on the testing structure shown in Fig. 5-8a by using the Agilent 4156 Precision Semiconductor Parameter Analyzer. The testing top-gate core-shell SiNW transistor structure consisted of one single SiNW with source/drain electrodes and top gate electrode. The gate width was 2µm and the spacings between gate and source/drain electrodes were 2µm. Fig. 5-8b shows the current ($I_D$) versus drain-source bias voltage ($V_{DS}$) (output characteristics) for our nominally undoped SiNW FET at different values of the gate voltages ($V_G$). $I_D$–$V_{DS}$ curves show that the drain current $I_D$ first negatively increases then saturates with increasing negative drain voltage ($V_D$). The family of the $I_D$–$V_{DS}$ shows that the $I_D$ negatively increases with the negative increase of $V_G$ from 0.5v to -1.5v (from top to down in -0.25v step). These indicate that the SiNW transistor is a typical p-channel FET.

Figure 5-8: SiNW transistor and the output characteristics. (a) The testing structure and (b) the corresponding output characteristics, $I_{DS}$ versus $V_{DS}$ diagrams with $V_G$ from -1.5v to +0.5v in 0.25v steps from top to bottom.
The linear relationship of $I_D$ and $V_{DS}$ at low bias indicates good ohmic contacts to the nanowire, which is consistent with the 4-point probe measurement.

A plot of $I_D$ versus $V_G$ (transfer characteristic) with $V_D$ fixed at -0.1 V is shown in Fig. 5-9. In this figure, the black curve is the linear plot of $I_D$ Versus $V_G$ (the scale is the left $I_D$ axis) and the red curve is the corresponding Log scale plot of the $I_D$ versus $V_G$ (the scale is the right $I_D$ axis).

From the log scale (red) plot, the device offers the on/off ratio of $10^6$ and subthreshold slope ($S$) of 130 mV/Dec. Although this value is approximately double the best value in single crystal silicon devices (70mV per decade) [6], this subthreshold slope is lower than typical reported values (typically >300 mV/Dec, with the minimum reported value to be the 140 mv/Dec) obtained for single silicon nanowire devices with back gate and top gate geometry [8][16][17][18]. This $S$ value is also comparable with the lowest reported value of 120 mV/Dec for vertical silicon nanowire array devices [17].
In addition, this value is lower than the best values in poly-Si TFTs (200mV per decade) [19].

The threshold voltage of the SiNW FET is -0.6v. The threshold voltage of -0.6v indicates that the transistor channel was in OFF state with 0 V gate voltage and required a negative $V_G$ to turn on. We believe that the low work function metal, Ti as top gate contact, induced a depletion or electron rich region underneath the gate region, which made the channel in OFF state at 0V gate voltage and required a negative $V_G$ to turn on the device. So the SiNW FET is an enhancement mode p-channel FET [6]. The transconductance is obtained from the slope of the linear region in the $I_{DS}$ versus $V_G$ plot at $V_{DS} = -0.1$ V (black curve in Fig. 5-9). The transconductance ($g_m$) for this nominally undoped SiNW is $10^{-3}$ µS.

In addition, during the transistor fabrication, the electron-beam direct writing was only carried out in the extruded/short nanochannel region, so there were no electron-beam damages to the SiO$_2$ regions outside the nanochannel, where our transistors were fabricated. This offers the ability of using the un-damaged SiO$_2$ as the dielectric layer and silicon substrate underneath the SiO$_2$ as the back-gate electrode, combining the top-gate research. Initial researches on the top-gate and back-gate combination were also carried out by applying back-gate voltages $V_B$ to the silicon substrate. Our initial results indicate that there was no leakage through the back-gate electrode and the properly applied back-gate voltages $V_B$ enhanced the device performance. More researches and optimizations are needed to further enhance their effects.
5.6 Mobility analysis

SiNW Transistors shown in Fig. 5-5, Fig. 5-7, and Fig. 5-8a have been successfully fabricated through our extruded/short nanochannel “grow-in-place” approach and characterized. In our top gate core-shell SiNW transistors, as-grown uniformly unintentionally doped SiNWs were used in these SiNW transistor fabrications. Fig. 5-10 shows the schematic cross-section view of our typical top-gate SiNW transistor. From our transistor fabrication in Fig. 5-6, the device is fabricated only on a uniformly unintentionally doped SiNW (slightly p-type). It has no heavily doped n$^+$ or p$^+$ regions and the source and drain contacts to the material are ohmic. In Fig. 5-10, the SiNW regions I, II, and III are same slightly p-type according to our as-grown unintentionally doped SiNW. Each of the regions has the same length $L_G$ ($L_G = 2 \mu m$ for transistor in Fig. 5-8a) and, further for simplicity, the work functions of the gate electrode and semiconductor are taken as the same.

![Figure 5-10: Schematic cross-section image of our transistor.](image)

In the literatures, there are also SiNW transistors with similar structures made from uniform single doping-type (e.g., boron doped) or unintentionally doped SiNWs. Most of these reported transistors were explained as conventional MOSFETs and their mobilities were extracted from the conventional MOSFET model. “Conventional”
MOSFET utilizes heavily doped source and drain regions to form “ohmic contacts” to a gate induced inversion layer. In the on-state, transport in this inversion layer controls the source-drain current $I_D$. The inverted channel is not shunted due to the presence of a reversed-biased n/p or p/n junction at the drain. In the off-state there is no inversion layer and the current $I_D$ is blocked by the reverse biased n/p or p/n junction at the drain. The thin film transistor is a variant of this in which the on-state channel is also not shunted but, in this case, due to a reversed bias i/n or i/p junction at the drain which is in series with the additional impediment of the thin, resistive i-layer under the gate. This body of literature models the drain current $I_D$ of these devices in the linear range of on-state operation using Eq. 5-1, where $C_I$ is the gate capacitance per area, $\mu$ is the channel hole mobility, $V_G$ is the gate-source voltage, $V_{th}$ is the threshold voltage, $V_{DS}$ is the drain-source voltage and $L_G$ is the channel length.

$$I_D = C_I \mu (V_G - V_{th}) V_{DS} / L_G^2$$

(Equation 5-1)

The effective hole mobility for most transistors in the literature were calculated from this transconductance $g_m$ through Eq. 5-2. The gate capacitance $C_I$ can be obtained from the equation $C_I = 2\pi \varepsilon_o \varepsilon L_G / \ln[(r_s + d)/r_s]$ by using cylinder model, where $\varepsilon_o$ is the vacuum permittivity, $\varepsilon$ is the dielectric constant of the gate dielectric SiO$_2$, $r_s$ is the radius of SiNW and $d$ is the thickness of the gate dielectric layer.

$$\mu = g_m L_G^2 / C_I V_{DS}$$

(Equation 5-2)

If we calculate the mobility for our transistor this way, the hole mobility for our nominally undoped SiNW transistor is only 0.25 cm$^2$V$^{-1}$s$^{-1}$, which is very low. However, this value is much higher than the reported mobility value of the nominally undoped
SiNW device [20]. In the literature, many p-channel SiNW devices were made from uniformly single doped p-type SiNWs, for example, boron doped SiNWs. It is worth to note that the reported hole mobilities (20-325 cm²V⁻¹s⁻¹) [8][15][21][22] of their p-type SiNWs in literature are much higher than our value and other reported value of unintentional doped SiNWs [20]. This fact actually conflicts with the expectation of mobility decreasing with increasing doping concentration. However, we have reason to believe that our calculation of 0.25 cm²V⁻¹s⁻¹ and the mobility calculations of their p-type SiNWs devices in the literature were based on the improper model. Their p-type SiNW FETs in the literature were depletion mode p-channel FETs, whose p-channels was introduced by doping, instead of field effect whose p-channel was totally induced by the field effect. The corresponding on-current was controlled on the material doping and not on the gate capacitance C₁, So their using of MOSFET equations, such as Eq. 5-2, for calculating the hole mobilities of their depletion mode p-channel FETs was improper. Their calculated mobilities were not the real hole mobilities and we believed that their real mobility should be much lower than their reported calculated values if using the proper model and equations. To properly address the mobility issue, we introduced an accumulation type MOSFET model in the next section.

5.7 Accumulation type transistor model

In this part, we propose and demonstrate a MOSFET transistor which operates quite differently from that described above. We term this device an accumulation type MOSFET (AMOSFET) because it relies on the formation of an accumulation layer under
the gate for its on-state. This AMOSFET device has an on-state that arises from the presence of an accumulation layer under the gate and an off-state that arises from fully depleting this region of the SiNW under the gate. The on-current is not controlled by the gate capacitance, and the on-current is controlled by the semiconductor doping concentration. The operation of such an AMOSFET is outlined in Fig. 5-11.

Figure 5-11: Structure and operation of the AMOSFET. Part (a) Off-state with the following features: (1) Channel of electrons can not form due to the adjacent p-region. If it were to form, current would be blocked by reverse biased channel/region III. (2) All of region II is depleted of holes. Part (b) On-state with the following feature: (3) Channel of holes provided by source.

Fig. 5-11a shows the AMOSFET off-state. A sufficiently positive bias applied to the gate completely depletes region II. The semiconductor can not invert easily in region II due to the adjacent p-type I and III regions. Even if it were to invert, transport in the inversion layer would be limited by the reverse bias p-region contacting this inversion
layer. In the on-state as shown in Fig. 5-11b, a sufficient negative gate bias \(-V_G\) will accumulate region II and a drain current \(I_D\) will flow when the drain voltage \(-V_{DS}\) is applied between the drain and source. Since region II is accumulated, \(I_D\) is controlled by regions I and II and must be a drift current which can be modeled to a first approximation, as Eq. 5-3

\[ I_D = eN_A \mu_p V_A / L_G \]  

(Equation 5-3)

Here \(N_A\) is the semiconductor doping density and \(V_A\) is a voltage obeying \(V_A \leq V_{DS}\). Eq. 5-3 describes the linear range of the output characteristics of an AMOSFET and is quite different from Eq. 5-1. The difference arises from the presence of regions I and III and from the presence of ohmic metal-semiconductor source-drain contacts to the p-material which regions I and III remove from the edges of the channel. Eq. 5-3 points out that, because of this structure, the linear region output characteristics of an AMOSFET are controlled by the doping \(N_A\) and not by the gate capacitance per area \(C_1\) as in Eq. 5-1. This equation further shows that \(I_D\) in the linear region will be of the order of the current which would flow for the same \(V_{DS}\) if there were no gate present. This can be controlled by adjusting the doping.

In this on-state situation, for a given \(V_{DS}\), the electric field from the source to the negatively biased drain must be significantly smaller in the accumulation layer than it is in regions I and III. Consequently, a negative charge in region I adjacent to the region I/region II boundary of Fig. 5-11 must develop. This charge in the p-type material can only come from a depletion region. Consequently, we propose that in an AMOSFET there is some \(V_{DS}\) in the on-state at which the \(V_A\) in Eq. (2) becomes fixed at \(V_A^\ast\) and
further increases in $V_{DS}$ take place across this depleted region. This causes the current to saturate at a value given by Eq. 5-4. The output and transfer characteristics that will result ideally from this overall behavior have the features expected of a “conventional” MOSFET.

$$I_D^S = eN_A \mu_p V_A^S / L_G$$ (Equation 5-4)

In addition, Because of this device’s use of ohmic contacts for the majority carriers of the single doping-type semiconductor and their positioning away from the channel edges, it suppresses the possibility of ambipolar behavior. We show experimentally that it does this quite successfully while achieving on-off ratios of $10^6$. The device is simple in structure and requires only one doping type which may be n or p, allowing CMOS architectures to be implemented. It requires no heavily doped n+ or p+ contacts. Instead the source and drain contacts to the material are ohmic metal contacts. The volume under the gate that becomes depleted in the off-state occupies the whole depth under the gate necessitating that this region be an ultra-thin semiconductor layer.

To further confirm this AMOSFET model, we uniformly ion-implanted the whole SiNWs to $1 \times 10^{18}$ cm$^{-3}$ (the TRIM simulation value). Due to the limit number of samples, only several transistors were fabricated from them and characterized. Unfortunately, the transistors showed leakage through gate electrode when gate voltages exceeded -1v. Additional researches are needed to optimize the ion-implantation doping parameters and oxidation. However, the transistors worked well for gate voltages smaller than -1V and gave us some information to confirm our AMOSFET model. Fig. 5-12 shows the output characteristics and the comparisons between the unintentionally doped SiNW transistor
(black plots) and the uniformly ion-implanted SiNW transistor (red plots), with gate voltages smaller than -1v. From the comparison, the current levels were increased about 3 orders of magnitude higher by the ion-implantation with the same gate voltages, at least in the gate voltage smaller than -1V regions. The ion-implantation work further confirmed that the doping determined the on-current, instead of the inversion layer in the conventional MOSFET.

From the discussions above, the mobility for our transistors should be extracted from the Eq. 5-3. Since we used unintentionally doped SiNWs and the doping concentration \( N_A \) is unknown, we can not calculate the real precise mobility value. Till now, no work in the literature has been done in measuring the doping concentration of the unintentionally doped SiNW. The doped SiNWs, such as boron doped SiNWs, in the literature are grown and doped by controlling flow rated of \( \text{SiH}_4 \) and \( \text{B}_2\text{H}_6 \) or TMB. The doping concentrations for these doped SiNWs are unknown either. A previous effort on

Figure 5-12: Output characteristics for our transistor made from unintentionally doped (black plots) and uniformly ion-implanted SiNWs (red plots).

From the discussions above, the mobility for our transistors should be extracted from the Eq. 5-3. Since we used unintentionally doped SiNWs and the doping concentration \( N_A \) is unknown, we can not calculate the real precise mobility value. Till now, no work in the literature has been done in measuring the doping concentration of the unintentionally doped SiNW. The doped SiNWs, such as boron doped SiNWs, in the literature are grown and doped by controlling flow rated of \( \text{SiH}_4 \) and \( \text{B}_2\text{H}_6 \) or TMB. The doping concentrations for these doped SiNWs are unknown either. A previous effort on
SiNW doping concentrations were carried out by secondary ion mass spectrometry (SIMS) [23]. However, this technique did not give accurate measurements due to its detection limit. It was difficult to accurately determine boron concentrations lower than \(1 \times 10^{18} \text{ cm}^{-3}\) in the nanowires using SIMS analysis. So there are no accurate doping concentrations available for unintentionally doped SiNWs and intentionally doped SiNWs, and the accurate calculation of mobility is not possible in this stage. However, if we reasonably estimate the doping concentration of our unintentionally doped SiNWs in the range between \(1 \times 10^{14} \text{ cm}^{-3}\) to \(1 \times 10^{16} \text{ cm}^{-3}\), then the calculated mobility of our transistor will be in the range of 10 \(\text{cm}^2\text{V}^{-1}\text{s}^{-1}\) to 1000 \(\text{cm}^2\text{V}^{-1}\text{s}^{-1}\). More work should be done to get accurate mobility calculation. Controlled doping such as ion-implantation can also be used to accurately dope the SiNWs and determine their mobilities for doped SiNWs.

### 5.8 Summary

In summary, we demonstrated a novel extruded/short nanochannel-template-guided “grow-in-place” approach for making nanowire transistors. Taking unintentionally doped SiNWs as example, we successfully made high performance SiNW transistors with no post-synthesis collection, nanowire alignment, and assembly steps, which overcame the difficulties in making nanowire devices from mass grown nanowires. With the SiNWs fixed and confined by the extruded/short nanochannels, the electrode contacts can be easily defined by simple photolithography. Our transistors offer high performance with high turn on/off ratio and sharp subthreshold slope. Our “grow-in-
place” nanowires can be easily combined with proper doping, structure design to further enhance device performances.

In this chapter, we made the demonstrating transistors with only one single SiNW by using our extruded/short nanochannel-guided “grow-in-place” approach. However, transistor devices with arrays of SiNWs can be made in the similar way with desired SiNW number and spacing. The spacing between the wires could be small to the limit of the making system, such as the limit of electron-beam lithography or nanoimprinting with sub-100nm spacing capacity. The nanowires are not limited to SiNWs, Other nanowires or nanotube devices can be fabricated by using different catalysts, precursor gases, and growth conditions. This approach is manufacturable since plenty of devices can be defined on the same substrate by techniques, such as nanoimprinting. In addition, because only the amount of nanowires needed is grown and those nanowires are always fixed by the nanochannels, this is a green technique with environmental benignancy. We believe that our approach offers a good way of making nanowire devices with good controls and in a manufacturable and environmentally friendly way.

In addition, an AMOSFET model was proposed to explain our device performance and to properly extract the mobility. Future work is needed to determine the doping concentrations and to extract the accurate mobility values.
References


Chapter 6

Summary and future work

6.1 Summary

In this thesis, we introduced a novel self-assembling “grow-in-place” approach for SiNW growth control and device fabrication. Our research has demonstrated for the first time that it is possible to go directly from a silicon precursor gas (e.g., SiH₄) to well controlled, self-assembled, and self-positioned SiNW/R devices without any intervening silicon material formation, collecting, positioning, and assembling steps. Our grow-in-place approach solved the major problems and challenges in nanowire growth control and nanowire device fabrication.

Crystalline SiNW/Rs have been successfully grown in nanochannel templates through our grown-in-place approach. From characterizations, we have shown that the pre-fabricated nanochannel templates could enable and control the VLS growth of SiNW/Rs. The nanochannel templates in our approach could be made where nanowires were needed and became permanent parts of the final devices. The nanochannels guided the SiNW/Rs through VLS LPCVD growth and offered good SiNW growth controls on their size, shape, number, orientation, position, and inter-wire spacing. The nanochannels confined and fixed the grown SiNWs for easy device fabrication. The electrode contacts could be either built-in to the nanochannel templates before nanowire growth or could be fabricated after nanowire growth and optimization.
SiNW transistors have been successfully fabricated from our well controlled grow-in-place SiNWs with back-gate, top-gate, and their combination geometries. Transistor fabrications were carried out from our encapsulated/long nanochannel templates and extruded/short nanochannel templates. These fabrications solved the major challenges in making nanowire devices due to the extreme small size of SiNWs.

The SiNW transistors made from encapsulated/long nanochannel templates offered full controls on SiNW growth, especially shape and precise inter-spacing. Source and drain electrodes could be built-in to capping layers of the nanochannel templates before nanowire growth. Silicon substrate could serve as the back-gate electrode and the top-gate electrodes could be built on the capping layer. SiNW transistors were ready after SiNW growth without any post-growth fabrication steps. Future work on alternative lithography techniques and high quality capping layers may solve the leakage problems and enhance device performance.

The SiNW transistors made from extruded/short nanochannel templates offered SiNW post-growth optimizations, such as catalyst removing, cleaning, oxidation and passivation. The thermal grown oxide shell around SiNW core offered high quality dielectric layer and interface. With the SiNWs fixed by extruded/short nanochannels, source/drain and gate electrodes were patterned by photolithography. The top-gate core-shell SiNW transistors made from our extruded/short nanochannel grow-in-place approach offered high transistor performance with on/off ratio of $10^6$ and sharp subthreshold slope (S) of 130 mV/Dec.

Mobility analyses for our SiNW transistors were carried out and an accumulation type MOSFET transistor model was proposed. Our AMOSFET transistors have an on-
state that arises from the presence of an accumulation layer under the gate and an off-
state that arises from fully depleting this region of the SiNW under the gate. The on-
current is not controlled by the gate capacitance, and the on-current is controlled by the
semiconductor doping concentration. Our initial ion-implantation work further supported
this device model. We have suggested that mobility calculation and device analysis
should be carried out by using this new AMOSFET model.

For the nanochannel fabrications in this thesis, the electron-beam lithography was
used to define the nanochannels. Other methods, such as nanoimprinting, immersion
lithography can also be used as alternative methods to remove the high-energy electron
damages and improve the manufacturability. SiNWs have been grown by our grow-in-
place approach and served as the demonstration. However, nanowires or nanotubes with
other materials, such as Ge, ZnO₂ or Si/Ge junction structure, also have the potential to
be controlled grown through this approach by using different catalysts, precursor gases,
and growth conditions. SiNW transistor fabrications were taken as an example to
demonstrate our grow-in-place approach of device fabrication. However, other
applications such as sensors could also be fabricated in the similar way with proper
device designs and structures. For the SiNW transistor fabrications, we made the
demonstrating transistors with only one single SiNW by using our “grow-in-place”
approach. However, transistor devices with arrays of SiNWs can be made in the same
way with desired SiNW number and spacings. The spacings between the nanowires can
be small to the limit of the making systems, such as the limit of electron-beam
lithography or nanoimprinting with sub-100nm spacing capacity.
The grow-in-place approach we have developed is environmentally safe since the fabricated nanowires are always confined and fixed; only the exact number of nanowires needed is fabricated. The growth nanochannels are horizontally arrayed and become a permanent part of the device structure. We believe this grow-in-place approach points the way to a manufacturable, high-throughput, and environmentally safe methodology for fabricating nanowire/ribbon devices which self-assemble and self-position into integrated circuits.

6.2 Future work

To optimize nanochannel fabrication, SiNW growth, transistor fabrication, and performance, future work is needed.

First, more work is needed to optimize our nanochannel template fabrication, especially for the encapsulated/long nanochannel templates. The encapsulated/long nanochannel template offers precise control on nanowire growth, especially on nanowire size, shape, and inter-wire spacing. The contacts for source/drain can be built inside the nanochannel template, so there is no post-growth process and nanowire devices are ready after SiNW growth. However, there were leakage problems for nanowire devices made from these encapsulated/long nanochannel templates. The leakage currents came through low quality or damaged dielectric layers. These dielectric layers could be either the low quality capping layer or the damaged oxide on the silicon substrate caused by the high energy electron-beam direct writing. To solve these problems, more researches should be carried out in making high quality capping layers or removing the damages from the
oxide/nitride on the silicon substrate. Possible solution could be using atomic layer deposition to deposit high quality films, especially high K dielectric layers, such as Al₂O₃, ZrO₂, or HfO₂, for both capping layer and bottom layer on silicon substrate. The electron-beam writing in the nanochannel definitions can also be replaced by non-damage lithography, such as nano-imprinting, immersion lithography to remove the high energy electron damages to the dielectric layer on the silicon substrate.

Second, more work is needed to optimize SiNW controlled growth. This work may include growth condition optimizations, including temperature, pressure, and gas flow rates to favor the heterogeneous deposition, while reduce the homogenous deposition. This is important to reduce the Si homogenous deposition on the nanochannel inlets and sidewalls. SiNW n/p type doping and selective doping are also important. More work is needed to determine dopant gas species, flow ratio, temperature, and their relation with the final doping concentrations. The doping interface quality is another concern for selective or n/p alternative doping profile.

Third, more work is needed to optimize our transistor fabrication and performance. For the transistors made from our grow-in-place SiNWs, the as-grown unintentionally doped SiNW gave relative low current level. To increase the current level, we can make devices by using nanowire array and nanoribbons. We can also increase the current level by proper doping. Selective doping is another way to enhance the transistor performance. In addition, contact effects between different metals with p or n type SiNWs can also be researched. Our “grow-in-place” approach can be combined with proper doping and structure design to further enhance device performance.
Fourth, the distances between the source/drain and gate electrodes can be adjusted to research the distance effects on the unipolar/ambipolar effect of transistors.

Fifth, more work is needed to develop more possible applications, such as sensing especially bio-sensors, from our grow-in-place approach, especially by using the extruded/short nanochannel device fabrication.

Sixth, nanowires or nanotubes with different materials could be grown and researched through our grow-in-place approach. Such materials include carbon nanotubes, Ge nanowire, Ge/Si heterostructure, ZnO$_2$ nanowires for different properties and applications.
Appendix

Nontechnical Abstract

Silicon nanowires (SiNWs) have attracted much attention recently, owing to their ability to serve as critical building blocks for emerging nanotechnologies. SiNWs are particularly promising because of the central role of silicon in semiconductor industry. The bulk properties of silicon have been well understood and the carrier type and concentration are well controllable. These would allow SiNW device fabrication to be compatible with current technologies and equipments. In addition, the extremely small size of SiNWs allows device fabrication with extremely high density and also offers high sensitivity. Applications have been demonstrated ranging from nanoelectronics to biosensors, such as transistors, protein sensors, and single virus sensors. Therefore, heavy researches have been carried out in SiNW growth and device fabrication.

The main advantage of SiNW growth is that silicon inherently grows in nanometer size. There is no need of complicated processes. The surface of the grown SiNW is much smoother and the doping can be well controlled during nanowire growth. SiNWs have been successfully grown through different methods. However, for most current SiNW growth methods, a large number of SiNWs was usually grown on the substrate in a messy condition; there are still big challenges in SiNW growth controls, such as SiNW size, number, position, orientation and inter-wire spacing. To make devices from these SiNWs, post-growth device fabrication steps are also needed. Due to the extremely small size of SiNWs, these device fabrication steps, such as SiNW
collecting, picking, positioning, aligning, and assembling, are extremely difficult. Most of current device fabrication methods are slow processes, low throughput, not mass manufacturable, and not compatible with standard semiconductor fabrication.

To solve these challenges in SiNW growth control and these difficulties in device fabrication, a novel self-assembling “grow-in-place” approach is introduced in this thesis. Pre-fabricated nanochannel templates in this approach confine, guide nanowire growth, and offer precise nanowire growth control. SiNWs with different sizes have been successfully grown in the nanochannel templates. Characterizations have indicated that this “grow-in-place” approach gave good control on crystalline SiNW size, shape, number, orientation, position, and inter-spacing. With the grown SiNWs confined and fixed by the nanochannel templates, SiNW transistors can be easily fabricated in-place where SiNWs are grown, without any post-growth fabrication difficulties, such as SiNW collecting, picking, positioning, aligning and assembling. SiNW transistors have been successfully fabricated from these well-controlled nanowires. Characterizations have shown that these transistors offer high performances with on/off ratio of $10^6$.

From the SiNW growth and transistor fabrication, this “grow-in-place” approach offers a novel way to make well controlled nanowires, to fabricate SiNW devices, and to assemble them into rational device geometries. The approach is also environmentally safe and benign since the fabricated nanowires are always confined and only the exact number needed is fabricated.

The applications of this “grow-in-place” approach are not limited in SiNW growth control and transistor fabrication. Nanowires from other materials, such as germanium and zinc oxide, and other devices, such as sensors, could also be developed
from this approach. So this “grow-in-place” approach points the way to a manufacturable, high-throughput, and environmentally safe methodology for fabricating nanowire devices which self-assemble and self-position into integrated circuits.
VITA

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Yinghui Shan was born on December, 02 1977, in Hebei China. He graduated from University of Science and Technology of China (USTC) in 2002 with a B.S. degree in Materials Chemistry and B.S. Minor in Electrical Engineering. Yinghui Shan began his graduate studies at The Pennsylvania State University in August 2002. He has authored or co-authored several papers and patents in Si nanowire controlled growth and device fabrication. Yinghui Shan’s research interests are in nano-, micro- device fabrication and characterization, nanowire growth and application.