

The Pennsylvania State University

The Graduate School

College of Engineering

**STRAIN ENGINEERING FOR STRAINED P-CHANNEL NON-PLANAR TRI-
GATE FIELD EFFECT TRANSISTORS**

A Thesis in

Electrical Engineering

by

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ABSTRACT

In this thesis the optimization of embedded source/drain (eS/D) shape profiles and device layouts for the 22nm node compressively strained P-channel tri-gate field effect transistors (FETs) is investigated using finite element method (FEM) simulations. Three device layout strategies namely 1) Nested fin layout 2) Nested gate layout and 3) Double nested layout were studied and the nested gate layout was found to introduce the maximum channel stress of all three. Out of the three eS/D shape profiles namely 1) Rounded eS/D 2) Sigma eS/D and 3) Square eS/D, square shaped S/D regions are found to induce maximum channel stress due to minimum average source to drain distance making them the best candidates for nested tri-gate transistors contrary to the planar case. Strained silicon-germanium (SiGe) FETs being a potential candidate for future technology nodes, a comparison between Si and $\text{Si}_{0.4}\text{Ge}_{0.6}$ with $\text{Si}_{0.6}\text{Ge}_{0.4}/\text{Ge}$ eS/D P-channel tri-gate FETs for the nested gate (5 tri-gates) based on average channel stress and corresponding mobility enhancements is discussed. Superior mobility enhancement of strained $\text{Si}_{0.4}\text{Ge}_{0.6}$ channel compared to strained Si channel offsets the disadvantage of the $\text{Si}_{0.4}\text{Ge}_{0.6}$ channel stress being slightly less than the Si channel. The evolution of the channel stress following S/D recess etch and eS/D re-growth for uniaxially strained SiGe fins obtained via global strain is also investigated to evaluate the maximum achievable stress levels for a combination of globally and locally induced uniaxial strain. The eS/D stressor technique is expected to remain an important technique especially in the face of channel strain relaxation following S/D ion implantation for extremely scaled P-channel tri-gate FETs with globally induced channel strain.

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1. INTRODUCTION

Moore's law has proved remarkably successful in predicting the phenomenal progress of the semiconductor industry since it was first stated. Fig. 1.1 and 1.2 illustrate the transistor count increase and the improvement in performance with subsequent technology nodes. The path breaking progress of the semiconductor industry has been possible due to continuous downscaling of the metal oxide field effect transistor (MOSFET) [1]. The downscaling of the MOSFET has not only significantly improved the performance of electronic gadgets but also brought down the cost per function drastically while continuously increasing the functions per unit chip area [1].

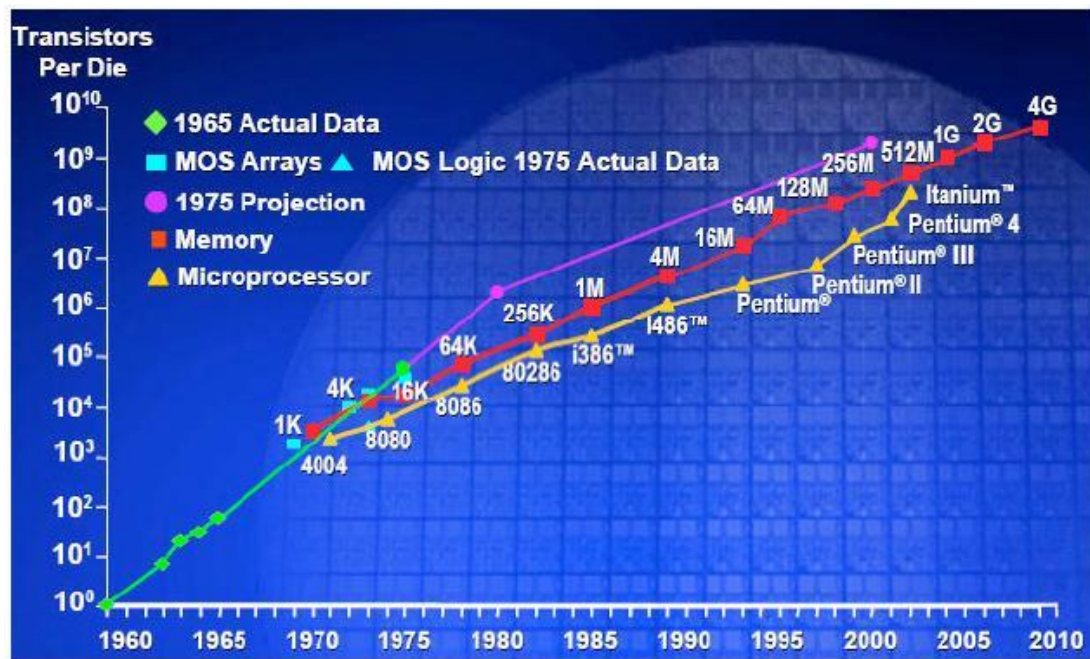


Fig. 1.1 Chip transistor count for memory and logic technology generations [1]

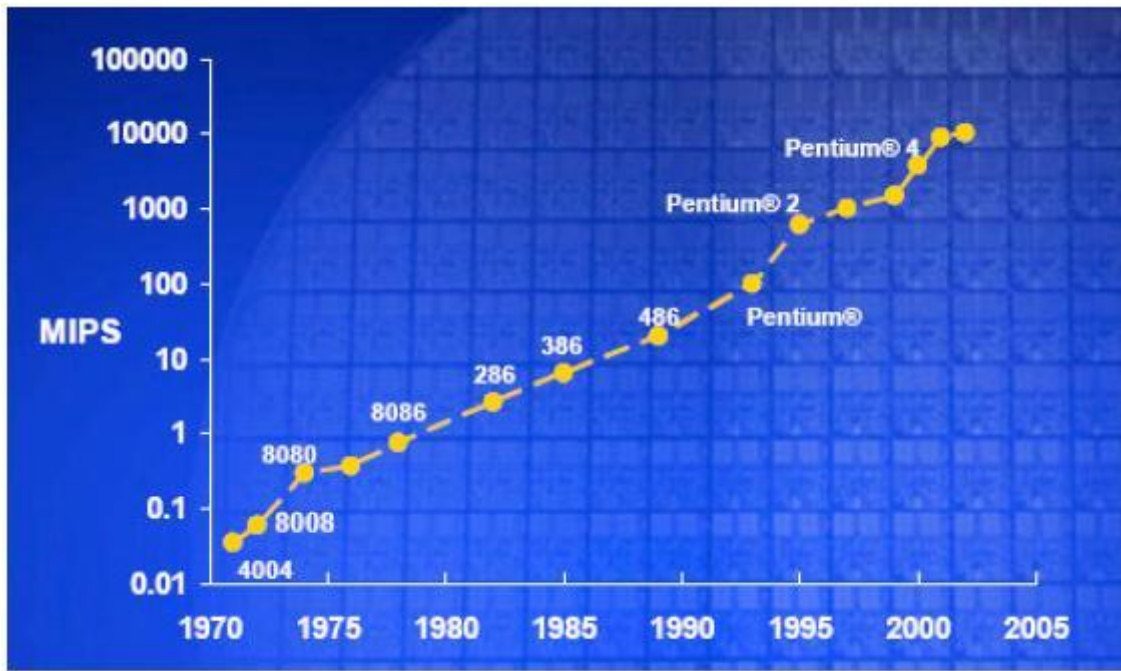


Fig. 1.2 Chip's performance in million instructions per second [2]

However in the recent years it has become painfully obvious that simple downscaling of the MOSFET will not result in the expected performance improvement of the MOSFET. In fact it is seen that further traditional scaling beyond the 90nm technology resulted in a significant degradation in the MOSFET performance implying the end of traditional MOSFET scaling and the benefits following it [3]. It was then that strain was introduced in state of the art MOSFET technology to regain the desired performance and paved the way for further scaling of the MOSFET [3]. Strain alters the band structure of the semiconductor favorably improving carrier mobility translating to improved device performance as discussed later [4-6].

The band structure of a semiconductor is one of its most important features providing useful insights into the electrical and optical properties of the particular semiconductor and thus gives us an idea of the possible applications for that particular semiconductor. Silicon has been the workhorse of the semiconductor industry especially in state of the art complementary metal oxide semiconductor (CMOS) technology nodes for almost 40 years [3]. It is therefore imperative to investigate Silicon's band structure thoroughly.

1.1 Silicon (Si) and Germanium (Ge) valence band structure

Silicon features an indirect band gap of 1.12 eV at room temperature [7]. The bulk band structure of silicon is shown in Fig. 1.1 below. Let us focus on the valence band structure which is comprised of three different bands out of which two bands, namely the heavy hole band and the light hole band are degenerate at the gamma point. The third band is the split off band which is separated from the other two bands at the gamma point by 0.044eV. The hole energy E versus wave vector (k) curves obey a parabolic relationship near the corresponding valence band maxima. The parabolic E - k relationship is as given below [8].

$$E = \hbar^2 k^2 / 2m^*$$

where $\hbar = h/2\pi$ is the modified Planck's constant and m^* is the carrier effective mass.

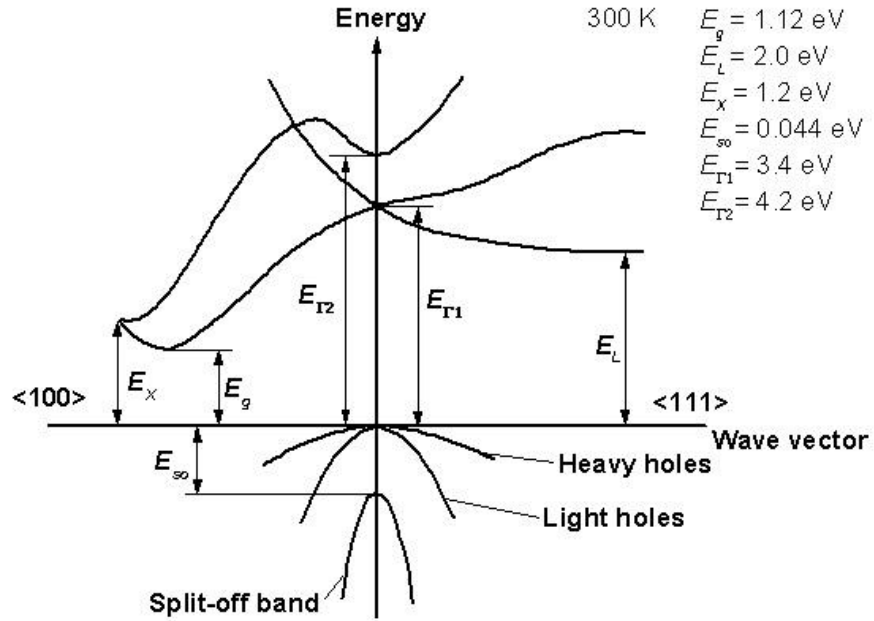


Figure 1.3: Silicon bulk band structure [7]

As the name suggests the heavy hole band has a higher hole effective mass than the light hole band along the crystal directions shown in Fig. 1.3. The hole mobility (μ) is inversely proportional to the hole effective mass (m^*) as given below.

$$\mu = q\tau/m^*$$

where τ is the carrier relaxation time constant.

Thus it is beneficial to have a lighter hole transport effective mass for improved performance.

The valence band structure of Ge is similar to Si as shown in Fig. 1.4 below with the difference that the effective masses of the heavy hole, light hole and split off bands are significantly lower than those of Silicon [7] making Ge an attractive option for future PMOSFETs.

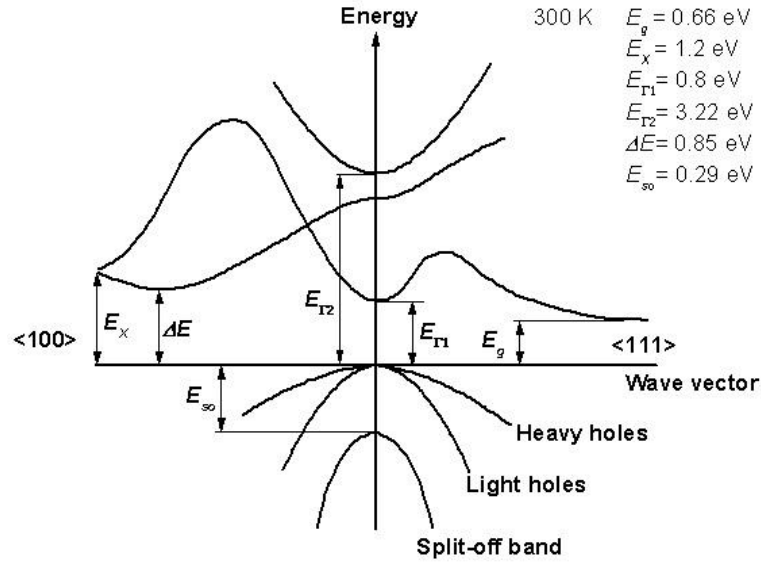


Fig. 1.4 Ge bulk band structure [7]

1.2 Valence band structure in a PMOSFET

In a MOSFET the carriers are confined close to the surface causing quantization of the carrier energy levels. This lifts the degeneracy of the light hole (lh) and heavy hole (hh) bands at the gamma point [5] as shown in Fig. 1.5 below. Increasing the normal electric field increases the degree of carrier confinement consequently increasing the splitting of the lh and the hh bands [5]. The typical channel orientation is along the <110> direction with the plane being (100) for CMOS.

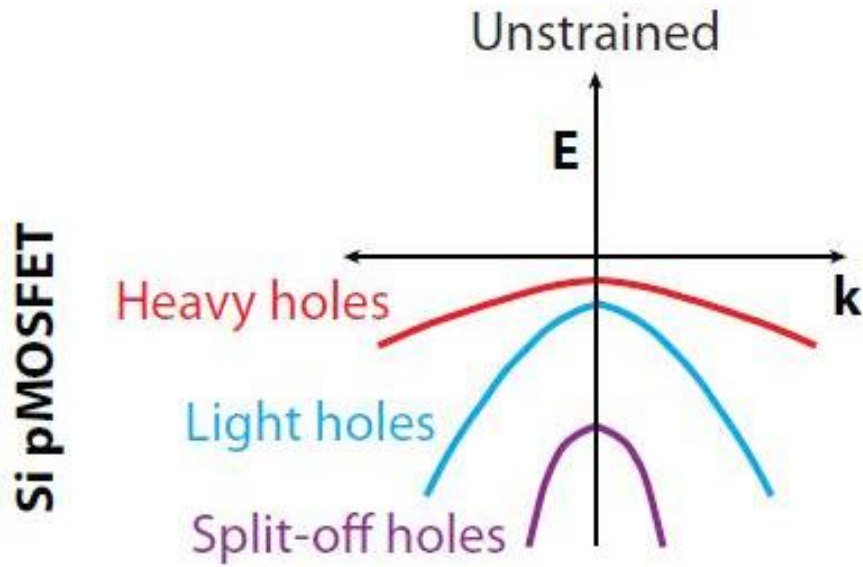


Fig. 1.5 Band splitting in MOSFET inversion layers [5]

1.3 Strained Si valence band structure

The lh and hh band degeneracy can also be lifted by destroying the crystal symmetry which is achieved by applying strain to the lattice. Strain not only lifts the degeneracy but also causes band warping which causes a significant reduction in the carrier effective mass [5]. The effective mass reduction due to band warping is the prime reason for the performance enhancement of PMOS [5]. The effects of biaxial and uniaxial strain are quite different in terms of the band warping and the splitting of the lh and hh bands. The valence band structure depends on the surface and channel orientation and similarly the strain effects also depend in the surface and channel orientation as can be seen in Fig. 1.6 below. It has been theoretically and experimentally proven that strain along $\langle 110 \rangle$ direction provides the largest mobility enhancement [5]. We can see from

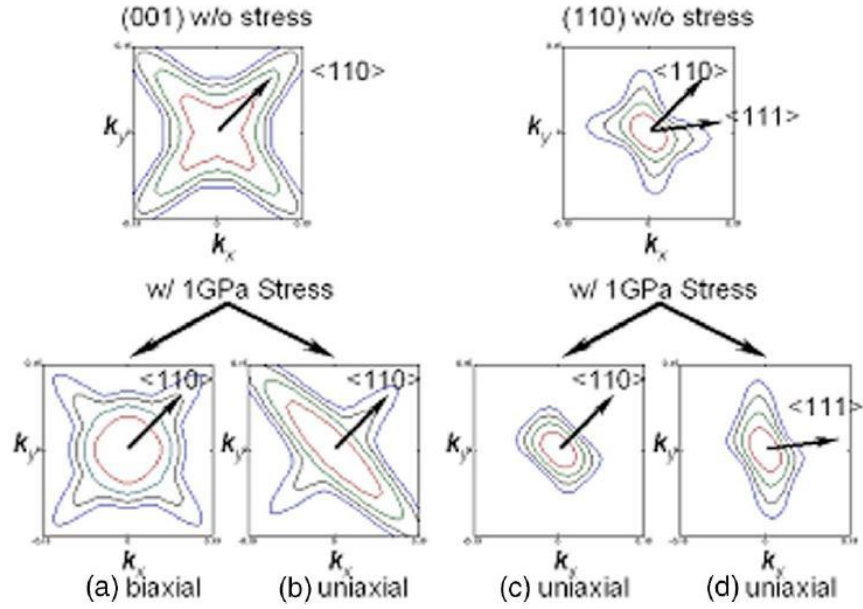


Fig. 1.6 Constant energy in plane k-contours for unstrained and strained Si hole inversion layers with different surface orientations [9]

Fig. 1.6 that for the (100)/ $\langle 110 \rangle$ channel orientation we get a significant reduction in the effective mass compared to the unstrained case. It is also evident that uniaxial compressive strain along $\langle 110 \rangle$ is more beneficial than biaxial compressive strain providing a much larger enhancement in the (100)/ $\langle 110 \rangle$ hole mobility. Applying strain for the (110)/ $\langle 110 \rangle$ channel doesn't provide significant mobility enhancement however the unstrained hole effective mass for the (110)/ $\langle 110 \rangle$ system is quite less than that for the (100)/ $\langle 110 \rangle$ channel as is evident from Fig. 1.6. Thus it is obvious that below a particular level of strain the (110)/ $\langle 110 \rangle$ channel will outperform the (100)/ $\langle 110 \rangle$ channel in terms of hole mobility.

1.3 Conclusion

The valence band structure of Si and Ge is quite complex and varies with both the surface and crystal direction. It is comprised of three different bands namely the heavy hole, light hole and the split off band. The heavy hole and light hole bands are degenerate at the gamma point for the bulk cases. The split off band maxima is located 44 meV below the other two bands' maxima for Si whereas for Ge the split off band is located 290 meV below the other two bands. Ge features significantly lower hole effective masses compared to Si consequently possessing higher hole mobility.

Carrier confinement in a PMOSFET inversion layer lifts the degeneracy of the hh and lh bands. The band splitting in a PMOSFET is proportional to the applied gate field. The lh and hh band degeneracy can also be lifted by applying strain to the lattice. Strain destroys the crystal symmetry and thus not only lifts the degeneracy but also causes band warping. The curvature of the hh band near the gamma point increases due to applied strain reducing the carrier effective mass and improving hole mobility. Uniaxial strain along the $\langle 110 \rangle$ direction causes the greatest reduction in hole effective mass thus offering a significant hole mobility enhancement.

2. STRAINED P-CHANNEL MOS/FIN/TRI-GATE FETS

2.1 Introduction

The benefits provided by strain in terms of performance enhancement are crucial for extending Moore's law beyond 90nm technology nodes. As seen before uniaxial compressive strain is more beneficial than biaxial strain for PMOSFET. Uniaxial strain not only provides a larger mobility enhancement but also causes a smaller threshold voltage shift compared to biaxial strain [5]. It is not surprising therefore that the focus has shifted from implementing biaxial strain to uniaxial strain in state of the art CMOS technology nodes. PMOS also shows a greater enhancement factor than NMOS with uniaxial strain [5] translating to a more balanced performance which is suitable for complementary technology. The channel orientations of interest for compressively strained PMOSFETs are i.) The (100)/ $\langle 110 \rangle$ channel due to its high mobility enhancement factor and ii.) The (110)/ $\langle 110 \rangle$ channel due to its inherently higher hole mobility than the (100)/ $\langle 110 \rangle$ channel [5] as seen before.

The key techniques for introducing uniaxial compressive strain in the Si channel are the embedded SiGe source-drain and compressive contact etch stop layer (cCESL) techniques [5].

2.2 Planar PMOS with embedded source/drain (S/D)

The embedded SiGe S/D technique was introduced in the 90 nm technology node and has been one of the key features of all the subsequent technology nodes [3]. This technique is implemented quite easily by introducing only a few additional steps in the conventional device process flow [3]. The embedded SiGe source-drain technique utilizes the lattice mismatch between Si channel and the SiGe source-drain to compressively strain the Si channel. The incorporation of embedded SiGe source-drain begins by a recess etching of Si in the source-drain regions followed by an epitaxial growth of the SiGe S/D regions with the desired Ge content. The embedded S/D recess etch depth is equal to the required thickness of the embedded SiGe S/D regions and is decided by the Ge content in the embedded SiGe S/D. Fig 2.1 shows a typical PMOSFET with embedded SiGe S/D regions.

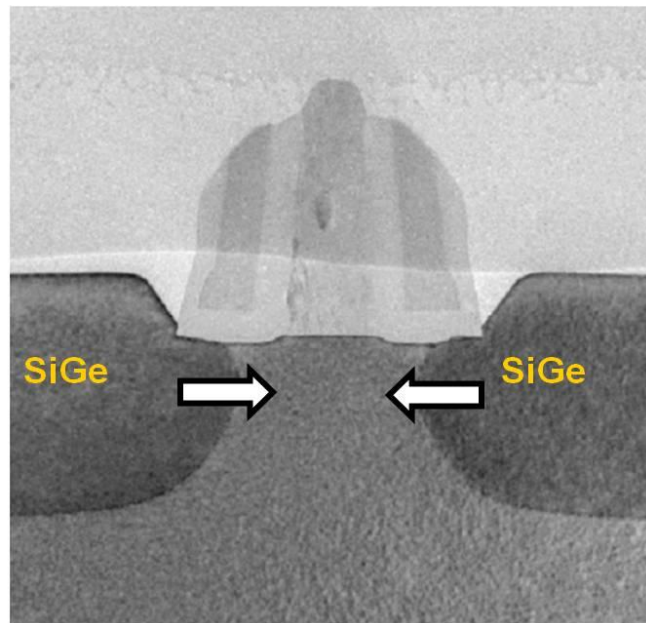


Fig. 2.1 Cross sectional TEM image of (100) eSiGe pFET [3]

It is essential that the embedded S/D regions remain defect free throughout in order to induce maximum strain in the channel as well to eliminate performance degradation due to defects. The maximum defect free thickness of the embedded SiGe S/D region is dictated by its lattice mismatch or equivalently its Ge content with the underlying Si substrate. The maximum thickness up to which a strained layer can be grown defect free is termed as the strained layer's critical thickness [10, 11]. Although it is possible to achieve meta-stable growth where the strained layer's thickness exceeds its critical thickness [12] the succeeding high temperature annealing steps will cause defects in the strained layers which are not acceptable. Thus it is advisable to have the embedded SiGe S/D region's thickness smaller than its critical thickness.

The embedded S/D technology has evolved over the subsequent technology nodes with the Ge content increasing from one technology node to the next. A considerable amount of effort has also been devoted to engineer the shape of the embedded S/D regions for maximizing the channel stress with the same S/D Ge content. The rounded embedded SiGe S/D as seen in Fig. 2.1 have been replaced by sigma shaped S/D regions as shown in Fig. 2.2 below. The sigma shaped S/D regions induce a greater stress in the channel than the rounded S/D regions as shown in Fig. 2.3. The sigma S/D regions have an added advantage of being virtually defect free due to the presence of (111) like surfaces (S/D and channel interfaces) which is not the case for rounded S/D regions due to presence of (110) like surfaces [13].

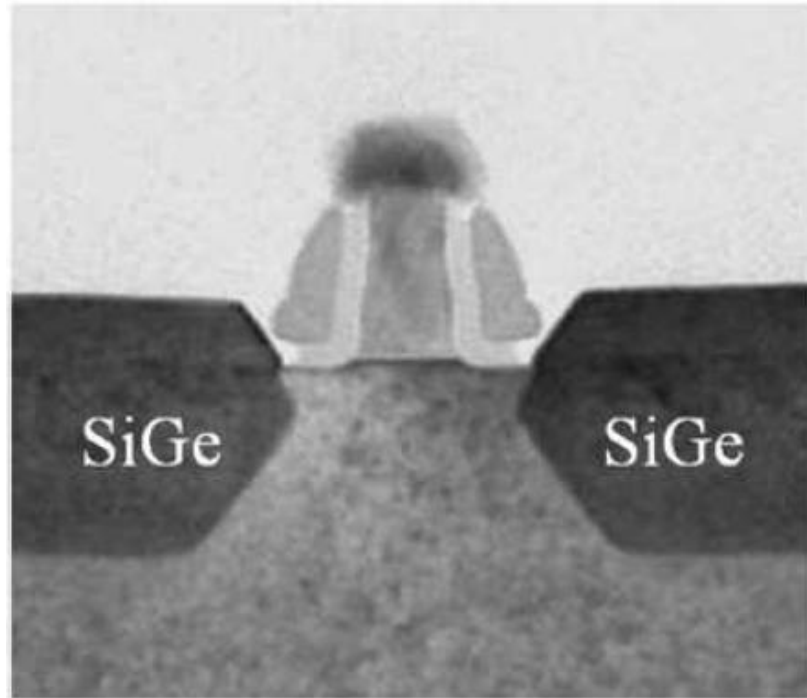


Fig. 2.2 TEM image of PMOSFET with sigma shaped S/D regions [13]

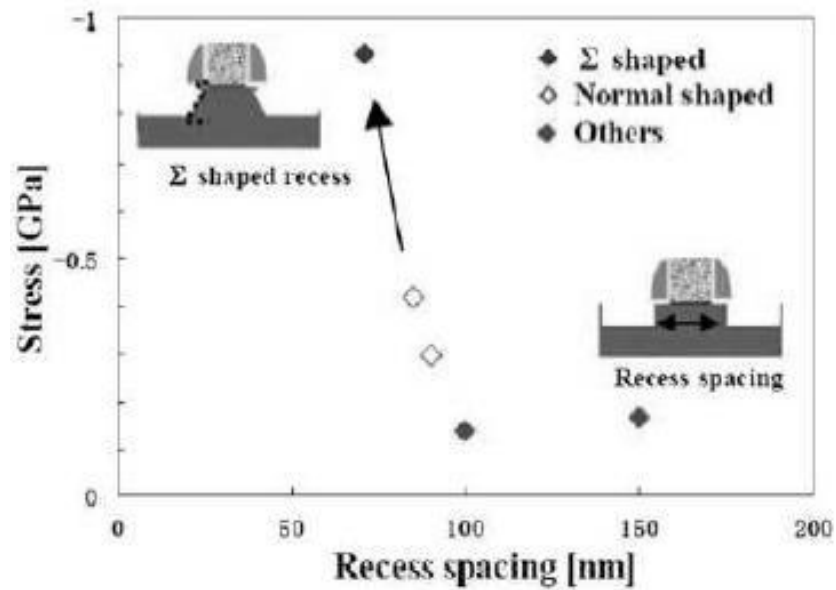


Fig. 2.3 CBED stress measurements with different recess shapes [13]

Additional modifications related to engineering the channel stress with the sigma S/D regions have been investigated and implemented in the conventional process flow. The gate first flow has been replaced by the gate last flow to further increase the channel stress. In this process a sacrificial poly-silicon gate is deposited followed the S/D recess etch and sigma eS/D regrowth inducing compressive stress in the channel. The sacrificial gate is then etched out resulting in approximately 50% increase in the channel stress as shown in Fig. 2.4 below.

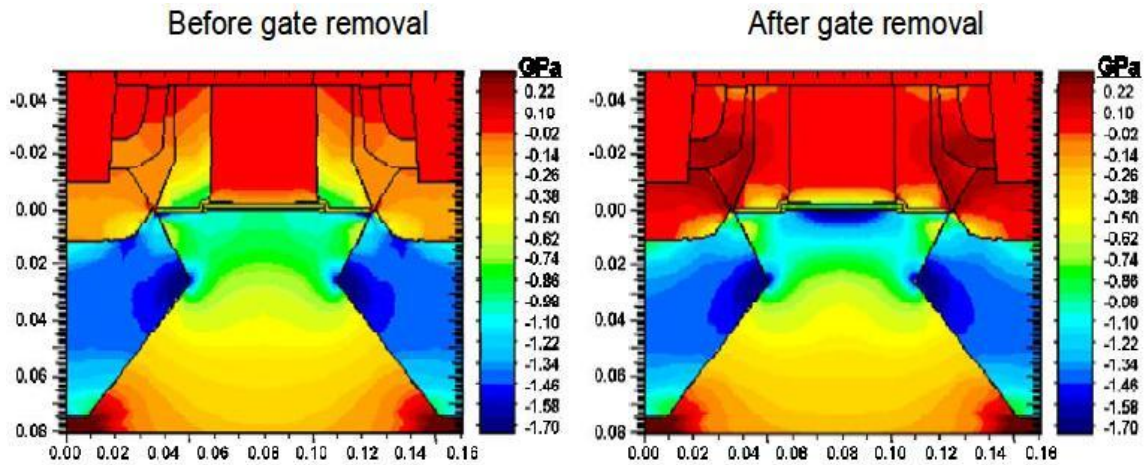


Fig. 2.4 Sacrificial gate etch resulting in a ~2x increase in channel stress [14]

2.3 Planar PMOS with etch stop layers

The second important technique for inducing strain in the channel is the use of strain inducing (tensile or compressive) etch stop layer. This technique is also relatively easy to implement in the conventional process flow. A strained etch stop layer in place of a neutral etch stop layer is deposited on top of the gate. The etch stop layer (ESL) tends to relax and in the process transfers strain to the underlying channel [15].

Fig. 2.5 illustrates typical device stress profiles using ESLs. Typically Silicon nitrides are used as stress liners for strained CMOS. Stress levels as high ~ 2.5 Gpa have been reported for strained CESLs [16].

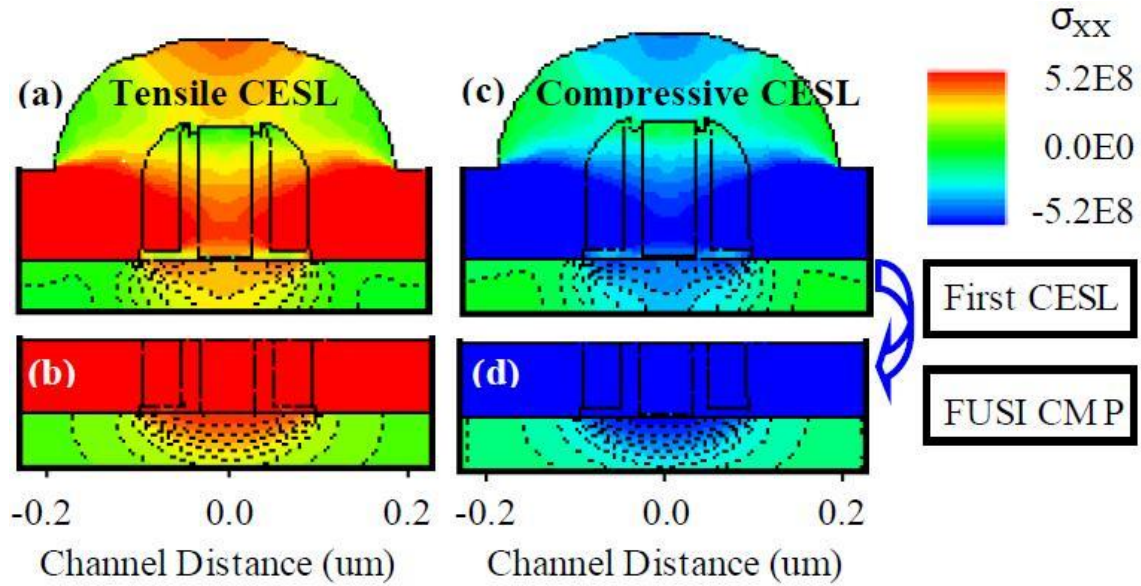


Fig. 2.5 Device stress profiles with tensile and compressive CESLs [17]

The key characteristic of a strained CESL is its stress level and the efficiency with which it can transfer stress to the channel. As MOSFET scaling advances in the sub 45 nm regime the requirements of CESL parameters are also becoming increasingly stringent to meet the corresponding technology node's performance requirements.

2.4 Strained p-channel Fin/Tri-gate FETs

The era of conventional scaling for planar MOSFETs faced some significant challenges at the 90nm technology node and the following technology generations as mentioned before. The most critical of those challenges were alleviating short channel effects such as threshold voltage shift, increased off state leakage, drain induced barrier lowering and other effects like increased gate leakage etc. Although techniques such as halo implantation, fully depleted silicon on insulator (SOI) have been resorted to alleviate the short channel effects along with the introduction of high-k/metal gate to overcome the problem of gate leakage enabling scaling to the sub 40nm regime, the short channel effects are still the greatest concern for sub 20nm technology nodes. A number of different device structures and material systems are being investigated to continue scaling beyond the 20nm technology node. Fig. 2.6 illustrates the speculated trend of the device architectures and material systems for future device generations.

Multiple gate FETs (MUGFETs) are emerging as the lead contenders for replacing planar CMOS technology for extremely scaled device architectures. MUGFETs or FinFETs attempt to address the challenge of eliminating or reducing short channel effects by implementing drastic changes in the planar MOSFET structure. Short channel effects can be mitigated by improving the gate control over the channel which is the main theme of double gate MOSFETs. MUGFETs/FinFETs take a similar approach except the fact that these are vertical structures with the gate wrapped around 3 sides as shown in Fig. 2.7 below.

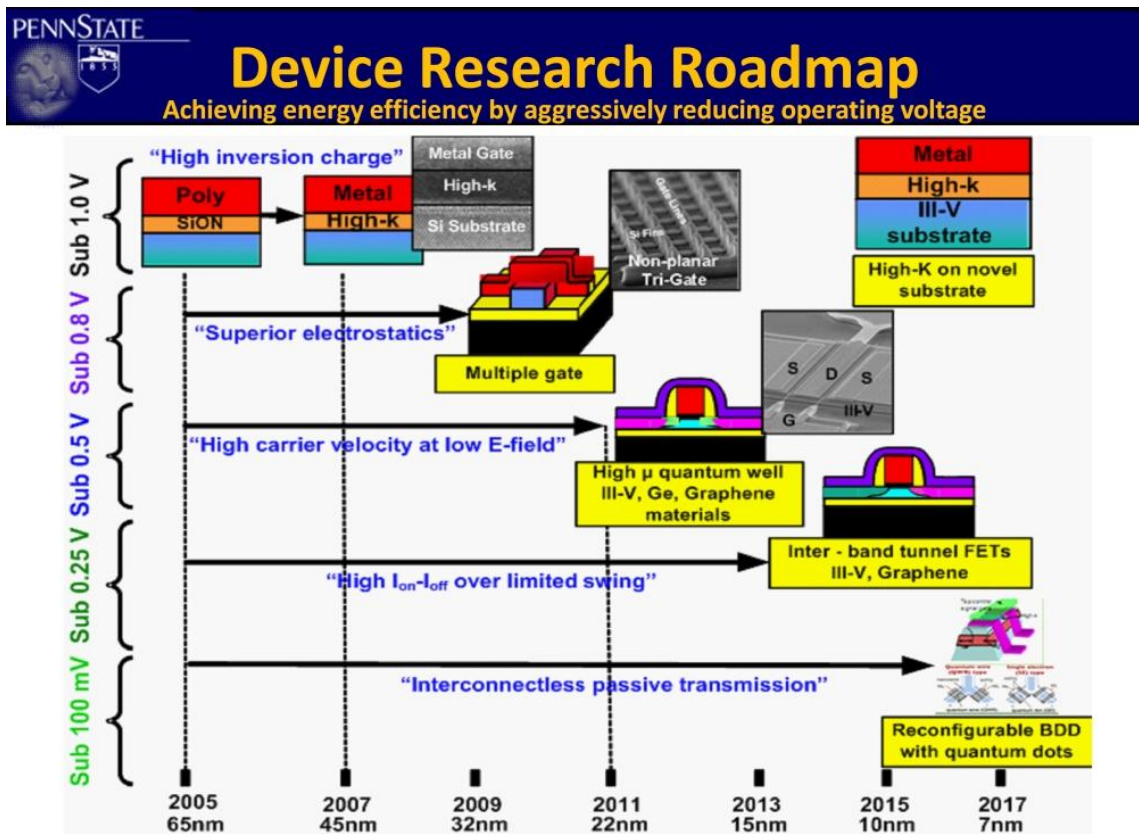


Fig. 2.6 Emerging device architectures [18]

If there is a thick oxide between the top channel and gate metal implying an un-gated top surface then the resulting structure is called FinFET [19] and is essentially a vertical double gate MOSFET. However if all the three surfaces namely the top surface and the two sidewalls are gated then the structure is called a tri-gate FET [20]. It is evident that the tri-gate/Fin FET structures will provide better gate control over the channel than in the case of planar MOSFETs as illustrated in the Fig. 2.8 significantly reducing the standby power consumption for extremely scaled devices.

Further modifications in the tri-gate/Fin FET structures like omega gate and gate all around (GAA) devices have also been proposed to obtain the ultimate gate control over the channel allowing device scaling in the sub 20nm regime.

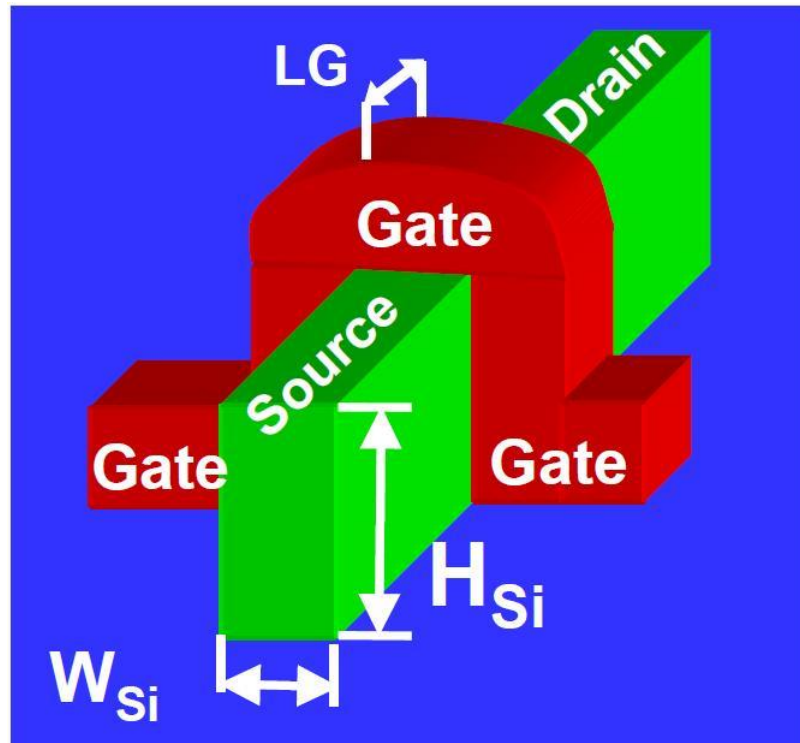


Fig. 2.7 Schematic of a MUGFET [21]

As seen before the performance improvements provided by implementing strain are critical for future technology nodes making it imperative for the subsequent technology nodes to be strain compatible. Strain induced performance enhancement for FinFETs has been investigated thoroughly both theoretically and experimentally over the past couple of years [19, 20, 23-25].

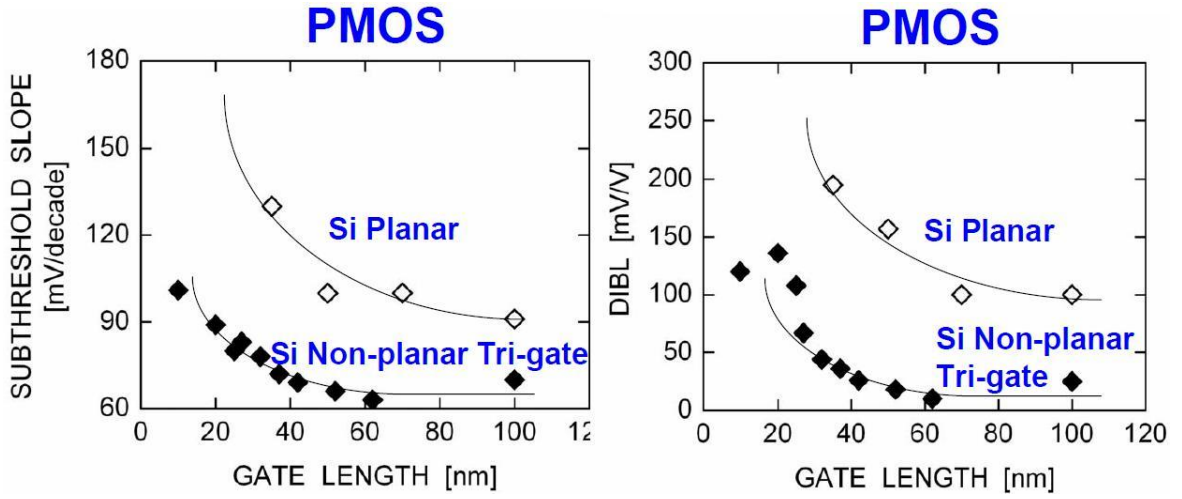


Fig. 2.8 SS and DIBL vs LG for planar and tri-gate PMOSFETs [21]

The strain implementation techniques for MuGFETs are the same as those for the planar case. The performance enhancements provided by the embedded S/D and contact etch stop layer techniques have also been investigated for Si channel MuGFETs [20, 24]. Fig. 2.9 illustrates the embedded S/D technique being implemented for Si MuGFETs as shown below.

The undercut etch reduces the S/D resistance by 40% improving the drain saturation current significantly by about 40% [20]. Fig. 2.10 plots the I_d - V_d curves for the MuGFETs in Fig. 2.9.

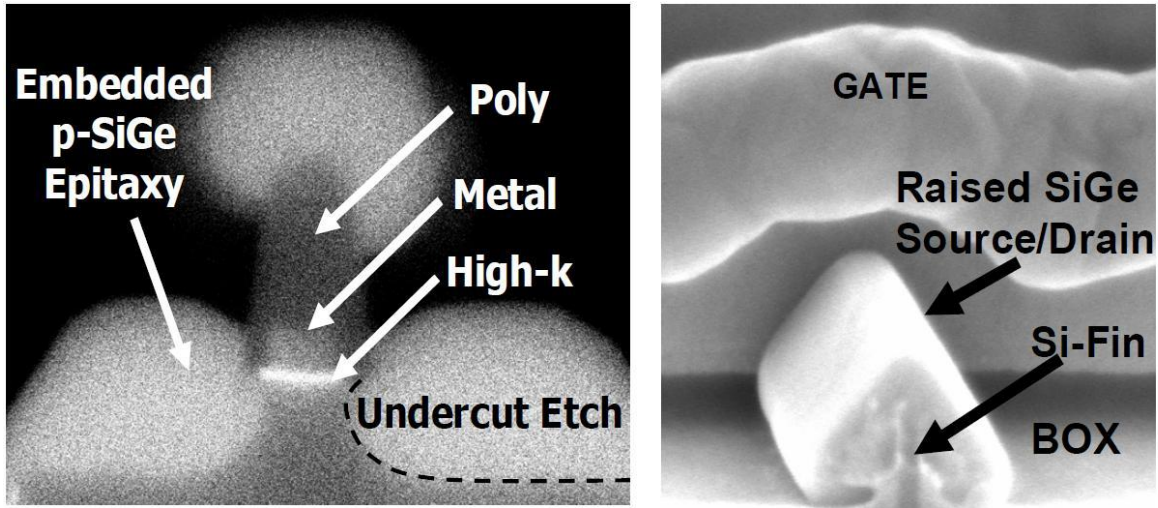


Fig. 2.9 X direction cross section for P-Trigate with SiGe raised S/D [20]

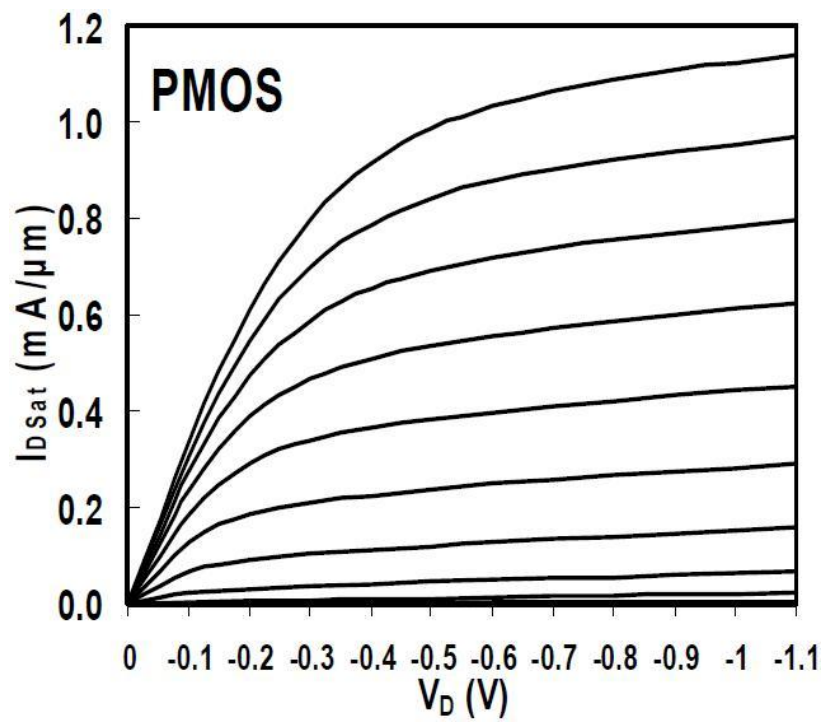


Fig. 2.10 Id-Vd curves for PMOS tri-gate shown in Fig. 2.12 [20]

The MuGFETs can also be nested together making the S/D contact formation much easier than that for a single MuGFET as shown in Fig. 2.11. The nested MuGFET S/D contacts feature significantly smaller contact resistance than for a single device. Contact resistance is a critical issue for MuGFET devices [22] due to the narrow width of the fins necessitating the implementation of nested architecture.

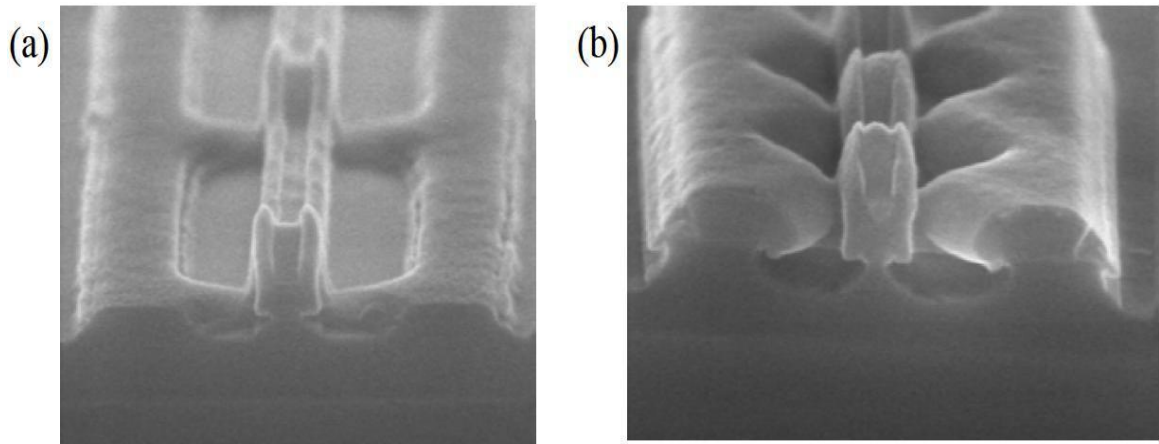


Fig. 2.11 Cross section SEM pictures (a) after recess etch and (b) after Ni silicidation

[23]

The performance enhancement of the MuGFETs shown in the figure above over a reference unstrained Si device at same I_{ON}/I_{OFF} ratios is plotted in Fig. 2.12 as shown below.

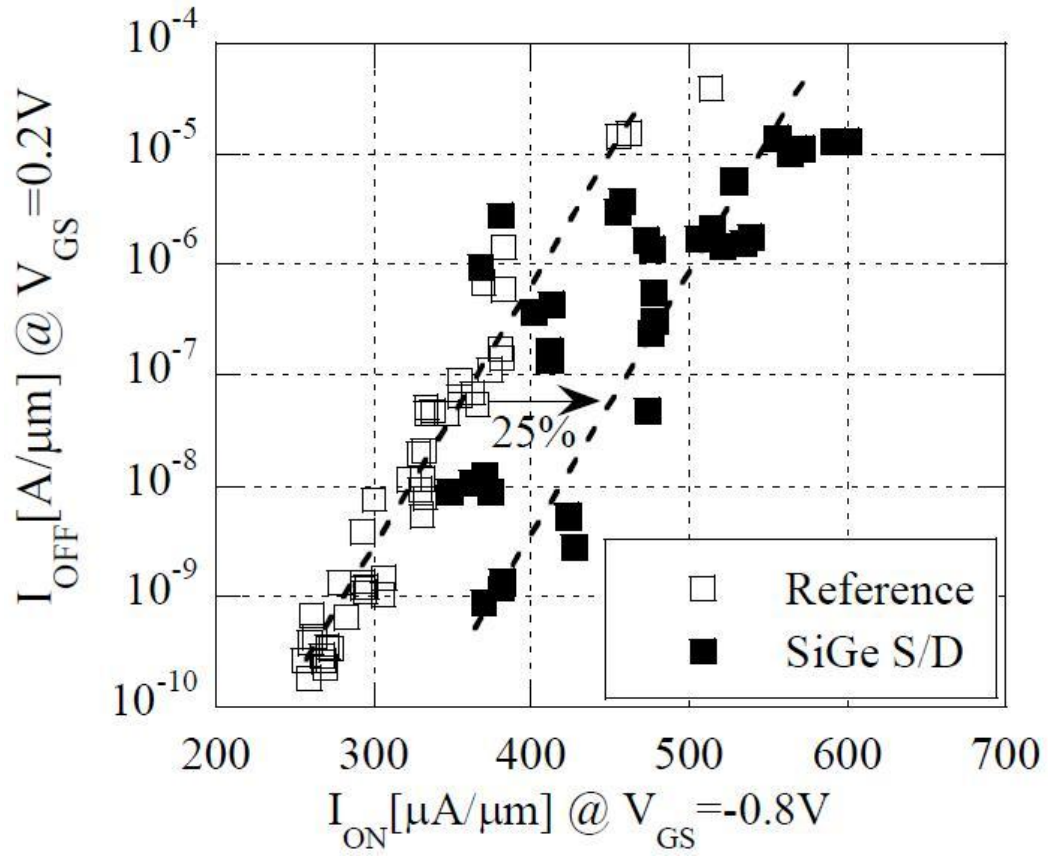


Fig. 2.12 Ion/Ioff plot of the reference devices versus the SiGe S/D device [23]

The mobility enhancement in strained Si FinFETs has also been studied using the wafer bending and stress liner techniques [24]. Fig. 2.13 illustrates the above mentioned techniques being implemented for straining Si MuGFETs and the drive current enhancement corresponding to the channel stress is plotted in Fig. 2.14

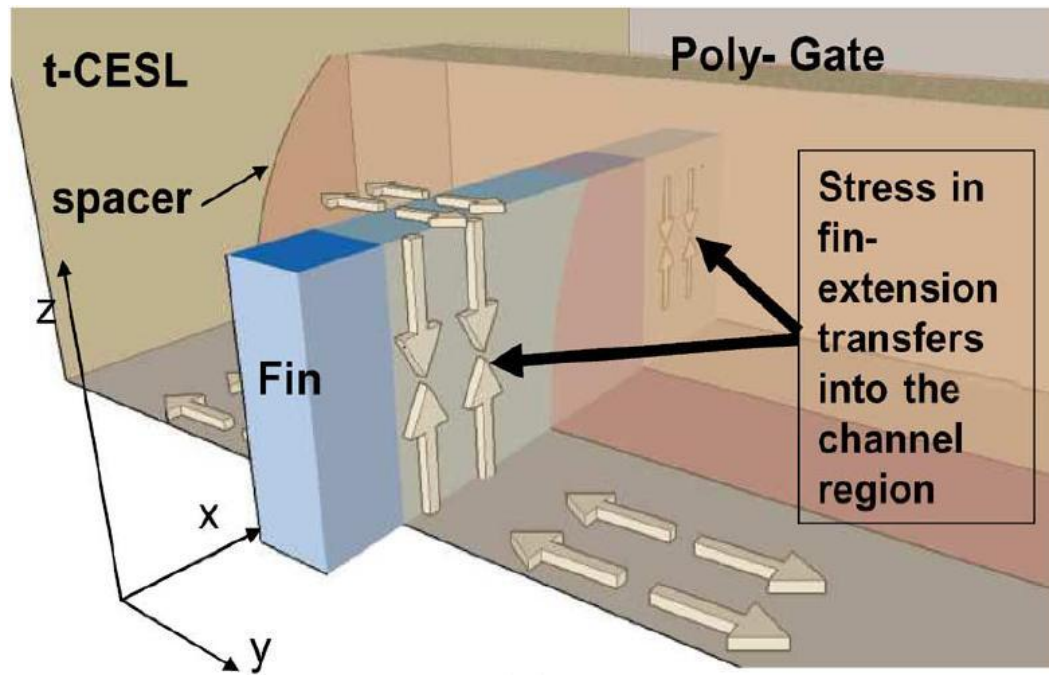


Fig. 2.13 Schematic diagram of a FinFET with a CESL along the fin extension [24]

Globally induced uniaxial strain is perhaps the most popular technique for strained MuGFETs [25-27]. Uniaxial strain is achieved by patterning bi-axially strained epitaxial layers as shown in Fig. 2.15. The added advantage of this technique is that materials with inherently higher mobilities (SiGe) can be directly grown on Si and patterned to achieve uniaxial strain resulting in even higher mobilities [25].

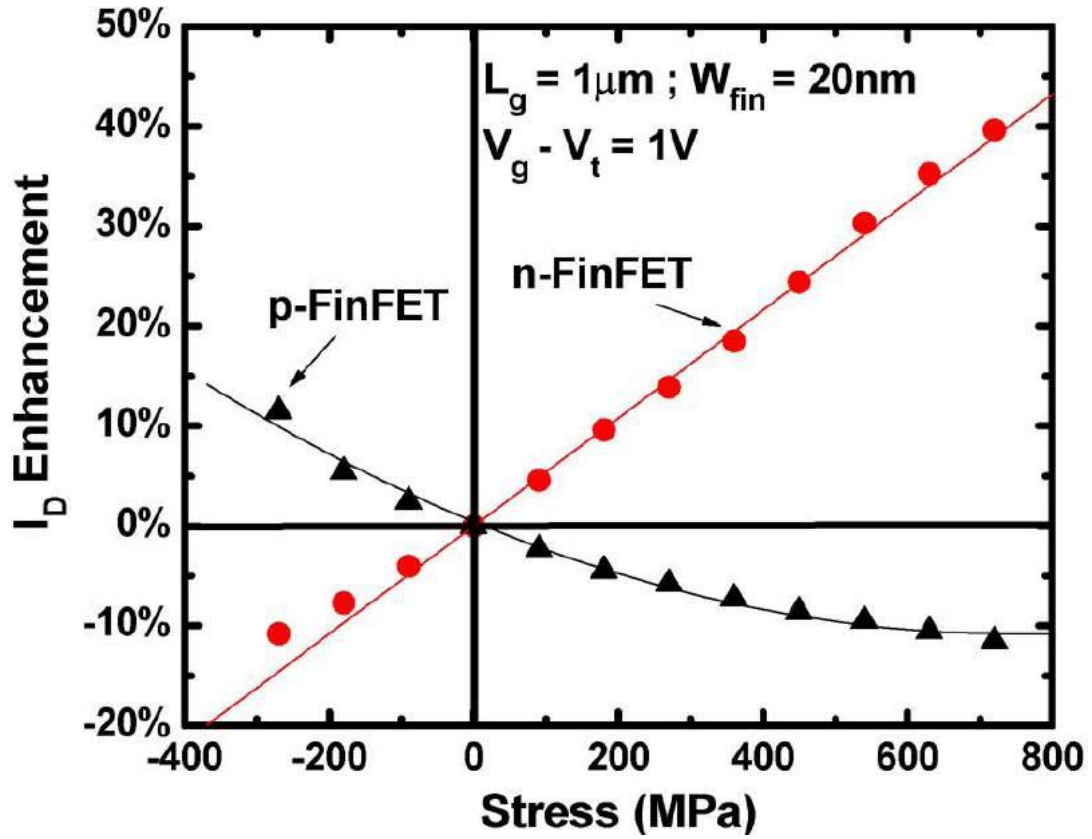


Fig. 2.14 Drain current enhancement with respect to the applied stress [24]

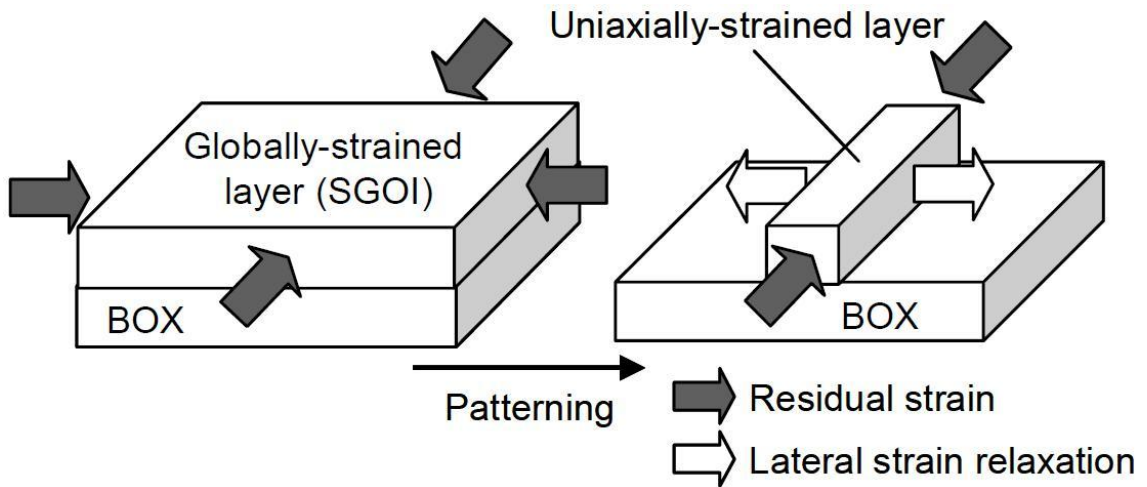


Fig. 2.15 Globally induced uniaxial strain via patterning [25]

Significant drain saturation current levels have been obtained using the globally induced uniaxial strain technique as shown in Fig. 2.16

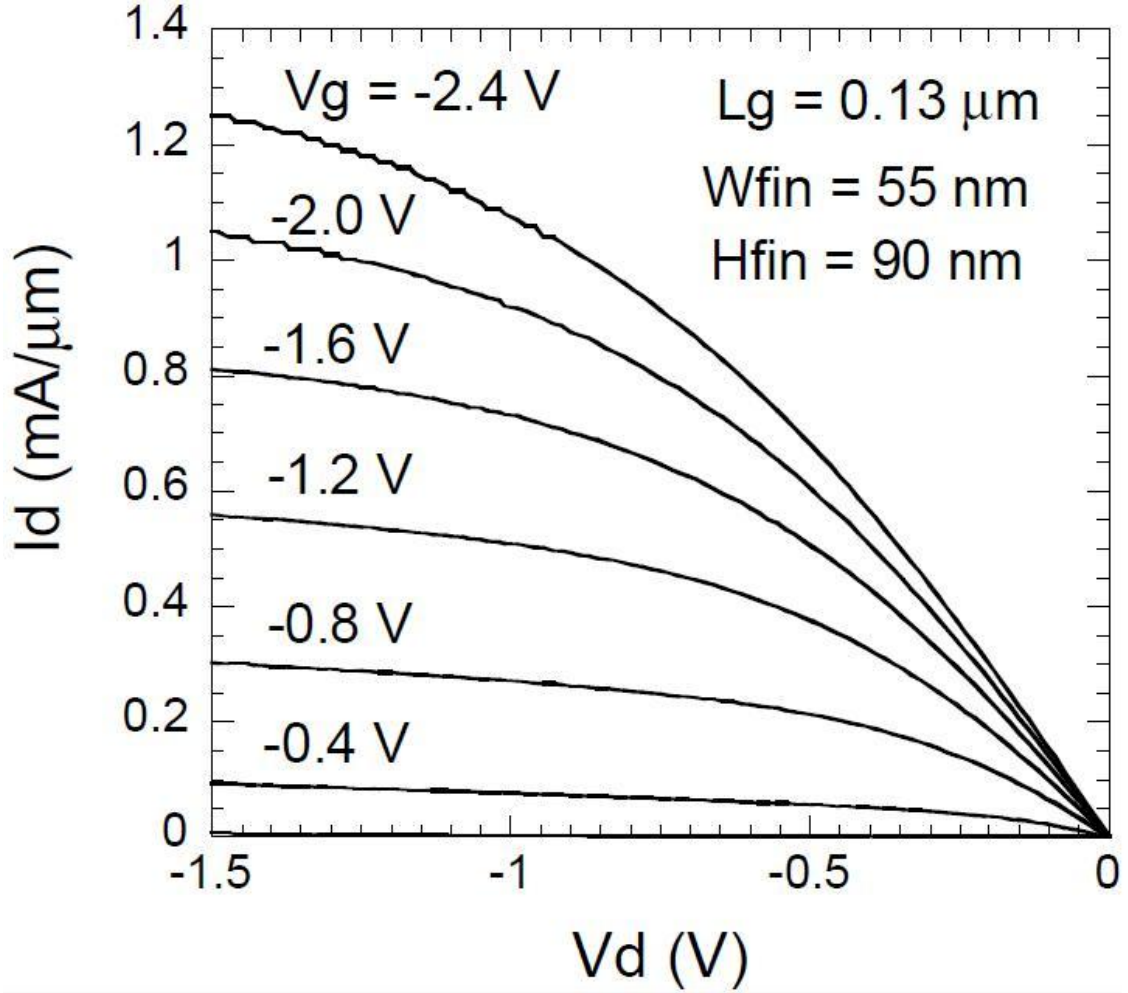


Fig. 2.16 I_d - V_d characteristics of a SGOI FinFET [25]

A $\text{Si}_{0.75}\text{Ge}_{0.25}/\text{Si}$ on insulator stack as shown in Fig. 2.17 has also been investigated [26] showing improved p-channel FET performance as shown in Fig. 2.18 below. The SiGe channel will be uniaxially strained due to patterning of the biaxially strained SiGe as mentioned before.

The channel stress will be quite high (~ 1.4 Gpa) due to the significant lattice mismatch ($\sim 1\%$) between the $\text{Si}_{0.75}\text{Ge}_{0.25}$ layer and the underlying Si. As the channel is (110)/<110> the performance improvement is not as significant as that for the (100)/<110> channel even for a significant amount of stress. The important thing to note is that the p-channel performance is closely matching the n-channel's performance which is critical for complementary technology.

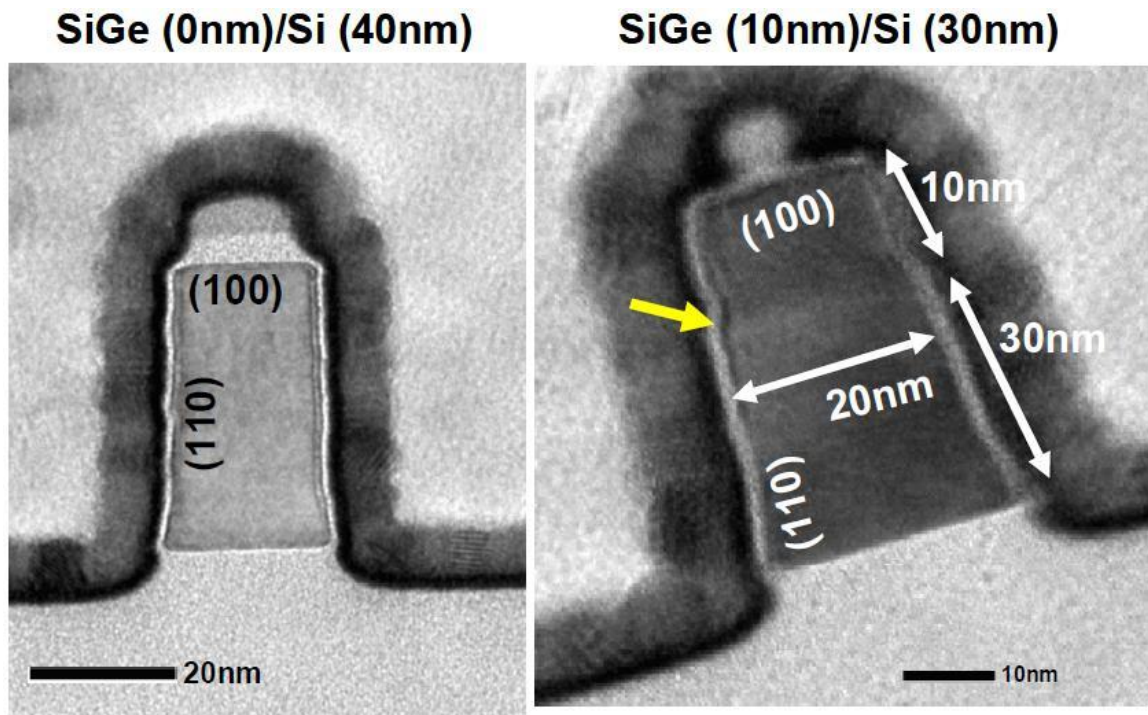


Fig. 2.17 (a) $\text{Si}_{0.75}\text{Ge}_{0.25}/\text{Si}$ stack with varying $\text{Si}_{0.75}\text{Ge}_{0.25}$ thicknesses [26]

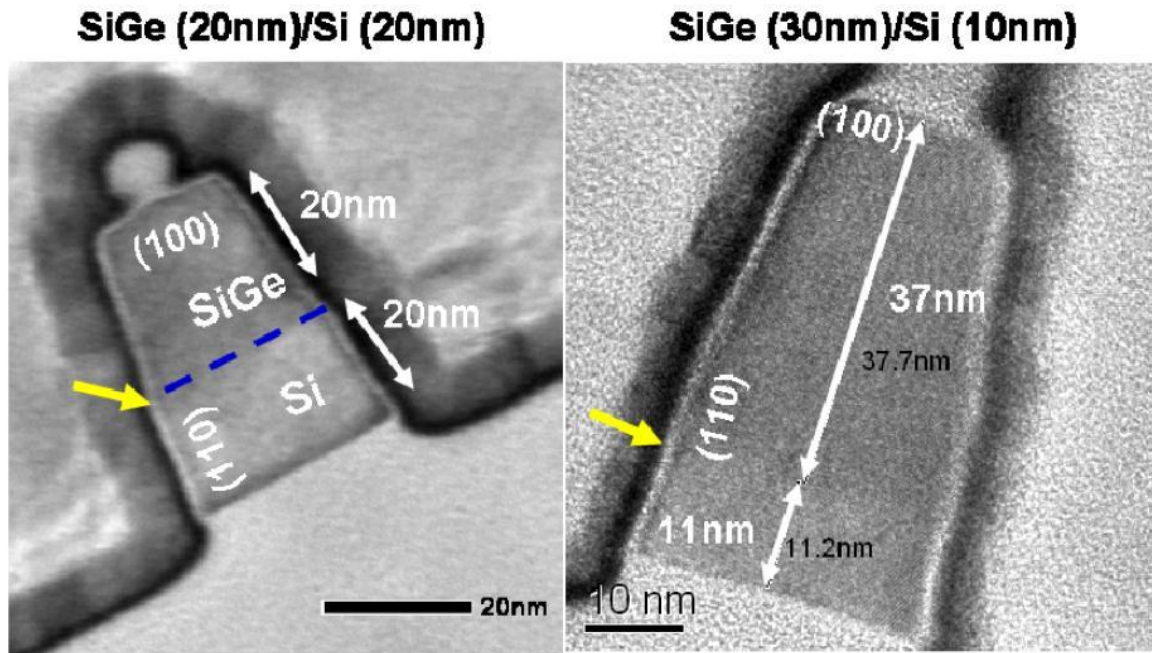


Fig. 2.17 (b) $\text{Si}_{0.75}\text{Ge}_{0.25}/\text{Si}$ stack with varying $\text{Si}_{0.75}\text{Ge}_{0.25}$ thicknesses [26]

It is evident that using a higher Ge content SiGe/Si stack, the p-channel will have exactly the same performance and might even be better than the n-channel. The critical thickness of the top SiGe layer will however be a concern as seen before due to the increasing lattice mismatch of higher Ge content SiGe layers with the underlying Si. There will be a trade-off between the desired enhancement and maximum possible critical of the SiGe/Si stack.

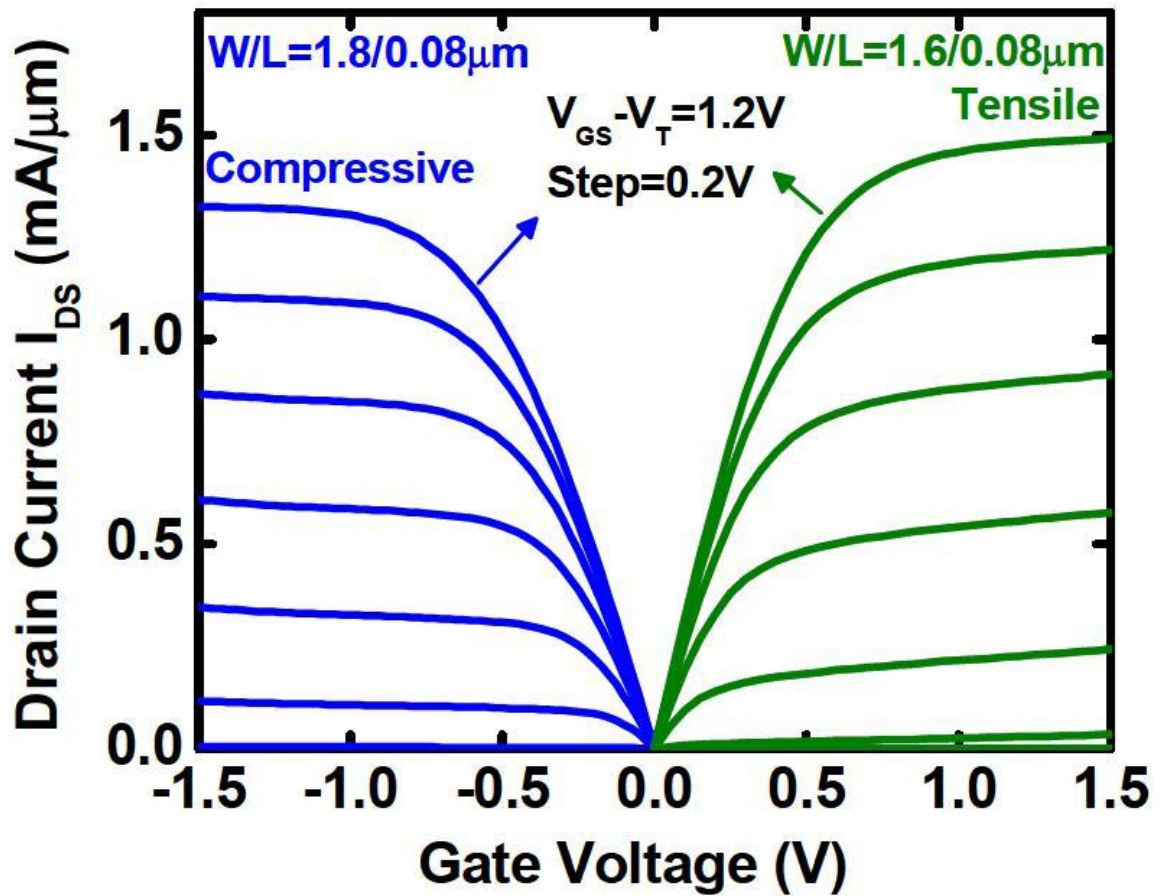


Fig. 2.18 I_D - V_d for p and n-channel FinFETs [26]

2.5 Conclusion

Channel strain engineering has been one of the key techniques responsible for continuous performance enhancement of the state of the art technology nodes allowing us to continue Moore's law well beyond the sub 90nm technology node. Strain alters the material band structure lowering the carrier effective mass consequently increasing the mobility ultimately translating to significantly improved device performance.

Uni-axial strain is more beneficial than bi-axial strain in terms of device performance with its added advantage of it being relatively easier to implement compared to bi-axial strain.

Although techniques like strain, halo implantation, high-k/metal gate have enabled us to scale the MOSFET till the 32nm technology node with acceptable short channel effects it has become obvious that drastic device structure/material changes are needed for future scaling. The Fin/Tri-gate structure addresses the short channel effects by increasing the gate electrostatic control over the channel.

Uni-axially strained Tri-gate/Fin FET is thus a topic of great interest and significant amount of research has already been done to investigate its viability in future technology nodes. The straining techniques are the same for the Tri-gate/Fin FET structures as those for the planar.

Alternate channel materials such as SiGe featuring higher hole mobilities than Si have been investigated for strained p-channel Tri-gate/Fin FETs. Uni-axially strained SiGe Tri-gate/Fin FETs are primarily obtained via patterning bi-axially strained epitaxial layers. Impressive performance enhancements over Si Tri-gate/Fin FETs have been demonstrated with strained SiGe as the channel material ensuring it's viability in replacing Si for future technology nodes.

3. OPTIMIZATION OF DEVICE LAYOUT AND EMBEDDED SOURCE/DRAIN SHAPE PROFILES FOR 22NM NODE STRAINED P-CHANNEL TRI-GATE FIELD EFFECT TRANSISTORS

3.1 Introduction

Tri-gate/Fin FETs are considered to be the lead contenders for replacing planar CMOS for future technology nodes as seen before. Alternate channel materials featuring higher mobility than Si are being investigated thoroughly to enable future scaling of the CMOS technology beyond the 22nm technology node. SiGe and Ge are gaining interest for replacing Si as channel material for future p-channel FETs as seen before. Strain engineered Si/SiGe/Ge P-channel tri-gate FETs is thus a topic of great current interest. Although globally induced uniaxial strain is a key technique for implementing strained P-channel tri-gate FETs, [28, 29] indicate that ion implantation induced S/D amorphization can relax the channel strain almost completely for extremely scaled gate lengths as illustrated in Fig. 3.1 below.

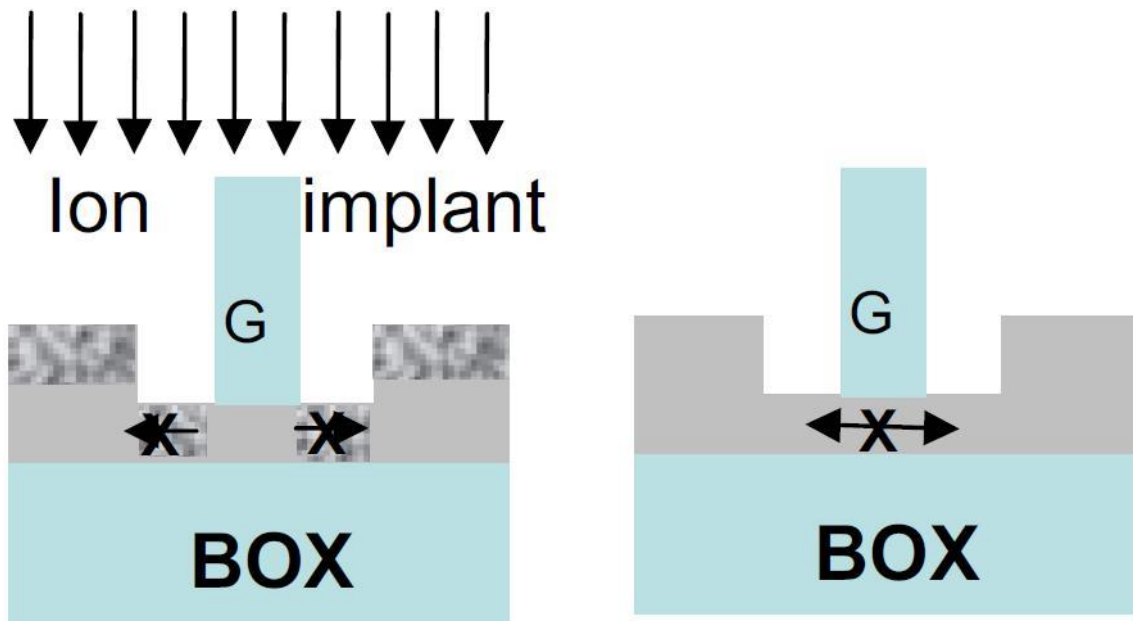


Fig. 3.1 uniaxial strain relaxation on ultra-thin SSDOI substrates with raised source/drain following shallow ion-implant amorphization, ϵ solid phase epitaxy anneal [28]

Embedded S/D induced strain in the channel which has been quite successful as a uniaxial stressor source in the planar MOS technology will thus be an attractive candidate for extremely scaled device dimensions. However, high level of channel strain using eS/D technique is difficult to implement in tri-gate FETs due to the absence of the shallow trench isolation. A nested device layout has to be adopted to minimize or eliminate source-drain relaxation and thus maximize the channel strain.

Thus, the average uniaxial strain retention for top plane and sidewall in P-channel tri-gate FETs will depend on the following factors: (a) Average distance between source and drain ($L_{S/D}$) (b) S/D Ge content (c) Number of gates (d) Number of fins (e) Shape of S/D regions (f) S/D etch depth (g) Channel Ge content (h) Residual strain due to patterning biaxial strained epitaxial layers retained after S/D recess etch and (i) Gate pitch. In this thesis a systematic study of the contribution of all the above factors to the average channel stress except the effect of gate pitch which is kept constant for all cases is done. Average stress values and mobility enhancements for (100) and (110) planes are calculated separately keeping in mind the anisotropic behavior of these quantities thus giving a more realistic estimate of achievable enhancements.

3.2 Simulation Methodology

FEM simulations are performed using COMSOL-Multiphysics. For benchmarking the FEM simulations, device structures with dimensions, substrate/channel and S/D compositions identical to those in [30-32] were simulated and the extracted stress values were compared with the corresponding measurements. A linear elastic model with orthotropic channel behavior was implemented in order to realistically estimate achievable levels of channel stress values. Elastic moduli, shear moduli and Poisson's ratios of Silicon and Germanium for (100)/<110> and (110)/<110> were obtained from [33] and the elastic moduli, shear moduli and Poisson's ratios for $\text{Si}_{1-x}\text{Ge}_x$ alloys were obtained by a linear interpolation between those for Silicon and Germanium. The lattice constant for $\text{Si}_{1-x}\text{Ge}_x$ was calculated from Vegard's law. Lattice mismatch of embedded S/D (eS/D) was incorporated as the thermal expansion coefficient of the S/D regions. No other stressor sources except the eS/D regions were assumed. The channel stress values extracted from the simulations show good agreement between simulated and experimental values as can be seen from Fig. 3.2 thus validating the choice of the elastic model and values of elastic moduli/Poisson's ratios used as well as the assumption of the S/D regions being the only stressor sources.

Table 3.1 Critical dimensions for 22nm, 14nm and 10nm nodes

Node	22 nm	14 nm	10 nm	
Fin Pitch = Gate Pitch [nm]	48	34	24	0.7X
L_G [nm]	25	21	17	0.85X
L_{eff} [nm]	13	10	9	$2X_{UD} = 12/11$ nm
W_{eff} [nm]	26	20	18	$L_{eff}/W_{eff} = 0.5$
W_{Si} [nm]	20	14	12	$T_{Ox} = 1$ nm
H_{Si} [nm]	40	28	24	$H_{Si}/W_{Si} = 2$

Table 3.1 gives the critical device dimensions for the 22nm, 14nm and 10nm nodes where

$$L_{eff} = L_G - 2X_{UD} \text{ where } X_{UD} \text{ is the S/D extension and}$$

$$W_{Si} = W_{eff} - 2(\epsilon_{Si}/\epsilon_{Ox})*T_{Ox} \text{ where } (\epsilon_{Si} \text{ is the dielectric constant for}$$

silicon, ϵ_{Ox} is the dielectric constant for SiO_2 and T_{Ox} is the equivalent oxide thickness). Figs. 3.3 and 3.4 illustrate the simulated structures for investigating the layout dependence of the average channel stress levels and corresponding mobility enhancements.

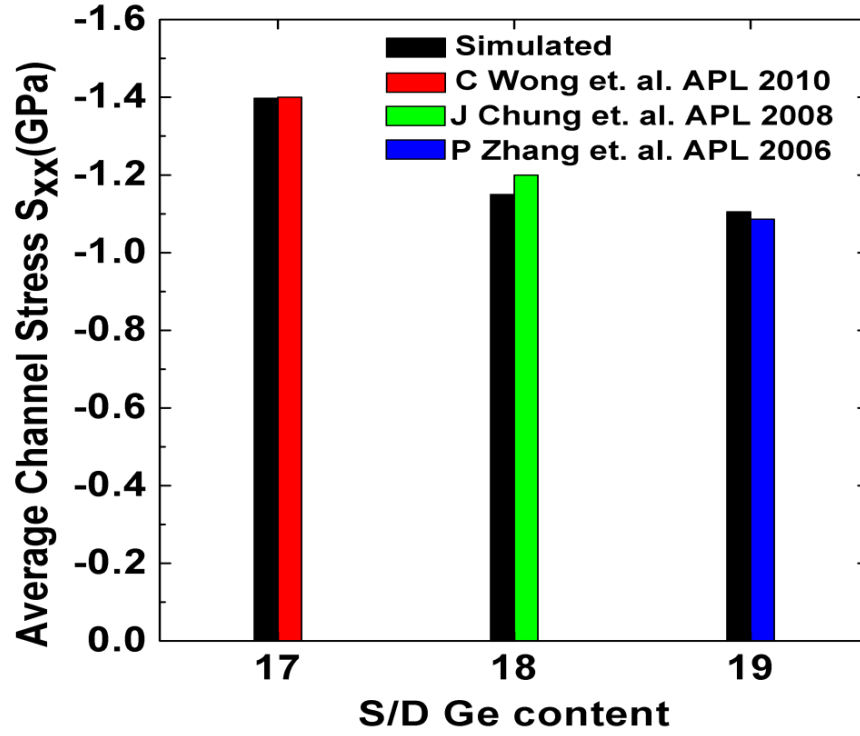


Fig. 3.2 FEM simulations benchmarked for sub 50nm compressively strained planar PMOSFETs

A relaxed Silicon substrate with isotropic behavior is assumed for P-channel Silicon tri-gate FETs whereas a relaxed $\text{Si}_{0.4}\text{Ge}_{0.6}$ virtual substrate with orthotropic behavior is assumed for $\text{Si}_{0.4}\text{Ge}_{0.6}$ channels. The top surface is the (100) plane with the sidewall being the (110) plane for all the device structures investigated. The channel direction is $\langle 110 \rangle$ for all cases. Average stress and corresponding mobility enhancements for top surface (100) and sidewalls (110) are extracted only for the central channel (red). An inversion layer thickness (t_{inv}) of 2nm for both (100) and (110) planes is assumed for calculation of average channel stress for all the structures simulated.

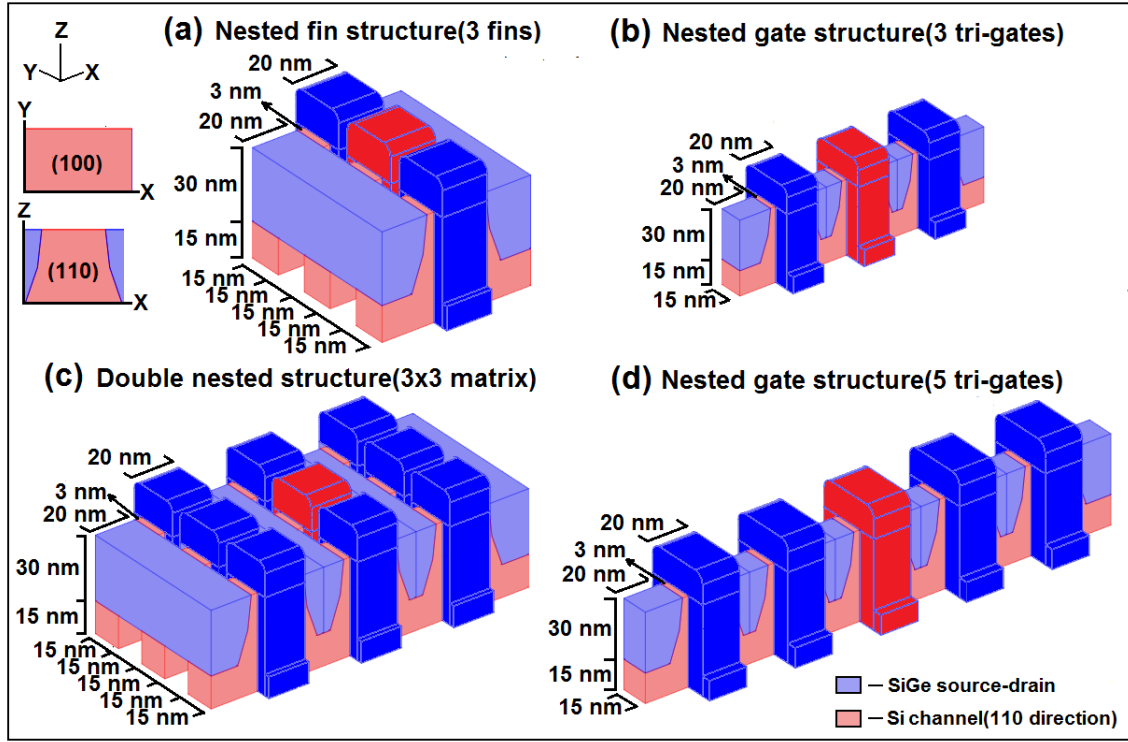


Fig. 3.3 Schematics of simulation structures for evaluating the contribution of $L_{S/D}$, S/D Ge content, Number of nested gates, Number of nested fins and S/D etch depth to the average channel stress

The surfaces are assumed to be traction free for all cases. A non-uniform mesh with fine meshing near hetero-interfaces/small regions and relatively coarser meshing farther away from hetero-interfaces/small regions is chosen so as to accurately estimate strain levels in regions with rapidly changing strain levels as well as to reduce the overall mesh points. For evaluating the contribution of (b) S/D Ge content, (c) number of gates and (d) number of fins to the average channel stress, device structures in Fig. 3.3 are simulated with three different S/D Ge contents (25%, 30% and 40%).

Device structures in Fig. 3.4 are studied to evaluate the effect of ϵ S/D shape and (g) channel Ge content on the average channel stress with $\text{Si}_{0.6}\text{Ge}_{0.4}/\text{Ge}$ S/D regions for $\text{Si}/\text{Si}_{0.4}\text{Ge}_{0.6}$ channel tri-gate FETs respectively.

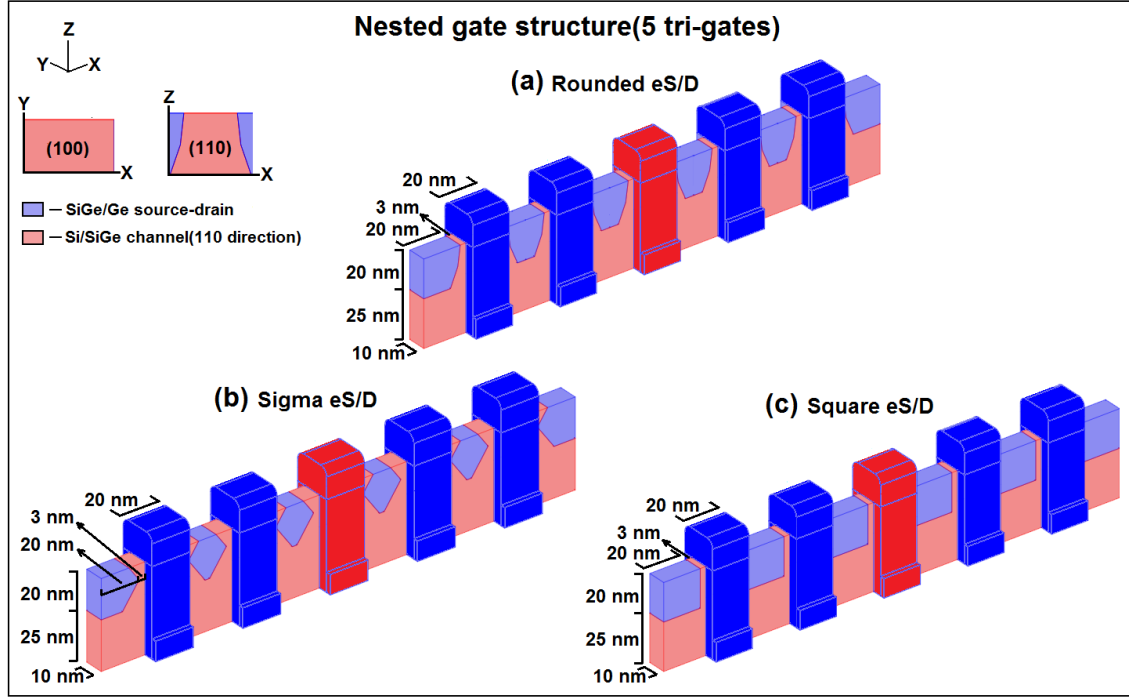


Figure 3.4 Schematics of simulation structures for evaluating the contribution of S/D shape and channel Ge content to the average channel stress keeping the same lattice mismatch between channel and S/D regions.

The contribution of etch depth is studied for the sidewalls of the nested gates (5 tri-gates) structure due to the sidewall dominated transport in tri-gate FETs. The S/D etch depth was reduced from 30nm to 20nm with the other dimensions as well as the channel/S/D compositions remaining the same.

The average stress values extracted from simulated structures in Figs. 2 and 3 are compared with the channel stress in [14] to get an estimate of the degradation of channel stress in tri-gate FETs compared to planar devices.

Currently strained P-channel tri-gate FETs are primarily fabricated by patterning biaxially strained epitaxial layers as seen before. The maximum channel stress achieved through a combination of residual stress and eS/D technique is thus of significant interest. The evolution of the channel stress following the S/D recess etch and eS/D(1.7% lattice mismatch with channel) re-growth for uni-axially strained $\text{Si}_{1-x}\text{Ge}_x$ epi-layers is investigated with three different channel Ge contents for the nested gate (5 tri-gates) structure with rounded eS/D regions in Fig. 3.3(d). The substrate is assumed to be a Silicon substrate with isotropic behavior.

The mobility enhancements of strained Si channels over unstrained Si channels are obtained from [5] shown in Fig. 3.5. The mobility enhancements for strained $\text{Si}_{1-x}\text{Ge}_x$ (110)/<110> channels over unstrained $\text{Si}_{1-x}\text{Ge}_x$ (110)/<110> channels are obtained by a linear interpolation between the enhancements for Si (110)/<110> channels [5] and Ge (110)/<110> channels [34].

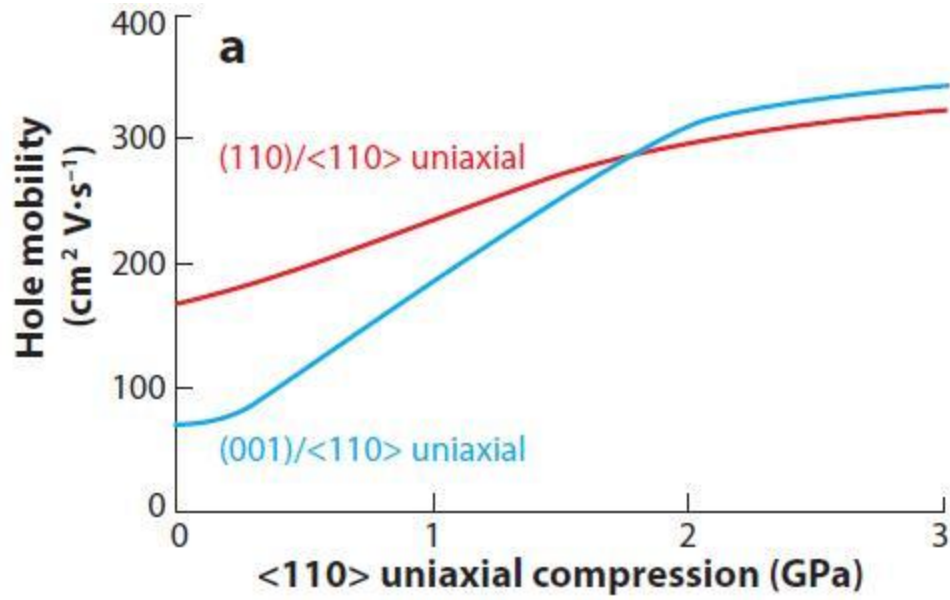


Fig. 3.5 Hole mobility as a function of <110> uniaxial compression for Silicon [5]

The mobility enhancement for strained Ge corresponding to the channel stress from [34] is shown in Fig. 3.6. The enhancements for (100)/<110> channels are taken from [5] as shown in Fig. 3.7.

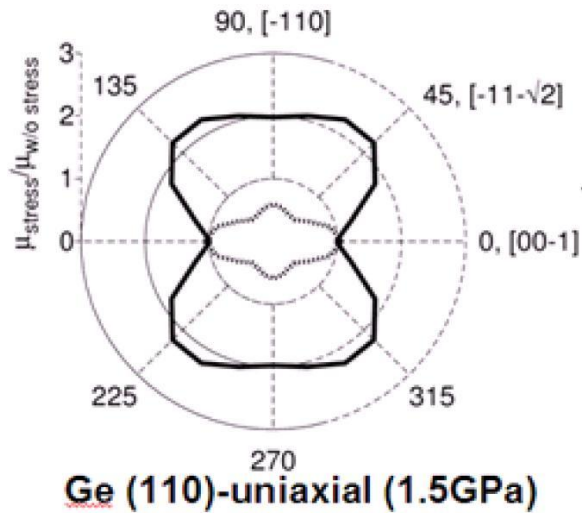


Fig. 3.6 Mobility enhancement for (110)/<110> Ge channel [34]

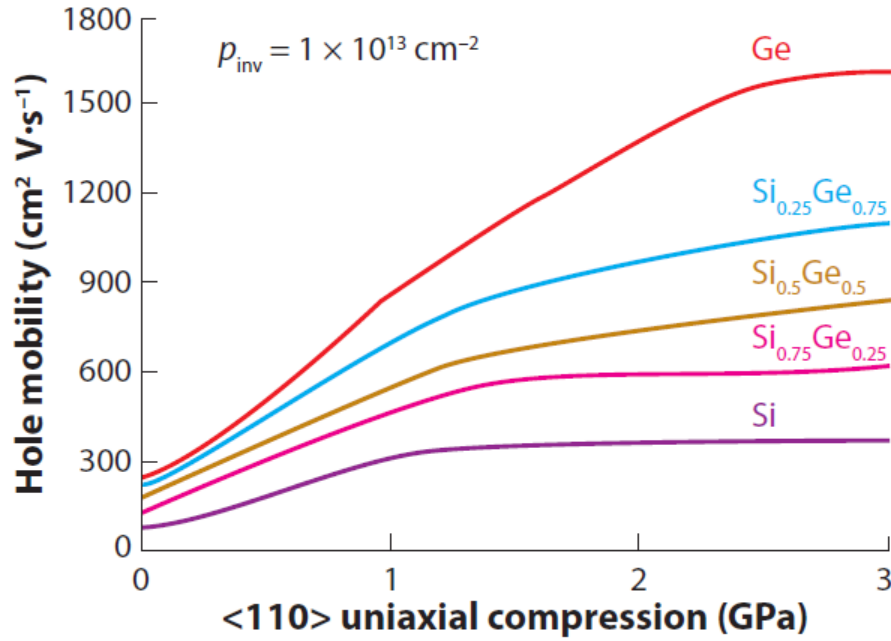


Fig. 3.7 Ge, Si, and $\text{Si}_{1-x}\text{Ge}_x$ hole mobility enhancement of a (100)-oriented device under $\langle 110 \rangle$ uniaxial compressive stress [5]

3.3 Results and Discussion

Figs. 3.8 (a, c) show the extracted average stress values for the (100)/ $\langle 110 \rangle$ and (110)/ $\langle 110 \rangle$ channels of device structures in Fig. 3.3 for three different Ge contents in the eS/D regions. Also plotted is the channel stress for the planar case with 30% eS/D Ge content [14] for comparison. The absence of STI causes significant reduction in the channel stress of the simulated structures compared to the planar case.

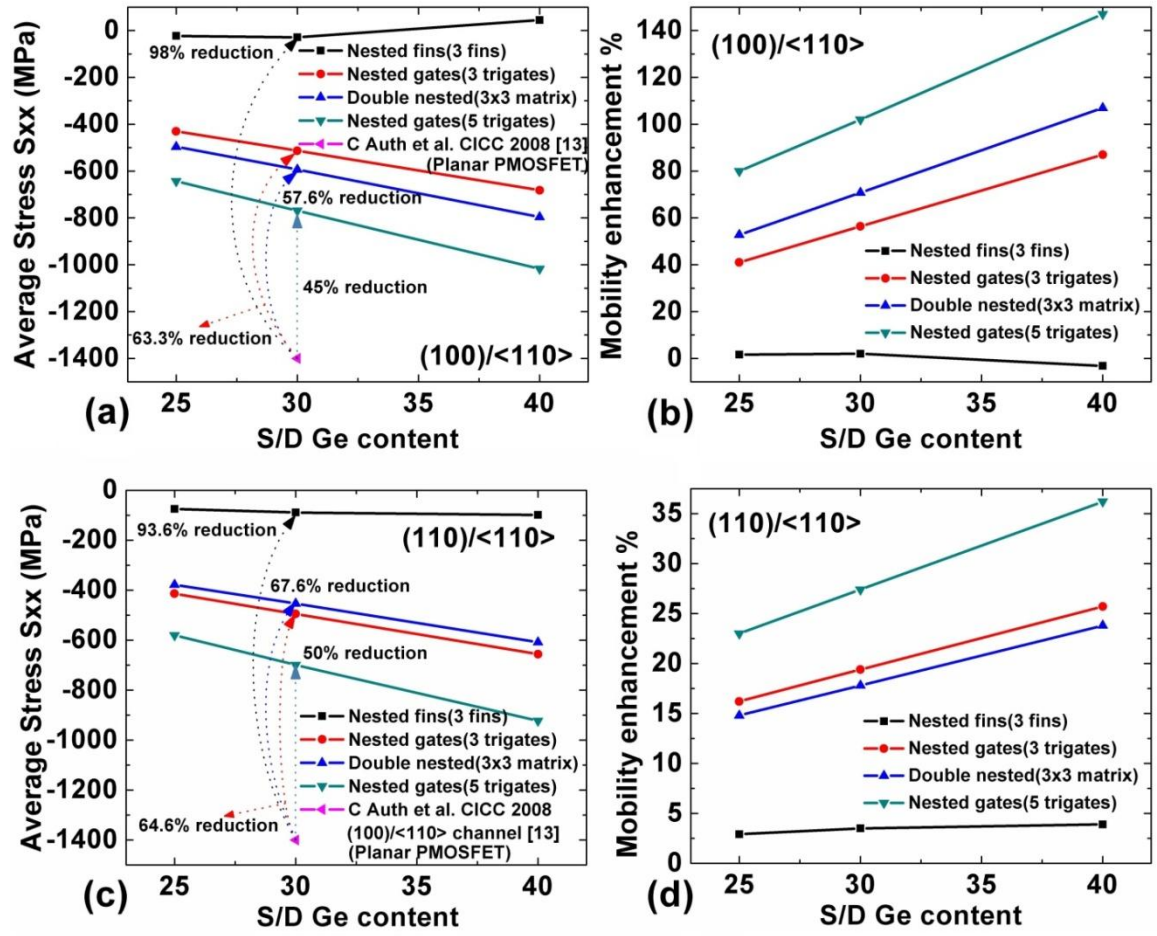


Fig. 3.8 Average channel stress and the corresponding mobility enhancements of the (100)/<110> and (110)/<110> channels plots for structures in Figs. 3.3(a-d)

The Nested fins (3 fins structure) shows a reduction of 98% in the average channel stress for the (100)/<110> channel orientation and a 93% reduction for the (110)/<110> channel orientation indicating almost complete relaxation of the S/D regions through their free surfaces without inducing strain in the channel.

It is thus apparent that merging the S/D regions and thus eliminating their free sidewalls for nested fins is not improving the channel stress. The relaxation of the free side domain walls (planes normal to the y direction) of the S/D regions needs to be minimized for significant improvement in the channel stress which is achieved by the nested gate and double nested structures. The nested gate (3 tri-gates) structure shows a 63.3% reduction in the average channel stress for the (100)/<110> channel orientation and a 64.6% reduction for the (110)/<110> channel orientation. The elimination of the free side domain walls of the active device's S/D regions is responsible for improving the channel significantly compared to the nested fins case. The double nested structure attempts to further improve the channel stress by eliminating one more set of free surfaces (sidewalls) by merging the S/D regions. The (100)/<110> channel stress shows the expected improvement over the nested gate (3 tri-gates) structure showing 57.6% reduction in the average channel stress. The (110)/<110> channel stress however shows a reverse trend and is actually smaller than that for the (110)/<110> channel of nested gate (3 tri-gates) structure. The free S/D region sidewalls which are eliminated in the double nested structure due to merging of S/D regions are responsible for introducing greater strain in the (110)/<110> channel for the nested gate structures as illustrated in Fig. 3.9. Hence the nested gate structure is preferable over the double nested structure for strained P-channel tri-gate FETs due to their sidewall dominated current conduction.

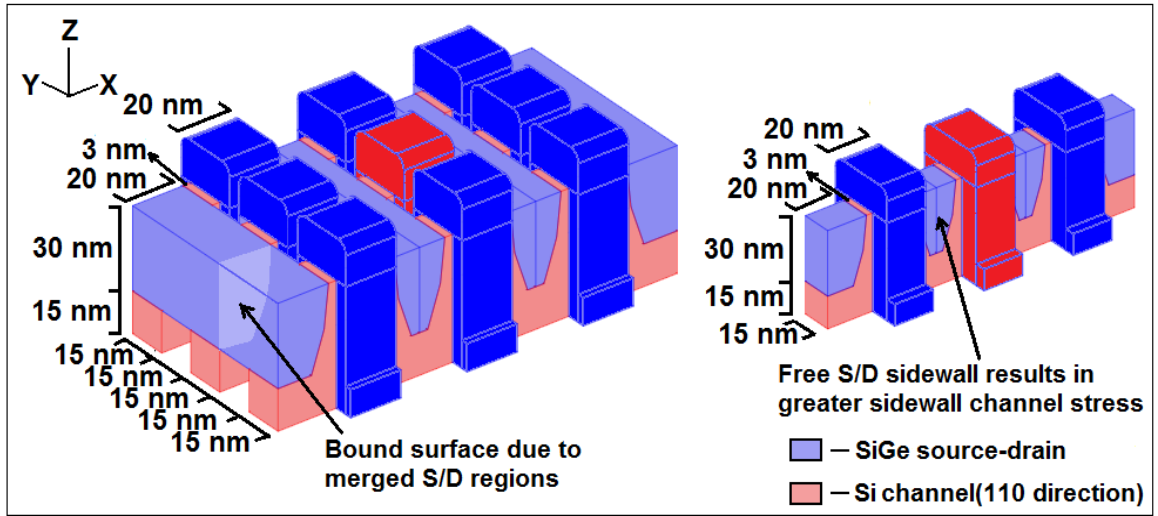


Fig. 3.9 Illustration showing dependence of sidewall channel stress on the nature of the S/D sidewalls

The significant reduction in its average channel stress of the nested gate (3 tri-gates) structure compared to the planar case [14] indicates that the free side domain walls of the extreme S/D regions are still playing a significant role in degrading the channel stress. The nested gate (5 tri-gates) shows the improvement in channel stress due to increasing the distance between the active channel and the free side domain walls of the extreme S/D regions further. The nested gate (5 tri-gates) shows a 45% reduction in the (100)/<110> channel stress and a 50% reduction in the (110)/<110> channel stress which is quite significant compared to the other structures. It is thus apparent that the average channel stress can be improved by increasing the number of nested gates until the channel stress is limited by other factors such as S/D Ge content, $L_{S/D}$ etc.

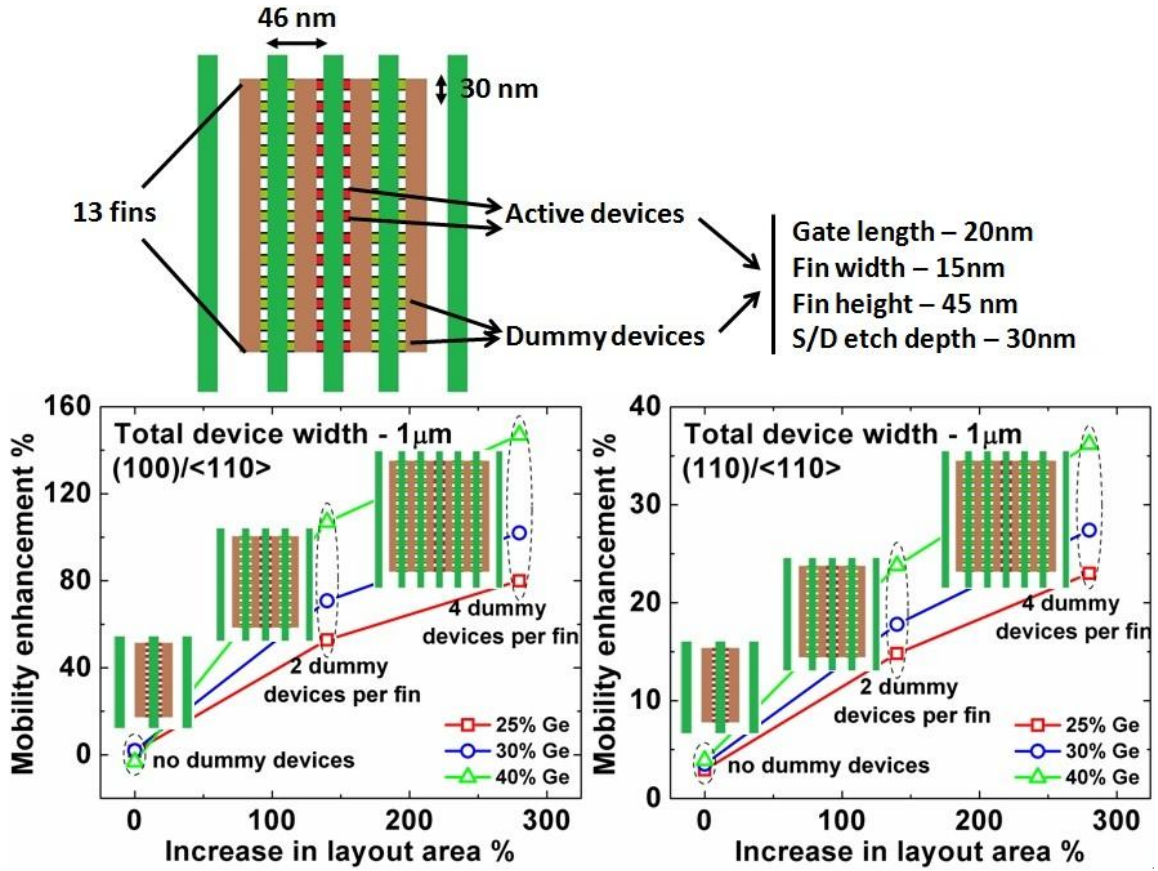


Fig. 3.10 Performance vs device density trade-off (22nm node)

Fig. 3.8(a, c) gives the improvement in the average channel stress with increasing S/D Ge content. The average stress for the (100)/<110> and (110)/<110> channels shows an enhancement of $\sim 1.6x$ on increasing the S/D Ge content from 25% to 40% for all structures except the nested fins structure. Average stress of the (100)/<110> channel for the nested fins structure goes to tensile from compressive while the (110)/<110> channel shows an enhancement of $\sim 1.3x$ when the S/D Ge content is increased from 25% to 40%.

The proximity of free side domain walls to the active channel in the nested fins structure is responsible for the significant channel stress degradation compared to the other structures for the same S/D Ge contents. The average (110)/<110> channel stress for the 20nm S/D etch depth nested gates (5 tri-gates) structure (15nm wide fin) is ~0.96x of the (110)/<110> channel stress for the 30nm S/D etch depth nested gates (5 tri-gates) structure.

The S/D etch depth is an important parameter for tri-gate FETs as it determines the total effective width of the device. The improvement in the channel stress due to increase in the S/D etch depth serves as an important addition to the increase in the current of the unstrained device. The corresponding mobility enhancements taken from [5] are plotted in Figs. 3.8(b, d). Fig. 3.10 illustrates the performance enhancement vs device density trade-off. We observe near zero mobility enhancement in the absence of dummy devices due to S/D relaxation via the free surfaces as seen earlier. Although significant mobility enhancement is obtained after implementing a layout with 4 dummy devices per fin, the increase in the layout area compared to the no dummy device case is unacceptable. Hence an optimum trade-off with respect to performance enhancement and active device density has to be estimated. The layout with 2 dummy devices per fin with 40% S/D Ge content seems to be the optimal solution offering impressive mobility enhancement with an acceptable reduction in active device density

Fig. 3.11 gives the average channel stress values and the corresponding mobility enhancements for the structures in Fig. 3.4. The average stress of the (100)/<110> and (110)/<110> Si channels of the sigma S/D nested gate (5 tri-gates) structure show a 52.4% and 56.2% reduction in channel stress from the planar case.

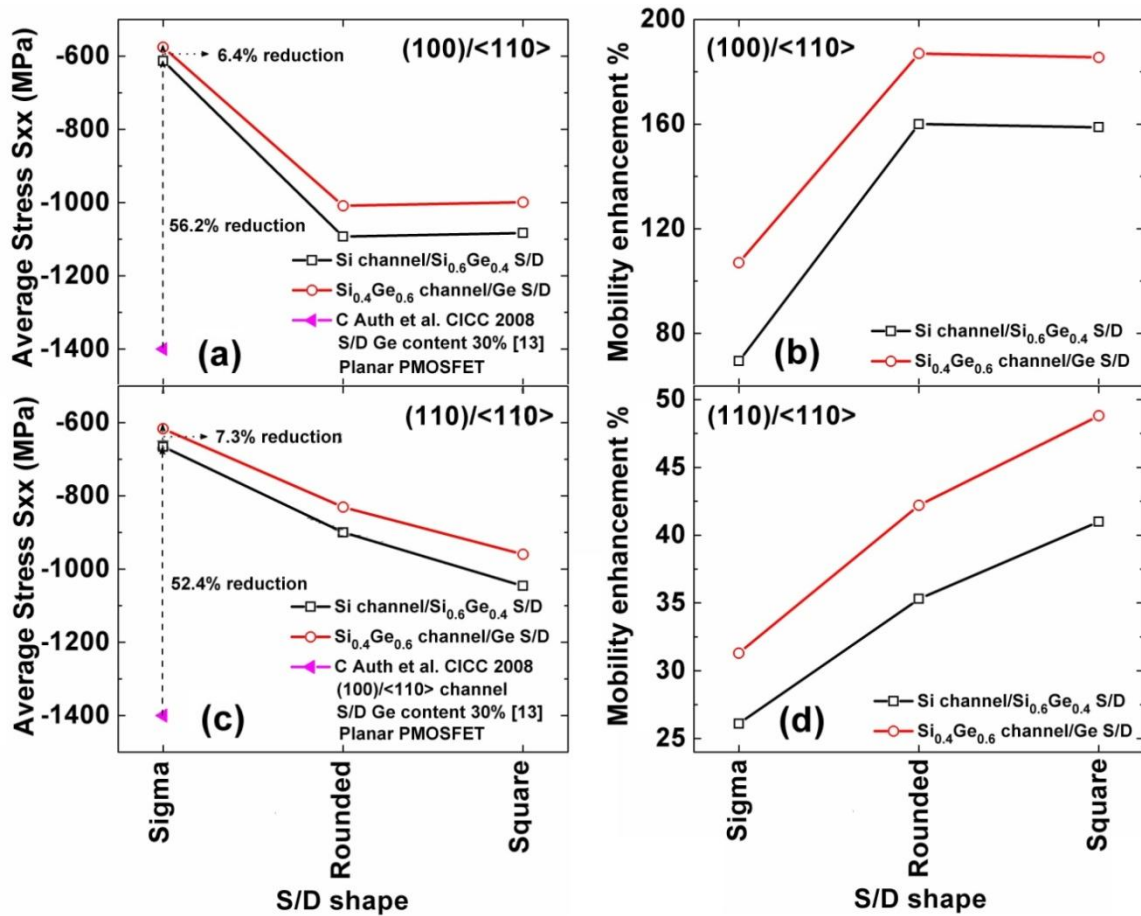


Fig. 3.11 Average sidewall (100)/<110> and (110)/<110> channel stress and corresponding mobility enhancement plots for structures in Figs. 3.4 (a-c)

The average stress of the (100)/<110> Si channels for both the rounded and square eSi_{0.6}Ge_{0.4} S/D structure show a stress reduction of ~22% from the planar case whereas the (110)/<110> Si channels show a 35.7% and 25.3% reduction in channel stress for the rounded and square eS/D respectively from the planar case.

The square S/D nested gate (5 tri-gates) structure has the least $L_{S/D}$ for the (110)/<110> channel compared to the other two S/D configuration resulting in the maximum stress. The $L_{S/D}$ for the (100)/<110> Si channels of the rounded and square eS/D nested gate structures are almost the same, resulting in almost equal stress values and mobility enhancements as seen in Fig. 3.11(b) but the $L_{S/D}$ for sigma S/D structure is significantly greater than the other two S/D profiles which causes the channel stress to degrade significantly. The mobility enhancements of strained Si for (110)/<110> channels are 26.1%, 35.3% and 41% for the sigma, rounded and square eS/D structures respectively. The (100)/<110> channels display much larger enhancements of 69.4%, 160% and 158.8% for the sigma, rounded and square eS/D structures respectively. Thus sigma S/D is not a viable option for tri-gate FETs although it is a better option for planar devices [13, 14].

The stress levels for the $\text{Si}_{0.4}\text{Ge}_{0.6}$ channel structures are $\sim 0.92x$ of the values for Si channel structures in Figs. 3.4(a-c) for the same lattice mismatch between the channel and S/D regions which is due to the smaller elastic moduli and Poisson's ratios of $\text{Si}_{0.4}\text{Ge}_{0.6}$ compared to Silicon. The mobility enhancements of $\text{Si}_{0.4}\text{Ge}_{0.6}$ for the (110)/<110> channels are 31.3%, 42.2% and 48.8% for the sigma, rounded and square eS/D structures respectively whereas the (100)/<110> channels show enhancements of 107%, 187% and 185.5% respectively. The sidewall stress profiles for Si/ $\text{Si}_{0.4}\text{Ge}_{0.6}$ channels with $\text{Si}_{0.6}\text{Ge}_{0.4}/\text{Ge}$ sigma S/D are plotted in Fig. 3.12

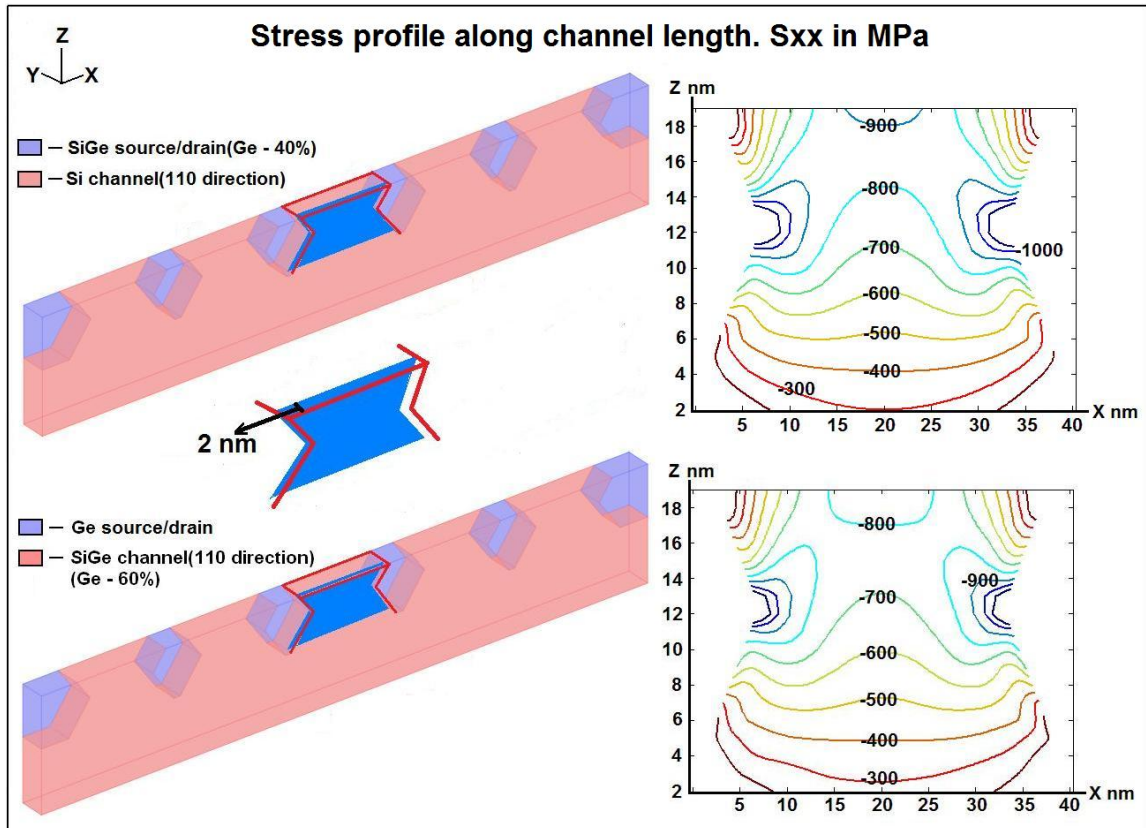


Fig. 3.12 Sidewall channel stress (S_{xx} in Mpa) profiles for the nested gate (5 tri-gates) with sigma S/D structure

Figs. 3.13(a-d) plot the stress profile evolution following bi-axially strained $\text{Si}_{0.75}\text{Ge}_{0.25}$ epitaxial growth on Si, fin patterning, S/D recess etch and eS/D(1.7% mismatch) re-growth. Fin patterning causes significant stress reduction ($\sim 31\%$) compared to the bi-axially strained layer as is evident from fig. 3.13 (b). The S/D recess etch further relaxes the residual stress of the fin almost completely due to the creation of free surfaces next to the channel.

The eS/D (1.7% mismatch) re-growth recovers the relaxed residual stress resulting from the S/D recess etch as seen in fig. 3.12 (d) confirming the viability of employing eS/D stressor technique for sub 32nm technology nodes.

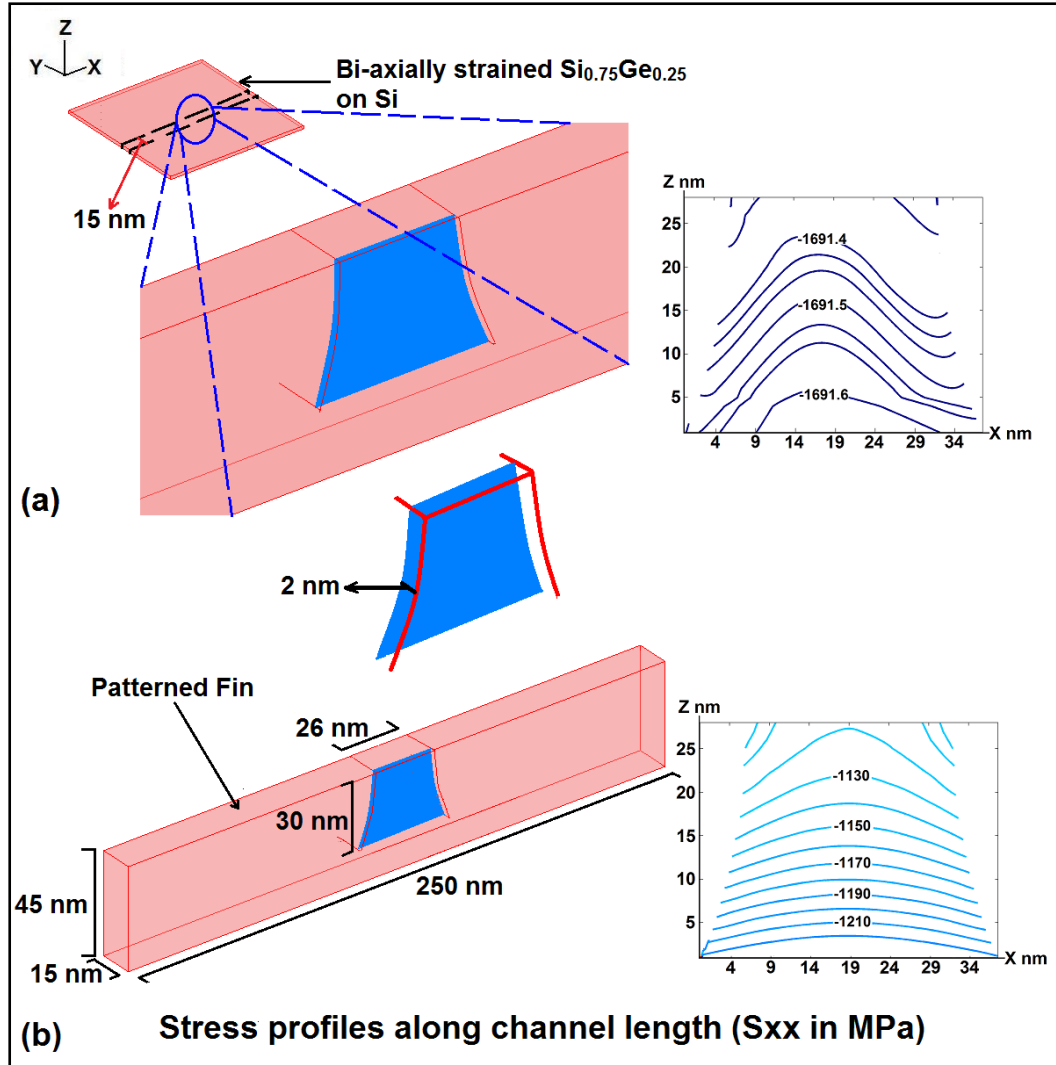


Fig. 3.13 (a,b) Stress profile evolution following bi-axially strained $\text{Si}_{0.75}\text{Ge}_{0.25}$ epitaxial layer growth, fin patterning

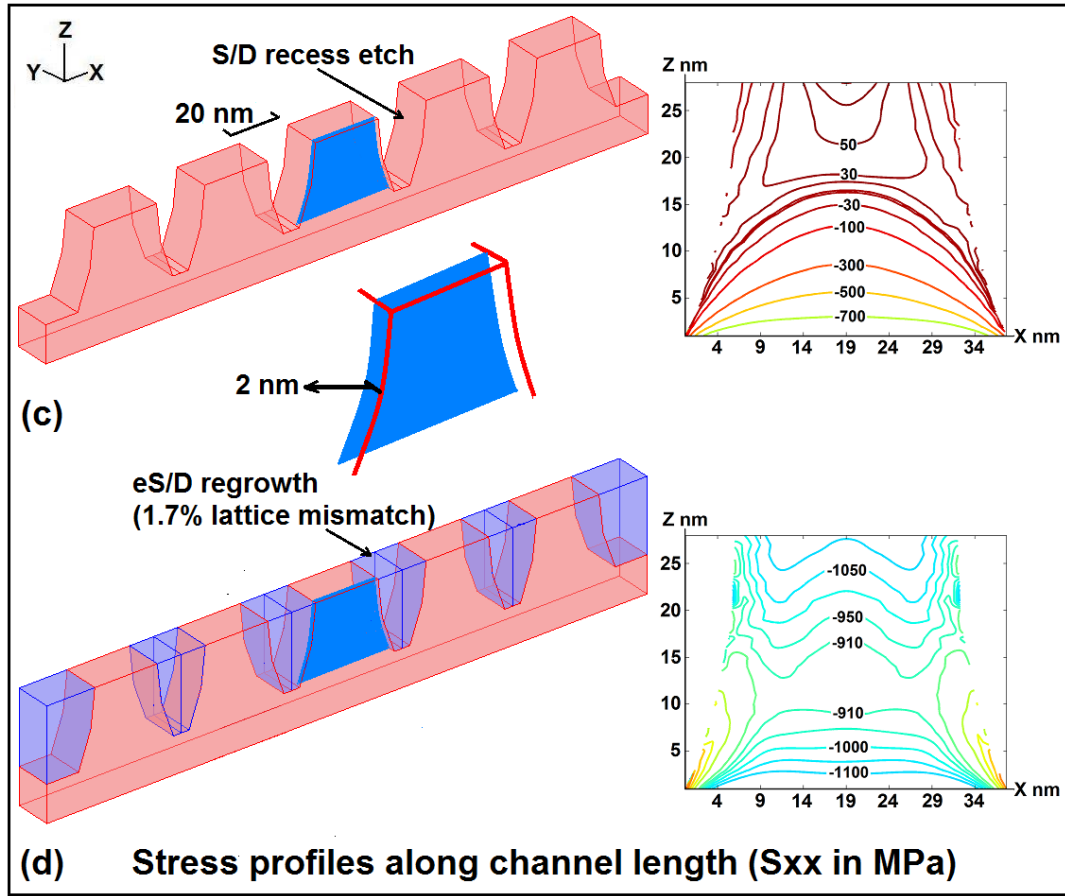


Fig. 3.13 (c,d) Stress profile evolution following S/D recess etch and eS/D re growth for nested gate (5 tri-gates) structure for Figs. 3.12 (a,b)

Fig. 3.14 plots the average sidewall stress vs fin length for a compressively strained $\text{Si}_{0.75}\text{Ge}_{0.25}$ on Si fin with the fin height and fin width dimensions being the same as those in Fig. 3.13b. The average sidewall stress will also depend on the Ge content of the SiGe fin. Increasing Ge content of the SiGe fin will increase the sidewall stress retention.

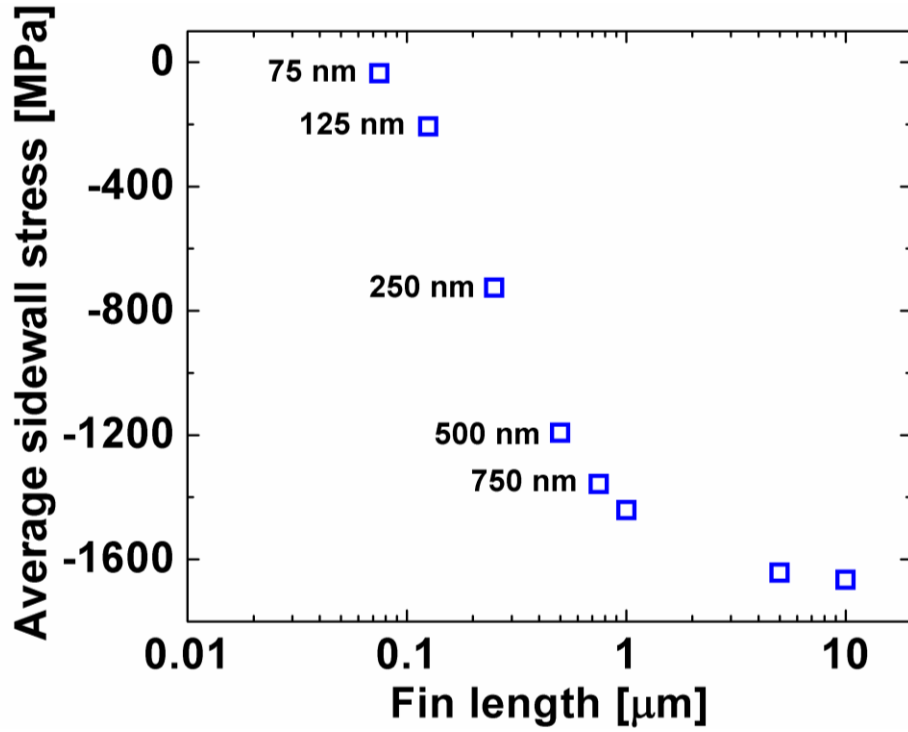


Fig. 3.14 Average sidewall stress vs fin length for 22nm node

Fig. 3.15(a) plots the residual stress for the (100)/<110> and (110)/<110> channels of uni-axially strained $\text{Si}_{1-x}\text{Ge}_x$ epitaxial layers for three channel Ge contents after S/D recess etch. The (100)/<110> channel stress shows similar behavior to the nested fins case due to the free surfaces next to the channel. The (110)/<110> channels show an average compressive residual stress due to the contribution from the lower fraction of the sidewall which is relatively farther away from the top free surface

Figs. 3.15 (b, c) show the average stress and the corresponding mobility enhancements respectively for a combination of the residual stress and the eS/D induced stress for the $\text{Si}_{1-x}\text{Ge}_x$ channels with different Ge contents. The (110)/<110> channels show increasing average channel stress with Ge content due to the increasing compressive residual stress resulting from greater lattice mismatch.

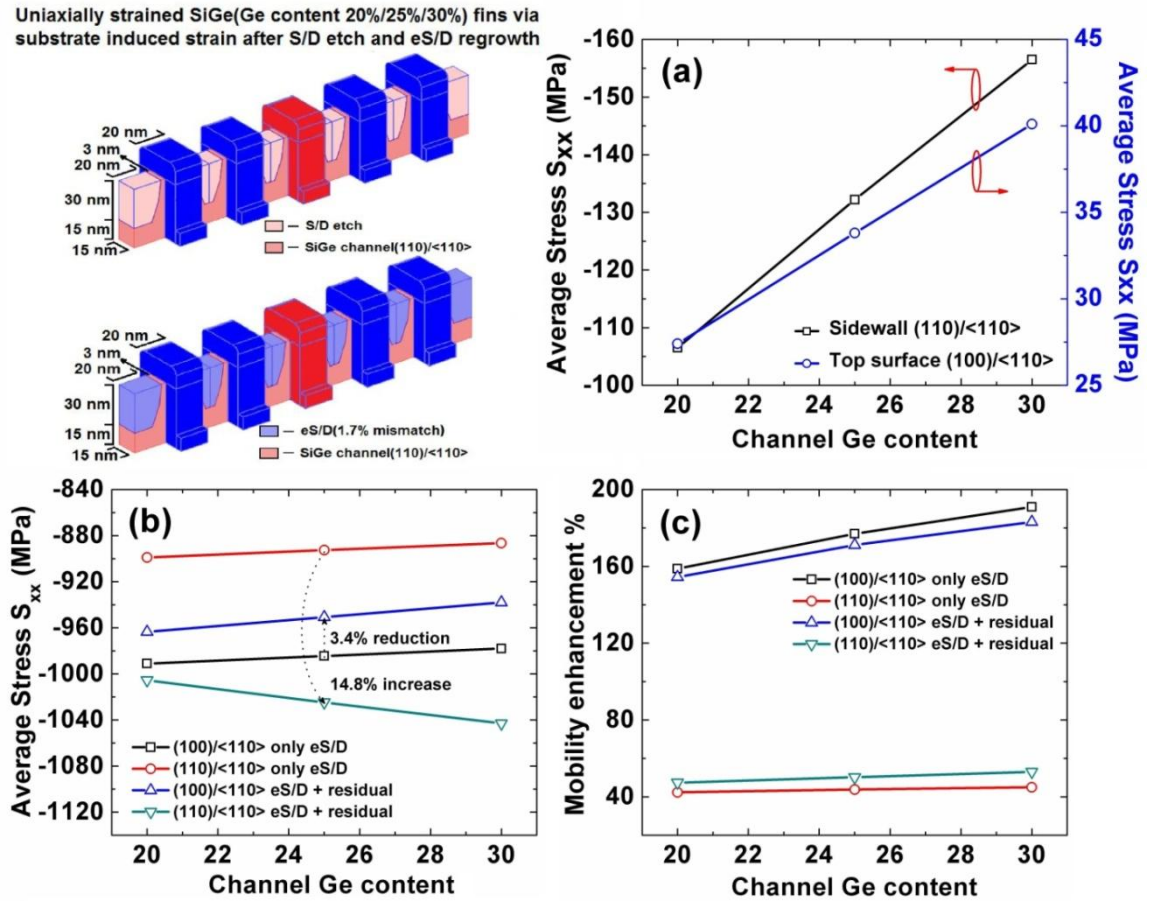


Fig. 3.15 Average channel residual stress and mobility enhancements after S/D recess etching, after eS/D regrowth

The (100)/<110> channels however show the same trend as the case when only eS/D stressors are used due to the residual stress becoming increasingly tensile for the (100)/<110> channel with increasing Ge content.

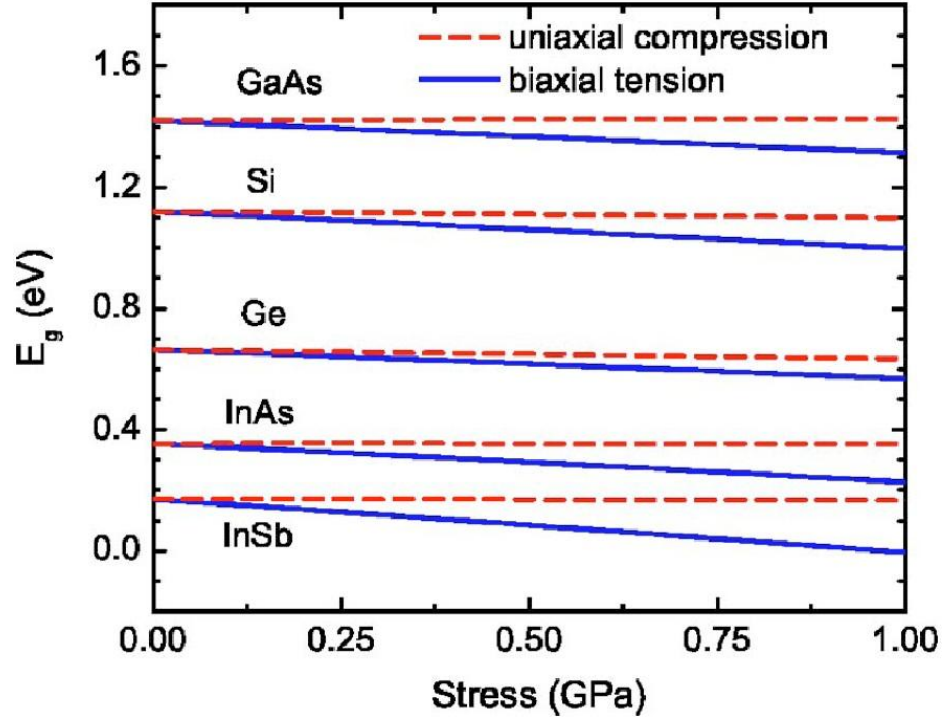


Fig. 3.16 Band gap variation with uniaxial compressive and biaxial tensile stress [35]

The variation in threshold voltage (V_T) due to the variation in the sidewall stress profile is an important consideration and needs to be addressed carefully. From the above Fig. we can see that the band-gap variation due to uniaxial compressive stress is $\sim 17\text{meV/GPa}$ for Si and $\sim 31\text{meV/GPa}$ for Ge. The uniaxial stress variation for the sidewall as shown in Fig. 3.13d is less than $\sim 100\text{MPa}$ across the sidewall. Hence it can be concluded that the V_T variation across the sidewall won't be significant enough [35] to degrade the sub-threshold slope of the device.

3.4 Conclusion

Nested gate layout displays greater channel stress than the nested fins and double nested structures stressing the significance of the reduced proximity between the channel and the extreme S/D free side domain walls in improving the channel stress. Channel stress can be improved by increasing the number of gates till it's limited due to other factors such as S/D Ge content, S/D etch depth. The free S/D sidewalls of the nested gate structure result in greater sidewall stress compared to the merged S/D case in double nested structures making nested gate structure more preferable over the former one.

Increasing eS/D Ge content offers significant improvement in the channel stress. The maximum Ge content however is dictated by the required S/D etch depth and vice versa which places a limitation on their use as independent controllable parameters for improving the channel stress.

The rounded S/D structure offers significant improvement in the channel stress over the sigma S/D structure which is converse to the planar case. The $L_{S/D}$ for Sigma eS/D structure is larger than for the other two structures resulting in significant channel stress degradation. Rounded S/D also offers greater flexibility in increasing the etch depth compared to sigma S/D as sigma S/D faces severe geometric constraints at the considered dimensions.

The eS/D technique when combined with the Nested gate layout structure demonstrates significant channel stress retention even for extremely scaled P-channel tri-gate FETs. The eS/D technique can thus be expected to continue to serve as an important addition to the conventional stressors for future P-channel tri-gate FETs.

4. FUTURE WORK

4.1 Experimental verification of the predicted mobility enhancements

The FEM simulations predict significant levels of achievable channel stress and mobility enhancements for the 22nm technology node with nested gate device layout. The next step would be to verify the stress levels and the corresponding mobility enhancements experimentally. Although ideally we would want to map the measured mobility enhancement with the measured channel stress it would be difficult to directly measure the level of channel stress as indicated in [32]. An estimate of the channel stress will have to be made based on the measured mobility enhancements.

A fabrication flow similar to that in Fig. 4.1 can be adopted to fabricate the simulated structures.

- Fin formation (SiN mask RIE)
- Sacrificial oxidation (2 nm dry O₂)
- HF wet etching
- Channel ion implantation
- SiN removal for Tri gate structure
- Gate oxide
- Gate formation
- Extension implantation (tilt 30°)
- Side wall formation
- Source/Drain implantation (tilt 0°)
- Activation spike anneal
- Ni SALICIDE

Fig. 4.1 Device fabrication flow for Fin and Tri-Gate SGOI MOSFETs [25]

The steps of S/D recess etch and eS/D regrowth will replace the S/D ion implantation step to achieve uni-axial strain in the channel.

The hole mobility can be extracted from the low V_{ds} regime of the I_d - V_d curves ensuring low field condition for accurate mobility extraction. The extracted mobility can be utilized to estimate the actual achievable channel stress for the respective structures. Further optimization of the structures in terms of the channel stress, S/D resistance, channel doping can be investigated to obtain optimum performance.

4.2 Scaled high Ge content SiGe and Ge multi-gate quantum well field effect transistors with varying levels of channel strain

Quantum well field effect transistors (QWFETs) have attracted considerable interest recently as they offer significant performance enhancement over conventional MOSFETs [36] which can allow us to continue device scaling beyond the 22nm technology node. QWFETs feature enhanced mobility compared to MOSFETs due to the separation between ionized dopant atoms and the carriers in the channel which reduces the ionized impurity scattering significantly improving the carrier mobility [37]. Fig. 4.2 illustrates how the separation of the carriers from their host dopant atoms is achieved. QWFET is a modification of the high electron mobility transistor (HEMT) where a dielectric is integrated with the HEMT essentially converting it into a FET [38, 39].

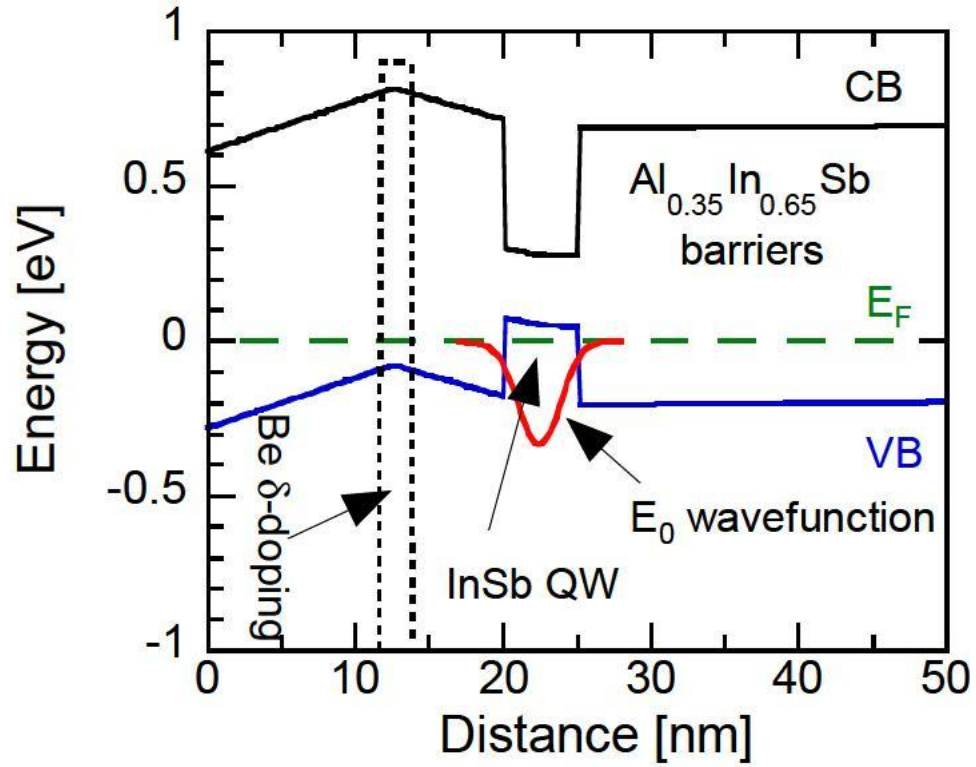


Fig. 4.2 Band diagram of InSb p-channel 1.9% compressively strained QWFET obtained using 8-band k.p simulation [38]

As mentioned before high Ge content strained SiGe alloys and Ge are being investigated thoroughly to replace Si as the channel material for PMOS in future technology nodes. It is evident that strained SiGe/Ge QWFET structures will offer greater advantages in terms of performance compared to bulk/SGOI/GOI structures due to their higher mobilities. Fig. 4.3 shows the structure of a recent study regarding strained Ge QWFET with an integrated high-k dielectric. Fig. 4.4 plots the mobility versus sheet carrier density in the channel for the strained Ge QWFET.



Fig. 4.3 Schematic of biaxially strained undoped Ge QW structure on a silicon substrate [39]

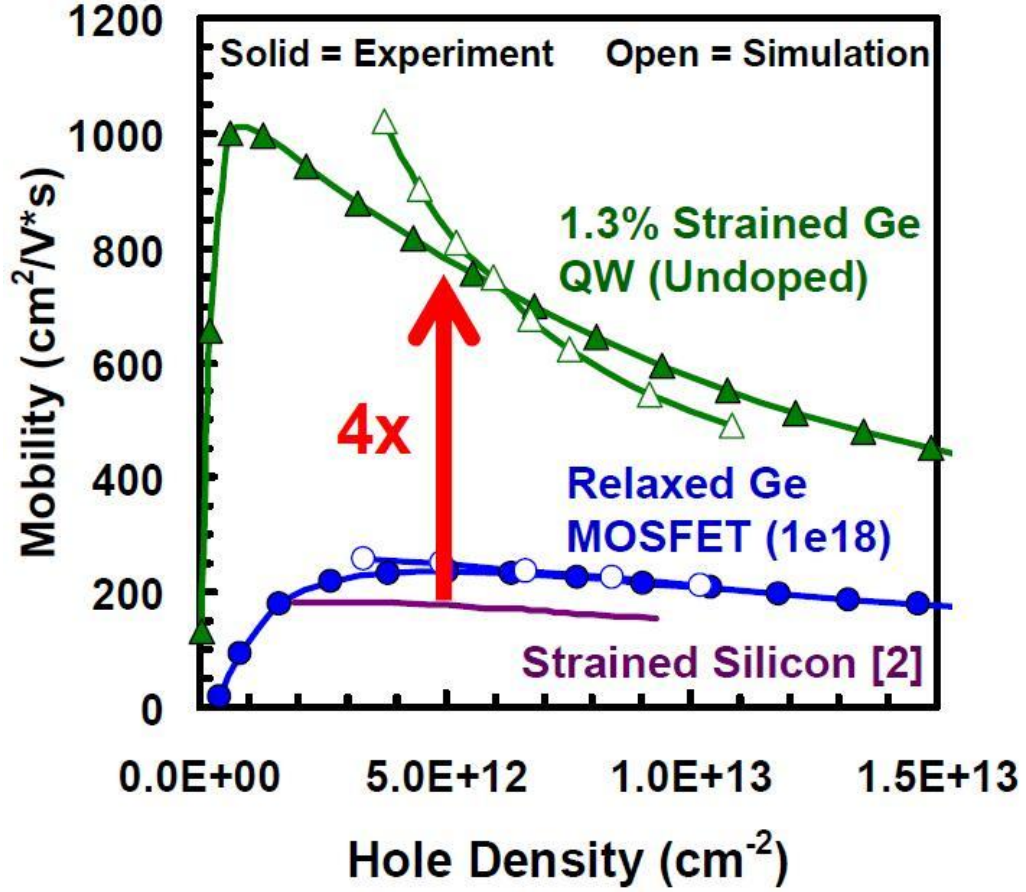


Fig. 4.4 Hole mobility vs sheet carrier density [39]

The device being planar is bi-axially strained and hence will not give the maximum possible mobility enhancement as can be inferred from the previous sections. For achieving maximum mobility enhancement the Ge QWFET will have to be uni-axially strained. Uni-axial strain can be achieved by patterning the planar QWFET into narrow fins as seen before. Implementing uni-axial strain in the Ge QWFET structure will further increase the hole mobility. The structure can be further optimized to obtain the optimum cut-off frequency f_T .

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