The Pennsylvania State University

The Graduate School

Graduate Program in Materials Science and Engineering

SYNTHESIS AND CHARACTERIZATION OF SILICON NANOWIRE ARRAYS FOR PHOTOVOLTAIC APPLICATIONS

A Dissertation in

Materials Science and Engineering

by

Sarah M. Eichfeld

Submitted in Partial Fulfillment
of the Requirements
for the Degree of

Doctor of Philosophy

August 2009

The dissertation of Sarah M. Eichfeld was reviewed and approved* by the following:

Joan M. Redwing
Professor of Materials Science and Engineering
Chair, Intercollege Materials Science and
Engineering Graduate Degree Program
Dissertation Advisor
Chair of Committee

Thomas E. Mallouk
DuPont Professor of Materials Chemistry and Physics

Suzanne E. Mohney
Professor of Materials Science and Engineering

Christopher L. Muhlstein
Associate Professor of Materials Science and Engineering
Corning Faculty Fellow

*Signatures are on file in the Graduate School

ABSTRACT

Due to rising energy costs and the growing demand for renewable energy, silicon nanowire arrays have become of interest for solar cells. Radial p-n junction silicon nanowire arrays allow for the decoupling of the directions of light absorption and carrier collection, which allows for the possibility of increased efficiencies. Prior device modeling studies have demonstrated that increased carrier collection can be obtained in radial p-n junction nanowires when the wire radius is approximately equal to the minority carrier diffusion length in the material. Consequently, radial p-n junction silicon nanowires are anticipated to enable increased efficiency in solar cells fabricated with less pure and therefore potentially lower cost silicon. Fabrication of these structures on low cost substrates such as glass would then enable a further cost reduction. The overall objective of this thesis was the development of processes for the fabrication of radial p-n silicon nanowires (SiNWs) using bottom-up nanowire growth techniques on silicon and glass substrates.

Vapor-liquid-solid (VLS) growth was carried out on Si(111) substrates using $SiCl_4$ as the silicon precursor. Growth conditions including temperature, P_{SiCl4}, P_{H2}, and position were investigated to determine the optimum growth conditions for epitaxially oriented silicon nanowire arrays. The experiments revealed that the growth rate of the silicon nanowires exhibits a maximum as a function of P_{SiCl4} and P_{H2}. Gas phase equilibrium calculations were used in conjunction with a mass transport model to explain the experimental data. The modeling results demonstrate a similar maximum in the mass of solid silicon predicted to form as a function of P_{SiCl4} and P_{H2}, which results from a change in the gas phase concentration of SiH_xCl_y and $SiCl_x$

species. This results in a shift in the process from growth to etching with increasing P_{SiCl4}. In general, for the atmospheric pressure conditions employed in this study, growth at higher temperatures >1000°C and higher $SiCl_4$ concentrations gave the best results. TEM analysis of silicon nanowires grown at different $SiCl_4$ concentrations revealed no distinct differences in the structural properties of the SiNWs. Doping of the SiNWs using trimethylboron (TMB) was also examined. Gated I-V measurements demonstrated that the SiNWs exhibited p-type behavior. Wires doped with a TMB/$SiCl_4$ ratio of 0.1 had a resistivity in the range of 10^{-3} Ω-cm. However, wires with a TMB/$SiCl_4$ ratio of $2x10^{-3}$ exhibited a resistivity of 10^3 Ω-cm.

The growth of silicon nanowire arrays on anodized alumina (AAO)-coated glass substrates was also investigated. Glass will not hold up to the high temperatures required for Si nanowire growth with $SiCl_4$ so SiH_4 was used as the Si precursor instead. Initial studies were carried out to measure the resistivity of p-type and n-type silicon nanowires grown in free-standing AAO membranes. A series of nanowire samples were grown in which the doping and the nanowire length inside the membrane were varied. Circular metal contacts were deposited on the top surface of the membranes and the resistance of the nanowire arrays was measured. The measured resistance versus nanowire length was plotted and the nanowire resistivity was extracted from the slope. The resistivity of the silicon nanowires grown in the AAO membranes was then compared to the resistivity of silicon nanowires grown on Si and measured using single wire four-point measurements. It was determined that the undoped silicon nanowires grown in AAO have a lower resistivity compared to nanowires grown on Si substrates. This indicates the presence of an unintentional acceptor. The resistivity of the silicon nanowires was found to change as the dopant/SiH_4 ratio was varied during growth. The growth and doping conditions developed from this study were then used to fabricate p-type SiNW arrays on the AAO coated glass substrates.

The final investigation in this thesis focused on the development of a process for radial coating of an n-type Si layer on the p-type Si nanowires. While prior studies demonstrated the fabrication of polycrystalline n-type Si shell layers on Si nanowires, an epitaxial n-type Si shell layer is ultimately of interest to obtain a high quality p-n interface. Initial n-type Si thin film deposition studies were carried out on sapphire substrates using SiH_4 as the silicon precursor to investigate the effect of growth conditions on thickness uniformity, growth rate and doping level. High growth temperatures (>900^oC) are generally desired for achieving epitaxial growth; however, gas phase depletion of the SiH_4 source along the length of the reactor resulted in poor thickness uniformity. To improve the uniformity, the substrate was shifted closer to the gas inlet at higher temperatures (950°C) and the total flow of gas through the reactor was increased to 200 sccm. A series of n-type doping experiments were also carried out. Hall measurements indicated n-type behavior and four-point measurements yielded a change in resistivity based on the PH_3/SiH_4 ratio. Pre-coating sample preparation was determined to be important for achieving a high quality Si shell layer. Since Au can diffuse down the sides of the nanowire during sample cooldown after growth, the Au tips were etched away prior to shell layer deposition. The effect of deposition temperature on the structural properties of the shell layer deposited on the VLS grown SiNWs was investigated. TEM revealed that the n-type Si shells were polycrystalline at low temperatures (650^oC) but were single crystal at 950°C. SiNW samples grown on glass were also coated; however, due to the temperature constraints, the maximum temperature used was 650^oC and therefore the n-type Si shells were polycrystalline.

SiNW arrays grown using $SiCl_4$ on Si(111) substrates were grown with a high degree of orientation and average growth rates of 3-4 μm/min at temperatures of 1050°C. Modeling results indicated the nanowire growth was limited by mass transport. SiNW arrays were also grown using SiH_4 on AAO coated glass. Epitaxial n-type Si regrowth was demonstrated on SiNW arrays

grown on Si(111) with $SiCl_4$. The n-type Si deposition was carried out using SiH_4 at 950°C and a total pressure of 3 Torr. SiNWs grown on AAO coated glass substrates were also radially coated with n-type Si; however, due to temperature limitations the shell was polycrystalline. Future work on this project could include a study on the doping of SiNWs grown using $SiCl_4$. Device measurements using the radial p-n junction SiNW arrays fabricated could also be carried out. Finally, a study on the effects of sample preparation, nanowire, and n-type shell doping could be correlated to the device measurements.

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

ACKNOWLEDGEMENTS

I would first like to express my gratitude to Dr. Joan Redwing first for giving me a job as an undergraduate and second for being willing to serve as my thesis advisor. I appreciate all that I have learned about CVD and nanowire growth. There are a few people who have also contributed to this research, and without them this project would not be complete. I would like to thank Rebeca Diaz for the initial single nanowire resistivity measurements and also Dr. Qi Zhang, Dr. Bangzhi Liu, Haoting Shen, and finally Dr. Xiaojun Weng for all of their help with TEM questions and also for the beautiful images they took.

Special thanks to Dave Snyder, Bill Everson and Randy Cavalero for giving some random high school kid a summer position working on SiC, without you guys I never would have known how much I love crystal growth and materials! I truly respect and admire you guys! Dave, thanks for pointing out what a good school PSU was! Randy, what can I say but thank you for finally leaving the door unlocked and all of the things you taught me, it truly helped in the lab!

Many thanks to the Redwing and Mohney groups both past and present members for all of their help and support. I have learned so much from all of our technical discussions! I would especially like to thank Ian for letting me borrow books from his "library", you always had the reference I needed! I would also like to extend my special thanks to Mary, Dan, Brian, and Dave for the soda breaks, running for pancakes, and also everyone who has been part of our rock band without them grad school would not have been as much fun. Dave and Erin, I do not know how to thank the both of you. I have been so lucky to have you both as friends. Dave you were a great officemate. I have learned so much from you both, and I look forward to continuing our friendship for years to come!

I would like to extend a special thank you to my family (Tom, Joan, Adam, Wayne, Elaine, Chris and Erin) and friends for all of their love and patience the past year while we have tried to finish up. Adam your visits to my office have kept life interesting and entertaining, I only hope to repay the favor someday.

Finally, to my wonderful husband, Chad, you have been my rock and can always make any day better. Thank you for all of your help scientifically but most of all thank you for all of your love and support, without you I never would have made it this far. *Armor Vincit Omnia.*

Chapter 1

Introduction

1.1 Motivation

The demand for energy has risen sharply over the past decade. World energy consumption increased 2.4% in 2007[1]. Much of the energy comes from fossil fuels such as oil, coal or natural gas. Fossil fuels will be unable to indefinitely sustain the need for energy and also contribute to pollution through CO_2 emissions. As the world energy consumption increases, the cost of oil, natural gas, and coal will only increase. It has become clear the world needs to find sustainable, clean energy resources. This has propelled the drive towards renewable energy. In 2006, total renewable energy consumption increased (Figure **1-1**). However, the use of renewable energy still pales in comparison to the fossil fuel usage[2]. Potential renewable energy sources include water, wind and sunlight. However, with energy costs rising and fossil fuels still being most heavily used, there is more of an incentive to create cleaner and cheaper ways of producing energy using these abundant resources.

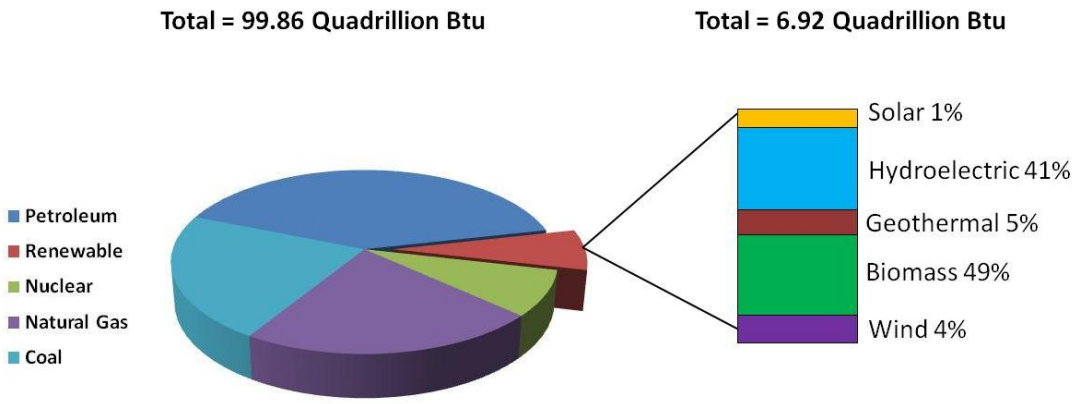


Figure **1-1**: The United States energy consumption in 2006.[2]

While sunlight is currently only being used for approximately 1% of the nation's renewable energy, it is the most abundant renewable energy resource and hits the earth with 174 petawatts of solar radiation per day. Nearly 1/3 of this gets reflected back into space but the rest comes back to earth. If all of that solar radiation were harnessed into energy, it would be double the energy of all of the earth's non-renewable (oil, natural gas, coal, uranium) resources.[3]

Conversion of sunlight into energy holds great promise not only for solar cells but other photovoltaic devices. This includes traditional solar cells and photoelectrochemical devices that use the sun for H_2 generation via water splitting. Currently, it is expensive to produce a high efficiency solar cell thus making it less appealing for consumers to use solar cells for a main source of energy. Solar cells have been around for many years but in the past decade sales have increased by 30%.[4] This is mostly due both technological advancements combined with government and economic policies. Currently 94% of the market is dominated by silicon

photovoltaic devices including amorphous, single and polycrystalline material. Semiconductor materials are often used for both photovoltaics and photoelectrochemical cells. This is because they have bandgap energies in a range where they can convert light into energy. Silicon is widely used due to its natural abundance, its nearly ideal bandgap of 1.1eV[5], and the existing infrastructure and technology associated with the semiconductor electronics.[6]

1.2 Silicon Photovoltaics

A typical solar cell structure consists of a junction between a n-type and p-type semiconductor[7]. Photons greater than the band gap are absorbed by the semiconductor. The absorption activates electron transitions from the valence band to the conduction band to generate electron-hole pairs. The carriers that diffuse into the depletion region before they recombine can be separated by the applied electric field. At the p-n junction, the electrons are swept towards the n-type side while the holes are swept towards the p-type sides thus generating a photovoltage (V_{OC}) as shown in Figure **1-2**. Recombination of the electron-hole pairs that are generated can lead to reduced efficiency. Recombination depends on the presence of recombination centers or carrier traps and the minority carrier diffusion length (L), which is the average distance a carrier can move from the point of generation until it recombines.

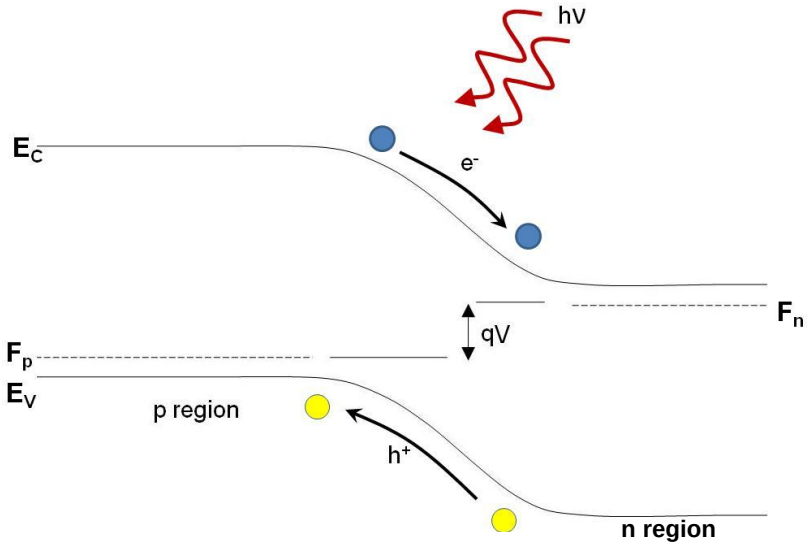


Figure **1-2**: Band diagram of a p-n junction.

In solar cell devices, the photogenerated of carriers can then be collected to an external circuit and used to power devices. A photovoltage used in conjunction with an electrolyzer can drive the chemical reaction to split water and thereby produce clean H_2.[8] This would be advantageous for hydrogen production and use in applications such as fuel cells. The current problems associated with these photovoltaic devices and also solar cells is the need for increased efficiency and reduced cost to make these types of devices and their applications economically viable.

The theoretical efficiency of a single material solar cell is 31% and in operation a single crystal Si solar cell can currently reach 16-20% efficiency.[4] However, this can only be achieved at a high cost, which makes it less economically viable. This is because single crystal Si must be high purity to achieve long minority carrier diffusion lengths. A typical planar solar cell is shown in Figure **1-3** below.

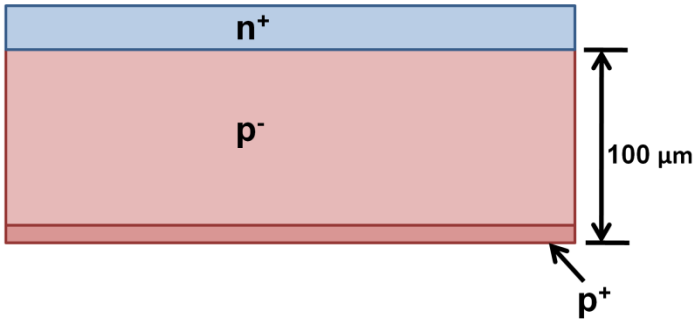


Figure **1-3**: Traditional planar solar cell geometry.

The silicon must be ≥ 100 µm to absorb the majority of solar radiation. However, the minority carriers must be able to diffuse comparable lengths without recombining so the minority carrier diffusion length needs to be large, in order for collection efficiencies to be high. If the minority carrier diffusion length is short, the minority carriers could recombine before they are collected. The minority carrier diffusion length varies with doping level and a plot of L versus the doping for silicon is shown in Figure **1-4** below. This is calculated using the equation for minority carrier diffusion length (L)[9]:

$$L = \sqrt{D\tau} \tag{1.1}$$

where D is the diffusivity, and τ is the carrier lifetime. The lifetime is determined by[9]:

$$\tau = \frac{1}{R_{ec}\, N} \tag{1.2}$$

where N is the dopant concentration and R_{ec} is the recombination coefficient which is a function of temperature and dependent on the band structure. For calculations in Figure **1-4** a typical value for indirect-bandgap semiconductors of 10^{-15}cm^3/s was used. For an n-type doping density of 10^{19}cm^{-3} the minority carrier diffusion length is approximately 4µm, while a p-type doping density of 10^{20}cm^{-3} has a minority carrier diffusion length of 200 nm. The p- region needs to be approximately 10^{16} cm^{-3} in order to have a diffusion length (L) to be ≥100 µm. In order to achieve this the material needs to be high quality with very few impurities as this would lead to shorter minority carrier diffusion lengths, which would decrease the efficiency of a planar structure, such

as shown in Figure **1-3**.This is why there is a large p- region in the planar solar cell geometry, so that the minority carrier diffusion length remains as large as possible.

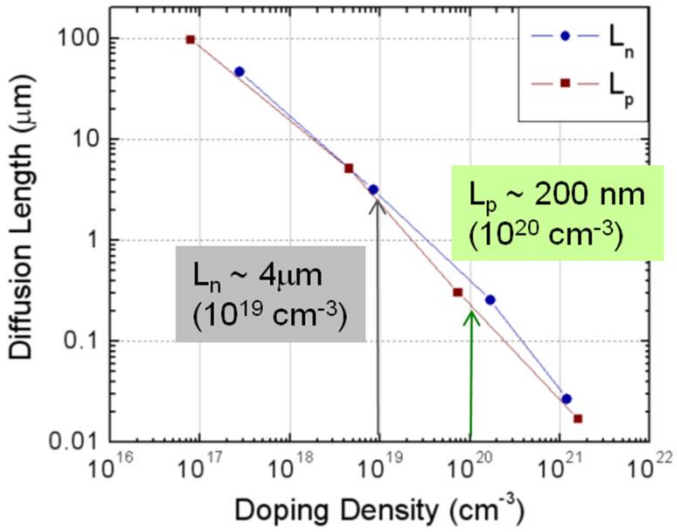


Figure **1-4**: Minority carrier diffusion length plotted versus doping density.[9]

The problem with single crystal planar Si solar cells is the high cost due to the high purity that is required. Polycrystalline Si cells are more affordable, however, the efficiencies are decreased (11-13 %) due to charge separation and recombination at the grain boundaries.[4] Research has been trying to bridge the gap between expensive, high efficiency single crystal Si solar cells and the lower cost and efficiency polycrystalline devices.

One way to improve the efficiency of devices made with lower quality silicon has been through exploration of alternative geometries that reduce the junction distance. Green *et al.* proposed a parallel multijunction solar cell with alternating p- and n-type layers.[10] The like polarity layers are connected in parallel shown in Figure **1-5**. Fabrication involves the deposition of alternating polarity Si layers, followed by laser grooving and groove-wall doping to form channels for a buried contact. The layer thicknesses in this type of geometry are shorter than the minority diffusion carrier length, which allows for shorter collection distances and increased

efficiency. Another multijunction cell, proposed by Sater *et al.*[11], utilizes edge illumination to eliminate the need for front/back contacts and allow for greater carrier collection similar to the parallel multijunction design. Fabrication of a vertical multijunction cell involves the stacking of several diffused p+nn+ silicon wafers by stacking, metalizing and alloying together. After dicing of the samples, etching to remove saw damage, passivation, and anti-reflection coatings are needed. These designs, while allowing for increased efficiencies in lower quality material, are still complex to fabricate due to numerous processing steps and do not significantly reduce the cost.

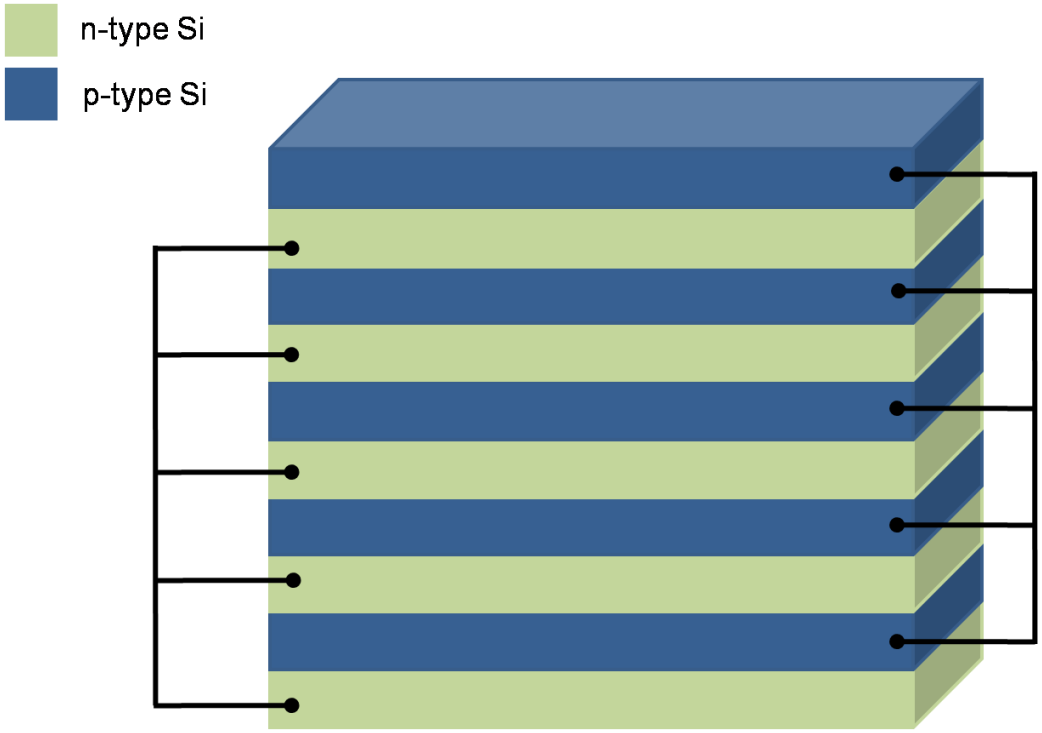


Figure **1-5**: Illustration of parallel multijunction concept with like polarity layers connected in parallel.[10]

1.2.1 Silicon Nanowire Solar Cell

Another way to increase the surface area in the direction of incident light and obtain a thin area in the direction of carrier collection would be to fabricate radial p-n junction whisker or nanowire solar cells. Diepers et al.[12] originally patented a solar cell design in 1979 consisting of a radial p-n semiconductor whisker array that is similar in theory to multi-junction solar cells. The patent proposes the use of single crystal Si whiskers to increase the surface to volume ratio to increase the quantum yield as opposed to a planar geometry.

A schematic of a radial p-n high aspect ratio solar cell is shown in Figure **1-6 (a)** and **(b.)** shows a close-up schematic showing the radial junction. Similar to the multijunction cells that take advantage of alternative architectures, this geometry may enable greater efficiency for two reasons. The first is a large distance (~100 μm) in the direction of incident light, which would allow for maximum light absorption. The second is a short distance in the direction of carrier collection to improve the collection efficiency of generated carriers. In addition, the highly textured surface provided by the wire array could provide enhanced light absorption.[13,14] Tsakalakos *et al.* observed increased broadband optical absorption in SiNW arrays on glass compared with solid thin films of similar thickness[13], while a similar observation by Fang *et al.* was made for arrays etched on Si(111) wafers.[14] This kind of design in theory could produce efficiencies equal to or higher than that of planar silicon cells made today.

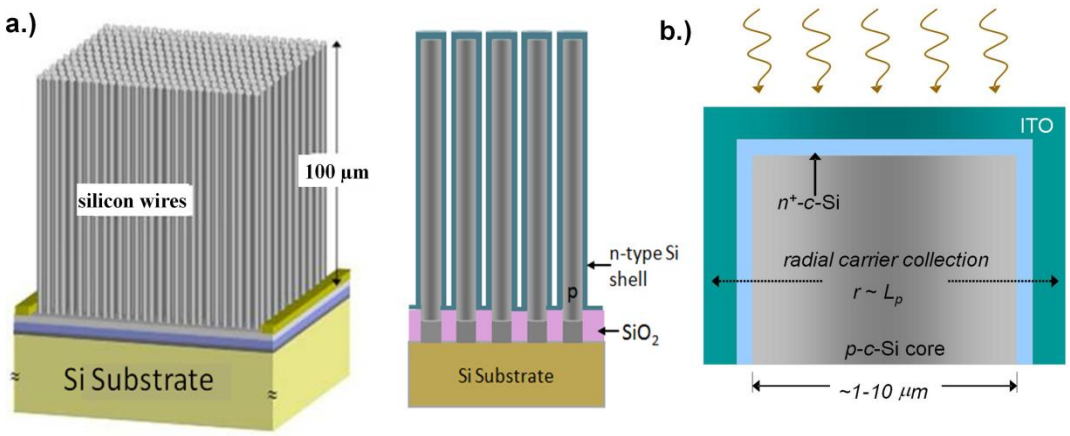


Figure **1-6**: High aspect ratio silicon solar cell. a.) A SiNW array grown on a Si wafer (left) and a cross-sectional view of the p-n junction (right) and b.) expanded view of a single SiNW showing the direction of carrier collection.

Device physics modeling performed by Kayes *et al.*[15] examined the performance of creating a radial p-n junction nanorod solar cell. This geometry takes advantage of a thick area (~100 μm) in the direction of incident light, which would allow for maximum light absorption and a short distance in the direction of carrier collection to improve the collection of generated carriers. This geometry is shown in Figure **1-6**. The model results indicated that it would be possible to achieve higher efficiencies from such a nanowire device compared to a planar Si single crystal solar cell provided that the wire radius is approximately equal to the minority carrier diffusion length and the doping levels are high enough that the nanowire radius is not fully depleted. The modeling also indicated that the trap density in the depletion region of the radial p-n junction nanorod solar cell must be relatively low ($< 3x10^{15}cm^{-3}$). The length of the solar cell must also have a length approximately equal to the optical thickness. If these criteria are met, potential efficiency gains between 1.5-11% are expected.

A finite element simulation of a 2D cylindrically radial p-n wire solar cell by Dr. Chito Kendrick following the approach of Kayes *et al.* and was compared to a planar device. The simulation was performed using Sentaurus TCAD software. The model was done assuming p-

type ($1x10^{18}cm^{-3}$) SiNWs of 2.5 µm diameter and 25 µm long. The n-type shell ($5x10^{18}$ cm^{-3}) had a 0.5 µm shell thickness as shown schematically in Figure **1-7(a)**. The model results predict a higher current density for a radial p-n junction cell compared to that of a planar cell of similar thickness and doping density (Figure **1-7(b)**). Based on these modeling results, it is anticipated that a radial p-n junction high aspect ratio solar cell will have a high efficiency and if grown on a low cost substrate will be able to be produced cost effectively.

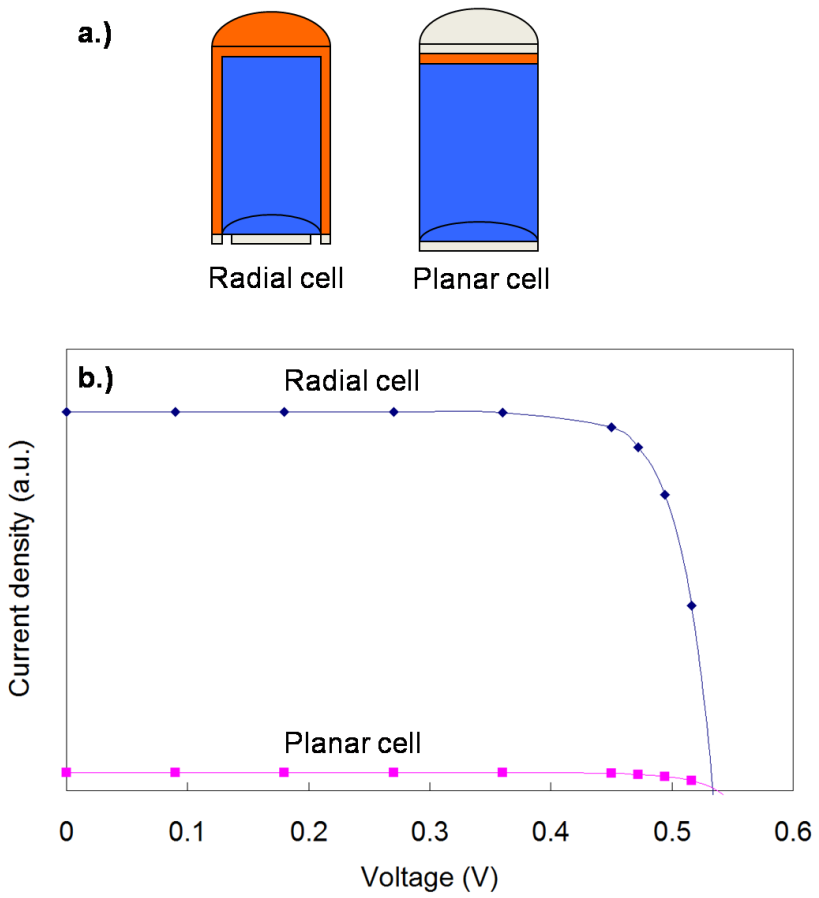


Figure **1-7**: a.) Schematic of a planar geometry and radial geometry and b.) Modeled current density versus voltage for both planar and radial geometry.

1.2.2 Fabrication of Silicon Nanowire Solar Cell

One way to potentially reduce the cost of such a device would be to use "bottom up" fabrication methods to create a large area high density wire array. To date, there have been numerous studies on single crystal silicon nanowire (SiNW) growth by the vapor-liquid-solid (VLS) mechanism. VLS growth uses a catalyst, most commonly Au, to create a Au-Si liquid alloy above its eutectic temperature of 363°C as seen in the phase diagram (Figure **1-8**).[16]

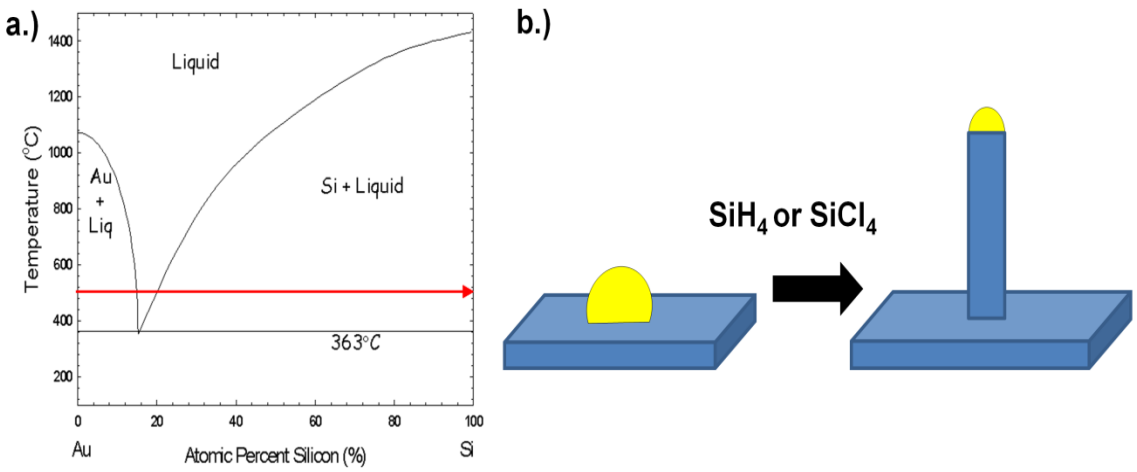


Figure **1-8**: a.) Phase diagram of Au-Si. b.) Schematic of VLS mechanism.

As the liquid alloy becomes supersaturated with Si, Si precipitates out to form a nanowire.[16] The size of the wire is controlled by the size of the initial Au catalyst. By combining VLS growth with chemical vapor deposition (CVD), complex structures such as radial and axial multijunctions can be achieved by in-situ doping through the tight control of precursor gases.[17-20] While there have been great strides in the understanding and control of nanowire growth, there are still many steps and details that need to be understood and mastered to utilize this approach to fabricate a large area, high aspect ratio SiNW array solar cells.

In order to create an "ideal" nanowire solar cell device there are several material requirements that must be met or addressed. The nanowires must be single crystal, and produced as a well ordered vertical array. The nanowire diameter and length should be uniform and high growth rates (μm/min) would be advantageous. Since the direction of light absorption is decoupled from the direction of carrier collection in this geometry, the length of the SiNWs still need to be long (100 μm), consequently, a faster nanowire growth rate would reduce sample growth time and thus be more cost effective. The ability to incorporate dopants during nanowire growth is also required. A smooth nanowire surface is important in order to achieve a high quality radial shell. Au forms deep level states in Si, which could lead to a decrease in carrier lifetimes. Since the silicon nanowires are grown using a Au catalyst it will be important to remove the Au prior to the shell layer formation.

The radial n-type silicon coating also has important requirements. Ideally, the n-type Si should be single crystal and the interface between the n-type shell and wire should be high quality with few impurities or defects present. As mentioned, this could lead to recombination at the p-n interface and yield poor device performance. The n-type Si coating should be conformal on the high aspect ratio structures with uniform thickness. Finally, the n-type Si must be controllably doped to maintain correct p-n carrier concentrations.

Recently, there have been several papers reporting the fabrication of single wire silicon nanowire solar cells.[14,18,20-24] Kempa *et al.* fabricated axial p-i-n and p-n silicon nanowire photovoltaic devices.[18] SiNWs were synthesized using Au nanoparticles via VLS. It was found that the p-i-n structures had an increased open circuit voltage (V_{OC}) and that the V_{OC} increased with increasing –i layer thickness. An efficiency of 0.5% under AM 1.5G illumination and V_{OC} of 0.29V were reported from the optimized p-i-n structure. An efficiency conversion of 0.46% under AM 1.5G illumination was also reported by Kelzenberg *et al.* for axial p-n junction single nanowire devices. [21] Samples were grown using $SiCl_4$ and the single nanowire backgated I-V

measurements revealed the wires to be n-type doped. Through electrical heating of a single Al contact on a SiNW, a rectifying axial p-n junction was created and exhibited photovoltaic behavior. Measurements corresponded to a solar conversion efficiency of 0.46% and V_{OC} = 0.19 V. Scanning photocurrent microscopy (SPCM) was used to determine the minority carrier diffusion length. Diffusion lengths of > 2μm were observed in VLS grown SiNWs.

Single wire solar cell devices have also been reported using radial p-n SiNWs. Tian *et al.* were able to produce radial p-n junction SiNWs grown via vapor-liquid-solid mechanism using SiH_4 as the Si precursor.[20] An n-type shell layer was deposited at a pressure of 25 Torr and a temperature of 650°C, using 0.15 sccm SiH_4 and 0.75 sccm PH_3. TEM revealed that the radial n-type shell was polycrystalline. The nanowires were removed from the substrate via sonication and only single nanowire measurements were carried out. It was reported that core/shell SiNW diodes performed better when a p-i-n radial structure was used. Photovoltaic efficiencies between 2.3-3.4 % under AM 1.5G illumination were reported using the p-i-n structure. The V_{OC} was 0.26 V. The catalyst used for p-type nanowire growth was not removed prior to shell deposition, which could lead to issues with device performance.

Several groups have reported radial p-n SiNW solar cell devices fabricated using large area nanowire arrays. These radial arrays were fabricated by wet etching[14,24], and also through vapor-liquid-solid growth.[20-23] Tsakalakos *et al.* grew p-type SiNWs via VLS growth with SiH_4, H_2 and HCl. The p-type wires were grown using a Au catalyst and Trimethylboron (TMB) at 650°C on stainless steel foil. The SiNWs were oxidized and stripped with HF prior to deposition of an n-type amorphous Si layer using PECVD to create the radial junction.[22] For these conditions the best V_{OC} was 0.13V and the devices exhibited a low efficiency due to a high series resistance.

Garnett *et al.* produced radial p-n junction SiNW arrays using wet etching of single crystal Si substrates to create the n-type core and LPCVD to deposit a p-type amorphous shell.[24] In trying to use low-energy, scalable processes, the SiNW arrays were fabricated by etching. The

a:Si shell was crystallized in an RTA at 1000°C for 10 seconds. After the crystallization step, TEM revealed that the shell was polycrystalline. Contacts were made to the back of the wafer using Ti/Ag (n-type Si core), and Ti/Pd on the p-type Si shell. An efficiency of 0.5% under AM 1.5G illumination and a V_{OC} of 0.29 V was reported for the SiNW array, which is similar to the 0.46% reported by Kelzenberg *et al.*[21] on a single nanowire. The demonstration of radial p-n junctions is a first step towards realization of a nanowire solar cell, although there is still much work to be done in order to achieve high efficiencies. The low open circuit voltages reported may contribute to the low efficiencies. A typical V_{OC} for an individual silicon solar cell with a 2 cm^2 area is approximately 0.5-0.6 V.[9] The low V_{OC} may be due to unoptimized diameter distributions, or local regions of shunting across cells, and the Au catalyst may limit the lifetime in Si.[22]

Experimentation on silicon nanowire arrays as photoelectrochemical cells has also been carried out.[25-27] A photoelectrochemical cell (PEC) is essentially a solar cell that generates electrical energy from light. Typically the cell uses a semiconductor and also a metal cathode in an electrolyte. A metal serves as the backside contact to the Si substrate while the liquid electrolyte acts as the top contact. Peng *et al.* obtained NW arrays via wet etching into a single crystal n-type Si wafer.[27] The nanowire diameters ranged from 20-300nm and it was found that etched Si nanowires have a rougher surface as compared to VLS grown SiNWs. For the PEC, the n-type SiNWs served as the photoelectrode and a Pt mesh as the counterelectrode immersed in a 40% hydrobromic and 3% bromine solution. Open circuit voltages on the n-type SINW arrays were between 0.66-0.73 V.

Goodey *et al.*[25] obtained SiNW arrays through vapor-liquid-solid growth using SiH_4 while Maiolo *et al.*[26] obtained arrays of nanowires using $SiCl_4$. In both cases the Au tips that served as a catalyst for nanowire growth were removed prior to making photoelectrochemical measurements. Goodey *et al.* used p-type doped SiNWs grown using SiH_4 and TMB at 500°C. The Au catalyst was etched away and the SiNW photoelectrode was immersed in a solution of

2mM tris(1,2'-bipyridl)ruthenium(II) hexafluorophosphate($Ru(bpy)_3^{2+}$) (bpy =2,2'-bipyridl) and 100 mM tetra(n-butyl)ammonium tetrafluoroborate ($TBAF_4$) in dry CH_3CN with a $Ag/AgNO_3$ reference and Pt gauze counter electrode.[25] A open circuit voltage of 0.22 V was obtained for SiNWs doped with a TMB/SiH_4 ratio of $2x10^{-4}$. Higher TMB/SiH_4 ratios yielded lower V_{OC}, which may be due to the higher doping causing an increase in the density of surface states at the nanowire surface. Maiolo *et al.* used n-type SiNWs grown at 1050°C with $SiCl_4$ and Au as the catalyst. The photoelectrochemical cell consisted of a 1,1'-dimethylferrocene($Me_2Fe)^{+/0}$ redox system in CH_3OH. The average open circuit voltage on the SiNW arrays was 0.389 V.

In summary, radial p-n junction nanorod solar cells were modeled and it was suggested that the nanowire radius needs to be approximately equal to the minority carrier diffusion length for optimum efficiency.[15] Single nanowire solar cells were fabricated and measurements made indicate that p-i-n structures have improved diode properties.[18,28] Diffusion length studies were carried out on axial p-n single nanowires formed by Al contact, with a reported diffusion length of approximately 2 μm.[21] Silicon nanowire arrays were fabricated both by VLS[22,23] and etching[24] methods on various types of substrates. Finally, photoelectrochemical cells have been created to measure the photovoltage of SiNW arrays.[25-27] In all cases, the radial shell of the nanowire was either amorphous or polycrystalline in nature. There have been no reports of single crystal radial shells to date. Also, it should be noted that in all cases the open circuit voltages are low, which means that recombination is occurring in the bulk, at the p-n interface or on the surface. The low V_{OC} could possibly be improved upon by growing high quality SiNWs and also by improving the p-n interface. The interface could be improved upon by growth of an epitaxial n-type Si shell as opposed to all the current devices that have been produced with a polycrystalline or amorphous shell.

1.3 Focus of this Study

The overall goal of this research is to develop processing technology for the fabrication of large area radial p-n junction SiNW arrays. Two substrates were used for this work: (111)Si which enables the epitaxial growth of Si nanowires; and anodized alumina-coated glass which is of interest for obtaining low cost devices.

The initial research focused on the growth of silicon nanowires on (111)Si using $SiCl_4$ to produce highly oriented, single crystal nanowire arrays at high growth rates which are needed for high efficiency solar cell devices. Prior studies of Si whisker growth using $SiCl_4$ focused primarily on understanding the mechanism of vapor-liquid-solid growth and the effects of diameter on growth rate. The work in this thesis was aimed instead at understanding the role of $SiCl_4$ gas phase chemistry in the nanowire growth process using a combination of experimental studies and thermodynamic modeling. Additional studies examined the effect of growth conditions on the orientation of the nanowires with respect to the substrate and the structural properties of the wires. Initial p-type doping studies of the Si nanowires grown with $SiCl_4$ were also carried out.

In order to create lower cost solar cells, the growth of silicon nanowires on anodized aluminum membranes (AAO) fabricated on indium tin oxide (ITO) coated glass substrates and AAO coated aluminum wires (provided by Illuminex Corp.) was investigated. In the glass samples, the ITO layer serves as the bottom contact to the p-type SiNWs while the AAO membranes provides a template for nanowire growth and serves to isolate the n-type radial coating from the ITO contact layer. Since nanowire growth using $SiCl_4$ occurs at temperatures greater than 800^{o}C which is too high for growth on glass, the SiNWs were fabricated using SiH_4 instead. Growth conditions for the VLS growth of SiNWs in AAO templates using SiH_4 were previously reported[29,30] and served as the basis for the initial studies reported in this thesis. The

effect of dopant/SiH_4 ratio on the resistivity of nanowires grown in free-standing AAO membranes was investigated. A method was developed to measure the resistivity of large area nanowire arrays grown inside the AAO membranes and the results were compared to that obtained from four-point resistance measurements of single nanowires.[31] These conditions were then used to fabricate undoped and p-type SiNWs on AAO-coated glass and AAO-coated aluminum wire substrates.

The deposition of conformal n-type Si shell layers on Si nanowires grown on (111)Si substrates and AAO-coated glass was then investigated as the final step in the fabrication of radial p-n junction nanowires. While the deposition of polycrystalline and amorphous Si shell layers on SiNWs was previously demonstrated for nanowire solar cell applications[20,21,24], the effect of deposition conditions on shell layer morphology has not been investigated in detail. Single crystal n-type Si shell deposition is of particular interest in order to fabricate high quality radial p-n junction interfaces but has not been reported thus far. Initial n-type Si thin film calibration studies were carried out to identify conditions to obtain suitable thickness uniformity and growth rate for the shell layer deposition studies. The effect of PH_3/SiH_4 ratio on the film resistivity and doping level was also determined to identify conditions that yielded highly doped layers. The growth conditions obtained from the calibration studies were then used in subsequent experiments to investigate the effect of growth temperature on the morphology of n-type Si shell layers deposited on SiNWs grown (111)Si substrates. The deposition of n-type Si on p-type SiNWs grown on AAO-coated glass substrates was also studied.

1.4 References

[1] B. Solar, "BP Statistical Review of World Energy June 2008," (2008).

[2] E. I. Administration, edited by U. S. D. o. Energy (Office of Coal,Nuclear, Electric, and Alternate Fuels
Washington, DC 20585, 2008).

[3] V. Smil, *Energy in nature and society: general energetics of complex systems* (The MIT Press, Cambridge, Mass, 2008).

[4] L. L. Kazmerski, Journal of Electron Spectroscopy and Related Phenomena **150,** 105-135 (2006).

[5] D. A. Neamen, *Semiconductor Physics and Devices Basic Principles*, 3rd ed. (McGraw-Hill Professional, 2003).

[6] M. D. D. James D. Plummer, and Peter B. Griffin, *Silicon VLSI Technology*, US ed ed. (Prentice Hall, 2000).

[7] S. O. Kasap, *Principles of Electronic Materials and Devices*.

[8] A. J. Bard and M. A. Fox, Accounts of Chemical Research **28,** 141-145 (1995).

[9] S. M. Sze, *Physics of Semiconductor Devices*, 2nd ed. (John Wiley & Sons, Inc., 1981).

[10] M. A. Green and S. R. Wenham, Applied Physics Letters **65,** 2907-2909 (1994).

[11] B. D. S. a. N. D. Sater, IEEE Photovoltaic Specialists Conference**,** 1019-22 (2002).

[12] H. Diepers, (Siemens Aktiengesellschaft, Fed. Rep. of Germany, 1979), p. 5.

[13] L. Tsakalakos, J. Balch, J. Fronheiser, M. Y. Shih, S. F. LeBoeuf, M. Pietrzykowski, P. J. Codella, B. A. Korevaar, O. Sulima, J. Rand, A. Davuluru, and U. Rapol, **1** (2007).

[14] H. Fang, X. D. Li, S. Song, Y. Xu, and J. Zhu, Nanotechnology **19** (2008).

[15] B. M. Kayes, H. A. Atwater, and N. S. Lewis, J. Appl. Phys. **97** (2005).

[16] R. S. Wagner and W. C. Ellis, Appl. Phys. Lett. **4,** 89-& (1964).

[17] Y. Cui, X. F. Duan, J. T. Hu, and C. M. Lieber, J. Phys. Chem. B **104,** 5213-5216 (2000).

[18] T. J. Kempa, B. Z. Tian, D. R. Kim, J. S. Hu, X. L. Zheng, and C. M. Lieber, Nano Lett. **8,** 3456-3460 (2008).

[19] L. J. Lauhon, M. S. Gudiksen, C. L. Wang, and C. M. Lieber, Nature **420,** 57-61 (2002).

[20] B. Z. Tian, X. L. Zheng, T. J. Kempa, Y. Fang, N. F. Yu, G. H. Yu, J. L. Huang, and C. M. Lieber, Nature **449,** 885-U8 (2007).

[21] M. D. Kelzenberg, D. B. Turner-Evans, B. M. Kayes, M. A. Filler, M. C. Putnam, N. S. Lewis, and H. A. Atwater, Nano Lett. **8,** 710-714 (2008).

[22] L. Tsakalakos, J. Balch, J. Fronheiser, B. A. Korevaar, O. Sulima, and J. Rand, Appl. Phys. Lett. **91** (2007).

[23] T. Stelzner, M. Pietsch, G. Andra, F. Falk, E. Ose, and S. Christiansen, Nanotechnology **19** (2008).

[24] E. C. Garnett and P. D. Yang, J. Am. Chem. Soc. **130,** 9224-+ (2008).

[25] A. P. Goodey, S. M. Eichfeld, K. K. Lew, J. M. Redwing, and T. E. Mallouk, J. Am. Chem. Soc. **129,** 12344-+ (2007).

[26] J. R. Maiolo, B. M. Kayes, M. A. Filler, M. C. Putnam, M. D. Kelzenberg, H. A. Atwater, and N. S. Lewis, J. Am. Chem. Soc. **129,** 12346-+ (2007).

[27] K. Q. Peng, X. Wang, and S. T. Lee, Appl. Phys. Lett. **92** (2008).

[28] B. Tian, T. J. Kempa, and C. M. Lieber, Chem. Soc. Rev. **38,** 16-24 (2009).

[29] T. E. Bogart, S. Dey, K. K. Lew, S. E. Mohney, and J. M. Redwing, Adv. Mater. **17,** 114-+ (2005).

[30] K. K. Lew, C. Reuther, A. H. Carim, J. M. Redwing, and B. R. Martin, J. Vac. Sci. Technol. B **20,** 389-392 (2002).

[31] S. M. Eichfeld, T. T. Ho, C. M. Eichfeld, A. Cranmer, S. E. Mohney, T. S. Mayer, and J. M. Redwing, Nanotechnology **18** (2007).

Chapter 2

Literature Review

2.1 Introduction

As mentioned in the previous chapter, the goal of this research is to develop fabrication processes that are needed to create both a high efficiency and low cost radial p-n junction silicon nanowire (SiNW) solar cell. This chapter is intended to review the existing literature in order to provide a sufficient background for the experimental results provided in later chapters. The chapter starts with a section covering SiNW growth (Section 2.2), which includes several subsections that discuss the status of *in-situ* doping, and electrical and structural properties. This is followed by a discussion of studies regarding epitaxial Si regrowth (Section 2.3) and a section on literature pertaining to the fabrication of and nanowire growth on low cost glass substrates (Section 2.4). The final section will provide a summary highlighting the important points of the literature review.

2.2 CVD Growth of Silicon

Silicon nanowire arrays can be produced over large areas using chemical vapor deposition (CVD) by means of the vapor-liquid-solid (VLS) mechanism. This section reviews important work in the field of CVD of silicon starting with a brief discussion of silicon thin film deposition (section 2.2.1) followed by growth of silicon nanowires (section 2.2.2). Section 2.3 will cover the growth of SiNWs including several subsections that detail the use of silane (SiH_4)

and silicon tetrachloride ($SiCl_4$). In-situ doping of silicon nanowires will also be discussed (section 2.3.4).

2.2.1 Silicon Thin Film Growth using $SiCl_4$

Silicon tetrachloride is one of the main Si precursors used in the CVD growth of epitaxial monocrystalline Si films. Growth of epitaxial Si films is commonly carried out in a hot wall CVD reactor using $SiCl_4$. The overall reaction is reversible and can be written as:

$$SiCl_4(g) + 2H_2(g) \rightleftharpoons Si(s) + 4HCl$$

The process is typically carried out at temperatures above 900°C and at atmospheric pressure. The two parameters that have been found to be most influential in controlling the formation of single crystal films are the concentration of $SiCl_4$ and the temperature. Bloem *et al.* using a hot wall, four zone furnace observed high quality epitaxy at temperatures above 1000°C and at low $SiCl_4$ concentrations.[1] The si films grown used H_2, HCl, and $SiCl_4$ or $SiCl_3$ to obtain different Cl/H ratios at temperatures between 950-1100°C. Theuerer *et al.* determined that epitaxial films produced at low temperatures (below 1000°C) had more defects present.[2] Bylander *et al.* also used a hot wall reactor and grew films at temperatures between 950-1350°C, in both a horizontal and vertical configuration. While the uniformity and growth rates varied based on reactor design, for both reactors it was observed that the growth rate was independent of temperature at temperatures above 1050°C.[3] The results of these experiments, which were all carried out at atmospheric pressure, suggested that the supply of reactant to the growth surface is the rate limiting factor at temperatures below 1200°C, and at higher temperatures the $SiCl_4$ adsorption rate becomes the rate determining step.[1,3,4] The growth rate *versus* 1/T for silicon thin film deposition at atmospheric pressure (Figure **2-1**) determined by Jasinski shows that the growth rate is strongly dependent on temperature below 1050°C; however, at higher temperatures

the temperature dependence of growth rate is reduced, and according to some reports, the growth rate becomes independent of temperature.[5] These data suggest that the growth of Si thin films using $SiCl_4$ is kinetically limited at temperatures < 1050°C, but is mass transport limited at temperatures above 1050°C.

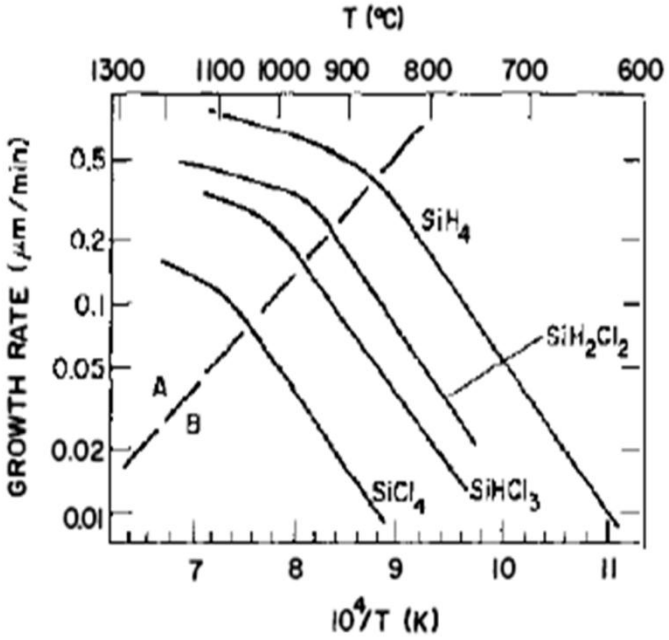


Figure **2-1**: Plot of growth rate vs 1/T for various silicon source gases under atmospheric pressure chemical vapor deposition. Region A represents mass transport limited growth and region B represents kinetically limited growth.[5]

The growth rate of silicon thin films as a function of P_{SiCl4} was also studied by Bloem *et al.*[6] using a horizontal hot wall reactor at atmospheric pressure with H_2 as the carrier gas. Figure **2-2** below shows that the growth rate increases to a maximum value and then begins to decrease with increasing P_{SiCl4}. Bylander *et al.* varied the $SiCl_4$ concentration in both vertical and horizontal geometry reactors and observed a growth rate behavior similar to that reported by Bloem.[3]

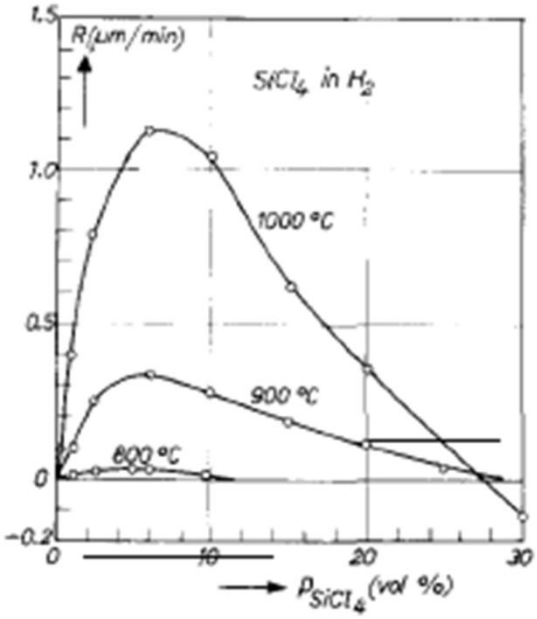


Figure **2-2**: The growth rate of silicon as a function of the input concentration of $SiCl_4$ for temperatures between 800 and 1000°C.[6]

Van Der Putte *et al.*[7] used a simple equilibrium model to predict the Si thin film growth rate as a function of P_{SiCl4} and temperature for comparison to the experimental data. This model assumes that the Si thin film deposition is limited by mass transport and that the diffusion coefficients of all gas phase species are identical. Consequently, the amount of silicon deposited on the substrate surface can be assumed to be equal to that predicted to form in the gas phase under equilibrium conditions. The gas phase concentrations were calculated at different $SiCl_4$ partial pressures at thermodynamic equilibrium. A mass balance was then used to predict the amount of solid silicon formed (growth rate) as a function of inlet $SiCl_4$ concentration at temperatures ranging from 1400-1600 K.[7] The gas phase species that were considered included Si, SiCl, $SiCl_2$, $SiCl_3$, $SiCl_4$, SiH, SiH_4, $SiHCl_3$, SiH_2Cl_2, SiH_3Cl, Cl, Cl_2, H, H_2, and HCl. The predicted Si growth rate (Si_{total}) was found by calculating the difference between the moles of silicon in the inlet gas (Si_{input}) and the moles of Si in the gas phase in its equilibrium state (Si_{eq}) at the growth temperature using the following equations:

$$Si_{input} = \frac{1}{4}\sum_{1}^{15} P_{Si_n} H_{m}{}_{Cl^l} = \frac{1}{4} Cl_{total} \quad (2.1)$$

$$Si_{eq} = \sum_{1}^{15} P_{Si_n} H_m Cl_l^n \quad (2.2)$$

$$Si_{total} = \frac{1}{4} Cl_{total} - Si_{eq} \quad (2.3)$$

Results of the prediction of the growth rate as a function of $SiCl_4$ concentration at different temperatures are shown in Figure **2-3**. The model predicts a growth rate that increases to a maximum, then decreases with increasing P_{SiCl4} for each of the included temperatures. The growth rate curves follow the same trend as the thin film results obtained experimentally, which are shown in Figure **2-2**. At higher partial pressures, an increase in the HCl concentration results in a change in the gas phase equilibrium which favors the reverse HCl etching reaction. The description of mass transfer in this diffusion controlled model (Figure **2-3**) used by Van der Putte is:

$$J = -D_i n \frac{dp_i}{dx} \quad (2.4)$$

where J is the flux of the compound over distance dx, p_i is the pressure and D_i is the diffusion coefficient at temperature T. D is related to D_O at temperature T_O using $D=D_O(T/T_O)^2$, where T_O is 273K and n is the total gas concentration (gmol/cm^3), calculated from the ideal gas law is $n=p/RT$. In this case p was considered to be 1 atm so that $n=(RT)^{-1}$. Van der Putte *et al.* also assumed a linear temperature gradient above the stagnant layer so that $T=T_s-(\Delta T/\delta)x$, where T_s is the temperature of the silicon surface, ΔT is the difference between the temperature of the silicon surface and the temperature of the gas (T_g) and δ is the thickness of the stagnant layer. The

coordinate normal to the silicon surface is x. Integrating equation 2.4 over the stagnant layer then resulted in equation 2.5:

$$J = \frac{D_O}{RT_O^2}\frac{\Delta T}{\delta}\left(P_g - P_s\right)\frac{1}{\ln\frac{T_S}{T_g}} \qquad (2.5)$$

In this case p_g is the partial pressure in the gas, where p_s is the partial pressure in equilibrium at the surface. In calculating the plots for this first model (Fig **2-3**), the gas and surface were assigned equivalent temperatures (T_s=T_g), and D_i was the same for each gas phase species.

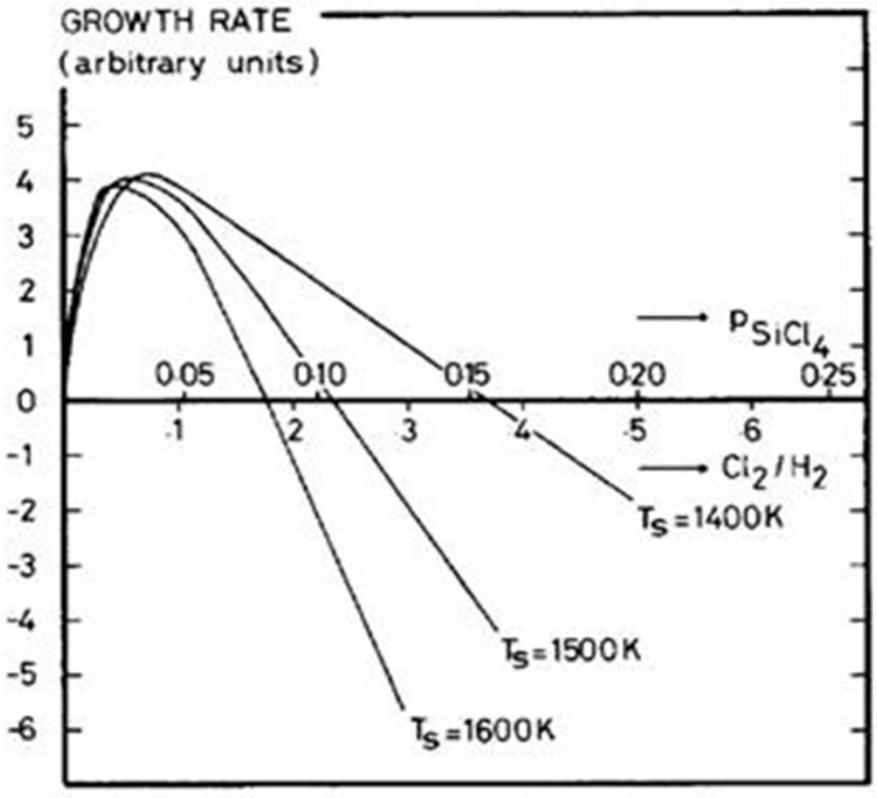


Figure **2-3**: Modeled growth/etch curves reported by Van der Putte *et al.* at different temperatures.[7]

However, the predicted transition from growth to an etching regime occurs at lower $SiCl_4$ input concentrations than was observed experimentally. A second model using equation 2.5 was then developed in which the different diffusion coefficients (D_i) were taken into account of the various compounds yielding trends similar to the experimental growth/etch curves including the transition from growth to etching regime. Despite more accurately identifying the transition point, this model, did not explain differences in experimental results reported at the same temperature by different groups which were in disagreement over where the point of zero growth rate occurred. Van der Putte *et al.* hypothesized that this may be due to a process parameter that can change from reactor to reactor.[7] A third model was therefore developed, with the assumption that this process parameter is the temperature gradient over the stagnant layer. The third model was calculated (eq. 2.5) taking into account both the different diffusion coefficients and also the effects of thermal diffusion. The assumption was made that D_i was dependent on temperature and that there is a temperature gradient across the boundary layer ($T_s \neq T_g$). This third model was found to agree very well with the experimental data and also explain the point of zero growth difference observed experimentally. Figure **2-4**, shows the growth/etch curves incorporating both the effects of thermal diffusion and also the different diffusion coefficients. This model proposes that the differences observed experimentally are due to temperature gradients, which can shift the growth/etch curve based on the particular reactor geometry.

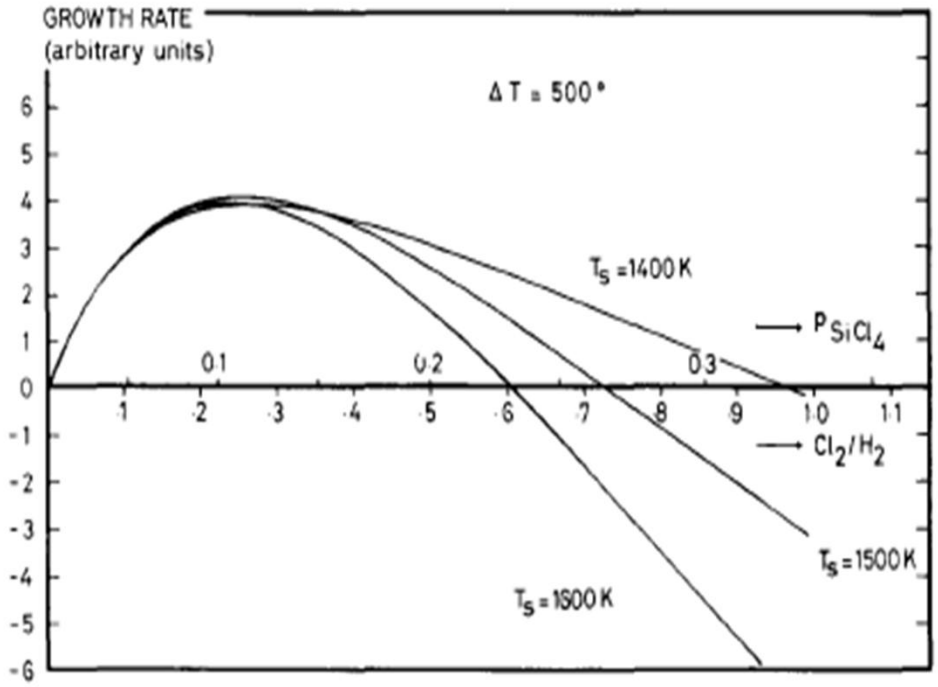


Figure **2-4**: Calculated growth/etch curves plotted as a function of the Cl_2/H_2 in the input gas using the third model proposed by Van der Putte. The curves are calculated at substrate temperatures of 1400-1600K and a temperature gradient of 500 degrees.[7]

2.2.2 Silicon Thin Film Growth with SiH_4

Silicon thin film growth using silane (SiH_4) differs from that involving $SiCl_4$. Growth from chlorine-containing species involves a reversible reaction in which kinetic competition occurs between growth and etching,[8] while growth from hydride precursors (SiH_4) primarily involves the thermal decomposition reaction:

$$SiH_4(g) \rightarrow SI(s) + 2H_2(g)$$

Deposition of the Si, which occurs by pyrolytic decomposition, can occur at temperatures as low as 600°C for polycrystalline growth and 850°C for epitaxial growth. Figure **2-1** shows the growth rate versus 1/T for both SiH_4 and $SiCl_4$. Silane has much higher growth rates in this temperature range and becomes mass transport limited sooner than $SiCl_4$. The early literature suggests that the silicon deposited from silane occurs via a single step reaction with no intermediate products, which is not the case for Si deposition using $SiCl_4$.[8]

Beers *et al.,* using a cold wall CVD reactor, grew silicon thin films using SiH_4 at atmospheric pressure and temperatures between 560-850°C.[9] In these studies, the films were amorphous silicon at temperatures below 650°C and polycrystalline at temperatures above 650°C. The growth rate was found to be strongly dependent on temperature, indicating a kinetically controlled regime. The activation energy (E_A) was calculated to be 51 kcal/mol for amorphous Si films and 38 kcal/mol for polycrystalline Si thin films grown above 650°C. Experiments performed by Bloem and Giling determined that the deposition rate is proportional to the P_{SiH4}, which is different from the increase and decrease in growth rate observed with increasing P_{SiCl4}.[8] The growth of Si thin films using 1% SiH_4 in N_2, 5% SiH_4 in H_2 and pure SiH_4 was carried out using a hot wall LPCVD system by Classen *et al.*[10] Several Si wafers were placed along the length of the reactor hot zone, and growths at temperatures between 550-850°C were studied. The growth rate using 1% SiH_4 in N_2 was higher than that of pure silane and 5% SiH_4 in H_2. It was found that at higher temperatures (>650°C) the Si growth rate dropped off due to depletion of the SiH_4.

The effect of growth rate on the incorporation of dopants was also studied by Baliga.[8] At low growth rates, there was no significant change in the incorporation of PH_3 for a fixed PH_3/SiH_4 ratio. However, at high growth rates the dopant concentration incorporated in the layer was found to decrease. A reduction in the silicon growth rate was also found to occur with increasing PH_3/SiH_4 ratios for growth with SiH_4.[11,12] It was suggested that the decrease in growth

rate with higher doping concentrations occurs due to the preferential adsorption of the group V hydrides (PH_3 and AsH_3) that can poison the surface for further adsorption of the Si.

2.3 Silicon Nanowire Growth

This section begins by describing the vapor-liquid-solid mechanism commonly used for SiNW growth. This is followed by an in-depth discussion of silicon nanowire growth using $SiCl_4$, since this was the primary silicon precursor used to produce oriented SiNW arrays in this study. A brief discussion of SiNW growth using SiH_4 is also presented as this was the Si precursor used to grow SiNWs in the anodized aluminum oxide (AAO) templates. Finally, a review of in-situ doping of silicon nanowires will be presented.

2.3.1 Vapor-Liquid-Solid Mechanism

The growth of Si whiskers using $SiCl_4$ was first reported in 1964 by Wagner and Ellis.[13] This was the first report of growth via a vapor-liquid-solid mechanism (VLS). They were able to grow large (1-10μm) diameter Si whiskers on Si (111) substrates with Au droplets at 950°C using H_2 reduction of $SiCl_4$.In VLS growth, the Au droplet forms a liquid alloy with Si above the Au-Si eutectic temperature (~360°C). As the Si precursor continues to be introduced, the Au-Si alloy becomes supersaturated and solid silicon precipitates out to form a Si whisker. Figure **2-5** is a schematic showing the nucleation of a nanowire using a metal catalyst.

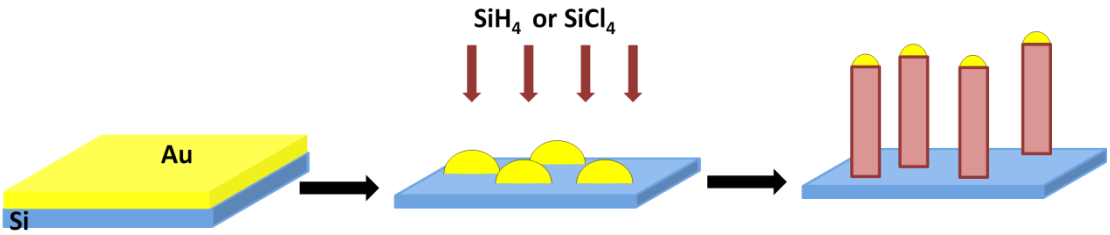


Figure **2-5**: Schematic of vapor-liquid-solid mechanism for SiNW growth.

2.3.2 SiNW Growth using $SiCl_4$

A range of temperatures (950-1200°C) have been reported for Si whisker growth using $SiCl_4$. Attempts to grow epitaxial Si whiskers were carried out at all these temperatures using $SiCl_4$ concentrations from 0.01 to 4%.[13-16] The VLS mechanism also confirmed by James and Lewis [17] who determined that the wires were growing epitaxially. In these early studies, the Si whiskers had large diameters (> 0.5 µm). Wagner *et al.* observed that etching of the Si substrate may occur even at low $SiCl_4$ concentration and that any temperature gradient across the droplet can lead to degradation of growth by creating a destabilization of the metal-Si liquid alloy.[16] Givargizov reported that the whiskers become heavily tapered above 1060°C, and that as the $SiCl_4$ concentration is increased, the Si whisker diameter decreases.[18]

Following a resurgence of research on nanotechnology, there has been a renewed interest in the growth of Si whiskers using $SiCl_4$, but with much smaller diameters than the prior work. Zhang *et al.* used high $SiCl_4$ concentrations (5-7 mol %) in an attempt to grow wires using a Ni catalyst. The SiNWs were not epitaxial, but were single crystal exhibiting an amorphous shell, possessing diameters of 50-500 nm. Higher reaction temperatures yielded larger diameter SiNWs. They also observed that at temperatures below 900°C, no SiNW growth was present. [19] Mao *et al.*, using Au for the catalyst, examined $SiCl_4$ concentrations from 0.01 to 1 mol % and observed

that nanowires only grew at low $SiCl_4$ concentrations (<1%). These SiNWs had very low growth rates (<6nm/min) and the nanowire diameter was approximately 75nm.[20] Mao was also unable to obtain epitaxial SiNWs.

Since then other groups have been able to obtain epitaxial SiNWs via $SiCl_4$. Hochbaum *et al.* were able to obtain epitaxial SiNWs on (111) Si substrates with diameters ranging from 40-100 nm using Au nanoparticles at low temperatures (800-850°C).[21] This is the first report of growth at a temperature below 900°C. It is notable that they used 10% H_2 in Ar as a carrier gas instead of pure H_2, which is what has been reported as the carrier gas by other groups. Recently, Kayes *et al.* grew larger diameter epitaxial SiNWs on patterned Si substrates, at low $SiCl_4$ concentrations and temperatures from 850-1100°C with H_2 as the carrier gas.[22] The nanowire diameter was approximately 1.5 μm. Optimal growth was observed at higher temperatures between 1000 and 1050°C; below that temperature range no SiNWs were observed to grow straight or normal to the surface. At temperatures above 1050°C, the oxide used to keep the Au pattern from migrating began to break down. Recent studies of Si nanowire growth using $SiCl_4$ suggest that the optimum temperature for epitaxial growth on Si (111) increases with increasing nanowire diameter.

It has also been reported in the literature that the temperature of VLS growth has an impact on the whisker/wire morphology.[14-16,18,23] As growth temperature is increased, periodic instabilities tend to develop, and that as temperature is reduced, the SiNW diameter can decrease. Wagner has shown that wires grown at higher temperatures (above 950°C) yield a hexagonal cross-section while at lower temperatures the cross-section becomes twelve sided by the formation of six {110} faces.[15] Wagner proposed that this is due to surface tension at the liquid-solid interface changing with deposition temperature and making different facets more kinetically favorable. The development of lateral faces was further studied by Nebol'sin *et al.* who concluded that at higher temperatures, the contact angle decreases allowing for the formation of

stepped {211} faces and periodic elevations on the lateral surface. [23] A small length of the nanowires near the Au tip was observed to not have faceting, and is attributed to that section being recrystallized silicon that has precipitated out of the liquid droplet upon reduction of growth temperature (Figure **2-6**).[24]

Figure **2-6**: Disappearance of faceting upon deposition of recrystallized silicon layer from the liquid droplet.[24]

2.3.3 Growth Mechanism Diameter Dependence

Givargizov summarized the VLS growth process in four steps.[18] Figure **2-7** shows a schematic that depicts the four main steps of the VLS process. The four steps are:

1.) Mass transport of the Si precursor in the gas phase.

2.) Chemical reaction of Si precursor on the vapor-liquid interface.

3.) Diffusion of the Si through the droplet.

4.) Crystallization step in which the Si precipitates out into a solid at the solid- liquid interface.

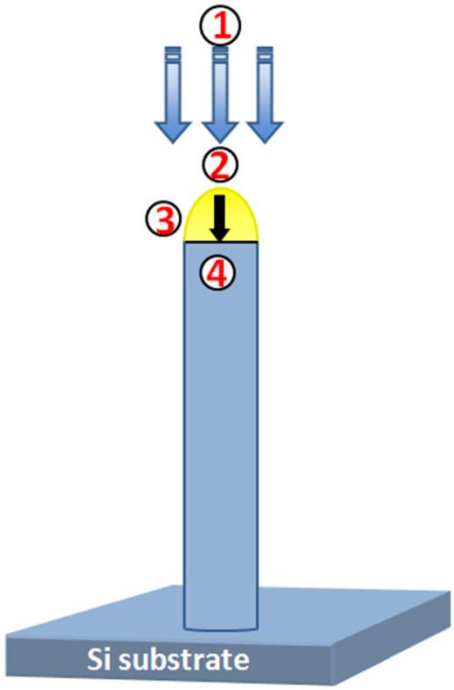


Figure **2-7**: Schematic showing steps of VLS process.

There has been some discussion as to which is the rate-limiting step. It has been determined that the diffusion of the Si through the droplet (step 3) can be ruled out since Si diffusion through a liquid droplet is too fast as to be rate determining.[18] The diffusion in liquid metals occurs very quickly. Furthermore, the activation energy in a liquid metal is typically 1-4 kcal/mol, which is low compared to the activation energy (22 kcal/mol) reported for SiNW growth with SiH_4.[25] While the diffusion coefficient of Si in the Au-Si liquid phase is not available, Lew *et al*. used the self-diffusion coefficient of Si in liquid Si to estimate the diffusion time of Si over a distance of 0.24 μm.[25] The diffusion time was estimated to be 1μs at 500°C.

Bootsma *et al.* and Lew *et al.* suggested that the incorporation step (step 2), the precursor gas decomposition at the vapor-liquid interface, was rate-determining due to the growth velocity dependence on parital pressure.[25,26] Givargizov, however, argued that the crystallization step (step 4) was the rate-determining step due to the growth rate dependence on diameter.[18] Schmidt *et al.* proposed that there is not one single rate-limiting step, but rather that a combination of both the incorporation and crystallization steps are rate-limiting,[27]

The growth rate dependence on diameter observed by Givargizov is in agreement with the Gibbs-Thomson effect, which as described by Givargizov[18] for VLS growth arises from the change in chemical potential with particle size according to:

$$\Delta\mu = \Delta\mu_0 - \frac{4\Omega\alpha_{vs}}{d} \tag{2.6}$$

where $\Delta\mu$ is the chemical potential difference of an adatom in the vapor and solid phases, $\Delta\mu_o$ is the chemical potential difference at a flat interface, Ω is the atomic volume of the adatom, α_{vs} is the free energy of the solid surface, and d is the nanowire diameter. As the nanowire diameter decreases, the vapor pressure increases and solubility of Si in the catalyst decreases, which leads to a decrease in supersaturation and driving force for growth. If the Gibbs-Thomson effect holds, then the nanowire growth rate would be expected to decrease as nanowire diameter decreases. Givargizov reported an increase in growth rate with increasing diameter, which is consistent with the Gibbs-Thomson relation.[18] However, contradictory behavior was observed by Weyher and Nebol'sin who reported a decrease in growth rate of SiNWs grown using $SiCl_4$ with increasing diameter.[23,28] This does not follow the Gibbs-Thomson relation and also shows that the growth process is likely more complex than initially thought.

Givargizov *et al.* also observed that at 1000°C and atmospheric pressure, as the $SiCl_4$ concentration increases the growth rate also increases.[14] Under these conditions, the growth rate

also increased with increasing diameter. The dependency of increasing growth rate with increasing NW diameter was similar for several different catalysts (Au, Pd, Ni, and Pt) (Figure **2-8(a)**. The equation used by Givargizov to describe the growth rate is included below as equation 2.7. In this equation V is the growth velocity, $\Delta\mu_O$ is the change in chemical potential, T is the temperature and d is the nanowire diameter. The specific free energy of the nanowire surface is defined by α, while Ω is the atomic volume of Si. In this case b is a coefficient independent of supersaturation.

$$V^{\frac{1}{n}} = \frac{\Delta\mu_o}{kT} b^{\frac{1}{n}} - \frac{4\Omega\alpha}{kT} b^{\frac{1}{n}} \frac{1}{d} \tag{2.7}$$

Weyher *et al.* observed the opposite dependency of growth rate versus nanowire diameter, where the growth rate decreases with increasing $SiCl_4$ concentration (Figure **2-8(b)**. These whiskers were grown at temperatures between 1000-1100°C using a Pt catalyst at atmospheric pressure.[29] Nebol'sin *et al.* also saw the same dependency as Weyher using a Au catalyst at 1000-1100°C.[24] The growth rate was again observed to decrease with increasing $SiCl_4$.

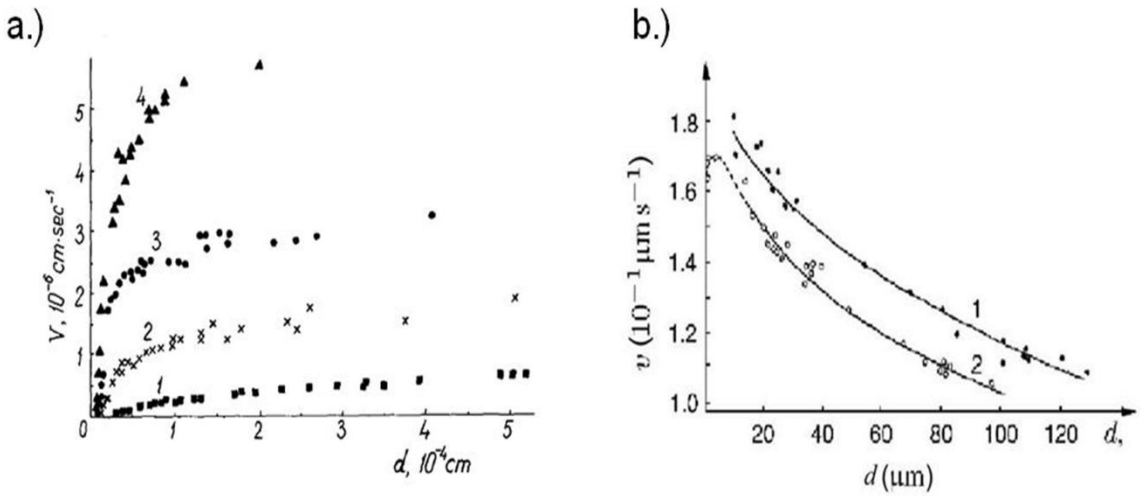


Figure **2-8**: Opposing diameter dependencies on the SiNW growth rate (V) by a.) Givargizov[18], and b.) Weyher.[29]

Schmidt *et al.* developed an empirical model in an attempt to explain the opposing partial pressure and diameter dependencies.[27] The model proposed that the diameter dependency on growth rate is a function of interplay between the rate of change of Si incorporation at the catalyst surface and the silicon crystallization at the liquid-solid interface with respect to supersaturation. The model assumes that growth proceeds via the VLS mechanism and Si is supplied directly to the droplet. The surface diffusion of the Si is neglected, and the diffusion of silicon through the droplet was assumed to be fast. For simplification, the crystallization velocity (ω) was assumed to be a monotonically increasing function of the chemical potential difference between the liquid catalyst and solid nanowire (μ_{ls}) and the incorporation velocity (α), is a monotonically increasing function of the chemical potential difference between the vapor phase and liquid catalyst (μ_{vl}). The chemical potential difference between the vapor phase and liquid catalyst (μ_{vl}) was expressed in terms of μ_{ls} using the identity $-\mu^{vl}=\mu^{ls}-\xi$, where ξ is the chemical potential difference between the vapor phase (μ_v) and the nanowire solid phase (μ_s). The crystallization velocity (ω) and incorporation velocity (α) are plotted as a function of supersaturation, Figure **2-9**.

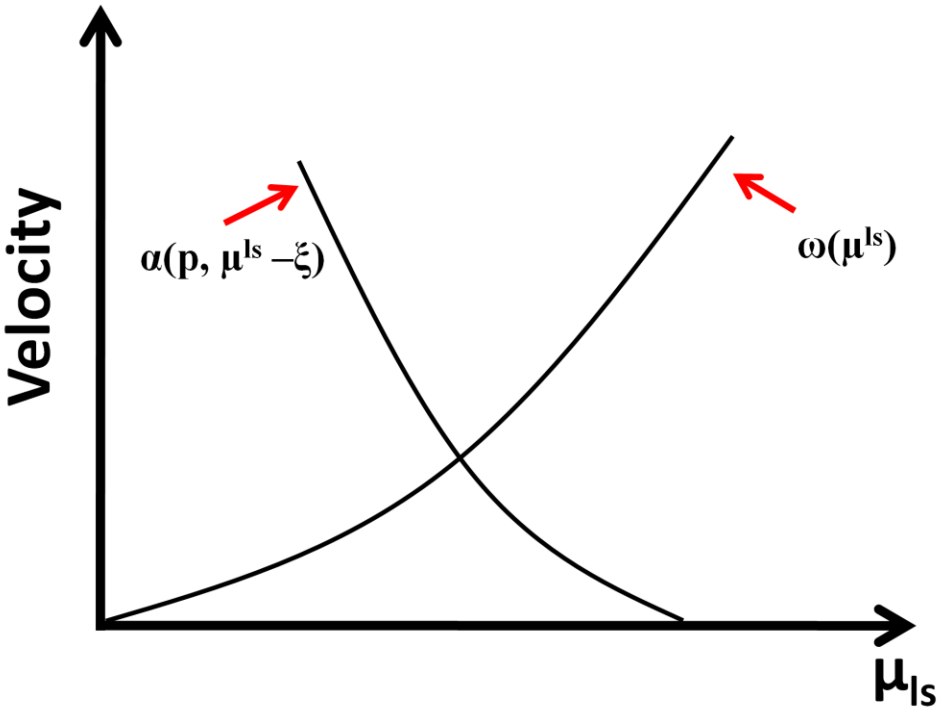


Figure **2-9**: Schematic of the incorporation velocity α and crystallization velocity $\omega(\mu^{ls})$ as a function of the droplet supersaturation μ_{ls}.[27]

In the plot, the α curve is flipped with respect to the vertical axis because of $\mu_{ls}<0$. Based on the Gibbs-Thomson effect, both the steady state supersaturation and steady state growth velocity become dependent on the nanowire radius. The diameter dependence then depends on the respective signs and magnitudes of the slopes α_1 and ω_1. The growth rate can be written as:

$$\boldsymbol{v} = \boldsymbol{v_0} + \Gamma \frac{\mathbf{2}\Omega^s \sigma^s}{\boldsymbol{r}} \tag{2.8}$$

where v_o is the growth rate as r approaches ∞, Ω^s is the atomic volume of the SiNWs, and σ^s is the specific free energy of the nanowire surface at the vapor-solid interface. Γ is given by:

$$\Gamma = \frac{\omega_1 \alpha_1}{\omega_1 - \alpha_1} \tag{2.9}$$

where ω_1 is the rate of change of the crystallization velocity (ω) with the supersaturation (μ_{ls}) and α_1 is the rate of change of the incorporation velocity with the supersaturation (μ_{ls})[27].

Assuming that the crystallization velocity ω has a positive slope, there are 2 possible cases to be considered. The first case is when $\alpha_1<0$, and Γ is negative. The growth rate increases with increasing radius and corresponds to the experimentally observed behavior shown in Figure **2-8** (a). The second case is when $\omega_1>\alpha_1>0$, causing Γ to become positive. The growth velocity would then decrease with increasing nanowire radius, which supports the experimental results obtained by Nebol'sin and Weyher.

2.3.4 SiNW Growth using SiH_4

One goal of this project is to obtain growth of nanowire arrays on low cost substrates such as glass. Depending on the composition, glass can soften or melt at temperatures between 600-1000 °C.[30] Since SiNW growth using $SiCl_4$ occurs at higher temperatures (>800 °C), SiH_4 must be used as a Si precursor gas. Since there have been numerous studies of SiNW growth using SiH_4, only a brief section covering the most relevant studies will be discussed. A detailed discussion of nanowire growth using SiH_4 can be found in Dr. K.K. Lew's thesis.[31]

SiNW growth using SiH_4 also occurs via the VLS mechanism. Above the Au-Si eutectic temperature of 363 °C, Au catalyzes the decomposition of SiH_4. Growth of SiNWs using SiH_4 as

the Si gas precursor has been achieved at lower temperatures, between 320-600°C and low pressures.[32] As the P_{SiH4} is increased, the growth rate linearly increases. Lew *et al.* reports an Arrhenius relation at temperatures between 400-500°C for SiNWs grown using SiH_4 in a AAO template, with an activation energy of 22 kcal/mol.[25] The growth rate was found to linearly increase with time at a P_{SiH4} of 0.65 Torr.

2.3.5 In-Situ Doping of SiNWs

The ability to precisely control the doping level and also dopant type (n or p) in nanowires is crucial for the fabrication of nanowire devices. In-situ doping of nanowires can be carried out through the addition of gas precursors of n- or p-type dopants along with SiH_4 or $SiCl_4$. For SiNWs grown using SiH_4, phosphine (PH_3) and diborane B_2H_6 are typically used as the n- and p-type dopant gases respectively. Cui *et al.* first reported successful in-situ doping of VLS grown SiNWs.[33] Transmission electron microscope (TEM) images revealed that the doped SiNWs were single crystal. Pan *et al.* reported poor crystalline quality and thick amorphous shells at high B_2H_6/SiH_4 ratios.[34] At high B_2H_6/SiH_4 ratios, the Au tip is continuously lost along the growing SiNWs. It was proposed by Pan *et al.* that enhanced Si deposition rate caused by high B_2H_6 incorporation could cause instability in the liquid/solid interface, leading to precipitation of Au nanoparticles. Subsequently, Lew *et al.* reported successful p-type SiNW growth using trimethylboron (TMB) instead of B_2H_6.[35] Back gated measurements revealed p-type conductivity and 4 point electrical measurements revealed the ability to control the resistivity by changing the TMB/SiH_4 ratio. Wang *et al.* demonstrated n-type conductivity and the ability to change the nanowire resistivity.[36] These nanowires were grown with a Au catalyst via a VLS mechanism. The growth temperature and pressure were 500 °C and 13 Torr respectively. The nanowires were doped in-situ using SiH_4 and PH_3 as the silicon and n-type precursors. By increasing the

dopant/SiH_4 ratios, the nanowire resistivity was found to decrease. [35,36] This parameter adjustment allows for the controlled growth and doping of SiNWs.

Controlled doping (p-type and n-type) of SiNWs grown via $SiCl_4$ has not been studied in detail. The addition of dopants during Si whisker growth using $SiCl_4$ was first reported by Wagner *et al.* In this case, small amounts of PCl_3 were added at certain times during growth to serve as a marker. [15] Characterization of the wires was then performed to observe potential branching and kinking.[37] Other dopant sources ($AsCl_3$ and BBr_3) were added to study the effect of impurities on wire morphology. The first and only report to date of p-type doping of $SiCl_4$-grown epitaxial SiNWs using boron tribromide (BBr_3) was for use in creation of a vertical SiNW field effect transistor (FET).[38] No details on the growth conditions were reported, although the wires were grown with 50nm Au colloids. To date there have been no systematic studies of the effect of doping on the structural and electrical properties of SiNWs grown using $SiCl_4$.

2.4 Epitaxial Regrowth

The final step in realization of a p-n junction SiNW array involves the epitaxial regrowth of n-type Si on p-type SiNWs. If the coating is polycrystalline, the grain boundaries at the p-n junction interface could lead to carrier recombination and a decrease in device efficiency. A single crystal coating would therefore be preferred. There have been reports of core-shell nanowires using different materials for the core and shell.[39-42] The first report both for silicon and Ge core/shell nanowires grown by CVD on the wires was by Lauhon *et al.*[42] Undoped silicon nanowires were grown, and then through changes in the growth conditions a radial p-type Si shell was deposited. The shell was initially amorphous, however, it was successfully recrystallized following annealing at 600°C for 30 minutes. The Au tips were not removed prior to radial deposition. Tian *et al.* have recently demonstrated radial p-n junction SiNWs grown using SiH_4

as the Si precursor.[43] In this paper, successful coating of p-type SiNWs was demonstrated. However, the n-type shell was polycrystalline. The n-type shell layer was deposited at a pressure of 25 Torr and a temperature of 650°C, using 0.15 sccm SiH_4 and 0.75 sccm PH_3. The catalyst used for p-type nanowire growth was not removed prior to shell deposition, which could lead to problems with device performance. Using a two-step CVD process, Dong *et al.*[44] grew a radial amorphous Si shell on single crystal silicon nanowires using conditions similar to those employed by Lauhon *et al.*[42] Garnett *et al.* used disilane to radially coat n-type SiNWs that were created via etching.[45] The initial coating was amorphous and then recrystallized at a higher temperature. TEM revealed the crystallized shell was polycrystalline. To date there have been no reports of single crystal radial Si shell deposition.

2.5 Silicon Nanowire Arrays Grown on Templated Glass

While high quality SiNW arrays on Si (111) are of interest for prototype devices, the ultimate goal is to produce radial p-n junction SiNW arrays on a lower cost substrate such as glass. One challenge involves growing high quality single crystal nanowire arrays on glass. In order to control diameter and ordering of the nanowires, an AAO template fabricated on ITO coated glass was used. The following section discusses the relevant literature on templated glass substrates, and also SiNW growth in AAO templates.

2.5.1 Si Nanowire Growth in Anodized Alumina Templates

Single crystal SiNWs have been successfully grown using non-crystalline substrates such as anodized alumina templates.[25,46] Bogart *et al.* was able to fabricate ordered arrays of AAO templates between 45-200 nm from Al foil.[46] The pore diameter varied linearly with anodization

voltage. Lew *et al.* synthesized SiNWs both inside the pores and outside the surface of the AAO templates using 10% SiH_4 as the source gas.[25] Templated nanowire growth allows for diameter control of the nanowires, and the template also provides a support structure for the nanowires. Growth was carried out using a 10% SiH_4 in H_2 mixture at temperatures between 400-500°C. Thin film deposition was observed at temperatures above 500°C. TEM on these SiNWs showed that the wires were single crystal. While CVD growth of nanowires using free-standing AAO templates has advantages, the templates can be fragile and difficult to handle. This leads to the use of AAO templates on more rigid substrates.

Shimizu *et al.* successfully fabricated an AAO template on a Si(100) substrate in order to grow epitaxial (100) SiNWs.[47] Aluminum was e-beam evaporated (~200 nm) onto a Si(100) substrate and anodized using oxalic acid at 40V. This left a thin Al barrier layer between the substrate and AAO that was removed using chemical dissolution in phosphoric acid. In order to produce epitaxial nanowires, there must be a clean Si surface (no oxide) present, so an HF dip was performed to remove any SiO_2 present[47]. After Au electrodeposition in the pores, epitaxial SiNWs were successfully grown using 5% SiH_4 in Ar. To date most of these samples have been small in area, which limits the overall scalability of creating low cost substrates.

2.6 Literature Review Summary

Chapter 2 of this thesis was intended to review the relevant literature pertaining to the growth of large area ordered radial p-n junction SiNW arrays. The large amount of information that was presented, including nanowire solar cells, growth of silicon nanowires, and also substrates could potentially be useful to those reading this thesis. This section provides a concise overview of the important points discussed from this published work.

SiNWs are grown via a VLS mechanism using Au as the metal catalyst.[13] Growth can be carried out using $SiCl_4$ at higher temperatures, and the optimum temperature for epitaxial growth on Si (111) increases with increasing nanowire diameter.[18-20,22] Givargizov *et al.* reports an increase in growth rate with increasing diameter consistent with the Gibbs-Thomson effect[14], while contradictory behavior was observed by Weyher and Nebol'sin.[24,29] The effect of growth conditions on the structural and electrical properties of SiNWs grown using $SiCl_4$ have not been examined in detail.

Silicon nanowire growth can also be achieved using SiH_4 as the precursor. It is more difficult to grow wires epitaxially, but nanowire growth is found to occur at lower temperatures (320-600°C).[32] There have been several studies on the doping of nanowires grown using SiH_4.[34-36,48] Phosphine (PH_3) is a common n-type dopant and increased PH_3/SiH_4 ratios lead to a decrease in resistivity.[36] Diborane (B_2H_6) and TMB have been used as p-type dopants and also lead to a decrease in resistivity with increasing dopant/SiH_4 ratio.[34,35] However, Pan *et al.* showed that high B_2H_6/SiH_4 ratios lead to poor crystallinity and thick amorphous shells on the nanowires.[34] Growth of silicon nanowire arrays on AAO templated glass have not been reported.

There have been successful reports of core/shell nanowire structures. Lauhon *et al.* successfully deposited an amorphous p-type shell and through annealing recrystallized the shell into single crystal.[42] Growth can be controlled to create a radial deposition on the nanowire by using higher temperatures and lower pressures than growth. Tian *et al.* were able to create a radial p-n junction SiNW through the same technique as Lauhon.[42,43] The n-type shell was determined to be polycrystalline. To date there have been no reports of epitaxial regrowth of n-type Si shells.

2.7 References

[1] J. Bloem, Y. S. Oei, H. H. C. Demoor, J. H. L. Hanssen, and L. J. Giling, J. Cryst. Growth **65,** 399-405 (1983).

[2] H. C. Theuerer, J. Electrochem. Soc. **108,** 649-653 (1961).

[3] E. G. Bylander, J. Electrochem. Soc. **109,** 1171-1175 (1962).

[4] J. Bloem, Y. S. Oei, H. H. C. Demoor, J. H. L. Hanssen, and L. J. Giling, J. Electrochem. Soc. **132,** 1973-1980 (1985).

[5] J. M. Jasinski, B. S. Meyerson, and B. A. Scott, Annu. Rev. Phys. Chem. **38,** 109-140 (1987).

[6] J. Bloem, W. A. P. Claassen, and W. Valkenburg, J. Cryst. Growth **57,** 177-184 (1982).

[7] P. Vanderputte, L. J. Giling, and J. Bloem, J. Cryst. Growth **31,** 299-307 (1975).

[8] *Epitaxial Silicon Technology*; *Vol.*, edited by B. J. Baliga (Academic Press. Inc., Orlando, FL, 1986).

[9] A. M. Beers and J. Bloem, Applied Physics Letters **41,** 153-155 (1982).

[10] W. A. P. Claassen, J. Bloem, W. Valkenburg, and C. H. J. Vandenbrekel, Journal of Crystal Growth **57,** 259-266 (1982).

[11] P. D. Agnello, T. O. Sedgwick, and J. Cotte, J. Electrochem. Soc. **140,** 2703-2709 (1993).

[12] R. F. C. Farrow and J. D. Filby, J. Electrochem. Soc. **118,** 149-& (1971).

[13] R. S. Wagner and W. C. Ellis, Appl. Phys. Lett. **4,** 89-& (1964).

[14] Givargiz.Ei and N. N. Sheftal, J. Cryst. Growth **9,** 326-& (1971).

[15] R. S. Wagner, J. Appl. Phys. **38,** 1554-& (1967).

[16] R. S. Wagner and C. J. Doherty, J. Electrochem. Soc. **113,** 1300-& (1966).

[17] D. W. F. James and C. Lewis, British J. of Apl. Phys. **16,** 1089-& (1965).

[18] E. I. Givargizov, J. Cryst. Growth **31,** 20-30 (1975).

[19] Y. J. Zhang, Q. Zhang, N. L. Wang, Y. J. Yan, H. H. Zhou, and J. Zhu, J. Cryst. Growth **226,** 185-191 (2001).

[20] A. Mao, H. T. Ng, P. Nguyen, M. McNeil, and M. Meyyappan, J. Nanosci. Nanotechnol. **5,** 831-835 (2005).

[21] A. I. Hochbaum, R. Fan, R. R. He, and P. D. Yang, Nano Lett. **5,** 457-460 (2005).

[22] B. M. Kayes, M. A. Filler, M. C. Putnam, M. D. Kelzenberg, N. S. Lewis, and H. A. Atwater, Appl. Phys. Lett. **91** (2007).

[23] V. A. Nebol'sin, A. A. Shchetinin, A. A. Dolgachev, and V. V. Korneeva, Inorg. Mater. **41,** 1256-1259 (2005).

[24] V. A. Nebol'sin, A. A. Shchetinin, A. N. Korneeva, A. I. Dunaev, A. A. Dolgachev, T. I. Sushko, and A. F. Tatarenkov, Inorg. Mater. **42,** 339-345 (2006).

[25] K. K. Lew and J. M. Redwing, J. Cryst. Growth **254,** 14-22 (2003).

[26] G. A. Bootsma and H. J. Gassen, J. Cryst. Growth **10,** 223-& (1971).

[27] V. Schmidt, S. Senz, and U. Gosele, Phys. Rev. B **75** (2007).

[28] J. Weyher, Materials Science and Engineering **20,** 171-177 (1975).

[29] J. Weyher, J. Cryst. Growth **43,** 235-244 (1978).

[30] *CRC Handbook of Chemistry and Physics 89th ed.*

[31] K.-K. Lew, (2005).

[32] J. Westwater, D. P. Gosain, S. Tomiya, S. Usui, and H. Ruda, J. Vac. Sci. Technol. B **15,** 554-557 (1997).

[33] Y. Cui, X. F. Duan, J. T. Hu, and C. M. Lieber, J. Phys. Chem. B **104,** 5213-5216 (2000).

[34] L. Pan, K. K. Lew, J. M. Redwing, and E. C. Dickey, J. Cryst. Growth **277,** 428-436 (2005).

[35] K. K. Lew, L. Pan, T. E. Bogart, S. M. Dilts, E. C. Dickey, J. M. Redwing, Y. F. Wang, M. Cabassi, T. S. Mayer, and S. W. Novak, Appl. Phys. Lett. **85,** 3101-3103 (2004).
[36] Y. F. Wang, K. K. Lew, T. T. Ho, L. Pan, S. W. Novak, E. C. Dickey, J. M. Redwing, and T. S. Mayer, Nano Lett. **5,** 2139-2143 (2005).
[37] R. S. Wagner, J. Phys. Chem. Solids**,** 347-& (1967).
[38] J. Goldberger, A. I. Hochbaum, R. Fan, and P. D. Yang, Nano Lett. **6,** 973-977 (2006).
[39] I. A. Goldthorpe, A. F. Marshall, and P. C. McIntyre, Nano Lett. **8,** 4081-4086 (2008).
[40] H. W. Kim and S. H. Shim, Adv. Eng. Mater. **9,** 92-95 (2007).
[41] J. A. Czaban, D. A. Thompson, and R. R. LaPierre, Nano Lett. **9,** 148-154 (2009).
[42] L. J. Lauhon, M. S. Gudiksen, C. L. Wang, and C. M. Lieber, Nature **420,** 57-61 (2002).
[43] B. Z. Tian, X. L. Zheng, T. J. Kempa, Y. Fang, N. F. Yu, G. H. Yu, J. L. Huang, and C. M. Lieber, Nature **449,** 885-U8 (2007).
[44] Y. J. Dong, G. H. Yu, M. C. McAlpine, W. Lu, and C. M. Lieber, Nano Lett. **8,** 386-391 (2008).
[45] E. C. Garnett and P. D. Yang, J. Am. Chem. Soc. **130,** 9224-+ (2008).
[46] T. E. Bogart, S. Dey, K. K. Lew, S. E. Mohney, and J. M. Redwing, Adv. Mater. **17,** 114-+ (2005).
[47] T. Shimizu, T. Xie, J. Nishikawa, S. Shingubara, S. Senz, and U. Gosele, Adv. Mater. **19,** 917-+ (2007).
[48] A. J. Learn and D. W. Foster, J. Appl. Phys. **61,** 1898-1904 (1987).

Chapter 3

Experimental Methodology

3.1 Introduction

In order to fabricate and grow silicon nanowire arrays for the eventual use as solar cell devices there were several systems and techniques employed. This chapter describes the substrate preparation for both AAO templated structures and silicon wafers. This will be followed by a discussion on the redesign of an atmospheric pressure group IV CVD system located in the Hosler building to accommodate growth using a liquid silicon tetrachloride ($SiCl_4$) source. A low pressure group IV reactor originally built by Dr. Kok-Keong Lew will be briefly described for its use in growth of SiNWs in AAO templates and n-type regrowth; detailed information on this system can be found in Dr. Lew's thesis.[1] Finally characterization techniques used to evaluate the nanowire and thin film deposition will be described.

3.2 Substrate Preparation

This section will discuss the two main types of substrates used for the growth of silicon nanowires in these studies. The first will be the anodized alumina membranes (AAO). The second substrate used in these studies is Si(111).

3.2.1 Electrodeposition of Au in AAO Membranes

Electrodeposition of Au and other contact metals was carried out for the VLS growth of SiNWs in AAO membranes. The template for vapor-liquid solid growth was prepared by using commercially available AAO membranes. These were purchased from Whatman Scientific, and had a pore diameter of 200 nm and a thickness of 60 microns. The process for membrane preparation is shown in Figure **3-1**. A thin (100 nm) layer of silver was evaporated onto the branched side of the membrane. The membranes are typically fabricated through anodization of an Al film using oxalic acid.[2] When this is carried out the pores are formed through most of the Al film but can leave smaller diameter "branched" pores near the one surface. The branched side of the membrane can be difficult for SiNW growth. The layer of silver deposited on the branched side of the membrane is then used as a conductive layer for electrodeposition in the pores and later as a backside electrical contact. Silver, cobalt, and gold were then electrodeposited into the membrane respectively.

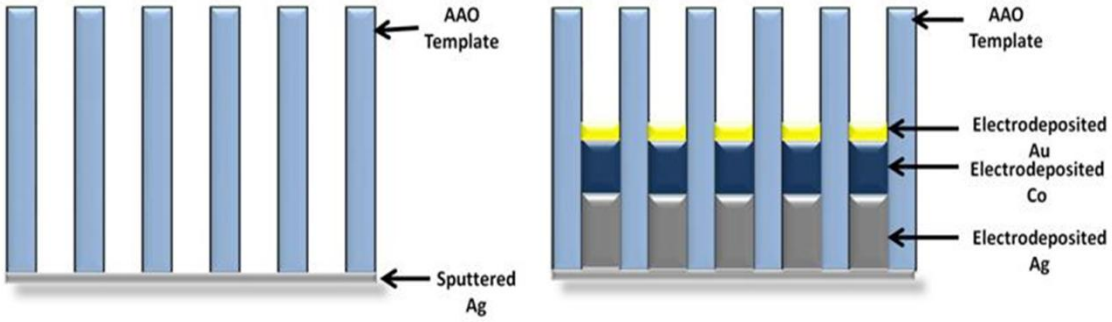


Figure **3-1**: Schematic demonstrating the electrodeposition of metals into a free standing AAO membrane.

Electrodeposition was performed using an electrochemical cell and a potentiostat. Further details on the set-up of electrodeposition can be found in Tim Bogart's thesis.[3] Current controlled deposition described by Martin *et al*.[4] was done to deposit the Ag. The potassium silver cyanide

and the potassium gold cyanide solutions, the silver and gold plating solutions, respectively, were purchased from Technic Inc. The silver was deposited at 0.575 A, and served as a filler to control the placement of the cobalt and gold in the membrane. The length of the silver segment dictated the length of the silicon nanowires inside of the membrane. Cobalt was then deposited on top of the silver layer using the process described by Mohammed *et al*.[5] The cobalt solution was prepared by mixing 500 g/L of cobalt sulfate, 17 g/L sodium chloride, and 45 g/L of boric acid. The plating current for the cobalt solution was 0.7 A. Mohammed *et al*. used electrodeposited cobalt segments in the AAO membrane to contact the grown silicon nanowires. During the VLS growth process, the cobalt reacts with the silicon nanowire to form a cobalt silicide. For these experiments, a cobalt calibration curve was created to determine the rate of cobalt deposition. The electrodeposition rates for Au and Ag were calculated and used from previous thesis experiments. This curve can be seen in Figure **3-2** below. The cobalt deposition rate measured was approximately 0.3 μm/min.

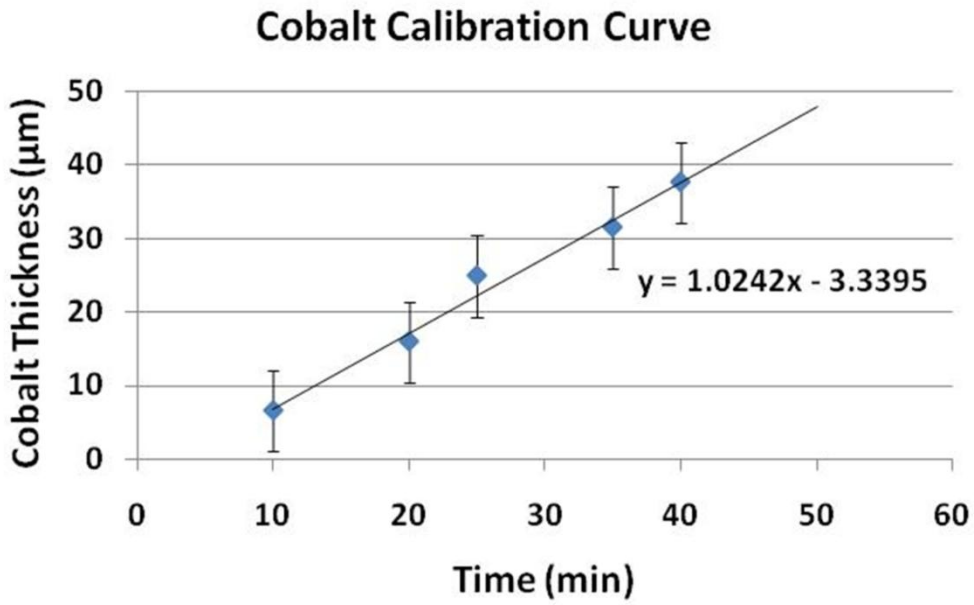


Figure **3-2**: Cobalt calibration curve showing the cobalt deposition rate.

Finally, the gold was deposited at 0.175 A from the potassium gold cyanide plating solution. The gold, which was deposited on top of the cobalt, acts as a metal catalyst for the nanowire growth. A schematic of the electrochemical cell set-up is shown in Figure **3-3** below.

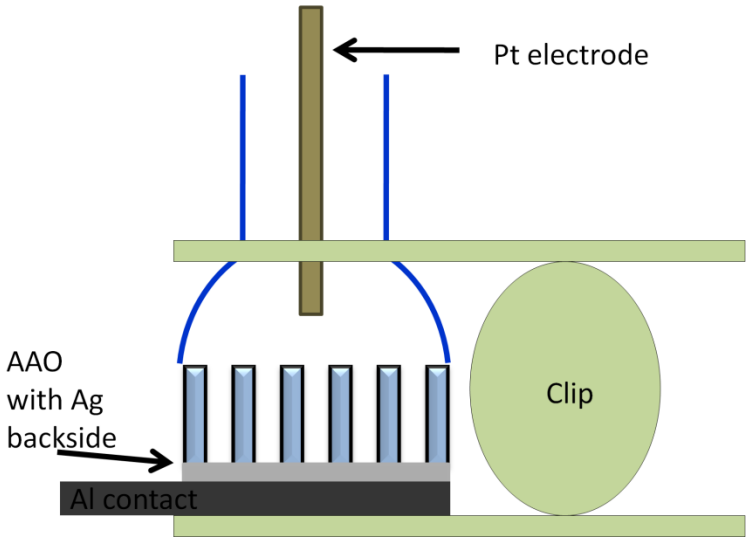


Figure **3-3**: A schematic of the electrochemical cell set-up.

The Al contact (shown in black) allows for hook up of the lead to the backside of the membrane, while the metal clip maintains pressure to ensure a good seal between the AAO template and the glass tube. Addition of the electroplating solution completes the cell circuit. Figure **3-4** below shows an SEM cross-section of the AAO template showing the electroplated metals.

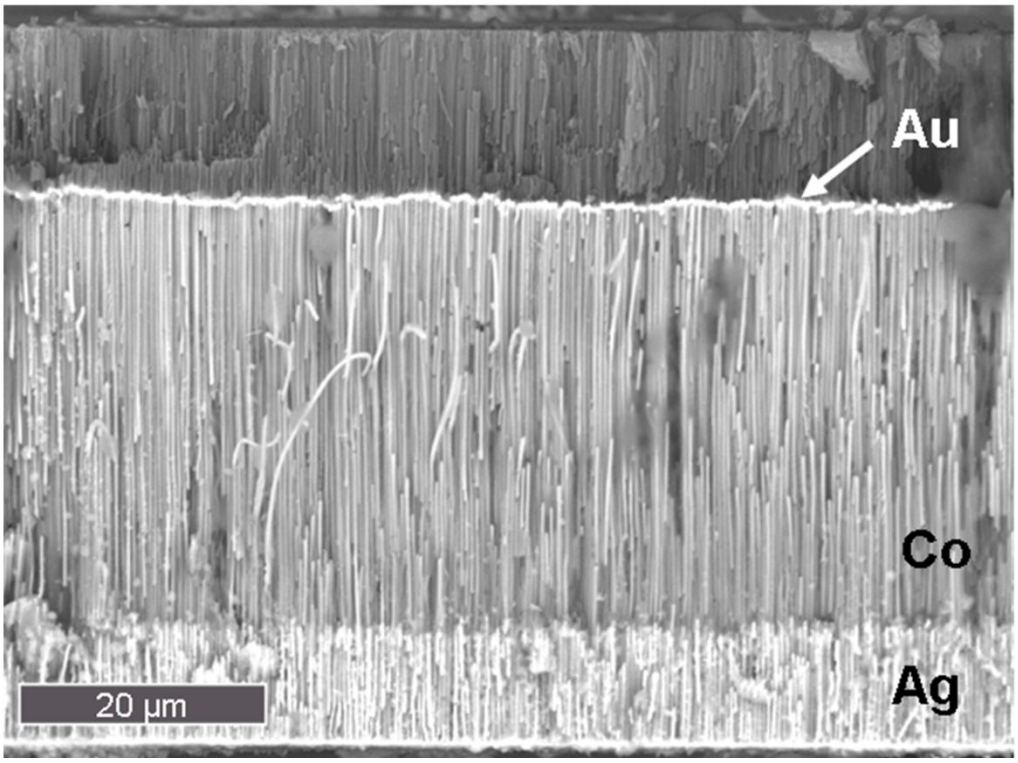


Figure **3-4**: SEM cross-section showing the electroplated Ag, Co, and Au inside an AAO template.

3.2.2 Silicon Wafer Preparation

As described in Section 1.3, the first goal was to create epitaxially oriented silicon nanowire arrays. This was carried out using silicon tetrachloride as the Si precursor, on a Si (111) substrate. Substrates were obtained from Addison Engineering Inc. The 2" diameter substrates were doped p-type and had a resistivity of 1-15 Ω-cm. Prior to all nanowire growth the substrates were cleaned ultrasonically using VLSI grade acetone ($(CH_3)_2CO$) followed by 2-propanol or isopropanol (C_3H_7OH or IPA) at room temperature, and DI water. After the wafers were cleaned, the native oxide was removed using a 10:1 buffered oxide etch (BOE) for 2 minutes. Once the oxide was removed, the wafers were promptly placed into the Denton Explorer™ sputter deposition system for Au sputtering at a pressure of 5 mTorr. Films for all experiments were

deposited by Chad Eichfeld. A 3nm Au thin film was used for all experiments unless otherwise noted. The SiNWs produced using the 3 nm Au film yielded diameters between 75-180 nm. The CVD system has a tube diameter of 1" O.D. so samples were then cleaved to fit inside. Just prior to placement in the quartz tube for growth, the samples are placed in a 10:1 buffered oxide etch (BOE) for 2 minutes to remove any native oxide present. As the samples are heated in the reactor the Au will break up forming Au balls, and the diameter of the Au dictates the nanowire diameter.

3.3 Si CVD Growth

3.3.1 Atmospheric Pressure Chemical Vapor Deposition (APCVD)

A small chemical vapor deposition system located in room 9 Hosler buiding was originally built by Dr. Joan Redwing and Dr. Kok-Keong Lew for the growth of SiNWs using 5% silane (SiH_4) in H_2 as the silicon precursor gas. This system also had the capability of p-type doping using 0.5 % trimethylboron (TMB) in H_2. In order to attempt oriented silicon nanowire growth, the system required the addition of a bubbler and additional lines to grow using liquid $SiCl_4$ as the Si precursor. Silicon tetrachloride is a liquid at room temperature with a vapor pressure of 195 Torr at 20°C. A picture of the completed CVD system can be seen in Figure **3-5** below. The system is equipped for growth of p-type doped or undoped SiNWs using SiH_4 or $SiCl_4$ with either H_2, Ar or a combination of the two carrier gases. The system can be divided into several parts including: (1) gas manifold, (2) Si precursor delivery system, (3) reactor, (4) system exhaust, and (5) safety/control systems. A detailed schematic of the reactor is included in the Appendix.

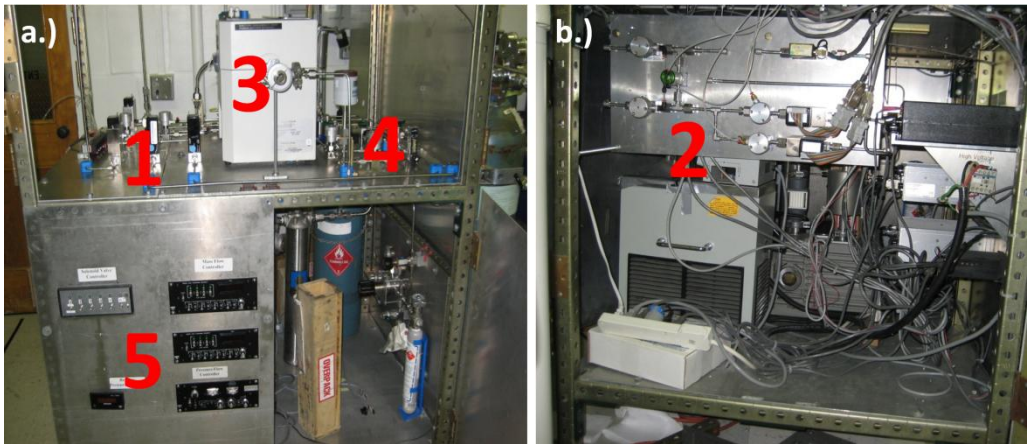


Figure **3-5**: Image of the $SiCl_4$ nanowire system in Room 9 Hosler. The red numbers indicate where each section is located. a.) Front view: 1 Gas Manifold, 3 Reactor, 4 Exhaust, and 5 Control/Safety and b.) Side view: 2 $SiCl_4$ gas manifold.

3.3.1.1 Gas Manifold

The gas manifold contains valves, mass flow controllers, tubings, and fittings to control the flow of the carrier gases, the p-type dopant trimethylboron (TMB) line, and the silicon precursors needed for nanowire growth. The only part not described in this section is the liquid precursor bubbler manifold, which will be covered in Section **3.3.1.2**. All lines are ¼" stainless steel tubing connected using metal sealed VCR fittings that are welded to the tubing.

Nitrogen, hydrogen, and argon are all supplied via ultra high purity gas cylinders provided by GTS. Both prior to and after growth, nitrogen is used to purge the system; during periods of non-use the reactor is left at atmospheric pressure (~760 Torr) containing ultra high purity (UHP) nitrogen. The nitrogen also is used as a purge for the system exhaust during growth. All experiments were carried out using either 100% H_2 as the carrier gas or a 10% H_2 in Ar mixture. The UHP H_2 cylinder is contained inside a ventilated gas cabinet. The other two gas supplies on the reactor are a 5% SiH_4 in H_2 (Solkatronix) and a TMB lecture bottle (Voltaix).

Two different concentrations of TMB were used on the reactor: a 0.5% TMB in H_2 and a 100 ppm TMB in H_2 cylinder. The gas supply manifold for all of the gas cylinders except nitrogen includes a regulator, leak check port between the regulator and cylinder, and a purge line to purge out any residual gases after runs. The leak check port can be used to check the lines after each tank change. Figure **3-6** shows a schematic of a gas supply configuration manifold.

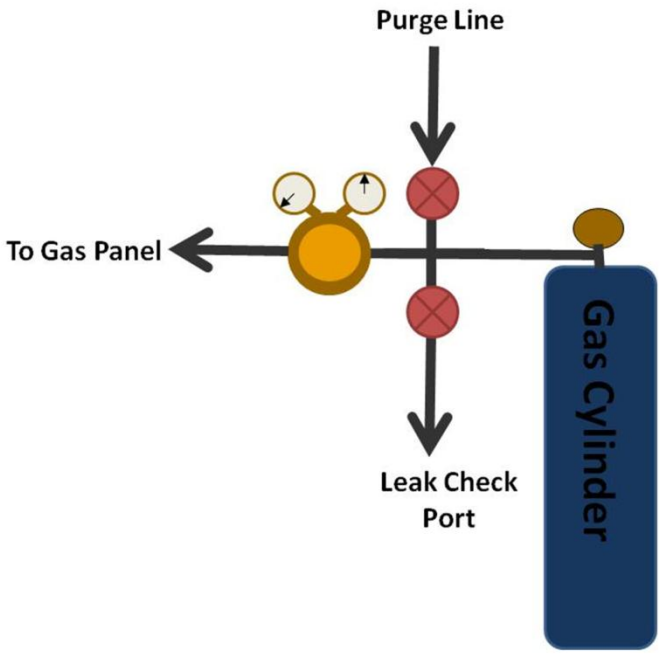


Figure **3-6**: Schematic of the gas supply configuration.

The gas supplied then continues past the regulator to the gas manifold. This includes pneumatic valves and mass flow controllers to control the flow of gases heading into the furnace for reaction. Figure **3-7** below shows a a.) schematic of the gas manifold and b.) an image of the actual system set-up. The $SiCl_4$ is slightly different since it is a liquid and will be described separately. The solid green line on the schematic indicates the tubing is horizontal and in plane with the valves. The dotted green line indicates the tubing is vertical and travels either above to

the exhaust or below to another section of the cabinet. The arrows on the MFC's indicate the direction of gas flow. The pneumatic valves are bellows sealed and actuated by using compressed air through a solenoid valve. When the valve is actuated the solenoid controls the compressed air to the bellows sealed pneumatic valve. The mass flow controllers (MFCs) are calibrated for a specific gas to allow only the set amount of gas through. By regulating the amount, tightly controlled amounts of gases can be flowed into the tube for growth. These parts are all connected using VCR fittings sealed with a metal gasket. When the VCR fitting is tightened the metal gasket is crimped thus creating a seal.

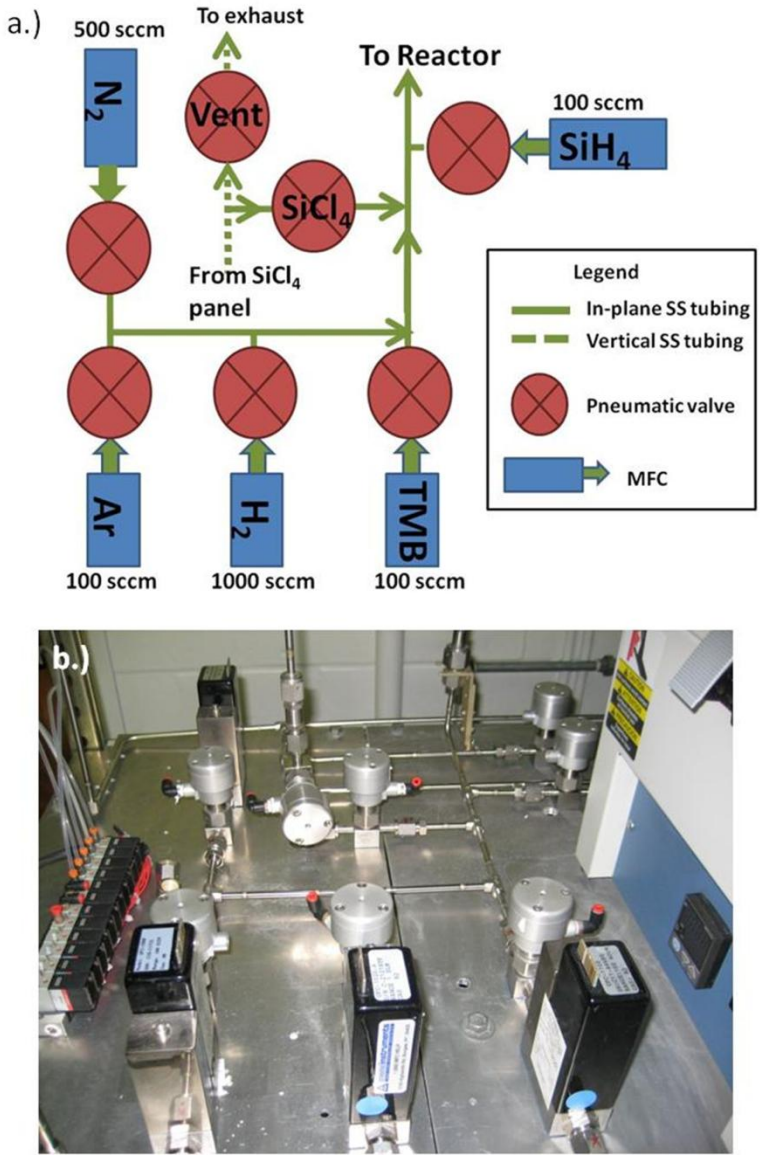


Figure **3-7**: a.) Diagram of the gas manifold showing the layout of the pneumatic valves and mass flow controllers and b.) an image of the completed manifold.

3.3.1.2 Si Precursor Delivery System

In order to grow SiNWs using $SiCl_4$, which is a liquid at room temperature, it was necessary to add a $SiCl_4$ precursor panel to the system. The melting point of $SiCl_4$ is -70°C and

the boiling point is 57.3 °C. The vapor pressure of $SiCl_4$ can be calculated using the Antoine eqn. 3.1, where P is pressure, T is temperature and A,B,C are Antoine coefficients 28.45, -2.39×10^3, -7.39 respectively.[6]

$$\log P = A + \frac{B}{(t + C)} \tag{3.1}$$

An image and schematic of the completed $SiCl_4$ panel can be seen in Figure **3-8** below. The gas panel utilizes mass flow controllers (MFC), a pressure controller, and pneumatic valves as described for the gas manifold in Section **3.3.1.1** above. An Epison III controller was also utilized on the $SiCl_4$ manifold to measure the concentration of $SiCl_4$ present in the carrier gas. This allowed for an accurate measurement of the $SiCl_4$ from run to run. The carrier gas, which can easily be switched to flow H_2, Ar or a combination of both, is controlled through mass flow controllers and solenoid valves. The MFC's then regulate the amount of carrier gas supplied to the stainless steel bubbler containing the liquid $SiCl_4$.

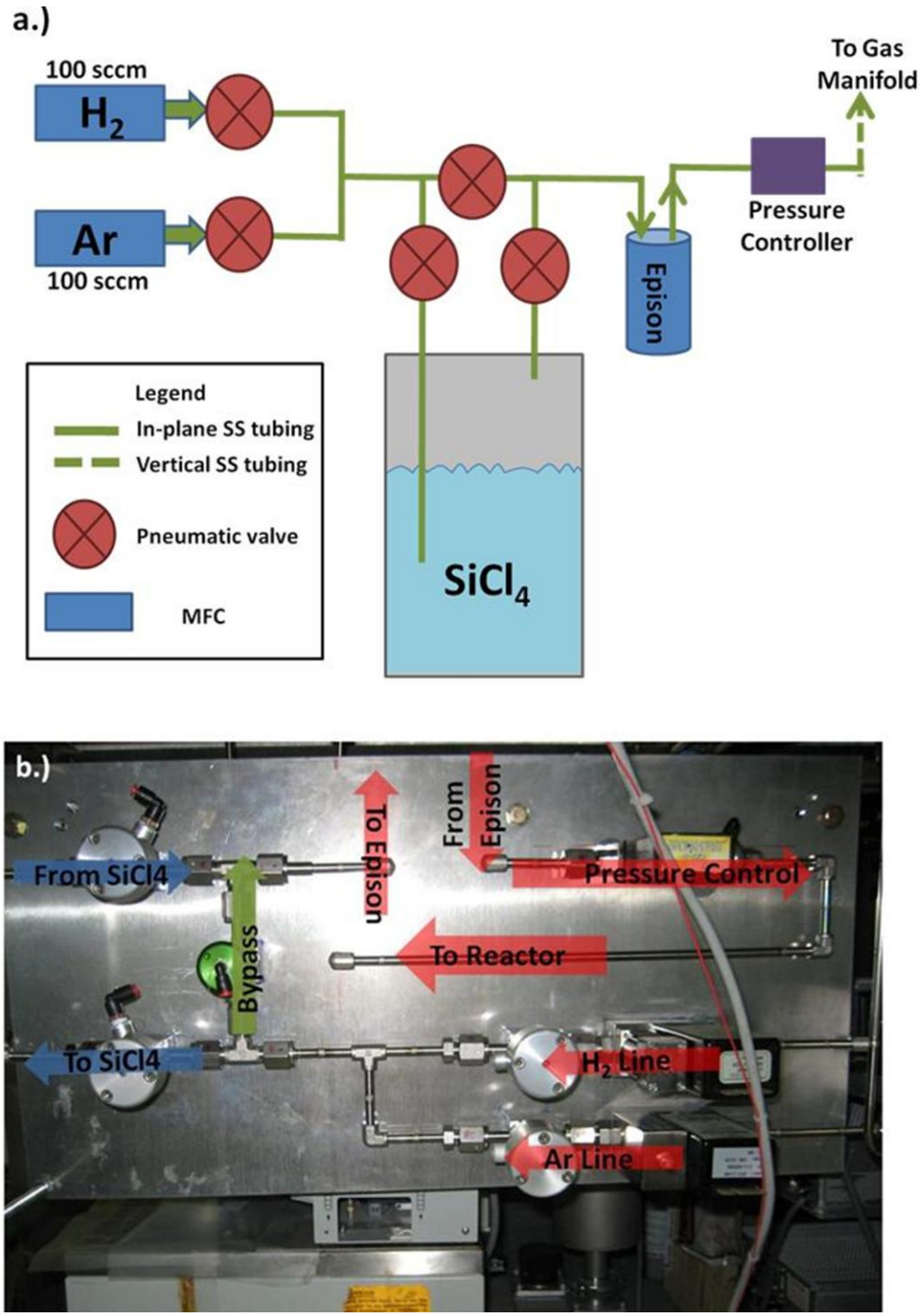


Figure **3-8**: a.) Simplified schematic of the $SiCl_4$ gas manifold. b.) Image of the $SiCl_4$ manifold, with all of the lines and components labeled by the red arrows. The Epison unit sits behind the panel due to space restrictions in the cabinet.

A pre-determined flow rate of carrier gas is directed into the stainless steel bubbler containing the liquid source (in this case $SiCl_4$ purchased from Strem Chemical). The carrier gas then "bubbles" through the liquid picking up a certain amount of $SiCl_4$ based on the temperature and pressure of the liquid. In all experiments the bubbler was kept in a constant temperature bath (Lauda) containing 50% H_2O and 50% ethylene glycol mixture and maintained at a temperature of -11.8°C. The pressure over the bubbler was maintained at 1300 Torr for all growth experiments using the pressure controller (Bronkhorst). The flow rate of $SiCl_4$ (eqn. 3.2) is determined using the carrier gas flow rate (η_{H2}), the vapor pressure of $SiCl_4$ (P_V), and the bubbler pressure (P_B). The blue arrows in Figure **3-8** indicate the flow through the bubbler and green arrow indicates the bubbler bypass. Both before and after growth the bypass line is used when the $SiCl_4$ is not in use.

$$\eta_{SiCl4} = \eta_{H2} \frac{\frac{P_V}{P_B}}{1-\left(\frac{P_V}{P_B}\right)} \tag{3.2}$$

Directly after the $SiCl_4$ bubbler and before the Bronkhorst pressure controller is an Epison III, which measures the concentration of gases in binary mixtures. The Epison works by measuring the speed of sound in the mixture and knowing the specific heat ratios and also the molecular weight of both the carrier gas and also the $SiCl_4$. The unit itself is an in-line stainless steel ultrasonic cell. The Epison has been an important addition to the $SiCl_4$ gas panel as there can be fluctuations in the $SiCl_4$ gas concentration, which can then be compensated for. A typical Epison concentration for $SiCl_4$ at a bath temperature of -11.8°C and a pressure of 1300 Torr is approximately 3.5 % +/- 0.3%. Calculating the concentration using the flow rate, vapor pressure, and bubbler pressure a concentration of 4.2 % is expected. Without the Epison, fluctuations in the $SiCl_4$ concentration cannot be accounted for and can lead to large differences in the growth of the SiNW arrays.

3.3.1.3 Reactor

The reactor is comprised of a 1 inch O.D. quartz tube approximately 24 inches in length and a Lindberg Blue M Mini-Mite furnace. The mini-mite is a split hinge furnace with a maximum temperature of 1100°C, and a type K thermocouple. The inlet gases connect into the reactor via a stainless steel flex line and on the outlet the tube connect to a T, thus allowing for a viewport and a ¼" tube leading to the exhaust. The samples are loaded into the reactor on a quartz boat through the viewport quick connect. The Furnace is equipped with a Eurotherm16 point programmable temperature controller, which allows for the ramps and dwells if needed. In all experiments, the furnace was heated to growth temperature and then cooled, there were no dwells or ramps programmed. The heat rate for the system is approximately 15 °C/min. The cooling rate without fans or opening the shell to cool faster is 20 °C/min. In Figure **3-9** below shows the temperature calibration for the furnace. Calibration was carried out flowing 100 sccm nitrogen through the reactor and using a type K handheld thermocouple. The furnace was set to a pre-determined temperature using the Eurotherm programmable controller and allowed to equilibrate to the set-point for 20 minutes. The thermocouple was placed into the center of the tube using a clamped ring stand to steady the thermocouple through the viewport end of the tube. Since the viewport end of the tube was open, insulation was placed around the thermocouple to plug the end of the tube and prevent heat loss. As can be seen the reactor is 20 °C hotter than the programmed set-point. Thus to keep all experiments at the correct temperature, the furnace was always set 20°C below the actual temperature required for growth. The hotzone in this set-up is located in the center of the Lindberg Blue M at a distance of 12" from the furnace view-port. The hotzone temperature is constant at 12" into the furnace and +/- 2.5 inches on either side of center. The temperatures required for growth experiments were usually 800-1050°C for $SiCl_4$ growth and

atmospheric pressure (~730 Torr) for $SiCl_4$ growth. Prior to each growth, samples were placed in the hot zone using a quartz rod marked to the proper distance.

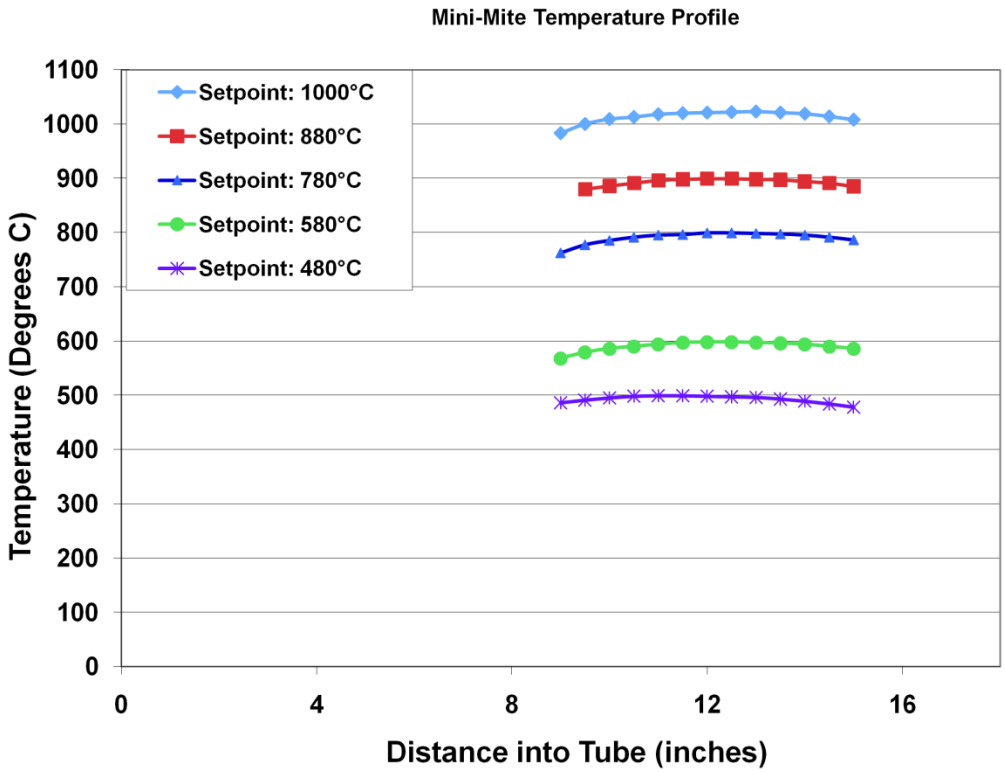


Figure **3-9**: Temperature calibration profile for the Lindberg Blue M Mini Mite Furnace.

3.3.1.4 System Exhaust

The exhaust, as seen from the schematic and image in Figure **3-10** has two different paths depending on the operating pressure of the reactor. For system purging and leak checking gases are flown through the mechanical pump and N_2 dilution line which is typically set at 5 slpm to dilute the exhaust gases below the flammability limit. For nanowire growth using $SiCl_4$ as the precursor, the exhaust bypasses the mechanical pump, since HCl can be corrosive to the pump.

The exhaust is diverted around the pump and consists of a vent line, check valve, and exhaust line with N_2 dilution and an oil bubbler. The N_2 dilution again dilutes the exhaust gases to safe levels, while the check valve and also oil bubbler set-up keep atmosphere (mainly oxygen) from back flowing into the reactor. The oil bubbler is set up so that the exhaust gases bubble through Fomblin oil and then the pressure flows out into the ventilation. Every six months, the $SiCl_4$ vent line was taken apart and cleaned using IPA and q-tips, as corrosion can sometimes occur with HCl coming into contact with any moisture in the atmosphere. If left uncleaned, corrosion can build up over time and obstruct gas flow in the vent line.

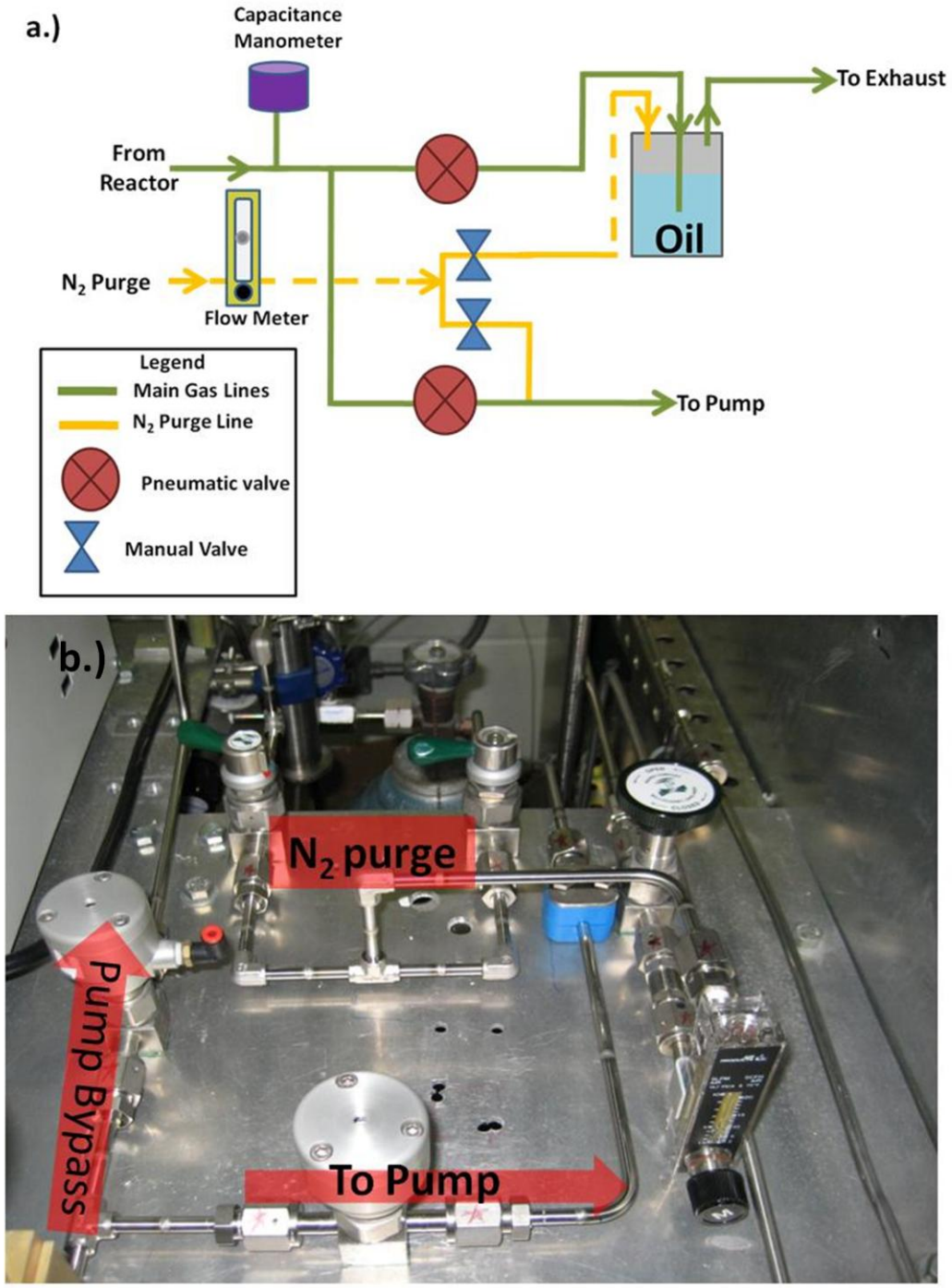


Figure **3-10**: a.) Schematic depicting the flow of gases after the furnace showing the nitrogen purge lines and pump bypass. b.) Image of the nanowire system exhaust showing both the exhaust line to atmosphere for $SiCl_4$ growth and the exhaust line to the pump for SiH_4 growth. There is a N_2 purge line tied into each exhaust line.

3.3.2 Low Pressure Chemical Vapor Deposition (LPCVD)

A second chemical vapor deposition system located in room 220 EE West building was also utilized for this research. This system is computer controlled and is equipped with a 10 % silane (SiH_4) in H_2 mixture and used as the silicon precursor. This system also had the capability of both p-type and n-type doping using a 2% trimethylboron (TMB) in H_2 and 500ppm phosphine (PH_3) in H_2 respectively. Details on the fabrication and design of this system can be found in Dr. Kok-Keong Lew's doctoral dissertation[1]. The system was used for SiNW growth experiments on AAO coated glass templates using silane, which will be described in Section **3.3.2.1**. Epitaxial regrowth of n-type Si was also carried out in this system and will be discussed in Section **3.3.2.2**.

3.3.2.1 Silicon Nanowire Growth in AAO Templates on Glass Substrates

Silicon nanowires were grown using anodized aluminum oxide templates on ITO coated glass. Since lower growth temperatures were required for glass substrates, samples were placed into the LPCVD system and grown using SiH_4 as the silicon precursor. The growth temperature was 500 ℃. System pressure was controlled using a throttle valve and during growth maintained a total pressure in the system of 13 Torr. A temperature profile for this system can also be found in Dr. Lew's thesis[1]. The hotzone was located in the center of the furnace. Similar to loading the samples in the APCVD system the boat was pushed into the proper place using a quartz rod.

3.3.2.2 Epitaxial Regrowth of n-type Si

The n-type regrowth experiments were all carried out in 220 EE West also using the LPCVD system with phosphine (PH_3) and SiH_4 as the n-type and Si precursors respectively. Samples were loaded into the reactor similar to the nanowire samples. Radial growth was carried

out at higher temperatures than nanowire growth to promote thin film deposition. The system was leak checked, purged, and the carrier gas was set up. One difference is there is no Au present to act as a catalyst and higher growth temperatures are used to promote thin film growth. Growth of n-type Si was carried out at temperatures between 650-950°C. To help achieve conformal coating of the nanowires, pressures used for epitaxial regrowth were maintained from 3-10 Torr.

3.3.3 Safety

The gas precursors utilized in growth and doping of silicon nanowires can be hazardous. Silane is pyrophoric, which means it can spontaneously ignite upon contact with air. Silane is also a highly flammable gas that can also cause respiratory damage. Phosphine is also flammable and can be lethal if inhaled. Trimethylboron is also similar and can cause thermal burns and respiratory problems if inhaled. Proper care must be taken in handling and working with these gases. The removal and installation of new cylinders are handled by a team of two people using self-contained breathing apparatus (SCBA) to change the cylinders. After installation or changing of any of the hazardous gas sources including SiH_4, PH_3 and TMB that particular section of the reactor is leak checked to ensure there is no possibility of toxic gases leaking. Leak checks are also performed after any maintenance where VCR fittings need loosened or the quartz tube is changed. A Pfeiffer helium leak detector is hooked up to the system and the area of the system being tested is pumped out using the leak detector. Helium is then sprayed at all the connection points and the leak rate of helium is measured to determine if a leak is present. Hand held H_2 detectors are also used to detect the presence of leaks. If a leak occurs the system and all hazardous gases are stored in ventilated enclosures to keep the gases from leaking into the room.

The systems are equipped with emergency shut-off buttons. In the event of an emergency, the button can be depressed and will then automatically close all pneumatic valves

and shut off the pump thus stopping the flow of gases. The system enclosure is also fitted with an air velocity monitor that has an audible alarm that sounds in the event of ventilation loss. Toxic gas alarms are present on the LPCVD system which will sound if a leak is detected. In the event of a tube breaking or sudden rise in pressure, the LPCVD system also has a safety shut off that when the upper limit pressure set-point (usually set at 650 Torr) is reached the system will shut-off and the alarm will trigger. This is to alert the user of a sudden rise in pressure.

3.3.4 Nanowire Growth Process

Depending on the specific sample and Si precursor being used, there were different growth conditions and pre-growth processing done on the nanowire arrays. Table **3-1** lists all of the different samples and standard processing conditions. Samples were loaded into the reactor and the reactor was leak checked by measuring the leak rate over a 5 minute period. This is important for two reasons: 1) since the precursors and dopant gases are toxic this ensures there will be no toxic gases leaking out and 2) oxygen contamination can cause problems with the nanowire growth and lead to poor samples.

Table **3-1**: Lists the typical substrates used for silicon nanowire growth and their conditions for nanowire growth.

Substrate	Pre-Growth Substrate Preparation	Si Precursor	Temperature (°C)	Pressure Range (Torr)
AAO Membrane	NA	SiH_4	500	13
AAO Coated Glass	NA	SiH_4	500	13
3 nm Au on Si (111)	2 min 10:1 BOE	$SiCl_4$	800-1050	730-760 Torr (Atm)

The reactor is then purged with nitrogen for ten minutes; any lines that were not used were then N_2 purged at this time. The nitrogen is then drained, except for the flow running to the exhaust as the purge gas. The carrier gas (H_2 or H_2 in Ar mixture) was then introduced into the reactor and stabilized at values ready for growth, which is typically 100 sccm. Hydrogen is flowed through the bubbler bypass for 10 minutes to purge the $SiCl_4$ manifold and then switched to flow through the bubbler. The $SiCl_4$ line was then switched to the vent line, which bypasses the reactor. This line was created so that the Si precursor was not flowed over the samples during heat up, which could lead to anomalies/instability in the nanowire growth. The growth pressure was set by either the throttle valve for LPCVD growth using SiH_4 or held at atmospheric pressure for APCVD growth using $SiCl_4$. The reactor was heated up to growth temperature. During heat up for samples grown using at atmospheric pressure chemical vapor deposition, $SiCl_4$ was flowed through the vent line to the exhaust during heat up to stabilize the $SiCl_4$. If SiH_4 was used, the gas was started flowing just before growth. Once at the proper growth temperature, the samples were held there for 5 minutes in order to let the system reach a steady state. Growth commenced at 5 minutes and the Si precursors were switched from the vent line into the reactor so that the flow passed over the samples in the reactor.

Once growth was finished, the Si precursor gases were switched back to the vent lines and the reactor was cooled back to room temperature. During cooling, a total flow of 100 sccm H_2 is maintained over the samples. Once below the eutectic temperature, the precursor and/or dopant lines were all emptied of any remaining gas and purged out with H_2 or N_2. When the temperature dropped below the Si-Au eutectic temperature, the pressure control was turned off and the carrier gases drained. Flow was then switched over to 500 sccm nitrogen for the remainder of the run. Once the temperature was below 100 °C the samples were unloaded.

3.4 Characterization Techniques

Upon removal of the samples from the reactor, a visual inspection was done to determine if there was indeed nanowire growth. Samples most often have a light brown color when nanowires are present. If a high number of samples are oriented the sample takes on a gray/brown color that requires the use of the Leitz Ergolux optical microscope to determine the presence of nanowires. The sample surface appears fuzzy in the optical microscope if wires are present. Scanning electron microscopy (SEM) characterization using the FEI Philips-XL20 was carried out. In this initial phase of characterization, both cross-sectional and plan view images are recorded and then using ImageJ software the length, diameter, and density were measured.

Samples were then characterized in more detail using the Leo 1530 field emission scanning electron microscope (FESEM). Sample analysis consisted of images including the substrate surface after growth and initial observation of the nanowire surface. This tool was also used for looking at the nanowire tip after growth in more detail to see if there was Au diffusion occurring.

Transmission electron microscopy (TEM) was also carried out on both nanowire samples and also the core/shell structures. TEM was carried out using the Philips 420 by Dr. Qi Zhang,

Haoting Shen and Dr. Xiaojun Wang. Analysis of the nanowire samples consisted of a detailed study of diameter, surface roughness, and growth direction. Analysis of the core/shell samples was carried out to examine the core/shell interface, defects present and the crystalline quality of the shell.

Four-point probe measurements were made to determine the resistivity of n-type doped silicon thin films. Samples were measured along the length of Si thin films grown on a sapphire substrate. The current was set at 10 mA for all samples except the undoped and lowest PH_3/SiH_4 ratio ($7x10^{-5}$), as they both hit compliance at 10 mA. Using the thickness of the silicon film, which was also measured along the sample length and the voltage, a resistivity was extracted using equation 3.3 below.[7]

$$\rho = \mathbf{4.532} \times \boldsymbol{t} \times \left(\frac{\boldsymbol{V}}{\boldsymbol{I}} \right) \tag{3.3}$$

The two samples that hit compliance were then measured using a van der Pauw structure[7] and calculating $R_{12,34}$ and $R_{23,14}$ by dividing the corresponding voltage and current. The ratio of the two resistances gives a value for R_r. Based on this the van der Pauw correction factor (F) was calculated to be 0.92 and the resistivity for these two samples was then calculated using the equation 3.4 below[7].

$$\rho = \frac{\pi}{\mathbf{ln(2)}} \times \boldsymbol{t} \times \left(\frac{(\boldsymbol{R}_{\mathbf{12,34}} + \boldsymbol{R}_{\mathbf{23,41}})}{\mathbf{2}} \right) \times \boldsymbol{F} \tag{3.4}$$

Hall measurements were also carried out to determine the carrier type and resistivity. Indium dots were placed in each corner of the sample and then heated on a hot plate for 10 minutes at a temperature of 60°C. The indium contacts were then measured on a curve tracer to determine if the I-V characteristics were linear and the contacts were ohmic. If the contacts were

ohmic they were then placed on the sample holder and the Hall data was collected. Details on the Hall system can be found in Dr. David Meyer's thesis.[8]

3.5 References

1 K.-K. Lew, (2005).

2 T. E. Bogart, S. Dey, K. K. Lew, S. E. Mohney, and J. M. Redwing, Adv. Mater. **17,** 114-+ (2005).

3 T. Bogart, (2004).

4 B. R. Martin, D. J. Dermody, B. D. Reiss, M. M. Fang, L. A. Lyon, M. J. Natan, and T. E. Mallouk, Adv. Mater. **11,** 1021-1025 (1999).

5 A. M. Mohammad, S. Dey, K. K. Lew, J. M. Redwing, and S. E. Mohney, J. Electrochem. Soc. **150,** G577-G580 (2003).

6 *CRC Handbook of Chemistry and Physics 89th ed.*

7 D. K. Schroder, *Semiconductor Material and Device Characterization*, 3rd ed. (John Wiley & Sons, New York, 1998).

8 D. Meyer, Thesis, The Pennsylvania State University, 2008.

Chapter 4

Synthesis and Characterization of SiNW Arrays using $SiCl_4$

4.1 Introduction

As stated in Section **1.3**, the motivation of this research is to develop fabrication methods to produce prototype photovoltaic devices on Si substrates. The ability to decouple the direction of light absorption from the direction of carrier collection by using a nanowire array geometry makes understanding the growth of SiNWs of interest to further advance nanowire solar cells. This chapter investigates the effect of growth conditions on the growth rate and structural properties of SiNWs grown on Si (111) substrates. In order to obtain oriented SiNW, arrays $SiCl_4$ was used as the silicon precursor. Thermodynamic modeling was be used to better understand the growth mechanisms responsible for nanowire growth using $SiCl_4$. Silicon nanowire growth rate versus silicon nanowire diameter was also examined to determine the dependency for comparison to prior reports. Finally, initial p-type doping of silicon nanowire arrays were carried out.

Interest in creating vertical arrays of silicon nanowires has generated a renewed interest in the use of $SiCl_4$ for growth of oriented silicon nanowire arrays. There have been several recent reports of nanowire growth using $SiCl_4$.[1-4] The ability to grow large arrays of silicon nanowire arrays on Si substrates via patterning using $SiCl_4$ has been demonstrated by Kayes et al.[4] An advantage to using $SiCl_4$ is that it is easier to obtain epitaxial nanowires due to the presence of HCl.[5] Silicon tetrachloride is also less expensive and not as hazardous as silane (SiH_4). Silane is also commonly used in nanowire growth to produce nanowires, typically at low pressures, and the growth rate increases with P_{SiH4} and also temperature.[5,6] Prior studies of nanowire growth with SiH_4 and $SiCl_4$ can be found in section **2.2**.

Silicon tetrachloride has been used as a gas precursor for the CVD growth of silicon nanowires since the 1960's [7-11] on (111) Si substrates by the vapor-liquid-solid (VLS) technique using Au as the catalyst. A detailed description of VLS growth can be found in section **3.3.4**. A range of temperature and growth conditions have been explored. Discussion of previous literature on the growth of SiNW arrays using $SiCl_4$ is reported in section **2.3.2**. There have been conflicting reports on the diameter dependence on SiNW growth rate.[12,13] A discussion of these opposing trends are in section **2.3.3**. There has also been little work done on the effect of P_{SiCl4} on nanowire growth rate using $SiCl_4$. The effects of gas phase chemistry on growth rate of silicon nanowires have not been examined in detail for $SiCl_4$.

In order to grow SiNW arrays controllably at high growth rates on Si (111), there needs to be an improved understanding of the effect of growth conditions on the SiNW properties. In this study, we have investigated the effect of growth conditions on the growth rate and structural properties of SiNWs grown with $SiCl_4$ and compared the results to predictions obtained from a gas phase thermodynamic equilibrium model of the $SiCl_4/H_2$ system. The results of p-type doping using trimethylboron (TMB) of the SiNW arrays will also be reported.

4.2 Experimental Details

4.2.1 Silicon Nanowire Growth on Si (111)

Silicon nanowire arrays were fabricated using 3 nm Au thin films sputter deposited on (111) Si substrates. Prior to growth, the native oxide was removed using a 10:1 buffered oxide etch (BOE) for 2 minutes. Samples were loaded onto a quartz boat and placed in an isothermal atmospheric pressure chemical vapor deposition (APCVD) reactor. SiNW arrays were then grown by the vapor-liquid-solid (VLS) technique using $SiCl_4$ as the source gas and either H_2 or a

mixture of 10% H_2 in Ar as the carrier gas. $SiCl_4$ is a liquid at room temperature and was transported into the reactor via a stainless steel bubbler that was maintained at a pressure of 1300 Torr and cooled to a temperature of -11.8 °C. Samples were grown at temperatures ranging from 800-1000 °C for times between 30 sec-10 minutes. The total gas flow over the samples was held constant at 100 sccm. The silicon tetrachloride ($SiCl_4$) partial pressure was varied from 1-16 Torr by varying the carrier gas flow rate from 5-100 sccm through the bubbler.

Nanowire lengths were measured via cross-sectional FESEM images of the sample and using ImageJ to determine individual nanowire lengths. Figure **4-1** below is a typical cross-sectional SEM image depicting how the nanowires were measured using ImageJ. TEM samples were prepared by sonicating the sample in isopropyl alcohol (IPA) for 5 minutes to mechanically release the wires from the substrate. The solution was then dispersed onto a lacey carbon grid. Analysis was then carried out to determine the structural properties, and growth directions.

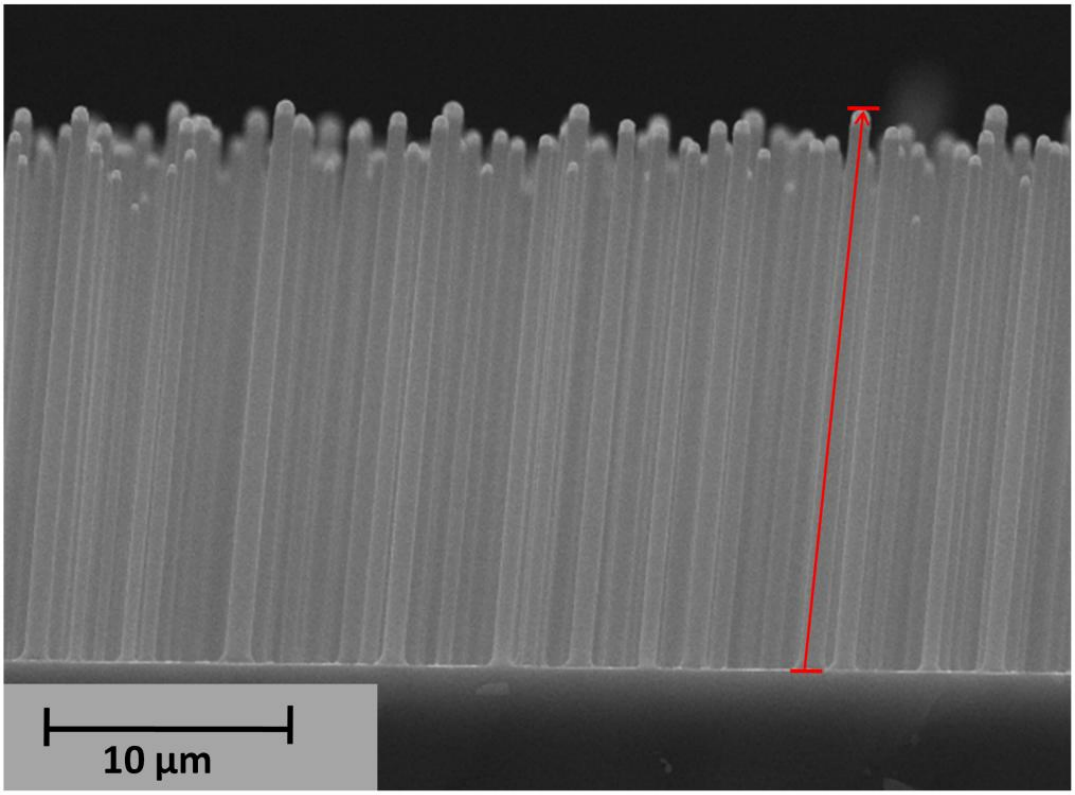


Figure **4-1**: Cross-sectional SEM image that depicts a silicon nanowire length measurement. The sample was grown at a temperature of 900 °C.

4.2.2 Thermodynamic Modeling

The reduction of chlorosilanes and especially $SiCl_4$ has been investigated for use in thin film deposition. A model was also developed by Van der Putte *et al*. in section **2.2.1** that will be followed in order to model the growth of SiNWs grown using $SiCl_4$. The reduction of $SiCl_4$ can be expressed as:

$$SiCl_4(v) + 2H_2 \Leftrightarrow Si(s) + 4HCl(v)$$

This reaction requires a high temperature (>1000°C) to produce high quality layers.[14] At these temperatures, the reaction of $SiCl_4$ and H_2 occurs very fast and the surface reactions are also

assumed to occur very fast. Based on these observations, it was assumed that the gas phase approaches an equilibrium state and there will be a balance between the amount of solid Si formed and etched. For Si thin film deposition with $SiCl_4$, it was proposed that the growth rate is limited by mass transport to the substrate surface. A gas phase equilibrium model was then used to predict the gas phase species concentrations for given Si thin film growth conditions.[14] For each gas phase species a reaction describing its decomposition and formation can be written as shown below for SiH_2Cl_2.

$$SiH_2Cl_2(v) \Leftrightarrow Si(s) + 2HCl(v)$$

The equilibrium constant for this reaction can then be seen as:

$$\boldsymbol{K_{eq}} = \frac{(\boldsymbol{a_{Si}})\left(\boldsymbol{P_{HCl}^2}\right)}{\boldsymbol{P_{SiH2Cl2}}} \tag{4.1}$$

Where a_{Si} is the activity of silicon(s), P_{HCl} is the partial pressure of HCl(v), and $P_{SiH2Cl2}$ is the partial pressure of SiH_2Cl_2. The value for K_{eq} at a specific temperature T is related to the change in Gibbs Free energy of formation ($\Delta G°$) for a given gas phase species and is given by:

$$\Delta G^\circ = -RT(\ln K_{eq}) \tag{4.2}$$

Thermodynamic calculations were done using the software package HSC Chemistry 5.1 and its data library which contains heat capacity, enthalpy, and entropy values for many chemical species. The individual elements are specified by the user as well as the temperature, pressure, and molar quantities for each species. Equilibrium concentrations and their phases can then be calculated as a function of amount of input concentrations (in this case $SiCl_4$), temperature, or

pressure by solving for the minimization of Gibbs free energy over the entire system using the equation:

$$G = \sum_i n_i (H_i - TS_i) \quad (4.3)$$

where G is the total free energy of the system, H is the enthalpy, T is temperature, n_i is the molar amount of the ith substance, and S is the entropy. The gibbs free energy is then minimized iteratively using the available thermochamical data and the GIBBS solver in HSC Chemistry. The solver is constrained by temperature, pressure, and a mass balance.

In comparing the calculations with the experimental results based on prior thin films studies it is assumed that the reaction rates are fast enough for the system to reach thermodynamic equilibrium. The modeling was done using conditions used for SiNW growth at atmospheric pressure and assuming steady state the flow rates were then converted to partial pressures. The gas phase species considered were Si, SiCl, $SiCl_2$, $SiCl_3$, $SiCl_4$, SiH, SiH_4, $SiHCl_3$, SiH_2Cl_2, SiH_3Cl, Cl, Cl_2, H, H_2, and HCl.[15]

The gas phase species concentrations calculated using HSC chemistry were then used to predict the amount of Si(s) formed. A simplifying assumption was made that the diffusion coefficients of all the gas phase species were equal. Consequently, the amount of Si formed in the gas phase can be assumed to be the same as that deposited as SiNWs on the surface. A mass balance was then used to determine the amount of solid silicon formed for the SiNW growth conditions. The predicted Si growth rate (Si_{total}) was found by calculating the difference in the moles of silicon in the inlet gas (Si_{input}) and the moles of Si in the gas phase in its equilibrium state (Si_{eq}) at the growth temperature for all of the species considered using the following equations (4.4, 4.5 and 4.6):

$$Si_{input} = \sum_{1}^{15} P_{Si_n H_m Cl_l}{}^{l} = \frac{1}{4} Cl_{total} \quad (4.4)$$

(4.5)

$$Si_{eq} = \sum_{1}^{15} P_{Si_n H_m Cl_l}{}^{n} \quad (4.6)$$

$$Si_{total} = Si_{input} - Si_{eq}$$

where the n, m, and l are integers and the total Si_{input} is ¼ of the total Cl input since the input gas is $SiCl_4$.

4.2.3 p-type Doping and Electrical Characterization

In-situ p-type doping was carried out at different temperatures and carrier gas concentrations. The TMB/$SiCl_4$ ratio was also varied using a 100 ppm TMB in H_2 lecture bottle from Voltaix. In order to measure the nanowire resistivity, 4-point resistivity measurements were carried out. The SiNWs were sonicated and released into an IPA solution just as was done for TEM. Individual SiNWs were then electrofluidically aligned[16] to an electrical testbed shown in the Figure **4-2**.

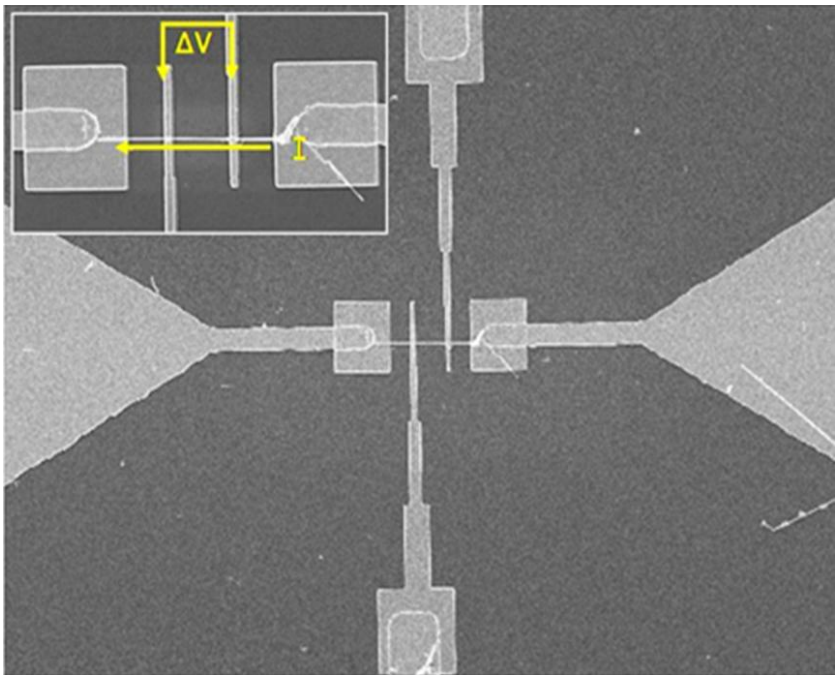


Figure **4-2**: FESEM image of the four-point resistivity electrical testbed.[17]

Four-point resistivity measurements were then made by applying a current between the outer two contacts and measuring the voltage between the inner two contacts. Using the electrical testbed with a backside contact allows for gated I-V measurements, which can provide information on the carrier type.

Four-point resistivity measurements were also made by Chad Eichfeld by taking the nanowires released in the IPA solution and dispersing them on a 75 nm thick silicon nitride covered Si wafer. A SF6 resist was spun on at 4krpm and baked at 190 C for 8 minutes. A diluted SPR3102 was then spun onto the wafer. An exposure array was then used to deterimine the proper exposure dose for this sample. The Heidelberg DWL66 laserwriter with a 2mm writehead was used to pattern areas along the length of the nanowire for contact deposition. A BOE etch was carried out prior to metal deposition. The samples were then placed in an e-beam evaporator where 250 nm of Ni was deposited. Metal liftoff was then performed in a 40°C Nano Remover PG (n-methyl pyrolodine). Samples were then rinsed in DI water and blown dry with N_2. Samples

were not purged with N_2 during measurements and no backside gating was performed to determine the carrier type with these measurements. Four-point measurements were then made at three points along the length of the wire and FESEM was used to measure the gaps and contact widths.

4.3 Results and Discussion

Based on prior thin film literature on $SiCl_4$ discussed in section **2.2**, there are a number of parameters that may also impact the growth of silicon nanowires as well. Based on the prior literature, the most important parameters are temperature, silicon tetrachloride partial pressure, hydrogen partial pressure and residence time of gases in the reactor tube. The growth rate versus nanowire diameter dependence was also examined.

4.3.1 Temperature Dependence

For initial experiments using silicon tetrachloride, the samples were placed in the center of the hotzone, which was described in section **3.3.1.3**. The samples were grown at a constant silicon tetrachloride concentration (P_{SiCl4} =3.6 Torr) on (111) Si with a 3nm Au thin film. A series of growths was carried out at various temperatures to determine the temperature range for which oriented nanowire growth was possible. For each sample, a total of from 15-20 individual silicon nanowire lengths were measured. The results discussion is limited to samples grown at temperatures of 800 °C and higher. Nanowires were present on samples grown below 800 °C; however, the wires were not oriented with respect to the surface and thus were not included in the analysis.

4.3.1.1 Orientation

The temperature does alter the crystallographic orientation of the nanowires with respect to the sample surface. The SiNW orientation was found to be strongly dependent on the growth temperature. The amount of SiNWs being <111> oriented perpendicular to the substrate increased from 18-80% at 800°C and 900°C respectively as shown in Figure **4-3**. The increase in SiNW orientation is most likely due to increased HCl removing any native surface oxide present.

Cross growth can be described as nanowires growing in other (111) orientations not perpendicular to the Si (111) substrate. At temperatures 950 °C and higher there is almost no cross-growth occurring. The average diameter of the SiNWs is approximately 130 +/- 50 nm for growth temperatures below 950 °C. At 950 °C, the average diameter increases to 162 +/- 78 nm and at a growth temperature of 1050 °C the average diameter is 223 +/- 90 nm. Since the heating time is longer for higher growth temperatures, the time in the reactor increases. This additional annealing may cause the Au, which can be highly mobile at these temperatures on Si to agglomerate differently and break up into larger average particles due. This is known as Ostwald ripening, in which the larger Au particles will continue to grow bigger, while the smaller particles shrink. Larger particles on a surface have a lower surface to volume ratio compared to the smaller particles, and thus have lower surface energy.

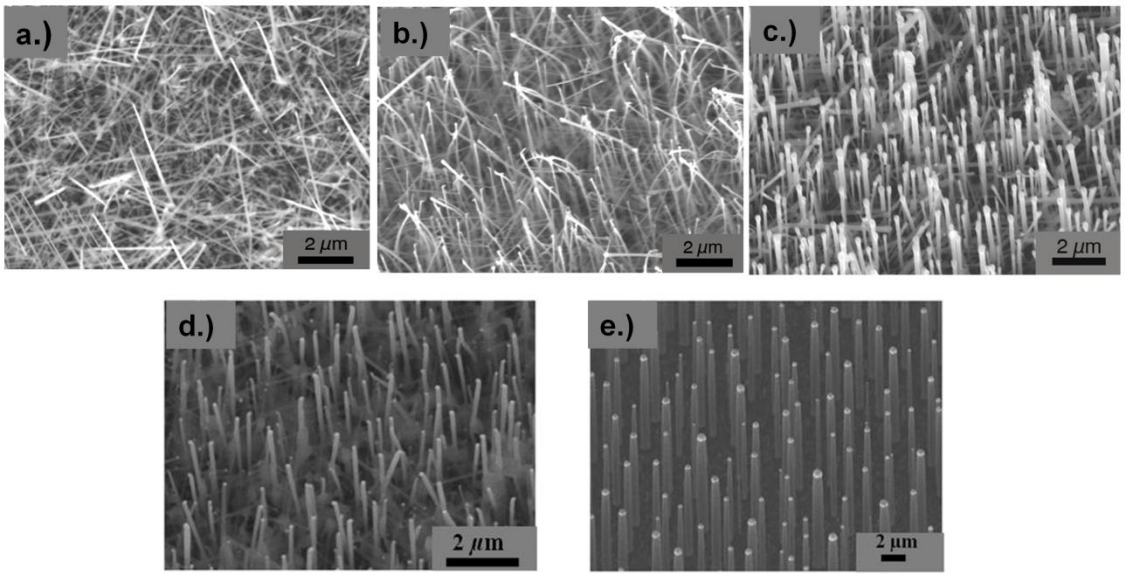


Figure **4-3**: FESEM images tilted 15 ° to show the orientation of the nanowires with respect to the Si (111) substrate at a.) 800°C b.) 850°C c.) 900°C d.) 950°C and e.) 1050 °C.

4.3.1.2 Growth Rate

The average SiNW length was plotted versus the growth time at temperatures between 850-950°C as shown in Figure **4-4**. The nanowire length increases linearly with time.

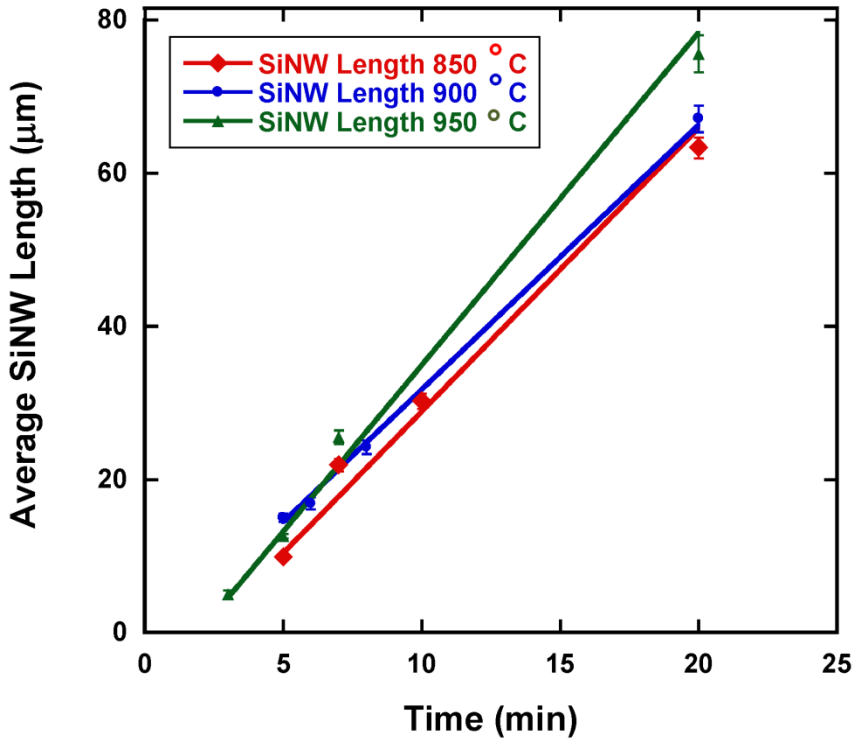


Figure **4-4**: Graph of average SiNW length versus time for different temperatures.

The growth rates are on the order of 3-4 μm/min and exhibit a small increase with temperature. It can be seen from the graph that the x-intercept is not zero suggesting there is an incubation time before the nanowire growth begins. The nanowire growth rate and incubation time for SiNW growth at 850, 900, and 950°C is reported in Table **4-1**. For these experiments the incubation time ranged from 1-1.4 min, this is similar to incubation times reported by Clement *et al.*who reported incubation times from 0.5-1.13 min for silicon nanowire grown using disilane.[18]

Table **4-1**: Table showing the SiNW growth rates and incubation times for different growth temperatures.

Temperature (° C)	**850**	**900**	**950**
Growth Rate (μm/min)	**3.4 +/- 0.22**	**3.5 +/- 0.06**	**4.1 +/- 0.18**
Incubation Time (min)	**1.2**	**1.0**	**1.4**

The silicon nanowire growth rate was plotted versus temperature in Figure **4-5**. This plot shows that the growth rate increases slightly as temperature is increased from 800°C up to 1050°C. The growth was carried out at atmospheric pressure and a P_{SiCl4} of 9 Torr. This weak temperature dependence indicates the growth may be in a mass transport limited regime, similarly to growth of Si thin films using $SiCl_4$ at high temperatures (>1050°C). Figure **2-1** shows the growth rate versus 1/T for $SiCl_4$. Based on this plot for $SiCl_4$, one would expect at temperatures below 1050°C the silicon nanowire growth to take place in the kinetically limited growth regime.

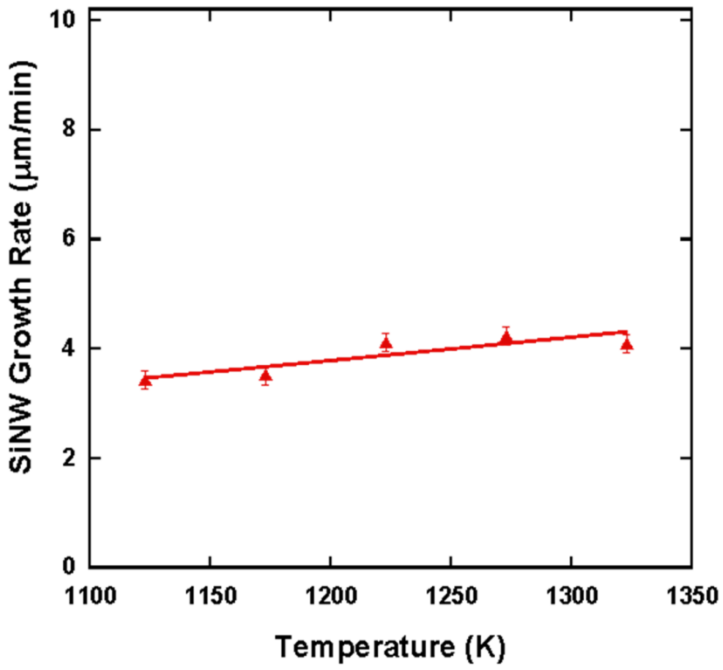


Figure **4-5**: Plot of silicon nanowire growth rate versus temperature between 800-1100°C fit using the power law $(T)^n$.

In this case the growth would be limited by flux to the surface (J) and can be described using equation 4.7[19], which describes the diffusion of gas through a stagnant boundary layer:

$$J = -\frac{D\left(P_g - P_s\right)}{\delta RT} \tag{4.7}$$

where δ is the thickness of the boundary layer, P_g is the vapor pressure of the gas and P_s is the vapor pressure at the substrate surface. This equation can be applied when the flow is viscous and laminar where the gas diffuses through a stagnant boundary layer of thickness δ adjacent to the substrate. The growth rate is then proportional to diffusivity (D). The diffusivity of the gas can be calculated using equation 4.8:[19]

$$D = -D_o \frac{P_o}{P}\left(\frac{T}{T_o}\right)^n \tag{4.8}$$

where D_0 is the value of diffusivity at standard temperature (T_0) and pressure (P_0) and n is an exponent. This equation describes the diffusion of gases through a stagnant system based off of kinetic theory. The diffusivity (D) is predicted to depend on pressure and temperature as $D \sim T^{3/2}/P$, however, n is experimentally found to be approximately 1.8[19]. Inserting equation 4.8 into equation 4.7, the dependence of growth rate on temperature has a T^{n-1} dependence, which experimentally is 0.8.This equation (4.8) can be applied to laminar flow where diffusion of a gas through the stagnant boundary layer of thickness δ is adjacent to the substrate. Using a power fit in Figure **4-5**, n has a value of 1.3, which is slightly lower than the theoretical value of 1.5 and the experimental value of 0.8. This further suggests that the SiNW growth is taking place in a mass transport limited regime.

4.3.2 Silicon Tetrachloride Partial Pressure

SiNW arrays were grown at atmospheric pressure, 950°C and a bubbler temperature and pressure of -11.8°C and 1300 Torr. The input silicon tetrachloride partial pressures (P_{SiCl4} = 1-16 Torr) were varied, by varying the amount of H_2 through the $SiCl_4$ bubbler, to determine the effect of $SiCl_4$ on the nanowire growth rate. Figure **4-6** shows both cross-sectional and plan view images of SiNW arrays grown at two different $SiCl_4$ partial pressures. Figure **4-6(a,b)** shows an array grown at P_{SiCl4} = 4.5 Torr . Figure **4-6(c,d)** was grown at a higher $SiCl_4$ partial pressure of P_{SiCl4} = 14 Torr. As can clearly be seen from the figure, the SiNW arrays grown at lower P_{SiCl4} are longer than the wires grown at higher $P_{SiCl4.}$ The growth at the higher silicon tetrachloride partial pressures has a much lower nanowire density, while SiNW arrays grown at lower partial pressures (P_{SiCl4} = 1-4 Torr) have a higher nanowire density across the substrate surface. In some samples, diameter ranges were observed. The large diameter nanowires typically had diameters

larger than 400 nm, while the small diameter nanowires had diameters smaller than 250 nm. In the growth rate studies, the large diameter nanowires were not taken into account for the growth rate measurements due to their large difference in growth rate compared to smaller diameter (<250 nm) nanowires. The diameter dependence and growth rate are reported in Section **4.3.5**. The growth rate appears to increase with increasing diameter and will be discussed later in the paper. The sample grown at P_{SiCl4}= 4.5 Torr has an average diameter of 82 +/- 31 nm, while the sample grown at P_{SiCl4} = 14 Torr has an average diameter of 110 +/-35 nm. Based on silicon nanowire diameter dependence reported later in section **4.3.5** the sample grown at 14 Torr should have a larger growth rate but experimentally the growth rate is smaller.

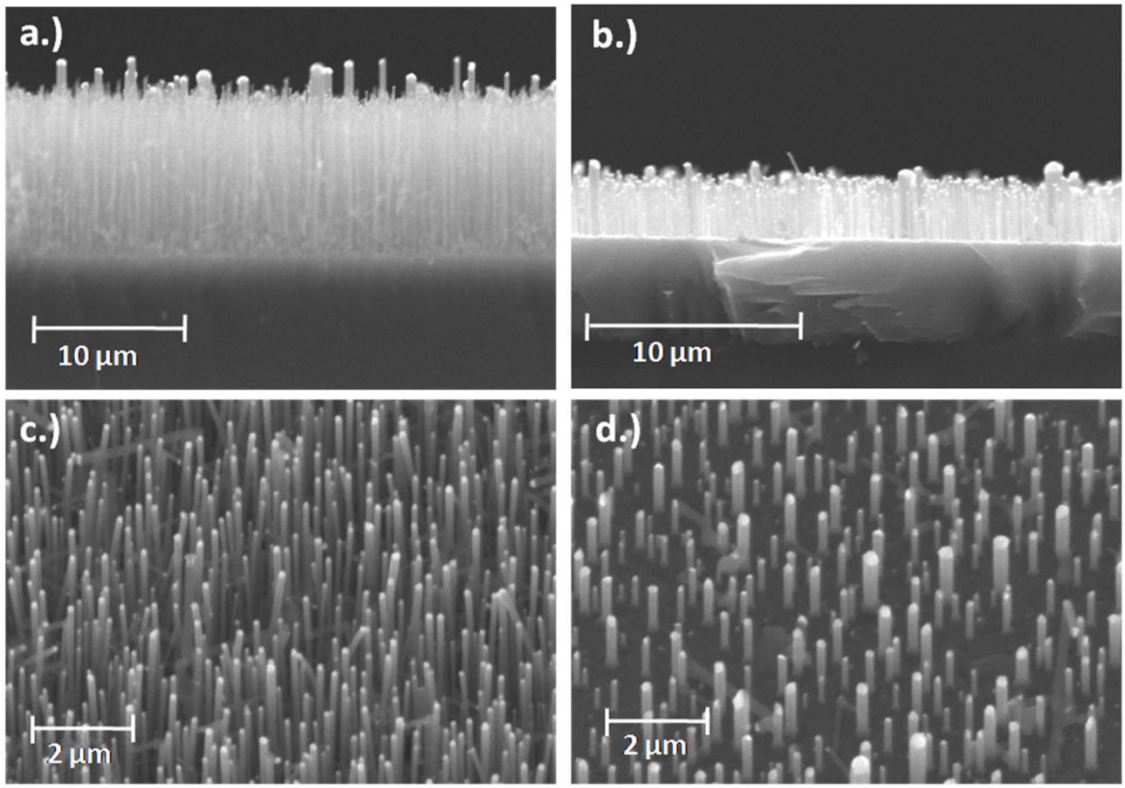


Figure **4-6**: Cross-sectional and plan view FESEM images of SiNW arrays grown at 950°C, and atmospheric pressure a.)/c.) grown at P_{SiCl4} = 4.5 Torr and b.)/d.) grown at P_{SiCl4} = 14 Torr.

The results seen in Figure **4-6** are interesting as the growth rate decreases at higher P_{SiCl4} so more detailed studies of the growth rate and P_{SiCl4} were carried out. As shown in Figure **4-7**, for nanowire growth using 100% H_2 as the carrier gas, the growth rate of the wires increased with increasing P_{SiCl4} at reduced partial pressures, reaching a maximum of ~ 10 μm/min at P_{SiCl4} of 4.5 Torr. Beyond this point, the growth rate decreased with increasing P_{SiCl4}. The growth rates themselves do not differ much within the temperature range of 800-1000°C as shown in Figure **4-7**. This trend of increasing and then decreasing growth rate with increasing P_{SiCl4} was seen for all the nanowire growths in this temperature range. This is similar to what has been reported for thin film growth using $SiCl_4$[20-22] (Fig. **2-2**). As the growth rate increases with increasing P_{SiCl4} until it reaches a maximum, then the growth rate then begins to decrease with increasing partial pressure. Van Der Putte et al. used equilibrium calculations to predict the solid silicon formation and explain the silicon thin film results [15] as discussed in section **2.2.1**.

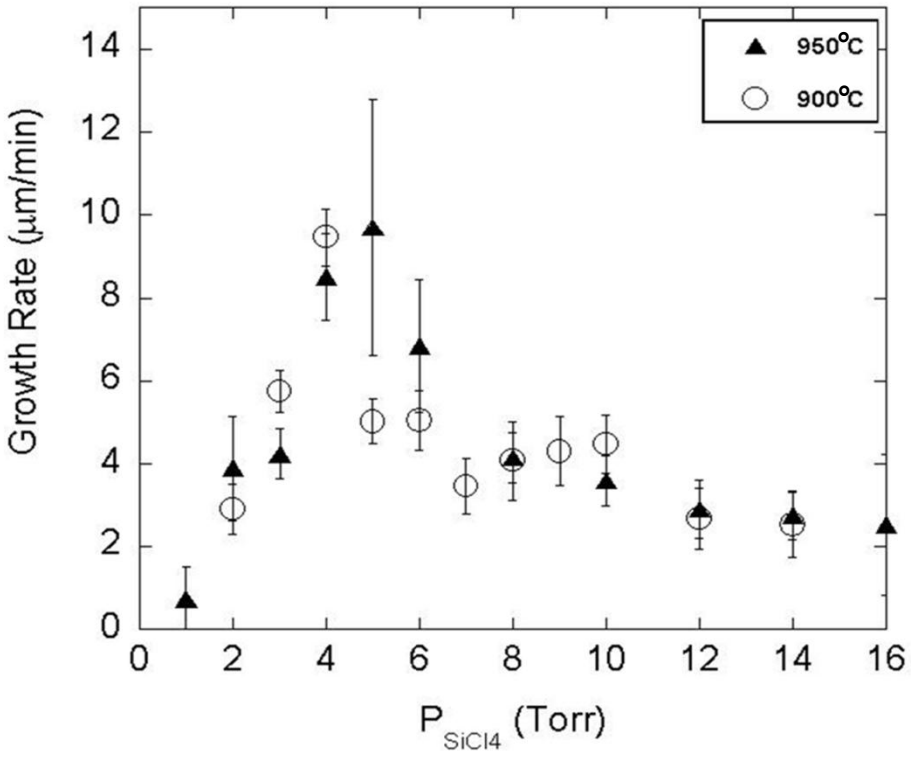


Figure **4-7**: Growth rate versus P_{SiCl4} for 100% H_2 at different temperatures.

4.3. 3 Gas Phase Equilibrium Calculations

Thermodynamic modeling was carried out in order to investigate the effect of P_{SiCl4} on growth rate. HSC Chemistry was used to calculate the gas phase equilibrium for the different gas phase species listed in section **4.2.2** followed by a mass balance to determine the amount of solid silicon produced for these conditions. Figure **4-8 (a)** and **(b)** show the gas phase equilibria and the predicted solid silicon formed respectively. The growth conditions for the model were atmospheric pressure and a temperature of 1050 °C with 100 % H_2 as the carrier gas. The thermodynamic model shows a similar maximum at a P_{SiCl4} = 5 Torr in the Si solid phase as that of the experimental SiNW growth rates P_{SiCl4}= 4.5 Torr at 950 °C.

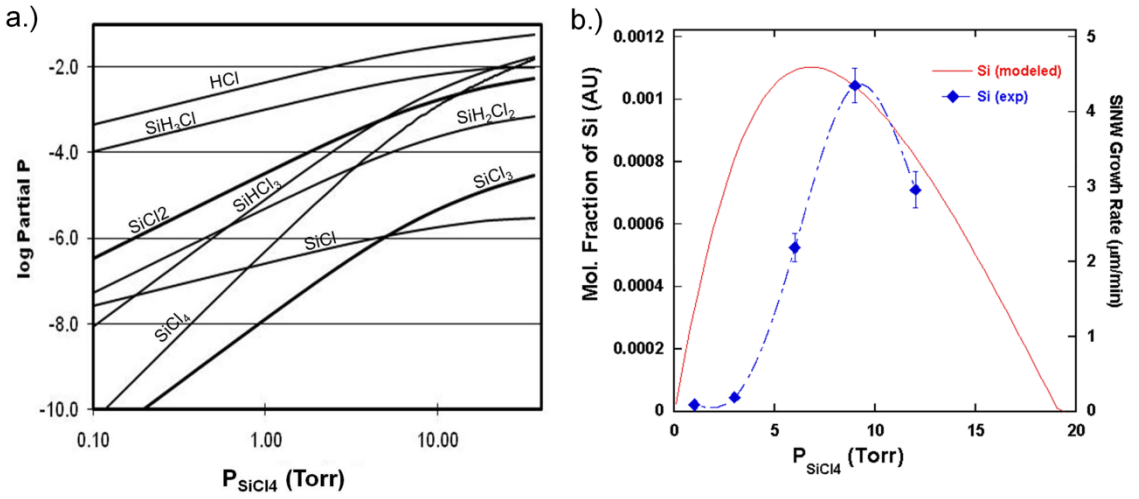


Figure **4-8**: a.)Gas phase species thermodynamically modeled using HSC chemistry and b.)Comparison of model predictions and SiNW growth rate at 1050°C 100% H_2 (0.5 step).

Experiments carried out at the same temperature as the model (1050°C) shown in Figure **4-8(b)** trends similarly to the predicted amount of solid silicon formation. Although the experimental results show a maximum growth rate at a higher P_{SiCl4}, this may be due to the model assumption that the diffusion coefficients of each gas phase species are the same. The models by Van der Putte *et al.* discussed in section **2.2.1** reported a shift in the growth rate maximum for the first model, where they used a single diffusion coefficient for all gas phase species. A better agreement for the growth rate maximums for the model and experimental thin film results was reported when each individual diffusion coefficient was taken into account for all of the gas phase species.[15] The dependence of wire growth rate on P_{SiCl4} is qualitatively consistent with the amount of solid Si predicted to form at equilibrium under these conditions.

The reduction in SiNW growth rate at higher silicon tetrachloride partial pressures results from a shift in the gas phase equilibrium, which leads to an increase in the chlorine containing gas phase species as the growth transitions into an etching dominated regime. The growth rate appears to transition from a growth to an etching regime as the chlorine containing gas phase species become more thermodynamically stable. Figure **4-9** plots the gas phase equilibrium

concentrations in kmol versus the $P_{SiCl4}$for different gas phase species. The SiH_xCl_y gas phase species are the ones that have a Si,H, and Cl component such as SiH_3Cl, SiH_2Cl_2. The $SiCl_x$ species only contain a Si and a Cl such as $SiCl_4$,$SiCl_3$,$SiCl_2$ and SiCl. Each line is the difference between a combination of the SiH_xCl_y and the $SiCl_x$ species. As can be seen in the graph the difference in the gas phase equilibrium concentration for the (SiH_3Cl + SiH_2Cl_2)-($SiCl_4$+$SiCl_2$+$SiCl_3$+SiCl) increases initially until approximately a P_{SiCl4} between 5-10 Torr and then begins to decrease similar to the behavior of the nanowire growth rate plotted in Figure **4-8**. Various other combinations are also plotted in Figure **4-9** below all show similar behavior.

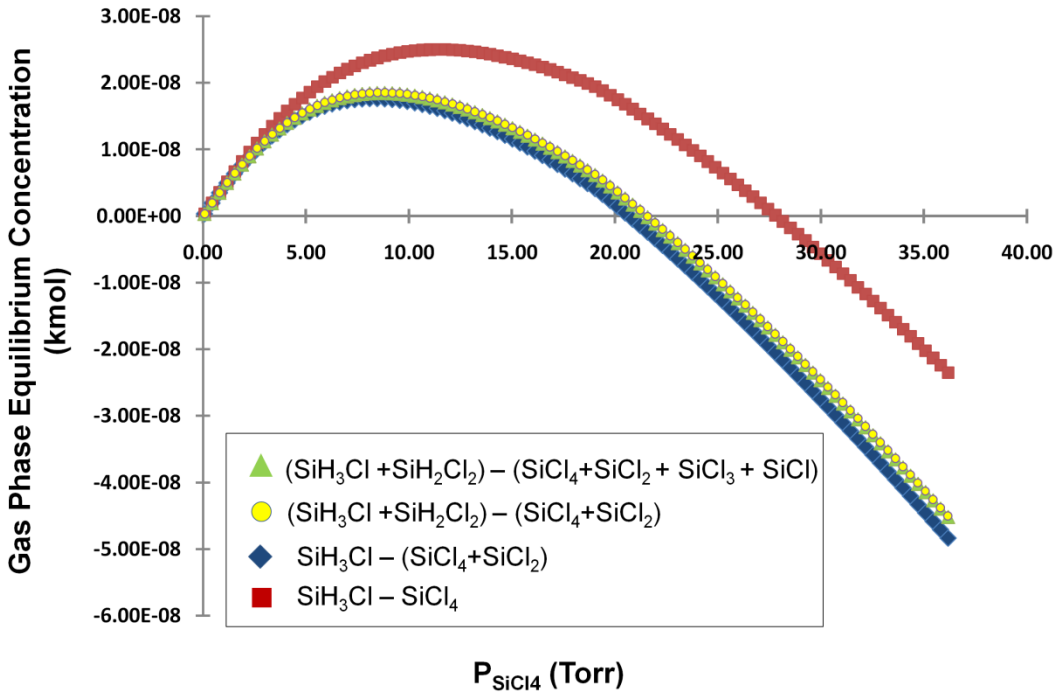


Figure **4-9**: The difference between the SiH_xCl_y and $SiCl_x$ gas phase equilibrium concentrations for increasing P_{SiCl4}.

The thermodynamic model above depicts the gas phase equilibrium concentrations for differences of SiH_xCl_y and $SiCl_x$. In the "growth" regime, the ΣSiH_xCl_y is > $\Sigma SiCl_x$. At a particular value of P_{SiCl4} the difference is at its maximum value, which is approximately at a P_{SiCl4} of 8-9 Torr. At a

P_{SiCl4} of 20-22 Torr the $\Sigma SiH_xCl_y = \Sigma SiCl_x$ and in the "etching" regime the $\Sigma SiCl_x$ become > than the the ΣSiH_xCl_y. This suggests that the SiH_xCl_y and $SiCl_x$ gas phase species are responsible for the competition between growth and etching. As the silicon growth rate begins to decrease due to etching, there becomes an increase in $SiCl_2$, $SiCl_3$ and SiCl species.

4.3.4 Carrier Gas Composition

Many of the chemical reactions in the Si-Cl-H system are dependent on the presence of hydrogen in the system. Since H_2 is a reactant in the process, the growth rate should be expected to vary with the partial pressure of H_2. To further investigate the change in growth rate with H_2 partial pressure, thermodynamic modeling was carried out to compare the gas phase species and analyze their effect on the growth of the SiNWs. Figure **4-10** shows the results for a P_{SiCl4} = 9.0 Torr and increasing amounts of H_2. The predicted amount of Si formed at a temperature of 1050°C increases as the amount of H_2 present in the carrier gas is increased until it reaches a maximum. Then the amount of Si predicted to form starts to decrease at higher concentrations of H_2, which may be due to an increase in the SiH_xCl_y gas phase species. This model suggests that lower amounts of H_2 may reduce the Si growth rate. The equilibrium gas phase concentrations suggest that as etching begins to dominate there is an increase in the SiH_xCl_y species concentrations and the solid silicon formation decreases. The decrease in silicon solid equals the amount of silicon acquired by these species. This shows that it could become more favorable to form the SiH_xCl_y species at higher P_{H2}.

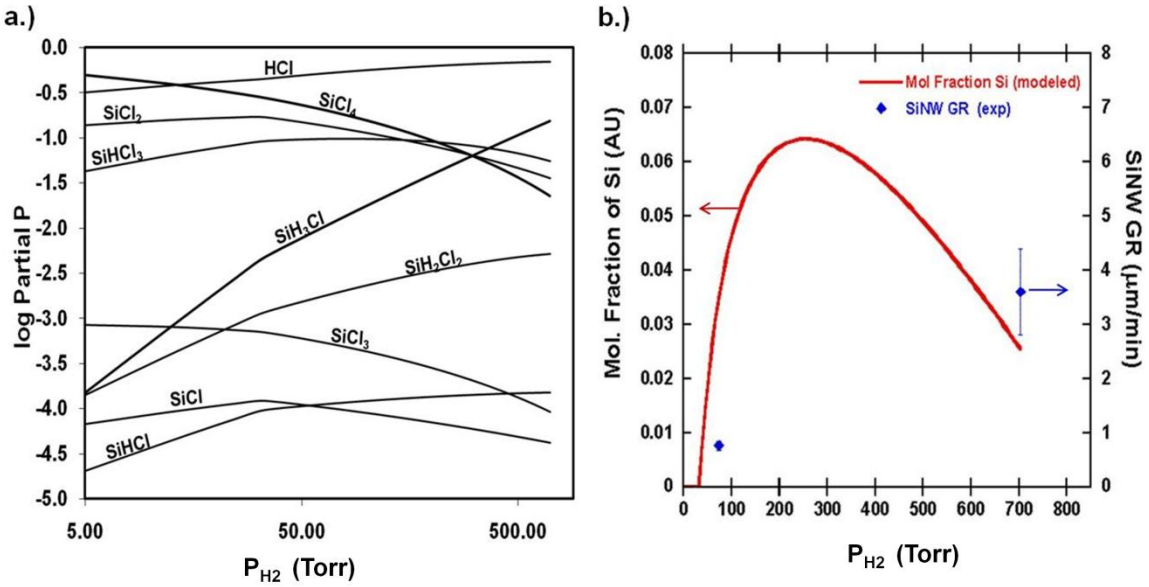


Figure **4-10**: a.) Gas phase species thermodynamically modeled using HSC chemistry for increasing P_{H2} at a steady P_{SiCl4}. b.) Comparison of model predictions and SiNW growth rate.

Experimental growths were carried out to verify the model predictions at 100% H_2 and 10% H_2 in Ar mixture were used as the carrier gases. A direct comparison between these two carrier gases was carried out on SiNWs grown at atmospheric pressure and a temperature of 950°C. Although the SiNW experiments were carried out at a growth temperature of 950°C, and the model used a temperature of 1050°C, the trends should be similar. The model could not be run at a temperature of 950°C since there is no solid Si predicted to form at this temperature. Nanowire growth most likely occurs at this temperature due to the presence of the Au catalyst. The growth rate obtained using a 10% H_2 in Ar carrier gas were reduced compared to the growth rate obtained using 100% H_2 as the carrier gas as shown in Figure **4-11**. These experiments were carried out to measure the growth rate versus P_{SiCl4} for both carrier gases. The results show that for both carrier gas compositions, the growth rate continues to increase with increasing P_{SiCl4} until it reaches a maximum value and then the growth rate decreases as it transitions into an etching dominated regime. However, for the 10 % H_2 in Ar the growth/etch curve shifts to a lower maximum growth rate and transitions into an etching regime at a lower P_{SiCl4}. The maximum

growth rate was ~4 μm/min reached at P_{SiCl4} at 3-6 Torr with 10% H_2 in Ar carrier gas as shown in Figure **4-11**.

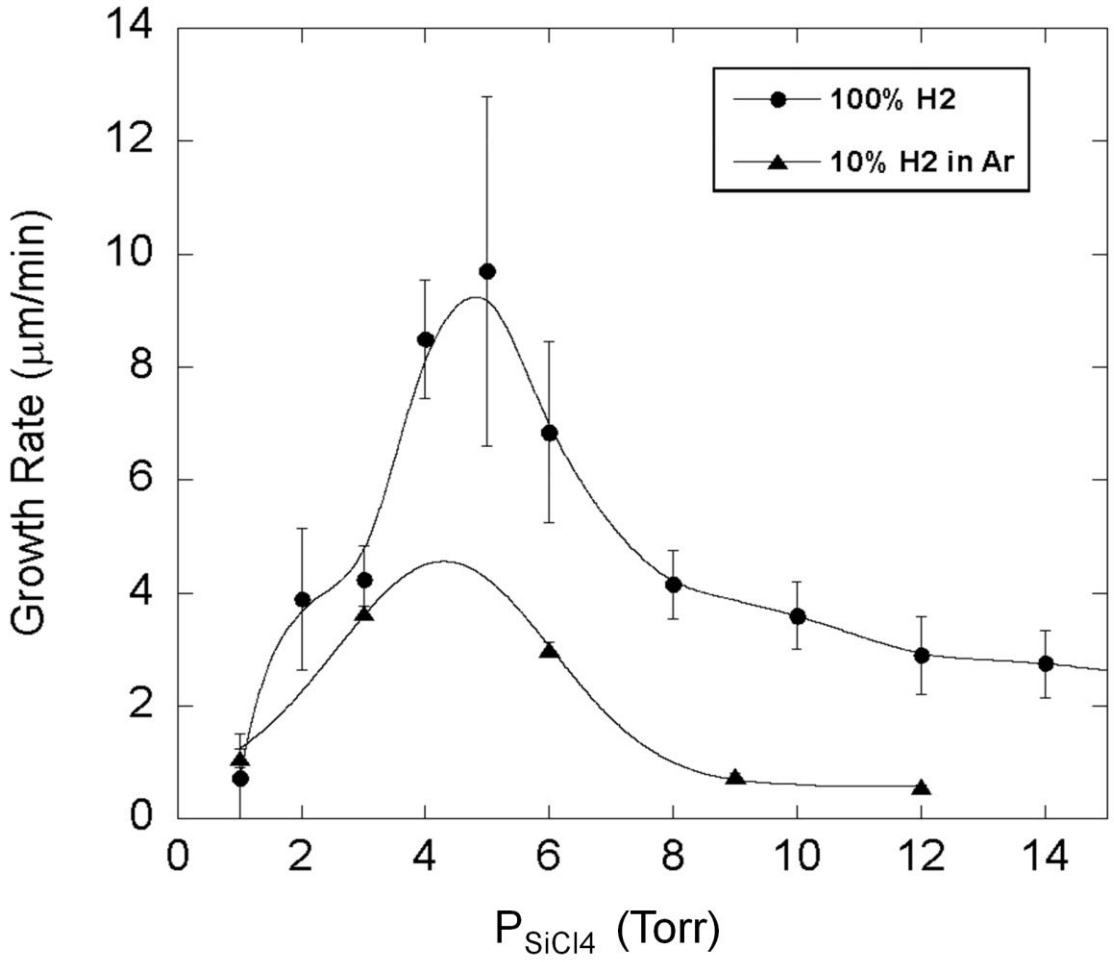


Figure **4-11**: Direct comparison of the SiNW growth rate vs. P_{SiCl4} for 100% H_2 vs. 10% H_2 in Ar carrier gas for SiNW arrays grown at atmospheric pressure, and 950 °C.

4.3. 5 Growth Rate versus Diameter Dependence

As discussed in section **2.3.3.3**, previous work has shown there is an opposing diameter dependence on growth rate that correlates with the P_{SiCl4} dependence. Givargizov reports an

increase in nanowire growth rate with increasing diameter and $P_{SiCl4.}$[12] Weyher reported a decrease in growth rate with increasing diameter and $P_{SiCl4.}$[13] A model developed by Schmidt et al. proposes that there is not only a diameter dependence but also a dependence on P_{SiCl4} as well.[23] In order to further investigate this opposing trend in diameter dependence, silicon nanowires were grown from a 3 nm Au thin film to measure growth rates and diameters. In order to determine a the nanowire diameters and their growth rates over large ranges, the 3 nm Au film was not annealed for 5 minutes at the growth temperature as other samples were. By starting growth immediately the Au did not have time to break up or for Ostwald ripening to occur, so a large diameter range was obtained. Silicon nanowires grown in this study were found to exhibit a growth rate dependence on the diameter. As can be seen in Figure **4-12**, the growth rate increased with increasing diameter. The plot (Figure **4-12b**) shows that while the growth rate is faster for wires grown with 100% H_2 both carrier gas compositions exhibit the same trend.

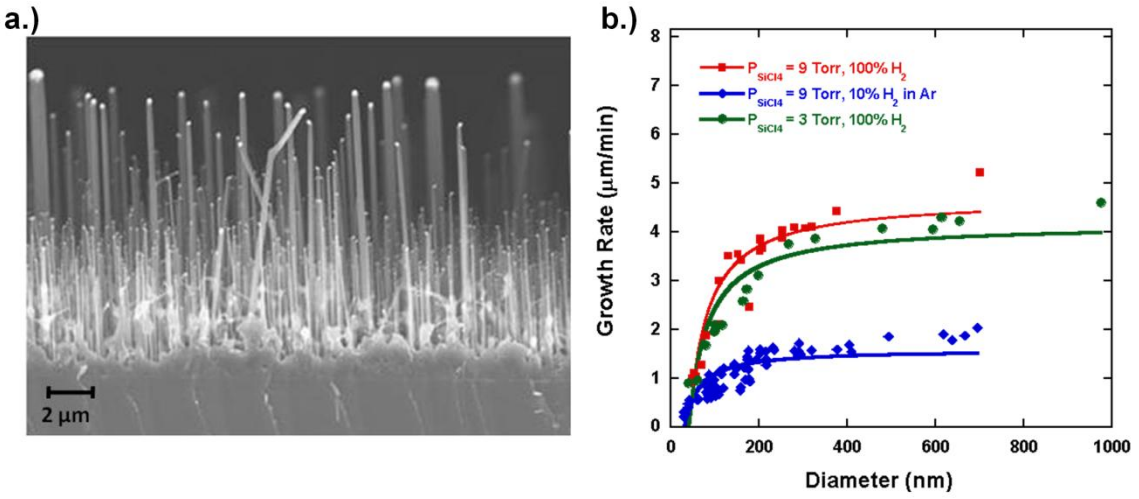


Figure **4-12**: a.) Cross-sectional FESEM image of a SiNW array grown using 10 % H_2 in Ar at 950 °C and atmospheric pressure showing diameter dependence to the growth rate. b.) SiNW growth rate vs. SiNW diameter for a low P_{SiCl4} = 3 Torr and high P_{SiCl4} = 9Torr using 100 % H_2 and a high P_{SiCl4} = 9 Torr using 10 % H_2 in Ar.

The observed trend is consistent with results reported by Givargizov et al. and as expected from the Gibbs-Thomson effect.[12] The model developed by Schmidt et al. was used to fit the growth rate versus nanowire radius data seen in Figure **4-12 (b)**.[23] The growth rate was given by equation 4.9:

$$v = v_0 + \Gamma \frac{2\Omega^s \sigma^s}{r} \tag{4.9}$$

where v_0 is the growth rate as $r \rightarrow \infty$, Ω^s is the atomic volume of a solid Si nanowire, σ^s is the specific free energy of the nanowire surface (vapor-solid interface) and Γ is defined as:

$$\Gamma = \frac{\omega_1 \alpha_1}{\omega_1 - \alpha_1} \tag{4.10}$$

where α_1 is the slope of the incorporation velocity (α), with the supersaturation (μ_{ls}) and ω_1 is the slope of the crystallization velocity (ω), with the supersaturation (μ_{ls}). As can be seen in the graph, the model results fit relatively well to the growth rate data. For 100 % H_2 carrier gas at P_{SiCl4} = 9 Torr, v_o was 4.7 μm/min +/- 0.14μm/min and for a P_{SiCl4} = 9 Torr and 10% H_2 in Ar carrier gas, v_o was 1.6 μm/min +/- 0.04 μm/min. The fitting parameter Γ was $-4x10^{-3}$ mmol s^{-1} J^{-1} and $-1x10^{-3}$ mmol s^{-1} J^{-1} for 100% and 10 % H_2 respectively. At low P_{SiCl4} = 3 Torr and 100% H_2, v_0 = 4.2 μm/min +/- 0.18 μm/min and Γ was $-4 x10^{-3}$ mmol $s^{-1}J^{-1}$. Γ is less than zero, which implies that the growth rate should increase with increasing wire diameter, which is in agreement with the experimental results. In Figure **4-12(b)** the model fits very well at nanowire diameters around and below 300 nm. The model begins to level off but the experimental data for both 100% and 10% H_2 still continues to increase slightly. This may be occurring because as the larger

SiNWs have a higher growth rate they also have a more direct supply of Si than the smaller diameter, which may reduce the growth rate. From equation 4.7, a faster growth rate for larger diameters would decrease the boundary layer compared to the slower growing SiNWs. That could explain the slight increase in the larger diameter wires compared to the model.

Schmidt also proposed that the P_{SiCl4} is correlated to the diameter dependence; however, the data obtained in this study shown in Figure **4-12(b.)** was obtained at a P_{SiCl4} of 9 Torr, which is in the etching regime where growth rate decreases with increasing P_{SiCl4}. To further investigate the P_{SiCl4} dependence, the growth rate with respect to nanowire diameter was compared for low silicon tetrachloride partial pressure (P_{SiCl4}=3 Torr), also shown in Figure **4-12(b)** below. The growth rate increases with increasing diameter similar to the data obtained at high P_{SiCl4} concentrations in the etching regime. This suggests that there is no dependence on silicon tetrachloride partial pressure.

4.3. 6 Effect of Inlet Distance and Residence Time

All previous experiments were carried out with the quartz boat containing the samples in the center of the hot zone with a total flow rate of 100 sccm passing over the samples during growth. The hotzone is defined as the point in the tube that has a constant temperature and was described in detail in section **3.3.1.3**. Figure **3-10** shows a plot of temperature versus position in the furnace. During growth runs, Si deposits can begin to accumulate on the quartz tube; however, it was observed that the deposits occur at the edge of the hotzone, closest to the inlet. In order to try and better control the growth rate and orientation of the nanowire arrays, a series of experiments studying the effect of residence time and boat position on nanowire growth were carried out. A schematic of the different boat and sample positions is shown in Figure **4-13**

below. The orange area in Figure **4-13(a.)** depicts where the hotzone is compared to the boat position. Boat #2 was slightly outside of the hotzone.

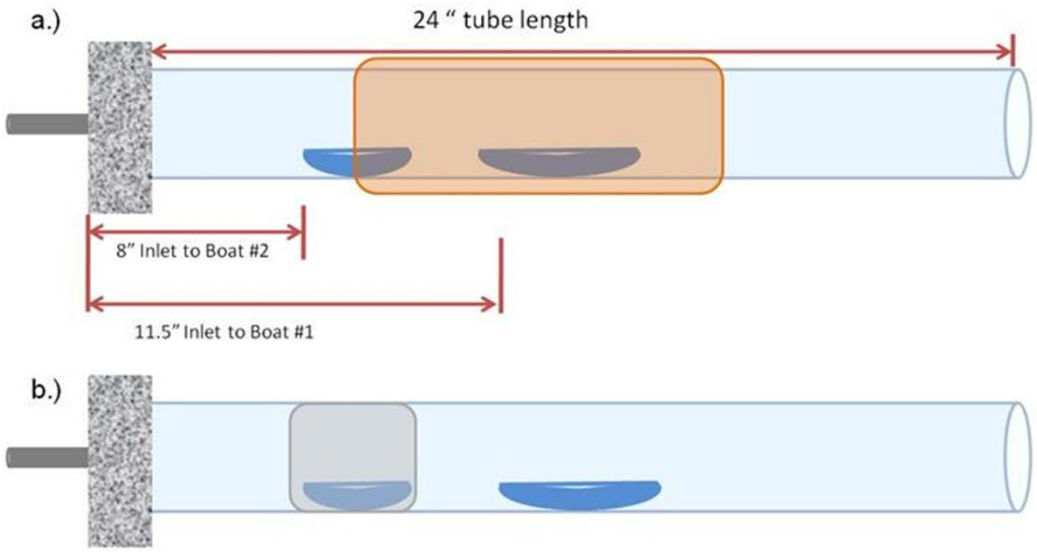


Figure **4-13**: Schematic showing a.) the location of the quartz boats during the experiments in reference to the hotzone and b.) the location of where the Si tube deposits were located in reference to the boats and gas inlet.

A total of 4 substrates were placed along the length of the boats and were labeled sample A, B, C, D, and were 8.5", 9", 11" and 12" away from the inlet respectively. In order to examine the effect of boat position, growth experiments were carried out in which the P_{SiC4} was 3.6 Torr and a total flow 100 sccm at a hotzone temperature of 950°C. Figure **4-14** shows representative SEM images of samples A, B, and C. Sample D had the same growth rate and % of wire orientation as sample C. Sample A, which was closest to the gas inlet had a growth rate of 3.1 +/- 0.07 μm/min. While in the same boat but ~ 0.5 " further away from the inlet, sample B had a faster growth rate of 6.0 +/-0.09 μm/min. The main difference between these two samples is that sample A was slightly outside of the hotzone and therefore at a lower temperature. The temperature of sample A was approximately from 935-945°C compared to 950°C in the hotzone. As the samples get

further from the inlet the growth rate increases and then begins to level out. Sample C and D had a growth rate of 4.6 +/- 0.09 µm/min.

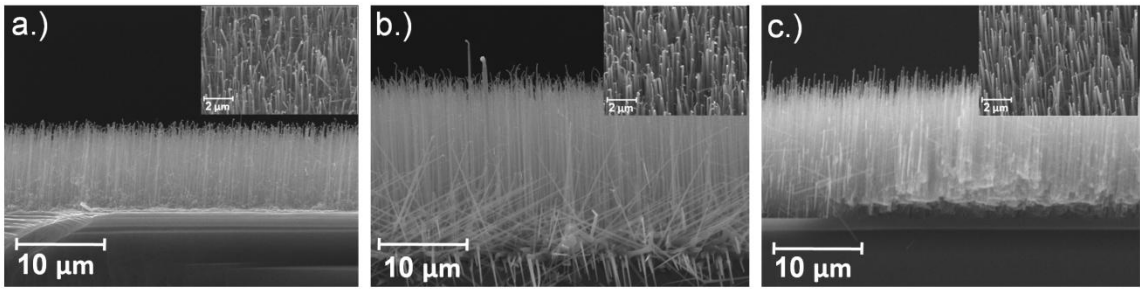


Figure **4-14**: SEM micrographs showing both a cross-section and top down (inset) of a.) sample A closest to the inlet b.) sample B and c.) sample C. Samples were grown at 950°C, total flow of 100 sccm, and P_{SiCl4}=3.6 Torr.

A plot of growth rate versus distance from the inlet is shown in Figure **4-15**. Since nanowire growth is dependent on the gas phase species and there is a constant competition between the growth and etching, it makes sense there is a change in growth rate with respect to the gas inlet distance. The growth rate just outside of the hot zone is the lowest, once in the hotzone more $SiCl_4$ breaks down allowing more Si in the gas phase. This is most likely not due to the sample outside the hotzone having a slightly lower temperature as the growth rate does not vary much with temperature (Figure **4-6**) Sample C and D have identical growth rates and % orientation; this is most likely due to the gases reaching equilibrium at this point in the reactor. Further investigation was carried out in the center of the hot zone, at the same location as samples C and D.

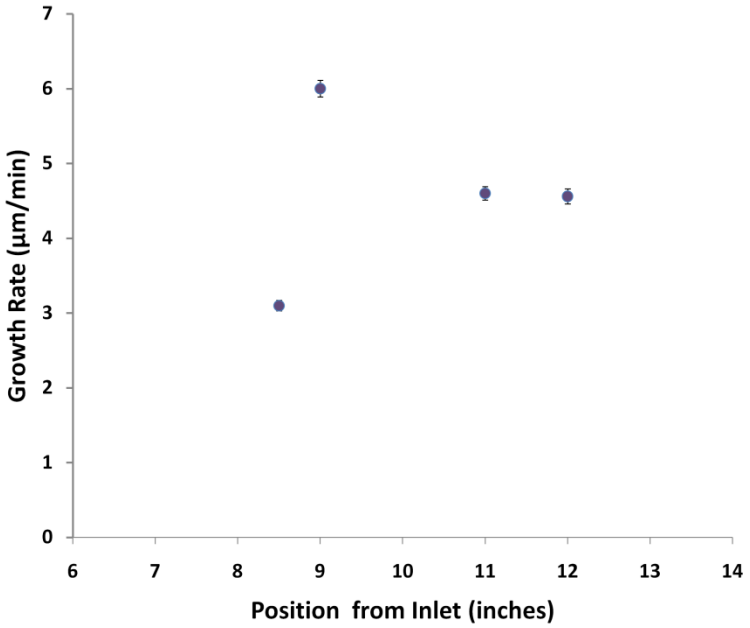


Figure **4-15**: Growth rate versus position from gas inlet showing an increase then decrease in nanowire growth rate with respect to position in the tube during growth.

Adjusting the total flow rate of gases over the samples in the growth chamber changes the gas residence time (t_{res}), which is essentially the time that the gases spend in the reactor. The residence time and gas velocity were calculated using the equations 4.11 and 4.12 respectively below, where the v_{tube} (cm^3) is the tube volume, A_{tube} (cm^2) is the cross-sectional area of the tube and F_{gas}(sccm) is the total inlet gas flow rate into the tube. Where the units sccm is the flow rate at standard temperature and pressure and therefore must be corrected. P_o and T_o are the standard temperature and pressure values of 273 K and 760 Torr, while P and T represent the temperature and pressure at growth conditions. These calculations were done assuming ideal gas conditions.

$$t_{res} = \frac{v_{tube}}{F_{gas}} \times \frac{P_o}{P} \times \frac{T}{T_o} \qquad (4.11)$$

$$v = \frac{F_{gas}}{A_{tube}} \times \frac{P_o}{P} \times \frac{T}{T_o} \qquad (4.12)$$

For all these experiments, the temperature was held constant at 950 °C and atmospheric pressure. The volume of the tube (v_{tube}) was191.5 cm^3, the area (A_{tube}) was 3.14 cm^2. The temperature T was 1223 K, T_0 = 273 K, and the pressure P = 730 Torr and P_0=760 Torr. As the total flow of the reactor is increased, the residence time decreases from 1071 seconds at a total flow of 50 sccm to 107 seconds at a total flow of 500 sccm, which means that the gas spends less time in the hot zone of the reactor. As can be seen in Figure **4-16**, as the total gas flow over the nanowire samples is increased the growth rate decreases.

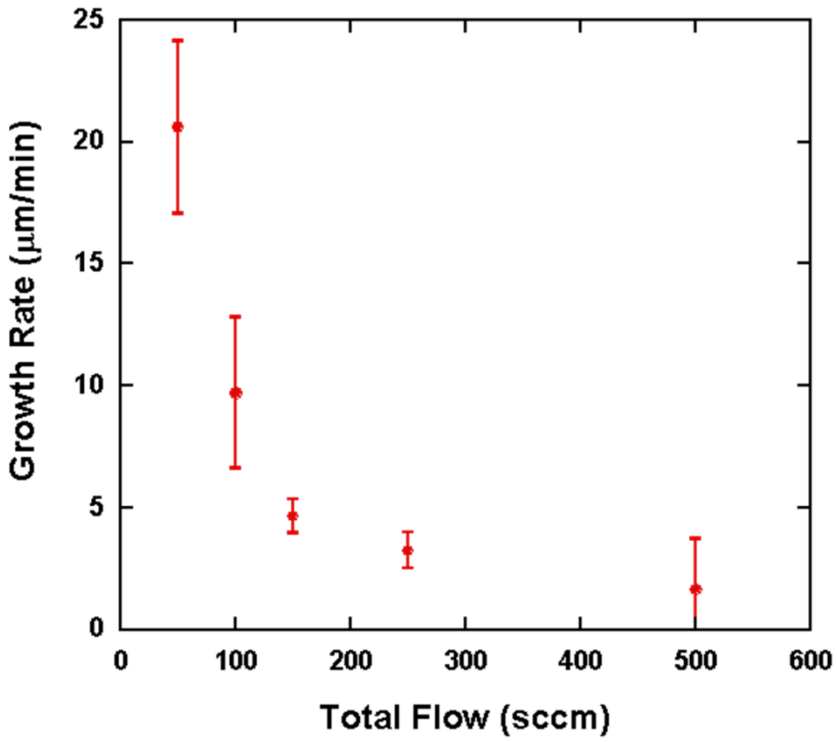


Figure **4-16**: Graph of SiNW growth rate versus total gas flow at 950°C.

The nanowires all had a large fraction of orientation with respect to the nanowire surface and average diameters of approximately 120 +/- 30 nm. Plots of growth rate versus v_{gas} and growth rate versus residence time (t_{res}) are shown in Figure 4-**17 (a)** and **(b)**. As the total gas flow is increased from 50-500 sccm the gas velocity increases causing gases to flow faster over the samples, thus decreasing the boundary layer thickness based on the equation 4.13:

$$\delta = \frac{10}{3}\frac{L\sqrt{\eta}}{\sqrt{v_0 \rho L}} \tag{4.13}$$

where δ is the boundary layer thickness, L is the distance along the tube, η and ρ are the viscosity respectively, and v_0 is the gas velocity. As the gas velocity is increased due to an increase in the total flow (F_{gas}), the boundary layer thickness decreases and then using equation 4.6 shows that the gas flux to the substrate surface increases which should cause the growth rate to increase. Experimentally the opposite trend is observed (Figure **4-17(a)**), which may be explained by the decrease in residence time as the total gas flow (F_{gas}) is increased. In this case there is less time for gases to reach equilibrium. Figure **4-17(b)** shows an increase in growth rate for longer residence times. This indicates that as the total gas flow rate (F_{gas}) increases the growth rate will decrease due to smaller residence times.

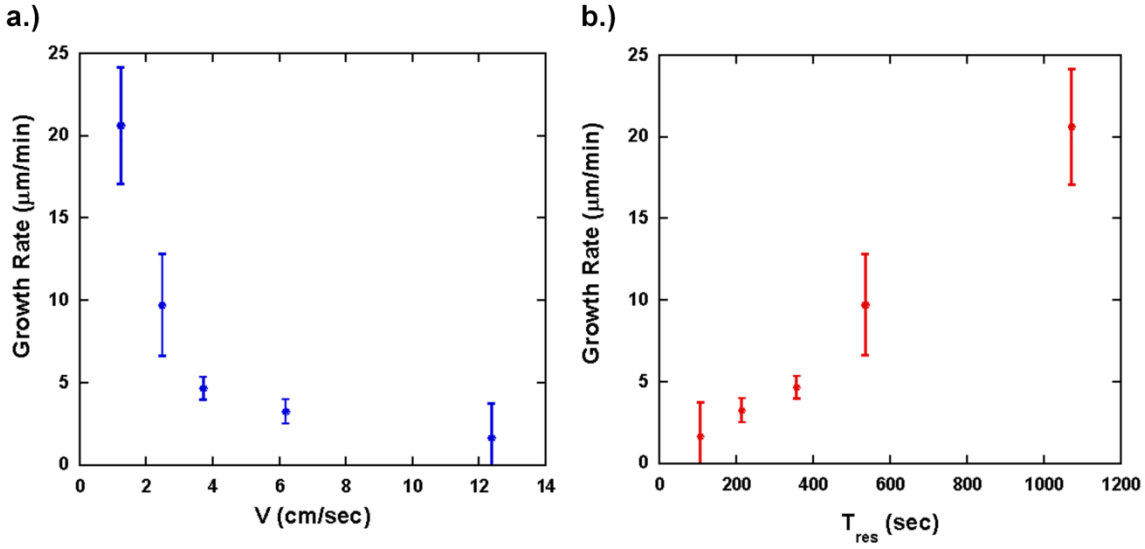


Figure **4-17**: Graph of growth rate obtained at 950°C versus a.) gas velocity (v_{gas}) and b.) residence time (t_{res}).

4.4 Structural Properties of Silicon Nanowire Arrays

The structural properties of the SiNW arrays were examined using the Phillips 420 TEM by Dr. Bangzhi Liu, Haoting Shen, Dr. Qi Zhang and Dr. Beth Dickey. The most controllable SiNW arrays with the best orientation were grown at high P_{SiCl4} concentrations with either 100% H_2 or a 10% H_2 in Ar mixture and examined by TEM. Representative images of these samples were shown in Figure **4-6**.

Initial TEM characterization of the SiNW arrays grown using $SiCl_4$ showed that the wires have a negligible surface oxide and little to no Au visible at the nanowire tips. Figure **4-18** shows a TEM micrograph of a SiNW grown using a P_{SiCl4} = 3 Torr and a temperature of 900°C. There is a small area of Au is visible, however, the Au tip is not present.

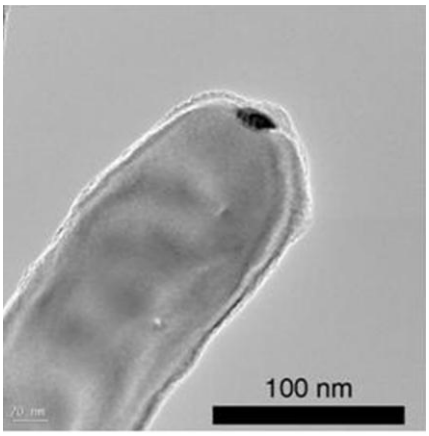


Figure **4-18**: TEM image by Dr. Bangzhi Liu of a typical SiNW tip grown using a P_{SiCl4} = 3 Torr at 900°C in 100 % H_2 carrier gas.

One important observation to note is the fact that there is a very thin (~2 nm) surface oxide present in the photo, which may have formed after growth. Kodambaka *et al*. reported a reduction in the diameter of the Au tip during SiNW growth which was attributed to the diffusion of Au down the sides of SiNWs grown with SiH_4 under UHV conditions ($1x10^{-8}$ Torr) when there was no oxide present on the wire surface.[24] The study was carried out by imaging nanowire growth in a TEM equipped for CVD growth. In these experiments, it is important to note that the growth rate was very low (5-8 nm/min) so substantial Au diffusion was likely to occur during NW growth. When a small oxygen partial pressure was added during growth, there was no loss of Au from the tip indicating that the surface oxide inhibited Au diffusion. In our experiments, the nanowire diameter is uniform from the base to the tip indicating that there is little or no Au loss occurring during growth. The Au loss from the tip is believed to occur primarily during cooldown after growth. This may be due to the difference in growth rate of our SiNWs grown using $SiCl_4$ which is ~1000-7000 nm/min, and is faster than the 5-8 nm/min growth rate reported for the wires grown by Kodambaka *et al*. Consequently, the faster growth rate allows less time for Au diffusion down the side of the nanowire during growth. Figure **4-19** shows two FESEM images

from a fast cooldown of 50°/min from 900°C to room temperature and also a slow cooldown of 15°/min.

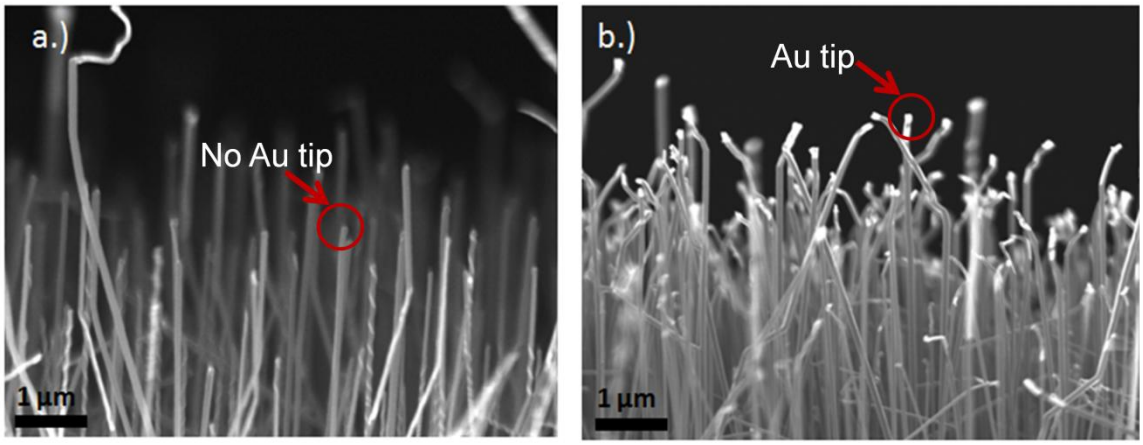


Figure **4-19**: FESEM images of SiNWS after a slow cooldown (a.) and a fast cooldown (b.).

From the FESEM images, the fast cooldown shows that there is more Au present at the tips of the SiNWs and for the slow cooldown there does not appear to be much Au at the nanowire tips. TEM of both the slow and the fast cooldown shows that even for the fast cooldown the Au is near the tip but has already started to diffuse down the length of the SiNW.

For SiNWs grown using SiH_4, significant Au loss from the tip is not commonly observed, however, the growth temperature is lower (500°C) than that used with $SiCl_4$. Surface migration of Au along silicon nanowire sidewalls has been reported by various groups growing under UHV conditions.[25,26] Since Au diffusion of the nanowire tip appeared to occur during cooldown, all further samples were cooled as fast as the reactor would allow (~50°/min) to minimize Au diffusion.

Samples grown using a 100% H_2 carrier gas were examined at both a low and high P_{SiCl4} to determine if etching of the sidewall was occurring at higher $SiCl_4$ concentrations. Figure **4-20** shows TEM images from a SiNW grown at a low P_{SiCl4} in 100% H_2. This particular sample was

grown at a temperature of 950°C, although there were no discernable differences in the structural properties of the SiNWs grown at other temperatures from 800-1000°C.

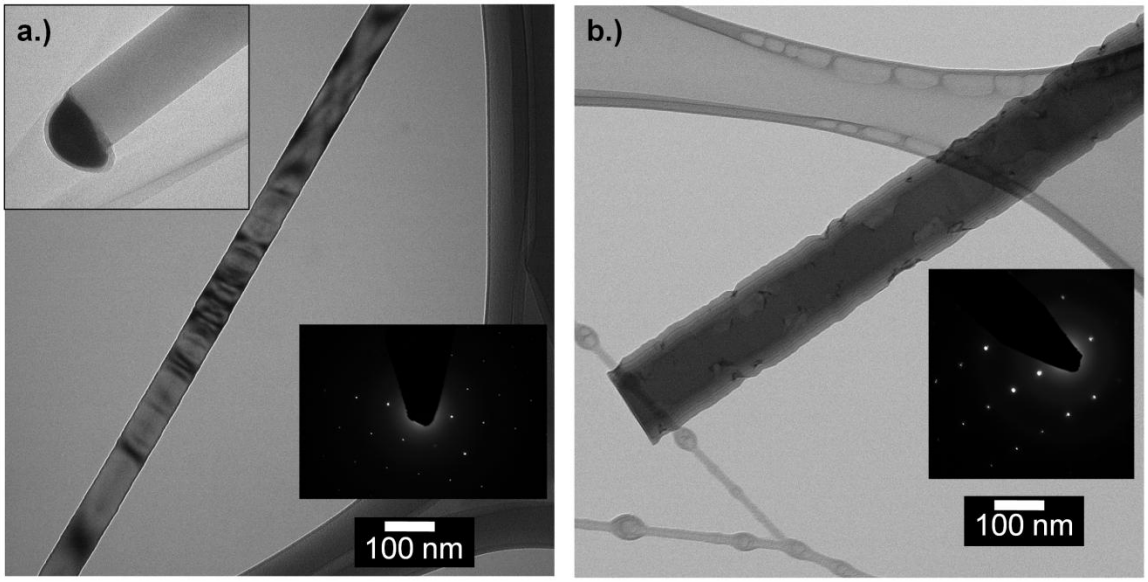


Figure **4-20**: TEM images obtained by Haoting Shen showing a.) SiNW tip and middle of nanowire and b.) the base of a SiNW for a P_{SiCl4} = 3 Torr with 100% H_2.

As can be seen from Figure **4-20(a)**, the nanowire surface is smooth and there does not appear to be much etching of the nanowire. Some of the nanowires do show a slight amount of tapering and some surface roughness at the nanowire base as shown in Figure **4-20(b)**. Regardless of the conditions, the nanowires are single crystal and 95% of the SiNWs are growing in the <111> direction. For these samples over 50 nanowires were measured to obtain the most common growth directions. There is little to no oxide present on the SiNW surface. Figure **4-21** shows a tip of a nanowire grown using 100 % H_2 at a high P_{SiCl4} = 10 Torr. The nanowire surface is also relatively smooth and does not show any significant etching as compared to the sample grown at P_{SiCl4} = 3 Torr.

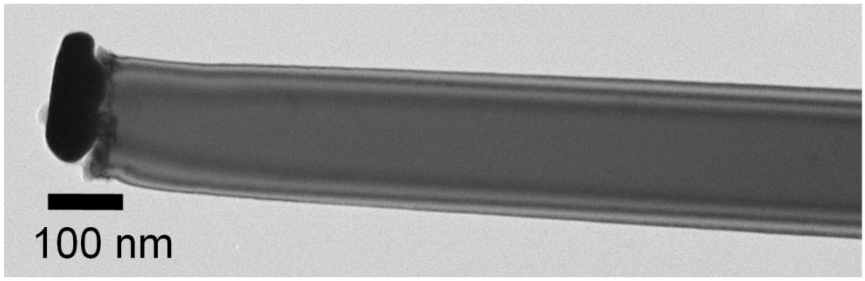


Figure **4-21**: TEM image of a SiNW tip grown using 100% H_2 at 950°C and a P_{SiCl4} = 10 Torr obtained by Haoting Shen.

The main difference between the nanowires grown at low P_{SiCl4} = 3 Torr and the nanowires grown at higher P_{SiCl4} = 10 Torr is the shape of the tip. Wires grown using high silicon tetrachloride partial pressures appear to have almost flat Au tips. The reason for the change in tip shape is not entirely understood, although it may be due to a change in surface tension if there is increased Cl present on the surface of the nanowire and/or in the Au tip at higher P_{SiCl4}.

Based on experimental and modeling studies carried out for SiNW growth using $SiCl_4$, it was determined that P_{SiCl4} and also the concentration of H_2 in the carrier gas have the most effect on the wire growth rate. It appears that higher P_{SiCl4} grown samples do not appear to have any additional surface roughness or visible sidewall etching. Samples grown using a 10% H_2 in Ar carrier gas were then examined to determine if the carrier gas had an adverse effect on the SiNWs. Figure **4-22** below shows low magnification and high magnification TEM images of SiNWs grown at a temperature of 950°C using a 10% H_2 in Ar gas mixture.

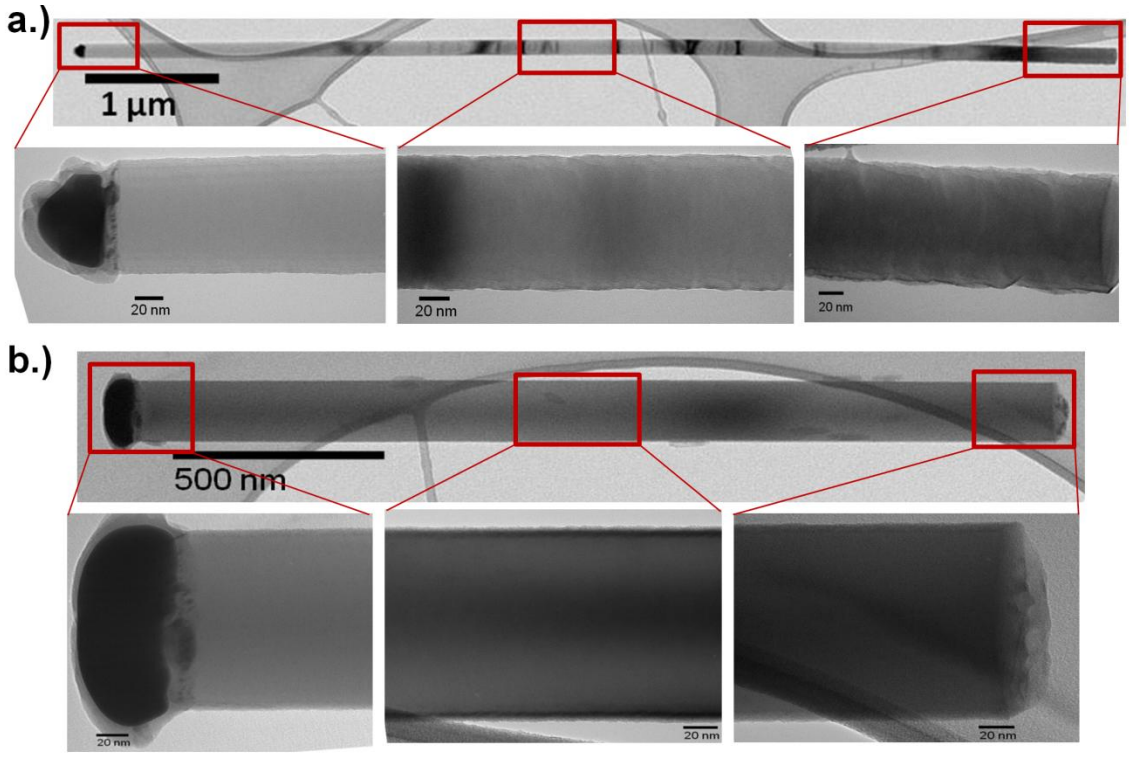


Figure **4-22**: TEM images of SiNWs grown at 10% H_2 in Ar and a low P_{SiCl4} = 3 Torr at a.) low magnification showing the entire wire and high magnification of the tip, middle and base of the nanowire. Image b.) shows a low magnification of a SiNW grown at 10% H_2 in Ar at a high P_{SiCl4} = 9 Torr at 950°C with a high magnification of the tip, middle and nanowire base. Images were taken by Haoting Shen.

As can be seen in the images, the wires appear similar to those grown with 100% H_2 shown in Figures **4-20 and 4-21**. There is some surface roughness present at the nanowire base; however, the change in P_{SiCl4} from a growth to etch regime does not appear to have any adverse effects on the nanowire surface. It does appear that in both the case of 100% H_2 (Figure **4-21**) and 10% H_2 in Ar, the nanowires grown at higher silicon tetrachloride partial pressures have non-hemispherical tips. The Au volume at the nanowire tip was estimated based on the Au tip dimensions and in all cases the volume was 1×10^5-5×10^5 nm^3, which suggests that Au diffusion down the nanowire from the tip is not causing the change in shape. Other possible explanations for this could be due to a change in the catalyst composition such as an increase in Cl or due to enhanced Au diffusion at higher P_{SiCl4}.

4.5 p-type doping of SiNWs

In order to achieve a working photovoltaic device, it is essential to have knowledge of the structural and electrical properties. While a number of studies have focused on the VLS growth of Si whiskers or nanowires using $SiCl_4$, there has been little work to develop in-situ techniques to dope the wires p-type or n-type. The ability to control the dopant/Si precursor ratio and thus control the resistivity of the nanowires will be essential to ultimately create a radial p-n junction solar cell. Initial studies were carried out in collaboration with Rebeca Diaz and Dr. Theresa Mayer to determine the resistivity of undoped SiNWs grown with $SiCl_4$ on (111) Si substrates in order to evaluate the background dopant concentration in the wires. The measurements were carried out on undoped SiNWs grown at a P_{SiCl4} =3.6 Torr at 950°C.

Gated I-V measurements revealed that the SiNWs grown with $SiCl_4$ are nominally p-type as shown in Figure **4-23**. Electrical characterization was conducted using a back-gated structure that includes topside source (S) and drain (D) electrodes and two additional voltage probes. Further details on the back gated structure can be found in Rebeca Diaz's thesis.[28]

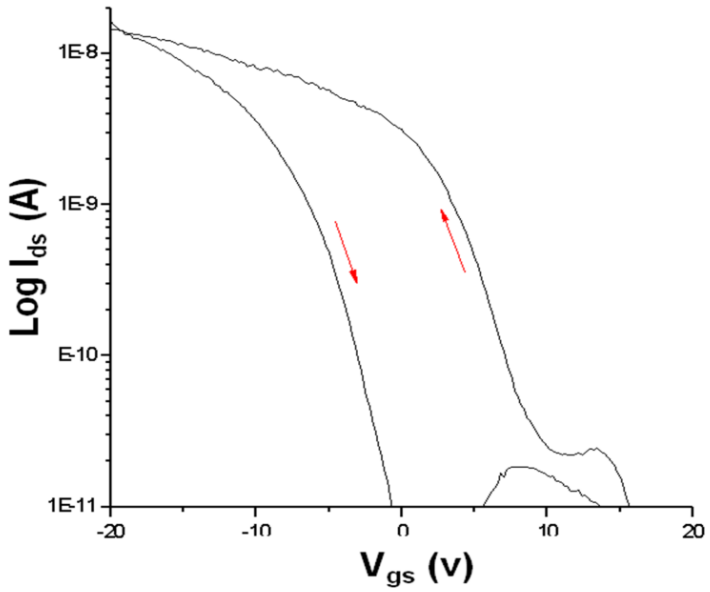


Figure **4-23**: Gated I-V measurements of undoped $SiCl_4$ grown SiNWs indicating p-type behavior.

The four point measurements indicated that the SiNW resistivity is in the range of 430 – 6100 Ω-cm. Assuming bulk mobility, this indicates an upper hole concentration of $5\times10^{14}cm^{-3}$.[29] The resistivity of intrinsic Si is 2×10^{6} Ω-cm, which indicates the wires have a lower resistivity than intrinsic bulk Si, which is likely due to the presence of a small amount of unintentional acceptors. This result indicates that the nominally undoped wires have a low background doping level and that it should be possible to change the nanowire resistivity by adding intentional dopants.

Initial p-type in-situ doping experiments were carried out using a 0.5% TMB in H_2 lecture bottle, and the lowest TMB/$SiCl_4$ ratio obtained with this concentration was 0.1. However, all single nanowire electrical measurements made showed using this ratio were highly doped with an average resistivity of 3×10^{-3} Ω-cm and assuming bulk mobility have a hole concentration of approximately $10^{20}cm^{-3}$.[29] Variation of the TMB/$SiCl_4$ ratio did not yield any change in the

doping. This lead to the lowering of the TMB cylinder concentration by installing a 100 ppm TMB in H_2 lecture bottle.

A series of SiNW arrays were grown at 950 °C, atmospheric pressure and a P_{SiCl4} = 12 Torr. The carrier gas used was a 10% H_2 in Ar mixture. The TMB/$SiCl_4$ ratio was varied from 8×10^{-5} to 2×10^{-3} in an attempt to controllably vary the doping and subsequently the nanowire resistivity. Based on the previous TMB/$SiCl_4$ ratio of 0.1 and a measured resistivity of $3x10^{-3}\Omega$-cm, the expected value for a TMB/$SiCl_4$ ratio of 8×10^{-5} is approximately $2\times10^{-1}\ \Omega$-cm and for a TMB/$SiCl_4$= 2×10^{-3} a resistivity of approximately $3\times10^{-2}\ \Omega$-cm was expected. Figure **4-24** is a plot of the SiNW growth rate versus TMB/$SiCl_4$ ratio for samples grown using both 100% H_2 at a temperature of 1050°C and also using 10 % H_2 in Ar at a temperature of 950°C.

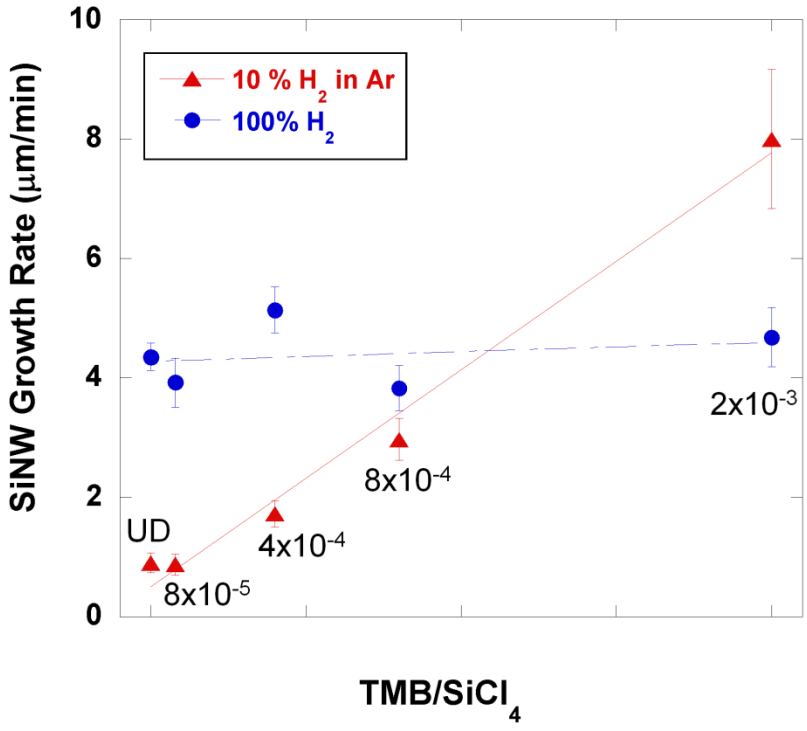


Figure **4-24**: Plot showing change in growth rate with respect to the TMB/$SiCl_4$ doping ratio.

The samples grown using a 10% H_2 in Ar carrier gas produced SiNW arrays with higher growth rates as the TMB/$SiCl_4$ ratio was increased. While samples grown using a 100 % H_2 carrier gas showed no large variation in growth rate with respect to the TMB/$SiCl_4$ ratio. The increase seen for the 10% H_2 in Ar carrier gas is most likely due to an increase in the amount of H_2. The flow rate of 100 ppm TMB in H_2 was 1.3 sccm for a TMB/$SiCl_4$ ratio of 8×10^{-5} and a P_{H2} of 80 Torr. For higher TMB/$SiCl_4$= 2×10^{-3} the TMB in H_2 flow rate was 25 sccm and the P_{H2} in the reactor of 235 Torr. The P_{H2} in the reactor increases with increasing TMB/$SiCl_4$ ratio for a 10% H_2 in Ar carrier gas and based on Figure **4-11** indicates that in this range of P_{H2} (80-235 Torr) the growth is increasing with increasing P_{H2}.The amount of 100 ppm TMB in H_2 added into the reactor to increase the TMB/$SiCl_4$ ratio increased the amount of H_2 present in the gas phase species, which based on the gas phase modeling will also increase the Si solid predicted to form. In the case of 100% H_2, the increased amount of TMB in H_2 added to the reactor did not substantially change the amount of H_2 present enough to drastically alter the growth rates.. Since the P_{H2} is not varied greatly with 100% H_2 as the carrier gas, the growth rate also does not vary greatly as the 100ppm TMB in H_2 is changed.

Four-point resistivity measurements were carried out on this set of samples by Chad Eichfeld and were carried out at three points along each nanowire and FESEM was used to measure the gaps and contact widths. The resistivity was measured at a current of 0.1 nA and a pulse width of 100 ms. The I-V curves were linear indicating that current was passed through all of the probes indicating that there were no open circuits. For these measurements there was no back gate to determine the carrier type. The highest doping ratio was a TMB/$SiCl_4$ = 2×10^{-3} and the average resistivity was found to be 1.26×10^{4} +/- 6.1×10^{3} Ω-cm. This is similar to the resistivity of undoped SiNWs grown using $SiCl_4$ measured above, indicating that there is very little B incorporation in the nanowires. This does not agree with the expected resistivity of

$3\times10^{-2}\Omega$-cm and may be caused by depletion of the TMB at these growth temperatures so that boron is not making it into the nanowires. A TMB tank with a concentration higher than 100ppm but lower than 0.5% in H_2 may be required to obtain control over the doping using $SiCl_4$.

4.6 Conclusions

It was demonstrated that SiNW growth from $SiCl_4$ under the conditions used in this study is dependent on gas phase thermodynamics and the balance of the Si formation and etching reactions similar to that observed for Si thin film deposition. Temperature was found to increase the growth rate slightly, which is consistent with mass transport. Increasing the P_{SiCl4} increases the growth rate initially and then transitions into an etching dominated regime. The experimental results were qualitatively consistent with the amount of solid Si predicted to form at equilibrium. The modeling also demonstrated that a change in the partial pressure of H_2 in the carrier gas leads to a shift in the growth/etch curves. In an etching dominated regime the gas phase concentrations of SiH_3Cl, SiHCl, SiH_2Cl_2, $SiCl_2$ and SiCl species increase thus taking Si away from the catalyst. This combined with a reduction in H_2 accounts for the shift in growth/etch curves. By varying the inlet concentrations of $SiCl_4$ and H_2, it is possible to tune the nanowire growth rate over a wide range (0.3-10 μm/min) enabling the growth of epitaxially oriented SiNW arrays with wire lengths greater than 50 μm which are of interest for the fabrication of high aspect ratio solar cell devices. TEM characterization has shown for varying conditions there is no significant change in the structural properties of the nanowire. There does not appear to be any increased roughening or etching of the nanowire sidewalls with respect to carrier gas or $P_{SiCl4.}$

Samples were also doped in-situ p-type through the addition of TMB during growth. Varied TMB/$SiCl_4$ and carrier gas concentrations were explored. Single nanowire resistivity was also measured to determine if a change in TMB would correlate to a change in resistivity. For a

TMB/$SiCl_4$=0.1 a resistivity of 3×10^{-3} Ω-cm was measured and a TMB/$SiCl_4$=2×10^{-3} yielded a resistivity of 1.26×10^{4} Ω-cm. This indicates that boron may not be incorporated into the SiNWs at a temperature of 950°C and lower concentrations. Growth rate of the silicon nanowires did not vary with the addition of TMB, when using a 100% H_2 carrier gas. A 10% H_2 in Ar carrier gas significantly reduced the P_{H2} so that addition of TMB in H_2 yielded a change in growth rate. Although the TMB doping can be carried out to still obtain oriented samples, there does not appear to be a change in resistivity with the 100ppm TMB concentration. This can be solved by increasing the TMB tank concentration. Through the exploration of various growth conditions and parameters the growth of highly oriented free-standing SiNW arrays has been better understood without the use of a template.

4.7 Reference

1 A. I. Hochbaum, R. Fan, R. R. He, and P. D. Yang, Nano Lett. **5,** 457-460 (2005).
2 B. M. Kayes, H. A. Atwater, and N. S. Lewis, J. Appl. Phys. **97** (2005).
3 Y. J. Zhang, Q. Zhang, N. L. Wang, Y. J. Yan, H. H. Zhou, and J. Zhu, J. Cryst. Growth **226,** 185-191 (2001).
4 B. M. Kayes, M. A. Filler, M. C. Putnam, M. D. Kelzenberg, N. S. Lewis, and H. A. Atwater, Appl. Phys. Lett. **91** (2007).
5 S. Sharma, T. I. Kamins, and R. S. Williams, Appl. Phys. A-Mater. Sci. Process. **80,** 1225-1229 (2005).
6 K. K. Lew and J. M. Redwing, J. Cryst. Growth **254,** 14-22 (2003).
7 R. S. Wagner and W. C. Ellis, Appl. Phys. Lett. **4,** 89-& (1964).
8 D. W. F. James and C. Lewis, British J. of Apl. Phys. **16,** 1089-& (1965).
9 Givargiz.Ei and N. N. Sheftal, J. Cryst. Growth **9,** 326-& (1971).
10 R. S. Wagner, J. Appl. Phys. **38,** 1554-& (1967).
11 R. S. Wagner and C. J. Doherty, J. Electrochem. Soc. **113,** 1300-& (1966).
12 E. I. Givargizov, J. Cryst. Growth **31,** 20-30 (1975).
13 J. Weyher, J. Cryst. Growth **43,** 235-244 (1978).
14 *Epitaxial Silicon Technology*; *Vol.*, edited by B. J. Baliga (Academic Press. Inc., Orlando, FL, 1986).
15 P. Vanderputte, L. J. Giling, and J. Bloem, J. Cryst. Growth **31,** 299-307 (1975).
16 A. S. Peter, D. N. Christopher, N. J. Thomas, S. M. Theresa, R. M. Benjamin, M. Jeremiah, and E. M. Thomas, Applied Physics Letters **77,** 1399-1401 (2000).

[17] K. K. Lew, L. Pan, T. E. Bogart, S. M. Dilts, E. C. Dickey, J. M. Redwing, Y. F. Wang, M. Cabassi, T. S. Mayer, and S. W. Novak, Appl. Phys. Lett. **85,** 3101-3103 (2004).
[18] T. Clement, S. Ingole, S. Ketharanathan, J. Drucker, and S. T. Picraux, **89** (2006).
[19] M. Ohring, *The Materials Science of Thin Films*, Second ed. (Academic Press, San Diego, 2002).
[20] J. Bloem, Y. S. Oei, H. H. C. Demoor, J. H. L. Hanssen, and L. J. Giling, J. Cryst. Growth **65,** 399-405 (1983).
[21] J. Bloem, Y. S. Oei, H. H. C. Demoor, J. H. L. Hanssen, and L. J. Giling, J. Electrochem. Soc. **132,** 1973-1980 (1985).
[22] E. G. Bylander, J. Electrochem. Soc. **109,** 1171-1175 (1962).
[23] V. Schmidt, S. Senz, and U. Gosele, Phys. Rev. B **75** (2007).
[24] S. Kodambaka, J. B. Hannon, R. M. Tromp, and F. M. Ross, Nano Lett. **6,** 1292-1296 (2006).
[25] J. B. Hannon, S. Kodambaka, F. M. Ross, and R. M. Tromp, Nature **440,** 69-71 (2006).
[26] T. Kawashima, T. Mizutani, H. Masuda, T. Saitoh, and M. Fujii, J. Phys. Chem. C **112,** 17121-17126 (2008).
[27] L. L. Kazmerski, Journal of Electron Spectroscopy and Related Phenomena **150,** 105-135 (2006).
[28] R. Diaz, Thesis, The Pennsylvania State University, 2007.
[29] D. K. Schroder, *Semiconductor Material and Device Characterization*, 3rd ed. (John Wiley & Sons, New York, 1998).

Chapter 5

Growth and Electrical Properties of Template Grown Silicon Nanowire Arrays

5.1 Introduction

The use of a vertical array of silicon nanowires (SiNWs) on low cost substrates such as glass would allow for solar cells to become a cost-effective alternative without sacrificing efficiency. Tsakalakos *et al.* proposed that low cost substrates such as foil or glass combined with radial p-n junction silicon nanowires synthesized by CVD could yield solar cells with improved cost benefit as compared to bulk solar cells at a comparable efficiency.[1] They have also shown that silicon nanowire arrays have an increased optical absorption across the spectrum as compared to solid thin films of the same thickness.[2] Further details can be found in section **1.2.1**.

Anodic aluminum oxide (AAO) membranes are of interest as a way to control the growth of silicon nanowires on low cost substrates such as glass. The AAO membranes provide a way to control nanowire diameter and to electrically isolate the radial coating from the p-type (or backside) contact. One limitation of glass substrates; however, is temperature. Soda lime glass softens at 700°C. Silicon tetrachloride cannot be used due to the high temperature required for nanowire growth. However, the use of a template on glass to direct the growth of silicon nanowires using SiH_4 would allow for low temperature and directed nanowire growth. Recently, fabrication of highly ordered AAO templates on silicon and glass substrates was demonstrated and was reviewed in section **2.5.1**.

The focus of this study, is to develop SiNW arrays in AAO templates on glass for the fabrication of radial junction nanowire solar cells. This project was done in collaboration with Dr.

Joe Habib and co-workers at Illuminex Corporation, who provided the AAO-coated glass substrates. This will encompass the electrical characterization of undoped and doped silicon nanowires in free-standing AAO membranes. The electrical results were compared to single nanowire electrical measurements. The growth of silicon nanowires was then carried out on AAO coated glass, (shown in Figure **5-1**) and AAO coated wire substrates (shown in Figure **5-2**).

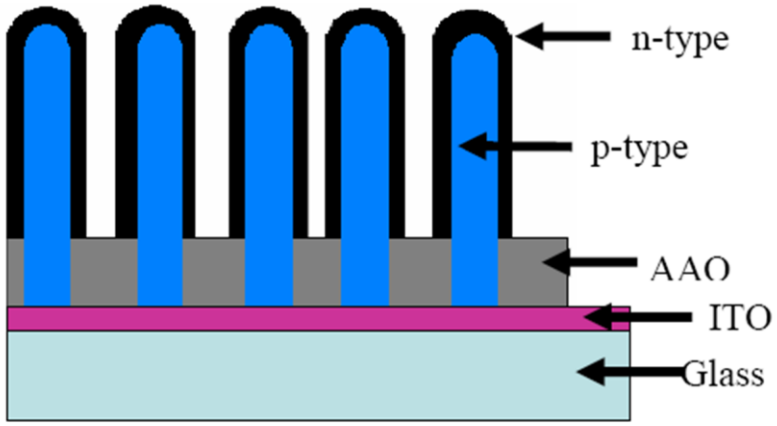


Figure **5-1**: Schematic of a silicon nanowire array on AAO coated glass substrate.

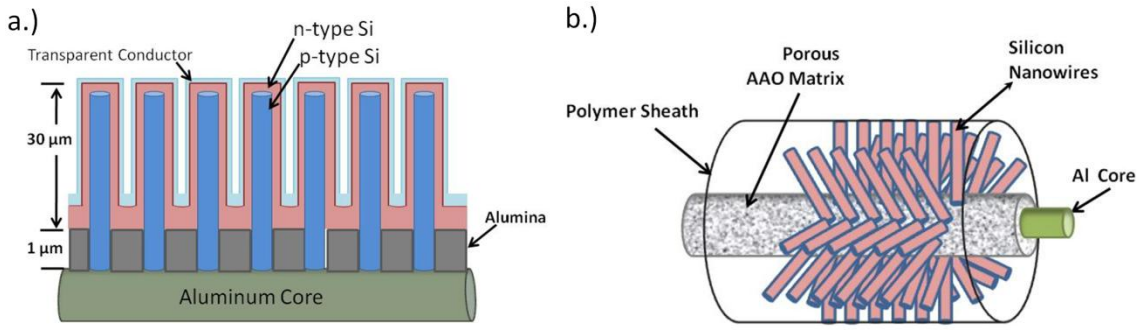


Figure **5-2**: a.) Device architecture detail, showing the Al core, p-type SiNWs growing through the insulating AAO and then coated with a continuous n-type Si layer which is then covered with an outer transparent conductive coating. b.) Complete schematic of a PV wire device showing silicon nanowires distributed about the aluminum core with a protective polymer coating.

5.2 Experimental Details

5.2.1 Free Standing AAO Membranes

SiNW arrays were first fabricated in free standing membranes using commercially available nanoporous AAO membranes (approximately 60 µm thick with a nominal pore diameter of 200 nm) purchased from Whatman Scientific. A description of membrane preparation and electrodeposition details can be found in section **3.2.1**. The cobalt length was varied from 30 to 50 µm to control the SiNW length inside of the membranes. Finally, a 250 nm gold plug was electrodeposited on top of the cobalt using a potassium gold cyanide solution. A schematic of this structure was shown in Figure **3-1**. In this structure, the gold serves as the catalyst for VLS growth of Si nanowires, and the cobalt serves both as a base for nanowire growth and a backside metal contact to the wires for the electrical measurements.

Silicon nanowire growth was carried out in a low pressure, hot wall chemical vapor deposition reactor at 500°C and 13 Torr as described in section **3.3.2**. A 10% mixture of SiH_4 in H_2 was used as the silicon precursor with intentional p-type and n-type doping carried out by adding trimethylboron (2% in H_2) or phosphine (100 ppm in H_2), respectively, to the inlet gas mixture. The total flow rate of gases through the reactor was held constant at 100 sccm. The total flow through the reactor was held constant at 100 sccm. The silane flowrate was held constant during growth at 50 sccm. For n-type doped SiNWs, a 500 ppm phosphine (PH_3) in H_2 was used as the precursor with 10% SiH_4 in H_2 at a 50 sccm flowrate as the silicon precursor.

5.2.2 AAO Membranes on Glass

The AAO coated glass substrates were fabricated by Illuminex Corporation using a process shown schematically in Figure **5-3**. A thin 100-150 nm ITO layer was deposited onto the glass substrate followed by an aluminum film approximately 1 μm thick deposited by e-beam evaporation. The aluminum films were then anodized using oxalic acid to form the AAO template. The diameter and center-to-center spacing of the pores were controlled by electrolyte concentration and type and these parameters are a linear function of the anodization voltage[3]. To ensure a clear opening through the AAO pores, anodization is carried out at a constant voltage 20-200 V to form a base array of ~30-60 nm diameter nanopores. This is carried out until the pores reach the desired depth. As the AAO template formed, a barrier layer typically remained at the AAO/ITO interface.

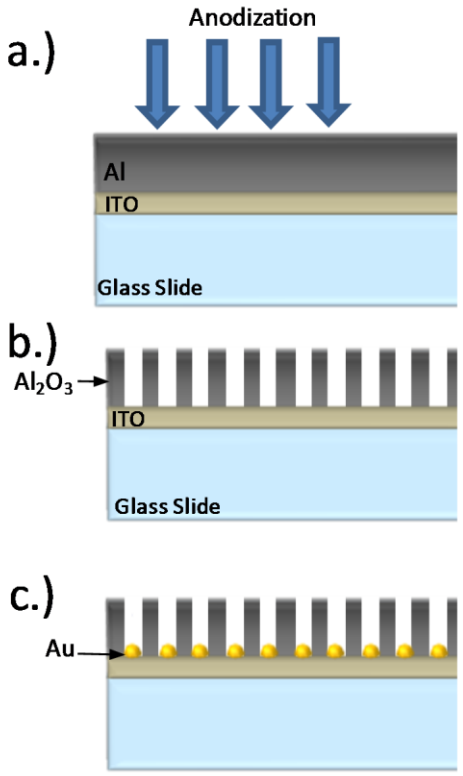


Figure **5-3**: Schematic of substrate fabrication process a.) anodic oxidation of Al thin film on an ITO layer on glass b.) AAO membrane is formed on the ITO layer through anodization, and c.) Au is electrodeposited into the pores.

Special care must be taken to remove this layer so that as the SiNWs are grown they will be in direct contact with the ITO layer. The anodization voltage is lowered in sequential steps of 1-10 volts at 1-5 minute intervals so that successively smaller nanofinger protuberances extend from the bottom of the pores into the Al_2O_3 barrier layer. Etching the Al_2O_3 in a 10 wt % phosphoric acid solution both widen the pores and opens them at the bottom to fully expose the ITO layer. The average pore size in these samples was around 98 +/-23 nm in diameter. Then approximately 25 nm of Au, which serves as the catalyst for VLS growth, was electrolessly deposited into the pores. Figure **5-4** shows a cross-sectional FESEM image of the all of the layers prior to nanowire growth.

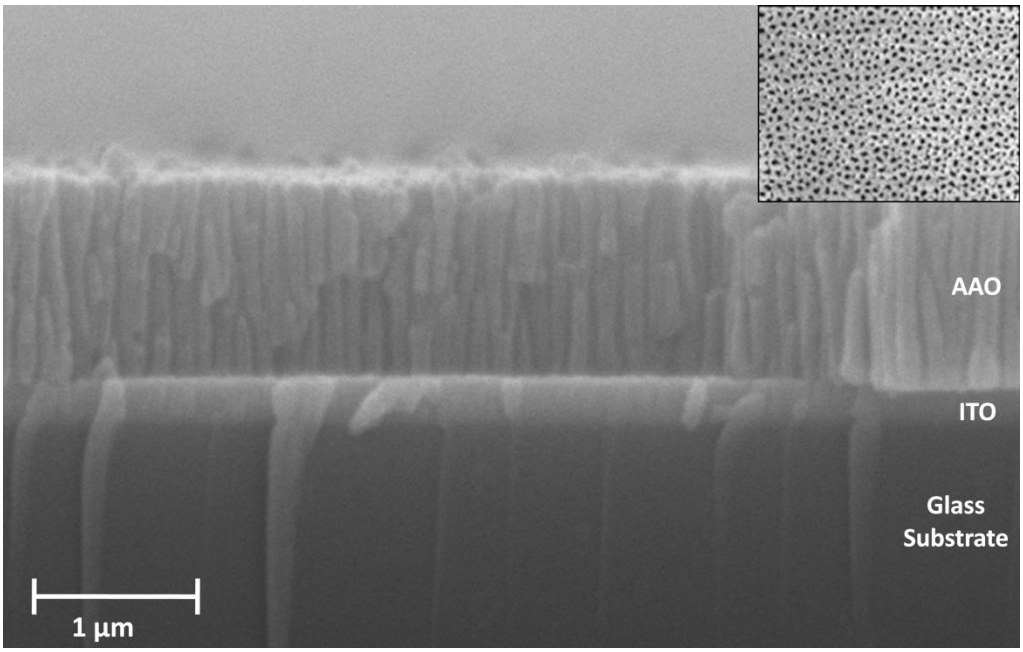


Figure **5-4**: AAO Membrane on glass slide side view of the structure showing the glass slide with the AAO membrane on top. Inset picture shows top-down view of AAO membrane.

5.2.3 AAO Aluminum Thread

Annodized aluminum oxide templates were also fabricated on aluminum wire by the Illuminex Corporation. The high purity aluminum thread was 200-250 μm in diameter. A cylindrical annodization cell was used by Illuminex to ensure that a uniform AAO layer was formed around the wire. As in the case with the AAO on glass, it is important that the barrier layer is removed when forming the pores. A phosphoric acid etch at the end clears any remnant Al_2O_3, thus providing a path for the seed, and subsequently the nanowires, to make direct contact to the Al core. The seeds were electrochemicaly deposited into the anodized pores using pulse plating. Commercial gold sulfite plating solution was utilized. After seed deposition, the Al_2O_3 was etched from representative samples to determine the gold seed size and distribution throughout the substrate by SEM imaging.

Prior to growth on any of the wire substrates, a way to place them into the reactor and allow for the precursor gases to pass over the entire 360 degrees of the sample was designed. A quartz boat was modified in order to achieve this. A quartz boat was created with a hook at one end for pushing and pulling samples in/out of the reactor. The boat had 7 slots cut into the boat sides. A schematic of the finished boat (Figure **5-5**) below shows a side view of the slots and a top view where the samples sit. This allowed for a large number of samples to be grown at the same time and allowed for nanowire array growth the entire way around the wire.

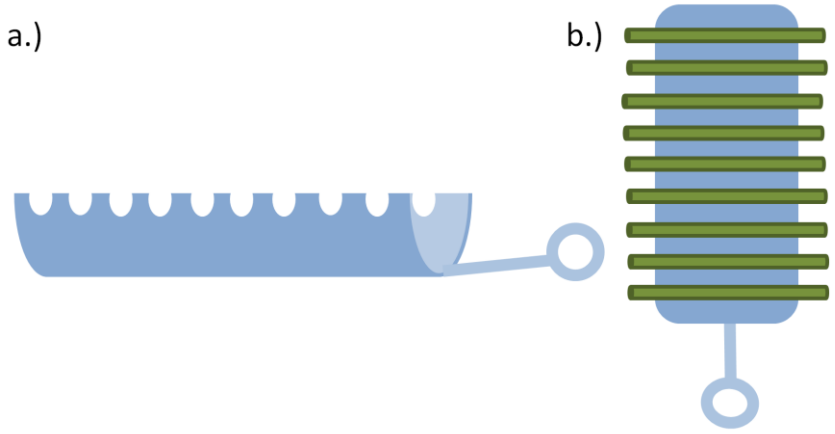


Figure **5-5**: Schematic of the boat design both a.) side view and b.) top down view. This is required to obtain even nanowire growth in a complete 360 degrees around the aluminum wire substrates.

5.3 Results

5.3.1 Electrical Characterization of SiNWs grown in Free-Standing AAO Membranes

For radial junction solar cells grown using a low cost templated substrate such as the AAO coated glass, it is important to controllably dope both the n-type and p-type Si. The goal of

this section is to electrically characterize intentionally doped silicon nanowire arrays grown in AAO in order to determine nanowire resistivity as a function of dopant/SiH_4 ratio.

5.3.1.1 Sample Fabrication

The silver was deposited at 0.575 A, and served as a filler to control the placement of the cobalt and gold in the membrane. The length of the Ag segment dictated the length of the Si nanowires inside of the membrane before they reached the membrane surface. The plating current for the cobalt solution was 0.7 A. Details on the electrodeposition can be found in Section **3.2.1**. Finally, the gold was deposited at 0.175 A. SEM characterization was then done on the membrane to make sure that the surface pores were not chemically damaged.

The flow rate of the SiH_4 gas mixture was 50 sccm resulting in a silicon nanowire growth rate on the order of 1 μm/min. For growth in the AAO membranes, SiH_4 diffuses into the pores and preferentially decomposes on the gold catalyst resulting in VLS growth of SiNWs within the pores. Cobalt reacts with silicon at the growth temperature, forming a thin cobalt silicide layer at the interface between the cobalt and SiNWs as previously report.[4] The SiNWs grow upward within the membrane pores eventually emerging from the membrane surface. A scanning electron microscope image (SEM) of a sample cross-section after SiNW growth is shown in Figure **5-6**.

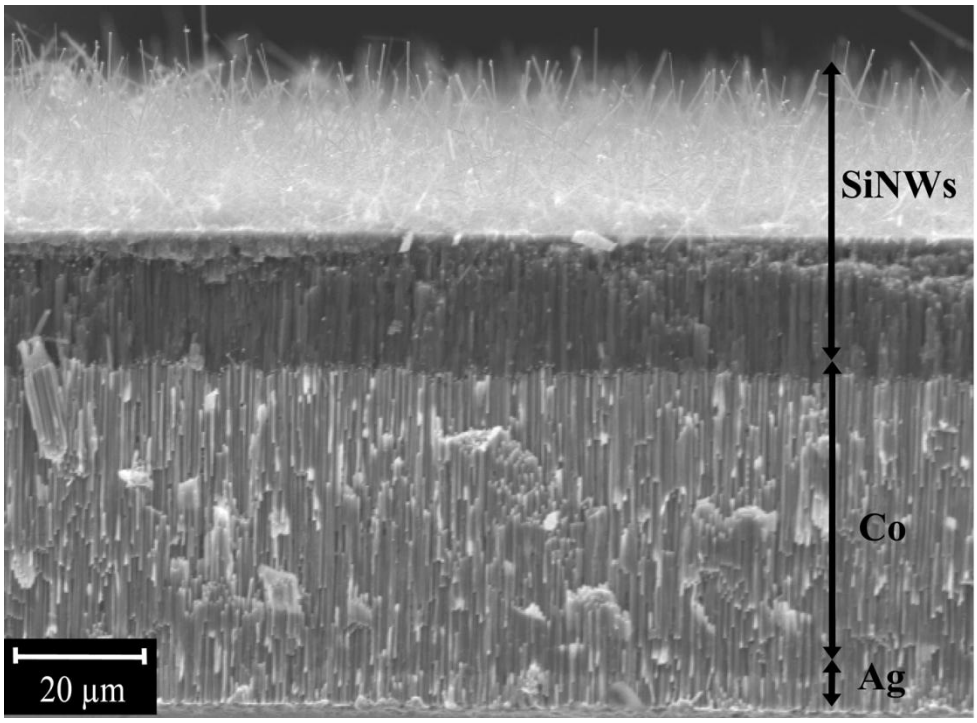


Figure **5-6**: Cross-sectional SEM image of sample after electrodeposition and nanowire growth.

For the lightly doped p-type wires, a highly doped SiNW segment ($TMB/SiH_4=2\times10^{-2}$), approximately 1 µm in length, was initially grown on top of the cobalt segment in an effort to reduce the contact resistance, and then the dopant/SiH_4 ratio was reduced to the appropriate TMB/SiH_4 ratios (2×10^{-3}, 2×10^{-4}) and held constant throughout the remainder of the growth. For n-type wires, a similar short highly doped SiNW segment ($PH_3/SiH_4=2\times10^{-3}$) was also initially grown, followed by a reduction to the appropriate PH_3/SiH_4 ratios (2×10^{-5}, 2×10^{-4}) for the rest of the wire growth. For each dopant/SiH_4 ratio studied, a series of samples were prepared in which the SiNW length inside the membrane was varied from approximately 5 to 25µm.

Large area circular metal contacts were sputter deposited on the top surface of the membranes to serve as electrical contacts for two-point resistance measurements. A schematic of the array measurement configuration is shown in Figure **5-7**.

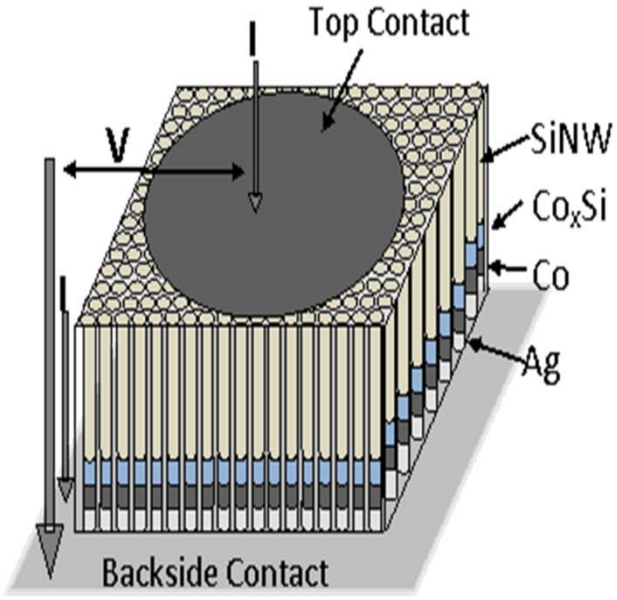


Figure **5-7**: Schematic of SiNW array sample and two point electrical measurement configuration.

In order to prepare a surface with a uniform top contact area suitable for metal deposition, the SiNWs protruding from the membrane after growth were polished away with diamond paper until a relatively flat surface of exposed SiNWs was obtained. Circular contacts with diameters ranging from 75 to 300 μm were deposited on the top surface of the membranes by sputter deposition or electron beam evaporation through a shadow mask. The contacts consisted of 400 nm thick Al for the p-type arrays and 50 nm Ti/50 nm Pt/100 nm Au for the n-type arrays. Both large (200-300 μm) and small (75 μm) diameter circular contacts were used depending on the sample doping as described in more detail in the next section. An array of contacts on the top surface is shown in Figure **5-8** and the inset shows a higher magnification view of the polished surface showing a high number of nanowires filling the pores, which is important for estimating the number of nanowires per contact. The bright spots visible in the inset are most likely Au left over on the membrane surface. After deposition, the top contacts were annealed for 30 minutes in N_2 at temperatures of 250°C for n-type and at 300°C for the p-type samples. Electrical measurements

were then carried out using a two point measurement configuration as shown in Figure **5-7** to obtain I-V curves of the SiNW arrays before and after annealing.

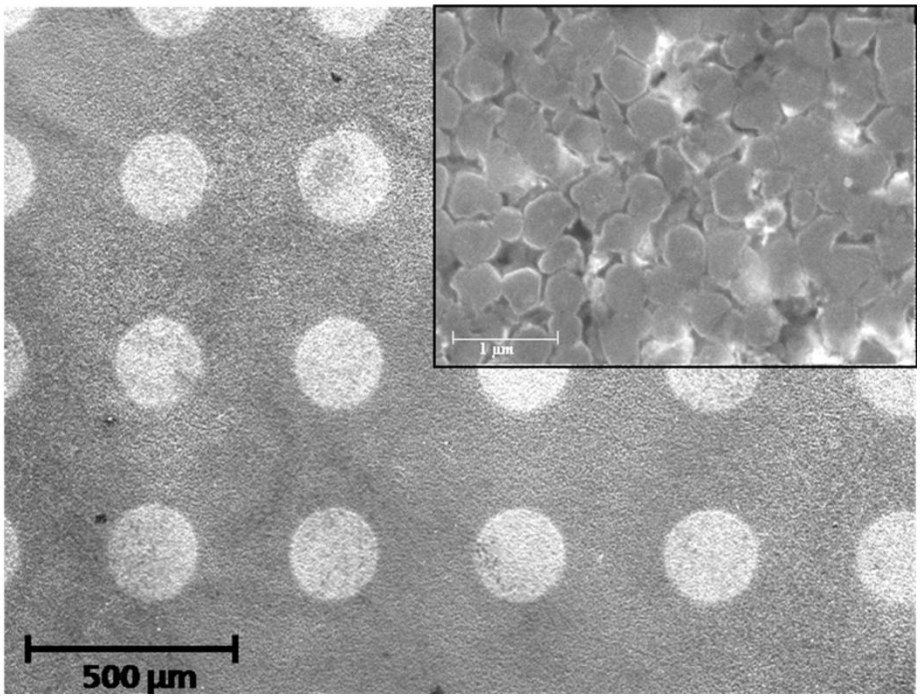


Figure **5-8**: SEM micrograph showing polished membrane surface with an array of top contacts. Inset shows polished membrane surface before contact deposition.

5.3.1.2 Electrical Properties

The resistivity of the SiNW arrays was extracted from measurements of the total array resistance. Current-voltage (I-V) curves obtained from as-deposited SiNW array samples were non-linear with the exception of the most highly doped p-type ($TMB/SiH_4 = 2\times10^{-2}$) and n-type ($PH_3/SiH_4 = 2\times10^{-4}$) samples, where linear behavior was observed. The I-V curves for the intentionally doped samples became linear after annealing in N_2 at temperatures of 250^{o}C for n-type and 300°C for both undoped and p-type samples; however, the undoped sample still

exhibited non-linear behavior. The I-V curves for this sample exhibit an asymmetry that indicates that the current is limited by the $CoSi_x$ contacts. Figure **5-9** shows I-V curves, a.) before annealing and b.) after annealing, for a p-type ($TMB/SiH_4=2\times10^{-3}$) SiNW array.

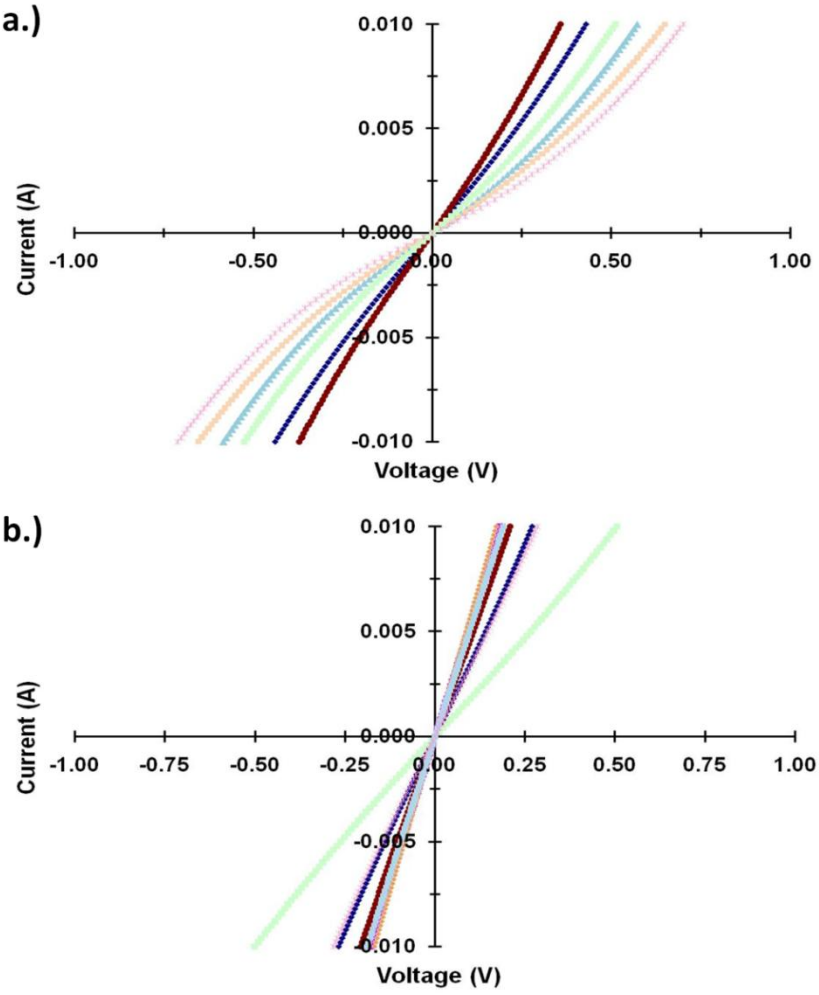


Figure **5-9**: I-V curves for a p-type ($TMB/SiH_4=2\times10^{-3}$) SiNW array both a.) before annealing and b.) after annealing. Each color line was a different metal dot on the sample. The resistance from each metal dot was then averaged to determine the average resistance.

The effect of annealing on the total resistance is shown in Figure **5-10** below. It can be seen that the total resistance decreases after the samples are annealed.

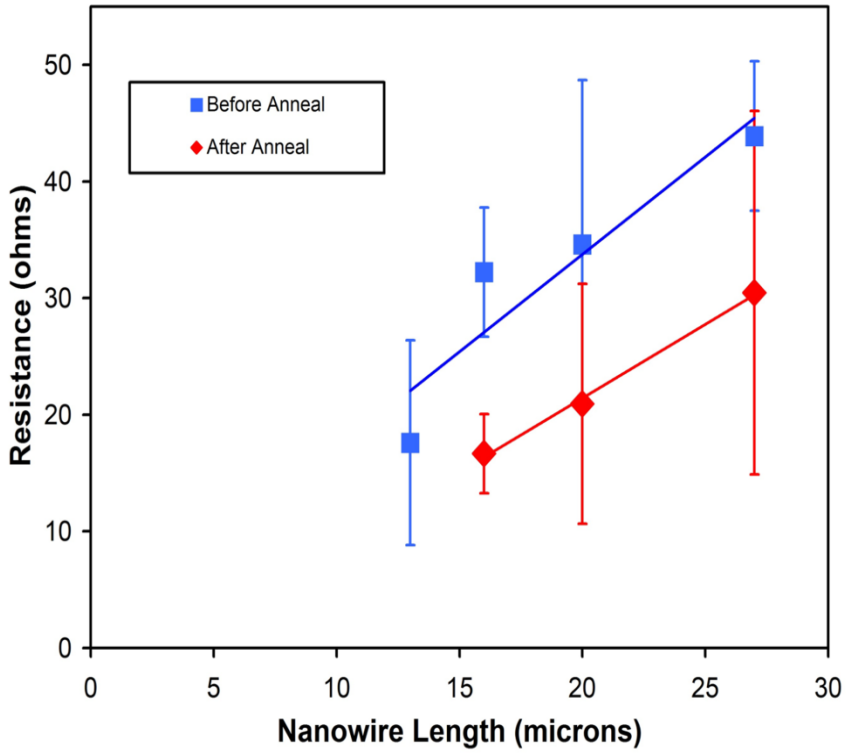


Figure **5-10**: Total resistance versus nanowire length for the SiNW arrays sample grown with $TMB/SiH_4=4\times10^{-3}$ before and after annealing.

Representative I-V curves obtained on the p-type ($TMB/SiH_4=2\times10^{-2}$), n-type ($PH_3/SiH_4=2\times10^{-5}$), and undoped samples are shown in Figure **5-11**. For each sample, I-V curves were measured on 10-15 top circular contacts to determine an average resistance and standard deviation. In the case of the undoped SiNW array sample, the resistance was obtained at a fixed current of 0.01A in order to maintain a fixed voltage drop across the contacts in all samples. An average resistance of 10.6 +/-2.5 Ω, 2.1 +/-0.3 Ω, and 20.8 +/-10.6 Ω was measured for the n-type (2×10^{-5}), p-type (2×10^{-2}), and undoped samples, respectively. The average resistance and standard deviation were measured for several different nanowire lengths for a particular doping level. It should be noted that the ~1 μm long highly doped p^+ and n^+ segment near the

silicon/cobalt interface was assumed to have a lower resistance compared to the rest of the nanowire and was therefore subtracted from the total nanowire length for each of the lower doped and undoped samples.

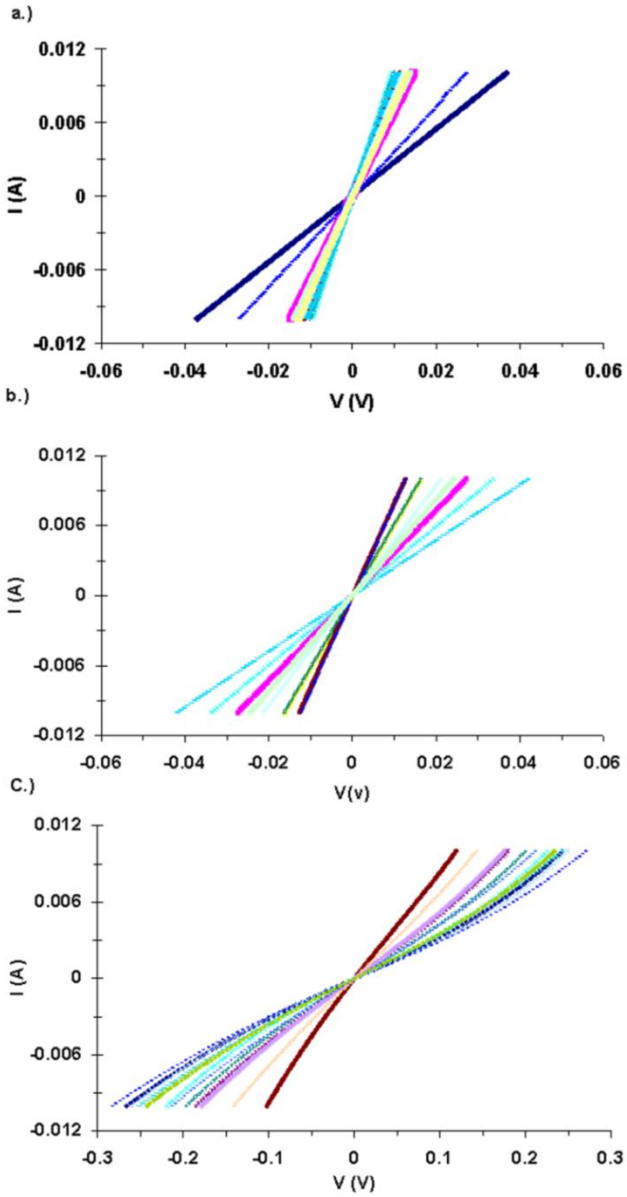


Figure **5-11**: Representative I-V curves of SiNW array samples after annealing. Each I-V curve represents data obtained from different circular top contacts measured on the same sample. **(a)** 18μm long SiNWs, TMB/SiH_4=2×10^{-2} **(b)** 13 μm long SiNWs, PH_3/SiH4 = 2×10^{-5} and **(c)** 16 μm long SiNWs, undoped sample. Each different color I-V curve represents one metal dot measured.

Assuming that the contact probe and metal resistances are negligible, then the total resistance measured for each circular top contact is given by $R_T = R_{C1} + R_{C2} + R_s$ where R_{c1} and R_{c2} are the metal/semiconductor contact resistances of the top and bottom contacts, respectively, and R_s is the semiconductor nanowire resistance. For the SiNW arrays, the semiconductor resistance can be approximated as $R_s = \rho L/NA$ where ρ is the SiNW resistivity, L is the nanowire length, A is the cross-sectional area of a single SiNW and N is the total number of nanowires in the area covered by a top circular contact. Therefore, by plotting $R_T NA$ versus L (Figure **5-12**), the nanowire resistivity is obtained from the slope of the line and the y-intercept ($(R_{c1}+R_{c2})NA$) provides information on the specific contact resistances.

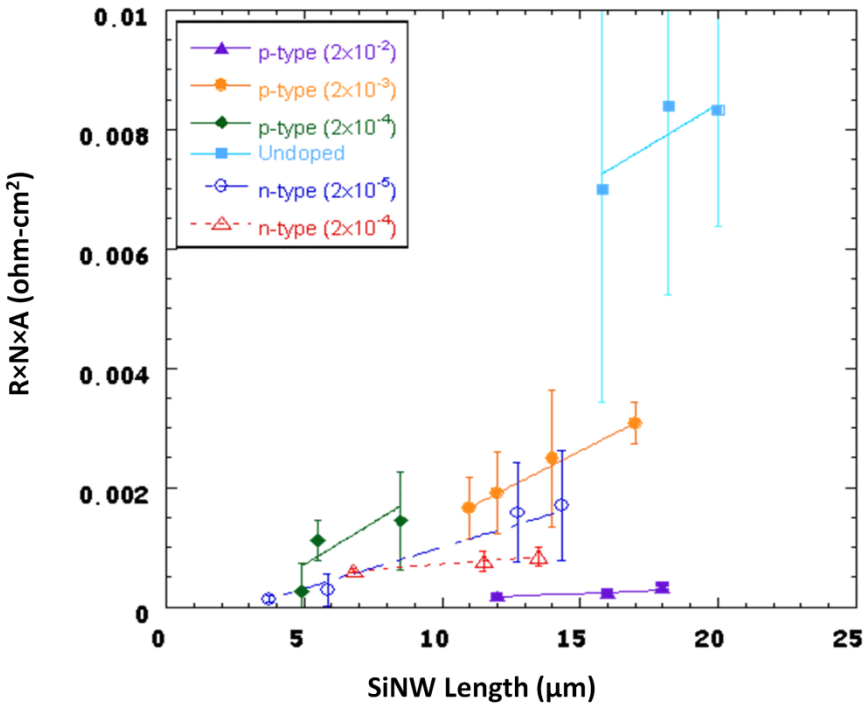


Figure **5-12**: The total resistance - nanowire contact area product ($R_T NA$) versus silicon nanowire length for intentionally doped and nominally undoped SiNW arrays grown with varying dopant/SiH_4 ratios.

For the nanowire arrays measured in this study, the cross-sectional area, *A*, was calculated assuming an average nanowire diameter of 300 nm, which was obtained from SEM images of the nanowires. Similar to prior publications,[5,6] surface depletion, which would reduce the effective cross-sectional area of the wires, was not taken into account in the calculations. The number of nanowires per unit area on the membrane surface was estimated at 6.75×10^8 cm^{-2} from SEM images. The nanowire density was multiplied by the area of the top contact to calculate the total number of nanowires in the array (*N*). Different top metal contact diameters ranging from 75 μm to 300 μm were used depending on the nanowire array resistivity. For samples with higher resistivity, larger diameter contacts (200-300 μm) were used for the measurement for ease of fabrication and testing. However, for the highly-doped n-type sample with low resistivity, the variation of R_T with *L* was too small to accurately determine the resistivity using the larger contact area. In this case, the top contact diameter was reduced to 75 μm, providing a factor of 16 increase in the slope of R_T versus L, thereby enabling measurements of arrays with lower resistivity. The estimated number of nanowires per array measurement *(N*) varied from 4.8×10^5 to 3×10^4 for the 300 μm and 75 μm diameter contacts, respectively.

The resistivity of the nominally undoped Si nanowires arrays was 2.7 +/- 1.9 Ω-cm. The large standard deviation may arise from the non-linearity of the I-V characteristics, which remained non-linear even after the undoped samples were annealed. The addition of dopant precursors during growth resulted in a decrease in the average nanowire resistivity to 0.18 +/- 0.06 Ω-cm for highly doped ($TMB/SiH_4 = 2\times10^{-2}$) p-type wires and 0.4 +/- 1 Ω-cm for the highly doped ($PH_3/SiH_4 = 2\times10^{-4}$) n-type wires. For some of the samples fabricated with 300 μm diameter top contacts, the y-intercept of the $R_T NA$ versus *L* plot was slightly negative. This negative intercept, which would indicate a negative contact resistance, arises from a combination of the generally low contact resistance of the samples combined with inaccuracies in the nanowire

length measurements. The nanowire length was obtained from cross-sectional SEM images similar to that shown in Figure **4-2** obtained from select areas of each sample. Variations in nanowire length across the sample may occur due to non-uniformities in metal electrodeposition in the membrane pores as well as variations in the amount of material removed from the surface during the polishing step for the top contact deposition. Furthermore, reaction between the Al top contact metal and the SiNWs during the annealing step could be particularly pronounced in this geometry, resulting in a further reduction of the effective length of the SiNWs. A systematic error in the measurement of the true length of the semiconductor nanowire segments would result in a shift in the plotted lines left or right and a corresponding error in the y-intercept, although the slope of the line, which provides the nanowire resistivity, would be unaffected. When the diameter of the top contact was reduced to 75 μm (Figure **5-12**, $PH_3/SiH_4=2\times10^{-4}$), a positive y-intercept of $3.6\times10^{-4}\Omega\text{-cm}^2$ was obtained corresponding to a total contact resistance of 17 $\Omega\text{-cm}^2$.

As shown in Figure **5-13**, the SiNW resistivities obtained from the array measurements decrease with increasing dopant/SiH_4 ratio for both p-type and n-type samples. Also plotted in Figure **5-13** are resistivity values previously reported in the literature[5,6] that were obtained from four-point resistance measurements of individual SiNWs grown out the top of AAO membranes under identical growth and doping conditions. For the single wire measurements a total of 10 wires were measured and the error bars represent the standard deviation of these measurements. Within the margin of the experimental error, the array resistivity data compares favorably with that obtained from single wire four-point measurements, demonstrating the general validity of our array measurement approach.

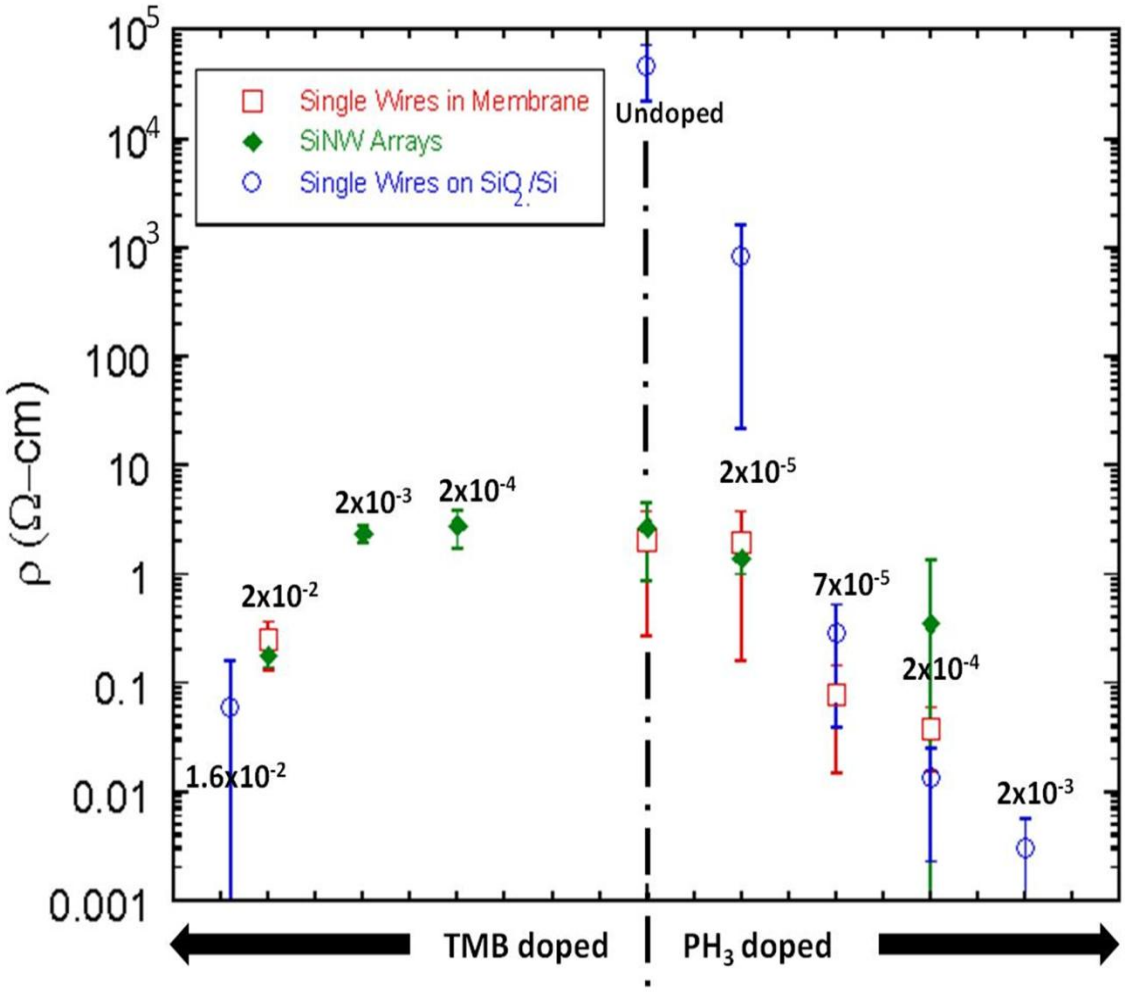


Figure **5-13**: Plot of resistivity versus dopant/SiH_4 ratio comparing the results obtained from the nanowire array measurements to those obtained from four-point resistance measurements of individual SiNWs grown out of an alumina membrane[15,16] and on oxidized Si substrates.

The undoped SiNWs grown in the anodized alumina membranes have an anomalously low resistivity as observed in our earlier work.[6] The average resistivity of the undoped SiNWs (1-3 Ω-cm) is orders of magnitude lower than that of intrinsic silicon (~2×10^5 Ω-cm)[7], indicating that the nanowires are unintentionally doped. Gated current-voltage measurements carried out on individual undoped Si nanowires grown in the AAO membranes indicate that the wires are p-type.[6] In an effort to identify the source of the unintentional acceptors, undoped SiNWs were also grown on gold-coated oxidized Si substrates in the same reactor using identical growth conditions

and four-point measurements were used to determine the average nanowire resistivity In this case, the undoped Si nanowires were also found to be p-type; however, the average resistivity was much higher, on the order of 10^4-10^5 Ω-cm, indicating a significantly reduced concentration of unintentional acceptors. This result is further supported by the resistivity data obtained on the lowest PH_3-doped SiNW sample ($PH_3/SiH_4=2\times10^{-5}$). Gated I-V measurements of the single wire samples grown in anodized alumina membranes revealed that the wires were p-type rather than n-type at this low PH_3 doping level indicating that the phosphorus donors were compensated by unintentional acceptor impurities. As shown in Figure **5-13**, the average resistivity of the lightly PH_3-doped ($PH_3/SiH_4=2\times10^{-5}$) SiNWs grown on oxidized Si substrates (ρ=820 Ω-cm) is several orders of magnitude higher than that of wires grown using the anodized alumina membranes (ρ=1.4 Ω-cm), and the wires exhibit n-type behavior. These results clearly demonstrate that the anodized alumina membrane is the primary source of unintentional acceptors in the SiNWs. As a result of the small volume and high surface area of the nanowires, it was not possible to directly measure impurities in the wires using standard chemical analysis methods such as secondary ion mass spectrometry or glow discharge mass spectroscopy. Residual aluminum remaining in the membranes from the anodization process is a possible source of the unintentional acceptors; however, other impurities arising from the membrane or the electrodeposition process cannot yet be ruled out.

5.3.2 Nanowire Growth on Templated Glass

Now that the resistivity of intentionally doped SiNWs inside an AAO membrane have been determined, this growth process can be used for the growth of SiNWs on AAO coated glass substrates for solar cell applications. As described earlier in the experimental section **5.2.2**, the AAO membranes were created on ITO coated glass shown in Figure **5-1**. The glass serves as a

low cost substrate that provides mechanical support for the AAO template. The ITO serves as the bottom contact to the p-type SiNWs so it was essential for the barrier layer to be removed between the AAO and ITO during annodization. The AAO not only serves as a template for nanowire growth but also serves as an electrically insulating barrier between the ITO and n-type coating once a device has been made.

Growth was carried out at a pressure of 13 Torr and a temperature of 500°C using 10 % SiH_4 as the Si precursor gas. A 2% TMB in H_2 was the p-type gas precursor. Further details on the nanowire growth can be found in section **3.3.2.1**. Since the ITO layer will serve as a backside contact to the SiNWs, a 1 micron p+ ($TMB/SiH_4=2\times10^{-2}$) section was first grown to minimize the contact resistance. The remainder of the wire was grown to a pre-determined doping level. This doping level was varied from $TMB/SiH_4=2\times10^{-3}$ through 2×10^{-2} for different samples for photovoltaic measurements. The SiNWs were approximately 15 microns long and the diameters ranged between 60-100 nm in diameter. Figure **5-14** shows a top down image of the high density p-type SiNWs, and a cross-sectional FESEM image showing the nanowires growing out of the AAO template with the ITO and glass layers. As can be seen from the top down view, there is a high density of SiNWs, however, from the cross-section it appears there are some pores that do not have a nanowire growing from them.

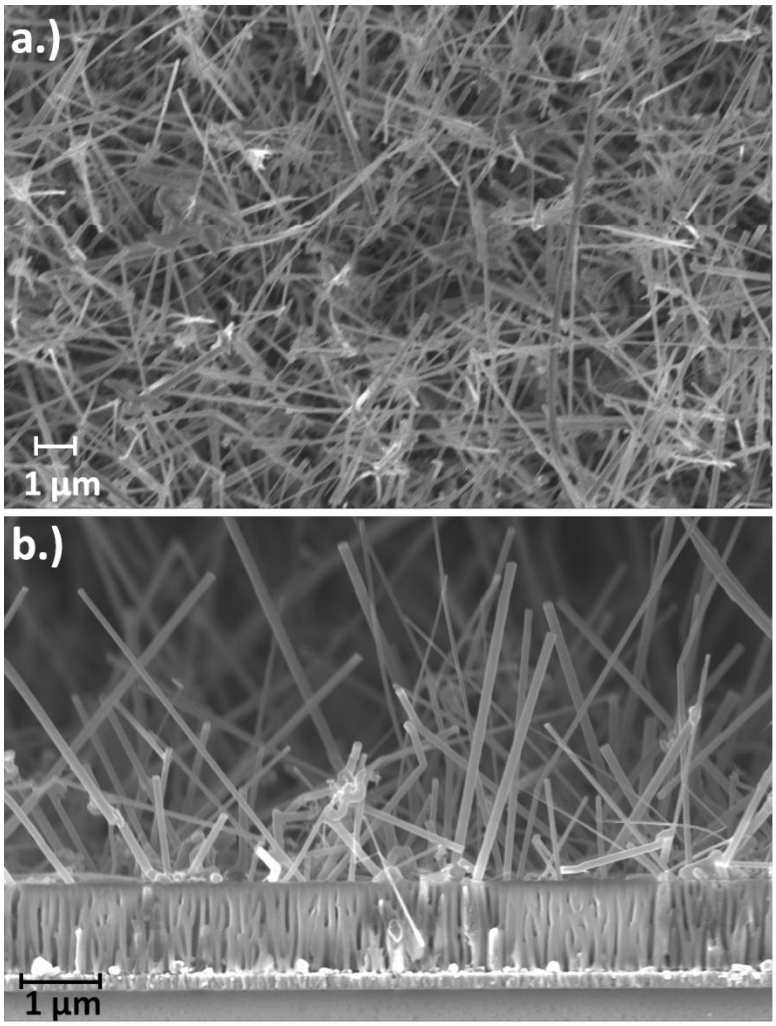


Figure **5-14**: a.) Top-down FESEM image of SiNWs growing out of the AAO template. b.) Side view of the p-type SiNW growth on AAO membrane on glass. In both images the Au tips were removed using GE 1848 Au etchant.

The samples exhibited a uniform coverage of Si nanowires over the entire sample surface (~3/4" wide x 1" long). To the naked eye, the nanowires appear as a dark brown textured surface on the AAO-coated glass slides, shown in Figure **5-15**.

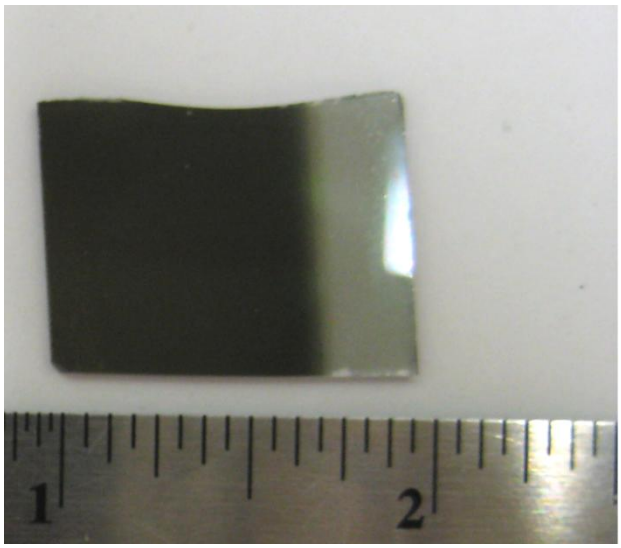


Figure **5-15**: Image of typical Illuminex substrate after p-type SiNW growth. The dark brown area is where the SiNWs have been grown.

5.3.4 Nanowire Array Growth on Templated Wires

Another low cost solar cell device architecture is a photovoltaic thread. Substrates of AAO templated wire were provided by the Illuminex Corporation and are shown in Figure **5-16**. The average pore diameter for the wire substrates was 86 +/- 16 nm. Since the sample geometry is more complex than previous nanowire growth runs on templated glass, a series of sample test runs were performed to ensure the samples would be able to withstand growth temperatures between 400-500°C.

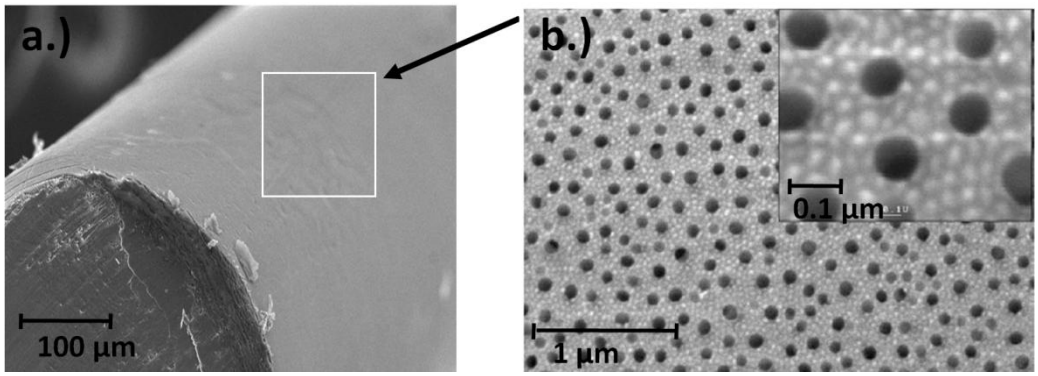


Figure **5-16**: SEM images of a.) a templated aluminum wire substrate and b.) higher magnification showing the AAO pores. Image courtesy of Illuminex Corporation.

Samples were placed into the reactor and heated up to the growth temperature of 500°C and were held at that temperature for 20 minutes before cooling. This was done to test the thermal stress on the substrate and ensure that the AAO template would not "peel" off of the Al wire base. No noticeable cracking or peeling of the AAO template was visible.

Undoped silicon nanowire growths were carried out using standard conditions that were successful for growth on the templated glass substrates. Samples were heated to 500°C at a system pressure of 13 Torr. A 10% SiH_4 in H_2 mixture was used as the silicon precursor at a flow rate of 50 sccm. SEM images of the sample surface shown in Figure **5-17** revealed that very few nanowires were present on the sample surface. It was hypothesized that not enough SiH_4 was getting to the Au seed inside the AAO pores. The Au particles are buried in the pores on a curved wire surface. In order for growth to occur the SiH_4 needs to diffuse far enough into the pores to preferentially react with the metal catalyst. A model of the SiH_4 diffusion and reaction in a nanopore was developed by Lew *et al.*[8] The model assumed steady state and a first-order reaction. The model determined that the temperatures ≤ 500°C and low pressures (< 10 Torr) were required to prevent the SiH_4 from depositing on the pore walls. Due to the curved nature of the samples the diffusion of the SiH_4 into the pores to react with the metal catalyst instead of the

pore walls may require different growth conditions than the growth conditions developed for growth on glass substrates.

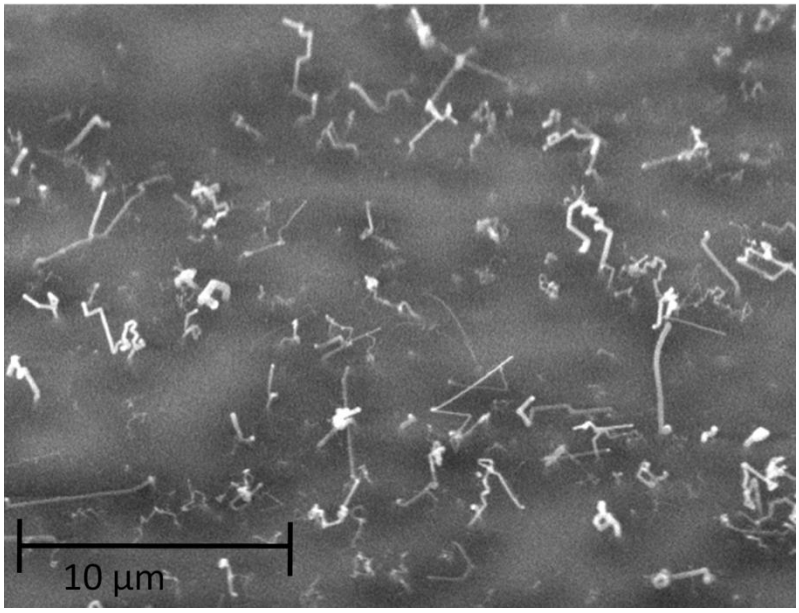


Figure **5-17**: SEM image of the templated wire surface after nanowire growth at 500 °C, P_{SiH4} = 0.65 Torr and a system pressure of 13 Torr.

As the surface curvature is increased and the pore size is slightly smaller compared to the planar templates, a series of experiments were carried out with lower pressures and SiH_4 flow rates in order to try and get more of the Si precursor into the pores. Table **5-1** lists the various samples and conditions that were varied including SiH_4 flow rate, pressure, and temperature. As can be seen in Figure **5-18** below, the conditions that yielded a high density of SiNWs that were straight was growth at a temperature of 500°C and a pressure of 3 Torr with a SiH_4 partial pressure of 0.65 Torr. The lower pressure was necessary to get enough of the precursor gas into the pores for nanowire growth. A lower pressure will increase the diffusivity of SiH_4 into the pores.[8] The growth at these conditions, however, was slower than the growth rates obtained at 13 Torr. This was compensated by increasing the growth time. Samples were doped n-type using a

500ppm PH_3 in H_2 source at $PH_3/SiH_4 = 2\times10^{-3}$. The samples were then returned to the Illuminex Corporation for conductive polymer sheath coating and studies for use as photovoltaic thread, and are currently under investigation.

Table **5-1**: The template wire sample and growth conditions for AAO templated Al wires.

	Temp (°C)	P_{total}	SiH_4 (sccm)	P_{SiH4}	Growth Time (min)	Wires (Y/N)
W36	425	13	100	0.65	90	Some
W37	500	13	100	0.65	20	N
W42	500	13	100	0.65	20	N
W50	425	13	100	1.3	120	N
W53a	425	13	100	1.3	120	Some on Surface
W57	425	13	100	1.3	120	Some on Surface
W58	425	13	100	1.3	120	Some
W56	400	13	100	0.65	90	N
W61	425	13	100	0.65	120	Y (kinked)
W53b	450	13	100	1.3	80	N
W59	450	13	100	1.3	80	Some on Surface
W68	450	13	100	1.3	80	Some on Surface
W70	450	13	100	1.3	80	N
W48	450	13	50	0.65	30	N
W71	450	13	50	0.65	30	N
W73	450	13	50	0.65	30	N
W 85	500	13	100	0.65	20	N
W 87	500	3	10	0.65	240	Y
W 91,93, 94	500	3	10	0.65	210	Y
W 45	500	3	50	0.65	45	Y

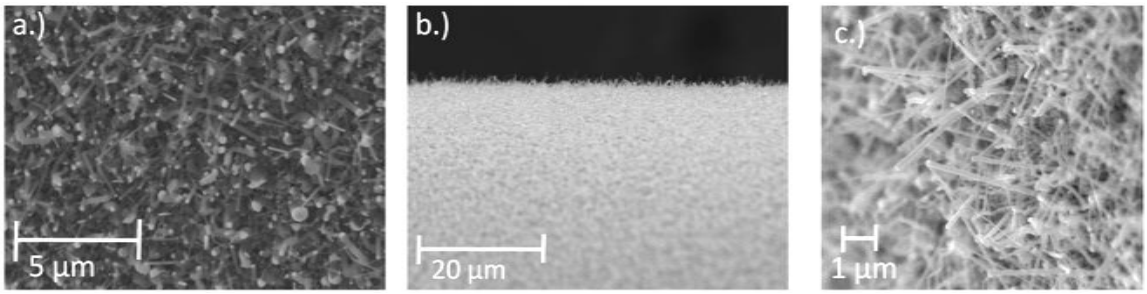


Figure **5-18**: SEM images of the sample using optimized nanowire growth conditions a.) top down b.) low magnification image showing surface curvature and c.) Side view showing high wire density.

5.4 Conclusions

The growth of high density, intentionally doped silicon nanowire arrays within the pores of AAO templates was demonstrated. A methodology was developed to contact and measure the resistance of the SiNW arrays, and nanowire resistivity was extracted from plots of array resistance versus nanowire length. The NW resistivity measured from the arrays decreased with increasing dopant/SiH_4 ratio and compared favorably with resistivity data obtained from four-point measurements of individual SiNWs grown under identical conditions. The AAO templates were found to introduce unintentional acceptors into the SiNWs during growth resulting in a resistivity in the range of 1-3 Ω-cm for nominally undoped SiNWs.

We have also demonstrated the ability to grow Si nanowires on low cost substrates using the AAO as a template. For successful nanowire growth on templated glass, the ITO layer that the SiNWs grow on can serve as a backside contact for solar devices. By utilizing the AAO template on the glass substrate, it was possible to grow a high density array of single crystal doped silicon

nanowires. The average nanowire diameter growing from the pores was 86 +/-18 nm, which is slightly less than the average pore size of 98 +/- 23 nm. From cross-sectional FESEM images it can be seen that not every pore had a nanowire growing from it, however, the nanowire density was high based on the plan view. The yield was not determined because the nanowire length and density covered the pores. The nanowire yield per pore could be improved through a careful study of growth and processing conditions. The nanowire yield is important because if a subsequent layer is deposited on the wires, it is possible that the n-type Si could diffuse into a pore without a nanowire and short out the diode. The growth of these SiNW arrays on glass is an important step in the realization of using SiNWs in a cost effective solar device. This method could be extended by the development of a radial coating and is reported in Chapter 6.

Finally, successful nanowire growth was achieved on a more complex low cost aluminum wire. For conformal nanowire growth in a full 360 degrees, a specially designed quartz boat was required. A range of growth conditions was explored to allow for better gas flow into the AAO pores to reach the Au seed layer. For optimal growth a lower system pressure was used in order to increase the diffusion into the pores.

5.5 References

1 L. Tsakalakos, J. Balch, J. Fronheiser, B. A. Korevaar, O. Sulima, and J. Rand, Appl. Phys. Lett. **91** (2007).

2 L. Tsakalakos, J. Balch, J. Fronheiser, M. Y. Shih, S. F. LeBoeuf, M. Pietrzykowski, P. J. Codella, B. A. Korevaar, O. Sulima, J. Rand, A. Davuluru, and U. Rapol, **1** (2007).

3 T. E. Bogart, S. Dey, K. K. Lew, S. E. Mohney, and J. M. Redwing, Adv. Mater. **17,** 114 (2005).

4 A. M. Mohammad, S. Dey, K. K. Lew, J. M. Redwing, and S. E. Mohney, J. Electrochem. Soc. **150,** G577-G580 (2003).

5 K. K. Lew, L. Pan, T. E. Bogart, S. M. Dilts, E. C. Dickey, J. M. Redwing, Y. F. Wang, M. Cabassi, T. S. Mayer, and S. W. Novak, Appl. Phys. Lett. **85,** 3101-3103 (2004).

6 Y. F. Wang, K. K. Lew, T. T. Ho, L. Pan, S. W. Novak, E. C. Dickey, J. M. Redwing, and T. S. Mayer, Nano Lett. **5,** 2139-2143 (2005).

[7] D. K. Schroder, *Semiconductor Material and Device Characterization*, 3rd ed. (John Wiley & Sons, New York, 1998).
[8] K. K. Lew and J. M. Redwing, J. Cryst. Growth **254,** 14-22 (2003).

Chapter 6

Epitaxial Regrowth of n-type Si

6.1 Introduction

The overall goal of this study is to develop the synthesis and processing technology to create large area radial p-n junction silicon nanowire arrays on Si (111) that can serve as photovoltaic devices. The previous chapters have discussed in detail the synthesis of SiNW arrays using different precursor gases and substrates. The final step in realization of a p-n junction SiNW array involves the epitaxial regrowth of n-type Si on the previously grown p-type SiNW arrays. To date there has been little work carried out on the deposition of radial nanowire coatings. It is desirable for the coating to be epitaxial, to achieve a high quality p-n junction interface. Any defects or impurities at the interface could affect eventual device performance. Prior literature studies have primarily reported polycrystalline Si coatings. The Au catalyst should also be removed since Au forms deep level states in silicon, which would affect the device performance. Recent reports on the fabrication of silicon nanowire solar cells have not explored in detail nor the conditions required to achieve radial epitaxial Si coatings on nanowire arrays. To date silicon shells deposited on SiNWs have been amorphous or polycrystalline (section **1.2.1**).

Studies carried out invesigated the growth conditions necessary to obtain uniformly thick epitaxial n-type Si shells on high aspect ratio SiNW arrays. Initial thin film growths were carried out on sapphire in order to characterize the doping, uniformity and thickness of the n-type Si films prior to deposition on the nanowires. Pre-treatment processing of the SiNW arrays was also examined, as that may impact the samples properties. The structural properties of the coatings as a function of growth conditions was investigated.

6.2 Silicon Substrates

Initial work on the electrical properties and growth rates for the n-type coating process will be discussed. This section will then describe the investigation of n-type Si regrowth on SiNW samples grown on silicon substrates. This includes a description of the different sample types, sample preparation and challenges, and the development of growth conditions needed to achieve epitaxial n-type Si regrowth.

6.2.1 Sample Types

Several different nanowire samples were used as substrates for the coating experiments. These include SiNW arrays grown from Au thin films on Si(111), SiNWs grown on patterned silicon substrates, and silicon pillars formed by deep reactive ion etching. The goal of these experiments was to develop the conditions necessary to achieve a radial, epitaxial n-type Si coating on the SiNWs.

Silicon nanowire arrays grown using a Au thin film were described in Chapter **4** of this thesis. A 3 nm Au thin film was sputter deposited on Si(111). The nanowire average diameters ranged from 100-200 nm depending on the growth conditions. A representative image of nanowires grown at 1050°C, atmospheric pressure and a P_{SiCl4}=9 Torr is shown in Figure **6-1**. The silicon nanowire arrays were approximately 10 +/- 1.2 μm long. These samples were used for FESEM and TEM characterization.

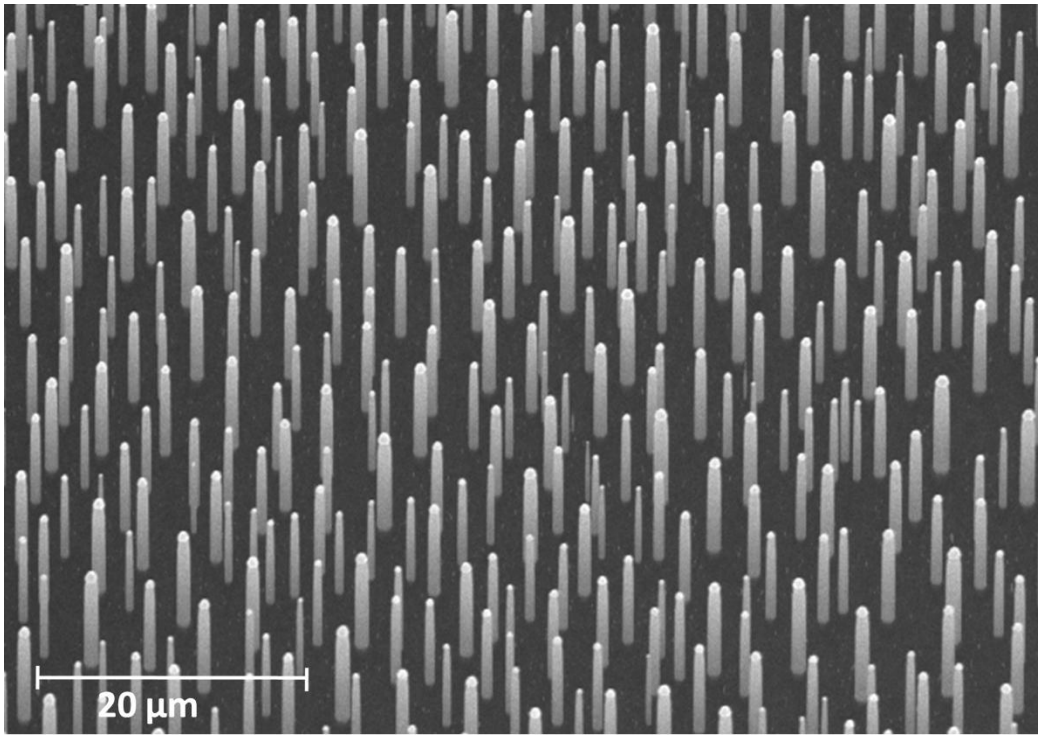


Figure **6-1**: SiNW arrays grown from a Au thin film on Si(111) and used for n-type Si regrowth experiments.

SiNW arrays grown on patterned Si(111) samples were also used for n-type Si regrowth experiments. These samples were fabricated and grown by Dr. Chito Kendrick. The substrates consist of a Si (111) substrate with an oxide layer that has lithographically defined pores. The patterned pores were etched using reactive ion etching (RIE) through the oxide to the Si (111) substrate. Au was then thermally evaporated into the pores using thicknesses between 300-500 nm. The remaining Au was then removed through lift-off and the Au left in the pores was annealed between 950-1050°C in H_2. The patterned samples had nanowires approximately 1-2 µm in diameter, depending on the pore size and Au thickness, and the wires were roughly 10 µm long, shown in Figure **6-2**.

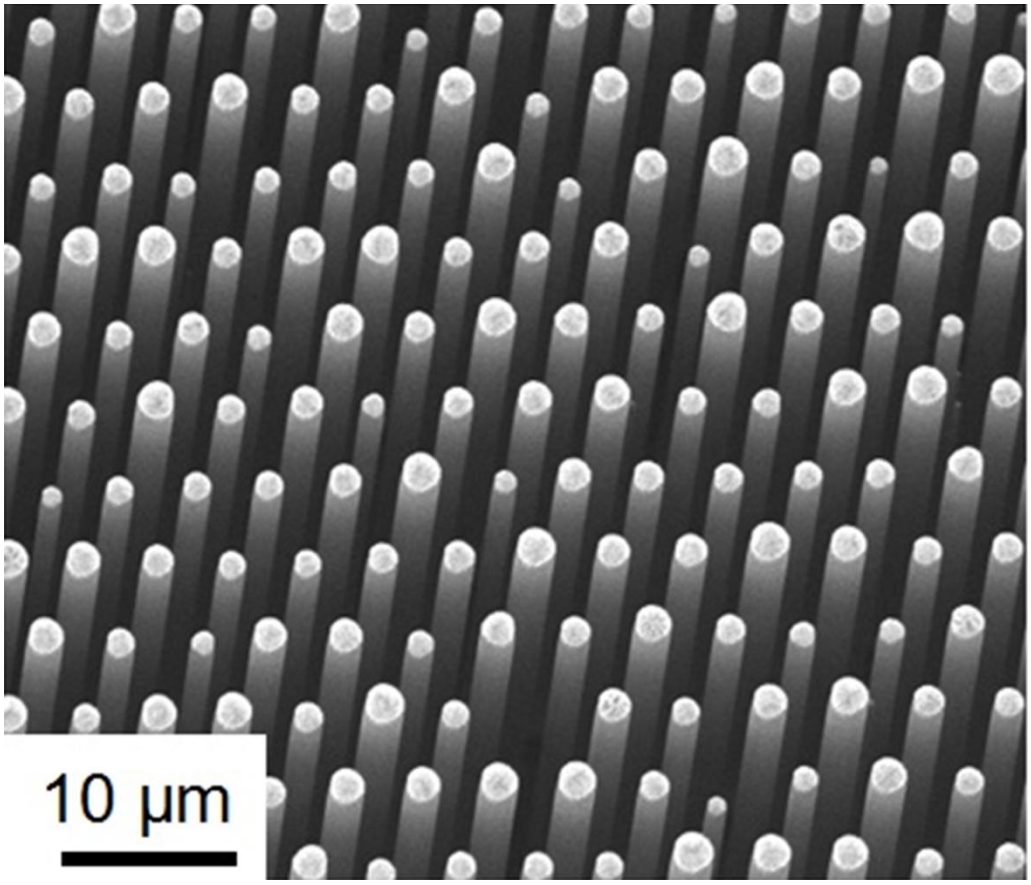


Figure **6-2**: SiNWs grown by VLS at 1050°C and P_{SiCl4}= 3 Torr on a patterned Si substrate.

Finally, silicon pillar arrays fabricated by Dr. Heayoung Yoon and Yu Yuwen were also used to investigate the epitaxial n-type Si regrowth. The pillar samples were fabricated on a p-type Si wafer using deep reactive ion etching. The pillars were 25 microns long and have diameters ranging from 1-3 µm depending on the sample. A representative FESEM image showing the pillar structure is shown in Figure **6-3** below. Both the patterned VLS grown SiNWs and the etched silicon pillars were used for electrical characterization.

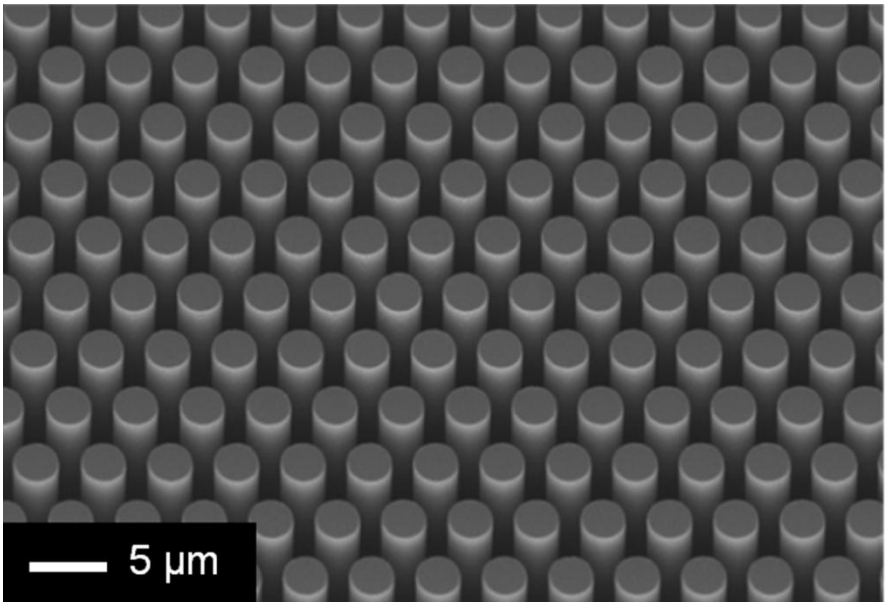


Figure **6-3**: FESEM image showing etched Si pillars.

6.2.2 Sample Preparation

The development of the radial n-type coating is important, but before coating experiments could begin the sample preparation must first be worked out. In order to achieve a clean interface between the SiNW and the n-type Si shell, there cannot be an oxide present. So during sample preparation, the oxide must be removed. The second question is the presence of Au, which is present on the tip of the SiNWs after VLS growth. The sample preparation for the silicon pillars was relatively straightforward since the pillars are thick (~1-3 µm) and there is no Au present on the sample. Preparation for the pillar samples required a 2 min 10:1 BOE etch to remove a 200 nm oxide on the pillars before placing the samples into the reactor.

Since it previously was reported that SiNWs can be radially coated with Si, without removing the Au tip[1], the first question to answer was whether or not the Au tips had to be removed for the n-type Si coating experiments. For an initial attempt at a radial n-type Si coating,

SiNW arrays grown using a 3nm Au thin film were used to determine the effect of the Au catalyst being left on the SiNW tips. The free standing SiNW arrays grown using $SiCl_4$ were used for n-type Si shell deposition. The temperature and pressure used was 650°C and 10 Torr respectively, similar to conditions reported by Tian *et al*.[1] Prior to growth, the Au was left on the nanowires and a short HF dip (10 sec) was done to remove any oxide that may have been present on the sample. Figure **6-4** shows FESEM images of the results. The sample consists of the initial SiNWs with small nanowire branches growing off of them. This indicates that the Au tips, which had diffused down the wire during initial SiNW growth, nucleated additional small SiNWs to form a "nanoforest", which has also been reported by Doerk *et al*.[2] The nanowire diameter increased after the deposition which means that while the Au nucleated additional nano branches, the actual main wire does have some n-type film deposition. The diameter of the nanobranches varies from 25-50 nm. This shows that the removal of Au prior to n-type shell deposition is a necessary step in the process. The removal of the Au tip was carried out on both patterned and Au thin film samples.

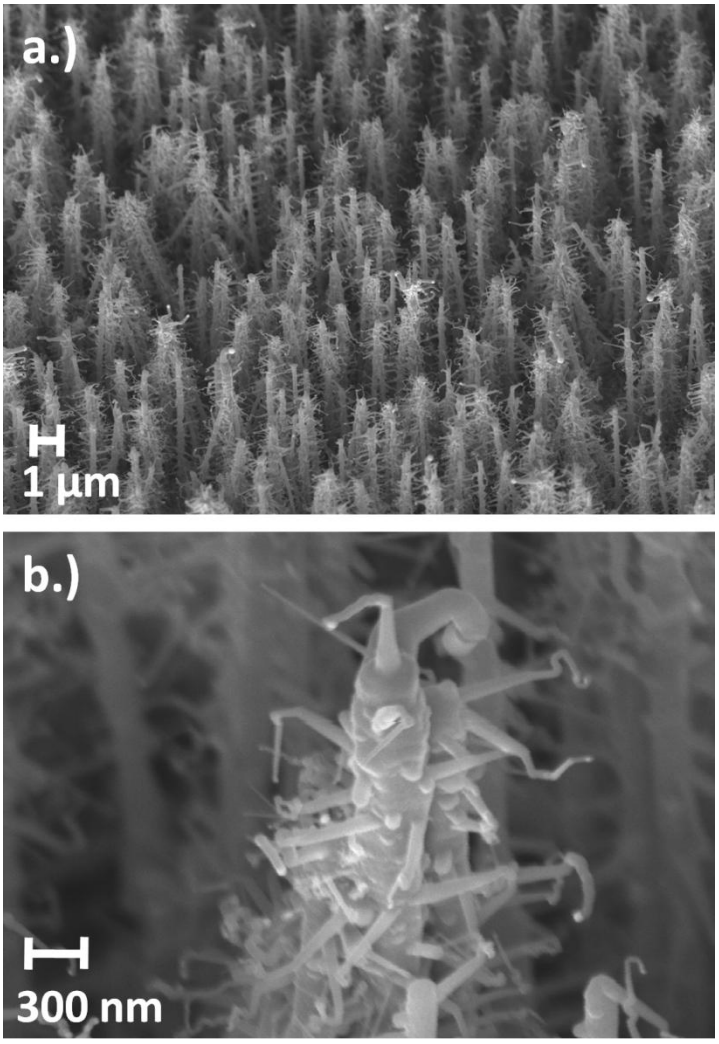


Figure **6-4**: FESEM image of a.) a "nanoforest" caused by trying to epitaxially regrow SiNWs without removing the Au tip and b.) a higher magnification image showing the many branches growing from a single nanowire.

Sample preparation for the smaller diameter (~100-200 nm) silicon nanowire arrays was then studied. The samples were grown using a 3nm Au thin film on a Si(111) substrate with $SiCl_4$ as the Si precursor. The nanowire growth conditions for these samples were discussed in Chapter **4**. In order to obtain a clean interface with negligible Au on the VLS grown SiNW arrays, the Au tip and any native oxide must be removed.

To remove the Au tips, a KI/I_2 complex commercial Au etchant (GE-8148) was purchased from Transene. The samples were immersed in the Au etchant for 10 minutes. Upon

removal of the sample from the Au etchant, the sample was rinsed in DI water. The samples were then left to dry in air. Examination of the samples using the Phillips XL-20 SEM followed to determine if the Au tips had been removed. Figure **6-5** shows an image of the sample a.) before and b.) after the Au etching step. Prior to the Au etchant step the nanowires did possess some cross-growth but there was also a large number of oriented SiNWs growing straight with respect to the substrate surface.

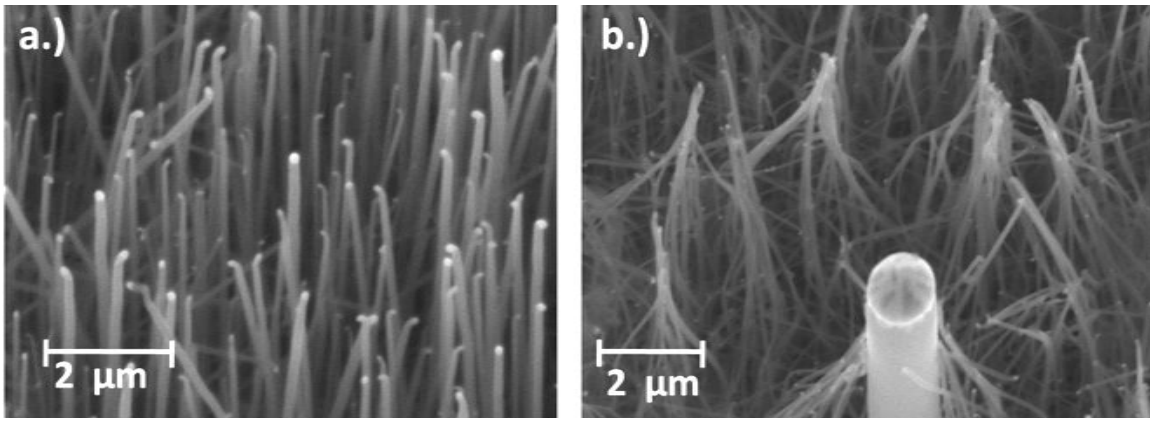


Figure **6-5**: SEM image showing the free-standing SiNW samples grown using $SiCl_4$ both a.) before and b.) after the Au etching process.

As can be seen in Fig. **6-5** (b), most of the Au tips are no longer present at the nanowire tip; however, the wires are bunched together or "tented". The tenting appears to be caused by liquid surface tension on the small diameter SiNWs pulling the tips together. To try and improve the Au etching on the SiNWs and attempt to dry the samples in such a way they did not tent, a series of experiments was carried out using samples from the growth run mentioned above to directly compare the method of drying. Samples were placed in the Au etchant for 10 minutes and then rinsed in DI water followed by either ethanol or hexane (C_6H_{14}). Ethanol has a liquid surface tension of 22.3 dyne/cm and hexane has an even lower surface tension of 18.4 dyn/cm at 20°C respectively.[3] Samples place in hexane were then removed from the hexane and left to dry.

Samples placed in ethanol were then placed in the critical point dryer available in the Huck Institute for Life Sciences Electron Microscopy facility. The critical point dryer uses supercritical CO_2 to dry the samples and avoids the damaging effects of surface tension. SEM micrographs in Figure **6-6** show the sample after Au etching and drying in (a.) hexane and (b.) critical point drying.

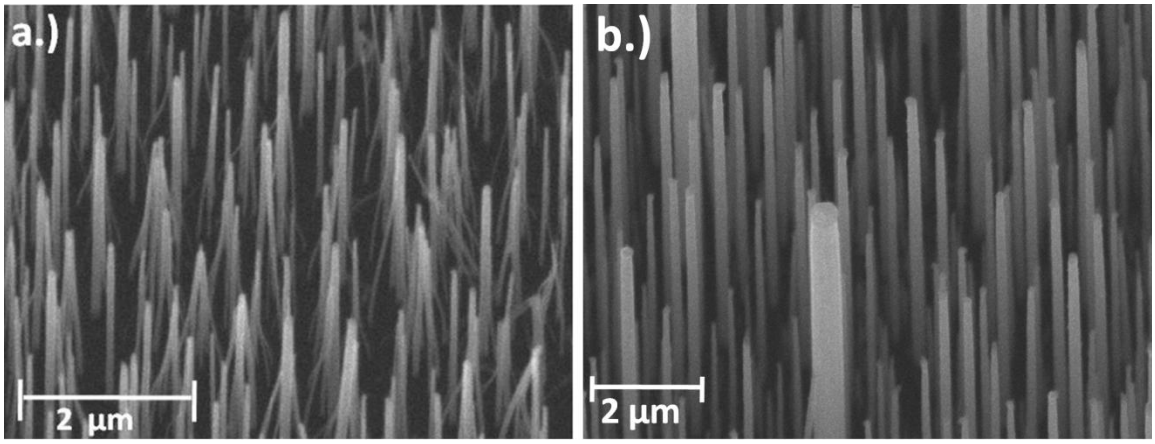


Figure **6-6**: SEM micrographs showing Au tip removal and sample drying in a.) hexane and b.) critical point drying.

The hexane did reduce the extent of nanowire tenting; however, there were still many wires that had tented. The sample dried using the critical point dryer (Fig**. 6-6 (b)**) did significantly reduce the amount of tenting. The subsequent samples were then dried using the critical point dryer.

The overall process used for sample preparation is described as follows. After SiNW growth, the Au tips were etched using KI/I_2 commercial Au etchant for 10 minutes, rinsed in DI water and finally dipped in BOE to remove any native oxide. The samples were then placed in ethanol and taken to the critical point dryer for drying. Since the critical point dryer is located across campus from the growth reactor, the samples were also dipped into a buffered oxide etch immediately prior to placing the SiNW samples in the reactor for n-type Si shell deposition.

Si coating experiments were also carried out on larger diameter silicon nanowires (0.5-2 μm) grown on patterned substrates. Samples were grown using $SiCl_4$ with conditions identical to the nanowires grown from Au thin films. The patterning allowed for growth of large and uniform wire diameters. These samples also allowed for the control of nanowire spacing on the (111) Si substrate. The larger wire diameters (0.5 - 2μm) were not as affected as much as the smaller diameter wires by the liquid surface tension so tenting was not readily visible. As a result, the patterned samples were handled similarly, after the Au tip removal, to the etched pillar samples described above. On the larger diameter SiNWs and also the etched pillars a BOE etch was done to remove any native oxide and is discussed at the beginning of section **6.2.2**. It was also noticed that larger diameter SiNWs required a longer etch to completely remove the Au tips. For nanowire diameters greater than 250 nm, the nanowire tips were etched for 30 minutes in order to make sure the Au had been completely removed. Figure **6-7** shows an SEM image of a patterned SiNW array on Si(111) after a Au etch. As can be seen in the photo the Au tips are no longer present. There does appear to be something left on the tip of the nanowires after etching. Since the nanowires are cooled rapidly, there may be some Si left in the Au that does not get etched away.

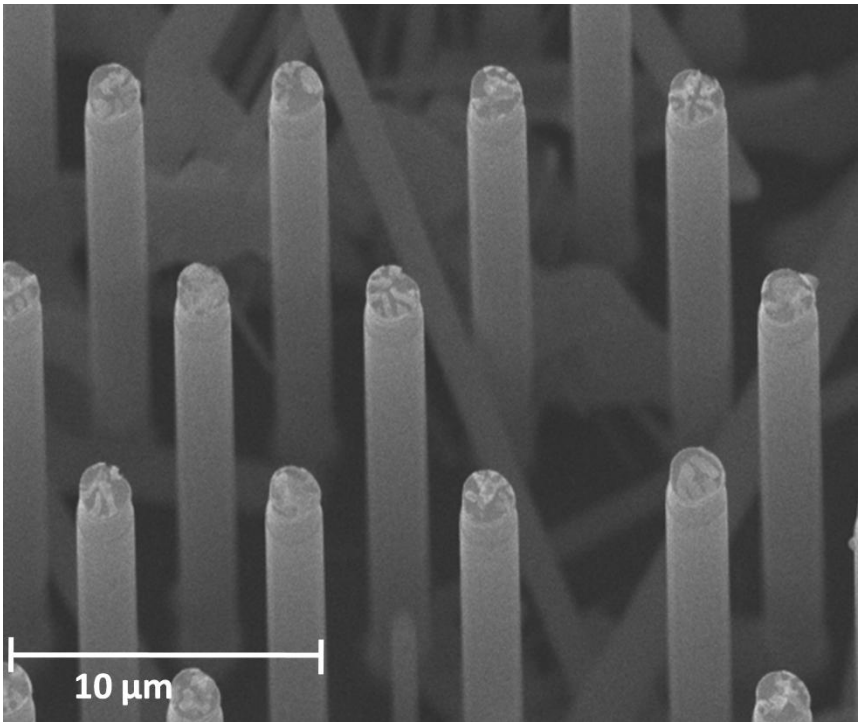


Figure **6-7**: Patterned SiNWs on Si(111) after a 30 minute Au etch.

6.2.3 n-type Si Thin Film Development

In order to understand and control the n-type silicon thin films on a SiNW array, it was first necessary to develop the processes and conditions necessary to achieve uniform and controllably doped silicon thin films. This section describes the calibration experiments that were carried out to determine the appropriate conditions required to deposit highly doped ($n>10^{19}$ cm^{-3}) n-type Si films with good thickness uniformity at the temperature range of interest (650-950°C). In order to determine growth rates and film resistivity, depositions were first carried out on sapphire substrates to enable selective etching and electrical characterization. The sapphire substrates were cleaned by sonicating the substrate for 10 minutes each in Acetone, IPA, and DI water. Samples were then blown dry using N_2.

6.2.3.1 n-type Silicon Deposition

Samples were loaded into the Labview controlled LPCVD reactor located in 220 EE West described in section **3.2.2**. This reactor is equipped with 500 ppm phosphine (PH_3) in H_2, which was used as the n-type dopant gas. The PH_3 lecture bottle was purchased from Voltaix Inc. For all n-type epitaxial regrowth experiments, a 10 % silane (SiH_4) in H_2 gas mixture was utilized as the Si precursor. The use of SiH_4 as the silicon gas precursor for the epitaxial regrowth experiments provides the ability to obtain thin film deposition at much lower temperatures than is required for $SiCl_4$. SiH_4 also will not form HCl, which can lead to etching of the film. Silicon thin film deposition was carried out using the process described in section **3.3.2.2**. The main difference for the thin film depositions is the process conditions were altered from that used for VLS growth to promote radial growth. This was done by growing at temperatures higher than 500°C. It was previously reported that thin film deposition begins to take place using SiH_4 at temperatures above 525°C in our LPCVD system.[4]

A range of growth conditions were considered in order to determine an optimal range for the deposition of n-type Si thin films. Growth temperatures between 650-950°C were investigated. The system pressure during growth was between 3-10 Torr. The lower pressure will increase the mean free path of the gas, allowing the gas further time to diffuse down into the nanowire arrays to increase the conformality of the coating. This is lower than the SiNW growth pressures of 13 Torr for VLS growth. A range of total flow rates were investigated between 100-400 sccm. Also, a range of SiH_4 flow rates were explored between 25-100 sccm. PH_3 was used as the n-type gas precursor. The PH_3/SiH_4 ratio was varied from 7×10^{-5} to 1×10^{-2}.

6.2.3.2 Sample Characterization

Sapphire substrates were used for initial characterization studies since the Si thin film needed to be selectively etched to measure the film uniformity and a growth rate. The n-type Si thin films on sapphire were placed on a glass slide and then set onto a hotplate at 165 °C. Once the samples were heated, black wax was then used to protect half of the sample. At this temperature, the black wax was pliable enough to cover the surface and serve as an etch mask. Any holes or non-uniformities in the black wax coating could lead to a poor step-height measurement. The samples were then removed from the hot plate and allowed to cool. The samples were then placed into a 30% by wt. KOH mixture held at a temperature of 80°C for 10 minutes. The black wax served as a protective barrier to the Si thin film. The areas not covered by black wax were etched away. The samples were rinsed in DI water and then sonicated in a bath of acetone for 30 minutes. The acetone removed the black wax leaving a sharp step from the Si thin film to the sapphire substrate. Profilometry measurements were carried out over the length of the substrate to measure the step height. Measurements were made with respect to the boat position to determine the film uniformity and also the growth rate.

In order to determine the electrical characteristics of the sample as a function of dopant/Si ratio, four-point resistivity measurements were made using a standard 4-pt probe. Hall effect measurements were also made at room temperature to determine the carrier type. Indium dots were placed in each corner of the sample and annealed at 100°C. Details of the Hall measurements and 4-pt resistivity measurements can be found in section **3.4**.

6.2.3.3 Effect of Growth Conditions

Based on prior literature for Si thin films and radial Si coating of SiNWs, a temperature of 650 °C with SiH_4 will yield a polycrystalline Si film[1,5]. For the initial development of an n-type Si deposition processes, 650°C was used as the starting temperature. Since the deposition temperature of 650°C may be too low to epitaxially regrow an n-type Si layer, further investigation focused on two higher temperatures of 850°C and 950°C. The sapphire substrates used for growth rate, uniformity, and resistivity measurements were expected to yield a polycrystalline Si thin film. For these experiments, two sapphire pieces approximately 2"× ¾" were placed along the length of the boat. These experiments were used to determine the film uniformity along the length of the boat. Initial experiments were carried out with a total gas flow of 100 sccm and a SiH_4 flow of 50 sccm for 5 minutes. The total system pressure was 10 Torr. Two boats were placed in the center of the hotzone to determine the range of thickness uniformity. A temperature profile for this reactor can be found in Dr. Robert Burke's thesis[6].

At a temperature of 650°C, the first sample (A) had a uniform film but the second sample (B) had a decreasing Si growth rate, shown in Figure **6-8**. Sample A was positioned closer to the gas inlet side of the reactor in the center of the hotzone and the second sample (B) was placed immediately behind it. The Si thin film deposition rate measured on the front sample was 18.6 ± 1.0 nm/min with good uniformity across the entire length. For the back sample, the growth rate decreased slightly with increasing distance along the sample length. This behavior arises due to depletion of SiH_4 from the gas stream which results in a gradual decrease in growth rate. The growth rate measured on the back sample was 16.4 ± 1.7 nm/min.

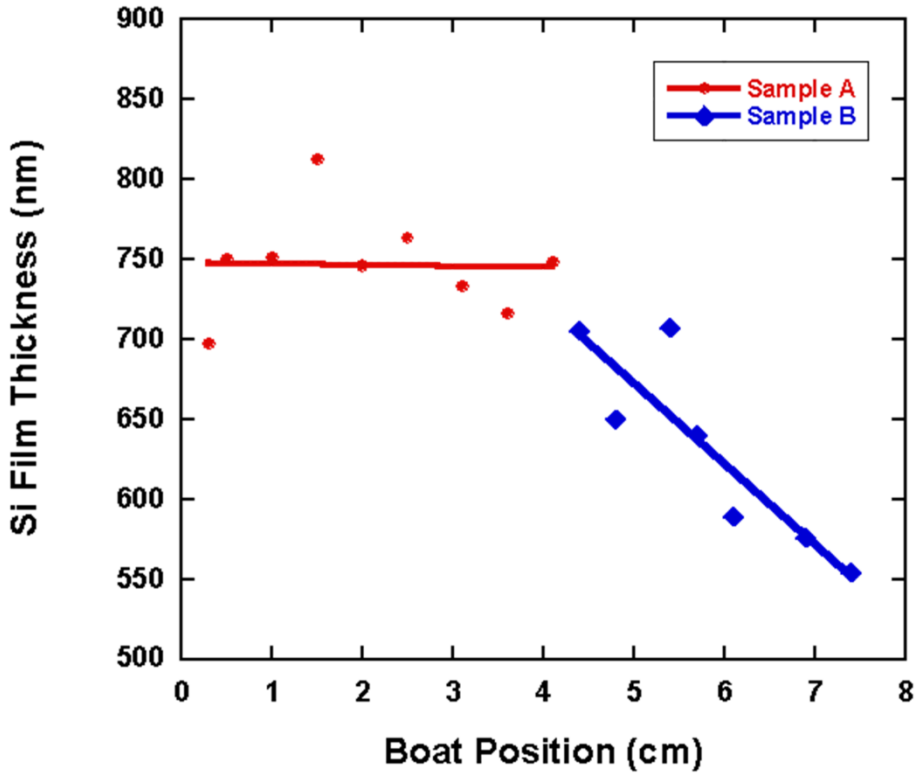


Figure **6-8**: Initial undoped Si thin film growth at 650 °C and a pressure of 10 Torr on sapphire, where sample A was placed in front of quartz boat and sample B placed towards the back of the boat.

At higher temperatures, the film uniformity across the length of the boat was expected to become worse due to increased SiH_4 reaction and gas phase depletion. To try and minimize the depletion effects, the total pressure of the system was lowered from 10 to 3 Torr for all experiments at temperatures of 850 and 950°C. Lower total pressures increase the mean free path of the gas, which may improve the film uniformity. At 850°C, the Si thin film thickness was found to be uniform over the first 3-4 cm of the boat (shown in Figure **6-9**) using a total pressure of 3 Torr, while at 950°C (shown in Figure **6-11**) the Si thin film thickness dropped off rapidly after the first 1.5 cm of the boat. Past the first 1" the silicon film was too thin for profilometry measurements. This is due to increased silicon depletion at the higher deposition temperatures.

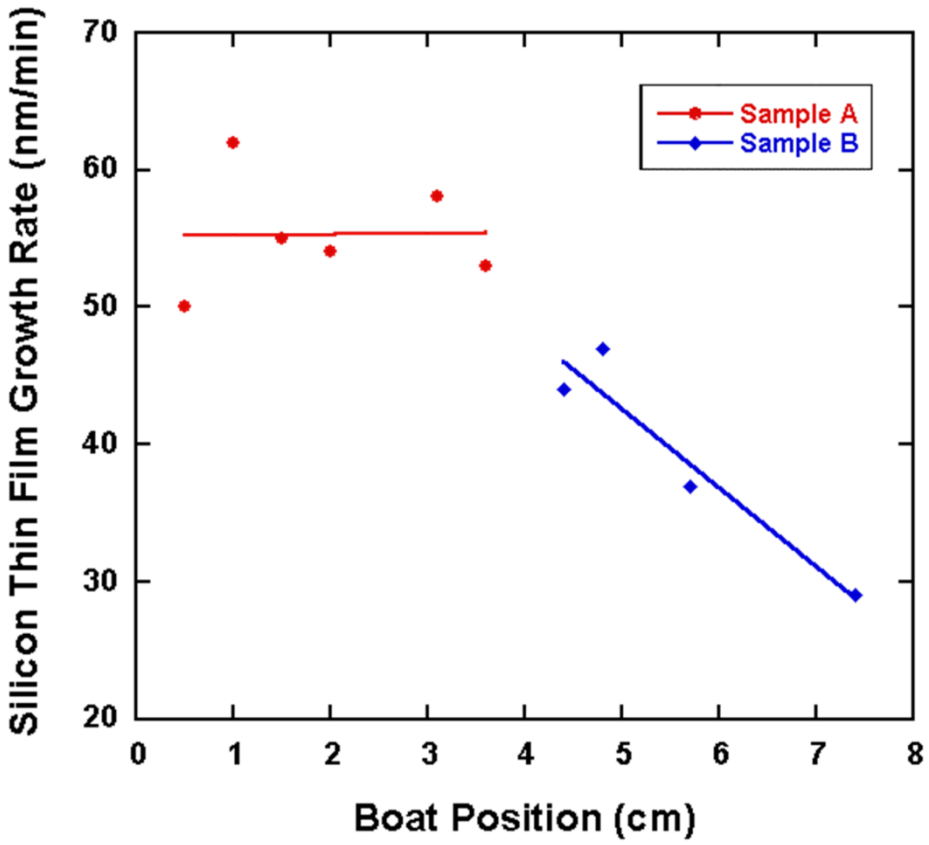


Figure **6-9**: Initial undoped Si thin film growth rate versus boat position at 850 °C and a pressure of 3 Torr on sapphire, where sample A was placed in front of quartz boat and sample B placed towards the back of the boat.

To determine the activation energy (Ea) a series of films were grown at each temperature (650-950°) and the growth rate at the front of the boat was measured. To keep the conditions consistent, the films were grown at a total pressure of 3 Torr, total gas flow of 100 sccm and SiH_4 flow rate of 50 sccm. The data was plotted using an Arrhenius form:

$$growth\ rate = Aexp\left(\frac{-E_A}{RT}\right) \quad (6.1)$$

where E_A is the activation energy for thin film deposition (shown in Figure **6-10**), R is the gas constant and T is temperature. The activation energy was calculated to be 15 kcal/mol, which is similar to the value of 20 +/-5 kcal/mol reported for thin film growth of SiH_4 by Henderson et al.[7]

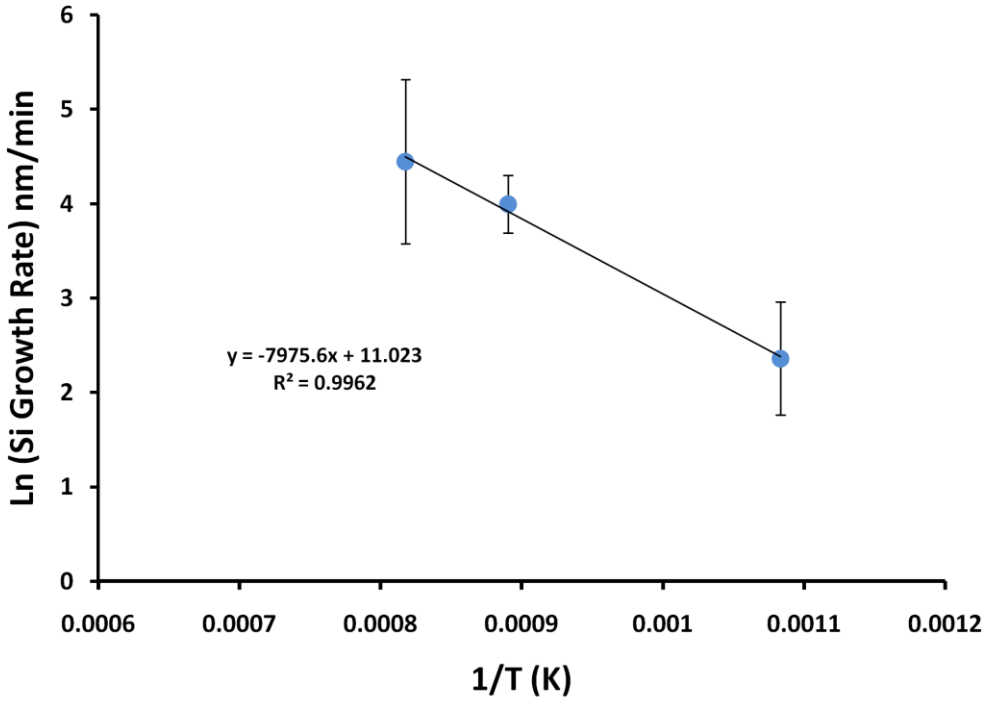


Figure **6-10**: Plot of Si growth rate versus temperature for Si thin film deposition using a flow rate of 50 sccm SiH_4, total flow of 100 sccm, and a pressure of 3 Torr.

The uniformity over the first 3-4 cm of the boat for films grown at 650°C and 850°C would be uniform enough to place 2 or 3 small samples or 1 larger sample in the boat for deposition. However, the Si depletion at 950°C is too large for uniform Si thin film deposition. In order to achieve better uniformity over a larger area and decrease depletion effects, a series of experiments were carried out varying the total flow rate and also SiH_4 concentration. The boat was also shifted 2" closer to the gas inlet to help combat depletion. Based on the temperature profile, the entire boat is still in the constant temperature region, so the entire boat should still be at a temperature of approximately 950°C. The total flow rate through the reactor across the samples was investigated first. By increasing the total gas flow, while keeping the P_{SiH4} constant, the average gas velocity is increased and the residence time in the reactor is decreased which

would decrease the extent of the SiH_4 reaction and gas phase depletion. A graph of the Si growth rate versus sample position in the boat is shown in Figure **6-11**. This is for a P_{SiH4} of 0.1 Torr at 950°C and a total system pressure of 3 Torr. The boat was shifted 2" past the hotzone center towards the gas inlet.

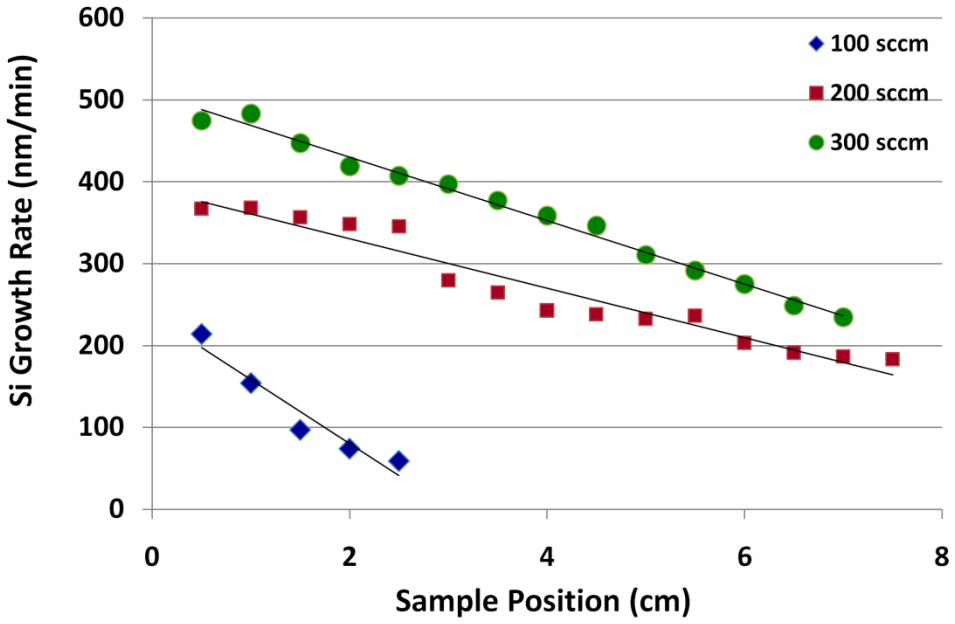


Figure **6-11**: Plot of Si thin film growth rate versus sample position at 950°C for different total flow rates.

The graph shows that a total flow rate of 100 sccm has the greatest amount of depletion. Increasing the total flow to 200 or 300 sccm greatly improves the uniformity thickness along the length of the boat and increases the growth rate. Although there still appears to be depletion present for higher total flow rates as the growth rate drops approximately 2 from the front to the back of the boat. Since a slower growth rate is desirable for thickness control, a total flow of 200 sccm was used for further experiments.

To further optimize depletion and growth rates at 950°C and 3 Torr, the P_{SiH4} was also varied using a total flow of 200 sccm to determine the growth rate. Figure **6-12** shows a plot of

Si growth rate versus the P_{SiH4}. As can be seen from the plot, as the P_{SiH4} was increased the growth rate also linearly increased. For this graph the Si growth rate was measured on the sample closest to the inlet, within the first 1 cm of the boat.

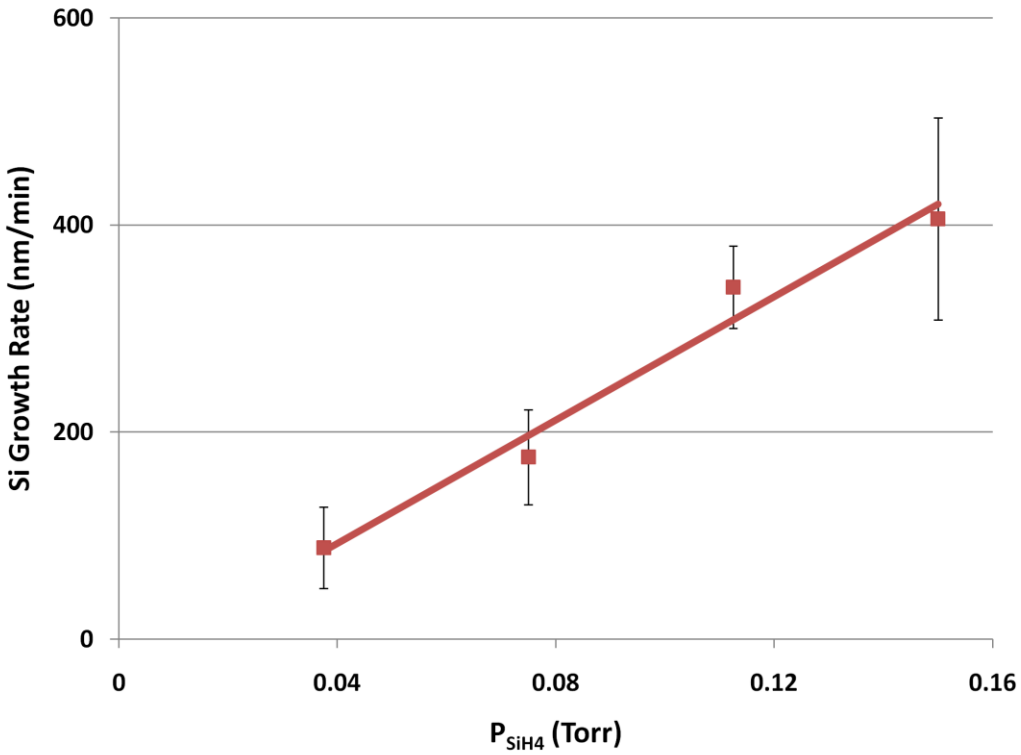


Figure **6-12**: Plot of Si thin film growth rate versus the P_{SiH4} at 950°C and 3 Torr.

Based on the initial high temperature experiments, samples grown at 850°C were placed in the center of the hotzone (a distance of 12" from the inlet) and grown using a total flow rate of 100 sccm and 50 sccm SiH_4 (P_{SiH4}=0.15 Torr). To increase the film uniformity across the length of the boat at 950 °C, the boat was placed 10" from the inlet to decrease the distance the SiH_4 traveled in the reactor before reaching the samples. The total flow will be increased to 200 sccm and the P_{SiH4}=0.037 Torr to maintain a slow growth rate, while still minimizing the effect of depletion in the reactor. Table **6-1** below shows the silicon growth rate for each temperature and optimized growth conditions.

Table **6-1**: The growth rate and growth conditions that were found to be optimal for specific growth temperatures.

Temperature (°C)	Pressure (Torr)	Total Flow (sccm)	SiH_4 Flow (sccm)	Growth Rate (nm/min)
650	**10**	**100**	**50**	**18.1**
850	**3**	**100**	**50**	**54.3**
950	**3**	**200**	**25**	**124**

6.2.3.4 n-type Doping

Using these optimized conditions n-type doping experiments were then carried out to develop suitable conditions for the formation of radial p-n junctions. Si thin films were deposited at 950°C, 3 Torr, 25 sccm SiH_4 and a total flow rate of 200 sccm. The PH_3/SiH_4 ratio was varied from undoped (no PH_3) to a PH_3/SiH_4 ratio of 1×10^{-2}. Four point resistivity measurements were made using a 4-pt probe to determine the film resistivity. Hall measurements were also made to determine the resistivity, electron concentration and carrier type. Both methods were described in the experimental methods section **3.4**.

The carrier type for all of the silicon films doped with PH_3 are n-type (shown in Table **6-2**). The resistivity measurements for both the 4-point probe and Hall effect show that as the PH_3/SiH_4 ratio is increased the resistivity decreases. Samples with very low PH_3/SiH_4 ratios were not measured with Hall because the Indium contacts were not ohmic and are listed in the table as NA.

Table **6-2**: A comparison of the carrier type and resistivity measurements from both 4-point probe and also Hall measurements at a.) 850°C and b.) 950°C.

a.)

	4-pt Probe		Hall Measurement		
PH_3/SiH_4	ρ 850°C (Ω-cm)	Bulk Dopant Density[8] ($/cm^3$)	ρ 850°C (Ω-cm)	Bulk Density (Hall) ($/cm^3$)	Carrier Type
0	-	-	-	-	-
7.00E-05	3.32E+01	-	NA	NA	NA
2.00E-04	1.49E+00	3.00E+15	1.70E+00	1.50E+18	n
7.00E-04	2.63E-02	1.00E+18	2.51E-02	2.00E+19	n
2.00E-03	1.04E-02	2.00E+18	NA	NA	n

b.)

	4-pt Probe		Hall Measurement		
PH_3/SiH_4	ρ 950°C (Ω-cm)	Bulk Dopant Density[8] ($/cm^3$)	ρ 950°C (Ω-cm)	Bulk Density (Hall) ($/cm^3$)	Carrier Type
0	7.00E+01	-	NA	NA	NA
7.00E-05	7.15E+01	-	NA	NA	NA
2.00E-04	6.75E+00	5.00E+15	2.80E-01	2.60E+18	n
7.00E-04	1.40E-02	6.00E+18	1.30E-02	4.00E+19	n
1.00E-02	1.0E-02	1.00E+19	9.30E-03	2.00E+19	n

A log-log plot of the resistivity values for all the samples both at 850 and 950 °C as a function of PH_3/SiH_4 ratio is shown in Figure **6-13** below.

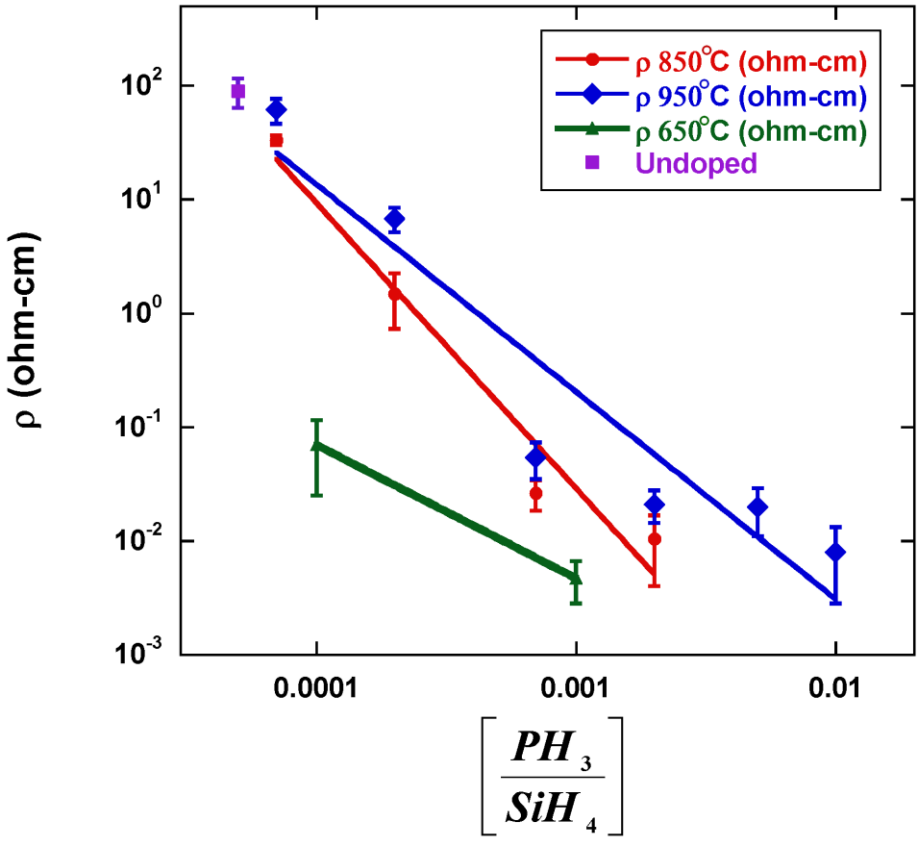


Figure **6-13**: Plot of resistivity versus the PH_3/SiH_4 ratio for n-type Si thin films grown on sapphire at 650, 850 and 950°C. The undoped Si thin film was grown at 950°C also.

As the PH_3 is increased the resistivity decreases indicating that the P is being incorporated into the film. The resistivity versus the PH_3/SiH_4 was fit to a power law where the resistivity (ρ) is equal to $[PH_3/SiH_4]^n$. At 650°C, n=-1.2, while at a temperature of 850°C and 950°C n is equal to -2.5 and -1.8 respectively. For a temperature of 650°C these resistivity values correspond to electron concentrations of $1.5\text{-}3\times10^{18}$ cm^{-3} ($PH_3/SiH_4=1\times10^{-4}$) and $1\text{-}2\times10^{19}$ cm^{-3} ($PH_3/SiH_4=1\times10^{-3}$), based on bulk mobility.[8] The undoped Si thin film, which was grown at a temperature of 950°C has a corresponding carrier concentration of approximately $10^{14}/cm^3$. The resistivity of $PH_3/SiH_4= 2\times10^{-3}$ is 0.02 Ω-cm, which corresponds to a carrier concentration of 10^{19} $/cm^3$ carrier concentration in n-type Si[8], this is similar to the bulk density from the Hall

measurements of $2\times10^{19}/cm^3$. The bulk dopant density was estimated from the four-point probe resistivity values assuming bulk mobility, these dopant density values are less than the bulk density calculated from the Hall measurements. This is due to the Hall measurements using the Hall mobility to determine the bulk density. The Hall mobility differs from conductivity mobility by a factor that is dependent on scattering mechanisms.

It has been previously reported that the Si deposition rate for thin films can change with the addition of phosphine.[5] A series of samples were grown with PH_3/SiH_4 ratios ranging from undoped to 5×10^{-3} and the growth rate was measured. Figure **6-14** below shows a plot of Si film thickness versus PH_3/SiH_4 ratio grown at 950°C. The Si thin film thickness does not vary with respect to the addition of PH_3 for the conditions that are being used. It is possible that higher PH_3 concentrations or increased deposition rates may have a greater effect on the growth rate but it does not apply to the conditions currently being used for radial n-type Si coating.

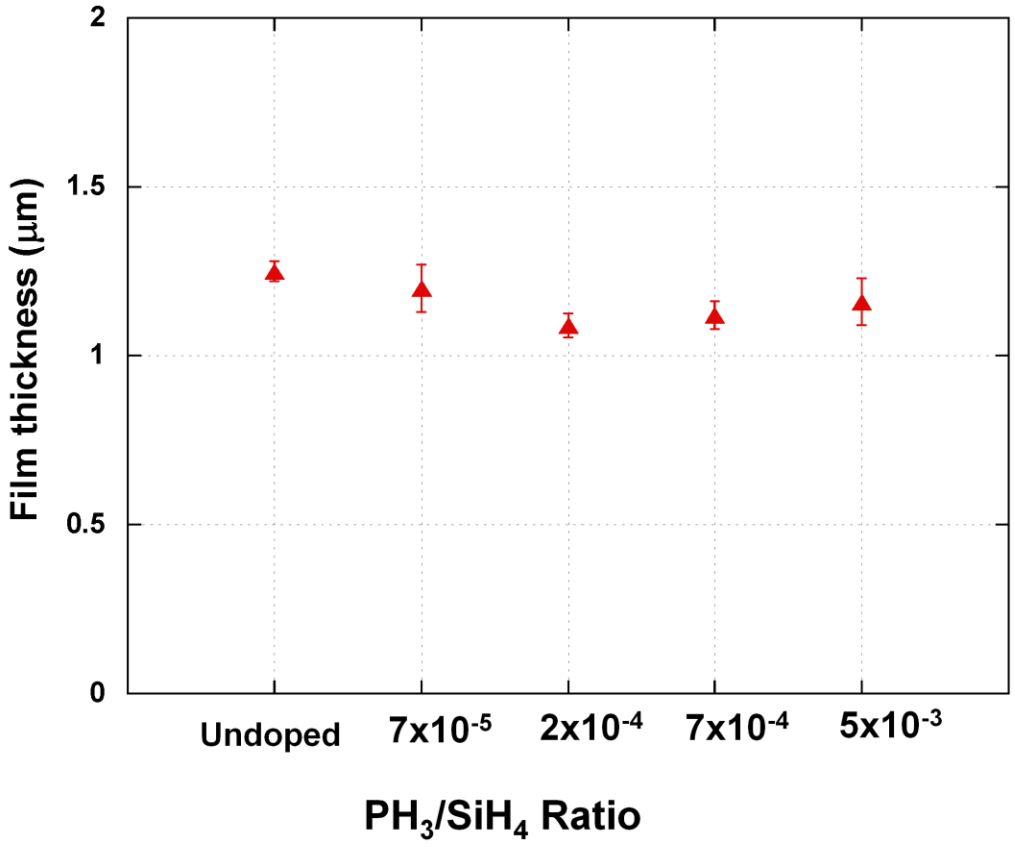


Figure **6-14**: Plot of Si thin film thickness versus PH_3/SiH_4 ratio.

6.2.4 Epitaxial n-type Si Regrowth

A range of process conditions were developed for the deposition of n-type Si thin films and the resistivity was correlated with a PH_3/SiH_4 ratio in the previous section. The following section investigates these growth conditions for the radial growth of n-type Si on SiNW arrays on Si(111) substrates. The samples coated included SiNWs grown from Au thin films, Au patterned samples, and etched Si pillars on Si (111). Each of these samples was prepared as described in section **6.2.2**. The goal of this investigation was to try and achieve a radial single crystal deposition on the nanowire arrays. The initial characterization and TEM was carried out on small

diameter (≤ 200 nm) samples. The conformality of the n-type Si coating and also the interface between the SiNW and n-type Si regrowth were studied. Larger diameter arrays of both the etched pillars and patterned $SiCl_4$ grown nanowires were coated using the same conditions to enable a direct comparison between etched and VLS grown Si wire arrays.

For each of these experiments, a SiNW sample grown from a Au thin film, patterned Au, and etched Si pillar were all placed into the reactor. The silicon nanowire arrays grown from the Au thin film (Fig. **6-1**) were approximately 10 +/- 1.2 µm long and had nanowire diameters ranging from 80-120 nm. The SiNWs grown on the patterned samples (Fig. **6-2**) were approximately 1 µm in diameter and roughly 10 µm long. The pillar samples (Fig. **6-3**) were 25 microns long with diameters ranging from 1-3 µm. The n-type Si deposition was carried out using phosphine (PH_3) and silane (SiH_4) as the n-type dopant and Si precursors. The PH_3/SiH_4 ratio was 2×10^{-3}. The growth conditions used for each temperature were based on the initial n-type Si development as listed in Table **6-1**. For these temperature experiments, the pressure was kept low (3 Torr) to try and increase the mean free path of the gas and improve the conformal coating. FESEM images of the n-type Si coating on SiNWs grown from a Au thin film are shown in Figure **6-15**. Figure **6-15(a)** and Fig. **6-15(b)** show the top and side of a SiNW after n-type Si deposition at 650°C. The surface appears rough and the nanowire appears circular in shape. Figure **6-15(c)** and Fig. **6-15(d)** show the n-type Si coating at a temperature of 850°C, where the nanowire has a hexagonal shape but also appears to be extremely rough. Figure **6-15(e)** and Fig. **6-15(f)** show a nanowire coated at 950°C. The surface of the wire appears smooth with many facets, while the overall shape of the wire appears hexagonal in nature.

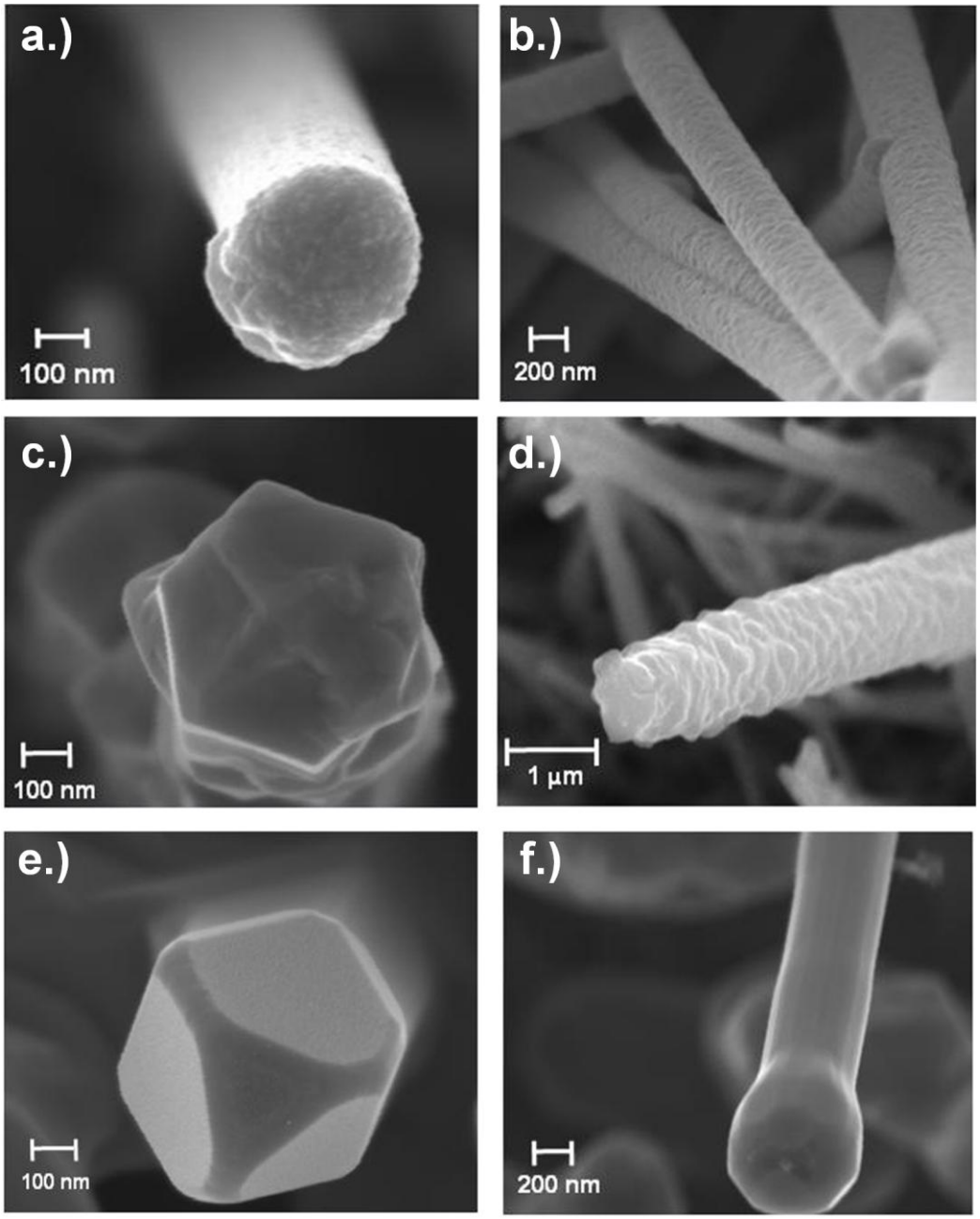


Figure **6-15**: FESEM images of the n-type Si deposition at a temperature of (a & b) 650°C, (c & d) 850°C and (e & f) 950°C showing both the tip of the nanowire and also a side view.

TEM characterization was then carried out on these core/shell structures by Dr. Xiaojun Weng and can be seen for n-type Si deposition at 650°C in Figure **6-16** below. As the deposition

temperature was increased, it was found that the n-type coating went from polycrystalline to single crystal.

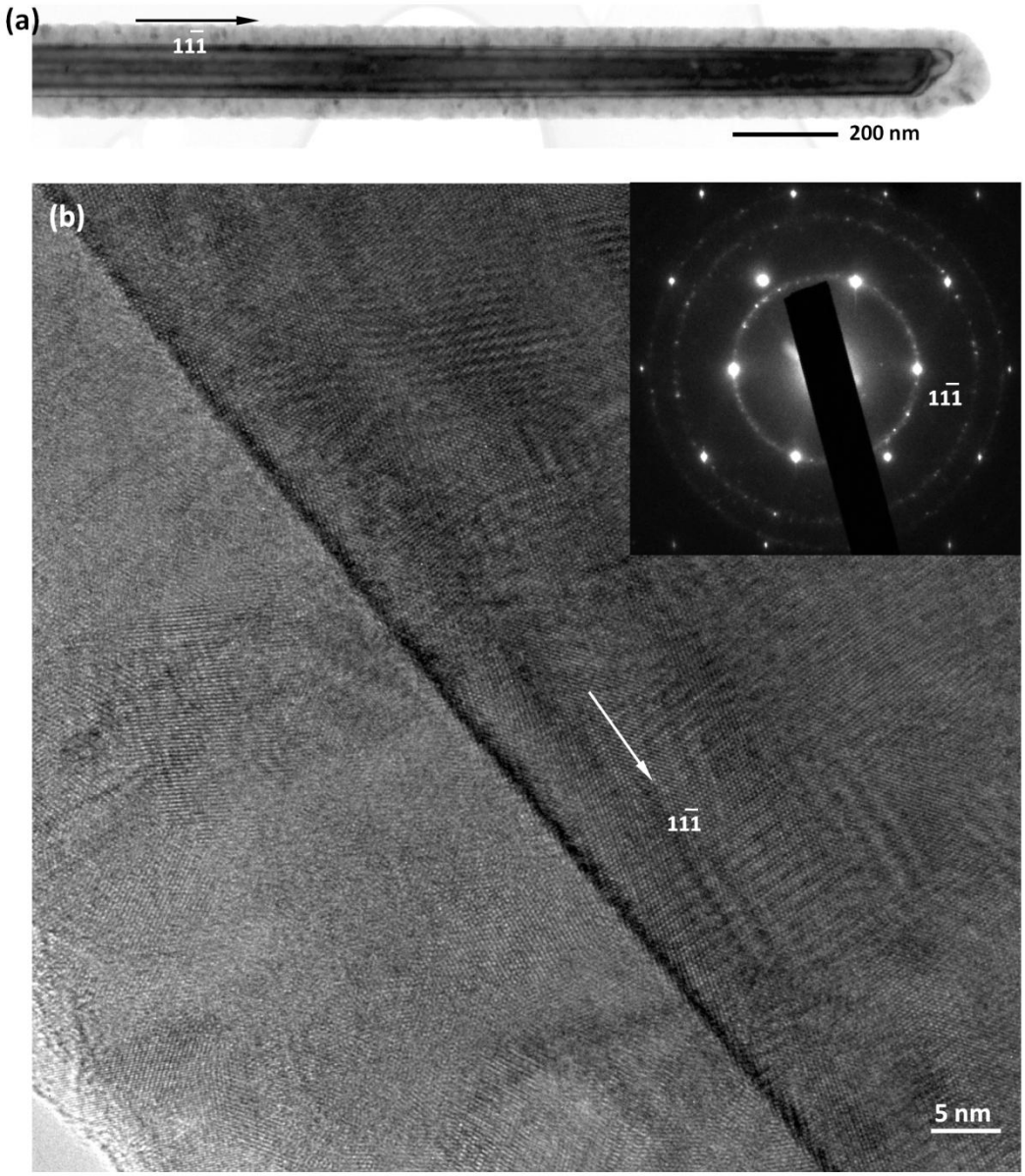


Figure **6-16**: (a)Low-magnification bright-field TEM image of a 650ºC core/shell Si NW. The shell is polycrystalline as indicated by the diffraction pattern shown in the inset of (b). High-resolution TEM shown in (b) indicates that the core/shell interface sharp.

For all of the samples, the nanowire core was single crystal and at 650°C as is shown in (Figure **6-16** (a.)), the n-type shell is polycrystalline and has a rough surface. The average grain size was 36 +/- 8.9 nm. As the temperature was increased to 850°C (Figure **6-17**) the shell has a larger average grain size of 96 +/- 33 nm and a thinner shell thickness.

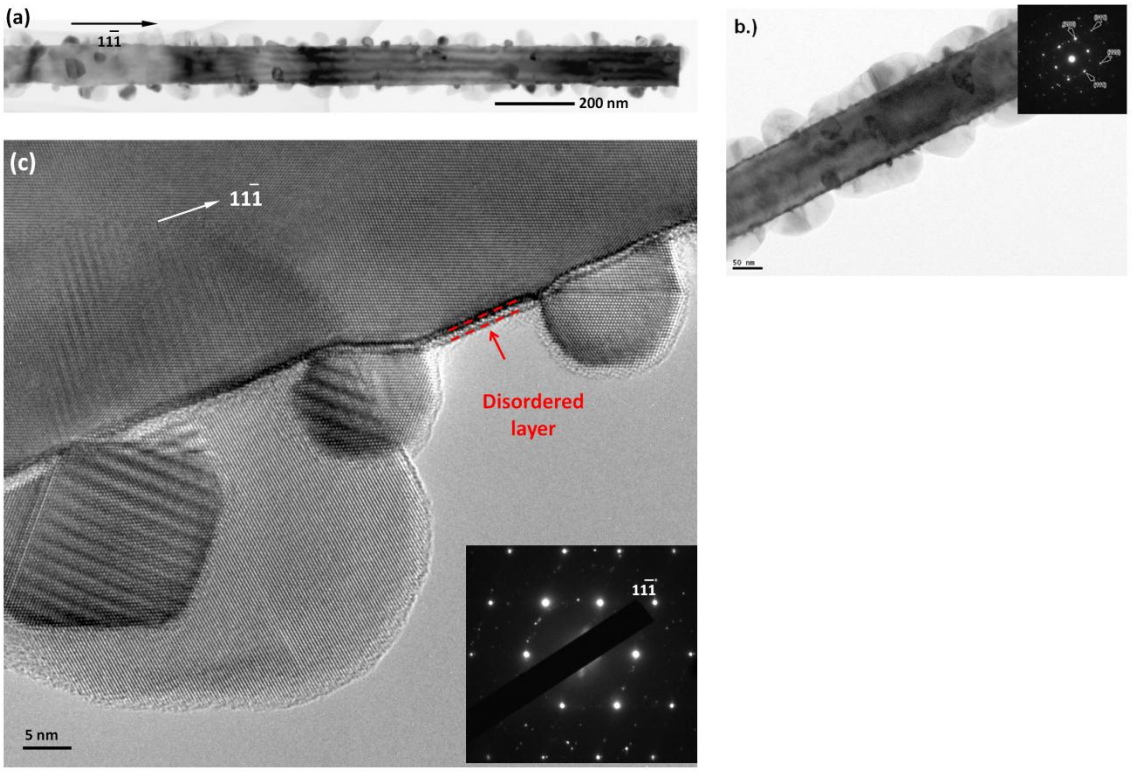


Figure **6-17**: (a)Low-magnification bright-field TEM image of an 850ºC core/shell Si NW. The shell is polycrystalline as indicated by the diffraction pattern shown in the inset of (c). The 850ºC shell layer is discontinuous and consists of nanometer scale Si islands. (b) Low magnification image of a different sample, also grown at 850°C. High-resolution TEM shown in (c) reveals a thin disordered layer at the core/shell interface.

The grains are not well coalesced. The increase in grain size with temperature is consistent with the zone structure model.[9] The grain structure depends on the amount of surface and bulk diffusion that occurs during deposition, which depends on temperature. The zone can be determined from the substrate temperature (T_s) and the melting temperature of the film (T_m),

which for Si is 1687K. At 650°C the T_s/T_m is around 0.5, which corresponds to zone II. In this zone the surface diffusion becomes more significant and the polycrystalline surfaces can be rough. At 850°C, the T_s/T_m is 0.6, which corresponds to zone III. In this zone, typically the bulk diffusion of atoms can give rise to larger grains and decreased roughness. The results are consistent with the zone model as the temperature increases the grain size also increases. The surface roughness is difficult to compare as the n-type Si film grown at 850°C did not fully coalesce. From the high resolution TEM (Figure **6-17(c)**) a thin amorphous layer is visible at the interface, this may be an oxide, which would prevent epitaxial growth from occurring.

At a higher temperature of 950°C with the same conditions (Figure **6-18**), the n-type shell is single crystal. The nanowire surface is smooth and the coating is growing epitaxially and it is difficult to distinguish the interface between the nanowire and the radial coating.

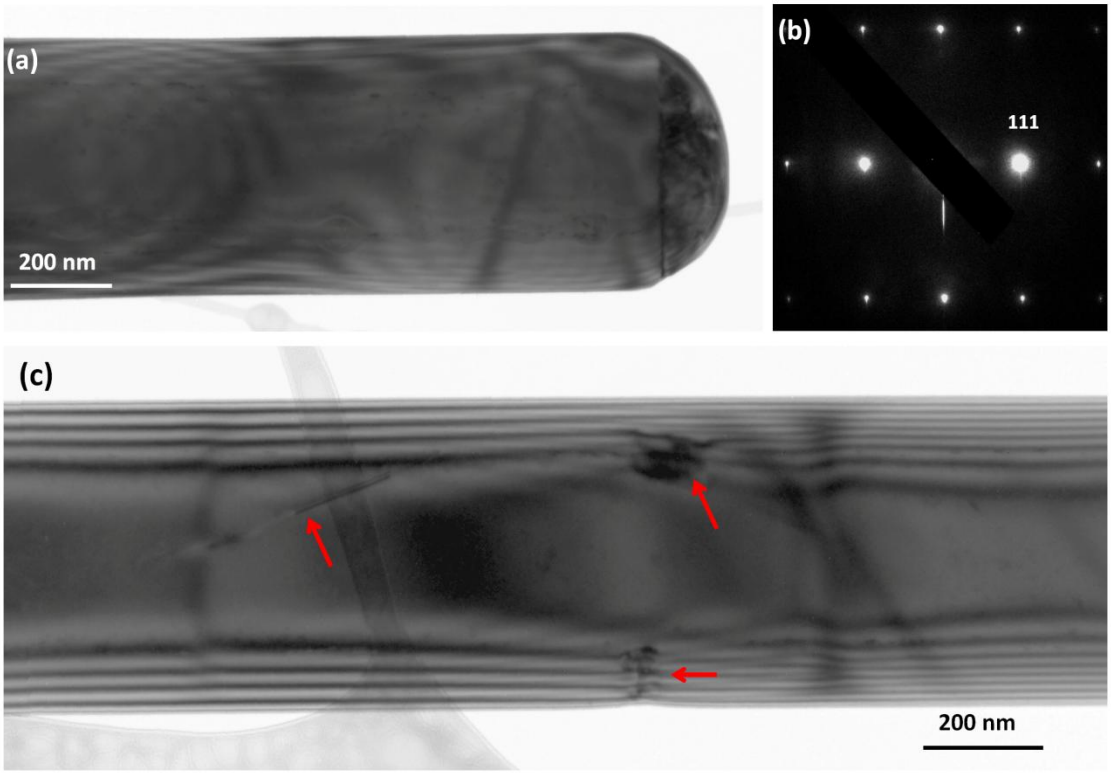


Figure **6-18**: (a) On zone axis bright-field TEM image of a core/shell Si nanowire collected near the top of the wire. (b) is the corresponding SAD pattern collected from the nanowire body. (c) Nanometer-scale black dots are often observed within the nanowires, that are likely defects.

The dark spots present in Figure (**6-18(c)**) are defects possibly present at the interface that could be dislocation loops due to stacking faults. The growth rate was measured based on the original nanowire diameter measured using FESEM images and ImageJ software, which was then subtracted from the measured radial coated nanowire diameter. TEM performed by Dr. Xiaojun Weng on the n-type coated SiNWs grown from a Au thin film revealed that the n-type coating at the tip of the SiNWs was highly defective, shown in Figure **6-18(a)**. This suggests that surface defects may have been introduced during the Au etching step.

Based on the above temperature results, a series of epitaxial n-type Si regrowth experiments were carried out at a temperature of 950°C, pressure of 3 Torr and P_{SiH4} of 0.037 Torr. The samples were doped with a PH_3/SiH_4 ratio of 2×10^{-3}. The SiNWs grown by VLS using a Au thin film and also patterned Au were placed in the reactor along with etched pillar samples for comparison. Figure **6-16** shows the etched pillar samples after n-type coating.

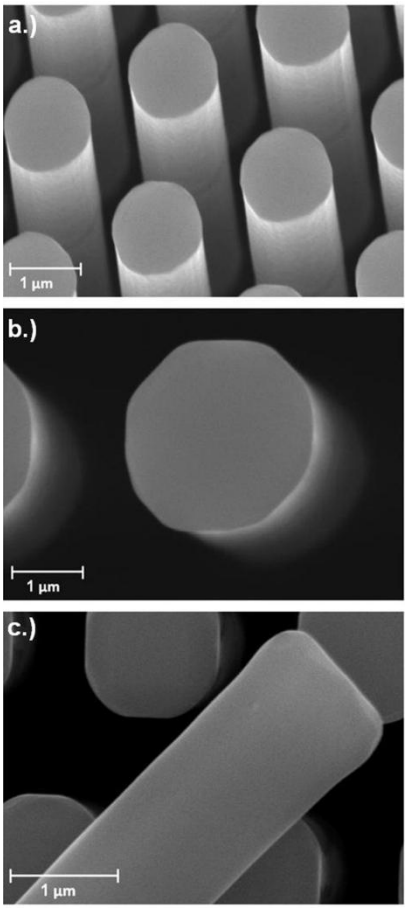


Figure **6-19**: SEM images of the etched Si pillars after radial n-type Si deposition showing the a.) pillar array at a 15 degree tilt, b.) plan view and c.) plan view of a pillar that had fallen over showing the pillar sidewall.

As can be seen, the pillar surface is smooth. Figure **6-20** shows an FESEM image of the n-type Si coating on VLS grown SiNWs, both the patterned samples and Au thin film samples. A direct

comparison between the etched Si pillars and VLS growth reveals a smooth surface on all samples. The etched Si pillars do not appear to have as distinct faceting as the VLS grown SiNWs do although this may be due to the larger diameter of the pillars.

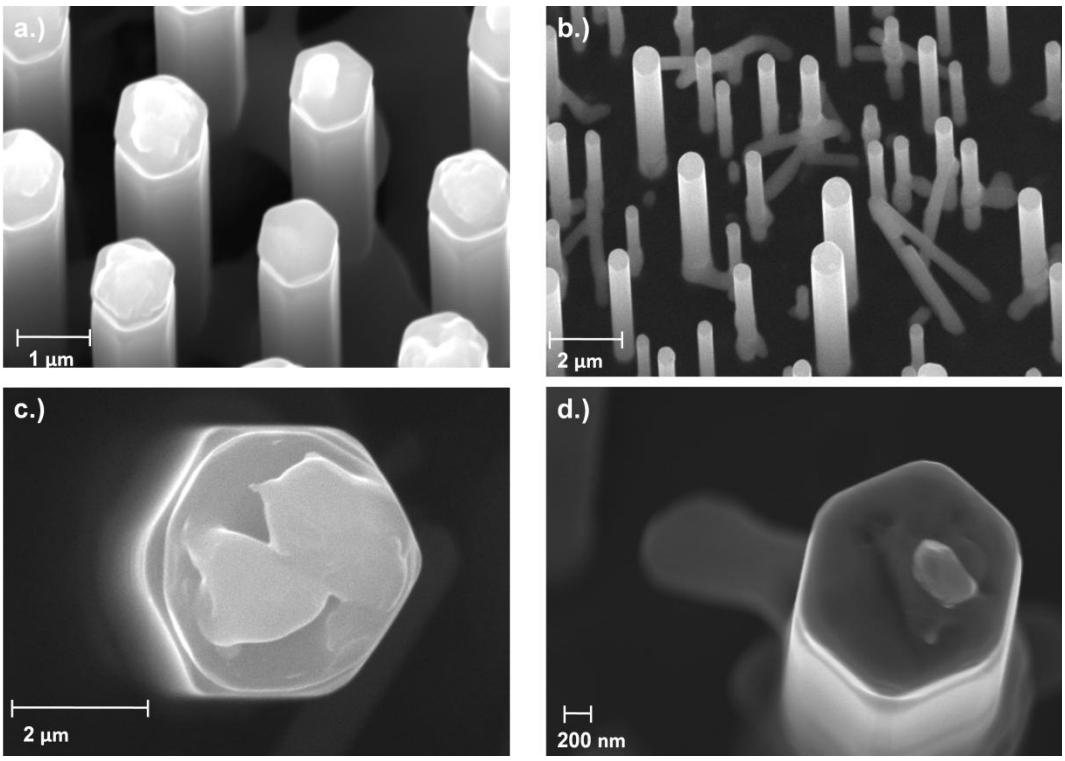


Figure **6-20**: FESEM of VLS grown SiNWs on Si(111) patterned with Au (a. & c.) and on Si(111) with a Au thin film (b. & d.) coated radially with n-type Si.

As can be seen, the VLS grown SiNWs also have a very smooth surface after epitaxial n-type Si deposition, although the nanowire tips after coating still appear to have some leftover residue still remaining on the tip. This was found to be left after the Au etch and may be Si that did not precipitate out of the catalyst during the nanowire growth or cooldown.

6.3 n-type Si Deposition on Glass Substrates

Radial n-type coating of p-type SiNWs grown on AAO coated glass substrates was also investigated. The growth of the SiNW samples was discussed in Chapter **5**. The following sections will discuss the samples, sample preparation, and the development of the n-type coating on glass substrates.

6.3.1 Substrates

Samples provided by the Illuminex Corporation consisting of ITO coated glass slides with an AAO template were obtained and p-type doped SiNWs were grown as described in detail in Chapter **5**. The main limitation of the glass substrates is the temperature. The glass substrates do not hold up above temperatures of 700°C. This limits the temperature of the n-type Si deposition to less than ~700°C.

6.3.2 Sample Preparation

Since the p-type Si nanowires are terminated with small gold nanoparticles after VLS growth, the Au tips needed to be removed to prevent the Au from diffusing throughout the sample during the higher temperature radial coating step as discussed in section **6.2.3**. The gold tips were removed by immersing the samples in a standard Au etchant solution (KI/I_2) for 3 minutes followed by 5 rinses in de-ionized water. The large number of DI rinses was carried out to ensure that all of the KI/I_2 was removed. Figure **6-21** shows an SEM plan view of the nanowires before (Figure **6-21(a)**) and after (Figure **6-21(b)**) the Au tips were removed.

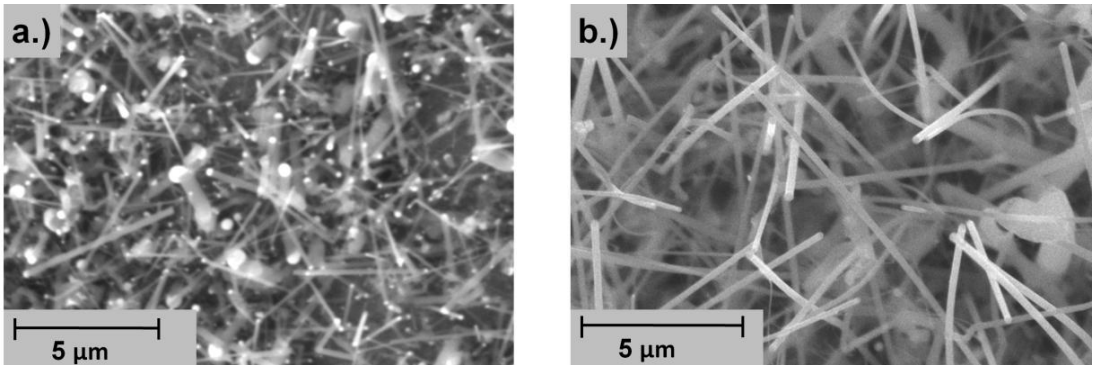


Figure **6-21**: SEM images before (a) and after (b) the Au tips were removed from the SiNWs grown on AAO coated glass substrates.

In the first set of samples, the Au etch step was followed by a short HF dip (1minute) which was used to remove the native oxide layer from the p-type Si nanowire surface prior to the n-type Si thin film deposition. Figure **6-22** shows both a low a.) and b.) high magnification cross-sectional FESEM images of the templated glass slide. The images revealed damage to the AAO membrane that was caused during sample processing. This damage allowed for n-type Si penetration down to the ITO layer. Further experiments on blank templated glass slides indicated that the BOE dip, which was done after growth of the p-type Si nanowires to remove native oxide from the nanowire surface, also etched away regions of the AAO membrane. Since the AAO membrane not only serves as a template for nanowire growth but also as a "buffer" between the ITO layer and n-type Si, the n-type Si penetration could effectively cause the photovoltaic to "short". Shorter BOE times were attempted but still yielded etching of the AAO pores.

Based on these sample preparation experiments, a final sample preparation for ITO coated glass slides with an AAO template was developed. After successful p-type SiNW growth, the samples were placed into the commercial KI/I_2 for 7 minutes followed by 5 DI rinses to ensure there is no Au etchant residue left on the samples. A quick oxide removal was performed by dipping the sample in 10:1 BOE for 10 seconds to try and minimize the etching of the AAO template.

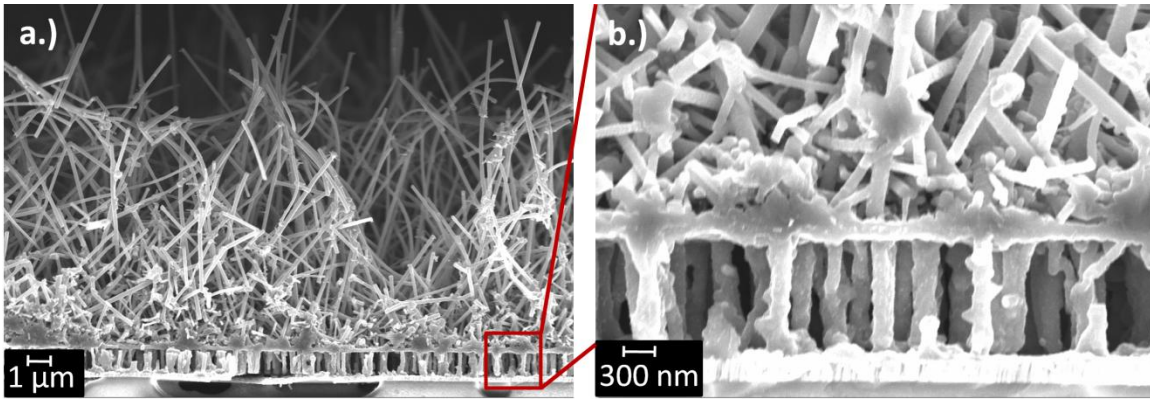


Figure **6-22**: (a) Low magnification and (b) high magnification FESEM images of sample cross-section after Au etch, HF dip and n-type Si thin film coating showing evidence of HF etching of the AAO membrane.

6.3.3 n-type Si Regrowth on Templated Glass

Samples were placed inside the LPCVD reactor for the n-type Si thin film coating, which was carried out using conditions determined from the calibrations runs described in section **6.2.1** (650^{o}C, 10 Torr total pressure, 100 sccm total gas flow, 50 sccm of 10% SiH_4 in H_2, $PH_3/SiH_4=1\times10^{-3}$). The n-type Si thin film deposition was carried out for 2 minutes for a target shell thickness of 20-40 nm. The average diameter of the p-type Si nanowire sample was 80 ± 20 nm. FESEM images of the nanowire samples after the deposition of the n-type Si shell layer are shown in Figure **6-23**. The nanowire surface has roughened after the radial n-type Si coating (Figure **6-23(a)** and in some areas, the nanowires appear to be joined together by the n-type shell coating (Figure **6-23(b)**). The average diameter of the nanowires increased to 230 ± 27 nm after deposition of the n-type Si shell layer.

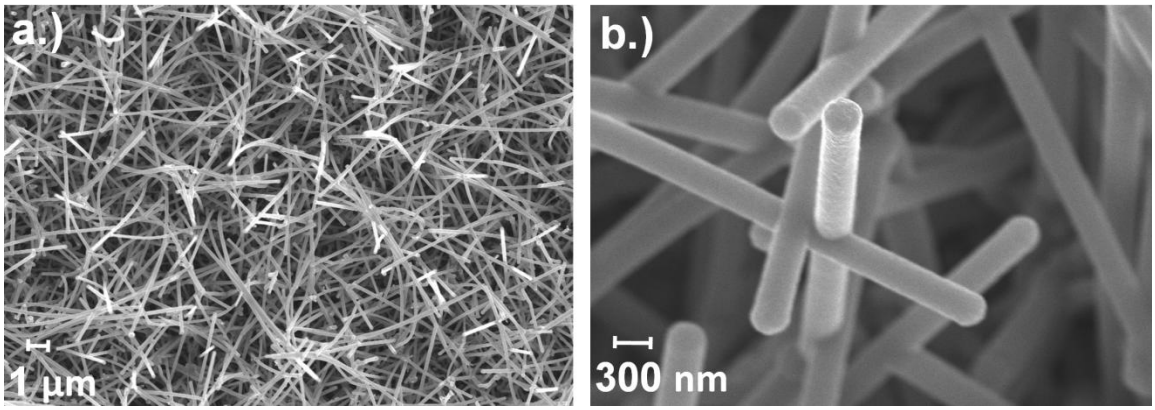


Figure **6-23**: (a) Low magnification and (b) high magnification FE-SEM images of radial p-n Si nanowires after n-type Si shell coating.

Transmission electron microscopy performed by Dr. Qi Zhang was used to characterize the structural properties of the radial p-n Si nanowires. To prepare the samples, the Si nanowires were removed from the substrate by mechanical agitation and were transferred to a TEM grid. As shown in (Figure **6-24(a)**), the thickness of the n-type Si thin film coating is relatively uniform along the length of the nanowire. The nanowires exhibit a clear core-shell structure (Figure **6-24 (b)**) consisting of a crystalline p-type Si nanowire core and a polycrystalline n-type Si shell layer. The thickness of the n-type Si shell layer is ~40 nm which is slightly larger than the target thickness of 20-30 nm. The structural properties of the nanowires are similar to those recently reported by Tian et al [1] for radial p-n Si nanowire photodiodes. The n-type Si shell layer is believed to be polycrystalline as a result of the relatively low deposition temperature that was used for these initial deposition experiments (650^{o}C). In order for epitaxial growth to be achieved, a higher n-type Si deposition temperature is needed as shown in section **6.2.4**. This poses a problem for templated samples, since the AAO membranes tend to flake off of the glass slide at higher temperatures due to differences in the thermal expansion of AAO and glass. The glass slides used as substrates melt at higher deposition temperatures (~ 800°C) so n-type Si depositions using higher temperatures were not explored with these samples.

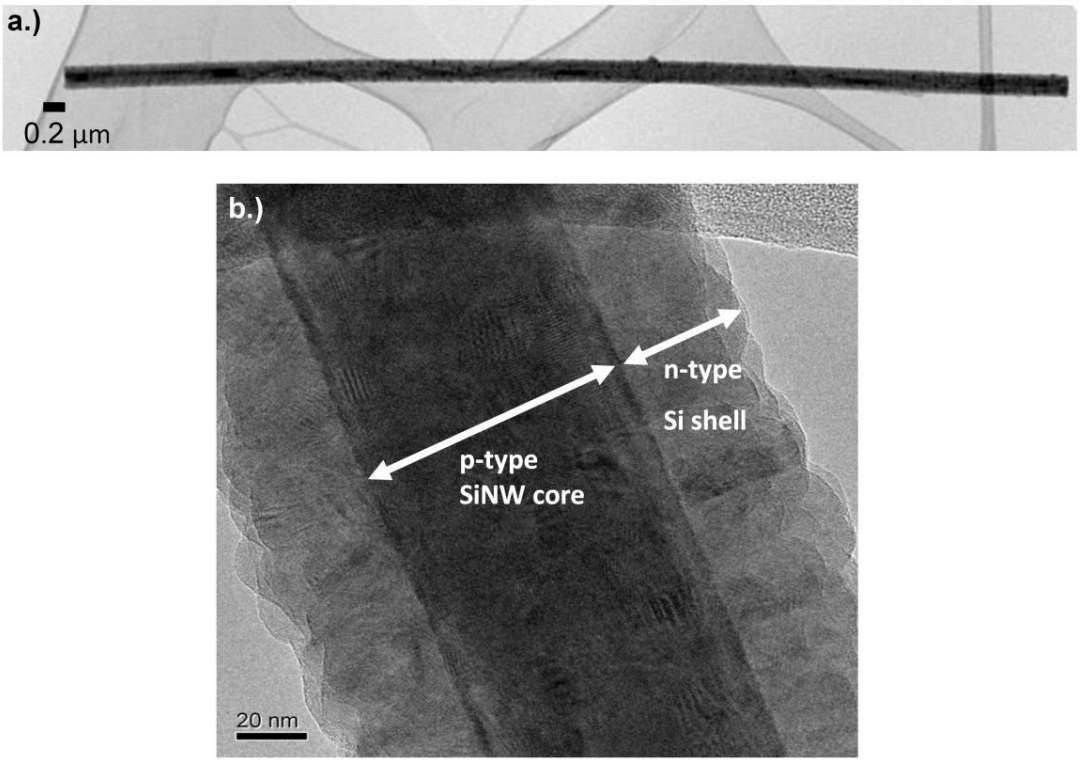


Figure **6-24**: (a) Low magnification TEM image of radial p-n Si nanowire. (b) High magnification TEM image of radial p-n Si nanowire showing crystalline p-Si core and polycrystalline n-Si shell layer.

6.4 Conclusion

Si thin film depositions were carried out using the LPCVD reactor and 10% SiH_4 as the Si precursor using a variety of different samples. Sample preparation experiments were carried out to determine the best techniques for etching Au tips and removing the oxide. It was found that the commercial Au etchant GE 8148 (KI/I_2) removed the Au tips. Larger Au tips required longer etch times. The small diameter SiNW tips "tented" due to capillary forces; this was solved by using critical point drying. Samples grown on glass exhibited an etching of the AAO membrane

during removal of the native oxide with 10:1BOE. This was minimized by using short etch times of 10 seconds.

A series of intial experiments were carried out on sapphire substrates to determine the thin film uniformity, growth rates, and resistivity of the n-type Si. The film uniformity along the length of the boat decreased with increasing temperature due to Si depletion. This was minimized by moving the samples closer to the gas inlet, decreasing the system pressure and also changing the total flow rate to 200 sccm. Once the conditions were optimized n-type doping was performed by varying the PH_3/SiH_4 ratio. The resistivity decreased as a function of increasing PH_3/SiH_4 ratios.

Using optimized growth conditions for n-type Si thin film deposition at 650, 850 and 950°C on SiNWs grown by VLS, it was found that the film changed morphology from polycrystalline at 650 and 850°C to single crystal at 950°C . The n-type Si shell was determined to be epitaxial when using a deposition temperature of 950°C. The epitaxial n-type Si shell was then deposited on both VLS grown SiNWs and etched Si pillars. On the VLS grown wires the n-type Si deposited at the nanowire tip region appears to be more defective than the rest of the conformal coatings. This could potentially be caused from the etching of the Au tips. The p-type SiNWs grown using AAO templates on ITO coated glass provided by the Illuminex Corporation were successfully n-type coated with a PH_3/SiH_4 ratio of 1×10^{-3}. TEM characterization revealed a polycrystalline coating. Due to the substrate, higher temperature depositions were not explored in this case.

6.5 References

[1] B. Z. Tian, X. L. Zheng, T. J. Kempa, Y. Fang, N. F. Yu, G. H. Yu, J. L. Huang, and C. M. Lieber, Nature **449,** 885-U8 (2007).

[2] G. S. Doerk, N. Ferralis, C. Carraro, and R. Maboudian, **18,** 5376-5381 (2008).

[3] *CRC Handbook of Chemistry and Physics 89th ed.*

[4] K.-K. Lew, (2005).

[5] *Epitaxial Silicon Technology*; *Vol.*, edited by B. J. Baliga (Academic Press. Inc., Orlando, FL, 1986).

[6] R. Burke, (2008).

[7] Henderso.Rc and R. F. Helm, Surf. Sci. **30,** 310-& (1972).

[8] D. K. Schroder, *Semiconductor Material and Device Characterization*, 3rd ed. (John Wiley & Sons, New York, 1998).

[9] M. Ohring, *The Materials Science of Thin Films*, Second ed. (Academic Press, San Diego, 2002).

Chapter 7

Thesis Summary and Future Work

7.1 Summary

Currently, single crystal solar cells are not economically viable. Polycrystalline Si solar cells are cheaper but have lower efficiencies due to charge separation and recombination at the grain boundaries. Silicon nanowire solar cells, utilitze the geometry of a radial p-n silicon nanowire array to decouple the direction of light absorption and the direction of carrier collection. This allows for a long nanowire and increased surface area in the direction of incident light, while maintaining a short collection distance, to improve carrier collection. Modeling studies have shown that a silicon nanowire array has the potential to produce efficiencies better than planar solar cells[15]. The goal of this research is to investigate the processing technology fabrication of large area radial p-n junction SiNW arrays on both Si(111) and glass substrates.

The effect of growth conditions on the growth of vertically aligned silicon nanowire arrays on Si(111) substrates was studied. Temperature was found to have little effect on the nanowire growth rate, while increased P_{SiCl4} was found to increase initially and then transition into an etching dominated regime. Based on the the gas phase thermodynamics and the balance of the Si formation/etching reactions, it was found that the SiNW growth using $SiCl_4$ is mass transport limited, similar to thin film growth from $SiCl_4$. The modeling also demonstrated the reduction of H_2 in the carrier gas also leads to a shift in the growth/etch curves. The experimental decrease in growth rate with decreasing the amount of H_2 carrier gas concentration supported the modeling data. TEM characterization has shown for varying growth conditions revealed that there is no significant change in the structural properties of the nanowire based on temperature, P_{SiCl4}

and carrier gas composition. The optimized growth conditions are a temperature of 1050°C, P_{SiCl4}=9 torr to obtain growth rates approximately 4 μm/min with 100% H_2 as the carrier gas. Trimethylboron was used for in-situ doping of the SiNW arrays. Varied TMB/$SiCl_4$ was carried out and single nanowire resistivity measurements were made. Using a 100 ppm TMB in H_2 there does not appear to be a substantial change in resistivity, however, a 0.5% TMB in H_2 cylinder was used to produce a TMB/SiH_4 of 1×10^{-1} and a resistivity of 10^{-3} Ω-cm. Based on these results it may be possible to incorporate boron into the SiNWs using TMB.

The growth of SiNW arrays on a low cost substrate such as glass was also investigated. The substrate consisted of an AAO template on ITO coated glass. A methodology was developed to contact and measure the resistance of the SiNW arrays, and nanowire resistivity was extracted from plots of array resistance versus nanowire length. The NW resistivity measured from the arrays decreased with increasing dopant/SiH_4 ratio and compared favorably with resistivity data obtained from four-point measurements of individual SiNWs grown under identical conditions. The AAO templates were found to introduce unintentional acceptors into the SiNWs during growth resulting in a resistivity in the range of 1-3 Ω-cm for nominally undoped SiNWs. successful nanowire growth on templated glass, the ITO layer that the SiNWs grow on can serve as a backside contact for solar devices. By utilizing the AAO template on the glass substrate it is possible to grow a high density array of single crystal doped silicon nanowires. The average nanowire diameter growing from the pores was 86 +/-18 nm, which is slightly less than the average pore size of 98 +/- 23 nm. Finally, nanowire growth was achieved on a more complex low cost aluminum wire. A range of growth conditions was explored to allow for better gas flow into the AAO pores to reach the Au seed layer. For optimal growth a lower system pressure of 3 torr at a growth temperature of 500°C was used in order to increase the diffusion into the pores.

Si thin film depositions were carried out using the LPCVD reactor and 10% SiH_4 as the Si precursor using a variety of different samples. Several samples were used including both VLS

grown SiNW arrays and also etched silicon pillars. Sample preparation experiments were carried out to determine the best techniques for etching Au tips and removing the oxide. It was found that the commercial Au etchant GE 8148 (KI/I_2) successfully removed the Au tips. The Au etch time scaled with increasing nanowire diameter. The small diameter SiNW tips "tented" due to surface tension and was resolved by using a critical point dryer after the Au etch and DI rinse.

A series of intial experiments were carried out on sapphire substrates to determine the thin film uniformity, growth rates, and resistivity of the n-type Si. The film uniformity along the length of the boat decreased with increasing temperature due to Si depletion at a temperature of 950°C. This was minimized by moving the samples closer to the gas inlet, decreasing the system pressure and also changing the total flow rate to 200 sccm. Once the conditions were optimized n-type doping was performed by varying the PH_3/SiH_4 ratio. The resistivity decreased as a function of increasing PH_3/SiH_4 ratios based on both four-point resistivity measurements and also Hall measurements. The silicon films were also determined to be n-type from the Hall data.

Using optimized growth conditions for temperatures of 650, 850 and 950°C, on SiNWs grown by VLS it was found the film went from polycrystalline at 650 and 850°C to single crystal at 950°C . The polycrystalline grain size was found to increase with increasing temperature. At 950 °C the n-type Si coating on the nanowire was determined to be epitaxial from the TEM characterization. The epitaxial n-type Si shell was then deposited on both VLS grown SiNWs and etched Si pillars. On the VLS grown wires the n-type Si deposited at the nanowire tip region appears to be more defective than the rest of the conformal coatings. This could potentially be caused from the etching of the Au tips.

The SiNWs grown using AAO templates on ITO coated glass provided by the Illuminex Corporation were successfully n-type coated with a PH_3/SiH_4 ratio of 1×10^{-3} at a temperature of 650°C. Samples grown on glass exhibited an etching of the AAO membrane during removal of the native oxide with 10:1BOE prior to n-type silicon deposition. This was minimized by using

short etch times of 10 seconds. TEM characterization revealed a polycrystalline coating. Due to the substrate higher temperature depositions were not explored.

7.2 Future Work

There has been little research carried out on the doping of silicon nanowires grown with $SiCl_4$. The doping studies that have been carried out have not reported on the effect of doping on the growth or electrical properties. It was observed in this study that the $SiCl_4$ was not significantly doped using 100 ppm TMB in H_2. However, using a 0.5% TMB in H_2 concentration and the lowest TMB/SiH_4 ratio of 1×10^{-1} the wires, grown at a temperature of 950°C had a resistivity on the order of 10^{-3} Ω-cm. Based on these results a TMB tank between 100 ppm and 0.5% TMB may lead to control of the nanowire resistivity at temperatures of 950°C. Another study to achieve a higher boron incorporation into the SiNWs at the higher temperatures required for growth would be the use of BCl_3. Boron trichloride could be used to achieve higher doping, which could then lead to lower resistivity in the SiNWs. Similarly it would be interesting to study the n-type doping of SiNWs grown using $SiCl_4$. There have currently been no systematic studies of doping using $SiCl_4$. To date there have been no reports of systematic doping studies using $SiCl_4$.

This research developed the processes necessary to fabricate radial p-n junction silicon nanowire arrays. The next step would be to fabricate solar cell devices using this structure. The effects of the sample preparation, such as damage induced during the etching of the Au tip, could then be studied for the effect on device properties. Likewise, silicon nanowire and shell doping, should be systematically investigated on the solar cell performance, using devices fabricated using the processes reported as a baseline. The interface quality and its effect on radial p-n junction solar cell devices could also be investigated.

7.3 References

[1] B. M. Kayes, H. A. Atwater, and N. S. Lewis, J. Appl. Phys. **97** (2005).

[2] R. S. Wagner and W. C. Ellis, Appl. Phys. Lett. **4,** 89 (1964).

[3] Y. Cui, X. F. Duan, J. T. Hu, and C. M. Lieber, J. Phys. Chem. B **104,** 5213-5216 (2000).

[4] T. J. Kempa, B. Z. Tian, D. R. Kim, J. S. Hu, X. L. Zheng, and C. M. Lieber, Nano Lett. **8,** 3456-3460 (2008).

[5] L. J. Lauhon, M. S. Gudiksen, C. L. Wang, and C. M. Lieber, Nature **420,** 57-61 (2002).

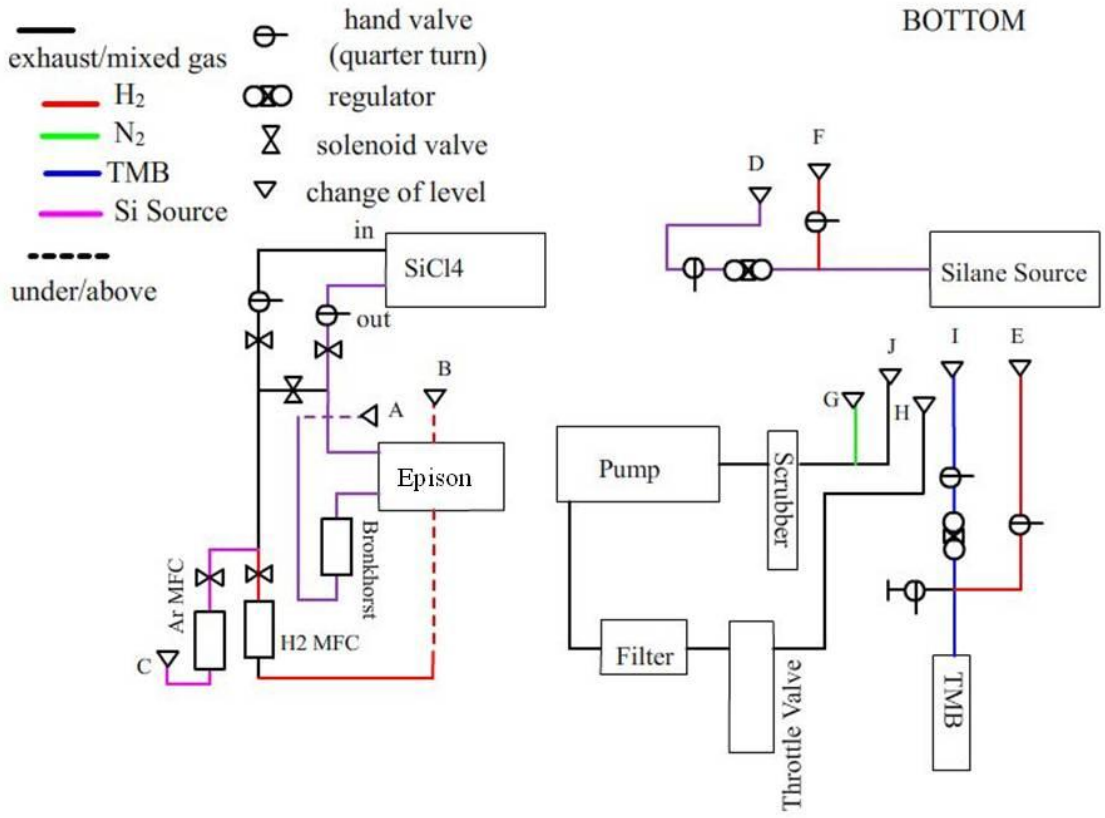
[6] B. Z. Tian, X. L. Zheng, T. J. Kempa, Y. Fang, N. F. Yu, G. H. Yu, J. L. Huang, and C. M. Lieber, Nature **449,** 885 (2007).

[7] M. D. Kelzenberg, D. B. Turner-Evans, B. M. Kayes, M. A. Filler, M. C. Putnam, N. S. Lewis, and H. A. Atwater, Nano Lett. **8,** 710-714 (2008).

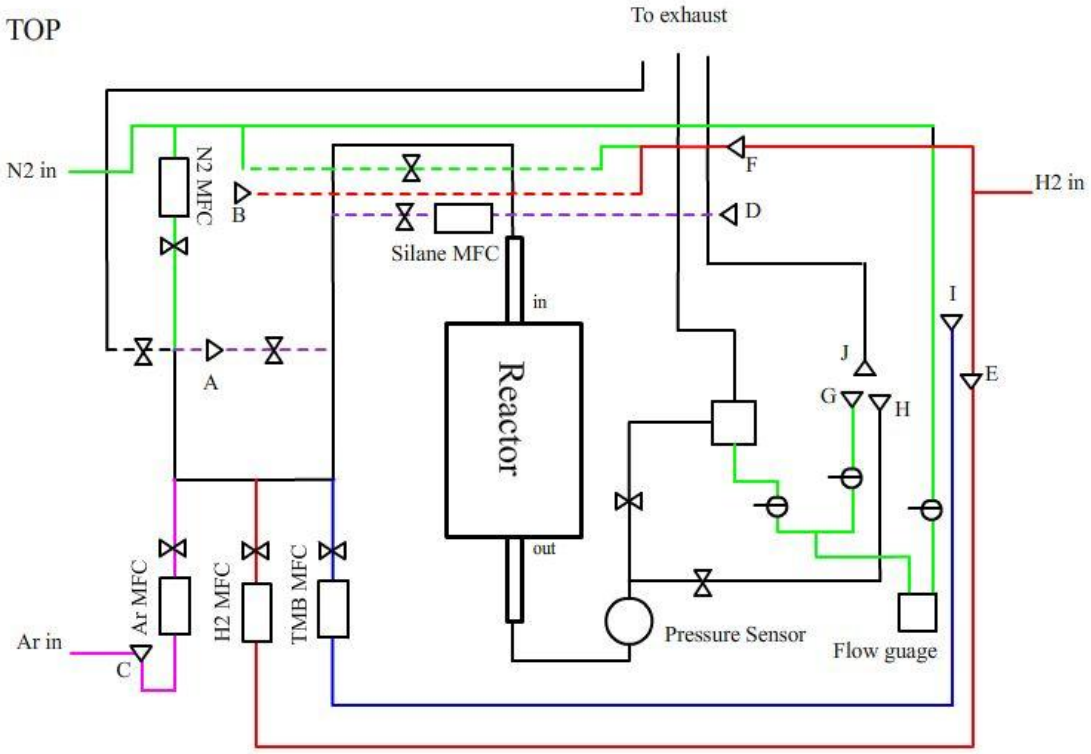
[8] E. C. Garnett and P. D. Yang, J. Am. Chem. Soc. **130,** 9224 (2008).

Appendix

Silicon Nanowire System Diagram



SiNW system diagram showing the bottom of the reactor cabinet.



SiNW system diagram showing the top of the reactor cabinet.

VITA

Sarah M. Eichfeld

Education

Ph.D. Materials Science and Engineering, 2009
The Pennsylvania State University, University Park, PA
Dissertation Topic: Synthesis and Characterization of Silicon Nanowire Arrays for Photovoltaic Applications

B.S. Materials Science and Engineering, Electronic and Photonics Option, December 2004
The Pennsylvania State University, University Park, PA

Select Publications

S.M. Dilts, A. Mohammad, K.K. Lew, J.M. Redwing, S.E. Mohney "Fabrication and electrical characterization of silicon nanowire arrays" Group-IV Semiconductor Nanostructures Symposium (MRS Proceedings Vol. 832), 2005, p 287-92
Outstanding Proceedings Ribbon Award

S.M. Eichfeld, T.T. Ho, C.M. Eichfeld, A. Cranmer, S.E. Mohney, T.S. Mayer, J.M. Redwing "Resistivity measurements of intentionally and unintentionally template-grown doped silicon nanowire arrays" Nanotechnology, 18 (31), Aug 2007

C.M.Eichfeld, C.Wood, B.Liu, **S.M.Eichfeld**, J.M. Redwing, S.E. Mohney "Selective plating for junction delineation in silicon nanowires" Nano Letters, 7 (9), Sept 2007

A.P. Goodey, **S.M.Eichfeld**, K.K. Lew, J.M. Redwing, T.E. Mallouk "Silicon nanowire array photoelectrochemical cells" Journal of the American Chemical Society, 129 (41), Oct 2007

C.Highstrete, M. Lee, A.L. Vallet, **S.M.Eichfeld**, J.M. Redwing, T.S. Mayer "Disorder dominated microwave conductance spectra of doped silicon nanowire arrays" Nano Letters, 8 (6), Jun 2008, p 1557-1561

T. T. Ho, Y. Wang, **S.M.Eichfeld**, K.K. Lew, B. Liu, S.E. Mohney, J.M. Redwing, T.S. Mayer "In-situ axially doped n-channel silicon nanowire field-effect transistors" Nano Letters, Nov 2008

S.M.Eichfeld, H. Shen, C.M. Eichfeld, S.E. Mohney, E.C. Dickey, J.M. Redwing "Thermodynamic Limitations on the growth of epitaxial Si nanowires by the VLS technique using $SiCl_4$" Journal of Crystal Growth, Manuscript in Progress