The Pennsylvania State University

The Graduate School

LOW COST INSTRUMENTATION AND INTERFACE FOR NEURAL RECORDINGS

A Thesis in

Electrical Engineering

by

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Submitted in Partial Fulfillment

of the Requirements

for the Degree of

Master of Science

May 2012

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Abstract

According to the World Health Organization (WHO), more than one billion people around the globe are affected by neurological disorders. Neurological disorders include epilepsy, migraine, and autism, and neurodegenerative disorders including Alzheimers, Parkinsons disease, multiple sclerosis, and neuropsychiatric disorders including depression and personality disorders. Neurological disorders affect people irrespective of their country of origin, country of residence, age, and sex. As the average life expectancy around the globe increases, and the population increases neurological disorders are estimated to grow multiple times their current number.

The adult human brain weighs about 3 pounds and contains some 100 billion neurons. Any dysfunctioning of these neurons could create problems and create a neurological disorder. Scientists and engineers are trying to understand the brain using various medical imaging techniques and better understand how the brain works and how any dysfunctioning can be prevented or overcome.

Over the years different forms of medical imaging have been developed to understand the complex human brain. The Electroencephalogram (EEG) is one of imaging techniques for spontaneous recording of the electrical activity from the brain. The EEG has been used widely for clinical purposes for diagnosing brain death, coma, monitoring the depth of anesthesia, localizing the regions of abnormalities in the brain. EEG is also widely used in research for cognitive and brain-state studies in psychology, neuroprosthetics, human factors, transportation safety and neuroeconomics.

Current EEG acquisition systems are bulky and expensive. This thesis fits within an effort to produce a very high performance EEG recording amplifier that will serve three overlapping efforts at the Penn State Center for Neural Engineering: to produce a low cost video-EEG system for use in the third world, to produce a low-enough cost EEG recording platform for distribution in classroom brain computer interface or another EEG related courses, and to develop flexible high performance instrumentation for ongoing neural recordings in animal studies.

A new low cost 8 channel EEG acquisition hardware has been developed which can record EEG data with high fidelity and whose component costs run less than a $100(USD) with of order 10 components. This system can be easily extended to a 16 channel or a 24 channel with just a few changes in the hardware and firmware design. My work has involved the development of the firmware code for the hardware. Different varieties of tests have been conducted to compare the performance of the prototype system with the standard clinical grade system and demonstrated its applicability using the well-known P300 paradigm for a Brain Computer Interface application. The above results prove that the prototype amplifier can serve as a low cost teaching tool and research tool.

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Acknowledgments

I am greatly indebted to my thesis adviser Dr. Gluckman and Dr. Insoo Kim for their extended support, motivation, and patience. The success of this work can be attributed to their deep expertise in electrical engineering, physics, bio-instrumentation, and human physiology. I am thankful to my fellow lab members Andrew Geronimo, Seneca Harberger, Stephen Van Wert, and all other CNE members who have helped me in one way or the other by serving as research subjects, helping in experimental setup to name a few. I would also like to thank Dr. Steven Schiff, Dr. Steven Weinstein, Dr. Kenneth Jenkins, and Dr. Julio Urbina for their great feedback on the thesis and the experimental recordings. Last, but not the least I am eternally obligated to my family for being a continuous source of motivation.

Dedication

To my family.

Chapter 1

Introduction

Studies conducted by physician Richard Caton, in 1875 led to the discovery of the electroencephalogram. In this study he recorded the electrical activity from exposed animal brains. This study was followed by further investigation by Danilevskys in 1876, and Beck in 1890 which produced results consistent with those of Caton. Almost 50 years later German psychiatrist Hans Berger recorded the first ever human EEG from the scalp.[1, 2, 5, 4] Ever since EEG has been used widely in various areas of studies and clinical diagnosis. The amplitude of the EEG ranges from 10 - 100 μV when measured on the scalp, and about 0.1 - 2 mV when measured on the surface of the brain. The bandwidth of the EEG signal measured on the scalp is limited due to the low pass filter effects of the scalp tissue to 0 - 30 Hz frequency range while those measured on the surface of the brain have useful frequencies in the 0 - 10 kHz frequency range with reports of useful high frequency events, and oscillations in the 800 Hz - to a few kHz. [9, 10]. EEG monitoring devices are widely used in hospitals including Intensive Care Units (ICU), for monitoring the brain activity of the patient, monitoring dose of anesthesia, sleep studies, diagnosis of coma and brain death. Their use in research includes neuroprosthetics research, cognitive and brain state studies in psychology, sleep studies, human factors, transportation safety and neuroeconomics.

1.1 Motivation

This thesis fits within an effort to produce a very high performance EEG recording amplifier that will serve three overlapping efforts at the Penn State Center for Neural Engineering: (1) to

produce a low cost video-EEG monitoring system for use in developing countries, (2) to produce a low-enough cost EEG recording platform for distribution in classroom brain computer interface or another EEG related courses, and (3) to develop flexible high performance instrumentation for ongoing neural recordings in animal studies, and other EEG research studies at CNE and across the Penn State Campus. The prototype hardware system design included the requirements of low cost, low component count, ease of programming and interfacing with standard computers and human compatibility/safety.

(1) Low Cost video-EEG monitoring: Developing nations have limited resources and lack high performing medical instruments. In addition they have widespread poverty and limited people with health insurance coverage adequate enough to pay their medical bills. Intensive care costs are even more expensive. This work is an ongoing effort to produce a very low cost 24 channel, video EEG monitoring system for use in developing countries. This system would run on a low cost netbook PC's.

(2) Low Cost EEG/BCI education: For the past three years at Penn State, Dr. Gluckman has offered an introductory course on non-invasive BCIs, and found that one of the significant limitations of the course was that it utilized a highly limited number of commercial, clinical-grade EEG amplifiers which cost greater than $ 25k. The costs limited the number of available recording platforms, which in turn led to significantly limited access for the students to the hardware. This limited access contributed to reluctance by students to fully investigate the potential of the hardware. In addition, it significantly restricted the students' ability to creatively develop their own interfaces and projects outside the commercially provided programming environment.

The skills for implementing and improving BCIs range from the basics of electronics and biopotential recordings, to the implementation of off-line and real-time signal processing, to the cognitive and human factors considerations in making a human-machine interface. Indeed, the interdisciplinary nature of this work often leads experts in one field or another to neglect the complexity of the challenges of the others. Therefore, it is of great educational benefit to use BCI as a platform for an integrated introduction to these topics. Additionally, the tools used in BCI overlap heavily with those used for cognitive and brain-state studies in psychology, human factors, transportation safety and neuroeconomics. The objectives was to design an eight channel acquisition amplifier for high performance EEG recording that could be readily distributed to each student, would be readily interfaced to a computer through many different computational

platforms, and would provide an educational platform for teaching both the hardware design elements as well as be exceedingly easy to use.

(3) High performance EEG and biopotential recording tool: Apart from clinical and education benefits, EEG is also being used by researchers in the field of psychology, human factors, transportation safety and neuroeconomics. At the Penn State Center for Neural Engineering two investigators Dr. Gluckman and Dr. Schiff in collaboration with other affiliates from Penn State University Park and Hershey campus have been studying neural recordings for predicting epileptic seizures in animals and humans. In more recent work they have also been used EEG recordings for predicting state of vigilance which could help in better prediction of seizures and also aid in driver safety. The prototype amplifier is targeted to replace most of the existing hardware acquisition circuitry in his laboratory. Across campus, investigators in Department of Psychology, Kinesiology, and the Penn State Social, Life, and Engineering Sciences Imaging Center frequently use EEG for various research studies. The prototype hardware developed can replace all low density EEG acquisition systems used at Penn State.

1.2 Related Work

There has been some related work which has been conducted over the years to produce a low cost EEG/ biosignal amplifier both in academic settings and in industry. Most of this work has been conducted in industry and is mainly targeted towards the gaming community. Some of these include work by Neurosky [7], Emotiv[6], and the open EEG project. Most of this work is deficient and does not meet the basic requirements for EEG acquisition. The most popular among these is the open EEG project [8] which provides just 2 input analog channels for $200-400 with 10 bit ADC resolution. To record EEG signal correctly a minimum resolution of 24 bit ADC is ideally required, to ensure the minimum signal recorded by an ADC is lower than the minimum value of the EEG signal. For a 24 bit ADC, with a 2.4 V reference voltage the minimum resolution would be 0.28 μV, which would be well within the measurable EEG range. Also, for most research purposes and clinical diagnosis, the EEG hardware must provide at least 8 input analog channels.

Neurosky markets its EEG acquisition device for a mere $100, but it provides only one fixed input channel. Emotiv headset provides fixed 14 input analog channels which costs around

$299 and another $500 for software. For research purposed it is important to have variable electrode positions. The need for development of a low-cost EEG acquisition is warranted.

1.3 Prototype

A prototype amplifier has been developed, which is a new low cost 8 channel EEG acquisition hardware which can record EEG data with high fidelity and whose component costs run less than a $100 (USD) with of order 10 components. The development of this system was enabled by the production of a commercially available biopotential amplifier (ADS1298, Texas Instruments, Inc.) [11] that forms 8 channels of preamplifier's and 24-bit continuous-time delta-sigma analog-to-digital converters (CT$\Delta\Sigma$ ADC) with digital communication interfaces and other peripheral circuits. The key advantage of the CT$\Delta\Sigma$ ADC in this architecture is that ideally they preclude the need for anti-alias filtering prior to digitization [12, 13, 14]. This system can be easily extended to a 16 channel or a 24 channel system by using multiple ADS1298 chips and with a few changes in the hardware and firmware design. Fig 1.1, 1.2, and 1.3 show the pictures of the 8 channel, 16 channel, and 24 channel prototype boards. Standard gold-plated cup EEG electrodes common to other systems were utilized which plug into the prototype acquisition hardware either through standard touch-free safety plugs, although a less-costly model is to use standard DB-9 or DB-25 type plugs. One example of the connection using touch-free plugs is shown in Fig 1.4.

Figure. 1.5 shows a real-time human EEG recording using the prototype amplifier. The

Figure 1.1: Picture of an 8 channel prototype, compared with size of a standard US quarter.

complete EEG recording system architecture is illustrated in Figure. 1.6. The acquisition hardware, (Figure. 1.6.) comprises of three main components: an analog front-end (ADS1298, Texas

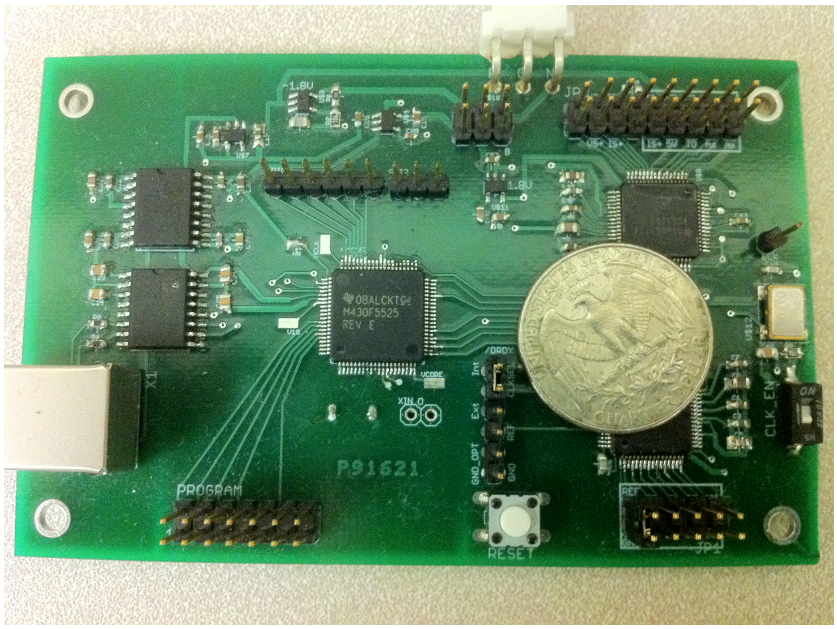

Figure 1.2: Picture of a 16 channel prototype, compared with size of a standard US quarter.

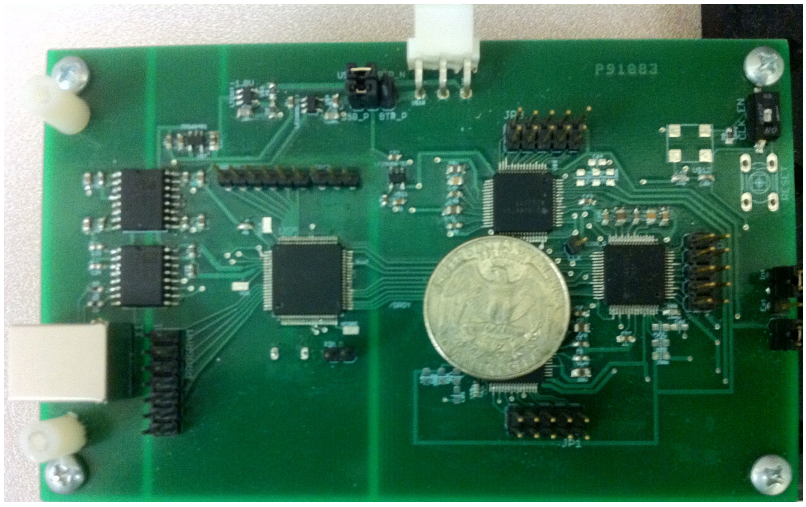

Figure 1.3: Picture of a 24 channel prototype, compared with size of a standard US quarter.

Instruments, Inc.), a microcontroller (MSP430F5525, Texas Instruments, Inc.), and isolation circuitry for USB and power (ADuM4160 and ADuM5000, Analog Devices, Inc.). The prototype hardware is recognized as a Virtual COM-port device on the PC, which can be easily accessed from within a variety of operating systems, such as Windows, Linux, and Mac OS, and software packages including MATLAB/Simulink, LabVIEW and user-written programs in C/C++.

My work has involved the development of the firmware code for the MSP430 interface with

Figure 1.4: Picture showing top view of the 24 channel prototype connected using touch-free plugs.

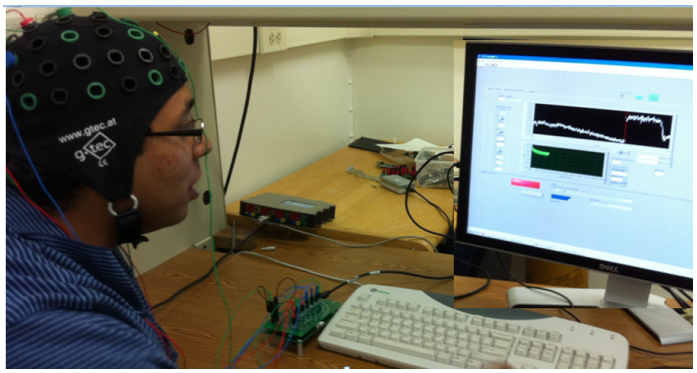

Figure 1.5: Overview of the acquisition system. Electrodes on the scalp connect to the low-cost EEG acquisition hardware, which provides a continuous stream of digital data to the computer.

the ADS1298, and the computer. Various tests have been conducted to compare the performance of the prototype with the standard clinical grade system and to validate the recordings. Acquisition software was written in MATLAB/Simulink environment. Care was taken while writing the acquisition software to avoid any sample drops and an internal counter on the microcontroller was created which detects any loss of data samples. Further human tests in form of brain computer interface recordings were conducted using the well established P300 paradigm.

This thesis is divided into five additional chapters. Chapter 2 gives an overview to the origin of bioelectric recordings, origin of biopotentials, introduction to EEG, the challenges associated with measuring EEG, and its applications with a focus on brain computer interfaces. Chapter 3 covers the hardware design, and describes the complete hardware design of the system

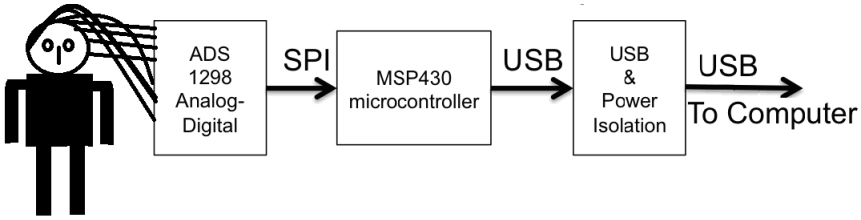

Figure 1.6: Overall architecture of the acquisition hardware. The main pieces involved are the TI-ADS1298 biopotential front-end digitizer, a low-cost microcontroller to program the front-end and transmit the data to computer, and a USB and Power isolation stage.

and lays down the framework for firmware design. Chapter 4 covers the firmware design, the interface between the PC, MSP430, and the ADS1298 and also includes code snippets. Chapter 5 covers the system validation results and chapter 6 defines future work and focuses on the possible future extensions of this work.

Chapter 2

Interfacing with the brain

Electrical engineers generally have a good insight about bio-instrumentation amplifier design but sometimes lack the knowledge of anatomy and physiology. It is important to understand the origin of biopotentials at the cellular level to interface with the brain to help solve biological problems. This chapter hence will start off with discussion about the origin of biopotentials at the cellular level and then will lead into detailed discussion about electroencephalogram, challenges and the applications where they are used, with a focus on brain computer interfaces as an application.

2.1 Biology behind neural signals

Bio-electric signals are produced as a result of electrochemical activity of excitable cells which are components of nervous, muscular and the glandular tissue. The cell membrane is essentially a very thin lipoprotein complex which allows passage to only some ions. The membrane essentially allows intracellular protein and other organic anions (A^-) to flow . At rest the cellular membrane is only slightly permeable to Sodium ions (Na^+) and freely permeable to potassium ions (K^+) and Chlorine ions (Cl^-). The ion concentration difference across membrane creates a diffusion gradient which causes ions to flow from higher concentration to lower concentration, creating an electric field that opposes this flow. This process continues until equilibrium is reached. The membrane potential at equilibrium is called the resting membrane potential. The resting membrane potential is given by the following equation which was first developed by Goldman in 1943 and later modified by Hodgkin and Katz in 1949.

$$E = \frac{RT}{F} \ln \left(\frac{P_K[K]_{\text{out}} + P_{Na}[Na]_{\text{out}} + P_{Cl}[Cl]_{\text{in}}}{P_K[K]_{\text{in}} + P_{Na}[Na]_{\text{in}} + P_{Cl}[Cl]_{\text{out}}} \right)$$

where E = The membrane potential (in Volts, equivalent to joules per coulomb)

P_{ion} = the permeability for that ion (in meters per second)

$[ion]_{out}$ = the extracellular concentration of that ion (in moles per cubic meter)

$[ion]_{in}$ = the intracellular concentration of that ion (in moles per cubic meter)

R = The ideal gas constant (joules per Kelvin per mole)

T = The temperature in Kelvins

F = Faraday's constant (Coulombs per mole)

To maintain a steady state ionic imbalance between the internal and external areas of the cell a continuous transport of ions is required. One prominent example of the active transport mechanism is the *Sodium Potassium Pump* which actively moves Na^+ out of the cell and the K^+ inside the cell in a 3 Na^+ : 2 K^+ ratio. The current associated to this sodium potassium current is an outward current which makes the cell more negative in charge. The energy for this pump is provided by cellular energy from the adenosine triphosphate(ATP) which is produced by mitochondria in the cell. To sum up the factors which influence the flow of ions across the membrane include (i) Diffusion Gradients, (ii) Inward Electric field, (iii) The membrane structure (availability of pores), and (iv) The Sodium Potassium Pump i.e. the active transport of ions against an established electrochemical gradient.

When a stimulus applied to the cell produces a rapid increase in the membrane potential which increases at a constant velocity, the cell is said to be in a depolarized state and this results in change the permeability to the Na^+ ions which rush into the cell and make the cell more positive in charge. Hence making inside of the membrane more positive. The incoming positive Na^+ ions cause the K^+ ions to flow out of the cell and increasing the membrane potential towards the Na Nernst Potential. As the cell reaches the Na Nernst membrane potential the Na^+ channels get inactivated and the Na^+ ions stop flowing into the cell and K^+ ions continue to flow out hence reducing the membrane potential towards the resting potential. As this happens the membrane potential reduces below the membrane resting potential which is known as hyper-polarization. After some time Na^+ and K^+ pump maintains ionic concentration gradient and Na^+ is pumped out of cell and K^+ is pumped in. Figure 2.1 shows the stages of a neuron when a stimulus is

applied at resting potential and an action potential is produced. [10, 9]

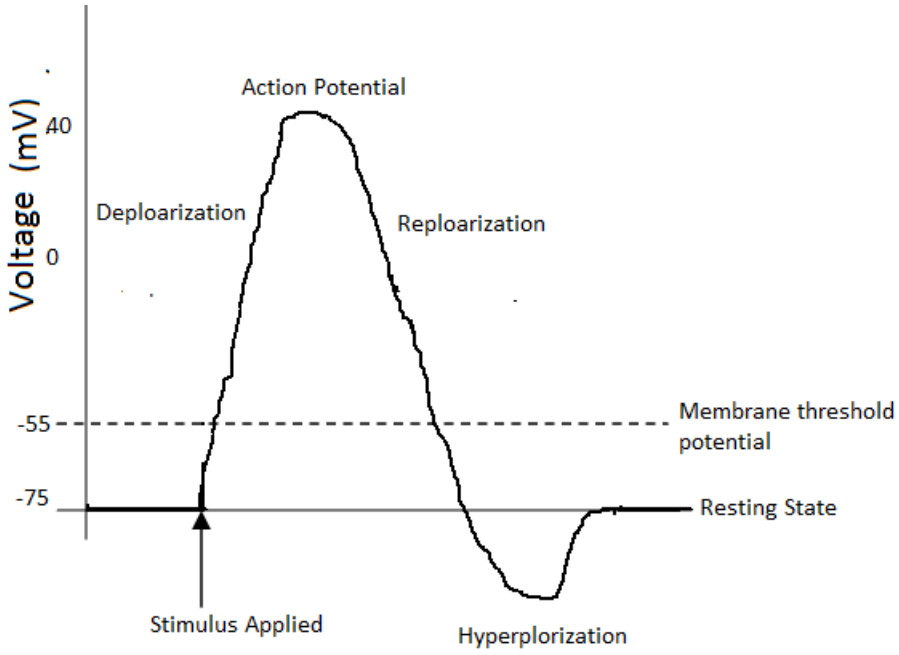

Figure 2.1: Figure shows the stage of a neuron when a stimulus is applied at resting potential and an action potential is produced.

2.1.1 Anatomy of the Human Brain

The human brain is the most important of the human nervous system. It monitors, senses, and regulates body operations. The brain consists of four main divisions:

1. **Brain Stem:** It is made up of the medulla oblongata, hind brain, and the midbrain. It is responsible for regulating the heartbeat, circulation of blood, respiration and other automatic functions which do not need active brain processing.

2. **Cerebellum:** It is called the little brain. It is an important part of the brain which is important in motor learning and movement. It helps maintain body balance and posture. It significantly impacts coordination when it is damaged.

3. **Limbic System:** The limbic system is called the emotional brain. It is involved in emotion, learning, motivation, and memory. It contains the thalamus, hypothalamus, amygdala, and the hippocampus.

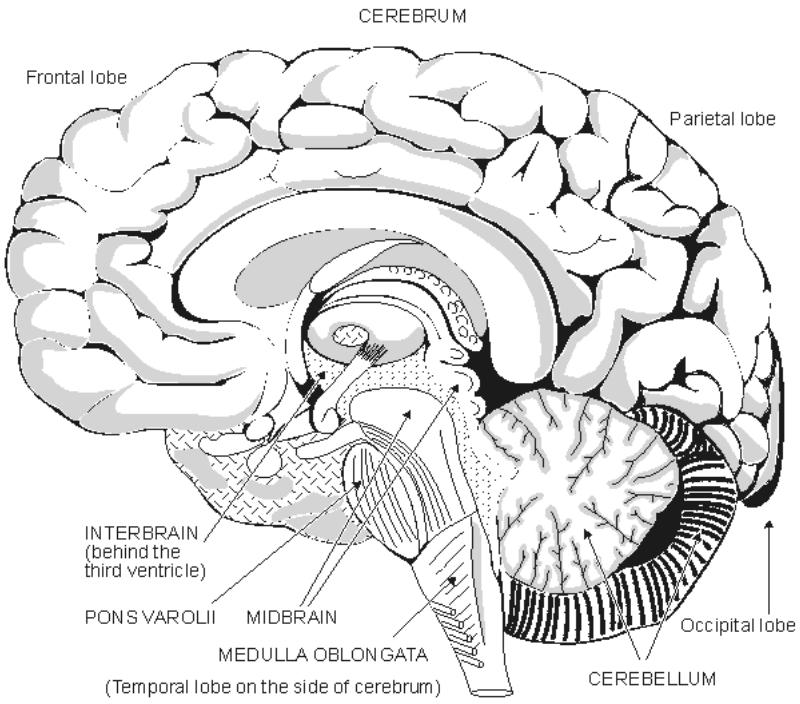

Figure 2.2: The anatomy of the brain: This figure shows the cerebrum, the four lobes namely, frontal, parietal, temporal, and occipital lobe. From J.Malamivuo and R. Plonsey, Bioelectromagnetism, Principles and Applications of Bioelectric and Biomagnetic Fields, Oxford University Press 1995

4. **Cerebral Cortex:** The cerebral cortex makes up 80% of the human brain. It enables abstract and symbolic thought. It is divided into hemispheres and allows communication between different parts of the brain. The left part of the brain controls the right part and vice-a-versa. The left hemisphere is responsible for language, logic, and motor behavior while the right side is used in recognition of faces, places, sound, and music. The cerebral cortex is divided into four different lobes.

   (a) Frontal Lobe: It is the largest lobe of the four and aids in movement planning, abstract thinking, and problem solving.

   (b) Temporal Lobe: The temporal lobe is responsible for hearing, language, and memory.

   (c) Occipital Lobe: It is responsible for vision.

   (d) Parietal Lobe: It is responsible for perception of stimuli like touch, pressure, temperature, and pain.

2.1.2 Electroencephalogram

The electroencephalogram (EEG) is the spontaneous recording of the electrical activity from the brain. The normal EEG is record from the human scalp and is a superposition of the potential of individual neurons. The EEG along the scalp usually measures in the range of 10μV-100μV and is band-limited in the frequency range 1Hz-30Hz. Electrical activity recorded on the exposed cortex is called electrocorticogram and is usually measured in mV range. The human EEG was first recorded by German neurologist Hans Berger in 1924. To measure the EEG the standard international 10-20 system is used for placing scalp electrodes. [10, 9]

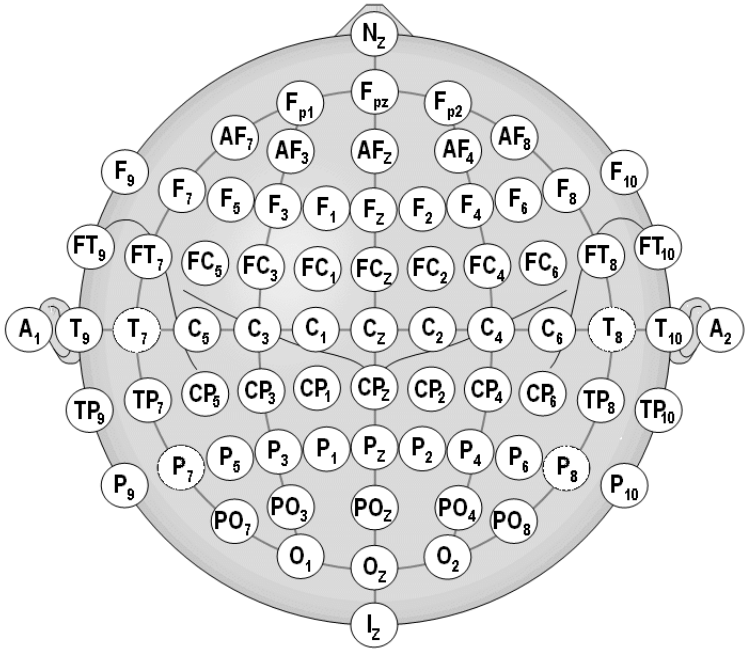

Figure 2.3: The map for recording EEG based on the international 10-20 system. Modified from J.Malamivuo and R. Plonsey, Bioelectromagnetism, Principles and Applications of Bioelectric and Biomagnetic Fields, Oxford University Press 1995

This system has been developed to best relate to the location of the underlying cerebral cortex. It was named the 10-20 system because the adjacent electrodes differ by either 10% or 20% of the total front and back or the right and left distance of the skull. The sites are named according to their corresponding cerebral lobe F(Frontal), T(Temporal), C(Central), P(Parietal), and O(Occipital). The central lobe constitutes each of the cerebral hemispheres and lies in the depth of central sulcus. "Z" refers to an electrode placed on the midline and numbers increase in an even fashion on the right hemispheres (2,4,6,8) and odd numbers (1,3,5,7) refer to those on

the left hemisphere. To find the midline the nasion which is the point between the forehead and the nose is measured and next the inion, the lowest point of the skull from the back of the head. The EEG exhibits some basic types of waves which are characterized by their frequency bands.

Alpha Waves: These waves were first to be discovered and hence are called the alpha waves. These waves are generally noticed in a resting state and range in the 8Hz-12Hz frequency zone.

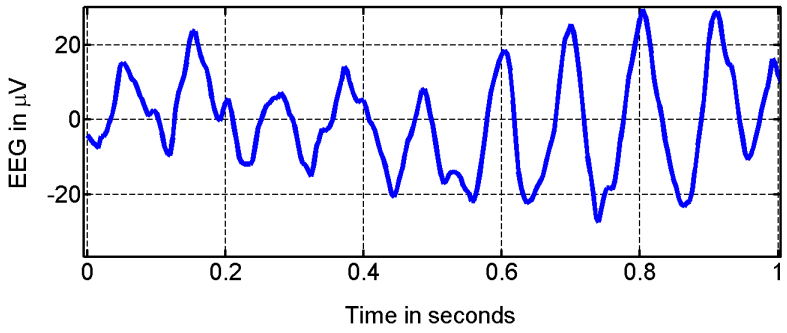

Figure 2.4: Alpha waves for 1 second window, grid spacing is 20μV

Beta Waves: Beta waves are generally observed during intense mental activity, thinking, and intense concentration. They are observed in the 12Hz-30Hz band.

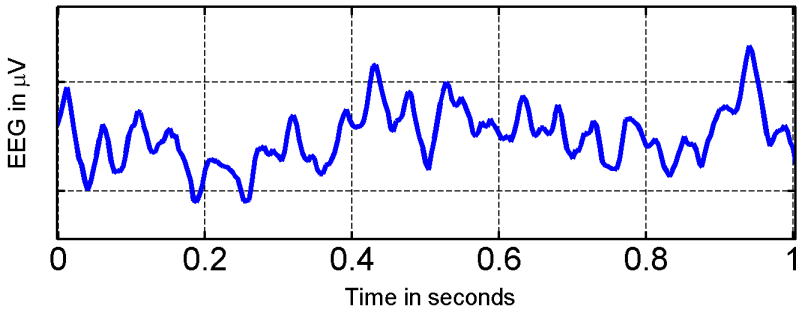

Figure 2.5: Beta waves for 1 second window, grid spacing is 20μV

Theta Waves: Theta waves are observed mostly in young children. In older children, and adults these waves are observed during meditative, drowsy, and sleep states. It is concentrated in the 4Hz-8Hz frequency band.

Delta Waves: Delta waves are high amplitude brain waves which are observed in deep sleep

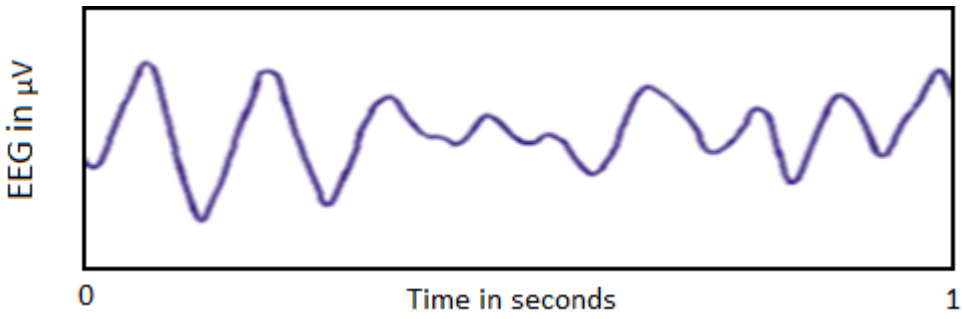

Figure 2.6: Theta waves for 1 second window.

states. Any disruption in delta activity either increase or decrease have been known to be associated with serious mental health disorders. They are observed in the frequency range between 0Hz-4Hz band.

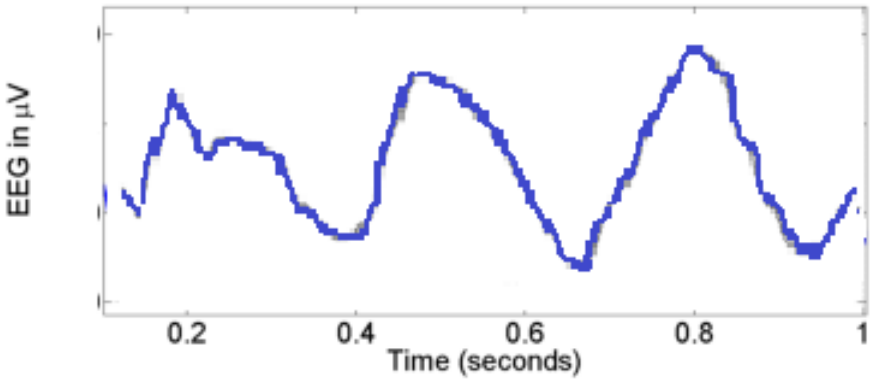

Figure 2.7: Delta waves for 1 second window 100 μVpp

2.2 Instrumentation

Biological signals including the EEG are measured as potentials, voltages. These signals are weak, contaminated by noise, and interference signals. To measure biological EEG signals, specialized amplifiers are required which can record the EEG with high fidelity. This section will discuss in detail the design factors, challenges and requirements for recording biological EEG signals, and will end with a brief discussion on various applications of the EEG signal.

2.2.1 Design Factors

In the design of a medical instrumentation system the following factors need to be kept in mind.

The input signal input range, bandwidth, and noise play a key role in the design of an instrumentation amplifier. EEG has range of 10μ V to 100 μV. The amplitude, the frequency band, and the noise levels of the signal play a key role in deciding the components of the instrumentation system. For EEG signals, an ADC with a resolution high enough is required to accurately measure EEG signal in the range from 10μ V to 100 μV and frequency band of 0.1 Hz to 100Hz. A part from these basic signal factors, environmental factors such as temperature and humidity put restrictions on the devices to be used. The areas power supply range and frequency either 50Hz or 60 Hz introduces variable noise at the power line frequency, which needs to be filtered out either in post-processing or by hardware filtering.

2.2.2 Challenges

Recording EEG signal poses various challenges, and requirements. These requirements must be met in order to record the EEG data with high fidelity. This subsection will give an introduction on the challenges of measuring EEG, and the requirements it poses on the hardware design.[10]

Input skin impedance: The human skin acts as a source of impedance in measurement of the EEG signal. Since the EEG signal is a weak signal to measure the signal on the scalp, impedance must be monitored and lowered. First the skin must be cleaned with rubbing alcohol, prepared with EEG skin preparation gel to reduce the electrode skin contact impedance. The skin impedance ranges from 10k-100kΩ and it must be reduced to around$<$5kΩ for recording EEG signals with high fidelity.

Common-mode signal: EEG signals are weak signals and are significantly affected by common-mode signals and have non-negligible offset. This poses challenges in measuring the EEG signal. An input impedance mismatch between electrodes contributes further to a high common mode signal. For this reason the amplifier design requires a high common mode rejection ratio. In order to achieve this, an instrumentation amplifier with high common-mode rejection ratio could be used, along with the use of a right-leg drive circuit.

Power Line Interference: The electrical power supply produces a great deal of interference at the power line frequency which is either 50Hz or 60Hz depending on region. With

good quality electrical connections and active shielding this artifact can be highly minimized. Computationally, this interference can be overcome by using a 60Hz or 50Hz notch filter.

Transients: Electrical transients can occur to electro surgical units, stimulation current artifact, motion artifacts, and switching power. Such transients can cause interference in the input signal and cause the amplifier to saturate. To avoid this voltage limiting devices need to be used.

Muscle Artifact: Muscle movements produce electromyogram (EMG) signal whose amplitude ranges from 100μV to 1000μV and most of the power is concentrated in the 50Hz-150Hz band. This signal significantly interferes with the EEG signal. However, given the frequency band a simple low pass filter at 30Hz can help get rid of most of this muscle artifact. Digital signal processing can be done either on software or hardware to remove these artifacts. Real time digital signal processing in environments like Simulink and LabVIEW can be easily done in software to get rid of these artifacts and get a relatively clean signal.

2.2.3 Requirements

Based on the design factors, and challenges in measuring EEG, the following are the basic requirements in the design of an instrumentation amplifier. [10]

High Gain: The amplifier must have a high gain to amplify the weak input signal and so that they are not affected by the internal noise of the amplifier. The amplifiers with higher gain would be more sensitive to small changes in the input signal.

High Input Impedance: The amplifier must have high input impedance so that they provide minimum loading of the EEG signal. The electrical loading can result in distortions, hence amplifiers must have a high input impedance generally greater than 10M Ω.

Low Input Bias Current: Op-amps have some amount of current which flows through their input connections in order for the input transistors to be properly biased. But this current flow should be limited for human safety and should be less than a few nA.

Wide Input Common Mode Range: Input common mode range is the average voltage at the inverting and non-inverting input pins. The amplifier must have a wide input common mode range so that it can accept the input EEG signal without affecting the input. The input common mode range must be rail to rail.

Common Mode Rejection Ratio (CMRR): It is the ability of an amplifier to reject

common gain and increase the differential signal. The higher the CMRR the lower is common mode noise.

Low Noise: Every electronic amplifier has some internal noise. These noise levels should be < 10 nV). Internal noise occurs due to thermal noise and flicker noise.

Input and Output Resistance: The amplifier circuits should not load external circuits (large input resistance) and should be efficient at driving external inputs with small voltage loss and hence have low output resistance)

Input Offset Voltage: Offset voltage should be as less as possible to avoid saturation of input signals. Offset voltage can be reduced by a number of methods which include nulling by adding an external nulling pot to the terminals which increases the emitter current through one of the large input transistors and lowers it through another. This is adjusted until offset voltage is set to zeros.

2.2.4 Functional Blocks

The block diagram in Figure 2.8 shows the basic pieces which need to be present in acquisition hardware. [10] At the minimum the following should be present in a bio-acquisition system :

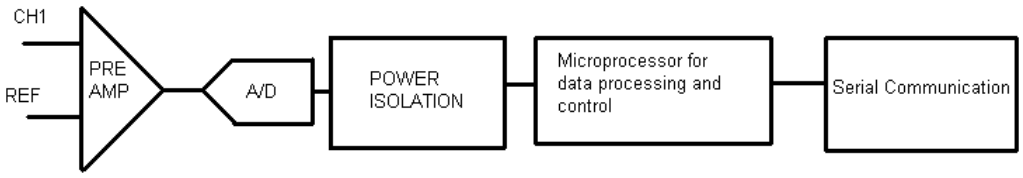

Figure 2.8: A modern data general instrumentation system is shown which contains pre-amplifiers, analog to digital converters, data processing, serial communication, and isolation circuitry

Preamplifiers: Amplifiers are required to increase the amplitude of the input analog signal and provide high input impedance to provide minimum overloading of the signal being measured. They must also have high rejection to the signal common to both the inputs of an amplifier, i.e. a high common mode rejection ratio (CMRR). For this purpose most commonly utilized circuitry is the instrumentation amplifier.

Analog-Digital Converters: Analog-digital converters are used to convert an analog signal into a digital bitstream. Analog signals are more susceptible to noise and need to be

digitized. Typically the input is sampled regularly at specific intervals of time T_s and this rate $1/T_s = F_s$ is called the sampling frequency. In a real-time, modern day instrumentation system must provide a programmable acquisition rate. These programmable acquisition rate ADCs need variable anti-aliasing filters. Anti-aliasing filters are expensive and one is required for each analog input. Aliasing will occur for a signal whose highest frequency component F is greater than one half of the sampling frequency F_s and the this higher signal frequency component cannot be distinguished from a lower frequency component which will be at $|F - nF_s|$ where n, is any integer.

Processing data : To process control the flow of digital conversion data produced by the ADC, additional digital circuitry. A control application needs to be developed to send, use, and store the digital bitstream. Most commonly microprocessors, microcontrollers, digital signal processors, and field programmable gate arrays are employed for these purposes.

Serial Communication : To process and visualize the digital data it is important to send this data to a PC, where this data can be easily analyzed and visualized. For this purpose quite often RS232, RS485 communication are used. Nowadays, most laptop computers, and netbook PC's lack these RS232 and RS485 ports which are being replaced by wired universal serial bus (USB), and wireless Bluetooth.

Isolation: Any electric current from the input terminals of a biopotential amplifier can result in an electric shock to the subject. To avoid this problem, the amplifier must have power isolation circuitry, so that the current through the electrode can be kept at safe levels and any artifact generated by the current could be minimized. Generally the isolation circuitry consists of three different isolations, the isolation of the digital supply, the analog power supply and digital data bit stream.

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2.2.5 Applications

EEG is one of the earliest and most widely used forms of medical imaging techniques. [10, 9] EEG has better temporal resolution in milliseconds which is much better than its counterparts the MRI and the CT scan. EEG is measured over the scalp and is non-invasive. EEG has been used for various interdisciplinary studies. Some of the uses of EEG are mentioned below:

Clinical Settings : EEG is widely used in hospitals and clinical settings. Some of these include, monitoring the depth of anesthesia, diagnosis of brain death and coma. They are also

used for intensive care patient monitoring, localization of seizures, epilepsy monitoring, diagnosis of other serious neurological disorders.

Research Use: Apart from use of EEG in clinical and hospital settings. EEG is widely used across different disciplines for research use. In research EEG studies are carried out on humans as well as rodent animals, monkeys, and other animals.

Biomedical Engineering/ Neural Engineering Research: In areas of biomedical/ neural engineering, EEG is used widely for research in seizure prediction algorithm development, feedback systems for prosthesis research. Most work in seizure prediction involves animal studies using epileptic rats. At the Center for Neural Engineering facility chronic video EEG monitoring are carried out for development of a novel seizure predictor. EEG studies can have various applications in rehabilitation devices, telepathy, and driver safety.

Psychology Research: EEG is widely used for various brain state studies in the field of psychology. These studies include study of sleep disorders, human developmental studies, cognitive studies, and human factors. EEG is also used for studying various mental health disorders including depression, bipolar disorders and other diseases.

Neuroeconomics: EEG is also used to study human decision making. It studies how neuroscience and human psychology research of risk, and decision making can be applied for developing models of economics. This research is mostly limited to academic settings in contrast to neuromarketing.

Neuromarketing: It is newly developed research area which is widely being used for marketing purposes in the industry. EEG is used for studying the brain response, to understand consumers like and dislikes. Big companies including Google and Pepsi use neuromarketing to measure consumer thoughts about their advertisements and products.

2.3 Brain Computer Interfaces

Many people with severe motor disabilities have disruption in the communication pathway between the brain targeted muscles. Some of these patients are totally locked-in and cannot move any part of their body. Over the past three decades many studies have demonstrated that brain computer interfaces(BCIs) utilizing EEG recordings as way of developing an alternative output communication pathway from brain. A brain computer interface (BCI), aims at restoring this

communication pathway to assist/augment human motor functions. [17, 20, 16, 19, 18, 21] Brain computer interfaces have been developed based on observations of the major EEG rhythms and event related potentials. Although brain computer interfaces were initially developed for providing alternate means of communication they are now being using in a myriad of applications. This chapter will discuss explore in detail some BCIs, their various applications and challenges.

2.3.1 Background

In the BCI literature BCI are generally divided into two different categories. (i) Dependent form of BCIs do not use normal output pathways to transfer the messages but activity must be present to produce brain activity. The most common form of dependent BCIs are visually evoked potentials where a gaze/ visual activity recorded from the scalp controls the EEG output. (ii) An independent BCI is one in which the BCI does not depend on the brains normal output pathways in any way and are mostly done by imagination and are of much more interest to the BCI research community . Examples of these include the P300, slow cortical potentials, mu and beta rhythms, and cortical neurons.

2.3.1.1 General BCI framework

Mason and Birch introduced a basic framework for a complete BCI system. [15] Figure 2.9 demonstrates a basic BCI System proposed by Mason and Birch. A BCI system has a subject whose electrical activity of the scalp is being monitored. A BCI system includes a subject, acquisition hardware, electrodes, a feature extractor, a feature translator, and a BCI paradigm with user interface.

In a common BCI system electrical activity is recorded from the scalp of a subject using electrodes, these signals are then digitized by the acquisition hardwares analog to digital converter. These digitized signals are then transformed into different values known as feature values or simply features. Mason and Birch stress that these terms should be consistent with the pattern recognition community and the output must be known as the feature vector. Examples of features could be in the time domain the amplitude of the evoked potentials and in the frequency domain the spectral power in the mu/beta bands.

The next stage of a BCI system is classification, which is also called translation. The translation algorithm, translates the signals extracted features into device independent logical

values. These translation methods can be linear or non-linear.

The final block in a BCI system is the control interface which converts the logical values outputted from the translator into device control signals where the device controller could be a software or hardware which converts the device control signals into physical signals and the actual device could be a synthesizer, a LED or a computer screen. The two broad categories of

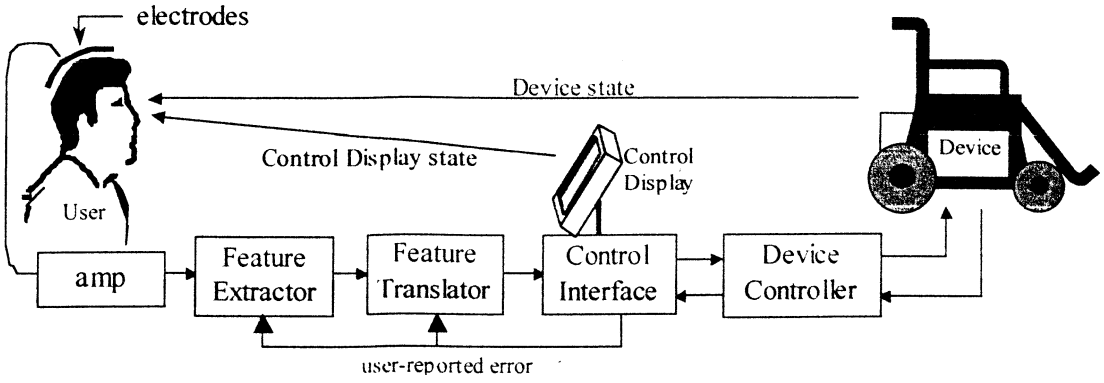


Figure 2.9: BCI system proposed by Mason and Birch. From A General Framework for Brain Computer Interface Design by Steven G. Mason, and Gary E. Birch

BCI namely the dependent and the independent BCI were discussed before. The next subsection will discuss in detail the different examples of those BCI which are currently being studied.

2.3.1.2 Types of BCI

Present-day non-invasive BCIs generally fall into our different categories [17] which include:

1. **Steady State Visually Evoked Potential (SSVEP):** Steady state visually evoked potentials fall into the category of dependent BCIs. Several studies conducted by Vidal, Sutter, and Middendorf et. al have demonstrated the use of visually evoked potentials for a BCI system with average bit rate of 10 -12 words a minute. These VEP based systems depend on the subjects ability to control gaze direction.

2. **Slow Cortical Potentials:** SCP's are among the lowest frequency recorded EEG waves from the cortex. These shifts occur over half a second to ten seconds. Negative SCPs are related to cortical activation, while positive SCPs are related to reduced cortical activation. Birbaumer et al. showed that subjects can learn to control their SCP and hence can control the movement of a cursor on a screen.

3. **P300 Evoked Potential:** One of the most successful and useful of the non-invasive EEG-based BCI modalities utilizes the oddball evoked responses typically from visual stimuli. Farewell and Donchin [19] are credited with demonstrating the first use of such responses to create a direct brain-activity to computer spelling system. Within such a paradigm, an array of targets for example letters for a speller are serially highlighted in random order. Each time a target is highlighted, it evokes a measurable brain signal or potential a visually evoked potential. If the subject concentrates on a particular target, the shape and time-course of the evoked potential corresponding to that target is different, and has a marked peak at approximately 300 ms after the stimulus, denoted the P300.

4. **Sensory Motor Rhythms or Imagined Motion:** Sensory motor rhythms have been used over the past decade for development of BCIs. Pfurtscheller and Lopes Da Silva showed that any movement or imagination of movement causes a decrease in the mu/beta rhythm, they term the decrease in rhythm as event related de synchronization or ERD. In awake people, the mu rhythm is observed at $8 - 12$ Hz in the EEG activity when the subject is not involved in any activity, hence it is also called the idling rhythm. Beta rhythms observed at $18 - 26$ Hz are believed to be harmonics of the mu rhythm. Since ERD and ERS do not require actual movement, they form a part of independent BCIs.

2.3.2 Challenges

Apart from basic challenges in measuring the EEG signal, there are more challenges in development of a successful BCI. The skills required for implementing and improving BCIs range from the basics of electronics and biopotential recordings, to the implementation of off-line and real-time signal processing, to the cognitive and human factors considerations in making a human-machine interface. Indeed, the multidisciplinary nature of this work makes implementing BCIs much more complex. Further due to risk of injury due to brain surgery and limited number of subjects available these recordings are mostly non invasive and hence do not provide good spatial resolution, are noisy, and require training for a subject to be able to use a BCI to its fullest potential. Overall BCIs are not completely robust and reliable, they are not perfect and cannot be used clinically. Further, most BCIs are slow and have lower information transfer rate/slower communication rate. Visually evoked BCI paradigms which require long periods of staring at the

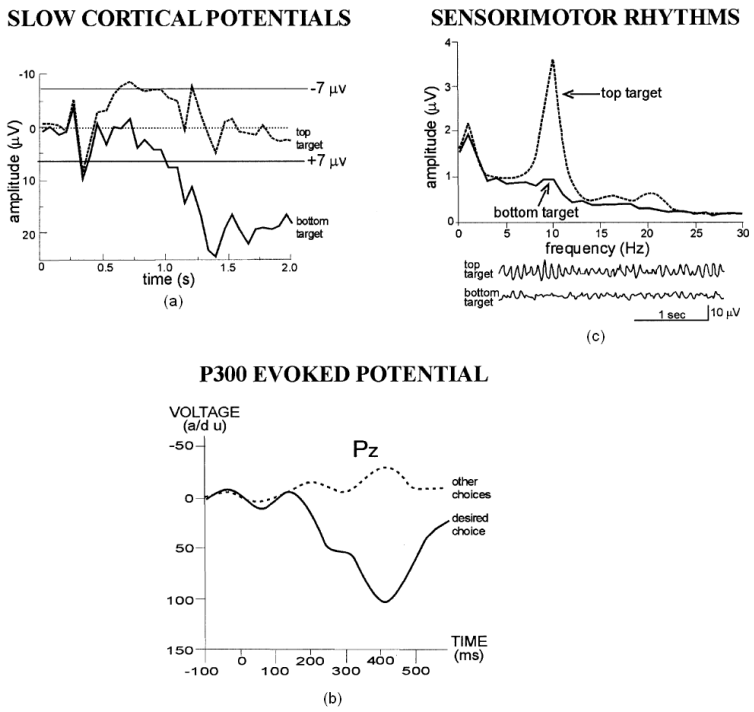


Figure 2.10: Different types of independent BCIs. Modified From Brain computer interfaces for communication and control J. R. Wolpaw et. al

screen and are not comfortable. Above all using BCI is a skill and requires that users learn and maintain this skill, not everybody can effectively control a BCI.

2.3.3 Applications

Although brain computer interfaces were initially developed for providing alternate means of communication they are now being using in a myriad of applications. This section aims to give a brief insight into the various applications of brain computer interfaces. [22]

1. **Assistive Technology:** The original motivation for developing BCIs was to provide assistive technology in forms of an alternative means of communication to people with locked-in syndrome and chronic diseases including the Amyotrophic Lateral Sclerosis (ALS). Researchers have been studying BCIs for over three decades now to develop effective assistive devices. There has been development of yes/no communication, various types of spellers and web browsers. Also combining elements of robotics researchers have been developing brain controlled wheelchairs

2. **Rehabilitation:** In the field of rehabilitation and neural prosthetics there is ongoing research to develop therapies to restore the motor control of affected subjects. Many research groups are studying neural plasticity and finding ways to somehow re-wire the brain. Pfurtscheller et al. showed that a paralyzed patient learnt to regulate their sensorimotor rhythms to control functional electrical stimulation (FES) of arm and hand muscles to perform simple tasks such as grasping a glass. Many other researchers in this field are carrying work on neural prosthetics and rehabilitation devices and remains to be a promising field.

3. **Diagnostics and Improving Cognition:** In addition to their use in assistive technologies and rehabilitation, BCIs have been developed to aid in clinical diagnosis, influencing, and improving cognitive functioning. Using neurofeedback, BCIs have been used in coma detection, attention monitoring for driver safety.

4. **Gaming:** BCIs games were initially developed for locked in patients. Some of these BCI games include the Berlin BCI which includes a simple Brain Pong game and a Pacman-style game, controlled by modulating Slow Cortical Potentials. BCIs have not stayed away from the commercial gaming world. Commercial organizations such as NeuroSky and Emotiv are developing BCI games.

Chapter 3

Hardware Design

The advances in technology and development of low cost, low power sensors, ADCs greatly aid in availability of medical instruments and thus contribute to better diagnosis. This chapter will discuss in detail the three main components of the ADS1298: an analog front-end (ADS1298, Texas Instruments, Inc.), a microcontroller (MSP430F5525, Texas Instruments, Inc.), and isolation circuitry for USB and power (ADuM4160 and ADuM5000, Analog Devices, Inc.).

3.1 Analog Front End:ADS1298

The use of ADS1298 aids remarkably in reduction of size, power (0.75mW/channel) and overall cost of the device. It has built-in programmable gain amplifiers (PGA) and CT(CT) $\Delta\Sigma$ ADCs dedicated to each channel. It includes an internal reference common for all ADCs, an on-chip clock oscillator, and a serial peripheral interface (SPI) communication port. Additionally it can be configured for various differential input and referencing configurations, as well as both passive and active ground configurations. [11]

In addition to basic switching, differencing, and modest preamplification, these ICs contain up to 8 simultaneous 24 bit continuous delta-sigma analog to digital converters (CT$\Delta\Sigma$ ADC) with data rates of 250 SPS to 32kSPS. The key advantage of the CT$\Delta\Sigma$ ADC in this architecture is that they remove the need for additional gain and ideally preclude the need for any anti-alias filtering prior to digitization [11], [12], [13], [14]. With variable data rates the cost of gain circuitry and analog anti-aliasing filters is high, the CT$\Delta\Sigma$ reduces the need of any such circuitry

and reduces cost considerably. The ADS1298 incorporates all of the features that are commonly required in medical ECG and EEG applications.

3.1.1 Features

The Figure. 3.1 shows the complete architecture of the ADS1298. This section will discuss the analog components of the ADS1298 followed by the digital interface to receive the conversion data from the device.

Electrical Characteristics : The power supply for the ADS1298 can be unipolar or

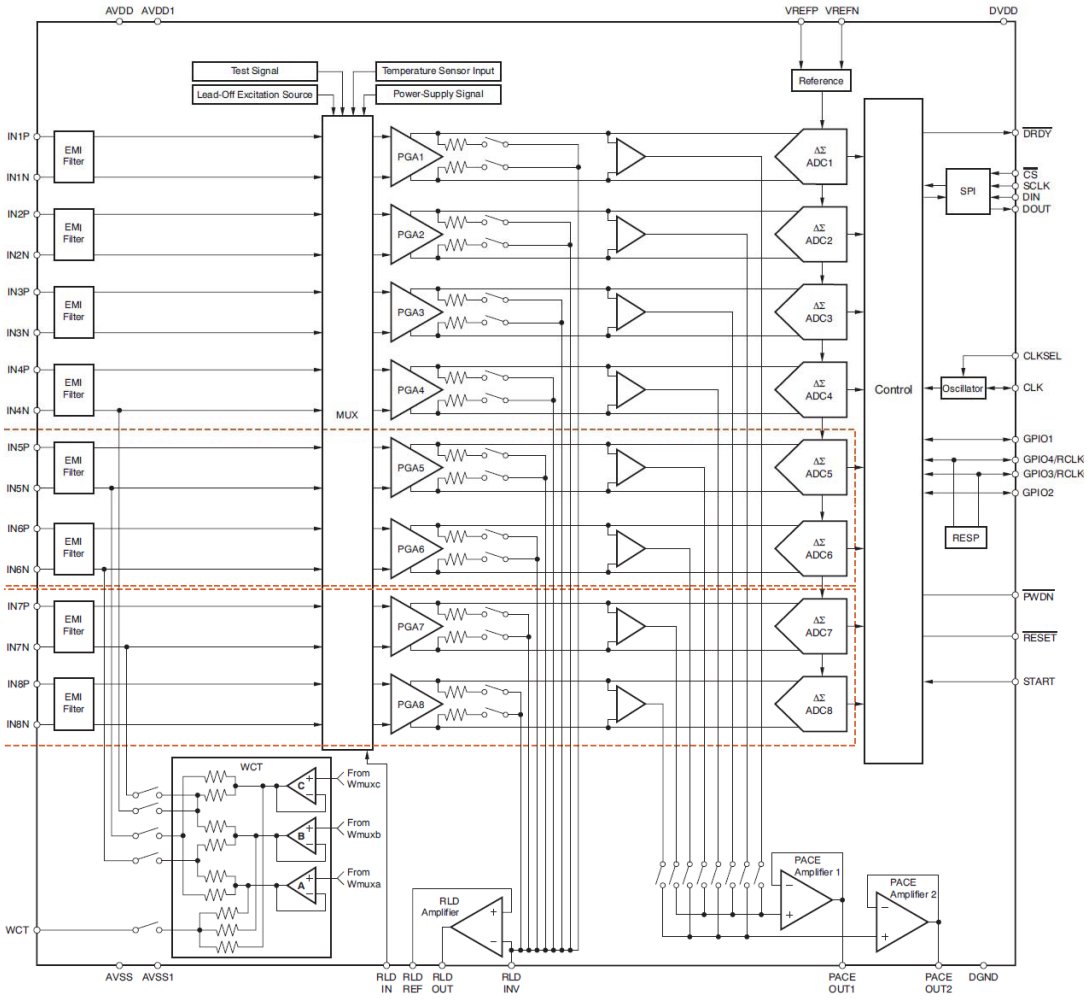


Figure 3.1: Figure shows the complete ADS1298 components including electromagnetic interference filter, programmable gain amplifiers, eight CTΔΣ ADCs, input reference, SPI interface, RLD amplifier, PACE amplifiers, Wilson Central Terminal circuitry, test signals and temperature sensor inputs.

bipolar with analog supply ranging from 2.7V to 5.25V and digital 1.65V to 3.6V. The prototype uses $\pm 1.8V$ analog power supply and a digital supply of 3.3V. The front end was operated in low power mode with an internal reference voltage of 2.4V. It has an operating temperature range which is 40°C to +85°C

Analog Input: The analog input to the ADS1298 is fully differential. The input positive voltage is INP and input negative is INN, the net signal INP−INN can span between $\pm V_{REF}/Gain$ where V_{REF} is reference voltage.

Programmable Gain Amplifier: The ADS1298 has eight low noise PGAs. It provides seven gain settings of 1, 2, 3, 4, 6, 8, and 12. By default this gain is set to 6.

EMI filter: ADS1298 provides an EMI filter to protect from disturbance created by electromagnetic induction. The EMI filter used is an RC filter with a -3dB bandwidth of 3MHz across all channels.

Input Multiplexer: The ADS1298 provides input multiplexers for configuring signal switching options easily. INP and INN are separate for each of the eight blocks. The ADS1298 provides the options of normal electrode input, input shorted, supply measurements, temperature sensor, test signals, right leg drive inputs, auxiliary differential input, lead-off excitation signals and auxiliary single ended inputs. TEST_PACE_OUT1, TEST_PACE_OUT2, and RLD_IN are common to all eight blocks and are used for testing and ECG specific functions discussed in later sections. VINP and VINN are separate for each of the eight blocks. Thus the multiplexer allows for easy changes in device configuration, and calibration. Channel specific settings can be changed by changing the CHnSET register and by writing the RLD_MEAS bit in the CONFIG3 register for using right leg drive measurement.

Continuous Time Delta Sigma (CTΔΣ)Modulator: Analog to digital converters are used to convert an analog signal into a digital signal. In this section, the CTΔΣ ADC conversion will be described. A continuous delta-sigma ADC consists of a CTΔΣ modulator followed by a digital low pass filter and a decimator. Figure 3.3 shows the basic block diagram of a Delta-Sigma converter, and Figure 3.4 shows a CTΔΣ modulator. [12, 13, 14] A complete block diagram is shown in Figure 3.5.

What differentiates the CTΔΣ ADC from other Nyquist or oversampled ADCs is that it ideally avoids the need of any other anti-alias filtering. The basic principle is to shape the quantizer noise such that most noise is shifted out of band and preclude or reduce the requirements

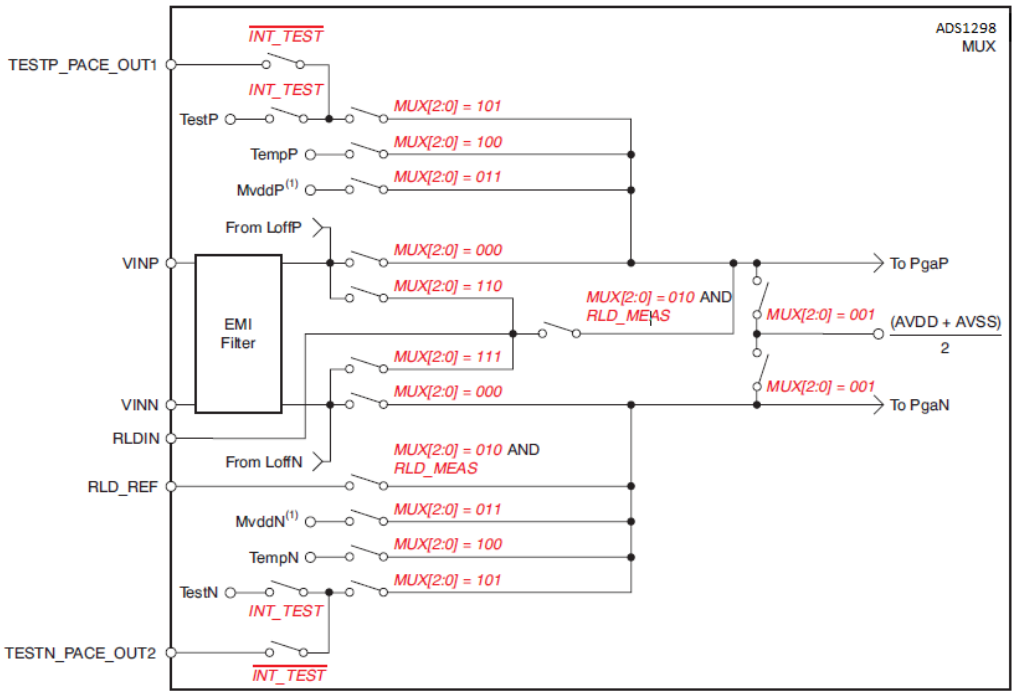


Figure 3.2: Figure shows input multiplexer options on the ADS1298 chip from ADS1298 datasheet.

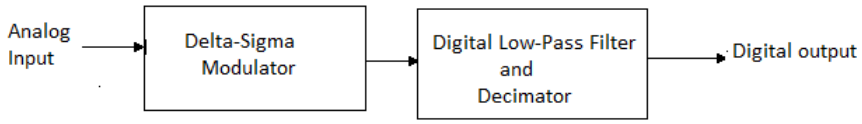


Figure 3.3: A delta-sigma ADC

of the anti-alias filtering. The CT$\Delta\Sigma$ converter uses oversampling by sampling at rate much higher than the desired output data rate. In contrast with a DT$\Delta\Sigma$ converter utilizes low-power CT integrators, and no switching capacitors, which makes them cheaper and reduces switching noise. Sampling occurs at output of the integrator before the quantizer in a CT$\Delta\Sigma$ converter, in contrast in a DT$\Delta\Sigma$ converter, sampling occurs at input of ADC. Each channel of the ADS1298 has a 24-bit $\Delta\Sigma$ ADC. The basic block diagram of a $\Delta\Sigma$ converter is shown in Figure. 3.2.

A CT$\Delta\Sigma$ modulator: It is the heart of the CT$\Delta\Sigma$ modulator. The block diagram of a first order CT$\Delta\Sigma$ converter is show in Figure. 3.3. The detailed block diagram of the first order modulator is shown in Figure. 3.4. Its output is a stream of N bit numbers at a high rate f_{MOD} called the modulator frequency 256k SPS in low power mode and 512kSPS in high power

mode when using internal oscillator). This is much faster than the final frequency F_{DR} at which samples are produced which is generally 250 - 32k SPS and the ratio F_{MOD}/F_{DR} is called the oversampling ratio.

The basic operation is as follows. First, the analog input goes into a difference amplifier, which subtracts (hence delta) the current value of the output to leave the error and then this error is filtered using a loop filter which is basically an integrator (similar to summation, hence sigma). The output of the integrator is converted from analog to digital using an ADC. This digital signal is then fed back and converted back to analog using a DAC so that it can be subtracted from the input, thus forming a feedback loop.

The ADS1298 consists of second order 16 bit CT$\Delta\Sigma$ modulator. A second order CT$\Delta\Sigma$ modulator helps produce bit streams which produce less noise at the low pass filter outputs. It is produced by simply cascading another stage of the input. The modulator samples the input signal at the rate of $f_{MOD} = f_{CLK}/4$ for high-resolution mode and $f_{MOD} = f_{CLK}/8$ for the low-power mode, where f_{CLK} denotes the frequency of the signal at the CLK pin and f_{MOD} denotes the frequency at which the modulator samples the input. On the ADS1298 the modulator samples the input signal at the rate of $f_{MOD} = f_{CLK}/4$ for high-resolution mode and $f_{MOD} = f_{CLK}/8$ for the low-power mode, where f_{CLK} denotes the frequency of the signal at the CLK pin =2.048MHz and f_{MOD} denotes the frequency at which the modulator samples the input.

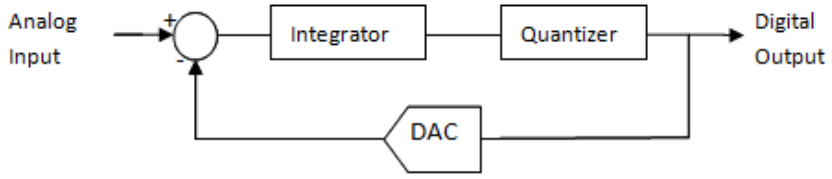


Figure 3.4: Block diagram of a first order $\Delta\Sigma$ modulator. It consists of a difference, loop filter, ADC, a sample and hold circuit, and a DAC

Low Pass Filter and Decimation Filter: The second part of the ADC handles purely digital signals. Its takes bits of data from the modulator and convert them to a slower stream of multi bit values. First the digital signal is processed by a low-pass filter. The filtered digital signal is then decimated to reduce the rate of samples from f_{MOD} to required sampling rate. On the ADS1298 the digital filter on each channel consists of a third-order sinc filter. The sinc filter is basically a variable decimation rate, third-order, low-pass filter. Data are supplied to this section of the filter from the modulator at the rate of f_{MOD}. The sinc filter attenuates the

high-frequency noise of the modulator, then decimates the data stream into parallel data. The frequency domain transfer function of the sinc filter is shown in the equation below, where N is decimation ratio detailed in table 3.4

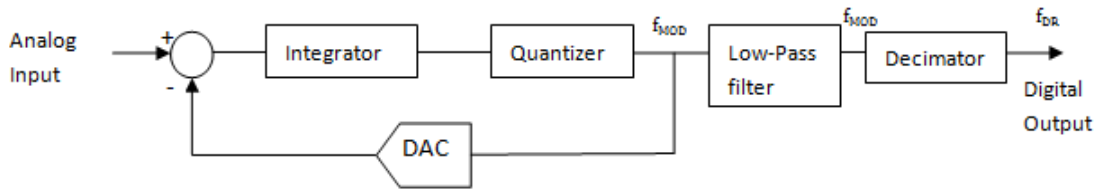


Figure 3.5: Figure shows the complete block diagram of a Delta Sigma ADC

$$H(f) = \left| \frac{\sin\left(\frac{N\pi \times f}{f_{MOD}}\right)}{N\left(\frac{N\pi \times f}{f_{MOD}}\right)} \right|^3$$

Reference: The ADS1298 provides option for using internal and external references. When using 3V analog supply reference voltage of 2.4 V must be used and when using 5V supply can be either 2.4V or 4V.

Clock: The ADS1298 provides option for using internal and external clocks. Internal clock is 2.048MHz. The clock select pin CLKSEL is used to select either external or internal clock. The CLKSEL pin must be pulled high for internal oscillator and low for external oscillator. The external clock frequency should range between 0.5MHz-2.25Mhz.

Data Format: The ADS1298 outputs a 24 bit value of data per channel in binary two's complement format with the most significant bit first. The smallest values which can be measured correctly is $V_{REF}/(2^{23}-1)$. Table 3.1 summarizes the ideal output codes for different input signals. Data rate of 16kSPS and 32kSPS have missing codes and only have 19 bits and 17 bits of resolution respectively and hence the last 5 and 7 bits respectively can be safely ignored.

3.1.2 Communicating with the ADS1298

ADS1298 needs to be programmed to operate at a specific data rate. The only way to communicate with the ADS1298 to program, and read conversion data from the ADS1298 chip is via serial peripheral interface(SPI) communication.

Serial Peripheral Interface is a common communication standard and is widely used to communicate with various peripherals such as sensors, control devices, camera lenses, memory

Input Signal (INP−INN)	$\mathbf{V}_{OUT}$
$\geq V_{REF}$	7FFFFFh
$+V_{REF}/2^{23}-1$	000001h
0	000000h
$-V_{REF}/2^{23}-1$	FFFFFFh
$\leq -V_{REF}(2^{23}/2^{23}-1)$	800000h

Table 3.1: Output ADC code for the range of input analog signals from $-V_{REF}$ to $+V_{REF}$ in twos complement format.

cards and LCD displays etc.[29]. It is a synchronous serial data link standard named by Motorola. In this standard, devices communicate in master/slave mode where the master device initiates the data frame. SPI communication has four logic signals:

i) SCLK :Serial Clock which is outputted from master

ii) MOSI :Master Out Slave in which is the data sent from the master device to the slave

iii)MIS0 :Slave Output, Master Input is the data received from the slave device

iv) $\overline{CS}$: is slave select enable (logic low).

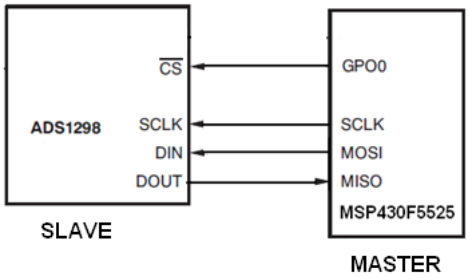


Figure 3.6: Figure shows serial peripheral interface communication with just one slave device, SCLK are shorted to each other, DOUT of master is connected to DIN of slave and vice-a-versa, and ($\overline{CS}$) is pulled to low

For communication during each SPI clock cycle, a full duplex data transmission occurs and the master sends a bit on the MOSI line and the slave sends a bit on the MISO line which is read by the master. Transmissions normally involve two shift registers of eight bits, one in the master mode and the other one in the slave mode, connected to each other in form of a ring buffer. Data is shifted out with the most significant bit first, while shifting a new least significant bit into the same register. After that register has been shifted out, the master and slave have exchanged register values. Then each device takes that value and stores it and performs the intended operation. If there is more data to exchange, the shift registers are loaded with new

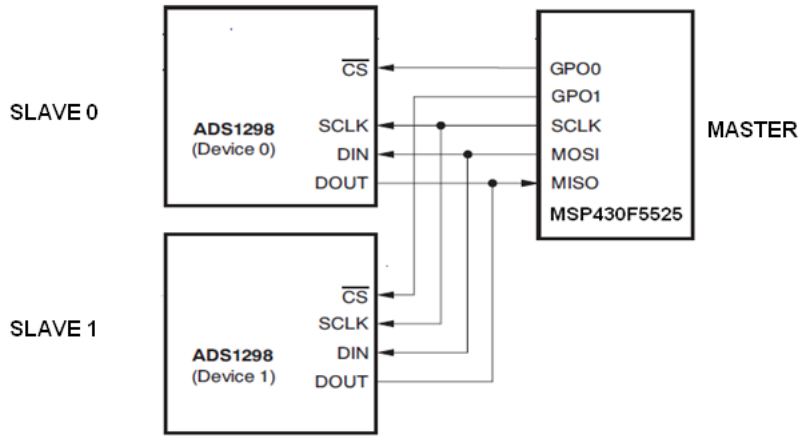


Figure 3.7: Figure shows serial peripheral interface communication with multiple slave devices in standard mode. In this mode SCLK, DIN, and DOUT are shared across devices but each device has its own ($\overline{CS}$)

data and the process repeats. The master can only select one device at a time. When multiple slave devices are present, the devices are cascaded together with DOUT, SCLK, and DIN shared for each slave device but individual chip selects for each device. Since at a time only one device can be selected, the chip select ($\overline{CS}$) must be pulled low for the device to be enabled and high for all other devices.

3.1.3 Command definitions

The ADS1298 provide a flexible way of programming and configuring the device by programming values into its registers. An opcode needs to be send through SPI communication to control and configure the operation of the device. There are three kinds of SPI commands which are summarized in Table 3.2:

System Commands: These commands are basic commands for resetting, starting conversions, stopping conversions, waking up from standby and entering into standby mode. They require only one fixed opcode to be sent from the host to the ADS1298 and they pose no restrictions on the SCLK rate.

WAKEUP: Sending this opcode exits the device from the standby mode. Any subsequent command must be sent after 4 t_{CLK} cycles.

STANDBY: Sending this opcode puts the ADS1298 to low power sleep mode and all

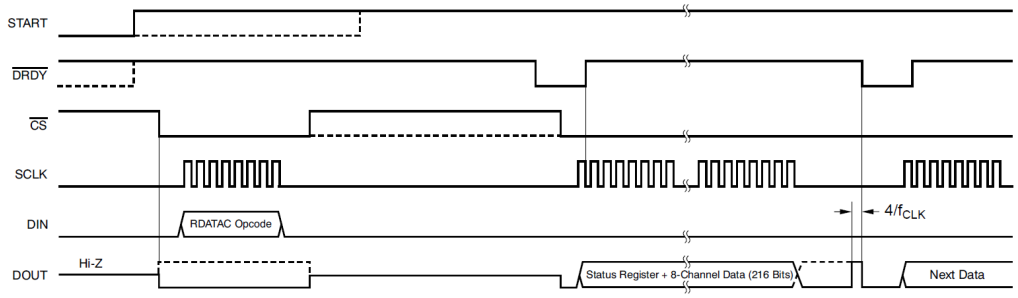


Figure 3.8: Timing diagram explaining the usage of Read data continuous mode command (RDATAC)

parts except the reference are shut down.

RESET: This command resets all registers to their default values. 18 t_{CLK} cycles are required to execute this command and no other commands should be sent during this time.

START: This opcode starts the data conversions. software control the START pin must be tied to low. If conversions are in progress this command will have no effect. A period 4 t_{CLK} cycles must be present between the start and any other command.

STOP: This opcode will stop conversions.

Data Read Commands: These commands are used for reading conversion data from the ADS1298. The ADS1298 provides two modes to read data namely RDATA where only one read operation is performed at a time, and read data in continuous mode (RDATAC) where continuous conversion takes place without the need to send another opcode. To stop continuous conversion SDATAC command must be sent, by default when the device powers up it is in RDATAC mode.

RDATAC: This command sets the ADS1298 into read continuous data mode without the need of sending subsequent opcodes. A data ready status pin ($\overline{DRDY}$) toggles whenever a new data is available. For this opcode to work first the START command must be sent. This mode is the default mode of the device on power-up and reset. It is cancelled by the Stop Read Data Continuous command. There is no restriction on the SCLK rate for this command but an update time of 4 t_{CLK} cycles must be present between subsequent retrieval SCLKs. A timing diagram for the RDATAC command is shown in Figure 3.8.

SDATAC: This command cancels the RDATAC command. There is also no restriction on SCLK, but there must be a delay of 4 t_{CLK} cycles between subsequent clock cycles.

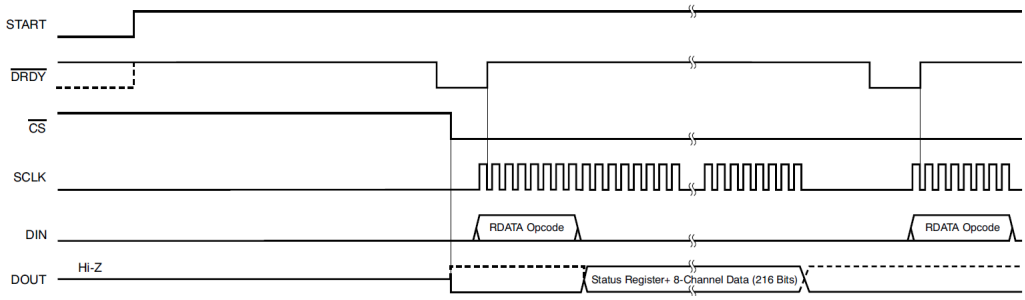


Figure 3.9: Timing diagram explaining the usage of Read data command(RDATA)

RDATA: This command is used for reading conversion data on a sample by sample basis. The START command must be issued for the RDATA opcode to work. In this command there is no restriction on SCLK and there is no update period, the read operation can overlap the next ($\overline{DRDY}$) without data contamination. Figure 3.9 shows the timing diagram for the RDATA opcode.

Register Read Commands: These commands are used for programming the ADS1298 by writing its register using WREG command and reading the register using RREG command. These commands need two byte opcodes to be sent. The first byte contains the command opcode and the register address. The seconds byte specifies the number of registers to be read -1. These commands being multi byte pose restrictions on the SCLK. The ADS1298 serial interface decodes commands in bytes and requires 4 clock cycles to decode and execute. Therefore, when sending multi-byte commands, a 4 t_{CLK} period must separate the end of one byte (or opcode), where $t_{CLK} = 1/f_{CLK}$. Since internal clock frequency is 2.048MHz, then the time to decode an instruction $t_{SDECODE}$ is (4 t_{CLK}) is 1.96μs. So when SCLK is 16MHz, one byte can be transferred in 500ns, this byte transfer time will not meet the $t_{SDECODE}$ specification and hence a delay must be inserted at the end of the second byte.

RREG: This opcode reads the register data, a two-byte opcode which followed by output data. The two byte opcode contains the command opcode and the register address (001r rrrr), where r rrrr is starting register address in the first byte . The second byte specifies the number of registers to read -1 (000n nnnn), where n nnnn is the number of registers to read -1. Figure 3.10 shows the timing diagram for the RREG command. On the 17th SCLK rising edge the MSB of the first register arrives. This command can be issued any time but multibyte command

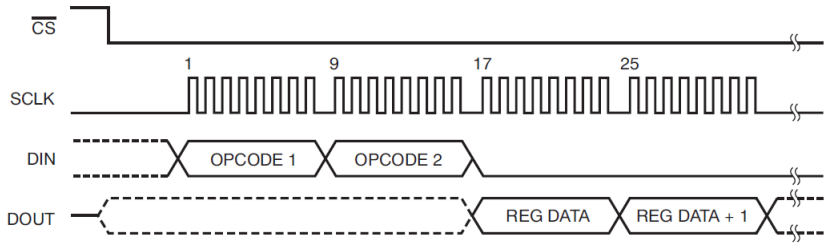


Figure 3.10: Timing diagram explaining the usage of Read register command(RREG)

restrictions apply.

WREG: This opcode writes the register data and programs the ADS1298 with the required settings. Similar to the RREG it is also a two byte opcode which contains the command opcode and the register address (001r rrrr), where r rrrr is starting register address in the first byte. The second byte specifies the number of registers to written−1 (000n nnnn), where n nnnn is the number of registers to be written −1. Figure 3.11 shows the timing diagram for the WREG command. This command can be issued any time but multibyte command restrictions apply.

COMMAND	DESCRIPTION	FIRST BYTE	SECOND BYTE
System Commands			
WAKEUP	Wake-up from standby mode	0000 0010 (02h)	
STANDBY	Enter standby mode	0000 0100 (04h)	
RESET	Reset the device	0000 0110 (06h)	
START	Start/restart (synchronize) conversions	0000 1000 (08h)	
STOP	Stop conversion	0000 1010 (0Ah)	
Data Read Commands			
RDATAC	Enable Read Data Continuous mode.	0001 0000 (10h)	
SDATAC	Stop Read Data Continuously mode	0001 0001 (11h)	
RDATA	Read data by command; supports multiple read back.	0001 0010 (12h)	
Register Read Commands			
RREG	Read n nnnn registers starting at address r rrrr	001r rrrr (2xh)	000n nnnn
WREG	Write n nnnn registers starting at address r rrrr	010r rrrr (4xh)	000n nnnn

Table 3.2: Table shows ADS1298 SPI Command Definitions including System commands, data read commands and register read/write commands.

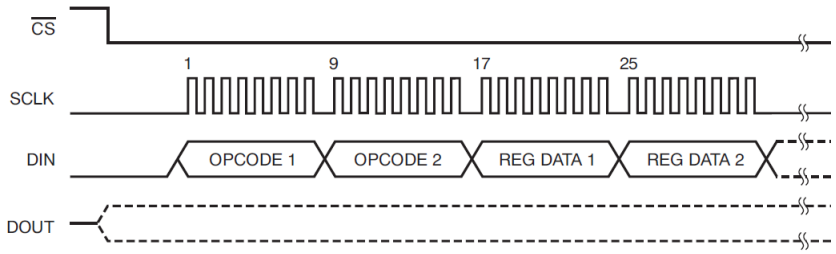


Figure 3.11: Timing diagram explaining the usage of write register command(WREG)

3.1.4 Programming the ADS1298

The ADS298 must be programmed by changing the values of its internal registers (for more details refer ADS1298 datasheet). This section will highlight some of the basic register settings which need to be changed.

Basic Settings: The basic settings comprise of setting the operating mode, sampling frequency, the programmable gain, and setting the internal multiplexer values on the ADS1298. In order to choose the clock source for the ADS1298, operating mode (high power or low power), and the sampling rate the configuration 1 register settings of the ADS1298 need to be set. Table 3.1 shows the register map for the configuration register 1. Bit 7 HR, determines controls the devices operating mode: 0 for low power, and 1 for high resolution. By default the prototype is in low power mode, and multireadback mode is used. Bit 6 $\overline{DAISY\_EN}$ determines which mode is enabled: 0 for daisy chain and 1 for multiple read back mode. Bit 5 CLK_EN: determines if the internal oscillator signal is connected to the CLK pin, when the CLKSEL pin = 1. It is 0 when oscillator clock output is disabled (default), and 1 when enabled. Bits[4:3] must always be set to '0'. Bits[2:0], DR [2:0] determine the output data rate of the device. For high resolution mode, $f_{MOD} = f_{CLK}/4$ and for low power mode, $f_{MOD} = f_{CLK}/8$. The table below determines the data rate based on sampling rate and power mode [11].

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
HR	$\overline{DAISY\_EN}$	CLK_EN	0	0	DR2	DR1	DR0

Table 3.3: Register map of configuration 1 register

BIT	DATA RATE	HIGH-RESOLUTION MODE	LOW-POWER MODE
000	$f_{MOD}/16$	32kSPS	16kSPS
001	$f_{MOD}/32$	16kSPS	8kSPS
010	$f_{MOD}/64$	8kSPS	4kSPS
011	$f_{MOD}/128$	4kSPS	2kSPS
100	$f_{MOD}/256$	2kSPS	1kSPS
101	$f_{MOD}/512$	1kSPS	500SPS
110 (default)	$f_{MOD}/1024$	500SPS	250SPS
111	Not used	N A	N A

Table 3.4: Table shows the values of DR[2:0] to be set to get the required sampling rate in low and high power mode of operation.

In order to set the reference values for the Delta Sigma ADC, the values in the CONFIG3

register must be set. Bit 7 PD_REFBUF determines the power-down reference buffer state. To power-down internal reference buffer bit 7 must be set to 0 (default) and 1 to enable internal reference buffer. Bit 6 Must always be set to '1'. Default is '1' at power-up. Bit 5 VREF_4V determines the reference voltage, VREFP. It should be set 0 for 2.4 V which is the default value. To set VREFP to 4V (use only with a 5V analog supply) it should be set to 1.

BIT 7	BIT 6	BIT 5
PD_REFBUF	1	VREF_4V

Table 3.5: Register map of Bist [7:5] of the configuration 3 register

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
PD	GAIN2	GAIN1	GAIN0	0	MUXn[2]	MUXn[1]	MUXn[0]

Table 3.6: Register map of CHnSET register

BITS[6:4]	Gain(default)
000	6(default
001	1
010	2
011	3
100	4
101	8
110	12

Table 3.7: Different possible gain values for changes in bits [6:4] of the CHnSET register.

To change the power mode, PGA gain, and input multiplexer settings the CHnSET registers need to be modified where n=1:8, one for each channel. For each channel to power down the channel the Bit 1 PD of the CHnSET register must be set to 1; by default it is 1 for normal operation. To change individual channel gains the bits [6:4] need to be changed. Bit 3 must always be set to 0. Bit [2:0] help set the input multiplexer settings. These are set to zero by default for normal electrode operation. They can be changed based on the values in the table 3.7.

Lead off Detection: Electrode impedances tend to decay over time, also due to subject movement the electrode connections may become loose. It is important to continuously monitor the electrode connections. It is done by injecting an excitation signal and measuring the output

MUXn[2:0]	Input multiplexer Settings
000	Normal electrode input (default)
001	Input shorted (for offset or noise measurements)
010	Used in conjunction with RLD_MEAS bit for RLD measurements.
011	MVDD for supply measurement
100	Temperature sensor
101	Test signal
110	RLD_DRP (positive electrode is the driver)
111	RLD_DRN (negative electrode is the driver)

Table 3.8: Different possible gain values for changes in bits [6:4] of the CHnSET register.

to determine status of electrode connection. ADS1298 provides two methods for determining the state of the electrode connection using either an ac signal or a dc signal. To accomplish lead off detection lead off sense positive (LOFF_SENSP) and lead off sense negative (LOFF_SENSN) of that specific channel must be set to '1'. The status of leads is reported in registers lead status positive LOFF_STATP and lead status negative, where'0' is lead-on (default) and '1'is lead-off. For lead off detection a current is passed whose direction is controlled by LOFF_FLIP for each channel.

Sample code to set dc lead-off with pull-up/pull-down resistors on all channels from the ADS1298 datasheet the registers LOFF, CONFIG4.First the comparator threshold should be set by writing to LOFF register 0x13 for 95% and 5%, pull-up/pull-down resistor. Next, turn on dc lead-off comparator by writing 0x02 to CONFIG4 and turning on p, and n-side of all channels for lead-off sensing.

Testing/ Calibration related functions : The ADS1298 provides options for internal noise testing, and calibration. These can be configured by changing the register values. In the CONFIG 2 register bit 4 INT_TEST bit is used to select the test source, 0 for external, and 1 for internal. The test signal amplitude can be set by using the TEST_AMP bit to determine the calibration signal amplitude. 0 for 1 $\times -(V_{REFP} - V_{REFN})/2.4mV$ (default) and 1 for double that values. To set the test signal frequency the TEST_FREQ[1:0] bits must be set to 00 for $f_{CLK}/221$ and 01 for $f_{CLK}/220$, 11 for dc conditions, and 10 is not used.

Electrocardiogram (ECG) related functions : The ADS 1298 provides various ECG specific functions which includes options for including the right leg drive, pace detect, and Wilson central terminal circuitry. The corresponding ADS1298 registers need to be programmed to make use of

these settings.

Right Leg Drive: The right leg drive circuitry is a technique to reduce the common mode signal by feeding the inverted common mode signal to the body. First the RLD_MEAS bit(RLD measurement) must be enabled to route right leg drive input (RLD_IN) to the channel with multiplexer setting 010. Next set RLD reference signal source RLDREF_INT to 0 for external signal or 1 for internal signal (AVDD-AVSS)/2. RLD buffer power bit in CONFIG3 register determines the RLD buffer power state, 0 for power down and 1 for enabling. For sensing lead off in RLD the RLD sense function RLD_LOFF_SENS is enabled. Finally the bit 0 in the configuration 3 register determines the RLD status 0 for connected and 1 for disconnected. To route the RLD_OUT signal through channel 4 N-side and measure RLD with channel 5, write 1xxx 0111 to CH4SET, and 1xxx 0010 to CH5SET.

Pace Detect: The ADS1298 provides a feature for PACE detection either using software or using an external hardware. For software the device must be operated at higher data rates generally > 8kSPS, followed by digital signal processing. The PACE register [7:5] must always be 0. PACE register [4:3], and register [2:1] help detect even channels on TEST_PACE_OUT1 and odd channels on TEST_PACE_OUT2 respectively. To turn on PACE buffer the bit 0 off PACE register must be turned on. Sample code to select channel 5 and 6 outputs for PACE is by writing 0001 0101 to PACE register.

Wilson Central Terminal: Is an effective way of measuring the ECG signal. It was suggested by Wilson et. al to use a central terminal as the reference for measurement of the electrocardiogram. This is formed by connecting a 30 k resistor and a 80pF capacitor from each terminal of the limb leads to a common point called the central terminal, as shown in Figure 3.12. In the standard 12-lead ECG, WCT voltage is defined as the average of Right Arm (RA), Left Arm (LA), and Left Leg (LL) electrodes. This voltage is used as the reference voltage for the measurement of the chest leads. The ADS1298 provide three low-noise amplifiers that generate the WCT voltage. There is flexibility to choose any one of the eight signals (IN1P to IN4N) to be routed to each of the amplifiers to generate the average signal. The RA, LA, and LL electrodes can be connected to any of the first four input analog channels. The three amplifiers

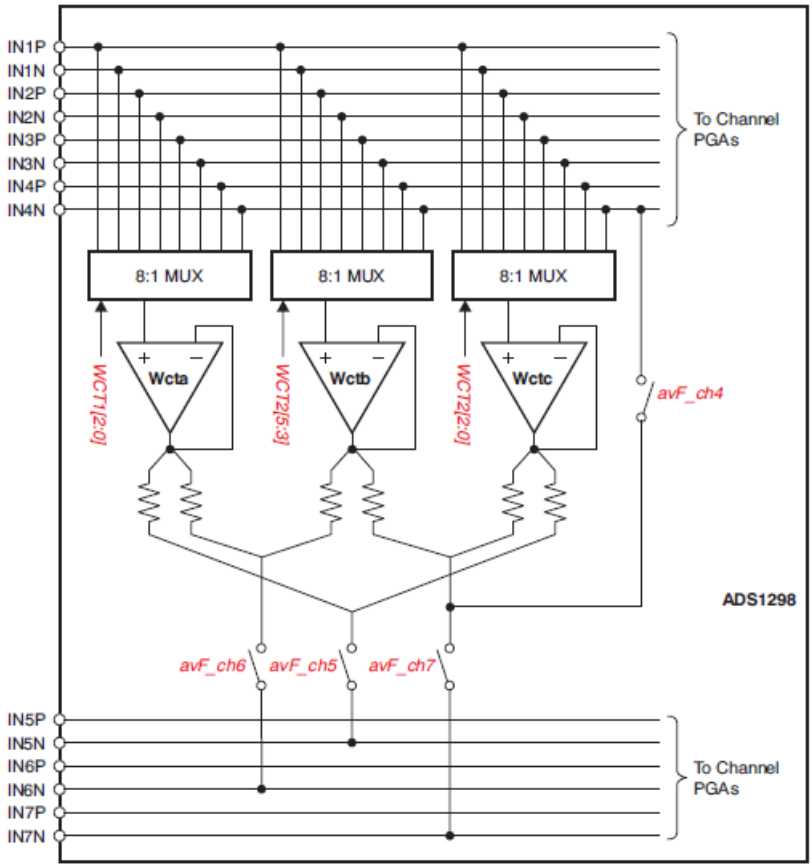


Figure 3.12: Wilson Central Terminal Connections from ADS1298 datasheet.

can be powered up and down individually. By powering up two amplifiers, the average of any two electrodes is generated at the WCT pin. The datasheet suggest use of more amplifiers to produce a noise immune signal.

3.1.5 Operating the ADS1298

Operating the ADS1298 involves going through a set of sequential steps. A complete block diagram of the hardware operation of the ADS1298 is shown in Figure 3.14. First the device must be powered up using the power up sequencing. First all digital and analog inputs must be pulled low. After connecting power supply, the clock signal must be supplied at the CLK pin, if wish to use external clock. Following a wait period of t_{POR} of 2^{16} clock cycles the power down($\overline{PDWN}$) pin, reset pin ($\overline{RESET}$) pin must be pulled high. Following a 1 second wait a reset pulse must be sent and after a $18t_{CLK}$ wait period the device can be used. First the SDATAC command

must be sent, followed by rest command. Next, the registers must be programmed by sending WREG command, where the reference must be set. Followed by, sending start opcode and reading conversion data using RDATAC opcode. In the design by default the $\overline{PDWN}$) pin, reset pin ($\overline{RESET}$), have been hardwired to high and the start pin ($\overline{START}$) to low. The output is stream of 27 bytes. The data format is (24 status bits + 24 bits × 8 channels) = 216 bits or 27 bytes. The format of the 24 status bits is: (1100 + LOFF_STATP + LOFF_STATN + 4 bits of the general purpose input output (GPIO) registers). The ADS1298 provides a total of four GPIO pins available in the normal mode of operation. Figure 3.13 shows the timing diagram for the DOUT register.

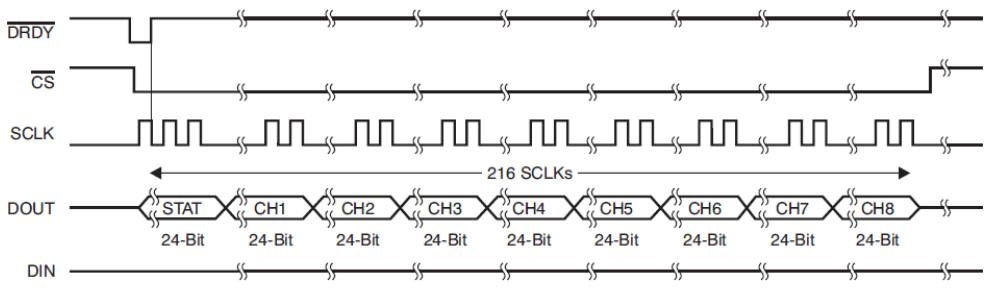


Figure 3.13: Timing diagram for Data out register (DOUT)

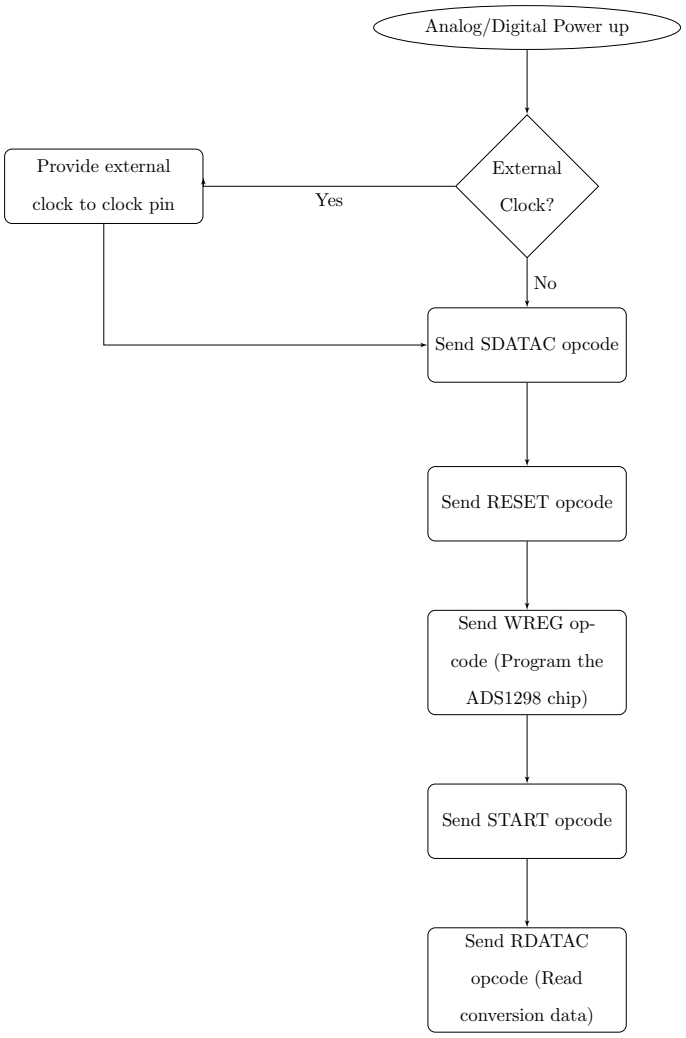


Figure 3.14: Flowchart summarizing the various series of operations of the ADS1298

3.2 MSP430F5525 Microcontroller

A low-power, low-cost microcontroller MSP430F5525 is used (available from Texas Instruments) for communicating with the ADS1298 and transmitting the conversion data from it to a computer. The MSP430F5525 device features a powerful 16-bit reduced instruction set architecture, a design strategy which is based on the idea that simplified instructions can provide higher performance if this simplicity enables much faster execution of each instruction. The CPU is integrated with 16 registers that provide reduced instruction execution time. The register-to-register operation

execution time is one cycle of the CPU clock. Four of the registers, R0 to R3, are dedicated as program counter, stack pointer, status register, and constant generator, respectively. The remaining registers are general-purpose registers. MSP430F5525 is fully integrated with USB 2.0 support, four 16-bit timers, a high-performance 12-bit analog-to-digital converter (ADC), two universal serial communication interfaces (USCI), hardware multiplier, Direct memory access controller, real-time clock module with alarm capabilities, and 63 I/O pins. operation. This section will describe the features of the MSP430, how to program the MSP430. [25]

Electrical Characteristics : The MSP430 can work at a voltage range from 1.8V -3.6V, the prototype uses a 3V supply. The power management module which will be discussed in the following sections is used to manage and supervise the power supply.

Operating Modes : The MSP430F5525 has been optimized for low power use. It has one active mode and six software selectable low-power modes of operation. An interrupt event can wake up the device from any of the low-power modes, service that request, and restore back to the low-power mode when done serving the interrupt routine.

Oscillator and System Clock: The core heart of any microprocessor or hardware subsystem is the clock which synchronizes and times all operations. Clock is a critical part of a real time embedded system. The clock system on the MSP430F5525 is supported by the Unified Clock System (UCS) module that includes support for a 32 kHz watch crystal oscillator (XT1), an internal very-low-power low-frequency oscillator (VLO), an internal trimmed low-frequency oscillator (REFO), an integrated internal digitally-controlled oscillator (DCO), and a high-frequency crystal oscillator XT2. The UCS module features digital frequency locked loop (FLL) hardware that which helps stabilizes the DCO frequency to a programmable multiple of the selected FLL reference frequency. The maximum oscillator frequency which can be generated by the internal oscillator(DC0) is 25MHz. XT2 CLK operation is required for USB. The different sources of clock signals:

Auxiliary clock (ACLK), is sourced from a 32 kHz watch crystal (XT1), a high-frequency crystal (XT2), the internal low-frequency oscillator (VLO), the trimmed low-frequency oscillator (REFO), or the internal digitally-controlled oscillator DCO.

Main clock (MCLK) is the system clock used by the CPU. MCLK can be sourced by same sources made available to ACLK.

Sub-Main clock (SMCLK) is the subsystem clock used by the peripheral modules. SMCLK

can be sourced by same sources made available to ACLK.

ACLK/n is the buffered output of ACLK divided by 2, 4, 6 , 8, 16,or 32.

Power Management Module (PMM): The Power management module is an important part of the MSP430 it supervises and manages all functions related to the power supply for the device. The PMM uses an integrated low-dropout voltage regulator (LDO) to produce a secondary core voltage (V_{CORE}) from the primary one applied to the device (DV_{CC}) which has wide range from $1.8V$ - $3.6V$. It generates the voltage from the (V_{CORE}) with up to four programmable output levels to provide for power optimization.

The PMM also includes supply voltage supervisor (SVS) and supply voltage monitoring (SVM) circuitry for (DV_{CC}) and (V_{CORE}) with programmable threshold levels, as well as brownout reset protection during device during power-on and power-off.

Watchdog Timer: The main purpose of the watchdog timer is to protect the system against software failures, such as the avoiding unintended infinite loops etc. The watchdog counts up and resets the MSP430 when it reaches its limit. Hence, the code must therefore keep clearing the counter before the limit is reached to prevent a reset.

Interrupts: Interrupts are asynchronous signals which cause a change to the normal flow of a software program. Interrupts are generally needed in time critical applications and the current application needs to be stopped and the interrupt needs to be attended to. Interrupts need to be enabled for them to be invoked. A simple example could be that an external ADC triggers an output indicating that a new sample is ready to be fetched, the microcontroller in this case should detect that change and read that new sample at that very instant. As a hardware system can have multiple peripherals which might need an interrupt, interrupts also need to have a priority in which they should be serviced; these can be configured in the firmware code. Interrupts can be generated by timers, ADC, I/O pins, DMA, watch dog, serial communication protocols etc.

Digital Input/Output: General purpose input/output pins on a microcontroller can be configured as either input or output using software. By default all pins are configured as inputs. Depending on the hardware some of these pins can be used to triggers interrupts. Specifically on the MSP430 only pins P1 and P2 can be configured for interrupts.

Configuration: Each of the I/O pins can be configured as output or input using software. They can also be used for performing special functions like timers, serial communication. In addition some of the pins can be used for generating inputs. The numbers of pins which can

generally generate interrupts are limited, for the MSP430F5525 only P1 and P2 can generate interrupts.

Direction of Registers (PxDIR): In order to configure the pins as output or input their direction needs to be defined which by default is set to input. Each bit in each PxDIR register is used to select the direction of the corresponding I/O pin. A bit of 0 configures the pin as input and a bit value of 1 configures the pin as output. NOTE: Writing to read-only registers PxIN registers results in increased current consumption while the write attempt is active.

Input Registers (PxIN) : These registers are read only and contain the value of the input signal at the corresponding I/O pin. A value of zero corresponds to a low input and a value of one corresponds to a value of high.

Output Registers (PxOUT): These registers are used to configure the corresponding I/O pin as a high or a low value. A value of zeros

Function Select Registers (PxSEL):I/O pins on the hardware can be used either for general I/O purposes or it can be used to serve peripheral module functions. By default I/O function is enabled and PxSEL is 0. To enable pin for peripheral module function PXSEL must be set to 1. One must note that PXSEL does not automatically set the pin direction. P1 and P2 interrupts are disabled when PxSEL is 1. When any PxSEL bit is set, the corresponding pins interrupt function is disabled.

Interrupts: Only pins P1 and P2 can generate interrupts which can be used in real time applications for processing inputs from external circuitry. Interrupts need to be enabled before they can be used.

Pin Interrupt Enable (PxIE) : This register is used to enable I/O interrupts. If any bit is set to one, interrupts corresponding to that I/O pin will be enabled provided global interrupts are enabled.

Pin Interrupt Edge Select (PxIES): Interrupt edge select is used to configure how the interrupt would be generated from the pin. If PxIES is set to zero interrupt is generate on low-to-high transition on the corresponding pin and one for a high-to-low transition

Pin Interrupt Flags (PxIFG) : An interrupt flag indicates whether an interrupt request has been served or it is still pending. Interrupt flag is set high when an interrupt is requested but has not yet been served. After the interrupt has been served this bit is cleared. This can also be changed through software. If any PxIFG flag becomes set during a Px interrupt the set interrupt flag

generates another interrupt.

Universal Serial Communication Interface: The MSP430 provides two universal serial communication interfaces :

USCI_A0 and USCI_A1: Each of these support enhanced serial universal asynchronous receive and transmit (UART) protocol with automatic baud rate detection, an IrDA Encoder and Decoder, and a synchronous serial peripheral interface.

USCI_B0 and USCI_B1: Each of these support serial inter-integrated circuit (I^2C) and synchronous SPI communication.

Direct Memory Access Controller: Direct memory access transfers or Direct Memory Access(DMA) is a common feature on modern microprocessors and personal computers which allows certain hardware subsystems within the computer to access system memory for reading and/or writing independent of the central processing unit (CPU). Microprocessors that have DMA channels can transfer data to and from devices with much less CPU overhead than those without a DMA channel. DMA transfers are commonly used in USB transfers, filter computations etc. The prototype uses single transfer mode for the DMA transfers. In this mode each byte transfer requires a separate trigger. The single transfer state is shown in Figure 3.15. The DMADT is zero for single transfer mode. The DMAxSZ register is used to define the number of transfers to be made. The DMADSTINCR and DMASRCINCR bits select if the destination address and the source address are incremented or decremented after each transfer. If DMAxSZ = 0, no transfer will occur.

The DMA source address (DMAxSA), destination address (DMAxDA), and size (DMAxSZ) registers are copied into temporary registers. The temporary values of DMAxSA and DMAxDA are incremented or decremented after each transfer. The DMAxSZ register is decremented after each transfer. When the DMAxSZ register decrements to zero, it is reloaded from its temporary register and the corresponding DMAIFG flag is set. In this mode the DMAEN bit is cleared automatically when DMAxSZ decrements to zero and must be set again for another transfer to occur. When DMALEVEL = 0, edge-sensitive triggers are used, and the rising edge of the trigger signal initiates the transfer while for level-sensitive triggers DMALEVEL should be set to one. DMA can be used for transferring data for many peripheral modules like timers, communication modules, ADC, DAC and hardware multipliers. A list of these is mentioned in table 3.1 with detailed descriptions.

The MSP430F5525 has 3 DMA modules: DMA0,DMA1,DMA2. DMA transfers are not interruptible by interrupts in general and the interrupt request remains pending until the DMA transfer is complete. DMA controller features in the MSP430F5525 include:

i) Up to three independent transfer channels
ii) Configurable DMA channel priorities
iii) Requires only two master clock/system clock (MCLK) cycles per transfer
iv) Byte or word and mixed byte/word transfer capability
v) Block sizes up to 65535 bytes or words
vi) Configurable transfer trigger selections
vii) Selectable-edge or level-triggered transfer
viii) Four addressing modes
ix) Single, block, or burst-block transfer modes

Universal Serial Bus: The MSP430F5525 provides a USB module which provides a full speed USB 2.0 specification support with baud rate of 12Mbps. The module supports full-speed operation of control, interrupt, and bulk transfers. USB can also be used as RAM, when not used for USB communication. USB protocols are complex and are not easy to implement. TI helps provides USB Communications Device Class (CDC) drivers in form USB CDC stacks. These CDC drivers make the USB appear up as a standard COM port on PC it is called a **Virtual COM Port**. COM ports are standard form of communication interfaces that provide an easy, quick setup for communication and are available on almost every computer. A virtual COM port on the other hand is a software emulation of an actual port, it can emulate all features of a serial port including, baud rate, data bits, parity bits, and stop bits. CDC uses bulk transfers, and provides a high bandwidth but requires a simple driver setup. TI also provides this USB CDC driver.

Joint Test Action Group (JTAG): In order to download the firmware on the MSP430, the code is written on the hardware's flash memory. There are three ways of programming the flash memory on the MSP430 namely the Joint Action Test Group i.e. the JTAG, the bootstrap loader using UART, and custom solutions using UART, SPI etc. The most common way is to use the JTAG interface.

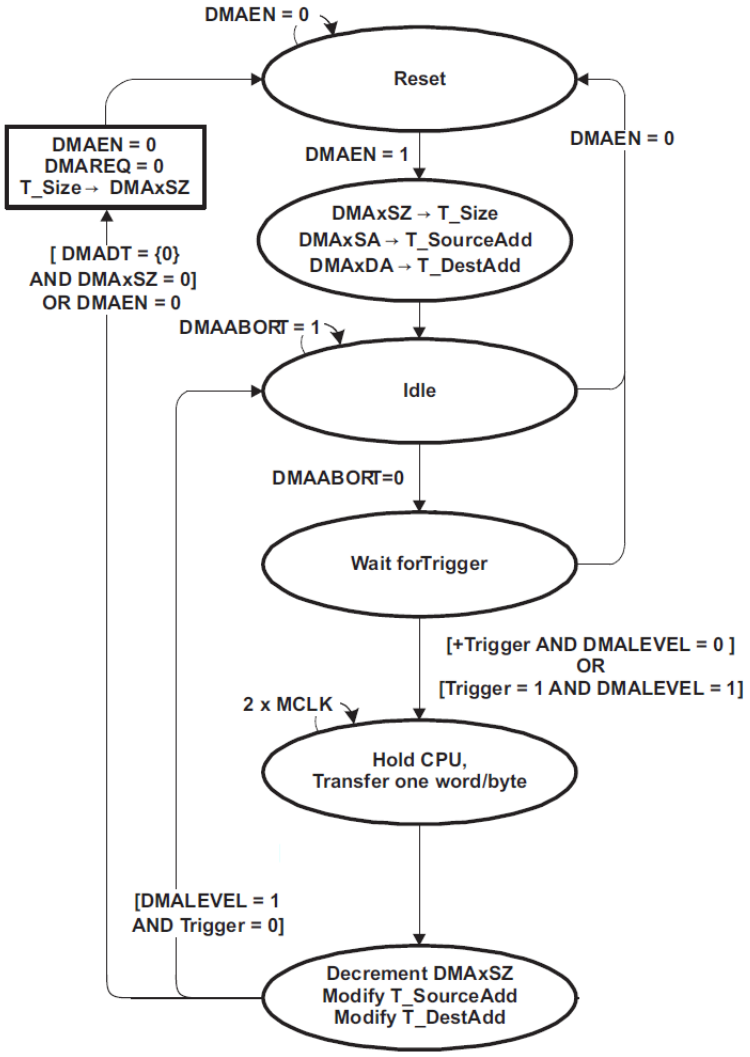


Figure 3.15: Flowchart for DMA transfer in single transfer mode

JTAG is the common name for IEEE 1149.1 Standard Test Access Port and Boundary-Scan Architecture. The JTAG was initially designed for testing printed circuit boards using boundary scan. Now it is also used for programming firmware and for accessing sub-blocks of integrated circuits to debug the system using single stepping and break pointing.

The standard JTAG interface requires four signals for sending and receiving data.

1. **Test Mode Select(TMS)**: This is an input signal which controls the JTAG state machine. The JTAG state machine can reset, access an instruction register, or access data selected by the instruction register.

2. **Test Clock (TCK)**: This signal is the clock input. On every clock pulse one bit data is transferred in and out of the TDI and TDO pins respectively.

3. **Test Data In (TDI)**: Test data in is the JTAG data input. This data must meet the setup and hold times. It also serves as the t_{CLK}input. t_{CLK}signal is an input clock, which is provided to the target device from an external source. This clock is used internally as the target device's system clock, MCLK, to load data into memory locations and to clock the CPU.

4. **Test Data Out (TDO)** : Test data out is JTAG data output, which is received after the falling edge of the TCK.

3.3 Isolation Circuitry: Power and USB:

Chapter 2 discussed the need for isolation circuitry to keep the subject safe from any electrical shocks and hazards. The prototype hardware utilizes the latest power isolation circuitry and USB isolation from Analog devices. [24, 23]

Power Isolator ADuM5000 : The prototype utilizes an Analog Devices isolated DC-to-DC converter ADuM5000 for supplying isolated power to the analog front-end for human safety. The dc-to-dc converter in this device provides regulated, isolated power in several combinations of input and output voltages 5 volts to either 5V or 3.3V and 3.3V to 3.3V. It has a secondary side controller which regulates the output voltage to either 3.3V or 5V using an isolated pulse-width modulation (PWM) feedback to the primary input voltage (V_{DD1}) side. This feedback in-turn provides higher power and efficiency. It provides a V_{DD1} input protection circuit which only enables the converter when the input voltage rises above the under voltage lock out (U_{VLO}) value. ADuM5000 chip support isolation voltage of 2500 V_{rms} for 1-minute duration.

USB Isolator ADuM4160 : The MSP430 microcontroller which provides USB support only presents the D+ and D- lines to the external pins for minimizing external components and simplifying the design. USB lines must automatically switch between actively driving D+ / D-, receiving data, and allowing external resistors to set the idle state of the bus. USB isolation in the D+/D- lines is challenging because the access to the output enable signals is required to control a transceiver and the isolator must know when to enable or disable the upstream and

down-stream output buffers and at the same time maintaining precise timing. A USB digital isolator ADuM4160 is used to transfer data between the microcontroller and a PC with up to 12 Mbps transfer speed. The ADuM4160 uses the edge detection and some logic to implement an isolator. It also detects the direction of data flow packet-wise and controls the state of the output buffers. It operates with the bus voltage on either side which ranges from 4.5 V to 5.5 V, and allows connection to V_{BUS} by regulating the voltage to the signaling level. ADuM4160 chips support isolation voltage of 5000 V_{rms} for 1-minute duration.

Chapter 4

Firmware Design

Firmware is a program or a piece of software code written to internally control electronic devices. Devices containing firmware range from remote controls, calculators, memory cards and even industrial robots, cameras and mobile phone. Firmware coding is mainly written in low level assembly language which is hardware dependent and also in high level language like C to speed up the development process. This chapter will start off with a description of the firmware design for the MSP430F5525 which was entirely coded in C language. Texas Instruments USB CDC stacks were used for rapid USB firmware development. This chapter discusses the firmware code design in detail. As discussed in Chapter 3, the communication between the ADS1298 and the microcontroller is accomplished using a SPI. For achieving maximum efficiency, direct memory access transfers have been set up to receive conversion data from the front-end to be sent to the computer. Communication between the microcontroller and the computer is done through a standard USB connection. The microcontroller is programmed and configured as a USB CDC device (USB Communication Device Class), that can be recognized as a Virtual COM-port device, which can be easily accessed from within a variety of operating systems, such as Windows, Linux, and Mac OS, and software packages including MATLAB/Simulink, LabVIEW and C/C++. The next section discusses an example of the software design for acquiring data using National Instruments LabVIEW software and processing that data using MATLAB.

The overall firmware design has been written in C and provides ease of modification of code. To maximize efficiency in receiving conversion data from the ADS1298 DMA transfers have been set up for SPI communication.

4.1 Programming the device

For programming firmware onto hardware special circuitry is required to download and store the code inside the device. The MSP430 provides flash memory and all the code is written in the flash memory. The code is retained even if the power supply is removed and the device is unplugged because flash memory is non-volatile. For in-circuit programming the device makes use of standard 4 pin JTAG circuitry to download and debug the code. For programming, the IAR embedded workbench and a USB field effect transistor MSP430 USB-Debug Interface MSP-FET430UIF were used. The MSP-FET430UIF includes USB debugging interface, used to program and debug the MSP430 in-system through the JTAG interface. The flash memory can be erased and programmed in seconds. Figure 4.1 shows a picture demonstrating how to program the device. [25, 11]

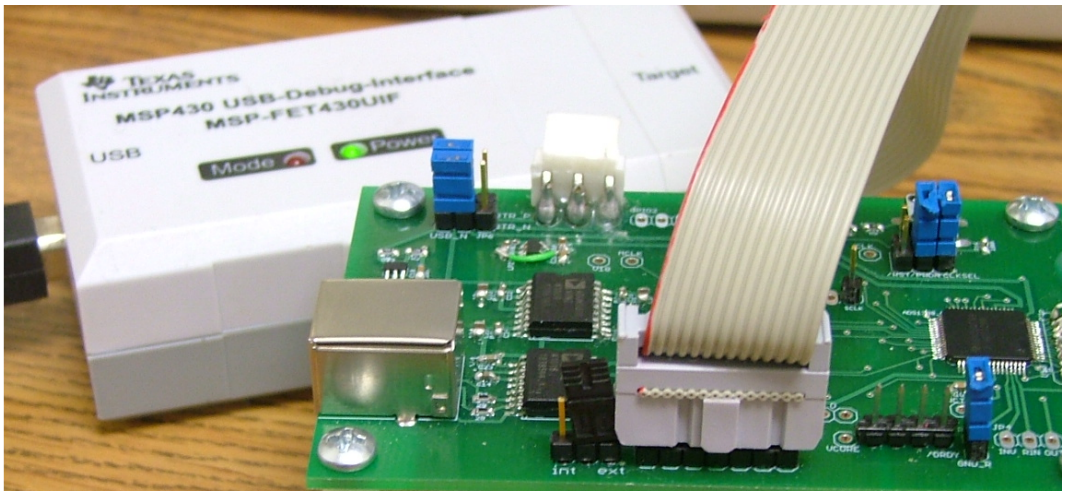


Figure 4.1: Programming the hardware using the MSP430 USB Debug-Interface MSP-FET430UIF using a 14 pin connector

4.2 Code Design

The flow of the firmware is shown in flowchart shown in Figure 4.2. This flowchart summarizes the firmware code design for the MSP430 microcontroller. A control application has been developed on the MSP430F5525 with the aid of TI USB CDC stacks for rapid USB development. The following paragraphs discuss in details the firmware design.

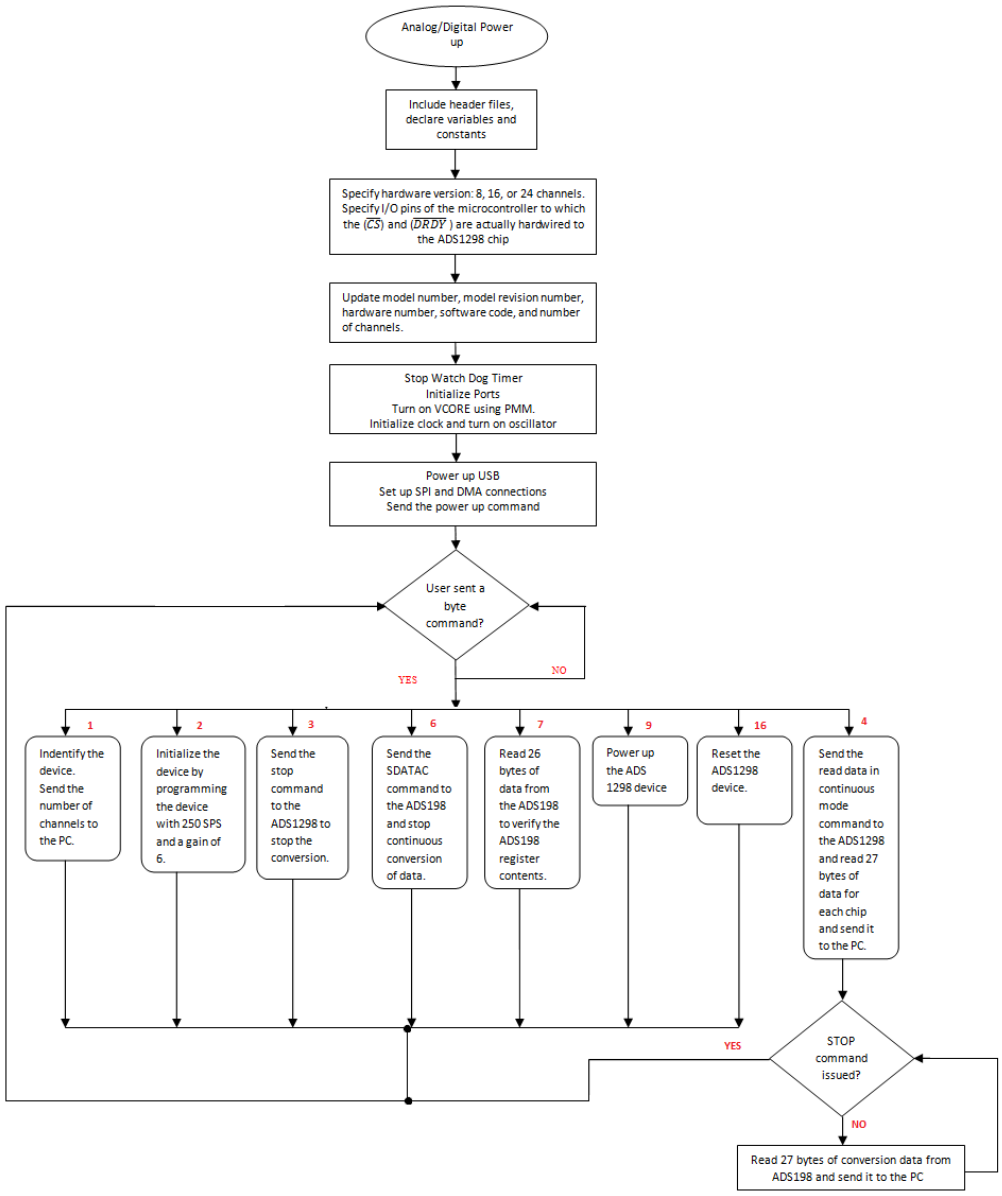


Figure 4.2: Flowchart summarizing the various series of operations of the ADS1298

Stopping Watchdog Timer

The operation of the watchdog is controlled by the 16-bit register WDTCTL in the MSP430F5525. It is guarded against accidental writes by requiring the password WDTPW = 0x5A in the upper byte. A reset will occur if a value with an incorrect password is written to WDTCTL. The

lower byte of WDTCTL contains the bits that control the operation of the watchdog timer. The WDTHOLD pin is pulled high to disable the watchdog timer.

Command	**Code**
Identify	0x01
Initialize	0x02
STOP	0x03
RDATAC	0x04
SDATAC	0x06
RREG	0x07
POWER UP	0x09
RESET	0x10

Table 4.1: Table shows the code word for performing the various commands

WDTCTL = WDTPW + WDTHOLD; // Stop watchdog timer

Initialize Device

To initialize the device first the unused pins must be made output low.

PxOUT = 0x0000;

PxSEL = 0x0000;

PxDIR = 0xFFFF;

Next using the power management module must be set the V_{CORE} voltage. Table 4.1 shows the relationship between the device voltage DV_{CC} voltage and the clock frequency based on which the PMMCOREVx settings are changed and the V_{CORE} voltage is set up. The universal clock system is used to enable the crystal XT2 and set clock frequency to that specified by USB_MCLK_FREQ in descriptors.h. For this application a system clock of 16MHz is utilized.

USB CDC code is used for all function related to USB which include enabling USB, sending, and receiving data from host(the MSP430) to the user. TI also provides us with USB CDC drivers which needs to be installed for USB communication. Using these files the USB is initialized and enabled. Finally the SPI and DMA connections are set up.

The USCI_A0 SPI communication interface and DMA0 and DMA1 are used for SPI transmit and receive operation respectively. A 4 pin master mode SPI connection is used, with MSB sent first, clock polarity high and clock phase low. The source the clock for this SPI communication is the SMCLK and divide by factor is controlled by UCA0BR0=4.

$\mathbf{f_{SYS}}$ **max in MHz**	$\mathbf{DV_{CC}}$ **in V**	**PMMCOREVx settings**
8	> 1.8	00
12	> 2.0	01
20	> 2.2	10
25	> 2.4	11

Table 4.2: Table shows the value of PMMCOREVx for given max system clock frequency and the device voltage (DV_{CC})

```
//Select SPI pins
P3SEL | = BIT3+BIT4; // P3.3,4 option select
P2SEL | == BIT7;


//Set up SPI
UCA0CTL1 | = UCSWRST; // **Put state machine in reset**
UCA0CTL0 | = UCMST+UCSYNC+UCMSB;


// Clock polarity high, MSB
UCA0CTL1 | = UCSSEL_2; // SMCLK
UCA0BR0 = 0x04; // SPI CLK = SMCLK (16 MHz)/UCABRO(4) = 4MHz
UCA0BR1 = 0;
UCA0MCTL = 0;// No modulation
UCA0CTL1 & = ~ UCSWRST; // **Initialize USCI state machine**
```

For efficient SPI communication DMA transfers have been set up for SPI communication . A transfer is triggered when USCIA0 receives new data. UCA0RXIFG is automatically reset when the transfer starts. A transfer is triggered when USCIA0 is ready to transmit new data. UCAx-TXIFG is automatically reset when the transfer starts. The DMA is used in a single byte, single transfer mode. The DMA code snippet is shown below.

```
// Set up DMA transfers for SPI
DMACTL0 = DMA1TSEL_16+DMA0TSEL_17;
// DMA0 - UCA0TXIFG
// DMA1 - UCA0RXIFG
```

```
// DMA0 setup
DMA0CTL = DMADT_0 | DMADSTINCR_0 | DMASRCINCR_0 | DMADSTBYTE |
DMASRCBYTE | DMALEVEL;
DMA0SA = (unsigned long)&Txstring
DMA0DA = (unsigned long)&UCA0TXBUF
DMA0SZ = 1;
Txstring=Rxstring=0;
// DMA1 setup
DMA1CTL = DMADT_0 | DMADSTINCR_3 | DMASRCINCR_0 | DMADSTBYTE |
DMASRCBYTE| DMALEVEL;
DMA1SA = (unsigned long)&UCA0RXBUF
DMA1DA = (unsigned long)&Rxstring;
DMA0SZ = 1;
```

A control application has been developed in inside function rx_data. This function keeps waiting for a receive from the user. This input is decoded to perform the required operation as requested. The function rx_data provides the following options namely Identification, Initialization, Serial number storing, reset, powering up, programming, reading registers, stopping continuous read data conversion, stopping conversion, read conversion data in continuous mode. The following subsections will discuss them in detail.

Identification

When a command of 0x01 is received from the user. The MSP430 returns the number of analog channels on the chip in turn identifying the chip.

Reset

When a command 0x10 is received from the user. The MSP430 resets the ADS1298 chip by sending the reset opcode using SPI communication. The pseudo code is given below, Bank_CS contains the pin number where chip select for the device is connected. To enable the device first the ($\overline{CS}$) must be pulled low and then the opcode must be sent.

```
//Enable Chip
```

```
    P1OUT &= ~Bank_CS;

// Send RESET opcode
    UCA0TXBUF = 6;

// Wait for code to be sent
    while (!(UCA0IFG&UCRXIFG))
    {
     dummy=dummy+1;
    }

// Disable the chip
    P1OUT |= Bank_CS;
```

Stop

Similarly when a command 0x03 is received from the user. The MSP430 stops the ADS1298 chip conversions by sending the stop opcode 0x0A using SPI communication i.e. UCA0TXBUF is set to 0x0A. Bank_CS contains the pin number where chip select for the device is connected. To enable the device first the ($\overline{CS}$) must be pulled low and then the opcode must be sent.

Stopping Continuous Conversions: SDATAC

When a command 0x06 is received from the user. The MSP430 stops data read continuous mode by sending the SDATAC opcode 0x11 using SPI communication.

Initialization

When a command 0x02 is received from the user. The MSP430 sends the SDATAC opcode. Next registers are written and the ADS1298 chip is programmed by sending the WREG opcode and writing the registers using SPI command for 250 SPS data rate, gain=6(default). The Register Write command is a two-byte opcode followed by the input of the register data. The first byte contains the command opcode and the register address. The second byte of the opcode specifies the number of registers to written -1. The WREG register can program maximum 25 registers in

total which have been discussed in detail in chapter 3. The starting register to be written need not always be the first one, and this can be changed.

```
//Enable Chip
P1OUT &= ~Bank_CS;

// Write WREG_SIZE registers based on register values
while (TXcount <WREG_SIZE)
{
 UCA0TXBUF = TX_WREG_MASTER[TXcount++];

// Wait till next byte has been sent
 while (!(UCA0IFG&UCRXIFG))
 {
 dummy=dummy+1;
 }
 dummy=UCA0RXBUF;
}

// Disable the chip
P1OUT |= Bank_CS;
```

where TX_WREG_MASTER = 0x41, 0x18, 0x66, 0, 0xCC, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0x0F, 0, 0, 0, 0, 0

Writing Registers: WREG

The firmware provides the user to choose from different sampling frequency values and programmable gain values. The following options have been provided.

Code in decimal		**Sampling Frequency**				
		250	500	1k	2k	4k
Gain	6	0x80	0x82	0x84	0x86	0x88
	12	0x81	0x83	0x85	0x87	0x89

Table 4.3: Code to be sent to the MSP430 to decode the sampling rate and programmable gain.

Power up the ADS1298

When a command 0x09 is sent from the user to the MSP430 the ads1298 goes through power up. This function powers up the master device using WREG command required when other chips are slaves and external clock is not used.

Read Registers: RREG

The RREG command is used to read the values of the ADS1298 registers. It can be used to verify whether the ADS1298 chip has been programmed properly or not. When the users send a command 0x07 to the microcontroller, the RREG opcode is sent to the ADS1298. The data output received is a 26 byte data.

Read Data in Continuous Mode: RDATAC

RDATAC mode is used to read the conversion data from the ADS1298 continuously. When a command 0x04 is send to the device the hardware sends the START opcode, followed by the RDATAC opcode to the ADS1298 chip. The received data can be stored to disk or processed for visualization in real time in LabVIEW, Simulink, or any other software environment.

The timing budget: RDATAC function uses continuous SPI transmissions from the microcontroller to the ADS1298. For achieving maximum efficiency this is done using DMA transfers. Each DMA byte transfer takes 2 MCLK cycles to be completed. MCLK frequency being set to 16MHz, and SCLK at 4MHz, by end of 4MCLK or 8 SCLK cycles 1 byte data would be received from the microcontroller which is 2μs. For 27 bytes of DOUT this equals 54μs+4t$_{CLK}$=55.95μs, which implies maximum possible theoretical sampling rate of 18kSPS. For a 16 channel system this would be 108μs+4t$_{CLK}$=9kSPS, and 4.5kSPS for a 24 channel system. The flow of the RDATAC command is described in the code snippets below.

```
//Enable Chip
P1OUT &= ~Bank_CS;


// Send 2 opcode bytes first start and then rdatac opcode
while (TXcount<2))
{
 UCA0TXBUF = TX_RDATAC[TXcount++]
```

```
// Wait till transfer ends

while (!(UCA0IFG&UCRXIFG))
{
dummy=dummy+1;
}
dummy=UCA0RXBUF;
}
TXcount=0; // Disable the chip
P1OUT | = Bank_CS;
```

Now the ($\overline{DRDY}$) pin should go high for some time, otherwise there is an error. Now wait for the next DRDY transition from high to low and enable the DMA transfers for starting SPI communication. After receiving all 27 byte data, the data is sent to PC and this repeats after every ($\overline{DRDY}$) transition until a stop command is sent.

```
//Check /DRDY0 Pin (Should be High)

if (!(P1IN & Bank_DRDY)
send_error();
while(!(P1IN & Bank_DRDY))
{
dummy=dummy+1;
}

//Wait for (DRDY) transition (High –> Low)
while((P1IN & Bank_DRDY))
{
dummy=dummy+1;
}
```

```
while(count<27)
 {
 DMA0CTL | = DMAEN;
 DMA1CTL | = DMAEN;
 while (DMA1CTL&DMAEN!=0);)
 count++;

// STORE DATA
if((count>0)&&(count<28))
DOUT[count-1]=Rxstring;
 }

// Check for stop command
USBCDC_receiveData(RXdata,1,1); // Check STOP command //
if (RXdata[0]==STOP)
 {
UCA0TXBUF=10;
stop=1;
i=0;
break;
 }
if(count==27)
sendData_inBackground(DOUT,27,1,1);
```

4.3 Software setup

National Instruments LabVIEW software was used to program the registers of the ADS1298 and receive conversion data from it using the MSP430 in real time. Care was taken while writing the software to avoid any sample drops. The internal counter was monitored to check for any sample losses. Robustness tests have been conducted by recording data over several days to check for

possible system crashes or sample drops. Using LabVIEW all the conversion data can be written to a binary file which was accessed later for easy data analysis, processing, and visualization.

Chapter 5

Experimental Setup and Results

This chapter will discuss the experimental setup used for the recordings conducted which include both solid state, and biological recordings. Following the experimental setup, the next section covers performance comparisons between the prototype amplifier and the clinical grade g.USBamp available from Guger Technologies [26].

5.1 Experimental Setup

This section describes in detail the experimental setup which was used in the following recordings for both the prototype amplifier and the g.USBamp. For all biological recording electrodes from the scalp were connected to the analog inputs on the amplifier board after first connecting the ground, and the reference electrodes. The amplifier was connected to the computer using a USB 2.0 port, and interfaced using MATLAB/Simulink environment or LabVIEW for real-time data acquisition. The data was recorded at 256 samples per second from the g.USBamp and at 250 samples per second from the prototype amplifier. In order to directly compare the signal quality with a commercially available unit, data was recorded from both the Prototype amplifier and a g.USBamp sequentially from the same source and subject by unplugging the leads from one amplifier and connecting them to the other. For biological recordings, electrodes from the subjects scalp for biological recordings were not disconnected and the leads from one amplifier were connected to the other. The subject did not move substantially in position between recordings, and the two amplifiers were kept next to each other on the same table behind the subject. The figure

below shows the experimental setup for human EEG recordings using the prototype amplifier or g.USB amplifier and interfacing in Matlab/Simulink environment or LabVIEW environment.

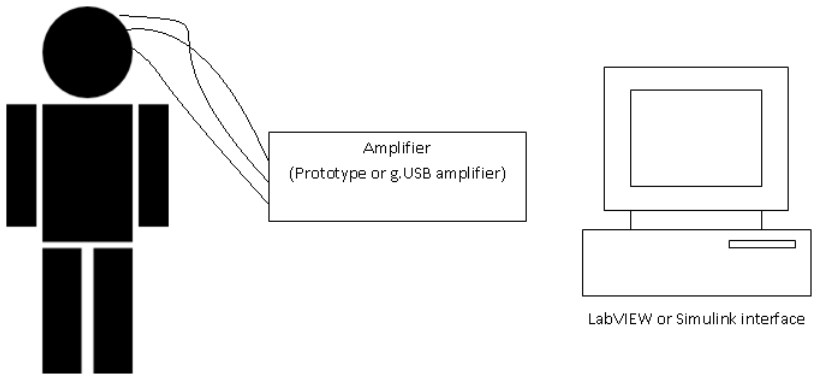


Figure 5.1: Figure shows the experimental setup for human EEG recordings using the prototype amplifier or g.USB amplifier and interfacing in Matlab/Simulink environment or LabVIEW environment.

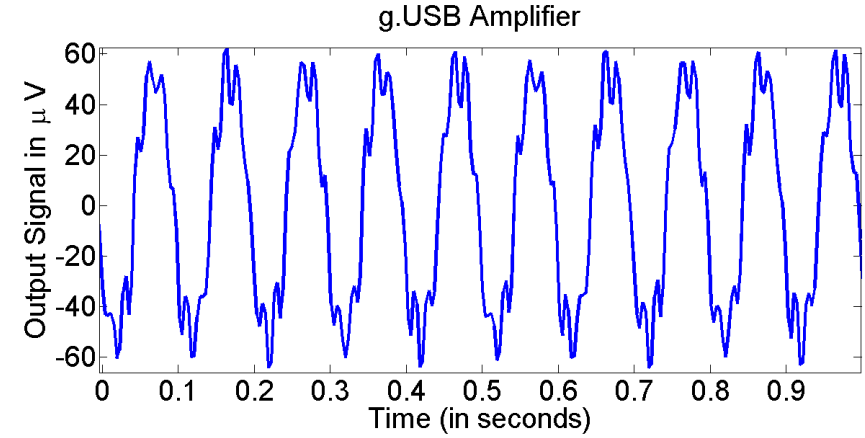
5.2 Results and Validation

In this subsection the results of the prototype acquisition hardware are described and a head to head comparison with the clinical grade g.USBamp is done. In order to directly compare the signal quality with a commercially available unit, data was recorded from both the Prototype amplifier and a g.USBamp sequentially. These comparisons have been demonstrated with a low input impedance waveform generator, passed through an isolation amplifier and a voltage divider for EEG recordings during eyes closed and eyes open conditions. Further comparison of the internal noise levels, and aliasing effects has been conducted. Finally, a P300 based BCI application has been developed which demonstrates its use as a low-cost research and teaching tool.

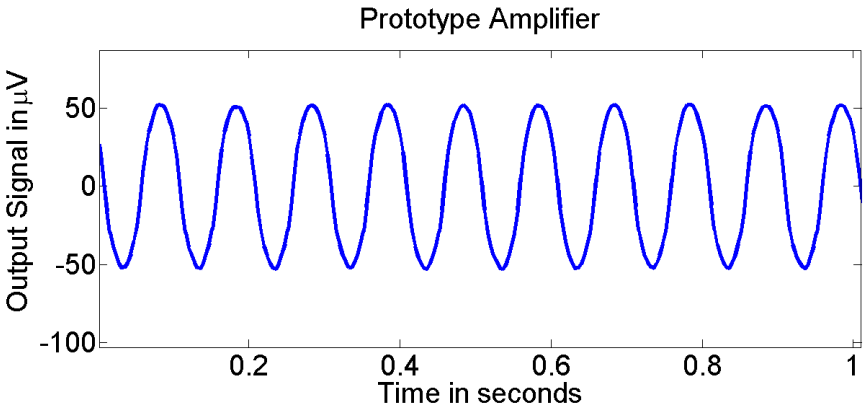
5.2.1 Solid State Signals

In this subsection the two acquisition systems' performance has been compared using a output from a waveform generator passed through a voltage divider. The recordings was done simultaneously from the two amplifiers. The input from the signal generator was a 10Hz, 50mV_{pp} sine wave which was passed through a voltage divider of 1000. Figure 5.2 shows the comparison

between the signal recorded from the prototype amplifier at 250 samples per second and from the g.USB amplifier sampled at 256 samples per second. Later a digital high pass filter at 0.5Hz was applied for visual purposes The signal on the prototype amplifier is much cleaner than the signal from the g.USBamp. Figure 5.3 shows the corresponding average power spectral density calculated using Pwelch method. The prototype amplifier has clearly lower 60Hz noise compared to the g.USB amplifier. Also the g.USB amplifier has other noise at 60±16Hz which is not present on the prototype amplifier.



(a) g.USBamp



(b) Prototype Amplifier

Figure 5.2: Comparison of a 10Hz sinusoid as measured with (a) the g.USBamp sampled at 256 samples per second (b) the prototype amplifier sampled at 250 samples per second. The only filtering involves in both these plots is a 0.5Hz high pass filter in software for visual purposes.

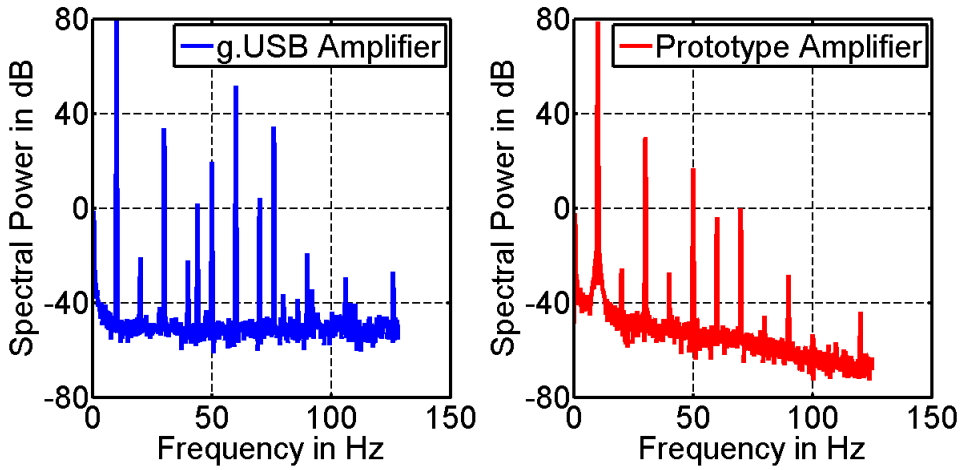


Figure 5.3: Comparison of the average power spectral density calculated using Pwelch method for the 10Hz sinusoid as measured with (a) the g.USBamp sampled at 256 samples per second (b) the prototype amplifier sampled at 250 samples per second. The only filtering involved in the raw data in both these plots was a software 0.5Hz high pass filter for visual purposes.

5.2.1.1 Noise Tests

In this subsection a comparison of the internal noise levels on the prototype amplifier and the g.USB amplifier has been conducted. These tests are important to determine whether the EEG signal is being measured with high fidelity.

5.2.1.2 Internal Noise Test

In these recordings both the systems acquire the data from one channel, with the reference, ground, and input to the channels were connected to each other externally using jumpers. The data from the prototype amplifier was recorded at 250SPS and from the g.USBamp at 256 SPS. The observation here is that the internal noise levels on the prototype amplifier range around $4\mu V_{pp}$ when input was recorded at 250 samples per second and data from one channel, with the reference, ground, and input to the channels were connected to each other externally using jumpers, compared to $6\mu V_{pp}$ on the g.USBamp. under same conditions with data sampled at 256 samples per second. The prototype amplifier has much lower internal noise level when compared with the g.USBamp. The g.USB amp has noise at 60±16Hz and significant noise at 90Hz which is not present on the prototype amplifier.

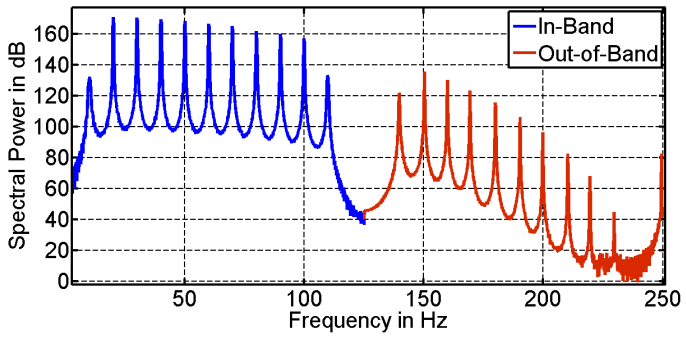


Figure 5.4: The power spectral density of in-band signal (20Hz-100Hz) Vs out-band signal (150Hz-230Hz) calculated using Pwelch for 5 second windows with half overlap

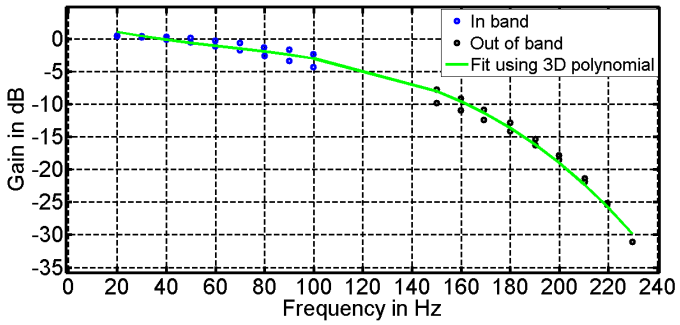


Figure 5.5: The gain in dB of in-band signal (20Hz-100Hz) Vs out-band signal (150Hz-230Hz) calculated using Pwelch for 5 second windows with half overlap, fitted using a 3D polynomial

5.2.1.3 Aliasing

In this subsection aliasing effects on the prototype amplifier were observed. Sweeping input of 50mVpp were fed from the waveform generator, with in-band frequencies from 20Hz-100Hz in steps of 10Hz and out-band frequencies from 150Hz-230Hz in steps of 10Hz. The following plots show the gain of the aliased waveforms. Data was sampled at 250Hz on the prototype amplifier, and the spectral densities were calculated using the Pwelch method for 5 second windows with half overlap. The plots below show the gain during in-band and out-band frequencies and corresponding fits of gain using a standard 3d polynomial fit, and the ADS1298 sinc filter gain equation. Chapter 2 described the that the ADS1298 consists of a third-order sinc filter on each channel, which is basically a variable decimation rate, third-order, low-pass filter. Data are supplied to this section of the filter from the modulator at the rate of f_{MOD} and the sinc filter attenuates the high-frequency noise of the modulator, then decimates the data stream by factor

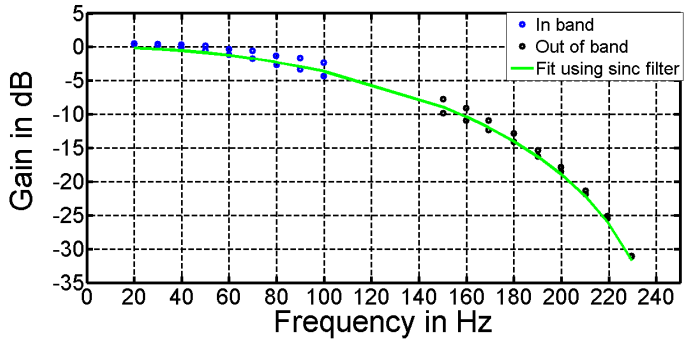


Figure 5.6: The gain in dB of in-band signal (20Hz-100Hz) Vs out-band signal (150Hz-230Hz) calculated using Pwelch for 5 second windows with half overlap, fitted using the sinc filter transfer function of the analog front-end.

N into parallel data. The frequency domain transfer function of the sinc filter is shown in the equation below:

$$\mathrm{H(f)}= \left| \frac{\sin\left(\frac{N\pi f}{f_{MOD}}\right)}{N \times \sin\left(\frac{\pi f}{f_{MOD}}\right)} \right|^3$$

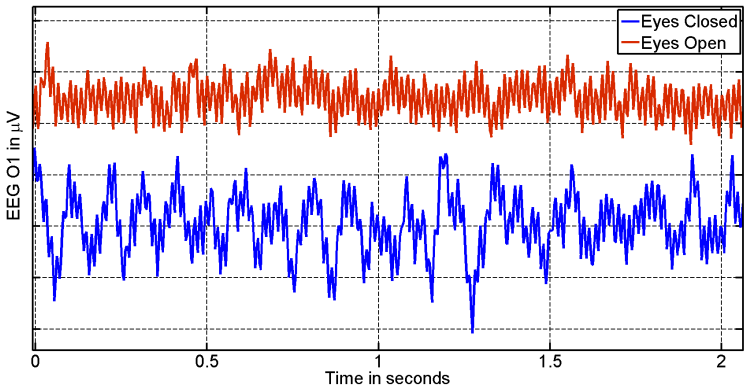
These plots clearly demonstrate that there is no aliasing, occuring with the prototype amplifier.

5.2.2 Biological Signals

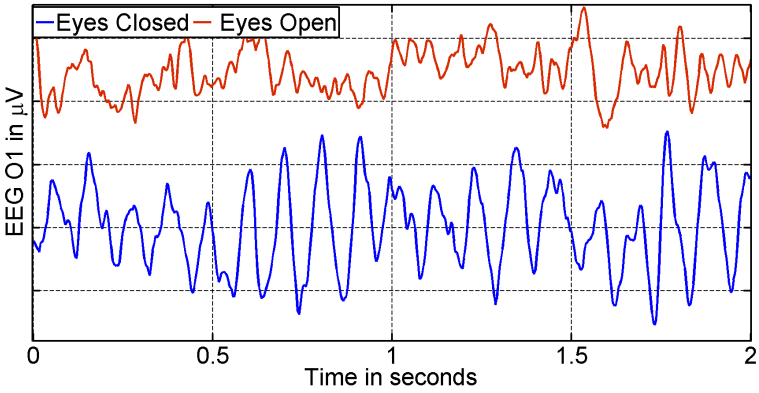
In this subsection tests results are summarized from recordings conducted from the human scalp, recorded from the prototype amplifier. A head to head comparison is done with a g.USB amp. Finally a P300 BCI application is developed and EEG recordings are conducted using the prototype amplifier. These results are summarized below.

5.2.2.1 EEG quality comparison

In order to directly compare the signal quality with a commercially available unit, data was recorded from both the Prototype amplifier and a g.USBamp from human biological signals, sequentially by unplugging the leads from one amplifier and connecting them to the other without removing the electrodes from the subjects scalp. The subject did not move substantially in position between recordings, and the two amplifiers were kept next to each other on the same table behind the subject. During the recording period, the subject was asked to spend consecutive one-minute periods in eyes-open then eyes-closed rest conditions. Short examples of EEG during



(a) g.USBamp



(b) Prototype Amplifier

Figure 5.7: Comparison of two seconds of eyes closed and eyes open recording of EEG signal from O1 referenced to CPz from (a) the g.USB amplifier sampled at 256 samples per second. Highly noise contaminated alpha waves are clearly observed during eyes closed.(b) the prototype amplifier sampled at 256 samples per second. Alpha waves are clearly observed during eyes closed condition. The only filtering involved is a 0.5Hz high post processing filter for visual purposes. EEG grid spacing is 20μV in each case.

eyes open and eyes-closed rest conditions are shown in Figure. 5.7, recorded from one subject from O1 referenced to CPz. This data was acquired with a sampling rate of 250 samples per second (SPS) from the prototype amplifier and at 256 samples per second from the g.USB amplifier. It should be noted that neither system utilized any other filtering than their inherent anti-aliasing filters and the post-processing-applied 0.5 Hz filter. Figure 5.8 the spectral power densities for these high-pass filtered recordings are shown. An averaging operation was performed over the

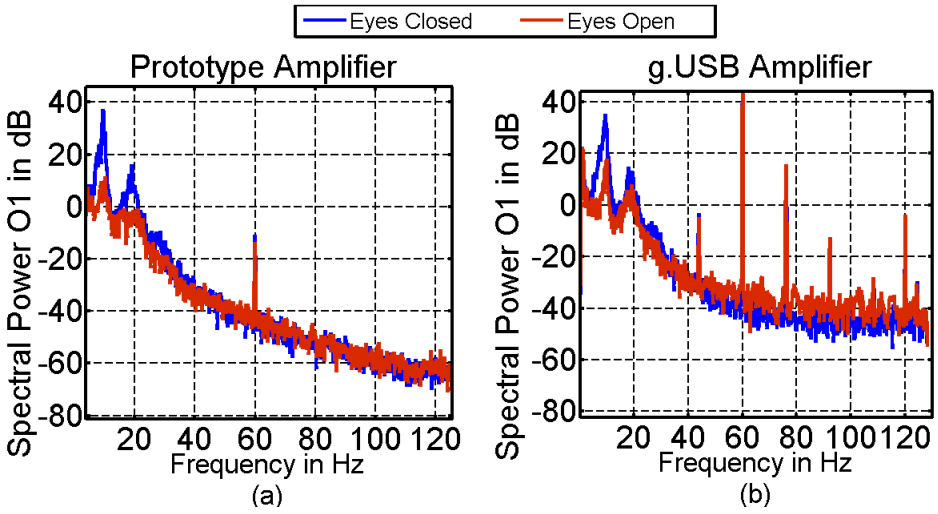


Figure 5.8: Comparison of average power spectral density using Pwelch method for sixty second periods from O1 referenced to CPz for eyes closed and eyes open using (a) the prototype amplifier sampled at 250 samples per second. (b) the g.USB amplifier sampled at 256 samples per second. The only filtering involves in both these plots is a 0.5Hz high pass filter in software for visual purposes. The 60Hz noise on the prototype amplifier is an order of magnitude lower than on the g.USBamplifier. Also the low frequency components of both the recordings match in distribution and magnitude.

full 60-second periods of same behavioral condition. It is clear that there is very little 60 Hz contamination of these signals in the raw traces and in the spectra. Also the low frequency components match approximately in distribution and magnitude. The g.USBamp has a much higher 60 Hz line noise, along with substantial additional harmonics and shoulder frequencies at $\simeq 60 \pm 16$ Hz. The background noise level on the g.USBamp appears to be about an order of magnitude higher than that for the prototype amplifier at the highest frequencies. [10]

5.2.2.2 Brain Computer Interface Recordings

An introduction to brain computer interface recordings has already been given in chapter 2. This sections demonstrates the use of the prototype hardware using the well established visually evoked P300 paradigm. Within an educational course, for a BCI choice system, students learn to detect in real time the visually evoked potential and discriminate from the presence or absence of the P300 which target the subject chose. In order to learn how to do so, and to determine the difference between the Choice and Not-Choice evoked potentials for a particular subject, is done typically by having the subject focus on a prescribed (and known to the analyzer) ordering of targets. The results of recordings and analysis from such a training period, for a user not already

well trained in the use of a P300 choice BCI have been presented. A pick 1 out of 8 targets paradigm was presented to the subject (illustrated in Figure. 5.9). [19, 9, 10]

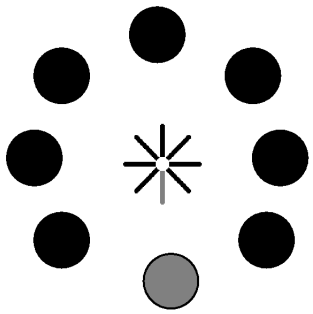


Figure 5.9: Pick 1 out of 8 targets paradigm. Modified from the Farewell and Donchin P300 speller for a period of 80ms each and an inter-stimulus interval of 120ms

The targets are flashed in random order for a period of 80ms each and an inter-stimulus interval of 120ms, while the indicator in the center instructs the subject which target to choose. It has been shown that to achieve a better classification on a trial to trial basis one must average over at least 2 presentations of each target in order to reduce variance and ensure the user didnt momentarily lose concentration during the presentation of the stimuli. In one trial, 3 presentations for each target were averaged, with a total of 40 trials in one recording session. Visual presentation as well as data acquisition was performed within the Simulink coding environment through a virtual COM port. Care was taken to track and minimize phase delays between when samples were taken vs. when they are analyzed in the code. The internal counter on the MSP430 was tracked to check for any sample drops. The data was recorded from one subject with almost no BCI training, from channels CPz, P3, P4, Pz, PO7, PO8, O1 and O2, with Cz as both reference and ground. These channels were chosen because visually evoked potentials are best observed at the occipital lobes. The incoming signal was sampled at 250 SPS using the Prototype amplifier. Data analysis included the following steps. First, all data was filtered using 5th order butter-worth filter with pass-band of 1-30 Hz. A common spatial pattern (CSP) filter was applied to the data [27, 28]. The CSP aims to create spatial mixtures of the channels under the assumption that the data comes from different sources that have different activations. Here these are represented by times of Choice (having both visual evoked potential and P300), and time of Not Choice (having just visual evoked potential). The evoked responses average for all Choice

and all Not Choice stimuli are shown in Figure. 5.10

One should note that the large difference near 300 ms post-stimulus time for those stimuli

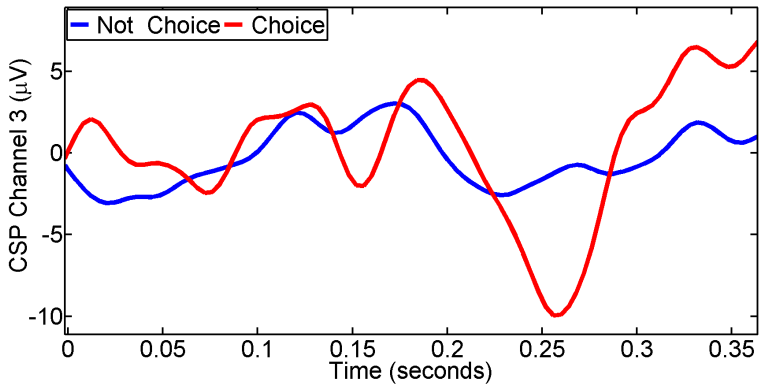


Figure 5.10: Visually Evoked Potential for Choice and Not-Choice targets averaged over 40 trials. Notice the large peak approximately 260 ms after the stimulus for Choice target stimuli

associated with Choice targets. In order to create a BCI discrete choice system, one needs to discriminate on a trial-by-trial basis which target was chosen. To do this, the data is downsampled by a factor of 10, and Fisher's linear-discrimination analysis (LDA) is used to separate the Choice from Not Choice evoked potentials. To further test the performance of this discrimination, the trials are separated in to training and testing trials to prevent over fitting of the data for good predictive discrimination.

Shown in Figure. 5.11 are the histograms of LDA values for the out-of-sample evoked potentials for Choice and Not Choice targets (the groups are well separated). An approximately 80% correct identification of the Choice target was observed. This reflects good performance for a first training set from an un-trained user.

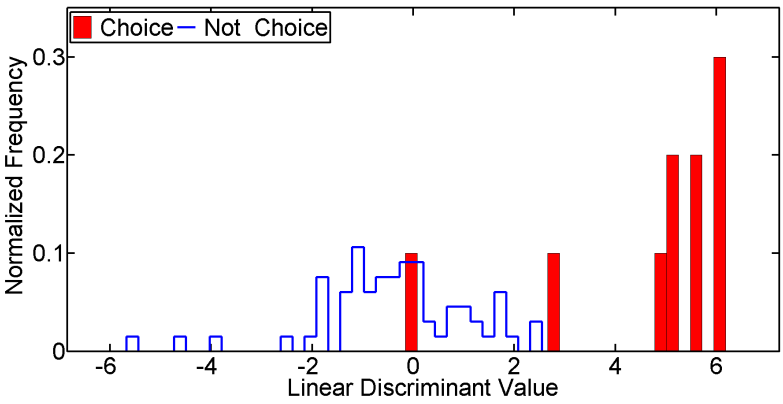


Figure 5.11: Classification of Out-of-sample Trials. Shown is the histogram of LDA values for Choice and Not-Choice evoked potentials for out of sample data (25%). The groups are well separated, and yields $\simeq 80\%$ correct identification of the chosen target

Chapter 6

Discussion and Future work

This thesis has demonstrated the development of a low-cost, light weight, high performance biopotential amplifier for neural recordings. The amplifier recordings have been tested and compared with clinical grade amplifiers and noise and robustness tests have been conducted. The prototype can record EEG data with high fidelity as shown in chapter 5. The cost is low enough for individual purchase by students in a BCI or other EEG related course. The prototype will aid in easy availability of instrumentation hardware to aspiring seniors and graduate student researchers. Since the hardware is built in house students/researchers will have a better idea of the possibilities and limitations of the hardware. They can post-process this data keeping these factors in mind and would able to troubleshoot hardware problems quickly, which would lead to increased productivity.

The prototype amplifier still has scope for further improvements. The following sections will discuss the possible extensions of this work.

Impedance Monitoring : First, and foremost this device needs to have skin electrode impedance measuring device which it is not capable of at this stage, as discussed in chapter 2, skin electrode impedances need to be monitored continuously to check for possible bad electrode connections, in both rodent and human recordings. Texas instruments new analog front-end ADS1299, to be launched in late 2011 or early 2012 would take care of these needs. This will only require a minor firmware and hardware re-design.

Higher common mode rejection ratio: Using right leg drive circuitry for measuring

the EEG signal can aid in lowering the common mode signal. By enabling RLD signals and description in chapter 3, this can be achieved.

Wireless: The development of a wireless solution will help eliminate long wires and make the subject more mobile. A head-stage could be used which would could have the ADS1298 chip and electrodes connected at the subjects head and having a wireless SPI communication with the microcontoller SPI interface. Possible circuitry which could be used for this could be Nordic semiconductors RF transceiver nRF24LU1+ and Texas Instruments eZ430-RF2500 for rapid wireless development. This feature will be most useful for use in human research and diagnostics. The wireless version would have some disadvantages which include high power consumption, and reduced bandwidth.

SD card logging: Developing countries have frequent power outages, and continuous monitoring of biosignals including the EEG, and the ECG might not be possible. The prototype amplifier does provide options for power-up using batteries but needs access to a USB 2.0 port for transferring conversion data, and programming the ADS1298. It could be a good idea to have all the data be sent to an SD card for logging and which can be later visualized either on a mobile phone, or on a computer later by a physician. The SD card would be advantageous if it would operate wirelessly.

Application Development: Tablet computers like the iPad, and smart phones like the iPhone, and Android have revolutionized the world of computing. Smart phone applications are being increasingly used by medical professionals. A similar application could be developed in the future which would wirelessly take data from the hardware and provide EEG visualization, filtering, and possible preliminary diagnosis with push notifications or automated calling feature for help in an emergency.

Hardware digital signal processing: Since EEG data is almost always contaminated by various artifacts, the EEG signal must be filtered for analysis. Providing options for hardware DSP and development of closed loop feedback systems could greatly aid in patient monitoring, diagnosis, research, and development of neural prosthetic devices. For diagnostic purposes the line noise must be filtered out the very least. Ideally it should also provide options for removal of eyes blink, ECG, teeth clenching, eyes rolling, muscle, and other artifacts, In research, developing control theory, and classification algorithms can greatly aid in development of prosthetic device like a brain controlled wheelchair, a closed loop seizure predictor, and many others. Implementing

DSP requires more computation and is best done using 32-bit digital signal processors, and field programmable gate arrays with full USB 2.0 support possibly as a virtual COM port.

On the fly programming: Currently, the MSP430 USB JTAG programmer is used to program the hardware. The current setup requires the programmer to be present to program the device. A good future work would be to implement JTAG programming without external hardware, just using software. This would help in reloading the firmware on the amplifier without having the big, expensive programmer present. Another advantage could be that the reloading the firmware could be done remotely.

Packaging: Another, important step for a biopotential amplifier is proper circuit shielding and avoiding electrical and magnetic interferences. The prototype needs to be shielded in a box, to prevent any external interferences. It is quite likely that the noise levels on the recordings would further reduce once this step is done.

Maintenance and Identification: Every electronic device needs to be maintained and should have unique identifiers and serial numbers both on the printed circuit board and the firmware. This helps in easy board identification, and troubleshooting hardware and software issues. The serial number should be printed on the hardware and a serial number generation tool could be developed using either C, MATLAB, or LabVIEW. This should be loaded on the firmware and could be accessed by the user. This will help in identifying which hardware, and firmware version is loaded on the amplifier to aid in post processing data analysis.

Appendix

Circuit Schematic and components of the 8 channel board

The following section contains the list of components used in the 8 channel version of the acquisition hardware. Figure 1 shows the complete schematic diagram of the 8 channel acquisition hardware.

Item	**Quantity**
Analog front end ADS1298 (No. of input analog channels/8)	1
Microcontroller MSP430F5525	1
Power Isolator ADum5000	1
USB Isolator ADum 4160	1
LT1964 (Adjust negative power)	1
LP2985A(Positive Power adjust) 2 each (3.3V and 1.8V)	4
TPS 60401 (inverter)	1
XO(4MHz)	1

Capacitor (10μF)	10
Capacitor (22μF)	1
Capacitor (1μF)	5
Capacitor (0.1μF)	10
Capacitor (10nμF)	3
Capacitor (100pF)	1
Capacitor (20pF)	2
Resistor 28Ω	4
Resistors 100k Ω	4
USB connection	1
JTAG Pin Header(14 pin)	1
Pin Analog sensors	10
Touch free pins	10
Printed Circuit board	1

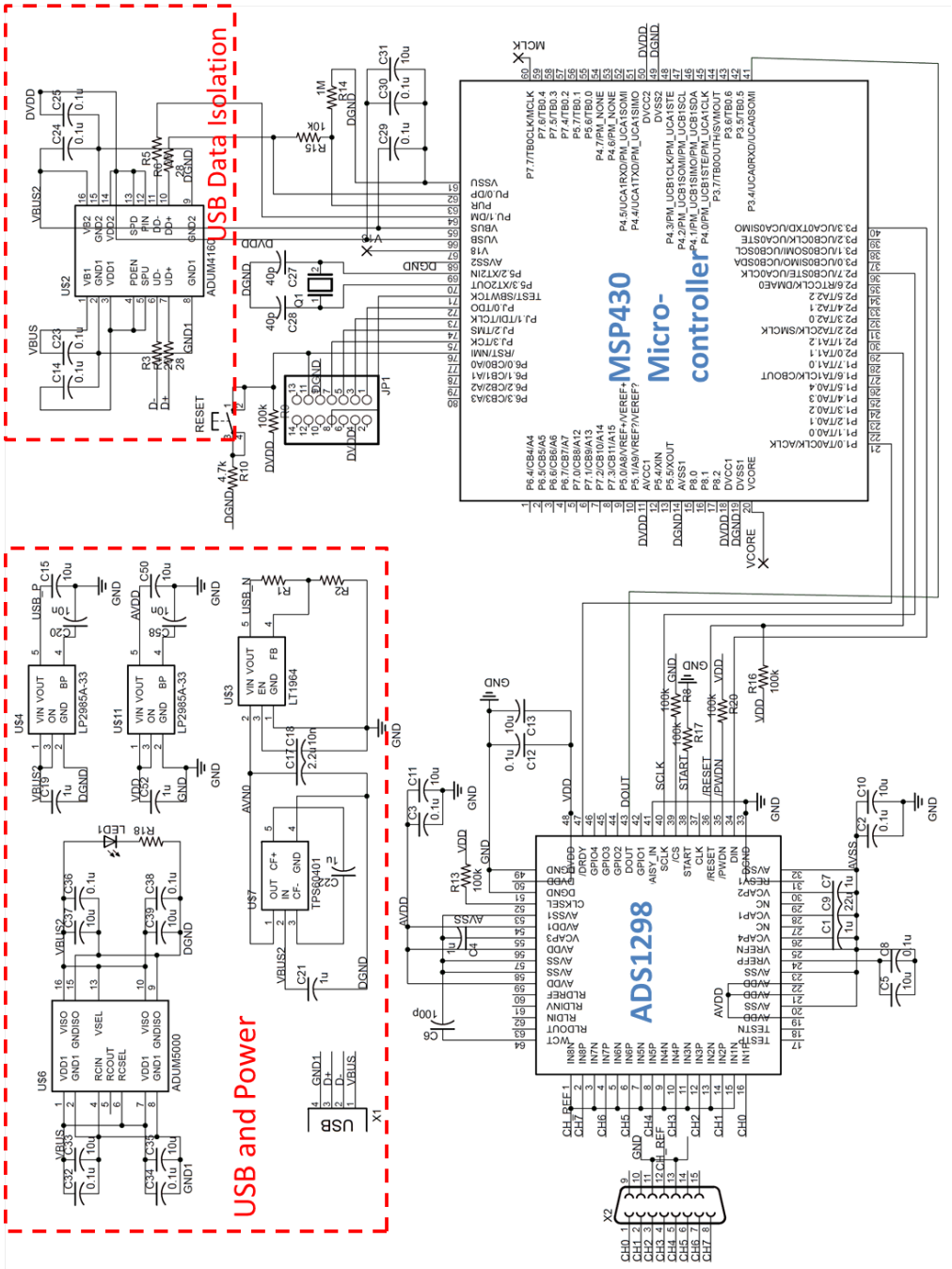


Figure A.1: Schematic diagram of the 8 channel board

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