SILICIDE AND GERMANIDE CONTACTS TO SILICON AND GERMANIUM NANOWIRES

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by

Nicholas S. Della

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The dissertation of Nicholas S. Dellas was reviewed and approved* by the following:

Suzanne E. Mohney  
Professor of Materials Science and Engineering  
Dissertation Advisor  
Chair of Committee

Theresa S. Mayer  
Professor of Electrical Engineering

Zi-Kui Liu  
Professor of Materials Science and Engineering

Joan M. Redwing  
Professor of Materials Science and Engineering  
Head of the Graduate Program of Materials Science and Engineering

*Signatures are on file in the Graduate School
ABSTRACT

Semiconductor nanowires have shown promise and garnered considerable interest for use in field-effect transistors, thin film transistors, and chemical and biological sensors. Electrical contacts to nanowire based devices have been identified as a source of performance limitations of these devices. For the successful application of nanowires into high-performance devices, a fundamental understanding of contact formation and contact properties is necessary. Furthermore, the formation of metallic silicides in the case of Si nanowires (SiNWs) or germanides in the case of GeNWs have proven to be an effective way to reduce the access and/or series resistance of nanowire devices. Here, the formation of silicides (Ti, V, Pt, Pd, and Ni) and germanides (Ni) in contacts to nanowires have been studied. Additionally, a method for accurate extraction of the Schottky barrier height in axial contacts to nanowires is demonstrated for Ni silicide contacts to n-type SiNWs.

We have found that as a basic criteria for forming axial metal silicide contacts to SiNWs from metal contact pads, the metal should be the dominant diffusing species (DDS) in the solid state reaction between the metal and Si for the phase formed. In the case of Ti and V, Si is actually the dominant diffusing species in the first phase formed, namely C49 or C54 TiSi$_2$ and VSi$_2$, and in this case the silicide is formed underneath the contact pad as opposed to along the SiNW itself. For Pt and Pd, the metal is the DDS in the first phase formed, Pt$_2$Si or Pd$_2$Si, and axial silicide segments are formed. However, in the case of Pt silicide formation, more severe annealing conditions cause a transformation to PtSi. In PtSi, Si is the DDS and Kirkendall voids form as a result of the unequal fluxes of Pt and Si causing a break to form at the interface between the PtSi and SiNW. In the case of Pd$_2$Si formation, Pd$_2$Si is the only phase that forms and the segment continues growth with increased annealing time and temperature; however, during silicidation of oxidized SiNWs Pd$_2$Si reacts through the SiO$_2$ shell surrounding the SiNW. This
situation would be problematic for forming structures in which the silicide contact is underneath a gate that must provide electrical isolation. A short would form between the gate and silicide contact if a transistor were made.

Fortunately, Ni silicides also form axial metal contacts and in the Ni-Si system for every Ni silicide phase that forms Ni is the DDS. We have also identified for the Ni-SiNW system that the orientation of the SiNW can determine the Ni silicide phase that forms. In the case of annealing Ni contact pads to [112] SiNWs, the high-temperature metastable $\theta$-Ni$_2$Si phase forms and is thermally stable until annealing conditions of 700°C and higher. At 700°C branches form as a compressive stress release mechanism and could result in electrical shorts to neighboring devices in high device density applications. When annealing Ni contact pads on SiNWs with [111] growth directions, NiSi$_2$ is the first phase to form and remains stable until temperatures in excess of 600°C where a transformation to NiSi occurs. In addition to identifying differences in the Ni silicide phase formed for different growth direction SiNWs, we have also identified differences in the kinetics of Ni silicide formation for [112] and [111] SiNWs. For [112] SiNWs, the formation of $\theta$-Ni$_2$Si is diffusion-limited with an activation energy of 1.45 ± 0.07 eV/atom. This activation energy is considerably lower than literature values of bulk lattice diffusion through Ni silicide compounds, and thus the diffusion mechanism is attributed to Ni diffusion along the Si/SiO$_2$ interface. For [111] SiNWs the formation of NiSi$_2$ is interfacial reaction limited with an activation energy of 0.76 ± 0.10 eV/atom. Furthermore, for the formation of $\theta$-Ni$_2$Si axial contacts to oxidized SiNWs, it was found the Ni reacted with the core of the SiNW, leaving the SiO$_2$ shell intact surrounding the $\theta$-Ni$_2$Si/SiNW interface. The ability of the $\theta$-Ni$_2$Si contact to react only with the Si core is a requirement for implementation into wrap-around gate Schottky diodes.
After identification of a suitable candidate, namely $\theta$-Ni$_2$Si contacts to SiNWs, was identified these contacts were integrated into wrap-around gate Schottky diode structures. Simulations by Karthik Sarpatwari showed that gating of the metal/semiconductor interface in full wrap-around gate Schottky contacts was an effective approach for extracting the true Schottky barrier height at the metal/semiconductor interface. For our $\theta$-Ni$_2$Si contacts to n-type SiNWs we were able to identify the same linear relationship between the ideality factor ($n$) and effective Schottky barrier height ($\phi_{B\text{eff}}$) measured under different gate bias conditions. By extrapolation of the linear $\phi_{B\text{eff}}$-$n$ plot to $n=1$ the actual barrier height at the $\theta$-Ni$_2$Si/n-SiNW interface is identified, in this case 0.57 eV. We measured Schottky barrier heights for SiNWs ranging in diameter from 60–100 nm and found no significant ($\pm$ 0.02 eV) deviation or trend with SiNW diameter. A new fabrication procedure for producing smaller diameter (30 nm and less) is also discussed and issues with integration of smaller diameter SiNWs into these structures due to the reduction of SiO$_2$ by the Al gate are mentioned.

Lastly, the formation of axial Ni germanide contacts to GeNWs was examined. We found that axial Ni germanide segments begin forming after annealing at 300°C for 2 min and continue growing with increased time and temperature. The Ni germanide phase is identified by matching of electron diffraction patterns to the Ni$_2$In prototype structure. A stoichiometry of Ni$_3$Ge$_2$ is assigned due to the lack of vacancy ordering observed in the electron diffraction patterns. All other Ni germanide phases with the Ni$_2$In prototype structure (B8 region of the phase diagram) have been reported previously to have some vacancy ordering with the exception of Ni$_3$Ge$_2$. After annealing at temperatures in excess of 400°C, a break is formed in the Ni germanide segment near the Ni germanide/GeNW interface. Plausible reasons for the break formation are discussed. We find the break formation problem can be worked around and that
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Chapter 1

Introduction

A nanowire can loosely be defined as a high aspect ratio material structure where the diameter is on the size scale of nanometers (nm) and the length is on the order of micrometers (μm) or greater. Nanowires can be composed of a wide range of different materials including metals (Au\textsuperscript{1,2}, Co\textsuperscript{3}), semiconductors (Si\textsuperscript{4,5,6}, Ge\textsuperscript{7,8}, InAs\textsuperscript{9}) and insulators (SiO\textsubscript{2}\textsuperscript{10}). Specifically, semiconductor nanowires have attracted interest for use as building blocks for nanoelectronic devices including field-effect transistors\textsuperscript{11,12}, light-emitting diodes\textsuperscript{13} and chemical sensors\textsuperscript{14,15}. For successful integration of nanowires into these applications, low resistance contacts are necessary in order to efficiently inject and extract current from the device.

Compared to conventional planar devices, nanowire based devices can offer some advantages. An advantage for field-effect transistors is the ability to be able to incorporate nanowires into devices where the channel of the transistor is fully surrounded by the gate. This allows for complete 360° symmetrical control of the channel and a reduction of short channel effects that can degrade device performance as planar technologies are scaled down\textsuperscript{16}. A great advantage for chemical sensors is that nanowires offer a structure with a large surface area to volume ratio. This situation causes the conductivity of the nanowire to be highly sensitive to the environment it is in and allows it to be used as a sensor where the conductivity of the nanowire can be calibrated to a specific chemical concentration.

Electrical contacts can greatly limit the performance of these nanoelectronic devices because the current flowing through the device often times can be limited by poor contacts\textsuperscript{17}. This problem was also previously demonstrated for contacts to carbon nanotube field-effect
transistors\textsuperscript{18}. Therefore, there exists a great demand to further the understanding of electron transport at metal/semiconductor interfaces and the effect that size can have on transport at these interfaces. This thesis will focus on solid-state reactions at the nanoscale, which will dictate the particular metal phase present at the metal/semiconductor interface, and on fabrication and evaluation of a device structure to extract the “true” Schottky barrier height of metal/semiconductor NW contacts.

**Basic Electrical Contact Theory**

When a metal contacts a semiconductor, there are a few basic physical phenomena that occur. Initially, when the metal and semiconductor have not yet contacted each other, the vacuum level (E_{Vac}) (defined as the energy level above which an electron is no longer bound to the material) of the metal and semiconductor are aligned at the same energy. As the metal and semiconductor initially come in contact (Figure 1-1(a)), the vacuum level of the metal and semiconductor remain aligned until the electrons in the metal and the electrons in the semiconductor have reached equilibrium. As this is occurring, the bands shift such that the Fermi level (E_F) of the metal and the E_F of the semiconductor align as the electrons reach equilibrium (Figure 1-1(b)). For an n-type semiconductor, depending on the values of the work function of the metal (\(\phi_m\)) and the electron affinity of the semiconductor (\(\chi_s\)), a barrier to electrons known as a Schottky barrier (\(\phi_{Bn}\)) will form with a value of, \(\phi_{Bn} = \phi_m - \chi_s\), defined as the Schottky-Mott limit. Alternatively, for a metal contacting a p-type metal, the Schottky barrier (\(\phi_{Bp}\)) forms with a value of, \(\phi_{Bp} = E_g - \phi_m - \chi_s\), where \(E_g\) is the band gap of the semiconductor.
**Figure 1-1:** Band diagram demonstrating (a) a metal and semiconductor initially coming into contact and (b) after the electrons in the metal and semiconductor have equilibrated. A more accurate model of metal/semiconductor contacts is shown in (c) where an interfacial layer is present with some interfacial defect state density ($D_{it}$) that can control the Schottky barrier height independently of the metal work function.

Unfortunately, this rather simple view of the formation of a Schottky barrier at the metal semiconductor interface almost never holds true. Rather, a more realistic picture of the metal/semiconductor interface involves some type of interfacial layer (Figure 1-1(c)) with the presence of some interface states\textsuperscript{19} with a particular density ($D_{it}$). Instead of the Fermi level of the metal aligning with that of the semiconductor, the Fermi level aligns with the surface Fermi level, which is determined by the degree of occupancy of the interface states, which will shift the surface Fermi level. The exact origin of the interface states is not well understood, and can vary depending on the semiconductor, but Tung\textsuperscript{20} suggests that dangling bonds at the semiconductor surface as well as an overlap of the wavefunction of electrons in the metal into the semiconductor are responsible for the formation of the interface states. Quite often an interface behavior
parameter $S$ is defined as, $S = \frac{d\phi_B}{d\phi_m}$. If $S = 1$, then the Schottky-Mott limit is observed, for $S < 1$, some degree of Fermi level pinning is observed. Figure 1-2 shows a plot of $S$ for a number of different semiconductors versus the difference in electronegativity showing that, in general, purely covalently bonded semiconductors exhibit a larger degree of Fermi level pinning than ionically bonded semiconductors.

![Figure 1-2: Plot of the interface behavior parameter (S) as a function of difference in electron affinity for semiconductor anion and cations. Δx of 0 is a purely covalent bond and an increase in Δx is an increase in the ionic nature of the bonding in the semiconductor. Plot modified from Kurtin et al.21](image)

It is clear from the above discussion on Schottky barrier formation that an understanding and engineering of the metal/semiconductor interface is necessary to have the potential to form metal/semiconductor contacts with predetermined Schottky barrier heights, or no Schottky barrier height at all to n and p-type semiconductors. However, due to the relative lack of control of the Schottky barrier height to Si devices, quite often one instead contacts a heavily doped region of the semiconductor in order to achieve a low-resistance Ohmic contact22. By heavily doping the
interface near where the metal comes in contact with the Si, the depletion region formed between the metal and Si is thinned, and as a result, electrons have a higher probability of tunneling through the barrier, increasing the current flowing through the contact. For this reason, as well as cost, contact to conventional planar Si devices is achieved by using a single metal to both n and p-type regions. The metal chosen to contact the devices is a midgap metal (i.e., Schottky barrier height is approximately half the band gap of the semiconductor) in order to achieve similarly performing contacts to both npn and pnp metal-oxide field-effect transistors (MOSFET), the most basic devices used for digital logic today.

**Introduction to Silicides**

In modern day MOSFETs, rather than simply contacting the source, gate and drain regions with a pure metal, silicides are more typically used. The reason for their use is that silicides have a number of attractive properties compared to their pure metal counterparts, and also lend themselves to the self-aligned silicide (or the so called salicide) process, illustrated in Figure 1-3. The main advantage of the salicide process is a reduction in the number of lithography steps. A few of the attractive properties of silicides include low electrical resistivities, formation at temperatures compatible with MOSFET device processing, stability in oxidizing environments, and stability of a particular stoichiometric phase (typically the phase with the lowest electrical resistivity) throughout processing and the lifetime of the device. The advantage of using a solid-state reacted silicide contact in a nanowire device is that for certain metals, the metallic silicide segment will form axially along the silicon nanowire. This creates a low-resistance segment of the device, effectively reducing the access resistance of the device. A reduction of the resistance of the device by this means can enhance the device performance.
Figure 1-3: Schematic diagram of the salicide process. The initial MOSFET with exposed source, drain and gate regions is shown in (a), followed by metal deposition over the entire wafer in (b). After metal deposition, (c) the wafer is annealed so that the metal reacts with exposed Si, initiating formation of metal silicide phases. After annealing, (d) a selective etch is performed to remove the unreacted metal and the final device is left with metallic contacts to the source, drain and gate.

In a typical binary metal-Si phase diagram, several different phases can exist. Each of these phases has a different electrical resistivity, and therefore it is often desirable to control the reaction between the metal and Si such that a particular phase (low-resistivity phase) forms and to determine the thermal stability of that phase. The thermal stability is important to understand because there are often several back-end-of-the-line processes that require subsequent anneals and one does not want the desired phase to change, resulting in degradation of device performance during these later processing steps.

Before discussing more recent work on metal/semiconductor nanowire reactions, it is important to understand past work that has been done on understanding silicide formation in
planar Si devices. A brief overview of thin film and bulk reactions will be given in the sections below, followed by more details of particular metal/Si systems in the chapters to follow. Of particular interest is how the supply and geometry of the metal and Si can affect the outcome of the reaction products. One area where this has been studied is in comparing bulk diffusion couples (i.e., unlimited supply of metal and Si) to thin-film diffusion couples (e.g., a metal film 100 nm or less thick on a Si wafer that is several hundred microns thick) and even in comparing extremely-thin-film (film thickness of only a few atoms) reactions to thin-film diffusion couples where the metal is 100 nm or less in thickness.

**Bulk and Thin Film Diffusion Couples**

In a bulk diffusion couple, where two materials are brought together into intimate contact, as the temperature is elevated, interdiffusion will occur if the two materials are not in thermodynamic equilibrium. Assuming that the diffusion couple is allowed to reach equilibrium at a given temperature, then the number and composition of the compounds to form at the interface between the two initial materials is determined by the phase diagram\(^25\). The thermodynamics (i.e., phase diagram) plays a role in determining the phases that form, but in order to predict the thickness of the layers, one must understand the kinetics or non-equilibrium processes such as diffusion. In comparison to thin-film reactions, the main difference is that for bulk reactions simultaneous phase formation is observed, and for thin-film reactions, a sequential phase formation is observed\(^26\). By simultaneous we mean to say that several phases will form in layers at the same time and that these phases will be determined by the phases that are thermodynamically stable on the phase diagram at the reaction temperature. Sequential phase formation is indicative of only a single phase forming at a given time between the two initial materials in the diffusion couple.
In comparing the thin-film diffusion couple to the bulk diffusion couple, one can argue that the reactions are extremely similar. The reasoning for the difference in sequential versus simultaneous phase formation is more of an issue of supply of the metal. For example, let us assume a metal of 100 nm thickness has been deposited on silicon and the relative interdiffusion coefficients of two phases, with generic names “A” and “B”, are a factor of 1000 different. Then also assuming that the thickness of a layer of a particular phase will be proportional to its interdiffusion coefficient, we find that when phase A reaches a thickness of 100 nm, phase B will be 1 only Å thick, or for all practical purposes non-existent\textsuperscript{27}. Since the metal supply is cut off, the secondary phase can no longer grow, unless it begins consuming the initial phase that formed. Furthermore, one can imagine a situation where two phases are competing for growth, but one is limited by diffusion and the other by interfacial reaction of the diffusion limited phase. In this case, the diffusion limited phase grows to a critical thickness, determined by the relative rate of supply material to the reaction front and the interfacial reaction rate of the phase that is growing at the expense of the diffusion limited phase. In this case, if the critical thickness is greater than the initial metal film thickness, one should not see simultaneous phase formation, and the interfacial reaction limited phase grows only when the metal supply has been fully consumed and there is no longer any supply of metal to continue growth of the diffusion-limited phase.

This logic can help to explain why sequential phase formation occurs in thin-film reaction couples and also help us to predict the first phase that should form in a thin-film reaction is usually the phase with the highest interdiffusion coefficient, though this does not always hold true and exceptions will be explained for a number of systems in the following chapters. One exception where the phase formation sequence is commonly altered is the use of very thin (< 10 nm) metallic films on Si wafers. In this case, the interfacial energy is the dominant factor in determining the first phase to form. The phase that forms typically displays an epitaxial
relationship to the substrate with a particular orientation that minimizes the strain energy at the interface due to any lattice mismatch between the two materials.28

The understanding of these thin-film reactions is of great importance in past and current state-of-the-art field-effect transistors. For contacts to electrical devices, there are a number of different silicide phases that can form from metal/Si contacts. Understanding the thermodynamics and kinetics relevant to these reactions is essential for creating high-performance thermally stable silicide contacts. In the past, kinetic issues related to the formation of TiSi₂ and CoSi₂ (the low electrical resistivity phases in the Ti-Si and Co-Si systems) have limited their use in state-of-the-art field-effect transistors.29 The low nucleation density of the disilicide phase in each of these systems led to problems with completely transforming contacts in small dimensions to the desired low-resistivity phase. This problem led to contacts with different properties across the wafer being processed (unacceptable by today’s stringent standards on electronic devices) and ultimately to the search for a replacement metallization. NiSi is now the silicide phase of choice in part because the formation of NiSi is diffusion controlled and also because less consumption of Si occurs during the phase transformation, which is important for silicon on insulator or shallow-body devices.30

Nanowire Diffusion Couples

Scaling from thin-film to nanowire diffusion couples, one must again take into account the supply changes of each constituent and also any size effects that may be present. In these nanowire diffusion couples, since the surface area to volume ratio is high, it may be expected that the interfacial energy will play a more significant role in these reactions. Additionally, the surface of the nanowire may provide a low energy pathway for diffusion compared to the oft-described vacancy assisted mechanism through the bulk lattice. One must also account for the
specific geometry of the reaction. In some studies, researchers have used thin metal films to contact SiNWs, while in others the reaction has been between a metallic and semiconducting nanowire. These two situations drastically change the supply of metal to the reaction front, and if the supply is cut off, then different phases will likely form compared to if the supply is continued.

We can use these ideas to consider some of the differences identified between thin-film and nanowire reactions in the Pt/SiNW case and the Ni/SiNW case. Starting with the the Pt/Si case, in thin-film reactions a sequential phase formation is often observed where Pt$_2$Si forms first followed by PtSi$^{31}$. Pt$_2$Si begins forming at a temperature of 250°C, and once the Pt film has been completely consumed, PtSi begins growing at a temperature of 300°C. Liu et al.$^{32}$ studied the solid state reaction between Pt thin films and vapor-liquid-solid grown SiNWs. They found that PtSi would form after annealing at 400°C and that Pt$_2$Si would only form if an excess of Pt was present (i.e., after full Pt-silicidation of the SiNW, pure Pt still remained and would continue reacting with PtSi to form Pt$_2$Si). In another study by Lin et al.$^{33}$, it was found that after annealing Pt contact pads on SiNWs at 520°C, PtSi would form axially along the SiNW with an epitaxial relationship to the SiNW. It was noted that despite a large lattice mismatch in one direction, no defects or dislocations were observed and an atomically abrupt, clean and straight interface was observed. This situation is in contrast to the atomically uneven interfaces usually observed for thin-film reactions of Pt on Si wafers and may be attributed to the difficulty in nucleating defects in some nanowire structures. The main difference in this particular study between the thin-film and nanowire reaction is that only a single phase is observed for the nanowire reaction, namely PtSi. Furthermore, in one report the PtSi is identified to grow epitaxially with an atomically “clean” interface compared to the jagged or stepped interfaces more typically observed for thin-film reactions of Pt on Si.

Ni/SiNW reactions have also been studied in a few cases, and stark differences can be observed compared to the thin-film case. The most common reports for the reaction of thin films
of Ni on Si wafers result in the formation of $\delta$-Ni$_2$Si formation at $< 400^{\circ}$C, followed sequentially by the formation of NiSi$^{14}$. NiSi thin films remain thermally stable on the Si wafer until temperatures in excess of 700$^{\circ}$C, where NiSi$_2$ begins nucleating. However, in the nanowire reactions, rather than a sequential phase formation, only a single phase is typically observed. The nickel silicide phase that forms can depend on the growth direction of the nanowire, as discovered in this thesis research, as well as the specific geometry and supply of nickel to the reaction. Additionally, the nickel silicide phase that grows is always found to have an epitaxial relationship to the SiNW. Details of the specific geometries and phases formed under different conditions will be reviewed in Chapter 3 and compared to results obtained in this thesis work for reactions between Ni contact pads and SiNWs of different growth directions.

**Electrical Contacts to Nanowires**

In addition to understanding the complex solid-state reactions that can occur on the nanoscale, it is important to understand the electron transport at the silicide/SiNW interface. One major difference between a conventional planar contact and a nanowire contact is the geometry, which affects the current transport in the contact (Figure 1-4). Also, in the nanowire case, there exists a large surface area to volume ratio. The significance of this ratio is that if the surface has different electrical properties than the bulk material, which is often the case because of surface defects as well as the influence of adsorbed layers on the surface, then the electrical conduction through the nanowire may be dominated by the surface. The effect of the surface on electrical conduction also means there may be a different charge carrier concentration at the surface as compared to the bulk, and because of this radial gradient in carrier concentration across the diameter of the nanowire, the depletion width of the Schottky barrier also varies along the cross-section of the contact.
Leonard and Talin\textsuperscript{35} have predicted that for planar wrap-around contacts to nanowires with a diameter less than 30 nm, the normalized contact resistance will increase exponentially compared to a planar contact of the same size with the same semiconductor doping density. Their explanation is that the reduced volume available for depletion in a nanowire results in less band bending, significantly reducing the effect of doping the semiconductor. In addition to the reduced band bending, Leonard and Talin also predict that Fermi level pinning may be partially relieved in contacts to nanowires. If Fermi level pinning is relieved, or at least partially relieved, this situation would allow for direct control of the Schottky barrier height by changing the metal work function in contact with the SiNW. In axial contacts, the issue of the limited volume for depletion no longer is problematic, but the relief of Fermi level pinning may still hold true. To shed more light on this fundamental issue, it is important to be able to extract the true Schottky barrier height of a metal/semiconductor NW contact as a function of size.

Because of the radial variation in the depletion width of axial contacts to semiconducting nanowires the Schottky barrier height extracted from a typical device will have an ideality factor greater than 1 and hence a modified Schottky barrier will be extracted. Sarpatwari et al.\textsuperscript{36} used
simulations to devise a method to extract the true Schottky barrier height of axial contacts to semiconducting nanowires. Because this structure was co-developed with this thesis work, the structure will be presented in detail in Chapter 4 along with details of processes necessary for fabrication of the structure. In brief, the structure (Figure 1-5) is composed of an axial contact to a semiconducting nanowire where the metal/semiconductor interface is completely surrounded by a dielectric and metal gate electrode. The advantage of this structure is that by surrounding the metal/semiconductor interface with a gate, the band bending at the metal/semiconductor interface can be modified by applying potential to the gate. In doing so, a series of different I-V curves can be measured on a single device by modifying the gate potential, and from this data the true barrier height can be extracted. This situation is similar to methods previously used on planar contacts where lateral inhomogeneities in the Schottky barrier height can cause difficulties in extracting the true Schottky barrier height of the region that is making the majority of the contact. In this case, a series of measurements is made on different contacts such that a series of I-V curves is obtained with different ideality factors and barrier heights. A linear correlation between the ideality factors and barrier heights is observed, and by extrapolating this plot to an ideality factor of 1, the “true” barrier height of the contact can be identified. This approach was demonstrated for planar Sn/n-Si\textsuperscript{37,38} and Ni/n-Si\textsuperscript{39} Schottky diodes. Note that extrapolation to an ideality factor of 1 may be appropriate for lightly doped semiconductors (n≤10\textsuperscript{16} cm\textsuperscript{-3}); however, for heavily doped semiconductors the plot should be extracted to the ideality factor for the image force lowered barrier (n\textsubscript{id}), which can be calculated by the equation\textsuperscript{40}:

\[ n_{IF} = 1 + \frac{1}{4} \left( \frac{q^3 N_d}{8\pi^2 \varepsilon_0^2 \varepsilon \varepsilon_0^2 \varepsilon_0^3 V_{bb}} \right)^{1/4} \]

where, q is the charge of the electron, N\textsubscript{d} is the dopant density, \varepsilon\textsubscript{s} and \varepsilon\textsubscript{∞} are the static and optical dielectric constants, and V\textsubscript{bb} is the band bending.
Similarly, for the axial nanowire contacts, we will determine the correlation between the Schottky barrier and ideality factor for different gate biases on a single device and then use this to determine the true barrier height. The primary difference between our experiments and the prior experiments on planar contacts is that in the planar case the Schottky barrier *height* is inhomogeneous and measurements are made on different devices to obtain different barrier heights and ideality factors, whereas for the axial nanowire contacts, the Schottky barrier *width* is inhomogeneous and measurements are made on a single device with different gate biases so that the Schottky barrier height may be studied as a function of nanowire size.

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Chapter 2

TEM Workbench

Introduction to Transmission Electron Microscopy

In order to study metal/Si nanowire (SiNW) reactions on the nanoscale and determine the crystal structure of phases formed as well as obtain chemically sensitive information about silicide compounds one of the most useful instruments available is transmission electron microscopy (TEM). TEM can offer advantages that are unparalleled by other techniques, including the ability to image and collect diffraction information on the nanoscale. The usefulness of this technique in studying silicide formation in SiNWs is the ability to simultaneously make measurements of the growth length of the silicide and determine the crystal structure of the silicide phase formed from the electron diffraction data.

The largest drawback typically associated with TEM is sample preparation. In order to collect useful data in the TEM, the sample must be electron transparent and as thin as possible to collect high-quality information about the material system of interest. Typically, for looking at nanowires in the TEM, the thickness of the sample is adequate and the nanowires may be dispersed onto a lacey C coated Cu grid and directly inserted into the microscope to collect data. However, if one would like to study a device structure or contact to a nanowire then a more complex structure must be fabricated. Here, the device structure we have developed will be referred to as the TEM workbench, shown schematically in Figure 2-1. The TEM workbench allows for the direct imaging of a single nanowire device with contacts so that the sample may be probed electrically to correlate structural and electrical properties of a particular device of
interest. This chapter will highlight TEM techniques of interest for characterizing silicide formation and also walk through the fabrication of the TEM workbench itself.

![Figure 2-1: Schematic diagram of the TEM workbench from both the top side and in cross-section.](image)

**Electron Diffraction**

One of the more intuitive methods for silicide identification in the TEM is by collecting electron diffraction patterns. Given that a material has some ordered crystalline structure, as the incoming electron beam interacts with the sample, constructive and destructive interference will occur between the electron waves scattering through the material creating a periodically spaced diffraction pattern. The intensity of the diffracted beams is directly related to the structure factor of the crystal with which the incoming direct beam has interacted. The structure factor is a quantity that is related to the atomic positions of atoms within the crystal as well as the relative scattering intensity of electrons from each particular atom. By knowing the initial atomic positions within a lattice, one can predict which crystallographic planes will cause constructive
interference resulting in a bright intense peak in the diffraction pattern. Furthermore, for the geometry encountered in the TEM, the only planes that will diffract from the crystal are ones perpendicular to the direct beam, i.e., for a cubic system the dot product of the direction normal to the incident beam with the corresponding plane of an observed diffraction spot will be zero. The spacing between diffracted beams is also directly proportional to the lattice spacing. Therefore, by indexing a given diffraction pattern, one can obtain information about the crystal structure of the material and the lattice parameters of the crystal from which the diffraction pattern has been obtained. This information can be directly applied to identifying silicide phases since most of the different silicide phases have unique crystal structures and lattice parameters. Pearson’s Handbook\textsuperscript{41} is an invaluable reference for a compilation of previous works identifying lattice parameters and atomic positions for a wide variety of binary systems. Therefore, a given pattern may be indexed to a particular structure, and then if the lattice constants also match within reason (typically about 1%), then a certain stoichiometry can be attributed to the region from which the diffraction pattern was collected.

\textbf{Electron Energy Loss Spectroscopy}

In addition to using electron diffraction to identify compounds, analytical TEM techniques such as energy dispersive spectroscopy (EDS) and electron energy loss spectroscopy (EELS) may be used to identify compounds from the chemical composition of the phase from which the spectrum has been collected. EDS data, while useful for the quick identification of elements present, can not accurately be converted to atomic percentages without the careful use of standards. Even by theoretical calculation of k-factors (a factor used to relate the relative peak intensities of two different elements from an EDS spectrum to the relative concentrations of each of those elements) the error is large (± 10 – 20\%)\textsuperscript{42}. For this reason and the lack of available
standards for the silicide phases studied in this thesis, EDS was not used as a method for identifying chemical composition of the silicide phases formed. Furthermore, the presence of the SiNₓ window beneath the sample would contribute to the Si signal creating further difficulties in EDS quantification of silicide composition.

EELS is a direct measurement of the inelastic scattering losses of electrons in the transmitted beam through the sample. The causes of energy losses of the inelastically scattered electrons can be caused by phonon excitations, plasmon excitations, inter- and intraband transitions, and inner shell ionizations. Each of these regions is shown in Figure 2-2 on a sample EELS spectrum. The low-loss portion of the spectrum, while containing interesting information about specific plasmon energies and the band gap of the material, can be difficult to resolve in detail without the use of a cold field-emission electron source or monochromator for the electron source. Use of a monochromator should be seriously considered, however, since a large number of electrons from the source are removed and low probe currents are the result. The electron signal may not be problematic for collecting data in the low-loss portion of the spectrum where counts are plentiful; however, at higher energies where higher counts are often desired this could actually degrade the quality of collected spectra.
**Figure 2-2:** Schematic diagram of a typical EELS spectrum. The zero-loss peak and details in the low-loss portion of the spectrum (energy on the order of 10’s of eV) are shown in (a) and core-shell ionizations at higher energies (energies on the order of 100’s of eV) are shown in (b).

The zero-loss peak is the most intense portion of the spectrum and if the full-width half maximum (FWHM) of this peak is too large, then its overlap into the low-loss portion of the spectrum can “drown” out detailed features about the band gap, phonon and plasmon excitations which have considerably lower intensities than that of the zero-loss peak. More easily resolvable features are in the high-energy loss portion of the spectrum. Peaks in the high-energy loss portion of the spectrum are caused by direct ionization of the sample and therefore will show up at energies with values equal to that of the initial electron energy (determined by the electron source) minus the ionization energy of a specific core-shell electron (determined by the binding energy of that electron). For much more detail on theoretical and experimental considerations of EELS the reader is referred to the text by Egerton. For convenience, the notation used for labeling of the high-energy energy loss portion of the spectrum is shown in Figure 2-3. For example, ionization of the $1s^{1/2}$ electrons is called the K edge, the $2s^{1/2}$ the L$_1$ edge, the $2p^{1/2}$ the L$_2$ edge, and the $2p^{3/2}$ the L$_3$ edge. Also, because of the relative similarities in energies of the L$_2$ and L$_3$ edges, this is typically referred to as a single edge called the L$_{2,3}$ edge, though both peaks should be clearly distinguishable.
Figure 2-3: Schematic of the core electron shells and the labeling notation used for EELS. EELS notation is labeled as the K, L, and M shells.

EELS spectra have been used in the past\textsuperscript{46,47,48} as fingerprints for the identification of different Ni silicide compounds. In Figure 2-4 an example in the shift in energy of the L\textsubscript{2,3} edge with decreasing Ni content in the stoichiometry of the Ni silicide phase is shown. The origin of this energy shift has been attributed to a reduced hybridization of Ni d states with Si p states in the Si-rich phases compared to the Ni-rich phases. In addition to the energy shift, Verleysen \textit{et al.}\textsuperscript{47} reported a decrease in the white lines intensity ratio for the L\textsubscript{3}/L\textsubscript{2} peaks as the composition changes from Ni-rich to Si-rich. The electron diffraction data in addition to information from EELS spectra will be used to corroborate the identification of the different Ni silicide compounds in Chapter 3; however, for other metal silicides studied we will exclusively use the electron diffraction patterns for identification.
Figure 2-4: EELS spectra of the Ni L$_{2,3}$ edge for different Ni silicide compounds showing an increase in the energy of the onset of the edge with increasing Ni content in the compound. Adapted from Cheynet and Pantel$^{46}$.

For the TEM work performed in this thesis a JEOL EM2010F microscope operated at 200 kV was used. The microscope is equipped with scanning TEM (STEM) capabilities, an annular dark field detector, Gatan Enfina EELS spectrometer (1.1 eV resolution in practice), and a high resolution pole piece ($C_s=0.5$ mm) allowing for an information collection limit of 1.9 Å. The sample holder used was a Gatan double tilt holder for tilting to different zone-axes of samples for collection of diffraction patterns.

Fabrication of TEM Workbench

The initial stages in the fabrication of the TEM workbench are similar to conventional nanowire device fabrication. A schematic overview of the entire process is shown in Figure 2-5, but will be described in detail in the following text.
Figure 2-5: Schematic diagram of process flow used to fabricate TEM samples. The process begins with (a) a Si wafer coated with 100 nm of SiN$_x$. (b) Ag electrodes are then patterned and deposited for electrofluidic alignment of the SiNWs. (c) The Ag alignment pads are etched away, and (d) Ni pads (or any other contact metal desired) are patterned and deposited to contact the aligned SiNWs. Finally, (e) a window is reactive ion etched (RIE) in the backside of the wafer, and (f) the Si is etched through with KOH to the frontside SiN$_x$ layer.

First, photolithography is used to pattern sacrificial alignment electrodes. This step is done using a double layer resist stack consisting of LOR2A as the first layer and S1805 as the top layer. The S1805 layer is photosensitive and is used for patterning, while the LOR2A layer is used to create a slight undercut (Figure 2-6(a)) beneath the S1805 layer for patterning of metals without the common “wings” that can be observed on metal layers patterned by a single layer resist structure (Figure 2-6(b)). The LOR2A layer is spun onto a three inch Si wafer coated with 100 nm of LPCVD SiN$_x$ at a speed of 4500 RPMs for 45 sec. The wafer is then baked at 180°C...
for 10 min to cure the photoresist. After the initial bake of the LOR2A layer, the wafer is allowed
to cool back to room temperature and then the S1805 photoresist is spun on at a speed of 4500
RPMs for 45 sec and soft baked at 110°C for 60 sec. A contact aligner (Karl Suss MJB3) is then
used to expose the photoresist to UV light through a mask in direct contact with the wafer for 4
sec. The mask is patterned opaque metal on a piece of transparent glass such that open areas in
the mask allow light through to exposed regions of the wafer. One cell of the mask is shown in
Figure 7. The actual mask contains a five by five array of this same pattern to make use of the
space available on a three inch diameter wafer. After exposure to UV light, the wafer is
developed for 60 sec in a commercial developer (CD-26) to remove exposed regions of the
photoresist. Next, the wafer is loaded into a vacuum chamber and the chamber is evacuated to a
pressure of $2\times10^{-7}$ Torr. Once the chamber has been evacuated, 80 nm of Ag is e-beam
evaporated onto the wafer. After evaporation, the chamber is vented and the wafer is put into a
commercially available photoresist remover (PG Remover) to remove the photoresist and metal in
undeveloped regions on the wafer.
After patterning the alignment electrode scheme, nanowires are electrofluidically aligned by grounding one electrode and applying an AC voltage to the second. The nanowires themselves are dispersed in ethanol by placing a small piece of the wafer from which the nanowires were grown, then sonicking the wafer for three one second pulses. The AC voltage frequency was typically 100 kHz and amplitude of ±5 V, though this can vary depending on the nanowire material type and diameter. While applying the AC bias to the electrodes, 3 – 5 μL of the nanowire solution is dispensed on top of the electrodes. This is done one to three times depending on the density of solution. The alignment sites are checked with an optical microscope after the first drop of nanowire solution is applied to determine if a suitable number of nanowires have aligned to the desired alignment sites.

Once the nanowires have been suitably aligned, the top contacts for the wafer are patterned. For the silicide and germanide formation studies described in Chapters 3 and 5, only a
single metal is patterned on top of the wafer to make contact so that the solid-state reaction between the metal film and semiconductor nanowire may be studied. If desired, more complex structures such as field-effect transistors or diodes could be patterned by using additional lithographic steps. The top contact mask layer pattern is shown in Figure 2-7 and is identical to the alignment electrode layer. The lithography steps detailed above for patterning the alignment electrodes are again used to pattern the top contact layer. The exception is that instead of evaporating Ag, a different metal of choice is used; for example, to study Ni silicide formation, Ni would be used for this contact layer. Before loading the sample into a vacuum chamber and evaporating the metal, a surface treatment is used to remove and native or intentional oxide layer on the surface of the semiconductor nanowires. For Si nanowires, 10:1 BOE (JT Baker Co.) was diluted to a ratio of 85:15 deionized water:BOE to increase the selectivity of the etch to SiO$_2$ over Si and also to reduce roughening of the Si nanowire surface that can occur when etching purely with 10:1 BOE$^{49}$. The etch time varies based on the oxide thickness, but for the native oxide an etch time of 25 sec was used and for nanowires with 10 – 15 nm of oxide an etch time of 90 sec was used. Note that 10 – 15 nm of SiO$_2$ is the common thickness found surrounding SiNWs after annealing in an O$_2$ furnace at a temperature of 900°C for 15 min with TCA present during oxidation.
Figure 2-7: Mask pattern used for alignment and the top contact in fabrication of the TEM workbench samples.

At this stage, the wafer has been processed to the state that the device or structure to be examined has been patterned on the top side of the wafer. The next series of processing steps are to etch the backside of the wafer so that the device is left suspended on the 100 nm thick SiN$_x$ layer coating the top side of the wafer. The first step is to selectively remove SiN$_x$ on the backside of the wafer in regions where we want to etch the Si through the wafer up to the front side SiN$_x$ layer, such that the non-etched SiN$_x$ on the backside of the wafer will act as a hard mask for wet etching of Si to the front side. Reactive ion etching (RIE) is used to etch the SiN$_x$ on the backside. First, the backside etch pattern is lithographically patterned on the backside of the wafer. For this step, S1827 resist is spun onto the backside of the wafer at 4500 RPM for 45 sec. The wafer is then soft baked at 115°C for 60 sec. Next, S1827 photoresist is spun onto the front side of the wafer and again soft baked at 115°C for 60 sec. Photoresist is spun onto the front side of the wafer to protect the devices that were patterned during the dry etch. The resist also prevents any scratching or etching of the top side SiN$_x$ film that will act as an etch stop for
the wet etch to selectively remove Si. If this top layer is damaged, the potassium hydroxide (KOH) used to etch the Si may leak through to the front side of the wafer during the wet etch and destroy the patterned devices.

Next, using a contact aligner, the wafer was exposed through the backside etch mask design (Figure 2-8). Note that the mask design consists of squares, which are aligned to the front side of the mask so that the Si was only etched in the region directly beneath the device. This alignment is possible because the Karl Suss MJB3 alignment system is equipped with an infrared light bulb underneath the wafer. This light shines up through the wafer (lightly doped Si is transparent in the infrared portion of the electromagnetic spectrum) and is blocked by metal patterned on the top side of the wafer so that the back side pattern may be aligned to metal previously patterned on the top side of the wafer. The S1827 resist requires an exposure of 7 sec followed by development in CD-26 for 60 sec. Note that this development time may increase if the infrared light is used for a prolonged length of time due to excessive heating of the wafer and the photoresist covering it.
Figure 2-8: Mask design used for RIE etching of the backside SiN<sub>x</sub> layer to produce a hard mask for KOH etching.

Also, the lines surrounding each of the squares were specifically patterned so that they would not etch through the wafer, but just a notch is etched so they may be used to cleave the wafer into smaller samples later for converting into sizes compatible with the TEM holder (holder size is a 3 mm diameter circle). Note that these lines do not intersect at the corners of the square to be cleaved. The reason for this is that if a cross is made on the top of a <100> Si wafer and etched in KOH, then <110> planes are exposed at the corners and because of the highly anisotropic nature of KOH wet etching of Si<sup>30,51,52</sup>, these <110> planes will etch very fast relative to other directions and result in etching into the direction of the patterned windows. The final result after KOH etching are large windows etched into the backside of the wafer, rather than smaller windows with the cleave lines surrounding the windows that is desired.
For the RIE etch, a PT720 dry etch system is used with the process gases CF$_4$ and O$_2$. The relative CF$_4$ and O$_2$ flow rates are 45:5 and the chamber pressure is held at 200 mTorr with an etch power of 100 W. The etch was performed for 2 min to remove the 100 nm of SiN$_x$ in the patterned regions on the back side of the wafer. Next the wafer was soaked in acetone to remove the photoresist on the front and back side of the wafer, followed by a soak in isopropyl alcohol to remove and acetone resist and then soaked in deionized water and blown dry with N$_2$.

Following the RIE etch, the last step in the fabrication of the TEM workbench samples is to remove the Si through the thickness of the wafer, leaving the patterned device structure on a thin SiN$_x$ window. A wet KOH etch was used to etch through the Si wafer. As mentioned above, wet KOH etching is highly anisotropic in nature. The $\langle 111 \rangle$ planes are etched the slowest, as a result $\langle 111 \rangle$ sidewalls are formed during etching. This causes the pyramidal type etch structure shown schematically in Figure 2-5(f). KOH will also etch the metal and semiconductor nanowires patterned on the top side of the wafer, so this must be protected during the etch. For this purpose, a special etch jig (commercially available from AMMT) was used. The wafer is mounted and sealed (Figure 2-9) so that only the backside of the wafer is exposed while the jig is fully submersed in KOH (with the exception of the handle). The KOH etch conditions were a KOH concentration of 30 wt% and a temperature of 90°C, monitored by a teflon thermocouple (stainless steel thermocouples may be attacked by the KOH solution and contaminate the sample). The etch rate under these conditions is approximately 1 – 2 μm/min, depending on the volume of the initial KOH used. As the etch proceeds, OH$^-$ ions are depleted in the solution and the etch rate is reduced with time. The reduction in OH$^-$ concentration is not necessarily problematic for the fabrication of the samples, but may require longer than expected etch times, especially if solutions are reused for subsequent etches of other wafers.
Figure 2-9: Schematic diagram of the AMMT holder used to seal off the front side of the wafer. The wafer is put face down into the holder and then the top ring seals around the outside of the back side of the wafer. As the jig is submerged in KOH only the backside of the wafer is exposed to the KOH solution.

Noteworthy is that the above fabrication sequence can frequently result in either leaking of the etch jig or windows breaking at the end of the etch and KOH leaking through to the front side. When hot KOH comes in contact with the front side of the wafer it almost immediately destroys patterned metal structures as well as the Si nanowires. As an alternative fabrication sequence, the above steps may be repeated out of order. Starting instead with the RIE etch of the backside SiN₃ pattern, followed by the KOH etch. This way, no etch jig needs to be used because the devices have not yet been patterned on the top side of the wafer. Even if a window breaks and KOH leaks through to the front side, nothing is patterned yet, and therefore cannot be destroyed. Following the etch, and subsequent deionized water soak and drying by N₂, nanowires
are randomly dispersed on the topside of the wafer. A different mask (schematically similar to the contact pattern shown in Figure 2-5(d)) than used before, consisting of four contact pads aligned to each SiNₓ window is lithographically patterned on the top side. Lastly, the contact metal of choice is evaporated to make contact with the nanowires. The advantage of this type of processing is that the yield is much greater than the previously described process for studying the reaction of metal contact pads with semiconductor nanowires. The disadvantages related to this process are mainly that the wires are randomly dispersed and the probability of a nanowire randomly spanning two contacts so that a two point electrical measurement could be made is extremely low. Also, as resist is spun onto the wafer, some windows break as a result of the fragile structure being spun at high speed. The number of windows broken is low (<10%) for a single spin, but for more complex structures where several layers may need to be patterned, this could actually adversely affect processing and result in a lower yield than the initially described process steps of first patterning the devices and then etching through the wafer.

In any case, once the wafer has been fully processed, the individual square samples are cleaved. At this point, any further processing necessary should be performed, such as subsequent annealing for studying the reaction between the contact and the nanowire. Then M-Bond 200 glue is applied to the outside of 3 mm diameter Cu apertures (SPI supplies) with a 1 mm hole in the center. The aperture is then glued to the topside of the TEM workbench sample so that the central 1 mm hole is centered around the SiNₓ window and structure patterned on the topside of the wafer. Gluing of the samples to the apertures is done so that the thick samples (wafer thicknesses used were 350 and 384 μm thick) will sit recessed in the center of the TEM holder and only the lip of the aperture will be in contact with the holder. The TEM holders are typically shallow and can only accept samples with thicknesses of approximately 50 μm or less.

The following chapter will focus on the application of the TEM workbench in the study of metal/SiNW reactions including Ti, V, Pd, Pt and Ni. Additionally, later in Chapter 5 the
study of solid-state reactions between Ni and Ge nanowires will be performed using the same approach but substituting Ge nanowires for the Si nanowires.

References


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Chapter 3

Metal and SiNW Solid State Reactions

The following chapter will focus on solid-state reactions between metal contact pads (Ti, V, Pd, Pt, and Ni) and Si nanowires (SiNWs). In each subsection a review of solid-state reactions between the specific metal and Si wafers will be described, followed by the results obtained for reaction between the contact pad and SiNWs for different annealing conditions. Lastly, a comparison between the two results and discussion of any differences observed will be presented. For further information about silicide properties and thin film work, and a comprehensive list of early references, the reader is referred to an early review of formation and characterization of transition-metal silicides by Nicolet and Lau. The main focus of this chapter is to identify metal-SiNW systems in which the metal will diffuse into the SiNW and react to form an axial silicide segment with reduced electrical resistivity compared to the semiconducting SiNW.

Ti Solid-State Reaction with SiNWs

Ti Silicide Thin Film Formation Review

Recall from Chapter 1 that in thin-film reactions, a sequential phase formation is typically observed during solid-state reactions between thin metal films and a Si wafer that is much thicker, and therefore greater in supply. TiSi₂ is a low-resistivity intermetallic compound that was of great interest for contacts to source, drain, and gate regions of complementary metal oxide semiconductor (CMOS) devices. TiSi₂ has two different polytypes, a base-centered orthorhomic
structure referred to as the C49-TiSi$_2$ and a face-centered orthorhombic structure referred to as the C54-TiSi$_2$ phase$^{54}$. The Ti-Si phase diagram is shown in Figure 3-1.

![Ti-Si phase diagram](image)

**Figure 3-1:** Ti-Si phase diagram from ASM Handbook$^{55}$.

The C49-TiSi$_2$ phase is typically the first phase to form in thin-film reactions, and has a moderately high resistivity (60 – 70 $\mu\Omega$-cm)$^{54}$. The desired phase to form, from an electronics application perspective, is the low-resistivity (15 – 18 $\mu\Omega$-cm)$^{54}$ C54-TiSi$_2$ phase; however, this phase does not form until temperatures in excess of 700°C and is nucleation limited. A problem was also found related to the use of this compound as the size of the transistor was shrinking. That is, because of the relatively low nucleation density of C54-TiSi$_2$ compared to the size of the contact openings, these contacts would either be partially transformed (Figure 3-2), not transformed at all, or possibly completely transformed$^{56}$. This situation led to contacts with dramatically different properties across the processed wafer, which was unacceptable for the high-performance requirements of CMOS devices.
Figure 3-2: Schematic diagram of a partially transformed TiSi$_2$ contact to Si wafer. The partial transformation is a device performance issue because the C49 and C54 phases of TiSi$_2$ have significantly different electrical resistivities. Figure adapted from Harper et al.$^{56}$

In looking at the Ti/Si wafer reactions more closely one can identify a number of relevant phenomena that may be related to the Ti/SiNW reactions. For one, because of the relatively low nucleation density discussed above, it may be unexpected to form the low-resistivity C54-TiSi$_2$ phase in a SiNW. Also, one would expect that if the Cu$_3$Au rule$^{57}$ is followed, that the richer element in a binary compound should be the dominant diffusing species (DDS). In the case of TiSi$_2$, the richer element is Si, and so we may expect that a lateral silicide segment might not form into the SiNW. Beyers and Sinclair$^{58}$ reported the phase formation sequence of Ti thin films on Si wafers to be purely an initial formation of C49-TiSi$_2$ followed by transformation to C54-TiSi$_2$ at higher temperatures. However, there are also reports of Ti$_5$Si$_3$$^{59,60}$ and/or TiSi$_4$ forming initially followed by the TiSi$_2$ transition. Because of the possibility of Ti$_5$Si$_3$ forming at lower temperatures, we reasoned that
the Ti/SiNW system may still be an interesting system to study since it is possible Ti could be the DDS in this compound. Therefore, the possibility remained that a lateral silicide segment of Ti$_5$Si$_3$ might be formed during the solid-state reaction of Ti thin films with SiNWs, and interest remained in the reaction between Ti thin films and SiNWs.

**Ti/SiNW Solid State Reaction Results**

Samples to study the solid-state reaction between Ti contact pads and SiNWs were fabricated as explained in Chapter 2 with the Ti being e-beam evaporated to a thickness of 80 nm. The SiNWs were grown via the vapor-liquid-solid growth technique using gold as a catalyst. The [112] SiNWs were grown from oxidized Si substrates to average lengths of 20 μm with an average diameter of 50 nm and lightly doped p-type with a B(CH$_3$)$_3$/SiH$_4$ flow ratio of 2x10$^{-5}$ during growth. The [111] SiNWs were grown using SiCl$_4$ from (111) Si wafers without intentional doping, with average diameters of 45 nm. Samples were annealed ex-situ at temperatures of 450, 600, 700, and 800°C for 2 min in a rapid thermal annealing (RTA) furnace purged with ultra high purity (UHP – composition 99.999% Ar) Ar. Different samples were annealed at each temperature to study exclusively the effect of a single anneal at each temperature, rather than a cumulative annealing effect.

Figure 3-3 shows TEM micrographs of samples of Ti contacts to SiNWs with the [112] growth direction annealed at each temperature. We can see that from these images there is no indication of lateral diffusion of Ti into the SiNW after annealing up to 800°C. We can observe from the darkened contrast surrounding the NWs underneath the pad that some solid-state reaction has occurred between the Ti contact pads and the SiNW after anneals at 600, 700, and 800°C for 2 min. Selected area electron diffraction (SAED) was used to determine the reaction
product. Table 3-1 lists the measured interplanar spacings for samples annealed at 450, 600, and 800°C for 2 min versus known interplanar spacings for Ti, C54-TiSi$_2$, and C49-TiSi$_2$.

For the SAED pattern obtained from the sample annealed at 450°C, all diffraction spots can be indexed as either pure Ti or as the C49-TiSi$_2$ phase. For SAED patterns collected at 600 and 800°C, all spots can be indexed as Ti and a mixture of C49 and C54-TiSi$_2$. The lack of lateral diffusion into the SiNW is not surprising, as the past work on TiSi$_2$ formation on Si wafers has shown that Si is the DDS in these reactions. Also, the observation of C54-TiSi$_2$ after annealing at 600 and 800°C is consistent with the temperature of ~700°C in thin-film reaction couples where the C49 to C54 TiSi$_2$ transformation is observed to occur at 700°C. Furthermore, the low nucleation density observed in thin film reactions may help to explain why even at 800°C there is evidence for the presence of C49-TiSi$_2$, rather than the complete transformation into the C54-TiSi$_2$ phase. Due to the relatively small contact area between the Ti contact pad and SiNW, there exists a smaller area for nucleation of the C54-TiSi$_2$ to occur, similar to the problems encountered in planar CMOS devices where partially transformed contacts exist when contacting line widths less than 100 nm in width. Additionally, no observable evidence is present for any difference between the reaction of the Ti contact pads and the [112] or [111] SiNWs.
Figure 3-3: TEM micrographs of Ti contacts on SiNWs annealed at (a) 450°C, (b) 600°C, (c) 700°C and (d) 800°C for 2 min.
Table 3-1: Listing of measured interplanar spacings compared to actual values that the measured values correspond to for pure Ti, C49-TiSi2, and C54-TiSi2.

<table>
<thead>
<tr>
<th>Temperature</th>
<th>Measured Interplanar Spacings (nm)</th>
<th>Actual Interplanar Spacings (nm)</th>
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<tr>
<td>450°C</td>
<td></td>
<td>C49-TiSi2 (130) - 3.51</td>
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<td></td>
<td>3.05</td>
<td>3.9</td>
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<td></td>
<td></td>
<td>C49-TiSi2 (130) - 3.510</td>
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<td>600°C</td>
<td>4.34</td>
<td>Ti (002) - 4.260</td>
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<td>4.47</td>
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<tr>
<td>700°C</td>
<td>6.63</td>
<td>Ti (110) - 6.777</td>
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<td>6.23</td>
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<td></td>
<td>7.79</td>
<td>C49-TiSi2 (202) - 7.811</td>
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<td>6.8</td>
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<td></td>
<td>10.3</td>
<td>C49-TiSi2 (332) - 10.183</td>
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<td>10.37</td>
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V Solid-State Reaction with SiNWs

V Silicide Thin Film Formation Review

V thin film reactions with Si wafers have also been studied, though not with as much interest for electronic applications as the Ti-Si system. In general, for thin V thin films on Si wafers the phase formation sequence begins with the formation of VSi2 at temperatures greater than 500°C.\(^{63,64,65,66}\) However, Krautle et al.\(^{64}\) reported on the effect of O at the interface. They observed that at a clean V/Si interface, VSi2 will form, but with O present at the interface the first phase to form was V3Si. Similar results were also obtained by Tu et al.\(^{65}\). The V-Si phase diagram is shown in Figure 3-4.
V/SiNW Solid State Reaction Results

Samples for studying the solid-state reaction between V contact pads and SiNWs were fabricated in the exact way as the Ti/SiNW samples, with the exception that 80 nm of V was e-beam evaporated as the contact material. Samples were annealed at 350, 400, 500, and 600°C for 2 min in an RTA furnace purged with UHP Ar. A TEM micrograph of a sample annealed at 500°C for 2 min is shown in Figure 3-5. Similar to the Ti-SiNW system, it appears that the contact pad has reacted with the SiNW, but no axial silicide segment is formed. Surrounding the SiNW is a region of dark contrast indicating there may be some diffusion of Si into the surrounding V pad. From these studies, we conclude that Si is the DDS in the initial stages of growth of silicides in the Ti-SiNW and V-SiNW systems and are not suitable systems for formation of axial low-resistance silicide segments for contacts to SiNWs.
Pt – SiNW Solid State Reaction

Pt Silicide Thin Film Formation Review

Pt thin film reactions on Si wafers have been studied quite extensively in the literature. PtSi is particularly interesting because of its low Schottky barrier height to p-type Si (0.2 eV\textsuperscript{67}) making it an attractive candidate for Ohmic contacts to p-type Si. Primarily two different phases are observed in reactions of Pt with Si, and for the reader’s convenience the Pt-Si phase diagram is shown in Figure 3-6.
Figure 3-6: Pt-Si phase diagram from ASM Handbook\textsuperscript{55}.

Wittmer\textsuperscript{68} found that Pt\textsubscript{2}Si will form at temperatures below 300°C, and at temperatures above 300°C, Pt\textsubscript{2}Si will transform into PtSi. For the formation of Pt\textsubscript{2}Si, it has been observed that the DDS is Pt, whereas for the formation of PtSi the DDS is Si\textsuperscript{69} as determined by radioactive tracer experiments. Previous work has also been performed on reactions in the nanowire geometry. Liu \textit{et al.}\textsuperscript{70} found that reaction between evaporated Pt on SiNWs began at 250°C, and at temperatures above 400°C, the reaction product was PtSi. They also observed that if the Pt was in excess (Pt films thicker than the SiNW diameter), then the phase that would form was Pt\textsubscript{2}Si due to the excess Pt available to continue reacting after the conversion to PtSi. Furthermore, they observed the effect of O contamination on the reaction. At temperatures less than 400°C, the presence of O at the Pt/SiNW interface was observed to retard the reaction, and at temperatures greater than 450°C, the reaction was found to proceed; however, the Pt silicide nanowire had a rough morphology. In another study by Lin \textit{et al.}\textsuperscript{71} of the reaction between Pt contact pads and
SiNWs, the epitaxial formation of PtSi was observed after annealing at 520°C. Lin also found that the Pt silicide segments would intrude through SiNWs with 2 nm of SiO$_x$ on the surface, resulting in PtSi/SiNW heterostructures surrounded by SiO$_x$.

**Pt/SiNW Solid State Reaction Results**

For the study of the reaction between Pt contact pads and SiNWs, samples were fabricated in the same way described in Chapter 2, here the exception being that 80 nm of Pt was sputtered. Sputtering was used for Pt deposition because it was found that films deposited by e-beam evaporation would completely delaminate during the lift-off process. Delamination in these Pt thin films was attributed to the high tensile stresses that can occur in thicker evaporated Pt films. Samples were annealed ex-situ at temperatures of 400, 450, 500, 600, and 700°C for 2 min in an RTA furnace purged with UHP Ar. SiNWs used in this study were grown under identical conditions to those described for the Ti and V reactions with SiNWs; however, we also studied the reaction of Pt with oxidized SiNWs. The SiNWs that were oxidized were the [112] p-type SiNWs and they were oxidized in O$_2$ in a furnace at 900°C for 15 min with the addition of trichloroethane (TCA).

No significant lateral silicide formation is observed after annealing at temperatures of 400 and 450°C for 2 min, as demonstrated in the TEM micrographs in Figure 3-7(a) and (b), respectively. After annealing at 500°C for 2 min, a short axial Pt silicide segment is formed. The average length of the Pt silicide segment after annealing at 500°C for 2 min is 92 nm. In some cases, the length is limited by a break in the nanowire at the interface between the Pt silicide and the SiNW. Increasing the annealing temperature to 600°C for 2 min results in an increase in the Pt silicide segment length. The average length after annealing at 600°C for 2 min is 300 nm (Figure 3-8(a)). Similar to the observations after annealing at 500°C, we see that some wires
break (Figure 3-8(b)) at the Pt silicide/SiNW interface and others remain as a continuous segment. The morphology of the wires after annealing at 600°C is a roughened surface with kinks along the wire. Kinking of the Pt silicide wires was observed by Liu et al. during their study of the reaction of Pt films on SiNWs. The formation of the kinks was considered a stress release mechanism during the solid-state reaction. Similar results were also obtained for the [111] growth direction SiNWs, and no significant difference between the [112] and [111] growth direction SiNWs is observed.

**Figure 3-7:** TEM micrographs of Pt contact pads on SiNWs annealed at (a) 400°C and (b) 450°C for 2 min showing that no significant lateral diffusion occurs at lower temperatures anneals.

SAED patterns from the Pt silicide segments of the nanowires were collected to determine the phase formed during the solid-state reaction. The insets in Figure 3-8 show diffraction patterns indexed as the Pt$_2$Si phase. Pt$_2$Si has the H$_2$Th prototype structure (space group I4/mmm) with lattice constants $a=0.3948$ nm and $c=0.5963$ nm$^2$. Initial formation of Pt$_2$Si is in agreement with the thin film reactions where this is the first phase formed, but in the thin film reactions, this phase can form at temperatures as low as 300°C. The lack of lateral formation of the Pt$_2$Si phase in the nanowire study until 500°C is not completely understood. Liu *et al.*
reported that the presence of oxygen contamination during annealing can lead to retarding the Pt-SiNW reaction until temperatures above 450°C. Although we do not expect oxygen contamination to be an issue, because samples were purged in UHP Ar that was run through a gettering furnace (hot furnace in which the gas is flowed through porous Ti sponge to reduce any oxygen contamination through the oxidation of the Ti sponge), the similarities in temperatures at which the reactions proceed (450°C in their study versus 500°C in this study) cannot be ignored, and for this reason we leave open the possibility that the presence of oxygen may be inhibiting the reaction at lower temperatures.

![TEM micrographs of Pt contact pads on SiNWs annealed at 600°C for 2 min. Axial Pt$_2$Si segments are formed along the nanowire and in some cases the wire is broken at the Pt silicide/SiNW interface.](image)

**Figure 3-8:** TEM micrographs of Pt contact pads on SiNWs annealed at 600°C for 2 min. Axial Pt$_2$Si segments are formed along the nanowire and in some cases the wire is broken at the Pt silicide/SiNW interface.

We find that for the reaction of Pt contact pads with oxidized SiNWs, similar results are obtained compared to the reaction of Pt with as-grown SiNWs. Note, in these reactions the oxide is etched away in the contact region surrounding the SiNW such that the Pt is in intimate contact with the SiNW core to study the reaction and possible intrusion of Pt$_2$Si nanowire segments into an SiO$_2$ shell. Average Pt$_2$Si segment lengths are 90 nm after annealing at 500°C for 2 min. Samples annealed at higher temperatures display longer Pt$_2$Si segment lengths. TEM
micrographs of samples annealed at 500, 600 and 700°C for 2 min are shown in Figure 3-9. The Pt$_2$Si segment length increases to an average of 250 nm after annealing at 600°C for 2 min, and after annealing at 700°C for 2 min the average Pt$_2$Si segment length increases to 320 nm. Compared to the results with no oxide shell the average lengths are similar. We can also see from the TEM images that the Pt silicide length stops at about the same point at which the oxide shell surrounding the SiNW is thick. The reason for this short region between the contact pad and SiNW where the oxide shell has been removed is that because in the double layer resist process described in Chapter 2, during the step in which BOE is used to remove the oxide shell it also removes the oxide in the undercut region.
Figure 3-9: TEM micrographs of Pt contact pads annealed on oxidized SiNWs at temperatures of (a) 500°C, (b) 600°C, and (c) 700°C for 2 min. The oxide shell can be seen as the lighter layer surrounding the pure SiNW, and the Pt silicide segments are retarded from continued axial growth at this point where the oxide shell is intact.

Foll and Ho\textsuperscript{73} reported on the effect of an interfacial SiO\textsubscript{2} layer between Pt thin films and Si wafers on the solid state reaction and formation of Pt silicide upon annealing these structures. They found that with a 3 nm thick SiO\textsubscript{2} layer at the Pt/Si interface, the reaction was substantially affected. The morphology of films was extremely rough, and also in some cases the Pt did not even react through the SiO\textsubscript{2} to form PtSi after annealing at 400°C for 1 h. Furthermore, Scott et al.\textsuperscript{74} performed a similar study with an interfacial layer of SiO\textsubscript{2} 2.4 nm thick. Scott found that
Pt$_2$Si would not form until annealing at temperatures in excess of 650°C. It is clear from these previous studies on thin films and the study by Liu et al. that oxygen contamination greatly affects the solid state reaction between Pt and Si and may be playing a role in retarding the reaction between the Pt thin film and SiNWs in our study; however, we were not able to identify a source for the oxygen contamination.

From the high-angle annular dark field (HA-ADF) image in Figure 3-10, we can see that the interface formed between the Pt silicide segment and the SiNW is not atomically abrupt. In the HA-ADF mode of the TEM, image contrast is determined predominantly by atomic mass. Therefore, the bright regions in the image are of heavy elements (Pt or PtSi$_x$, compounds) and the lighter regions are from lighter elements (the SiNW or the SiN$_x$ support film). The HA-ADF image in Figure 3-10 shows islands of Pt silicide in the nanowire ahead of the silicide/SiNW interface. This observation is rather undesirable from the point of view of studying the electrical properties of the silicide/SiNW interface. These islands of Pt silicide could provide for an additional current transport pathway, making the accurate extraction of the Schottky barrier height difficult. The presence of these islands would greatly alter and create a non-homogeneous depletion width at the Pt silicide/SiNW interface. The inhomogeneity of the depletion width would further complicate and cause difficulties in accurate extraction of the Schottky barrier height of these contacts.
**Figure 3-10**: HA-ADF images of an axial Pt$_2$Si segment formed showing the non-abrupt interface formed between the silicide and the SiNW. Small islands of Pt silicide are observed away from the interface formed by the main segment of Pt$_2$Si and the SiNW.

Figure 3-11(a) shows a TEM micrograph of a sample annealed at 500°C for 2 min in which the wire has broken. A higher magnification image of the Pt silicide segment is shown in Figure 3-11(b). The abrupt contrast change along the wire from the segment near the pad to the segment at the end where the wire is broken is indicative of a change in composition. The SAED patterns also reveal that there is a difference in the crystal structure between these two regions. The SAED pattern collected from the region near the Pt pad can be indexed as the Pt$_2$Si phase, and the region at the end of the Pt silicide segment where the segment has broken, can be indexed as PtSi. PtSi crystallizes with the orthorhombic MnP prototype structure (space group Pnma) with the lattice constants $a=0.5595$ nm, $b=0.3603$ nm, and $c=0.5932$ nm$^7$. This discovery of a change in the phase near the interface in the nanowires that have broken can help us to explain why the wires break. For the formation of Pt$_2$Si, Pt is the DDS, and we can assume that during this reaction that Pt is diffusing into the SiNW to cause the solid-state reaction into the Pt$_2$Si phase. However, as the PtSi phase begins growing near the Pt$_2$Si/SiNW interface, there is a
change in the kinetics of the reaction. For the formation of PtSi in the thin film reaction couples, it has been observed that Si is the DDS. In this case, Si is diffusing away from the SiNW into the Pt$_2$Si to transform the segment into PtSi. As this reaction proceeds, and similar to the well-described Kirkendall void phenomena caused by uneven fluxes in diffusion couples, voids form in the SiNW, effectively cutting off the supply of Si to the reaction and leading to a broken nanowire.

**Figure 3-11:** (a) TEM image of a wire broken after annealing at 500°C for 2 min and a high magnification view of the tip of the Pt silicide segment showing the formation of PtSi at the tip of the Pt silicide segment where it has broken. Insets are Fourier transforms from the image used to identify the Pt$_2$Si and PtSi segments.

For implementation of a silicide contact into the wrap-around gate Schottky diodes described in Chapter 1, a few key criteria need to be met. For one, the silicide must form axially down the nanowire, which the Pt$_2$Si segments meet; however, the axial segment must also be able to intrude into an oxide shell surrounding the nanowire to provide electrostatic isolation from the gate. The Pt$_2$Si segments do not meet this second criterion, and therefore, are not suitable candidates to study in the wrap-around gate Schottky diode structure. Furthermore, for
incorporation into the wrap-around gate structure, silicide segment lengths should be at least 1 μm in length, and here we find segment lengths no longer than 400 nm.

**Pd – SiNW Solid-State Reactions**

**Pd Silicide Thin Film Formation Review**

In the solid state reaction between thin films of Pd and Si wafers, Pd$_2$Si is the first phase observed to form. The Pd-Si phase diagram is shown in Figure 3-12. Pd$_2$Si begins forming after annealing at temperatures of 250°C and greater$^{75,76,77}$. Chen and Chen$^{77}$ found that over a temperature range of 250 – 800°C epitaxial Pd$_2$Si formed on Si wafers, and in the temperature range of 850 - 1000°C PdSi begins forming. Pd$_2$Si crystallizes with the hexagonal Fe$_2$P prototype structure (space group P6$_2$m), and PdSi has the orthorhombic MnP prototype structure (Pbnm)$^{72}$. Interestingly, Pd$_2$Si forms with an epitaxial orientation relationship to the Si substrate with the relation [0001]Pd$_2$Si//[111]Si and (060)Pd$_2$Si//(022)Si, which is not completely surprising because of the similarities in the symmetry commonly observed along the c-axis of certain hexagonal structures and the [111] direction of many cubic structures. Through the use of marker experiments, researchers have found that both Si and Pd diffuse in the formation of Pd$_2$Si. To date, no published reports on Pd silicide formation by solid state reaction with SiNWs exist to the best of the author’s knowledge.
Pd/SiNW Solid State Reaction Results

For the study of the reaction between Pd contact pads and SiNWs, samples were fabricated in the same way described in Chapter 2, here the exception being that 80 nm of Pd was e-beam evaporated. Samples were annealed ex-situ at temperatures of 350, 400, 450, 550, and 700°C for 2 min in an RTA furnace purged with UHP Ar. SiNWs used in this study are grown under identical conditions to those described for the Ti, V, and Pt reactions with SiNWs; however, we also studied the reaction of Pd with oxidized SiNWs. The SiNWs that were oxidized were [112] n-type SiNWs and they were oxidized in O₂ in a furnace at 900°C for 15 min with the addition of trichloroethane (TCA). In this case, n-type wires were chosen because of their possible implementation into the wrap-around gate Schottky diode structure described in Chapter 1 to study the Schottky barrier height of Pd silicide contacts to n-type SiNWs.
After annealing samples with 80 nm of Pd on [112] growth direction SiNWs at 350°C for 2 min, we find that axial Pd silicide segments form. The Pd silicide segment grows to an average length of 280 nm, and the surface morphology of the Pd silicide segment is extremely rough, as shown in the TEM image in Figure 3-13(a). Annealing of Pd on [112] SiNWs at 400°C for 2 min (Figure 3-13(b)) results in continued growth of the Pd silicide segment to an average length of 540 nm, again with a rough morphology. Higher temperature anneals for the [112] SiNWs at 450°C (Figure 3-13(c)) and 700°C (Figure 3-13(d)) for 2 min result in a continued increase in the length of the Pd silicide segment to average lengths of 1.12 μm and 4.54 μm, respectively. A plot of the Pd silicide length with SiNWs with the [112] growth direction as a function of annealing temperature for 2 min is shown in Figure 3-14. As can be seen from Figure 3-13, Pd silicide segments formed at all temperatures have a rough surface morphology. The axial Pd silicide segment forms at all temperatures as a polycrystalline segment. All SAED patterns from individual grains along the Pd silicide segments can be indexed as Pd$_2$Si. Insets in Figure 3-13 show diffraction patterns indexed as Pd$_2$Si at annealing temperatures of 350, 400, 450, and 700°C.
Figure 3-13: TEM micrographs of Pd contact pads on SiNWs annealed at (a) 350°C, (b) 400°C, (c) 450°C, and (d) 700°C for 2 min showing the axial growth of the Pd$_2$Si segments and the increase in length of the Pd$_2$Si segments with increasing temperature. Insets are indexed electron diffraction patterns from the Pd silicide segment identified as Pd$_2$Si. Note in (d) the Pd pad has agglomerated and the large dark droplets are pure Pd as identified by electron diffraction patterns.
Figure 3-14: Plots of Pd silicide length as a function of temperature for isochronal anneals of 2 min. In (a) the Pd$_2$Si length is shown on a linear scale and in (b) the length is shown on a log scale as a function of inverse temperature to show the Arrhenius type behavior.

Figure 3-15 shows a low magnification TEM micrograph of a sample annealed at 700°C. Although solid-state reaction has occurred, and long Pd$_2$Si segments are formed, the Pd contact pad itself has balled up on the surface. This situation is problematic from the perspective of making electrical measurements on Pd$_2$Si segments, since the islands of Pd are not all in direct
contact and the underlying SiNₓ is electrically insulating. In order to contact these devices, a successive photolithography step would be necessary in order to make electrical contact to the nanowire. Electron diffraction patterns collected from the Pd islands are indexed as pure Pd, suggesting that no intermetallic compound has formed through the reaction of the Pd with the SiNₓ. Pd agglomeration because of surface energy minimization considerations in the thin (80 nm) Pd film could be responsible for the island formation.

![Figure 3-15: Low magnification TEM image of Pd contact pads after annealing at 700°C showing that the Pd has wet the SiNₓ membrane and then balled up during annealing.](image)

During the solid state reaction of Pd contact pads with oxidized SiNWs, Pd again diffuses into the wire and an axial Pd$_2$Si (identified by SAED patterns) is formed. Unlike the Pt silicide segments formed during the reaction of Pt with oxidized SiNWs, in which the Pt silicide segment stops growing when it has reached the oxidized portion of the SiNW, the Pd$_2$Si segments continue reacting down the wire. However, rather than just reacting with the Si core of the NW, the Pd$_2$Si also partially reacts through the oxide shell surrounding the core of the SiNW. The degradation
of the dielectric oxide shell surrounding the SiNW limits the application of axial Pd$_2$Si contacts to wrap-around gate Schottky diodes to study the Schottky barrier height of the contacts, or for use in nanowire FETs. Figure 3-16 shows a TEM micrograph of a sample with oxidized SiNWs annealed at 450°C for 2 min. It is clear that the oxide shell is still intact in some regions along the silicide segment; however, the irregular morphology of the Pd$_2$Si segment shows that reaction has occurred through the oxide shell surrounding the nanowire. Higher magnification TEM images (Figure 3-16(b)) show that there is no longer any oxide shell on the surface of these regions where it appears the Pd$_2$Si has reacted through the oxide shell.

![Figure 3-16: TEM micrographs of the reaction of a Pd contact pad with a SiNW after annealing at 450°C for 2 min. The higher magnification image clearly shows that Pd silicide has reacted through the amorphous SiO$_2$ layer covering the surface of the SiNW.](image)

Similar to the previous studies on Pt silicide formation in thin films, oxygen contamination effects on Pd$_2$Si formation in thin films have also been studied. Foll and Ho$^{73}$ reported on the formation of Pd$_2$Si with a 3 nm oxide layer at the interface initially between the Pd film and Si wafer. They found that compared to reactions with no oxide layer at the interface, the interface between the Pd$_2$Si and the Si was very rough when an intentional 3 nm thick oxide
was present at the interface. Additionally, the surface morphology of the sample with the intentional 3 nm oxide was much rougher (approximately 30 nm amplitude) compared to that of the samples with no oxide at the interface. Furthermore, Scott et al.\textsuperscript{74} studied the effect of a 2.4 nm thick oxide at the interface between a Pd thin film and Si wafer on the reaction. Scott et al. found that unlike the exaggerated retardation of reaction observed for Pt, Pd thin films would react through the oxide layer at temperatures as low as 400°C. Compared to the Pt case, an argument was made that the relative mobility of Pd through the oxide layer is greater than that of Pt and this mobility leads to the formation of Pd$_2$Si at lower temperatures in the presence of an oxide layer compared to the higher temperatures required for Pt$_2$Si formation when an oxide layer is present at the interface.

From these experiments, we can determine that Pd$_2$Si contacts to SiNWs are not suitable for being studied in the wrap-around gate Schottky diode structure or for nanowire FETs. Due to the reaction through the oxide shell surrounding the SiNWs, electrostatic isolation between the Schottky contact and gate would be difficult to achieve without additional photolithography and deposition steps.

**Ni Solid-State Reaction with SiNWs**

**Ni Silicide Thin Film Formation Review**

In planar metal-oxide-semiconductor field-effect transistors (MOSFETs), the use of nickel monosilicide (NiSi) as an Ohmic contact material has recently become attractive; however, there are a number of different phases in the Ni-Si system (Figure 3-17) and an understanding of the formation and thermal stability of NiSi in different geometries is of great interest. In the past, scaling has lead to problems with the Ti-Si and Co-Si systems for the formation of phases with
low electrical resistivity. Previously, Chang et al.\textsuperscript{78} has observed that the formation of NiSi\textsubscript{2} could occur at much lower temperatures than normally observed in contacting Si through openings in SiO\textsubscript{2} less than approximately 100 nm\textsuperscript{2} in size. It is expected here that in the formation of axial Ni silicide contacts to SiNWs, the nanowire geometry can play an increased role in the Ni silicide phase formation.

\textbf{Figure 3-17:} Ni-Si phase diagram from ASM Handbook\textsuperscript{55}.

Differences have previously been identified between the reaction of Ni/Si bulk diffusion couples and thin films of Ni on Si\textsuperscript{79,80}. The most notable difference is the sequential phase formation encountered in thin films versus the simultaneous phase formation observed in bulk diffusion couples. In a bulk diffusion couple, the Ni and Si supplies are large enough that neither becomes limited. Additionally, the bulk couples are generally held at high temperature for long times, resulting in reaction regions with thicknesses on the order of microns and allowing all thermodynamically stable phases on the phase diagram to grow simultaneously. It has also been
observed that the phases grow in thicknesses proportional to their relative interdiffusion coefficients. On the other hand, in a reaction of a Ni thin film on a Si wafer, a sequential phase formation occurs. Typically, \( \delta\)-Ni\(_2\)Si initially grows because its interdiffusion coefficient is highest at low reaction temperatures \( (<400 \, ^\circ \text{C}) \). All of the Ni film is consumed in this reaction, and \( \delta\)-Ni\(_2\)Si is the only phase that usually forms. Following the complete consumption of Ni and formation of \( \delta\)-Ni\(_2\)Si, NiSi begins forming via the reaction of \( \delta\)-Ni\(_2\)Si with the underlying Si wafer. NiSi is stable until high temperature (greater than 700 °C), at which NiSi\(_2\) begins nucleating. The NiSi and NiSi\(_2\) phases have similar free energies of formation; hence, there is only a small driving force for formation of NiSi\(_2\), resulting in a nucleation barrier, which explains why NiSi\(_2\) usually forms only at high temperatures.

Note that in these thin film reactions, it has been concluded that grain boundary diffusion plays an important role in the formation of \( \delta\)-Ni\(_2\)Si. Activation energies commonly observed for the formation of \( \delta\)-Ni\(_2\)Si are about 1.3 – 1.5 eV/atom. Ciccariello et al. studied the differences in activation energy of grain boundary and lattice diffusion using radioactive Ge and Ni isotopes as tracers to monitor diffusion. Ge was chosen as a substitute for Si because no radioactive Si tracers were available. They identified that grain boundary diffusion had significantly lower activation energy (1.71 eV/atom) than lattice diffusion (2.48 eV/atom). If single crystal silicide segments form from SiNWs, there are no grain boundaries to act as a short-circuit pathway to diffusion, but, due to the large surface area to volume ratio for nanowires, the surface or silicide/SiO\(_2\) interface may act as the pathway for fast diffusion.

Deviations exist from the typical thin film reaction described above, particularly for very thin films. Si orientation effects on Ni-silicide formation are also observed in the reactions of extremely thin films of Ni on Si. During silicidation of Ni films that are approximately 10 nm or less in thickness on (111), (011) and (001) Si wafers, epitaxial NiSi\(_2\) formation is reported as the initial phase formed [10,11]. Additionally, Teodorescu et al. found that on (111) and (100)
oriented Si wafers with a thin chemical oxide, epitaxial NiSi$_2$ is the first phase to form at temperatures below 400 °C when 12 nm thick Ni films react with the Si wafers. NiSi$_2$ has the cubic fluorite crystal structure and is lattice-matched well to Si with a mismatch less than 1%. Gibson et al. studied the reaction of thin Ni films on (111) and (100) oriented wafers as well. For the (111) Si wafers, they found that $\theta$-Ni$_2$Si is initially formed at a temperature of 300 °C, and upon further annealing it is converted to epitaxial NiSi$_2$. Interestingly, the $\theta$-Ni$_2$Si phase is not expected to grow according to the phase diagram until temperatures in excess of 825°C. The $\theta$-Ni$_2$Si (001) plane is extremely similar to the Si (111) plane. The in-plane bond distances on the (001) plane of $\theta$-Ni$_2$Si are 3.836 Å with an angle between rows of atoms of 60°. This compares very well with the Si (111) plane that has in-plane spacings of 3.84 Å and an angle between bonds of 60°. Part of the explanation for the early formation of $\theta$-Ni$_2$Si when very thin Ni films are deposited on (111) Si is that the excellent lattice match minimizes the free energy of the system, because in very thin films (1–2 nm thick), a large fraction of atoms initially lie at the Ni/Si interface. However, in a reaction of the same very thin Ni films on (100) oriented wafers, the $\theta$-Ni$_2$Si phase is not observed because the absence of four-fold symmetry in the hexagonal structure does not allow for a good epitaxial match between $\theta$-Ni$_2$Si and Si in this particular orientation.

In the limited work available on the silicidation of SiNWs by Ni, one finds several differences in phases observed and no evidence of a sequential phase formation. Appenzeller et al. reported that Ni$_2$Si (not identified as $\delta$ or $\theta$-Ni$_2$Si or supported by diffraction data) formed axially along the SiNW after annealing for 30 s at 280 °C. Lu et al. found NiSi under annealing conditions in the range of 500–650 °C for Ni-silicidation of [111] SiNWs. Sheu et al. and Wu et al. also observed NiSi. Results obtained by Wu et al. differ from others in that no significant lateral diffusion was observed after silicidation despite the high temperature (550 °C),
long time (5 min) and secondary annealing step carried out at 600 °C. This lack of lateral diffusion was verified in their work by the fact that the silicide segment length was approximately equal to the patterned Ni stripe deposited on top of the SiNW. The experimental setup of Lu et al. differs from our study and other studies because they reacted Ni nanowires in point contact with SiNWs and observed silicide formation at the ends of the SiNW, not at the Ni/Si contact region. Zhang et al.\textsuperscript{92} have identified predominantly δ-Ni\textsubscript{2}Si forming over a range of annealing conditions from 500–950 °C for 30 s using polycrystalline SiNWs, with traces of NiSi, Ni\textsubscript{3}Si\textsubscript{2} and θ-Ni\textsubscript{2}Si identified at different temperatures. Additionally, Weber et al.\textsuperscript{93} have reported the formation of single crystalline NiSi\textsubscript{2} after siliciding [110] SiNWs using electrolessly deposited Ni pads at an annealing temperature of 480 °C. These studies further suggest that differences may exist in the phase formation sequence of Ni silicide in SiNWs compared to their bulk and thin film counterparts.

**Ni/SiNW Solid State Reaction Results**

For the study of the reaction between Ni contact pads and SiNWs, samples were fabricated in the same way described in Chapter 2, here the exception being that 80 nm of Ni was e-beam evaporated. Samples were annealed ex-situ at temperatures of 300, 350, 400, 450, 500, 550, 600 and 700°C for 0, 2, 4, 8 and 12 min in an RTA furnace purged with UHP Ar. SiNWs used in this study are grown under identical conditions to those described for the Ti, V, Pt, and Pd reactions with SiNWs; however, we also studied the reaction of Ni with oxidized SiNWs. Note for the [112] SiNWs the doping was lightly p-type and for the [111] SiNWs there was no doping. The SiNWs that were oxidized were [112] n-type SiNWs and they were oxidized in O\textsubscript{2} in a furnace at 900°C for 15 min with the addition of trichloroethane (TCA). In this case, n-type wires were chosen because of their possible implementation into the wrap-around gate Schottky
diode structure described in Chapter 1 to study the Schottky barrier height of Ni silicide contacts to n-type SiNWs.

**Reaction of Ni with [112] SiNWs**

After samples were annealed at 300 °C for 2 min, no visible reaction between the Ni and SiNW is observed. After annealing at 350 °C, Ni silicide formation down the wire is observed with an average length of 50 nm. It is expected that Ni will diffuse into the SiNW and form an axial silicide segment along the SiNW because Ni is the dominant diffusing species in the phases in the Ni-Si system\(^94\). Further Ni silicide formation can be identified at 400 °C by the image contrast change along the SiNW, as shown in Figure 3-18(a). The SAED patterns from the silicide (Figure 3-18(b) and (c)) show that the silicide formed is hexagonal \(\theta\)-Ni\(_2\)Si, the same phase observed at 350 °C. When possible, two patterns were taken by tilting to different zone axes, specifically the [401] and [201] directions, and the angle tilted matched the angle between these two directions in the hexagonal system. It should be noted that \(\theta\)-Ni\(_2\)Si is a metastable phase under these annealing conditions, and should not be observed according to the phase diagram until temperatures above 825 °C\(^95\). The \(\theta\)-Ni\(_2\)Si nanowire segment is single crystalline, and has a slightly larger diameter than the original diameter of the unconverted SiNW, which is expected because of the volume increase due to the formation of \(\theta\)-Ni\(_2\)Si.
Figure 3-18: (a) TEM image showing sample annealed at 400 °C for 2 min and (b) SAED patterns from samples annealed at 400 °C for 2 min identified as θ-Ni$_2$Si by the (b) [201] and (c) [001] zone axis diffraction patterns.

Figure 3-19 shows a TEM image of a sample which was annealed at 300 °C for 2 min and then at 450 °C for 2 min, which are the conditions that were used by a previous student to form a Ni-silicide Schottky contact to a SiNW for preliminary studies of the Schottky barrier height\textsuperscript{96}. The 300 °C pre-annealing does not cause significant silicidation axially down the SiNW, and it was observed in the present work that similar results were obtained using a single anneal at 450 °C for 2 min. It can be seen that silicidation occurs at 450 °C and the silicide travels on average 500 nm, compared to an average of 150 nm at 400 °C. From Figure 3-19 it is apparent that the NW can be divided into three sections, each identified by a change in NW diameter. Section I is the unconverted SiNW, which has a diameter of 59 nm. The SAED pattern shows that the growth direction of the SiNW was [112]. Section II has been converted into θ-Ni$_2$Si, as again confirmed by SAED. Section II has slightly larger diameter (65 nm at the
maximum or a 10% increase) compared to the unconverted SiNW, but the diameter is close to the unconverted SiNW diameter at the growth front. By comparing the SAED patterns between the silicide and Si, the epitaxial orientation relationship between the $\theta$-Ni$_2$Si and SiNW is found to be $\theta$-Ni$_2$Si[001]/Si[11\overline{1}] and $\theta$-Ni$_2$Si(100)/Si(112). Section III is close to the Ni pad and has a much larger diameter (72 nm). This section was not found in the samples annealed at lower temperatures. Unfortunately, the SAED patterns (not shown) did not provide conclusive phase identification. The patterns obtained from these regions do have large lattice spacings that rule out all but the Ni$_{11}$Si$_{12}$ and Ni$_3$Si$_2$ phases. Of these phases, Ni$_{11}$Si$_{12}$ seems more likely because an intermediate phase between the pure Ni pad and $\theta$-Ni$_2$Si should not have a composition more Si-rich than the $\theta$-Ni$_2$Si phase.

![Figure 3-19](image.png)

**Figure 3-19:** TEM image showing samples annealed at 300 °C for 2 min and then 450 °C for 2 min, with an epitaxial relation of $\theta$-Ni$_2$Si[001]/Si[11\overline{1}] and $\theta$-Ni$_2$Si(100)/Si(112). The nanowire is split into three regions; region I is the original SiNW, region II is $\theta$-Ni$_2$Si, and region III is an unidentified Ni-rich silicide phase.
From the electron diffraction data we have identified the epitaxial orientation relationship of $\theta$-Ni$_2$Si[001]/Si[11 $\overline{1}$] and $\theta$-Ni$_2$Si(100)/Si(112). Interestingly, for the (100) $\theta$-Ni$_2$Si and (112) Si planes, there is a very good lattice match (Figure 3-20), and therefore it is not surprising that the planes coincide at the interface between the silicide segment and the SiNW. For $\theta$-Ni$_2$Si, the (100) in-plane bond distances are 2.474 Å and 3.836 Å with a bond angle of 90°, which compares well with that of the (112) Si in-plane bond distances of 2.35 Å and 3.840 Å with a bond angle of 90°. This results in a -5.1% mismatch in one direction and 0.1% mismatch in the other direction. Additionally, the cross-section of a [112] oriented wire is nearly rectangular with the two long sides being bound by (111) type planes and the other two by a combination of (110) and (311) type planes$^9$. These surfaces surrounding the SiNW are important to recognize because they will be the point of initial contact between the Ni film and SiNW. As mentioned above, $\theta$-Ni$_2$Si is nearly perfectly lattice matched to the Si (111) surface in that the (001) in-plane spacing is 3.836 Å compared to 3.840 Å for the Si (111) in-plane spacing, and both have bond angles of 60°. Thus, an epitaxial arrangement is favorable over much of the original circumference of the SiNW as well. Although there is not a good lattice match for the (110) and (311) planes, these planes comprise a smaller fraction of the overall surface area of the original SiNW compared to the (111) planes where the $\theta$-Ni$_2$Si can initially nucleate and then grow.
Samples were also annealed at temperatures of 500, 600 and 700 °C for 2 min each. In each case, the phase observed was again θ-Ni$_2$Si, consistent with the samples annealed at lower temperatures. However, after annealing at 700 °C for 2 min, branches were observed to form from the main θ-Ni$_2$Si silicided nanowire (Figure 3-21). Using SAED, the branches were also observed to be the same phase as the main silicide segment, θ-Ni$_2$Si. However, extra diffraction spots were also observed in the SAED patterns from the θ-Ni$_2$Si silicide segments. These extra spots are attributed to micro-twinning, which can be observed from the inset in Figure 3-21(b), and can be caused by large compressive stresses. The direction along which the micro-twins formed and the additional spots observed in the diffraction pattern are consistent when the
microscope’s rotation calibration is considered. This rotation calibration is necessary because the electrons do not travel in a straight path down the column of the microscope. The Lorentz force exerted on the electrons causes them to travel in a helical path and for some microscopes the rotation is not accounted for and by changing magnification the image will rotate. Interestingly, the native oxide thickness may not be uniform around the SiNW. As observed by TEM, branches form at locations where the silicide has broken through the oxide, providing further evidence that the $\theta$-Ni$_2$Si phase is under a large compressive stress. The large indiffusion of Ni compared to the negligible outdiffusion of Si and increase in volume of the $\theta$-Ni$_2$Si phase compared to the original Si volume are all reasons for compressive stress to build in the nanowire. The mechanism for formation of these branches may be similar to the formation of Sn whiskers encountered in electronic packaging$^{98}$. In any case, it is a significant phenomenon because in the use of SiNWs for electronic devices, these branches could cause shorts between two neighboring devices.
Figure 3-21: (a) TEM image showing overview of a sample annealed at 700 °C for 2 min and (b) higher magnification image. Diffraction patterns (c) and (d) from the main silicide segment (trunk), where (c) and (d) show extra spots from micro-twinning and (e) shows the diffraction pattern from a branch, showing that the branch is the same δ-Ni₂Si phase as the main part of the nanowire, but without the extra spots from the micro-twins.

For the implementation of the axial δ-Ni₂Si nanowire segments into wrap around gate Schottky diodes, the silicide segment must be able to intrude into an oxidized SiNW, consuming the Si core and leaving the SiO₂ layer intact. The SiO₂ layer is integral in the performance of the wrap around gate Schottky diodes, and reduction of the oxide will lead to undesirable device transfer characteristics. As we previously observed for the Pt-SiNW and Pd-SiNW, systems there can be problems with the compatibility of these axial silicide segments forming through the core of the oxidized SiNWs without affecting the gate dielectric (SiO₂) layer. Figure 3-22 shows a TEM micrograph of a sample annealed at 500°C for 2 min. The SiO₂ shell clearly still remains after silicidation and is covering the δ-Ni₂Si nanowire segment. This experiment shows that the
0-Ni\textsubscript{2}Si segments will be suitable candidates for studying their Schottky barrier height in the wrap around gate Schottky diode structure, and results will be discussed in Chapter 4.

Figure 3-22: (a) Low-magnification TEM image of an oxidized SiNW after annealing at 500°C for 2 min to form an axial Ni silicide segment. From the higher magnification image in (b), we can see the oxide shell remains intact on the surface of the Ni silicide segment and the SiNW after formation of the axial Ni silicide segment.

Reaction of Ni with [111] SiNWs

The SiNWs with a [111] growth direction were also silicided by the method described above with 80 nm of Ni. Annealing at 450 °C for 2 min again results in a silicide forming axially down the SiNW. However, in the case of the [111] oriented SiNWs, the silicide phase is identified as NiSi\textsubscript{2} by SAED. Figure 3-23 shows an HRTEM image of a silicided SiNW with insets of digital Fourier transforms (FTs) from the silicide segment and the SiNW. From the FTs we can determine that an epitaxial orientation exists between the NiSi\textsubscript{2} segment and SiNW. The epitaxial relation is identified as NiSi\textsubscript{2}[\{1\ 1\ 0\}\//Si[\{1\ 1\ 0\}] and NiSi\textsubscript{2}(111)//Si(111). From the HRTEM image in Figure 3-23(b) we can also deduce that the NiSi\textsubscript{2}/Si interface is atomically abrupt. Similar to the case of the in-plane spacings being well-matched for the (100) 0-Ni\textsubscript{2}Si and
(112) Si planes, the in-plane spacings of the (111) NiSi₂ and (111) Si planes are also very well lattice-matched. A schematic of the surface planes and planes along the growth direction is shown in Figure 3-24. The in-plane mismatch between the atomic spacings on the (111) NiSi₂ and (111) Si planes is only 0.9%. In addition to having a good lattice match along the growth direction, there is lattice matching to the surface of the SiNW as well, which is what was originally contacted by the Ni pad. The cross-section of a [111] growth direction SiNW is hexagonal, being bound on all six facets by (112) type planes. The in-plane spacings for NiSi₂ along the (112) direction are 3.80 and 2.33 Å and have only a 0.9% mismatch to the in-plane Si spacings of 3.84 Å and 2.35 Å.

Figure 3-23: (a) Ni-silicided [111] oriented SiNW after annealing at 450 °C for 2 min and (b) HRTEM image of silicide/SiNW interface. The inset FTs are identified as the [1 1 0] NiSi₂ zone axis and the [1 1 0] Si zone axis with an epitaxial relation of NiSi₂[1 1 0]//Si[1 1 0] and NiSi₂(111)//Si(111).
Figure 3-24: Schematic diagrams of the (112) and (111) Si planes compared to the (112) and (111) NiSi$_2$ planes showing there is good lattice match between the growth direction of the NiSi$_2$, the Si nanowire and between the surface planes of the Si nanowire and the NiSi$_2$.

To corroborate the SAED and FTs, EELS spectra were collected on Ni-silicided SiNWs with [112] and [111] growth directions. Cheynet and Pantel$^{100}$ reported a shift to higher energies with increasing Si content in the Ni L$_{2,3}$ edge of EELS spectra for thin film Ni-silicides. Since absolute energy positions are difficult to monitor because of instabilities and drift effects on the EELS spectrometer, spectra were collected from the Ni pad as well as the silicide segments. The Ni L$_{2,3}$ edge from the Ni pad was used as a standard, and the shifts were measured from the Ni pad Ni L$_{2,3}$ edge since the Ni pad is common to both types of samples (diffraction patterns from the Ni pad confirmed that the Ni pad had not reacted with the underlying SiN$_x$ window). EELS spectra from Ni, 0-Ni$_2$Si and NiSi$_2$ are shown in Figure 3-25. We observe a shift in energy of 1
eV for $\theta$-Ni$_2$Si relative to Ni, and a shift of 2.5 eV for NiSi$_2$ relative to Ni representing a net shift of 1.5 eV between the two silicide phases observed. The shift in the Ni L$_{2,3}$ edge to higher energies is caused by the reduced hybridization of Ni d states with Si p states, causing Si-rich silicides to have the Ni L$_{2,3}$ edge at higher energies. This finding is in agreement with and corroborates our analysis from the SAED and FT patterns.

**Figure 3-25:** EELS spectra showing the Ni L$_{2,3}$ edge for pure Ni, $\theta$-Ni$_2$Si and NiSi$_2$ showing a shift from pure Ni at the lowest energy to higher energy from $\theta$-Ni$_2$Si and NiSi$_2$ at the highest energy.

The solid state reaction between the Ni contact pads and [111] SiNWs was also studied at higher temperatures. In this case, the SAED shows the formation of the low-resistivity NiSi phase after annealing at temperatures in excess of 600°C. Figure 3-26 shows a TEM image of the silicided [111] oriented SiNW after annealing at 700°C for 2 min. In contrast to the SiNWs with [112] growth directions silicided at 700 °C, no branches are observed to form. Both of the ratios of the volume of NiSi$_2$ and NiSi to Si per Si atom are smaller than that for $\theta$-Ni$_2$Si compared to
Si. This suggests that less compressive stress would build up in the constrained nanowire geometry and explains why no branches emerge from the silicided [111] SiNWs.

Figure 3-26: TEM image of SiNW silicided by Ni pad at 700 °C for 2 min. Inset shows SAED pattern of the NiSi [103] zone axis.

The formation of NiSi in the SiNWs with [111] growth directions is also consistent with what is observed in silicidation of (111) oriented Si wafers by very thin Ni films. In the planar silicidation case, NiSi$_2$ is observed to form epitaxially at approximately 400 °C, and upon continued reaction at increased time and temperature, the NiSi$_2$ is converted to NiSi. NiSi remains stable until temperatures above 700 °C, where NiSi$_2$ begins nucleating. We suspect the same may occur in the nanowire silicidation; however, the SiN$_x$ membranes used to fabricate the TEM samples could not be annealed at temperatures much greater than 700 °C without cracking.

Comparison of Results to Previous Nanowire Studies

In comparison of our results to others, the only previous studies that explicitly mention the orientation of the SiNW and identify the silicide phase that forms are those by Lu et al., Wu et al., and Weber et al. Lu et al. used [111] oriented SiNWs in point contact with NiNWs and found
NiSi to form over a range of annealing temperatures of 500 – 650 °C. It is also worth mentioning that important differences may exist in the reaction of NiNWs with SiNWs compared to a Ni pad with SiNWs. In fact, in the NiNW/SiNW reaction, the silicide forms at the ends of the SiNW, not at the NiNW/SiNW interface. This differs from our work and others who have observed the silicide to form at the interface between a Ni pad and SiNW. Our initial annealing condition of 450 °C is also lower than the lowest temperature studied by Lu et al., which was 500 °C. Conversely, the work by Wu et al. shows NiSi formation on a [112] oriented SiNW, differing from the θ-Ni₂Si phase we identified to form after annealing from 350 – 700 °C. However, the annealing and processing conditions of Wu et al. differ significantly from our work as well. Wu et al. annealed at a temperature of 500 °C for 5 min, then etched the Ni pad and proceeded with a secondary anneal at 600 °C for an unspecified time period. They also used a very narrow Ni line to contact the SiNW and saw negligible lateral diffusion from the Ni source, contrary to the large lateral diffusion we and others have observed when using a large Ni pad to supply the silicidation reaction. We suspect that in the case of a thin Ni strip contacting the SiNW, the supply of Ni is cut off before enough Ni is able to diffuse into the SiNW to grow a long axial segment. The combination of the Ni supply being cut off during the reaction, and also complete removal of the Ni by etching followed by a secondary anneal, makes it difficult to compare the reaction products encountered in each of the experiments.

Weber et al. studied the silicidation of [110] SiNWs and found that NiSi₂ formed after annealing at 480 °C. The cross-section of a [110] SiNW is triangular and bound by (111) planes. Both the θ-Ni₂Si and NiSi₂ phases are well lattice-matched to (111) Si, and the θ-Ni₂Si phase is actually slightly better matched to Si on this plane, so one might expect it to be found in these conditions given our findings. However, the growth direction of the SiNW is [110]. There is a poor lattice match between the (110) Si plane and any orientation of the θ-Ni₂Si phase; however, NiSi₂ is matched with only a 0.9% mismatch in-plane with (110) Si. It seems from these relations
identified that both the initial SiNW interface that the Ni supply is in contact with, as well as the growth front of the silicide, are important factors in determining silicide phase formation and stability in SiNWs.

**Kinetics of Ni Silicide Formation for [111] and [112] SiNWs**

In the previous section, all samples were annealed isochronally for 2 min to study the phase formed at different temperatures as well as any change in the phase formed by annealing at higher temperatures. In the following section, silicide lengths were studied as a function of temperature and time in order to determine the kinetics and identify rate limiting steps in the reactions for the [111] and [112] SiNWs and determine any differences between the two. The average diameters of the SiNWs with [112] and [111] growth directions were 60 and 63 nm, respectively, with diameters ranging from as low as 50 to as high as 75 nm for both types of SiNWs. Note, a small range in diameters was specifically chosen for the study of kinetics of Ni silicide formation because the silicide growth length has been shown in a previous study by Appenzeller *et al.*\(^87\) to depend on the diameter of the SiNW. For example, Figure 3-27 shows a plot of Ni silicide length versus diameter for an annealing condition of 450°C for 8 min on SiNWs with a [112] growth direction. An FE-SEM (Leo 1530) was used to measure the silicide lengths, and the growth directions were determined by the surface morphology of the SiNW segment. As mentioned previously, the [111] SiNWs have a hexagonal cross-section and the [112] SiNWs have a rectangular cross-section. In the FE-SEM we can see the facets and determine the growth direction of the SiNW. Figure 3-28 shows a FE-SEM image of a nanowire annealed at 450°C, and it is clear we can determine from the contrast changes along the length of the nanowire the length of the silicide segment as well as the growth direction.
Figure 3-27: Plot of Ni silicide length versus SiNW diameter showing a diameter dependence on the length of Ni silicide formed for an annealing condition of 450°C for 8 min using SiNWs with a [112] growth direction.

Figure 3-28: FE-SEM image of [111] SiNW with an axial Ni silicide segment that has been formed after annealing at 450°C. The growth direction of the SiNW can be determined from the faceting of the SiNW and the silicide length can be determined by the contrast difference generated in the image because of the mass differences between Ni and Si.
A plot of the silicide length as a function of time for different temperatures for the [112] growth direction SiNWs is shown in Figure 3-29(a). Note, the silicide length has been found in a previous study by Appenzeller et al. to have a diameter dependence and for this reason nanowires with average diameters of 65 nm were compared at each of the annealing conditions to eliminate any effect of the diameter dependence on the study of the kinetics. It is clear that the time dependence is not linear, but is parabolic in nature. This parabolic time dependence of the growth is indicative of a diffusion limited reaction. The growing silicide phase was identified by the earlier TEM study as $\theta$-Ni$_2$Si. The $\theta$-Ni$_2$Si is a high-temperature phase in the Ni-Si system and usually not encountered in thin film reactions; therefore, there is limited information about any kinetic parameters limiting the growth of this phase such as the activation energy of diffusion through the bulk and/or lattice. However, for the low-temperature orthorhombic structured $\delta$-Ni$_2$Si many studies have been performed to analyze the kinetics of growth. The activation energy for the growth of this phase is typically 1.3 – 1.5 eV/atom and is limited by grain boundary diffusion of Ni through the growing $\delta$-Ni$_2$Si layer. From the plot of the natural logarithm of the $\theta$-Ni$_2$Si growth constant versus $1/kT$ (Figure 3-29(b)), where $k$ is Boltzmann’s constant and $T$ is temperature, we extract an activation energy of 1.45 ± 0.07 eV/atom. Furthermore, this value compares favorably with the activation energy observed (1.4 eV/atom) for lateral diffusion couples forming $\delta$-Ni$_2$Si. This value does fall well within the range of activation energies identified for formation of the low-temperature $\delta$-Ni$_2$Si phase. A major difference between our nanowire geometry and the thin film geometry is that for the thin film case, a polycrystalline $\delta$-Ni$_2$Si layer can form with grain boundaries acting as fast pathways for diffusion. For the single crystal $\theta$-Ni$_2$Si nanowire segment, there are no grain boundaries; however, the SiO$_2$/$\theta$-Ni$_2$Si interface may act as a fast pathway for diffusion. Therefore, the rate limiting mechanism for the formation of the $\theta$-Ni$_2$Si segment is diffusion of Ni along the SiNW/SiO$_2$ interface. Note that it is
not a free exposed Si surface the Ni is diffusing along in this situation. Since we observe similar results for θ-Ni$_2$Si nanowire segment lengths for intentionally oxidized and as-grown SiNWs, we can conclude that Ni is not diffusing on the free surface, because in that situation it would also have to diffuse through the SiO$_2$ layer to react with the Si core. Previous studies have shown that the reaction of Ni is retarded by the presence of even thin layers of SiO$_2$, and surely a 10 – 15 nm thick SiO$_x$ layer would greatly inhibit this reaction. Therefore, the Ni is likely diffusing by diffusion along the Si/SiO$_2$ interface.
Figure 3-29: Kinetic data for silicide length versus time for the [112] SiNWs shown on a linear scale in (a). The growth with time is parabolic, indicated by the linear relationship in the (b) silicide length squared versus time plot. The inset shows the length squared versus time to demonstrate the parabolic time dependence. An Arrhenius plot revealing an activation energy for \( \theta \)-Ni\(_2\)Si formation of 1.45 ± 0.07 eV/atom is shown in (b).
In the case of the NiSi$_2$ growth in the [111] SiNWs, the time dependence of the growth of the NiSi$_2$ nanowire segment is linear (Figure 3-30(a)) for temperatures of 400, 450, and 500°C. However, at 550°C the relationship is between growth length and time is not exactly linear. This nonlinearity may be due to a combination of linear and parabolic time dependent processes limiting the growth at high temperature. For instance, the growth may be linear at times less than 4 min, but then change to parabolic at times greater than 4 min as shown by the data fit in Figure 3-30(a). Linear kinetics typically describe reactions whose rate limiting step is an interfacial reaction. For the [111] SiNWs, the limiting step is the rearrangement of atoms at the NiSi$_2$/SiNW interface to form a layer of NiSi$_2$, rather than diffusion limited as observed for the formation of 0-Ni$_2$Si in the [112] SiNWs. The activation energy extracted from the slope of the plot of the natural log of NiSi$_2$ growth rate versus $1/kT$ (Figure 3-30(b)) was $0.76 \pm 0.10$ eV/atom calculated only using the data from 400, 450, and 500°C. In layer by layer regrowth of NiSi$_2$ achieved by ion bombardment of amorphous NiSi$_2$ films, linear kinetics are also observed with activation energies of $0.9 - 1.2$ eV/atom$^{102,103}$. These activation energies extracted for NiSi$_2$ recrystallization are larger than what we have observed for NiSi$_2$ formation in [111] SiNWs; however, in this case the film must completely recrystallize from the amorphous state to the fluorite structured NiSi$_2$. In our situation, the SiNW is already crystalline and when supplied by the solid state diffusion of Ni, a slight rearrangement of atoms at the interface is necessary for transformation from Si with the diamond cubic structure to the NiSi$_2$, and it may be expected that this would be a lower energy process than complete recrystallization from the amorphous state. Alternatively, Katsman et al.$^{104}$ suggested that the linear growth of silicide nanowire segments could be limited by diffusion from the nanowire periphery; however, in our study the extracted activation energy is much lower than that of grain boundary ($\sim 1.4$ eV/atom) or lattice diffusion (even higher) in nickel silicides.
Figure 3-30: (a) Silicide length versus time for SiNWs with the [111] growth direction. The growth with time is linear indicating an interfacial reaction is the rate limiting step for formation at 400, 450, and 500°C. (b) Arrhenius plot for extraction of an activation energy for NiSi$_2$ formation of 0.76 ± 0.10 eV. Data at 550°C is best fit using a linear relationship until 4 min, followed by a parabolic relationship after 4 min.

Note, the rates of silicide formation differ significantly depending on whether the SiNW growth direction is [111] or [112]. Although the activation energy for NiSi$_2$ growth in the SiNWs with [111] growth directions is lower than that for growth of $\Theta$-Ni$_2$Si in the SiNWs with [112]
growth directions, the growth rate is actually slower for NiSi₂ compared to θ-Ni₂Si. However, the growth rate is not solely determined by the activation energy; the pre-exponential factor for the rate constant also plays a role. In the case of linear kinetics, the length of the silicide segment can be related to the annealing time by the equation, \( L = kt \), where \( L \) is the length of the silicide segment formed, \( k \) is a rate constant, and \( t \) is the annealing time. Furthermore, the rate constant can be expressed as an Arrhenius relation as, \( k = k_0 \exp(-E_a/k_BT) \), where \( k_0 \) is the pre-exponential factor, \( E_a \) is the activation energy, \( k_B \) is Boltzmann’s constant, and \( T \) is temperature. Therefore, on a plot of the natural log of silicide growth rate versus inverse temperature, the slope is related to the activation energy and the intercept is related to the pre-exponential factor. Conversely, for diffusion limited kinetics the silicide length is related to time by the equation, \( L = (k't)^{1/2} \), where \( k' \) is a rate constant. The rate constant, \( k' \), can also be expressed by an Arrhenius relation as, \( k' = k'_0 \exp(-E_a/k_BT) \), where \( k'_0 \) is the pre-exponential factor. In this case, \( k' \) is related to the diffusion coefficients in the growing and adjacent phases. For the case of NiSi₂ growth in the SiNWs with [111] growth directions, the pre-exponential factor, \( k_0 \), is \( 4.8 \times 10^5 \) nm/s, while for θ-Ni₂Si growth in the SiNWs with [112] growth directions the pre-exponential factor, \( k'_0 \), is \( 4.3 \times 10^{13} \) nm²/s. Note, in the case of θ-Ni₂Si the growth length is related to the square root of the pre-exponential factor, while the NiSi₂ growth length is linearly related to the pre-exponential factor.

**Conclusions**

In summary, we have found significant differences in the formation of axial Ni silicide segments when annealing Ni contact pads on SiNWs. For the case of [112] SiNWs, θ-Ni₂Si is the only phase to form and for [111] SiNWs NiSi₂ grows followed by a sequential transformation to NiSi at temperatures in excess of 600°C. We also demonstrated the formation of axial θ-Ni₂Si
through Si/SiO₅ core/shell nanowires leaving the SiO₅ shell intact. This finding suggests the feasibility of using these axial θ-Ni₂Si segments into wrap around gate Schottky diodes for analysis of the Schottky barrier height. This work is the basis of the Schottky barrier height study performed in Chapter 4.

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Chapter 4

Wrap-Around Gate Schottky Diodes

In metal/semiconductor electrical contacts, the Schottky barrier height is the most fundamental parameter that can describe electrical transport at the metal/semiconductor interface. The basics of the theory of formation of the Schottky barrier were described previously in this thesis in Chapter 1, and for a rather thorough review of modern concepts in the theory of Schottky barrier formation and Fermi level pinning, the reader is referred to the review by Tung. In order to study the Schottky barrier height in contacts to nanowires, one would like to identify a method for extracting the true barrier height at the metal/semiconductor interface, rather than an effective barrier height. A review of Schottky barrier height measurements of contacts to nanowires will be given in the following section, followed by a review of the methodology described by Sarpatwari et al. for extracting the true Schottky barrier height of axial contacts to SiNWs. Lastly, the fabrication of wrap-around gate Schottky diodes and analysis of data collected from these diodes will be described.

For review, in order to extract the Schottky barrier height, the forward-bias portion of the current-voltage data is fit by the thermionic emission model (Figure 4-1). At large forward bias, the series resistance can dominate the current transport characteristics of a Schottky diode, and therefore the data is only fit in the regime where on a plot of the natural log of the current versus the voltage is linear. The thermionic emission equation is given by:

\[ J = J_0 \exp(q(V-IR)/nkT) \{ 1 - \exp(-q(V-IR)/kT) \} \]

and \[ J_0 = I_0/A = A^{**}T^2 \exp(-q\Phi_B/kT); \]

where \( J \) is the current density, \( J_0 \) is the saturation current density, \( q \) is the charge of the electron, \( V \) is the applied voltage, \( I \) is the current, \( I_0 \) is the saturation current, \( R \) is the resistance, \( n \) is the ideality factor, \( k \) is Boltzmann’s constant, \( T \) is temperature, \( A \) is area, \( A^{**} \) is Richardson’s
constant, and $\phi_B$ is the Schottky barrier. When the ideality factor exceeds unity, there can be a number of factors responsible, including image force lowering, an increase in the diode current due to tunneling at the metal/semiconductor interface, and barrier height inhomogeneities. The effect of image force lowering depends on the doping density of the semiconductor, but is typically much less than 0.1 eV even for heavily doped semiconductors. Therefore, for the previously described systems where the ideality factors are generally much greater than 1.1, it is expected that tunneling and/or barrier height inhomogeneities are playing an important role in deviation of the effective barrier height compared to the true barrier height.

Figure 4-1: Schematic of absolute value of current-voltage relationship expected from a Schottky diode. The current displayed is on a natural log scale. Under forward bias in region I, the current can be modeled by the thermionic emission equation, and in region II the series resistance of the diode limits current flow. Under reverse bias current flow is limited by the reverse biased Schottky diode.

Schottky Barrier Height Measurements of Contacts to Nanowires

Considering the importance that the Schottky barrier plays in determining the transport characteristics of nanowire-based electrical devices, very little work\textsuperscript{107,108,109,110} has been performed to date on studying nanowire Schottky diodes and analyzing the Schottky barrier.
heights and ideality factors for different contact materials to nanowires. In the study of Au contacts to n-GaN nanowires, Lee et al.\textsuperscript{107} found barrier heights of 0.5 to 0.8 eV with strong temperature dependence. More strikingly, in this study ideality factors ranging from 7 to 11 were found. It is not accurate to call these barrier heights the true Schottky barrier height at the metal semiconductor interface because of these extremely large ideality factors. For Au contacts to n-ZnO nanowires, Das et al.\textsuperscript{108} found barrier heights in the range of 0.4 to 0.65 eV and corresponding ideality factors ranging from 1.1 to 1.6. Though these ideality factors are much closer to the ideal value of 1 than in the study of Au on n-GaN, ideality factors greater than 1 are an indication of additional current transport mechanisms besides purely thermionic emission, and/or barrier height inhomogeneities. Leonard et al.\textsuperscript{109} studied diameter dependent transport properties between Au contacts to GeNWs. They did not extract barrier heights, however, they found ideality factors in the range of 2 to 4. Interestingly, they also found that the small-bias conductance density increased with decreasing nanowire diameter. This effect was attributed to electron-hole recombination being the dominant transport mechanism in these diodes. As the GeNW diameter is decreased, the average distance to the surface, where they suggested electron-hole recombination was mostly occurring, is also decreased and as such the electron-hole recombination time is decreased. Lastly, in the study of Ni and \( \theta \)-Ni\(_2\)Si contacts to n-SiNWs, Woodruff et al.\textsuperscript{109} found barrier heights ranging from 0.26 to 0.49 eV and ideality factors ranging from 1.8 to 4.7 for Ni contacts to n-SiNWs, and barrier heights ranging from 0.52 to 0.69 and ideality factors ranging from 1.1 to 1.2 for \( \theta \)-Ni\(_2\)Si contacts to n-SiNWs. Note, in the first set of values listed in the study by Woodruff et al., the SiNWs were heavily doped n-type, and it was expected that tunneling would play an important role in transport across the metal/semiconductor interface resulting in lower measured effective barrier heights and ideality factors greater than unity.
A likely culprit for the large contribution of tunneling on transport in nanowire contacts is the effect of surface charge. Charge on the surface of the nanowire can create a surface accumulation layer or depletion layer that can have a significant effect on the electrical transport characteristics of a nanowire because of the large surface area to volume ratio of the nanowire. Note, the presence of a surface depletion layer will not increase the tunneling contribution at the surface; however, will result in a barrier width inhomogeneity along the metal/semiconductor interface. An effective way to prevent the non-uniformity in carrier concentration along the radius of the nanowire would be to symmetrically gate the metal/semiconductor interface. Using information we gained in studying the formation of axial silicide contacts in Chapter 3, we know that we can form axial nickel silicide contacts to oxidized SiNWs leaving the SiO$_2$ shell intact. We can then use this SiO$_2$ shell surrounding the nickel silicide/SiNW interface as a gate dielectric, and surround this interface with a metal to apply gate bias and electrostatically change the carrier concentration profile in the nanowire. A schematic image of this type of device called a wrap-around gate Schottky diode is shown in Figure 4-2.
Figure 4-2: Schematic diagram of the wrap-around gate Schottky diode device proposed for extracting the true Schottky barrier height of axial contacts to SiNWs. The device is shown from an angled top-view in (a) and in cross-section in (b).

Introduction to Wrap-Around Gate Schottky Diodes

Sarpatwari et al.\textsuperscript{106} modeled the current-voltage (I-V) relationship for a wrap-around gate Schottky diode. Sentaurus Device simulator was used to study device characteristics by simultaneously solving Poissons equation in 3D and the current continuity equation in 3D with trap statistics. It was found that for n-type SiNWs, negative gate bias would create a surface inversion condition (carriers at the surface change from electrons to holes) and positive gate bias would create a surface accumulation of electrons, with flat-band (uniform carrier concentration profile across diameter of the SiNW) and depletion conditions falling under more moderate gate bias conditions. For the simulation, a Schottky barrier height was also defined at the metal/semiconductor interface by the user. The goal of the simulations was to identify a method to extract this input or true Schottky barrier height from the non-ideal I-V data collected under
different gate bias conditions. For each I-V curve obtained for a given gate bias condition, the ideality factor and effective barrier height was extracted by fitting the data with the usual thermionic emission equation. By changing the gate bias, and running the device simulations again, a family of I-V curves could be obtained for a single nanowire diameter. It was found that if the ideality factor was plotted against the Schottky barrier height, a linear relationship between the two could be identified (Figure 4-3). By extrapolating this linear relationship to $n=1$, the input or true Schottky barrier height can be extracted. This methodology then provides a framework for extracting the true Schottky barrier height of axial contacts to SiNWs from non-ideal I-V data from a single device. The advantage of the ability to perform this analysis on a single device is that the Schottky barrier height may be studied as a function of nanowire size to determine any change in the Schottky barrier height with a reduction in nanowire diameter.

![Figure 4-3: Plot of ideality factor (n) versus effective Schottky barrier height showing linear relationship between the two for a wrap-around gate Schottky diode. Extrapolating the linear fit to n=1 gives the true input barrier height used in the Sentaurus device simulations. Plot modified from Sarpatwari et al.](image)

The following section describes the fabrication of the wrap-around gate Schottky diodes, followed by analysis of data collected from electrical measurements made on the samples. These
samples were used to test the validity of the simulations and the application of the linear $n-\varphi_B$ relation to data from real world nanowire devices.

Fabrication of Wrap-Around Gate Schottky Diodes

The fabrication of the wrap-around gate Schottky diodes begins with a 3” double side polished Si wafer. The wafer is sent to the Penn State Nanofabrication facility for coating with 100 nm of low-pressure chemical vapor deposition (LPCVD) SiNx. The deposition conditions for the LPCVD are a substrate temperature of 820°C, reactor pressure of 300 mTorr, and inlet gas flow rates of ammonia and dichlorosilane of 180 and 40 sccm, respectively. The purpose of the SiNx layer is to provide electrical isolation of the fabricated device on the top of the wafer from the underlying Si wafer. After the LPCVD SiNx deposition, a double layer photoresist stack is spun onto the wafer, similar to that described in Chapter 2 for the fabrication of the TEM workbench samples. The main difference here is that rather than S1805 as the top layer of photoresist, SPR3012 is used as the top layer of photoresist. To reiterate, the procedure for creating the double layer resist stack, LOR2A is first spun on at a speed of 4000 RPM for 45 sec and then cured on a hot plate at 180°C for 10 min. After the wafer is allowed to cool back to room temperature, SPR3012 photoresist is spun on at 4000 RPM for 45 sec and then soft-baked on a hot plate at 95°C for 60 sec. The purpose of using SPR3012 rather than S1805 is that the SPR3012 is photosensitive in the wavelength of UV radiation (i-line) used in the GCA 8000 stepper. Furthermore, the advantage of using the stepper over conventional contact lithography is that better resolution is achievable. The resolution of the GCA 8000 stepper is nominally 0.6 μm compared to 1 μm for conventional contact lithography. After the double layer resist stack has been spun onto the wafer, the first metallization layer is patterned. This first layer acts as sacrificial alignment electrodes to align the SiNWs to predetermined locations so that further
patterning may be done to create the gate, Schottky, and Ohmic contacts to the SiNW. A schematic of a single cell of this first layer is shown in Figure 4-4(a). A close up view of the individual alignment site is shown in Figure 4-4(b). The SiNW is nominally placed between the two finger electrodes. The full cell is patterned by the stepper 32 times on the wafer to use as much of the Si wafer area as possible. The specific exposure parameters for the stepper are an exposure of 0.9 s and focus value of -18, though these parameters may be subject to change with time. After exposure by the stepper, the photoresist is developed in CD-26 developer for 60 s. The wafer is then loaded into an e-beam evaporation system and pumped to a base pressure of 2x10^{-7} Torr. Once the base pressure has been reached, 80 nm of Ag is e-beam evaporated onto the substrate. The evaporation system is then vented and the wafer is removed and immediately transferred into a solution of Remover PG in order to dissolve away the remaining resist and metal in undesired areas, leaving behind only metal in the areas patterned specifically by the mask shown in Figure 4(a). The Remover PG solution is placed on a hotplate set to 80°C to accelerate dissolution of the photoresist.
Figure 4-4: (a) Overview of pattern used for alignment of SiNWs and (b) close-up image of an individual alignment site where single SiNW devices are to be fabricated after alignment. Note: The name of this mask is “WAGDIODE12”.

Once the Ag alignment electrodes have been patterned, a local Al back gate is patterned between alignment electrodes so when SiNWs are aligned they lie on top of the local Al back gate, and subsequent lithography steps may be used to pattern a local top gate to create a gate that completely surrounds the SiNW. Again, the same double layer resist stack described above is spun onto the wafer, and the second layer pattern (Figure 4-5) is exposed using the stepper and then developed. The strip shown in Figure 5 is aligned such that it is patterned directly between the two finger electrodes to which the SiNW is aligned, shown in Figure 4-4(b). For the local back gate, 60 nm of Al is e-beam evaporated and excess resist and metal are removed by liftoff.
After the Ag alignment electrodes and local Al back gate have been patterned, the SiNWs are aligned using the electrofluidic alignment process. The SiNWs used for alignment are grown by the vapor-liquid-solid method and doped with P. The SiNWs are grown to a total length of 16 μm with lightly and heavily doped segments. The lightly doped segments are grown first, and are grown to a length of 10 μm with a PH$_3$/SiH$_4$ ratio of 1x10$^{-4}$. The heavily doped segments are grown second and are grown to a length of 6 μm with a PH$_3$/SiH$_4$ ratio of 2x10$^{-3}$. The SiNWs were then soaked in Transene Au etchant to remove the Au catalyst particles on the tips of the SiNWs. Next, the SiNWs were oxidized in a furnace with O$_2$ and TCA flowing at a temperature of 900°C for 15 min. A TEM micrograph of a SiNW after oxidation is shown in Figure 4-6. The SiO$_2$ thickness surrounding the SiNW varies depending on the starting SiNW diameter, but averages 10 to 15 nm for these SiNWs which range in diameter from 50 to 100 nm before oxidation. After oxidation, the nanowires are sonicated into isopropanol to disperse the SiNWs for alignment. An AC signal with frequency of 100 kHz and amplitude of ±5 V is applied to the alignment electrodes. While applying the AC signal, 3–5 μL of isopropanol with SiNW solution is placed onto the alignment electrodes. Once the drop of solution has dried, a second
drop may be placed if necessary. The alignment cell should be checked in between each drop applied using an optical microscope to determine for the density of SiNWs in solution how many drops are necessary to nominally place single wires at the alignment sites; whereas, placing too much solution or even too dense of a solution may create alignment sites with more than one SiNW in the desired alignment location.

![TEM micrograph of a SiNW after oxidation at 900°C for 15 min with TCA flowing. The SiO$_2$ shell thickness is 14 nm.](image)

**Figure 4-6:** TEM micrograph of a SiNW after oxidation at 900°C for 15 min with TCA flowing. The SiO$_2$ shell thickness is 14 nm.

After alignment of SiNWs, the Ni Schottky contact is patterned on one side of the SiNW. A schematic of the Ni contact layer pattern is shown in Figure 4-7. Again, a double layer resist stack is spun onto the wafer, followed by exposure with the stepper and development in CD-26. However, in this case prior to loading the wafer into the evaporation chamber a solution of 15% 10:1 BOE and 85% deionized water is used to remove the SiO$_2$ layer surrounding the SiNW in the contact region such that when the Ni contact is deposited it will intimately contact the SiNW
instead of the surrounding SiO$_2$ layer. The wafer is submersed in the deionized water/BOE solution for 90 s to remove the SiO$_2$ layer, and then removed and rinsed with deionized water and blown dry with N$_2$. Immediately after this SiO$_2$ etch step, the wafer is loaded into the evaporation chamber and pumped down to prevent regrowth of SiO$_2$ as the sample is exposed to air. After the chamber is pumped down to a pressure of 2x10$^{-7}$ Torr, 80 nm of Ni is e-beam evaporated. The chamber is then vented and liftoff is performed using heated Remover PG.

Figure 4-7: Schematic of single alignment site after removal of Ag alignment pads and patterning of the Ni contact to the left of the local back gate. Note: The name of this mask is “WAGDIODE34”.

Next, a Ti/Al Ohmic contact is patterned to the opposite side of the SiNW that the Ni contact was just previously patterned. The device with the Ti/Al contact layer is shown schematically in Figure 4-8. The Ti/Al contact layer is patterned using the same double layer resist stack described above, followed by exposure with the stepper and development in CD-26. The same deionized water/BOE solution described above is used to remove the intentional SiO$_2$ layer in the Ti/Al contact area, and is again performed for 90 s. The sample is then transferred to the e-beam evaporation system, which is pumped down to a pressure of 2x10$^{-7}$ Torr. A film of 50 nm of Ti, followed by 50 nm of Al is deposited to form the Ohmic contact to the SiNWs. Excess metal and photoresist is then removed in heated Remover PG.
Figure 4-8: Schematic of individual alignment site after patterning of Ohmic Ti/Al contact. The Ti/Al contact pad is on the right side of the device. Note: The name of this mask is “WAGDIODE34”.

Lastly, the Al top gate is patterned such that it is directly on top of the local back gate patterned in the second lithography step. A schematic of device with this additional layer is shown in Figure 4-9. A double layer resist stack is again used, followed by exposure using the stepper and lastly development in CD-26. After exposure and development, the wafer is loaded into the e-beam evaporation system, and 100 nm of Al is deposited. Liftoff is then performed to remove excess photoresist and Al, leaving the completely patterned wrap-around gate Schottky diodes. In order to form the axial silicide contact a final annealing step is performed using an RTA furnace. The RTA furnace is purged with UHP Ar prior to annealing. The complete wafer is annealed at 550°C for 3 min to form a nickel silicide segment that will intrude underneath the gate electrode, leaving the SiO₂ shell such that the nickel silicide/SiNW interface is surrounded symmetrically by the SiO₂ shell as well as the Al top gate to electrostatically modify the metal/semiconductor interface.
**Figure 4-9:** Schematic overview of individual alignment site after final patterning of local Al top gate. This overview is the device pattern in final form with the Ni contact on the right side (green), Ti/Al contact on the right (blue), and Al wrap around gate in the center (yellow). Note: The name of this mask is “WAGDIODES”.

**Analysis of I-V Data from Wrap-Around Gate Schottky Diodes**

Electrical measurements were made on samples before annealing to form the axial silicide contact as well as after annealing. The system used to perform the electrical measurements was a Cascade probe station equipped with an Agilent 4156B Precision Semiconductor Analyzer. The probe station was purged with N₂ prior to making measurements and all measurements were made at room temperature. The purpose of making measurements before annealing was to determine which devices had SiNWs aligned properly. For a given device, one can tell from optical microscopy if a SiNW spans the three contacts; however, given the asymmetry of the Schottky diode and the variation in doping of the wires, we needed to determine if the lightly doped segment of the SiNW is contacting the Ni contact pad and heavily doped segment contacting the Ti/Al contact pad or vice versa. For this analysis, bias was applied to the Ni contact pad, while the Ti/Al contact pad was held at ground. For this case, the Schottky diode should be forward biased for positive voltages and reverse biased for negative voltages; i.e.,
we should see current flow when applying positive bias and rectification under negative bias to
the Ni contact pad.

After annealing, electrical measurements were again performed on devices in which
current was able to flow through the device and the SiNW was determined to be aligned properly.
Figure 4-10 shows representative I-V curves from a device before and after annealing. After
annealing we observe a large increase in the overall current flowing through the device. This is
likely because we have now incorporated a metallic segment into the nanowire, and reduced the
overall length of the semiconducting SiNW in the device. Effectively, this reduces the series
resistance of the device and allows larger currents to flow.

![I-V curves](image)

**Figure 4-10:** I-V curves obtained from wrap-around Schottky diode (a) before annealing to form
axial θ-Ni$_2$Si segment and (b) after annealing to form θ-Ni$_2$Si segment, both with no applied gate
bias. The overall device current is increased after introduction of the low resistance silicide
segment.

In order to apply the linear n-φ$_B$ relationship found in the Sentaurus device simulations by
Sarpatwari *et al.*, I-V curves under different gate bias conditions were collected. Representative I-V curves for different gate bias conditions are shown in Figure 4-11. A trend
that is immediately identified with gate bias is that for negative gate biases we are able to shut off
the device and greatly limit current flow through the device, with the exception of leakage current
that may flow from the gate contact through the SiO$_2$ dielectric layer surrounding the SiNW. When negative gate bias is applied, surface depletion occurs and the resistivity of the SiNW segment increases causing less current to flow then when no bias is applied to the gate electrode. Additionally, because of the depleted surface, at the Ni silicide/SiNW interface, the depletion width near the surface is wider compared to the depletion width with no bias applied to the gate. The increase in the series resistance of the device, as well as increase in depletion width near the surface where depletion occurs, are responsible for the loss in current as negative gate bias is applied compared to the condition where no bias is applied to the gate electrode.

**Figure 4-11:** Forward bias I-V curves for wrap-around gate Schottky diodes for several different gate bias conditions. Under negative gate bias the device current is effectively shut off, while for increasingly positive gate bias more and more current is allowed to flow.

In the I-V curves collected under positive gate bias conditions, an increase in current is observed for increasingly positive gate biases. For increasingly more positive gate bias, the overall current through the device increases when the Schottky diode is forward biased. This
trend is to be expected, because the SiNWs are doped n-type. The reasoning for the increase in current is that as positive gate bias is applied, a surface accumulation layer forms near the surface of the SiNW. The local increase in carrier concentration in the near surface region of the SiNW creates a pathway with a lower resistivity compared to the resistivity of the SiNW with no gate bias applied. This effectively reduces the series resistance of the SiNW and causes an increase in the current flowing through the device. The second reason for the increase in current is again due to the near surface accumulation layer of electrons that forms due to the positive gate bias applied. At the metal/semiconductor interface in the same near-surface region, because of the local increase in electron concentration, the Schottky barrier depletion width is preferentially thinned in the near-surface region of the metal/semiconductor interface. Thinning of the Schottky barrier creates a situation where the tunneling current through the Schottky barrier is increased, causing an increase in current flow through the Schottky diode under forward bias. For increasingly positive gate bias conditions, these effects become more pronounced.

In order to confirm the majority of current flowing through the device was actually current flowing from the Ni contact through the Schottky barrier, into the SiNW, and then into the Ohmic Ti/Al contact, a test for leakage through the gate dielectric was performed. The gate leakage test was done by biasing the Ni contact at -0.1 V, and the current travelling from the Ni contact to the Al gate contact was measured while sweeping the gate bias from -1 V to +1 V. A plot of the leakage current is shown in Figure 4-12. At +1 V the gate leakage current is approximately 10 pA. Comparatively, at +1 V of gate bias the total current flowing through the device is more than 10 nA, more than 1000 times greater than the leakage current. From these data we can confidently say that most of the measured current is flowing through the $\theta$-Ni$_2$Si/n-SiNW Schottky diode, as opposed to an alternate conduction path such as through the gate dielectric, into the gate metal, and then back through the dielectric into the SiNW.
Figure 4-12: Leakage current from Al wrap around gate while Ni contact is biased at -0.1 V and the Ti/Al contact is grounded. The leakage current is several orders of magnitude lower than the current observed flowing from the Ni contact to the Ti/Al contact indicating that the leakage current does not significantly contribute to the current measured in the wrap-around gate Schottky diode. The gate voltage is swept from -1 V to +1 V and then back from +1 V to -1 V.

From each of the I-V curves obtained under forward bias conditions, the ideality factor and effective Schottky barrier height can be extracted by fitting the I-V data with the thermionic emission equation. Figure 4-13 shows an n–\(\varphi_{\text{Beff}}\) plot with data extracted from the same device for which I-V data is shown in Figure 11. It is clear that the relationship between n and \(\varphi_{\text{Beff}}\) is linear, with lower values of \(\varphi_{\text{Beff}}\) for larger values of n, and vice versa. By linearly fitting the data and extrapolating to an ideality factor of 1, a Schottky barrier height of 0.57 eV is obtained.

From TEM analysis of the Ni silicide formation performed in Chapter 3, we have identified the Ni silicide phase formed in [112] growth direction SiNWs as \(\theta\)-Ni\(_2\)Si. Unfortunately, this particular phase is a high-temperature phase not commonly observed in thin-film reactions, so to the best of the author’s knowledge, no data exist on the value of the Schottky barrier height in
contacts to Si to make a comparison. However, there are several reports in the literature on the Schottky barrier height of the more common low temperature $\delta$-Ni$_2$Si phase. The Schottky barrier height of $\delta$-Ni$_2$Si to n-type Si is in the range of 0.62 to 0.75 eV$^{114,115}$. The Schottky barrier height we obtained is slightly lower than these values; however, it may be expected that that barrier height will differ since the Ni silicide crystal structure differs from that of the orthorhombic structured $\delta$-Ni$_2$Si. Furthermore, we observe an epitaxial interface between the $\theta$-Ni$_2$Si and the SiNW. In epitaxial contacts between NiSi$_2$ and Si, the Schottky barrier height can vary depending on the epitaxial relationship between the NiSi$_2$ and the Si as well as the orientation of the Si wafer$^{116,117}$. All of these reasons suggest that it would not necessarily be expected that the Schottky barrier height of $\theta$-Ni$_2$Si to n-type SiNWs would be the same as $\delta$-Ni$_2$Si contacts to planar n-type Si wafers.

![Figure 4-13](image.png)

**Figure 4-13:** Plot of ideality factor versus effective Schottky barrier height for a wrap-around gate Schottky diode. The relationship is linear and by imposing the method described by Sarpatwari et al. a Schottky barrier height of 0.57 eV is found by extrapolating the linear fit to $n=1$. 
Using the method described above, Schottky barrier heights were extracted for 8 different devices with SiNW diameters ranging from 60 to 120 nm. There is some slight scatter in the data with extracted Schottky barrier heights ranging from 0.54 to 0.58 eV; however, no trend with SiNW diameter is evident. This is not quite surprising, though, since any quantum mechanical size effects that have been predicted to affect the Schottky barrier height have been predicted to only occur in contacts to SiNWs with diameters less than 10 nm\textsuperscript{118,119}. The remainder of this chapter will focus on challenges associated with integration of small-diameter SiNWs into the wrap-around gate Schottky diode process.

**Fabrication of Small Diameter SiNW Wrap-Around Gate Schottky Diodes**

In order to further study the effect of SiNW size on the Schottky barrier height, SiNWs with smaller diameters were synthesized by Sharis Minassian in Dr. Joan Redwing’s group. The growth of these small diameter SiNWs is similar to that described above; however, instead of using a thin Au film that results in random SiNW diameters, Au nanoparticles with a well defined size are used. For this specific study, Au nanoparticles with starting diameters of 20 nm were utilized. Diameters of 20 nm were chosen because although the as-grown SiNW will have a diameter of 20 nm, after oxidation to form a 10–15 nm thick dielectric shell, a much smaller diameter core will result. The following equation can be used to predict the final core SiNW diameter after oxidation if the desired oxide thickness and starting SiNW diameter are known\textsuperscript{120};

\[
a_0^2 = \frac{b^2}{2.25} + \frac{1.25}{2.25} a^2,
\]

where \(a_0\) is the starting radius of the SiNW, \(a\) is the Si core radius after oxidation, and \(b\) is the total radius after oxidation. For example, for a starting 20 nm diameter SiNW, after oxidizing to form a 9 nm thick shell, a 10 nm diameter Si core remains. SiNWs were oxidized in a furnace with O\textsubscript{2} and TCA flowing at 900°C for 12 min. A TEM micrograph of a SiNW after
oxidation is shown in Figure 4-14. The core SiNW diameter is 13 nm with an 8 nm thick SiO$_2$ shell surrounding the SiNW.

![Figure 4-14: TEM micrograph of a 20 nm SiNW after oxidation at 900°C for 12 min. The remaining Si core is 13 nm with an 8 nm thick SiO$_2$ shell surrounding the SiNW.](image)

During typical NW device fabrication, these SiNWs would be incorporated into device structures using the same processing steps described at the beginning of this Chapter. However, in this case it was found that the electrofluidic alignment step commonly used to place the SiNWs at predetermined locations for patterning devices was largely ineffective for the oxidized small diameter SiNWs implemented here. Motayed et al.\textsuperscript{121} calculated effective dielectrophoretic forces on GaN nanowires as a function of NW diameter and showed that the force on the GaN nanowire can drop by an order of magnitude with a change of diameter from 100 to 50 nm. Using even smaller diameter SiNWs in this study, it is expected the dielectrophoretic force on the
SiNW may be even smaller compared to the SiNWs with diameters ranging from 60 to 100 nm, leading to the lack of attraction to the alignment electrodes. Furthermore, with the oxide shell surrounding the SiNW, there is only a small (10 nm or less) conducting core of Si, which may also reduce the attractive dielectrophoretic force to the alignment electrodes.

Due to the inability to use dielectrophoretic alignment to align the SiNWs, an alternative approach for fabricating devices with small diameter oxidized SiNWs was developed. For this process, a Si wafer with 100 nm of LPCVD SiNx is loaded into an e-beam evaporation system and 60 nm of Al is deposited on one side. Small diameter oxidized SiNWs are then randomly dispersed on top of the Al layer. The same double layer resist stack described previously (LOR2A/SPR3012) was spun onto the wafer. Using the Heidelberg DWL66 laser writer at the Penn State Nanofabrication facility, sites with SiNWs were identified by the optical microscope on this system. Once a site with a SiNW was identified, the first layer was patterned. This first layer is shown schematically in Figure 4-15 and is used to pattern the local Al back gate underneath the SiNW. The 2 mm write head was used on the laser writer with a dgr setting of 1.161 and a 10% filter to reduce the intensity of the incident laser beam to 10% of the initial laser intensity. The advantage of using the laser writer here instead of conventional contact lithography is that a predefined pattern on a mask does not need to be used. Rather, the laser beam is rastered over the substrate and the shutter is opened and closed to expose specific regions to the laser beam radiation determined by a premade user file. For each exposure site, the exact coordinates were collected so that additional layers can be patterned. By knowing the coordinates of each alignment site from the center of the wafer, the wafer can be shifted to the exact position of each identified SiNW site to pattern the Ni Schottky contact, Ti/Al Ohmic contact, and Al top gate layer.
Figure 4-15: Schematic diagram of pattern used in the direct laser write process for fabricating small diameter Schottky diodes. After patterning the exposed Al, regions are etched leaving the SiNW on top of a local Al back gate to be further processed to pattern the Ni Schottky contact, Ti/Al Ohmic contact, and Al local top gate.

After exposure of the first layer by the laser writer, the wafer is developed in the commercially available CD-26 developer. The wafer was intentionally over developed in this case to etch through the Al in the exposed regions. The CD-26 developer is known to slowly etch Al, and this was used to our advantage for this specific processing step to locally remove Al, leaving only the Al strip and cross-pattern shown in Figure 4-15. The remaining photoresist was then removed using Remover PG. The Ni contact was then patterned in a similar fashion described above. A double layer resist stack was spun onto the wafer, and the Ni contact region was patterned by the laser writer. Before Ni deposition, the same oxide etch removal step described for the larger diameter SiNW devices was performed to make intimate contact between the Ni contact pad and the SiNW. Similarly, the Ti/Al contact was patterned in the same way except to contact the other side of the SiNW, and then lastly the Al top gate was patterned similarly with the exception that no oxide etch was performed to leave the SiO$_2$ to function as a
gate dielectric. An SEM image of the final patterned device is shown in Figure 4-16. To form the $\theta$-Ni$_2$Si Schottky contact, the wafer was annealed at 550°C for 3 min.

![SEM image](image)

**Figure 4-16:** SEM image of a small diameter SiNW wrap-around gate Schottky diode. The SiNW is approximately in the center and is the line laterally spanning all three electrodes.

**Electrical Measurements on Small-Diameter Schottky Diodes**

Measurements similar to those described for the larger diameter SiNWs were first performed to test which SiNWs were aligned properly such that the $\theta$-Ni$_2$Si segment was contacting the lightly doped segment of the SiNW and the Ti/Al contact was contacting the heavily doped end of the SiNW. Standard two-point measurements on the devices show diode-like behavior. Figure 4-17 shows an I-V curve from one of the small-diameter Schottky diode devices. If we further investigate this device and check the current flow from the Ni contact to the gate, as well as the Ti/Al contact to the gate, we find that current flow through the device is
unlikely confined to the nanowire. Figure 4-18 displays I-V curves measured of current flowing from the Ni contact to the gate and the current flowing from the Ti/Al contact to the gate for the same device with I-V data shown in Figure 4-17. It is apparent from this test that the leakage current to the gate is on the order of the current measured for the 2 point measurement from the Ni contact to the Ti/Al contact. This leakage path through the oxide creates a situation in which the current flowing through the device is not limited by the 0-Ni₂Si/n-SiNW Schottky barrier, and the Schottky barrier height cannot be extracted from the I-V data.

**Figure 4-17:** I-V data collected from a small diameter SiNW wrap-around gate Schottky diode biasing the Ni contact and grounding the Ti/Al contact with no applied gate bias. The device shows some asymmetry in the forward and reverse bias portions of the curve, as expected for a Schottky diode.
Figure 4-18: Leakage current measured from the (red circles) Al gate to the Ti/Al contact and from the (black squares) Al gate to Ni contact. For the small diameter SiNWs, the leakage current is a significant portion, if not all of the current, observed in the current measured from the Ni contact to the Ti/Al contact shown in Figure 17. The voltage applied and shown on the x-axis of the plot is applied to the Al gate while the Ti/Al or Ni contact is grounded.

One issue that may be problematic in these devices is the nature of the SiO$_2$ layer grown on the surface of the SiNW. In the case of the larger diameter wires, leakage currents of about 10 pA were observed and typically the current from the Schottky contact to Ohmic contact was approximately 1 μA. In these small-diameter SiNW devices, total currents from the Schottky contact to Ohmic contact of less than 20 pA are observed. In this case, the leakage current from the gate is significant, and in most cases is likely the primary source of conduction between from the Ni electrode to the Ti/Al electrode. The remainder of this chapter focuses on investigating whether the SiO$_2$ dielectric shell is damaged during device processing.
Failure Analysis of Small-Diameter Schottky Diodes

In order to investigate the status of the SiO$_2$ shell after device processing, a focused ion beam (FIB) was used to cut a cross-section of the device to directly image the SiO$_2$ layer in the TEM and determine the status of the SiO$_2$ layer underneath the gate. The FIB was used to cut a lateral cross-section such that the entire length along the SiNW underneath the Al gate could be imaged to determine where damage may have occurred during device processing. Figure 4-19 shows schematically where and how the FIB cross-section is cut from the device. Initial thinning was performed at Penn State using the FEI Quanta 3D system to thin the sample to electron transparency. TEM images of the cross-section are shown in Figure 4-20. It is clear from these images that the sample has not yet been thinned from both sides completely so that only a slice of the SiNW underneath the gate is obtained. Al grains in front and/or in back of the SiNW from the Al gate interfere with imaging the entire nanowire. In the section where the SiNW can be seen, it is evident that the SiO$_2$ shell is still intact; however, further thinning of the sample is needed to remove excess Al to better view the complete Si/SiO$_2$ interface underneath the gate. The SEM column in the FEI Quanta 3D system does not have the resolution necessary to view the Al gate region in detail to determine when the sample has been thinned and the surface of the SiNW is exposed, and for this reason the sample was not able to be completely thinned removing all of the excess Al surrounding the SiNW.
Figure 4-19: Schematic diagram of the FIB sample used to determine if the gate dielectric is damaged during device processing. To the left is shown the longitudinal cross-section to be cut (top view), and to the right is the desired cross-section to be obtained and analyzed. The lines with arrows on the left figure indicate where lines are cut with the FIB, and then further thinned in the direction of the arrows in order to thin the sample to electron transparency.

From the bright-field TEM image in Figure 4-20(a) the Al gate stack region is observable; however, it is difficult to distinguish the different Al, SiO₂, and Si layers that should be present. By inserting an objective aperture into the back focal plane of the objective lens, the (111) Si diffraction spot can be selected to image with. In this dark-field mode, contrast is generated only by regions in the image that generate diffracted beams to the selected scattering angles by the objective aperture. In Figure 4-20(b) the bright layer in the image is certainly the SiNW; however, it does not appear to extend completely underneath the Al gate. This is suspected to be caused by interference in imaging caused by excess Al present in front and/or behind the SiNW, because the sample has not been completely thinned to the SiNW region by the FIB.
Figure 4-20: (a) Bright-field TEM micrograph of the Al gate region of the device. It is difficult to determine where the SiNW lies from the bright-field image; however, in the dark field image using the (111) Si diffracted beam the location of the SiNW underneath the Al gate is apparent. (c) A dark-field STEM image shows in the region of the SiNW that is observable that the SiO$_2$ shell is still intact on top of the SiNW.

Furthermore, from the DF-STEM image a thin amorphous layer is identified between the Si and Al wrap around gate. This layer is presumably the SiO$_2$ dielectric that surrounds the SiNW. As observed by TEM prior to integration into the Schottky diodes, the SiNWs after oxidation have an 8–10 nm thick SiO$_2$ shell surrounding them; however, from the DF-STEM image the measured oxide thickness surrounding the SiNW is 5–6 nm.

The gate of the Schottky diode device consists of Al surrounding an oxidized SiNW. During annealing to form the axial silicide the Al film may reduce the SiO$_2$ into AlO$_x$. The reduction of SiO$_2$ by Al has been reported in metal-oxide-semiconductor structures in the past. Activation energies for this process have been found to be between 1.4 and 3 eV in the temperature range of 350–670°C. Note, the lower activation energies observed are observed in cases where the oxide layer being observed for breakdown is only 1–2 nm. In situations more similar to the thicker oxides we have integrated into our devices, approximately 10 nm and larger, the activation energies are between 2 and 3 eV. Comparing these values to the
activation energy of 1.4 eV/atom found for the formation of an axial $\theta$-Ni$_2$Si segment in SiNWs with [112] growth directions the competing processes are problematic. In forming the axial silicide segment, the dielectric quality of the thermally grown SiO$_2$ shell is degraded by being annealed in contact with the Al wrap-around gate. For the small-diameter SiNWs, because the drive current through the device is lower than that for larger diameter devices, the leakage current through the gate significantly affects the measurement of current through the Schottky diode for devices in which small diameter SiNWs are integrated into the wrap-around gate Schottky diodes.

Because the activation energy for dielectric breakdown of SiO$_2$ has been reported in some cases to be between 2–3 eV, lower temperature anneals were also performed to form the axial $\theta$-Ni$_2$Si segment. By annealing at lower temperatures for longer times, it was expected that if the activation energy for SiO$_2$ degradation is larger than that for $\theta$-Ni$_2$Si formation (1.4 eV/atom), then the SiO$_2$ degradation will be relatively less complete at lower temperatures. In order to form a segment 1.5 μm in length, an annealing condition of 450°C for 12 min was chosen, based on the kinetic study in which it was found that this annealing condition would result in formation of a $\theta$-Ni$_2$Si segment 1.5 μm in length. A second annealing condition of 375°C for 3 h was chosen based on the equation;

$$t_2 = \frac{t_1 e^{E_A/kT_1}}{e^{E_A/kT_2}},$$

where $t_2$ is the desired annealing time at temperature $T_2$ to form a silicide of length $L$, $t_1$ is a known annealing time to form a silicide of length $L$ at a temperature of $T_1$, $E_A$ is the activation energy, and $k$ is Boltzmann’s constant. However, even under these annealing conditions, fabricated devices were found to have similar transport characteristics as the small diameter devices described previously. Namely, the current from the Schottky to Ohmic contact was only slightly larger than the current observed from the gate to the Schottky contact or to the Ohmic contact. This suggests that the leakage current through the gate dominates the transport
characteristics of the device, making it impossible to extract useful information about the Schottky barrier height of the Schottky contact in these small diameter Schottky diodes. The primary reason for this problem may be the reduction of the insulating SiO$_2$ shell by Al.

Conclusions

The application of simulations performed by Sarpatwari et al.\textsuperscript{106} on using the linear $n$-$\varphi_B$ relationship to identify the true Schottky barrier height of axial metal/semiconductor nanowire contacts was demonstrated for $\theta$-Ni$_2$Si contacts to n-SiNWs. A Schottky barrier height of 0.57 eV was found, with no diameter dependence for SiNWs with diameters ranging from 60–100 nm. A new fabrication procedure for laser writing contacts and gate electrodes was also described for the implementation of small diameter (20 nm or less) SiNWs into the wrap-around gate Schottky diodes. However, most likely due to two competing thermally activated processes, namely formation of the axial Ni silicide contact and reduction of the SiO$_2$ by Al, no useful electrical data were extracted from these devices to analyze the Schottky barrier height of contacts to small diameter SiNWs.

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Chapter 5
Ni Germanide Formation in Contacts to Germanium Nanowires

Introduction – GeNWs and Ni Germanide Contacts

The following chapter will focus on the solid state reaction between Ni contact pads and germanium nanowires (GeNWs) in a series of experiments similar to those performed in Chapter 3, with the exception that GeNWs are used to replace the SiNWs. GeNWs, like their SiNW counterparts, have attracted considerable interest for applications such as field-effect transistors and chemical and biological sensors. GeNWs in particular are interesting because of the higher carrier mobilities of Ge compared to Si. Furthermore, Ge has a larger exciton Bohr radius than Si, making quantum confinement effects more readily observable in larger-diameter GeNWs.

For Ge-based electronics, it is reasonable to expect that a process analogous to the Ni-salicide process for germanide formation would be useful for contacts to Ge-based devices. Due to the relative immaturity of Ge-based technology, considerably less work has been completed to understand the phase formation sequence and thermal stability of phases in the Ni-Ge system compared to those in the Ni-Si system. For the reaction of Ni thin films on Ge wafers, the observed phase formation sequence begins with the formation of a Ni-rich germanide (orthorhombic Ni$_2$Ge, hexagonal Ni$_2$Ge, monoclinic Ni$_5$Ge$_3$ or hexagonal Ni$_3$Ge$_2$). All of these phases have been found to form under similar annealing conditions; typically the first Ni germanide phase begins forming at temperatures of about 250—300°C. The first Ni germanide phase to form, regardless of stoichiometry, then continues to react with the underlying Ge wafer to form a more Ge rich Ni germanide layer. Next, NiGe forms and remains thermally stable up to temperatures in excess of 500°C, when agglomeration of the film begins. Again, regardless of
the composition of the first Ni germanide phase to form, NiGe is always the second phase to form. The Ni-rich germanides are not reported to form with an epitaxial relation to the Ge substrate, but NiGe has been reported to form epitaxially\textsuperscript{138}. This contrasts with the situation described in Chapter 3 for the Ni-Si system where epitaxial relations between growing Ni silicides and the underlying Si wafer have been observed for a number of silicide phases including \(0\)-Ni\(_2\)Si, NiSi, and NiSi\(_2\). For comparison, the Ni-Si and Ni-Ge phase diagrams are shown in Figure 5-1.

**Figure 5-1:** (a) Ni-Ge phase diagram compared to (b) Ni-Si phase diagram from ASM Handbook\textsuperscript{139}.
Another difference that has been observed between Ni-Si and Ni-Ge thin film reactions is that for Ni-Si reactions a sequential phase formation is typically observed; whereas, for the Ni-Ge thin film reactions a simultaneous phase formation has been reported\textsuperscript{140}. In this case, Ni\textsubscript{5}Ge\textsubscript{3} and NiGe were found to form simultaneously as a Ni thin film was annealed on a Ge wafer. The justification for the simultaneous phase formation in the case of the Ni germanides is that the critical thickness of Ni\textsubscript{5}Ge\textsubscript{3} before simultaneous growth occurs is only approximately 20 nm. Comparatively, for simultaneous growth of Ni silicides the critical thickness of Ni\textsubscript{2}Si is approximately 200 nm, which is typically never observed because thin film reactions are typically studied with Ni films 100 nm or less in thickness. It is unknown what effect this difference may or may not have in the nanowire reactions because of the stark differences already observed in SiNW reactions compared to previously studied thin-film reactions described in Chapter 3.

**GeNW Growth and Characterization**

In this study, GeNWs were grown by the vapor-liquid-solid method from 3 nm thick Au films on oxidized Si wafers by Sharis Minassian in Dr. Joan Redwing’s laboratory. GeH\textsubscript{4} was used as the precursor gas for the GeNW growth. The growth temperature was 300°C, the reactor pressure was 50 Torr, and the growth time was 80 min. GeNWs were then sonicated from the growth substrate into isopropanol, and electron-transparent contacts were fabricated by a method described in detail in Chapter 2. In the present work, a deionized water soak for 90 s was used to remove the native oxide on the GeNWs prior to e-beam evaporation of 80 nm thick Ni contacts, which differs from the use of buffered hydrofluoric acid to remove the native oxide on SiNWs. Samples were then annealed \textit{ex-situ} in a rapid annealing furnace (AG Associated Heat Pulse 610) in ultrahigh purity Ar at temperatures of 300, 350, 400, 450, 500 and 600°C for 2 min each.
Transmission electron microscopy (TEM) was performed using a JEOL EM-2010F field-emission TEM with a Gatan double-tilt holder.

GeNWs were first sonicated into isopropanol and dispersed onto lacey C coated Cu grids and loaded into the TEM to determine the crystallinity and growth directions of the GeNWs. All GeNWs were found to be single crystalline with diameters ranging from 30 to 100 nm and an average of 55 nm. A distribution of growth directions was found to exist. Out of 14 GeNWs analyzed for growth directions, 8 were found with [110] growth direction, 2 with [111] growth direction, and 4 with [112] growth directions. A distribution of growth directions is to be expected because the GeNWs were grown from oxidized Si wafers. The SiO$_2$ layer on the surface is amorphous and there is no reason for epitaxy to occur like is observed for [111] growth direction SiNWs grown from [111] Si wafers. Additionally, the distribution in growth directions allows for us to study any effects of the nanowire growth direction on Ni germanide reaction products.

**Results of Ni Contact Pads Annealed on GeNWs**

Axial nickel germanide segments begin to form after 2 min at 300°C, as shown in Figure 5-2(a). The average length of the nickel germanide segment after 2 min at 300°C is 20 nm. After annealing at 350°C for 2 min, the nickel germanide segment is observed to increase in length to 230 nm on average (Figure 5-2(b)). The axial nickel germanide segment is polycrystalline with grain boundaries that extend across the entire cross-section of the NW. Selected area electron diffraction (SAED) patterns (Figure 5-3) taken from individual grains of nickel germanide were matched to the Ni$_2$In prototype structure with the space group P6$_3$/mmc$^{141}$. We measured lattice parameters of $a=3.95\text{Å}$ and $c=5.18\text{Å}$, which is in relatively good agreement with values determined by x-ray diffraction ($a=3.947 \text{ Å}$ and $c=5.037 \text{ Å}$) for different phases of nickel.
germanide in the Ni<sub>2</sub>In prototype structure. Interestingly, we find that nickel germanide grains are misaligned from each other by only 2-3°. The low angle of the grain boundaries, suggestive of low-energy interfaces, may explain why different grains are able to form during the growth of the nickel germanide segment. Furthermore, we find that the growth direction of the GeNW does not affect the phase formation. For [111], [112], and [110] growth direction GeNWs the same nickel germanide phase is observed, unlike the SiNW growth direction dependence of solid-state reactions between Ni and SiNWs studied in Chapter 3. Interestingly, the Ni<sub>2</sub>In structure observed here is the same as the structure observed for the θ-Ni<sub>2</sub>Si phase found when annealing Ni contact pads on [112] growth direction SiNWs; however in the Ni-Si system there is no discrepancy over compounds with differing stoichiometries but the same crystal structure.

![Figure 5-2](image-url)  
**Figure 5-2:** (a) TEM micrograph of Ni contact on GeNW annealed at 300°C for 2 min showing the initial formation of an axial Ni germanide compound. (b) Sample annealed at 350°C for 2 min showing increase in length of Ni germanide segment with multiple grains.
The match of the SAED patterns from the TEM to the prototype structure Ni$_2$In suggests that the stoichiometry of the nickel germanide phase is Ni$_2$Ge; however, there are a number of different phases reported with very similar crystal structures, including Ni$_5$Ge, Ni$_5$Ge$_3$, Ni$_{19}$Ge$_{12}$, Ni$_{17}$Ge$_{12}$ and Ni$_3$Ge$_2$. The Ni$_2$In structure is similar to the NiAs prototype structure with the exception that there is an additional Ni sublattice present in the Ni$_2$In structure compared to the NiAs structure. Figure 5-4 illustrates the NiAs and Ni$_2$In prototype structures with the different Ni sublattices shown in different colors to differentiate between the two. The difference between the Ni$_x$Ge stoichiometries listed above is due to vacancies on one of the Ni sublattices, causing deviation from the ideal Ni:(Ge or In) stoichiometry of 2:1. According to Ellner et al., vacancies on one of the Ni sublattices result in different stoichiometries in the B8 phase region of the Ni-Ge system. Work performed by Larsson and Withers using electron diffraction suggested that these vacancies may be ordered in many of the phases, giving rise to the different stoichiometries of the related nickel germanides; however, we have not been able to identify any
ordering, as might be revealed by electron diffraction spots in addition to those expected from the Ni$_2$In prototype structure. We do not rule out the possibility that vacancies are present; however, based on the work of Larsson and Withers, the phase that seems most consistent with diffraction data obtained herein is Ni$_3$Ge$_2$, because of the lack of vacancy ordering observed in this structure. Larsson and Withers reported that this phase was the only one within the B8 region of the Ni-Ge phase diagram to display no additional ordering or superstructure.

![Ni$_2$In prototype structure and NiAs prototype structure](image)

**Figure 5-4:** (a) Illustration of the Ni$_2$In prototype structure and (b) NiAs prototype structure. The two different Ni sublattices are shown in different colors (purple and red) to easily distinguish the differences between the two structures.

Annealing the Ni/GeNW samples at 400°C for 2 min further increases the length of the nickel germanide segment to 660 nm on average. The nickel germanide segment is again found to be polycrystalline, and SAED patterns from each of the grains are matched to the prototype Ni$_2$In structure. Annealing of the samples at temperatures in excess of 450°C results in fracture in the nickel germanide segment near the nickel germanide/GeNW interface, as shown in Figure 5-5(a). A high magnification view of the break formed in the nickel germanide segment is shown in Figure 5-5(b). Annealing samples at 500 or 600°C for 2 min also results in a break near the
nickel germanide/GeNW interface, and the nickel germanide segments are similar in length to those observed after annealing at 450°C for 2 min. Therefore, regardless of whether samples are annealed at 450, 500 or 600°C for 2 min, the break forms shortly after the axial nickel germanide segment is formed. The Ni supply is then cut off, resulting in similar nickel germanide segment lengths for all three annealing temperatures.

Figure 5-5: (a) TEM micrograph of Ni contact pad on GeNW annealed at 450°C for 2 min resulting in a break in the Ni germanide segment. In (b) a higher magnification image of the break in the Ni germanide segment is shown. Annealing under these particular conditions would be problematic for creating axial Ni germanide segments in high performance GeNW devices.

There are a number of possible explanations for why the nickel germanide nanowire segments break after annealing at or above 450°C, some more plausible than others. One explanation involves unequal fluxes of Ni and Ge. To date, only one study by Marshall et al.\textsuperscript{144} has been performed to identify the diffusing species in the formation of Ni germanides, specifically finding that Ni is the dominant diffusing species in the formation of Ni\textsubscript{3}Ge. For the particular Ni germanide formed here, Ni\textsubscript{3}Ge\textsubscript{2}, the dominant diffusing species is not known. Perhaps Ge becomes the dominant diffusing species in Ni\textsubscript{3}Ge\textsubscript{2} at or above 450 °C, eventually leading to the formation of a void in the growing Ni germanide segment near the Ge NW.
However, the break is always about 50 nm away from the Ge NW rather than right at the germanide/Ge NW interface, which leads to some doubt about this explanation. A less likely explanation is that the germanides segment begins to agglomerate, akin to the agglomeration of NiGe thin films on Ge wafers at temperatures as low as 500°C or the Rayleigh instability observed in other nanowires. However, the germanides nanowire segment in our study does not break into beads anywhere else along its length, making this explanation less likely. Another possible explanation involves stress in the nanowire created by the thermal expansion mismatch between the nickel germanide segment and the GeNW. During rapid heating and cooling cycles in the RTA, perhaps a crack initially forms in the nanowire to relieve stress. It is also conceivable that more than one of these factors is at play.

The break in the wires at annealing temperatures of 450°C and higher does not eliminate the possibility of forming longer nickel germanide segments. In order to form longer nickel germanide segments without breaking the NWs, lower annealing temperatures may be used for longer times. For example, annealing at 400°C for 5 min results in forming nickel germanide segments with average lengths of 1.5 μm. Under these annealing conditions, axial nickel germanide contacts can be incorporated into structures such as those described by Sarpatwari et al. in order to study the Schottky barrier height of axial contacts to semiconductor NWs or to reduce the access resistance of GeNW transistors.

**Conclusions**

In summary, we have found that Ni contact pads react with GeNWs to form axial nickel germanide segments after annealing at 350°C for 2 min. Fracture in the nickel germanide segment occurs near the nickel germanide/GeNW interface for annealing temperatures of 450°C or higher, but long segments may be grown if the annealing temperature is limited to 400 °C and
longer annealing times are used. The ability to grow long nickel germanide segments microns in length will be useful for incorporation of nickel germanide contacts into GeNW field effect transistors and other nanoelectronic devices.

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Chapter 6

Conclusions and Future Work

Conclusions

We have found that as a basic criteria for forming axial metal silicide contacts to SiNWs from metal contact pads, the metal should be the dominant diffusing species (DDS) in the solid state reaction between the metal and Si for the phase formed. In the case of Ti and V, Si is actually the dominant diffusing species in the first phase formed, namely C49 or C54 TiSi$_2$ and VSi$_2$, and in this case the silicide is formed underneath the contact pad as opposed to along the SiNW itself. For Pt and Pd, the metal is the DDS in the first phase formed, Pt$_2$Si or Pd$_2$Si, and axial silicide segments are formed. However, in the case of Pt silicide formation, more severe annealing conditions cause a transformation to PtSi. In PtSi, Si is the DDS and Kirkendall voids form as a result of the unequal fluxes of Pt and Si causing a break to form at the interface between the PtSi and SiNW. In the case of Pd$_2$Si formation, Pd$_2$Si is the only phase that forms and the segment continues growth with increased annealing time and temperature; however, during silicidation of oxidized SiNWs Pd$_2$Si reacts through the SiO$_2$ shell surrounding the SiNW. This situation would be problematic for forming structures in which the silicide contact is underneath a gate that must provide electrical isolation. A short would form between the gate and silicide contact if a transistor were made.

Fortunately, Ni silicides also form axial metal contacts, and in the Ni-Si system, for every Ni silicide phase that forms, Ni is the DDS. We have also identified for the Ni-SiNW system that
the orientation of the SiNW can determine the Ni silicide phase that forms. In the case of annealing Ni contact pads to [112] SiNWs, the high-temperature metastable $\theta$-Ni$_2$Si phase forms and is thermally stable until annealing conditions of 700°C and higher. At 700°C branches form as a compressive stress release mechanism and could result in electrical shorts to neighboring devices in high device density applications. When annealing Ni contact pads on SiNWs with [111] growth directions, NiSi$_2$ is the first phase to form and remains stable until temperatures in excess of 600°C, where a transformation to NiSi occurs. In addition to identifying differences in the Ni silicide phase formed for SiNWs with different growth directions, we have also identified differences in the kinetics of Ni silicide formation for [112] and [111] SiNWs. For [112] SiNWs, the formation of $\theta$-Ni$_2$Si is diffusion-limited with an activation energy of $1.45 \pm 0.07$ eV/atom. This activation energy is considerably lower than literature values of bulk lattice diffusion through Ni silicide compounds, and thus the diffusion mechanism is attributed to Ni diffusion along the Si/SiO$_2$ interface. For SiNWs with [111] growth directions the formation of NiSi$_2$ is interfacial reaction limited with an activation energy of $0.76 \pm 0.10$ eV/atom. Furthermore, for the formation of $\theta$-Ni$_2$Si axial contacts to oxidized SiNWs, it was found the Ni reacted with the core of the SiNW, leaving the SiO$_2$ shell intact surrounding the $\theta$-Ni$_2$Si/SiNW interface. The ability of the $\theta$-Ni$_2$Si contact to react only with the Si core is a requirement for implementation into wrap-around gate Schottky diodes.

After identification of a suitable candidate, namely $\theta$-Ni$_2$Si contacts to SiNWs, was identified, these contacts were integrated into wrap-around gate Schottky diode structures. Simulations by Karthik Sarpattwari showed that gating of the metal/semiconductor interface in full wrap-around gate Schottky contacts was an effective approach for extracting the true Schottky barrier height at the metal/semiconductor interface. For our $\theta$-Ni$_2$Si contacts to n-type SiNWs we were able to identify the same linear relationship between the ideality factor ($n$) and
effective Schottky barrier height ($\varphi_{\text{Beff}}$) measured under different gate bias conditions. By extrapolation of the linear $\varphi_{\text{Beff}}$-$n$ plot to $n=1$ the actual barrier height at the 0-Ni$_2$Si/n-SiNW interface is identified, in this case 0.57 eV. We measured Schottky barrier heights for SiNWs ranging in diameter from 60 – 100 nm and found no significant ($\pm$ 0.02 eV) deviation or trend with SiNW diameter. A new fabrication procedure for producing smaller diameter nanowires (30 nm and less) was also developed, but issues with integration of smaller diameter SiNWs into these structures due to the reduction of the SiO$_2$ shell by the Al gate remain and are discussed.

Lastly, the formation of axial Ni germanide contacts to GeNWs has been examined. We found that axial Ni germanide segments begin forming after annealing at 300°C for 2 min and continue growing with increased time and temperature. The Ni germanide phase is identified by matching of electron diffraction patterns to the Ni$_2$In prototype structure. A stoichiometry of Ni$_3$Ge$_2$ is assigned due to the lack of vacancy ordering observed in the electron diffraction patterns. All other Ni germanide phases with the Ni$_2$In prototype structure (B8 region of the phase diagram) have been reported previously to have some vacancy ordering with the exception of Ni$_3$Ge$_2$. After annealing at temperatures in excess of 400°C, a break is formed in the Ni germanide segment near the Ni germanide/GeNW interface. Plausible reasons for the break formation are discussed. We have found the break formation problem can be worked around and that longer Ni germanide segments with average lengths of 1.5 μm can be formed after annealing at 400°C for 5 min.

**Future Work**

The work here provides information that may allow researchers to predict particular metal/semiconductor systems where axial contacts may be formed. Specifically, systems in which the first phase forming during the solid-state reaction between the metal and
semiconductor has the metal as the DDS are ideal candidates for systems to form axial contacts. As a first estimate for determining whether the metal is the DDS or not, the Cu$_3$Au rule may be applied. This rule may be applied not only in metal/Si and metal/Ge systems, but also in contacts to binary semiconductors such as InAs. For instance, recently the formation of axial Ni$_x$InAs contacts was demonstrated when annealing Ni contacts on top of InAs nanowires. Additionally, the work on the Ni-SiNW and Ni-GeNW reactions could be extended to Ni-Si$_{1-x}$Ge$_x$NW reactions.

Furthermore, because of the abrupt nature of the interfaces that result after the solid state formation of axial contacts, interesting new structures could be explored. A number of semiconducting silicides exist including $\beta$-FeSi$_2$ (direct band gap of 0.85 eV) in which interesting semiconducting heterostructures could be created between Si and and the semiconducting silicide. Furthermore, ferromagnetic silicides, including Fe$_3$Si, could potentially find application as contacts for injection of spin polarized currents for spintronic applications. Note, in both cases the Fe-SiNW system is appropriate and further study of this system could certainly result in novel structures for light emitting or spintronic applications.

Lastly, the work herein has laid out a framework for further detailed studies on the Schottky barrier height of axial silicide contacts. A number of problems were encountered in this work in the application of the wrap-around gate Schottky diodes to small-diameter SiNWs less than 30 nm in diameter. The most notable is the issue of the gate leakage current dominating the transport measurements, making extraction of the Schottky barrier difficult. The root of this problem appears to be the native SiO$_2$ dielectric grown by thermally oxidizing the SiNWs, which is reduced by the wrap-around Al gate. An alternative, and one adopted by the semiconductor industry for other reasons, is to use high-k dielectric materials as the gate dielectric as opposed to the native SiO$_2$. At the Penn State nanofabrication facility the atomic layer deposition (ALD) system is capable of depositing HfO$_2$ and Al$_2$O$_3$ with dielectric constants of 13.9 and 11.5,
respectively. By incorporating these ALD deposited gate dielectric materials, the gate leakage current could be minimized allowing for the I-V curves to be limited by the Schottky barrier. This change would make possible extraction of the Schottky barrier height from I-V data. The dielectric could be deposited onto the as-grown SiNWs still standing on the original growth substrate and then the wires would be sonicated from the substrate and device fabrication using the same procedures described in Chapter 4 would be applied to fabricate the wrap-around gate Schottky diodes. A methodology similar to this could also be applied to the Pd$_2$Si contacts where the SiO$_2$ layer was consumed during the solid state reaction. Depending on the relative mobility of Pd in the different gate dielectric materials, the Pd$_2$Si/SiNW interface could also be studied by using alternative gate dielectric materials.
Appendix

Fabrication of Small Diameter Wrap Around Gate Schottky Diodes

In the following appendix, steps are listed for the fabrication of the wrap around
gate Schottky diodes using small diameter SiNWs described in Chapter 4.

1) Start with heavily doped double side polished Si wafer coated with 100 nm of LPCVD
   SiNx on both sides. The LPCVD coating is deposited by a staff member at the Penn State
   nanofabrication facility.

2) Clean wafer by soaking in acetone for 5 min, followed by soaking in isopropyl alcohol
   for 5 min and lastly a soak in deionized water for 5 min.

3) Blow wafer dry with N₂.

4) Deposit 60 nm of Al onto one side of the wafer.

5) Randomly disperse nanowires onto the Al coated surface covering all regions where
   devices are desired – typically the entire wafer.

6) Using lithography benches at the Penn State nanofab, spin LOR2A onto one side of the
   wafer using the spin program “S.20.40/45”. Note: This program is a static spin cycle at
   4000 RPM for 45 s.

7) Start program and dispense resist in the center of the wafer until it has spread covering
   ~2/3 of the wafer. There is a 10 s delay from starting the program until the wafer will
   actually start spinning. Hit next step on spin panel control to start spinning if resist is
   dispensed before the delay is over to prevent drying of the resist on the wafer.

8) Bake wafer at 180°C for 10 min

9) Place wafer onto cool metallic plate until back to room temperature – should only take 30
   – 60 s
10) Spin SPR3012 on top of LOR2A layer previously spun, using same program “S.20.40/45” and again dispensing as described in Step 5.

11) Bake wafer at 95°C for 60 s.

12) Turn on laser for Heidelberg DWL66 Laser Writer and wait 20 minutes for laser to warm up.

13) Check to make sure the appropriate laser write head is loaded – for this application should be 2mm write head.

14) Check to make sure appropriate filters are located in the beam path – for this application should use the 10% filter. Note that the laser intensity can vary with the lifetime of the laser and if incorrect exposures are found the laser intensity can be modified using by changing the filter. The numbers on the filters indicate the transmitted intensity through the filter, i.e. a 10% filter reduces the laser intensity to 10% of its original value.

15) Load wafer onto center of plate and apply vacuum using the vacuum valve located on the stage.

16) Click “INIT” on laser writer computer to move stage underneath write head.

17) Click “Focus” on laser writer computer to focus the write head.

18) Find center of wafer and set as 0,0 point.

19) Load job file “DELLAS_1” under menu Job -> Load Job.

20) Note: This job file is a 5 x 5 array in which three of the cells are set as GCAGLOBAL alignment patterns for future theta alignment of the wafer. The other 22 cells will write the file WAGDIODE_BGATE. Array shown in Figure A-6-1.
21) Under Job -> Run Job, select expose.

22) The exposure series will begin with the first cell, which is the top left corner of the array. While viewing the wafer with the optical microscope image shown on the monitor, move around on the wafer until a wire lying horizontally is found.

23) Drag cross-hairs to the center of the horizontal wire and click “OK”. Note: Very important to copy down x-y coordinates of where each wire site is because in latter patterning steps these coordinates will be used as a shift from the center of the wafer to find each wire site.

24) Exposure will begin on this cell and the pattern will be written. This particular pattern is shown schematically in Chapter 4 as Figure 15.
25) Continue these steps until all cells have been exposed.

26) Unload wafer from laser writer.

27) Turn off laser if last user of laser writer for the day.

28) Develop wafer using CD-26 developer and immerse wafer in solution for 60 s.

29) Heat Transene Al etchant Type D to 40°C and immerse wafer to etch Al in exposed areas for

30) Rinse wafer with deionized water for 2 – 3 min to remove all Al etchant residue that may remain on wafer.

31) Blow wafer dry with N₂.

32) Soak wafer in Remover PG to remove all unexposed/undeveloped LOR2A and 3012 resist remaining on the wafer.

33) Rinse wafer with deionized water.

34) Blow wafer dry with N₂.

35) Follow steps 6 – 11 to spin LOR2A/SPR3012 double layer resist stack onto wafer.

36) Follow steps 12 – 17 to turn on laser, load wafer into laser writer, and center wafer.

37) Apply theta correction using each of the three crosses patterned along the center of the wafer.

38) Load job file “DELLAS_3” under menu Job -> Load Job.

39) Note: In this job file there is only 1 alignment site. The pattern file name for the second layer is WAGDIODE_LEFT. The x-y coordinates taken down in step 22 will be used as shifts to go to each wire site and expose. Then a new job is started and the next alignment shift is applied to go to the second site, and so on until all 22 wire sites are exposed.

40) Apply x-y shift to shift stage to the first wire alignment site.
41) Set the center of the pattern as 0,0. Note, the nanowire, and the patterned Al local back
gate should be visible now on the optical microscope. The 0,0 point should be
approximately in the middle of where the nanowire crosses the local back gate.

42) After setting the center as 0,0, select Job -> Run Job -> Expose. In this job file, an
alignment step will first be performed where the laser writer will find and center each of
the four corners of the first pattern in order to correct any misalignment from the manual
alignment performed. After the alignment step the pattern will be exposed.

43) After exposing, shift the wafer back to 0,0, which should be the center of the wire site
you just exposed.

44) Apply a negative x,y shift with the coordinates of the first alignment site to shift back to
the center of the wafer.

45) Set this location as 0,0.

46) Continue steps 40 – 45 until all 22 sites have been exposed.

47) Unload wafer from laser writer.

48) Develop wafer in CD-26 for 60 s.

49) Mix solution of 85% deionized water and 15% 10:1 buffered oxide etch.

50) Submerse wafer in solution and etch for appropriate time. For an oxide 15 nm in
thickness the time should be 90 s.

51) Rinse wafer with deionized water and blow wafer dry with N₂.

52) Immediately load wafer into Edwards evaporator, or whichever deposition system is
preferred and pump to a pressure no greater than 2 x 10⁻⁷ Torr.

53) Deposit 80 nm of Ni.

54) Liftoff in PG Remover.

55) Rinse wafer with deionized water and blow wafer dry with N₂.

56) Follow steps 6 – 11 to spin LOR2A/SPR3012 double layer resist stack.
57) Follow steps 12 – 17 to turn on laser, load wafer into laser writer, and center wafer.

58) Follow step 37 to apply theta correction.

59) Load job file “DELLAS_3” under menu Job -> Load Job.

60) Note: In this job file there is only 1 alignment site. The pattern file name for the third layer is WAGDIODE_RIGHT. The x-y coordinates taken down in step 22 will be used as shifts to go to each wire site and expose. Then a new job is started and the next alignment shift is applied to go to the second site, and so on until all 22 wire sites are exposed.

61) Follow steps 40 – 46 to align and expose all 22 wire sites with the third layer pattern.

62) Unload wafer from laser writer.

63) Develop wafer in CD-26 for 60 s.

64) Follow steps 49 – 52 to remove thermal oxide in contact region and load wafer into evaporation chamber.

65) Deposit 50 nm of Ti and 50 nm of Al.

66) Liftoff in PG Remover.

67) Rinse wafer with deionized water and blow wafer dry with N₂.

68) Follow steps 6 – 11 to spin LOR2A/SPR3012 double layer resist stack.

69) Follow steps 12 – 17 to turn on laser, load wafer into laser writer, and center wafer.

70) Follow step 37 to apply theta correction.

71) Load job file “DELLAS_3” under menu Job -> Load Job.

72) Note: In this job file there is only 1 alignment site. The pattern file name for the fourth layer is WAGDIODE_TOPGATE. The x-y coordinates taken down in step 22 will be used as shifts to go to each wire site and expose. Then a new job is started and the next alignment shift is applied to go to the second site, and so on until all 22 wire sites are exposed.
73) Follow steps 40 – 46 to align and expose all 22 wire sites with the third layer pattern.

74) Unload wafer from laser writer.

75) Develop wafer in CD-26 for 60 s.

76) Deposit 100 nm of Al.

77) Liftoff in PG Remover.

78) Rinse wafer with deionized water and blow wafer dry with N₂.

79) Anneal sample to form Ni silicide segment of desired length. See Chapter 3 for appropriate conditions for desired silicide length.
Nicholas S. Dellas

Nicholas Dellas was born in Raymond, NH on May 27th, 1983. He attended Raymond High School and graduated in 2001. He then attended the University of New Hampshire and studied Physics with a Material science option and graduated *cum laude* in 2005 with a B.S. degree. From UNH, Nicholas began graduate work in the department of Materials Science and Engineering at the Pennsylvania State University. He finished his MS degree at Penn State in December 2006 under the supervision of Dr. Suzanne Mohney, with his thesis work focusing on laser direct writing of copper interconnects for printed wiring boards. He then continued on in Dr. Mohney’s research group pursuing his Ph.D. in the department of Materials Science and Engineering studying the formation and characterization of silicide and germanide contacts to silicon and germanium nanowires, and finishing in the spring of 2011.