INVESTIGATION OF DIELECTRIC OVERLAYERS AND
DEVICE PROCESSING ON TRANSPORT AND PERFORMANCE OF
EPITAXIAL GRAPHENE FIELD EFFECT TRANSISTORS

A Thesis in
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by
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ABSTRACT

Graphene is a two-dimensional, one-atom thick layer of carbon atoms arranged in a honeycomb lattice. Exhibiting exceptional physical and electronic properties, graphene has attracted much recent attention as a novel material with potential applications in electronics and photonics. Although technical and scientific progress in the field of graphene has been rapid, many important issues remain as barriers to practical technological implementations of the material for electronic applications. Among these, device processing and materials integration without degradation or disruption of the excellent intrinsic properties of graphene are paramount.

In this thesis, materials integration of metals and dielectrics with epitaxial graphene is investigated. Various contact metals, pre-treatments, and post-treatments are compared and a reproducible, robust process for producing low specific contact resistivity metal contacts to epitaxial graphene is developed. Similarly, various gate dielectrics and methods of deposition are investigated and a reproducible, robust technique for the deposition of thin, high-k gate dielectrics on epitaxial graphene is developed. This technique utilizes high-k oxide seeds evaporated directly from a high-purity oxide source using electron beam physical vapor deposition as a seed layer for subsequent growth by atomic layer deposition. Importantly, this method not only produces uniform, conformal, and robust gate dielectrics, but also leads to an improvement in the transport properties of the underlying graphene, which has been attributed to dielectric screening and a reduction of remote charged impurity scattering. Finally, the combination of optimized contacts and high-k gate dielectrics on epitaxial graphene has allowed for the demonstration of high extrinsic current gain cutoff frequencies for graphene radio-frequency transistors.
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Chapter One: Introduction

1.1 – Goal of this Thesis

In recent years, graphene has attracted much attention as a material with potential applications in electronics and photonics. Although technical and scientific progress in the field of graphene has been rapid, many important issues remain as barriers to practical technological implementations, including high contact resistances, non-scalable synthesis techniques, and highly complicated device processing. This thesis describes an investigation to understand and overcome these barriers and to advance graphene-based technologies. Specifically, a robust technique for the formation of low specific contact resistivity contacts and also a technique for the deposition of gate dielectrics which act to enhance graphene-based transistor performance have both been developed. These developments have allowed for the demonstration of high extrinsic current gain cutoff frequencies for radio frequency graphene transistors using wafer scale growth and processing techniques. The goal of this thesis is to provide a general introduction to graphene, to summarize the efforts and progress made in developing these technologies, and to suggest future work to further advance graphene-based electronics.

1.2 – Graphene

1.2.1 – Discovery of Graphene

Graphene is a two-dimensional carbon allotrope composed of $sp^2$ bonded carbon atoms arranged in a hexagonal, honeycomb pattern that is only one atom thick. Prior to its discovery, the existence of two-dimensional crystals was thought to be impossible due to thermodynamic considerations.\(^1\) In 2004, Novoselov et al. experimentally demonstrated
the first stable, free-standing two-dimensional crystal, graphene.\textsuperscript{4} Graphene crystals, as well as other two-dimensional crystals discovered in 2004, were found to be continuous and have a high degree of crystallinity,\textsuperscript{4,5,6,7,8} and were found to exist stably on non-crystalline substrates,\textsuperscript{5,7} in liquid suspension,\textsuperscript{4,9} and as suspended membranes.\textsuperscript{8} The existence of two-dimensional crystals has since been reconciled with thermodynamic theory by explaining the crystals as existing in a meta-stable state that has been quenched from bulk material. Since their discovery, two-dimensional materials have proven to be a rich experimental platform and have demonstrated interesting physical and electronic properties not found in bulk, three-dimensional materials.

1.2.2 – Structure of Graphene

At its most basic level, graphene is simply a monolayer of graphite which has been sufficiently isolated from its environment as to be considered free standing.\textsuperscript{10} In fact, the first experimental demonstration of graphene was made by physically cleaving single layers of graphene from graphite sources composed of thousands to millions of layers of graphene.\textsuperscript{4} Like graphite, graphene has a planar structure composed of carbon atoms which are arranged in a hexagonal lattice with an atomic separation of roughly 0.142 nm.\textsuperscript{11} Within this structure, each carbon atom is connected to three others through three in-plane $sp^2$ hybridized $\sigma$-bonds to create a honeycomb pattern with an ideal bond angle of 120° between each atom. The one remaining electron orbital per carbon atom ($p_z$) exists as a highly delocalized $\pi$-orbital. Figure 1 shows the ideal hexagonal structure of graphene, where the two identical atoms of each unit cell are labeled as sublattice $A$ and sublattice $B$. 
Figure 1. Ideal honeycomb structure of graphene. The two sublattices are labeled as $A$ and $B$.

The two-dimensional structure of graphene can be manipulated to form other carbon allotropes. In this sense, graphene can be thought of as a building block for carbon allotropes of other dimensionalities. Zero-dimensional fullerenes are created by wrapping graphene into the shape of a sphere, one-dimensional carbon nanotubes are created by rolling graphene into tubes, and three-dimensional graphite is formed by stacking graphene in a Bernal stacking order (ABAB), as shown in Figure 2.
Figure 2. Bernal stacking of two layers of graphene. Repetition of these two layers in an ABABAB pattern produces bulk graphite.

1.2.3 – Properties of Graphene

Owing to its unique two-dimensional structure, graphene is host to many exceptional electronic and physical properties including a tensile strength of 130 GPa, which makes graphene the strongest material yet measured, and a thermal conductivity measured between 4800 and 5300 Wm⁻¹K⁻¹, higher than both diamond and carbon nanotubes. Although graphene is host to many amazing properties, in the initial years since its discovery most research has focused on graphene’s electronic properties and the underlying physics that explain them. The interest in graphene’s electronic properties is a result of, first, the fundamentally different way in which charge carriers in graphene are described as compared to other materials and, second, its exceptional electronic transport properties. These two aspects of graphene make it attractive as an experimental platform for the investigation of quantum electrodynamics (QED) that have no other condensed matter analog, yet also as a novel material for the implementation of unique device architectures that make use of graphene’s interesting properties or structure. For instance, by confining charge carriers to an isolated monolayer of atoms, graphene allows for direct access to the charge carriers by
other materials such as superconductors or ferromagnetics and might allow for new ways to manipulate spin, or psuedospin, or might allow for unique sensing applications.

1.2.3.1 – Physics Behind Graphene: The Massless Dirac Fermion

While the Schrödinger equation is usually sufficient to describe the behavior of charge carriers in conventional materials, graphene’s charge carriers are more naturally described using the Dirac equation (also known as the Dirac-Weyl equation). The (2+1)-dimensional Dirac equation (1) describes quasiparticles called massless Dirac fermions, which can be seen either as electrons that have lost their rest mass or as neutrinos that have acquired the electronic charge. These quasiparticles display a linear dispersion relation (2) at low energies, where the particle energy is linearly related to the momentum through the Fermi velocity, $v_F = 1 \times 10^6 \text{ m/s}$.

\[
(1) \quad \mathbf{R} = \frac{\hbar}{2\pi v_F} \begin{pmatrix} 0 & k_x - ik_y \\ k_x + ik_y & 0 \end{pmatrix} = \frac{\hbar}{2\pi v_F} \mathbf{\tilde{\sigma}} \cdot \mathbf{k}
\]

\[
(2) \quad E(\mathbf{k}) = \pm \frac{\hbar}{2\pi} v_F \sqrt{k_x^2 + k_y^2}
\]

This relationship represents a significant departure from the Schrödinger equation, not only because of the linear dispersion relation (massless particle), but also because the Pauli matrix in the equation above, $\mathbf{\tilde{\sigma}}$, refers to pseudo-spin instead of real-spin. This difference of pseudo-spin arises because the electronic states near zero energy are composed of identical states on each of the two sublattices ($A$ or $B$), which add an additional degree of freedom much like conventional electron spin does in bulk materials. In this way, pseudo-
spin represents “which lattice” and the 2D Pauli matrix is used to specify pseudo-spin as opposed to real-spin. In graphene, pseudo-spin related effects dominate over real-spin ones due to the fact that QED-specific phenomena are often inversely proportional to particle velocity, where $c/v_f \approx 300$. Figure 3 shows three-dimensional E-k diagrams for traditional “Schrödinger fermions” compared to Dirac-like particles.

![Figure 3](image-url)

**Figure 3.** Comparison of E-k diagrams for various quasiparticles. Conventional Schrodinger fermions show the expected parabolic dispersion relation (leftmost). Graphene charge carriers at low energies are best represented as massless Dirac fermions (center right), while charge carriers in bi-layer graphene are best represented as massive chiral fermions (rightmost). Different colors represent pseudo-spin of the charge carriers. Figure adapted from Ref. [10].

Conventional Schrodinger fermions display the expected parabolic dispersion relation, where particle energy is related to the square of momentum divided by the effective mass (Fig. 3a). In graphene, the conduction and valence bands display a linear, conical shape known as the Dirac cone (Fig. 3c). This is similar to ultra-relativistic Dirac particles (Fig. 3b) except that in graphene the speed of light is replaced by the Fermi velocity and the Pauli matrix represents pseudo-spin as opposed to real-spin. For bi-layer graphene, the particles are best represented as massive chiral fermions (Fig. 3d), which exhibits four graphene sub-lattices.
In either single or bi-layer graphene, the electron energy bands (pink) and hole energy bands (blue) are three-fold degenerate at the two unique points of the sub-lattice (A and B), leading to six equivalent Dirac cones (differing only by pseudo-spin) that meet at the six corners of the two-dimensional, hexagonal Brillouin zone as shown in Figure 4.\textsuperscript{15}

![Figure 4.](image.png)

**Figure 4.** Three-dimensional band structure of graphene showing the six Dirac cones in the first Brillouin zone. Adapted from Ref. [15].

The meeting point between the two energy bands in $k$-space occurs at the Fermi energy of graphene (zero-energy) and represents a vanishing density of states. The vanishing density of states can also be thought of as a zero energy bandgap; and, for this reason, graphene is often referred to as either a zero-bandgap semiconductor or semi-metal. Although such a band structure suggests extremely high resistance at this zero-energy point, random thermal fluctuations and deformations of the graphene sheet lead to the generation of both electrons and holes and the formation of electron-hole puddles which result in a universal minimum conductivity ranging between $4e^2/h$ to $8e^2/h$ (5.8 – 2.9 kΩ) depending on the intrinsic impurity concentration.\textsuperscript{16}
Besides pseudo-spin, charge carriers in graphene can also be described by another quantity, which is termed chirality. Chirality, or handedness, can be thought of as the projection of the 2D Pauli matrix onto the direction of motion and is positive for electrons and negative for holes. The combination of pseudo-spin and chirality are important for understanding many of the phenomena of graphene, such as Klein tunneling.

1.2.3.2 – Electronic Transport Properties

Although graphene’s novel Dirac like particles and structure have been the focus of many works, arguably it is the exceptional electronic transport properties, even at room temperature and high carrier concentrations, that have been the highlight of application focused research. This is because the high crystalline quality of graphene samples and unique band structure of the material leads to extremely fast conduction of charge carriers, where mobilities greater than 200,000 cm²/Vs have been reported for suspended samples in vacuum and at low temperatures \(^{17}\) and values of 10,000 – 15,000 cm²/Vs are routinely reported for exfoliated samples on SiO₂ at room temperature.\(^4,^{18}\) These large mobilities lead to extremely long mean free paths for charge carriers and might allow for room temperature ballistic transport in graphene-based devices. Moreover, electron’s and hole’s demonstrate nearly symmetric transport properties as a result of the symmetry of the Dirac-cone about the zero energy point (Fermi energy). Figure 5 plots resistivity of graphene as a function of gate bias (Fermi level), showing nearly symmetric hole- and electron-branches. E-k diagrams inset into the figure show the semi-metal transition across the Dirac point.
Additionally mobilities appear to be weakly dependent on temperature, indicating that transport is likely limited by remote charged impurity scattering and suggesting that these values may yet be improved. Importantly, mobilities remain high up to carrier concentrations on the order of $10^{13}$ carriers/cm$^2$ and carrier concentrations can be easily tuned between electrons and holes through electrical gating or chemical doping. Besides high mobilities, graphene also demonstrates high saturation velocity, with values up to $3 \times 10^7$ cm/s measured for graphene on SiO$_2$ at low carrier concentrations$^{19}$ and theoretical predictions of $4.6 \times 10^7$ cm/s for full-band Monte Carlo simulations of intrinsic graphene$^{20}$ and an extremely high current carrying capacity, with current densities as high as $10^8$ A/cm$^2$ reported for graphene nanoribbons with widths on the order of 20 nm$^{21}$. These properties far surpass typical semiconducting materials. Table 1 lists the bandgap, electron/hole mobility, thermal conductivity and intrinsic carrier concentration of several common semiconductors compared to graphene, where graphene excels in both carrier mobility and thermal conductivity.
Table 1. Bandgap, mobility, thermal conductivity, and intrinsic carrier concentration of common semiconductors as compared to graphene. Data sourced from Ref. [22].

<table>
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<th>Bandgap (eV)</th>
<th>Electron Mobility (cm² V⁻¹ s⁻¹)</th>
<th>Hole Mobility (cm² V⁻¹ s⁻¹)</th>
<th>Thermal Conductivity (W cm⁻¹ K⁻¹)</th>
<th>Intrinsic Carrier Concentration at 300K (cm⁻³)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Si</td>
<td>1.12</td>
<td>≤1,400</td>
<td>≤450</td>
<td>1.3</td>
<td>1.10 x 10¹⁰</td>
</tr>
<tr>
<td>Ge</td>
<td>0.66</td>
<td>≤3,900</td>
<td>≤1,900</td>
<td>0.58</td>
<td>2.0 x 10¹³</td>
</tr>
<tr>
<td>GaN</td>
<td>3.39</td>
<td>≤1,000</td>
<td>≤200</td>
<td>1.3</td>
<td>3.4 x 10¹⁰</td>
</tr>
<tr>
<td>SiC (4H/6H)</td>
<td>3.23/3.0</td>
<td>≤900/≤400</td>
<td>≤120/≤90</td>
<td>3.7/4.9</td>
<td>~1 x 10⁻⁵</td>
</tr>
<tr>
<td>Diamond</td>
<td>5.46-5.6</td>
<td>≤2,200</td>
<td>≤1,800</td>
<td>6-20</td>
<td>~1 x 10⁻²⁷</td>
</tr>
<tr>
<td>GaAs</td>
<td>1.42</td>
<td>≤8,500</td>
<td>≤400</td>
<td>0.55</td>
<td>2.1 x 10⁶</td>
</tr>
<tr>
<td>InAs</td>
<td>0.35</td>
<td>≤40,000</td>
<td>≤500</td>
<td>0.27</td>
<td>1 x 10¹⁵</td>
</tr>
<tr>
<td>Graphene</td>
<td>0-0.2</td>
<td>≤200,000</td>
<td>≤200,000</td>
<td>48-53</td>
<td>~2.7 x 10⁻¹⁶</td>
</tr>
</tbody>
</table>

Considering graphene’s excellent electronic transport properties in combination with its near symmetric ambipolar conduction of both holes and electrons and unique Dirac-like description of charge carriers, it’s easy to understand the great excitement generated by this amazing material since its discovery.

1.2.4 – Synthesis of Graphene

Although the initial discovery of graphene was ground breaking in establishing the stability of two-dimensional crystals, the synthesis technique used to produce those first samples could be considered somewhat inelegant. The technique, referred to as exfoliation, relies on micro-mechanically cleaving two-dimensional crystals from a three-dimensional
graphite bulk by physically dragging highly-ordered pyrolitic graphite (HOPG) across a substrate\textsuperscript{5} or by peeling off graphene layers using scotch tape.\textsuperscript{4} The process of exfoliation produces high-quality graphene crystallites up to 10 \( \mu \text{m} \) long, but simultaneously produces bi-layer and multi-layer crystallites as well. Because of the various types of crystallites produced during exfoliation, optical microscopy must be utilized to search out and identify single-layer graphene crystallites for further processing or testing. Although exfoliation produces crystallites of extremely high crystallinity that demonstrate excellent electronic properties, the technique is decidedly time consuming and impractical for wide-scale manufacturing. Synthesis by mechanical cleavage has become more efficient in recent years, even incorporating the use of ultrasonication to create suspensions of sub-micron graphene crystals which can be used to coat arbitrary substrates,\textsuperscript{23} but the introduction of new synthesis techniques such as CVD or sublimation have allowed for wafer scale synthesis of large-grained, polycrystalline graphene films and have provided promise for the eventual commercialization of graphene-based electronic technologies that require high quality, affordable graphene substrates.

\textbf{1.2.4.1 – Chemical Vapor Deposition on Metals}

The synthesis of graphene by chemical vapor deposition (CVD) on metal substrates has proven to be an excellent large-scale growth technique. Although this technique has been known to produce thin carbon films for more than 40 years, it was not until the discovery of free standing graphene and its phenomenal properties that CVD growth of carbon films became an important focus of many researchers.

When discussing synthesis of graphene on metals by CVD, there are two separate methods that must be considered: first, the method of segregation of bulk-dissolved carbon
at the surface \textsuperscript{24} and, second, the method of surface decomposition of carbon-containing precursors.\textsuperscript{25} For the first technique, carbon must first be dissolved into the metal substrate before segregation can occur. Carbon dissolution can be achieved by keeping the sample in contact with a graphite source at elevated temperatures as well as other techniques, as summarized in Ref [23]. Segregation takes place as the metal is cooled and temperature as well as cooling rate can be used to control the synthesis and morphology of the resulting graphene film. For the second technique, surface decomposition, graphene synthesis occurs by decomposition of one of various precursors, including methane, propene, ethylene, and others, onto a metal substrate at high temperatures (1000 °C). In both the segregation and decomposition techniques, transition metals such as Cu, Ni, Ru, or Ir are used as the substrate for graphene synthesis. The success of the technique comes from the fact that the growth process is self-limiting and controllable, where the growth of a single- or few-layer carbon film halts further segregation/deposition of carbon onto the metal substrate and temperature and concentration/partial pressure can be manipulated to controllably produce monolayer or few-layer films.

Although both techniques are found to produce continuous sheets of graphene, often with large domains regardless of the crystalline quality of the underlying metal, the use of a conductive metal substrate complicates device fabrication when considering graphene for electronic applications. In order to make CVD deposited graphene technologically viable, transfer\textsuperscript{26,27} and transfer-free\textsuperscript{28} processes have been developed in the past few years, where CVD graphene can be relocated onto an insulating substrate for subsequent device fabrication. In these processes, graphene films are usually bonded to a temporary substrate, often a simple polymer film that can be spun on top of the CVD graphene. The temporary substrate is then used to support the monolayer as it is removed from the metal substrate and
transferred onto an insulating substrate. After transfer, the temporary substrate can be etched away to leave only the graphene on top of its insulating substrate.

### 1.2.4.2 – Sublimation of Si from SiC

Unlike CVD based synthesis techniques, growth of graphene by sublimation of Si from SiC requires no transfer step. Instead, the technique produces a thin carbon film on top of a semi-insulating SiC substrate that allows for subsequent device processing. Silicon sublimation occurs at high temperatures (~1400-1600 °C) and can take place either in ultra-high vacuum or in an argon atmosphere. The use of argon during the sublimation process can help to improve film morphology, leading to reduced pitting and much larger domain sizes than achievable using high vacuum sublimation.\(^\text{29}\) Additionally, SiC substrates are often subjected to a hydrogen etch before the sublimation step, which takes place at elevated temperatures (>1500 °C). The use of a hydrogen etch prior to graphene synthesis is effective in removing much of the residual surface damage caused by SiC polishing techniques and promotes growth of large grains. Importantly, the hydrogen etch also leads to significant step-bunching and the formation of terraces across the SiC surface.\(^\text{30}\) Terrace formation exposes the (1\(\bar{1}0n\)) crystallographic plane of the SiC at the step-edge, as shown in Figure 6, which has important implications for the graphene morphology on the Si-face of the substrate.
Both 4H- and 6H-SiC crystals can be used for synthesis, with graphene growing on both the (0001) (silicon-terminated) and (000\(\bar{1}\)) (carbon-terminated) crystal faces. The two unique crystal faces exhibit different growth modes, which produce very different graphene films. Graphene produced by sublimation of Si from SiC is referred to as epitaxial graphene, or EG, where Si-face EG is designated as EG\(_{\text{Si}}\) and C-face EG is designated as EG\(_{\text{C}}\).

Growth on the Si-face (0001) produces single- or few-layer graphene which exhibits the same Bernal stacking found in bulk graphite. Because of its Bernal stacking, Si-face epitaxial graphene may also be referred to as few-layer graphite, or FLG. Although growth on the Si-face is self-limited and highly controllable down to a single monolayer of graphene, the presence of step-edges across the substrate surface lead to regions of multi-layer graphene interspersed between few-layer regions. This phenomenon is a result of the fact that graphene growth on the (1\(\bar{1}\)0\(n\)) crystal face differs from the (0001) face, where growth on the (1\(\bar{1}\)0\(n\)) face occurs at lower temperatures and is not self-limiting. This can lead to multi-layer regions of graphene at step edges, as shown in Figure 7.
It is thought that step-edges serve as nucleation sites for the graphene film due to their high density of dangling bonds and defective nature. \(^{31}\) Figure 8 shows a cross-sectional TEM micrograph of a step-edge that shows multi-layer graphene growth along the \((1\bar{1}0n)\) crystal face while the \((0001)\) terrace ledges show no graphene indicating that the \((1\bar{1}0n)\) face serves as a nucleation site for graphene growth.

**Figure 7.** Cross-sectional TEM micrograph (a) showing the growth of multi-layer graphene on the \((1\bar{1}0n)\) crystal face (c), while graphene growth on the \((0001)\) crystal face is limited to single- or bi-layer graphene (b). Adapted from Ref. [31].

**Figure 8.** Cross-sectional TEM micrographs of graphene nucleated on the terrace step edge of SiC at 1325 °C. Many-layer graphene is possible along the \((1\bar{1}0n)\) plane and can occur before growth of graphene on the terrace face \((0001)\). Adapted from Ref. [31].
Along the (0001) crystal face, $\text{EG}_\text{Si}$ layers are strongly bound to the substrate by means of a carbon buffer layer, which induces strong doping and significant spectral disorder at low energies near the Dirac point.\textsuperscript{32,33} Away from the Dirac point (at higher energies) Si-face epitaxial graphene display’s the typical linear dispersion relation of graphene.\textsuperscript{32} Mobilities for Si-face epitaxial graphene were initially much lower than C-face epitaxial graphene, CVD graphene, and exfoliated graphene, but are now approaching the values found in CVD graphene (~3000 cm$^2$/Vs). The limited mobility of Si-face epitaxial graphene is likely due partially to the presence of the carbon buffer layer.

Along with the problem of multi-layer regions of graphene as a result of step-bunching across SiC substrates, reduced mobility of $\text{EG}_\text{Si}$ samples remains an issue for high performance graphene devices using Si-face epitaxial graphene. Recent work to cleave $\text{EG}_\text{Si}$ from the carbon buffer layer by hydrogen intercalation has led to substantial improvements in electronic transport properties as well as reduced doping,\textsuperscript{34} suggesting that passivation or removal of the buffer layer is integral to high performance $\text{EG}_\text{Si}$.

As opposed to growth on the Si-face, growth on the C-face occurs rapidly and with little control, producing multi-layer graphene that exhibits a mix of rotationally faulted and Bernal stacked layers of graphene.\textsuperscript{35} Graphene layers that are rotationally faulted are referred to as turbostratic graphene. C-face graphene, in contrast to graphene produced on the Si-face and before passivation of the buffer layer, exhibits little doping and exceptional electronic quality due to its more free-standing nature from the SiC substrate. The improved isolation of C-face graphene is attributed to weak electronic coupling between the rotationally faulted layers in combination with shielding by the outermost graphene layers.\textsuperscript{36} The interface between graphene and the C-face of the SiC substrate is less understood than on the Si-face.

Although the weak coupling between layers promotes high mobilities, it also limits device applications. This is because external electric fields are effectively screened by only a
few layers of graphene, leaving the additional layers as shunt conducting channels that reduce device performance. Controlled growth of few or mono-layer graphene on the C-face could circumvent this problem, but, at this time, such highly controlled growth has not been possible.

1.3 – Graphene Field-Effect Transistor

The metal-oxide-semiconductor field-effect transistor (MOSFET) is the building block of modern integrated circuits and dynamic memories. Figure 9 shows the basic structure of the MOSFET, a four-terminal device with terminals designated as gate, source, drain, and body. The basic function of the MOSFET is to act as a switch, which can be suited for various electronic applications ranging from digital logic to high-frequency analog applications.

![Figure 9. Schematic cross-section of basic MOSFET structure.](image)

The MOSFET operates by use of the field-effect, where an appropriate voltage applied to the gate terminal is used to modulate the conductivity of the transistor by forming
a conductive channel between the source and drain terminals that puts the transistor into an on state. Without appropriate bias to the gate, the channel remains resistive and the transistor exists in an off state, or non-conducting state. In the conventional MOSFET, semiconductors such as silicon, gallium arsenide, indium phosphide, and gallium nitride, among others, can be utilized to form the channel of the device, where the unique ability of semiconductors to modulate their conductivity over several orders of magnitude makes them appropriate for switching applications. The different material and electronic properties of the various semiconductors make them suitable for specific applications.

Graphene’s exceptional electronic properties have made it of great interest for electronic applications; and, although not truly a semiconductor, the graphene-based field-effect transistor, or GFET, has received considerable attention. This is likely due in part to the increasing challenges facing the IC industry as it attempts to continuously scale the silicon transistor, such as increased short channel effects or the increasing dominance of parasitics in device operation. It is these challenges that have lead the IC industry to seek out alternative, post-silicon materials that offer better performance or new opportunities to overcome these challenges. Another reason for interest in the graphene FET is its potential to outperform conventional semiconductors. Graphene offers not only high electron and hole mobilities and a large saturation velocity, but is the ultimate two-dimensional material, being only one monolayer thick. This two-dimensionality may represent the ideal platform for controlling short channel effects in ultra-scaled devices. Together, these attributes have attracted much initial interest in graphene-based FETs, but there exist significant challenges to the success of such a device in either digital or analog applications.

For the graphene-based FET to be successful in digital applications, the engineering of a bandgap is paramount. Without a bandgap, the semi-metal graphene will not be able to achieve the on-off ratios necessary to be a viable replacement for silicon logic devices.
Fortunately, several solutions have been suggested for the formation of an electronic bandgap in graphene, including the application of a transverse electric field to bi-layer graphene,\(^3\) utilization of strain,\( ^4\) or the confinement of large-area graphene to form one-dimensional graphene nanoribbons,\(^5\) although the exact origin of the band gap in graphene nanoribbons is still under debate. Despite the difficulty of bandgap engineering in graphene transistors, several experimental demonstrations of GFETs with room temperature on-off ratios ranging from \(<2\) to \(100\) have been successfully realized using single-layer graphene, bi-layer graphene, and graphene nanoribbons. Still, these on-off ratios are several orders of magnitude lower than that required for digital applications as defined by the International Technology Roadmap for Semiconductors (\(>10^4\)\(^6\)) and further work remains to advance graphene to the point where it might be a viable alternative to Si-based CMOS.

Alternatively, graphene may be well suited for radio-frequency (RF) applications, where on-off ratios and power usage constraints are relaxed and the goal of the device is to operate as quickly as possible.\(^7\) Figure 10 shows a small-signal equivalent circuit of a FET for such an application along with the equivalent device schematic.
Figure 10. Schematic diagram of typical FET showing parasitic resistances and capacitances (a) and equivalent small-signal model (b) adapted from Ref [41].

Transistor RF performance is dependent on maximizing the gain and reducing parasitics of the small-signal circuit, where Equation (3) relates the device parameters to the small-signal current gain cut-off frequency \( f_T \).

\[
(3) \quad f_T \approx \frac{g_m}{2\pi} \left( \frac{1}{C_{GS} + C_{GD}} \right) \frac{1}{1 + g_{ds}(R_S + R_D)} + \frac{1}{C_{GD} \beta_m (R_S + R_D)}
\]
The small signal cut-off frequency represents the maximum switching frequency of the FET and is defined as the frequency at which the magnitude of the small-signal current gain becomes unity. Cut-off frequency, along with Mason’s Invariant and other parameters, is often used as a figure of merit to evaluate the performance of RF technologies. In this way, shorter channel lengths (smaller $C$), higher mobilities (higher $g_m$), and reduced series resistances ($R_D, R_S$) all lead to increased RF performance (higher $f_T$).

With its excellent possibility for scaling to sub-20 nm gate lengths, high transconductance and sufficiently low noise level, graphene could be an excellent candidate for RF electronics that operate into the THz regime. To this end, researchers have demonstrated graphene based RF FETs and have utilized them in low-noise amplifiers, frequency mixers, and frequency multipliers only a few years after the first reported graphene FET. Although graphene transistors in recent years have reached an impressive *intrinsic* current gain cut-off frequency ($f_T$) of 300 GHz, the *extrinsic* performance of RF GFETs has lagged behind intrinsic performance, with the highest reported extrinsic $f_T$ ($\sim 30$ GHz) over an order of magnitude smaller than the highest reported intrinsic $f_T$ (300 GHz).

The difference in extrinsic and intrinsic performance of graphene FETs is a direct result of device parasitics. Parasitic resistances in the form of contact resistances ($R_C$) or ungated portions of graphene combine to create high access resistances ($R_S, R_D$) that degrade RF performance. Additionally, un-optimized device designs might lead to unacceptably high parasitic capacitances. Along with device parasitics, the limited saturation behavior demonstrated by graphene devices and the in-ability to integrate top-dielectrics without degradation of transport properties in the underlying graphene combine to limit the ultimate achievable RF performance of graphene FETs by leading to high $g_d$ and reduced mobility (low $g_m$). In order to push graphene-based technologies forward, metal-graphene contacts
and top-gate dielectrics on graphene must be better understood and optimized. Additionally, the weak-saturation of graphene devices, device processing, and short-channel effects in graphene FETs must also be better understood.

1.3.1 – Metal-Graphene Contact

To-date the focus of electronic and opto-electronic graphene research has been to push speed and sensitivity to the extreme;\textsuperscript{56,57,58} however, little attention has been given to a potentially limiting factor in one’s ability to extract the phenomenal properties of graphene: the metal-graphene contact. Of the studies that investigate contact resistance to graphene, the lowest reported resistances are on the order of $5 \times 10^{-6}$ ohm-cm\textsuperscript{2}\textsuperscript{,59,60,61,62,64}. Although, specific contact resistances of $10^{-7}$ ohm-cm\textsuperscript{2} have been reported for Ti/Pt/Au contacts to epitaxial graphene,\textsuperscript{63} limited explanation was provided as to how these low values were achieved. Yet, in order to push graphene-based RF transistor operating speeds into the near terahertz regime, device scaling will require ohmic contacts exhibiting a specific contact resistance $< 1 \times 10^{-9}$ ohm-cm\textsuperscript{2}.\textsuperscript{64}

Currently, understanding of the graphene contact is limited. The vanishing density of states at the Dirac point leads to a low density of states (DOS) that is thought to allow metals to dope underlying graphene through a charge transfer process, as simulated using density functional theory (DFT).\textsuperscript{65} In this process, the difference in work functions between the metal and graphene are shifted into equilibrium by moving electron’s from metal to graphene. Because the density of states in graphene is much lower than that of the metal, a small transfer of charge between the materials leads to a substantial shift in the Fermi level of the graphene and a small shift in the Fermi level of the metal. While charge transfer leads to the formation of a dipole layer and establishes equilibrium between the metal and graphene,
it is thought that charge redistribution is also impacted by a metal-graphene chemical interaction, which may have a significant repulsive contribution.\textsuperscript{65} Figure 11 compares the DOS and energy band diagrams of metal contacts to graphene versus other materials.

![Figure 11. Comparison of DOS and energy band diagrams for graphene and carbon nanotubes (CNT), and conventional Schottky contacts to silicon. Adapted from Ref [66]](image)

In graphene, limited DOS at the Dirac point combined with the lack of a bandgap leads to a charge transfer to the graphene from the metal. In metallic carbon nanotubes (CNT), the higher density of states prevents any shift in the energy diagram as the CNT is able to absorb electrons without a large shift in the Fermi level. For the case of the semiconductor CNT, the CNT remains charge neutral, although the ratio of holes to electrons changes as the metal and CNT are brought into contact. This behavior is very similar to the case of the conventional metal-semiconductor contact, where the Fermi level shifts within the bandgap but there is no net accumulation of charge.
Although DFT results suggest that doping of graphene by metal contacts can be predicted using a simple analytical model, experimental graphene devices offer significantly more complex material systems as opposed to a simple metal-graphene junction and may not always exist at the Dirac point. For instance, the presence of a carbon buffer layer between at the substrate-graphene interface for the case of EG$_\text{Si}$ leads to extensive doping of the graphene, which alters the work function difference between the metal and graphene and leads to a much higher DOS in the graphene. Additionally, impurities and the presence of defects or thin layers of contamination between the metal and graphene might lead to a dramatic change in the difference between the two material’s work functions by altering the graphene metal spacing and the dipole interaction at the metal-graphene interface. Additionally, contact-induced strain or process dependent chemisorptions/physisorption differences may lead to a change in the effective work function at the metal-graphene interface.

These complications have led to experimental results that have not shown good agreement with predicted results. Particularly, Raman spectroscopy was used to show the appropriate correlation of G-peak with work function of metal contacts on graphene (where the G-peak exhibits a dependency on the Fermi level), but the carriers induced in the graphene did not match the predicted work function difference. These results indicate that the ideal work functions of the metals might not be accurate for the case of metals on graphene. Additionally, the interesting results of substrate modulated contact resistance in double-gated graphene FETs (top- and back-gated) also point to complexities at the metal-graphene interface and provide evidence for an altered energy dispersion at the metal-graphene interface or the presence of a thin effective dielectric interfacial layer at the metal-graphene interface that capacitively couples the graphene to the contacts.
1.3.2 - Dielectric-Graphene Interface

Within the GFET, the dielectric acts as an insulating spacer that capacitively couples the metal gate to the graphene channel, allowing the channel, and thus the transistor output, to be modulated. In this way dielectrics are a fundamentally essential component of the GFET and must serve several roles. First, the dielectric stack mustn’t degrade the underlying graphene structurally or reduce carrier mobility as to limit device performance. Second, the dielectric must isolate the channel and gate sufficiently to prevent leakage currents and should be robust and resistant to breakdown. Third, the dielectric should provide a good electrical interface at the graphene channel and not introduce significant amounts of fixed charge, mobile oxide charge, or interface states as to reduce the performance of the graphene FETs. Finally, the gate stack should effectively couple the metal gate to the channel and should be thin with respect to the channel length in order to reduce short channel effects.

In fabricating the graphene FET, various techniques have been used to implement top-gate dielectrics, including electron-beam physical vapor deposition (EBPVD), functionalized atomic layer deposition (ALD), and seeded ALD (either through use of a thin oxidized metal layer or a polymer buffer layer). Additionally, physical assembly techniques such as the use of thin alumina nanoribbons or self-aligned oxidized nanowires have been employed with success, although the extent to which these techniques are scalable is not clear.

While current implementations of the GFET have shown great promise using these techniques, top-gate dielectrics often cause an undesirable degradation in the transport properties of the underlying graphene, often reported as a decrease in carrier mobility. Alternatively, calculations have shown that high dielectric constant (high-κ) materials should have the effect of suppressing charged impurity scattering in the underlying graphene leading
to an increase in carrier mobility.\textsuperscript{81,82} Such an increase in carrier mobility has been shown variously by increasing the dielectric constant of a solvent overlayer\textsuperscript{83,84} or by use of an ice overlayer,\textsuperscript{85} but increase in carrier mobility with deposition of high-\(\kappa\) dielectric by conventional means such as EBPVD, chemical vapor deposition (CVD), or ALD has yet to be experimentally demonstrated.

1.3.2.1 – Physical Vapor Deposition of Dielectrics on Graphene

PVD techniques, such as EBPVD, pulsed laser deposition (PLD), spin-coating or sputtering are all suitable techniques for the deposition of thin oxide films. These techniques rely on physical processes such as thermal evaporation or sputtering to transfer source material to the substrate in order to deposit a thin film in a non-reactive or reactive environment. Although these techniques can be used to deposit dielectrics of various compositions on arbitrary substrates, including graphene, the physical processes used can often cause significant damage to the underlying substrate onto which the dielectric is deposited. Using Raman analysis of graphene after depositing a layer of SiO\textsubscript{2} by various PVD techniques, Figure 12 shows the extent of structural damage caused by the various processes.\textsuperscript{86}
Raman analysis is used to compare the relative damage introduced by the various techniques by comparing the intensities of the D and G-peaks in the graphene Raman signature. A large D/G ratio indicates a large degree of structural disorder, which is indicative of a highly damaging deposition process. Of the PVD techniques, spin coating and EBPVD lead to the smallest change in the magnitude of the D/G, indicating minimal incorporation of defects or structural damage in the underlying graphene. The deposition of oxides by PLD and RF sputtering, on the other hand, leads to significant increase in the D/G ratio and even leads to a quenching of the 2D peak (Raman signature produced by pristine graphene). The significant increase in graphene defectiveness for these two techniques leads to a degradation in the electronic transport properties of the underlying graphene and precludes their use for the deposition of gate dielectrics for graphene based electronics. Although spin-coating is found to be the least damaging PVD process, the technique is suitable only for the deposition of dielectrics that can be spun onto graphene in liquid form.
Unfortunately, this requirement means that spin-coating is unsuitable for the deposition of high-\(\kappa\) dielectrics, which will allow for better control of short channel effects and have the potential of improving transport properties by reducing remote charged impurity scattering.

Alternatively, a thin layer of low-\(\kappa\) dielectric deposited by a spin-on process can be used as a seed layer for subsequent deposition of dielectrics by another approach. The seed layer can be thought of as a buffer against physically damaging processes. Still, the use of a low-\(\kappa\) seed layer acts to increase the equivalent oxide thickness (EOT) of the dielectric stack and might prevent high-\(\kappa\) dielectrics from screening out remote charged impurity scattering, which are both undesirable for high performance GFETs.

**1.3.2.2 - Atomic Layer Deposition of Dielectrics on Graphene**

Atomic layer deposition (ALD) is a well developed technique for depositing dielectrics with a high degree of control over film thickness. Additionally, the technique can be used to deposit ultra-thin dielectrics. ALD is a CVD-based process that relies on sequential use of two gas phase precursors that are fed into a reactor in short pulses. The precursors react to deposit a single mono-layer of the desired material in a self-limiting process. After each sequential deposition of a new mono-layer, the reaction chamber is purged before the next precursor is supplied. In this way, purge gases and precursors are supplied to the reaction chamber, which is often at elevated temperature, in order to deposit a compound sequentially, layer by layer.

Deposition of dielectrics by \(\text{H}_2\text{O}\)-based ALD onto pristine graphene is complicated by the hydrophobic nature of the graphene surface\(^8^7\) and the lack of any functional groups that might allow for the molecular absorption of the gas precursors. Instead of uniform and
conformal dielectric thin films, attempts to deposit dielectrics by ALD onto pristine graphene lead to selective growth at steps between graphene layers or defects, such as pentagon-hexagon pairs or vacancies, while most of the surface remains uncoated. Figure 13 shows atomic force microscopy (AFM) micrographs of exfoliated graphene before and after deposition of ALD deposited Al₂O₃.

Figure 13. AFM micrographs of few-layer exfoliated graphene sample before (a) and after (b) deposition of ALD deposited Al₂O₃. (b) shows that the nucleation and growth of the Al₂O₃ film occurs only at steps in the graphene or at localized defects. (c) and (d) are schematic cross-sections of the samples. Adapted from Ref [88].

Figure 13b clearly shows the nucleation of dielectric growth along graphene edges and defects. The nucleation process is schematically illustrated in Figure 13c,d. In order to promote molecular absorption and, hence, dielectric growth over the graphene surface, surface functionalization of the graphene can be used to create additional functional groups for dielectric nucleation. To this end, chemical functionalization has been employed using either NO₂-TMA (trimethylaluminum) or O₃, which is flown into the reactor before
dielectric deposition. Although these techniques lead to uniform thin films <10 nm thick and without any pinholes, the use of chemical functionalization also produces an undesirable degradation in the transport properties of the underlying graphene, as shown in Figure 14.

In Figure 14, an increase in hysteresis and shift in the Dirac point is attributed dually to the introduction of a significant density of charge traps and a large fixed charge density in close proximity to the graphene. Additionally, severe degradation of both the on-off ratio and drive current is observed. This degradation is attributed to a high density of charged impurities that act to scatter carriers in the channel or, possibly, to interface phonon scattering from the deposited high-κ dielectric.

![Figure 14](image.png)

**Figure 14.** Transfer curve of back-gated exfoliated graphene before (black) and after (red) deposition of top-dielectric by ALD using a NO₂-TMA chemical functionalization, showing degradation in transport properties. Adapted from Ref [72].

Alternative to the use of chemical functionalization to create additional surface functional groups, the use of thin dielectric layers deposited prior to ALD growth can be used as a seed layer to promote coverage and uniformity. Seed layers spin-coated onto the
graphene surface\textsuperscript{76} or deposited as a thin metal layer using EBPVD\textsuperscript{74,75,79,80} have both been employed successfully for subsequent growth of dielectrics by ALD.

For the case of spin-coated seeds, a low-\(\kappa\) polymer (NFC 1400-3CP) was diluted in propylene glycol monomethyl ether acetate (PGMEA) and spun onto the graphene surface. ALD was utilized to deposit a 10 nm layer of HfO\(_2\) over the approximately 10 nm thick buffer layer.\textsuperscript{76} Dielectric constants of 13 for the HfO\(_2\) layer and 2.4 for the buffer layer were measured using capacitive analysis, while back-gate and top-gate measurements were used to compare transport properties before and after deposition of the top-gate stack.\textsuperscript{76}

![Graphene transfer curve](image)

**Figure 15.** Back-gated transfer curves of exfoliated graphene flake with polymer buffered HfO\(_2\) dielectric by ALD. The grey curve corresponds to the flake before deposition of top-gate while the green curve is just after deposition of the NFC polymer. The blue curve is after deposition of HfO\(_2\) by ALD while the red curve is after a 50 W O\(_2\) plasma etch. Adapted from Ref [76].

Although the polymer buffered high-\(\kappa\) ALD process was successful in preserving transport properties of the graphene (Fig. 15), the polymer buffer layer led to a p-type shift in
Additionally, the low-\(\kappa\) buffer layer prevented any enhancement of the graphene transport properties by dielectric screening by the high-\(\kappa\) ALD dielectric.

EBPVD represents an alternative approach to the deposition of seed layers. Although EBPVD has been shown to be more damaging than spin-deposited techniques according to Raman analysis (Fig. 12), the extent of damage is not as great as other PVD processes. Using EBPVD to deposit a thin layer of metal (1 – 2 nm), several groups have successfully demonstrated seeded ALD growth of high-\(\kappa\) dielectrics.\(^{74,75,79,80}\) The advantage of this technique is that it does not necessitate a low-\(\kappa\) buffer layer. Instead, a thin metal such as aluminum can be deposited directly onto the graphene surface using EBPVD. After removing the metal-coated graphene from the e-beam deposition chamber, the thin metal layer can be subsequently oxidized to form a high-\(\kappa\) metal oxide buffer layer, after which deposition of the bulk dielectric can take place by ALD. This process is referred to as M-ALD. Figure 16 shows AFM micrographs demonstrating the successful use of M-ALD to deposit dielectrics on epitaxial graphene using aluminum, titanium, and tantalum metal seeds.\(^{80}\)
Figure 16. AFM micrographs showing complete coverage of EG graphene using metal oxide seeded ALD with aluminum (a,b), titanium (c,d), and tantalum (e,f). Temperature of the ALD deposition is found to affect uniformity and coverage where Al₂O₃ requires temperatures >150°C and TiO₂ and Ta₂O₅ show uniform films for temperatures <150°C. Adapted from Ref. [80].

Although the EBPVD evaporated metal film should act to form a buffer layer that protects the graphene from subsequent processing, the interaction between the metal and graphene as the metal undergoes a metal $\rightarrow$ metal-oxide phase transition is not well understood. TEM micrographs of the graphene-dielectric interface after deposition of
dielectrics by M-ALD on Si-face epitaxial graphene show that most metal-seeds do not lead to increased defectiveness from as-grown graphene, Figures 17a, b, c, d.

![Figure 17. TEM micrographs of M-ALD deposited dielectrics using various metals (a-d). No significant structural defects are observed, except for the case of Ta$_2$O$_5$. Raman analysis of the same samples (e) confirms an increase in defectiveness for graphene coated with a Ta$_2$O$_5$ film deposited by M-ALD. Adapted from Ref [80].]

In Figure 17d, Raman analysis shows that negligible change in the D/G ratio occurs for all dielectrics deposited by M-ALD except for the case of Ta$_2$O$_5$, confirming that most seeds do not lead to increased defectiveness. On the other hand, the large increase in the D/G ratio with deposition of Ta$_2$O$_5$ indicates a significant increase in defectiveness, which is attributed to a large change in the unit cell volume during the metal $\rightarrow$ metal-oxide phase transition of the M-ALD process (Hf, Al, and Ti phase transitions exhibit smaller volume...
Importantly, this increase in defectiveness has been linked to degraded transport properties using non-contact mobility measurements, where tantalum seeded dielectrics show the most severe degradation in mobility over all other seeds. No seeds were found to improve mobility despite theory suggesting the reduction of charged impurity scattering with high-κ dielectric overlayer. Although these results focus on the effects of dielectric overlayers on the epitaxial graphene system, similar results are found for high-quality exfoliated graphene samples, where reductions in mobility of 40% and ~20% have been reported for samples utilizing oxidized aluminum seeds.

Degradation of transport properties with use of oxidized metal seed despite reports that metal seeds introduce minimal amounts of disorder into the underlying graphene indicate that the oxidized metal seed might be a large source of scattering for charge carriers in the graphene. Additionally, thickness dependent measurements of M-ALD deposited dielectrics show that graphene mobility decreases as top-gate dielectric thickness is increased. These results suggest the presence of charged defects in the dielectric that act as remote charged impurity scatterers and lead to reduced mobility. Figure 18 schematically represents this phenomenon, where point defects such as oxygen vacancies occupy an energy level above the graphene Fermi level and become charged by injecting an electron into the graphene to bring the oxide and graphene Fermi levels into equilibrium.
Figure 18. Energy band diagrams of graphene-oxide interface just in contact (a) and in equilibrium (b). The two materials come to equilibrium as the defects in the metal-oxide inject electrons into the graphene, leaving behind charged defects in the dielectric overlayer. Adapted from Ref [79].
Chapter Two: Experimental Plan and Methods

2.1 – Growth

In this work, sublimation was chosen as the synthesis technique. This technique was utilized to produce Si-face epitaxial graphene. The use of epitaxial graphene allowed for wafer-scale growth and processing, which, combined with the high degree of thickness control over EG_{Si}, provided high-throughput, high-yield synthesis and fabrication of graphene test structures and devices on SiC substrates. A pilot scale physical vapor transport (PVT) furnace was used for the synthesis process, which utilized inductive heating to reach temperatures as high as 1900 °C. The diameter of the PVT furnaces allowed graphitization of SiC samples as large as 100 mm diameter wafers.

With such large samples, it was possible to section the samples into multiple regions that underwent simultaneous processing using different processing techniques or materials. Using sectioned samples, comparative studies of processing techniques or materials integration could be performed on a single sample. Alternatively, multiple smaller SiC samples could be prepared concomitantly in a single graphitization step and then processed simultaneously using different processing techniques or materials. In this way, the PVT furnace provided several ways for the preparation of samples and sets of samples that facilitated comparative studies between different processing techniques or the use of different materials, such as gate dielectrics.

Graphene synthesis was achieved on the Si-face of semi-insulating 6H-SiC (II-VI, Inc.) substrates using low-pressure, Ar mediated sublimation at 1600 °C.\textsuperscript{90} As noted in Figure 19, an in \textit{situ} H\textsubscript{2} etch was performed by heating the sample to 1600°C in a 5% H\textsubscript{2}/Ar mixture at 600 Torr and holding for 60 min.
The use of an *in situ* $\text{H}_2$ etch was effective in removing much of the residual surface damage caused by SiC polishing techniques and promoted growth of large grains. Figure 20 shows the effect of the hydrogen etch step in removing residual surface damage from the SiC substrate.
Low temperature (1500 – 1400 °C) etches were found to reduce surface damage, although a significant amount remained (Fig. 20). High temperature (1700 – 1600 °C) etches were found to completely eliminate residual surface damage from the substrate, but were also found to promote step bunching. The step bunching led to the formation of terraces and terrace step edges, where terrace dimensions typically ranged from 1 to 5 μm wide and step edges were found to be 7 to 15 nm tall.

Following the etch step, the chamber was cooled to 1050°C under the H₂/Ar atmosphere and then cycle purged between 1x10⁻⁶ and 1 Torr with Ar gas in order to remove all H₂ gas from the furnace. Subsequently, the temperature was ramped to 1625°C under a 600 Torr Ar atmosphere to prepare for graphitization. Once the growth temperature was reached, the Ar pressure was quickly reduced to 1 torr and held for 15 min to allow for

Figure 20. Series of four AFM micrographs showing the effects of hydrogen etching the SiC substrate at different temperatures for 60 minutes each. Adapted from Ref. [31].
Graphitization. Following graphitization, the Ar pressure was returned to 600 torr and the furnace was cooled to room temperature.

Graphitization of SiC samples according to this process was found to produce primarily monolayer $E_G^{Si}$ on the SiC (0001) terraces and primarily bilayer $E_G^{Si}$ on the ($1\bar{1} 0n$) terrace step edges. Graphene thickness and layer number was confirmed by TEM and Raman analysis. Before Raman analysis, the SiC substrate and graphene Raman spectra must undergo deconvolution. This was accomplished by capturing the Raman spectrum of a bare SiC sample and subtracting out this spectrum from the convoluted spectra as shown in Figure 21. In this figure, the green spectrum represents the deconvoluted graphene spectrum.

![Graphene Raman Spectrum](image)

**Figure 21.** Deconvolution of substrate and graphene Raman spectra. The graphene spectrum (green) is produced by subtracting the SiC spectrum (red) from the convoluted spectrum (blue). Adapted from Ref. [31].
After deconvolution, analysis of the graphene 2D peak allows for the determination of number of graphene layers. As shown in Figure 22a, monolayer and bilayer graphene exhibit unique 2D peak shapes as compared to bulk graphite (>5 layers of graphene). Additionally, the two peak shapes differ in the fact that monolayer graphene can be fit with a single Lorentzian, while bilayer graphene necessitates four Lorentzians. Additionally, a shift in the 2D peak position from ~2760 cm$^{-1}$ to ~2730 cm$^{-1}$ was found when increasing from monolayer graphene to bilayer graphene. Although TEM micrographs confirmed the presence of monolayer and bilayer graphene on the (0001) crystal face of the SiC substrates (Fig. 22b,c), utilization of Raman mapping of the 2D peak position of the as-grown EG$_S_i$ and correlating this peak position with the peak fitting, revealed that most of the (0001) terraces are covered with a single layer of graphene (Fig. 23).

Figure 22. Raman spectra (a) showing the presence of monolayer and bilayer graphene on the SiC (0001) crystal face, confirmed by cross-sectional TEM micrographs (b) and (c), showing monolayer and bilayer graphene respectively. Adapted from Ref. [35].
Figure 23 shows a Raman map of a typical EG_{Si} Hall cross produced under the experimental growth conditions, which clearly resolves growth uniformity of the EG_{Si} graphene over the (0001) terraces. The Raman map plots the 2D peak position as a function of location across the sample, where the color bar to the right of the map describes the peak position as function of color.

In Figure 23, the red regions displayed a 2D peak position near 2760 cm\(^{-1}\) and were shown to be comprised mainly of monolayer graphene by correlating the 2D peak position with a single Lorentzian fit.\(^{35}\) Thus, the monolayer graphene was shown to be uniform over a majority of the Hall cross using the 2D peak position map. These regions can be described as an array of wide stripes separated by thin green stripes which run across the surface of the sample. The thin green stripes displayed a 2D peak position shifted to ~2730 cm\(^{-1}\) and were shown to be bilayer graphene by correlating the 2D peak position to a four Lorentzian fit.\(^{35}\)

\(^{35}\)
These bilayer regions comprised a small minority of the Hall cross surface area. The existence of multilayer graphene across terrace step edges was attributed to the different growth mode that occurs on terrace step edges, while the presence of step edges was due to the use of the *in situ* H₂ etch used to remove residual surface damage before graphitization.

2.2 – Materials Characterization

Materials characterization represents an invaluable set of tools for the analysis and characterization of the as-synthesized and post-processed graphene. Atomic force microscopy (AFM), scanning electron microscopy (SEM), and transmission electron microscopy (TEM) were used to evaluate surface morphology and structure of the as-deposited graphene and gate dielectrics, while Raman spectroscopy was used to evaluate the quality and thickness of as-grown graphene and to quantify any structural change to the graphene with deposition of dielectric overlayer. Additionally, x-ray photoelectron spectroscopy (XPS) was used to evaluate the graphene surface throughout device processing by determining the surface chemistry of the samples and detecting the presence of contaminants.

2.2.1 – Atomic Force Microscopy

AFM is a high-resolution scanning probe microscopy which consists of a cantilever with a sharp tip (probe) as well as a laser and detector. The laser and detector are designed to measure the amount of deflection of the cantilever as it is scanned across the sample. A
piezoelectric tube, or a combination of piezoelectric components, is used to move the sample in the $x$, $y$, and $z$-directions. Figure 24 shows a simple schematic of an AFM microscope.

![Figure 24. Schematic of atomic force microscope showing cantilever, laser and detector, and piezoelectric scanner. The cantilever is scanned across the sample using a feedback loop to keep the tip at constant force.](image)

Adapted from Ref. [91].

A Veeco Dimension 3100 AFM system was utilized to acquire all AFM micrographs in this work. AFM allowed for characterization of dielectric films deposited on graphene by measuring surface topology. As a characterization technique, it was used primarily to evaluate surface roughness, conformity, uniformity, and coverage of the dielectric films.

### 2.2.2 – Scanning Electron Microscopy

Scanning electron microscopy (SEM) utilizes a high-energy beam of electrons that is scanned across a sample. As the beam is scanned, electrons are scattered from the sample and then collected and focused to form an image. Although several imaging modes exist, the
primary imaging mode relies on the detection of secondary electrons which are ejected from the sample atoms by inelastic scattering with the interrogating beam of high-energy electrons. SEM micrographs offer a very high-resolution image of surface structure and topology.

A FEI Quanta 2000 scanning electron microscope using a Schottky field emission gun (FEG) was used to take all SEM images. Although more expensive and time consuming than AFM, SEM proved to be an excellent technique for observing the as-fabricated device structure and the condition of the source/drain contacts post-processing.

2.2.3 – Transmission Electron Microscopy

Transmission electron microscopy (TEM) is another type of electron microscopy which uses a high-energy beam of electrons that are transmitted through an ultra-thin specimen. The specimen is prepared by mechanical polishing followed by focused ion beam (FIB) milling. The electrons which pass through the sample interact with the atoms to scatter and form an image, which is magnified and focused onto an imaging device.

A JEOL 2010F transmission electron microscope was used to take all TEM micrographs in this work. TEM was utilized to characterize the growth of graphene by sublimation, by allowing direct observation of the number of graphene layers and any defects in the substrate or graphene. Additionally, TEM allowed for direct observation of the dielectric-graphene interface in order to quantify any structural degradation of the graphene with deposition of dielectric.
2.2.4 – Raman Spectroscopy

Raman spectroscopy is a versatile tool for the characterization of as-grown and post-processed graphene, allowing for analysis of defectiveness, crystallite size, and number of layers. Raman spectroscopy is a vibrational spectroscopic technique that uses visible light to interrogate the low-frequency modes of a material. The technique relies on inelastic scattering of high intensity monochromatic light (laser) with the optical phonons in a sample. Energy of the reflected phonons is reduced for those that impart energy to the sample in the form of lattice phonons and is increased for those that absorb lattice phonons. Due to their change in energy, these reflected phonons are shifted spectrally to lower or higher frequencies, respectively, corresponding to Stokes and anti-Stokes shifts, respectively. Raman spectrometers utilize sophisticated holographic gratings and multiple dispersion stages to isolate the shifted phonons from the Rayleigh scattered phonons.

![Diagram of Raman bands](image)

**Figure 25.** Rayleigh, Stokes, and Anti-Stokes bands reflected from a sample, plotted as a function of frequency along with the corresponding change in states that produces each band (above).
A WITec confocal Raman microscope with a 488 nm laser wavelength, diffraction limited lateral resolution of ~340 nm, and spectral resolution of 0.24 cm\(^{-1}\) was utilized for Raman spectroscopy. Raman spectra were collected using a spatial step size of 300 nm, laser power of ~60 mW (at sample), and with an integration time of 0.5 – 3 sec. Raman spectra were taken using either a low- or high-resolution spectrometer grating. The low-resolution spectral grating consisted of 600 gratings/mm and allowed for collection of the D, G, and 2D peaks of the graphene spectrum between the wavenumber values of 500 – 3000 cm\(^{-1}\). The high-resolution spectral grating consisted of 1800 gratings/mm with a spectral window of approximately 1000 cm\(^{-1}\) that allowed for the detailed capture of the 2D peak with increased accuracy over the low-resolution grating in determining both peak position and peak shape.

Raman analysis of the graphene samples required deconvolution of the SiC and graphene Raman signals, which was achieved by subtracting out the Raman spectrum of bare SiC. In graphene, the D, G, and 2D peaks are utilized to analyze the quality of the sample, where the 2D peak shape is correlated with number of graphene layers, as is the 2D/G ratio, and the D/G ratio is correlated with defectiveness. Figure 26 shows the typical Raman spectrum of graphene.
In Figure 26, the 2D/G ratio is greater than 1, indicating a graphene like Raman signature. Such a Raman signature suggests that the number of graphene layers is less than ten and likely less than 5. Additionally, the D/G ratio is small, indicating high-quality graphene. In order to determine the number of graphene layers more quantitatively, a peak fitting of the 2D peak can be utilized. The 2D peak occurs as a result of a double resonance process due to second order zone-boundary phonons with opposite momentum.\textsuperscript{92} In single layer graphene, this double resonance condition leads to a single 2D peak, which is easily fitted with a single Lorentzian peak. In bi-layer graphene, the interaction of the two graphene sheets causes the $\pi$ and $\pi^*$ bands to divide into four bands, thus causing the single 2D peak of graphene to degenerate into four peaks at nearly the same frequency.\textsuperscript{92} A careful fitting of the 2D peak of bi-layer graphene reveals four Lorentzians.
2.2.5 – X-ray Photoelectron Spectroscopy

X-ray photoelectron spectroscopy (XPS) is a quantitative spectroscopic technique that uses a beam of x-rays to analyze the surface chemistry and composition of the top 1 – 10 nm of a sample. XPS utilizes a monochromatic beam of X-rays ranging from 1 to 2 keV to eject photoelectrons from the core level electrons of atoms within the sample. The energy of the ejected electrons is measured by a high-resolution spectrometer, from which the binding energy of the electron within the atom is determined. Because the binding energy of an electron is dependent on its chemical surroundings, XPS allows not only for determination of elemental, but also chemical identification.

A Kratos Analytical Axis Ultra XPS system with a 15 μm spatial resolution was used to collect all XPS spectra in this work. The system uses a Al K-alpha x-ray source. XPS spectra were utilized to determine the oxidation state of the as-deposited and post-processed dielectrics and also to characterize the surface chemistry of the graphene during device processing and patterning.

2.3 – Device and Test Structure Fabrication

In this work, various test structures and electronic devices were prepared on graphitized SiC substrates using conventional device processing techniques. The first step in this process was the careful cleaning of the graphitized samples. Next, the isolation level was lithographically patterned across the sample. In this work, a GCA 8000 i-line stepper was used to pattern the samples at all levels. With the isolation level patterned, a plasma etch was employed to etch away the exposed graphene and isolate the active regions, after which all photoresist was stripped from the sample and the sample was cleaned. The isolation level
was used to isolate the active regions of the devices and eliminate any shunt conductances. As shown in figure 27, the patterning and deposition of the source/drain contacts followed, with appropriate pre-process and/or post-process steps applied before or after the deposition of the contacts.

![Graphene schematic diagram](image)

**Figure 27.** Schematic representation of the various steps involved from in fabricating graphene devices starting with graphene synthesis.

The contacts were deposited using e-beam evaporation, after which the sample was again stripped and cleaned. Next, top-gate dielectrics were deposited over the entirety of the sample, after which a pad-open was patterned and performed in order to remove the dielectric covering the source/drain contact pads. Finally, patterning and deposition of the top-gate contacts took place, after which the samples were ready for electrical characterization following one last strip and clean. More details regarding device processing are presented in the following sections.
2.3.1 – Sample Preparation and Cleaning

After graphitization and before device processing, graphene samples underwent an initial standard clean that included soaking each sample in a PRS-3000 (alfa aesar) bath heated to 90°C for 30 minutes, followed by an isopropyl alcohol bath for 1 minute, and N₂ blow dry. This standard clean was then utilized repeatedly throughout device processing to simultaneously strip photoresist from the samples, clean them, and prepare them for subsequent patterning and processing.

2.3.2 – Isolation

The first step in processing the samples was to define the active regions of the test structures and devices. To accomplish this, first, a photoresist mask was prepared and patterned across the sample. A bilayer resist stack consisting of LOR 5A (Microchem Corp.) and Megaposit SPR-3012 (Rohm & Hass, Inc.) was used, where utilization of a bilayer resist process allows for superior edge acuity compared to single layer resist stack. Although edge acuity was not as much a concern for the isolation step as for the metal deposition step, the use of a standard resist stack throughout all processing was preferred. The photoresist acted as a protective mask that shielded the active regions from the isolation etch. The resist was exposed using an i-line UV lightsource via the GCA 8000 stepper, after which the exposed resist was developed in Microposit MF CD-26 developer (Rohm & Hass, Inc.). A DI water bath and N₂ blow dry followed the resist develop.

After developing the resist mask, the samples were exposed to an O₂ plasma etch using a PlasmaTherm PT720 Reactive Ion Etch tool. The O₂ plasma etch lasts for 2 minutes at 75 W and utilized a mixture of O₂ and Ar gasses where 100 sccm of O₂ and 8 sccm of Ar were flowed into the etch chamber. The etch is effective in removing any exposed graphene
from the SiC substrate, where the resist mask is used to protect the active regions of the test structures and devices. Finally, the samples were stripped and cleaned for the next step using the standard clean as detailed in section 2.3.1.

2.3.3 – Source/Drain Contacts

The second step in processing the samples was to pattern and then deposit the first layer of metallization (source/drain contacts) of the test structures and devices using a lift-off process. To accomplish this, first, a photoresist mask was prepared and patterned across the sample. A bilayer resist stack consisting of LOR 5A (Microchem Corp.) and Megaposit SPR-3012 (Rohm & Hass, Inc.) was used, where utilization of a bilayer resist process allows for superior edge acuity compared to single layer resist stack. The resist was exposed using an i-line UV lightsource via the GCA 8000 stepper. The exposed resist was developed in Microposit MF CD-26 developer (Rohm & Hass, Inc.). After developing the resist, a DI water bath and N₂ blow dry were used to remove any residual developer.

After developing the resist mask and before the metal deposition, a pre-deposition descum was performed on certain samples in order to remove any resist residue from the graphene surface. A Metroline M4L Plasma Etcher was used to perform the de-scum, which could last 60 to 120 seconds at 100 W with 150 sccm of O₂ and 50 sccm of He. The short plasma etch was found to be an effective tool in reducing contact resistances.

After completing any pre-processing steps, the samples were loaded into the electron-beam physical vapor deposition system (EBPVD), which was subsequently evacuated to < $10^{-6}$ Torr. In this work, a Semicore electron-gun/thermal evaporator was used to deposit the source/drain metal stack, which consisted of two layers of metal. The first layer (10 nm) could be one of several metals, including Cu, Ni, Ti, Pd, and Pt, while the second layer (50
nm) was always chosen to be gold. The deposition process was monitored using a quartz crystal thickness monitor and metal deposition rate was controlled to a maximum of 0.3 nm per second with an initial slow ramp in deposition rate. Additionally, a pre-soak was utilized before deposition in order to create a uniform melt. Once the source/drain metals were deposited, the samples were allowed to cool under vacuum before venting the deposition chamber and removing the samples, after which the samples were stripped and cleaned for the next step using the standard clean as detailed in section 2.3.1.

2.3.4 – Top-gate Dielectrics

The fourth step in device processing was to deposit the top-gate dielectric. This was accomplished by depositing a thin layer of dielectric over the entirety of the sample, after which a source/drain pad-open was performed. In this work, deposition of gate dielectric was comprised of various steps, with ALD and EBPVD being utilized to prepare either EBPVD seeded ALD films or EBPVD-only films.

EBPVD seeded ALD dielectrics utilized a ~2 – 3 nm seed layer of SiO₂, Al₂O₃, or HfO₂ deposited via non-reactive EBPVD at < 1x10⁻⁶ Torr, using a Semicore electron-gun/thermal evaporator. Following the organic clean, samples were loaded into an e-beam evaporation chamber and pumped to 1x10⁻⁶ Torr, after which ~2 – 3 nm of the appropriate oxide seed was deposited from a high purity oxide source. The deposition process was monitored using a quartz crystal thickness monitor and deposition rate was controlled to a maximum of 0.3 nm per second with an initial slow ramp in deposition rate. Additionally, a pre-soak was utilized before deposition in order to create a uniform melt. The samples were allowed to cool under vacuum before being removed from the deposition chamber. After being removed from the e-beam chamber, samples were immediately loaded into the ALD
chamber to deposit the desired gate dielectric. The ALD chamber was preconditioned with 10 nm of the desired gate dielectric to reduce the introduction of any contaminants into the as-deposited dielectrics. Atomic layer deposition was accomplished in two steps: seed oxidation and dielectric deposition. First, seed oxidation was achieved using a 10 second pulse of H$_2$O followed by a 30 second wait, which was cycled 10 times at 100°C. This oxidation step was utilized to insure that as-deposited EBPVD seeds were fully oxidized before proceeding with deposition of the ALD dielectrics. Second, oxide deposition was achieved utilizing a water based chemistry that required a pulse of water followed by a wait period and a pulse of the correct precursor followed by another wait period. The necessary pulses and wait periods were material and temperature specific, and happen according to a set number of cycles. A Cambridge Savannah 200 atomic layer deposition tool was used to deposit all ALD films in this work. Table 2 summarizes the seed material, ALD precursor, and deposition temperatures utilized in this study.

<table>
<thead>
<tr>
<th>EBPVD seed material</th>
<th>ALD dielectric material</th>
<th>ALD precursor</th>
<th>deposition temperature (°C)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Al$_2$O$_3$ or HfO$_2$</td>
<td>Al$_2$O$_3$</td>
<td>Triethylaluminum</td>
<td>300</td>
</tr>
<tr>
<td>Al$_2$O$_3$, HfO$_2$, or SiO$_2$</td>
<td>HfO$_2$</td>
<td>Tetrakis(dimethylamino)hafnium</td>
<td>250</td>
</tr>
</tbody>
</table>

The seeded ALD process in this work can be considered similar to previous work utilizing oxidized metal seeds (metal→metal-oxide),$^{79,80}$ but with one important distinction: the seed is deposited directly from a high-purity oxide source. This process, referred to as oxide seeded ALD (O-ALD), omits the metal to metal-oxide phase transition of the oxidized metal seeded process (M-ALD), which may be a source of transport degradation in graphene.
Compared to other techniques for depositing dielectrics, O-ALD requires no chemical functionalization of the graphene surface, which may alter electronic properties; bypasses the oxidation step of M-ALD techniques, which may degrade carrier mobility;\textsuperscript{79,80} and allows for a high-κ seed layer in intimate contact with the graphene as opposed to techniques utilizing low-κ seeds. It is thought that these differences should allow for minimal impact on carrier transport while simultaneously promoting dielectric screening, though charge traps and/or a high density of fixed oxide charge may still negatively affect transistor performance and charge transport in the underlying graphene.

In addition to seeded ALD dielectrics, 5 and 10 nm EBPVD dielectrics composed solely of Al\textsubscript{2}O\textsubscript{3} or HfO\textsubscript{2} were also prepared under the same conditions as the EBPVD seeds. Table 3 details the composition and thickness of the various gate dielectrics studied.

<table>
<thead>
<tr>
<th>deposition technique</th>
<th>seed layer\textsuperscript{a}</th>
<th>seed thickness (nm)</th>
<th>dielectric layer</th>
<th>dielectric thickness (nm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>O-ALD</td>
<td>SiO\textsubscript{2}</td>
<td>2</td>
<td>HfO\textsubscript{2}</td>
<td>10</td>
</tr>
<tr>
<td>O-ALD</td>
<td>HfO\textsubscript{2}</td>
<td>2</td>
<td>Al\textsubscript{2}O\textsubscript{3}</td>
<td>8</td>
</tr>
<tr>
<td>O-ALD</td>
<td>HfO\textsubscript{2}</td>
<td>2</td>
<td>HfO\textsubscript{2}</td>
<td>8</td>
</tr>
<tr>
<td>O-ALD</td>
<td>Al\textsubscript{2}O\textsubscript{3}</td>
<td>2</td>
<td>Al\textsubscript{2}O\textsubscript{3}</td>
<td>8</td>
</tr>
<tr>
<td>O-ALD</td>
<td>Al\textsubscript{2}O\textsubscript{3}</td>
<td>2</td>
<td>HfO\textsubscript{2}</td>
<td>8</td>
</tr>
<tr>
<td>EBPVD</td>
<td>-----</td>
<td>-----</td>
<td>HfO\textsubscript{2}</td>
<td>5</td>
</tr>
<tr>
<td>EBPVD</td>
<td>-----</td>
<td>-----</td>
<td>HfO\textsubscript{2}</td>
<td>10</td>
</tr>
<tr>
<td>EBPVD</td>
<td>-----</td>
<td>-----</td>
<td>Al\textsubscript{2}O\textsubscript{3}</td>
<td>5</td>
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<tr>
<td>EBPVD</td>
<td>-----</td>
<td>-----</td>
<td>Al\textsubscript{2}O\textsubscript{3}</td>
<td>10</td>
</tr>
</tbody>
</table>

After depositing the top-gate dielectric over the entirety of the sample by either EBPVD or O-ALD, the samples were allowed to cool under vacuum (EBPVD) or in the
ALD system (O-ALD). After cooling to room-temperature, the samples were cleaned for the next step using the standard clean as detailed in section 2.3.1.

2.3.5 – Pad-Open

The next step in device processing was the removal of the deposited gate dielectric from the already deposited source/drain contact pads. Because the gate dielectric was deposited over the entirety of the sample, this step was critical in exposing the contact pads so that probes could make contact to the test structures and devices without the top gate dielectric acting as a dielectric barrier. This step is accomplished using a photoresist mask to protect the gate dielectric except in regions where probes need to make contact to the first metallization layer, namely the source/drain contact pads. A bilayer resist stack consisting of LOR 5A (Microchem Corp.) and Megaposit SPR-3012 (Rohm & Hass, Inc.) was used. The resist was exposed using an i-line UV lightsource via the GCA 8000 stepper. The exposed resist was developed in Microposit MF CD-26 developer (Rohm & Hass, Inc.). After developing the resist, a DI water bath and N₂ blow dry were used to remove any residual developer.

After developing the resist mask, the samples were exposed to a reactive ion plasma etch using an Applied Materials Magnetically Enhanced Reactive Ion Etch (MERIE) dielectric etch tool. The MERIE etch lasts for 6 minutes at 70 W and utilized a mixture of CHF₃ and CF₄ gasses. The etch is effective in removing the deposited top-gate dielectric from the source/drain contact pads, where the resist mask is used to protect the dielectric in other regions of the sample. Finally, the samples were stripped and cleaned for the next step using the standard clean as detailed in section 2.3.1.
2.3.6 – Gate Contacts

The final step of device processing was the patterning and deposition of the top-gate metal contact and contact pad. To accomplish this, first, a photoresist mask was prepared and patterned across the sample. A bilayer resist stack consisting of LOR 5A (Microchem Corp.) and Megaposit SPR-3012 (Rohm & Hass, Inc.) was used. The resist was exposed using an i-line UV lightsource via the GCA 8000 stepper. The exposed resist was developed in Microposit MF CD-26 developer (Rohm & Hass, Inc.). After developing the resist, a DI water bath and N₂ blow dry were used to remove any residual developer.

After developing the resist mask and before the metal deposition, a pre-deposition de-scum was performed to remove any resist residue from the top-gate dielectric. A Metroline M4L Plasma Etcher was used to perform the de-scum, which lasted 60 seconds at 100 W with 150 sccm of O₂ and 50 sccm of He.

After completing the plasma de-scum, the samples were loaded into the electron-beam physical vapor deposition system (EBPVD), which was subsequently evacuated to < 10⁻⁶ Torr. In this work, a Semicore electron-gun/thermal evaporator was used to deposit the gate metal stack, which consisted of a thin adhesion layer (10 nm) of Ti and a thick (50 nm) Au overlayer. The deposition process was monitored using a quartz crystal thickness monitor and metal deposition rate was controlled to a maximum of 0.3 nm per second with an initial slow ramp in deposition rate. Additionally, a pre-soak was utilized before deposition in order to create a uniform melt. Once the source/drain metals were deposited, the samples were allowed to cool under vacuum before venting the deposition chamber and removing the samples, after which the samples were stripped and cleaned for the next step using the standard clean as detailed in section 2.3.1.
2.3.7 – Device Geometries

In this work, several different test structures and devices were fabricated. Transfer length measurement (TLM) structures were used to evaluate the metal-graphene contacts, and consisted of a set of six pairs of metal pads with varying distance between each pair of pads (Figure 28). The width of the pads, Z, was 25 μm and consistent between all sets, while pad spacing varied for each pair of pads and ranged from 0.75 μm to 3.0 μm.

![Figure 28. Optical micrograph of TLM test structures (0.7 refers to a pad spacing, d, of 0.75 μm.](image)

Van der Pauw (VdP) structures were used to measure Hall mobility and carrier concentration and consisted of 5x5 μm squares as shown in Figure 29. Both gated and ungated VdP structures were prepared.
Radio-frequency (RF) graphene field-effect transistors (GFETs) were fabricated with a range of source-drain spacings and gate dimensions. In this work, all GFETs utilized a two-finger gate design as shown in Figure 31. The two finger design allows for the use of conventional ground-signal-ground probes for high-frequency measurements.
Transistors utilized source-drain spacings of either 1.0 or 1.5 µm, with most device testing performed on the GFETs utilizing a source-drain spacing of 1.0 µm. On each die, GFETs of varying gate length ($L_g$) and gate width ($W_g$) were patterned. Gate widths were either 3, 5, 10, or 25 µm, while gate lengths were either 1.0, 1.25, or 1.5 µm.

### 2.4 – Electrical Characterization

#### 2.4.1 – Contact Resistance

In order to characterize both contact resistance and specific contact resistance, the transfer length method (TLM) was utilized. The TLM method utilized the TLM structures described in section 2.3.7. The technique required an additional etch to restrict the current flow to the graphene that exists between the two pads and eliminate any shunt conductances. This etch was accomplished during the isolation step. In this technique, direct current (DC) measurements of the total resistance ($R_T$) between two contact metallizations were plotted as a function of the spacing between the contacts. Plotting $R_T$ in this way allowed for the extraction of contact resistance ($R_C$), sheet resistance ($R_S$), and transfer length ($L_T$), where $R_T$ was the sum of the metal resistance ($R_M$), the metal/graphene interfacial resistance ($R_C$), and the graphene sheet resistance ($R_S$) as shown in Figure 32.
Figure 32. Generalized schematic of the origin of various resistances that arise in graphene devices.

Assuming the metal resistance to be negligible compared to all other resistances and assuming the contact pads are of sufficient size, the transfer length method yields:

\[
(4) \quad R_T = R_S \times \frac{d}{Z} + 2R_C;
\]

where \( R_S \) was measured in Ohms/square, \( d \) is the spacing between TLM contacts, and \( Z \) is the width of the TLM structures. Plotting \( R_T \) versus contact spacing \( (d) \), the slope of the line yields \( R_S/Z \); while the value of \( R_T \) at \( d = 0 \) is twice \( R_C \). Further extrapolation of the line to \( R_T = 0 \) yields a negative contact spacing \( (-d) \) that is equal to twice the transfer length \( (L_T) \). The transfer length represents the distance over which the majority of the current passes between the metal and graphene and can be either shorter or longer than the length of the metal contact. The previous analysis is only valid when \( L_T \) is less than the length of the metal contact. Finally, utilization of \( L_T \) allowed the extrapolation of the specific contact resistance \( (\rho_c) \) via: \( \rho_c = R_G \times (L_T)^2 \). Figure 33 shows a typical TLM data set and labels the extracted parameters.
Figure 33. Example data set from a set of measurements on a TLM test structure with parameters of interest labeled. Adapted from Ref. [93].

The specific contact resistance ($\rho_c$), a measure of the metal/graphene interfacial resistance, is highly sensitive to metal/semiconductor interfacial reactions or device processing conditions that could lead to interfacial contamination. Thus it was an ideal way to evaluate the quality of the metal/graphene electronic interface.

When performing TLM measurements, a four-point Kelvin probe setup was utilized to mitigate the effects of external series resistances in the probes, cables, and measurement equipment. Figure 34 shows such a setup.

Figure 34. Schematic representation of four-point Kelvin probe setup. Adapted from Ref. [93].
Employing a four-point technique, two probes are utilized to carry the current while the other two are utilized to measure the voltage between the contact pads. This setup allows the voltage measuring probes to carry effectively zero current. Thus, the probe and cable resistances can be eliminated by calculating resistance using the voltage measured between the two voltage measuring probes and the current carried by the current carrying probes.

### 2.4.2 – Hall Effect Measurements

Hall effect measurements were used to evaluate the effect of seed layer and dielectric overlayer on carrier transport within the graphene by measuring carrier density and Hall mobility before and after deposition of the dielectric overlayer. Changes in carrier density were indicative of a charge transfer process between the graphene and dielectric, as discussed in section 1.3.2., while changes in Hall mobility might be linked to an increase in scattering due to impurities or a decrease in scattering due to dielectric screening.

The Hall effect measurement relies on the Hall effect to determine carrier density. The Hall effect is the effect produced when a perpendicular magnetic field \( B \) is applied to a current. The applied magnetic field induces a Lorentz force on the charge carriers according to:

\[
F = q(E + v \times B);
\]

where the Lorentz force, \( F \), on each carrier is a function of the carrier charge, \( q \), the carrier velocity, \( v \), and the applied magnetic field, \( B \). The Lorentz force in conjunction with
the electric current leads to a displacement of carriers to one side of the sample, producing an electric field which is perpendicular to both the current and applied magnetic field as shown in Figure 35. This electric field produces a voltage, known as the Hall voltage, $V_H$.

![Figure 35. Schematic representation of Hall effect measurement where $I_x$ is the current source and $V_H$ is the measured Hall voltage.](image)

The Hall coefficient, $R_H$, is defined as:

$$ (6) \quad R_H = \frac{dV_H}{BI} $$

where $d$ is the thickness of the sample, $V_H$ is the Hall voltage, $B$ is the applied magnetic field, and $I$ is the applied current. Using a single carrier model that assumes the presence of only one carrier type, carrier density is extracted from $R_H$ according to Equation (7) while Hall mobility is extracted using $R_H$ along with the sheet resistance of the sample, as shown in Equation (8). Such a model is valid for heavily doped Si-face graphene where carrier concentration is fixed per layer and dominated by a single carrier type, unlike C-face multilayer graphene where carrier type and density can vary layer to layer.94
where \( N_{sh} \) is the sheet carrier density of charge carriers in carriers/cm\(^2\), \( \mu_{Hall} \) is the Hall mobility in cm\(^2\)/V·sec, and \( R_{sh} \) is sheet resistance in Ohms/square. Hall mobility is a measure of carrier mobility that is determined from the Hall effect and differs from conductivity mobility by the Hall factor, \( r \). The Hall factor usually lies between 1 and 2 and is related to the type of scattering mechanisms present in the sample. For the case of ideal charged impurity scattering, which is thought to play a dominant role in graphene samples, \( r \) is typically 1.93.\(^{95,96}\)

The Hall effect measurements were carried out using the Van der Pauw (VdP) structures as described in section 2.3.7. Hall effect measurements were made under high vacuum (< 5x10\(^{-8}\) Torr) at 300 K in a ±0.5 T magnetic field prior to and following deposition of the gate dielectric using a 10 µA direct current source. Hall effect measurements allowed direct sampling of carrier density and Hall mobility without relying on curve fitting. It also had the advantage of removing any uncertainty due to the accurate measurement of back or top gate capacitances, which is important for the case of top-gated graphene.\(^{97}\) Samples were annealed \textit{in situ} and under vacuum at 400 K for 60 min before measurement in order to ensure desorption of water or other contaminants from the surface of the graphene, preventing any extrinsic doping of the EG except that caused by the gate dielectric or the substrate. Gated Hall effect measurements were also performed under vacuum to determine the extent to which carrier density could be modulated by gate bias. In addition to Hall effect measurements under vacuum, both un-gated and gated Hall effect measurements in ambient atmosphere were also performed.
Hall effect measurements under vacuum were preformed in a LakeShore CPX-VF Cryogenic Probe Station. The system utilizes a refrigerant coolant system to cool a superconducting magnet to 5 K, allowing for magnetic fields up to 2.5 T in a vertical field arrangement. Additionally, temperature controllers allowed for measurements from 2 – 400 K, while a Varian turbo pump was utilized to evacuate the system before cooling. For Hall effect measurements under ambient conditions, a Nanometrics Hall System was used. The Nanometrics system employs a 0.5 T permanent magnet in a vertical field arrangement which can be mechanically rotated into positive and negative field orientations. Hall effect measurements under positive and negative fields were averaged together in an attempt to account for any non-symmetric effects as a function of geometry. Both systems sourced a 10 µA direct current to measure sheet resistance and Hall voltages using a Van der Pauw Hall arrangement.

2.4.3 – Direct Current Electrical Characterization of Transistors

GFET performance was characterized using drain current versus gate voltage \((I_{ds}-V_{gs})\) sweeps at \(V_{ds}=1V\), also referred to as a transfer curve, and drain current versus drain voltage \((I_{ds}-V_{ds})\) sweeps at select gate biases. Typical \(I_{ds}-V_{gs}\) plots for samples utilizing the ~10 nm thick top-gate dielectrics were swept from \(-3 \text{ V} < V_{gs} < 3 \text{ V}\), although voltage range scaled with dielectric thickness. From these plots, several parameters of interest were extracted, listed in Table 4.
Table 4. Parameters of interest extracted from direct current measurements of GFETs.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Definition</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_{ds,max}$</td>
<td>Peak drive current during a single $I_{ds}$-$V_{gs}$ sweep.</td>
</tr>
<tr>
<td>$I_{ds,min}$</td>
<td>Minimum drive current during a single $I_{ds}$-$V_{gs}$ sweep.</td>
</tr>
<tr>
<td>On-off Ratio</td>
<td>Ratio of peak drive current to minimum drive current, $I_{ds,max}/I_{ds,min}$.</td>
</tr>
<tr>
<td>$g_{m,max}$</td>
<td>Peak transconductance ($g_m$), where $g_m = \frac{\partial I_{ds}}{\partial V_{gs}}$.</td>
</tr>
<tr>
<td>$g_{m,min}$</td>
<td>Minimum transconductance ($g_m$), where $g_m = \frac{\partial I_{ds}}{\partial V_{gs}}$.</td>
</tr>
<tr>
<td>$V_{half,forward}$</td>
<td>Voltage where $I_{ds} = 1/2(I_{ds,max} - I_{ds,min}) + I_{ds,min}$ as $V_{gs}$ is swept from negative to positive bias.</td>
</tr>
<tr>
<td>$V_{half,reverse}$</td>
<td>Voltage where $I_{ds} = 1/2(I_{ds,max} - I_{ds,min}) + I_{ds,min}$ as $V_{gs}$ is swept from positive to negative bias.</td>
</tr>
<tr>
<td>$\Delta V_{half}$</td>
<td>Hysteresis between $I_{ds}$-$V_{gs}$ sweeps, $V_{half,forward} - V_{half,reverse}$.</td>
</tr>
<tr>
<td>$I_{g,leak}$</td>
<td>Maximum gate leakage current during a single $I_{ds}$-$V_{gs}$ sweep.</td>
</tr>
</tbody>
</table>

Peak drive current ($I_{ds,max}$), peak transconductance ($g_{m,max}$), an on-off ratio were extracted from the $I_{ds}$-$V_{gs}$ sweeps. Additionally, maximum gate leakage current ($I_{g,leak}$) and minimum drive current ($I_{ds,min}$) were extracted from the plots. Finally, hysteresis was calculated from the $I_{ds}$-$V_{gs}$ sweeps and was defined as the difference between $V_{half,forward}$ and $V_{half,reverse}$, where $V_{half,forward}$ was the voltage at which the current was halfway between $I_{ds,min}$ and $I_{ds,max}$ while sweeping from negative to positive gate biases and $V_{half,reverse}$ was the same voltage while sweeping from positive to negative gate biases. Figure 36 shows a typical transfer curve. These parameters were important in comparing the various gate dielectrics.
studied, where higher peak drive currents, peak transconductances, and on-off ratios indicated higher performance devices.

![Figure 36](image-url).

**Figure 36.** Typical transfer curve with $I_{ds,min}$, $I_{ds,max}$, $g_{m,max}$, $V_{half,forward}$ and $V_{half,reverse}$ labeled (left) and typical set of $I_{dc}$-$V_{ds}$ curves (right).

A Keithley SCS-4200 Semiconductor Characterization System was utilized to make all DC measurements. The system made use of Keithley 4200 MPSMU (medium power source-measure unit) and Keithley 4200 HPSMU (high power source-measure unit), both with optional pre-amps for increased accuracy during low current measurements. The SCS-4200 controlled a Cascade Microtech 12000 Prober, which allowed for automated, wafer-scale testing of DC FET performance. Cascade Microtech ACP40-GSG-150 probes were used to make contact to the device under test. These probes utilized an air coplanar design with a 150 µm pitch that allowed for device characterization from DC to 40 GHz and
displayed a characteristic impedance of 50 Ohms. The probes utilized a ground-signal-ground (GSG) design which facilitated RF measurement as shown in Figure 37.

![Figure 37. Schematic representation of GSG probes making contact to a RF GFET.](image)

Similar to TLM measurements, a Kelvin probe setup was utilized for DC FET measurements. In this case though, the Kelvin probe setup was applied to an Anritsu Kelvin Bias Tee model number K252 that allowed for the superposition of a high-frequency small signal voltage over the DC signal. The superposition of a small signal voltage allowed for RF characterization up to 40 GHz. Figure 38 schematically illustrates the test setup.
2.4.4 – Small Signal Characterization of Transistors

Small signal transistor characterization was completed using an Anritsu 37269B Vector Network Analyzer which was integrated with the Keithley SCS-4200 characterization system as shown in Figure 38. The use of a vector network analyzer allows for the accurate characterization of scattering parameters (S-parameters) by measuring the amplitude and phase of test signals going into and out of the device under test (DUT). The Anritsu network
analyzer was utilized to measure S-parameters from 50 MHz to 40 GHz at select bias conditions.

A short-open-load-through (SOLT) calibration was performed before all RF measurement sessions using a Suss MicroTec CSR-8 Calibration Substrate. This allowed for the quantification of systematic errors in the setup by moving the plane of measurement to the probe tips and calibrating out any error due to cabling or probes. The SOLT method is a two-port calibration which is typical for coaxial transmissions. It relies on a short, open, and load at each port in order to measure reflection errors and isolation between the ports. Additionally, the through standard is used to measure frequency response tracking. After calibration, the device measurements can be error-corrected for greater accuracy.

Extrinsic small signal current gain \( H_{21} \overset{\text{def}}{=} \frac{I_2}{I_1} \), where \( I_2 \) is the output current and \( I_1 \) is the input current) was extracted from the devices in order to determine the extrinsic current gain cut-off frequency \( f_T \) of the transistors, where \( H_{21} \) is determined from the measured S-parameters according to Equation (9).

\[
(9) \quad H_{21} = \frac{-2S_{21}}{(1-S_{11})(1+S_{22})+S_{12}S_{21}}
\]

Additionally, on-wafer de-embed structures consisting of open and short structures were used to calibrate out pad and device parasitics so that intrinsic small signal current gain might be characterized. The de-embed process follows Equation (10), where the measured S-parameters of the open and short structures are removed from the S-parameters of the DUT by first converting the S-parameters to Y-parameters.

\[
(10) \quad Y_{\text{intrinsic}} = [(Y_{DUT} - Y_{\text{open}})^{-1} - (Y_{\text{short}} - Y_{\text{open}})^{-1}]^{-1}
\]
Ideally, the extracted extrinsic and intrinsic $H_{21}$ should follow a $1/f$ relationship with measurement frequency. The point where $H_{21}$ is equal to unity represents the maximum frequency at which current gain is found ($I_2/I_1 = 1$) and is defined as the small signal current gain cutoff frequency ($f_T$). Additionally, Mason’s unilateral power gain can be extracted from the S-parameters according to Equation (11):

$$U = \frac{|S_{21} - 1|^2}{2\pi |S_{12}|^2 - 2\text{Re}(S_{21})}$$

Similar to the extraction of $f_T$, $f_{\text{max}}$ can be extracted from $U$ by finding the frequency at which $U$ is equal to 1. $f_{\text{max}}$ represents the maximum frequency at which there exists power gain and is called the maximum oscillation frequency. Both $f_T$ and $f_{\text{max}}$ are used as figures of merit to evaluate the performance of RF GFETs, where higher values represent higher performing devices.
Chapter Three: Results

3.1 – Optimizing the Metal-Graphene Interface

As discussed in Section 1, the metal-graphene interface is a critical component of the graphene transistor that has the potential to limit ultimate device performance in the form of parasitic resistances. These parasitic resistances become even more important as the channel is scaled to shorter lengths due to the fact that the channel resistance, $R_{ch}$, scales with channel length while contact resistances, $R_C$, does not. Although the metal-graphene interface is not well understood, it is clear from initial work that the metal-graphene interface must be improved.

Initial work studying the effect of various gate dielectrics on GFET performance indicated that the metal-graphene interface was of poor quality when metal contacts were simply evaporated onto the graphene without any pre- or post-processing. Figure 39 shows two subsequent transfer curves for one of these initial devices. The device utilized a Ti/Au metal stack for source/drain contact metallizations and employed no pre- or post-processing.
Figure 39. Two subsequent transfer curves of GFET utilizing Ti/Au source/drain metallizations without any pre- or post-processing to improve contact resistance. The leftmost plot shows the initial transfer curve while the rightmost plot shows a subsequent sweep.

In Figure 39, the reverse sweep from positive $V_{gs}$ to negative $V_{gs}$ shows the expected behavior of a EG$_{Si}$ GFET undergoing gate modulation, but the forward sweep, which occurred first, exhibits a sudden loss of conduction through the channel for $V_{gs}$ ranging from -7 to 0 V. This sudden loss of conduction can be explained by an interfacial contamination layer at the metal-graphene interface that works to effectively halt conduction through the channel at low bias conditions. This interfacial contamination layer might be the result of photoresist residue or some other type of contamination layer that exists on top of the graphene during source/drain contact metallization and can be thought of as a thin dielectric spacer between the metal and graphene. This thin dielectric spacer can be punched through at high bias conditions. The normal behavior of a subsequent transfer curve (Fig. 37b) and the reverse sweep of the first transfer curve (Fig. 37a), indicates that such an interfacial contamination layer likely existed and that the contamination layer may have experienced permanent punch through during the first transfer curve at large positive gate biases. The
existence of a thin contamination layer also might explain the interesting results of substrate modulated contact resistance in double-gated graphene FETs. 98, 99

In order to determine the presence of any contamination on the surface of the graphene, X-ray photo-electron spectroscopy (XPS) was utilized on a pristine EG\textsubscript{Si} surface and compared to EG\textsubscript{Si} that has been initially coated with photoresist (either Microchem LOR 5A or SPR-3012), subsequently flood exposed to ultraviolet light, and finally soaked in resist developer. Figure 40 compares the XPS spectra of these three graphene samples.

![Graphene XPS spectra](image)

**Figure 40.** X-ray photoelectron spectroscopy reveals that the graphene and SiC peaks are severely attenuated following lithographic processing, suggesting that residual resist residue remains. Adapted from Ref. [100].

The XPS results showed that the use of photoresist in graphene processing leads to the appearance of both C-O and C=O peaks in the XPS spectra (Fig. 40), while pristine EG\textsubscript{Si}
showed no such peaks. These peaks indicated high levels of carbon-oxygen single (C-O) and double (C=O) bonds and was indicative of a residual contamination layer as a result of photolithographic processing. Additionally, Figure 40 showed a severe attenuation in the graphene and SiC XPS peaks after photolithographic processing, indicative of a contamination layer that coated the EGs samples.

Although pristine graphene exhibited no contamination, the necessity to pattern the graphene during the isolation step and before source/drain metallization to ensure good adhesion of the source/drain contacts prompted the investigation into pre- and post-process steps that could effectively remove the residual photoresist contamination from the graphene.

3.1.1 – Effect of Pre- and Post-Processing on Metal-Graphene Interface

Previous work suggested that thermal treatments in an H2 ambient at elevated temperature (> 400 °C) provided a route to effectively remove photoresist residue following photolithographic processing; as a result, initial attempts utilized a rapid thermal heat treatment to contact graphene “through” the resist residue. Whereas previous work showed reduced photoresist residue after thermal treatments for uncovered graphene samples, the remaining residue for the metalized graphene suggested that an “in situ” processing step could lead to significantly reduced contamination compared to the post-metallization thermal treatment. This was due to the fact that contact metallization likely reduces or prevents the photoresist contamination from being effectively reduced (removed) by the post-process H2 heat treatment.

The utilization of oxygen plasma is often used to isolate the graphene channel in devices by etching away the graphene; however, we found it can also be utilized to remove residual resist prior to metal deposition when implemented properly. Figure 41 shows the
effect of $O_2$ plasmas of various durations on the XPS (left) and Raman spectra (right) of $E_{G_{Si}}$ samples that had undergone photolithographic processing using SPR-3012 photoresist.

Figure 41. As evidenced by the reduction in SiC substrate attenuation, resist residue is successfully removed through the utilization of an $O_2$ plasma treatment (a), however, as the plasma treatment progresses, the underlying graphene degrades. Raman spectroscopy (b) confirms the formation of a high density of defects (evidenced by the increase in D peak intensity), which correlates with the formation of C-O bonds found in XPS (a). Adapted from Ref. [Error! Bookmark not defined.].

In Figure 41, the use of an oxygen plasma after photolithographic processing was shown to reduce the attenuation of the SiC substrate XPS peak, yet also to introduce a significant C-O peak. The reduction in attenuation of the SiC peak was attributed to the removal of resist residue through the utilization of an $O_2$ plasma treatment; however, as the plasma treatment progresses, it is thought that the $O_2$ plasma introduced a significant number of defects into the exposed graphene. Raman spectroscopy (Fig. 41, right) was utilized to confirm the formation of a high density of defects (evidenced by the increase in D peak intensity), which correlated with the formation of C-O bonds found in XPS.
Although XPS results indicated the successful removal of residual photoresist contamination through use of an O₂ plasma, the increase in defectiveness of the exposed graphene suggested that the metal-graphene interface might be degraded. TLM structures were utilized to determine the absolute effect of pre- and post-treatments on the specific contact resistivity, ρc, of the metal-graphene interface, shown in Figure 42.

The use of a lithographic process without surface modification or rapid thermal heat treatment (400°C, 60 – 240 sec, post-metallization) generally resulted in ρc values > 10⁵ Ohm-cm² (Figure 42), indicating a poor interface between the graphene and metal. The high ρc was attributed to remaining photoresist contamination on the surface of the graphene prior to contact metallization.
Figure 42. Comparison of pre- and post-metallization treatments on the specific contact resistance of Ti/Au contacts. Adapted from Ref. [Error! Bookmark not defined.].

Although samples employing a post-metallization rapid thermal processing treatment did show a reduction in $\rho_c$ by up to 7x (120 sec treatment, Fig. 42), the specific contact resistance remained quite high ($>10^{-5}$ Ohm-cm$^2$); indicating that photoresist residue at the metal/graphene interface persisted during rapid thermal post-processing.

Utilization of a low power O$_2$ plasma treatment (“ash”) prior to metal deposition was shown to provide superior contact resistances compared to un-treated or post-processed contacts (Fig. 42) with optimal resistances achieved with use of an O$_2$ plasma treatment lasting 90 seconds ($4x10^{-7}$ Ohm-cm$^2$). Evident from XPS (Fig. 41, left), the use of an O$_2$ plasma resulted in removal of photoresist residue after a 60 sec plasma treatment; however, simultaneously, the graphene peak intensity was severely attenuated and was replaced by a
combination of C-C and C-O bonds. Expectedly, as the etch time was increased to 120 sec
the C-C bonding was further reduced, being replaced by C-O bonds.

Degradation of the graphene exposed to the O₂ plasma was confirmed by Raman
spectroscopy (Fig. 41, right), where the D/G peak ratio indicated a graphene domain size of
~10 nm.⁹² Even under the most benign conditions there was degradation in the structure of
the graphene (evidenced by the increase in D/G ratio); however, ρc continued to improve as
the O₂ plasma treatment time increased from 30 – 90 sec to an average value of 4x10⁻⁷ Ohm-
cm². Upon reaching 120 sec, ρc began increasing again, which was correlated with a severe
degradation in the Raman 2D peak intensity (Fig. 41, right), suggesting that the bulk of the
sp²-bonding expected in graphene had been destroyed. Additionally, an increased fraction of
the chemistry included C-O bonding (Fig. 41, left), suggesting that the formation of
graphene-oxide might have occurred.

Initial evaluation of the “defectiveness” measured by Raman spectroscopy may lead
to the conclusion that the graphene is no longer suitable for device applications; however,
only the graphene that will be covered by the metal contact is exposed to the O₂ plasma and
one should consider that, in all cases, the graphene channel is protected. Post-contact
metallization Hall effect measurements indicated that graphene between the contacts
remained unaffected by the plasma treatment, experiencing no degradation in carrier mobility
compared to graphene test structures utilizing un-treated contacts (utilizing no pre- or post-
processing) or utilizing contacts prepared using a post-metallization thermal treatment with
H₂.
3.1.2 – Effect of Combining Pre- and Post-Processing on Metal-Graphene Interface

For an additional set of EG\textsubscript{Si} samples, pre-process O\textsubscript{2} plasma treatments were combined with post-process thermal treatments at various temperatures. Thermal treatments with H\textsubscript{2} were performed after removal of photoresist residue by low power O\textsubscript{2} plasma etch and contact metallization. Thermal treatments were increased in duration to 15 minutes. Following heat treatment, there was a 1.3 – 5x reduction in specific contact resistance compared to the O\textsubscript{2} plasma treatment alone, as shown in Figure 42. An optimized specific contact resistance of approximately 5x10\textsuperscript{-8} Ohm-cm\textsuperscript{2} was achieved by combining an O\textsubscript{2} plasma pre-treatment with a thermal treatment at 450 – 475 °C.

3.2 – Effect of Choice of Metal on the Metal-Graphene Interface

As discussed in Section 1, theory suggests that the use of contact metallization with a large difference in work function (\(\varphi\)) compared to graphene may result in a charge transfer that leads to doping of the underlying graphene and formation of a dipole at the metal-graphene interface. The charge transfer process leads to an increased density of states in the graphene at the metal-graphene interface and should reduce contact resistance at the metal-graphene interface. To explore this, metal contacts were prepared using a 90 sec O\textsubscript{2} plasma etch pre-treatment prior to deposition of Al (\(\varphi = 4.31\)), Ti (\(\varphi = 4.35\)), Cu (\(\varphi = 4.7\)), Pd (\(\varphi = 5.16\)), Ni (\(\varphi = 5.23\)), or Pt (\(\varphi = 5.64\)) metals.\textsuperscript{103} Graphene exhibits an electron work function of 4.49 eV, resulting in absolute work function differences ranging from -0.2 to 1.2eV, although effective differences may be different due to impurities or the presence of defects at the metal-graphene interface. Such defects might lead to a dramatic change in the difference between the two material’s work functions by altering the graphene metal spacing and the
dipole interaction at the metal-graphene interface.\textsuperscript{41,60,65} Figure 43 shows the resulting average specific contact resistances measured from fifteen TLM structures and plots them as a function of the theoretical ideal work function difference between the metal (first layer) and graphene.

![Graph showing contact resistance vs. work function difference](image)

**Figure 43.** Comparison of specific contact resistance for different composition contact metallizations (using a O\textsubscript{2} plasma pre-treatment). Adapted from Ref. [Error! Bookmark not defined.].

Although \(\Delta \phi\) varied from -0.2 to 1.2eV, little difference in specific contact resistance between metallizations was found. While there was a clear lack of trend with \(\Delta \phi\), it is important to note that the graphene in this work was fundamentally altered through use of O\textsubscript{2} plasma pre-treatment and can no longer be considered “pristine” at the metal-graphene interface. XPS and Raman spectroscopy (Fig. 41) indicated that the graphene was highly defective with a large fraction (> 10%) of C-O bonds. The highly defective nature of the...
graphene and chemical modification at the metal-graphene interface could explain the relatively similar specific contact resistances between metallizations, where process dependent chemisorptions/physisorption differences may lead to a change in the effective work function difference at the metal-graphene interface.\textsuperscript{66}

Finally, it is important to note that the use of some metallizations, even with acceptable specific contact resistance, may not be warranted due to loss of adhesion or highly non-uniform surface coverage. Specific examples of common issues related to the deposition of aluminum and copper on graphene surfaces are illustrated in Figures 44 and 45.

![Figure 44. SEM micrograph of Al/Au contact metallization showing significant delamination. Adapted from Ref. [Error! oomark not defined.].](image)

Figure 44 is an SEM micrograph that shows that the use of aluminum as a first level metallization resulted in severe delamination of the contacts from the graphene surface. The inability of the Al/Au contact metallization to provide sufficient contact to the underlying graphene was evidenced by TLM measurements which revealed exceedingly high and
variable specific contact resistances. This phenomenon was also found to occur in metallization schemes that utilized layers of Pd or Pt with thicknesses greater than 15 nm, although use of Pd or Pt layers <15 nm resulted in no delamination.

Figure 45. AFM micrograph of thin Cu films deposited on graphene showing agglomeration of Cu to the extent that it was not useful in device processing. Adapted from Ref. [Error! Bookmark not defined.].

Figure 45 is an atomic force micrograph of a 5 nm Cu film deposited on graphene that shows an island-like growth morphology for Cu on graphene. Islands exhibited heights as high as 20 nm, suggesting that the utilization of copper as a first layer resulted in highly non-uniform metallization. Such a morphology is unacceptable for device processing, as evidenced by the unacceptably high specific contact resistances listed in Figure 43.

3.3 – Depositing Gate Dielectrics on Graphene

As discussed in Section 1, the dielectric-graphene interface is a critical component of the graphene transistor that has the potential to limit ultimate device performance in the form of degraded transport properties. In this thesis, a novel technique for the deposition of dielectrics on graphene by atomic layer deposition (ALD) was investigated. This technique
utilized direct deposited oxide films as a seed layer for subsequent growth of ALD dielectric overlayers, referred to as O-ALD. This technique differed from previous work which utilized thin metal seeds that were oxidized to form a seed layer for subsequent ALD, referred to as M-ALD, and previous work which utilized low-κ polymer seeds for subsequent ALD.

Compared to other techniques for depositing dielectrics, O-ALD requires no chemical functionalization of the graphene surface, which may alter electronic properties; bypasses the oxidation step of M-ALD techniques, which may degrade carrier mobility;\textsuperscript{79,80} and allows for a high-κ seed layer in intimate contact with the graphene as opposed to techniques utilizing low-κ seeds. It is thought that these differences should allow for minimal impact on carrier transport while simultaneously promoting dielectric screening, though charge traps and/or a high density of fixed oxide charge may still negatively affect transistor performance and charge transport in the underlying graphene.

\textbf{3.3.1 – Dielectric Film Morphology}

Similar to previous work utilizing oxidized metal seeds,\textsuperscript{80} seeding by direct deposited oxide was found to be an effective technique for the nucleation of conformal ALD growth, with AFM showing uniform and complete coverage for films as thin as 10 nm (total thickness including seed layer).
Figure 46. AFM micrographs of O-ALD dielectrics of varying compositions deposited on graphene.

Figure 46 compares AFM micrographs of O-ALD dielectrics of varying compositions deposited on graphene. The micrographs indicate complete and uniform coverage of the graphene surface by the O-ALD deposited films with no pinholes present. Root mean square (RMS) surface roughness for O-ALD dielectrics was found to be 0.84 nm and 1.7 nm for Al$_2$O$_3$/Al$_2$O$_3$ and HfO$_2$/HfO$_2$, respectively, and roughly 2.4 and 3.2 nm for HfO$_2$/Al$_2$O$_3$ and Al$_2$O$_3$/HfO$_2$, respectively, using AFM. Interestingly, O-ALD dielectrics of heterogeneous composition exhibited a significant increase in RMS surface roughness. Additional surface roughness for heterogeneous O-ALD films is undesirable and is anticipated to negatively affect gate leakage uniformity in the GFETs due to dielectric thinning at or around the channel region. It is thought that the additional surface roughness found for heterogeneous
gate stacks could be a result of a rough interfacial region between the EBPVD seed and ALD dielectric. Figure 47 shows TEM cross-sections of O-ALD gate stacks of various seed/dielectric combinations.\textsuperscript{104}

![TEM micrographs show the interface between oxide seed and ALD dielectric for $\text{Al}_2\text{O}_3/\text{Al}_2\text{O}_3$ (d), $\text{HfO}_2/\text{Al}_2\text{O}_3$ (e), $\text{Al}_2\text{O}_3/\text{HfO}_2$ (f), and $\text{HfO}_2/\text{HfO}_2$ (g) gate stacks, where the heterogeneous O-ALD films (e) and (f) produced a particularly rough interfacial region. The scale bar is 3 nm in length. Adapted from Ref. [104].}]

Although Figures 47a and 47d lack the contrast to discern any interfacial region between the seed and dielectric overlayer, Figures 47b and 47c illustrate a rough interfacial region at the seed-dielectric overlayer interface. The significant reduction in RMS surface roughness for homogeneous gate stacks coupled with the presence of a rough interfacial region for heterogeneous dielectrics as discerned by TEM indicated that the heterogeneous
interface was likely a significant source of roughness in the O-ALD deposited dielectrics. Any increase in interfacial roughness near the graphene channel is undesirable in that it may lead to increased interface roughness scattering of carriers in the channel.

Additionally, Figure 47a shows the EG\textsubscript{Si}-dielectric interface and indicated that O-ALD processing did not significantly alter the structure of the underlying graphene. The lack of structural degradation with use of O-ALD dielectrics was supported by Raman analysis of graphene before and after deposition of O-ALD dielectrics (Fig. 48). Figure 48 shows G and D peaks of the EG\textsubscript{Si} before and after deposition of O-ALD dielectric.

![Figure 48. Averaged Raman spectra for O-ALD gate dielectrics show that seed layers did not degrade the underlying graphene structurally. Adapted from Ref. [104].](image-url)
The plotted spectra were averaged over several hundred locations across the samples, after which each spectra was normalized to achieve an equivalent intensity G peak. The low D/G ratio for the as-grown sample indicated high crystalline quality of the epitaxial graphene. Additionally, the lack of any significant change in the D/G ratio with deposition of dielectric by O-ALD (Fig. 48) indicated that the O-ALD deposition technique did not significantly alter the structure of the underlying graphene. Similar results were found for both metal seeded\textsuperscript{80} and EBPVD dielectrics that underwent Raman analysis. Although an increase in D/G peak ratio was not found for O-ALD or EBPVD dielectrics in this work or most M-ALD dielectrics in previous work (Ref. [80]), it should be noted that M-ALD dielectrics using a tantalum metal seed did produce a large change in the D/G peak ratio. This change was attributed to the large change in unit cell volume with oxidation and was confirmed through TEM to have a highly destructive effect on the underlying graphene.

3.3.2 – Effect of Dielectric Overlayers on Carrier Transport

Hall effect measurements were used to evaluate the effect of seed layer and dielectric overlayer on carrier transport within the graphene by measuring carrier density and Hall mobility before and after deposition of the dielectric overlayer. Dielectric overlayers were found to affect Hall mobility ($\mu_{\text{Hall}}$) as well as carrier concentration ($n_s$), as shown in Figure 49. As-grown samples (black symbols) exhibited $\mu_{\text{Hall}}$ of 700 – 1100 cm$^2$/V·s and $n_s$ of 5 – 8x10$^{12}$ cm$^{-2}$ (n-type), typical of Si-face EG.\textsuperscript{105,106} The overall variation in as-grown carrier concentration and Hall mobility found between samples indicated the challenge of obtaining uniform doping across multiple samples, although samples prepared in a single run often showed little variation.
From Figure 49, we see that as-grown samples appeared to follow a \( \mu_{\text{Hall}} \propto n_s^{-1} \) trend (black dashed line), where samples that were more heavily doped (n-type) were found to have reduced mobility. Such a trend has been previously reported for Si-face EG,\(^{105}\) although it was unclear from the un-gated measurements whether this trend was due only to a change in carrier concentration or also a change in sample quality. In order to determine the actual \( \mu_{\text{Hall}} \) dependency on \( n_s \), gated Hall effect measurements were performed on samples utilizing O-ALD deposited dielectric films. These samples utilized a duplicate process to
seed the dielectric overlayers, but increased the thickness of the ALD deposited overlayer from 8 to 18 nm to ensure complete coverage for the large Van der Pauw structures (25 μm²). The gated Hall effect measurements of O-ALD coated samples (Fig. 50) revealed a $\mu_{\text{Hall}} \propto n_s^{-X}$ dependency, where $X$ ranged from 0.5 - 0.26 (Al₂O₃ seeded samples) to 0.27 – 0.15 (HfO₂ seeded samples).

![Graph](image)

**Figure 50.** Gated Hall effect measurements revealed a dependency for $\mu_{\text{Hall}}$ and gate modulated carrier concentration, $n_s$, where $\mu_{\text{Hall}} \propto n_s^{-X}$ and $X$ ranged from ~0.2 - 0.3. Adapted from Ref. [104].

The gated Hall effect measurements were a direct measure $n_s$ and its effect on $\mu_{\text{Hall}}$ and, although it is unclear at this time if as-grown dielectrics would follow a similar $\mu_{\text{Hall}} \propto n_s^{-X}$ dependency as O-ALD coated samples, both measured and observed dependencies showed that an increases in $n_s$ after deposition of dielectric should lead to a subsequent
decrease in $\mu_{\text{Hall}}$, unless deposited dielectrics also acted to modify the scattering physics for charge carriers within the graphene.

In this thesis all dielectrics were found to cause an increase in $n_s$. This phenomenon was likely due to the presence of oxygen vacancies or other charged defect complexes which doped the graphene through a charge transfer process.\textsuperscript{79,107} Although all dielectrics caused an increase in $n_s$ not all dielectrics subsequently caused a decrease in $\mu_{\text{Hall}}$. Figure 49 shows that high-$\kappa$ seeded dielectrics deposited by EBPVD (orange and blue circles) and by O-ALD (filled and half-filled red and blue squares) caused both an increase in $\mu_{\text{Hall}}$ \textit{and} an increase in $n_s$. Conversely, low-$\kappa$ seeded dielectrics deposited by O-ALD (SiO$_2$/HfO$_2$; half-filled green squares) led to decreased $\mu_{\text{Hall}}$ with increased $n_s$.

Comparing the high-$\kappa$ and low-$\kappa$ seeded dielectrics, the high-$\kappa$ seeds, in effect, simply acted to shift the $\mu_{\text{Hall}} \propto n_s^{-X}$ dependency upwards from and in parallel with the low-$\kappa$ dependency, similar to the case of high-$\kappa$ solvents on exfoliated graphene.\textsuperscript{83} The increase of $\mu_{\text{Hall}}$ with deposition of high-$\kappa$ was attributed to dielectric screening,\textsuperscript{81–85} signifying a reduction in scattering by remote charged impurities, and represented the first time such an increase has been observed using conventional deposition techniques on EG. Compared to previous work using M-ALD, it is thought that the use of direct deposited oxide seed in O-ALD deposited films helps to preserve transport properties in the EG in order that dielectric screening is not masked by a degradation of mobility.

Assuming the measured $\mu_{\text{Hall}} \propto n_s^{-X}$ power dependencies of the O-ALD coated samples were also valid for as-grown samples, one can make a rough estimation of the change in $\mu_{\text{Hall}}$ with deposition of dielectric. This is achieved by fitting the measured average dependency to each individual pair of $\mu_{\text{Hall}}$ and $n_s$ data points. The change in $\mu_{\text{Hall}}$ could then be estimated by calculating the percent change between as-grown and post-dielectric $\mu_{\text{Hall}}$ at
some fixed $n_s$. The change in $\mu_{Hall}$ per VdP structure could then be average for all structures utilizing the same dielectric stack. Using this technique, it was found that hafnia seeded O-ALD dielectrics produced an average increase in Hall mobility of 73 - 57%, alumina seeded O-ALD dielectrics produced an average increase of 52 - 43%, and EBPVD dielectrics produced an average increase of ~15% regardless of composition. Importantly, the estimated increase in $\mu_{Hall}$ produced by O-ALD dielectrics with heterogeneous seed/dielectric structure ($\text{HfO}_2/\text{Al}_2\text{O}_3$, $\text{Al}_2\text{O}_3/\text{HfO}_2$) was roughly 20% smaller than that produced by homogeneous O-ALD structures ($\text{HfO}_2/\text{HfO}_2$, $\text{Al}_2\text{O}_3/\text{Al}_2\text{O}_3$), which may be indicative of increased surface roughness scattering. Figure 51 schematically represents the calculation technique used to estimate percent increase in $\mu_{Hall}$. 
The estimated changes in mobility for O-ALD dielectrics were slightly lower than those predicted by theory. In Ref. [83], the suppression factor, $S$, is a result of application of the Born approximation while modeling the scattering potential for a Coulombic scatterer. $S$ is dependent on the effective relative permittivity, $\varepsilon = (\kappa_s + \kappa)/2$, where $\kappa_s$ and $\kappa$ are the dielectric constants of the substrate and a dielectric coating of at least a few nanometers, respectively. Adapting the effective relative permittivity equation to Al$_2$O$_3$/Al$_2$O$_3$ ($\varepsilon_r \sim 7$, from capacitance measurements) and HfO$_2$/HfO$_2$ ($\varepsilon_r \sim 16$, from capacitance measurements)
on a SiC substrate ($\varepsilon_r \sim 10$; 6H polymorph\textsuperscript{22}) and solving for the suppression factor should result in ~1.6x and ~2.5x increases in $\mu_{\text{Hall}}$, respectively.

EBPVD-only dielectrics exhibited a reduced improvement in $\mu_{\text{Hall}}$ relative to O-ALD dielectrics (~15% as compared to 50 – 65%). This reduced improvement could be the result of a higher intrinsic defect concentration in these films relative to the O-ALD films leading to increased remote charged impurity scattering. The presence of a large concentration of charged defects in the EBPVD films was supported by thickness dependent measurements of $n_s$ that suggested increased defect concentration with continued use of the EBPVD technique. Figure 52 plots fractional change in Hall mobility versus fractional change in carrier density ($\mu_{\text{Hall}}/\mu_0$ versus $n_s/n_0$ where $\mu_0$ and $n_0$ are the as-grown $\mu_{\text{Hall}}$ and $n_s$) for EBPVD HfO$_2$ samples of varying thickness.

![Normalized Hall effect data ($\mu_{\text{Hall}}/\mu_0$ and $n_s/n_0$ where $\mu_0$ and $n_0$ are as-grown Hall mobility and carrier concentration, respectively). Adapted from Ref. [104].](image)

Figure 52.
For 5 nm thick EBPVD HfO$_2$ films, a small increase in $n_s$ from as-grown of 10% was found which increased to 40% for 10 nm thick films (Fig. 52). The increase in $n_s$ was also accompanied by an expected decrease in $\mu_{Hall}$ (also shown in Fig. 49). Fallahazad et al showed a similar dependence on dielectric thickness for M-ALD dielectrics on exfoliated graphene,$^{79}$ where a decrease in mobility was reported that was attributed to an increase in the charged impurity concentration with increasing thickness due to a charge transfer process between the graphene and oxygen vacancies within the dielectric. While no mobility decrease was found for EBPVD deposited dielectrics of different thicknesses in this work, it is thought that a similar charge transfer process was responsible for the thickness dependence of $n_s$ and might be indicative of a large defect concentration in these films. The lack of mobility degradation with thickness for the EBPVD dielectrics in this work was likely due to the lower intrinsic mobility of the EG system ($\mu \sim 1000$) as compared to the exfoliated graphene on SiO$_2$ studied by Fallahazad et al ($\mu \sim 10000$), or due to a higher defect concentration in M-ALD dielectrics relative to EBPVD.

3.4 – DC Performance of Graphene FETs

Hall effect measurements for O-ALD and EBPVD dielectrics clearly indicated that successful integration of a top-gate dielectric is possible without disrupting the transport properties of EG and that proper choice and deposition of dielectrics are critical in optimizing the performance of top-gate dielectrics on EG. However, in addition to optimizing the effect of the overlayer on transport properties, the choice of material and deposition technique must produce top-gates that satisfy the main functions of a gate dielectric, which are to sufficiently
isolate the channel from the gate and to capacitively couple the gate to the channel. An investigation of the DC performance of the GFETs utilizing O-ALD and EBPVD gate dielectrics was performed in order to compare the two techniques and the various gate compositions for use in graphene based transistors.

3.4.1 – Effect of Dielectric on Leakage and Gate Modulation of Carriers

While the majority of the O-ALD gate stacks averaged $5 \times 10^{-12} - 8 \times 10^{-12}$ A/µm$^2$, leakage currents for O-ALD HfO$_2$/Al$_2$O$_3$ gates exhibited significant variability, ranging from $2 \times 10^{-11}$ to $7 \times 10^{-7}$ A/µm$^2$ ($V_{gs}$=3V) for different dimension GFETs with different degrees of gate overlap. The variability in gate leakage for HfO$_2$/Al$_2$O$_3$ gated GFETs was attributed to a high RMS roughness relative to others. The small amount of gate leakage current for the majority of O-ALD gated GFETs confirmed oxide seeding as a robust functionalization technique ensuring uniform coverage of ALD dielectrics. Most gate stacks exhibited hard breakdown at fields ranging between 4 – 9 MV/cm and with little correlation to composition or deposition technique. For breakdown at this field strength, B-mode failure was expected$^{108}$ and suggested the presence of dielectric thinning, confirming AFM results indicating thickness variability on the order of ±2 nm. Table 5 summarizes the gate leakage through the deposited dielectrics, where a range of $I_{leak}$ is presented representing the average gate leakage through over 100 GFETs of various device dimensions.
Table 5. Summary of gate leakage through gate dielectrics deposited by various techniques and exhibiting various compositions

<table>
<thead>
<tr>
<th>deposition technique</th>
<th>seed / dielectric combination</th>
<th>$I_{\text{leak}} @ V_{gs}=3\text{V}$ (A/μm²)</th>
</tr>
</thead>
<tbody>
<tr>
<td>O-ALD</td>
<td>HfO₂ / HfO₂</td>
<td>5.6x10⁻¹² - 8.4x10⁻¹²</td>
</tr>
<tr>
<td>O-ALD</td>
<td>HfO₂ / Al₂O₃</td>
<td>1.7x10⁻¹¹ - 6.7x10⁻⁷</td>
</tr>
<tr>
<td>O-ALD</td>
<td>Al₂O₃ / Al₂O₃</td>
<td>4.4x10⁻¹² - 7.3x10⁻¹²</td>
</tr>
<tr>
<td>O-ALD</td>
<td>Al₂O₃ / HfO₂</td>
<td>5.8x10⁻¹² - 8.8x10⁻¹²</td>
</tr>
</tbody>
</table>

Besides isolating the channel from the gate metallization, the gate dielectric must also act to capacitively couple the gate contact to the channel so that the carrier concentration in the channel can be modulated be effectively modulated. Table 6 summarizes the ability of the investigated dielectrics to perform this task, showing $C_{ox} / q$, $\beta$, and $n_0$, where $\beta$ is defined from $n_s \equiv \beta \cdot V_{gs} + n_0$ with $n_s$ as the carrier density in the channel, $V_{gs}$ as the applied gate bias, and $n_0$ as the carrier density at zero-bias conditions. In this way, $\beta$ is a measure of the number of carriers that are modulated by an applied gate voltage. Ideally, $C_{ox} / q$ and $\beta$ should be equivalent, although the effects of quantum capacitance, traps, and non-idealities all contribute to degrade $\beta$ from its ideal value. $\beta$ was extracted from gated Hall effect measurements at room temperature in ambient conditions (Fig. 50).

Table 6. Carrier modulation for O-ALD gates of varying seed/overlayer combination

<table>
<thead>
<tr>
<th>seed / dielectric combination</th>
<th>$C_{ox} / q$ ($e^/-Vx10^{12}$)</th>
<th>$\beta$ ($e^/-V \times 10^{12}$)</th>
<th>$n_0$ ($e^/-cm^2$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>HfO₂ / HfO₂</td>
<td>7.5</td>
<td>2.12</td>
<td>5.5x10¹²</td>
</tr>
<tr>
<td>HfO₂ / Al₂O₃</td>
<td>6.3</td>
<td>1.43</td>
<td>5.6x10¹²</td>
</tr>
<tr>
<td>Al₂O₃ / Al₂O₃</td>
<td>5.0</td>
<td>1.57</td>
<td>7.2x10¹²</td>
</tr>
<tr>
<td>Al₂O₃ / HfO₂</td>
<td>5.6</td>
<td>2.27</td>
<td>8.2x10¹²</td>
</tr>
</tbody>
</table>
Comparing the $C_{ox} / q$ and $\beta$ values listed in Table 6, it is clear that the measured dependency of $n_s$ on $V_{gs}$ was significantly less than that anticipated by measurements of $C_{ox}$. This discrepancy was attributed to a significant density of traps within the as-deposited gate dielectrics due to the fact that quantum capacitance effects are anticipated to be small at such high carrier concentrations (away from the low DOS at the Dirac point).

3.4.2 – Effect of Dielectric on Direct Current Measurements of GFETs

Direct current (DC) measurement of GFETs utilizing O-ALD and EBPVD gate dielectrics were compared, confirming the benefits of high-$\kappa$ EBPVD and O-ALD as techniques for optimizing GFET performance. Figure 5 plots the transfer curves ($I_{ds}$-$V_{gs}$ sweeps) of four different GFETs that utilized various different gate dielectrics. In the figure, the high drive current and large modulation of the GFETs utilizing high-$\kappa$ EBPVD and O-ALD dielectrics are contrasted with the low drive current and small modulation of the GFET utilizing a low-$\kappa$ O-ALD dielectric.
As can be seen in Fig. 53, the combined effects of doping by the both the SiC substrate and the deposited gate dielectrics resulted in GFETs that were heavily doped n-type. The doping was so severe as to cause the NP to be inaccessible for most devices in this thesis, even with extreme biasing of the device, which caused significant dielectric breakdown and degraded performance of the GFETs.

Due to process variability and scatter in the results, peak transconductance ($g_{m,\text{max}}$) and peak drive current, $I_{ds}$ ($I_{ds} @ V_{gs}=3V, V_{ds}=1V$) were extracted from $I_{ds}$-$V_{gs}$ sweeps for more than 500 devices utilizing various gate dielectrics and these extracted values were plotted (Fig. 54).
Figure 54. Plot of peak transconductance versus peak drive current for GFETs utilizing gate dielectrics deposited by EBPVD and O-ALD techniques. Adapted from Ref. [104].

The plot of peak transconductance versus peak drive current is sectioned into three regions by black dotted lines (Fig. 54). The left-most region represents the poorest performing devices while the right-most region represents the best performing devices. GFETs utilizing low-κ SiO₂ seeded O-ALD gates (Fig. 52; left-most section) exhibited average \( I_{dss} < 50 \, \mu\text{A}/\mu\text{m} \) and average \( g_{m,max} < 10 \, \mu\text{S}/\mu\text{m} \) and represented the lowest performance GFETs in this work. Low \( I_{dss} \) and \( g_{m,max} \) for SiO₂ seeded O-ALD was attributed to reduced mobility and increased \( n_s \) relative to high-κ seeded gates (Fig. 49). Additionally, high contact resistances (\( R_c \)) were found for this sample, where the oxygen plasma pre-treatment was omitted. For all other samples, the use of plasma pre-treatment reduced \( R_c \) to less than 200 Ω-μm, making contact resistance negligible under depletion conditions and
roughly 20% of the total resistance under accumulation. For the case of SiO$_2$ seeded GFETs, it is anticipated that reduction of $R_c$ should lead to a shift in the average $I_{dss}$ and $g_{m,max}$ closer to 100 $\mu$A/$\mu$m and 20 $\mu$S/$\mu$m in accord with the highest performing SiO$_2$ seeded GFETs. On the other hand, GFETs utilizing high-$\kappa$ EBPVD or high-$\kappa$ seeded heterogeneous O-ALD gates (Fig. 54; middle section) showed a 3-4x increase in $I_{dss}$ to 340 – 440 $\mu$A/$\mu$m and $g_{m,max}$ to 40 – 70 $\mu$S/$\mu$m, with 5 nm EBPVD HfO$_2$ gated GFETS displaying $g_{m,max}$ up to 140 $\mu$S/$\mu$m. Homogeneous O-ALD gated GFETs (Fig. 54; right-most section) exhibited exceptional FET characteristics with average $I_{dss}$ = 550 – 780 $\mu$A/$\mu$m and average $g_{m,max}$ = 66 – 134 $\mu$S/$\mu$m depending on gate composition. Of the homogeneous O-ALD gated GFETs, HfO$_2$/HfO$_2$ GFETs were found to be superior to all others with $I_{dss}$ up to 971 $\mu$A/$\mu$m and $g_{m,max}$ up to 175 $\mu$S/$\mu$m. The increase in performance for GFETs utilizing high-$\kappa$ EBPVD and high-$\kappa$ O-ALD dielectrics was attributed to a reduction of remote charged impurity scattering through dielectric screening, leading to increased carrier mobility. The superior performance of homogeneous O-ALD gated GFETs relative to heterogeneous O-ALD was attributed to removal of the seed/overlayer interface which was thought to negatively affect carrier transport in the channel through increased interface roughness scattering.

Transfer curve hysteresis in O-ALD GFETs ranged from 0.5 – 0.7 V with no statistically significant trending according to gate composition. Additionally, we found an increase in hysteresis for EBPVD gates to 1V, which was in agreement with a higher density of charge traps for EBPVD dielectrics relative to O-ALD. The passivation or reduction of these traps by thermal processing or optimized reactive depositions is anticipated to significantly reduce hysteresis.

Additionally, we note that Al$_2$O$_3$ seeded O-ALD dielectrics led to reduced $g_{m,max}$ relative to HfO$_2$ seeds at a given $I_{dss}$. This was attributed to a difference in the NP between
the HfO$_2$ and Al$_2$O$_3$ coated samples, where a change in the intrinsic $n_s$ at zero-bias conditions (Table 6) leads to a shift in the NP. For Figure 54, $g_{m,max}$ and $I_{dss}$ are both dependent on the gate capacitance ($C_{ox}$), $\mu_{eff}$, and carrier density according to $g_{m,max} = \mu_{eff}C_{ox}V_{ds}$ and $g_{m,max} = \mu_{eff}C_{ox}(V_{gs} - V_{NP})V_{ds}$, respectively. Therefore, $\frac{\partial g_{m,max}}{\partial I_{dss}}$, the slope of the regression plotted in Fig. 54 is related to $(V_{gs} - V_{NP})^{-1}$ if and only if $g_{m,max}$ and $I_{dss}$ occur at equivalent bias conditions. Although $g_{m,max}$ and $I_{dss}$ generally refer to different points on the transfer curve, the overall similarity between transfer curves leads to a constant relationship between $g_{m,max}$ and $I_{dss}$ for the different O-ALD GFETs. This relationship means that, approximately, $\frac{\partial g_{m,max}}{\partial I_{dss}} \approx (V_{gs} - V_{NP})^{-1}$. Therefore, the change in slope between Al$_2$O$_3$ and HfO$_2$ seeded regressions in Figure 54 can be explained by the fact that the Al$_2$O$_3$ seeded gates are displaced farther from the NP than the HfO$_2$ seeded gates under the same bias conditions (Table 6, $n_0$). The EBPVD GFETs, which are shown to have the smallest zero-bias condition $n_s$ after deposition of gate (Fig. 49), also show the steepest slope (smallest magnitude $|V_{gs} - V_{NP}|$).

### 3.4.3 – Effect of Heterogeneous O-ALD Dielectrics on DC GFET Performance

The difference in performance between homogeneous and heterogeneous high-$\kappa$ seeded O-ALD gated FETs highlighted in Figure 52 and in estimation of change in $\mu_{Hall}$ (Fig. 51) illustrates a key consideration for gate dielectric implementation: the effect of seed/overlayer interface on carrier transport. Figure 55 compares the homogeneous and heterogeneous high-$\kappa$ seeded O-ALD gated GFETs, showing representative transfer curves for O-ALD gated GFETs of varying seed/overlayer composition.
Figure 55. Transfer curves of four representative GFETs utilizing high-$\kappa$ O-ALD gates illustrating increased $I_{ds}$ and $g_{m,max}$ for GFETs utilizing homogeneous gate stacks. Adapted from Ref. [104].

Evident from Figure 55, heterogeneous gate dielectrics led to a decrease in $I_{ds}$ of more than 30% compared to homogeneous gate dielectrics using the same seed material. The absolute difference in average (post-dielectric) $\mu_{Holl}$ and $n_s$ between samples with the same oxide seed was $< 4\%$ (Fig. 49) and does not provide sufficient explanation for the differences found in $I_{ds}$.

Alternatively, the effective mobility ($\mu_{eff}$) of the GFETs can be extracted using a simple charge control model: $J_{ds} = \mu_{eff} \frac{c_{ox}}{A} (V_{gs} - V_{NP}) V_{ds}$, where $J_{ds}$, is drain current normalized by width, $\frac{c_{ox}}{A}$ is the gate capacitance normalized by area, $V_{gs}$ is the applied gate bias, $V_{NP}$ is the neutrality point (NP), and $V_{ds}$ is the driving voltage.\textsuperscript{63} In this work, the charge
control model was modified to become \( J_{ds} = \mu_{eff}(\beta \cdot V_{gs} + n_0)V_{ds} \), where \( n_0 \) is the measured intrinsic \( n_s \) at zero-bias conditions (Table 6, \( n_0 \)) and \( \beta \) relates the charge carrier density to the applied gate bias (Table 6, \( \beta \)) and is extracted from gated Hall effect measurements at room temperature in ambient conditions. The modified model alleviates the \( V_{NP} \) constraint by directly sampling the carrier concentration at zero-bias conditions and uses gated Hall effect measurements in place of \( C_{ox} \) to make a more accurate estimation of carrier density in the channel in the presence of a large number of traps and any quantum capacitance effects. The model does not address contact resistance, although \( R_c \) was found to be uniform between the high-\( \kappa \) seeded O-ALD samples. Figure 56 plots \( \mu_{eff} \) as a function of \( n_s \) and provides evidence that the degraded performance of heterogeneous dielectric GFETs was the result of an approximate 40 – 30\% degradation in \( \mu_{eff} \) compared to homogeneous gate stacks.
Figure 56. Extracted $\mu_{eff}$ plotted as a function of $n_s$ confirms a degradation in $\mu_{eff}$ of 30 – 40% for GFETs with heterogeneous O-ALD gate dielectrics. Adapted from Ref. [104].

Although Hall effect measurements show little change between heterogeneous and homogeneous O-ALD dielectrics, it is speculated that interface roughness scattering had a greater impact on GFET measurements and only minimally impacted Hall effect measurements. The strong dependency of interface roughness scattering on carrier energy, yet weak dependency of remote charged impurity scattering on carrier energy help to explain why the overall contributions of these two scattering processes could change significantly between Hall effect and DC FET characterization at high drain biases. Therefore, the degradation of $\mu_{eff}$ for heterogeneous O-ALD dielectrics was attributed to surface roughness scattering, although further work to model the scattering physics for this
system is necessary in order to develop a complete understanding of how the heterogeneous gate dielectric interface impacts transport in GFETs.

3.5 – Small Signal Performance of Graphene FETs

Extrinsic $H_{21}$ was extracted from high-$\kappa$ O-ALD gated GFETs with gate dimensions $W=10\ \mu m$ and $L=1\ \mu m$. More than 5 GFETs were characterized for each of the four different gate stacks (HfO$_2$/HfO$_2$, HfO$_2$/Al$_2$O$_3$, Al$_2$O$_3$/Al$_2$O$_3$, and Al$_2$O$_3$/HfO$_2$). Extrinsic current gain was extracted for each GFET for $V_{ds}=1$, 2, and 3V while $V_{gs}$ was swept from -3 to -2V (5 points). $H_{21}$ is plotted for representative devices under these bias conditions in Figures 57, 58, 59, and 60.

![Figure 57. $H_{21}$ extracted from S-parameters of a HfO$_2$/HfO$_2$ O-ALD gated GFET at various bias conditions.](image-url)
Figure 58. $H_{21}$ extracted from S-parameters of a HfO$_2$/Al$_2$O$_3$ O-ALD gated GFET at various bias conditions.

Figure 59. $H_{21}$ extracted from S-parameters of a Al$_2$O$_3$/Al$_2$O$_3$ O-ALD gated GFET at various bias conditions.
Figure 60. $H_{21}$ extracted from S-parameters of a Al$_2$O$_3$/HfO$_2$ O-ALD gated GFET at various bias conditions.

Figure 61 summarizes the small signal results. In this figure, both the average maximum and average minimum extracted $f_T$ is plotted as a function of $V_{ds}$ for the high-$\kappa$ O-ALD gated GFETs utilizing the four different gate stack combinations. A unique curve fill is then applied between the maximum and minimum curves.
Extrinsic small signal current gain cutoff frequency \( (f_T) \) was found to increase with increasing drive voltage for all combinations of O-ALD dielectric. The increase in \( f_T \) was found to be approximately linear with \( V_{ds} \), showing an approximate 2x increase in \( f_T \) as \( V_{ds} \) was increased from -1 to -3 V. Similar to DC performance of GFETs, the presence of a seed/overlayer interface was found to negatively impact \( f_T \), where GFETs utilizing homogeneous O-ALD gate dielectrics exhibited \( f_T \) that was enhanced by 10 – 70%. Figure 62 plots the increase in maximum and minimum \( f_T \) as a function of \( V_{ds} \) for the GFETs utilizing HfO\(_2\) and Al\(_2\)O\(_3\) seeded O-ALD gate dielectrics.
Although use of homogeneous gate dielectric was found to increase both maximum and minimum $f_T$ for all investigated bias conditions, Figure 62 shows that the percent increase in $f_T$ degraded as $V_{ds}$ was increased from -1 to -3V. Regardless, homogeneous gate stacks outperformed heterogeneous gate stacks and demonstrate *extrinsic* $f_T > 2$ GHz at $V_{ds} = 1$V and up to 5.8 GHz at $V_{ds} = 3$V. Figure 63 plots $|H_{21}|$ as a function of frequency for representative O-ALD gated GFETs biased close to peak transconductance.
Based on DC performance of the O-ALD gated GFETs, the extrinsic RF performance of homogeneous HfO$_2$/HfO$_2$ gated GFETs was expected to surpass all others; however, the results indicated similar performance for both HfO$_2$/HfO$_2$ and Al$_2$O$_3$/Al$_2$O$_3$ seeded GFETs, with the highest recorded $f_T$ demonstrated using an Al$_2$O$_3$/Al$_2$O$_3$ gated device. The similar performance between the homogeneous gated was likely the result of device processing variation between samples. Although measured $f_T$ should ideally be a measure of mobility, extrinsic GFET measurements may deviate from direct measurement as a result of parasitic capacitances and resistances, which may vary due to processing variation. None-the-less, Figure 63 clearly shows that the presence of a heterogeneous dielectric in GFETs can significantly degrade RF performance.
Chapter Four: Conclusions

In this thesis, materials integration of metals and dielectrics with epitaxial graphene was investigated. Various contact metals, pre-treatments, and post-treatments were compared and a reproducible, robust process for producing low specific contact resistivity metal contacts to epitaxial graphene was developed. Similarly, various gate dielectrics and methods of deposition were investigated and a reproducible, robust technique for the deposition of thin, high-k gate dielectrics on epitaxial graphene was developed. Importantly, this method not only produces uniform, conformal, and robust gate dielectrics, but also leads to an improvement in the transport properties of the underlying graphene, which was attributed to dielectric screening and a reduction in remote charged impurity scattering. Finally, the combination of optimized contacts and high-k gate dielectrics on epitaxial graphene has allowed for the demonstration of high performance GFETs with excellent peak drive currents, peak transconductances, and extrinsic current gain cutoff frequencies.

4.1 – Contacts

Through process optimization, we have demonstrated that the combination of a “gentle” O₂ plasma etch and subsequent heat treatment can result in superior contact resistance values, which are necessary for high speed micro- and nano-electronic technologies based on graphene. XPS was utilized to show that the use of an O₂ plasma resulted in removal of photoresist residue, but that, simultaneously, the graphene peak intensity was severely attenuated and was replaced by a combination of C-C and C-O bonds after use of O₂ plasma. The degradation of the graphene exposed to O₂ plasma was
confirmed by Raman spectroscopy; however, \( \rho_c \) was shown to increase despite damage to the graphene to an average value of \( 4 \times 10^{-7} \text{Ohm-cm}^2 \text{O}_2 \) plasmas lasting 30 – 90 sec.

Although we found little difference in specific contact resistance by varying the ideal metal/graphene work function difference, the severely altered graphene structure and chemistry prior to metallization complicates comparison to ideal models of the metal-graphene interface.

### 4.2 – Gate Dielectrics

Several factors have been considered for integrating dielectrics with EG for device applications including the importance of choice of seed layer on FET performance and dielectric screening, as well as the effect of seed/dielectric interfaces on FET performance.

AFM was used to indicate complete and uniform coverage of the graphene surface by EBPVD and O-ALD deposited films, although RMS surface roughness was shown to be on the order of 1 – 2 nm. Raman spectroscopy and TEM micrographs were used to show that O-ALD deposited films introduced minimal structural damage to the EG.

Hall effect measurements were utilized to show an improvement in \( \mu_{\text{Hall}} \) with deposition of high-\( \kappa \) EBPVD and O-ALD dielectrics despite an increase in \( n_s \), which was attributed to dielectric screening and a reduction in remote impurity scattering. The percent increase in Hall mobility was estimated by assuming a \( \mu_{\text{Hall}} \propto n_s^{-X} \) dependency, where \( X \) ranged from 0.5 - 0.15 and was extracted from gated Hall measurements in atmosphere of VdP Hall structures gated with O-ALD dielectrics. With the assumed dependency, mobility improvement was found to be 73 - 57% for hafnia seeded O-ALD dielectrics, 52 - 43% for alumina seeded O-ALD dielectrics, and ~15% for EBPVD dielectrics regardless of composition. The increase in \( \mu_{\text{Hall}} \) produced by O-ALD dielectrics with heterogeneous
seed/dielectric structure (HfO$_2$/Al$_2$O$_3$, Al$_2$O$_3$/HfO$_2$) was roughly 20% smaller than that produced by homogeneous O-ALD structures.

The reduced improvement in $\mu_{Holl}$ for EBPVD-only dielectrics relative to O-ALD dielectrics was attributed to a higher intrinsic defect concentration in these films relative to the O-ALD films leading to increased remote charged impurity scattering. The presence of a large concentration of charged defects in the EBPVD films was supported by thickness dependent measurements of $n_s$ that suggested increased defect concentration with continued use of the EBPVD technique.

### 4.3 – DC Performance

GFET performance was characterized using $I_{ds}$-$V_{gs}$ sweeps and extracting several parameters of interest, including peak drive current, peak transconductance, and maximum leakage current.

Gate leakage currents averaging $5 \times 10^{-12} - 8 \times 10^{-12}$ A/$\mu$m$^2$ for the majority of O-ALD gated GFETs confirmed oxide seeding as a robust functionalization technique ensuring uniform coverage of ALD dielectrics. Hard breakdown ranging between 4 – 9 MV/cm was found for the EBPVD and O-ALD gate dielectrics with little correlation to composition or deposition technique, suggesting the presence of dielectric thinning and confirming AFM results indicating thickness variability on the order of ±2 nm.

GFETs utilizing high-κ EBPVD and high-κ seeded O-ALD gates were demonstrated and showed dramatically improved performance relative to GFETs utilizing low-κ seeded O-ALD gates, attributed to dielectric screening. GFETs were demonstrated with drive currents and transconductances up to 971 $\mu$A/$\mu$m and 235 $\mu$S/$\mu$m using a wafer scale growth
technique, where the excellent performance of high-κ seeded O-ALD gated GFETs was attributed to the combination of low resistance contacts and enhanced transport through dielectric screening. Additionally, DC performance of heterogeneous O-ALD gated GFETs was shown to be degraded roughly 30 – 40% from homogeneous O-ALD gated GFETs.

Electrical characterization of GFETs using a charge control model was used to extract $\mu_{\text{eff}}$, showing the degradation of effective mobility in the presence of a heterogeneous gate stack. The degradation of effective mobility for heterogeneous gate stacks was attributed to increased surface roughness scattering.

4.4 – Small Signal Performance

Small signal performance of O-ALD gated GFETs was characterized by extracting the small signal current gain, $H_{21}$, from the measured extrinsic scattering parameters.

Extrinsic small signal current gain cutoff frequency ($f_T$) was found to increase with increasing drive voltage for all combinations of O-ALD dielectric. The increase in $f_T$ was found to be approximately linear with $V_{ds}$. Similar to DC performance of GFETs, the presence of a seed/overlayer interface was found to negatively impact $f_T$, where GFETs utilizing homogeneous O-ALD gate dielectrics exhibited $f_T$ that was enhanced by 10 – 70%.

Although DC characterization and Hall effect measurements suggested that homogeneous HfO$_2$ O-ALD gated GFETs should demonstrate the highest small signal performance, this was not the case. Instead, both HfO$_2$ and Al$_2$O$_3$ gated homogeneous O-ALD GFETs showed similar performance, which was attributed to process variation during device fabrication and the effects of parasitics on the extrinsic RF device performance.
Chapter Five: Future Work

Only a few years after the first reported graphene FET researchers have been able to successfully incorporate them in low-noise amplifiers, frequency mixers, and frequency multipliers. The rapid advance of graphene technology in only a few short years is a testament to its phenomenal intrinsic properties and its potential as an electronic material for use in advanced or novel applications. Although it is uncertain at this time whether graphene will ultimately surpass III-V and Si semiconductors in the RF or digital application space, the unique structure and properties of graphene present exciting opportunities in these and other application spaces.

Although graphene transistors in recent years have reached an impressive intrinsic current gain cut-off frequency ($f_T$) of 300 GHz, the extrinsic performance of RF GFETs has lagged behind intrinsic performance. The difference in extrinsic and intrinsic performance of graphene FETs is a direct result of device parasitics. Parasitic resistances in the form of contact resistances or un-gated portions of graphene combine to create high access resistances that degrade RF performance. Additionally, un-optimized device designs might lead to unacceptably high parasitic capacitances. Along with device parasitics, the limited saturation behavior demonstrated by graphene devices and the in-ability to integrate top-dielectrics without degradation of transport properties in the underlying graphene combine to limit the ultimate achievable RF performance of graphene FETs by leading to high $g_d$ and reduced mobility (low $g_m$).

In this thesis, metal-graphene contacts and top-gate dielectrics were investigated as components of the graphene-based FET. Optimized processes for the formation of contacts and deposition of gate dielectrics were developed, yet, in order to push graphene-based technologies forward, metal-graphene contacts and top-gate dielectrics on graphene must
continue to be optimized. Additionally, the weak-saturation of graphene devices, device processing, and short-channel effects in graphene FETs must also be better understood. By working to improve the material properties and utilizing optimized device architectures that minimize parasitics and help to control short-channel effects, GFET RF performance can be developed to its ultimate potential. Whether this will be enough to surpass conventional semiconductors is unknown at this time, but graphene devices cannot be competitive with current semiconductor devices without continued work to optimize and understand.

Following are several key areas of improvement that EG<sub>Si</sub>-based devices must overcome in order to achieve high performance, wafer-scale graphene-based devices.

### 5.1 – Hydrogen Intercalation to Improve Carrier Mobility

Although use of sublimation allows for highly controllable, wafer-scale synthesis of graphene on SiC substrates, the presence of a buffer layer on EG<sub>Si</sub> leads to distortion of the Dirac cone and reduced transport properties relative to pristine exfoliated graphene. In order to continue to advance the performance of epitaxial graphene, the removal, or passivation, of the carbon buffer layer is desirable.

Recently, successful “cleaving” of the buffer layer in EG<sub>Si</sub> was achieved via hydrogen intercalation. This process, which in its simplest form amounts to exposing EG<sub>Si</sub> to molecular hydrogen at elevated temperatures, results in what is referred to as quasi-free standing epitaxial graphene (QF-EG<sub>Si</sub>). The process allows for the passivation of the carbon buffer layer that exists between the EG<sub>Si</sub> and SiC substrate by terminating the SiC surface in H-bonds and converting the buffer layer into a single-layer of graphene. The carrier mobility and transport properties of QF-EG<sub>Si</sub> are increased substantially over non-
hydrogen intercalated EG$_{Si}$ due to its more free-standing nature, confirmed by angle resolved photoemission spectroscopy (ARPES) and Hall effect measurements.

The increase in transport properties found with hydrogen intercalation should lead directly to improved DC and RF GFET performance through increased drive currents, transconductances, and cutoff frequencies. Thus, the incorporation of hydrogen intercalation into the process flow of GFET fabrication should be of paramount importance.

### 5.2 – Reducing Output Conductance

The large output conductance of graphene based devices is a result of weak-saturation behavior. The weak saturation behavior of GFETs is a result of ambipolar conduction which prevents pinch-off in the graphene channel. As the drain bias is increased, the channel is depleted of one type of carrier and inverted to the other type, thus allowing for increased drain current as the drain bias is increased. In order to maximize the RF performance of the graphene-based FET, the large output conductance of the GFET must be reduced. Initially, there are two ways to go about doing this.

The first method relies on the fact that a small saturation region plateau is observed in the ideal GFET $I_{ds}$-$V_{ds}$ curve as the channel is initially depleted of majority carriers by the drain bias at the drain end of the channel, but before the drain bias increases to the point where the carrier type is inverted. If the GFET is biased so that the device operates in this regime, the output conductance can be reduced, leading to improved high frequency performance and cutoff frequency.

The second method requires the utilization of a technique to open a bandgap in the graphene. By opening a bandgap, the output conductance can be reduced by reducing
ambipolar conduction as the drain bias increases. Additionally, the opening of a bandgap would also lead to improved on-off ratios. The combination of these two changes should lead to improved transistor performance, although the opening of a bandgap might also act to degrade the carrier mobility in the channel. As discussed in Chapter 1, there are several techniques that might be used to open a bandgap in graphene.

5.3 – Optimizing GFET Design to Minimize Device Parasitics

In order to access the excellent intrinsic properties of graphene, the effect of device parasitics must be minimized, including parasitic resistances due to un-gated portions of the channel or un-optimized contacts and parasitic capacitances due to un-optimized device structures. These parasitics act to reduce the device performance by limiting transconductance and, ultimately, the extrinsic small signal performance.

In order to minimize the effects of parasitics, they must first be quantified and characterized, requiring an extensive study of RF performance of GFETs of various gate length, width, and source-drain spacing, as well as device processing, and their effects on device parasitics. Such a study should make use of de-embed structures allowing device parasitics can be extracted from extrinsic S-parameters so that the source or cause of such parasitics might be discerned.

Continued optimization of the metal-graphene contact are anticipated to reduce parasitic contact resistances, while the adoption of a self-aligned process or source-drain extensions might be used to reduce the un-gated regions of the channel and reduce access resistance. Further work to identify device architectures that minimize parasitic capacitances or other device parasitics is necessary.
5.4 – Optimizing the Gate Dielectric Using Post-Processing

Although the results presented in this thesis show that use of O-ALD deposited gate dielectrics can lead to a substantial improvement in transport properties (up to 70%) and DC GFET performance, the significant amount of hysteresis present in $I_{ds}$-$V_{gs}$ curves suggest that the dielectric-graphene interface can be improved.

The extent of hysteresis found for O-ALD and EBPVD gated GFETs combined with a thickness dependence of mobility for EBPVD dielectrics suggest the presence of a large degree of charge traps which contribute both to hysteresis and also to limiting carrier mobility. The passivation or reduction of these traps or other defects that might exist within the as-deposited dielectric should lead to improved carrier mobility and reduced hysteresis.

For silicon devices, utilization of post-processing techniques such as heat treatments in forming gas have allowed for the reduction of such defects. Similarly, post-processing heat treatments of dielectrics on graphene-based devices could lead to substantial improvements in device performance. Therefore, work should continue to understand the dielectric-graphene interface and how best to optimize it so as to achieve a low density of charge traps and interface states, which degrade transistor performance.
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