TRANSPORT IN
SILICON QUANTUM DOTS EMBEDDED IN A
RARE EARTH OXIDE

A Thesis in
Engineering Science
by
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ABSTRACT

In this thesis, the room temperature quantum confinement effects in an array of Silicon (Si) quantum dots embedded in Gadolinium Oxide (Gd₂O₃) rare earth dielectric matrix is reported using photoluminescence (PL) spectroscopy. The high intensity and the small FWHM (0.12eV) of the PL peak indicate high crystalline quality and a narrow size distribution range (1 σ = 0.25nm) of the quantum dots. Electron storage density of 8x10¹² cm⁻² (corresponding to two electrons per quantum dot) is achieved by employing low programming voltage sweeps (-4V to 0V) as validated by the room temperature capacitance-voltage measurements. A temperature and field dependent study of the transport through the Si dot embedded Gd₂O₃ MOS tunnel diode structures is also presented. The tunneling mechanism assisted by the confined levels in the quantum dots and oxygen vacancy related trap level in the Gd₂O₃ dielectric is explained using physics based analytical models. The beneficial effect of forming gas anneal in controlling the trap density is also reported.

This device has potential to be used in nanocrystal flash memory devices operating at low voltage. Better control of trap density and reducing the size of nanocrystal to about 3nm to allow only one energy level per dot could improve the performance of the device. It would be interesting to further study the Coulomb oscillations and the in-plane transport in coupled quantum dot array device. This could have potential applications for making single electron transistors at room temperature.
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1. INTRODUCTION

1.1 What is a Quantum Dot?

Semiconductors are the basic building blocks of modern electronic industry and they comprise of groups of II-VI, III-V, or IV-IV materials. The conductivity of a semiconductor can be tuned by applying a voltage or light which makes possible a plethora of applications in electronics and optoelectronics. Quantum dots or nanocrystals are metallic or semiconducting materials the dimensions of which are in the range of 1-10 nm, with the exact size being dependent on the material system and the length scale of the quantum confinement. The unique optical and electronic properties of the nanocrystals are being actively researched for a variety of applications including nanomedicine, alternate energy, nanoelectronics, optoelectronics and solid-state displays.

In a quantum dot, the motion of charge carriers is confined spatially in all the three dimensions. This gives rise to quantized energy levels in the conduction and valance bands. Just as atoms are natural boxes that contain electrons in different energy levels, quantum dots could be thought of as “artificial atoms” which can store charges in discrete energy levels.

1.2 Density of States

Density of States refers to the number of states that a carrier can occupy per unit volume per unit energy at a specific temperature. By multiplying the density of states
with the probability that a state is occupied can give the number of electrons at each energy level per unit volume [1].

### 1.3 Density of States Calculation

The Density of States (DOS) in a semiconductor crystal with periodic potential is estimated as the density per unit volume and energy of the number of solutions to Schrodinger’s equation [1]. Consider a cubic piece of semiconductor with a side $L$. Assume that this can be modeled as an infinite quantum well with potential in the well taken as zero. The electrons in the well are free to move with an effective mass of $m^*$. Schrödinger’s equation along the x direction is given by eqn. 1.1

$$\frac{-\hbar^2}{2m^*} \frac{d^2\psi(x)}{dx^2} + V(x)\psi(x) = E\psi(x) \quad (1.1)$$

Boundary Conditions are

$$\psi(x) = 0, \text{ at } x = 0 \text{ and } x=L \quad (1.2)$$

The solutions to wave equation are of the form

$$\psi(x) = A \sin(k_x x) + B \cos(k_x x) \quad (1.3)$$

where $A$ and $B$ are constants. On applying the boundary conditions we get,

$$k_x = \frac{n\pi}{L}, \quad n = 1, 2, 3.. \quad (1.4)$$
Similar analysis can be done for \( y \) and \( z \) directions. Each possible solution of the Schrödinger’s equation then corresponds to a cube in the \( k \)-space with size \( n\pi/L \) as shown in figure 1.1.

![Figure 1.1: Calculation of the number of available energy states to accommodate electrons with wave number less than \( k \) [1]](image)

The total number of solutions to Schrödinger’s equation can be found by dividing the total volume in the first quadrant of the sphere with radius ‘\( k \)’ by the volume corresponding to a single solution. This has to be multiplied by a factor of 2 to account for the two possible spins for a given state. The total number of states in a volume of \( L^3 \) is given in eqn.1.5

\[
N = \frac{4}{3} \pi k^3 \cdot \frac{1}{8} \left( \frac{L}{\pi} \right)^3 \cdot 2 
\]  

(1.5)
The density per unit energy is given by

\[
\frac{dN}{dE} = \frac{dN}{dk} \frac{dk}{dE} = \left(\frac{L}{\pi}\right)^3 \pi k^2 \frac{dk}{dE}
\]  

(1.6)

From the parabolic E-k relationship,

\[
E = \frac{\hbar^2 k^2}{2m^*} \quad \Rightarrow \quad \frac{dk}{dE} = \frac{m^*}{\hbar^2 k} \quad \text{where} \quad k = \sqrt{\frac{2m^* E}{\hbar^2}}
\]  

(1.7)

Density of states, the number of states per unit volume per unit energy is given by

\[
g(E) = \frac{1}{L^3} \frac{dN}{dE} = \frac{8\pi\sqrt{2}}{h^3} m^{3/2} E^{3/2}, \quad \text{for} \ E \geq 0
\]  

(1.8)

The above expression is defined for \(E>0\). For electrons in the conduction band, the minimum energy position is the bottom of the conduction band, \(E_c\). The DOS for conduction band electrons can be expressed as given in Eqn. 1.9.

\[
g_c(E) = \frac{8\pi\sqrt{2}}{h^3} m_c^{3/2} \sqrt{E - E_c}, \quad \text{for} \ E \geq E_c
\]  

(1.9)

where \(m_c\) is the effective mass which describes the curvature of the conduction band.

Similar expression for DOS can be written for holes in the valance band as in Eqn.1.10.
\[ g_v(E) = \frac{8\pi \sqrt{2}}{h^3} m_v^{3/2} \sqrt{E_v - E}, \text{ for } E \leq E_v \] (1.10)

where \( m_v \) is the effective mass which describes the curvature of the valence band.

1.4 Density of States for Quantized Systems

The above expression for DOS is valid for a bulk semiconductor where the carriers are free to move in all the three spatial dimensions. In other words, carriers in a bulk semiconductor have three degrees of freedom and there will be a continuum of energy levels in the conduction and valance bands. If one of the physical dimensions of the material is reduced so that the motion of carriers in that direction is restricted, then the continuum of energy levels that normally exists in the conduction band or valance band of solids is transformed into a set of discrete energy states or quanta [1]. Number of states between \( k \) and \( k + dk \) in 1, 2 and 3 dimensions is given by

\[ \frac{dN_{3D}}{dk} = 2 \left( \frac{L}{2\pi} \right)^3 4\pi k^2 \] (1.11)

\[ \frac{dN_{2D}}{dk} = 2 \left( \frac{L}{2\pi} \right)^2 2\pi k \] (1.12)

\[ \frac{dN_{1D}}{dk} = 2 \left( \frac{L}{2\pi} \right) \] (1.13)

For a bulk semiconductor, the expression for DOS is same as in Eqn. 1.9. For a quantum well where particles are confined to a plane, DOS can be written as
This expression is only considering the first energy level. This has to be summed along all the quantized energy levels to get the final density of states, which will be a staircase function given by

\[ g_{c,2D}(E) = \frac{4\pi}{h^2} m^* \sum_n H(E - E_n) \]  

(1.15)

where \( H(E-E_n) \) is the Heaviside step function which will be zero for \( E<E_n \) and 1 for \( E>E_n \) and \( n \) is the quantum number along the quantized direction.

For the case of a quantum wire in which particles are confined along a line, 2D confinement gives rise to two quantum numbers \( n_1 \) and \( n_2 \).

\[ g_{c,1D}(E) = 2\sqrt{\frac{2\pi}{h^2}} m^* \sum_i \frac{1}{\sqrt{E - E_{n_1n_2}}} H(E - E_{n_1n_2}) \]  

(1.16)

For a 0-D structure or a quantum dot, the \( k \) values will be quantized in x, y and z directions. Available energies will be discrete and DOS can be represented as delta functions at those allowed energies. The graphical representation of the DOS for 3D (bulk), 2D (quantum well), 1D (quantum wire) and 0D (quantum dot) is shown in figure 1.2.
Table 1-1 shows the number of degenerate states for the ten lowest energy levels in a quantum well (2D), quantum wire (1D) and a quantum dot (0D). \(E\) is the energy of the \(i\)-th energy level, \(E_0\) is the ground state energy and \(n(E)\) is the number of degenerate states having an energy \(E\). In the quantum well, the ratio of \(i\)-th energy level to the ground state is proportional to \(k^2\), the wave number along the quantized direction. In this case, the degeneracy is one since there is only one value of \(k\) which can give a ratio that is proportional to \(k^2\). For the quantum wire, this ratio is proportional to \(k_x^2+k_y^2\). This give rise to a degeneracy of two as \((1,2)\) and \((2,1)\) and different energy states though the sum \(k_x^2+k_y^2\) is the same for both. Finally for the quantum dot case, the ratio of energy is proportional to \(k_x^2+k_y^2+k_z^2\) and there are six ways \(k_x,k_y,k_z\) can be arranged to get this ratio. Hence the degeneracy is six.
Table 1.1: Number of degenerate states \( n(E) \) for the ten lowest energy levels in a quantum well (2D), quantum wire (1D) and a quantum dot (0D)\[1\].

<table>
<thead>
<tr>
<th>State</th>
<th>2D Electron gas (Quantum Well)</th>
<th>1D Electron gas (Quantum Wire)</th>
<th>0D Electron gas (Quantum Dot)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>( E/E_0 )</td>
<td>( n(E) )</td>
<td>( E/E_0 )</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>3</td>
</tr>
<tr>
<td>2</td>
<td>4</td>
<td>1</td>
<td>6</td>
</tr>
<tr>
<td>3</td>
<td>9</td>
<td>1</td>
<td>9</td>
</tr>
<tr>
<td>4</td>
<td>16</td>
<td>1</td>
<td>11</td>
</tr>
<tr>
<td>5</td>
<td>25</td>
<td>1</td>
<td>12</td>
</tr>
<tr>
<td>6</td>
<td>36</td>
<td>1</td>
<td>14</td>
</tr>
<tr>
<td>7</td>
<td>49</td>
<td>1</td>
<td>17</td>
</tr>
<tr>
<td>8</td>
<td>64</td>
<td>1</td>
<td>18</td>
</tr>
<tr>
<td>9</td>
<td>81</td>
<td>1</td>
<td>21</td>
</tr>
<tr>
<td>10</td>
<td>100</td>
<td>1</td>
<td>27</td>
</tr>
</tbody>
</table>

The above degeneracy values are when the \( k \)-values are different. If some of the \( k \)-values are identical, then the degeneracy will be determined by the principle of combinations 
\((n!/m!,, \text{ where } n \text{ is the total number of quantized states and } m \text{ is the number of identical states})\).
1.5 Conclusions

Depending on the barrier height which sets the confinement, the number of available states can vary. For a silicon quantum dot of size 4 nm in diameter in an SiO$_2$ matrix, we would expect 3 confined states as given below.

State=1  Energy levels: (1,1,1)
State=2  Energy levels: (2,1,1),(1,2,1),(1,1,2)
State=3  Energy levels: (2,2,1),(1,2,2),(2,1,2)

The first state has a degeneracy of one and the second and third energy states have a degeneracy of three. Three energy states will be available which can accommodate a total of 14 electrons per quantum dot. This phenomenon has been exploited in nanocrystal memories where in precise control over threshold voltage is obtained by storing one or two electrons per quantum dot [2]. High density, low power operation and improved scalability can be achieved by using quantum dot non-volatile memory instead of floating gate memory. Quantum dot lasers have been demonstrated with temperature insensitive 10 Gbps operation above room temperature which was not possible using a quantum-well laser [3]. The wavelength of the laser can be tuned by changing the size of the quantum dot which allows it to operate at wavelengths previously not possible using semiconductor laser technology. Single electron transistors operating at room temperature with periodic oscillations in their output characteristics have been demonstrated using quantum dots [4]. The size of the quantum dots can be tuned to make the Coulomb charging energy higher than thermal energy (kT). Quantum dot displays are very appealing for energy efficient lighting as they use one-fifth to one-tenth as much power...
as LCDs [5]. Quantum dots give a very narrow emission spectrum which can outperform organic LEDs in the purity of colors that they emit.
2. APPLICATIONS OF QUANTUM DOT TECHNOLOGY

2.1 Introduction

Quantum dots are regarded as one of the potential candidates for next generation nanoelectronic devices and photonic devices [6]. Because of the quantum confinement in three dimensions, they have discrete density of states which results in interesting electrical and optical properties. In the energy space, quantum dots represent a region of low potential surrounded by high potential. Electrons which fall into this quantum box will be confined spatially due to the high potential required to escape. Applications of quantum dots cover a variety of fields including Single Electron Devices, Non-Volatile Memories, Photodetectors, Quantum Computing, Photovoltaics, LEDs, etc. The atomic like energy states of quantum dots give rise to particle-size dependent fluorescence which is harnessed in fabricating optical probes for biological and medical imaging.

According to market research group BCC (Business Communications Company), the global market for quantum dot technology is expected to increase at a compound annual rate of nearly of 91 percent over the next five years, and be worth $721.1 million in 2013[7]. BCC’s analysis breaks the market down into five application segments: stand-alone colloidal QDs, electronics, optoelectronics, optics and solar energy. Segments expected to launch in 2009 include electronics and optics. The optics segment will show larger growth, as QD-based lasers and other optical components impact communication applications. The electronics segment will see the launch of first generation QD-based
flash memory products and is slated to generate $45.8 million in 2010 and $61.0 million in 2013, for a CAGR of 10.0 percent. Quantum dots for applications in optoelectronics and solar energy are expected to launch in 2010. BCC suggests that in the markets noted, the combined forces of technology push and market pull, due in part to the growing involvement of multinational companies, will lead to a marked increase in both colloidal and in-situ QD production.

Since quantum dot lasers and LEDs are near established technologies, the focus of this chapter is to elucidate the applications of quantum dots in the non volatile storage and third generation photovoltaic space.

2.2 Quantum Dot Non-Volatile Memory

Semiconductor based flash memory has become increasingly popular for compact consumer applications like mobile phones, I-pods, memory sticks, video camera and, very recently, for solid-state replacement for computer hard disk. Flash has high storage density but rather slow write and erase times due to high voltage operation in the Fowler-Nordheim regime [8]. The basic structure of a flash memory transistor is shown in figure 2.1. There is a layer of silicon between gate electrode and the channel which stores the charge. A traditional Flash memory uses a poly Silicon floating gate for charge storage. There are other types of memory called SONOS (Silicon-Oxide-Nitride-Oxide-Silicon) which uses traps in the silicon nitride or oxynitride for charge storage.
To store charges in the floating gate, two main techniques are used – hot carrier injection and tunneling [8]. Hot carriers are those carriers which have high enough energy to cross the insulating barrier into the floating gate. A band diagram illustrating the same is shown in figure 2.2.
Hot carriers are generated by applying high potential between the source and the drain. These accelerated electrons will get into the floating gate under the application of a gate bias. Tunneling refers to quantum-mechanical behavior of the electron wave function where it extends through the barrier layer. This permits the electrons to tunnel into the floating gate layer. For good charge retention in the floating gate, the tunneling layer has to be thick. On applying field, this tunnel barrier thickness can be reduced and the charges can tunnel out of the floating gate. This is known as Fowler-Nordheim tunneling where the carriers tunnel through a triangular potential well as shown in figure 2.3.

![Figure 2.3: The barrier thickness is reduced by applying a potential (right) increasing the tunneling injection efficiency [8]](image)

It is very difficult to erase the stored charge through hot carrier injection, and hence Fowler-Nordheim tunneling is used for erasing operation. However, hot carrier injection causes degradation to the tunnel oxide and leads to reliability issues. A way to overcome this is by designing a Flash memory which can operate in the direct tunneling regime [9]. By using nanocrystal Silicon instead of poly-Si gate, the tunnel oxide can be
made thinner without compromising charge retention. In fact, using nanocrystal floating gates enhance the retention characteristics as even if one of the dots in a floating gate is discharged through pin holes, it does not leak the stored charge in other dots. The use of nanocrystals enables low programming voltages, enhanced charge retention, direct tunneling operation which results in greater endurance for read/write cycles and enhanced device reliability. Hence the nanocrystal memories are very attractive from a scaling point of view.

Dr. Sandip Tiwari of IBM, T.J. Watson Research Center has reported on a Flash memory device using Silicon nanocrystals which operates in the Direct Tunneling regime with a very long refresh time at room temperature [9]. A schematic of the device is shown in figure 2.4.

![Figure 2.4: (a)Schematic of the device (b) Band diagram during storage (c) Band diagram during erase [9]](image-url)
Tunnel oxide is about 1.5nm thick and direct tunneling is the dominant charge storage mechanism. Injection of electrons occurs via direct tunneling from the inversion layer of the transistor when it is in ON state. The injected electrons further screen the applied gate potential resulting in lower channel conduction. In other words, the threshold voltage of the device has been shifted (towards more positive voltage for this n-channel device). This VT window is used in storing/erasing the data. The shift in threshold voltage is given by eqn. 2.1 [9],

\[
\Delta V_T = \frac{qn_{well}}{\varepsilon_{ox}} \left( t_{cntl} + \frac{1}{2} \frac{\varepsilon_{ox}}{\varepsilon_{Si}} t_{well} \right) \quad (2.1)
\]

Here \( \Delta V_T \) is the threshold voltage shift, \( n_{well} \) is the density of quantum dots, \( t_{cntl} \) is the control oxide thickness and \( t_{well} \) is the size of the nano-crystal well. For a nano-crystal 3nm in size and 5nm in-plane spacing, the dot density will be about \( 4 \times 10^{12} \, \text{cm}^{-2} \). With a control oxide thickness of 4nm and oxide dielectric constant of 13 (Gd\(_2\)O\(_3\)), the shift in threshold voltage will be 0.32 V for single electron storage of the quantum dot. This shift of \( V_T \) is very appreciable and a well designed transistor changes its sub-threshold current by about 5 orders of magnitude for this shift of \( V_T \). This current difference can be easily sensed.

Removing the charge stored in the nanocrystals requires lowering the energy of the substrate compared to the nanocrystal. The dots are surrounded by oxide matrix which prevents tunneling between dots. The actual leakage of the dots is determined by the quiescent bias state of the dots which leaves the band alignment unfavorable for
tunneling. Thus the nanocrystal memory has a very long retention time and non-volatility is achieved with low tunnel oxide thickness.

Figure 2.5 shows the shift in threshold voltage as a function of applied gate voltage. The steps in the curve are due to single electron storage in the nanocrystals. At higher temperatures this step is not seen. The authors claim that at least 3nm sized dots are required to see the steps at room temperature.

![Figure 2.5: Threshold voltage as a function of static gate voltage obtained using pulsed measurement at the quiescent gate voltage](image)

The refresh times of the nanocrystal device are very large as shown in table 2.1. However there is an increase in the erase time for these devices. Enhanced read/write cycles have been achieved in these devices due to its operation in the direct tunneling
regime. The advantages in speed, power and scalability make quantum dots potential candidates for non-volatile storage applications.

<table>
<thead>
<tr>
<th>Oxide Thickness</th>
<th>Write Condition</th>
<th>$\Delta V_T$</th>
<th>Refresh Time</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.6 nm</td>
<td>200 ns 3 V</td>
<td>$\approx 0.65$ V</td>
<td>$&gt; 1 \text{ wk (RT)}$</td>
</tr>
<tr>
<td>2.1 nm</td>
<td>400 ns 3 V</td>
<td>$\approx 0.48$ V</td>
<td>$&gt; 1 \text{ wk (RT)}$</td>
</tr>
<tr>
<td>3.0 nm</td>
<td>1 $\mu$s 3 V</td>
<td>$\approx 0.55$ V</td>
<td>$&gt; 1 \text{ wk (RT)}$</td>
</tr>
<tr>
<td>3.6 nm</td>
<td>5 $\mu$s 4 V</td>
<td>$\approx 0.50$ V</td>
<td>$&gt; &gt; 1 \text{ hr (85 C)}$</td>
</tr>
</tbody>
</table>

Table 2.1: Threshold shift and refresh time characteristics of Si NC Flash [9]

![Dispersion in threshold voltage as a function of effective channel length](image)

Figure 2.6: Dispersion in threshold voltage as a function of effective channel length [10]
As MOS device scaling continues, dispersion in the threshold voltage due to random dopant fluctuations become an important issue for floating gate flash memory cell. Figure 2.6 shows the dispersion in threshold voltage ($\sigma V_T$) as a function of effective channel length. For normal operation of a flash memory the threshold voltage window ($\Delta V_T$) should be about $3\sigma V_T$. For a transistor with an effective gate area of 25nm x 25nm, $\sigma V_T$ will be about 0.1V and for the normal operation of the device a $V_T$ window of 0.3V is required.

2.3 Quantum Dot Enhanced Solar Cells

The maximum thermodynamic efficiency for the conversion of unconcentrated solar irradiance into electrical free energy in the radiative limit, assuming detailed balance, a single threshold absorber, and thermal equilibrium between electrons and phonons, was calculated by Shockley and Queisser in 1961 to be about 31% [11]. The two major factors that limit the conversion efficiency of solar cells in Shockley-Queisser analysis are; (1) photons with energy above bandgap relax through phonon emission and (2) sub bandgap energies are not absorbed. So to improve the efficiency, the high energy carriers have to be collected before they relax to the band edge via phonon emission and also the sub bandgap photons have to be absorbed via some mechanism.

Semiconductor quantum dots (QD) can increase photon conversion efficiency by two mechanisms: (1) Multiple Exciton Generation (MEG) from a single photon and (2) formation of Intermediate Band (IB) in the bandgap, which enables absorption of sub
band gap energy photons. This is because of a number of factors due to quantization effects like, slowed hot electron-hole pair (exciton) cooling, formation of minbands in quantum dot arrays, elimination of requirement to conserve crystal momentum, enhanced impact ionization process to generate secondary electron-hole pairs etc.

Very efficient multiple electron–hole pair generation (MEG) by one photon has been reported recently in PbSe, PbS, PbTe, and CdSe nanocrystals [12]. Although 300% quantum yield was measured for exciton formation in the QDs, no group has yet reported enhanced photocurrent with photocurrent quantum yields greater than 100% in any QD-based photovoltaic device. This could be due to enhanced recombination on the surface of the quantum dots. Such experiments are currently in progress.

Different solar cell configurations have been proposed based on quantum dots, namely (1) QD array used in the i-region of a p-i-n photovoltaic cell which is expected to reduce carrier cooling and permits transport and collection of hot carriers, (2) QD sensitized nanocrystalline TiO₂ which produces quantum yields greater than 1 due to impact ionization (QDs replace dyes in dye-sensitized TiO₂ solar cell and upon photoexcitation of the dot, electrons are injected very efficiently from the excited state of dot to the conduction band of TiO₂), and (3) QDs dispersed in a blend of electron and hole conducting polymers which enable selective contacts to both electrons and holes [13]. All these approaches simply represent different modes of collecting and transporting photo generated carriers produced in the QDs. Also there have been other approaches to
To facilitate transition from IB to CB (Conduction Band) there should be enough electrons in the IB. Also to promote excitation of electrons from VB (Valence Band) to IB, there should be enough vacant states in the IB. Hence the IB must be half filled with electrons for optimal performance.
A typical structure of a QD-IB solar cell consists of multiple layers of InAs/GaAs QDs sandwiched between $p$ and $n$ GaAs emitters and grown by MBE in the Stranski-Krastanov growth mode [15]. This cell exhibits extended response for photon energies lower than GaAs bandgap, however the photocurrent appeared to be same as that of a GaAs test sample (without QDs). Also there has been a slight degradation in the open circuit voltage which may be due to effective reduction in the total bandgap due to InAs and also because of higher density of defects and poor absorption due to QDs. Nevertheless, experiments suggest that with improved materials and design, the IB solar cell can enhance the photocurrent without degrading voltage and help improve the efficiency significantly.
3. TRANSPORT STUDIES OF SILICON (Si) QUANTUM DOTS EMBEDDED IN EPITAXIAL GADOLINIUM OXIDE (Gd$_2$O$_3$)

3.1 Introduction

Quantum dot memories using Si and Ge nanocrystals are of special interest for nonvolatile storage applications. Conventional floating gate memories require a fairly thick tunnel oxide and high programming voltages. Scaling the tunnel oxide thickness can cause the charge to leak through defect states present in the oxide affecting retention time. By replacing the floating gate with Si nanocrystals, it is possible to scale down the oxide and also reduce the programming voltages.

Semiconductor nanocrystals (SNCs) are better compared to metal nanocrystals (MNCs) for storage applications as shown in figure 3.1 [16]. In MNCs, quantum confinement effects become appreciable only at very small dot sizes (~1nm for Ni). To get precise control over the threshold voltage window, it is desirable to have only one energy level in the quantum dot which allows storage of two electrons per dot. This control on storage is not possible using MNCs. Among Si and Ge nanocrystals, Si has orders of magnitude better retention characteristics compared to Ge as shown in figure 3.2. This is due to the more pronounced quantum confinement effects in Ge due to its lower density of states effective mass. This makes Si nanocrystals potential candidates for non-volatile storage applications.
Integrating single crystal Si nanostructures in epitaxial oxides has been of interest recently. The high dielectric constant (~13), favorable band offsets [17] and process compatibility with Si CMOS technology make rare earth oxides (REOs) potential candidates for high-k applications. Among REOs, Gd$_2$O$_3$ is potential candidate matrix for...
embedding Si nanocrystals due to its symmetric band offset with Si and negligible lattice mismatch. Figure 3.3 shows the lattice mismatch of Si with rare earth oxides. Lattice constant of Gd$_2$O$_3$ (a = 10.812 Å) is very close two twice that of Si (2a = 10.862 Å) which gives a misfit of about 0.4% [18]. It is highly relevant to understand the charging mechanism and the effect of trap states in the oxide on the electrical characteristics of the device.

![Figure 3.3: Lattice Mismatch for Rare Earth Oxides with Silicon and Germanium [18]](image)

In this chapter, we report on the room temperature quantum confinement effects in an array of Si quantum dots (QDs) embedded in Gd$_2$O$_3$ dielectric matrix using photoluminescence (PL) spectroscopy. The high intensity and the small FWHM (0.12eV) of the PL peak indicate high crystalline quality and a narrow size distribution range (1 $\sigma$ = 0.25nm) of the quantum dots. Electron storage density of 8x10$^{12}$ cm$^{-2}$ (corresponding to two electrons per quantum dot) is achieved by employing low programming voltage sweeps (-4V to 0V) as validated by the room temp Capacitance-Voltage (CV)
measurements. We further present a temperature and field dependent study of the transport through the Si dot embedded Gd$_2$O$_3$ MOS tunnel diode structures. The tunneling mechanism assisted by the confined levels in the quantum dots and oxygen vacancy related trap level in the Gd$_2$O$_3$ dielectric is explained using physics based analytical models. The beneficial effect of forming gas anneal in controlling the trap density is also reported.

### 3.2 Device Fabrication

High quality single crystalline Si dots (3-4 nm) with a dot density of 4x10$^{12}$cm$^{-2}$ were grown within a Gd$_2$O$_3$ matrix using solid-source molecular beam epitaxy (MBE). A schematic of the MBE deposition chamber is shown in figure 3.4. The device schematic is shown in figure 3.5. Gd$_2$O$_3$/Si(NC)/Gd$_2$O$_3$ stacks were fabricated on n- and p-type Si(111) substrates (0.1-0.3 ohm.cm). The epitaxial Gd$_2$O$_3$ tunnel oxide layer was grown at 675 °C on specially prepared silicon surfaces under an oxygen partial pressure 5x10$^{-7}$ mbar [19]. Subsequent deposition of Si at high temperatures (>400 °C) led to single crystal Si nanocrystal formation on epitaxial Gd$_2$O$_3$ surface which was eventually capped with a Gd$_2$O$_3$ control oxide layer. Aluminum gate was deposited using shadow mask evaporation.

The preparation of Si substrates and the structural evolution of the oxide layer and the Si nanoclusters were investigated *in situ* by reflection high-energy electron diffraction
(RHEED), and *ex situ* by atomic force microscopy (AFM) and transmission electron microscopy (TEM).

Figure 3.4: Schematic of the MBE chamber [18]

Figure 3.5: Schematic of the Si quantum dot capacitor structure (Si QD embedded in Gd$_2$O$_3$ matrix)
A TEM cross section of the device is shown in figure 3.6. X-ray diffraction results (figure 3.6) show crystalline Gd2O3 and Si dots with the (111)Gd2O3 || (111)Si.

Figure 3.6: TEM cross section showing crystalline Si QD embedded in Gd2O3 [18]

Figure 3.7: X-ray diffraction results on the device showing single crystalline Gd2O3/Si/Gd2O3 stack on Si(111) [18]
Si quantum dot peaks overlaps with the substrate and hence cannot be distinguished. Also we could see small peaks in the XRD data which are called “layer oscillations”. These are thickness fringes due to finite layer of Gd$_2$O$_3$ on and under Si layer. These fringes appear only when we have sharp interface.

Photoluminescence measurements were done prior to metallization using Ocean Optics HR2000 spectrometer. Current-voltage and capacitance-voltage characteristics have been studied using HP4156A Semiconductor Parameter Analyzer and HP4285A Precision LCR meter.

3.3 Photoluminescence Results and Analysis

Photoluminescence studies were done to study the emission properties and the quantum confinement effects of the nanocrystal Silicon (nc-Si)). PL peaks with high intensity were obtained at room temperature with the peaks shifting towards higher energy with smaller dot sizes, consistent with the quantum confinement effect behavior. Two sets of samples with different dot sizes were analyzed. Figures 3.8 and 3.9 show the PL spectra of samples with dot sizes of 4.5 and 3.5 nm, respectively as a function of the increase in bandgap of Silicon ($\Delta E$).
Figure 3.8: PL spectra of the 4.5 nm Si sample

Figure 3.9: PL spectra of the 3.5 nm Si sample
The magnitude of bandgap widening due to quantum confinement in nc-Si can be expressed as $\Delta E = \frac{4.122}{d^{1.39}}$ [20]. Here $\Delta E$ is the increase in bandgap due to quantum confinement. The profile of PL distribution has been explained in reference [21] taking into account quantum confinement effects. A normal distribution of nanocrystal size was assumed in deriving the expression. The intensity of the PL peak as a function of $\Delta E$ is given below,

$$I(\Delta E) = K(\Delta E)^{-5.32} \exp\left[\frac{\left(\frac{4.122}{\Delta E}\right)^{0.72} - d_0}{2\sigma^2}\right]^2$$

where $d_0$ is the dot size and $\sigma$ is the mean distribution. This expression was used to fit the PL peaks and dot size and mean distribution were estimated. The size distribution was less than 7% of the dot diameter in each case. These observed $\Delta E$ values were in accordance with quantum confinement effects as shown in figure 3.10.

![Figure 3.10: Experimental and theoretical $\Delta E$ vs dot size](image-url)
In the first set $\Delta E = 0.53$ eV which corresponds to a dot size of 4.5 nm. In the second case there are two peaks, the first one at $\Delta E = 0.65$ eV and a second one with $\Delta E = 0.76$ eV. The peak at 0.76eV is due to QCE from nc-Si with a dot diameter of 3.4nm and the peak at 0.65eV is due to emission from Localized Surface States. As the dot size decreases, interface defects increase which give rise to the LSS peak [22]. Since the excitation energy was 488 nm (2.54eV) in the second case, the possibility of multiple exciton generation was ruled out. To get MEG, the photon energy has to be at least twice the bandgap of the quantum dot [23]. Since the photon energy (2.54eV) is less than sum of energies of the two peaks (3.61eV), it is not possible for multiple exciton generation to happen.

3.4 Capacitance-Voltage Characteristics

Capacitance-voltage measurements were done on both n-type and p-type devices. Figure 3.11 shows the CV sweep at 1MHz for the n-type sample. The conductance peaks for the forward and backward sweep is shown in figure 3.12. The clockwise hysteresis in the CV is due to electron injection from the substrate at high voltage. The shift in the conductance peaks between forward and backward sweeps is due to this charging of the nanocrystals. The control samples without dots have negligible hysteresis as shown in figure 3.13 [18]. The peak conductance in the G-V curves arises from the dissipative mechanism due to charging of the interface states. The position of the peaks depends on the energy level of the interface state within the conduction band of Si which is normally close to midgap.
Figure 3.11: CV hysteresis measurement for a Si quantum dot capacitor on a n-type Si substrate

Figure 3.12: GV hysteresis measurement for a Si quantum dot capacitor on a n-type Si substrate
Shift in the peak positions between forward and backward GV sweeps is due to charging of nanocrystals which shifts the flatband voltage of the device.

The shift in the flat band voltage was 0.7V at room temperature. The number of electrons in the quantum dots and the threshold voltage shift are related by

\[
\Delta V_t = \frac{qn_{\text{well}}}{\varepsilon_{\text{ox}}} \left( t_{\text{cntl}} + \frac{1}{2} \frac{\varepsilon_{\text{ox}}}{\varepsilon_{\text{Si}}} t_{\text{well}} \right)
\]  

(3.2)

where, \(t_{\text{cntl}}\) is the thickness of the control oxide under the gate, \(t_{\text{well}}\) is the linear dimension of the nanocrystal well, \(\varepsilon_{s}\) are the permittivities, \(q\) is the magnitude of electronic charge, and \(n_{\text{well}}\) is the density of nanocrystals [9].
The estimated dot density for a sample with 3nm Si dot and 5nm in-plane spacing is about $4 \times 10^{12}$ cm$^{-2}$ from AFM and SEM measurements [18]. Using this dot density, the $V_t$ shift for single electron charging of the dots is estimated to be about 0.32V. The observed $V_t$ shift would then correspond to about 2 electrons per dot.

3.4 Current-Voltage Characteristics and Transport Models

Current-voltage characteristics of the device as a function of temperature is shown in figures 3.14 and 3.15. It is interesting to note that the origin of the IV curve is shifted. This is due to the charging effect of the nanocrystal which causes the IV curve to be shifted to the left or right of the origin. The charging effect can also add asymmetry to the shape of the IV curve [24]. Similar shifts of origin due to nanocrystal charging effects have been reported in literature [25]. Fig. 3.16 shows a large hysteresis in the IV characteristics which together with the CV measurements confirm the charging effect of nanocrystals.

The JV curve consists of two distinct regimes as shown in figure 3.14 - 1) Quantum dot assisted tunneling regime at low fields where the tunneling current is weakly dependent on the applied field, and 2) Poole-Frenkel assisted tunneling regime at high field where the tunneling current is strongly dependent on the field. The mechanisms acting in these regimes are explained below.
Figure 3.14: Jg-Vg vs temperature for a Si quantum dot capacitor on a p-type Si substrate

Figure 3.15: Jg-Vg vs temperature for a Si quantum dot capacitor on a n-type Si substrate
Energy band diagrams for the structure were simulated using Sentaurus Device Simulator. Figure 3.17 shows the band diagram of quantum dot embedded oxide, 3.19 shows the charge density in the quantum dot and 3.18 shows the band diagrams without quantum dots, for three voltages in the low field regime.
Figure 3.17: Simulated energy band diagram for Si quantum dot and Gd$_2$O$_3$ oxide capacitor

Figure 3.18: Simulated energy band diagram for the Gd$_2$O$_3$ oxide capacitor without quantum dot
A positive fixed charge was added to account for the $V_{FB}$ shift. The bandgap of the quantum dot has been estimated from the PL measurements to be 1.85eV. Schroedinger wave equation was not solved in the simulation. For the conduction band of Si quantum dot, the first energy level is represented by solid line and the second energy level by dotted line. As shown in the band diagram, the tunneling at low field is a two step process. $T_1$ is the tunneling probability from the semiconductor to the second energy level in the quantum dot. $T_2$ is the tunneling probability from the quantum dot to the conduction band of oxide.

Figure 3.19: Simulated electron density for the device with quantum dot as a function of bias voltages
As shown in the band diagram in figure 3.17, the field across the tunnel oxide remains the same for different applied voltages ($V_3 > V_2 > V_1$) in the low field regime. This is due to charge storage in the quantum dot as shown in figure 3.19. Since this field remains constant, $T_1$ will be weakly dependent on applied field and the net tunneling probability, $T$ will be limited by $T_1$. Hence there will be a weak dependence of tunneling current with applied field. In the case of oxide without quantum dot as shown in figure 3.18, the field across the oxide increases with applied voltage and this gives rise to a stronger field dependence of tunneling current.

The tunneling through the second level in the oxide is similar to Trap Assisted Tunneling (TAT) mechanism [26]. The two-step TAT model treats $T_1$ and $T_2$ as two tunneling events in series. The net tunneling probability is given by $T_1 T_2 / (T_1 + T_2)$ and the tunneling current is given by

$$J = \int_0^{X_1} \frac{C_t q N_t T_1 T_2}{(T_1 + T_2)} dx$$  \hspace{1cm} (3.3)

where $C_t$ is a slowly varying function of electron energy, $N_t$ is the quantum dot concentration. The schematic of the mechanism is shown in figure 3.20.

The tunneling probabilities $T_1$ and $T_2$ are given by [26],

$$T_1 = K \exp \left( -\frac{4(2qm_{ox})^{1/2}}{3\hbar} \frac{3}{2} xE_{QD}^{1/2} \right)$$  \hspace{1cm} (3.4)
\[ T_2 = \exp \left( -\frac{4(2qm_{\text{ox}})^{1/2}}{3\hbar E} E_{QD}^\frac{3}{2} \right) \] (3.5)

where \( K \) is a constant to account for tunneling across the tunnel oxide layer \( E \) is the electric field across the oxide, \( x \) is the distance and \( E_{QD} \) is the trap level as shown in fig. 8.

\[ J = \frac{C_i q N_i T_2}{A} \left( A x_1 - \ln \left( \frac{1 + T_2 \exp(Ax_1) / K}{1 + T_2 / K} \right) \right) \] (3.6)

Figure 3.20: Schematic of the low field tunneling mechanism

Here the dependence of \( T_1 \) on the oxide electric field is considered to be negligible due to the charging effect of nanocrystals. On integrating equation 3.3 using expressions in 3.4 and 3.5, we get
The denominator in the expression $1+T_2/K$ can be approximated by 1. In the numerator, $T_2\exp(Ax_1)/K \gg 1$. A simplified expression can be obtained as shown in eqn. 3.8

$$J = \frac{2C_iN_i qE_{QD} \exp[(-D/E)E_{QD}^{3/2}]}{3E} + \ln K \quad (3.8)$$

where

$$D = \frac{4\sqrt{2qm_{ox}}}{3\hbar} \quad (3.9)$$

The factor $\ln K$ could be ignored as this is insignificant. This expression should be able to match the experimental IV curve in the low field region, as this already takes into account that the tunneling is limited by $T_1$. A plot of $\ln(JE_{ox})$ vs $1/E_{ox}$ should give a straight line according to the eqn. 10 and the trap level can be estimated from the slope of the curve.

$$\ln(JE) = (-DE_{QD}^{3/2}) \frac{1}{E} + \ln G \quad (3.10)$$

where

$$G = \frac{2C_iN_i qE_{QD}}{3} \quad (3.11)$$

Figures 3.21 and 3.22 show $\ln(JE_{ox})$ vs $1/E_{ox}$ plots for n-type and p-type devices respectively in the low field regime.
Figure 3.21: $\ln(J_{E_{ox}})$ vs $1/E_{ox}$ for Si quantum dot and Gd$_2$O$_3$ oxide capacitor structure on n-Si substrate

Figure 3.22: $\ln(J_{E_{ox}})$ vs $1/E_{ox}$ for Si quantum dot and Gd$_2$O$_3$ oxide capacitor structure on p-Si substrate
There is a very good match between the experimental data and the analytical model. The extracted trap energy of 0.19 eV was consistent for both the substrates. This energy level corresponds to the second energy level in the Si quantum dot. There is a parallel shift in the data for different temperatures. This is due to the temperature dependence of the trap assisted tunneling [26].

In the high field regime, there is a strong dependence of tunneling current with electric field and temperature. This has been characterized by Poole Frenkel emission from traps present within the oxide. A schematic of the mechanism is shown in figure 3.23. Electrons tunnel into the traps present in the oxide through a mechanism similar to Fowler-Nordheim tunneling. As the applied voltage increases, the barrier for the trapped electrons lowers and the electrons get emitted into the conduction band from the traps.

Figure 3.23: Schematic of high field tunneling (Dotted line across the oxide is the trap level and dashed line in the QD is the second energy level)
This barrier lowering is shown in figure 3.24. Solid line represents the Coulombic barrier without applying electric field. Dashed line shows the effect of an applied electric field. As we can see the effective barrier for the carriers in the trap gets lowered by $\Delta \phi$ due to the field. When this barrier becomes low enough, the traps will contribute to conduction.

![Figure 3.24: Mechanism of Poole-Frenkel Effect showing barrier lowering with applied electric field. Slope of the dash-dot line gives the electric field [27].](image)

The expression for current density due to Poole-Frenkel emission is given by [27]

\[
J = CE \exp \left( \frac{-q \left( \varphi_T - \sqrt{\frac{qE}{\pi \varepsilon}} \right)}{kT} \right)
\]

(3.13)

where $E$ is the electric field in the oxide, $\varphi_T$ is the trap energy, $\varepsilon$ is the dynamic dielectric constant and $C$ is the pre-exponential factor.
Plots of $\ln(J/E)$ vs $\sqrt{E}$ are shown in figure 3.24 which confirms the PF mechanism. The activation energy plot $\ln(J/E)$ vs $1/kT$ is shown on the in figure 3.25 for two gate voltages. As seen from the plot, at low temperatures the PF emission gets suppressed and the mechanism will be limited by Quantum Dot Assisted Tunneling as discussed before. From the slope of the activation energy plot, trap level has been estimated to be $1.06\pm0.03\text{eV}$ for the p-type device and $1.03\pm0.03\text{eV}$ for the n-type device. This trap energy level corresponds to oxygen vacancy in the high-k dielectric during the growth process at $5\times10^{-7}$ torr.

As shown in the schematic in figure 3.23, tunneling into the traps at high fields is similar to Fowler Nordheim (FN) tunneling and a plot of $\ln(J/E_{\text{ox}}^2)$ vs $1/E_{\text{ox}}$ gave a straight line which confirmed the same. From the slope of the FN fitting, the effective barrier height (from conduction band of Si to the trap level, $\varphi_B$) was estimated. Effective mass of $0.29m_0$ was used in the calculation [28]. Figure 3.26 shows the FN plots.
Figure 3.25: Poole-Frenkel fitting for Si quantum dot and Gd$_2$O$_3$ oxide capacitor structure on n-Si substrate

Figure 3.26: Activation energy plot for Si quantum dot and Gd$_2$O$_3$ oxide capacitor structure on n-Si substrate
However there is a parallel shift for curves at different temperatures due to the PF emission occurring simultaneously. Consistent results have been obtained for both n-type and p-type devices. The extracted barrier height was 1.05eV for both the cases. Adding $\phi_B$ and $\phi_T$ should give the conduction band offset between Si and Gd$_2$O$_3$. This value came out to be 2.08eV for n-type and 2.12eV p-type devices. The estimated conduction band offset from our analysis is in good agreement with previously reported value of 2.1±0.1eV from spectroscopic ellipsometry technique [29].

Figure 3.27 shows the experimental JV curve fitted with analytical models in the high field and low field regimes. The models fit very well with experimental data.
Figure 3.28: Experimental data fitted with theoretical models for high and low field regimes for Si quantum dot and Gd$_2$O$_3$ oxide capacitor structure on n-Si substrate at 300K

All the above analyses were done for electron injection from the substrate. The left side of the IV curve is due to electron injection from the metal side. It has been verified conduction mechanism is similar to the substrate injection case. There was no hole injection for both p type and n type devices. This is due to the higher barrier height for holes (3.9eV) compared to electrons (2.0eV) for Al. For higher work function metals like Pt (4.65eV), there could be hole injection from the substrate at negative voltages. For storage applications, it is not desirable to have carrier injection from the metal and right work function metals have to be chosen for n-type and p-type devices. Pt will work for p-type devices for hole storage and Al for electron storage in n-type devices.
3.5 Effects of Annealing

The variation in the tunneling characteristics due to different processing conditions was studied. Figure 3.28 compares the JV characteristics of p-type devices with different processing history- 1) as grown sample 2) Foaming Gas Annealed (FGA) samples for 7 min at 450°C and 3) FGA for 12 min at 450°C. It could be seen that the PF tunneling comes down with annealing. This shows that the trap density decreases with annealing. PF tunneling is not desirable for charge storage applications as it limits the storage of charge and the trap density in the oxide should be annealed out to reduce PF tunneling.

![Effect of Annealing on IV Characteristics (p-Si substrate)](image)

Figure 3.29: JV characteristics showing decreased PF conduction with annealing
CV measurements of the annealed samples also show a shift in the $V_{FB}$ with annealing which corresponds to less positive oxide charge (figure 3.29). Similar shift in $V_{FB}$ was obtained for the n-type devices and it could be concluded that FG annealing is to be done for sufficient time to control trap density in the devices.

![Figure 3.30: CV hysteresis measurement for Si quantum dot and Gd$_2$O$_3$ oxide capacitor structures on n-Si substrate](image)

For the p-type devices (figure 3.29), the hysteresis arises from gate electron injection due to lower barrier height with Al gate electrode (2 eV). Here the $V_{FB}$ shift corresponds to storage of less than 2 electrons per dot. This is because PF conduction sets in before the dots are charged to the full capacity.

PL peaks for the annealed samples showed higher intensity due to less non-radiative recombination from the traps (figure 3.30).
Tunneling mechanism in Silicon quantum dot embedded Gd$_2$O$_3$ MOS devices was studied. Low field tunneling was characterized by quantum dot assisted tunneling. The extracted activation energy of 0.19eV corresponds to the second energy level in the Si dot. There is a weak dependence of tunneling current on applied field in the low field regime due to charge storage in the nanocrystal. For high field, conduction is due to Poole-Frenkel emission from the traps. A trap energy of 1.03 eV was estimated from the activation energy plots which corresponds to oxygen vacancies in the dielectric. It was shown that trap density in the oxide could be reduced by FG annealing.
CV hysteresis measurements showed a threshold voltage shift of 0.7eV which corresponds to a storage of 2 electrons per nanocrystal. This device has high potential to be used in a nanocrystal Flash memory operating at low voltage. Better control of trap density and reducing the size of nanocrystal to about 3nm to allow only one energy level per dot could improve the performance of the device. High work function metal (Pt) should be used for hole storage applications and low work function metal (Al) for electron storage. It would be interesting to further study the Coulomb oscillations of the nanocrystals and also the in-plane transport of the device. This could have potential applications for making Single Electron Transistors at room temperature.
4. FUTURE WORK

4.1 Prospects of Si Quantum Dot Embedded Gd$_2$O$_3$ for Non-volatile Storage

For continued non-volatile memory (NVM) scaling, it is required to replace the poly-Si floating gate with trap-based flash and Si nanocrystal embedded in Gd$_2$O$_3$ is a potential candidate for achieving high density and low power operation. For a transistor with an effective gate area of 25nm x 25nm, dispersion in threshold voltage ($\sigma V_T$) due to random dopant fluctuations will be about 0.1V [10] and for the normal operation of the device a $V_T$ window of at least 0.3V (3*$\sigma V_T$) is required. The Si dot device we have studied could precisely store two electrons per quantum dot which gave a $V_T$ window of 0.7V. The device can operate with low power in the direct tunneling regime where there is no hot carrier degradation.

In this device, charge is stored in discrete individual quantum dots. Therefore a charge loss defect will cause only loss of a few electrons per cell as opposed to loss of all the charge stored in a floating gate. This improves the reliability and also allows scaling of the tunnel oxide which results in low power operation. The device shows good retention and endurance characteristics with negligible loss of stored charge (figures 4.1 and 4.2) [18]. The interference between adjacent floating gates can be also reduced by using Si quantum dot instead of floating gate. It is also very important to control the size distribution of the nanocrystal which can cause fluctuations in the $V_T$ for different
devices on the same chip. We have achieved very good control on the dot size (±0.25 nm dispersion for a 3.5nm Si dot) as indicated by the sharp peaks in the PL.

Figure 4.1: Retention Characteristics of epi-Gd$_2$O$_3$/Si QD/epi-Gd$_2$O$_3$/Si [18]

Figure 4.2: Endurance Characteristics of epi-Gd$_2$O$_3$/Si QD/epi-Gd$_2$O$_3$/Si [18]
Staircase IV characteristics were observed at room temperature for the device. Figure 4.3 shows the IV characteristics for Si quantum dot and Gd2O3 oxide capacitor structure on n-Si substrate. Low noise measurement techniques are required to further study this behavior as a function of temperature.

![Figure 4.3: Conductance peaks as a function of temperature for the Si quantum dot and Gd2O3 oxide capacitor structure on n-Si substrate](image)

The self capacitance of Si quantum dots embedded in oxide is given by [33]

\[
C = 4\pi e_{\text{ox}} r \left[ 1 + \frac{r}{2l} + \frac{\left(\frac{r}{2l}\right)^2}{1 - \left(\frac{r}{2l}\right)^2} \right]
\]  

(4.1)

where \( r \) is the radius of the quantum dot, \( l \) is the distance between center of the dot and the substrate surface. The self capacitance for 3.5 nm Si dot in Gd2O3 is calculated to be 2.97aF. Energy required to add an additional electron to the dot, the Coulomb charging
energy is given by $q^2/C$ (54meV). Since this energy is greater than thermal energy (26 meV) it is possible to observe Coulomb charging effects at room temperature. This effect can be utilized in making Single Electron Transistors (SETs) operating at room temperature.

4.2 Quantum Dots and Single Electron Transistors

As transistors continue to scale down, quantum nature of electrons and holes become important in the device structure and operation. A conventional field effect transistor (FET) is a switch that turns on when electrons are added to a semiconductor and turns off when they are removed, by the application of a gate bias. These FETs are almost classical in their physics and only a few numbers that characterize their operation are governed by quantum mechanics. However, if a transistor has electrons confined in a small volume that communicates with the electrical contacts by tunneling, then the behavior of the device will be entirely quantum mechanical. One such transistor, which turns on and off every time an electron is added to it is called a single Electron Transistor (SET). SETs are considered to be potential candidates for future low power and high density applications. In order for the device to be operated at room temperature, the electrical characteristics should be free from thermal fluctuations. This sets a limit on the size of the confined islands to be no larger than 10nm.

A schematic of a SET is shown in figure 4.3. A small area of semiconductor is isolated from its surroundings by two tunneling barriers. A gate is capacitively coupled to
the island with the intention of modifying the island’s electrochemical potential. Energy band diagram of the SET showing the Coulomb blockade energy that must be overcome to add an additional electron to the quantum dot is shown in the bottom.

![Figure 4.4: (Top) Schematic of the Single Electron Transistor (SET) Structure. (Bottom) Energy band diagram of SET showing Coulomb Blockade energy that must be overcome to add additional electron to quantum dot [30]](image)

**4.3 Coulomb Gap**

Consider a metallic island weakly coupled with two tunneling contacts as shown in figure 4.4.
Assume that the droplet has a continuous energy band. The occupation probability of the energy levels is given by the Fermi-Dirac distribution, $f(E) = \frac{1}{1 + \exp \left( \frac{E-E_F}{kT} \right)}$ where $E_F$ is the Fermi level. The carrier distribution in the droplet is shown in figure 4.5.

At $T=0K$, all the states below $E_F$ are occupied, but as the temperature is increased states within a few $kT$ above $E_F$ are occupied with a probability of $f(E)$ and a few states below $E_F$ are vacant with a probability of $1-f(E)$ as shown in figure 4.5. The states below
EF are referred to as ionization levels as their energy is measured by ejecting electrons from these levels and the levels above EF are referred to as affinity levels as their energy is measured by injecting electrons to these levels. The energy required to eject an electron from the first ionization level is given by \( q^2(N-1)/C \) where N is the total number of electrons in the droplet and C is the capacitance of the droplet. This is because the ejected electron feels potential due to remaining N-1 electrons in the droplet. Similarly, the amount of energy released on adding one electron to the first vacant level above EF is given by \( q^2N/C \). The electron being injected has to overcome the potential due to the N electrons in the droplet. The difference between the first ionization level below EF and the first affinity level above EF, \( q^2/C \), is referred to as the Coulomb gap. The effects of Coulomb gap is seen only when the thermal energy is less than \( q^2/C \). In the case of a droplet with 10nm, the Coulomb gap is less than 26meV and the effect will be observed only at low temperature (figure 4.6).

![Band diagram when the Coulomb gap is significant compared to thermal energy kT](image)

**Figure 4.7:** Band diagram when the Coulomb gap is significant compared to thermal energy kT[30]

For droplets with about 3nm size, it is possible to have a Coulomb gap of about 60meV which is greater than a few kT (self capacitance of the droplet is about 3aF).
Hence it is possible to build single electron transistors which can operate at room temperature by confining the carriers within a quantum dot of less than 3nm size.

### 4.4 Physics of SET

![Schematic of SET](image)

**Figure 4.8: Schematic of SET [31]**

Schematic of an SET is shown in figure 4.7. It consists of a layer of GaAs separated from the gate electrode by a thin barrier layer of insulating AlGaAs. The barrier layer is delta doped with Si which can donate electrons. These delta doped layers can supply electrons to the GaAs channel forming a 2D electron gas at the GaAs/AlGaAs interface. The 2DEG is confined in a direction perpendicular to the GaAs/AlGaAs interface and confinement in the other two directions is achieved by applying a fixed negative potential to the confining electrodes. The gate voltage can be varied to adjust the potential of the confined electrons.

When the gate voltage is increased the potential minimum in which the confined electrons are trapped becomes deeper which causes the number of trapped electrons to increase. However the charge in the trap increases in discrete steps due to Coulomb gap which is reflected in the conductance between source and drain. Figure 4.8
shows the conductance of SET as a function of gate voltage. The conductance is measured by applying a small drain bias such that the current is proportional to $V_{ds}$. As seen in the figure, the conductance increases and decreases by several orders of magnitudes almost periodically in $V_g$. The spacing between the peaks is the voltage required to add one electron to the artificial atom. The name “single electron transistor” comes the observation that the transistor turns on and off every time an electron is added to it.

![Figure 4.9: Conductance of an SET as a function of gate voltage](image)

The energy band diagram of an SET during different operating points is shown below [32]. The applied drain bias is less than the Coulomb gap. Without proper gate voltage the electron tunneling is blocked by the Coulomb Blockade as shown in figure 4.9 and there will not be any tunneling current. On applying enough gate bias to overcome the blockade, the Fermi energy will align with the unpopulated state in the quantum dot, allowing tunneling into the quantum dots as shown in figure 4.10.

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The future research on SETs looks very bright. By using self assembled quantum dots with small size (~3nm), it is possible to fabricate SETs which can operate at room temperature. The study of quantum confinement effects and transport through the quantum dots is very relevant in understanding the physics and operation of these devices.
Quantum dots are regarded as one of the potential candidates for next generation nano electronic devices and photonic devices. The global market for quantum dot technology is expected to increase at a compound annual rate of nearly 91 percent over the next five years, and be worth $721.1 million in 2013. Because of the quantum confinement in three dimensions, they have discrete density of states which results in interesting electrical and optical properties. In the energy space, quantum dots represent a region of low potential surrounded by high potential. Electrons which fall into this quantum box will be confined spatially due to the high potential required to escape. Applications of quantum dots cover a variety of fields including Single Electron Devices, Non-Volatile Memories, Photodetectors, Quantum Computing, Photovoltaics, LEDs, etc. The atomic like energy states of quantum dots give rise to particle-size dependent fluorescence which is harnessed in fabricating optical probes for biological and medical imaging.

In this thesis, the room temperature quantum confinement effects in an array of Silicon (Si) quantum dots embedded in Gadolinium Oxide (Gd₂O₃) rare earth dielectric matrix is reported using photoluminescence (PL) spectroscopy. The high intensity and the small FWHM (0.12eV) of the PL peak indicate high crystalline quality and a narrow size distribution range (1 σ = 0.25nm) of the quantum dots. Electron storage density of 8x10¹² cm⁻² (corresponding to two electrons per quantum dot) is achieved by employing low programming voltage sweeps (-4V to 0V) as validated by the room temperature
capacitance-voltage measurements. A temperature and field dependent study of the transport through the Si dot embedded Gd$_2$O$_3$ MOS tunneling diode structures is also presented. The tunneling mechanism assisted by the confined levels in the quantum dots and oxygen vacancy related trap level in the Gd$_2$O$_3$ dielectric is explained using physics based analytical models. The beneficial effect of forming gas anneal in controlling the trap density is also reported.

This device has potential to be used in nanocrystal flash memory operating at low voltage. Better control of trap density and reducing the size of nanocrystal to about 3nm to allow only one energy level per dot could improve the performance of the device. It would be interesting to further study the Coulomb oscillations and the in-plane transport in coupled quantum dot array device. This could have potential applications for making single electron transistors at room temperature.
REFERENCES


