AMORPHOUS SILICON AND ORGANIC THIN FILM TRANSISTORS
FOR ELECTRONIC APPLICATIONS

A Thesis in
Electrical Engineering

by

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ABSTRACT

Recently, flexible thin film electronics has attracted huge research interest, and as now, many prototypes are being developed and demonstrated by companies around the world, including displays, logic circuit, and solar cells. Flexible electronics offers many potential advantages: it can not only generate new functions like flexible displays or solar cells, also allow very low cost manufacturing through the use of cheap polymeric substrates and roll-to-roll fabrication.

a-Si:H TFT fabrications are compatible with flexible polyimide substrate materials. With the interests in the space environment, for the first time, we tested the performance changes of flexible a-Si:H TFTs, on polyimide substrates, due to irradiation and mechanical stress. Significant changes were found on TFTs after irradiation with fast electrons, which, however, was essentially removed by post-irradiation thermal annealing. On the other hand, few changes were found in TFTs by mechanical stress. These preliminary results indicate that it can be readily engineered for space applications.

Furthermore, for the first time, we designed and fabricated ungated n+ µC-Si and gated a-Si:H strain sensors on flexible polyimide substrates. Compared with commercial metallic foil strain sensors, ungated µC-Si sensors and gated a-Si:H sensors are two orders of magnitude smaller in area and consume two orders or magnitude less power. Integration with a-Si:H TFTs can also allow large arrays of strain sensors to be fabricated.

To take advantage of lower glass-transition-temperature polymeric substrate materials, reduced processing temperature is desired. The 150 ºC low-temperature
deposition process is achieved by using hydrogen dilution in the PECVD process. The TFT performance and bias stability property are tested similar to that of a 250 °C process. These results suggest its viability for practical applications.

For even lower process temperature, we have considered organic TFTs. As a practical demonstration, we integrated pentacene TFTs with OLEDs in a simple display. Pentacene TFT passivation techniques were researched, and a PVA and parylene bilayer structure was used. We designed and demonstrated 48 × 48-pixel active matrix OTFT-OLED displays, and to our best knowledge, they are the largest on glass substrates and the first on flexible PET substrates. Device performance, uniformity and stability are also compared. These results demonstrate that pentacene TFTs are viable candidates for active-matrix OLED displays and other flexible electronics applications.
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Chapter 1

Introduction

1.1 Overview

Over a few decades, crystalline silicon and CMOS technology have been dominating integrated circuit fabrications, and the technology keeps scaling down to increase the density and improve the speed. There is, however, a large market for low-cost, large area electronics where silicon MOSFET is not economical. For those applications, thin film transistors (TFTs) are the technology of choice. Unlike silicon MOSFET, TFTs are field-effect transistors which use a thin film of semiconductor material as the active layer and can be deposited inexpensively on a variety of substrate materials. Today, the largest market for TFTs is flat panel displays. Hydrogenated amorphous silicon (a-Si:H) TFTs currently dominate the display market, functioning as pixel drivers in high information content displays. Currently glass substrates are the most widely used materials. However, the low-cost and large-area fabrications are compatible with arbitrary substrates, such as metal, polymeric film, cloth, and even paper sheets, among them, the most promising one is flexible polymeric substrates.

Recently, flexible electronics has attracted huge research interest and as now, many prototypes are being developed and demonstrated by companies around the world, including displays, logic circuits, and solar cells. Although conventional electronic substrates such as semiconductor wafers and glass plates have many desirable properties
for device processing, their inherent physical characteristics can limit possible applications. However, the flexible substrates, unlike rigid, brittle, heavy, and bulky inorganic substrates, are mechanically rugged, thin, and lightweight, and they potentially promise many new applications. In addition, their use will be more cost effective due to use of cheap polymer substrates and roll-to-roll fabrications.

1.2 Research Objective and Thesis Organization

This thesis will discuss some flexible electronic applications using a-Si:H and pentacene thin film technologies. First we will introduce some background knowledge in Chapter 2, which includes basic physics of a-Si:H TFTs, the process on polyimide substrates, and previous work of pentacene organic TFTs.

Chapter 3 covers the flexible a-Si:H thin film electronics for space applications. Irradiation and mechanical tension induced changes are discussed on flexible a-Si:H TFTs. Then, ungated n+ μC-Si and gated a-Si:H strain sensors were developed on 50μm thick polyimide substrates. The sensitivity of both types of stain sensors is extracted, and these sensors are compared with metallic foil strain sensors in terms of area and power consumption. By adding hydrogen dilution, the temperature for the a-Si:H TFT process was lowered from 250 °C to 150 °C, and device performance in stability was compared.

Chapter 4 discusses the passivation issue for pentacene OTFTs. Despite of mobility and threshold voltage preservation, the moisture trapped in PVA degrades sub-threshold performance of pentacene TFTs. In OLED applications, the moisture will further harm OLED lifetime. Inorganic material like RT PECVD SiN and organic
material like parylene have been used to directly passivate pentacene OTFTs. The passivation results are compared and degradation mechanisms are analyzed. Finally, we solved the problem by using a PVA and parylene bilayer structure.

In Chapter 5, we cover the design, fabrication, and performance of pentacene OTFT driven 48 × 48-pixel AM OLED displays on both glass and PET substrates. The pentacene OTFTs were characterized in terms of their performance, uniformity and stability on the backplanes. To our best knowledge, the demonstrations are the largest OTFT driven AM OLED on glass substrates and the world’s first on flexible PET substrates.

Chapter 6 provides conclusions for this thesis work and a brief discussion of future work on these topics.
Chapter 2

Background on Flexible Thin Film Transistors

2.1 Flexible Substrates

Although conventional electronic substrates such as semiconductor wafers and glass plates have many desirable properties for device processing, their inherent physical characteristics can limit possible applications. However, the flexible substrates, unlike rigid, brittle, heavy, and bulky inorganic substrates, are mechanically rugged, thin, and lightweight, and they have the potential for many new applications.

Recently, flexible electronics has attracted huge research interest, and as now, many prototypes are being developed and demonstrated by companies around the world, including displays, logic circuits, and solar cells. Flexible electronics offers many potential advantages: it not only can generate new applications, it also will be cost effective due to the use of cheap polymer substrates and roll-to-roll fabrications.

To enable the flexible electronics, a flexible substrate must be used to replace the conventional rigid substrate, which can be thin glass, stainless steel foil, or polymeric film. Compared with the fabrications on rigid substrates such as glass plates and semiconductor wafers, the semiconductor fabrication on flexible substrates has many process challenges, such as mechanical strength, sample cleaning, thermal management, chemical resistance, surface properties, and process compatibility. Depending on the
applications, some of the requirements will determine the substrate choice, and there may be multiple choices for some applications.

However, we believe polymeric substrates will be the ultimate choice. We have fabricated a-Si:H thin film transistors (TFTs) on flexible polyimide substrates and pentacene organic TFTs on polyethylene naphthalate (PEN) and polyethylene terephthalate (PET) films. The substrate choices are mostly based on the process temperature and compatibility.

2.2 a-Si:H TFTs

Since Spear and LeComber showed that hydrogenated amorphous silicon (a-Si:H) could be doped by adding phosphine or diborane [1], and since the first solar cell device was demonstrated by Carlson and Wronski in 1976 [2], research in a-Si:H technology has led to a wide variety of applications. In addition to exploitation of its photosensitive properties for photovoltaics, a-Si:H has been used as a switching device in large area electronics such as solid state imagers, electronic copiers, printers, scanners, and flat panel displays [3]. These applications typically use a-Si:H as the semiconducting material in a TFT to provide the switching element. To date, a-Si:H TFT has been the second leading semiconductor in terms of revenue simply because of widely used flat panel display. The primary reason for the success of a-Si:H is because of its ability to be deposited at relatively low temperatures and on very large area substrates. The low process temperature (typically 250-300 °C) allows low-cost glass substrates to be used. In addition, the ability to deposit a-Si:H over very large areas (> 3 m diagonal mother panels
are common) with sufficient uniformity is a major advantage because of the increasing demand for larger displays.

2.2.1 Physics of Amorphous Silicon

Amorphous silicon retains the basic tetrahedral bonding structure found in crystalline silicon; however, it lacks long-range order due to deviations in bond lengths and angles [4]. This bonding disorder, along with bonding defects created by vacancies, causes the electronic properties to vary from those of the crystalline material. The defects, known as “dangling bonds”, cause the Fermi level to be pinned. Also, a scattering and trapping of carriers occurs, which severely degrades the carrier mobility of materials. By incorporating hydrogen into the film, the “dangling bonds” are passivated, mostly in the form of Si-H bonds, and the density of defect states is reduced from $\sim 10^{19}$ cm$^{-3}$ to $\sim 10^{16}$ cm$^{-3}$ [5].

The electrons and holes have a scattering length of about an inter-atomic spacing, and consequently a free carrier mobility of only about 10 - 20 cm$^2$/V-s compared to 1350 cm$^2$/V-s in crystalline silicon. Perhaps more significantly, the disorder causes an exponential tail of localized states at the band edges, extending into the forbidden gap. The energy dividing the extended and localized state is known as the mobility edge. An illustration of the density of states and energy band diagrams is shown in figure 2-1.
Conduction of both electrons and holes occurs near the mobility edges, but involves frequent trapping and release from these localized states; consequently, the effective carrier mobility is further reduced and is also thermally activated. It turns out that the conduction band tail is narrower than the valence band tail, so that electrons have a much higher mobility than holes. Table 2-1 lists some of the key electronic parameters.

Table 2-1: Typical material parameters for a-Si:H. The exact values depend on the detail of the deposition conditions.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Electron drift mobility</td>
<td>1 cm²/V-s</td>
</tr>
<tr>
<td>Hole drift mobility</td>
<td>0.003 cm²/V-s</td>
</tr>
<tr>
<td>Optical band gap</td>
<td>1.8 eV</td>
</tr>
<tr>
<td>300K conductivity (undoped)</td>
<td>$10^{-11} \Omega^{-1} cm^{-1}$</td>
</tr>
<tr>
<td>Hydrogen concentration</td>
<td>10 at. %</td>
</tr>
</tbody>
</table>

Despite the large amount of bonded hydrogen, undoped a-Si:H retains about $10^{16}$ cm⁻³ dangling bond defects, which form electronic states near the middle of the band gap. These defects control the trapping and recombination of carriers. In doped material the
defect density increases by 2 - 3 orders of magnitude. For this reason, doped layers are primarily used for junctions rather than active layers. Hence, the channel of the TFT is undoped.

Hydrogen is essential for the good electronic properties of a-Si:H but does have some adverse effects. Light induced defect generation was discovered early in the studies of a-Si:H solar cells [2], and this causes the solar cell efficiency to decrease slowly by 10 – 20 % over many days of exposure. The mechanism of defect generation has to do with the breaking of Si-H bonds by the energy of electron-hole recombination.

2.2.2 Fabrication Process

Kapton® film is chosen as the polymeric substrate for a-Si:H thin film in our group at Penn State. Kapton® is a high performance polyimide and has a semi-clear, yellowish-brown appearance. The complete aromatic structure provides excellent temperature stability and chemical resistance. Kapton® polyimide is also a space-qualified material and is highly resistant to radiation [6]. It has been successfully employed in applications at temperatures ranging from –269 °C to 400 °C. In addition, Kapton® has a very small coefficient of thermal expansion (CTE = 12×10^{-6}/°C), which is quite useful for device processing at high temperature.

50-µm thick Kapton® E polyimide film was used as the flexible substrate. The substrate was first heated at 250 °C for 24 hours under vacuum to reduce the level of moisture and volatile contaminants, as well as to pre-shrink the material for improved thermal dimensional stability prior to the TFT processing. For ease of handling during
device fabrication, the film was mounted on a glass carrier with a silicone-based, pressure
sensitive adhesive [7]. The adhesive allows the substrate to be readily released from the
rigid carrier by a simple peel-off following fabrication.

Figure 2-2: (a) Cross-section and (b) top view of the a-Si:H TFT.

Figure 2-2 shows the cross-section and top view of the a-Si:H TFTs fabricated on
Kapton® polyimide substrates. Before the deposition, the Kapton® surface was treated by
reactive ion etch (RIE) oxygen plasma for 5 minutes to improve the adhesion. Gate
electrodes for the devices were patterned by standard photolithography and wet etching
techniques from a 75 nm thick film of chromium deposited by thermal evaporation. A tri-
layer stack comprised of a silicon nitride (SiN) gate dielectric layer (300 nm), an intrinsic
a-Si:H active layer (50 nm), and a SiN passivation layer (300 nm) was then deposited
using a three chamber load-lock plasma-enhanced chemical vapor deposition (PECVD)
system with a maximum temperature of 250 °C. The top SiN layer was patterned by
photolithography and diluted buffered oxide etch (BOE) wet etching and the intrinsic a-
Si:H was patterned by KOH wet etching using top SiN as an etching mask. Then the
bottom gate dielectric SiN layer was patterned by another step of photolithography and
diluted BOE wet etching. After that, a 50 nm n-type microcrystalline silicon (n+ µC-Si)
contact layer was deposited at 250 °C using PECVD, and 200 nm thick molybdenum (Mo) source/drain contact electrodes were deposited by DC sputtering. The Mo contact electrodes were patterned by a combination of CF$_4$ RIE and wet etching in Mo etch (HNO$_3$:H$_3$PO$_4$:DI H$_2$O = 1:6:9). The n$^+$ μC-Si layer was patterned by chlorine based plasma dry etch using Mo as a mask. Finally, the polyimide film was peeled off the glass carrier and ready to test.

Figure 2-3 shows the typical a-Si:H TFT characteristics on glass and polyimide substrates. Apparently, the devices on glass and polyimide show very close performance.

![Figure 2-3: Typical a-Si:H TFT characteristics on glass and polyimide substrates.](image)

2.3 Pentacene OTFTs

2.3.1 History

Since the first report of a TFT with an organic semiconductor as the active layer came in 1983, many early investigations of organic TFTs were centered on long-chain
organic molecules or polymers, like polyacetylene and polythiophene, which showed saturation field-effect mobility of up to $10^{-4} \text{ cm}^2/\text{V} \cdot \text{s}$ and on/off current ratio of up to $10^5$ [8-10]. Most polymer films, however, do not have strong crystal forming tendencies and are typically not well ordered. Polymer semiconductor films typically have low carrier mobility as a result of this lack of order in the films. Short-chain organic molecules or small molecules have shown better performance. These materials tend to form well-ordered molecular crystals and typically show improved intermolecular transport compared to polymers through increased $\pi$-orbital overlap between adjacent molecules.

In the late 1990s, the first organic TFTs with useful field-effect mobility were reported using optimized alpha-sexithienyl ($\alpha$-6T). These organic TFTs had field-effect mobility in the $0.1 - 0.2 \text{ cm}^2/\text{V} \cdot \text{s}$ range and on/off current ratio as large as $10^7$ [11-13]. The demonstration of a mobility of $0.1 \text{ cm}^2/\text{V} \cdot \text{s}$ revealed the potential for organic TFTs in commercial applications and generated a significant amount of research interest.

To date, the best overall performance observed for organic TFTs is with the active layer of the small molecule pentacene. Our group at Penn State has reported pentacene active layer organic TFTs with field-effect mobility $> 2.0 \text{ cm}^2/\text{V} \cdot \text{s}$, on/off current ratio of $10^8$, and sub-threshold slope as low as 0.6 V/decade [14-16]. Researchers at 3M, University of Minnesota, Bell labs and Samsung Corporation have fabricated similar or better performance devices in recent years; as a result, pentacene has become the most extensively studied organic semiconductor material.
2.3.2 Pentacene Thin Film

The large field-effect mobility observed in organic TFTs with thermally evaporated pentacene active layers is attributed to a high degree of molecular ordering in the films [17]. Molecular ordering has also been reported to play a large role in other organic TFT materials with good performance such as α-6T [18]. Carrier transport in the field-induced channels in pentacene and other organic semiconductors is most likely dominated by the difficulty in moving carriers from one molecule to the next and across grain boundaries. A high degree of molecular ordering, which leads to better π-orbital overlap, is expected to improve inter-molecular transport.

Pentacene is an aromatic hydrocarbon consisting of five benzene rings fused together in a row. Due to the asymmetry of the molecule, pentacene has a low-symmetry triclinic crystal structure. The molecular structure of pentacene is shown in figure 2-4. Normally, as-purchased pentacene is not electronic grade material; therefore, it must be purified in our laboratory by temperature gradient vacuum sublimation. The process is repeated to maximize purity [15]. Purification of the pentacene material is important for obtaining low off-state leakage currents and large on/off current ratios.

![Pentacene molecular structure](image)

Figure 2-4: Pentacene molecular structure.

Both X-ray diffraction and Atomic Force Microscopy (AFM) images are used to characterize the molecular ordering of pentacene films deposited on silicon dioxide over
a wide range of substrate temperatures (20 °C – 120 °C). Figure 2-5a shows X-ray diffraction pattern (CuK radiation with the diffraction vector aligned perpendicular to the substrate surface) for a pentacene film with 1500 Å average thickness deposited at a rate of 2 - 3 Å/s onto a thermally oxidized silicon substrate held at 60 °C during deposition [15]. The family of peaks corresponds to a spacing of the structure of single crystal pentacene [19]. Figure 2-5b shows an AFM image of an evaporated pentacene film on an oxidized silicon substrate. Terracing of the grain surface is visible, with a typical terrace height of ~ 15 Å, roughly corresponding to the length of the long axis of the pentacene molecule. These results indicate that pentacene films evaporated onto silicon dioxide substrates at elevated temperature are highly ordered, with the long axis of the molecule nearly perpendicular to the substrate.

Figure 2-5: (a) X-ray diffraction pattern of pentacene thin film on thermal oxide; (b) AFM image of pentacene on thermal SiO$_2$. 
2.3.3 Bottom and Top Contact Structures

Normally, we start with putting metal gate and gate dielectrics on substrates when we build our TFTs. Then the semiconductors and source/drain metal layers are deposited on top. When the source/drain metal contacts are patterned on top of organic semiconductors, we refer to them as top contact device structures; otherwise, they are called bottom contact device structures. Figure 2-6a shows a simple version of top contact pentacene OTFT using a heavily doped silicon wafer as the gate electrode and substrate and thermal oxide as the gate dielectric. Figure 2-6b shows bottom contact device structure. These device configurations are favorable for organic semiconductor characterizations and early demonstrations because they provide the convenience of gate and gate dielectric and substrate material.

![Cross-section of a top and bottom contact pentacene TFT](image)

Figure 2-6: Cross-section of a (a) top and (b) bottom contact pentacene TFT.

The top contact structure usually has better contact effect from source-drain metal electrodes to organic semiconductors and shows higher field-effect mobility. Although there are reports on top contact achieved by the stamping soft lithography method [20], they are mostly realized in the method of evaporation through shadow masks. Like most small molecule organic semiconductors, pentacene is sensitive to photoresist developers
and organic solvents found in normal photolithography process. The exposure of the pentacene active layer to common organic solvents has been shown to cause severe degradation in device performance as a result of a solvent-induced phase transition in the pentacene film [21]. TFTs for practical applications will require a more complex device structure with photolithographically patterned metal contacts. As a result, only bottom contact device structures are used for photolithographically patterned devices.

### 2.3.4 Gate Dielectric Surface Treatment

Pentacene TFT performance improves significantly when the silicon dioxide gate dielectric surface is treated with the silane coupling agent octyldecyltrichlorosilane (OTS) prior to active layer deposition [22]. The substrate and OTS solution are placed in a vacuum oven, allowing the OTS to form a self-assembled monolayer on the silicon dioxide surface. This treatment lowers the surface energy of the silicon dioxide, which is expected to allow for improved molecular ordering that ultimately leads to improved $\pi$-orbital overlap. Pentacene TFTs with OTS treated silicon dioxide gate dielectric typically show a factor of 2 to 3 improvement in saturation field-effect mobility over untreated silicon dioxide, as well as improved sub-threshold slope. OTS treated top contact pentacene TFTs have been reported with organic TFT mobility as large as 2.1 cm$^2$/V·s [14].
### 2.3.5 Pentacene TFTs on Glass or Plastics

Although the previous device structures were useful for early demonstrations, they are impractical for most real-world applications because they share the common gate electrode and gate dielectric. More complex device structures in which the gate electrodes, gate dielectric, and source and drain contacts are deposited and patterned photolithographically are required for the fabrication of integrated circuits or display backplanes. Pentacene TFTs on glass and PEN substrates have also been demonstrated in our labs [16, 23]. Figure 2-7 shows the cross-section of a photolithographically patterned bottom contact pentacene TFT on a glass or polymeric substrate.

![Diagram of pentacene TFT](image)

Figure 2-7: The cross-section of a PVA patterned pentacene TFT.

50nm Nickel gate electrodes are deposited by sputtering, and they are patterned by wet etching. 300nm silicon dioxide gate dielectric was deposited by a reactive ion-beam sputtering system and patterned by lift-off. 100nm palladium source and drain contacts were deposited by ion-beam sputtering and patterned using lift-off. Then 50nm pentacene thin film is deposited by thermal evaporation after an OTS vapor treatment of the oxide gate dielectric. To avoid exposure of the pentacene film to harmful organic solvents during patterning, the water-soluble polymer polyvinyl alcohol (PVA) was used as the photoresist, and field pentacene was removed by RIE O$_2$ plasma dry etching [23]. After
pentacene patterning, as shown in figure 2-8, the TFTs often show $\sim$ pA off current and $>1.0\ \text{cm}^2/\text{V} \cdot \text{s}$ field-effect mobility. However, the sub-threshold slope was often degraded, and a knee-shaped curve usually happened in the sub-threshold region in the log of drain current versus gate-source voltage characteristic. This is most likely due to residual moisture in the film and/or at the interface, but we don’t understand the mechanism. This slow turn-on characteristic will increase the voltage needed for the circuit.

![Graph](image)

Figure 2-8: Typical bottom contact pentacene TFT characteristics after PVA patterning: (a) $I_D$ vs $V_{GS}$; (b) $I_D$ vs $V_{DS}$. 
Chapter 3
Flexible Substrate a-Si:H Thin Film for Space Applications

3.1 Introduction

Recently, there has been growing interest in the fabrication of hydrogenated amorphous silicon thin film transistors (a-Si:H TFTs) on flexible substrates, and most efforts have been focused on potential commercial applications, such as flexible displays, image sensors or detectors and electronic textiles [24-27]. Electronically active deployable space structures are another application that can benefit from the light weight, large area, and rollable or foldable characteristics of a-Si:H thin film on flexible substrates [28-31]. For example, a large-area deployable synthetic aperture radar antenna array can be made on flexible substrates to fit in a standard launch vehicle [32]. The structures can be constructed to stow with size much smaller than that of the fully deployed application, and at the appropriate time following launch, a variety of deployment mechanisms can be used to bring the application to its operational configuration. There is a need to integrate sensing and control electronics within the structure. However, conventional silicon-based electronics are difficult to integrate with such large, thin structures, due to a variety of concerns including mass, reliability, and manufacturing issues. Flexible a-Si:H TFTs and thin films are potentially one of the key enabling technologies that may allow the integration of a wide range of sensors and actuators into these types of structures [33].
There are several technical challenges to the successful use of flexible substrate a-Si:H TFTs in space applications. The devices must withstand the harsh space environment, including radiation exposure and mechanical stress, without requiring massive and/or rigid shielding during deployment and operation. Our work is focused, therefore, on addressing the critical aspects of device reliability in relevant simulated space environments, particularly with regard to radiation. There were previous studies that demonstrated radiation-damage resistance of a-Si:H photodiodes from medical X-Ray radiation conditions [34] and a-Si:H thin film solar cells from space radiations [35, 36]. Previous studies with ionizing radiation have also been performed with X-ray [37, 38] and protons [39] for a-Si:H TFTs. These studies examined the transfer characteristics of a-Si:H TFTs after various doses of radiations. However, all these previous works were based on the devices fabricated on rigid substrate materials, for example, quartz and glass substrates. For space applications, the radiation-damage resistance property needs to be re-examined for flexible a-Si:H TFTs. We explored the fast electron radiation effect on flexible polyimide substrate a-Si:H TFT performance. In addition, elevated-temperature annealing of the induced radiation damage is examined. The radiation damage mechanisms are also discussed.

After the launch, the structure will expand to its designed shape. To guarantee the proper expansion during deployment and good shape maintenance during its operation, shape sensors / strain sensors are needed on the structures. We designed and fabricated ungated doped microcrystalline silicon (µC-Si) strain sensors and gated a-Si:H strain sensor on polyimide substrates, and we then compared them with conventional metallic foil strain sensors in terms of geometry, sensitivity, and power consumption.
a-Si:H TFTs fabricated on flexible substrates are of interest for applications in light weight, rugged, and flexible electronics. As of now, most of them are using either stainless steel foil or polyimide substrates such as Kapton® from Dupont Company due to the high process temperature. However, Kapton® is a yellowish colored plastic, which limits its applications to displays. To take advantage of clear transparency and accommodate low-cost commercially available polymeric substrates, like PEN and PET, fabrication temperatures less than about 150 °C are desired, significantly lower than what is typically used for fabrication on glass substrates (>250 °C). Both Wagner’s group in Princeton University and Nathan’s group in University of Waterloo have done a great deal of work on low temperature a-Si:H TFT process [1,2]. However, the stability of the devices is also critical.

3.2 Irradiation and Mechanical Stretching Effect

3.2.1 Sample Fabrication

a-Si:H TFTs are fabricated on 2" × 2" Kapton® E polyimide substrates, and figure 3-1 shows the cross-section drawing and microscopic view of a-Si:H TFT. For detailed substrate preparation and sample fabrication processes, see section 2.2.2. The channel length (L) and width (W) of the devices we used in this study were 24 µm and 40 µm, respectively. After sample fabrication, the Kapton® film is peeled off from the glass carrier and silicon gel for testing.
3.2.2 Fast Electron Irradiation and Thermal Anneal

3.2.2.1 Experimental Conditions

An array of 30 a-Si:H TFTs on a polyimide substrate was evaluated in this study. The a-Si:H TFTs were irradiated with 1 MeV fast electrons at the Jet Propulsion Laboratory (JPL) Dynamitron facility, with total doses up to 1 Mrad (Si). Devices were probed before and after irradiation with an Agilent 4156B Semiconductor Parameter Analyzer, and device characteristics, including saturation field-effect mobility ($\mu_{\text{sat}}$), linear field-effect mobility ($\mu_{\text{L}}$), threshold voltage ($V_T$), and sub-threshold slope (S) were extracted from the electrical data. Saturation mobility was determined from the slope $d\sqrt{I_{ds}/dV_{GS}}$ at $V_{DS} = 20V$, and threshold voltage was determined by extrapolating that slope line to $I_{DS} = 0$. Linear mobility was obtained from the slope $dI_{DS}/dV_{GS}$ at $V_{DS} = 0.1V$. Following initial characterization of the irradiated devices, they were thermally annealed at 200°C on a hotplate for two hours, and then they were re-measured.
\subsection*{3.2.2.2 Results and Discussion}

After the measurement before radiation, TFT characteristics were extracted from their transfer curves. The typically device shown characteristics with threshold voltage ($V_T$) of 3.9 V, saturation field-effect mobility ($\mu_{\text{sat}}$) of 0.70 cm$^2$/Vs, Linear field-effect mobility ($\mu_L$) of 0.67 cm$^2$/V-s, sub-threshold slope ($S$) of 0.5 V/Dec, and off-current less than 1 pA. The 30 TFTs measured shown a relatively uniform performance and Table 3-1 shows the statistics in terms of $V_T$, $\mu_{\text{sat}}$, $\mu_L$, and $S$ for all devices.

\begin{table}[h]
\centering
\begin{tabular}{|c|c|c|c|c|}
\hline
 & $V_T$ (V) & $\mu_{\text{sat}}$ (cm$^2$/Vs) & $\mu_L$ (cm$^2$/Vs) & $S$ (V/Dec) \\
\hline
Mean & 3.80 & 0.70 & 0.67 & 0.52 \\
Standard deviation & 0.50 & 0.08 & 0.11 & 0.05 \\
Standard error & 0.10 & 0.01 & 0.02 & 0.01 \\
\hline
\end{tabular}
\caption{Statistics of TFT performance before radiation.}
\end{table}

After 1 Mrad (SI) total dose of 1 MeV fast-electron exposure, two TFTs were completely inoperable. Although this may have been due to the effect of the radiation dose, the performance of the remaining devices suggests the devices that failed were compromised during substrate handling or device probing. The remaining 28 TFTs had radiation-induced device changes, but showed good transistor action before and after irradiation. All 28 working devices had off-current below 1 pA both before and after irradiation and after thermal anneal.

The $V_T$ change data are calculated by post-irradiation threshold voltage minus pre-irradiation values. Figure 3-2 plots the histogram of the $V_T$ changes of these devices after irradiation and after post-irradiation thermal annealing. The distribution data after radiation is expressed in a histogram with each bucket width of 1 V. Histogram
distribution is used because the data are sparse from -7 V to 4 V and are hard to express in a simple statistic equation. Nonetheless, there are two groups of devices: one with large negative $V_T$ shifts and the other with un-changed or slightly positive mean-value $V_T$ shifts. After post-irradiation thermal annealing, all devices recovered their $V_T$ almost to the pre-irradiation value. Since the $V_T$ shifts data are so small and close, they are expressed in the form of a normal distribution with mean value of -0.32 V, standard deviation of 0.32 V, and standard error of 0.06 V.

![Figure 3-2](image)

**Figure 3-2:** The distribution of threshold voltage changes for all devices after irradiation and thermal annealing.

**Figure 3-3** shows the distribution of the $\mu_{\text{sat}}$ changes of these devices after irradiation and after post-irradiation thermal annealing. Similar to $V_T$ shifts, $\mu_{\text{sat}}$ change data after the irradiation are expressed in the form of a histogram with each bucket width of 0.05 cm$^2$/Vs, which spans from -0.10 cm$^2$/Vs to 0.25 cm$^2$/Vs. But in general, the $\mu_{\text{sat}}$ changes tend to be positive. After post-irradiation thermal annealing, all devices recovered their $\mu_{\text{sat}}$ almost to the pre-irradiation value. The $\mu_{\text{sat}}$ changes are expressed in
the form of a normal distribution with mean value of -0.03 cm²/ Vs, standard deviation of 0.028 cm²/ Vs, and standard error of 0.005 cm²/ Vs.

Figure 3-3: The distribution of saturation field-effect mobility changes for all devices after irradiation and thermal annealing.

Figure 3-4 shows the distribution of the μ_L changes of these devices after irradiation and after post-irradiation thermal annealing. Generally the devices only show the slightest changes in terms of μ_L. Since the μ_L changes are so small, they are both expressed in the form of normal distribution in Figure 3-4. After radiation, device μ_L changes show a mean value of 0.03 cm²/ Vs, a standard deviation of 0.029 cm²/ Vs, and standard error of 0.005 cm²/ Vs. After post-irradiation thermal annealing, the μ_L changes show a mean value of -0.006 cm²/ Vs, a standard deviation of 0.028 cm²/ Vs, and standard error of 0.005 cm²/ Vs. The μ_L changes are so small that we can basically neglect the changes in the μ_L from the irradiation and thermal anneal.
Figure 3-4: The distribution of linear field-effect mobility changes for all devices after irradiation and thermal annealing.

Figure 3-5 shows the distribution of the S changes of these devices after irradiation and after post-irradiation thermal annealing. In general, all devices increase S values after the radiation and recover to their original values after the thermal anneal. Again, S change data after the irradiation are expressed in the form of a histogram with each bucket width of 0.1 V/Dec, which spans non-uniformly from 0.2 V/Dec to 1.5 V/Dec. After post-irradiation thermal annealing, all devices recovered their S almost to the pre-irradiation value, and the S changes are expressed in the form of a normal distribution with mean value of -0.005 V/Dec, standard deviation of 0.07 V/Dec, and standard error of 0.013 V/Dec.
Our data show that $\mu_L$ was relatively unaffected by both radiations and thermal anneals. Since $\mu_L$ is particularly sensitive to changes in device source resistance (including contact resistance), our data suggest that the irradiation did not result in significant changes in the n+ doped $\mu$C-Si contact layers and interfaces.

Generally, the irradiation had a significant effect on a-Si:H TFTs in terms of characteristic changes. Although $\mu_L$ is almost unchanged, all devices show obvious changes in $V_T$, $\mu_{sat}$, and $S$. All devices, however, recovered within $\pm 5\%$ of its original value after post-radiation thermal anneal. There are two degradation mechanisms of a-Si:H TFTs commonly reported: (1) charge trapping in the gate dielectric insulator [37] and (2) trap state creation in a-Si:H at the semiconductor and insulator interface [40]. For the first one, incident radiation initially creates electron-hole pairs and more mobile electrons are easier to reach the electrodes, thereby leaving a net excess of holes, which
then act as fixed positive charge centers in the dielectric layer. The fixed positive charges will primarily act to decrease TFT $V_T$. The creation of defect states at semiconductor and insulator interface arise from the generation of dangling bonds by breaking of weak Si-Si bonds or Si-H bonds. The creation of dangling bond defect states, which can trap charge carriers in the intrinsic a-Si:H layer, usually result in an increase in $V_T$ and $S$.

The two damage mechanisms discussed above can mostly explain the effect of radiation on our devices. The increases in $S$ suggest that a-Si:H active layer deep state density is increased or that the state distribution is broadened by irradiation. The recovery of the initial value of sub-threshold slope, after post-irradiation annealing, suggests that the dangling bond deep states become passivated for the most part.

As shown in above figures (Figure 3-2 to Figure 3-5), the overall irradiation-induced changes observed for the flexible substrate a-Si:H TFTs can be grouped in two types. Type I shows an increase in $\mu_{sat}$, a very small change in $V_T$, and a significantly increased sub-threshold slope after irradiation. The major irradiation-induced changes for this group occur in the a-Si:H active layer, most likely creating deep density states in the energy gap. Figure 3-6 shows typical device characteristics for this type after fabrication, radiation, and thermal anneal. The change in sub-threshold slope suggests that a-Si:H active layer deep state density is increased by irradiation. The increase in the density of deep states also results in the slight increase in device $V_T$. The increase in $\mu_{sat}$, however, suggests a decrease in the density of the band tail states. This phenomenon, in which the sharpening of the band tail slope leads to an increase in $\mu_{sat}$, has also been seen in the bias-stress test of a-Si:H TFTs [41] and is consistent to the speculation of moving states from band tail to deep mid gap region.
Type II shows a large negative shift in $V_T$, and a slight increase in both $S$ and $\mu_{\text{sat}}$ after irradiation. The major irradiation-induced changes for this group occur in the SiN dielectric layer, most likely due to creating of fixed positive charges in the bottom and top SiN dielectrics. Figure 3-7 shows typical device characteristics for this type after fabrication, radiation, and thermal anneal. The large negative shift in $V_T$ suggests that fixed positive charge traps in dielectrics were created by irradiation. The slight increase in $S$ suggests a very small increase in the density of deep states in the energy gap. The slight increase in $\mu_{\text{sat}}$, however, may not necessarily be attributed to the decrease in the density of the band tail states as in Type I devices. Instead, the larger $(V_G-V_T)$ number, due to the negative shift of $V_T$, simply gives rise to a higher ratio of mobile carriers to gate-induced charges. As a result, the effective $\mu_{\text{sat}}$ increases slightly.
Figure 3-7: Type II TFT characteristics: (a) $I_D$ vs $V_{GS}$ at $V_{DS}=20V$ before, after irradiation, and after anneal; (b) $I_D$ vs $V_{DS}$ before, after irradiation, and after anneal.

Apparently, in some irradiated TFTs, one effect dominates, and in others, the two effects combine. It is not clear why different devices appear to have different dominant irradiation-induced effects and some devices appear to have mixed effects, considering a relatively uniform irradiation. However, irradiation-induced changes for both groups, and for devices with mixed effects, are recovered within a ±5% of their original values, by modest post-irradiation annealing.

3.2.3 Mechanical Stretching Effect

Electronics integrated within the flexible structures experience various forces during deployment (e.g., unrolling and tensioning) or operation, raising the concern of mechanical stress related device failure. For example, devices experiencing prolonged tensioning may fail due to the influence of creep and/or delamination of films. To simulate a tensioning of a membrane structure, unidirectional tensile testing was done using an Instron 1331 load frame. Figure 3-8 shows a schematic of the stretching test.
The sample substrate was clamped on the edges and a 10-pound load was applied for one hour, corresponding to a uniaxial in-plane tension of about 2500 PSI.

Figure 3-8: Schematic drawing showing mechanical stretching tests structure. The 2500-PSI uniaxial stress is applied and held on sample substrate for one hour.

An array of 20 a-Si:H TFTs were characterized before and after application of the tension. Table 3-2 summarizes the test results. Two of the 20 devices were inoperable following application of the tension, most likely because of handling or probing damage. Figure 3-9 (a) and (b) show the threshold voltage and saturation field-effect mobility before and after stretching. And Figure 3-10 shows sub-threshold slope comparison of devices between pre- and post-stretching. About 70% of the working devices showed only minor changes in device characteristics. A few devices showed somewhat larger changes. Figure 3-11 shows the typical device characteristics before and after the stretching. These results suggest that mechanical tensioning need not cause significant changes in devices on flexible substrates, but that additional optimization, particularly of the high-modulus devices structure on a low-modulus substrate, may be useful.
Table 3-2: TFT characteristics before and after stretching.

<table>
<thead>
<tr>
<th>TFT Number</th>
<th>Before stretching</th>
<th>After stretching</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Mobility (cm²/Vs)</td>
<td>Threshold voltage (V)</td>
</tr>
<tr>
<td>1</td>
<td>0.5763</td>
<td>4.4</td>
</tr>
<tr>
<td>2</td>
<td>0.7469</td>
<td>5.3</td>
</tr>
<tr>
<td>3</td>
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<td>3.2</td>
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<td>4</td>
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</tr>
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<td>5</td>
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<td>4.8</td>
</tr>
<tr>
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<td>4.1</td>
</tr>
<tr>
<td>7</td>
<td>0.6125</td>
<td>6.2</td>
</tr>
<tr>
<td>8</td>
<td>0.7701</td>
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</tr>
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<tr>
<td>20</td>
<td>0.4970</td>
<td>6.5</td>
</tr>
</tbody>
</table>

Figure 3-9: (a) the threshold voltages and (b) field-effect mobility of devices before and after the mechanical stretching.
Figure 3-10: The sub-threshold slopes of devices before and after the mechanical stretching.

Figure 3-11: Typical TFT characteristics before and after mechanical stretching: (a) $I_D$ vs $V_{GS}$ at $V_{DS}=20V$; (b) $I_D$ vs $V_{DS}$.

3.2.4 Summary

Irradiation and mechanical tension induced changes were evaluated for arrays of a-Si:H TFTs on Kapton® polyimide substrates. Significant changes were found on TFTs after irradiation with fast electrons at a dose of 1 Mrad. However, the irradiation-induced
changes were essentially removed by post-irradiation thermal annealing at 200 °C for two hours. Few changes were observed for TFTs after a substrate tension of about 2500 psi. These results indicate that flexible substrate a-Si:H TFTs can be readily engineered to survive the mechanical stresses of space deployment and may survive fast electron irradiation with minor changes in device characteristics.

3.3 Flexible Strain Sensors

After the structure expands in space during the deployment or the operation, the shape of the structure needs to be known in order to fulfill its normal function. Therefore, a flexible strain/shape sensor is required to be integrated in the whole structure, which in turn requires the sensor to be flexible, light weight and to have low-power-consumption. Also, mechanical strain and stress are very important physical parameters in various applications, such as shape, strain, and force monitoring applications. Currently, metallic foil and rigid substrate semiconductor piezo-resistors are most often used as strain sensing elements. Emerging applications like smart hands in robotics [42], flexible sensing arrays in aeronautics [43], and novel diagnostics and surgery [44-46], have strict requirements on sensor size, power consumption and reliability, or flexibility.

Typically, as figure 3-12 shows, strain sensors use resistors connected in a Wheatstone bridge configuration and mounted on the surface of the body to be tested. A resistance change, which is normally caused by either geometric change or resistivity change induced by applied mechanical strain or stress, unbalances the bridge, thereby
resulting in a differential output voltage from two orthogonal contacts (V+ and V-). The benefit of the Wheatstone bridge is to measure very small relative change in resistance.

Metallic foil strain sensors, typically with a gage factor of 2-5, take advantage of geometry-induced strain and are available on flexible substrates; however, they are normally large in size due to the long serpentine resistors required. Unfortunately they also have high power consumption. Semiconductor sensors, for example crystalline silicon, can provide good strain sensitivity, with a gage factor of about 50-150, with significantly reduced sensor area and also reduced bridge power consumption; however, they normally require rigid substrates. Cesare, et. al. have demonstrated ungated a-Si:H thin film shear strain sensor on glass substrate with good linearity and direction discrimination [47]. However, the rigid substrate is a limitation for many applications.

![Wheatstone Bridge Diagram](image)

Figure 3-12: Schematic drawing of Wheatstone bridge.

For the first time, ungated n+ microcrystalline silicon (μC-Si) strain sensors and gated a-Si:H strain sensors designed and fabricated directly on flexible polyimide substrates. To have a better comparison, we first introduce the metallic foil strain sensors. Then the fabrication process and measurement of μC-Si and gated a-Si:H strain sensors
are discussed in detail in the following part. Finally, the sensors are compared in terms of geometry, sensitivity, and power consumption.

### 3.3.1 Metallic Foil Strain Sensors

Figure 3-13 shows the mask layout of single bridge, which contains four individual metal foil strain gages, each consisting of a 14 μm wide and 95 mm long wire, connected to form a Wheatstone bridge with orthogonal strain response in adjacent resistors. The total area of the sensor is about 4.4 mm × 4.4 mm. The increase of resistance in the first and third quadrants, due to vertical elongation, will unbalance the bridge and send out a positive output. Conversely, horizontal elongation results in a negative output due to the increase of resistance in the second and fourth quadrants. Therefore, the direction of strain/stress can be determined from the sign of output.

![Figure 3-13: Mask layout of the Wheatstone bridge.](image)

50um thick Kapton® E film was used as the substrate. For substrate preparation procedure, see section 2.2.2. 300-nm thick platinum was deposited by ion beam sputtering and patterned by lift-off. The platinum was chosen because its gage factor,
G=12, is much higher than most other metallic materials, G = 2. Figure 3-14 shows pictures of a finished strain gage from a scanning electron microscope (SEM) and optical microscope, respectively.

![SEM and optical microscope images](image-url)

Figure 3-14: Strain gage bridge pictures by (a) SEM and (b) optical microscope.

The sensor was electrically connected to the test equipment. An Agilent 4156 semiconductor parameter analyzer was used to both supply the sensor excitation and measure the bridge output voltage. An excitation voltage of 5 V was applied to the two contacts on opposite sides of the bridge under test, and two orthogonal contacts were used to measure the sensor differential output voltage. Figure 3-15 shows the strain sensor differential output voltage when polymeric film was bent to different extents. The negative and positive parts in the output correspond to horizontal and vertical bending, respectively. The non-zero output when flat is due to the slight asymmetry among the four resistors. Since our purpose was to introduce the idea of metallic foil strain sensors, the test was not calibrated with bending radius.
Figure 3-15: Strain gage bridge differential output when polyimide film was bent.

To achieve complex shape sensing, we can integrate the sensors to an array by adding two transistor switches on differential output terminals for each sensor. By switching on and off the transistors, we can read out the selected sensor output and translate that signal to local radius.

### 3.3.2 Ungated µC-Si Strain Sensors

#### 3.3.2.1 Sensor Fabrication

Figure 3-16 shows the top view and cross-section view of sensor structure for ungated µC-Si strain sensors.
Figure 3-16: (a) The top view and (b) cross-section view of sensor structure for ungated µC-Si strain sensors.

A single 100-nm thick n+ µC-Si layer was deposited by PECVD system at 250°C from a gas mixture of SiH₄:PH₃:H₂=8:1:800 at a pressure of 0.5 torr and power density of 333 mW/cm². Then, 300 µm × 300 µm n+ µC-Si islands are patterned using photolithography and chlorine-based plasma dry etching. Following the patterning, 300 nm thick Molybdenum contacts are deposited by DC sputtering and patterned by a combination of CF₄ reactive ion etching (RIE) and wet etching. After sample fabrication, the polyimide film is peeled off the glass carrier for sensor characterization. Figure 3-17 shows the microscopic view of several completed strain sensors with different orientations.
3.3.2.2 Sensor Testing

Anisotropic conductive film (ACF) bonding is used to electrically connect strain sensor samples to a flexible cable, which, on the other end, connects to the print circuit board for testing. Figure 3-18 shows finished and bonded strain sensors on polyimide film at flat and bent conditions.

Figure 3-17: Microscopic view of ungated µC-Si strain sensor on polyimide substrate.

Figure 3-18: The picture of finished strain sensors on polyimide with ACF bonded flexible cable: (a) at flat and (b) bending states.
For initial testing, an Agilent 4156 semiconductor parameter analyzer is used to both supply the sensor excitation and measure the bridge output voltage. A bias current scan (0 to 100 µA) is applied to two contacts on opposite sides of the strain bridge under test, and two orthogonal contacts are used to measure the sensor output voltage. The polyimide film is bent around various cylinders with different diameters: 90, 76.6, 50.4, 41.7 and 25.5 mm, and along certain directions in which strain is applied to the sample in parallel, perpendicular, or angle 45° with respect to the direction of the current flow.

3.3.2.3 Sensor Sensitivity

Figure 3-19 shows the bridge output voltage as a function of applied current bias under various bending conditions (various cylinder radii) for strains parallel to and at 45°, with respect to a line connecting the bridge bias electrodes.

Figure 3-19: Ungated μC-Si strain sensor bridge output voltage as a function of bridge excitation current bias for bending radii of 90, 76.6, 50.4, and 41.7 mm for (a) strains parallel to and (b) at 45° with respect to a line connecting the bridge excitation electrodes.
For strain parallel to the bias current direction, the bridge output increases with bias current, but has shown only very slight changes between different bending radiiuses. The output is non-zero due to intrinsic unbalance of the bridge and can be easily offset if required. Strain perpendicular to the bias current direction produces a similar result. Strain applied at 45 ° with respect to the bias current direction produces a large variation from the zero strain bridge output, with the variation proportional to the strain. The sign of the variation from zero strain output depends on which 45 ° angle is chosen. After the conversion of strain from bending radius, we plot, in figure 3-20, the bridge output at 100 µA current bias as a function of strain for perpendicular, parallel, and at 45 ° directions, from which the sensitivities of 3 mV/%, 6 mV/%, and 64 mV/% are extracted for perpendicular, parallel and at 45 ° bending, respectively.

Figure 3-20: The bridge output, at a 100µA current bias, as a function of strain for perpendicular, parallel, and 45° directions, from which the sensitivities were extracted.

The sensitivity dependence on direction is due to both geometry and resistivity changes. The voltage sensing contacts remain geometric symmetry when bending
direction is either parallel or perpendicular to the bias current direction and the potential difference between two sensing contacts is minimal. However, sensor asymmetry is greatest for a 45° direction bending, and the potential difference on the sensing contacts is largest. With the static voltage drop between bias contacts (7.5 V) at 100 µA bias current, the gage factor $G$ can be calculated from sensitivity and static voltage drop as follows:

$$G = \frac{\Delta V}{V} = \frac{\Delta V}{\varepsilon} = \frac{64 \times 10^{-3}}{0.001} = \frac{64}{7.5} = 8.5$$ (1)

These results show a gage factor of ~ 8.5, which is higher than that of metallic foil strain sensors (about 2) but lower than crystalline silicon sensors (50 - 150). This is because strain induces both resistivity and geometry related resistance changes in the $\mu$C-Si sensor, but the randomness of the $\mu$C-Si grain orientation reduces the resistivity change compared to crystalline silicon.

Because of the high resistivity of the $\mu$C-Si compared with metallic foil sensors ($10^{-1} \Omega$-cm compared to $\sim 10^{-5} \Omega$-cm), serpentine resistors are not needed and the sensor area can be reduced from a few tens of mm$^2$ of metallic foil sensor to $\sim 300 \mu$m × 300 µm or even smaller. The reduced sensor area and simple sensor shape can improve the fabrication yield and also make the sensor less sensitive to defects. In addition, the power consumption is improved from a few tens mW per metallic foil sensor to $\sim 1$ mW per n+ $\mu$C-Si sensor.
3.3.2.4 Measurement Repeatability

A preliminary test of sensor measurement repeatability is carried out by bending and relaxing the strain sensors seven times. Figure 3-21a shows seven output measurements as a function of the bias current for both flat and 41.7 mm bending radius, indicating reasonably good repeatability. The sensor output voltage for 100 uA bias current is plotted in figure 3-21b, and again shows good repeatability. The small difference between measurements may be related to stress relaxation between the inorganic sensor film and the organic substrate.

Figure 3-21: (a) Seven-time bridge output measurements as a function of the bias current at both flat and 41.7 mm bending radius conditions; (b) All the output voltages measured under 100 uA bias current condition.
3.3.3 Gated a-Si:H Strain Sensor

3.3.3.1 Sensor Fabrication

As shown in the top and cross-section views in figure 3-22, the structure of gated a-Si:H strain sensors is much like that of a-Si:H TFTs except four source-drain contacts on top layer are used instead of two.

![Figure 3-22: The structure of gated a-Si:H strain sensor: (a) Top view of the sensor; (b) cross-section view of the sensor.](image)

The fabrication process was essentially the same as that used for a-Si:H TFTs on polyimide substrate [25]. Gate electrodes were first patterned by standard photolithography and wet etching of a 75 nm thick chromium layer deposited by thermal evaporation. A tri-layer stack comprised of a SiN gate dielectric layer (300 nm thick), an intrinsic a-Si:H active layer (50 nm thick), and a SiN passivation layer (300 nm thick) was then deposited by PECVD with a maximum processing temperature of 250 °C. The
SiN gate dielectric layer thickness was determined to have a low-leakage between gate and source-drain layers. After the intrinsic a-Si:H layer and SiN passivation layers were patterned by photolithography and wet etching, a 50 nm n+ μC-Si contact layer was deposited at 250 °C by PECVD and patterned by photolithography and chlorine-based RIE. The bottom SiN gate dielectric layer was then patterned by wet etching and a 300 nm thick molybdenum layer was deposited by a DC sputtering system and patterned using a combination of CF₄ RIE and wet etching to form the TFT source and drain contacts. The sensor active area is 410 μm × 410 μm and the contact area to intrinsic layer is 40 μm × 40 μm with center-to-center spacing of 325 um on each side. Table 3-3 lists the thickness of layers for gated a-Si:H strain sensors.

Table 3-3: Thickness of layers for a-Si:H strain sensors.

<table>
<thead>
<tr>
<th>Thickness (nm)</th>
<th>Gate metal</th>
<th>Gate dielectric SiN</th>
<th>Intrinsic a-Si:H</th>
<th>Passivation SiN</th>
<th>N+ uC-Si</th>
<th>Mo</th>
</tr>
</thead>
<tbody>
<tr>
<td>75</td>
<td>300</td>
<td>50</td>
<td>300</td>
<td>50</td>
<td>300</td>
<td></td>
</tr>
</tbody>
</table>

3.3.3.2 Sensor Testing

The test apparatus is the same for gated a-Si:H strain sensors as μC-Si strain sensors except for the excitation scheme. For these sensors, a bias voltage (0 to 20 V) is applied to two opposite contacts while the gate is maintained at either −5 V or 20 V, corresponding to off state or measurement state; the sensor output voltage is measured at the other two orthogonal contacts.
3.3.3.3 Sensor Sensitivity

With the sensor gate voltage at -5 V, corresponding to the off-state of the device, the sensor has very large impedance and draws no bias current (<1 pA). With sensor gate voltage at 20 V, a carrier channel is formed in the a-Si:H layer, and the sensor draws current and produces a sensor bridge output.

Figure 3-23 shows output voltages as a function of bias voltages under different bending radii (90 mm, 76.6 mm, 50.4 mm, and 41.7 mm) for strains perpendicular to and at 45 ° with respect to current directions.

Similar to ungated µC-Si strain sensors, strain applied at 45 ° with respect to the bias current direction produces a larger output signal than strain applied parallel to or perpendicular to the bias direction. The nonlinear regions for output bias shown in figure 3-23 are due to the transistor-like character of the gated sensors. For sensor excitation voltage much less than the gate voltage minus the threshold voltage (~ 2 V
here) the sensor acts as a variable resistor, so the output voltage is roughly a linear function of the sensor supply voltage. For sensor supply voltage comparable to or larger than the gate voltage minus the threshold voltage, the current begins to saturate, so the output curves flatten.

Accordingly, as shown in figure 3-24, the sensitivity of 0.4 mV‰, 1.3 mV‰ and 47.6 mV‰ are extracted for parallel, perpendicular and at 45° bending, respectively. These results show ~2.4 gage factor, similar to regular metallic foil strain sensors. The lower gage factor compared to the µC-Si devices is likely related to the absence of a resistivity change in the gated a-Si:H.

![Gated a-Si:H Strain Sensors](image)

Figure 3-24: The gated a-Si:H strain sensor output, under 20V bias, as a function of strain for perpendicular, parallel, and 45° directions, from which the sensitivities were extracted.

For an excitation voltage of 20 V, the sensor conducts about 0.5 µA current and consumes about 10 µW, or about two orders of magnitudes less than the ungated µC-Si strain sensors. In addition, in the off state the sensor consumes almost no power. The low power and gated operation are particularly of interest for low-power strain-sensing arrays.
3.3.4 Summary

Metallic foil strain sensor and two different kinds of semiconductor strain sensors, ungated n+ µC-Si and gated a-Si:H, were directly fabricated on 50 µm thick polyimide substrates. These sensors were characterized with different bending directions (perpendicular, parallel, and 45° to the bias direction) and with different bending diameters (90 mm, 76.6 mm, 50.4 mm, 41.7 mm, and 25.5 mm). The sensitivity of both types of strain sensors produces a large variation between 45° strain and parallel or perpendicular strain with respect to the bias direction. Table 3-4 lists the comparison of metallic foil sensor, ungated µC-Si sensor and gated a-Si:H sensor in terms of sensor area, power consumption, gage factors.

Table 3-4: Comparison of flexible strain sensors

<table>
<thead>
<tr>
<th></th>
<th>Metallic foil</th>
<th>µC-Si</th>
<th>a-Si:H</th>
</tr>
</thead>
<tbody>
<tr>
<td>Area (mm²)</td>
<td>19.4</td>
<td>0.09</td>
<td>0.16</td>
</tr>
<tr>
<td>Bias</td>
<td>7.7 V</td>
<td>100 µA</td>
<td>20 V</td>
</tr>
<tr>
<td>Power (mW)</td>
<td>12.35</td>
<td>0.77</td>
<td>0.01</td>
</tr>
<tr>
<td>Gage factor</td>
<td>~ 2</td>
<td>8.5</td>
<td>2.4</td>
</tr>
<tr>
<td>Gated</td>
<td>No</td>
<td>No</td>
<td>Yes</td>
</tr>
</tbody>
</table>

Apparently, ungated µC-Si sensors and gated a-Si:H sensors use two orders of magnitude less area than the metallic foil strain sensors. In terms of power consumption, ungated µC-Si sensors need only 6% of that of metallic foil sensors, and gated a-Si:H sensors, at on state, need only 0.1% of metallic foil sensors. Furthermore, the gated a-
Si:H sensor virtually need zero-power since normally it is at off state and conducts no current.

The small sensor size and ease of integration with a-Si:H TFTs will allow several strain sensors with different orientations to be combined to allow strain direction as well as magnitude to be unambiguously determined. Combination with TFTs can also allow large arrays of strain sensors to be fabricated on flexible substrates.

### 3.4 Low temperature a-Si:H TFTs on Kapton with Improved Stability

Both a-Si:H TFTs and sensors previously fabricated in our group are on flexible polyimide substrates. Additionally, stainless steel foil is also used sometimes as the substrates [48]. Both polyimide and stainless steel foil substrates are chosen because of the high temperature (above 250 °C) in the PECVD deposition process. However, the polyimide substrates, like Kapton®, are yellowish colored, and stainless steel foil is opaque, so applications are limited for displays. To take advantage of clear transparency and accommodate low-cost commercially available polymeric substrates, like polyethylene naphthalate (PEN) and polyethylene terephthalate (PET), we desire to use fabrication temperatures at 150 °C or less, significantly lower than what is typically used for fabrication on glass substrates (>250 °C). Interest in the low temperature a-Si:H TFT process has grown significantly since Nathan and Gleskova [27, 49] demonstrated a-Si:H TFTs fabricated at 150 °C or less. However, no one has mentioned the device stability that is important for many practical applications.
First, we discovered that device characteristics deteriorate rapidly as the process temperature with the regular recipe is lowered. By adding hydrogen dilution [49] to the gas mixture, we can make a-Si:H TFTs at 150 °C with performance that is comparable to that which is created with high temperature process. The device stability is tested by applying bias stress, and then compared with high temperature TFTs. Finally, simple electronic circuits of a digital inverter and a ring oscillator are demonstrated.

### 3.4.1 Lower Process Temperature Without $H_2$ Dilution

50µm Kapton® E films are mounted on a glass carrier in the same way as described in section 2.2.2., and the same PECVD recipe is used for fabricating a-Si:H TFTs except we lower the process temperature from 250 °C to 200 °C and 150 °C, respectively. The devices are tested and the results are compared with that of high temperature devices. Figure 3-25 shows measured mobility for different channel-length TFTs at 250 °C, 200 °C, and 150 °C, respectively. The saturation field-effect mobility is observed to have a 50 % and more than two orders of magnitude drop for 200 °C and 150 °C process, respectively, compared with normal 250 °C process. Besides the mobility decrease, the threshold voltage is shifted to the positive side for lower process temperature as well.
Figure 3-25: TFT mobility from different process temperatures.

Figure 3-26 compares the typical characteristics of same size TFT at both 250 °C and 200 °C. The mobility drops from 1.1 cm²/Vs to 0.4 cm²/Vs, while threshold voltage shifts from 3.0 V to 5.5 V.

Figure 3-26: Comparison of the typical TFT characteristics at both 250 °C and 200 °C.
When the temperature is lowered even more, to 150 °C, not only is the mobility degraded too much, but the gate dielectric SiN also loses its dielectric strength, and the devices show huge gate leakages. The results suggest that lower process temperature generates large trap state density at the dielectric/semiconductor interface that degrades device mobility and changes threshold voltage.

### 3.4.2 Lower Process Temperature with H₂ Dilution

#### 3.4.2.1 SiN

To improve the SiN dielectric quality at 150 °C, hydrogen dilution is added during the PECVD process [49]. The process condition is listed as follows: process pressure of 500 mTorr, power density of 0.08 W/cm², gas flow-rate of SiH₄:NH₃:H₂ = 4:40:176 sccm, and temperature of 150 °C. The deposition rate is about 0.73 Å/s, much lower than that of the regular 250 °C process (2.8 Å/s).

We characterize the SiN film by capacitance-voltage (C-V) and current-voltage (J-V) tests and compare it with SiN from the 250 °C process. A lightly doped silicon wafer was used as the substrate, and a blank layer of SiN without H₂ dilution at 250 °C and a blank layer of SiN with H₂ dilution at 150 °C, respectively, were deposited by PECVD. Then aluminum top electrodes were deposited through a shadow mask by thermal evaporation. The thickness of SiN was determined, by spectroscopic ellipsometry, to be 104 nm and 112 nm for 250 °C and 150 °C SiN, respectively. In addition, the refractive index of SiN is measured by spectroscopic ellipsometry: \( n = 1.81 \)
and 1.80 for 250 °C and 150 °C SiN, respectively. Figure 3-27a shows measured C-V curve from which the permittivity of SiN film is extracted: about 6.1 and 6.2 for 250 °C and 150 °C SiN, respectively. Figure 3-27b shows the J-V curves for both SiN, from which the resistivity and break-down voltage can be extracted. They show similar resistivity of around $2 \times 10^{15} \, \Omega\text{-cm}$ and break-down electric field of 6 MV/cm. Table 3-5 summarizes the properties of SiN from the 250 °C and the 150 °C process.

![Figure 3-27: SiN characteristics: (a) C-V measurement; (b) I-V measurement.](image)

Table 3-5: Properties of SiN from 250 °C and 150 °C process.

<table>
<thead>
<tr>
<th></th>
<th>250 °C</th>
<th>150 °C</th>
</tr>
</thead>
<tbody>
<tr>
<td>Refractive index, n</td>
<td>1.81</td>
<td>1.80</td>
</tr>
<tr>
<td>Permittivity, $\varepsilon_r$</td>
<td>6.1</td>
<td>6.2</td>
</tr>
<tr>
<td>Break-down field</td>
<td>&gt; 6 MV/cm</td>
<td>&gt; 6 MV/cm</td>
</tr>
<tr>
<td>Resistivity</td>
<td>$2.2 \times 10^{15} , \Omega\text{-cm}$</td>
<td>$1.7 \times 10^{15} , \Omega\text{-cm}$</td>
</tr>
</tbody>
</table>
3.4.2.2 Doped µC-Si

Since the regular process recipe already includes huge amounts of H\textsubscript{2} (flow-rate of SiH\textsubscript{4}:PH\textsubscript{3}:H\textsubscript{2} = 2:3:1000), the same recipe is used for both doped µC-Si depositions except at different temperatures. The other deposition conditions were: process pressure of 1 torr and power density of 600 mW/cm\textsuperscript{2}. The transfer length method was used to test the contact resistance and resistivity of the doped µC-Si. The results are plotted in Figure 3-28 for different deposition temperatures. In addition, the test was repeated after the film was thermally annealed by a hotplate bake for one hour. The anneal temperature is 150 °C for the film deposited at 150 °C, and 200 °C for the film deposited at 200 °C and above. The contact resistance of the N+ on top of the a-Si:H layer at 150 °C shows twice as much as 250 °C process, and both are lowered slightly after the thermal anneal. The resistivity of the N+ layer on a-Si:H layer is slowly increased from 0.10 Ω-cm at 250 °C to 0.15 Ω-cm at 150 °C. Although both contact resistance and resistivity increase after lowering the process temperature, their magnitude is still too small to play a role in a-Si:H TFTs’ characteristics.
Figure 3-28: (a) N+ contact resistance vs. deposition temperature on a-Si:H and SiN film; (b) N+ resistivity vs. deposition temperature on a-Si:H and SiN film.

3.4.2.3 a-Si:H TFTs

In addition to the above recipes for SiN and n+ μC-Si layers, the a-Si:H intrinsic layer was deposited with H₂ dilution (flow-rate of SiH₄:H₂ = 10:100) at 0.5 torr and 0.047 W/cm² power density at 150 °C. The deposition rate is about 0.57 Å/s. By using the above mentioned process for SiN, a-Si:H, and n+ μC-Si layers, a-Si:H TFTs were finished on Kapton polyimide substrates at the highest process temperature of 150 °C. Figure 3-29 shows the measurement, from which the TFT characteristics can be extracted: saturation field-effect mobility of 1.0 cm²/V-s, threshold voltage of 3.2 V, and sub-threshold slope of 0.4 V/Dec.
Figure 3-29: a-Si:H TFT characteristics, deposited at 150 °C: (a) $I_D \sim V_{GS}$; (b) $I_D \sim V_{DS}$.

In plotting the mobility of devices with and without H$_2$ dilution process in figure 3-30, we found that the mobility is similar between the 250 °C without H$_2$ process and the 150 °C with H$_2$ process. The results suggest that the 150 °C process is a possible replacement for the high temperature one.

Figure 3-30: Mobility comparison with and without H$_2$ dilution.
3.4.2.4 TFT Instability

Very often, a-Si:H TFTs need to be operated at continuous-on state for a certain amount of time in real applications: an example is the OLED drive TFT. Some changes in characteristic may adversely affect the circuit performance. For example, the threshold voltage shift in drive TFTs of active matrix OLED back-plane will directly degrade the uniformity in brightness of that display.

TFTs’ instability can be observed in their transfer characteristics, and this instability manifests itself as a parallel shift of the I-V characteristics to the right when the gate bias voltage is positive and to the left when the gate bias is negative, i.e., a threshold voltage ($V_t$) shift. The $V_t$ shift is believed to involve two mechanisms: charge trapping in the SiN gate insulator and deep trap levels in the a-Si:H film [5]. The $V_t$ shift depends strongly on the gate bias, while it varies only slightly with the drain voltage. Therefore, the $V_t$ shift data is usually obtained under gate bias stress conditions. However, the thermal annealing process is proved to be effective in recovering the initial I-V characteristics.

We performed the TFT instability test by stressing gate and drain voltages at 20V for 10 minutes, and TFT characteristics were compared before and after the bias stress for both 250 °C without H$_2$ process and 150 °C with H$_2$ process. Figure 3-31a shows the test result for TFT with the H$_2$ diluted 150 °C process, and about 1.0 V shift is observed after the bias stress. As a comparison, the TFT with the 250 °C process was tested, and the result is shown in Figure 3-31b. A shift of approximately 0.7 V is observed. Closer observation of curves in logarithm scale for both devices indicates that the original curve
got a parallel shift in sub-threshold region, which suggests that the trap density state remains the same after our bias stress test and that charge trapping in the SiN gate insulator plays the dominant role. The similar $V_t$ shift suggests that TFTs with an $H_2$ diluted 150 °C process are comparable to TFTs created with the 250 °C process in terms of stability and could be a viable replacement in many practical applications.

Figure 3-31: Bias stress test on a-Si:H TFTs at the process of (a) 150 °C with $H_2$ dilution and (b) 250 °C.

### 3.4.2.5 Digital Inverter and Ring Oscillator

Integrated by these low temperature process a-Si:H TFTs, some simple digital circuits were realized. Figure 3-32 shows the schematic and microscopic view of a digital inverter circuit.
Figure 3-32: (a) Schematic and (b) microscopic view of inverter.

The pull-up transistor is 40 \( \mu \text{m} \) wide and 20 \( \mu \text{m} \) long and pull-down transistor is 400 \( \mu \text{m} \) wide and 20 \( \mu \text{m} \) long. Figure 3-33 shows the output as a function of input voltage and a gain of about 2.0 is extracted from the slope in the middle point of the curve. Clearly an eye pattern is observed from the plot, which means it will function well as an inverter in digital circuits.

Figure 3-33: Inverter output as a function of input voltage.
A 5-stage ring oscillator was realized by cascading five digital inverters in a round way, and an extra buffer inverter was added for measurement. Figure 3-34 shows its schematic and microscopic view. Two designs of inverters were used in the ring oscillator circuit: $\beta=5$ and $\beta=10$ ($\beta$ is defined as the ratio of channel width over channel length of pull-down TFT to that of pull-up TFT). In addition, two gate-source overlap design rules, 2 $\mu$m and 5 $\mu$m, are used in the circuit. Smaller gate-source overlap decreases the device capacitance, so the expectation is that the circuit will run faster.

![Diagram of 5-stage ring oscillator](image)

Figure 3-34: (a) Schematic and (b) microscopic view of 5-stage ring oscillator.

Figure 3-35 plots the measured single stage propagation delay as a function of power supply for different $\beta$ and gate-source overlap configurations. The propagation delay decreases rapidly with the increase of supply voltage, then slowly levels off. The inverter with $\beta=5$ shows better propagation delay parameter than the inverter with $\beta=10$. As expected, 2 $\mu$m gate-source overlap certainly works faster than 5 $\mu$m overlap. Nevertheless, under 20 V power supply, the propagation delay is less than 3 $\mu$s.
Figure 3-35: Single stage propagation delay vs. power supply voltage.

3.4.3 Summary

Using a regular recipe, a-Si:H TFT performance deteriorates rapidly with the decrease of process temperature. By adding hydrogen dilution, a-Si:H TFT deposited at 150 °C shows similar performance as that of undiluted 250 °C process. The stability of TFT was tested using bias stress tests, and TFTs of both processes show close results. Simple digital circuits, such as a digital inverter and a ring oscillator, were demonstrated and characterized. These results suggest that low temperature H₂ dilution a-Si:H TFT is viable for practical applications, and it could potentially prove useful in taking advantage of low temperature polymeric substrates.
Chapter 4
Pentacene OTFT Passivation

4.1 Background Knowledge

As previously mentioned, our p-type pentacene TFTs with a silicon dioxide gate dielectric typically show a positive threshold voltage. This means that an accumulation layer is present at the semiconductor-gate dielectric interface at zero gate bias. This accumulation layer leads to a large leakage current that flows through the pentacene layer outside the gated area even when the device is biased in the off state. This leakage current significantly reduces on/off current ratio and leads to crosstalk between adjacent devices and circuit elements, both of which are serious concerns for applications such as active matrix displays.

In early demonstrations, like pentacene TFTs on thermally oxidized heavily doped silicon wafers as shown in Figure 4-1a, active layer leakage was reduced by physically scratching around the active device area with a probe tip. As shown in Figure 4-1b, the pentacene TFT circuits on glass can utilize a Corbino TFT layout so that the drain contact is completely surrounded by the underlying gate electrode and no ungated pentacene is in contact with the drain when the device is biased in the off state. Using a Corbino TFT design, pentacene TFTs and circuits on glass were fabricated with off current less than 1pA and on/off current ratio > 10^6 [16]. The Corbino TFT design is unattractive, however, for fabricating integrated circuits or large TFT arrays because an
additional metal level is required to make an interconnection between the gate of one device and the source/drain of another. Another method of active layer patterning to reduce leakage is the direct use of a shadow mask during the pentacene deposition as Figure 4-1c illustrates. This method, however, is impractical for high-resolution applications due to the difficulty of alignment of shadow mask. The three methods of reducing active layer leakage mentioned here have limited utility in realizing pentacene TFTs and circuits compatible with commercial applications.

![Figure 4-1: (a) scratch around active region to isolate pentacene; (b) Carbino layout; (c) shadow mask pentacene evaporation.](image)

Ideally, the organic active layer would be patterned in a method similar to a-Si:H TFTs where a mask is patterned on top of the active layer and the exposed regions are etched away by directional plasma etching. This would allow the pentacene in the field region to be removed, thereby eliminating the leakage path between the source and drain contacts. A photolithographic process of this type, however, is highly problematic for most organic semiconductors because they are sensitive to organic solvents commonly encountered in photolithography. Pentacene films undergo a phase transformation and buckle when exposed to common organic solvents such as acetone and isopropyl alcohol, which results in significant degradation in device performance [21].
To avoid exposure of the pentacene thin film to harmful organic solvents during patterning, Sheraw demonstrated that the water-soluble polymer polyvinyl alcohol (PVA) could be used as the photoresist which could mask the pentacene in channel from being removed by RIE O$_2$ plasma dry etching [23]. Figure 4-2 shows the cross-section of a PVA patterned pentacene TFT.

![Figure 4-2: The cross-section of a PVA patterned pentacene TFT.](image)

After patterning, the TFTs often can conserve the field-effect mobility and show ~pA off current. However, the sub-threshold slope is often degraded and a knee-shape curve usually happens in the sub-threshold region in the log of drain current versus gate-source voltage characteristic. This is most likely due to residual moisture in the film and/or at the interface.

As we integrate the pentacene TFTs with OLED materials, moisture trapped in PVA thin film is a big concern for the OLED lifetime. A new pentacene patterning and passivation technique has to be developed. We have tried both inorganic and organic materials like RT PECVD SiN and parylene-C to passivate pentacene thin film.
4.2 Room Temperature PECVD SiN Passivation

For convenience, a thermally oxidized heavily-doped silicon wafer is used as the substrate, gate electrode, and the gate dielectric. Platinum source/drain electrodes are sputtered by ion mill and patterned by lift-off. The pentacene thin film active layer is deposited by thermal evaporation at a deposition rate of 0.1 – 0.5 Å/s following a 3-hour OTS vapor treatment. The substrate is heated to 60 °C during deposition to promote molecular ordering in the film. Then, the sample is loaded into room temperature plasma enhanced chemical vapor deposition (RT PECVD) system, and 300nm SiN is deposited directly on top of pentacene thin film.

To test the passivation effect, TFT characteristics were measured and compared before and after the direct deposition of SiN on pentacene TFTs without a patterning of the SiN. Figure 4-3 plots TFT drain current as a function of gate-source voltage before and after passivation.

Figure 4-3: TFT characteristics of drain current as a function of gate-source voltage before and after the SiN passivation.
The TFT performance is greatly degraded from the passivation: the field-effect mobility dropped from 0.6 cm$^2$/Vs to 0.08 cm$^2$/Vs, and the threshold voltage shifted from -1.7 V to -17.3 V. The TFT characteristic change is the result of the increase of trap state density in pentacene thin film on semiconductor/dielectric interface.

Two possible factors may affect the pentacene thin film during the SiN deposition: the short wavelength UV exposure and physical particle bombardment. To understand the degradation mechanism, the PECVD deposition was repeated with the device covered with a quartz plate. Since the quartz plate blocked the physical particle bombardment while still allowing UV light to pass through during the deposition, the TFT underwent the near UV exposure only. After the running of SiN deposition, the samples were measured and TFT characteristics were plotted in Figure 4-4.

![Figure 4-4](image)

Figure 4-4: TFT characteristics of drain current as a function of gate-source voltage before and after the SiN passivation with a quartz plate on top.

A similar degradation was observed again: the field-effect mobility dropped from 0.43 cm$^2$/Vs to 0.06 cm$^2$/Vs and the threshold voltage shifted from 0.8V to –11V. Apparently, UV exposure kills the pentacene TFTs.
4.3 Parylene Passivation

4.3.1 Parylene Property

Parylene is the generic name for the poly-para-xylelene class of polymers that are known for their ability to polymerize on surfaces from an active monomer gas with no liquid phase involved. Parylene-based polymers have been commercially available for over 25 years and have found widespread use as environmental and electrical isolation coatings for electronic circuits, automotive sensors, and medical substrates [50] due to their ability to form conformal coatings.

Parylene has some important advantages: it is virtually a room temperature deposition, and it forms a uniform pinhole free film with outstanding barrier property which shows very low permeability to moisture and gases. Also, it shows extreme chemical resistance against most common organic solvents and most acids and bases; in addition, it provides superior electrical properties such as extremely high dielectric strength and very high resistivity. For this work, parylene C was used because of its excellent combination of physical and electrical properties. Table 4-1 lists its important properties.
Table 4-1: Properties of Parylene-C.

<table>
<thead>
<tr>
<th>Property</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dielectric strength (V/cm)</td>
<td>$2.7 \times 10^6$</td>
</tr>
<tr>
<td>Dielectric constant at 1 kHz</td>
<td>3.1</td>
</tr>
<tr>
<td>Moisture absorption (wt. %)</td>
<td>0.06</td>
</tr>
<tr>
<td>Minimum process</td>
<td>27</td>
</tr>
<tr>
<td>Volume resistivity (Ω-cm)</td>
<td>$6 \times 10^{16}$</td>
</tr>
<tr>
<td>Glass transition temperature</td>
<td>80</td>
</tr>
<tr>
<td>Decomposition temperature</td>
<td>290</td>
</tr>
<tr>
<td>Refractive index</td>
<td>1.64</td>
</tr>
<tr>
<td>Deposition method</td>
<td>vapor</td>
</tr>
<tr>
<td>Patterning method</td>
<td>dry etch</td>
</tr>
<tr>
<td>Solvent resistance</td>
<td>good</td>
</tr>
</tbody>
</table>

The parylene coating process is a three-step procedure that includes vaporization, pyrolysis, and polymerization. The parylene C coating process, schematically represented in Figure 4-5, begins with the vaporization of the precursor dimer (di-para-xylelene), a granular white powder, at 150°C and a pressure of 1 torr. This results in a dimer gas that moves toward the pyrolysis chamber where at 680 °C and 0.5 torr, the dimer is cracked, yielding the monomer (a diradical para-xyelelene). The monomer then enters the room temperature deposition chamber at 100 mtorr where it adsorbs and polymerizes on all surfaces, resulting in a high molecular weight polymer (polychloro-p-xyelelene). The parylene deposition is done by a PDS Labcoater 2010.
4.3.2 Parylene Passivation

The vacuum deposition from the polymerization of parylene is actually desirable for pentacene passivation because of the compatibility of standard photolithography process on top of parylene. Similar to the SiN passivation test, platinum source-drain bottom contact and shadow-masked gold top contact pentacene TFTs on a thermally oxidized heavily doped silicon wafer were prepared for convenience, and 0.5 µm parylene was then deposited on top at room temperature. TFT characteristics were measured and compared before and after the deposition without a patterning of the parylene. As shown in Figure 4-6a, the bottom contact TFT shows a 50% decrease of
field-effect mobility from 1.60 cm²/Vs to 0.81 cm²/Vs, while the threshold voltage has a 2 V shift to the negative side. Figure 4-6b shows that the top contact TFT has a 40% decrease of field-effect mobility from 1.26 cm²/Vs to 0.75 cm²/Vs, while the threshold voltage has a 1.8 V shift to the positive side. Both cases show a 40-50% drop in mobility while maintaining almost the same threshold voltage.

Figure 4-6: (a) Bottom and (b) top contact pentacene TFT characteristics changes with parylene passivation.

Since pentacene thin film usually grows in the 3-D form of a polycrystalline structure, parylene molecules can easily gain access to the semiconductor/dielectric interface layer. The parylene-pentacene interaction may partially oxidize the pentacene channel layer and cause the degradation on mobility.

4.3.3 PVA and Parylene Bi-layer Passivation

As we know, parylene directly on top of pentacene will hurt pentacene TFT performance by somehow interacting with the pentacene channel layer. A direct solution to this would be a buffer layer between the pentacene channel layer and the parylene
passivation layer. Since polyvinyl alcohol (PVA) has been used as a photo-patternable etch mask for pentacene, it can work as a buffer layer.

After PVA patterning of the pentacene TFT, 1μm parylene was then coated by a Labcoater 2010 and patterned by standard photolithography and RIE O$_2$ dry etching. Figure 4-7(a) shows a cross-section view of the device. The TFT characteristics were measured before and after the parylene passivation. Figure 4-7(b) shows the curve of drain current as a function of gate-source voltage. The mobility has a small decrease from 0.62 cm$^2$/Vs to 0.53 cm$^2$/Vs, and the mobility shifted from -1 V to 2 V. This result suggests that the etch-mask PVA can protect pentacene thin film from parylene passivation by acting as a buffer layer.

![Graph](image)

**Figure 4-7:** (a) cross-section view of bi-layer passivation of PVA and parylene; (b) pentacene TFT characteristic change after parylene passivation with PVA as a buffer layer.

As a result, the bi-layer of the PVA and the parylene structure, on one hand, can passivate the pentacene TFTs, and on the other hand, shield OLED materials from
moisture exposure. However, the moisture permanently trapped in PVA and cannot be removed, so this method is still a temporary solution.

4.4 Summary

In order to avoid the PVA moisture degradation on OLED, new passivation techniques are required. Inorganic material like RT PECVD SiN and organic material like parylene have been tried to directly passivate pentacene TFTs. Unfortunately, both fail. The UV light during SiN deposition basically kills pentacene thin film, and parylene-pentacene interaction degrades the device mobility by 50%. For the time being, we solve the problem by using a PVA and parylene bilayer structure. However, it is desirable to get rid of the moisture in the PVA layer completely. It is possible to find certain polymer materials which have the similarly good properties as parylene-C, however, don’t react to pentacene thin film. Parylene-N seems to be one of the possible candidates. Parylene-N doesn’t have the chlorine atom in its molecular structure compared with parylene-C, and our preliminary results suggest it works better than parylene-C for pentacene passivation.
Chapter 5

Pentacene OTFT Driven AM OLED Display

5.1 Introduction

5.1.1 Background Knowledge

The high demand for portable electronics such as cell phones, laptops, personal digital assistants, and digital cameras, has helped make flat panel display (FPD) manufacturing a $50 billion a year industry with approximately 25% annual growth [51]. While the FPD industry is currently dominated by liquid crystal technology, there has been a tremendous amount of interest in, and research on, organic light emitting diodes (OLEDs). OLED displays have several advantages over liquid crystal displays (LCDs). Unlike liquid crystals, OLEDs are emissive and therefore are brighter, have a wider viewing angle, and do not require backlights or filters, allowing thinner, lighter, and more power efficient displays. OLEDs are already used in a number of commercial products, for example Kodak’s digital camera, and the OLED display market is expected to reach $3 billion annually by the year 2007 [51].

An OLED is an electroluminescent device that consists of a single layer or stack of organic layers sandwiched between two conductive electrodes. When a bias is applied, current flows through the device, and electrons and holes are injected into the organic layer. When they meet, the recombination gives off lights characteristic of the band gap
of organic material. The stability of OLEDs is a problem as both the OLED material and the cathode metal can degrade when exposed to moisture. OLED pixels are often encapsulated with an impermeable barrier in order to improve their lifetime.

For high information content displays, active-matrix pixel addressing provides improved display performance and reduced power consumption. In active matrix addressing, each individual pixel is controlled by one or more thin film transistors (TFTs). The most basic active matrix OLED pixel, as Figure 5-1 shows, consists of a select and drive TFT, storage capacitor, and the emissive OLED.

![Figure 5-1: Two TFT OLED pixels.](image)

During display operation, a pulsed bias is applied to the gate of the select TFT, turning the TFT on and allowing a simultaneous data pulse to be applied to the gate of the drive TFT. The drive TFT is turned on and current is permitted to flow through the OLED. The storage capacitor retains the gate bias on the drive TFT until the pixel is again addressed. The select TFT only needs to charge the storage capacitor during the select pulse and therefore is often smaller than the drive TFT, which powers the OLED.
The larger the drive TFT, the more current it can supply to the OLED, making it possible to use low performance (low field-effect mobility) TFTs at reasonable drive and data voltages simply by increasing the size of the drive TFT. A large drive TFT, however, reduces the aperture ratio of bottom-emitting pixels by leaving less emissive area. Using more efficient OLEDs can reduce the required drive TFT size.

To date, most active matrix OLED displays have used polysilicon TFTs as the active elements because they can provide sufficient current at low voltages and acceptable device dimensions, and they are capable of integrated drive electronics [52-54]. Sanyo/Kodak even commercially manufactured the 2.2" OLED displays for their EasyShare digital cameras. However, improvements in the efficiency of OLEDs allow lower mobility TFTs, such as those based on a-Si:H and organic semiconductors, to be used as OLED drive devices [55, 56]. Compared with polysilicon TFTs, a-Si:H is a mature technology, with established infrastructure, and it is more suitable for large displays. Organic TFTs with performance similar to a-Si:H [14, 57], although at their early stage of development, show the potential for low temperature and low cost manufacturing. One reason why organic TFTs have gained so much attention is because they can, in principle, be manufactured on polymeric substrates in a roll-to-roll process, which would be a revolutionary change from current batch process manufacturing. Displays fabricated on polymeric substrates can be flexible, lightweight, and rugged, all of which are very attractive properties for portable electronics.

The largest concern with using organic TFTs in active matrix (AM) OLED displays is whether sufficient current can be supplied at low voltages. In addition, several critical issues, such as dielectric integrity, device passivation and integration technique,
and TFT uniformity, still need to be addressed. Nonetheless, organic TFTs may be an option for large area and low cost displays while LTPS TFTs may be well suited for high-end small displays.

### 5.1.2 Drive Requirements

With the demonstration of active matrix OLED TV displays from Samsung and Philips (2005 Society of Information Display Conference exhibit), it is generally agreed that TFTs with mobility as low as that of a-Si:H are good enough to supply OLED current. Pentacene TFTs have shown similar device performance in terms of mobility, and we don’t see principle limitations of the pentacene OTFTs on OLED displays applications. Given the area of OLED and mobility of TFTs, the drive TFT size (W/L) is determined by the OLED drive current requirement.

Since the low current in OLED is non-emissive, the off-current requirement on drive TFT is really loose. However, in an active matrix OLED display, the gate voltage on the drive TFT, held by the help of a storage capacitor, needs to be held constant during the whole frame time after it has been charged through select TFT during the line-scan time, which, similar to the LCD case, requires sufficient low off-current for the select TFTs not to discharge the pixel capacitor. The size of select TFT is determined to have 99% of the data voltage charged on a storage capacitor. With a similar size of storage capacitor for both LCD and OLED display, a device with W/L of a few is sufficient for VGA size of display at 60Hz.
The drive TFTs are always operating in saturation regime ($V_{DS} > V_G - V_T$) while select TFTs are mostly in linear regime. Since most pentacene TFTs for display applications are using bottom contact structure for easy patterning of the metal contacts, the contact resistance is relatively high, especially in linear regime. As a result, most pentacene TFTs show lower linear mobility than saturation mobility. Therefore, the higher on-resistance of select transistors will increase (dis)charging time for the storage capacitor, which must be considered when determining select-TFT size.

As OLED technology improves its lifetime, the drive TFT stability turns out to be more important. Since the drive TFT is continuing under the single polarity stress when at the OLED is lit up, the threshold voltage shift will finally impair or even lose the pixel. Although this is not a problem for poly-Si TFTs, it’s a critical issue in both a-Si:H and pentacene TFTs driving plans.

With current OLED technology advances, like higher efficiencies, lower turn-on voltages, and smaller drive currents for same light outputs, pentacene TFTs still look plausible for this application.

### 5.1.3 Highlight Differences from LCD

This section discusses a simple comparison of the transistors in LCD and OLED pixels. Although an OLED pixel needs more transistors than that in a LCD, the requirement on select transistors in an OLED pixel is almost the same as the transistor in a LCD application. They share the common goal of (dis)charging the storage capacitors, which for the most part, will have similar size too, given that a liquid crystal capacitor is
normally much smaller than a storage capacitor. So usually a small transistor with the size of $W/L \approx 3$ will suffice for VGA-size displays. However, the drive transistor in an OLED pixel usually will be much larger than select transistor to provide enough OLED current. In the case of a-Si:H and pentacene TFTs, it will take much more area and limit the pixel aperture ratio, especially for bottom emission displays.

The TFTs in a LCD panel are operated under stress conditions of both positive and negative gate biases. Positive voltages are applied to the gate electrode in a pulsed mode. Between pulses, the gate is biased to negative voltages. Therefore, it is expected that these positive and negative shifts tend to cancel each other out. So we normally see much better stability of a-Si:H TFTs on LCD panels than on discrete devices. But it is totally different for TFTs on OLED panels because the drive TFTs are under constant bias stress. As a result, usually a complex pixel design will be necessary to complement the device instability [52].

The TFTs in LCDs are acting as pure switches. As long as their gate biases are well above the threshold voltage and data voltage, they pass the exact data voltage to liquid crystal capacitor without distortions. There is no stringent requirement on the uniformity of transistors. However, the drive transistors in OLED displays determine the OLED current. A small change in threshold voltage and mobility will directly affect the current that in turn affects the brightness. As a result, the OLED display requires an extreme control on the TFT uniformity.
5.1.4 Complex Pixel Design

With the device non-uniformity and instability in mind, it is more practical to use a more complex circuitry in the pixel design. There are many proposals published in literature for both poly-Si and s-Si:H TFTs and most of them are using 4-T structures. Dawson, et. al. proposed a 4-T structure that uses two additional poly-Si transistors to auto zero the threshold voltage of the current drive transistor [54]. This technique can eliminate the threshold voltage variations; however, it does not deal with mobility variations. Another 4-T structure based on a-Si:H was proposed by Yi He which uses a current-programming method to compensate for both threshold and mobility variations [58], but it has the disadvantage that charging time for low data current is long. To overcome this problem, a 4-T current-mirror structure was also proposed by Yumoto to scale the data current and reduce charging time at low data current [59]. However, all above methods are not taking account of the OLED degradation due to operation, and more work is necessary.

5.2 Pentacene OTFT Backplane Design

5.2.1 Pixel Design

As Figure 5-1 shows, the previously described simple two-TFT pixel layout was used, which consists of a select and drive TFT, storage capacitor, and the emissive OLED. Normally, a larger drive TFT will supply more current to OLED; however, it reduces the aperture ratio of bottom-emitting pixels by leaving less emissive area.
The average current necessary to produce a bright display (100 cd/m²) is approximately 10 mA/cm² [60]. If we choose a pixel size of 500 µm × 500 µm and aperture ratio of 50%, a steady current of 12.5 µA is necessary. Assuming a TFT operating in saturation, the required mobility can be calculated according to Eq. 5.1.

\[ \mu = \frac{I_{\text{SAT}}}{W} \frac{1}{2L} \frac{C_{\text{ox}}}{(V_{\text{GS}} - V_{\text{T}})^2} \]  

5.1

To achieve the proper current levels by drive TFT using a convenient device geometry (W = 200 µm, L = 20 µm), a silicon dioxide gate dielectric thickness of 300nm, a reasonable threshold voltage of +10 V, and a gate source voltage of -30 V, a mobility of 0.14 cm²/Vs is required according to Eq. 5.1. A well-fabricated pentacene TFT normally shows mobility much higher than this requirement.

Since the select TFT is used only for (dis)charging the storage capacitor (gate capacitor of the drive TFT is much smaller than storage capacitor), we can just use a conveniently small device geometry, W = 20 µm, L = 20 µm. This transistor is basically working in a linear region, and the on resistance of the select TFT can be calculated by Eq. 5.2:

\[ R_{\text{ON}} = \frac{V_{\text{DS}}}{I_D} = \frac{1}{\mu C_{\text{ox}}(V_{\text{GS}} - V_{\text{T}})} \frac{W}{L} \]  

5.2

Taking a modest mobility of 0.5 cm²/Vs, a V_{GS} of -30 V, and a V_{T} of +10 V, respectively; the on-resistance is only 2MΩ calculated according to Eq. 5.2. Assuming a storage capacitor of 1.2 pF, which conveniently corresponds to an area of 200 µm × 50 µm, the (dis)charging time is only 2.5 µs, much less than the required row time for a
middle size display (~ 100 µs). During each frame time, the storage capacitor has to hold the charges so that the drive TFT can keep a constant gate voltage, which results in a constant current flowing through the drive TFT and OLED. Assuming that the TFT has 10 pA off current, although the off-current is normally around a few pico-Ampere, that the frame time is 10 ms (corresponding to 100 Hz refresh rate), and that the storage capacitor is 1.2 pF. The voltage holding decay, according to Eq. 5.3, is only about 0.1 V. This result is relatively small compared to the normal operation voltage range of 40 V even for this worst-case scenario.

\[ \Delta V = \frac{\Delta Q}{C_s} = \frac{I_{off} t_{FRAME}}{C_s} \]  \hspace{1cm} 5.3

All of the above calculations indicate that the pentacene TFT is feasible for use in an AM OLED display backplane. The pixel design finally came with a pitch of 500 µm and an aperture ratio of 54 %. The drive transistor had a W/L ratio of 10 (200µm/20µm), and the select transistor had a W/L ratio of 1 (20 µm/20 µm). A 48×48-pixel bottom-emission display panel was designed on a 64 mm × 64 mm glass substrate.

To obtain a good yield, a design rule of 10 µm has been used for the minimum feature size (line width or separation) for most structures on the test panel. The coarseness of this design rule is not directly related to the use of organics, but rather to the simplicity of the photolithographic process.
5.2.2 AIM-Spice simulation

Before developing a pixel circuit, Simulation of pentacene TFT, OLED and OTFT/OLED active pixels are carried out using the integrated circuit modeling program AIM-Spice. Like other analog circuit simulators, AIM-Spice is a new version of SPICE, which uses Berkeley SPICE version 3 as its kernel and conveniently includes advanced new models for a-Si:H and poly-Si TFTs.

It is more meaningful to choose the drive TFT from a pentacene OTFT with a mediocre performance, like a mobility of 0.6 cm$^2$/Vs and a threshold voltage of 10 V, which is a device very easy to achieve after a decade of research work in this area. OTFT and OLED device models were formed using measured device data, and the simulation was performed using dimensions consistent with the pixel design in the previous part. The OTFT has a channel width of 200 µm and channel length of 20 µm, and the OLED has an area of 1.25×10$^{-3}$ cm$^2$ (250 µm × 500 µm). The device dimension was chosen to be the same as that in our design in the previous part, so that we could have a comparison later.

Figure 2-1a shows drain current as a function of gate-source voltage and Figure 2-1b plots drain current as a function of drain-source voltage. As expected, in addition to the predicted mobility and threshold voltage, it has off-current of less than 10pA, sub-threshold slope of 2 V/Dec.
Figure 5-2: AIM-Spice simulation on drive pentacene OTFT with W=200µm and L=20µm: (a) $I_D$ vs. $V_{GS}$, (b) $I_D$ vs. $V_{DS}$.

Similarly, a small molecule OLED with mediocre performance like regular turn-on voltage was simulated and shown in Figure 5-3.

Figure 5-3: AIM-Spice simulation of OLED with the area of $1.25 \times 10^{-3}$ cm$^2$.

After the integration of OTFT and OLED as shown in Figure 5-4a, OTFT driven OLED currents under various data voltages were simulated and shown in figure 5-4b. Apparently it responds to the data voltage very well. The OTFT/OLED on-current is well
above our requirement of 12.5µA, as we expected. The OTFT/OLED on-current is lower than the discrete OTFT because the voltage drop on the OLED partially took away the drain voltage of the OTFT, and the working point in pentacene OTFT wasn’t in the deep saturation anymore. Still, the OLED current was close to the OTFT current at lower drain-source bias.

![Diagram of OTFT and OLED integration](image)

**Figure 5-4**: AIM-Spice simulation of the integration of OTFT and OLED: (a) OTFT and OLED integration schematic; (b) OLED current as a function of various data voltages.

In the bottom emission AMOLED displays driven by a-Si:H TFTs, the ITO anodes are connected to the source terminals of TFTs, and the data voltages applied on the gate are shared between the TFT gate-source and the OLED bias voltage because a-Si:H TFTs are NMOS devices. As a result, the data voltages have to be increased to accommodate the sharing of data voltages. In contrast, pentacene TFTs are PMOS devices, and because the OLEDs are connected on their drain terminals, the data voltages we applied are completely dropped at the gate-source junction.
**5.2.3 Mask Layout**

The overall layout of the display backplane is shown in Figure 5-5. It falls within 2.5" × 2.5" square in order to be easily used with our lithography tools. Clearly visible in the center of the panel is a 48 × 48 OTFT pixel array with long leads to the edges for external driving connections, three passive pixels (one 2 × 2 mm², two 1 × 1 mm²) with long leads to the right edge, an 8 × 8 small OLED array, 3 groups of various storage capacitance (0.75 pF, 1.2 pF, 2.4 pF) single pixels, 4-transistor-driven OLED pixels, and structures for measurements of TFT stability. Besides that, we put many TFT testing structures and processing monitors, such as an array of test transistors for measurements of transistor uniformity, cross-over structures for a dielectric integrity test, parallel TFTs for off-current measurement, contact resistance measurement structures (transfer length method), and contact angle measurement pads.

Figure 5-5: Mask layout of display backplane.
Once the TFT backplane was fully fabricated, the OLED stack and cathode were deposited as blanket layers through shadow masks.

### 5.3 Fabrication Process

Figure 5-6 shows a cross section of the pixel, including the select TFT, storage capacitor, the drive TFT and OLED. And the thickness of layers is listed in Table 5-1.

![Diagram of pixel structure](image)

Figure 5-6: Cross-section of the OLED pixel on glass substrates.

The substrate is 0.7 mm glass coated with 85 nm ITO film. First, the ITO film was patterned by photolithography and wet etching (HNO$_3$:HCl:H$_2$O = 1:9:10) at 40 °C. A 50nm chrome gate layer was deposited by sputtering and patterned by wet etching. A 300 nm thick ion-mill sputtered SiO$_2$ was used as the gate dielectric and patterned with lift-off. The ion-mill sputtered SiO$_2$ was chosen for two reasons: first, it tends to have a smoother dielectric surface, and more importantly, it establishes an adsorbate for octadecyltrichlorosilane (OTS). Both will help pentacene grow in a more ordered manner. A 100 nm platinum source-drain layer was deposited by sputtering and patterned by lift-off. A self-assembled monolayer OTS was formed on the sample by vapor prime
in a vacuum oven for 3 hours, which played a key role in improving the pentacene TFT performance by lowering the surface energy of the dielectric [14]. A 50 nm pentacene layer was then thermally evaporated at 60 °C at a rate of 0.1 – 0.5 Å/s. Since pentacene thin film is normally in a light accumulation state on the field region, an isolation step was necessary to minimize the leakage current between adjacent devices and conduction lines. Regular photoresist was not suitable for this work because the organic solvents in photoresist will deteriorate the pentacene thin film [21]. Instead, in-house mixed polyvinyl alcohol (PVA) water based photoresist [61] was used to mask the active region, and reactive ion etching (RIE) oxygen plasma was used to remove field pentacene. 1 µm parylene was then coated by Labcoater 2010 and patterned by standard photolithography and RIE oxygen plasma dry etching. On the one hand, parylene was good insulator, and it passivated all the areas on the sample except the ITO anode area and the contact pads area; on the other hand, parylene has very low permeability to moisture, and it acted as an encapsulation for PVA, which otherwise results in the deterioration of OLED material. The OLED stack was deposited onto the TFT backplane through a shadow mask by thermal evaporation in an OLED deposition system. The organic layers were: 75 nm 4,4'-bis[N-(1-naphthyl)-N-Phenyl-amino] biphenyl (α-NPD) as the hole transport layer, and 75 nm tris (8-hydroxyquinoline) aluminum (Alq3) as the electron transport layer. Next, a 220 nm magnesium/silver alloy cathode was deposited through shadow mask. Finally, the OLED display area was encapsulated by a glass slide and sealed by UV cured epoxy.
Table 5-1: Thickness of layers for OLED pixel.

<table>
<thead>
<tr>
<th>Thickness (nm)</th>
<th>ITO</th>
<th>Gate metal</th>
<th>SiO₂</th>
<th>Pc</th>
<th>PVA</th>
<th>Parylene</th>
<th>NPB</th>
<th>Alq</th>
<th>Mg/Ag</th>
</tr>
</thead>
<tbody>
<tr>
<td>85</td>
<td>50</td>
<td>300</td>
<td>50</td>
<td>500</td>
<td>1000</td>
<td>75</td>
<td>75</td>
<td>220</td>
<td></td>
</tr>
</tbody>
</table>

Figure 5-7a shows a picture of a sample before OLED deposition and glass encapsulation. Figure 5-7b shows a microscopic view of the pixel in the array, in which the select line, data line, select TFT, storage capacitor, drive TFT and ITO anode are labeled.

5.4 Dielectric Integrity Improvement

In display applications, yield is very important; one component is gate dielectric integrity. Actually, we have seen failures of displays due to the gate to source/drain shorts. Therefore, we have designed a cross-over test vehicle, which has connected rows
of metal lines at the bottom layer, crossing over columns of metal lines at the top layer, sandwiched in between dielectric islands.

Among the possible good quality low temperature dielectrics were ion-mill sputtered silicon oxide, ion-mill sputtered aluminum oxide, room temperature PECVD SiN, and polymer material parylene-C. The ion-mill sputtered oxide was deposited at 80°C in order to lower the film stress. The room temperature SiN was deposited virtually around 60 °C due to the plasma heating. The parylene was deposited at room temperature with very low stress (<10^7 Pa for 1 µm film). A test of 20 crossover vehicles was carried out for all these dielectrics, and the yield was then calculated. Figure 5-8 shows the layout of the crossover test vehicle, in which all columns are tied together and lie down on the bottom, and there are 1, 2, 4, 8, 16, 32, and 64 rows running across the columns on top, respectively, while the dielectric layer is between the metals.

Figure 5-8: Cross-over test vehicle mask layout.
The cross-over I-V curves were measured for different dielectrics, and the results are summarized in Table 5-1. Clearly, the ion-mill sputtered oxides perform badly in terms of crossover yield with almost zero yield for 8200 crossovers. However, it yields relatively well at small number of crossovers. The RT SiN performs much better than ion-mill sputtered oxide with 80% yield at 8200 crossovers even under 100 V bias. 1µm thick parylene worked well in insulating too, yielding 90% at 8200 crossovers under 100 V bias. In the case of the TFT backplane, both the ion-mill sputtered oxide and the RT SiN could be conveniently deposited as gate dielectrics, and the RT SiN and parylene could easily be used for passivation layers.

Table 5-2: Crossover yield summary for different low temperature dielectrics.

<table>
<thead>
<tr>
<th></th>
<th>Bias</th>
<th>1 x 128</th>
<th>2 x 128</th>
<th>4 x 128</th>
<th>8 x 128</th>
<th>16 x 128</th>
<th>32 x 128</th>
<th>64 x 128</th>
</tr>
</thead>
<tbody>
<tr>
<td>300nm SiO₂</td>
<td>40V</td>
<td>89%</td>
<td>72%</td>
<td>61%</td>
<td>39%</td>
<td>11%</td>
<td>0%</td>
<td>0%</td>
</tr>
<tr>
<td>370nm Al₂O₃</td>
<td>40V</td>
<td>100%</td>
<td>95%</td>
<td>95%</td>
<td>80%</td>
<td>60%</td>
<td>35%</td>
<td>5%</td>
</tr>
<tr>
<td>300nm RT SiN</td>
<td>40V</td>
<td>100%</td>
<td>100%</td>
<td>100%</td>
<td>90%</td>
<td>100%</td>
<td>75%</td>
<td>85%</td>
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<tr>
<td></td>
<td>100V</td>
<td>100%</td>
<td>100%</td>
<td>100%</td>
<td>88%</td>
<td>94%</td>
<td>63%</td>
<td>81%</td>
</tr>
<tr>
<td>1µm Parylene</td>
<td>40V</td>
<td>100%</td>
<td>100%</td>
<td>100%</td>
<td>100%</td>
<td>100%</td>
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</tbody>
</table>

Besides dielectric integrity, good semiconductor/dielectric interface is also important for gate dielectrics in terms of TFT performance. The ion-mill sputtered SiO₂ normally shows a smooth surface with a mean-square roughness of about 2 Å, which is an important factor in growing the well-ordered pentacene thin film. More importantly, it establishes an adsorbate for a self-assembled monolayer of octadecyltrichlorosilane (OTS), which played a key role to improve the pentacene TFT performance by lowering the surface energy of the dielectric [14]. It nominally has a good breakdown strength of
8×10^6 V/cm [16], which, however, is hard to achieve for a uniformly large area due to possible pin-holes in the oxide.

Another possibility for a good quality gate dielectric is silicon nitride deposited by RT PECVD with a breakdown strength of 3 × 10^6 V/cm. One drawback of this film is that it typically has an RMS surface roughness of 20 Å and a peak-to-valley roughness of 200 Å. Pentacene TFTs fabricated using this rough SiN have shown field-effect mobility of ~ 10^{-3} cm^2/V-s. Devices made using OTS treated RT SiN showed improved performance, but mobility was still limited to less than 0.1 cm^2/Vs. The poor device performance compared to SiO_2 gate dielectric pentacene TFTs is attributed to the large surface roughness of the RT SiN films and the difficulty in forming a high quality OTS monolayer on SiN.

Then a SiN/SiO_2 bi-layer gate dielectric process was used to take advantage of the combination of good qualities of SiN and SiO_2 films. SiN film is used to improve the dielectric strength, while sputtered SiO_2 smoothes the surface and makes it easily treated by OTS. The bi-layer normally consists of a thick layer of SiN, typically 200 nm thick, followed by a thin layer of SiO_2, usually 100 nm thick. The surface roughness of the bilayer is about 20 Å rms and about 200 Å peak-to-valley measured by AFM over a 5 µm × 5 µm area. Field-effect mobility for bilayer gate dielectric pentacene TFTs with OTS treatment is usually about 0.5 ~ 1.0 cm^2/Vs.
5.5 Test Results

5.5.1 Pentacene OTFT Backplane

After the backplane fabrication, samples are tested and characterized in terms of both TFT performance and process yield. Figure 5-9 shows the typical characteristics of the drive TFT. Figure 5-9a is a plot of drain current versus gate-source voltage at drain source voltage of -40 V, from which the TFT characteristics of mobility, threshold voltage, sub-threshold slope and on-off ratio can be extracted out. Figure 5-9b is a plot of drain current versus drain-source voltage for a range of gate-source voltage. The drive TFT provides a saturation current of 70 µA at -40 V drain-source voltage, which clearly satisfied our design requirement. TFT characteristics were extracted: the saturation field-effect mobility is 0.6 cm²/Vs, the threshold voltage is 12.6 V, the sub-threshold slope is 2.5 V/Dec, and on/off ratio is greater than $10^7$.

![Figure 5-9](image)

Figure 5-9: Typical drive-TFT characteristics: (a) $I_D$ vs. $V_{GS}$, (b) $I_D$ vs. $V_{DS}$.
OLED is a current driven light-emitting device, i.e., the brightness is directly proportional to the current of the drive TFT, which demands TFT uniformity in the array. A 105 drive TFT uniformity test array (W/L = 200 µm / 20 µm) on the sample is measured; the most important parameters, field-effect mobility and threshold voltages, are plotted in Figure 5-10. With a 94.2% yield for the array, statistics on threshold voltage show 13.7 V mean value, 0.78 V standard deviation, and 0.078 standard error; statistics on field-effect mobility show 0.584 cm²/Vs mean value, 0.017 cm²/Vs standard deviation, and 1.7×10⁻³ standard error.

![Test of TFT Uniformity](image)

**Figure 5-10**: Mobility and threshold voltages for a 105 drive-TFT uniformity test array.

Although the data here shows that we can achieve relative uniform TFT performance, it is still not good enough for a display application, so certain compensation circuits may be needed in the pixel design, which, however, increase the complexity of pixel circuits.
5.5.2 Pentacene OTFT Stability

Stability is another critical issue for display application. A bias stress test ($V_G = -40$ V, $V_{DS} = -40$ V) was carried out on the pentacene OTFT for various amount of time. Figure 5-11 shows the TFT characteristics before and after the bias stress. Clearly, a few voltages are observed on the threshold voltage shift after a 20-minute bias stress. This definitely will affect OLED brightness during its operation. Very little literature discusses the bias stress effect of pentacene. However, Knipp suggests that the shift of threshold voltage in pentacene TFTs may be due to a reversible structural change in the pentacene film, which is induced by the accumulation of either holes or electrons and which creates deep localized states near the interface [62]. Even though the problem can be made less critical by using lower driving voltage on OTFT due to improvement on OLED turn-on voltage and current efficiency, further improvement of the stability of pentacene OTFTs are still needed. Otherwise, a more complex pixel driving circuit are desired, which, however, tends to increases the driving circuit complexity and decrease the yield.

![Bias stress test of drive-TFT](image)

Figure 5-11: Bias stress test of drive-TFT.
5.5.3 Integration of OTFT and OLED

After the OLED deposition and encapsulation, the passive OLED pixel is tested first. Figure 5-12 shows the I-V characteristics of a passive OLED pixel with an area of 2×2 mm². The OLED has a turn-on voltage of around 2.2 V and shines green light when biased above 10V.

![I-V characteristics of a passive OLED pixel.](image)

Figure 5-12: I-V characteristics of a passive OLED pixel.

The active OTFT driven OLED pixel is also tested. Figure 5-13a shows the OTFT and OLED integration schematic, and Figure 5-13b plots OLED current under different data voltages. Because a few micro-ampere is more than enough to drive our OLED pixel, apparently, OLED can be easily driven by pentacene OTFT. The cathode voltage is shared between the TFT and OLED, and the measurement in a discrete pixel shows that OLED only takes 9 V of the total 40V when at full brightness because of high channel and contact resistance of pentacene OTFT.
Figure 5-13: (a) OLED active pixel schematic and (b) OLED current under different data voltages.

5.5.4 Display Array Pictures

Figure 5-14a,b show a 48 × 48 array driven with all the pixels in the on and off state. As figure 5.1 shows, the display is driven at the following conditions: $V_{DD} = 20 \text{ V}$ and $V_{CA} = -10 \text{ V}$. At the all-on condition, $V_{SELECT} = 0 \text{ V}$ and $V_{DATA} = 0 \text{ V}$, while at the all-off condition, $V_{SELECT} = 0 \text{ V}$, $V_{DATA} = 30 \text{ V}$. Figure 5-14c shows the array in the stripe pattern.
Figure 5-14: A 48 × 48 pixel array driven with all the pixels in the (a) all-on, (b) all-off states and stripe pattern.

There were many noticeable defects in the display since the process was not being done in a clean room. Several pixels were on when they were supposed to be off, and they were off when they were supposed to be on. The large number of defects demonstrates how important it is to process in a clean environment in order to yield large area electronics. Attempts at minimizing the number of defects were made by reducing the number of particles and more thoroughly cleaning the substrates during the process. While it was difficult to demonstrate a defect free display, the goal of demonstrating that pentacene TFTs could be used to supply sufficient current for OLED was accomplished.

5.6 Flexible OLED Display

With a pentacene OTFT driven AMOLED display demonstrated on glass substrates, the next natural step is to go flexible. While there have been several examples of flexible OLED displays [63-66] there have not been any demonstrations of organic TFT driven active-matrix OLED displays fabricated on polymeric substrates. Displays on
polymeric substrates have advantages in both function and cost. With the advantages of a low processing temperature, it is possible to use low cost manufacturing methods such as roll-to-roll processing and thereby produce inexpensive displays. In addition, flexible substrates make the display more attractive because it is flexible, lightweight, and rugged. In some applications, the displays may have less stringent requirements on performance. For example, a display with less than 100% pixel yield, low resolution, or a short lifetime may be acceptable. Here, we demonstrated the preliminary results on pentacene OTFT driven active-matrix OLED displays on flexible polymeric substrates.

5.6.1 Technical Challenges

The technology of flexible OLED displays covers many components and supporting technologies which are still under development. These technologies must be compatible and converge to enable a truly flexible display. The necessary technologies include robust flexible substrates, barrier layers, thin film transistors, transparent conducting materials, flexibility of thin films, encapsulation layers and so on, which have been thoroughly reviewed by Crawford in his book of flat panel display technology [67]. We will cover some difficulties and challenges that resulted from the transfer of our technology to polymeric substrates, which include the substrate selection, dimensional stability, surface smoothness and surface passivation.
5.6.1.1 Substrate Selection

Clarity of the film is important for bottom emissive displays, and a total light transmission (TLT) of 85% over 400–800 nm is required. Among many possible polymeric substrates, polyethylene naphthalate (PEN), polyethylene terephthalate (PET), polycarbonate (PC), and polyethylene sulfonate (PES) are potential substrate materials for these kinds of applications. Although they share some common properties, they are different in some respects, such as glass transition temperature, thermal shrinkage, linear expansion coefficient, chemical resistance, and moisture absorption. Sheraw has demonstrated pentacene OTFT driven polymer-dispersed liquid crystal displays on PEN substrates [68]. Although PET shows properties that are inferior to other films, like low glass transition temperature around 80°C, higher thermal shrinkage, and poor chemical resistance, it has the advantage of low cost. To really take advantage of the low temperature process in organic TFT fabrications, we chose to use PET film as our substrate material. The preliminary demonstration of flexible active matrix OTFT/OLED display on PET substrates justifies the possibility of other polymeric substrate materials including PEN, PC and PES.

The PET films with a nominal thickness of 125 µm were used as the substrate material. They were first cleaned by a thorough rinse in acetone and IPA. They were then heated at 150 °C in a vacuum oven for several hours to reduce the level of moisture and volatile contaminants and to pre-shrink the material for improved thermal dimensional stability prior to the processing. The films are laminated to glass carriers using a
removable pressure-sensitive silicone-gel adhesive, as described in Chapter 2, to improve thermal coupling, maintain a flat surface, and provide rigid support during processing.

5.6.1.2 Dimensional Stability

Dimensional stability is critical in enabling a film to ensure precision registration of the different layers in the final device and for the multi-layer device to be able to withstand thermal cycling. Plastic films undergo a variable and undesirable change in dimensions at the glass transition temperature ($T_g$), due to both molecular relaxation events associated with the increased mobility of the polymer chains and also ‘shrinkage’ or ‘expansion’ associated with the relaxation of residual strain within the oriented parts of the film structure. These changes in the plastic film usually directly affect the integrity of the thin film on top. For example, we have observed that chromium thin film buckled and SiN film cracked after heat cycles on PET substrates because of too large of thermal expansion. To estimate the substrate shrinkage, a technique which calculates the misalignment of registration marks between layers has been used. Figure 5-15 shows an example.
The smaller and brighter marks are from the top metal layer, and the bigger and darker marks are from the bottom gate metal layer. The total shrinkage is the sum of the shift of top registration marks with respect to bottom marks. The relative shrinkage can be calculated by total shrinkage divided by physical dimension between the marks on two sides. Normally we observed shrinkage of ~ 1000 ppm for PET substrate and ~ 500 ppm for PEN substrate after our OTFT processes. Large shrinkage not only requires large tolerance in mask design, but also hurts the integrity of the films deposited on the substrates.

Usually pre-annealing the substrate can greatly reduce shrinkage. Basically, we bake the polymeric film first in a vacuum oven for 12 hours at a temperature higher than their glass transition temperature and lower than their soften point if they don’t have an melting point. For example, we pre-anneal PET and PEN films at the temperatures of 150°C and 170°C, respectively. The substrates with pre-annealing show much smaller shrinkage after the sample fabrications. Figure 5-16 compares the relative shrinkage of PET substrates with and without pre-annealing after OTFT fabrication process.
Figure 5-16: The relative shrinkage, after every OTFT fabrication step, of PET substrates with and without pre-annealing.

With pre-annealing the substrate shrinkage decreases from ~ 1000 ppm down to ~ 200 ppm and the shrinkage tends to level off after a few steps as well. This level of shrinkage makes the pattern shifts still within the 10 µm design tolerance and allows us to use the same masks designed for the glass substrate. It is noteworthy that the substrate shrinkage is complicated: sometimes it shows relative expansion rather than monotonous shrinkage, which may be the result of swelling due to solvents and water uptake. To minimize this effect, we put a layer of RT PECVD SiN as a passivation layer for the PET substrate. Also, the high Young’s modulus of this inorganic film will also help prevent further dimensional change.

5.6.1.3 Surface Quality

The substrate surface smoothness is critical to pentacene OTFT performance. Pentacene thin film tends to form smaller grains on a rough dielectric, and the TFTs show
lower mobility. Because the add-on fabrication processes basically duplicate the surface smoothness, the thin film deposited on top will show similar roughness as the substrate, if not worse. Figure 5-17 shows an AFM image of the PET substrate surface before any process, from which we can extract the mean square roughness and peak to valley roughness of 10 Å and 90 Å, respectively. The surface smoothness is worse than silicon and glass substrates, but still a relatively acceptable number to have mediocre-performance pentacene TFTs.

![AFM image of the PET substrate surface.](image)

Figure 5-17: AFM image of the PET substrate surface.

Although the PET films show relatively smooth surface microscopically, they also come with surface scratches, spikes, and defects. Figure 5-18 shows an example of surface scratches on PET substrates, which may influence the integrity of subsequent layers such as barrier and conductive coatings. To solve this problem, we need a better manufacturing of polymeric films, especially on the surface quality. Otherwise, a planarization layer has to be used to smooth the surfaces [67].
The cleanliness of the flexible substrates is also essential to ensure the integrity of subsequent layers such as the conductive coatings and dielectric layers. Without the harsh cleaning procedures like that used for inorganic substrates, particulates on the surface of polymeric substrates surfaces may also be an issue for the yield of display.

5.6.1.4 Chemical Resistance

A wide range of solvents and chemicals is used when processing the various layers in the display, and the effect of water and solvent absorption will have a considerably detrimental effect on dimensional stability. This will become increasingly important as processing moves towards roll to roll.

An inorganic layer, 500nm RT PECVD SiN, is used to passivate the plastic substrates, which protects the substrates from the fabrication process and helps maintain substrate dimensional stability by minimizing solvent or moisture up-take. Since the
Young’s modulus of this inorganic layer is much higher than plastic film, even the thin film helps to maintain the substrate dimensional stability.

### 5.6.2 Fabrication Process

The fabrication process was similar to that used on glass substrates. Figure 5-19 shows the cross-section of the pixel on the PET substrates. The only difference is that a layer of 500 nm RT PECVD SiN was first used to passivate the polymeric substrate so that we could treat the substrate like a glass substrate to some extent. As we mentioned earlier, the passivation SiN layer will protect PET film from solvent and water moisture adsorption and help restrain the substrates from dimensional shrinkage during the process.

![Cross-section of the pixel on PET substrates](image)

Figure 5-19: Cross-section of the pixel on PET substrates.

We treated the SiN passivated PET substrate like a glass substrate, and pentacene TFTs were fabricated on top for the display array. Then the blank layer of OLED stack (60 nm NPB + 50 nm Alq) and aluminum cathode were evaporated through a shadow
mask on the sample. Figure 5-20 shows the microscopic view of a pixel after the OLED deposition. The scan line, data line, select TFT, storage capacitor, drive TFT, and OLED emission area are clearly shown in the picture.

![Microscopic view of pixel on PET substrate after OLED deposition.](image)

Figure 5-20: Microscopic view of a pixel on PET substrate after OLED deposition.

Unlike the OLED display on glass substrates, the OLED display array on PET substrates doesn’t have an encapsulation on top. To elongate its lifetime, we store and test the OTFTs in a glove box.

### 5.6.3 Test Results

#### 5.6.3.1 Pentacene OTFT on PET substrates

Similar procedures were used to test the OTFTs on PET substrates. As we mentioned earlier, the SiN layer usually shows a rough surface and the devices built on top normally show lower mobility than that of smooth surfaces. Figure 5-21 shows the
typical characteristics of drive OTFTs on PET substrates, from which the saturation field-effect mobility, threshold voltage, sub-threshold slope and on-off ratio can be extracted as $0.2 \text{ cm}^2/\text{Vs}$, $0.4 \text{ V}$, $2.5 \text{ V/Dec}$, and greater than $10^7$, respectively. Apparently, it is not quite as good as the results on glass substrates, mostly due to the SiN passivation layer induced rough substrate surfaces. However, we believe the smoothness of this SiN layer could be improved by changing the deposition conditions.

Figure 5-21: Typical OTFT characteristics on PET substrates. (a) $I_D \sim V_{GS}$, (b) $I_D \sim V_{DS}$.

The 105 drive OTFT uniformity test array ($W/L = 200 \mu\text{m} / 20 \mu\text{m}$) on the sample was measured; the most important parameters, field-effect mobility and threshold voltages, were plotted in Figure 5-22. Statistics on threshold voltage show $0.54 \text{ V}$ mean value with $0.55 \text{ V}$ standard deviation; statistics on field-effect mobility show $0.15 \text{ cm}^2/\text{Vs}$ mean value with $0.009 \text{ cm}^2/\text{Vs}$ standard deviation. Although the field-effect mobility is lower than that of glass substrates, the standard deviation data are actually smaller than that of glass substrates. The results suggest that we can still achieve relative uniform TFT performance for display applications.
Figure 5-22: Mobility and threshold voltages for a 105 drive-OTFT on PET substrates.

Even though the problem can be made less critical by using lower driving voltage on the OTFT due to improvement of OLED turn-on voltage and current efficiency, further improvement of the performance of pentacene OTFTs on PET substrates is desired.

5.6.3.2 Integration of OTFT and OLED

After the OLED deposition, the passive OLED pixel is tested first. Figure 5-23 shows the I-V characteristics of a passive OLED pixel with an area of 2×2 mm². This OLED shows similar on-current characteristics but has a little higher off-current than Kodak OLED on glass substrate, which is unimportant because we don’t have a negative bias on OLED cell during display operation.
Figure 5-23: I-V characteristics of a passive OLED pixel on a PET substrate.

The active OTFT driven OLED pixel was also tested. Figure 5-24 shows the active pixel OLED current under different data voltages. Apparently, OLED current is modulated by data voltage on drive OTFT.

Figure 5-24: Active OLED pixel current under different data voltages on a PET substrate.
**5.6.3.3 Display Array Test**

The display sample was bonded to the driving electronics using flexible conducting tapes, and Figure 5-25 shows the flexibility of the display sample.

![Flexibility of display sample after bonding of flexible tapes.](image)

Figure 5-25: Flexibility of display sample after bonding of flexible tapes.

Then the array of the $48 \times 48$ pixel OLED display was tested. Figure 5-26 shows the brightness grayscale for the array driven with all the pixels under different data voltages. Apparently, the OLED pixel brightness responds to data voltage well.

![Display brightness under different data voltages.](image)

Figure 5-26: Display brightness under different data voltages.

To test the data voltage storage function on the storage capacitor in the pixel, a stripe-pattern picture was fed into the display and Figure 5-27 shows the result. Although it has some defects, the dark and bright stripes are clearly observable. This result suggests that we did demonstrate a working display on a PET substrate.
Figure 5-27: Stripe pattern demonstrated by the display on a PET substrate.

Figure 5-28 also shows the display function at bent condition during the operation. Although there are many noticeable defects on the display since the process is not being done in a clean room, the goal of demonstrating that pentacene OTFTs could drive OLED pixel on flexible polymeric substrates was accomplished.

Figure 5-28: A 48×48-pixel active matrix OLED display lit up at bent condition.
5.7 Summary

We have integrated pentacene OTFT with an OLED pixel with the help of PVA and parylene bilayer passivation technique, and designed and fabricated pentacene OTFT driven 48×48-pixel AM OLED displays on both glass and PET substrates. To our best knowledge, they are the largest AM OLED displays on glass substrates and the first ever demonstration on flexible PET substrates. However, the process still needs to be improved to have a better yield. These results demonstrate that pentacene TFTs are viable candidates for active-matrix OLED displays.
Chapter 6
Conclusions and Future Work

6.1 Flexible a-Si:H Thin Film Electronics

Irradiation and mechanical tension induced changes were evaluated for arrays of a-Si:H TFTs on Kapton® polyimide substrates. Significant changes were found on TFTs after irradiation with fast electrons at a dose of 1 Mrad. However, the irradiation-induced changes were essentially removed by post-irradiation thermal annealing at 200 °C for two hours. There are few changes observed for TFTs after a substrate tension of about 2500 psi. These results indicate that flexible substrate a-Si:H TFTs can be readily engineered to survive the mechanical stresses of space deployment and may survive moderate irradiation with minor changes in device characteristics.

For the first time, ungated n+ μC-Si and gated a-Si:H strain sensors were designed and directly fabricated on 50 μm thick polyimide substrates. These sensors were characterized with different bending conditions, perpendicular, parallel, and 45 ° to the bias direction, and with different bending diameters, 90 mm, 76.6 mm, 50.4 mm, 41.7 mm, and 25.5 mm. The sensitivity of both types of strain sensors produces a large variation between 45 ° strain and parallel or perpendicular strain with respect to the bias direction. Compared with metallic foil strain sensors, the ungated μC-Si sensor and gated a-Si:H sensor use two orders of magnitude less area and power consumption. In addition,
combination with a-Si:H TFTs can also allow large arrays of strain sensors to be easily fabricated on flexible substrates.

Using a regular recipe, a-Si:H TFT performance deteriorates rapidly with the decrease of process temperature. By adding hydrogen dilution, a-Si:H TFT deposited at 150 °C shows similar performance as that of the 250 °C process. The stability of the TFT was tested using bias stress tests, and TFTs of both processes showed close results. Simple digital circuits, like a digital inverter and a ring oscillator, were demonstrated and characterized. These results suggest that low-temperature H₂-dilution a-Si:H TFTs are viable for practical applications and potentially useful to take advantage of low temperature polymeric substrates.

6.2 Pentacene OTFT Driven OLED Display

We have integrated pentacene OTFT with OLED pixel for displays. In order to avoid the PVA moisture degradation on OLED lifetime, inorganic material like RT PECVD SiN and organic material like parylene have been tried to directly passivate pentacene OTFTs. However, the UV light during SiN deposition basically kills pentacene thin film, and parylene-pentacene interaction degrades the device mobility by 50%. For the time being, we solved the problem by using a PVA and parylene bilayer passivation structure.

We designed and demonstrated pentacene OTFT driven 48 × 48 pixel AM OLED displays on both glass and PET substrates. To our best knowledge, these demonstrations are the largest on glass substrates and the first ever on flexible PET substrates. The
pentacene OTFTs were characterized in terms of their performance, uniformity and stability. These results demonstrate that pentacene TFTs are viable candidates for active-matrix OLED displays.

6.3 Future Works

Both ungated μC-Si and gated a-Si:H strain sensors can sense the strain up to 0.2% due to the yield point of inorganic materials. However, the inorganic thin film will tend to crack or peel off of polymeric substrates when the strain is higher than that. In addition, the large mismatch between the stiffness of inorganic thin film and polymeric substrate materials tends to less represent the strain in substrates. Organic conductors or semiconductors have a larger yield point in terms of strain, which can be used to expand the sensing range. In addition, the low Young’s modulus in organic materials will match better with polymeric substrates.

For pentacene OTFTs, we need better passivation techniques than the PVA process. Although the bilayer of PVA and parylene passivation temporarily solved the problem, the water moisture permanently trapped in PVA. Either inorganic or organic materials which are compatible with pentacene thin film need to be developed for practical applications. The first possible candidate is parylene-N, which owns similar properties as parylene-C while seems to show less effect on top of pentacene thin film.

OLED displays are current driven devices; the display brightness is directly proportional to its current. Although our process can make relatively uniform pentacene OTFT in terms of performance, further improvements are still needed for practical
display applications. Alternatively, more complex design in the pixel structure is desired to compensate the small non-uniformity in OTFT performance. Pentacene OTFTs also showed instability under bias stress condition, which is a serious problem for practical applications, especially when the device is under constant bias condition. On the one hand, the TFT suffers from self-heating under the constant bias stress during the operation which may therefore affect the contact of devices. Furthermore, this instability can be inherently due to either the trap state generation in semiconductor itself or the charge generation in dielectrics. More efforts to solve this problem are necessary before use in any commercial applications is a reality.
REFERENCES


Vitae

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