The Pennsylvania State University

The Graduate School

TOWARD UNDERSTANDING THE ELECTRICAL PROPERTIES OF METAL/SEMICONDUCTOR SCHOTTKY CONTACTS: THE EFFECTS OF BARRIER INHOMOGENEITIES AND GEOMETRY IN BULK AND NANOSCALE STRUCTURES

A Dissertation in

Engineering Science and Mechanics

by

Karthik Sarpatwari

Submitted in Partial Fulfillment

of the Requirements

for the Degree of

Doctor of Philosophy

August 2009

The thesis of Karthik Sarpatwari was reviewed and approved* by the following:

Osama O. Awadelkarim
Professor of Engineering Science and Mechanics
Dissertation Co-Advisor, Co-Chair of Committee

Suzanne Mohney
Professor of Materials Science and Engineering
Dissertation Co-Advisor, Co-Chair of Committee

Bernhard R. Tittmann
Professor of Engineering Science and Mechanics
Schell Professor

Samia A. Suliman
Assistant Professor of Engineering Science and Mechanics

Suman Datta
Associate Professor of Electrical Engineering

Judith A. Todd
P. B. Breneman Department Head of Engineering Science and Mechanics

*Signatures are on file in the Graduate School.

Abstract

The work presented in this thesis comprises of two parts. Part I deals with Schottky contacts to the wide bandgap (WBG) semiconductors SiC, GaN and ZnO. These semiconductors offer great promise for a wide variety of electronic and optoelectronic applications. Schottky barriers to WBG semiconductors are attractive in particular for high temperature/high power diodes, photodetectors, and gas sensors. However, the Schottky barriers exhibit non-ideal behavior, due in part to inhomogeneities originating from immature crystal growth and device processing technologies. Apart from being a versatile electronic component, the Schottky diode is a valuable test structure. The Schottky contact is routinely used to probe substrate and epilayer quality by different electrical characterization techniques.

It is well established that the current-voltage-temperature (I-V-T) characteristics of Schottky contacts are routinely affected by the presence of barrier height inhomogeneities (BHI). Consequently, Schottky diode parameters such as the Schottky barrier height and the Richardson constant extracted using the I-V-T measurements can deviate from their actual values. The effects of BHI on the extracted Schottky barrier height have been studied in the literature. However, the effects of BHI on the Richardson constant have not been thoroughly explored and are the focus of the first part of this thesis. Based on the inhomogeneous Schottky barrier model provided by Tung, a new method for the extraction of the Richardson constant is developed. The new method is applied to the Richardson constant determination of n-type ZnO and GaN. Excellent agreement with the theoretical value is obtained in both cases.

The advent of the nanoelectronics era has resulted in the Schottky contact evolving from the relatively simple, planar structure into a more complex structure.

Compared to bulk Schottky contacts, the Schottky barrier properties are expected to be widely different at the nanoscale. For example, the I-V characteristics of nanoscale Schottky contacts are affected by the contact size and geometry. Due to the increased surface-to-volume ratio, the conduction properties of nanoscale Schottky contacts are also influenced by surface conditions such as surface charge and traps. Depending on contact size, geometry and surface conditions, an enhanced tunneling current contribution can be expected, further distorting the I-V characteristics from the simple thermionic emission model. Determination of the true Schottky barrier height in nanoscale contacts to semiconductor nanowires is important from both technological and fundamental scientific perspectives. In the second part of this thesis, we employ a simulation-based approach to study the conduction properties of an axial Schottky nanocontact to a surround-gate nanowire. A systematic study of the effects of surface charge on the I-V characteristics of the axial nano Schottky/nanowire system is undertaken. Based on the study, a method is proposed to extract the true Schottky barrier height from the I-V characteristics. The proposed method can serve as a valuable aid for interpreting experimental I-V data and can facilitate exploration of size effects on the Schottky barrier formation at the nanoscale.

Table of Contents

List of Figures

List of Tables

Acknowledgments

I have spent several days delaying to write this segment of the thesis and it is entirely due to the fact that it is hard to convey the immense sense of gratitude i feel towards everyone involved directly or indirectly in shaping my graduate life at Penn state. Any combination of words i come up with feel inadequate, and keeping this in mind, i feel a simple thank you is the best i can do. I thank my advisors for their guidance and support all through these years. Without their inputs, ideas and effort, i would not have been able to complete this work. I would like to thank Dr.Samia for serving on my committee and also offering help and encouragement on numerous occasions. My other committee members, Dr.Tittmann and Dr.Suman Datta, have been immensely gracious with their time and inputs that have been really useful to me. My thanks to several other faculty members across Penn state who have been very kind in clearing road blocks so that i could carry on my research smoothly. Dr.Vijaykrishnan, Dr. Jian Xu, Dr. Ashok, Dr. Tom Jackson, Dr. Theresa Mayer, Dr. Mark Horn have provided access to their lab equipment, resources and time that have helped me immensely. Interaction with their graduate students have often resulted in very fruitful discussions and for that i am grateful. Special thanks to Dr.Steve Durbin and Dr.Martin Allen for their fantastic collaborative effort that has formed the basis for a large part of this thesis. The department of Engineering Science and Mechanics has provided support for my graduate studies all through these years and i am really thankful for the help and support. The ESM faculty and staff have been kind to answer my questions and guide me through different stages of my graduate life. For that, i am really thankful.

Over the few years, i have been at Penn State, i have had the opportunity to collaborate with several people. It will be hard to name each and every one of them but i will try: Lucas, Subbu, Shiva, Suresh, PP, HP, Charan, Martin, Fan, Alan, Brian, Bob, Chad, Nick, Heayoung. I am confident that i have forgotten several others but i still acknowledge their help on countless occasions. My friends at PCG and elsewhere have often readily offered help through their words (sometimes loaded with sarcasm) and actions (sometimes proven counter-productive). Finally,

my family...

Several years ago, i received a call some time in the night that i got into Penn state and I still remember the excitement i felt. Late in to the night, my parents and I discussed about the prospect of getting a PhD. My mother had named me Karthik based off a character in one of her favorite novels. Although i think she intended me to be a different kind of doctor, it will not be too bad if i do end up as the other doctor. I am really grateful to have a very dear, caring family and an incredible wife. They have offered their criticism in their own unique ways and made the whole job about ten times easier (approximately). Thank you all!

Chapter 1

Schottky barrier: Modeling and Physics

1.1 Semiconductor surface

The surface plays an important role and can often dictate the electronic properties of a semiconductor device. The surface is basically an extended defect where the periodic structure of the crystal is interrupted. An unpassivated surface such as a freshly cleaved wafer has an abundance of dangling bonds that represent a non-equilibrium energy state. Under such conditions, the surface can spontaneously re-construct to form a lower energy surface structure. Surface re-construction is driven by the need to maintain charge neutrality and is dictated by chemical bonding [1]. For example, silicon is tetravalent and covalently bonds using sp^3 orbitals. At the surface of a single crystal silicon cleaved along the <111> direction the tetragonal

bonding of the surface atoms are severed resulting in an sp^2 hybridization and a lone pair. The lone pair has a higher energy as compared to a bond pair and contributes to the overall surface energy. The lone pair also interacts with the sp^3 orbitals and distorts the tetrahedral structure. In response, the surface tends to re-construct to minimize the free energy of the surface, and also return to overall charge neutrality. Kinetic constraints imposed by growth conditions, foreign contaminants and defects can all affect the final atomic structure of the surface.

The surface of a semiconductor inherently contains some surface states that are characteristic of the semiconductor surface. Depending on the detailed electronic and atomic structure at the surface, discrete energy states can be distributed within the bandgap of the semiconductor. Surface states can be of either acceptor or donor types with the density of donor type being larger closer to the conduction band minima (CBM). On the other hand, the acceptor states tend to have larger density close to the valence band maxima (VBM), and at a certain energy location within the band gap the acceptor state density matches the donor state density. The cross-over point is known as the charge neutrality level (CNL) and has special significance in the physics of heterojunctions and interfaces.

The relative difference between CNL and the equilibrium Fermi-energy level determines the intrinsic band bending, charge state and magnitude present at the semiconductor surface. When the Fermi-level is below the CNL, positive charge is stored in the surface states, and for an n-type semiconductor a slightly downward

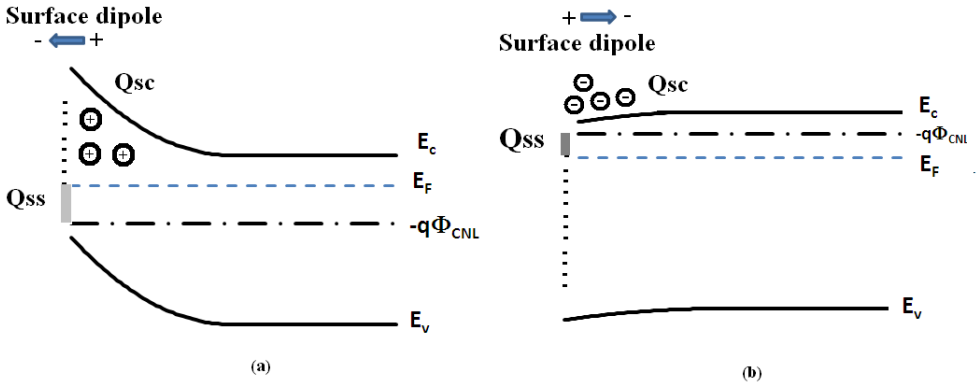

Figure 1.1. Band bending and surface dipole under surface depletion and accumulation conditions

band bending and surface charge accumulation results. On the contrary, when the CNL is above the Fermi-level, a net negative charge appears in the surface states, and consequently, the bands bend upwards resulting in a surface depleted condition [2]. Figure 1.1 shows the two different scenarios discussed above. The charge stored in the surface states (Q_{ss}) along with the charge induced in the semiconductor (Q_{sc}) forms a surface dipole layer. A flat band condition arises when the CNL coincides with the Fermi-level position, but in most semiconductors, the CNL differs from the Fermi level by a few tenths of an eV giving rise to either surface depleted or accumulated conditions. The magnitude and direction of the surface dipole is dependent on the semiconductor band structure, semiconductor growth and surface preparation conditions. Apart from the dependence of the surface properties on the intricate atomic and electronic structure of the native surface, the surface properties can be also influenced by the introduction of a metal layer on the semiconductor.

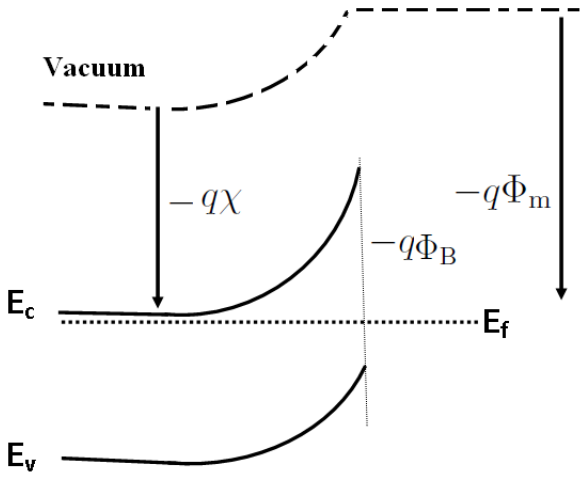

Figure 1.2. Band diagram of the Schottky metal/semiconductor contact under equilibrium conditions

1.2 Metal/semiconductor (MS) interface

A simple view of the MS interaction is shown as a band diagram in Figure 1.2. A Schottky contact results due to the workfunction difference between the metal and semiconductor. The Schottky-Mott model predicts that the difference between the metal workfunction (Φ_m) and the semiconductor electron affinity (χ) would equal the resultant barrier height (Φ_{B}):

$$\Phi_{\mathrm{B}} = \Phi_{\mathrm{m}} - \chi \tag{1.1}$$

The Schottky-Mott model predicts that for a given semiconductor the Schottky barrier height (SBH) changes along with the metal workfunction. However, experimentally measured SBH on several semiconductor systems often do not seem to follow eq. 1.1, as predicted by the Schottky-Mott theory. The simple view as-

sumed by the Schottky-Mott model is often violated at a real MS interface. The Schottky-Mott model is considered to describe the non-interacting limit of the SB formation models since it considers the SBH as a result of the bulk metal and semiconductor workfunction differences. The Schottky-Mott model does not place any emphasis on the MS interface properties, and hence, does not account for the effect of the metal/semiconductor interaction on the resultant Schottky barrier.

Over the past few decades, several studies have focused on extending the Schottky-Mott model to account for the wide range of deviations observed. Earlier approaches relied on the presence of a thin interfacial layer with high defect density to screen the effect of metal workfunction. Experimental evidence of SBH insensitivity to metal workfunction even in intimate MS contacts led to alternate approaches such as the metal-induced-gap-states. Subsequent approaches have almost always relied on the presence of the interface or surface states that can pin the Fermi level. The key difference between the various models is the dominant source for these interface states or pinning traps. These models can be collectively classified as *gap states* based models and are briefly examined next.

1.2.1 Gap state models

Apart from the intrinsic surface state distribution, gap states related to metal atoms, foreign contaminants or defects can also be present. A thin interfacial layer with inherently high defect density is often assumed to be present at the MS

interface. Surface states present at the interface have been suggested as a source for Fermi-level pinning. However, Fermi-level pinning has also been suggested at intimate MS interfaces, and to account for FL pinning, Heine proposed that the surface states are induced due to the interaction of metal with the semiconductor surface [3]. The metal-induced-gap-states (MIGS) model proposes that the electron wave function within the metal tails into the semiconductor giving rise to overlap of the metal and semiconductor conduction bands. As a result, electronic states can exist within the energy band gap, and for intimate MS interfaces these gap states can still pin the Fermi-level.

The primary effect of the surface states is to pin the surface Fermi-level, limiting the workfunction dependence of the obtained SBH. On the other hand, gap states can be induced through the metal deposition process resulting in defect creation. The unified defect-induced-gap-state (DIGS) model relies on pinning due to defects generated by the metal deposition process [4, 5].

Based on the MIGS approach, the barrier height can be related to the CNL and the pinning parameter ($S = \partial\Phi_{\mathrm{B}}/\partial\Phi_m$ [6]) through

$$\Phi_{\mathrm{B}} = \Phi_{CNL} + S(\chi_m - \chi_s). \tag{1.2}$$

In eq. 1.2, Φ_{CNL} is the CNL potential from the Fermi-level, χ_m and χ_s are the electronegativities of the metal and the semiconductor, respectively. In the case of strongly pinned interfaces, the SBH is independent of the metal workfunction and

is said to approach the Bardeen limit ($S = 0$). Strong surface Fermi-level pinning has been shown to occur for surface state densities exceeding 10^{13} cm^{-2} eV^{-1} [7]. For a weakly pinned surface, the SBH dependence on the metal workfunction approaches the Schottky-Mott limit, and in this case the value of S approaches 1.

The MIGS approach accounts for the semiconductor contribution through CNL (Φ_{CNL}) and the metal/semiconductor bulk contributions through the electronegativity difference. The SBH is determined primarily by the CNL (solely determined by the semiconductor) and the effect of secondary factors such as surface dipoles due to the electronegativity difference. Surface states or foreign contaminants can further contribute to the deviation.

Another approach that has been recently developed by Tung is based on the chemical interaction between the metal and semiconductor right at the interface [8]. Bond polarization (BP) theory, as proposed by Tung, accounts for the interaction between the metal and the underlying semiconductor through charge re-distribution that occurs at a metal/semiconductor interface. For a stable MS contact, chemical bonding occurs to some degree and this involves breaking of surface bonds and formation of new bonds. Brillson reported the dependence of the pinning parameter on the heat of formation and emphasized that for the case of a reactive MS interface the pinning was weak [9]. In the BP scenario, the MS interface properties are affected by all three components of the MS system: metal, semiconductor and the interface-specific region (ISR). In contrast to other models,

which account for the observed metal workfunction dependence solely through the bulk metal and semiconductor properties, the ISR is a direct result of the chemical interaction between the metal and the semiconductor atoms at the interface, and the surface charge distribution depends on the electronegativity difference between the atoms present at the interface. Prior to the metal deposition, the semiconductor atoms are involved in some kind of bonding with their nearest neighbors. The bond length is different from the bulk, and the surface structure is essentially disordered. A fraction of the surface atoms still have dangling bonds and are energetically favored to form new bonds. The presence of surface defects such as micropipes or dislocations further contributes to the complexity of the surface structure and introduces localized structural variations.

In order to obtain a more intuitive understanding of the BP model, consider two planes of atoms A and B located at the surface and just below the surface, respectively. The bond polarity between the two planes depends on the electronegativity difference and results in charge re-distribution between the involved atoms. When a plane of metal atoms (M) approaches the surface, the surface bonding picture changes to accommodate the incoming metal atoms. The interface structure is dictated by similar constraints of chemical bonding, free energy minimization and charge neutrality that govern the surface re-construction process. Depending on the electronegativity difference between M, A and B, one can envision a partial bonding to emerge between M, A and B planes. This process involves charge

transfer across the interface, and the final charge distribution is dictated by the interface structure and conversely the interface structure is refined by the charge transfer. The final ISR structure determines the bond length between the metal and semiconductor surface atoms, and this bond length can vary spatially across the interface (especially for polycrystalline metal films). The charge transfer across the MS interface results in an interface dipole that can vary spatially as well. The magnitude of charge transfer depends on the bulk metal and semiconductor properties (such as electronegativity difference and semiconductor ionicity) and the equilibrium bond length is specific to the interface (depends critically on growth and processing conditions). Hence, the resultant interface dipole depends on the bulk metal and semiconductor properties and also is characteristic of the specific interface structure.

The preceding discussion points to the fact that the barrier height depends on details of the interface structure. Specifically, a surface dipole layer induced by intrinsic surface states, defects, MIGS or possibly other sources affects the interface barrier height. In the case of polycrystalline metal contacts to a semiconductor, the surface dipole can vary spatially and can result in lateral variations of barrier height. The interface barrier height variation has a profound impact on the carrier injection and transport properties of a Schottky diode. Early evidence of the inhomogeneous nature of the Schottky contact was observed as low barrier regions within a high barrier height background [10]. The inhomogeneous nature

of the contact was attributed to non-uniform interfacial reaction of the metal with the semiconductor. Careful analysis of transport properties can be a valuable aid to develop, validate and understand the Schottky barrier formation mechanism. Advanced surface characterization tools such as the ballistic electron emission microscopy (BEEM), as well as scanning electron microscopy coupled with the electrical characterization methods, provide essential and comprehensive experimental data required to validate any proposed models. In the next section, we review the basics of carrier transport across Schottky contacts with a special emphasis on the inhomogeneous barrier framework.

1.3 Carrier injection and transport across the M/S interface

Transport across the metal/semiconductor system is dictated by carrier injection, trapping and carrier transport processes. The relative rates of these processes are generally bias and temperature dependent, and the conduction properties of the system are a result of an interplay between these processes. For example, in a Schottky contact to a moderately-doped semiconductor, at low bias values the conduction properties are limited by carrier injection over the barrier. However, in the case of low mobility and large trapping density materials such as organic semiconductors, the injected carriers need not be transported effectively. In such

cases, carrier transport and trapping/de-trapping mechanisms would determine the conduction behavior of the system. Carrier trapping/de-trapping and injection phenomena are usually temperature activated processes, and hence, their effect on conduction properties are heavily affected by the measurement temperature.

In the case of a Schottky contact to an ordered single crystal semiconductor, carrier injection rather than transport determines the conduction properties of the diode. Transport across a spatially homogeneous Schottky barrier, in the ideal case, is given by the thermionic emission theory. Carrier transport occurs by emission over the barrier, and the key assumption is that the Fermi-level remains constant across the depletion region. Under thermionic emission the emitted carries are termed hot carriers, since these carriers have higher energy compared to the carriers in thermal equilibrium within the metal. The emitted hot carriers loose their additional energy through collisions with the metal lattice and with other carriers.

1.3.1 Thermionic emission

Under thermionic emission theory, as proposed by Bethe, the current-voltage-temperature characteristics of the Schottky diode are given by

$$I = AA^{*}T^{2}\exp(-\beta\Phi_{\mathrm{B}})\exp(\frac{\beta V}{n})\left\{1-\exp\left(-\beta V\right)\right\}, \tag{1.3}$$

where A is the geometric area of the Schottky contact, A^* is the Richardson constant, and n is a phenomenological term known as the ideality factor. V is the voltage drop across the diode and is related to the applied bias V_a by $V = V_a - IR_s$, where R_s is the parasitic resistance. Figure 1.4 shows the typical forward bias I-V characteristics measured at room temperature. For an ideal diode, at low forward bias values, the I-V characteristics are linear on a semi-log scale. At higher current levels, the I-V characteristics are dominated by series resistance, and a sub-linear behavior is seen on the semi-log scale. In the reverse-bias regime, the current-voltage relation is expected to approach the saturation current (I_{sat}) given by

$$I_{sat} = AA^*T^2 \exp\left(-\beta\Phi_{\mathrm{B}}\right) \tag{1.4}$$

Experimental current-voltage-temperature (I-V-T) characteristics are often fitted to the ideal thermionic emission equation, and this exercise provides a baseline from which deviations are measured and interpreted. Traditionally, the extent of deviation from ideality is inferred through the extracted values of the ideality factor (n) and the barrier height (Φ_{B}). Under ideal conditions, the value of n equals 1 and the barrier height should equal the Schottky-Mott limit, $\Phi_m - \chi$. If one considers the effects of image force lowering, then the ideal values of n and Φ_{B} would be slightly different. The effect of image force lowering is a slight increase in the ideality factor and a corresponding lowering of the barrier height.

The image force controlled ideality factor can be estimated using

$$n_{if} \approx 1 + \frac{1}{4}\left[\frac{q^3 N_d}{8\pi^2 \epsilon_s^3 V_{bb}^3}\right]^{\frac{1}{4}}, \tag{1.5}$$

and the corresponding barrier lowering is given by

$$\Delta\Phi_{\mathrm{B}} \approx \left(\frac{q^3 N_d V_{bb}}{8\pi^2 \epsilon_s^3}\right)^{\frac{1}{4}}. \tag{1.6}$$

In equations 1.5 and 1.6, N_d is the semiconductor doping, V_{bb} is the band bending and ϵ_s is the dielectric constant of the semiconductor. The value of n_{if} depends on the doping density and, typically, ranges between 1.01 for moderate doping levels to about 1.03 for a heavily doped semiconductor. Extracted ideality factor values, however, tend to be much larger than the image force limit, and this suggests other dominant mechanisms such as tunneling across the barrier. Minority carrier injection can also contribute to the total current. Depending on the barrier profile, these mechanisms can also dominate the total current.

The extracted ideality factor and barrier height values exhibit bias and temperature dependence, and a variety of trends have been reported in the literature [11, 12]. The temperature dependence of the ideality factor and barrier height is often used to identify the dominant transport mechanisms (for example, [13, 14, 15]). Prior to the inhomogeneous Schottky barrier model, deviant trends exhibited by ideality factor and extracted barrier height were typically attributed to interface

and surface traps. A thin interfacial layer was assumed to be present at the MS interface that could influence the I-V-T characteristics. Interface traps or surface states (in the case of intimate MS interfaces) along with other mechanisms (such as field emission and generation-recombination) have been held responsible for greater-than-unity ideality factors. Recently, the notion of an inhomogeneous barrier has been gaining wide applicability and seems to be able to explain the wide variety of trends observed in real Schottky diodes [16, 17]. Prior to the inhomogeneous barrier models, analytic approaches implicitly assumed that the emission occurs over a spatially homogeneous barrier.

Apart from high ideality factors, a Schottky diode can exhibit a larger reverse leakage current than expected from thermionic emission theory. In some cases, a double diode behavior can be seen and has been reported for several semiconductor systems. Preliminary analytical approaches handled this behavior using a parallel diode approach, wherein two (or more) distinct regions with different barrier heights were assumed to contribute to the total current. The current-voltage relation in this case is a sum of all the individual diode contributions and can be written as

$$I(V_a) = A^* T^2 \sum_i A_i \exp\left(-\beta \Phi_{bi}\right) \{\exp\left(\frac{\beta V_a}{n_i}\right) - 1\}, \tag{1.7}$$

where A_i, n_i and Φ_{bi} are, respectively, the area, ideality factor and barrier height of the i^{th} diode.

1.3.2 Observation of barrier height inhomogeneities (BHI)

Electrical characterization of Schottky contacts provides valuable insights into the metal/semiconductor interface, near-surface and bulk semiconductor properties. For this reason, the Schottky contact is often used as a test structure to assess intrinsic material quality, and the Schottky test structure is also a valuable process monitor (for deposition processes). Quasi-static electrical characterization such as current-voltage-temperature (I-V-T) and capacitance-voltage-temperature-frequency (C-V-T-ω) measurements are simple to set-up but can provide a comprehensive set of information. Coupled with physical analysis methods such as ballistic electron emission microscopy (BEEM), scanning electron microscopy (SEM) and other microscopy methods, the interface and bulk semiconductor properties can be thoroughly investigated. Apart from quasi-static electrical characterization, transient measurements such as deep level transient spectroscopy (DLTS) and random telegraph signal (RTS) noise measurements can give information about energetically shallow and deep defects.

Experimental evidence for lateral variations of the barrier height were observed in the form of double diode behavior, and the variations were attributed to a non-uniform interfacial reaction [18]. Several electrical, optical and physical characterization tools have been used for observing and verifying barrier inhomogeneities in different metal/semiconductor systems. The effect of barrier height inhomogeneities on I-V-T characteristics has been reported by several groups (for example,

[19, 20, 21, 22]). The I-V-T measurements are, by far, the most sensitive electrical characterization methods. On the other hand, capacitance-voltage measurements are more affected by the mean barrier height and are relatively insensitive to barrier height fluctuations. Internal photoemission (IPE) studies have also revealed the presence of barrier inhomogeneities [23]. RTS noise from the inhomogeneous Schottky diode has been associated with charge trapping and de-trapping by interface traps in defective patches. RTS noise signal has been used to probe the energy location and density of traps in the patch [24].

Depth-resolved cathodoluminescence spectroscopy (DR-CLS) studies on Ni/SiC Schottky diodes reveal spatially non-uniform interface traps giving rise to spatial variation in Fermi-level pinning [25, 26]. In GaN Schottky diodes, inhomogeneities are associated with the presence of threading dislocations [27]. In the case of SiC, the inhomogeneities are associated with few extrinsic localized defects [28, 29]. Metal grain boundary and morphology induced inhomogeneities have been reported in [30, 31]. Different sources have been cited for various metal/semiconductor systems, and the source and nature of inhomogeneity is not always apparent from any individual measurement.

Comprehensive physical characterization using ballistic electron emission microscopy (BEEM), scanning tunneling microscopy, scanning capacitance microscopy, and atomic force microscopy to map the location variation of barrier height has been reported [28, 32, 33, 34, 35, 36]. These studies reveal a broad distribution

of barrier heights and propose that the low barrier patches lie at the tail end of the distribution. Low barrier patches around localized defects in GaN have also been detected using these characterization methods. These measurements are usually coupled with the observed current-voltage characteristics to obtain a complete physical and electrical picture of the diodes. For I-V analysis, over the past three decades, different theories have been developed and these are examined in the following sections.

1.4 Framework for barrier height inhomogeneities

1.4.1 Zero-order model

Earlier analytical approaches analyze the observed double diode behavior as a non-interacting parallel diode model. In the non-interacting parallel diode model, the metal/semiconductor interface is assumed to be comprised of distinct low barrier and high barrier regions. The net current in the non-interacting model is given by the sum of all contributions from the individual diodes. The non-interacting parallel diode model is a good approximation when the spatial variation of the barrier height is larger than the depletion region. The model tends to err significantly when the lateral variations in contact barrier are at a length scale comparable to the depletion region width. In general, the interaction between high and low barrier regions needs to be considered and an outline of the method developed by

Tung is examined next.

1.4.2 First-order interacting model

As stated earlier, the conduction properties of a real MS interface tend to deviate from ideality on a regular basis. The observed non-ideal behavior can be broadly categorized into double diode behavior and a slight curvature in the semi-log I-V plot. Based on the discussion on the underlying mechanism of SBH formation in polycrystalline metal contacts, it can be conjectured that the SBH can vary according to the spatial variation of the interface dipole. The interface dipole magnitude depends on the metal, semiconductor and the ISR properties, and based on the BP approach, the magnitude would depend on the surface charge and the equilibrium bond length between the metal and surface semiconductor atoms. The dipole magnitude would further depend on the presence of extrinsic defects and other contaminants. It is evident that the spatial variation of the interface dipole (and hence, the SBH) can be quite complicated depending on the atomic and electronic structure of the interface. However, for the sake of simplicity, two special cases that are of great interest will be considered here.

The first case is the presence of highly localized SBH patches within an otherwise homogeneous barrier. Localized Fermi-level pinning due to defects of extrinsic origin can give rise to such a scenario. Depending on the size and nature of these patches, double diode behavior can be observed in the I-V characteristics. On

the other hand, a more subtle variation of the SBH can be envisioned that, on average, can be modeled as a Gaussian distribution of barrier height. In this case, the I-V characteristics would be smeared out resulting in ideality factors being greater than 1. Even for these simplified cases, the interface dipole is spatially extended and the interaction between high and low barrier regions is not analytically tractable and numerical solutions need to be sought. However, in the case of a rapidly fluctuating SBH, the interface dipole can be approximated as a point dipole to facilitate finding a closed-form expression for the I-V characteristics of an inhomogeneous SBD.

Utilizing the point dipole approximation, Tung derived analytic expressions for the effects of barrier height inhomogeneity on the current-voltage-temperature characteristics. Conduction through low barrier regions (also termed as patches) can be dictated by the high barrier regions depending on the size of the low barrier patches and also the difference between the low and high barrier height regions ($\Delta = \Phi_{\mathrm{BH}} - \Phi_{\mathrm{BL}}$). The surrounding high barrier region can give rise to a saddle point potential within the low barrier region, and this saddle point potential governs carrier emission for the low barrier regions. The saddle point potential is also bias and temperature dependent and results in a wide variety of possible I-V characteristics. Figure 1.3 shows a technology computer aided design (TCAD) simulation of the influence of a surrounding high barrier region on the potential profile within the low barrier region. The high barrier region can modulate the

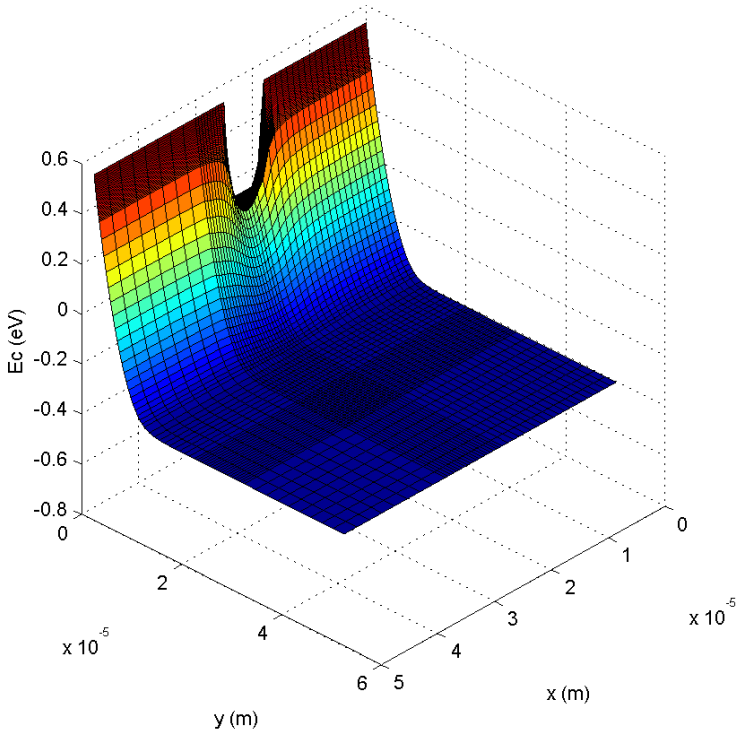

Figure 1.3. Pinch-off effect of the high barrier region on the embedded low barrier region

effective low barrier diode area and the effective barrier height seen by the carriers emitted within the low barrier region.

Diodes exhibiting double diode behavior are characterized by anomalous high current at low forward bias values and are modeled as low barrier patches mixed within a uniform high barrier region (Φ_{BH}). The low barrier regions are characterized by the local barrier height (Φ_{BL}) and the size of the patch (R_0). The double-diode behavior is modeled using a dilute density of low barrier patches (C_1) that have very similar Δ and R_0 values. Tung proposed a reduced patch parame-

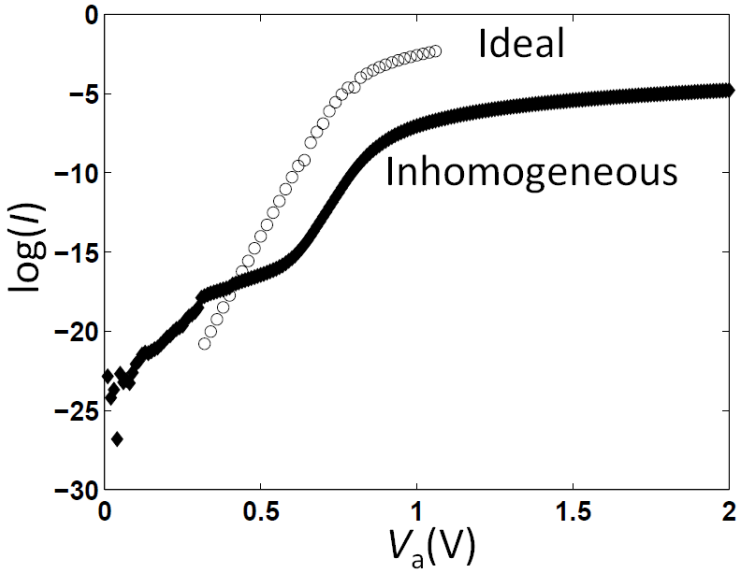

Figure 1.4. Typical current-voltage response of an ideal and inhomogeneous diode

ter, γ $(= 3\left(\frac{\Delta R_0^2}{4}\right)^{\frac{1}{3}})$, to couple the effects of Δ and R_0 on the I-V characteristics using a single parameter [17].

Tung's parameters capture the inhomogeneity phenomenon, and unlike the conventional Schottky diode parameters, these parameters are bias and temperature independent (termed as *true system* parameters). γ is used to qualify (and quantify) the effect of inhomogeneity on the I-V characteristics. For example, if two patches of different interfacial barrier height difference (different Δ) and different patch sizes have the same γ, these patches are identical in terms of their effect on I-V characteristics (for patch sizes less than the depletion region width).

The double-diode characteristics can be determined by patch density (C_1), γ and the homogeneous high barrier height (Φ_{BH}). The contribution from the low barrier patches characterized by a single γ value towards the total current can be

expressed as

$$I_L = \left(\frac{4\pi C_1 \gamma}{9\beta\beta_1}\right) \exp\left(\beta\beta_1\gamma\right) I_{L0}, \tag{1.8}$$

where

$$I_{L0} = A^* T^2 \exp(-\beta\Phi_B) \left(\exp(\beta(V_a - I_L R_{sp})) - 1\right). \tag{1.9}$$

In eq. 1.8, $\beta_1 = (V_{bb}/\eta)^{1/3}$, with $\eta = \epsilon_s/qN_d$ is defined as the doping parameter. η captures the BHI sensitivity of the substrate depending on the doping density. In the case of higher doping density (small η), the low barrier regions are harder to pinch off and can dominate the total current. The total current is a sum of the low barrier current contribution (I_L) and the homogeneous high barrier contribution (obtained using eq. 1.3).

Apart from the double diode behavior, barrier inhomogeneities can have other less pronounced effects. In diode systems that exhibit large ideality factors ($n > 1$), the I-V characteristics typically exhibit a curvature on a semi-log scale. This curvature gives rise to a bias dependence of the ideality factor and barrier height. In other words, the extracted ideality factor and barrier heights depend on the bias range selected for curve-fitting. In the inhomogeneous barrier model framework, such deviations are explained in terms of small fluctuations around the homogeneous barrier height. The low barrier current contribution, in this case, is given

by

$$I_L = \left(\frac{8\pi C_1 \sigma^2}{9\beta_1}\right) \exp\left(\frac{\beta^2 \beta_1^2 \sigma^2}{2}\right) I_{L0}. \tag{1.10}$$

In eq. 1.10, σ is the spread of the patch parameter distribution. At a real MS interface, the low barrier patch scenario could be much more complex. A more generalized formulation would provide additional flexibility of using one equation to model any kind of I-V characteristics. The total current contribution from the low barrier patch distribution is given by

$$I_L = \left(\frac{4\pi C_1}{9\beta\beta_1^2}\right) \left\{\gamma + \beta\beta_1\sigma^2\right\} \exp\left(\beta\beta_1 \left(\gamma + 0.5\beta\beta_1\sigma^2\right)\right) I_{L0}. \tag{1.11}$$

Physically, the generalized model can be interpreted as the presence of distinct low barrier patches with a certain size distribution. The generalized distribution is characterized by the distribution mean (γ_0), spread (σ) and peak value (C_p) and can be reduced to either of the above models and the homogeneous case under appropriate conditions such as:

- $\gamma_0 > 0$ and $\sigma = 0$ would yield the double diode behavior
- $\gamma_0 = 0$ and $\sigma > 0$ would model diodes exhibiting high ideality factor
- $\gamma_0 = 0$ and $\sigma = 0$ reduces to the homogeneous Schottky barrier model

Measured I-V characteristics are typically fitted with the appropriate analytic

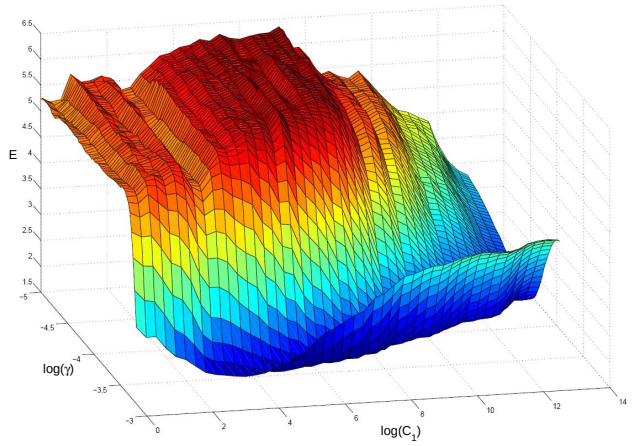

Figure 1.5. Energy topography in C_1 and γ space for inhomogeneous diodes

expressions provided by Tung, and the fitting exercise is used to estimate the patch parameters. The fitting process minimizes the error between simulated and experimental I-V characteristics. The error function, typically termed the energy function, is defined as

$$E = \frac{1}{N} \sum_{i=1}^{N} \left| \ln \left(\frac{I_{\text{exp}}}{I_{\text{pre}}} \right) \right|. \tag{1.12}$$

E is a function of the Schottky diode parameters (C_1, γ, Φ_{BH}). The energy topography as a function of C_1 and γ is shown in Figure 1.5.

The energy terrain in the case of an inhomogeneous diode is quite rough and exhibits a plethora of local minima. The presence of local minima is both a result of increased number of parameters and also their contrasting effects on the I-V

characteristics. The parameter search space is quite large compared to the ideal diode case. Hence, the presence of local minima and considerably large search space warrants a different approach to curve fitting. Deterministic methods such as the multi-dimensional Newton-Raphson method require a good initial guess and also are susceptible to getting stuck at local minima. A heuristic approach such as the simulated annealing algorithm can sample large search domains uniformly and can avoid getting stuck at local minima [37].

The energy terrain shown in Figure 1.5 has the key features of local minima and an extended global minima contour. The extended global minima suggests that multiple solution points would satisfactorily fit the I-V curves. The simulated annealing algorithm is quite adept at moving out of local minima but is weak in approaching global minima. The presence of an extended global minima contour further complicates the task of finding optimal solutions.

In the literature, several groups fit the I-V characteristics to obtain certain C_1 and γ values. However, the energy terrain clearly indicates that multiple points would satisfy the equations. The presence of an extended global minima line indicates that a unique patch parameter set cannot be obtained from pure I-V-T fitting. The preceding example shows that the effects of barrier height inhomogeneities on the extracted Schottky diode parameters needs to be considered carefully.

Different transport mechanisms have different signature I-V-T characteristics,

and it is often hard to de-couple the effects of individual mechanisms completely. Analysis of the I-V-T characteristics aims to filter these interlaced effects, in an effort to find the true Schottky barrier height. These analytical approaches further aid in the understanding of the basic SBH formation mechanism. Engineering contacts to semiconductors with the desired properties can then rely on solid principles based on an understanding of the formation mechanism.

The work presented here can be considered a two-part thesis: the first part concerns with Schottky diode parameter extraction in wide bandgap (WBG) semiconductors. The growth and processing of WBG semiconductors are still far from mature, and, hence, Schottky contacts to these semiconductors are more likely to be affected by BHI. Experimental determination of the Richardson constant for WBG semiconductors has been largely inconsistent and often deviate from the theoretically expected values. Hence, these contacts can provide the required experimental data for a BHI aware I-V-T analysis.

The second part of the thesis focuses on the analysis of I-V characteristics of Schottky contacts at nano dimensions. Schottky contacts to nano structured semiconductors (such as nanowires) provide access to the Fermi-level pinning phenomenon at the nano scale. The study of these two parts is further motivated next, in terms of fundamental importance and technological relevance.

1.5 Wide bandgap (WBG) semiconductors

As the power electronics industry seeks higher power and faster switches, it is widely accepted that silicon technology is fast approaching its theoretical limits [38, 39]. Research into WBG semiconductors is based on the exceptionally attractive set of properties of this class of semiconductors. Properties such as high thermal conductivity, high breakdown field strength, low thermal generation leakage, and direct nature of the bandgap lead to excellent figure-of-merit in many electronic devices [40, 41, 42, 43]. Apart from power electronics applications, WBG semiconductors are of key importance to optoelectronic applications such as light emitting diodes (LEDs) and lasers.

WBG semiconductors occur almost exclusively as compound semiconductors of binary, ternary and quaternary systems (except for diamond). Given the breadth of possible applications and issues concerning the varied aspects related to WBG semiconductors, we consider the three most important candidates: SiC (IV-IV), GaN (III-N) and ZnO (II-VI). The experimental data presented in this thesis is on Schottky contacts to these semiconductors as well. Hence, the subsequent overview is also pertinent to the on-going discussions concerning parameter extraction in BHI affected Schottky contacts.

Table 1.1. Summary of basic properties and comparison between 4H-SiC, GaN and ZnO

Property	4H-SiC	ZnO	GaN
Band gap(eV)	3.2 [44]	3.3 [45]	3.4 [46]
Breakdown field (MV/cm)	2.5 [47]	11 [48]	2.2 [49]
Thermal conductivity (W/cm.K)	3.3 [50]	1.3 [48]	2.1 [46]
Ionicity	0.65	1.9	1.23

1.5.1 Substrate growth processes

The availability of low cost, high quality single crystal wafers of WBG semiconductors has not been achieved yet. Growth processes similar to the mature liquid phase Czokralski method for silicon are not directly available for most WBG semiconductors. Silicon carbide (SiC), for example, does not melt but directly sublimes at around 2100 ℃ [51]. Bulk single crystal SiC wafers have been grown using the modified Lely's approach. Also, silicon carbide exists in several stable polytypes, hence, polytype mixing is a big problem in silicon carbide. Epitaxial growth of one polytype would contain inclusions of other polytypes [52, 53, 54], and since different polytypes of silicon carbide have widely varying electronic properties, such inclusions would lead to inconsistent behavior. Apart from polytype mixing, point and extended defects such as comet tails and micropipes can also contribute to inferior substrate quality. Even though significant advancements have been achieved in the single crystal quality, the dislocation defect density still remains pretty high [55, 56, 57].

III-N semiconductors, on the other hand, are grown using different epitaxial,

physical and chemical deposition processes. For GaN, the epitaxial layer is usually grown on a hetero substrate with a buffer layer to reduce dislocations [58]. In some cases, laterally-extending overgrown structures have been shown to have fewer dislocations [59]. A variety of substrates such as sapphire, SiC, silicon and copper have been used to grow gallium nitride (GaN) epitaxial layers [60, 61, 62]. High dislocation densities are characteristic of GaN and AlGaN films, and these dislocations have been cited as the source for excess reverse bias leakage in Schottky diodes to these semiconductors [60, 63, 64].

ZnO is another WBG candidate that has received renewed interest for applications in optoelectronics and space electronics. Besides being a wide band gap semiconductor, ZnO has the additional advantage of the availability of high quality single crystal substrates [65, 45]. High purity ZnO has been reported to be fabricated using different methods such as hydrothermal [66], melt-grown [67], vapor-phase [68], epitaxial [69] and pulsed laser deposition [70] methods. However, device performance in ZnO has been shown to be greatly affected by intrinsically occurring point defects related to oxygen vacancies [71].

1.5.2 Doping, etching and annealing processes

n-type doping of WBG semiconductors is facilitated readily due to the presence of intrinsic, shallow defects, but p-type doping of WBG semiconductors has been more challenging. Although low resistivity p-type epilayers on GaN have been achieved,

the activation efficiency is still low and requires a careful annealing process [72, 73]. High temperature annealing is typically required to activate dopants in WBG semiconductors. High temperature annealing of SiC has been shown to cause marked increase in surface roughness through a process known as step bunching (in SiC) [74]. Dopant diffusion is also prohibitively slow and requires very high temperatures for reasonable diffusion profiles [75, 73, 76]. Dopant incorporation can be achieved using ion implantation but at the cost of introducing dislocation loops and defects [77, 73, 78]. Although in the case of III-N semiconductors, the dopants are typically introduced in situ during epitaxial growth.

The high bond strength of SiC and GaN makes it difficult to find optimal wet etching recipes, and so dry etching methods need to be relied on. Dry etching methods such as reactive ion etching (RIE) coupled with ion implantation creates crystal damage that is, in general, difficult to anneal out in these semiconductors. Amorphization of the crystal structure due to implantation damage has been found to be difficult to anneal out, as the re-crystallized structure is not of high quality. Also, in SiC, the recrystallizing domains can be of different polytypes giving rise to complex defect structures [79, 80]. On the other hand, ZnO has been shown to be amenable to wet etching processes, and this further contributes to low surface defect densities achievable on ZnO [81].

1.6 Contacts to WBG semiconductors

Interest in Schottky contacts to WBG semiconductors is rooted in the expectation that the wider bandgap would allow fabrication of Schottky contacts with large barrier heights. In contrast to Si Schottky contacts, Schottky contacts to WBG semiconductors such as SiC and GaN have shown stronger response of the measured SBH on the metal workfunction, indicating weaker Fermi-level pinning [82, 83, 84, 85, 86]. Kurtin et al. suggested the interface behavior parameter dependence on semiconductor ionicity [87]. For covalently bonded semiconductors, the pinning parameter, S, is expected to be low and hence for elemental semiconductors, the Fermi level pinning is expected to be strong. On the other hand, for ionic semiconductors, large values of S have been observed. For compound semiconductors with a large electronegativity difference between the cation and the anion (large ionicity), the pinning is expected to be weak. For SiC, the electronegativity difference is about 0.65 and a pinning parameter value of about 0.7 has been reported [82, 88].

Spatially and energetically localized defects have been shown to influence the FL pinning scenario in SiC [26]. The effect of pinning through surface states is lower in SiC because the pinning surface states are not located within the band gap. This has been attributed to the relatively large ionicity of SiC (compared to Si). The effect of ionicity has been proposed by Kurtin et al., where the penetration depth of MIGS is inhibited due to the polar nature of the bonds. In this case,

the screening effect of MIGS is substantially reduced leading to FL unpinning. Another suggested explanation for the relatively small FL pinning effect is the surface state bunching in ionic semiconductors, which results in surface states aggregating towards the band edges rather than being distributed across the bandgap [85]. Apart from the intrinsic surface states and MIGS, defect-induced gap states can still pin the Fermi level. The growth and processing technology of SiC is still far from mature, and the abundance of several stable polytypes gives rise to a significantly high defect density in the substrate. 3C and 8C stacking faults within the 4H-SiC matrix have been shown to form localized defects within the bandgap, and these defects can partially pin the Fermi level [89]. However, these pinning defects tend to be localized and so the Fermi level pinning is also localized. Weak Fermi-level pinning has been observed in GaN, and this has been attributed to the large ionicity of GaN [85, 86, 90, 91]. In the case of GaN, FL pinning due to interface states localized around surface pits due to the presence of threading dislocations has been suggested. For GaN, a pinning parameter of about 0.4 has been reported suggesting weak FL pinning scenario in the case of GaN [90]. In ZnO, FL pinning associated with point defects such as oxygen vacancies has been proposed [92].

Despite weaker Fermi-level pinning in most of the WBG semiconductors, it is widely recognized that Schottky contacts to WBG semiconductors are affected by barrier height inhomogeneities. Defects at the surface that are inherent to the

growth processes or form due to subsequent processing steps can greatly impact the Schottky barrier properties. Schottky contacts to the WBG semiconductors are affected by the presence of BHI, which can distort the observed I-V characteristics. The source of BHI can be extrinsic in nature (defects such as micropipes) or can be intrinsic to the MS interface (MIGS), but the overall effect of these mechanisms results in spatial variation of the surface dipole layer. Depending on the nature of the surface dipole layer, a wide variety of I-V-T characteristics can be observed. Localized defects such as micropipes can give rise to double diode behavior and a more gradual variation in surface dipole can give rise to n greater than 1.

Traditionally, analysis of I-V-T characteristics attempts to extract the true Schottky barrier parameters such as the homogeneous barrier height and Richardson constant. The I-V-T characteristics can be fitted using Tung's model to extract the patch parameters. Methods that attempt to incorporate the effects of BHI on the observed I-V characteristics utilize the extracted patch parameters as a basis for subsequent analysis. For example, the extracted patch parameters can be used to modify the original Richardson plot. The Richardson plot is constructed from the I-V-T characteristics and is used for the experimental determination of the Richardson constant.

1.7 Thesis organization: Part I

Part I of this thesis discusses carrier injection and transport properties of Schottky contacts to WBG semiconductors. Chapter 2 deals with the effects of minority carrier injection on the measured I-V and capacitance-voltage (C-V) characteristics. Schottky diodes are ideally majority carrier devices; however, a small fraction of minority carriers can be injected across the interface. Minority carrier injection is of special significance in diodes with large barrier heights such as those to WBG semiconductors.

Chapter 3 focuses on understanding the effects of BHI on the extracted Schottky contact parameters through the use of a simulated diode system. The system is based on the analytic expressions provided by Tung. Based on the understanding obtained from the simulated system, a new method that provides an effective way to extract Schottky diode parameters is presented. The application of the proposed approach to the experimentally measured I-V-T characteristics of n-ZnO and n-GaN Schottky diodes is also discussed. The remainder of the thesis deals with Schottky contacts at nano-dimensions. The motivation to study Schottky contacts at nano-dimensions and the technological relevance is addressed next.

1.8 Contacts at nano dimensions

1.8.1 Scaling of Schottky contacts

The inception of the integrated circuit (IC) (in 1958) and subsequent efforts devoted to transistor scaling has revolutionized the semiconductor industry. Complementary metal-oxide-semiconductor (CMOS) has emerged as the industry choice IC, and transistor scaling primarily concerns with the scaling of the metal-oxide-semiconductor field-effect-transistor (MOSFET). Technological innovations required to continuously shrink the MOSFET have also been valuable for other fields such as power electronics, microelectro and mechanical systems (MEMS) and nanotechonology. With device critical dimensions (CD) down to a few tens of nanometer, it is widely believed that transistor scaling is approaching hard physical limitations. Although the focus remains intensely on the ability to shrink the transistor size, it is being widely recognized that contacts to these devices require attention as well [93, 94]. Tailoring the contact properties such as contact resistance is important to reduce parasitic series resistance-induced device performance degradation. At the nanoscale, the contact properties may be greatly different from the bulk case, and it is highly desirable to tailor the contact properties to meet device design constraints. An understanding of the size effects on the contact properties and an appreciation of the limitations can help engineer optimal contacts.

The nanoelectronics era has also witnessed the transformation of the Schot-

tky structure from a simple planar and bulk contact to a more complex set of structures. Self-assembled metal nano dots and nano clusters on semiconductor substrates [95, 96], aligned nanotubes and nanowires [97, 98], axially-aligned contacts to nanotubes and nanowires [99], and conductive AFM or STM probing of semiconductor substrates are some examples where Schottky contacts at the nanoscale come into play.

Apart from the technological importance, understanding the contact properties of nano-size semiconductors is important from a fundamental scientific perspective. Contacts to nano dimensional structures provide a means to understand the basic formation mechanism of Schottky barriers. At the nanoscale, the interaction between the metal and semiconductor can be markedly different from the bulk case. The differences between the two cases can be organized into two categories. The first category accounts for differences based on the interface and surface effects, and the second category captures contact size and geometry related effects.

1.8.2 Interface and surface effects

In the simple SB formation model, the Schottky barrier is influenced by the metal and semiconductor workfunctions and the magnitude and sign of the interface dipole. The interface dipole is dictated by the detailed electronic structure of the interface that forms as a result of the metal/semiconductor interaction. The interaction between metal and semiconductor results in the formation of MIGS, and

the presence of defects can further contribute to additional gap states. In contacts at nano-dimensions, the interaction between metal and semiconductor changes due to the reduced length scale. The reduced dimensionality of nanostructures can affect the distribution of MIGS due to a change in screening length and, in effect, alter the interface dipole magnitude [100]. A systematic and thorough investigation of the FL pinning strength at the nanoscale is still lacking; however, a few reports have suggested that the FL pinning is expected to be weaker at the nanoscale [101, 102].

Compared to the bulk contacts, the surface plays a much more significant role in nano-dimensional contacts due to an increased surface area/volume ratio. For the sake of comparison, consider a bulk Schottky contact of 1 μm $\times 1\mu$m area to a cube of silicon and a 1 μm long nanowire of 50 nm radius. In the case of the bulk contact, for about 10,000 atoms of bulk atoms, there is one surface atom. On the other hand, in the case of the nanowire, there is one surface atom for just 10 bulk atoms. The energetically active surface atoms can acquire charge through interaction with ambient molecules (such as H_2O), and this surface charge can alter the nanowire conduction properties. Due to increased surface/volume ratio, the surface charge can be comparable to the intentional doping level of the nanowire.

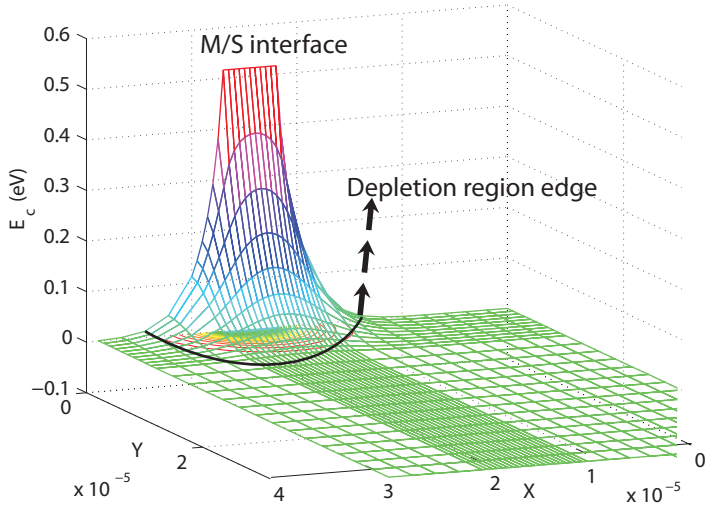

Figure 1.6. Barrier profile for the case of a nanoscale contact to a bulk semiconductor. Figure also shows the isopotential contours indicating the depletion region edge profile.

1.8.3 Size and geometry effects

In the conventional bulk, planar Schottky contact, the metal and semiconductor contact size and geometry do not affect the barrier profile. The electrostatics at the metal/semiconductor interface changes as one enters the nanoscale regime. The difference from the bulk, planar Schottky contact is reflected in the Poisson's equation. The Poisson's equation is given by

$$\frac{\partial^2 \Phi}{\partial^2 x} + \frac{\partial^2 \Phi}{\partial^2 y} + \frac{\partial^2 \Phi}{\partial^2 z} = -\frac{\rho}{\epsilon_s}, \tag{1.13}$$

where Φ is the electrostatic potential, ρ is the space charge density and ϵ_s is the semiconductor permittivity. The Poisson equation (eq. 1.13) along with the appropriate boundary conditions dictates the potential barrier shape.

In a bulk, planar Schottky contact, the electric field components along the MS

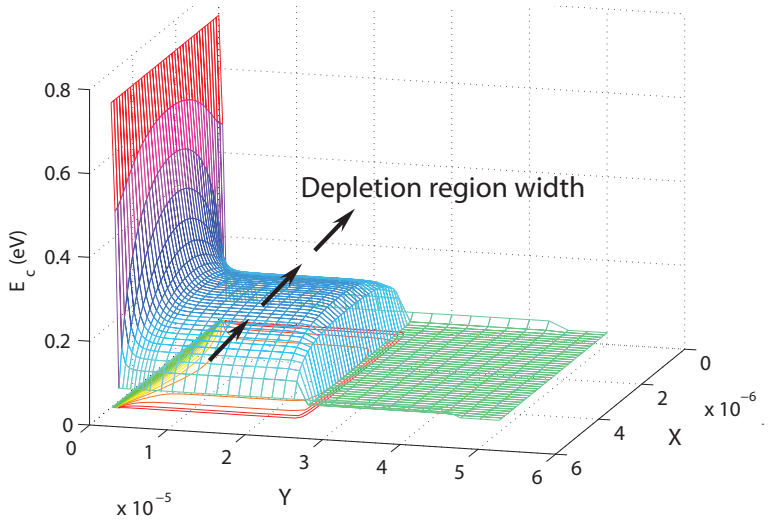

Figure 1.7. Barrier profile for a nanocontact to a nanowire with positive charge placed along the nanowire length. Isopotential contours depicting the depletion region edge have also been shown.

interface ($\vec{E_x}$ and $\vec{E_y}$) are negligible compared to the electric field in the direction perpendicular to the MS interface. In this case, the 3D Poisson equation can be reduced to a 1D case, and the depletion region surface is a plane parallel to the MS interface. However, for nano Schottky contacts, the lateral field components cannot be ignored, and in this case, the more generalized 3D Poisson's equation needs to be considered. Figure 1.6 shows the barrier profile for the case of a nanocontact to a bulk semiconductor. Unlike in the bulk contact, the depletion region edge is not parallel to the MS interface and, further, is thinner along the contact edges.

Figure 1.7 shows the barrier profile for the case of a nanocontact to a nanowire under the influence of positive charge placed along the nanowire length. In this case, the depletion region edge can have both axial and radial variation. The

depletion region profile can further be influenced by the presence of surface charge along the nanowire length. Radial variation of the depletion region width can be observed with the barrier width being thinner at the nanowire periphery. From a contact size and geometry perspective, these examples illustrate that the Schottky contact at the nanoscale can be widely different from the bulk case. The barrier shape dictates the conduction properties of the nanowire and the Schottky contact I-V characteristics cannot be explained using simple thermionic emission theory. Enhanced tunneling current contribution is possible in nano Schottky contacts due to barrier thinning. Special attention needs to be devoted to account for these effects, and wherever applicable additional transport mechanisms such as field-emission need to be considered.

1.9 Thesis organization: Part II

The focus of the second part of this thesis is to analyze the I-V characteristics of axially-aligned Schottky nano contacts to nanowires, in an effort to extract the true Schottky barrier height from the I-V characteristics. The I-V characteristics of the metal/nanowire system deviate from the thermionic emission theory due to contact geometry and surface charge effects discussed earlier. TCAD based simulations are used to understand the geometry and surface condition effects on the conduction properties of the metal/NW contact. Based on the TCAD simulations, a new approach is proposed to extract the Schottky barrier height.

Extracting the true Schottky barrier height is essential to investigating the barrier formation mechanisms at the nanoscale.

Chapter 4 details the simulation methodology and the results obtained from application of this methodology to different simulation cases, and experimental I-V characteristics are presented. As mentioned earlier, the nanowire surface can affect the conduction properties of the nanowire.

Finally, chapter 5 presents the adaptation of the charge pumping method to probe the interface quality of nanowire based field-effect-transistors. This method can be used to assess the dielectric/nanowire interface quality and can provide valuable inputs to the simulation methodology of parameters such as interface trap density. Chapter 6 concludes the thesis and outlines future directions to further extend the work developed in this study.

Chapter 2

Minority carrier injection in Schottky contacts to WBG semiconductors

2.1 Introduction

Schottky barrier diode is called a majority carrier device since the total current flowing through the Schottky diode is mainly due to the flow of majority carriers. In general, the total current flowing through a Schottky barrier diode is a sum of the majority carrier and minority carrier contributions. The minority carrier contribution is usually much smaller than the majority carrier current and does not affect the observed I-V characteristics. The presence of minority carrier injection current in Schottky diodes was first proposed by Scharfetter [103]. Scharfetter proposed the minority carrier injection efficiency (γ) parameter as a measure of the influence of minority carrier injection on the I-V characteristics. The minority

carrier injection efficiency is the ratio of the minority carrier current density to the total current density and can be written as

$$\gamma = \frac{J_p}{J_n + J_p} \sim J_p/J_n, \tag{2.1}$$

where J_p is the minority carrier current density and J_n is the majority carrier current density.

γ increases with increasing forward current density suggesting that at large forward bias, minority carrier injection can be quite large. Yu and Snow showed that minority carrier injection is larger in systems with larger barrier height and low substrate doping density [104]. The efficiency of a Schottky contact to inject minority carrier depends on the Schottky barrier height, semiconductor doping density, and minority carrier recombination velocity at the ohmic contact end. Minority carrier injection is also affected by the carrier recombination velocity at the ohmic contact. The recombination velocity at the ohmic contact influences the spatial profile of the minority carriers thereby affecting the minority carrier diffusion current. An ideal hi-lo junction (n^+/n) ohmic contact reflects minority carriers and in this case, the recombination velocity is zero. In this case, minority carrier injection is inhibited. If the ohmic contact acts as a minority carrier sink, the recombination velocity approaches infinity and in this case, minority carrier injection is promoted.

In this chapter, we investigate the impact of minority carrier injection on the

observed I-V and C-V characteristics of Re/4H-SiC Schottky diodes. Both the I-V and C-V characteristics show deviations from the expected behavior and minority carrier injection offers a good explanation for the observed deviation. In the literature, similar deviations observed on Al/4H-SiC Schottky diodes [105] and Ag/p-Si Schottky diodes [106] and have been analyzed incorrectly using the space charge limited current formulation.

2.2 Experimental procedure

2.2.1 Diode fabrication

The process flow for the fabrication of Schottky diodes is relatively simple and requires few processing steps. Figure 2.1 shows a brief description of the various stages in the Schottky diode fabrication process. The surface of the semiconductor plays a critical role in determining the diode properties; hence, special attention is devoted to surface preparation and cleaning. A degreasing procedure is often employed to clean any organic residue on the surface. A typical degreasing procedure involves a short rinse using acetone, isopropyl alcohol (IPA) and a short de-ionized (DI) water rinse. Occasionally, a short ultrasonic pulse is used to dislodge any particulate contaminants. Contamination from metallic ions can be reduced by using special cleaning recipes such as the Standard Clean 1 (SC1) RCA cleaning procedure [107]. SC1 is widely employed in the CMOS process flow for cleaning Si

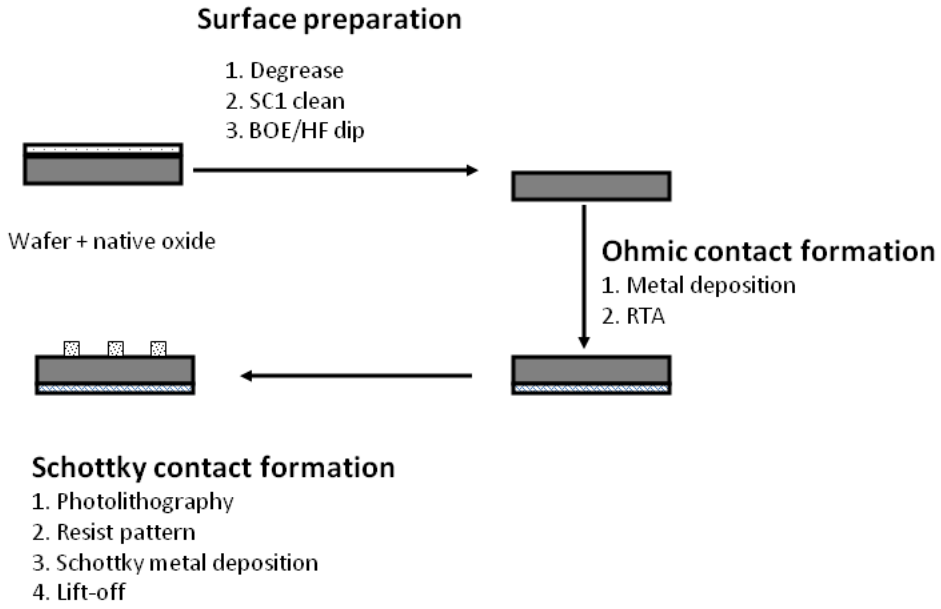

Figure 2.1. Summary of Schottky diode fabrication process flow

wafers [108]. Prior to metal deposition, the wafer is usually subjected to a short HF dip or a buffered oxide etch to remove any native oxide. The presence of native oxide can prevent obtaining a uniform intimate contact between the metal and the semiconductor. The desired metal can, then, be deposited using any of the physical deposition processes such as sputtering, thermal or e-beam evaporation. The ohmic contact is formed first by either blanket deposition of the desired metal stack over a large area followed by a rapid thermal annealing step. In the case of heteroepitaxially grown substrates, such as GaN, the ohmic contact is patterned on the top side of the wafer using photolithography.

Schottky contacts can be either defined using a shadow mask or can be patterned using photolithogrpahy. A shadow mask consists of a thin metal hard mask with holes patterned that define the desired contact area. The shadow mask is jux-

taposed alongside the wafer and constrained together during the Schottky metal deposition process. For contacts at sub-micron dimensions, however, patterning using photolithography is much more suitable. In this process, a photoresist is spun on to the wafer surface followed by a soft bake. The contact pattern is defined using lithography followed by resist development using the appropriate developer. Following lithography, resist development, and metal deposition, metal contacts can be defined using the lift-off process.

In this study, a 5 μm thick n-type 4H-SiC epi layer grown on a 375 μm thick wafer with a resistivity of 30 mΩ–cm was used. The epi-layer doping concentration was 10^{16} cm^{-3}. Following a degreasing rinse, the wafer was subjected to an SC1 clean [107] and a brief HF dip. The back side contact was formed by evaporating nickel followed by a vacuum anneal at 900 ℃. Schottky contacts of Re, Ti and Ti (10%)/W (90 %) were sputter deposited to a thickness of 250 nm to form the Schottky contact (contact area of 10^{-2} cm^2). Electrical characterization of these diodes are detailed in this chapter with a focus on the impact of minority carrier injection on the observed characteristics.

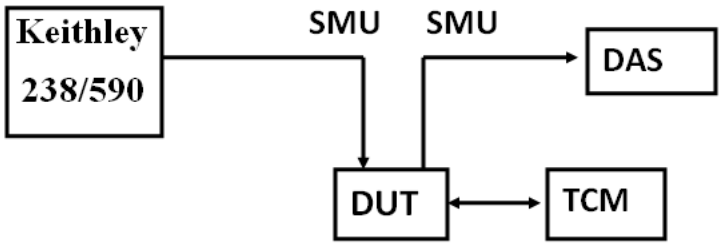

Figure 2.2. Schematic of a general I-V-T/C-V-T measurement

2.3 Electrical characterization

2.3.1 I-V and C-V

Figure 2.2 shows the general schematic of the experimental setup used for electrical characterization of Schottky diodes. For I-V measurements, a source measurement unit (SMU) supplies the appropriate voltage bias conditions to the device-under-test (DUT) through co-axial BNC cables, and the corresponding current is measured using a separate SMU and recorded into a data acquisition system (DAS). Device temperature is typically monitored and controlled using a temperature controller. Capacitance-voltage (CV) measurements are also performed using a similar set-up and instead of a current-voltage source measurement unit, an LCR meter is used. For this study, current-voltage-temperature (I-V-T) characteristics of Re, Ti and Ti/W/4H-SiC were obtained using a Biorad DL8010 system over the temperature range 100–300 K. Capacitance-voltage data were obtained using a KEITHLEY 590 source measurement setup.

2.3.2 Transient measurements

Deep level transient spectroscopy (DLTS) is a very powerful defect characterization tool that allows the determination of sub-surface trap concentration along with capture cross-section and energetic location with respect to the conduction or valence band. The set-up required for DLTS is much more involved than required for a simple C-V measurement. The required components for DLTS and the information flow is shown in Fig. 2.3.

In a typical DLTS measurement, a train of voltage pulses is triggered by the pulse generator and is input into the capacitance meter. The capacitance meter, in turn, applies these train of pulses to the DUT and measures the DUT response. A typical input voltage pulse train and the corresponding DUT capacitance response is shown in Fig. 2.4. The DUT response is fed into the analog-to-digitial (ADC) converter after it is sent through a pre-amplifier. The digitized transient response is stored in the data acquisition system and is analyzed using a fast Fourier transform. This method is known as the Fourier transform deep level transient spectroscopy (FT-DLTS) and is widely used for defect characterization. The theoretical basis for DLTS and the operation principles have been detailed in the literature [109]. A brief description of the method is outlined to facilitate discussion of the results obtained from DLTS studies of Re/4H-SiC Schottky diodes.

The DUT is first cooled to a low temperature ($\sim$ 100 K) and at a fixed temperature, the DUT is held at a constant reverse bias. A voltage pulse is then applied

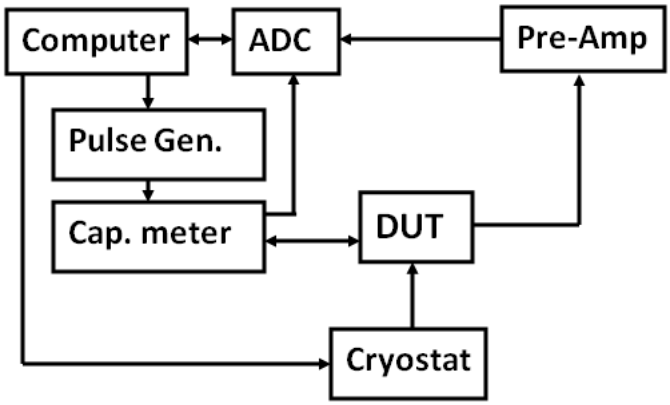

Figure 2.3. Block diagram schematic of a typical DLTS experiment

that pushes the device towards forward bias (depending on the voltage pulse amplitude), and a transient is observed in the depletion region capacitance. Under the application of a voltage pulse, the depletion region capacitance increases due to trapped charge and also smaller depletion region width. The initial peak in the capacitance is proportional to the trap density. The space charge capacitance responds quickly to any change in the applied bias; the trapped charge, however, cannot respond in a similar fashion. Emission of the trapped charge depends on the trap location with respect to the Fermi level and temperature. The time constant for carrier emission from a discrete trap located at E_t below the conduction band is given by

$$\tau^{-1} = \sigma_t \bar{V} N_c \exp\left(-\frac{Ec - E_t}{kT}\right), \tag{2.2}$$

where σ_t is the capture cross-section, $\bar{V}$ is the mean thermal velocity of the carriers, and N_c is the effective density of states in the conduction band. Analysis of

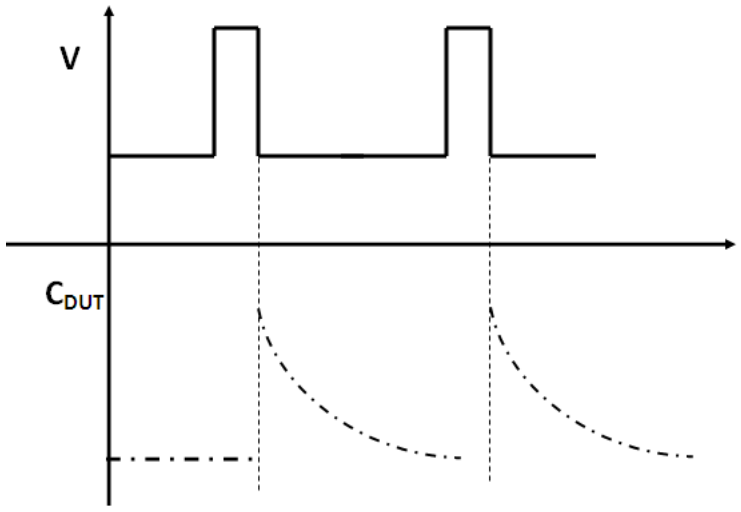

Figure 2.4. Input voltage pulse train and corresponding capacitance transient output from the DUT

the observed capacitance transient can yield the emission time constant, and by gradually changing the DUT temperature, one can obtain the time constant as a function of the device temperature. An Arrhenius plot constructed from the emission time constant and inverse temperature is used to obtain the energetic location of the trap [109]. In the current study, FT-DLTS measurements were performed using the BioRad DL8010 system. The sample was cooled to 100K and was held under a reverse bias of 5 V. A voltage pulse of 3 V amplitude and 1 ms duration was applied and the capacitance transient was measured. The temperature was slowly ramped to the room temperature at a rate of about 1.5 K/s.

2.4 Results and Discussion

Figure 2.5 shows the typical current density-voltage (J-V) characteristics observed for Re/4H-SiC Schottky barrier diodes (SBDs). At lower voltages, a linear region is observed on the semi-log plot indicating that thermionic emission is the dominant conduction mechanism. At these low forward bias values (0.1–0.3 V), the current characteristics can be analyzed using the ideal thermionic emission theory given by

$$J = A^* T^2 \exp(-\beta \Phi_B) \exp\left(\frac{\beta}{\eta} V\right) \{1 - \exp(-\beta V)\}. \tag{2.3}$$

In Equation (2.3), A^* is the Richardson's constant, T is the temperature, and $\beta = q/kT$ is the inverse thermal voltage (k is the Boltzmann's constant and q is the electronic charge). V is the voltage drop across the Schottky diode, which is related to the applied voltage (V_a) by $V = V_a - IR_s$. R_s is the series resistance and I is the total current. Φ_B and η are the conventional Schottky diode parameters (effective Schottky barrier height and ideality factor, respectively).

The linear fit of the semi-log J-V plots (shown in Fig. 2.5) in the low-voltage (0.1–0.3 V for Re and 0.5–0.65 for Ti) region yields contact barrier heights of 0.98 ± 0.01 eV for the Re/4H SiC SBDs and 1.23 ± 0.01 eV for the Ti/4H-SiC SBDs. The diodes also show ideality factor values close to 1 of $\eta = 1.05 \pm 0.03$ for Re/4H-SiC SBDs and $\eta = 1.26 \pm 0.04$ for Ti/4H-SiC SBDs. SiC Schottky

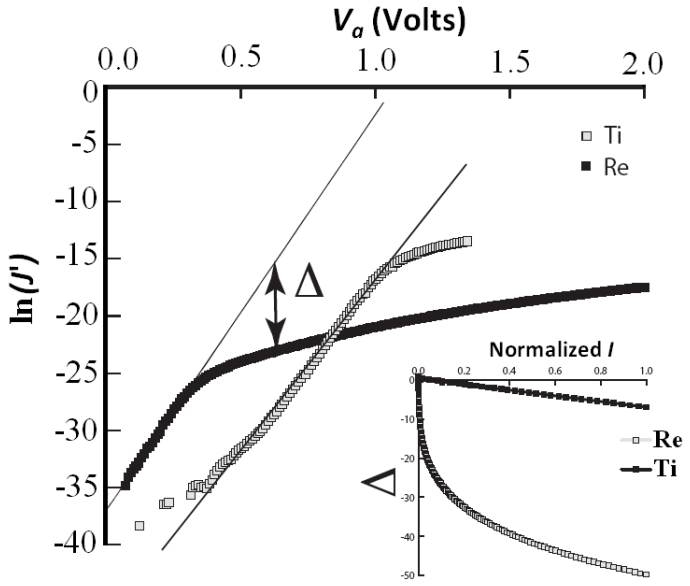

Figure 2.5. Typical J-V characteristics of the Re and Ti/4H-SiC Schottky diodes. The y-axis in this case is $\ln\left(\frac{J}{A^*T^2}\right)$ and is denoted as $\ln(J')$. The inset shows the parameter Δ as a function of normalized current for titanium and rhenium diodes (as described in Section 2.4).

diodes are typically affected by lateral variations in barrier height and often exhibit deviations from the expected thermionic emission theory. However, near unity ideality factors in the Re/4H-SiC Schottky diodes point towards a homogeneous nature of the metal/semiconductor interface. Interestingly, Re is known to form a thermodynamically stable contact with SiC, and the absence of an initially non-uniform reaction may be favorable for achieving a low ideality factor [110].

The I-V relation, in the case of Re/4H-SiC Schottky diodes, is a power law at higher voltages ($V_a > 0.4\ V$) and is indicative of space charge limited current. The power law relation cannot be explained on the basis of an inhomogeneous Schottky barrier model. Space charge limited current [111, 112] is typically observed in low

mobility materials such as organic semiconductors or amorphous semiconductors (such as a-Si) [113, 114]. The presence of carrier trapping centers can cause charge build-up in the system, thereby affecting the I-V characteristics. As mentioned earlier, SCLC has been observed previously in SiC Schottky diodes as well [105].

Extracted barrier height and ideality factors are utilized to extrapolate the ideal J-V characteristics at higher voltages using

$$\ln\left\{\frac{J}{A^*T^2}\right\} = \underbrace{\frac{\beta}{\eta}V_a - \beta\Phi_{\mathrm{B}}}_{J_p} - \beta\frac{IR_s}{\eta}. \tag{2.4}$$

The extrapolated values (J_P) are then used to obtain the series resistance using

$$\ln\left\{\frac{J}{A^*T^2}\right\} - J_p \equiv \Delta = -\beta\frac{IR_s}{\eta}. \tag{2.5}$$

The difference between the actual and extrapolated values, referred to as Δ in Eq. (2.5), is ideally linearly related to the total current and the slope can be used to extract the series resistance. The inset of Fig. 2.5 shows typical Δ vs I plots for the Re/4H-SiC SBDs and similarly prepared Ti/4H-SiC SBDs. For clarity of comparison, the current values have been normalized with respect to the current at $V_a = 1.5\ V$. The Ti/4H-SiC SBDs show a linear behavior, as expected from a diode with a simple series resistance, as predicted by Eq. 2.5. However, Re/4H-SiC SBDs exhibit a significant non-linear Δ versus I relationship indicating deviation from a simple series resistance. This suggests that the conduction mechanism at

higher voltages in Re/4H-SiC SBDs departs very significantly from that in the Ti/4H-SiC SBDs and, hence, from Eq. 2.3. We have recently analyzed in detail the J-V behavior of the type observed in Ti/4H-SiC SBDs [37] and will focus this article on the type of J-V characteristics observed in Re/4H-SiC SBDs.

At higher voltage values, the J-V characteristics can be approximated well by the power law $J - V^m$ with $m \approx 4.5$ at room temperature. This dependence is usually attributed to an exponential distribution of traps and is given by

$$J = q^{1-l}\mu N_c \left(\frac{2l+1}{l+1}\right)^{l+1} \left(\frac{l}{l+1}\frac{\epsilon_s\epsilon_0}{N_t}\right)^{l} \left(\frac{V}{d^2}\right)^{l}\frac{V}{d}, \tag{2.6}$$

where

$$l = \frac{T_t}{T}. \tag{2.7}$$

In Eq. (2.6), N_t is the total density of traps, T_t is often called the characteristic temperature and d is the sample thickness.

Experimental data on Al/4H n-SiC SBDs taken from ref. [105] also shows a similar power law dependence of current on voltage. In ref. [105], the authors simply plug the value of μ obtained from the literature to fit the data using Eq. 2.6. However, from the available data, one could easily extract the expected mobility values under the exponential trap distribution assumption. We have analyzed I-V-T data on the Re/4H-SiC diodes, as well as data reported in ref. [105], under the

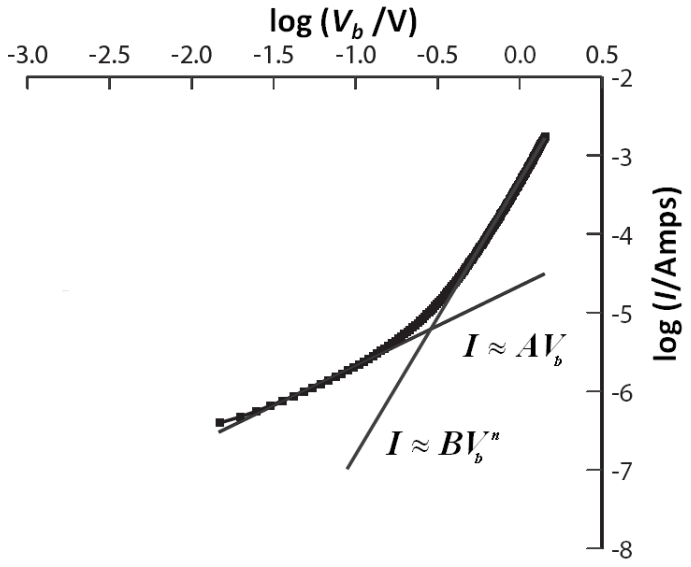

Figure 2.6. Current as a function of potential drop across SiC bulk showing typical space charge limited current behavior.

exponential trap distribution assumption. This analysis yields very low mobility values (10^{-4} cm^{2}V/s), which do not correlate well with the commonly expected value of mobility in SiC [115]. Also, an exponential trap distribution in 4H-SiC seems very unlikely due to the ordered nature of the material. Based on the arguments presented in this section, we abandon the assumption that the power law is due to an exponential distribution of traps and look for an alternative explanation.

Alternatively, the potential drop across the semiconductor bulk can be approximated using

$$V_b = V_a - \frac{\eta}{\beta} \ln\left(1 + \frac{I}{I_{sat}}\right), \tag{2.8}$$

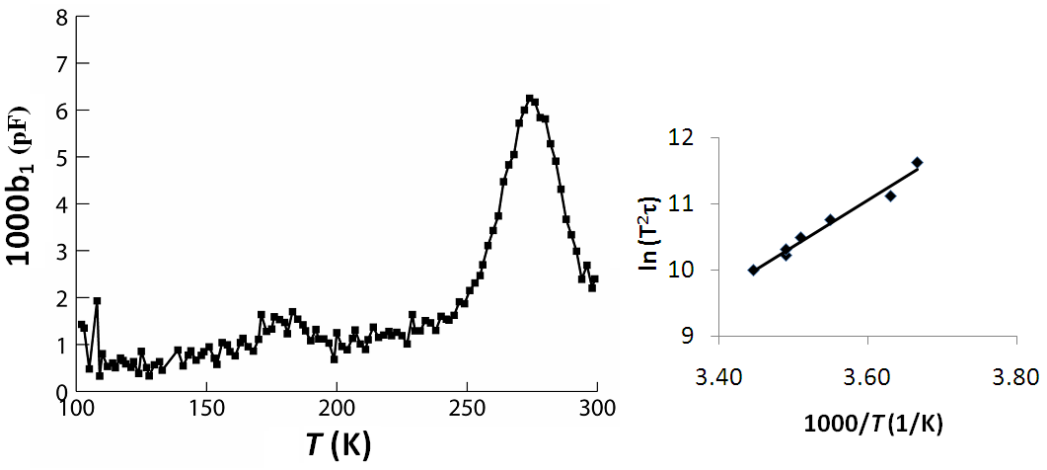

Figure 2.7. DLTS signal from the Re/4H-SiC Schottky diode. Inset shows the Arrhenius plot for the Z_1 trap.

where

$$I_{sat} = AA^*T^2 \exp\left(-\beta\Phi_B\right). \tag{2.9}$$

In an ideal diode, the bulk potential drop (V_b) should be linearly related to the current flowing through the diode. Figure 2.6 shows the observed relationship between current and V_b in Re/4H-SiC Schottky diodes. The observed relationship is also strongly indicative of space charge limited current. In the lower voltage regime, the relationship between I and V_b is linear, indicating ohmic behavior, followed by a SCLC behavior at higher voltages. In the higher voltage regime, the current varies with V_b as $I = BV_b^n$, where B is a proportionality constant ($n \geq 2$).

Figure 2.7 shows the FT-DLTS spectrum observed for a Re/4H-SiC diode. In Fig. 2.7, b_1 is the first sine coefficient in the Fourier transform of the capacitance

transient. The inset shows the Arrhenius plot for a trap located at an energy depth of $E_t = 0.6$ eV below the conduction band edge. The trap concentration is determined from the signal intensity and is estimated to be 10^{12} cm^{-3}. The electron trap has a capture cross-section of $\sigma = 3.8 \times 10^{-13}$ cm^2 and is extracted from the intercept of the Arrhenius plot (shown in Fig. 2.7). These values are very close to those reported for an intrinsic defect in SiC known as the Z_1 defect center [116].

The trap density obtained by the DLTS measurements is orders of magnitude smaller than the carrier density (10^{16} cm^{-3}). Also, excess injected charge of a magnitude comparable to the equilibrium free carrier density cannot be achieved at such voltage levels. In organic semiconductors and insulators, either or both of the above conditions are met and one can observe trap-limited I-V characteristics. In 4H-SiC, neither of these conditions are satisfied, and hence it is unlikely that SCLC behavior is due to majority carrier traps. Double carrier injection in solids can also give rise to SCLC-like behavior. The preceding analysis points to the conclusion that space charge limited current due to minority carrier injection is the most likely cause for the observed I-V characteristics.

Forward bias C-V measurements have been used to further assess the role of minority carrier injection in the conduction properties of Re/4H-SiC SBDs. Figure 2.8 shows the observed C-V characteristics of Re/4H-SiC and Ti/4H-SiC SBDs in forward bias. The reverse bias characteristics are typically used to obtain

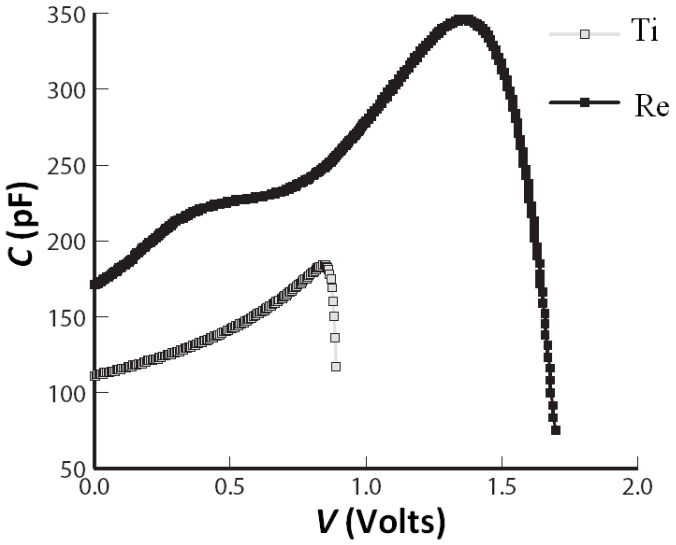

Figure 2.8. Forward bias capacitance-voltage curve of Re and Ti/4H-SiC Schottky diodes.

the doping profile of the underlying substrate. The peak in the forward bias region of the C-V characteristics is due to interface traps and series resistance as analyzed in ref. [117]. Ti/4H-SiC SBDs follow the expected C-V characteristics; however, Re/4H-SiC SBDs show excess capacitance in forward bias. Werner et al. have shown, in the case of Si Schottky diodes, that such excess capacitance signature can be attributed to minority carrier injection, and the excess capacitance is not related to interface traps [118].

Minority carrier injection under forward bias conditions would occur from the Schottky metal into the substrate. At low forward bias voltage values, the current is primarily limited by thermionic emission, and most of the applied voltage drops across the depletion region. In this case, there is negligible electron and hole Fermi-level splitting. With increasing forward bias, the Fermi-level splitting increases

and results in higher minority carrier injection. Eventually, most of the voltage drop is seen as the difference between the electron and hole quasi Fermi-levels and corresponds to the bulk voltage drop. Since the majority carrier current is primarily governed by the drop across the diode (V), and with increasing minority carrier injection there is very little variation in V, the majority carrier current contribution does not increase with increasing forward bias. As excess minority carriers are injected, the current is limited mainly by the injection and transport of holes across the semiconductor bulk.

Werner et al. have suggested that under ideal conditions, an ohmic contact to a hi-lo junction acts as a good reflecting boundary for minority carriers and inhibits minority carrier injection at the Schottky contact [118]. In the case of a poor ohmic contact, the injected minority carriers are not reflected effectively at the hi-lo junction and can recombine at the ohmic contact. Although Re forms a good homogeneous contact, an imperfect ohmic contact in our Schottky diodes may have made possible the minority carrier injection at the Schottky contact. Minority carrier injection would be detrimental to device operation, not only in terms of the limitation due to space charge, but also because of minority carrier storage and slower reverse recovery.

However, I-V characteristics show other deviations such as $n > 1$, high reverse leakage current and double diode behavior. These deviations are commonly observed in Schottky diodes and have been explained well by the inhomogeneous

Schottky barrier model. The effects of BHI on the I-V characteristics on the extracted Schottky diode parameters are examined in the next chapter. Starting with a survey of the current approaches to account for effects of BHI on the extracted conventional Schottky diode parameters, a new method that extends the applicability of existing methods is proposed.

Chapter 3

Effects of barrier height inhomogeneities on Richardson constant determination

3.1 Introduction

In order to use the current-voltage (I-V) response to accurately obtain the Schottky barrier height of a metal/semiconductor (MS) junction, it is necessary to know the Richardson constant (A^*), and this is one of the most compelling reasons for an accurate determination of the Richardson constant [119]. The Richardson constant is extracted from the so-called Richardson plot using measured I-V-T data. In practice, the extracted Richardson constant may be far from the theoretically expected value, and in many cases, by orders of magnitude. Several researchers

have investigated the cause for the discrepancy and proposed different explanations [119, 16, 120, 121, 122]. Earlier approaches (circa mid 80's and early 90's) focused on the temperature and interface electric field dependence of the barrier height (as proposed by Wagner [123]). Recent approaches focus on incorporating the effects of barrier height inhomogeneities (BHI) on the measured I-V-T curves, and a modified version of the Richardson plot is often used (for example, [121, 124, 35, 125, 126, 127]).

Effects of BHI on the extracted barrier height are widely recognized. Analytical approximations that capture these effects are available to interpret experimental I-V-T data. No such provision exists for the extracted A^* until this study. To begin with, we demonstrate the limitations of previous approaches in greater detail and also provide further experimental support for our proposed approach.

First, we review previous methods that are typically used to account for the deviations of the Richardson plot from the ideal case. We specifically focus on the methods that address barrier height inhomogeneities. Next, we apply these methods to a simulated dataset in order to gain insights into the applicability and limitations of these widely-used approaches. Based on the BHI framework provided by Tung, we explicitly derive the dependence of the Richardson constant on the BHI parameters. The new approach filters the effects of BHI on the extracted Richardson constant without the need for parameterized fitting or modifying the original Richardson plot. The proposed approach is applied to determine the

Richardson constant of n-type ZnO and GaN.

3.2 Review of existing methods

In the ideal Schottky diode case, under forward bias, the carrier conduction process is limited by emission of carriers from the semiconductor over a spatially homogeneous barrier at the MS interface into the metal. In this case, the carrier conduction and hence, the current is given by

$$I = I_{\text{sat}} \exp\left(\frac{\beta}{n}(V_a - IR_s)\right)\left[1 - \exp\left(-\beta V_a\right)\right], \tag{3.1}$$

where

$$I_{\text{sat}} = AA^*T^2 \exp\left(-\beta\Phi_{\text{Beff}}\right). \tag{3.2}$$

In Eq. 3.1 and 3.2, I is the total current, A^* is the Richardson constant, A is the the diode area, β is the inverse thermal voltage (q/kT), V_a is the applied voltage, R_s is the series resistance, T is the absolute temperature, n is the ideality factor and Φ_{Beff} is the apparent or effective Schottky barrier height.

The Richardson constant is extracted from the current-voltage-temperature (I-V-T) characteristics using the Richardson plot. The saturation current, I_{sat}, is

obtained from the I-V data at different temperatures using

$$\ln\left(\frac{I}{1-\exp\left(-\beta V_a\right)}\right) = \frac{\beta}{n}V_a + \ln\left(I_{\text{sat}}\right). \tag{3.3}$$

This equation is applicable at low currents under forward bias, where the effects of series resistance can be neglected. From the obtained I_{sat} values, the Richardson plot is constructed by plotting $\ln\left(I_{\text{sat}}/AT^2\right)$ vs. $1/T$. The slope and intercept of the Richardson plot yield the effective barrier height and Richardson constant respectively, as indicated by

$$\ln\left(\frac{I_{\text{sat}}}{AT^2}\right) = -\frac{q\Phi_{\text{Beff}}}{k}\frac{1}{T} + \ln(A^*). \tag{3.4}$$

The bias and temperature dependence of the Schottky diode parameters (n and Φ_{Beff}) give rise to a slight curvature in the $\ln(I) - V$ plot. As a result of the curvature, the saturation current (I_{sat}) values used in the Richardson plot are heavily influenced by the bias range selected for curve-fitting. Numerous deviations from the ideal thermionic emission theory have been proposed and examined in real Schottky diodes. Some of the key effects that significantly affect the measured Richardson constant are outlined next.

3.2.1 Temperature dependence of Φ_B

In one of the earliest treatments of non-ideality in the extraction of A^*, the discrepancy between the measured and theoretical A^* values was explained using a linear temperature dependence of the homogeneous barrier height (Φ_{B0}). The temperature dependence of the homogeneous barrier height is given by

$$\Phi_{B0}(T) = \Phi_{B0}(0) + \alpha T. \tag{3.5}$$

In equation 3.5, α is the temperature coefficient of the barrier height. Using this method, the corrected Richardson constant value A_c^* is related to the uncorrected value (A_{uc}^*) [119, 128] by

$$A_c^* = A_{uc}^* \exp\left(q\alpha/k\right). \tag{3.6}$$

The temperature coefficient is obtained from capacitance-voltage-temperature (C-V-T) measurements. For silicon, the temperature coefficient of the barrier height has been correlated with the temperature coefficient of the bandgap, and it has been suggested that the temperature dependence is associated with the Fermi-level pinning position [122, 125, 129]. The Richardson constant is expected to be independent of the barrier metal and is a property of the semiconductor alone [119]. However, even the corrected Richardson constant values have been found to depend on the choice of metal [128]. The temperature dependence of the barrier

height would be less significant for systems exhibiting weak Fermi-level pinning, since in this case the temperature coefficient of Φ_{B} would be much smaller. Also, for diodes exhibiting ideality factors far greater than 1, other dominant factors can distort the Richardson plot.

3.2.2 Flat band barrier height analysis

Wagner et al. observed a linear correlation between the ideality factor and barrier height and attributed this dependence to interface electric field dependence of the effective barrier height [123]. A flat band barrier height (Φ_{B}^{f}) concept is introduced and is considered a real MS interfacial property since it is measured at zero electric field. The flat band barrier height can be expressed in terms of the ideality factor and apparent barrier height as given by

$$\Phi_{\mathrm{B}}^{f} = n\Phi_{\mathrm{Beff}} - (n-1)V_n. \tag{3.7}$$

In Eq. 3.7, V_n is the bulk potential and equals $(1/\beta)\ln(N_c/N_d)$, where N_c is the effective density of states in the conduction band and N_d is the doping density. In the case of non-ideal Schottky diodes, a curvature is usually observed in the original Richardson plot. Unewisse et al. suggested a modified version of the Richardson

plot using a flat band saturation current [120], as defined by

$$I_{\rm sat}^{f} = AA^{*}T^{2} \exp\left(-\frac{q\Phi_{\rm B}^{f}}{nkT}\right). \tag{3.8}$$

In this case, the abscissa of the Richardson plot is modified to $1/nT$ instead of $1/T$ according to

$$\ln\left(\frac{I_{\rm sat}^{f}}{AT^{2}}\right) = -\left(\frac{q\Phi_{\rm B}^{f}}{k}\right)\frac{1}{nT} + \ln(A^{*}). \tag{3.9}$$

Apart from the linear correlation between n and $\Phi_{\rm B}$, an anomalous increase in ideality factor with decreasing temperature was observed by Padovani and Sumner [11]. This behavior is commonly known as the T_0 anomaly, and the interface electric field model does not offer an explanation for the T_0 anomaly. The inhomogeneous Schottky barrier models, as explored by several authors in late 1980's and early 1990's, was able to account for many of the observed anomalies and deviations.

In recent years, the inhomogeneous Schottky barrier concept has been applied to explain a wide range of observed I-V characteristics. A brief overview of the inhomogeneous Schottky barrier models is presented next, in the context of their application towards modifying the Richardson plot. For the case of barrier inhomogeneities that vary on the length scale of the depletion region width, two theories are widely employed. Werner and Güttler propose an interacting Gaussian distribution of barrier heights to account for the presence of spatial inhomogeneities

[16]. The second model proposed by Tung relies on a patchwork of low barrier regions embedded within a homogeneous high barrier region [17].

3.2.3 Werner and Güttler's model

Using a Gaussian distribution of barrier heights characterized by a voltage and temperature dependent spread parameter (σ_Φ), the inhomogeneous barrier model is able to account for a variety of observed deviations. The model is able to address the problem of T_0 anomaly observed in several MS systems. Also, the model is able to account for deviations observed in extracted ideality factors and effective barrier heights. A central feature of the model is the emergence of the ideality factor as a result of the voltage deformation of the potential profile fluctuation, or in other words, the voltage dependence of the barrier distribution parameter, σ_Φ. Using the Gaussian distribution of barrier heights, the model is able to account for the curvature in the Richardson plot. A modified Richardson plot has been suggested based on Werner and Güttler's model and is given by

$$\ln\left(\frac{I_{\text{sat}}}{T^2}\right) - \left(\frac{q^2\sigma_\Phi^2}{2k^2T^2}\right) = \ln(AA^*) - \frac{q\Phi_{\text{B0}}}{kT}. \tag{3.10}$$

A key feature of Werner and Güttler's model is the *bias independence of the ideality factor*. Hence, the model applicability is limited to experimental data that conforms to this principle, although experimental data in the literature are regularly fitted with the Gaussian distribution model without this constraint met.

Tung's model, on the other hand, accounts for barrier inhomogeneities in a slightly different way. Tung's model accounts for bias and temperature dependence of the Schottky diode parameters using bias and temperature independent patch parameters and is discussed next.

3.2.4 Tung's model

As stated earlier, the I-V characteristics of a real MS interface often deviate from the ideal case. The observed non-ideal behavior can be broadly categorized into double diode behavior and a slight curvature in the semi-log I-V plot. Diodes exhibiting double diode behavior are characterized by anomalous high current at low forward bias values and are modeled as low barrier patches mixed within a uniform high barrier region (Φ_{BH}). The low barrier regions are characterized by the local barrier height (Φ_{BL}) and the size of the patch (R_0). Depending on the interfacial barrier height difference between low and high barrier regions ($\Delta = \Phi_{BH} - \Phi_{BL}$) and the patch size, the high barrier region can affect the potential within the low barrier region. Under such conditions, the low barrier region is said to be "pinched off" by the high barrier region. The pinch-off phenomenon gives rise to a saddle point potential within the low barrier region, and the saddle point potential governs the carrier transport across the low barrier region. The saddle point potential is both bias and temperature dependent and can account for the observed voltage dependent Schottky diode parameters for the low barrier region.

Tung proposed a reduced patch parameter, γ, to couple the effect of Δ and R_0 (as defined by Eq. 3.11) [17]. According to Tung, the double diode behavior can be modeled using a dilute density (C_1) of patches characterized by very similar γ values, where

$$\gamma = 3\left(\frac{\Delta R_0^2}{4}\right)^{\frac{1}{3}}. \tag{3.11}$$

Many Schottky diodes do not exhibit double diode behavior, but they do still show a slight curvature in the semi-log I-V plot. Tung suggests a semi-Gaussian distribution of the reduced patch parameter (γ) to account for the slight curvature in the semi-log I-V plot. The distribution is characterized by a mean value, $\gamma_0 = 0$, spread σ, and total density of patches C_1.

It is well established that the curved nature of the Richardson plot can be a result of BHI. The effects of BHI on Richardson constant determination using Werner's model [16, 130, 131] and Tung's model [35, 22] have been attempted in the literature.

Based on Tung's model, some authors have attempted to account for the effects of BHI by using an effective area rather than the overall contact area [124]. In an inhomogeneous Schottky diode, at low temperatures, the current preferentially flows through the low barrier regions. In this regime, the total area contributing to the current conduction is a small fraction of the geometric area of the Schottky contact. I-V-T data are fitted using the analytic expressions provided by Tung

to obtain the low barrier patch density and σ parameters. At a given bias and temperature, the effective area of the low barrier patches can be estimated using

$$f = \frac{8C_1\pi\sigma^2}{9\beta_1}, \tag{3.12}$$

where

$$\beta_1 = \left(\frac{V_{bb}}{\eta}\right)^{1/3}. \tag{3.13}$$

In Eq. (3.13), V_{bb} is the band bending at the measured bias, and η is the doping density dependent parameter and equals ϵ_s/qN_d. ϵ_s is the dielectric constant of the semiconductor. The Richardson plot is then modified, using this effective area term, to

$$\ln\left(\frac{I_{\text{sat}}}{fT^2}\right) = \ln(AA^*) - \frac{q\Phi_{\text{B0}}}{kT}. \tag{3.14}$$

However, it should be noted that the effective area of the low barrier patches is both bias and temperature dependent.

A key aspect of these analytical approaches is the hypothesis that the current contribution mainly comes from the low barrier regions. This assumption need not hold true across the measurement temperature range and particularly at higher temperatures. The effective area contribution is estimated using the patch spread

parameter (σ) and the patch density (C_1) obtained through the I-V-T fitting exercise. However, the BHI parameters (C_1 and σ) cannot be uniquely determined from the I-V-T characteristics since multiple sets of BHI parameter values can fit the I-V-T data. Hence, a consistent method for calculating the effective area is not possible and is riddled with a great degree of uncertainty.

Another approach that tries to incorporate BHI effects on Richardson constant relies on invoking the T_0 approximation [125, 130, 35] originally proposed by Padovani and Sumner [11]. Experimental data on several Schottky diode systems exhibit the T_0 anomaly over a limited temperature range, and in this range the ideality factor can be expressed as

$$n = 1 + \frac{T_0}{T}. \tag{3.15}$$

The T_0 parameter has been attributed to presence of BHI and within the BHI framework provided by Tung, T_0 can be written as

$$T_0 = \left(\frac{\sigma^2}{3\eta\beta_1}\right)\frac{q}{k}. \tag{3.16}$$

The modified Richardson plot is constructed by plotting $\ln\left(\frac{I_{\text{sat}}}{AT^2}\right)$ vs. $1/nT$ as suggested by

$$\ln\left(\frac{I_{\text{sat}}}{AT^2}\right) = -\frac{q\Phi'_{\text{Beff}}}{nkT} + \ln(fA^*). \tag{3.17}$$

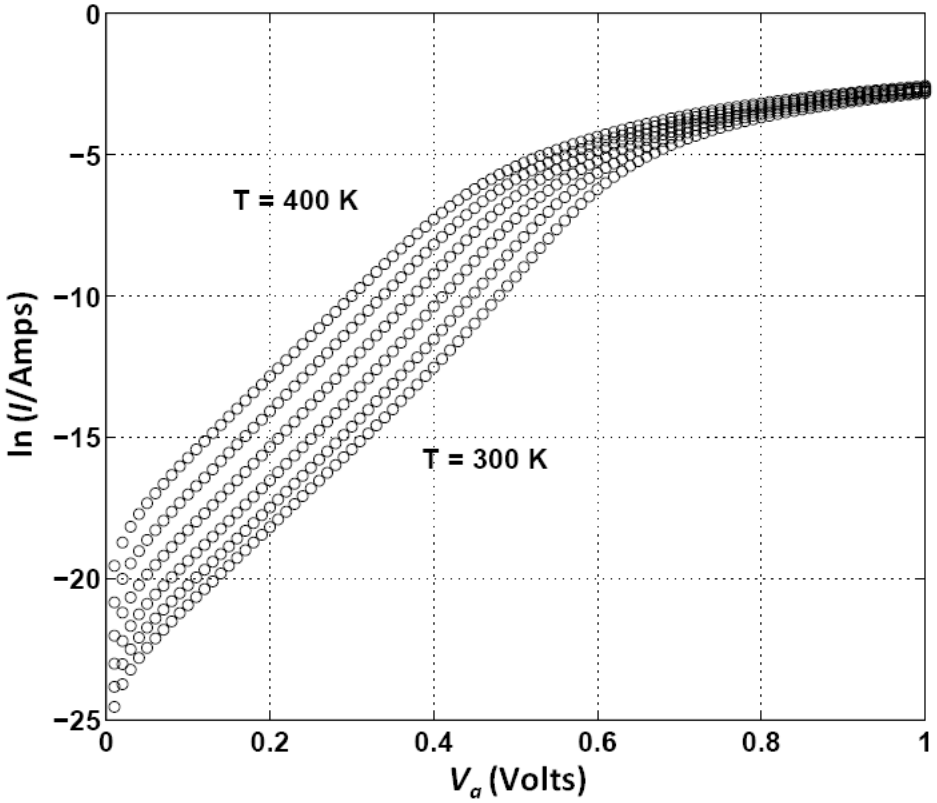

Figure 3.1. *I-V-T* characteristics simulated using Tung's equations. A homogeneous barrier height of 1.2 eV, C_1 of 10^7 cm^{-2} and σ of 10^{-4} cm$^{2/3}$ eV$^{1/3}$ have been used in this case.

However, the obtained Richardson constant is still an effective value that is scaled by the fractional area covered by the low barrier regions (f). The effective barrier height obtained from the BHI modified Richardson plot is given by

$$\Phi_{\mathrm{B}}^{'} = \Phi_{\mathrm{B0}} - \frac{n-1}{\beta} \ln\left(\frac{N_c}{N_d}\right). \tag{3.18}$$

3.3 Extended inhomogeneity analysis

From the above discussion, it is evident that there are quite a few methods that attempt to account for the deviation of the extracted Richardson constant from the expected value. In this section, we investigate the applicability and limitations of previous methods using a controlled I-V-T dataset obtained from analytical expressions by Tung for the case of a semi-Gaussian distribution of the patch parameter γ. A wide range of device characteristics can be simulated by varying the homogeneous barrier height (Φ_{B0}) and BHI parameters (C_1 and σ). Forward bias I-V characteristics are obtained across a wide range of temperature values, and the simulated data are treated in a similar fashion as one would treat experimental I-V-T data. Figure 3.1 shows the typical simulated I-V-T characteristics obtained using analytical expressions provided by Tung. A patch density C_1 of 10^7 cm^{-2}, σ of 10^{-4} cm$^{2/3}$ eV$^{1/3}$, and a Φ_{B0} of 1.2 eV have been used in this case.

3.3.1 n-Φ_B and T_0 analysis

Schmitsdorf et al. showed that the observed linear correlation between n and Φ_B could be explained in terms of Tung's BHI model [132]. The linear correlation between n and Φ_B is reported in several MS systems and provides a simple way to account for the effects of BHI on the extracted Schottky barrier height without the need for complicated parameterized fitting of the I-V-T characteristics.

However, the linear correlation observed between n and Φ_B is valid only for a

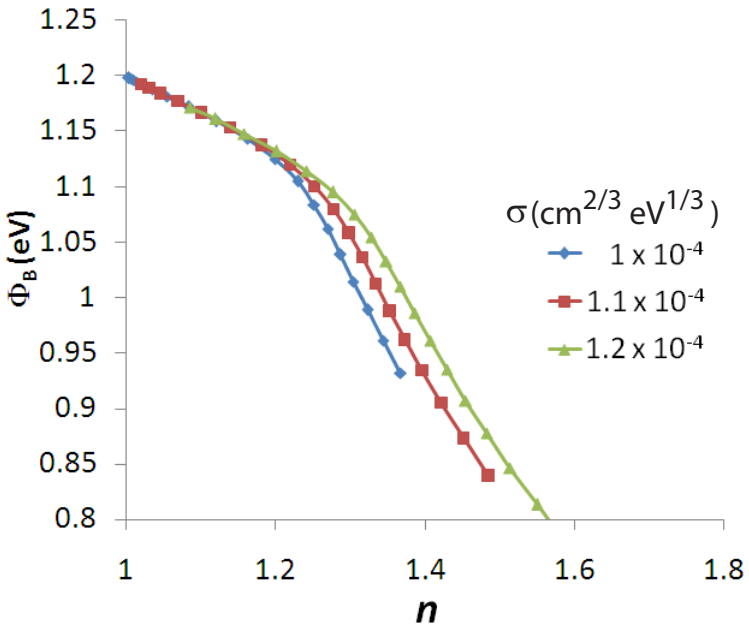

Figure 3.2. n-Φ_{Beff} plot for devices simulated with different σ values and a patch density of $C_1 = 10^7 \mathrm{cm}^{-2}$. A homogeneous barrier height of 1.2 eV was used in the simulation.

narrow range of ideality factors as pointed out by Schmitsdorf et al. [132]. Figure 3.2 shows an n-Φ_{B} relation for a family of simulated devices, and each device is characterized by a different σ value. For low ideality factors ($n < 1.2$), the ideality factor and effective barrier height are linearly correlated. The linear correlation can be extrapolated to $n = n_{\mathrm{if}}$, where n_{if} is the image force controlled ideality factor, yielding the zero-bias barrier height Φ_{B0}. Adding the zero-bias barrier height and the barrier height lowering due to the image force ($\Delta\Phi_{\mathrm{B}}$), one can obtain the homogeneous barrier height.

The image force controlled ideality factor can be estimated using

$$n_{\mathrm{if}} \approx 1 + \frac{1}{4}\left[\frac{q^3 N_d}{8\pi^2 \epsilon_s^3 V_{bb}^3}\right]^{\frac{1}{4}}, \tag{3.19}$$

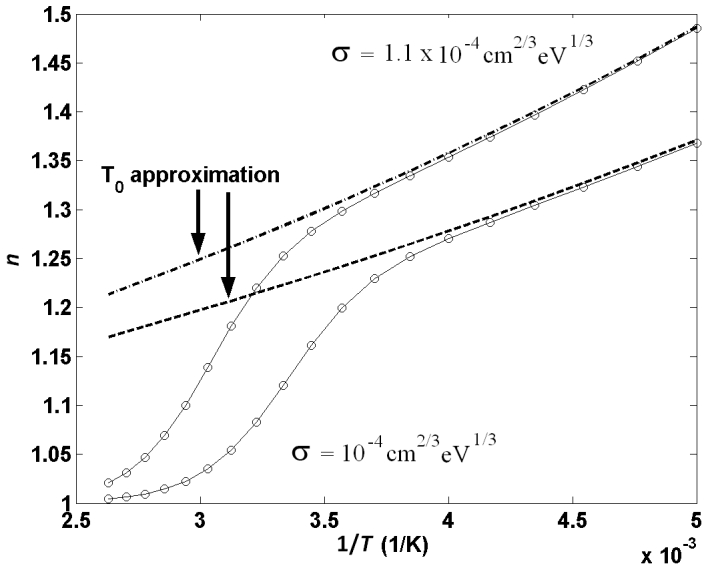

Figure 3.3. Temperature dependence of the extracted ideality factor for two different σ values. A patch density of $1 \times 10^7 \mathrm{cm}^{-2}$ and a homogeneous barrier height of 1.2 eV is assumed.

and the barrier lowering due to image force is given by

$$\Delta\Phi_{\mathrm{B}} \approx \left(\frac{q^3 N_d V_{bb}}{8\pi^2 \epsilon_s^3} \right)^{\frac{1}{4}}. \tag{3.20}$$

For moderately doped semiconductors, extrapolating to $n = 1$ yields a close estimate of the homogeneous barrier height, since in this case, n_{if} is very close to 1. It should be noted that a linear correlation is observed at high ideality factor values as well, but the straight line in this region does not extrapolate to the input barrier height and can give erroneous extrapolated barrier height values.

Figure 3.3 shows the ideality factor as a function of the inverse temperature for two different values of σ. At lower temperatures (high n), the temperature dependence of n can be approximated using the T_0 approximation (as given by

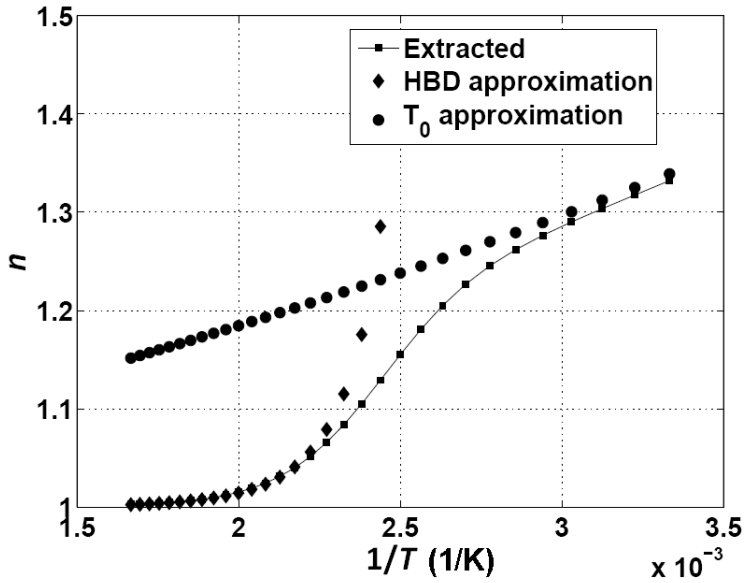

Figure 3.4. Extracted ideality factor, T_0 approximation and HBD approximation for a simulated device

Eq. 3.15), and in this regime, the total current is dominated by the contribution from low barrier (LB) regions. At higher temperatures (low n), the temperature dependence of the ideality factor deviates significantly from the T_0 approximation. Although BHI has been suggested as the source for the T_0 parameter by both Tung [17] and Werner et al. [16], the abrupt change of slope in the n vs. $1/T$ curve has not been investigated yet. At lower ideality factor values, the current-voltage characteristics have been found to be dominated by the homogeneous high barrier region. This regime is defined as the high barrier (HB) dominated regime. Experimental data on several Schottky diode systems exhibit the T_0 anomaly; however, an important point to be noted is that the T_0 anomaly effect is observed over a limited temperature range [16, 11].

Starting from the analytic expressions for I-V-T characteristics for an inhomo-

geneous diode, one can show that the voltage and temperature dependence of the ideality factor in the HB dominated (HBD) regime is given by

$$n = 1 + \left(\frac{8\pi C_1 \sigma^4}{27\beta_1^2 \eta} \exp\left(\frac{\beta^2 \beta_1^2 \sigma^2}{2} \right) \right) \beta. \tag{3.21}$$

The barrier height in terms of ideality factor is given by

$$\Phi_{\text{Beff}} = \Phi_{\text{B0}} - 3(n-1)V_{bb}. \tag{3.22}$$

A clear linear relation between n and Φ_{Beff} is observed, and for $n = 1$, Φ_{Beff} becomes equal to Φ_{B0}. The relevant derivations of these expressions are provided in the Appendix.

Figure 3.4 shows the extracted ideality factor as a function of the inverse temperature ($1/T$). At lower temperatures (higher ideality factor), the T_0 equation gives a good fit to the ideality factor curve. The T_0 regime is the LB dominated regime. At higher temperatures, the ideality factor values deviate significantly from the T_0 line, and the HBD approximation (equation 3.21) yields a much better fit. In the HB dominated regime, Eq. 3.21 captures the bias and temperature dependence of n, and analytical approaches that invoke the T_0 approximation in this regime would yield erroneous results.

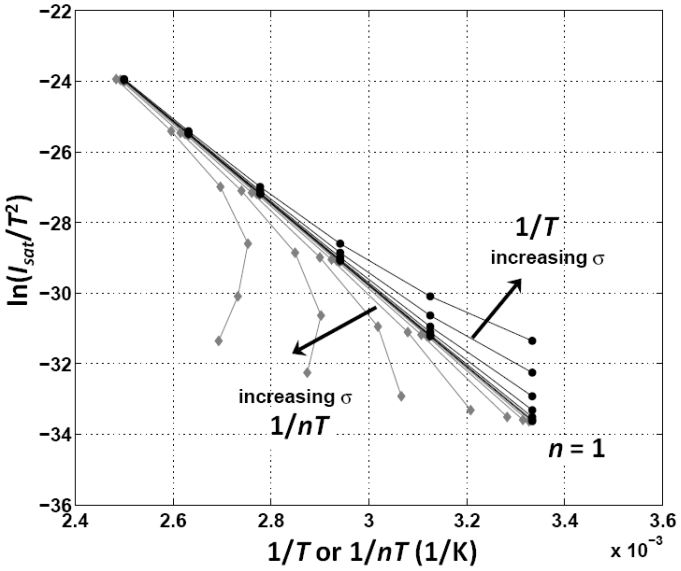

Figure 3.5. Effect of σ on the Richardson and modified Richardson plot. Larger σ values correspond to greater deviation from ideality and therefore larger ideality factor values.

3.3.2 Richardson plot

The effect of increasing departure from ideality ($n = 1$) on the Richardson plot is shown in Figure 3.5. For the case of $n = 1$ or low σ values, the $1/T$ and $1/nT$ plots coincide, and the obtained values of A^* and Φ_B values correlate well with the input values. For moderate high ideality factor values, the extracted A^* and Φ_B values from the original or modified Richardson plot can be quite different from the input or actual values. With increasing BHI parameter values (C_1 and σ), n tends to increase, resulting in a curvature or distortion of the Richardson plot. Curvature of the original Richardson plot has been reported widely and, in this case, the modified version of the Richardson plot is often employed [121, 125, 126, 127]. However, as suggested by Fig. 3.5, the modified Richardson plot is not always

successful in rectifying the curvature observed in the original Richardson plot.

3.3.3 Application of existing methods

From the preceding discussion, it is evident that the presence of BHI affects the Richardson plot, and therefore, the extracted Richardson constant. A systematic investigation of the effect of BHI parameter values (C_1 and σ) on the extracted Richardson constant is, however, still missing. In order to understand the applicability of the conventionally reported methods, we apply previous methods for analyzing I-V-T characteristics to a set of simulated devices obtained by varying the BHI parameters (C_1 and σ). Several methods have been proposed in the literature, but we have chosen to focus on three approaches: the original plot (M_1), modified plot (M_2) [120] and effective area method (M_3) [124]. The original plot method is the simple original Richardson plot that does not account for any of the deviations, whereas in the modified version of the Richardson plot, the abscissa and ordinate are changed to $1/nT$ and $\ln\left(\frac{I^f_{\text{sat}}}{AT^2}\right)$ respectively (according to Eq. 3.9). The effective area method is a more recent approach (proposed by Roccaforte et al. [124]) that attempts to account for the effects of BHI on the Richardson plot by calculating the effective area for conduction using Eq. 3.12. In this case, the total current is assumed to be dominated entirely by the low barrier patches and the geometric area term (A) is scaled by an effective area term (f).

Figure 3.6 shows the extracted Richardson constant as compared to the input

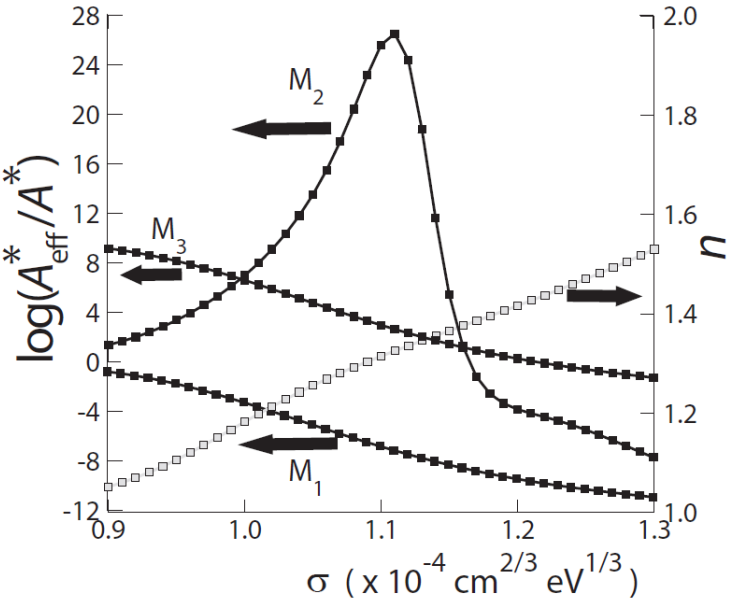

Figure 3.6. Effect of σ on the extracted Richardson constant using the original Richardson plot (M_1), modified Richardson plot (M_2) and effective area method (M_3). A Richardson constant of 26 A cm^{-2} K^{-2}, homogeneous barrier height of 1.2 eV and a patch density of 1×10^7 cm^{-2} were used in the simulations. In the case of extraordinarily high Richardson constant values, it has been found that the Richardson plot is longer linear and the method applicability is, therefore, questionable.

Richardson constant value as a function of σ using the three different approaches. A patch density of 1×10^7 cm^{-2}, homogeneous barrier height of 1.2 eV, and donor density of 10^{16} cm^{-3} was used in this case. Forward bias I-V curves in the temperature range of 300–400 K were used to obtain the original and modified Richardson plots. Fig. 3.6 also shows the extracted ideality factor at room temperature. At low σ values (corresponding to low n), the original Richardson plot yields Richardson constant values close to the input Richardson constant. However, with increasing ideality factor values (larger n), the Richardson constant extracted using the original Richardson plot can quickly deviate from the true value. In other words, the

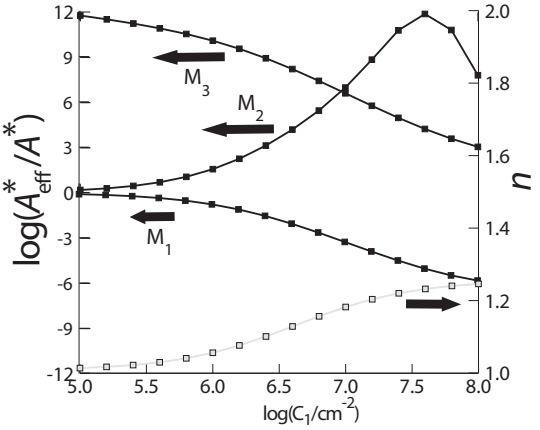

Figure 3.7. Effect of C_1 on the Richardson constant extracted Richardson constant using the original Richardson plot (M_1), modified Richardson plot (M_2) and effective area method (M_3). A Richardson constant of 26 A cm^{-2} K^{-2}, homogeneous barrier height of 1.2 eV and $\sigma = 1 \times 10^{-4}$ cm$^{2/3}$ eV$^{-1/3}$ were used in the simulations. In the case of extraordinarily high Richardson constant values, it has been found that the Richardson plot is longer linear and the method applicability is, therefore, questionable.

extracted Richardson constant value is an effective value that depends on the extent of deviation the MS interface exhibits from ideality. The modified Richardson plot (M_2) also suffers from similar discrepancies and can yield reasonable Richardson constant values for low n, but with increasing n, the extracted Richardson constant can deviate significantly from the input value. The Richardson constant extracted using the effective area method can vary over orders of magnitude from the input Richardson constant value. The effective area method can yield a Richardson constant value close to the input value for large ideality factor values since the method is applicable when the contribution from low barrier regions dominates the total current. However, as shown in Fig. 3.6, even an accurate knowledge of C_1 and σ does not ensure an accurate determination of the actual Richardson constant since the effective area is both bias and temperature dependent. Figure 3.7 shows the

effect of patch density (C_1) on the Richardson constant extracted using the three different approaches (original, modified and effective area methods). The effect of varying C_1 is similar to the effect of varying σ, and with increasing C_1 values the ideality factor increases and results in a larger departure of the extracted A^* value from the actual value. The preceding analysis shows that these earlier methods fail to provide an accurate method to account for the effects of BHI and tend to either underestimate or overestimate the value of the actual Richardson constant.

To summarize, the T_0 approximation cannot be applied for low ideality factor cases or more specifically in the HB dominated regime. n-Φ_{Beff} plots show the presence of distinct linear regimes that can be attributed to the HB (low n) and LB (high n) dominated regimes. Extrapolation of the n-Φ_{B} plot in the HB dominated regime gives the homogeneous high barrier height, but in the case of the LB dominated regime, the extrapolation yields an effective barrier height higher than the homogeneous barrier height. Although the T_0 anomaly equations are a good approximation of the voltage and temperature dependence of the ideality factor in the LB dominated regime, the approximation is not valid in the HB dominated regime. Depending on the extent of inhomogeneity, the Richardson constant extracted using previous approaches can deviate significantly from the actual value. Hence, there is a need for an accurate method that can filter the effects of BHI on the extracted Richardson constant.

3.4 Proposed approach

In the HB dominated regime, the effects of BHI on the Richardson plot are reduced. Despite the reduced impact of BHI in the HB dominated regime, the Richardson constant extracted using the original Richardson plot can vary over orders of magnitude. Realizing the limitations of previous approaches, we have proposed a new and different approach based on Tung's BHI model [133].

The current flowing through an inhomogeneous Schottky diode characterized by the BHI parameters C_1 and σ is given by

$$\frac{I}{1-\exp(-\beta V)} = AA^*T^2 \exp\left(-\beta\Phi_{\mathrm{B}}\right)\left\{1+\frac{8C_1\pi\sigma^2}{9\beta_1}\exp\left(\frac{\beta^2\beta_1^2\sigma^2}{2}\right)\right\}\exp(\beta V), \tag{3.23}$$

where β_1 equals $(V_{bb}/\eta)^{\frac{1}{3}}$. In Equation (3.23), V_{bb} is the band bending at the measurement bias and $\eta = \epsilon_s/(qN_d)$ is a doping density dependent parameter[17] η determines the overall patch strength, and at higher doping levels (low η), conduction through low barrier regions is enhanced.

Taking the natural log of both sides of Eq. 3.23 and using the approximation $\ln(1+x) \approx x$ in the HB dominated regime, we can re-write Eq. (3.23) as

$$\ln\left(\frac{I}{1-\exp(-\beta V)}\right) = \beta V + \underbrace{\ln(AA^*T^2) + \frac{8\pi C_1\sigma^2}{9\beta_1}\exp\left(\frac{\beta^2\beta_1^2\sigma^2}{2}\right) - \beta\Phi_{\mathrm{B}}}_{\ln(I_{\mathrm{sat}})}. \tag{3.24}$$

Setting the $\ln(I_{\text{sat}})$ term from Eq. 3.24 equal to that in Eq. 3.4, we obtain

$$-\beta\Phi_{\text{Beff}} + \ln(A^*_{\text{eff}}) = -\beta\Phi_{\text{B}} + \ln(A^*) + \left\{\frac{8\pi C_1\sigma^2}{9\beta_1}\right\}\exp\left(\frac{\beta^2\beta_1^2\sigma^2}{2}\right). \tag{3.25}$$

Recognizing that the effective barrier height is the slope of the Richardson plot and can be obtained from the saturation current expression (given in Eq. 3.24),

$$\Phi_{\text{Beff}} = -\frac{\partial \ln\left(\frac{I_{\text{sat}}}{AA^*T^2}\right)}{\partial\beta} = \Phi_{\text{B}} - \left\{\frac{8\pi\beta_1 C_1\sigma^4}{9}\right\}\exp\left(\frac{\beta^2\beta_1^2\sigma^2}{2}\right)\beta. \tag{3.26}$$

Using Equations 3.25 and 3.26, we can now express the effective Richardson constant (A^*_{eff}) as

$$\ln(A^*_{\text{eff}}) = \ln(A^*) + \left(\beta - \frac{1}{\beta\beta_1^2\sigma^2}\right)(\Phi_{\text{Beff}} - \Phi_{\text{B}}). \tag{3.27}$$

Equation 3.27 shows that the extracted Richardson constant (A^*_{eff}) can be related to the effective barrier height (Φ_{Beff}), homogeneous Richardson constant (A^*) and homogeneous barrier height (Φ_{B}). A linear relationship between $\ln(A^*_{\text{eff}})$ and Φ_{Beff} exists, and as Φ_{Beff} approaches Φ_{B}, A^*_{eff} approaches A^*.

Equation 3.25 suggests that the extracted barrier height and Richardson constant are correlated, and as Φ_{B} approaches the homogeneous barrier height, the effective Richardson constant approaches the unaffected, homogeneous value (A^*). In other words, in the HB dominated regime, with diminishing BHI effect, both the

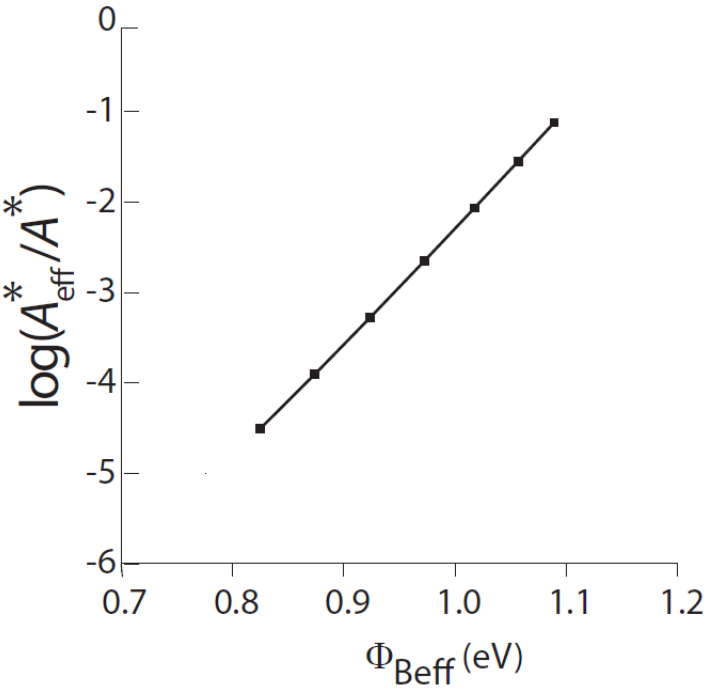

Figure 3.8. Linear correlation between $\ln(A^*_{\text{eff}})$ and Φ_{Beff} extracted from the original Richardson plot for several simulated devices. An input barrier height of 1.2 eV and Richardson constant of 26 A cm^{-2} K^{-2} have been assumed in this case.

effective barrier height and Richardson constant values approach their true values in a correlated fashion.

Figure 3.8 shows a typical $\log(A^*_{\text{eff}})$-Φ_{Beff} constructed using the extracted Richardson constant and effective barrier height values from several simulated devices. A homogeneous barrier height of 1.2 eV and A^* of 26 A cm^{-2} K^{-2} were assumed in this case. C_1 and σ values were chosen randomly within the range $1-5\times10^7$ cm^{-2} and $0.9-1.1\times10^{-4}$ cm$^{2/3}$ eV$^{1/3}$, respectively, to generate the data points on the plot. As mentioned earlier, in the HB regime, the n-Φ_{Beff} plot can be extrapolated to the homogeneous barrier height. The HB regime is indicated by the absence of bowing in the Richardson plot. Using the extracted ideality factor in the HB

dominated regime, and the effective barrier height from the Richardson plot, an n-Φ_{Beff} plot can be constructed. The $\ln(A^*_{\mathrm{eff}})$-Φ_{Beff} plot can be constructed using the $\ln(A^*_{\mathrm{eff}})$ and Φ_{Beff} values obtained from a set of devices. The homogeneous Richardson constant can then be extracted by extrapolating the $\ln(A^*_{\mathrm{eff}})$-Φ_{Beff} plot to $\Phi_{\mathrm{Beff}} = \Phi_{\mathrm{B0}}$. The zero-bias barrier height can be obtained from the n-Φ_{Beff} plot by extrapolation to $n = n_{\mathrm{if}}$.

Alternatively, the n-Φ_{Beff} plot can be constructed by using n values from the HB dominated regime and effective barrier height extracted from the I-V characteristics. However, to use the I-V characteristics to extract the effective barrier height, one would need to assume the Richardson constant. Since the n-Φ_{Beff} plot is coupled with the $\ln(A^*_{\mathrm{eff}})$-Φ_{Beff} plot to extract the true Richardson constant, assuming a Richardson constant value for the n-Φ_{Beff} is not justified. In order to overcome this limitation, an iterative approach can be employed. To begin, an initial guess for A^* is chosen to allow construction of the n-Φ_{Beff} plot. The homogeneous barrier height can then be extracted from the n-Φ_{Beff} plot and coupled with the $\ln(A^*_{\mathrm{eff}})$-Φ_{Beff} plot, so that a new estimate of the A^* value can be obtained. The new A^* value can then be used to modify the n-Φ_{Beff} plot, and the process is repeated until the desired convergence criteria is reached.

Application of the proposed methodology to emerging semiconductors such as the WBG class is particularly useful since experimental verification of the Richardson constant is largely hindered due to the lack of availability of good quality Schot-

tky diodes. As suggested by the above discussion, even modest ideality factors can result in a great scatter in the extracted Richardson constant. Consequently, the Richardson constant for WBG semiconductors such as ZnO, GaN is not very well established. In the following sections, we discuss the application of this method to the determination of Richardson constant of n-ZnO and n-GaN.

3.5 Application to IrO_x/n-ZnO I-V-T characteristics

Previously published temperature dependent studies on ZnO Schottky diodes report high ideality factor values ($n > 1.3$), and as a result, the extracted A^* values (about 0.2 A cm^{-2} K^{-2}) are far lower [134, 135] than the theoretical value. Recent studies indicate that nearly-ideal Schottky contacts to ZnO can be obtained through modified deposition techniques [136]. Nevertheless, we find that the extracted A^* values can still exhibit significant diode-to-diode variation.

In this work, we investigate the I-V-T characteristics of multiple low ideality factor SBDs fabricated using 300 μm diameter iridium oxide (IrO_x) Schottky contacts on the m-plane ($1\bar{1}00$) face of a melt grown bulk ZnO wafer from Cermet, Inc. (USA). A net donor concentration of 1×10^{17} cm^{-3} was determined from capacitance-voltage measurements. The fabrication procedure for these IrO_x diodes follows the methodology described in detail elsewhere [136]. Diode fabri-

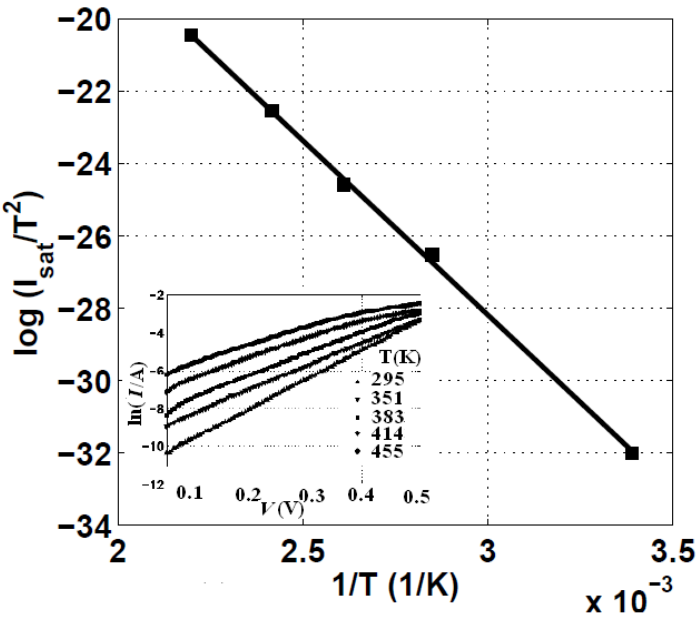

Figure 3.9. Typical Richardson plot extracted from I-V-T data (shown in the inset) of a Schottky contact to n-ZnO. From the I-V data at different temperatures, n and $I_{\rm sat}$ can be extracted using Eq. 3.1.

cation was carried out by Dr. Martin Allen at the University of Cantebury, New Zealand. The wafer was mounted on a hot stage, and the temperature was controlled and monitored using a Temptronics temperature controller, chromel-alumel thermocouple and a Keithley 2000 temperature measurement system. Electrical characterization was performed using a Keithley 4200 semiconductor characterization system. A typical Richardson plot of $\ln(I_{\rm sat}/AT^2)$ versus 1/T (shown in Fig. 3.9) can be constructed from the I-V-T characteristics (Fig. 3.9 inset) of the diodes tested in this study using Equations 3.1 and 3.4. Table 3.1 shows the effective Richardson constant ($A^*_{\rm eff}$), effective barrier height ($\Phi_{\rm Beff}$) and ideality factor extracted for several devices. The most important observation from Table 3.1 is that the extracted values of $A^*_{\rm eff}$ vary over a wide range. We also note that the

extracted values of A^*_{eff} are significantly different from the theoretically predicted value [135] for n-type ZnO of 32 A cm^{-2} K^{-2}.

Device No.	A^*_{eff} (A cm $^{-2}$ K^{-2})	Φ_{Beff} (eV)	n (295 K)
1	2.0	0.82	1.12
2	1.7	0.82	1.12
3	6.1	0.86	1.09
4	0.8	0.78	1.17

Table 3.1. Extracted effective Richardson constant and barrier height values for different devices obtained using the original Richardson plot

Figure 3.10 shows the linear correlation between $\ln(A^*_{\text{eff}})$ and Φ_{Beff}. The homogeneous A^* value is obtained by extrapolation to $\Phi_{\text{Beff}} = \Phi_{\text{B}}$. The homogeneous barrier height Φ_{B} can be determined from a plot of the effective barrier height versus the ideality factor for multiple SBDs. Φ_{B} is obtained by extrapolating the Φ_{Beff}-n plot to $n = n_{\text{if}}$, where n_{if} is the image force controlled ideality factor, [137] which has a value of 1.028 for these SBDs. Figure 3.11 shows the Φ_{Beff}-n plot for our SBDs from which a homogeneous barrier height of 0.91 $\pm$ 0.01 eV is extracted. Using this value, Fig. 3.10 yields a homogeneous Richardson constant for n-ZnO of 27 $\pm$ 7 A cm^{-2} K^{-2}, in very close agreement with the theoretically expected value of 32 A cm^{-2} K^{-2}. From Eq. 3.27, it can be seen that when the effective barrier height is lower than the homogeneous barrier height, the extracted Richardson constant tends to be lower than the expected Richardson constant. Although the HB regime is most amenable for the Richardson plot, the extracted Richardson constant value can still be lower than the expected value even when data are collected

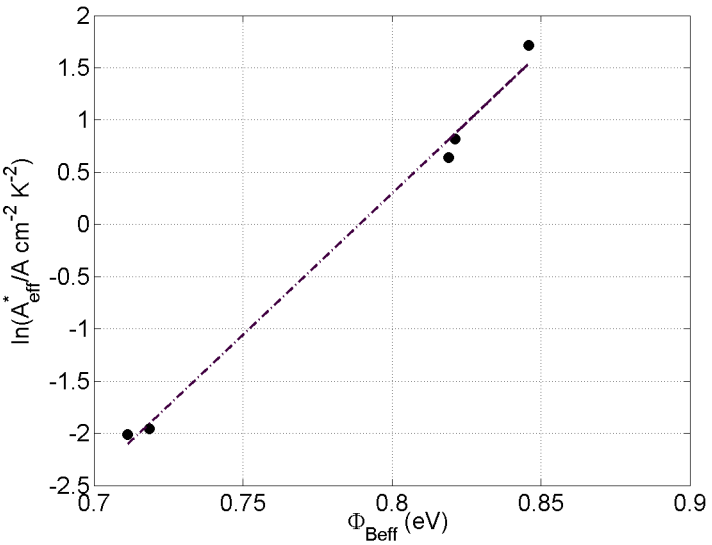

Figure 3.10. Linear correlation between $\ln(A^*_{\text{eff}})$ and Φ_{Beff} obtained from the Richardson plots for several devices.

in this regime. As the effective barrier height approaches the homogeneous barrier height, the effects of BHI become negligible and the extracted A^* approaches the homogeneous value. The present approach overcomes some of the difficulties with other commonly employed approaches, which rely on modifying the original Richardson plot in different ways [124, 16, 120, 138, 122]. Methods focusing on incorporating the effects of BHI tend to extract Tung's patch parameter (σ) from the I-V-T characteristics. Unfortunately, a unique patch parameter value is not possible from an I-V-T fitting exercise due to the presence of multiple solutions. Hence, these approaches do not offer an accurate method to account for BHI on the obtained Richardson constant value. Instead, we have utilized a linear correlation between the effective Richardson constant and barrier height values based on Tung's BHI model. The method has been used to extract the Richardson con-

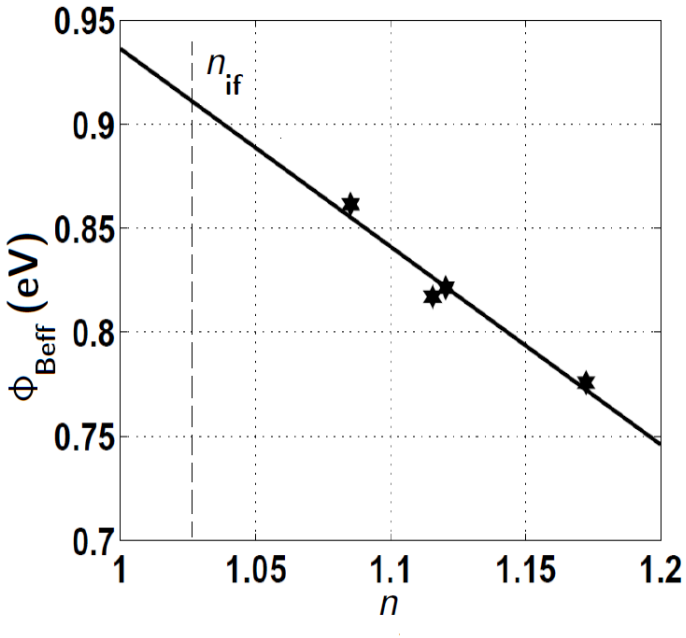

Figure 3.11. Φ_{Beff}-n plot used to determine the homogeneous barrier height of the IrO_x/n-ZnO Schottky diode.

stant of n-type ZnO using I-V-T characteristics measured on IrO_x/n-ZnO Schottky diodes. Using a homogeneous barrier height value of $\Phi_B = 0.91 \pm 0.01$ eV (obtained from the Φ_{Beff}-n plot), the linear correlation between $\ln(A^*) - \Phi_B$ yields a homogeneous Richardson constant value of 27 ± 7 A cm^{-2} K^{-2}. The obtained Richardson constant value is in very close agreement with the theoretically expected value of 32 A cm^{-2} K^{-2} and is, by far, the closest to the theoretical Richardson constant. The error bars are due to slight variations in the $\ln(A^*_{\text{eff}})$-Φ_{Beff} and n-Φ_{Beff} plots that occur as a result of the selected bias range used for parameter extraction and also diode-to-diode variations. Establishing the Richardson constant of n-ZnO using the proposed approach is one of the main contributions of this thesis. To further corraborate the approach, the application of the proposed method to determine

the Richardson constant of n-GaN from the I-V-T characteristics of Au/Ni/n-GaN Schottky diodes is described next.

3.6 Application to Au/Ni/n-GaN I-V-T data

3.6.1 Fabrication procedure

A GaN epi-layer doped with Si grown on a sapphire substrate was used for Schottky diode fabrication. Prior to the ohmic contact and Schottky metal deposition, the sample surface was cleaned using 10% HCl for 45 s. The ohmic contact was formed by depositing Ti/Al/Ni/Au layers of 30/120/50/20 nm thickness using e-beam evaporation followed by rapid thermal annealing at 800 ℃ for 60 s. Circular contacts (area = 10^{-3} cm^2) of Ni/Au (50/150 nm) were deposited using e-beam evaporation, and the contacts were defined using lift-off. A net donor concentration of 1 $\times 10^{17}$ cm^{-3} was determined from capacitance-voltage measurements of the Schottky contacts.

3.6.2 Device characterization

For the I-V-T measurements, the sample was mounted on a hot stage, and the temperature was controlled and monitored using a Temptronics temperature controller, chromel-alumel thermocouple and a Keithley 2000 temperature measurement system. Electrical characterization was performed using a Keithley 4200 Semiconduc-

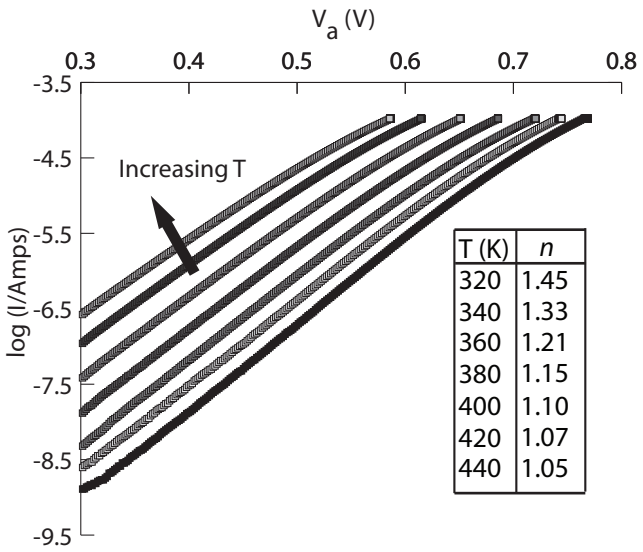

Figure 3.12. Typical *I-V-T* characteristics measured for Au/Ni/n-GaN Schottky diodes

tor Characterization system. *I-V-T* characteristics of the Au/Ni/n-GaN Schottky diodes were measured from 320–440 K, and a typical plot on a semi-log scale is shown in Figure 3.12. The diodes exhibit an ideality factor of about 1.45 at T = 320 K, and the ideality factor decreases to about 1.05 at T = 440 K. The high ideality factor values obtained at lower temperatures can be attributed to the presence of barrier height inhomogeneities. Contribution due to field emission can be neglected due the low doping density levels in these diodes. With increasing temperature the low barrier region contribution becomes less significant, and the current conduction becomes spatially homogeneous (ideality factor close to one).

Figure 3.13 shows a typical Richardson plot obtained from the *I-V-T* data of the n-GaN Schottky diodes. As evident in Figure 3.13, the effect of BHI is manifested as a curvature in the original Richardson plot.

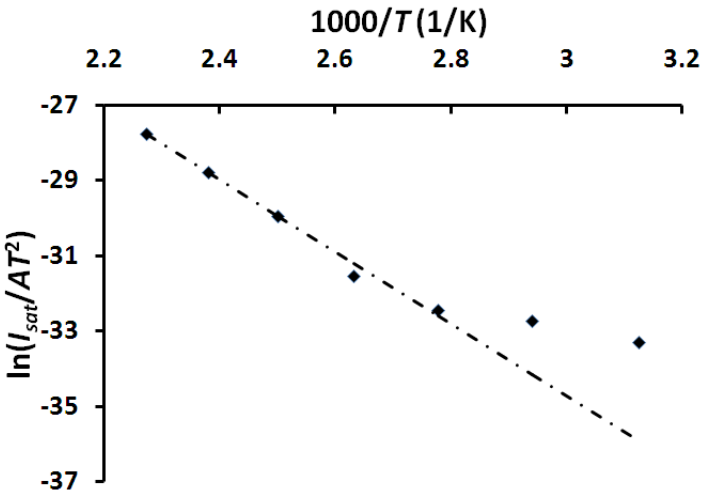

Figure 3.13. Typical Richardson plot obtained for the Au/Ni/n-GaN Schottky diode

Applying Equations 3.3 and 3.4 to the I-V-T data measured in the high temperature regime, we obtain the barrier height and Richardson constant for different devices. Due to the presence of BHI, these values would be expected to differ from the homogeneous values and are deemed as effective ones. Table 3.2 shows the extracted barrier height and Richardson constant values for different devices. The extracted Richardson constant values show a scatter over several orders of magnitude and are, also, orders of magnitude lower than the theoretical value of 26.4 A cm^{-2} K^{-2}. Depending on the extent of BHI, the extracted Richardson constant is found to vary greatly from device to device.

Figure 3.14 shows the correlation observed between the extracted barrier height and Richardson constant values on a semi-log scale. As suggested by our preceding discussion, as the barrier height increases towards the homogeneous barrier height, the extracted Richardson constant value increases from a low value towards the

Device No.	A^*_{eff} (A cm $^{-2}$ K^{-2})	Φ_{Beff} (eV)	n (380 K)
1	1.3 $\times 10^{-2}$	0.88	1.22
2	3.2 $\times 10^{-2}$	0.89	1.18
3	7.1 $\times 10^{-4}$	0.77	1.28
4	3.1 $\times 10^{-3}$	0.82	1.25

Table 3.2. Extracted Richardson constant values for different GaN Schottky diodes obtained using the original Richardson plot

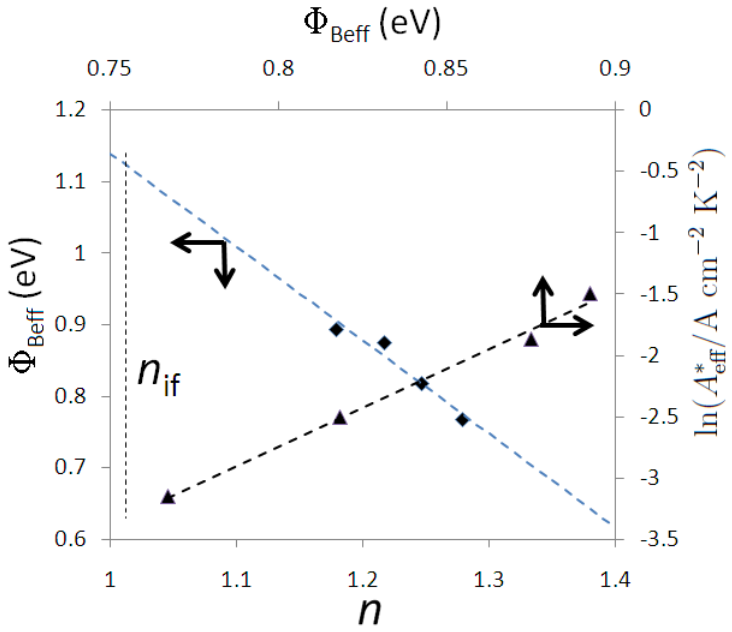

Figure 3.14. Linear correlations between n-Φ_{Beff} values and Φ_{Beff}-ln(A^*_{eff}) values

expected Richardson constant. Extrapolating the observed linear correlation to the point where the barrier height equals the zero-bias barrier height, we can obtain a good estimate of the actual Richardson constant value. The n-Φ_{Beff} plot is shown in Figure 3.14 and can be used to obtain the zero-bias barrier height. A zero-bias barrier height of 1.13 $\pm$ 0.01 eV is obtained by extrapolating the n-Φ_{Beff} plot to the image force controlled ideality factor, $n_{\text{if}} = 1.01$ (using Eq. 3.19).

A homogeneous Richardson constant value of 26 $\pm$ 6 A cm^{-2} K^{-2} can be

obtained using Figure 3.14 and Φ_{B0}. The homogeneous Richardson constant is in excellent agreement with the theoretically expected value of 26.4 A cm^{-2} K^{-2} [139]. It is important to note that a wide range of A^* values have been reported in the literature [140, 141, 142, 143, 144]. The discrepancy between experimentally observed A^* and theoretically expected value is typically attributed to inferior diode quality. However, even for diodes exhibiting low ideality factor values, the extracted Richardson constant can vary over orders of magnitude. The proposed approach overcomes this difficulty by filtering the effects of BHI on the extracted Richardson constant value.

3.7 Summary of results

Previous approaches to extract the Richardson constant, and the assorted modifications to the original Richardson plot to account for different non-ideality contributions, are described. Unfortunately, the currently employed methods can provide inaccurate results and fail to effectively filter the BHI effects. In this chapter, we have elaborated upon these shortcomings, and have also provided a new approach we recently proposed. In this chapter, this method is applied to IrO_x/n-ZnO and Au/Ni/n-GaN Schottky diodes as an example. The new method is based on Tung's BHI model and takes advantage of a linear correlation between the extracted Richardson constant and the effective barrier height.

Based on the preceding analysis and discussion, we can provide a few sim-

ple guidelines that are useful to account for the effects of BHI on the extracted Richardson constant. One of the key points to be noted is that even in the case of moderate ideality factors (~ 1.1), the extracted Richardson constant can be widely different than the expected or actual value. It has been difficult to extract an accurate Richardson constant using previous approaches due to large variations from device to device. When the Richardson plot exhibits bowing, higher measurement temperatures should be used, instead of using the modified Richardson plot. As suggested earlier, the modified Richardson plot does not necessarily provide an accurate method to extract the Richardson constant. In the case of MS diodes with low homogeneous barrier heights, adequately high temperatures might not be accessible since I-V-T measurements are further complicated due to series resistance effects or due to interfacial reactions at high temperatures. After choosing the appropriate temperature window, the original Richardson plot can be used to extract the effective Richardson constant and effective barrier height for each of a set of devices. These values can then be used to construct the $\ln(A^*_{\text{eff}})$ vs.Φ_{Beff} plot. In order to obtain the homogeneous Richardson constant, one would need the zero-bias barrier height, and this can be obtained from the n-Φ_{Beff} plot. The n values in the HBD regime along with the effective barrier height can be used to construct the n-Φ_{Beff} plot.

Using the proposed linear correlation and the widely-used n-Φ_{Beff} plot, we have analyzed I-V-T data from the simulated semi-Gaussian BHI model, IrO_x/n-ZnO

and Au/Ni/n-GaN Schottky diodes. Excellent correlation between the expected and extracted values has been shown for these cases. The proposed method offers a simple way to extract Richardson constant, and, in essence, is similar to the n-Φ_{Beff} analysis. The proposed method is particularly valuable for semiconductor systems that are still shrouded in uncertainty due in part to immature crystal growth and processing methodology.

For moderately doped semiconductors, Schottky diode parameters extracted from the I-V characteristics are heavily influenced by the presence of BHI. The work presented in this article has dealt with re-visiting the applicability of the commonly employed approaches to the extraction of Richardson constant. The need for a methodology that relies on application of BHI principles and, thereby, accounts for the effects of BHI on the extracted Richardson constant has been realized. An explicit relation between the extracted Richardson constant and the BHI parameters serves as the basis for the proposed approach. This approach has been shown to provide an accurate way to extract the Richardson constant from the I-V-T characteristics of an inhomogeneous Schottky barrier diode.

Chapter 4

Extracting the Schottky barrier height from axial contacts to semiconductor nanowires

4.1 Introduction

Nanoscale contacts are important for novel devices based on semiconductor nanowires such as field effect transistors and chemical and biological sensors [145, 146]. For a variety of reasons, the behavior of these contacts can depart significantly from that of their microscale counterparts. For example, in the case of nanoscale contacts to a bulk semiconductor, barrier width thinning is predicted by solving the Poisson equation in this geometry, and an increase in tunneling current is experimentally observed [147, 148]. Apart from geometric effects, Fermi-level pinning at the inter-

face between the metal and semiconductor might be reduced for nanoscale contacts compared to bulk Schottky contacts [149, 102].

Experimental data on the current-voltage (I-V) characteristics of Schottky contacts to different semiconductor nanowires (such as Si, ZnO and GaN) show deviation from the conventional thermionic emission theory [150, 98, 151]. Large ideality factors have been observed in Schottky contacts to n-GaN nanowires [151], whereas room-temperature ideality factors of about 1.2 for Ni contacts to n-type Si nanowires [150], or 1.1 for Pt contacts to n-ZnO [98] nanowires and axial θ-Ni_2Si/Si nanowires [150], have been reported. A tunneling current contribution has been suggested to be the source for the observed deviation from thermionic emission theory. In addition, the Schottky barrier depletion width can be influenced by surface charge present along the adjacent surface of the nanowire [152]. For these reasons, the Schottky barrier height extracted from the current-voltage (I-V) characteristics might be significantly different from the actual barrier height. So far, a systematic investigation of the effect of the nanowire surface on the metal/nanowire Schottky diode I-V characteristics and the means to extract the true Schottky barrier height from the I-V characteristics has not been reported. The goal of this work is to analyze simulated I-V characteristics of an axial Schottky barrier diode to a semiconductor nanowire with a surround gate in order to devise a method to accurately extract the Schottky barrier height from experimental I-V data. A surround gate structure provides symmetric control over the nanowire surface and facilitates a

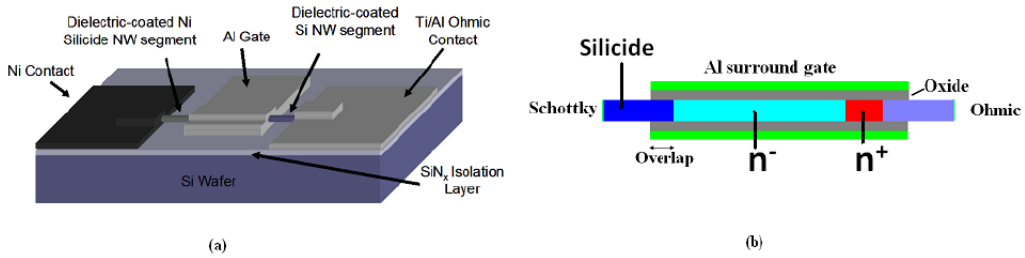

Figure 4.1. (a) Schematic of a surround-gate nickel silicide/n-Si NW Schottky diode structure. The specific metals shown were used in the nanofabricated device described later in the paper, while the simulations are more general for metallic and Si segments. (b) Cross-sectional schematic showing gate and silicide overlap.

systematic study of the effect of surface charge on the I-V characteristics. The surround-gate structure is also of importance because of its use in nanowire FETs (NWFETs) and is expected to help further device scaling [153, 154]. A key finding of the study is that I-V characteristics as a function of the surround gate bias are required to extract the true barrier height of the metal/semiconductor Schottky barrier diode. The range of required gate biases depends on the nanowire doping density, trap density at the oxide/nanowire interface, and measurement temperature. Under the influence of gate bias, the relative contributions of tunneling and thermionic emission can be modulated, and spatially non-uniform tunneling current density is found to be the key factor distorting the simulated I-V characteristics. Application of the proposed methodology to experimental data collected from a surround-gate θ-Ni_2Si/n-Si nanowire device is finally presented.

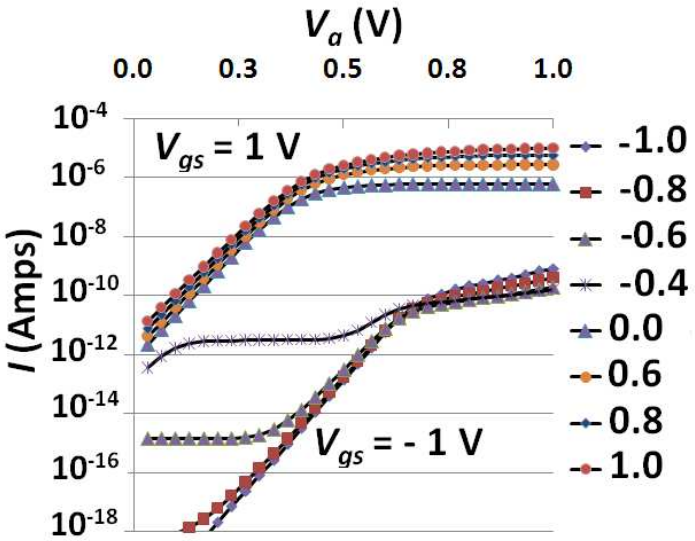

Figure 4.2. Typical *I-V* characteristics simulated using SDEVICE for the structure shown in Figure 4.1.

4.2 Simulated device structure and parameters

Figure 4.1(a) shows a schematic of the surround gate nanowire Schottky diode structure that we have used in our study. The device structure consists of an 0.8 μm long lightly doped n-type nanowire followed by a 0.2 μm long n^+ segment. Doping of the lightly doped segment can be varied and is treated as a simulation parameter in our study. An oxide shell of 10 nm thickness surrounds the 25 nm radius nanowire, and an aluminum gate wraps around to form a cylindrical metal-oxide-semiconductor structure. Traps distributed uniformly across the forbidden gap are assumed to be present at the Si/SiO_2 interface along the nanowire length. Interface trap density is treated as a simulation parameter to assess its effect on conduction through the nanowire Schottky diode. The nanowire rests on a SiN_x isolation layer deposited on an n-type Si wafer. A Schottky contact is defined

on the lightly doped side, and the barrier height in this simulation depends on the work function of the metal. However, the simulation results are valid even if Fermi-level pinning is present, in which case, we are simply running a simulation for a particular Schottky barrier height. The barrier height affects the current-voltage-temperature (I-V-T) characteristics and also the relative contributions of thermionic emission and thermionic field emission. An ohmic contact is defined on the heavily doped segment.

In the actual surround gate (SG)-NW Schottky diode described later in this paper, the Schottky contact is a metal silicide formed by rapid thermal annealing of the deposited contact metal. The silicidation process results in a cross-sectionally uniform and an atomically abrupt metal silicide/nanowire contact that can be reproducibly fabricated [155]. However, the contact silicidation process does not guarantee a self-aligned silicide-gate structure and almost always results in some amount of gate overlap onto the dielectric-coated silicide segment. Figure 4.1(b) shows a cross-sectional schematic of the possible overlap between the gate and the silicide segment. The impact of the resultant gate overlap on the conduction through the silicide/NW Schottky barrier is also studied using device simulations.

The device structure is simulated using Sentaurus Structure Editor, and the device characteristics are simulated using the 3D Sentaurus Device (SDEVICE) simulator. Poisson's equation in 3D and the current continuity equations with trap statistics, along with the appropriate boundary conditions, are solved using

the device simulator to obtain the I-V-T characteristics. The simulation set-up is used to explore the effect of nanowire doping, interface trap density, gate bias, Schottky barrier height and temperature on the conduction properties of the surround-gate nanowire Schottky diode.

4.3 Gate bias effects

Forward bias I-V characteristics as a function of the surround gate bias were obtained for a matrix of the listed input parameters. Figure 4.2 shows the typical I-V characteristics (T = 300 K) obtained for a gate sweep from -1 V to +1 V. An input barrier height of 580 meV and NW doping density of 10^{16} cm^{-3} were used in this case. Negative gate voltage corresponds to a surface inversion condition for the portion of the NW unaffected by the Schottky barrier. With increasing gate voltage, the nanowire surface switches to surface depletion followed by accumulation. Under ideal thermionic emission theory for bulk contacts, the current-voltage relationship is given by

$$\ln\left(\frac{I}{1-\exp(-\beta V_a)}\right) = \beta\frac{V_a}{n} - \beta\Phi_{\text{Beff}} + \ln(AA^*T^2). \tag{4.1}$$

In Eq. 4.1, I is the total current flowing through the diode under application of a forward bias of V_a, β (q/kT) is the inverse thermal voltage, A is the cross-sectional area of the diode, A^* is the Richardson's constant and T is the absolute

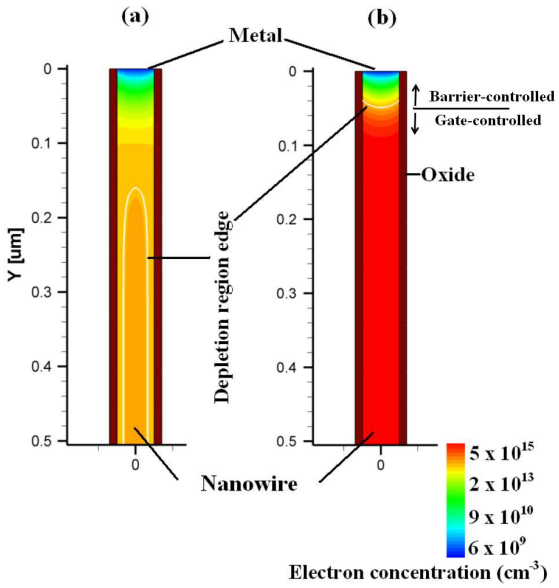

Figure 4.3. Depletion region edge profile under (a) surface depletion and (b) surface accumulation conditions.

temperature. The constants q and k are the electronic charge and Boltzmann constant, respectively. The diode behavior is characterized by the conventional Schottky diode parameters; n is the ideality factor and Φ_{Beff} is the effective barrier height. In the case of an ideal Schottky contact, n approaches unity and the effective barrier height approaches the homogeneous barrier height Φ_{B}.

A family of I-V curves (a typical case shown in Fig. 4.2) is generated by stepping through appropriate gate-to-source voltages V_{gs} and sweeping the Schottky contact from 0 to + 1V. In each case, the I-V data are then treated as would normally be done for a planar Schottky barrier diode. As the gate voltage is increased, the

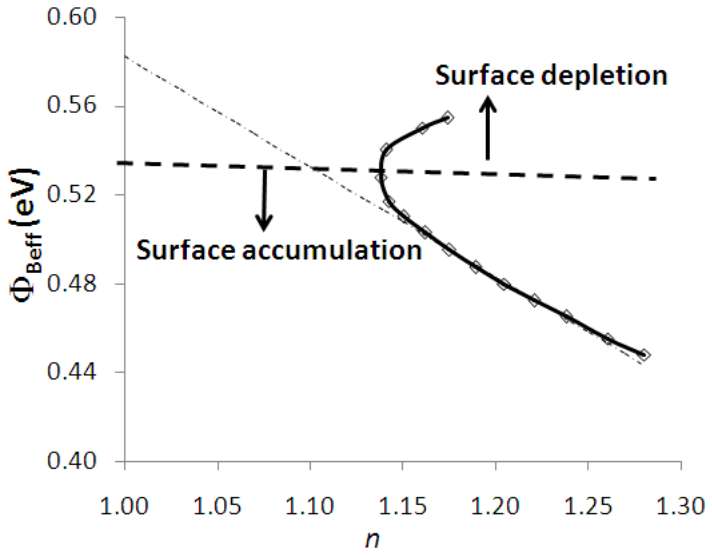

Figure 4.4. Typical n-Φ_{Beff} plot constructed using values extracted from I-V characteristics at different gate biases.

portion of the NW unaffected by the Schottky barrier shifts from surface depletion to surface accumulation. In the surface depletion regime, the effective diode area is reduced and results in an increase in apparent barrier height. As the gate voltage is swept into the surface accumulation regime, the apparent barrier height decreases. The decrease in the apparent barrier height is attributed to a tunneling contribution and is examined in detail later. The relative extent of electrostatic control over the semiconductor NW exerted by the Schottky contact and the surround gate is a result of the interplay between several parameters: NW doping density, applied bias, interface trap density, temperature and Schottky barrier height. Close to the metal/nanowire interface, the nanowire fixed and free charge densities are strongly influenced but not exclusively controlled by the Schottky contact. Away from the metal/nanowire interface, the surround gate provides symmetric control over the

nanowire surface and can be used to accumulate, deplete or invert the surface of the nanowire.

For gate voltages less than the flat band voltage (V_{FB}), the nanowire surface is depleted, and for $V_{gs} > V_{FB}$, the nanowire surface is accumulated. Electron concentration contours are shown in Figure 4.3 for surface depletion and surface accumulation conditions. Each case results in a curvature to the axial Schottky barrier depletion region edge. Under surface accumulation conditions, the barrier width thins along the nanowire periphery. Also, with increasing gate bias, the depletion region edge moves closer to the MS interface. Apart from thermionic emission over the barrier, gate bias dependent barrier thinning can enhance tunneling contributions across the periphery of the contact. Consequently, the current-voltage (I-V) characteristics in the surface accumulation conditions depart from the ideal thermionic emission theory giving rise to $n > 1$. It should be noted that even under zero gate-bias conditions, the depletion region edge can vary radially, and the sign and degree of this variation depends on the nature and density of interface traps on the nanowire surface along its length. The surround-gate architecture provides maximum control over the nanowire surface and allows us to override the effect of interface traps on the nanowire conduction properties.

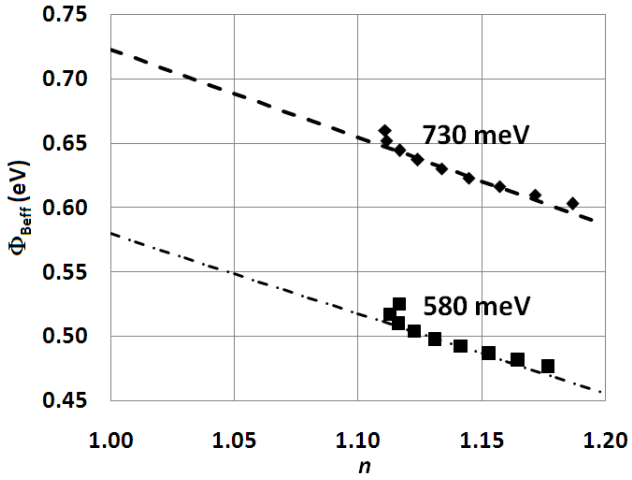

Figure 4.5. Linear correlation between n and Φ_{Beff} for two different input barrier height cases. Gate bias values ranging between 0.2–1 V were used in both cases.

4.4 n-Φ_{B} analysis

Simulated I-V data obtained from SDEVICE are treated in this work in a similar fashion to the I-V characteristics of a bulk contact. An important distinction, however, is that the extracted ideality factor and effective barrier height are a function of the surround gate bias. An n-Φ_{Beff} plot can be constructed using the gate bias dependent ideality factor and effective barrier height values. A typical n-Φ_{Beff} plot is shown in Fig. 4.4 and exhibits certain unique features as discussed below. For $V_{gs} > V_{\mathrm{FB}}$, the nanowire surface is accumulated and carrier conduction is due to a combination of thermionic emission and tunneling processes. The tunneling current contribution increases with increasing gate bias and results in an increase in ideality factor and a corresponding decrease in the effective barrier height. At gate bias values that result in moderate accumulation at the nanowire surface, a linear correlation between n and Φ_{Beff} is observed, and this linear region can be

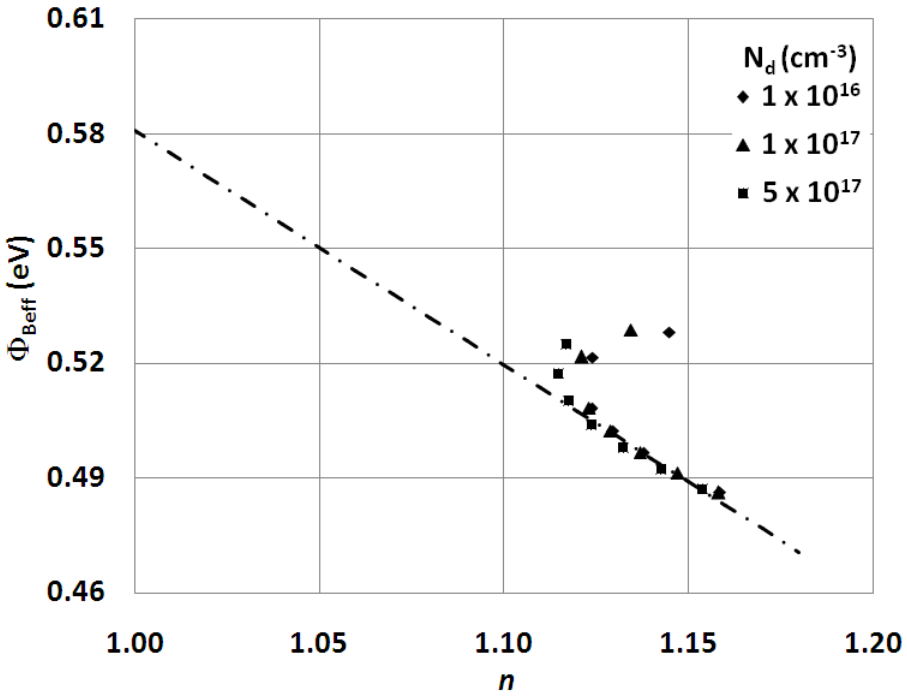

Figure 4.6. Effect of nanowire doping density on the n-Φ_{Beff} plot. An input Schottky barrier height of 580 meV, oxide/nanowire interface trap density of 1×10^{12} cm^{-2} eV^{-1} and $T = 300$ K have been assumed.

extrapolated to the actual barrier height. Under deep accumulation conditions, the tunneling current contribution becomes dominant and results in larger ideality factor values. For these slightly larger n values, a departure from the n-Φ_{Beff} linear correlation is observed. For $V_{gs} < V_{\text{FB}}$, the effective area for conduction is reduced due to depletion induced by the surround gate. As the nanowire is pushed deeper into depletion, the effective area for conduction further decreases and results in an increase in both the ideality factor and effective barrier height values.

Figure 4.5 shows the n-Φ_{Beff} plot for the cases of two different input barrier heights (580 and 730 meV). The nanowire is assumed to be doped n-type with a donor density of 10^{16} cm^{-3} and is simulated at 300 K. Ideality factor and Φ_{Beff}

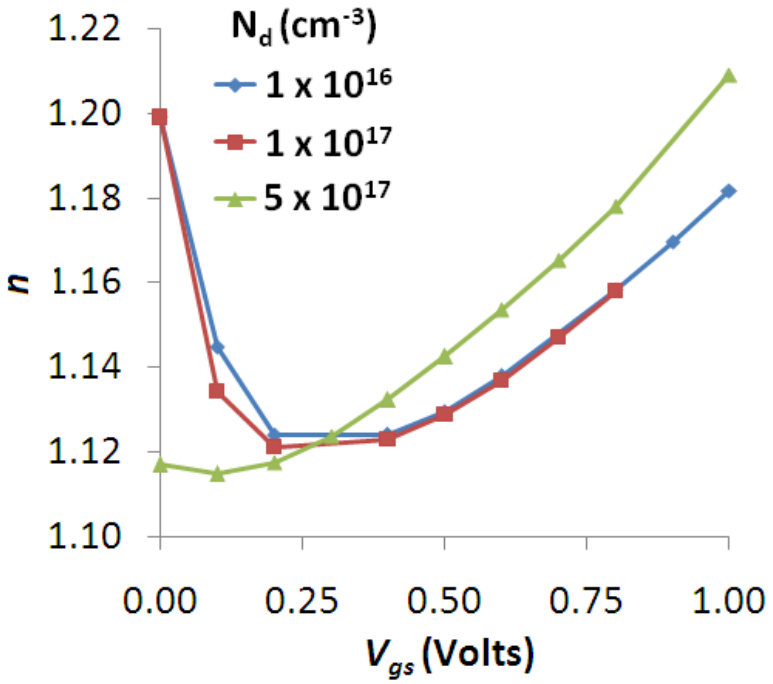

Figure 4.7. Extracted ideality factor as a function of V_{gs} for different nanowire doping densities.

values obtained at different gate bias conditions are used to generate Fig. 4.5, and the linear region can be extrapolated to $n = 1$ to obtain the input barrier height in both cases. The minor effect of image force lowering is discussed later in the paper. The linear correlation has been observed under different conditions of interface trap density, NW doping density, input barrier height, gate overlap and temperature. Depending on the MS interface barrier height, nanowire doping density, gate overlap and temperature, the tunneling current contribution to the total current differs. In order to verify the applicability of the n-Φ_B plot to determine the true barrier height, I-V-T characteristics were obtained for different test cases by varying these simulation parameters and are examined next.

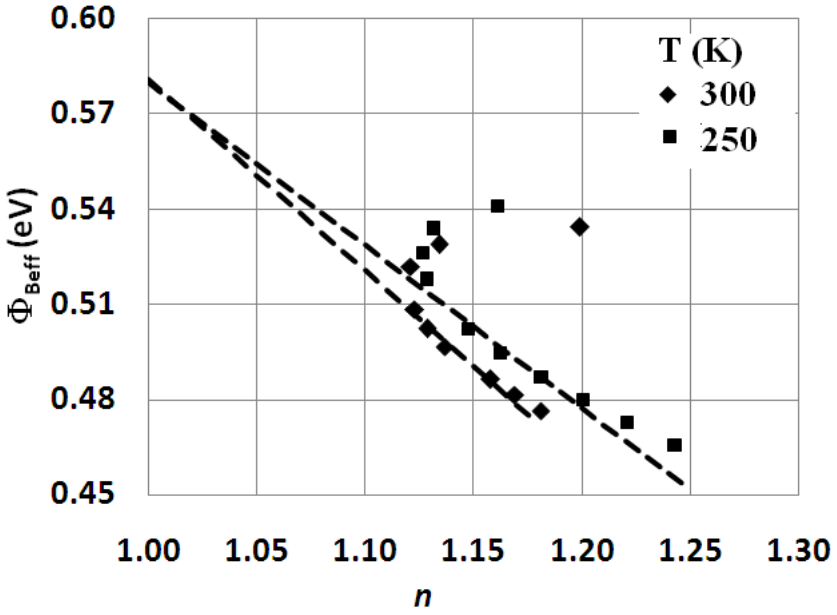

Figure 4.8. Effect of temperature on the n-Φ_{Beff} plot for the case of a nanowire doped to 10^{16} cm^{-3} with an interface trap density of 10^{12} cm^{-2} eV^{-1}. In this case, an input Schottky height of 580 meV has been used.

4.4.1 Effect of NW doping density

Figure 4.6 shows the n-Φ_{Beff} correlation obtained for three different NW doping densities (10^{16}, 10^{17} and 5×10^{17} cm^{-3}). In this case, we have assumed the Si/SiO_2 interface to be devoid of interface traps and the temperature is set to 300 K. Larger tunneling current contributions are expected at higher doping densities, so an increase in ideality factor is observed for higher doping density. Figure 4.7 shows the dependence of the extracted ideality factor on the applied gate bias. At a given gate bias in surface accumulation condition, the ideality factor increases with increasing nanowire doping density (Fig. 4.7), but the doping density does not have a noticeable effect on the n-Φ_{Beff} plot, as seen in Figure 4.6. The n-V_{gs} plot is useful

for estimating the gate voltage regime for surface accumulation conditions. As the gate voltage is swept from surface depletion to surface accumulation conditions, the ideality factor decreases initially and increases thereafter. As a consequence, the n-V_{gs} plot exhibits a minimum at a certain gate voltage ($V_{gs}^{\min}$). For $V_{gs} > V_{gs}^{\min}$, the surface moves deeper into surface accumulation and an increase in the ideality factor with gate voltage is observed. For $V_{gs} < V_{gs}^{\min}$, the ideality factor decreases with increasing gate voltage as the surface moves from a depleted condition to flat band condition.

4.4.2 Effect of temperature

Figure 4.8 shows the n-Φ_{Beff} correlation at two different temperatures (300 and 250 K). A Schottky barrier height of 580 meV, nanowire doping density of 10^{16} cm^{-3}, and an interface trap density of 10^{12} cm^{-2} eV^{-1} were used in this case. With decreasing temperature, the contribution due to thermionic emission is reduced, and we observe larger deviations from ideal behavior. Hence, for a given gate bias in the surface accumulation condition, the ideality factor increases with decreasing temperature. Figure 4.9 shows the n-V_{gs} variation for the two different temperatures, with higher ideality factor values for $T = 250$ K. Extrapolating the linear correlation from an n-Φ_{Beff} plot at either of the temperatures yields a barrier height of 580 $\pm$ 3 meV.

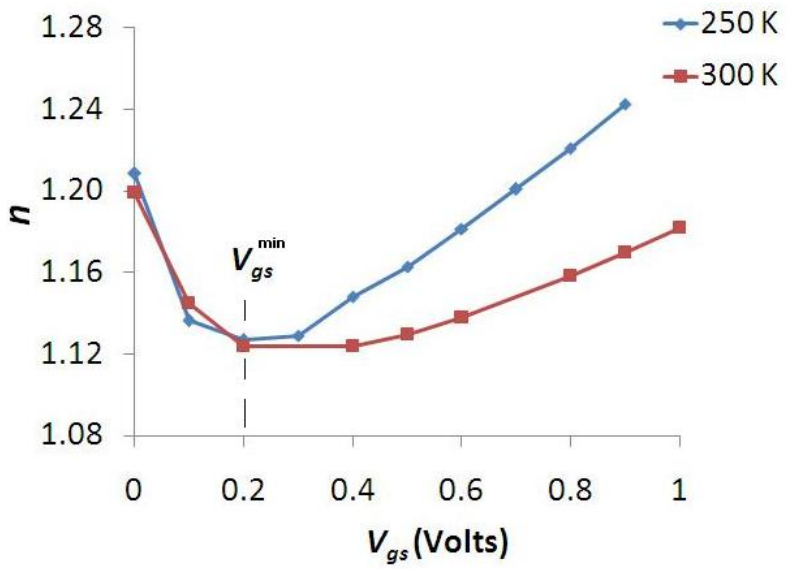

Figure 4.9. n-V_{gs} variation for different temperatures.

4.4.3 Effect of interface traps

Unlike the case we have examined so far, real silicon/oxide interfaces often contain traps. In a bulk Schottky contact, traps are present at the MS interface, and these defect states can pin the Fermi level, thereby dictating the obtained barrier height. A local variation of the interface trap density and their energies have been postulated to give rise to lateral variations in the barrier height [25]. In the case of a Schottky contact to a nanowire, the reduced size of the contact makes less likely such lateral variations of barrier height. However, traps present at the adjacent oxide/nanowire interface can influence conduction at the metal/NW contact. In these simulations, interface traps distributed uniformly across the energy band gap and with electron and hole capture cross-section values of 10^{-14} cm^2 are assumed to be present along the Si/SiO_2 interface. The I-V characteristics as a function of

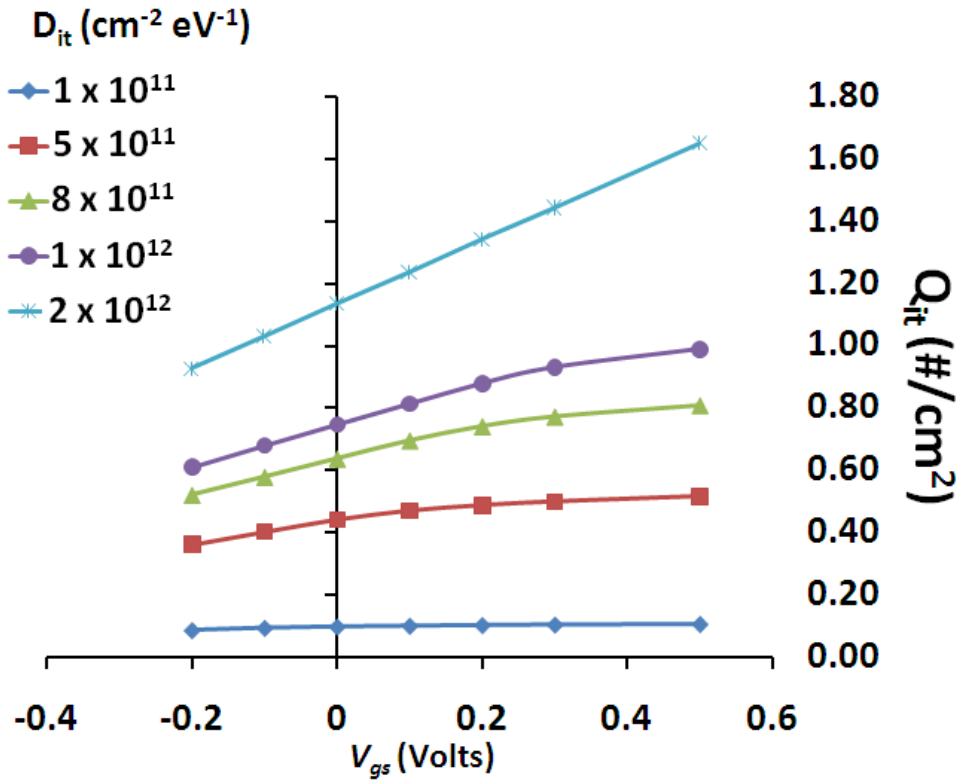

Figure 4.10. Trapped interface charge (for different interface trap densities) as a function of the applied gate bias.

gate bias have been simulated for different interface trap densities. The primary effect of interface traps is to increase the flat band voltage and postpone the surface accumulation condition. The presence of fixed oxide charge shifts the flat band voltage, but interface traps "smear" the effect of gate voltage. Under the application of a gate bias, a part of the gate voltage is used in free carrier accumulation, and the rest results in an increase in trapped interface charge. However, the increase in interface trapped charge with gate voltage is not linear and implies a gate bias dependent interface trap capacitance. Figure 4.10 shows the trapped interface charge as a function of the applied gate voltage. The onset of strong surface accu-

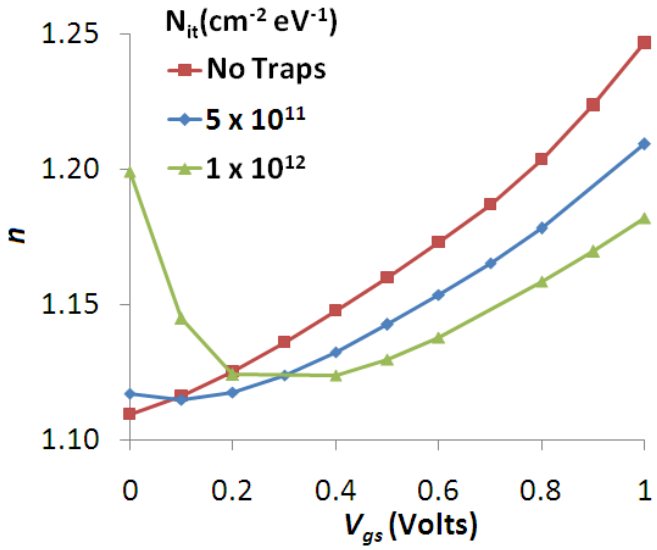

Figure 4.11. Effect of interface trap density on the n-V_{gs} plot.

mulation occurs when the gate voltage dependence of the interface trapped charge saturates. Any change in the gate voltage is therefore utilized in accumulation of free carriers at the surface and also in modulating the trapped charge at the oxide/nanowire interface. At higher interface trap densities, significantly higher gate voltages are required to saturate the trapped interface charge. Figure 4.11 shows the variation of n with V_{gs} for different interface trap densities. With increasing trap density, the MS depletion region edge is pinned more effectively by the oxide/nanowire interface traps. Hence, for a given gate bias, the MS depletion region is found farther into the nanowire away from the MS interface, resulting in a lower tunneling current contribution at a given gate bias. As a result, for a given gate bias, the extracted ideality factor is lower for higher interface trap densities. Figure 4.12 compares the n-Φ_{Beff} plot for different interface trap densities. The n-Φ_{Beff} plots display a curvature at low n values that becomes more prominent

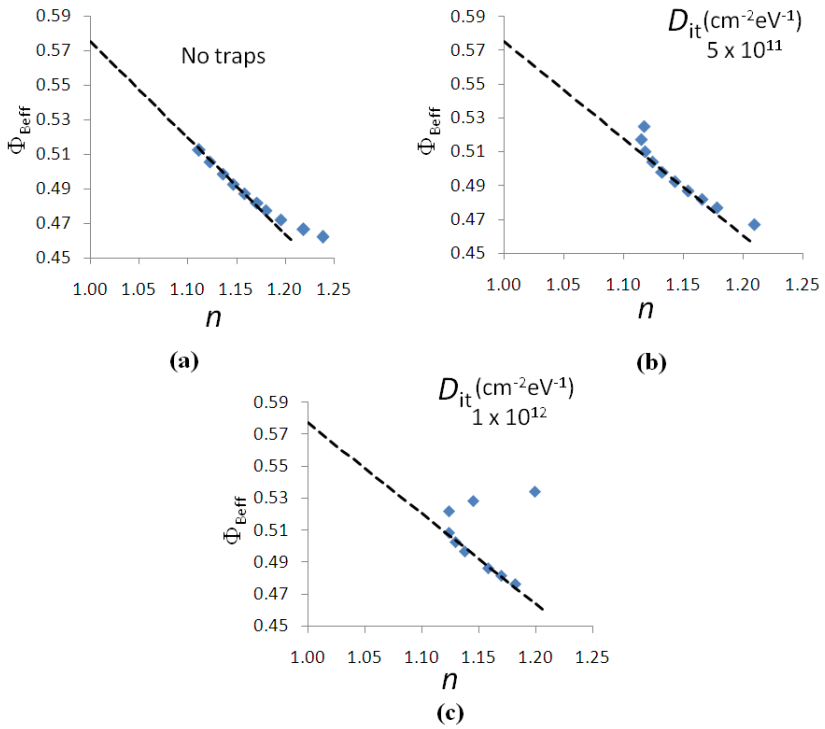

Figure 4.12. n-Φ_{Beff} plot for different interface trap densities: (a) no interface traps with $0 < V_{gs} < 0.5$ was used for the linear correlation, (b) 5×10^{11} cm^{-2} eV^{-1} traps with $0.2 < V_{gs} < 0.7$ was used for the linear correlation, and (c) 1×10^{12} cm^{-2} eV^{-1} traps with $0.4 < V_{gs} < 1$ was used for the linear correlation. An input Schottky barrier height of 580 meV, nanowire doping density of 10^{16} cm^{-3}, and $T = 300$ K have been assumed.

with increasing trap density. The curvature results from using n-Φ_{Beff} values from the surface depletion conditions. For these values, the applied V_{gs} is lower than the corresponding $V_{gs}^{\min}$, and in this regime, both the ideality factor and barrier height decrease with increasing gate bias. At a high enough gate bias, the surface is under accumulation irrespective of the surface trap density, and in this regime, the n-Φ_{Beff} plot is linear and can be used to extrapolate to the input barrier height. Compared to a planar Si/SiO_2 interface, the nanowire Si/SiO_2 interface might have a higher interface trap density. In the case of a nanowire, the oxide growth occurs

along different crystal orientations (and at different rates). Interface trap densities on the order of 2×10^{12} cm^{-2} eV^{-1} have been estimated based on subthreshold slope calculations for Si NWFETs [156]. However, the interface trap density could be reduced through post-oxidation annealing treatment [157, 158, 159].

4.4.4 Effect of gate overlap

Depending on the gate-silicide overlap, the capacitive coupling effect of the gate on the MS depletion region can differ and is examined here. Figure 4.13 shows the n-V_{gs} plot for different cases of gate overlap. The self-aligned case is when there is no gate overlap on the silicide segment. Under surface accumulation conditions, for a given gate bias, the ideality factor increases with increasing overlap. For larger gate overlap, the peripheral barrier thinning effect is enhanced, resulting in a larger tunneling contribution for a given gate bias. Figure 4.14 shows the correlation between n and Φ_{Beff} for different overlap conditions. In all cases, a barrier height of 580 $\pm$ 7 meV is obtained by extrapolating to $n = 1$ and matches the input barrier height used for the simulations.

4.4.5 Image force lowering effect

In the case of a homogeneous Schottky contact to a bulk semiconductor, the effective barrier height equals the zero-bias barrier height (Φ_{B0}) and can be related to

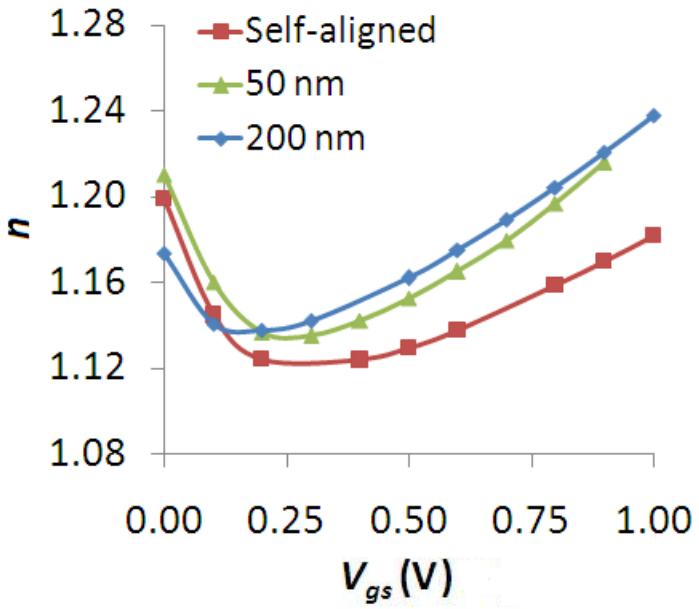

Figure 4.13. Effect of gate overlap over the n-V_{gs} plot.

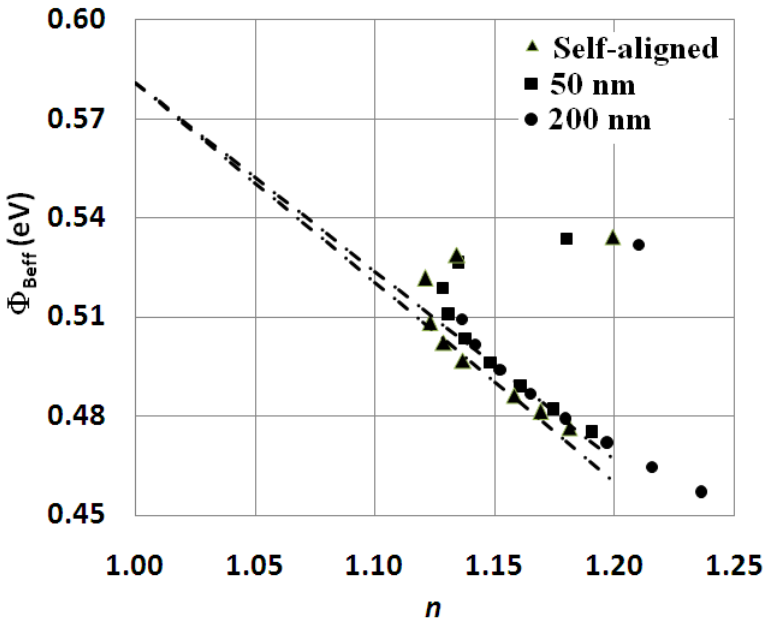

Figure 4.14. Effect of gate overlap over the n-Φ_{Beff} variation. An input Schottky barrier height of 580 meV, nanowire doping density of 10^{16} cm^{-3}, and interface trap density of 10^{12} cm^{-2} eV^{-1} have been assumed.

the homogeneous barrier height (Φ_{B}) by

$$\Phi_{\mathrm{B0}} = \Phi_{\mathrm{B}} - \Delta\Phi_{\mathrm{B}}, \tag{4.2}$$

where $\Delta\Phi_{\mathrm{B}}$ is the barrier lowering contribution due to the image force effect. The extent of barrier lowering due to the image force depends on the substrate doping density (N_d) and is given by [137]

$$\Delta\Phi_{\mathrm{B}} = \left(\frac{q^3 N_d V_{bb}}{8\pi^2 \epsilon_\infty^2 \epsilon_s \epsilon_0^3} \right)^{\frac{1}{4}}. \tag{4.3}$$

In Eq. 4.3, V_{bb} is the band bending, ϵ_0 is the permittivity of free space, and ϵ_s and ϵ_∞ are the static and optical dielectric constants. The image force barrier lowering effect also results in a slight increase in the ideality factor to n_{if} and is given by [137]

$$n_{\mathrm{if}} = 1 + \frac{1}{4} \left(\frac{q^3 N_d}{8\pi^2 \epsilon_\infty^2 \epsilon_s \epsilon_0^3 V_{bb}^3} \right)^{\frac{1}{4}}. \tag{4.4}$$

It should be noted that the effective barrier height and the image force controlled ideality factor show weak dependence on the applied bias. For moderately doped silicon, $\Delta\Phi_{\mathrm{B}}$ is typically about 10–30 meV, and n_{if} ranges from 1.01–1.03. Apart from the gate induced tunneling current contribution, the effective barrier height is also affected to a small extent due to the image force effect. The image

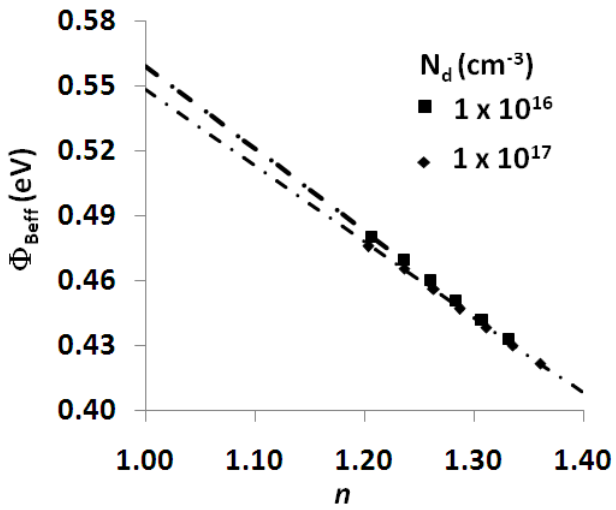

Figure 4.15. Effect of image force lowering on the n-Φ_{Beff} plot for the two different doping densities. An interface trap density of 10^{12} cm^{-2} eV^{-1}, input Schottky barrier height of 580 meV, and $T = 300$ K have been assumed.

force barrier lowering contribution would be of relatively greater significance for nanowires with a higher doping density. Fig. 4.15 shows the effect of barrier lowering on the n-Φ_{Beff} plot generated from room temperature I-V characteristics for the case of two different NW doping densities (10^{16} and 10^{17} cm^{-3}). The input barrier height is 580 meV and a gate overlap of 200 nm is used in both cases.

The n-Φ_{Beff} plot should be extrapolated to $n = n_{\text{if}}$ to obtain the zero-bias barrier height. The homogeneous barrier height can be obtained from the zero-bias barrier height using Eq. 4.2 and the estimated $\Delta\Phi_{\text{Beff}}$ value. Using the n-Φ_{Beff} plots shown in Fig. 4.15, a zero-bias barrier height of 560 and 550 meV can be obtained for 10^{16} and 10^{17} cm^{-3} NW doping densities, respectively. The zero-bias barrier heights are slightly lower than the homogeneous barrier height, and with increasing NW doping density, the zero-bias barrier height value is further lowered.

$\Delta\Phi_B$ values of 20 meV and 30 meV are estimated using Eq. 4.3. Using the zero-bias barrier height and the corresponding $\Delta\Phi_B$ values, a homogeneous barrier height of 580 meV can be obtained irrespective of the NW doping density. In the case of low to moderate doping levels, the value of n_{if} is close to 1 ($\sim$1.01) and extrapolating to $n = 1$ yields a good estimate of the homogeneous barrier height, as is done in the earlier sections of this paper.

In the preceding sections, different scenarios have been presented, and these cases illustrate the general applicability of the n-Φ_{Beff} method to obtain the true barrier height of a MS nanowire contact. A linear correlation between the extracted n and Φ_{Beff} is observed in inhomogeneous bulk Schottky diodes [132]. Although a linear correlation between n and Φ_{Beff} is observed in the nanowire case as well, the origin of the correlation is entirely different. In the nanowire case, gate bias dependent tunneling current gives rise to deviation from ideality and is the reason for the correlation between n and Φ_{Beff}.

4.5 Application to experimental data

4.5.1 Fabrication procedure

Silicon NWs were grown by the vapor-liquid-solid (VLS) method from a gold catalyst to a length of 16 μm with lightly and heavily doped n-type segments [160]. The lightly doped n-type segment was grown first to a length of 10 μm with a

PH_3/SiH_4 ratio of 1×10^{-4}, and then the heavily doped n-type segment was grown to a length of 6 μm with a PH_3/SiH_4 ratio of 2×10^{-3}. The SiNWs were soaked in Transene Au etchant to remove the Au tips from the nanowire and then thermally oxidized to form a 15 nm thick oxide shell surrounding the Si NW.

Sacrificial Ag electrodes were patterned on a Si wafer coated with 100 nm of SiN_x using photolithography, and a local Al back gate was patterned between the two Ag electrodes. SiNWs with a 15 nm thick oxide shell were then electrofluidically aligned to the Ag electrodes [161]. A window was next patterned over one of the Ag contacts (over one end of the nanowire) using photoresist, and the Ag electrode was etched away. Before depositing the Ni contact, a solution of 15% 10:1 BOE and 85% deionized water was used to remove the oxide shell surrounding the SiNW in the contact region. 80 nm of Ni was e-beam evaporated for the Schottky contact. A second window was opened to the second Ag electrode on the other end of the nanowire, and the Ag was again etched away along with the oxide shell surrounding the SiNW in this second contact region. 50 nm of Ti with a 50 nm cap of Al were then e-beam evaporated and used as the Ohmic contact to the SiNW. The Al top gate was then patterned on top of the local Al back gate to form a complete wrap-around gate surrounding the oxidized SiNW. Lastly, the devices were annealed at 550 ℃ for 240 s to form an axial nickel silicide segment that extended into the wrap-around gate such that the silicide/Si interface was surrounded by both the oxide shell of the SiNW and the Al wrap-around gate.

Note that the Ohmic contact does not react laterally down the nanowire under these conditions.

4.5.2 Electrical characterization

I-V characteristics were measured on a θ-Ni_2Si/n-Si NW Schottky diode at room temperature in a N_2 environment using an Agilent 4156B Precision Semiconductor Parameter Analyzer. Figure 4.16 shows the n-Φ_{Beff} plot obtained using the measured I-V characteristics at different gate bias values ($0.5 < V_{gs} < 1.5$ V). With increasing gate bias, the ideality factor increases and apparent barrier height decreases. In the case of the Sentaurus simulations, extrapolation of the linear n-Φ_{Beff} plot to $n = 1$ yields the actual barrier height, neglecting image force lowering. Using the same principle, in the case of the experimental θ-Ni_2Si/n-Si NW Schottky diode, a barrier height of 557 meV is obtained by extrapolation to $n = 1$, where image force lowering is expected to be small for the lightly doped nanowires. A future publication will address the effect of nanowire diameter on the Schottky barrier heights extracted by this method.

4.6 Conclusions

I-V characteristics of surround-gate Schottky diodes to semiconductor NWs have been simulated using SDEVICE. I-V characteristics of nanowire Schottky diodes are highly sensitive to the adjacent semiconductor surface, and a surround gate

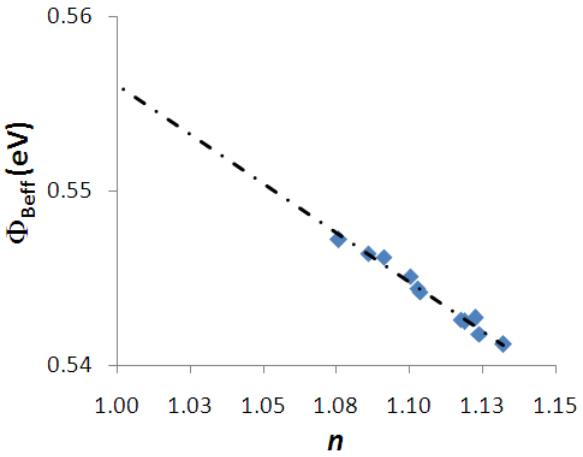

Figure 4.16. Linear correlation between n and Φ_{Beff} obtained from experimental I-V characteristics.

provides symmetric control of the surface condition. Under surface accumulation conditions, a spatially non-uniform tunneling contribution can be significant. The tunneling current contribution is gate bias dependent, and with increasing gate bias, the apparent barrier height decreases. As the gate bias is increased from surface depletion towards the flat band condition, both the ideality factor and barrier height decrease together. This trend is in contrast with the surface accumulation conditions, wherein increasing the gate bias increases the ideality factor and decreases the effective barrier height.

In this article, we have proposed a simple method for Schottky barrier height extraction from the I-V measurements of surround-gate Schottky contact to semiconductor nanowires. Spatially varying barrier width in these contacts has been shown to be the source for departure from thermionic emission, due to enhanced tunneling along the nanowire periphery. For a given metal/NW contact, the tun-

neling contribution can be modulated by varying the gate bias. Within limits, under surface accumulation conditions, a linear correlation between n and Φ_{B} has been observed, and extrapolating the linear correlation to $n = 1$ yields the input barrier height for Schottky barriers to lightly doped semiconductor nanowires. The n-V_{gs} plot exhibits a minimum at V_{gs}^{min} that signals the onset of surface accumulation conditions.

The linear correlation is shown to be valid considering the effects of NW doping, interface trap density, interface barrier height, temperature and gate overlap. In the case of nanowires with higher doping density, the image force lowering effect becomes important. Extrapolation of an n-Φ_{Beff} plot to $n = n_{\mathrm{if}}$ yields the zero-bias barrier height (Φ_{B0}). The homogeneous barrier height can then be obtained using Φ_{B0} and the estimated $\Delta\Phi_{\mathrm{B}}$ value. The extrapolated barrier heights under different test conditions have been found to be in good correlation with the input barrier height. A linear correlation between n and Φ_{B} is also observed for the case of experimental data from Ni silicide/n-Si nanowire Schottky diodes, and extrapolation to $n = 1$ yields a barrier height of 557 meV. In the next chapter, we review the application of a modified-version of the charge pumping method to qualify the oxide/nanowire interface. The methodology presented therein can be used to characterize the oxide/nanowire interface. The proposed method can serve as basis for comprehensive experimental investigations on the effects of interface condition on the nanowire conduction properties.

Chapter 5

Low frequency three terminal charge pumping applied to silicon nanowire field-effect-transistors

5.1 Introduction

Charge pumping (CP) is an important technique commonly used to assess gate oxide integrity and the overall reliability of metal-oxide-semiconductor field-effect transistors (MOSFETs) [162]. In its basic form, CP allows for a quantitative measure of the oxide-semiconductor interface trap density. Variants of the method have been developed over the past few decades to obtain the spatial and energy distribution of traps, electron and hole capture parameters, and localized damage profile due to electrical stress [163, 164, 165]. Often coupled with transfer charac-

teristics, CP can be used to uncover dominant damage mechanisms under different accelerated test conditions, such as hot-carrier and Fowler-Nordheim stresses [166]. In a bulk MOSFET the conventional CP (CCP) method employs four device contacts (gate, drain, source, and substrate/body), and the CCP output is a substrate current generated under the action of a large signal gate pulse. However, with the continuous miniaturization and diversification of devices, the field-effect transistor (FET) structure has evolved from planar "bulk MOSFET" to a variety of structures, such as the thin-film transistor, silicon-on-insulator (SOI) FET, and the trench-gated U-shaped vertical MOSFET (UMOSFET). In these structures, substrate/body contact is generally unavailable; hence, applying CCP to characterize these devices is not possible. However, we have recently modified the CCP technique and developed a three-terminal CP (3T-CP) version, which can be applied to three-terminal FETs [167].

Short channel effects continue to pose significant challenges to CMOS operation, and these effects are further aggravated with scaling [168]. As device dimensions shrink, encroaching source and drain electric field effects on the channel weaken gate control. In an effort to reinforce gate control over the channel, the planar CMOS multiple gate, FinFET, Ω gate and eventually surround gate architecture are being considered [169]. A surround gate FET allows for maximum electrostatic control by the gate over the surface and is expected to provide good short channel effect tolerance. The surround gate-nanowire FET (SG-NWFET) is an important

candidate for non-planar CMOS and is being studied as a viable device design to combat short channel effects. In addition, FETs based on silicon nanowires grown using the vapor-liquid-solid (VLS) technique have been demonstrated for applications such as high performance vertical transistors [170] and chemical and biological sensors [146]. The oxide/nanowire interface plays an important role in determing the performance of these devices and its detailed study is, hence, critical. Charge pumping is indispensable to such a study, and its application to NWFETs can render available valuable information on defect densties and long-term reliability. However, the SG-NWFET also lacks a substrate/body contact and is, therefore, a three-terminal FET that is not amenable to CCP.

We herein apply 3T-CP to silicon SG-NWFETs to measure trap density in the vicinity of the Si/SiO_2 interface. We show that a strong CP output is obtained and can be used to probe interface and near-interface trap densities. This report describes the first application of the CP technique to nanowire transistor structures.

5.2 Experimental procedure

Figure 5.1(a) shows a cross-sectional schematic of the active device region. Axially doped (n^+-p^--n^+) Si NWs are grown using the VLS growth technique as discussed in ref. [157]. The SiNW diameter is $\sim$ 34 nm as determined by field emission scanning electron microscopy (FESEM). The NW structure is thermally oxidized using

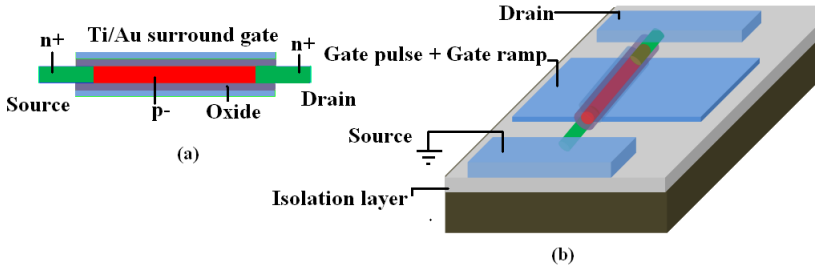

Figure 5.1. a) Cross sectional schematic of the active device segment b) Schematic of the 3T-CP setup.

dry O_2 at 700 ℃ for 4 h to form a uniform 16 nm thick oxide shell. Subsequently, the n^+ ends of the NW are aligned onto Ti/Au contacts using electric-field-assisted assembly. A Ti/Au(20/60 nm) global-back-gate is sputter depsoited onto the back-side of the n^{++} substrate. The source and drain contacts are defined over the n^+ nanowire segment using e-beam lithography. Ti/Au (80/40 nm) was deposited using e-beam evaporation to form the top-gate to complete the non-self-aligned surround-gate structure. The entire active structure rests on a SiN_x isolation layer on a heavily doped silicon substrate. Detailed description of the device fabrication procedure is given elsewhere [157].

For transfer characteristics measurements, current flowing from the drain to source (I_{ds}) is measured while the gate and drain contacts are biased relative to the source contact. Keithley 238 source and measure units (SMU) are used to apply the appropriate bias and measure the resultant current. Voltage pulses required for charge pumping are generated using an Agilent 33250A signal generator.

Fig. 5.1(b) shows the biasing and measurement configuration used for the 3T-CP measurements. Details of the 3T-CP method are given in ref. [167]. Briefly,

however, 3T-CP utilizes a square voltage pulse (V_p) of a given frequency, f, superimposed on a base gate voltage ramped between two values of a gate-to-source voltage V_{gs}. The charge pumping current, I_{CP}, is the drain current measured as a function of V_{gs}. For our SG-NWFETs we used $V_p = 2$ V, f between 0.5 and 400 kHz, and V_{gs} between -1 and 0.25 V.

5.3 Results and discussions

The transfer characteristics of the SG-NWFET were measured at a drain-to-source voltage (V_{ds}) of 100 mV by sweeping the gate-to-source voltage (V_{gs}) from -3 to +3 V. Figure 5.2 shows the measured transfer characteristics on a semi-log scale. The devices exhibit good on-to-off state current ratio ($I_{\text{on}}/I_{\text{off}}$) values exceeding 10^4 at a V_{ds} of 100 mV.

A threshold voltage value of 248 mV is extracted by extrapolating the linear portion of the transfer characteristics, and a linear transconductance (g_m) of 50.1 nS is obtained at the turn-on voltage. The inverse subthreshold slope (S) is 292 mV/decade and is significantly higher than the ideal value of 60 mV/decade. The high value of S is indicative of a high interface trap density at the Si/SiO_2 interface, and it is important to note that no efforts were made to optimize the processing of the SiO_2/Si interface in this device. A large interface trap density at the oxide/silicon interface can give rise to a strong CP signal, and this device is therefore a good candidate for the first application of our 3T-CP method. Post-oxidation

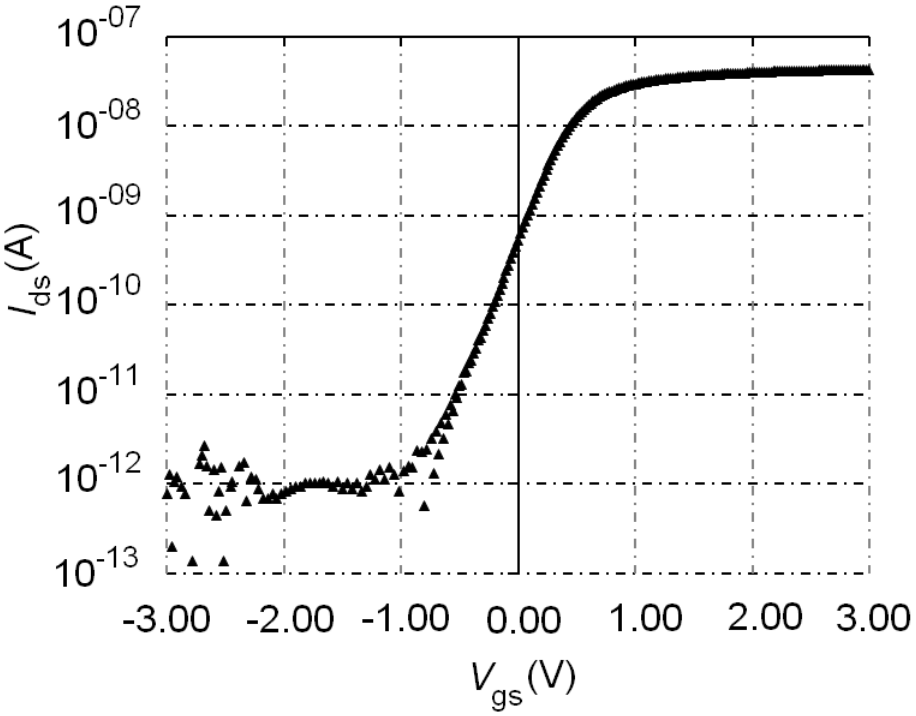

Figure 5.2. Transfer characteristics measured by sweeping V_{gs} from -3 to +3V while holding V_{ds} at 100 mV.

annealing treatments have been shown to greatly improve the interface quality and are planned for future devices [157, 171].

Subthreshold swing can be used to extract the average interface trap density [172] using

$$S = 2.3\frac{kT}{q}\left(1 + \frac{C_{it}}{C_{ox}}\right). \tag{5.1}$$

In Eq. (5.1), C_{it} is the interface trap capacitance and C_{ox} is the oxide capacitance. Using Eq. (5.1), an interface trap density value (D_{it}) of $\sim 6 \times 10^{12}$ cm^{-2} eV^{-1} is estimated from the subthreshold swing value. The interface trap density obtained

from the subthreshold slope measurements is used as a reference to compare the trap density value that will be obtained using 3T-CP method as described next.

In the 3T-CP method as the base gate voltage is swept, the NW surface is pulsed between inversion and accumulation. During inversion, interface traps are populated by electrons coming from the drain and source ends of the device. During accumulation the trapped electrons recombine with incoming holes and the interface traps are, hence, emptied of electrons and are now ready to fill with electrons flowing from the drain/source in the next inversion cycle. The charge pumping current, I_{CP}, is measured at the drain end and is related to the interface trap density [167]. Fig. 5.3 gives I_{CP} for different pulse frequencies. A clear dependence of I_{CP} on f is shown in the figure, and this is expected to be the case for the low frequency charge pumping response. However, at higher frequencies ($f > 50$ kHz), the maximum charge pumping current, I_{CP}^{max}, is found to saturate and does not exhibit a strong frequency dependence. I_{CP}^{max} saturation with frequency is not observed in our previous applications of 3T-CP to MOSFETs [167], although it apparently is the case for SG-NWFETs.

Apart from being a three terminal device, the SG-NWFET has very limited supply of holes because of the minuscule neutral bulk volume. In each charge pumping cycle, a large fraction of the majority carrier holes would be lost due to recombination with the trapped electrons at the SiO_2/Si interface. At lower frequencies, these holes can be replenished by thermal generation in the depletion

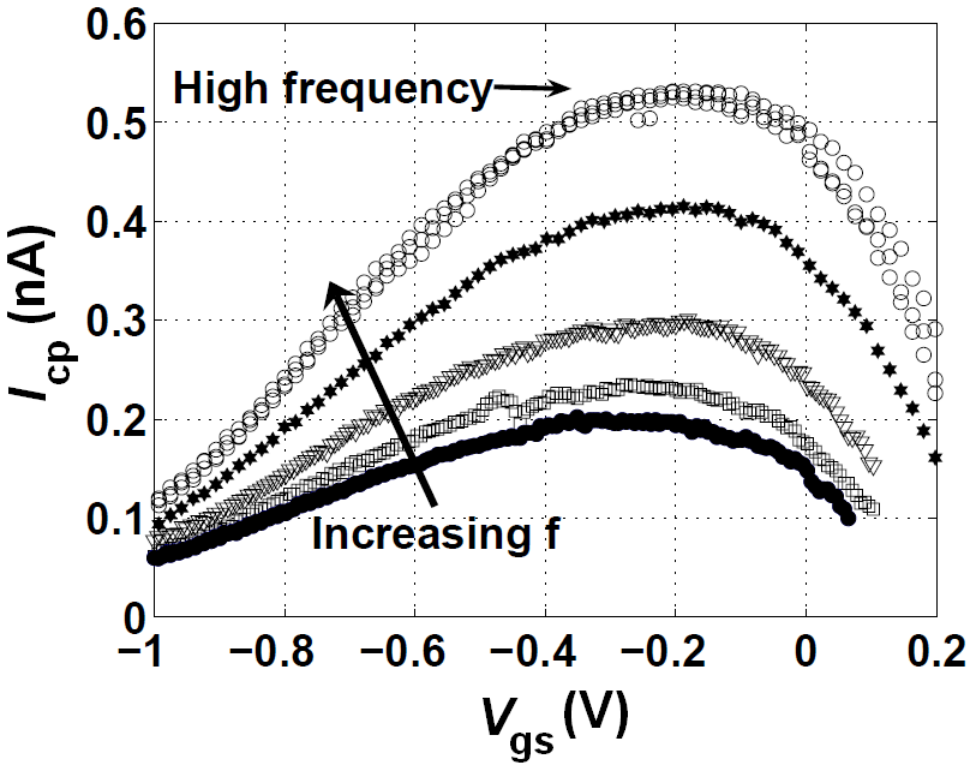

Figure 5.3. 3T-CP signal in a SG-NWFET measured at different pulse frequencies.

region. The thermal generation rate is determined by the temperature dependent time constant for the process. At frequencies far greater than the thermal generation rate, the majority carrier concentration available for recombination is limited by the thermal generation process. Hence, at higher frequencies, the charge pumping current does not increase linearly with frequency and exhibits a saturation behavior. The above mechanism is suggested as a possible explanation for the observed saturation of I_{CP}^{max} with f at high frequency levels.

The frequency dependence of I_{CP}^{max} is generally taken to be of the form [162].

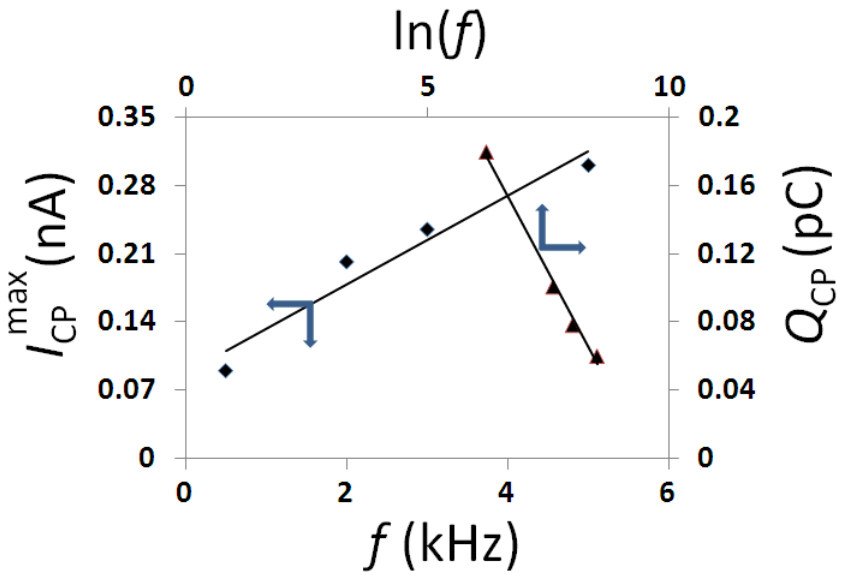

Figure 5.4. I_{CP}^{max} as a function of applied frequency and Q_{CP}^{max} variation with $\ln(f)$ measured in our SG-NWFET.

$$I_{cp}^{max} = qA_g D_{it} \Delta\Psi_s f \tag{5.2}$$

In Equation (5.2), A_g is the gate area, q is the electronic charge, D_{it} is the average interface trap density, and $\Delta\Psi_s$ is the surface potential change when the MOSFET switches from inversion to accumulation. One could use Eq. (5.2) in a linear plot of I_{CP}^{max} versus f and extract D_{it} from the slope of the fitted straight line. Our attempt to do so is shown in Fig. 5.4, and a $D_{it} = 7 \times\ 10^{13}$ cm^{-2} eV^{-1} is obtained in our SG-NWFETs.

D_{it} obtained for the SG-NWFET from 3T-CP is an order of magnitude higher than that estimated from the subthreshold swing. The relatively high D_{it} obtained

from 3T-CP may be attributed to the low frequency of measurement, which enables timely population/depopulation of oxide traps in the neighborhood of the SiO_2/Si interface. At low frequencies, near-interface "slow" oxide traps can also contribute to the total charge pumping current. In the past low frequency CCP has been employed to probe slow oxide traps close to the interface in short channel MOSFETs [173]. In low frequency charge pumping the relationship between I_{CP}^{max} and frequency is no longer linear as suggested by Eq. (5.2). The depth into the oxide measured from the interface over which oxide traps contribute to I_{CP} is dependent on the frequency: this depth is larger the lower the measurement frequency. The total charge pumped $Q_{CP}^{max} = I_{CP}^{max}/f$ at low frequency is related to the frequency as given by

$$\frac{dQ_{cp}}{d\log f} = -qA_g N_{it}(x_m)\lambda_e \Delta\Psi_s. \tag{5.3}$$

In Eq. (5.3), N_{it} is the trap concentration per unit volume of the SiO_2/Si interface and near interface SiO_2 bulk at a maximum tunneling distance (x_m). λ_e is the inverse attenuation factor for electrons in SiO_2 and can be estimated using

$$\lambda_e = \frac{\hbar}{\sqrt{8m_e^*\Phi_e}}. \tag{5.4}$$

In Eq. (5.4), $\hbar$ is the reduced Planck's constant, m_e^* is the effective tunneling mass, and Φ_e is the injection barrier for electrons from silicon into SiO_2 and equals 3.1

eV. The maximum tunneling distance at any given frequency can be estimated using

$$x_m \approx \frac{1}{2k_0} \ln\left(\frac{1}{2f}\sigma_n \bar{v} n\right). \tag{5.5}$$

In Equation (5.5), k_0 is the decay constant and for a barrier of 3.1 eV the value of $1/2k_0$ is approximately 0.7 Å [174], σ_n is the electron capture cross section, $\bar{v}$ is the average thermal velocity and n is the carrier concentration [174, 175]. Using a free carrier concentration value of 1×10^{16} cm^{-3} and assuming a uniform capture cross-section value of 1×10^{-14} cm^2, the maximum tunneling distance for a pulse frequency of 1kHz is estimated to be about 0.76 nm.

The total charge pumped in our SG-NWFETs as a function of the pulse frequency, f, on a semi-log scale is shown in Fig. 5.4. Applying Equations (5.3) and (5.4) to the Q_{CP}^{max} versus $\ln f$ plot of Fig. 5.4, one gets $N_{it} \approx 6.9 \times 10^{19}$ cm^{-3} eV^{-1}. Using the estimated tunneling distance of 0.76 nm, an average interface trap density of $D_{it} \approx 1.2 \times 10^{13}$ cm^{-2} eV^{-1} is obtained. This value of D_{it} correlates very well with that obtained from the subthreshold swing measurements. The high D_{it} obtained in the SG-NWFETs may arise in part from the cylindrical oxide growth inherent to the geometry of the device [156]. As mentioned earlier, the high interface trap density in these devices may also be reduced using optimized post-oxidation annealing treatments [157, 171]. No such treatments were used for our devices since high interface trap density is desirable to detect the CP signal.

5.4 Conclusion

We have applied a modified three-terminal CP technique that we recently developed [167] to the study of the SiO_2/Si interface and neighboring oxide traps in a SG-NWFET structure. Frequency saturation of the CP signal is observed to occur in the SG-NWFET at higher measurement frequencies. At low measurement frequencies, however, near-interface slow oxide traps are observed to contribute to the measured 3T-CP signal. Analysis of our 3T-CP measurements have revealed a trap density of $\sim 1.2 \times 10^{13}$ cm^{-2} eV^{-1} in the SG-NWFET, which is in agreement with trap density estimates made from subthreshold swing measurements [157]. This is the first time that CP has been applied to NWFETs, and this study demonstrates the applicability of the technique to three terminal SG-NWFETs.

Chapter 6

Conclusions and Future Work

6.1 Contacts to WBG Semiconductors

The first part of this thesis focuses on electrical characterization of Schottky contacts to WBG semiconductors. These semiconductors tend to contain more defects than silicon or even some of the mature III-V systems. Schottky contacts to WBG semiconductors, therefore, are far from ideal and show deviant behavior in their electrical characteristics. Also, the wide bandgap nature of these materials results in larger barrier heights compared to Si. Due to the larger barrier heights obtainable, minority carrier injection is more of a concern in these diodes. Space charge limited current-like behavior has been observed in Re/4H-SiC Schottky diodes. Using a combination of I-V, C-V and DLTS methods, the observed SCLC characteristics have been attributed to minority carrier injection as opposed to trap limited SCLC (reported in the literature).

Apart from minority carrier injection, the I-V characteristics can be heavily influenced by the presence of barrier height inhomogeneities. An important goal of electrical characterization is the determination of the homogeneous barrier height. The homogeneous Schottky barrier height is a fundamental parameter that characterizes the metal/semiconductor system. An increasing amount of literature relies on analytical approaches based on the inhomogeneous Schottky barrier model to account for the observed deviations. In order to account for the effects of BHI on the extracted effective Schottky barrier height, an n-Φ_{B} plot is typically employed. The n-Φ_{B} plot provides a simple way to filter the effects of BHI. In order to use the I-V characteristics to determine the Schottky barrier height, knowledge of the Richardson constant is essential. However, an accurate approach to extract the Richardson constant in the presence of BHIs is still lacking. A key goal of this thesis has been to account for limitations of existing approaches to extract the Richardson constant. In light of these limitations, the need for a new method has been recognized. Based on the BHI framework provided by Tung, a linear correlation between the extracted barrier height and $\ln(A^*)$ has been proposed. This linear correlation coupled with the widely used n-Φ_B plot has been used to extract the actual Richardson constant.

The linear correlation is one of the key contributions of the current work. This method has been applied to the determination of the Richardson constant of emerging WBG semiconductors such as ZnO and GaN. The application of the method

to ZnO is of particular importance since the Richardson constant is not well established. An A^* value of 27 A cm^{-2} K^{-2} has been estimated using the proposed approach. This value is by far the closest reported to the theoretical value of ZnO of 32 A cm^{-2} K^{-2}. This method has also been applied to the determination of Richardson constant of GaN, and close agreement with the theoretically expected value has also been obtained.

6.2 Contacts to Nanowires

The second part of the thesis is focused on the Schottky contacts to nanowires. Electrical characteristics of a Schottky contact to a nanowire differ markedly from those of a bulk Schottky contact. The I-V characteristics of a Schottky contact to a nanowire are influenced heavily by the adjacent nanowire surface. Depending on the surface charge magnitude and sign, the current conduction can vary. In order to systematically investigate the effects of surface condition on the I-V characteristics of an axial metal/nanowire contact, a surround gate architecture has been used. TCAD simulations have been used to gain insights into the effect of a surround-gate bias on the metal/semiconductor nanowire I-V characteristics. Based on these simulation studies, a method has been proposed to extract the true Schottky barrier height from the I-V characteristics.

Under the influence of surface charge, the depletion region width can vary radially and axially as well. The effective area for conduction is reduced in surface

depletion conditions, and under surface accumulation conditions, spatially non-uniform tunneling current localized along the nanowire periphery can contribute to the total current. The ideality factor and effective barrier height have been found to be surround-gate bias dependent. A linear correlation has been found between the ideality factor and effective barrier height obtained as a function of gate bias. The linear relation has been found to be valid in the case of surface accumulation conditions, and this straight line when extrapolated to $n = 1$ yields the homogeneous barrier height. The gate voltage required for the onset of surface accumulation can be determined by an n-V_{gs} plot. Using a combination of the n-Φ_{B} and the n-V_{gs} plots, the true Schottky barrier height can be determined. RT I-V measured on θ-Ni_2Si/n-Si NW Schottky contacts have also been analyzed and a linear correlation between n and Φ_{B} has been observed. The proposed method presents a simple way to analyze and interpret experimental I-V characteristics of Schottky contacts to nanowires.

Given the significant role played by the oxide/nanowire interface on conduction in the nanowire, it is important to control the interface quality. A modified version of the conventional charge pumping method known as the 3 terminal charge pumping method has also been applied to nanowire field effect transistors for the first time. 3T-CP method has been used to characterize the oxide/nanowire interface, and an interface trap density of 10^{12} cm^{-2} eV^{-1} has been determined. The charge pumping method can provide inputs such as interface trap density to the

TCAD simulation set up. Simulation and experimental methods presented in this work can together serve as a characterization toolset that can be used to further investigate contact and dielectric interfaces in semiconductor nanowire devices.

6.3 Future Work

The main focus of this thesis has been the development of analytical approaches that would allow determination of the true Schottky contact parameters. The inhomogeneous Schottky barrier model is gaining prominence, and analytical approaches based on the BHI framework are still not thoroughly investigated. For example, a strong and meaningful correlation between extracted BHI parameters and experimental data are still missing. Given the complexity of real MS contacts, a detailed study involving TCAD simulations and analytical approaches can provide more insight into the significance of the extracted patch parameters. Correlation with samples that have been fabricated with the intentional incorporation of barrier height inhomogeneities would be the next step.

At the nanoscale, the Schottky contact has evolved from a simple planar structure to a more complex creature with the effects of size and geometry becoming significant. The methods provided in this thesis are a first step in exploring different trends and unique features exhibited at the nanoscale. Size dependence of the Schottky barrier and its effect on Fermi-level pinning are just a few directions for continuing further investigations.

Appendix A

Non-technical abstract

Metal contacts to semiconductors are ubiquitous in diverse electronic applications such as power diodes, light emitting diodes (LEDs) and gas sensors. For these applications, novel semiconductors such as silicon carbide, zinc oxide and gallium nitride have excellent potential and have gained a great deal of attention. Schottky contacts to these semiconductors can provide valuable inputs that can aid in improving material quality and thereby obtaining superior performance. This is often accomplished by interpretation of electrical characteristics such as current-voltage measurements. Extraction of Schottky barrier parameters is hampered due to the presence of material defects at the metal/semiconductor interface. For a large part, the first of this thesis relies on the pioneering work done by Dr. Raymond Tung (then at AT & T Bell Labs) known as the inhomogeneous Schottky barrier model. This model has been largely successful in explaining the different trends exhibited by the current-voltage characteristics of real Schottky diodes. Parameter extrac-

tion based on the inhomogeneous Schottky barrier model is one of the key goals of this thesis. So far, methods presented in the literature have been found to be incomplete in the incorporation of the inhomogeneous Schottky barrier concepts. In this thesis, existing approaches to analyze current-voltage measurements are extended to provide a more thorough analysis. The analysis methodology presented here provides a means to accurately extract Schottky barrier parameters.

On the other hand, contacts at extremely small dimensions (nanoscale) are being studied due to their relevance in nanoelectronics. Nanocontacts are important from both technological and fundamental perspectives. The behavior of these contacts is much different from that of macroscale contacts and hence electrical characterization of these contacts needs to be considered differently. In this thesis, a method to analyze the current-voltage measurements of nanocontacts has been proposed based on simulations. Contact size and geometry effects are important in these nanocontacts. A simulation based approach allows a systematic exploration of these effects on the conduction properties of nanocontacts to nanowires. Due to substantially larger surface area/volume ratio in nanocontacts, the impact of surface on the conduction properties of nanocontacts to nanowires is also quite important. In the second part of this thesis, a method to address the effects of surface and geometry on the extracted parameters from current-voltage measurements is presented. The proposed approach would serve as a useful method to investigate Schottky barrier properties at the nanoscale.

Bibliography

[1] Duke, C. B. (1996) "Semiconductor Surface Reconstruction: The Structural Chemistry of Two-Dimensional Surface Compounds," *Chemical Reviews*, **96**(4), pp. 1237–1260.

[2] Moormann, H., D. Kohl, and G. Heiland (1979) "Work function and band bending on clean cleaved zinc oxide surfaces," *Surface Science*, **80**, pp. 261–264.

[3] Heine, V. (1965) "Theory of Surface States," *Physical Review*, **138**(6A), p. A1689.

[4] Spicer, W., T. Kendelewicz, N. Newman, K. Chin, and I. Lindau (1986) "The mechanisms of Schottky barrier pinning in III-V semiconductors: Criteria developed from microscopic (atomic level) and macroscopic experiments," *Surface Science*, **168**(1-3), pp. 240–259.

[5] Hasegawa, H. and H. Ohno (1986) "Unified disorder induced gap state model for insulator–semiconductor and metal–semiconductor interfaces," *Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures*, **4**(4), pp. 1130–1138.

[6] Cowley, A. M. and S. M. Sze (1965) "Surface States and Barrier Height of Metal-Semiconductor Systems," *Journal of Applied Physics*, **36**(10), pp. 3212–3220.

[7] Bardeen, J. (1947) "Surface States and Rectification at a Metal Semi-Conductor Contact," *Physical Review*, **71**(10), p. 717.

[8] Tung, R. T. (2001) "Formation of an electric dipole at metal-semiconductor interfaces," *Physical Review B*, **64**(20), p. 205310.

[9] Brillson, L. J. (2007) "Interface bonding, chemical reactions, and defect formation at metal-semiconductor interfaces," in *J. Vac. Sci. Technol. A*, vol. 25, AVS, p. 943949.

[10] Ohdomari, I. and H. Aochi (1987) "Size effect of parallel silicide contact," *Phys. Rev. B*, **35**, p. 682686.

[11] Padovani, F. A. and G. G. Sumner (1965) "Experimental Study of Gold-Gallium Arsenide Schottky Barriers," *Journal of Applied Physics*, **36**(12), pp. 3744–3747.

[12] Saxena, A. (1969) "Forward current-voltage characteristics of Schottky barriers on n-type silicon," *Surface Science*, **13**(1), pp. 151–171.

[13] H.Zhang, E.J.Miller, and E.T.Yu (2006) "Analysis of leakage current mechanisms in Schottky contacts to GaN and Al$_0.25$Ga$_0.75$N/GaN grown by molecular-beam Epitaxy," *Journal of Applied Physics*, **99**, pp. 264–283.

[14] Chand, S. and J. Kumar (1996) "On the existence of a distribution of barrier heights in Pd$_2$Si/Si Schottky diodes," *Journal of Applied Physics*, **80**, pp. 288–294.

[15] Dogan, H., H. Korkut, N. Yildirim, and A. Turut (2007) "Prediction of lateral barrier height in identically prepared Ni/n-type GaAs Schottky barrier diodes," *Applied Surface Science*, **253**, pp. 7467–7470.

[16] Werner, J. H. and H. H. Gttler (1991) "Barrier inhomogeneities at Schottky contacts," *Journal of Applied Physics*, **69**, pp. 1522–1533.

[17] Tung, R. T. (1992) "Electron transport at metal-semiconductor interfaces: General theory," *Phys. Rev. B*, **45**, p. 1350913523.

[18] Ohdomari, I. and K. N. Tu (1980) "Parallel silicide contacts," *Journal of Applied Physics*, **51**, pp. 3735–3739.

[19] Defives, D., O. Noblanc, C. Dua, C. Brylinski, M. Barthula, V. Aubry-Fortuna, and F. Meyer (1999) "Barrier inhomogeneities and electrical characteristics of Ti/4H-SiC Schottky rectifiers," *Electron Devices, IEEE Transactions on*, **46**(3), pp. 449–455.

[20] McCafferty, P. G., A. Sellai, P. Dawson, and H. Elabd (1996) "Barrier characteristics of PtSi/p-Si Schottky diodes as determined from I-V-T measurements," *Solid-State Electronics*, **39**(4), pp. 583–592.

[21] Zhu, S., R. L. V. Meirhaeghe, C. Detavernier, F. Cardon, G. Ru, X. Qu, and B. Li (2000) "Barrier height inhomogeneities of epitaxial CoSi2 Schottky contacts on n-Si (100) and (111)," *Solid-State Electronics*, **44**(4), pp. 663–671.

[22] Calcagno, L., A. Ruggiero, F. Roccaforte, and F. L. Via (2005) "Effects of annealing temperature on the degree of inhomogeneity of nickel-silicide/SiC Schottky barrier," *Journal of Applied Physics*, **98**.

[23] Tanabe, A., K. Konuma, N. Teranishi, S. Tohyama, and K. Masubuchi (1991) "Influence of Fermi-level pinning on barrier height inhomogeneity in PtSi/p-Si Schottky contacts," *Journal of Applied Physics*, **69**, pp. 850–853.

[24] Ouisse, T., E. Platel, T. Billon, and H. Lahreche (1997) "Observation of random telegraph signal in SiC Schottky diodes," *Electronics Letters*, **33**(22), pp. 1907–1909.

[25] Tumakha, S., D. J. Ewing, L. M. Porter, Q. Wahab, X. Ma, T. S. Sudharshan, and L. J. Brillson (2005) "Defect-driven inhomogeneities in Ni/4HSiC Schottky barriers," *Applied Physics Letters*, **87**.

[26] Ewing, D. J., L. M. Porter, Q. Wahab, X. Ma, T. S. Sudharshan, S. Tumakha, M. Gao, and L. J. Brillson (2007) "Inhomogeneities in Ni/4H-SiC Schottky barriers: Localized Fermi-level pinning by defect states," *Journal of Applied Physics*, **101**.

[27] Hsu, J. W. P., M. J. Manfra, D. V. Lang, S. Richter, S. N. G. Chu, A. M. Sergent, R. N. Kleiman, L. N. Pfeiffer, and R. J. Molnar (2001) "Inhomogeneous spatial distribution of reverse bias leakage in GaN Schottky diodes," *Applied Physics Letters*, **78**(12), pp. 1685–1687.

[28] Im, H. J., Y. Ding, J. P. Pelz, and W. J. Choyke (2001) "Nanometer-scale test of the Tung model of Schottky-barrier height inhomogeneity," *Phys. Rev. B*, **64**, pp. 5771–5775.

[29] Skromme, B. J., E. Luckowski, K. Moore, M. Bhatnagar, C. E. Weitzel, T. Gehoski, and D. Ganser (2000) "Electrical characteristics of Schottky barriers on 4H-SiC: the effects of barrier height nonuniformity," *Journal of Electronic Materials*, **29**, pp. 376–383.

[30] Tung, R. T. (1984) "Schottky-barrier formation at single-crystal metal-semiconductor interfaces," *Physical Review Letters*, **52**, pp. 461–464.

[31] Miura, Y., K. Hirose, K. Aizawa, N. Ikarashi, and H. Okabayashi (1992) "Schottky barrier inhomogeneity caused by grain boundaries in epitaxial Al film formed on Si(111)," *Applied Physics Letters*, **61**, pp. 1057–1059.

[32] Talin, A. A., R. S. Williams, B. A. Morgan, K. M. Ring, and K. L. Kavanagh (1994) "Nanometer-resolved spatial variations in the Schottky barrier height of a Au/n-type GaAs diode," *Phys. Rev. B*, **49**, p. 1647416479.

[33] Yi, W., I. I. Kaya, I. B. Altfeder, I. Appelbaum, D. M. Chen, and V. Narayanamurti (2005) "Dual-probe scanning tunneling microscope for study of nanoscale metal-semiconductor interfaces," *Review of Scientific Instruments*, **76**(6), 063711.

[34] Brazel, E. G., M. A. Chin, and V. Narayanamurti (1999) "Direct observation of localized high current densities in GaN films," *Applied Physics Letters*, **74**, pp. 2367–2369.

[35] Iucolano, F., F. Roccaforte, F. Giannazzo, and V. Raineri (2007) "Barrier inhomogeneity and electrical properties of Pt/GaN Schottky contacts," *Journal of Applied Physics*, **102**, pp. 2367–2369.

[36] Spradlin, J., S. Dogan, J. Xie, R. Molnar, A. A. Baski, and H. Morko (2004) "Investigation of forward and reverse current conduction in GaN films by conductive atomic force microscopy," *Applied Physics Letters*, **84**, pp. 4150–4152.

[37] Sarpatwari, K., L. Passmore, S. Suliman, and O. Awadelkarim (2007) "Analysis of current-voltage-temperature characteristics in SiC Schottky diodes using threshold-accepting simulated-annealing techniques," *Solid-State Electronics*, **51**(5), p. 644649.

[38] Bhatnagar, M. and B. Baliga (1993) "Comparison of 6H-SiC, 3C-SiC, and Si for power devices," *Electron Devices, IEEE Transactions on*, **40**(3), pp. 645–655.

[39] Casady, J. B. and R. W. Johnson (1996) "Status of silicon carbide (SiC) as a wide-bandgap semiconductor for high-temperature applications: A review," *Solid-State Electronics*, **39**(10), pp. 1409 – 1422.

[40] Johnson, E. (1965) "Physical limitations on frequency and power parameters of transistorss," *IRE International Convention Record*, **13**, pp. 27–34.

[41] Keyes, R. W. (1972) "Figure of merit for semiconductors for high-speed switches," *Proceedings of the IEEE*, **60**.

[42] Chow, T. P. and R. Tyagi (1994) "Wide bandgap compound semiconductors for superior high-voltage unipolar power devices," *Electron Devices, IEEE Transactions on*, **41**, pp. 1481–1483.

[43] Yoder, M. N. (1996) "Wide bandgap semiconductor materials and devices," *Electron Devices, IEEE Transactions on*, **43**, p. 16331636.

[44] Haberstroh, C., R. Helbig, and R. A. Stein (1994) "Some new features of the photoluminescence of SiC(6H), SiC(4H), and SiC(15R)," *Journal of Applied Physics*, **76**(1), pp. 509–513.

[45] Ozgur, U., Y. I. Alivov, C. Liu, A. Teke, M. A. Reshchikov, S. Dogan, V. Avrutin, S. Cho, and H. Morkoc (2005) "A comprehensive review of ZnO materials and devices," *Journal of Applied Physics*, **98**(4), pp. 041301–103.

[46] Morkoc, H., S. Strite, G. B. Gao, M. E. Lin, B. Sverdlov, and M. Burns (1994) "Large-band-gap SiC, III-V nitride, and II-VI ZnSe-based semiconductor device technologies," *Journal of Applied Physics*, **76**(3), pp. 1363–1398.

[47] v. Muench, W. and I. Pfaffeneder (1977) "Breakdown field in vapor-grown silicon carbide p-n junctions," *Journal of Applied Physics*, **48**(11), pp. 4831–4833.

[48] Nause, J. and B. Nemeth (2005) "Pressurized melt growth of ZnO boules," *Semiconductor Science Technology*, **20**, pp. 45–48.

[49] Dmitriev, V. A., K. G. Irvine, J. Carter, N. I. Kuznetsov, and E. V. Kalinina (1996) "Electric breakdown in GaN p-n junctions," *Applied Physics Letters*, **68**(2), pp. 229–231.

[50] Slack, G. A. (1964) "Thermal Conductivity of Pure and Impure Silicon, Silicon Carbide, and Diamond," *Journal of Applied Physics*, **35**(12), pp. 3460–3466.

[51] R.Powell, A. and L. B.Rowland (2002) "SiC Materials - Progress, Status, and Potential Roadblocks," *Proceedings of the IEEE*, **90**.

[52] Y.M.Tairov and V.F.Tsvetkov (1978) "Investigations and growth processes of ingots of silicon carbide single crystals," *J.Cryst.Growth*, **43**, pp. 209–212.

[53] Tairov, Y. and V.F.Tsvetkov (1981) "General Principles of Growing Large-Size single crystals," *J.Cryst.Growth*, **52**.

[54] Pensl, G. and W. Choyke (1993) "Electrical and Optical Characterization of SiC," *Physica B*, **185**, pp. 264–283.

[55] Liu, J. L., J. Q. Gao, J. K. Cheng, J. F. Yang, and G. J. Qiao (2007) "Methods for the reduction of the micropipe density in SiC single crystals," *Journal of Materials Science*, **42**, pp. 6148–6152.

[56] Rendakova, S. V., I. P. Nikitina, A. S. Tregubova, and V. A. Dmitriev (1998) "Micropipe and dislocation density reduction in 6H-SiC and 4H-SiC structures grown by liquid phase epitaxy," *Journal of Electronic Materials*, **27**, pp. 292–295.

[57] Nakamura, D., I. Gunjishima, S. Yamaguchi, T. Ito, A. Okamoto, H. Kondo, S. Onda, and K. Takatori (2004) "Ultrahigh–quality silicon carbide single crystals," *Nature*, **430**, pp. 1009–1012.

[58] Amano, H., N. Sawaki, I. Akasaki, and Y. Toyoda (1986) "Metalorganic vapor phase epitaxial growth of a high quality GaN film using an AlN buffer layer," *Applied Physics Letters*, **48**, pp. 353–355.

[59] Fini, P., L. Zhao, B. Moran, M. Hansen, H. Marchand, J. P. Ibbetson, S. P. DenBaars, U. K. Mishra, and J. S. Speck (1999) "High-quality coalescence of laterally overgrown GaN stripes on GaN/sapphire seed layers," *Applied Physics Letters*, **75**, pp. 1706–1708.

[60] H.Zhang, E.J.Miller, and E.T.Yu (2006) "Analysis of leakage current mechanisms in Schottky contacts to GaN and $Al_{0.25}Ga_{0.75}N$/GaN grown by molecular-beam Epitaxy," *Journal of Applied Physics*, **99**, pp. 264–283.

[61] Inoue, S., K. Okamoto, N. Matsuki, T.-W. Kim, and H. Fujioka (2006) "Epitaxial growth of GaN on copper substrates," *Applied Physics Letters*, **88**, pp. 1009–1012.

[62] Takahashi, K., K. Yasui, M. Suemitsu, A. Kato, Y. Kuroki, M. Takata, and T. Akahane (2006) "Epitaxial growth of Hexagonal GaN films on SiC/Si Substrates by Hot-Mesh CVD Method," *Advanced Materials Research*, **11-12**, pp. 261–264.

[63] Miller, E. J., E. T. Yu, P. Waltereit, and J. S. Speck (2004) "Analysis of reverse-bias leakage current mechanisms in GaN grown by molecular-beam epitaxy," *Applied Physics Letters*, **84**, pp. 535–537.

[64] McCarthy, L., I. Smorchkova, H. Xing, P. Fini, S. Keller, J. Speck, S. P. DenBaars, M. J. W. Rodwell, and U. K. Mishra (2001) "Effect of threading dislocations on AlGaN/GaN heterojunction bipolar transistors," *Applied Physics Letters*, **78**, pp. 2235–2237.

[65] Look, D. C. "Recent advances in ZnO materials and devices," **80**.

[66] Croxall, D. F., R. C. C. Ward, C. A. Wallace, and R. C. Kell (1974) "Hydrothermal growth and investigation of Li-doped zinc oxide crystals of high purity and perfection," *Journal of Crystal Growth*, **22**(2), pp. 117–124.

[67] Reynolds, D. C., C. W. Litton, D. C. Look, J. E. Hoelscher, B. Claflin, T. C. Collins, J. Nause, and B. Nemeth (2004) "High-quality, melt-grown ZnO single crystals," *Journal of Applied Physics*, **95**(9), pp. 4802–4805.

[68] Kasuga, M. and S. Ogawa (1983) "Electronic Properties of Vapor-Grown Heteroepitaxial ZnO Film on Sapphire," *Japanese Journal of Applied Physics*, **22**, pp. 794–798.

[69] Chen, Y., D. M. Bagnall, H. jun Koh, K. tae Park, K. Hiraga, Z. Zhu, and T. Yao (1998) "Plasma assisted molecular beam epitaxy of ZnO on c -plane sapphire: Growth and characterization," *Journal of Applied Physics*, **84**(7), pp. 3912–3918.

[70] Vispute, R. D., V. Talyansky, Z. Trajanovic, S. Choopun, M. Downes, R. P. Sharma, T. Venkatesan, M. C. Woods, R. T. Lareau, K. A. Jones, and A. A. Iliadis (1997) "High quality crystalline ZnO buffer layers on sapphire (001) by pulsed laser deposition for III–V nitrides," *Applied Physics Letters*, **70**(20), pp. 2735–2737.

[71] Mosbacker, H. L., Y. M. Strzhemechny, B. D. White, P. E. Smith, D. C. Look, D. C. Reynolds, C. W. Litton, and L. J. Brillson (2005) "Role of near-surface states in ohmic-Schottky conversion of Au contacts to ZnO," *Applied Physics Letters*, **87**(1), p. 0121023.

[72] Nakamura, S., T. Mukai, M. Senoh, and N. Iwasa (1992) "Thermal Annealing Effects on P-Type Mg-Doped GaN Films," *Japanese Journal of Applied Physics*, **31**, pp. 139–142.

[73] Sheu, J. K. and G. C. Chi (2002) "The doping process and dopant characteristics of GaN," *Journal of Physics: Condensed Matter*, **14**, pp. 2501–2505.

[74] Powell, J. A. and D. J. Larkin (1997) "Process-Induced Morphological Defects in Epitaxial CVD Silicon Carbide," *Physica Status Solidi B Basic Research*, **202**, pp. 529–548.

[75] Tajima, Y., K. Kijima, and W. D. Kingery (1982) "Diffusion of ion implanted aluminum in silicon carbide," *The Journal of Chemical Physics*, **77**, pp. 2592–2598.

[76] Davis, R. F., G. Kelner, M. Shur, J. W. Palmour, and J. A. Edmond (1991) "Thin Film Deposition and Microelectronic and Optoelectronic Device Fabrication and Characterization in Monocrystalline Alpha and Beta Silicon Carbide," *Proceedings of the IEEE*, **79**, pp. 677–701.

[77] Persson, P. O. A. ., L. Hultman, M. S. Janson, A. Hallén, R. Yakimova, D. Panknin, and W. Skorupa (2002) "On the nature of ion implantation induced dislocation loops in 4H-silicon carbide," *Journal of Applied Physics*, **92**, pp. 2501–2505.

[78] Pearton, S. J., C. B. Vartuli, J. C. Zolper, C. Yuan, and R. A. Stall (1995) "Ion implantation doping and isolation of GaN," *Applied Physics Letters*, **67**, pp. 1435–1437.

[79] Wendler, E., A. Heft, and W. Wesch (1998) "Ion-beam induced damage and annealing behaviour in SiC," *Nuclear Instruments and Methods in Physics Research Section B: Beam Interactions with Materials and Atoms*, **141**, pp. 105–117.

[80] Anwanda, W., G. Brauera, P. G. Colemanb, M. Voelskowa, and W. Skorupaa (1999) "Characterisation of defects in ion implanted SiC by slow positron implantation spectroscopy and Rutherford backscattering," *Applied Surface Science*, **149**, pp. 148–150.

[81] J., Z., E. N. W., C. Y., Y. B. V., and L. Y. (2004) "Wet-Chemical Etching of (1120) ZnO Films," *Journal of Electronic Materials*, **33**(6), pp. 556–559.

[82] Itoh, A. and H. Matsunami (1997) "Analysis of Schottky Barrier Heights of Metal/SiC Contacts and Its Possible Application to High-Voltage Rectifying Devices," *physica status solidi (a)*, **162**(1), p. 389408.

[83] Porter, L. M. and R. F. Davis (1995) "A critical review of ohmic and rectifying contacts for silicon carbide," *Materials Science and Engineering B*, **34**(2-3), p. 83105.

[84] Han, S. Y. and J. Lee (2004) "Interpretation of Fermi level pinning on 4H-SiC using synchrotron photoemission spectroscopy," *Applied Physics Letters*, **84**(4), p. 538540.

[85] Foresi, J. S. and T. D. Moustakas (1993) "Metal contacts to gallium nitride," *Applied Physics Letters*, **62**(22), p. 28592861.

[86] Binari, S., H. Dietrich, G. Kelner, L. Rowland, K. Doverspike, and D. Gaskill (1994) "Electrical characterisation of Ti Schottky barriers can n-type GaN," *Electronics Letters*, **30**(11), p. 909911.

[87] Kurtin, S., T. C. McGill, and C. A. Mead (1969) "Fundamental Transition in the Electronic Nature of Solids," *Physical Review Letters*, **22**(26), p. 1433.

[88] Lee, S., C. Zetterling, and M. stling (2001) "Schottky barrier height dependence on the metal work function for p-type 4H-silicon carbide," *Journal of Electronic Materials*, **30**(3), pp. 242–246.

[89] Ding, Y., K. Park, J. P. Pelz, K. C. Palle, M. K. Mikhov, B. J. Skromme, H. Meidia, and S. Mahajan (2004) "Cubic inclusions in 4H-SiC studied with ballistic electron-emission microscopy," *Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films*, **22**(4), p. 13511355.

[90] Schmitz, A., A. Ping, M. Khan, Q. Chen, J. Yang, and I. Adesida (1998) "Metal contacts to n-type GaN," *Journal of Electronic Materials*, **27**(4), pp. 255–260.

[91] Ivanova, L., S. Borisova, H. Eisele, M. Dahne, A. Laubsch, and P. Ebert (2008) "Surface states and origin of the Fermi level pinning on nonpolar GaN(1[overline 1]00) surfaces," *Applied Physics Letters*, **93**(19), p. 1921103.

[92] Allen, M. W. and S. M. Durbin (2008) "Influence of oxygen vacancies on Schottky contacts to ZnO," *Applied Physics Letters*, **92**(12), pp. 122110–3.

[93] Kim, S.-D., C.-M. Park, and J. Woo (2002) "Advanced model and analysis of series resistance for CMOS scaling into nanometer regime. II. Quantitative analysis," *Electron Devices, IEEE Transactions on*, **49**(3), pp. 467–472.

[94] Chieh, Y.-S., A. Perera, and J. Krusius (1992) "Series resistance of silicided ohmic contacts for nanoelectronics," *Electron Devices, IEEE Transactions on*, **39**(8), pp. 1882–1888.

[95] Ruffino, F., M. G. Grimaldi, F. Giannazzo, F. Roccaforte, and V. Raineri (2006) "Size-dependent Schottky Barrier Height in self-assembled gold nanoparticles," *Applied Physics Letters*, **89**(24), 243113.

[96] Lee, T., J. Liu, N. Chen, R. Andres, D. Janes, and R. Reifenberger (2000) "Electronic Properties of Metallic Nanoclusters on Semiconductor Surfaces: Implications for Nanoelectronic Device Applications," *Journal of Nanoparticle Research*, **2**(4), pp. 345–362.

[97] Chen, Z., J. Appenzeller, J. Knoch, Y. ming Lin, and P. Avouris (2005) "The Role of Metal-Nanotube Contact in the Performance of Carbon Nanotube Field-Effect Transistors," *Nano Letters*, **5**(7), pp. 1497–1502.

[98] Heo, Y. W., L. C. Tien, D. P. Norton, S. J. Pearton, B. S. Kang, F. Ren, and J. R. LaRoche (2004) "Pt/ZnO nanowire Schottky diodes," *Applied Physics Letters*, **85**(15), pp. 3107–3109.

[99] Weber, W. M., L. Geelhaar, A. P. Graham, E. Unger, G. S. Duesberg, M. Liebau, W. Pamler, C. Cheze, H. Riechert, P. Lugli, and F. Kreupl (2006) "Silicon-Nanowire Transistors with Intruded Nickel-Silicide Contacts," *Nano Letters*, **6**(12), pp. 2660–2666.

[100] Lonard, F. and J. Tersoff (2000) "Role of Fermi-Level Pinning in Nanotube Schottky Diodes," *Physical Review Letters*, **84**(20), p. 4693.

[101] Hasegawa, H., T. Sato, and C. Kaneshiro (1999) "Properties of nanometer-sized metalsemiconductor interfaces of GaAs and InP formed by an in situ electrochemical process," in *Papers from the 26th conference on the physics and chemistry of semiconductor interfaces*, vol. 17, AVS, pp. 1856–1866.

[102] Leonard, F. and A. A. Talin (2006) "Size-Dependent Effects on Electrical Contacts to Nanotubes and Nanowires," *Physical Review Letters*, **97**(2), pp. 026804–4.

[103] Scharfetter, D. (1965) "Minority carrier injection and charge storage in epitaxial Schottky barrier diodes," *Solid-State Electronics*, **8**(3), pp. 299–311.

[104] Yu, A. Y. C. and E. H. Snow (1969) "Minority carrier injection of metal-silicon contacts," *Solid-State Electronics*, **12**(3), pp. 155–160.

[105] Zhang, J. and W. R. Harrell (2003) "Analysis of the IV Characteristics of Al/4HSiC Schottky diodes," *JVSTB*, **21**.

[106] F.Yakuphanoglu, N. Tugluoglu, and S. Karadeniz (2007) "Space charge limited conduction in Ag/p-Si Schottky diode," *Physica B.*, **392**, pp. 188–191.

[107] Kern, W. and D. A. Puotinen (1970) "Cleaning solutions based on hydrogen peroxide for use in silicon semiconductor technology," *RCA Rev.*, **31**, p. 187206.

[108] Kern, W. (1990) "The Evolution of Silicon Wafer Cleaning Technology," *Journal of The Electrochemical Society*, **137**(6), pp. 1887–1892.

[109] Lang, D. V. (1974) "Deep-level transient spectroscopy: A new method to characterize traps in semiconductors," *Journal of Applied Physics*, **45**(7), pp. 3023–3032.

[110] McDaniel, G. Y., S. T. Fenstermaker, W. V. Lampert, and P. H. Holloway (2004) "Rhenium ohmic contacts on 6H-SiC," *Journal of Applied Physics*, **96**(9), p. 53575364.

[111] Rose, A. (1955) "Space-Charge-Limited Currents in Solids," *Physical Review*, **97**(6), p. 15381544.

[112] Lampert, M. A. (1956) "Simplified Theory of Space-Charge-Limited Currents in an Insulator with Traps," *Phys. Rev.*, **103**, p. 16481656.

[113] Ashok, S., A. Lester, and S. J. Fonash (1980) "Evidence of space-charge-limited current in amorphous silicon Schottky diodes," *Electron Device Letters, IEEE*, **1**, p. 200202.

[114] Campbell, A. J., D. D. C. Bradley, and D. G. Lidzey (1997) "Space-charge limited conduction with traps in poly(phenylene vinylene) light emitting diodes," *Journal of Applied Physics*, **82**, p. 63266342.

[115] Galvagno, G., F. Roccaforte, A. Ruggiero, L. Calcagno, E. Zanetti, M. Saggio, F. Portuese, and F. L. Via (2006) "Temperature dependence of the c-axis drift mobility in 4H-SiC," *Microelectronic Engineering*, **83**(1), p. 4547.

[116] Dalibor, T., G. Pensl, H. Matsunami, T. Kimoto, W. J. Choyke, A. Schner, and N. Nordell (1997) "Deep Defect Centers in Silicon Carbide Monitored with Deep Level Transient Spectroscopy," *Physica Status Solidi (A), Applied Research*, **162**, p. 199225.

[117] Chattopadhyay, P. and B. RayChaudhuri (1993) "Frequency dependence of forward capacitance-voltage characteristics of Schottky barrier diodes," *Solid-State Electronics*, **36**(4), p. 605610.

[118] Werner, J., A. F. J. Levi, R. T. Tung, M. Anzlowar, and M. Pinto (1988) "Origin of the Excess Capacitance at Intimate Schottky Contacts," *Physical Review Letters*, **60**(1), p. 53.

[119] Missous, M. and E. H. Rhoderick (1991) "On the Richardson constant for aluminum/gallium arsenide Schottky diodes," *Journal of Applied Physics*, **69**(10), pp. 7142–7145.

[120] Unewisse, M. H. and J. W. V. Storey (1993) "Conduction mechanisms in erbium silicide Schottky diodes," *Journal of Applied Physics*, **73**(8), pp. 3873–3879.

[121] Hardikar, S., M. Hudait, P. Modak, S. Krupanidhi, and N. Padha (1999) "Anomalous current transport in Au/low-doped n-GaAs Schottky barrier diodes at low temperatures," *Applied Physics A: Materials Science & Processing*, **68**(1), pp. 49–55.

[122] McCafferty, P. G., A. Sellai, P. Dawson, and H. Elabd (1992) "Barrier characteristics of PtSi/p-Si Schottky diodes as determined from I-V-T measurements," *Solid-State Electronics*, **39**(4), pp. 583–592.

[123] Wagner, L. F., R. W. Young, and A. Sugerman (1983) "A note on the correlation between the Schottky-diode barrier height and the ideality factor

as determined from I-V measurements," *Electron Device Letters, IEEE*, **4**(9), pp. 320–322.

[124] Roccaforte, F., F. L. Via, V. Raineri, R. Pierobon, and E. Zanoni (2003) "Richardson's constant in inhomogeneous silicon carbide Schottky contacts," *Journal of Applied Physics*, **93**(11), pp. 9137–9144.

[125] Acar, S., S. Karadeniz, N. Tugluoglu, A. B. Selcuk, and M. Kasap (2004) "Gaussian distribution of inhomogeneous barrier height in Ag/p-Si (1 0 0) Schottky barrier diodes," *Applied Surface Science*, **233**(1-4), pp. 373–381.

[126] Asubay, S., mer Gll, B. Abay, A. Trt, and A. Yilmaz (2008) "Temperature-dependent behavior of Ti/p-InP/ZnAu Schottky barrier diodes," *Semiconductor Science and Technology*, **23**(3), p. 035006.

[127] Hamida, A. F., Z. Ouennoughi, A. Sellai, R. Weiss, and H. Ryssel (2008) "Barrier inhomogeneities of tungsten Schottky diodes on 4H-SiC," *Semiconductor Science and Technology*, **23**(4), p. 045005.

[128] Srivastava, A. K., B. M. Arora, and S. Guha (1981) "Measurement of Richardson constant of GaAs Schottky barriers," *Solid-State Electronics*, **24**(2), pp. 185–191.

[129] Aboelfotoh, M. O. and K. N. Tu (1986) "Schottky-barrier heights of Ti and $TiSi_2$ on n-type and p-type Si(100)," *Phys. Rev. B*, **34**(4), p. 23112318.

[130] Cetin, H. and E. Ayyildiz (2005) "Temperature dependence of electrical parameters of the Au/n-InP Schottky barrier diodes," *Semiconductor Science and Technology*, **20**(6), pp. 625–631.

[131] Biber, M., C. Coskun, and A. Trut (2005) "Current-voltage-temperature analysis of inhomogeneous Au/n-GaAs Schottky contacts," *The European Physical Journal Applied Physics*, **31**(2), pp. 79–86.

[132] Schmitsdorf, R. F., T. U. Kampen, and W. Monch (1997) "Explanation of the linear correlation between barrier heights and ideality factors of real metal-semiconductor contacts by laterally nonuniform Schottky barriers," in *The 24th conference on the physics and chemistry of semiconductor interfaces*, vol. 15, AVS, pp. 1221–1226.

[133] K.Sarpatwari, O.O.Awadelkarim, M.W.Allen, S.M.Durbin, and S.E.Mohney (to be published) "Extracting the Richardson Constant: IrO_x/n-ZnO Schottky Diodes," *Applied Physics Letters*.

[134] Sheng, H., S. Muthukumar, N. W. Emanetoglu, and Y. Lu (2002) "Schottky diode with Ag on (112-bar 0) epitaxial ZnO film," *Applied Physics Letters*, **80**(12), pp. 2132–2134.

[135] von Wenckstern, H., G. Biehne, R. A. Rahman, H. Hochmuth, M. Lorenz, and M. Grundmann (2006) "Mean barrier height of Pd Schottky contacts on ZnO thin films," *Appl. Phys. Lett.*, **88**(9), pp. 092102–3.

[136] Allen, M. W., R. J. Mendelsberg, R. J. Reeves, and S. M. Durbin (2009) "Oxidized noble metal Schottky contacts to n-type ZnO," *Appl. Phys. Lett.*, **94**(10), 103508.

[137] Mönch, W. (2001) *Semiconductor surfaces and interfaces*, Springer, New York.

[138] Chand, S. and J. Kumar (1997) "Effects of barrier height distribution on the behavior of a Schottky diode," *J. Appl. Phys.*, **82**(10), pp. 5005–5010.

[139] Khan, M. R. H., T. Detchprohm, P. Hacke, K. Hiramatsu, and N. Sawaki (1995) "The barrier height and interface effect of Au-n-GaN Schottky diode," *Journal of Physics D: Applied Physics*, **28**(6), pp. 1169–1174.

[140] Hacke, P., T. Detchprohm, K. Hiramatsu, and N. Sawaki (1993) "Schottky barrier on n-type GaN grown by hydride vapor phase epitaxy," *Applied Physics Letters*, **63**(19), pp. 2676–2678.

[141] Schmitz, A. C., A. T. Ping, M. A. Khan, Q. Chen, J. W. Yang, and I. Adesida (1996) "Schottky barrier properties of various metals on n-type GaN," *Semiconductor Science and Technology*, **11**(10), pp. 1464–1467.

[142] Ping, A., A. Schmitz, M. A. Khan, and I. Adesida (1996) "Characterisation of Pd Schottky barrier on n-type GaN," *Electronics Letters*, **32**(1), pp. 68–70.

[143] Wang, L., M. I. Nathan, T. Lim, M. A. Khan, and Q. Chen (1996) "High barrier height GaN Schottky diodes: Pt/GaN and Pd/GaN," *Applied Physics Letters*, **68**(9), pp. 1267–1269.

[144] Miller, E. J., E. T. Yu, P. Waltereit, and J. S. Speck (2004) "Analysis of reverse-bias leakage current mechanisms in GaN grown by molecular-beam epitaxy," *Applied Physics Letters*, **84**, pp. 535–537.

[145] Cui, Y., Z. Zhong, D. Wang, W. U. Wang, and C. M. Lieber (2003) "High Performance Silicon Nanowire Field Effect Transistors," *Nano Letters*, **3**(2), pp. 149–152.

[146] Cui, Y., Q. Wei, H. Park, and C. M. Lieber (2001) "Nanowire Nanosensors for Highly Sensitive and Selective Detection of Biological and Chemical Species," *Science*, **293**(5533), pp. 1289–1292.

[147] Smit, G. D. J., S. Rogge, and T. M. Klapwijk (2002) "Scaling of nano-Schottky-diodes," *Applied Physics Letters*, **81**(20), pp. 3852–3854.

[148] Donolato, C. (2004) "Approximate analytical solution to the space charge problem in nanosized Schottky diodes," *Journal of Applied Physics*, **95**(4), pp. 2184–2186.

[149] Hasegawa, H., T. Sato, and S. Kasai (2000) "Unpinning of Fermi level in nanometer-sized Schottky contacts on GaAs and InP," *Applied Surface Science*, **166**, pp. 92–96.

[150] Woodruff, S. M., N. S. Dellas, B. Z. Liu, S. M. Eichfeld, T. S. Mayer, J. M. Redwing, and S. E. Mohney (2008) "Nickel and nickel silicide Schottky barrier contacts to n-type silicon nanowires," in *35th Conference on the Physics and Chemistry of Semiconductor Interfaces (PCSI)*, vol. 26, AVS, Santa Fe, New Mexico (USA), p. 15921596.

[151] Lee, S.-Y. and S.-K. Lee (2007) "Current transport mechanism in a metal/GaN nanowire Schottky diode," *Nanotechnology*, **18**(49), p. 495701.

[152] Piscator, J. and O. Engstrm (2008) "A new mechanism for modulation of Schottky barrier heights on silicon nanowires," *Physica E: Low-dimensional Systems and Nanostructures*, **40**(7), pp. 2508–2512.

[153] Yeo, K. H., S. D. Suk, M. Li, Y.-Y. Yeoh, K. H. Cho, K.-H. Hong, S. Yun, M. S. Lee, N. Cho, K. Lee, D. Hwang, B. Park, D.-W. Kim, D. Park, and B.-I. Ryu (2006) "Gate-All-Around (GAA) Twin Silicon Nanowire MOSFET (TSNWFET) with 15 nm Length Gate and 4 nm Radius Nanowires," in *Electron Devices Meeting, 2006. IEDM '06. International*, pp. 1–4.

[154] Peng, J. W., S. J. Lee, G. C. A. Liang, N. Singh, S. Y. Zhu, G. Q. Lo, and D. L. Kwong (2008) "Improved carrier injection in gate-all-around Schottky barrier silicon nanowire field-effect transistors," *Applied Physics Letters*, **93**(7), pp. 073503–3.

[155] Dellas, N. S., B. Z. Liu, S. M. Eichfeld, C. M. Eichfeld, T. S. Mayer, and S. E. Mohney (2009) "Orientation dependence of nickel silicide formation in contacts to silicon nanowires," *Journal of Applied Physics*, **105**(9), pp. 094309–7.

[156] Liu, B., Y. Wang, T. ta Ho, K.-K. Lew, S. M. Eichfeld, J. M. Redwing, T. S. Mayer, and S. E. Mohney (2008) "Oxidation of silicon nanowires for top-gated field effect transistors," *Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films*, **26**(3), pp. 370–374.

[157] Ho, T. T., Y. Wang, S. Eichfeld, K. K. Lew, B. Liu, S. E. Mohney, J. M. Redwing, and T. S. Mayer (2008) "In Situ Axially Doped n-Channel Silicon Nanowire Field-Effect Transistors," *Nano Lett.*, **8**(12), p. 43594364.

[158] "Chemistry of Si-SiO2] interface trap annealing, volume = 63, doi = 10.1063/1.340317, number = 12, journal = Journal of Applied Physics, author = Michael L. Reed and James D. Plummer, month = jun, year = 1988, keywords = ANNEALING,CHEMICAL REACTION KINETICS,EXPERIMENTAL DATA,HIGH TEMPERATURE,INTERFACES,MATHEMATICAL MODELS,SEMICONDUCTOR DEVICES,SILICON,SILICON OXIDES,TEMPERATURE DEPENDENCE,TRAPPING, pages = 5776–5793," .

[159] Deal, B. E. (1974) "The Current Understanding of Charges in the Thermally Oxidized Silicon Structure," *Journal of The Electrochemical Society*, **121**(6), pp. 198–205.

[160] Wang, Y., K. Lew, T. Ho, L. Pan, S. W. Novak, E. C. Dickey, J. M. Redwing, and T. S. Mayer (2005) "Use of Phosphine as an n-Type Dopant Source for Vapor-Liquid-Solid Growth of Silicon Nanowires," *Nano Letters*, **5**(11), pp. 2139–2143.

[161] Smith, P. A., C. D. Nordquist, T. N. Jackson, T. S. Mayer, B. R. Martin, J. Mbindyo, and T. E. Mallouk (2000) "Electric-field assisted assembly and alignment of metallic nanowires," *Applied Physics Letters*, **77**(9), pp. 1399–1401.

[162] Groeseneken, G. and H. E. Maes (1997) "Basics and applications of charge pumping in submicron MOSFET's," in *Microelectronics, 1997. Proceedings., 1997 21st International Conference on*, vol. 2, pp. 581–589.

[163] Chen, W., A. Balasinski, and T. P. Ma (1993) "Lateral profiling of oxide charge and interface traps near MOSFET junctions," *Electron Devices, IEEE Transactions on*, **40**(1), pp. 187–196.

[164] Mahapatra, S. (1999) "A direct charge pumping technique for spatial profiling of hot-carrier induced interface and oxide traps in MOSFETs," *Solid-State Electronics*, **43**(5), pp. 915–922.

[165] Tsuchiaki, M., H. Hara, T. Morimoto, and H. Iwai (1993) "A new charge pumping method for determining the spatial distribution of hot-carrier-induced fixed charge in p-MOSFETs," *Electron Devices, IEEE Transactions on*, **40**(10), pp. 1768–1779.

[166] Suliman, S. A., N. Gallogunta, L. Trabzon, J. Hao, G. Dolny, R. Ridley, T. Grebs, J. Benjamin, C. Kocon, J. Zeng, C. M. Knoedler, M. Horn, O. O. Awadelkarim, S. J. Fonash, and J. Ruzyllo (2001) "The impact of trench geometry and processing on the performance and reliability of low voltage power UMOSFETs," in *Reliability Physics Symposium, 2001. Proceedings. 39th Annual. 2001 IEEE International*, pp. 308–314.

[167] Passmore, L. J., K. Sarpatwari, S. A. Suliman, O. O. Awadelkarim, R. Ridley, G. Dolny, J. Michalowicz, and C. T. Wu (2005) "Modified three terminal charge pumping technique applied to vertical transistor structures," in *J. Vac. Sci. Technol. B*, vol. 23, AVS, pp. 2189–2193.

[168] Hu, C. (2004) "Device challenges and opportunities," in *VLSI Technology, 2004. Digest of Technical Papers. 2004 Symposium on*, pp. 4–5.

[169] Yang, F.-L., D.-H. Lee, H.-Y. Chen, C.-Y. Chang, S.-D. Liu, C.-C. Huang, T.-X. Chung, H.-W. Chen, C.-C. Huang, Y.-H. Liu, C.-C. Wu, C.-C. Chen, S.-C. Chen, Y.-T. Chen, Y.-H. Chen, C.-J. Chen, B.-W. Chan, P.-F. Hsu, J.-H. Shieh, H.-J. Tao, Y.-C. Yeo, Y. Li, J.-W. Lee, P. Chen, M.-S. Liang, and C. Hu (2004) "5nm-gate nanowire FinFET," *VLSI Technology, 2004. Digest of Technical Papers. 2004 Symposium on*, pp. 196–197.

[170] Björk, M. T., O. Hayden, H. Schmid, H. Riel, and W. Riess (2007) "Vertical surround-gated silicon nanowire impact ionization field-effect transistors," *Applied Physics Letters*, **90**(14), 142110.

[171] Deal, B. E. (1974) "The Current Understanding of Charges in the Thermally Oxidized Silicon Structure," *Journal of The Electrochemical Society*, **121**(6), pp. 198C–205C.

[172] Sze, S. (1969) *Physics of semiconductor devices*, New York:Wiley, pp.315–316.

[173] Paulsen, R. E. and M. H. White (1994) "Theory and application of charge pumping for the characterization of Si-SiO2 interface and near-interface oxide traps," *Electron Devices, IEEE Transactions on*, **41**(7), pp. 1213–1216.

[174] Heiman, F. and G. Warfield (1965) "The effects of oxide traps on the MOS capacitance," *Electron Devices, IEEE Transactions on*, **12**(4), pp. 167–178.

[175] Lu, C.-Y., K.-S. Chang-Liao, P.-H. Tsai, and T.-K. Wang (2006) "Depth Profiling of Border Traps in MOSFET With High-k Gate Dielectric by Charge-Pumping Technique," *Electron Device Letters, IEEE*, **27**(10), pp. 859–862.

Vita

Karthik Sarpatwari

1594 S.Riverstone Ln, Apt. 301
Boise, ID 83706

karthik.sarpatwari@gmail.com
1-814-777-1157

Education

- PhD, Engineering Science and Mechanics, The Pennsylvania State University
  - Dissertation advisors: Profs. O. O. Awadelkarim and S. E. Mohney
- M.S, Engineering Science, The Pennsylvania State University
- B.Tech., Metallurgical Engineering, Indian Institute of Technology Madras

Research experience

Effects of barrier height inhomogeneities on Schottky barrier parameter extraction

- Numerical and analytical approaches to extract true Schottky barrier parameters
- Experimental determination of Richardson constant of ZnO, GaN

TCAD simulation study of axial Schottky contacts to nanowire

- Method to extract true Schottky barrier parameters from current-voltage characteristics of Schottky contacts to nanowires
- Effects of surface charge on nanowire conduction properties studied using 3D TCAD simulations

Publications

- Extracting the Richardson constant: IrO_x/n-ZnO Schottky diodes, K. Sarpatwari, O. O. Awadelkarim, M. W. Allen, S. M. Durbin and S. E. Mohney, **Applied Physics Letters**, **242110**, Vol.94, No.24, 2009
- Analysis of currentvoltagetemperature characteristics in SiC Schottky diodes using threshold-accepting simulated-annealing techniques, K. Sarpatwari, L. Passmore, S. A. Suliman and O. O. Awadelkarim, **Solid State Electronics**, Vol.51, Issue 5, 2007