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CHARACTERIZATION OF MOS CAPACITOR GATE OXIDE EMBEDDED WITH SILICON QUANTUM DOTS

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ABSTRACT

In this study, characterization of Metal Oxide Semiconductor (MOS) capacitor embedded with Silicon Quantum Dots (QDs) is done. This study aims to understand the oxidation dependent size variation of Si QDs. Ion implantation being the choice of deposition for Si nanocrystal experiments, a different technique: Mist Deposition is chosen as a vehicle of deposition for this study. Deposition of times of 20 mins and 10 mins with a density of .1mg/ml is chosen with the QDs suspended in toluene. Colloidal Si QD solution is prepared which is then mist deposited onto an n-type silicon substrate. The substrate, along with the QDs, is thermally oxidized at 800°C for a pre-calculated time: 5 min (2.14 nm), 30 min (4.63 nm) and 90 min (8.34 nm). Metal (Aluminum) contacts are deposited on the samples thus forming MOS capacitors—embedded with Si QDs.

Primary method of characterization is electrical characterization along with AFM surface studies on selected samples. Electrical characterization involving Current-Voltage (I-V) and Capacitance-Voltage (C-V) measurements are employed to understand the role by QDs in altering the MOS capacitor behavior. With varying oxide thickness, the characterization results obtained are analyzed to understand the oxidation dependent size variation of the oxidized Si QDs. The oxide thickness is varied to also study the role of oxide in assisting tunneling. C-V hysteresis is performed to memory effect or charge storage in the QDs.

The results obtained confirm the QD size dependent variation of electrical characteristics of MOS capacitors. I-V measurements confirm QDs playing a role while the C-V measurements

indicating the existence of tunneling current. Hysteresis measurements strongly indicate charge storage in the QDs while being absent in the control samples (without QDs). AFM measurements also indicate the QDs on the sample surface agglomerating forming lumps.

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Chapter 1: INTRODUCTION

The need for larger storage and processing power has been the driving force of the semiconductor industry. As technology improves bringing greater detail to life, ability for larger storage is becoming more demanding. As the chips keep gradually scaling down, the usage of linear memory is reaching its fundamental limits. Devising newer methods of storage is apparent. Silicon nanocrystals provide an immediate choice for such applications. Silicon is abundant on the earth's crust and the material has been researched thoroughly for its usage as computer chips as well as memory applications. The contemporary flash memory devices use a Floating Gate MOS capacitor architecture that has shown reliability over the years. However, as the device is reaching its architectural limits newer structures are paving way. Nanocrystals embedded in the gate/tunnel oxide are being thoroughly studied and have shown promising results of up to $1e^-$ /nanocrystal [1]. The whole scope of this project is to study the importance of Si nanocrystals for possible memory applications.

The data storage device today represents a large part of the semiconductor market. They are divided in two main groups: Volatile memories (SRAM and DRAM) and Non-volatile memories (EEPROM; Electrically Erasable Programmable Read-Only Memory). Volatile memories, allow the data to be accessed and modified very quickly, but lose their data when the power supply is turned off Non-volatile memories, on the other hand, do not require any power to retain the information stored in the memory cell. The "flash" cells technology has become one of the most promising solutions to data storage because of their excellent compromise between flexibility and cost. They allow high densities of data storage, quick erase and program times along with a good reliability (more than 10,000 erase cycles) [1, 2].

One of the key elements of a flash cell is the tunnel oxide. When the cell is not in use, the tunnel oxide is responsible for the data retention: this insulator layer retains the charges stored in the device. It also allows the transfer of charge when the state of the cell is modified (program or deprogrammed). The repeated erase and write cycles tend to degrade the quality of the oxide, reducing the lifetime. As with other semiconductor devices (mainly MOSFETs), the constant scaling down of the devices sizes results in a reduction of the oxides thicknesses and increase in the electric field. Problems then start to surface at this point: higher leakage currents (loss of data), more trapped charges or a degraded resistance. Future is seen with nanocrystal (or Quantum Dot) based memories, offering lower voltage operation (energy efficiency) and larger capacities [1, 2].

1.1 Flash Memory Operation

A flash cell is basically a traditional MOS transistor with a specific gate stack, which retains electrons even without power supply. The device can be electrically programmed (write operation), deprogrammed (erase operation) and read. Unlike other memory devices, no UV light is needed, and the cells to be erased or programmed can be chosen precisely. The gate is made up of a Floating Gate (FG) surrounded by an insulator and controlled by the control gate (CG), a second gate on the top (Fig 1.1). Being electrically isolated, the floating gate is able to store charges, and their presence or absence corresponds to the two states of the cell, logic 0 or 1 [1, 2].

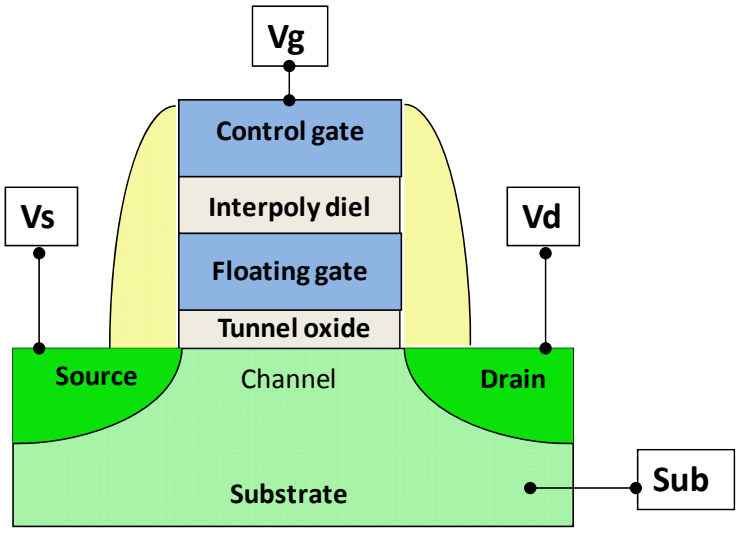

Fig. 1.1.1: Schematic of a Flash memory cell

The first dielectric, the tunnel oxide (TO), is a nitrated silicon oxide in the range of 95 to 100 A°. It acts as an isolation layer between the channel and the FG. This oxide has to be thick enough to prevent electron leakage from the FG to the channel by tunneling effects, in order to provide long enough data retention times. Simultaneously, is should also bear repeated write/erase operations. The target lifetime is around 20 years, or 10^4 to 10^5 program times, with large amount of energy involved. Reliability becomes one of the main concerns of the cell characteristics. Until now, the standard thickness of the TO has remained around 100 A°, and in order to decrease this value, techniques using high-k metal gate or silicon nitride are being investigated. The dielectric between the FG and the CG is an oxide-nitride-oxide stack (ONO), with thickness ranging around 43A°/52A°/52A° respectively. The rest of the cell has the same structure as a MOS transistor [1, 2].

Read operation

The read operation of a programmed cell is done by applying a fixed and positive voltage on the FG (+5V) and on the drain (+0.7V), and by measuring the resulting current in the cell like a MOS transistor. The source, well and bulk are all grounded. The presence or absence of charges in the FG will change the threshold voltage of the cell and thus the current driven at a given bias voltage on the CG. If the bias voltage is chosen appropriately and if there are enough charges in the FG, the current of the erased cell (no charges, logic 1) is high while the current of a programmed cell (charges, logic 0) is low. In the case of an n-MOS, if the TO is filled with electrons (charged), the gate voltage first has to compensate the TO charges before starting to attract electrons to create the channel, resulting in a higher threshold voltage [1, 2].

Write

The write operation consists of an injection of electrons in the FG from the channel through the TO. The challenge is to force the charge through an insulating layer. The mechanism involved in flash cells is called “channel hot electron” (CHE), or “hot electron injection” (HEI). The electrons are accelerated in the channel by an electric field between the source and the drain, and deviated toward the FG by the vertical field between the CG and the channel, thus gaining enough kinetic energy to overcome the energy barrier and cross the oxide layer. The high energy levels involved in this operation explain the necessity of having a TO resistant enough to bear electron injections without degrading itself [1, 2].

Erase

The principle behind the erase operation remains the same: to force electrons through the TO. Here, the electron injection from the FG to the channel is achieved through Fowler-Nordheim

tunneling. Since the bias applied on the CG is high, the energy barrier between the FG and the channel becomes triangular. Unlike the write operation, the electrons travel though the oxide to the substrate on a vertical axis [1, 2].

Chapter 2: BACKGROUND

2.1 Nanocrystals

In the interdisciplinary field of nanotechnology, any particle that behaves and exists in a whole new way that can be clearly distinguished from its bulk form. Nanocrystal is one such term applied to materials that differ in properties from its bulk form. Many physical phenomena in its natural form exist in size ranging from 1nm to 200nm. Nanocrystalline materials are so different that quantum mechanics plays a huge role in its properties and the physics behind it has to be investigated with a whole new dimension. Nanocrystals may or may not demonstrate size-related properties e.g. change in the bandgap with respect to size or moving from direct bandgap to indirect bandgap material.

Using NCs opens up new possibilities of fabricating novel materials and devices for applications that were previously viewed as material limitations with bulk materials. The interactions with proximal NCs leading to new collective phenomena not observed with bulk materials and as its properties may be size dependent the combination the former and latter lead to exotic applications. The future appears bright for nanocrystals. Engineering the size and composition of nanocrystals is a whole new field in itself. Despite being exotic in existence, nanocrystals face several challenges with thermodynamics, deposition as well as fine tuning of its properties.

2.1.1 Quantum Dots

Quantum Dots can be understood as synthetic or artificial atoms. The energy levels are discretized similar to an atom therefore Quantum dots can be understood as “artificial” atoms.

These atoms are engineered to observe quantum effects through electron confinement. Several other definitions exist: 1) Any solid material in the form of a particle with a diameter comparable to the wavelength of an electron; 2) Quantum dot is a semiconductor whose excitons are confined in all the three spatial directions. Quantum confinements come in other dimensions 2D (Quantum Well), and 1D (Quantum Wire); further confinement leads to a 0D quantum dot. These quantum dots form a subset of nanocrystals where the nanocrystal sizes are further shrunk to a point where quantum effects become more significant and quantum confinement comes to play.

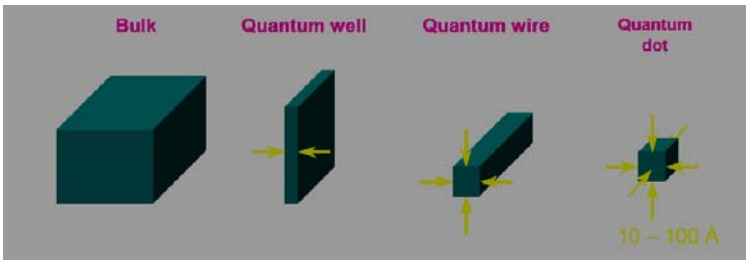

Fig. 2.1.1.1: Spatial confinements leading to n-dimensional nanostructures

Some of the classical scaling laws come to significance for nanostructures, mainly surface to volume ratio (S/V), Power requirement and wear life [3]. Surface area ($S \approx d^2$) and volume ($v \approx d^3$) relate to each other by − −. This implies larger surface area for smaller clusters. A larger surface area has a larger number of atoms and dangling bonds [3]. The power requirement scales as $P \approx d^3$. There, devices made of nanostructures would be expected to operate with a miniscule amount of power. The wear life is proportional to the thickness (d) and inversely proportional to the erosion rate. Erosion rate scales with surface area (d^2) yielding to a wear life scaling of 1/d [3]. It is due to these properties that QDs of interest to scientists.

2.1.2 Density of States calculation

In statistical and condensed matter physics, Density of States (DOS) for a system describes the number of available states that are ready to be occupied. Prior to calculating density of carriers, DOS must be calculated. In the derivation below, DOS' dependence on the dimensionality will be seen. Consider a cubic piece of semiconductor with a side *L*. Assumption can be made to model the semiconductor as an infinite quantum well where the electrons in the well are free to move with an effective mass of *m**. The Schrödinger's equation can be given by [4, 5]

$$\frac{\hbar^2}{2m^*} * \frac{d^2\Psi(x)}{dx^2} + V(x)\Psi(x) = E\Psi(x)$$

Boundary conditions are $\Psi(x) = 0$ at $x = 0$, $x = L$.

The solutions of the wave equation are of the form $\Psi(x) = A sin(k_x x) + B cos(k_x x)$

Where A and B are constants. On applying the boundary conditions we get [4, 5]

$$k_x = \frac{n\pi}{L}, \text{ n} = 1, 2, 3$$

A similar approach can be used to find k_y and k_z. Each of the possible solution corresponds to a cube in the k-space as shown in the figure below [4, 5].

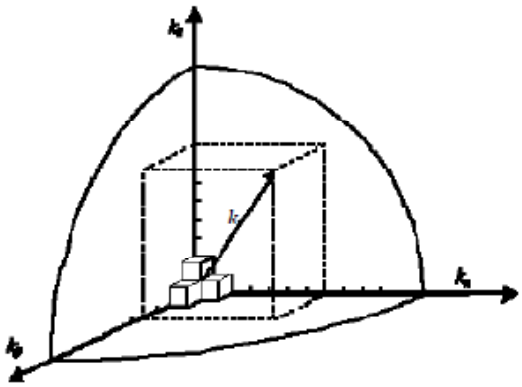

Fig. 2.2.2.1: Dimensions in k-space

The total number of solutions with a different value for k_x, k_y and k_z and with a magnitude of the wavevector less than k is obtained by calculating the volume of one eighth of a sphere with radius k and dividing it by the volume corresponding to a single solution, $(\pi/L)^3$, yielding [4, 5]:

$$N = 2 \times \frac{1}{8} \times (\frac{L}{\pi})^3 \times \frac{4}{3} \times \pi \times k^3$$

A factor of 2 is multiplied to take into account the two possible spins for each solution. The density per unit energy is [4, 5]:

$$\frac{dN}{dE} = \frac{dN}{dk}\frac{dk}{dE} = (\frac{L}{\pi})^3 \pi k^3 \frac{dk}{dE}$$

The kinetic energy E of a particle is related to the wavenumber, k, by [4, 5]:

$$E(k) = \frac{\hbar^2 k^2}{2m^*}, \text{ providing} \frac{dk}{dE} = \frac{m^*}{\hbar^2 k} \text{ and } k = \frac{\sqrt{2m^* E}}{\hbar}$$

The density of states (3D) per unit volume per energy, g(E) becomes [4, 5]:

$$g(E) = \frac{1}{L^3}\frac{dN}{dE} = \frac{8\pi\sqrt{2}}{h^3} m^{*3/2}\sqrt{E}, \text{ for } E \geq 0.$$

As Quantum Dots are 0D structures, the density of states (DOS) for 0D case is also needed. When considering a 0D case no free motion is possible as the electrons are confined in all the three directions. Because there is no k-space that can be filled with electrons, all available states exist as discrete energies. Thus, in 0D case, the DOS can be represented with a delta function [5]:

$$g(E)_{0D} = 2\delta(E - E_C)$$

Degrees of freedom	Dispersion (kinetic energy)	Density of states	Effective density of states
3 (bulk)	$E = \frac{\hbar^2}{2m^*}(k_x^2 + k_y^2 + k_z^2)$	$\rho_{DOS}^{3D} = \frac{1}{2\pi^2}\left(\frac{2m^*}{\hbar^2}\right)^{\frac{3}{2}}\sqrt{E - E_C}$	$N_c^{3D} = \frac{1}{\sqrt{2}}\left(\frac{m^* kT}{\pi\hbar^2}\right)^{\frac{3}{2}}$
2 (slab)	$E = \frac{\hbar^2}{2m^*}(k_x^2 + k_y^2)$	$\rho_{DOS}^{2D} = \frac{m^*}{\pi\hbar^2}\sigma(E - E_C)$	$N_c^{2D} = \frac{m^*}{\pi\hbar^2}kT$
1 (wire)	$E = \frac{\hbar^2}{2m^*}(k_x^2)$	$\rho_{DOS}^{1D} = \frac{m^*}{\pi\hbar}\sqrt{\frac{m^*}{2(E - E_C)}}$	$N_c^{1D} = \sqrt{\frac{m^* kT}{2\pi\hbar^2}}$
0 (box)	–	$\rho_{DOS}^{0D} = 2\delta(E - E_C)$	$N_c^{0D} = 2$

Fig. 2.2.1.2: Summary of DOS for 3D, 2D, 1D, and 0D structures [5]

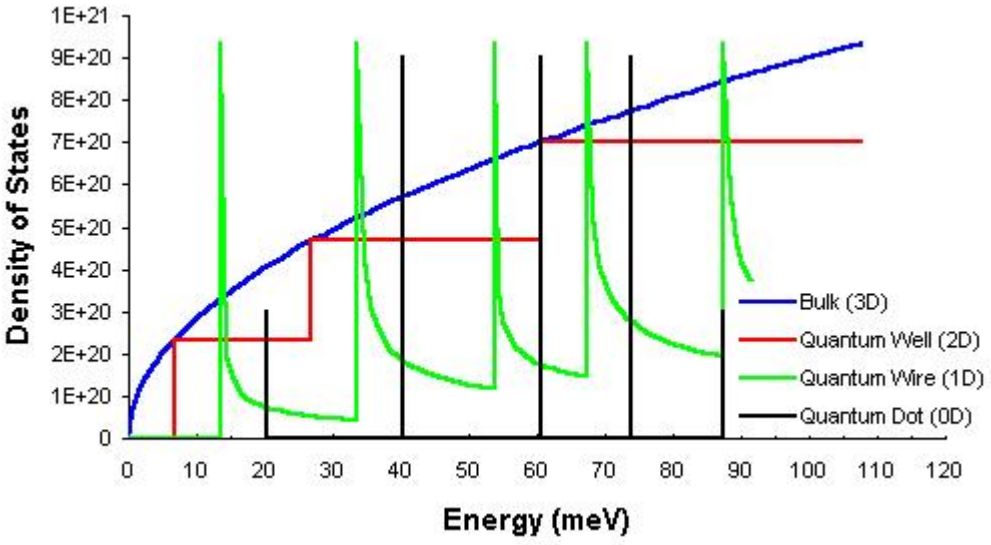

Fig. 2.3.1.3: Density of States vs. Energy for various dimensions [5]

2.1.3 Quantum Dots Synthesis

Synthesis of Quantum Dots can be divided into two distinct paths: Top-down and Bottom-up approach. Bottom-up approaches seek to have smaller (from the molecular level) components built up into more complex assemblies, while top-down approaches seek to create nanoscale devices by using larger, externally-controlled ones to direct their assembly. The top-down approach primarily relies on micro-patterning such as photolithography and ink-jet printing. Bottom-up approach relies on manipulating the chemistry of the molecules to create a desired shape. The manipulation also involves altering surface chemistry to assist "self-assembly" of the molecules [33-37].

Top-down Etch: Lithography is the primary technique employed to create quantum dots [33, 34]. The figure below illustrates top-down approach of creating quantum dots. The disadvantages of Lithography technique are [35]:

1. Edge effects
2. Defects due to reactive ion etching
3. Less control over size
4. Low quantum efficiency
5. Slow, less density, and prone to contamination

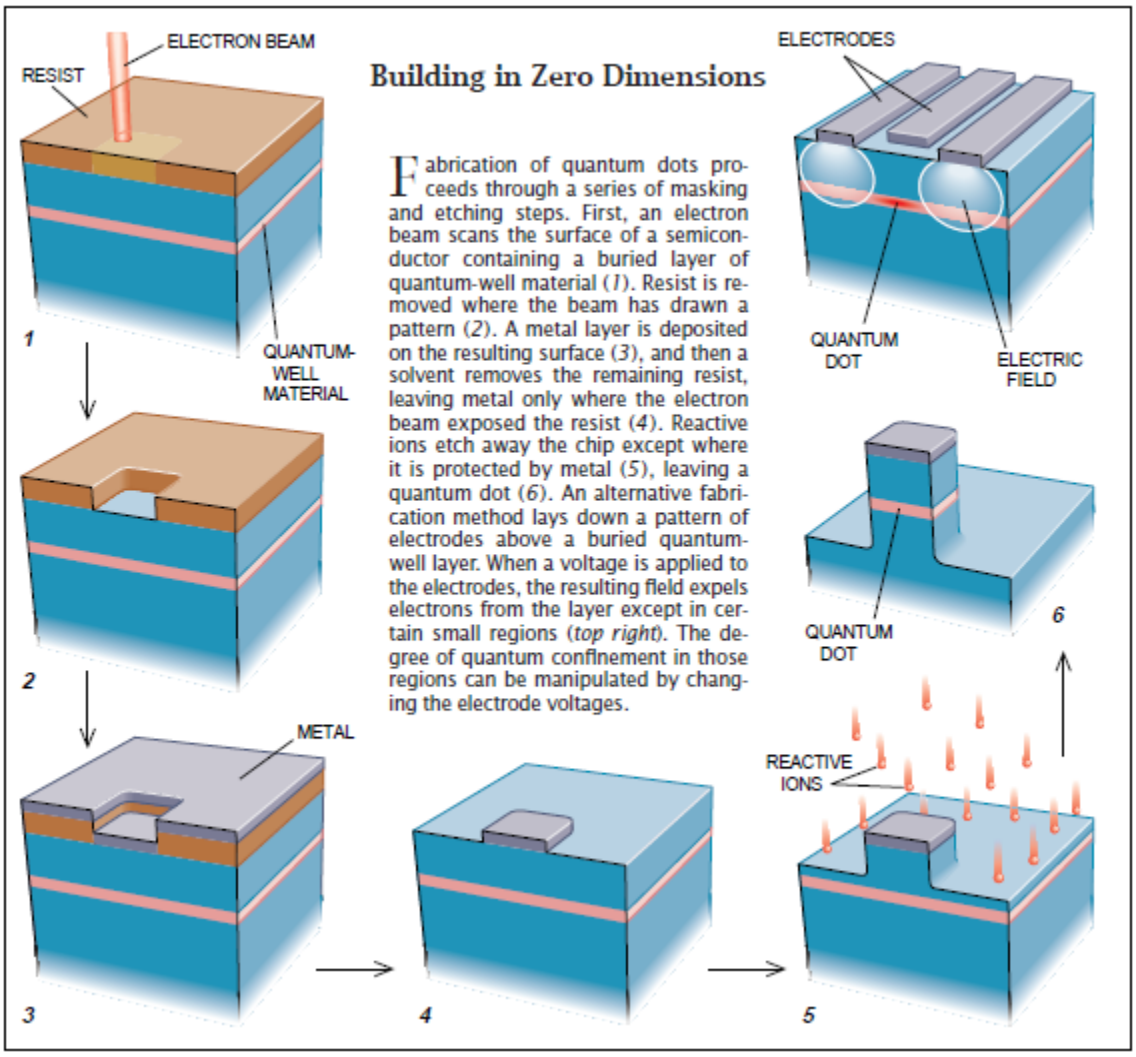

Fig. 2.1.3.1: Illustration of top-down approach for creating quantum dots [10]

Bottom-up Approach:

Self-Assembly is a bottom-up processes in which a disordered system of pre-existing components forms an organized structure or pattern as a consequence of specific, local interactions among the components themselves, without external direction. Epitaxial techniques such MBE (Fig below) and ALD are employed for bottom-up approaches [35].

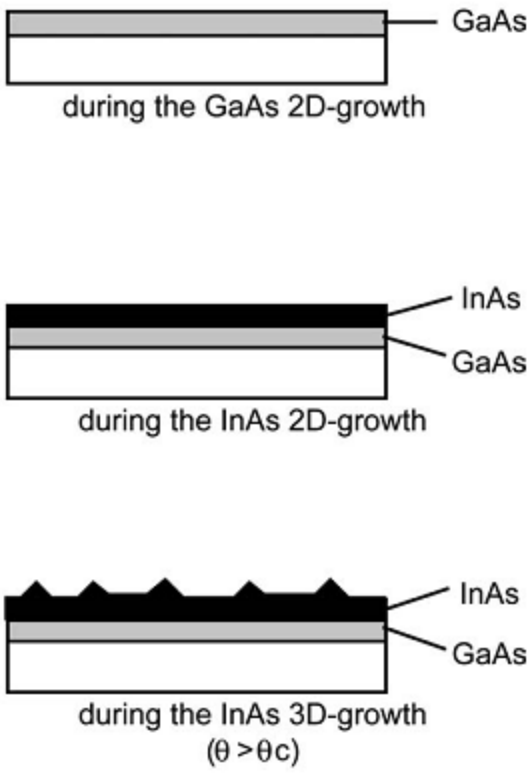

Fig. 2.1.3.2: Illustration of self-assembly using MBE [35]

Colloidal route: This is another bottom-up technique where supramolecular chemistry is employed to create nanoparticles. Synthesis of colloidal nanocrystals is done with a combination of solution chemistry and crystal growth. The size of nanoparticles can be controlled by: reaction time, temperature, Reagent/Stabilizer concentration (more nucleation, small size) and Surfactant chemistry (provide capping layer leading to more binding, more steric effect, small size), and reagent addition [36, 37].

2.1.4 Applications of Quantum Dots

Nanocrystal Memory Application

Unlike the traditional flash memory, a nanocrystal memory has nanocrystals embedded into the oxide. The nanocrystals have control oxide on the gate and tunnel oxide (between nanocrystals and substrate). In nonvolatile memories (EEPROM), electrons are injected by tunneling into a floating gate to cause a threshold voltage shift. This threshold voltage shift is detected by current sensing [1, 23, 24]. The threshold shift magnitude is related to the charge in the floating gate, the thickness of the control oxide, and other device parameters. To achieve non-volatility in Flash EEPROM's, the tunneling oxide thickness is maintained high enough (-7 nm) [1, 2, 23]. The use of large oxide thicknesses necessitates large voltages for the injection of charge into the floating gate. These large voltages result in hot-carrier degradation.

In a nanocrystal memory the charge loss through lateral paths to the contacting regions is suppressed by use of a larger inter-nanocrystal spacing. Thus, smaller oxide thicknesses—less than 5 nm—becomes a possibility [23, 24]; Smaller oxide thicknesses also lead to low voltage operation. Charger storage using nanocrystal memories have attractive characteristics:

1) Faster write times due to the large current densities in the direct tunneling regime of thin oxides [1, 23, 24].
2) Extremely low degradation because of operation of the device in direct tunneling regime where hot carrier effects are strongly reduced [23].
3) Longer retention time at much smaller injection oxide thickness due to coulomb blockade and quantum confinement [23, 24].
4) Operation at smaller voltages and lower power along with simple low cost fabrication process [23, 24].

5) Excellent immunity to stress induced leakage current and defects within the floating gate or insulating layers due to the distributed nature of the charge storage in the discontinuous nanocrystal layer [24].
6) Reduced punch through achieved by eliminating drain-to-floating gate coupling, allowing shorter channel lengths, and smaller cell area [24].

It is believed that silicon nanocrystal floating gate memories could outperform conventional floating gate memory devices. Outperformance is attributed to faster read and write times, higher reliability, and lower power dissipation. However, the issue lies with nanocrystal uniformity in size. Unless the nanocrystals are free from interface states they may limit the switching speed by distribution of charge transit times and charging voltages [24].

Quantum Dot Photovoltaics

In a solar cell, negatively doped (n-type) material with extra electrons forms a junction with positively doped (p-type) material, with extra holes in the band otherwise filled with valence electrons. When a photon with energy matching the band gap strikes the semiconductor, it is absorbed by an electron, which jumps to the conduction band, leaving a hole. Both electron and hole migrate through the junction's electric field in opposite directions. When the solar cell is connected to an external circuit, an electric current is generated. Photons with energy higher than the band gap are absorbed while photons with less energy than the band gap slip right through without being absorbed. The excess energy is wasted, and dissipated as heat. It is possible to improve on the efficiency by stacking materials with different band gaps together in multi-junction cells. Stacking dozens of different layers together can increase efficiency theoretically

to greater than 70 percent [11, 13, 16]. But this results in technical problems such as strain damages to the crystal layers.

Quantum dots have quantum optical properties that are absent in the bulk material due to the confinement of electron-hole pairs (called excitons) on the particle [3]. The primary advantage of quantum dots is their tunable bandgap [3, 10, 11]. This means the wavelength of radiation absorption or emission can be adjusted at will: the larger the size, the longer the wavelength of light absorbed and emitted [3]. Lead Sulphide (PbS) QDs have absorption peaks that can be tuned from ~800 to ~2000 nm [11, 17]. The greater the bandgap of a semiconductor, the more energetic the photons absorbed, and the greater the output voltage. On the other hand, a lower bandgap results in the capture of more photons including those in the red end of the solar spectrum, resulting in a higher output of current but at a lower output voltage. An optimum bandgap can be selected for highest possible solar energy conversion. This can also be achieved by using a mixture of quantum dots of different sizes to capture the maximum amount of the incident light [11]. Another advantage of quantum dots is that they can be molded into a variety of different form and variety of substrates; this property cannot be achieved with bulk semiconductors. In the colloidal form suspended in solution, they can be processed for deposition on inexpensive substrates such as plastics, glass or metal sheets [11, 12, 13, 15, 17].

Infrared photovoltaic cells – which transform infrared light into electricity - are attracting much attention, as nearly half of the approximately $1000 Wm^3$ of the intensity of sunlight is within the invisible infrared region. So it is possible to use the visible half for direct lighting while harvesting the invisible for generating electricity [11, 13, 14]. Photovoltaic cells that respond to infrared can even capture radiation from a fuel-fire emitter; and co-generation of electricity and

heat are said to be quiet, reliable, clean and efficient. A 1 cm^2 silicon cell in direct sunlight will generate about 0.01W, but an efficient infrared photovoltaic cell of equal size can produce theoretically 1W in a fuel-fired system [11].

The formation of multiple excitons per absorbed photon happens when the energy of the photon absorbed is far greater than the semiconductor band gap. This phenomenon does not occur in bulk semiconductors where the excess energy simply dissipates away as heat before it can cause other electron-hole pairs to form. But in semiconducting quantum dots, the rate of energy dissipation is significantly reduced, and the charge carriers are confined within a minute volume, thereby increasing their interactions and enhancing the probability for multiple excitons to form [25, 26, 27].

2.2 Mist Deposition

The term Mist deposition is very self-explanatory. Needless, Mist deposition is a physical liquid deposition method developed to deposit liquid precursors without the inherent limitations of spin coating. It can be used to deposit a wide variety of materials: ferroelectrics, high-k dielectrics, organic semiconductors, photoresist, and quantum dots. In this deposition, the precursors are created to form fine droplets than are deposited on to the substrate. The fine mist is then uniformly deposited on then deposited in a controlled fashion. The mist then uniformly coalesces on the surface. Like in spin coating the mist deposition is followed by thermal curing of the film. This technique is analogous to spray deposition only, that the particles are accelerated on the substrate with the presence of an electric field. The other main characteristic is its ability to create fine droplets.

The principle behind mist deposition is to force the solution to be deposited into a three chambered atomizer through a venture type nozzle to convert the liquid into droplets of mist. The advantage of mist deposition is that it is not restricted by the shape of the substrate and the environment is so controlled that films as thick as 3nm can be deposited with relative ease [21].

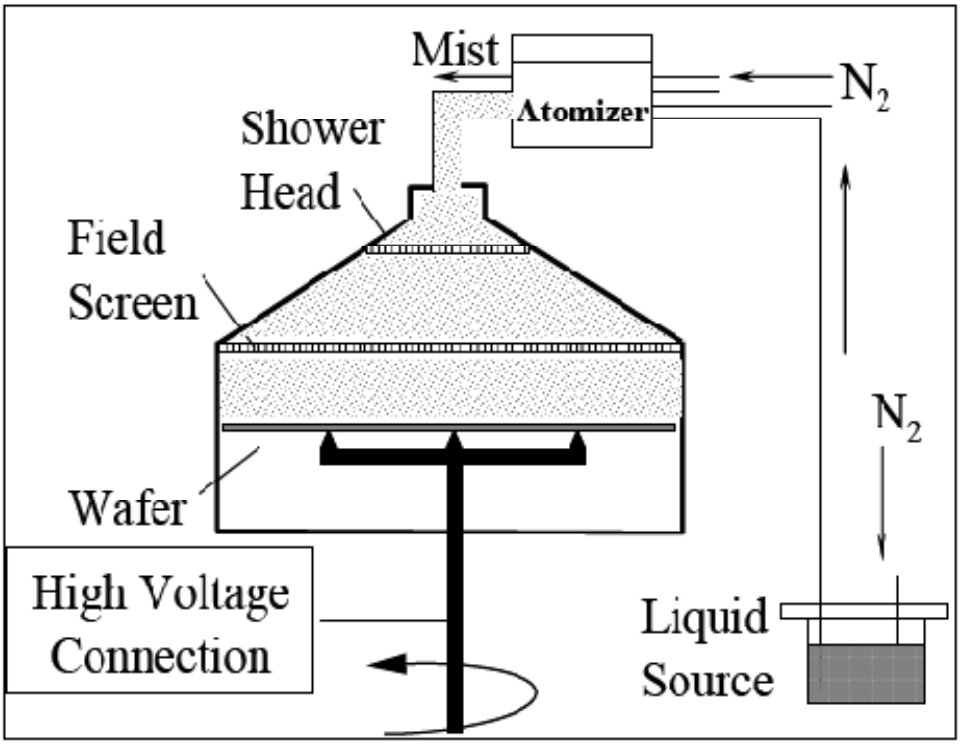

Fig. 2.2.1: Schematic of Mist Deposition System [21]

2.2.1 Deposition Process

As the deposition has no interaction with the substrate, the substrate can be any odd-shaped or non-rigid material i.e. flexible substrates. This is one of the primary advantages of mist deposition. The liquid precursor is a colloidal solution, Si nanocrystals suspended in toluene, which is carried by ultra-pure nitrogen gas by siphoning. This ultra-pure nitrogen aids in converting the mist into charged droplets which is then carried onto the deposition chamber. The mist droplets become charged by the principle of shearing friction, being separated from the

liquid. The positive charging of droplets is balanced by an equal amount of negatively charged droplets; this makes the mist neutral. The mist droplets of the desired size can be filtered and carried onto the substrate. This size selection is accomplished with the help of two mass impactors present inside the atomizer by inertial separation. The deposition takes place in the presence of an electric field which can be optimized from 0-10kV/cm. The substrate holder can be rotated by a motor at a constant speed of 10 RPM. This assists in film uniformity during deposition.

2.2.2 Parameter variation

The film thickness can be controlled by the deposition time, liquid concentration (density), flow rate and strength of the electric field. For Si QDs, the flow rate and electric field are optimized hence no changes are made to this. Time is the easiest and the most flexible parameter; film thickness can be increased by increasing the time. Varying the concentration (density) also increases the deposition thickness but has been observed to be rougher [19]. Higher liquid flow rate can be changed (increased) to hasten the deposition process but can lead to higher surface roughness [19, 22]. The final parameter electric field is just as pivotal as the others. Deposition can be carried out with the absence of electric field and presence of only gravitational field. However, it has been observed that the mist can be swept away be exhaust flow [22]. The presence of a strong electric field restricts the mist to the substrate. It is reported that higher electric field accelerate more mist towards the substrate [21, 22]. By varying these parameters, different film thickness from 3 nm to 500 nm have be deposited [21].

2.3 MOS Capacitors

After p-n junction devices, a Metal Oxide Semiconductor (MOS) capacitor is the topic of interest to device engineers. Prior to developing MOSFET, a MOS capacitor is built to study the dielectric properties, capacitance response and charge carrier statistics. A MOS capacitor has a simple structure; it is stacked with metal, dielectric (usually SiO_2) and substrate (n or p-type). The substrate doping can vary from 1×10^{14} cm^{-3} to $1*10^{18}$ cm^{-3}. A p-type substrate requires a bottom contact while bottom contact for n-type substrate is optional.

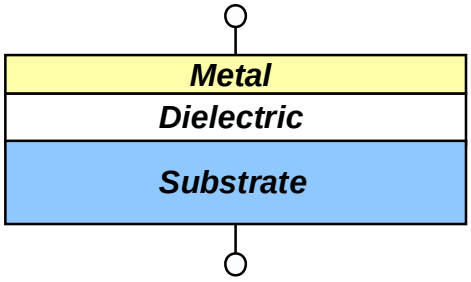

Fig. 2.3.1: Schematic of a Metal Oxide Semiconductor (MOS) capacitor

Despite slight structural variance from traditional capacitors, MOS Capacitor shows similar behavior under bias. In order to study a MOS capacitor performance, the device is tested under high and low frequency while the voltage is swept (from negative to positive). The capacitance depends on the voltage that is applied to the gate (with respect to the body). There are roughly three regimes of operation separated by two voltages: (1) Accumulation in which mobile carriers of the same type as the body accumulates at the surface (electrons); (2) Depletion in which the surface is devoid of any mobile carriers leaving only a space charge or depletion layer; (3) Inversion in which mobile carriers of the opposite type to the body (holes) aggregate at the surface to "invert" the conductivity type. These three regimes offer an explanation of semiconductor surface changes. The two voltages that demarcate the three regimes are (a)

Flatband Voltage (V_{FB}) which separates the accumulation regime from the depletion regime and (b) the Threshold Voltage (V_T) which demarcates the depletion regime from the inversion regime.

Surface Accumulation (VGB > VFB): An applied positive gate voltage larger than the flatband voltage ($V_{GB} > V_{FB}$) induces positive charge on the "metal" gate and negative charge in the semiconductor. The only negative charges available are electrons and they accumulate at the surface. The electron concentration at the surface is above the bulk value, thus leading to a condition that is called surface accumulation. The flatband voltage (V_{FB}) is the voltage at which there is no charge on the plates of the capacitor and hence there is no electric field across the oxide. Its numerical value depends on the doping of the semiconductor and on any residual interface charge that may exist at the interface between the semiconductor and the insulator. When the surface of the semiconductor is accumulated, a plot of the charge per unit area (Q_N) at the semiconductor / oxide interface versus the applied voltage (V_{GB}) is linear and the slope is the oxide capacitance per unit area, C_{ox} , which is given by

$$C_{MOS,Accumulation} = C_{Max} = A * C_{ox} = A * \frac{\varepsilon_{ox}}{t_{ox}}$$

where ε_{ox} is the permittivity of the oxide and it is $3.9\varepsilon_o$. ε_o is the permittivity of free space or air. $\varepsilon_o = 8.854 \times 10^{-14}$ Fcm^{-1}. The unit for C_{ox} is Fcm^{-2}.

Surface Depletion ($V_T < V_{GB} < V_{FB}$): If the applied gate voltage is brought below the flat band voltage (remember the flat band voltage is the gate voltage at which there is no charge in the MOS capacitor), a negative charge is induced at the interface between the poly-silicon gate and

the oxide. This leads to a positive charge being induced at the other interface i.e. the oxide/semiconductor interface. This could only be accomplished by "pushing" all the mobile negative carriers (electrons) away and exposing the fixed positive charge from the donors. Hence the surface of the semiconductor is depleted of mobile carriers leaving behind a positive space charge. The space charge layer resulting behaves also like a capacitor having a capacitance per unit area (C_D), which depends on V_{GB} and is given by

$$C_D(V_{GB}) = \frac{\varepsilon_{Si}}{x_d(V_{GB})}$$

where ε_{Si} is the permittivity of the silicon and it is $11.7\varepsilon_o$. ε_o is the permittivity of free space. $\varepsilon_o = 8.854 \times 10^{-14}$ Fcm^{-2}. x_d is the depleted silicon layer thickness. The unit of C_D is Fcm^{-2}. The silicon depletion layer thickness increases as the gate voltage decreases because more electrons are pushed away exposing more fixed positive ionized dopants leading to thicker space charge layer. The capacitance of the depleted silicon decreases and hence the MOS capacitance decreases as the gate voltage is decreased.

Surface Inversion ($V_{GB} < V_T$): If the applied gate voltage is lowered below the threshold voltage (V_T), the semiconductor surface inverts its conduction type from n-type to p-type in our particular situation. The threshold voltage (V_T) is defined as the gate voltage at which the conductivity type of the surface layer changes from n-type to p-type because more holes have been attracted to the surface comparable to the number of electrons that existed at the surface at flatband. It demarcates the depletion region from the inversion region. Starting from flatband, as the gate voltage is lowered negative mobile carriers (electrons) are "pushed away" from the Si/SiO_2 interface, a positive space charge is exposed. We approximate this as a depletion layer in which we make the assumption that the layer is devoid of all mobile carriers. However, this is

only an approximation. What happens in reality is that the density of electrons decreases exponentially from the surface going into the bulk. An important fact pertinent to this discussion is that we assumed that system is in quasi-equilibrium, hence the law of mass action $p_o n_o = n_i^2$ is still valid. Thus at the surface, the number of electrons decreases as the applied voltage decreases. Correspondingly, the number of holes at the surface increases as the applied gate voltage decreases. At a particular voltage called the threshold voltage (V_T) the concentration of holes at the surface exceeds the concentration of electrons in the bulk. The conductivity type of the silicon surface is thus inverted.

2.4 Tunneling in MOS Capacitors

The quality of gate oxide directly determines the performance of an MOS capacitor. As the oxide thickness is reduced, the oxide becomes more susceptible to electron tunneling; the probability of electron tunneling also increases rapidly. Theoretically in classical mechanics, particles cannot penetrate through a barrier. However, in Quantum Mechanics it has been proven otherwise. This concept of penetration is called electron tunneling. There are two basic tunneling mechanisms: Fowler-Nordheim and Direct Tunneling. The mechanism is dependent on the oxide thickness where thicker oxides lead to Fowler-Nordheim tunneling and at thinner oxides direct tunneling takes place. Electron tunneling (both forms) can be primarily observed in SiO_2-Si interface when the oxide thickness is below 10 nm. Direct tunneling is observed at thickness below 4-5 nm [6, 7] and Fowler-Nordheim (FN) tunneling can be observed above 5nm thickness [42].

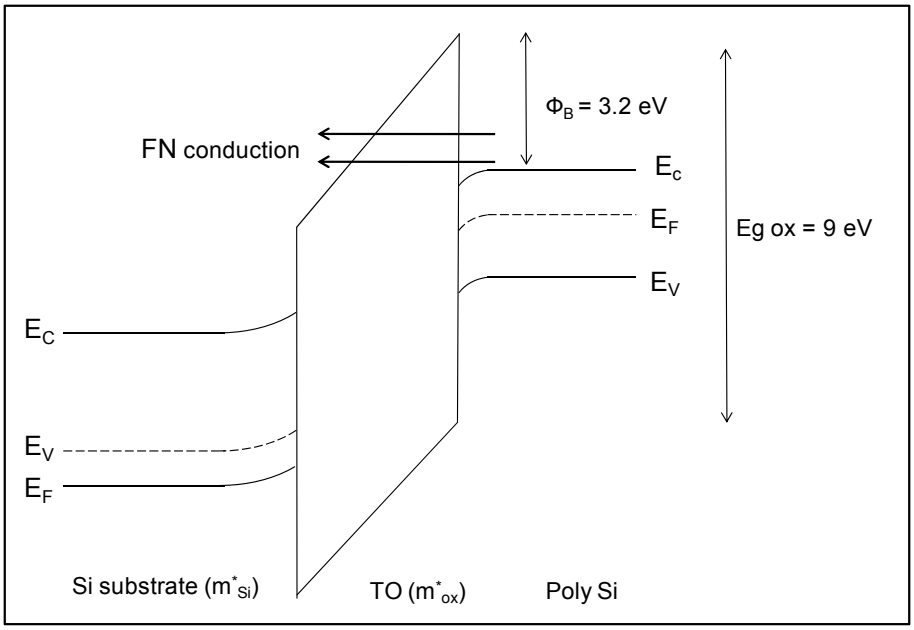

Fig. 2.4.1: Fowler-Nordheim tunneling regime [42]

At a given energy level, the FN current is the product of the carrier charge, the carrier velocity, the number of available carriers (product of number available of states and occupancy probability) and tunneling probability (the probability for a carrier to cross the oxide). The most common way to express the Fowler-Nordheim tunneling current density is to consider the approximation of a triangular barrier. Different expressions can be found in the literature [42]:

$$I_{FN} = \frac{q^2}{8 \cdot \pi \cdot h} \cdot \frac{E_{ox}^2}{\phi_B} \cdot \exp\left(-\frac{8}{3} \frac{\pi}{h} \left(2 \cdot q \cdot m_{ox}\right)^{1/2} \frac{\phi_B^{3/2}}{E_{ox}} \right)$$

ϕ_B is the barrier height, E_{ox} is the electric field across the oxide (the potential drop across the oxide divided by its thickness). Some others take into account the effective masses of Si and the considered oxide. FN tunneling exists in oxide thickness greater than 5 nm [42].

Direct Tunneling: This form of tunneling exists when the oxide thickness is less than 5 nm [42]. Unlike FN tunneling, direct tunneling occurs through a trapezoidal potential barrier. The barrier

height of the incident electron is higher more than the oxide potential drop thus the term direct tunneling [42].

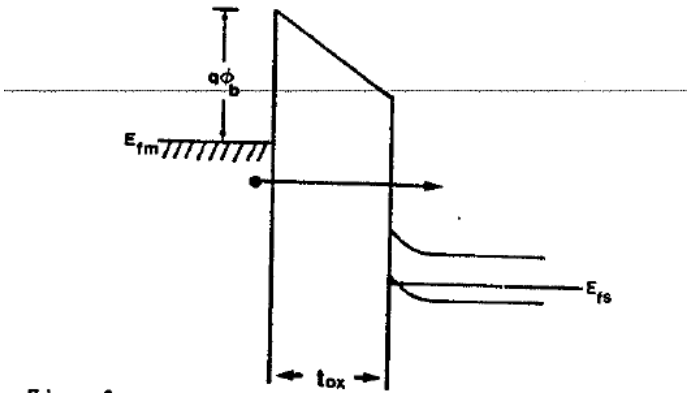

Fig. 2.4.2: Direct tunneling regime [42]

2.5 Kinetics of Oxidation of Nanocrystals

The primary method of creating or embedding Si nanocrystals in the SiO_2 is through ion implantation [8, 9]. The Si atoms are implanted into the SiO_2 and then thermal annealed. The annealing process "settles" the ions forming nanocrystals. The size and the density of the nanocrystals can be controlled by altering the ion energy and anneal temperature. This is a very easy way to achieve Si NCs in SiO_2.

In this project, the quantum dots are oxidized after they are mist deposited on to the substrate. A control sample (planar n-type Si wafer with native oxide etched prior) is also oxidized to determine the oxide growth; the oxide thickness is obtained using an ellipsometer. There is a caveat in using the control sample as reference. The control sample has a planar surface while

the quantum dots are 3-D in structure. Several models have been studied to estimate the dot size after being oxidized.

The structure of quantum dot is fundamentally different from planar silicon. Being 3-D is nature, there are different stress forces acting on the surface. This primarily has a retarding effect on the nanocrystal. The primary stress contributors are: stress normal to Si/SiO_2 interface and compressive stress in the bulk of the oxide. The former reduces the surface reaction rate while the latter is responsible for self-limiting oxidation [29, 32].

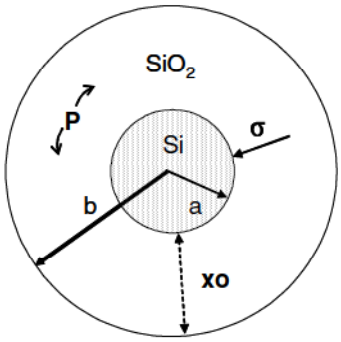

Fig. 2.5.1: Stresses on and in the composite nanocrystal [28, 32]

P is the tensile stress generated in the oxide shell; σ is the normal stress at the Si/SiO2 interface; a is the NC core radius; b is the radius of NC core plus the oxide shell. This figure elaborates the stresses and forces acting in and on the nanocrystal. The oxidation rate for a spherical Si NC can be expressed by [28]:

$$\frac{Nd(b-a)}{dt} = \frac{C^*}{\frac{1}{ks} + \frac{a^2}{b^2 h} + \frac{a(b-a)}{bD}}$$

Where a is the NC core radius, b is the radius of NC core plus the oxide shell; N the number of oxidant molecules incorporated into SiO_2 per unit volume of oxide grown. ($N=2.2\times10^{22}$

molecules/cm^3 for dry oxidation), ks is the surface reaction rate constant at the SiO_2/Si interface, h is the surface mass transfer constant of oxidant, D is the diffusivity of oxidant in SiO_2 and C* is the oxidant solubility in SiO_2 [28].

Chapter 3: OBJECTIVE

Nanocrystals are being keenly pursued because of its promise to offer higher storage density for memory applications. The objective of this project is study the electrical characteristics of MOS capacitors with Si nanocrystals embedded in the gate oxide. Mist Deposition is used to deposit nanocrystals on the oxide (SiO_2). The electrical characteristics (involving I-V and C-V) assist in explaining the role played by nanocrystals in the oxide. Blank wafers (control samples) are also oxidized and characterized to be used as reference while studying the I-V and C-V curves.

The secondary objective is to test the quantum tunneling phenomenon in the nanocrystals. It has been reported that tunneling assists in charge trapping or storage of electrons [1]. This can be directly studied using I-V and C-V characterization. Memory effect can be observed from hysteresis. A forward and reverse voltage sweep is performed along with stress tests to understand hysteresis.

Chapter 4: EXPERIMENTAL PROCEDURE

4.1 Device Fabrication

Si Nanocrystals are embedded into a basic Metal Oxide Semiconductor (MOS) Capacitor. The deposition technique used is novel to this study. As nanocrystals cannot be directly used, a colloidal solution is prepared. A density of .1mg/ml is chosen. The solution is then deposited using mist deposition over time lengths: 20 mins and 10 mins. A clean 4 inch Si wafer is used as a substrate on which the deposition takes place. Four different quarters are cut and nanocrystals are deposited on the substrate simultaneously. Each wafer is oxidized for different times with one sample (quarter wafer) left unoxidized. The oxidization takes place in a dry oxidation furnace at 800 °C with times for each of the wafer quarter: 5 min, 30 mins, and 90 mins for three of the wafer quarters. This also oxidizes the nanocrystals shrinking the overall diameter of the crystals. Ellipsometry was used to confirm the oxide thicknesses: 5 min (2.14 nm); 30 min (4.63 nm); 90 min (8.34 nm). Depending on the oxidation time, the nanocrystals may exist from 1-3nm for shorter oxidation time to almost nonexistent in longer oxidation time (90 min; 8.34 nm). The purpose is also to see the effect of nanocrystals scarcely embedded in oxide. This helps in understanding the extent of nanocrystals' effect on I-V and C-V shifts.

After the oxidation, metallization of the wafer takes place using an e-beam evaporator. Prior to rear contact deposition, the native oxide is removed with diluted HF and wiped using a cotton swab. Blank deposition takes place at the bottom of the wafer for the sake of contact consistency with the measurement probe. Aluminum is again used to make contacts on the top of the wafer with shadow masks in place. The shadow masks have three different contact area sizes: 1.98×10^{-2} cm^2; 1.11×10^{-2} cm^2; 4.95×10^{-3} cm^2; large, medium and small respectively.

4.2 Electrical Measurements

As the study involves electrical characterization, Current-Voltage (I-V) and Capacitance-Voltage (C-V) are essential. C-V was carried out using HP 4192A Low Frequency impedance analyzer (100 kHz) and I-V was performed on Keithley 237 high voltage source. I-V and C-V hysteresis is also performed to complement I-V, C-V curves and to confirm the findings. A negative to positive voltage is performed and immediately a positive to negative voltage during which a shift is observed. The extent of the shift in curves tells the charge trapped or stored in the nanocrystals.

C-V measurement provides important information such as accumulation capacitance, flat-band voltage and trap behavior. The electrical characterizations are also done across contact area sizes: 1.98×10^{-2} cm^2; 1.11×10^{-2} cm^2; 4.95×10^{-3} cm^2, large, medium and small respectively.

Chapter 5: RESULTS AND DISCUSSION

The purpose of this project is to study electrical characteristics of MOS capacitor with Si QDs embedded in SiO_2. The oxide characteristics can be understood by performing electrical characterizations. The obtained results will be compared with results from various literary sources confirming the role of quantum dots embedded in the oxide along with the presence of tunneling, and the role control and gate oxide.

After the quantum dots are deposited on the substrate, the samples are oxidized for different times at 800 °C: 5 min, 30 min, and 90 min (oxide thicknesses of 2.13 nm, 2.46 nm and 8.34 nm, respectively, for planar Si control samples). Initial oxide growth and times were calculated. Control samples were placed simultaneously during oxidation to check for oxide thickness. An important point to keep in mind is that the quantum dots "tangentially" adhere to substrate. As oxidation takes place on the surface of the quantum dot, the control oxide (in between gate and the Si QD) and tunnel oxide (in between Si QD and the substrate) are formed in situ.

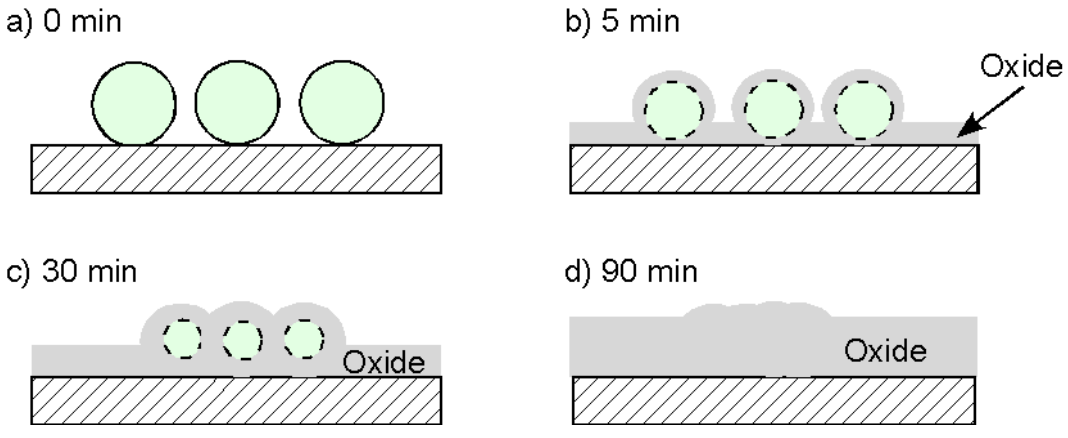

Fig. 5.1: Schematic of Quantum Dots oxidized for different oxide times

5.1 Oxide time relation with Current and Capacitance Characteristics

Basic I-V and C-V curves are first obtained for blank samples and samples with QDs embedded. No Capacitance-Voltage plots can be obtained for the 0 min oxidation sample due to conductive properties of the QDs. Looking at the current-voltage plot (Fig 5.1.1) of the (0 min) sample, it can be confirmed that the quantum dots are perfectly conducting. The current initially close to zero shoots up as the voltage increases to a point where the I-V system steps in clipping of high currents. The plot confirms linear behavior of the QDs (see Fig 5.1.1).

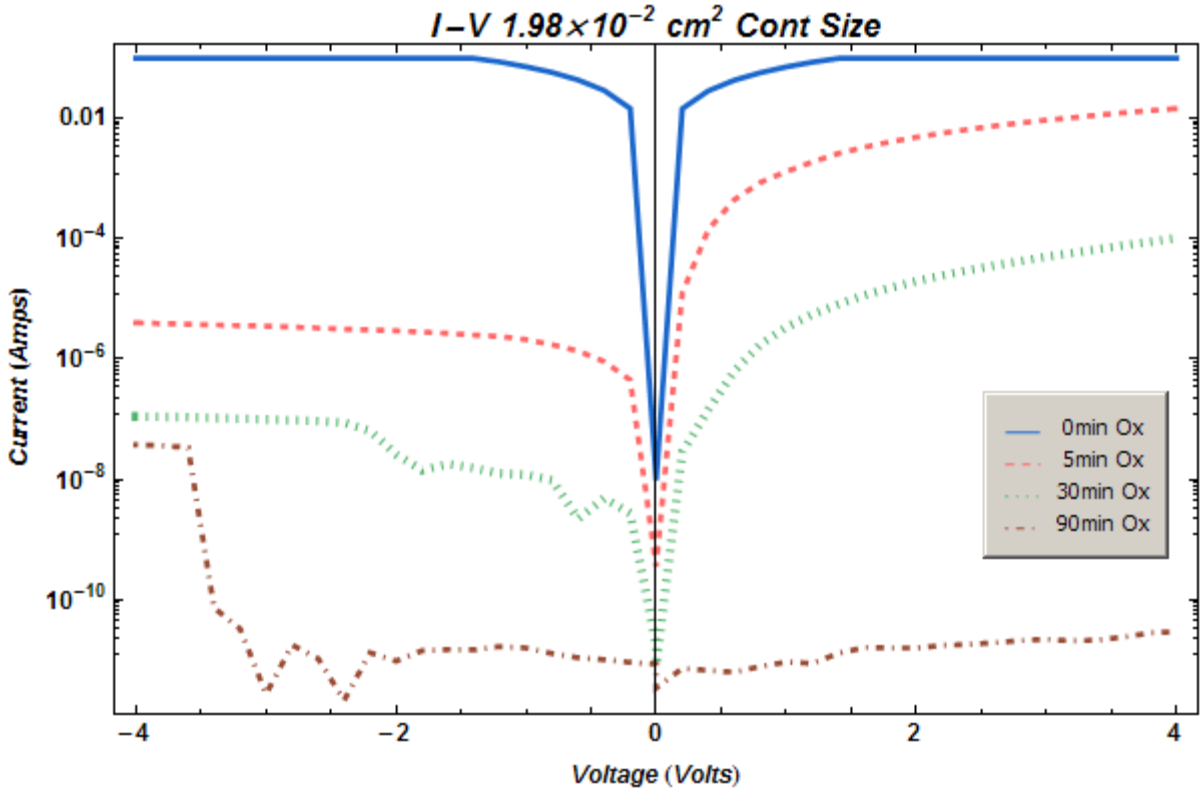

Fig. 5.1.1: I-V Characteristics across oxidation times

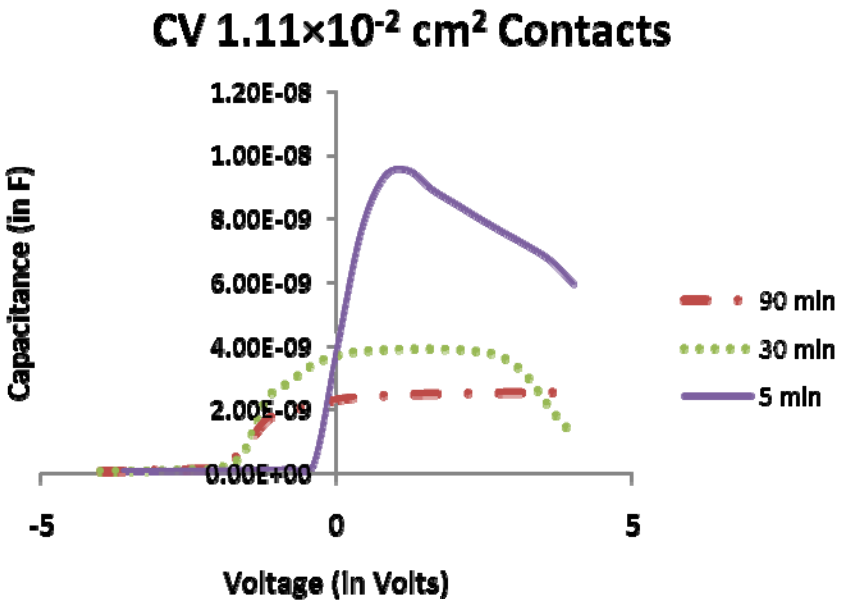

Fig. 5.1.2: C-V Characteristics across oxide times

As the oxidation time increases, the surface of the QD is oxidized. For the 5 min oxidation, the device shows both "capacitor-like" C-V and "diode-like" I-V behavior. At this point a safe assumption can be made that the QDs are oxidized (despite retarded oxidized growth; see Sect 2.6) and the QDs are playing a role by affecting the electrical characteristics. The existence of C-V curves indicates oxidation of the surface. However as the device reaches accumulation, the capacitance suddenly drops; This can be attributed to tunneling that exists through the oxide. As studied previously, the QDs oxidize much slower than planar Si sample, the oxide thickness surrounding the Si core shell is in the direct tunneling regime [6, 7] i.e. less than 5 nm [42]. The sudden capacitance drop means existence of a conductive pathway [7] through the oxide and QDs [7]. The conductive pathway is initially through the oxide (tunneling) and later the charged QDs resists electron transition reducing the current flow [7].

From the C-V plot for 30 min (Fig. 5.1.2) oxidation sample, the device exhibits near-MOS Capacitor like behavior. The operation regimes i.e. Inversion, Depletion and Accumulation can be distinctly observed. This confirms that the QDs were oxidized further and the overall oxide thickness increased. In comparison with 5 min oxidation sample, the accumulation capacitance for 30 min oxidation sample is much lower; this is concurrent with the expected: capacitance is inversely proportional to the oxide thickness. Capacitance can be given by:

$$C_{ox} = \frac{\varepsilon_r \varepsilon_0 A}{t_{ox}},$$

where ε_r is the relative permittivity of the oxide, ε_0 is the dielectric constant, t_{ox} is the oxide thickness and A is the area of the capacitor (contact area = capacitor area in our case).

If the plot for the 30 min sample is closely examined, there is drop in capacitance in the accumulation region (Vg > 3 V). This concurs with 5 min oxidation sample of the existence of tunnel currents. The capacitance drop due to tunneling is again because of the tunnel oxide thickness which is in the direct tunneling regime [42]—less than 5 nm; this means that the tunnel oxide thickness is less than 5 nm. Despite the QDs being conductive, there is a striking difference in the I-V characteristics of the control (Blank) vs. QD samples (Fig 5.1.4 shown for 30 min case). The oxidized QD sample conducts less electricity than the blank sample. This can be attributed to loss of tunneling pathways as the QDs trap electrons [6]. The trapped electrons in the QDs prohibit charge transfer or conduction leading to reduced current [6] (see Section 5.3).

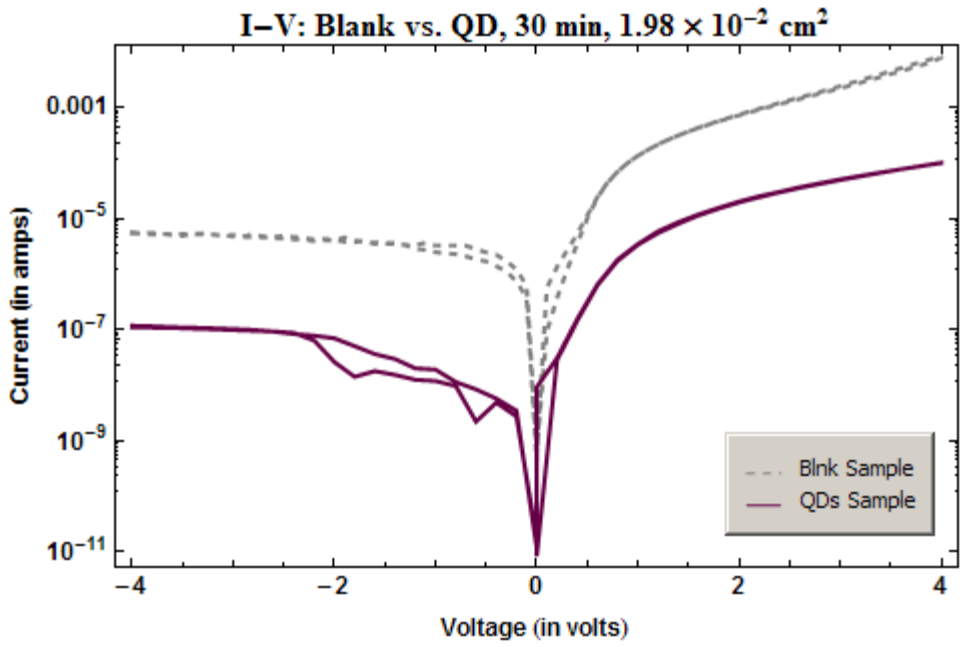

Fig. 5.1.3: I-V characteristics of Blank (Control w/o QDs) vs. QD sample for 30 min oxidation

The 90 min sample confirms that the QDs are completely oxidized. The complete MOS capacitor like behavior (Fig 5.1.2) and lack of significant currents (from the I-V characteristics, Fig 5.1.4) confirm this claim. As the control sample is planar and the oxide growth is higher (~ 7.4 nm), thinking in relative terms, the QDs are completely oxidized and swamped by the local oxide growth completely. In comparison with blank (control) sample, where low currents are expected, the QDs shows similar current range (Fig 5.1.6). Breakdown voltage was obtained for the sample (Fig 5.1.6). The breakdown voltage is indicative of MOS capacitor like behavior. At 90 min oxidation time, it is evident that most if not all the QDs are oxidized, shown the C-V and I-V curves along with breakdown voltage (Fig. 5.1.6) for Blank (control) and QD samples.

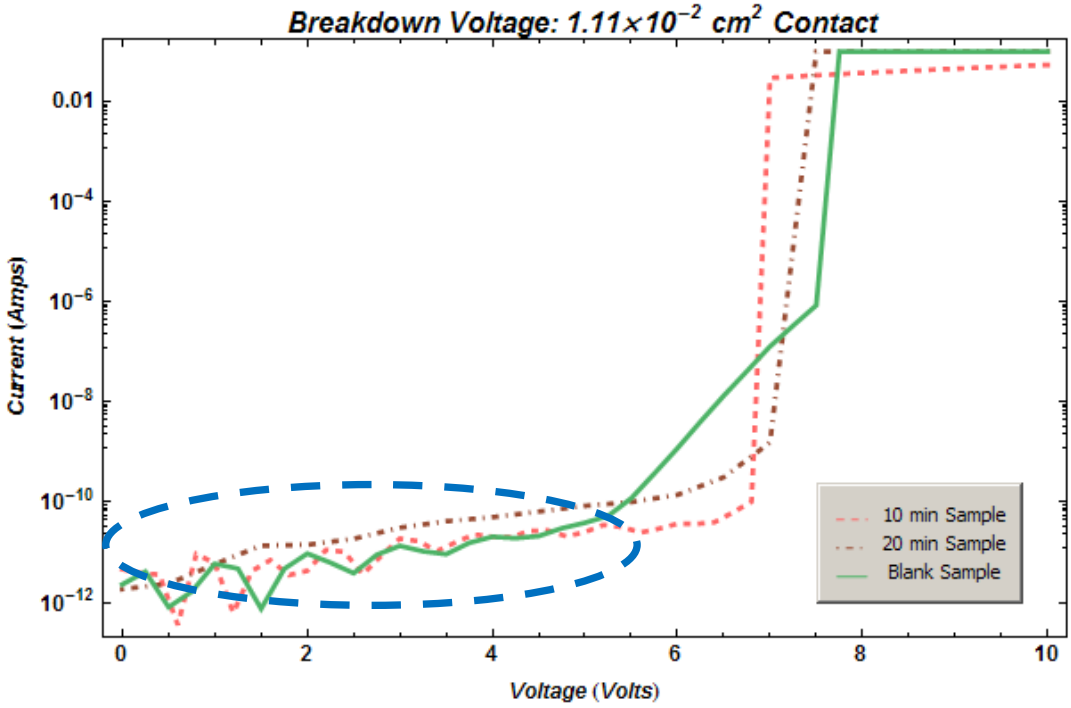

Fig. 5.1.4: Breakdown voltages for 90 min oxidation for Blank Sample, 10 min and 20 mins deposition

5.2 Tunneling dependence on tunnel oxide thickness

Tunneling current has a direct effect on electrical measurements. Tunneling current is responsible for capacitance drop as noticed in the Fig. 5.2.1. A wafer is "pre-oxidized" oxidized thermally for 5 mins (2.14 nm) at 800 °C and Si QDs were deposited after oxidation. The deposited Si QDs are not oxidized again. The wafer has a tunnel oxide (2.14 nm) but no control oxide. The "pre-oxidized" wafer has a planar surface and the oxide growth complies with the calculated oxide growth times.

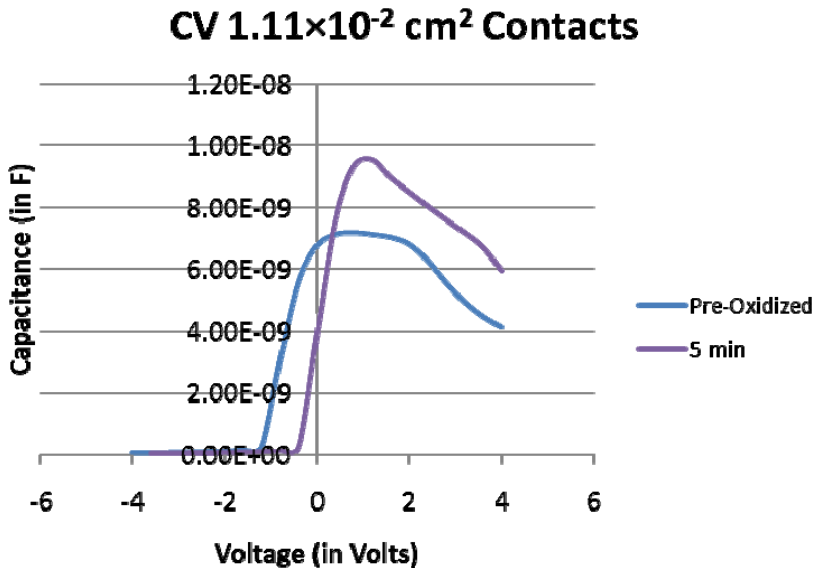

Fig. 5.2.1: C-V of Pre-Oxidized and 5 min oxidized QDs

Figure 5.2.1 has the C-V plot of pre-oxidized and 5 min oxidation sample. The accumulation capacitance is higher for 5 min sample than the pre-oxidized wafer despite having the same oxidation time. As the capacitance is inversely related to the oxide thickness (— , higher capacitance of 5 min oxidation sample suggest lower oxide thickness. This agrees with the proposed case of slower oxide growth of Si QDs [29, 31, 32].

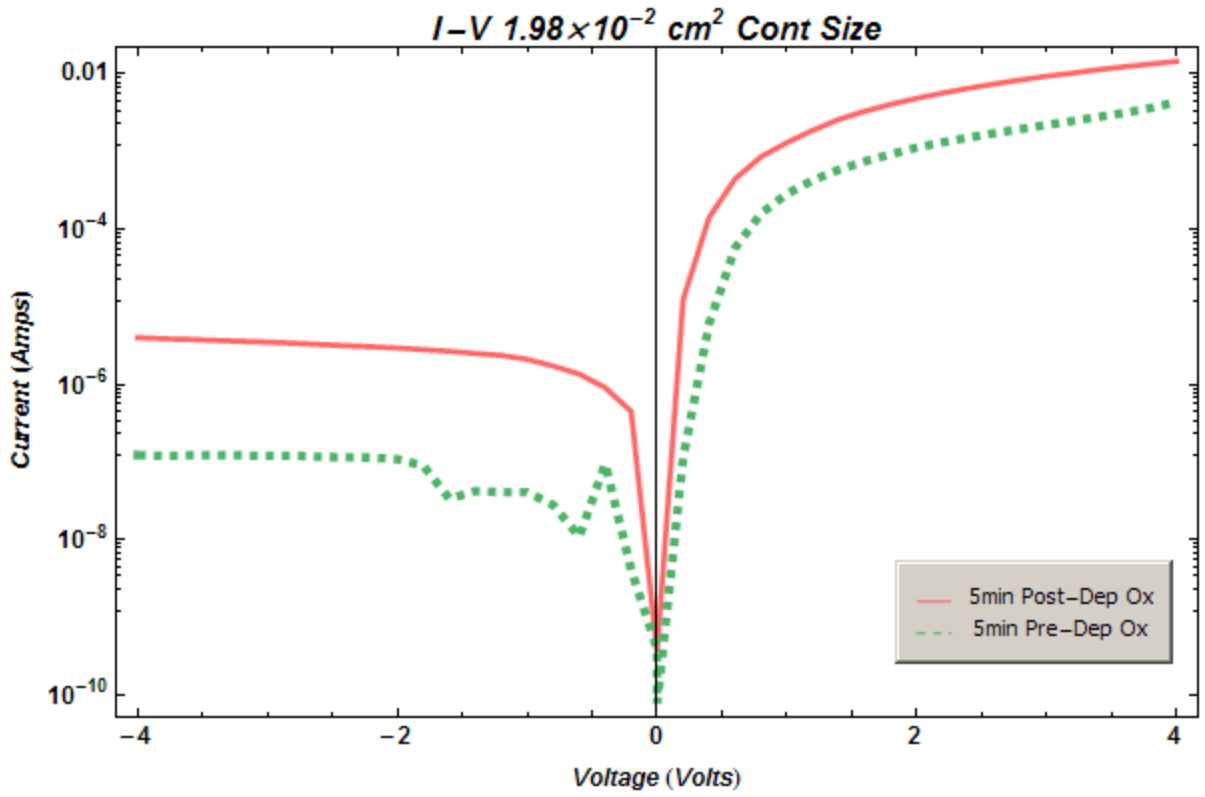

Fig. 5.2.2: Current dependence on tunnel oxide thickness for pre-oxidized (Pre-dep) and 5 min oxidation sample (Post-Dep)

I-V characterization was also performed for pre-oxidized and 5 min sample (Fig. 5.2.2). It is noticed that the pre-oxidized oxide (dotted line; 5 min pre-dep oxidation) has lower current than the 5 min oxidation sample (straight line; 5 min pos-dep oxidation). It is reported that tunneling current is dependent on the tunnel oxide thickness with inverse proportionality being observed. As this goes with the proven case that pre-oxidized sample has larger tunnel oxide thickness (2.34 nm) than the 5 min oxidation sample, the observed plot in the figure (Fig. 5.2.2) is credible.

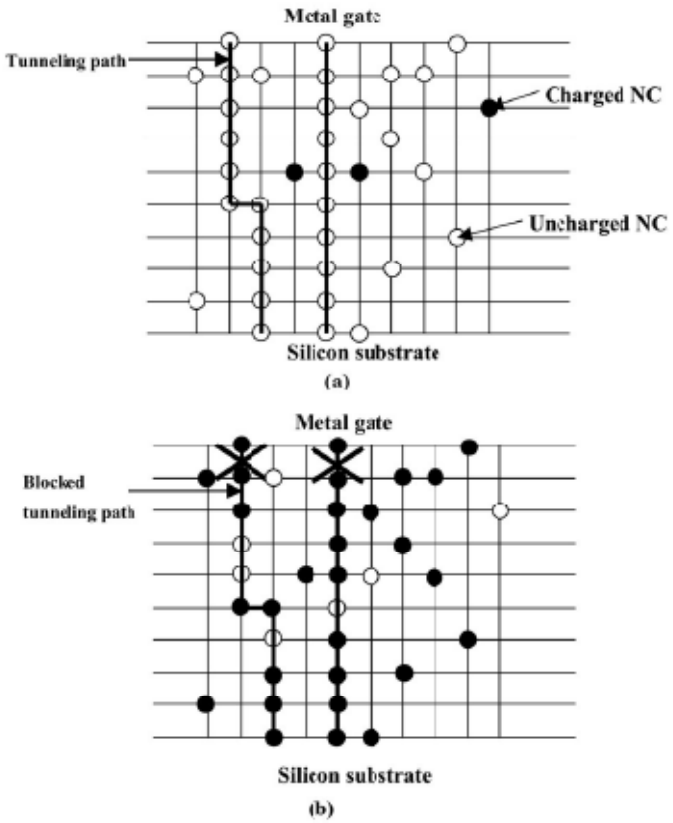

Fig. 5.2.3: Schematic illustration of conduction pathways through QDs [6]

The effect of charge/discharge of Si QDs on the current conduction can be clearly illustrated with Fig. 5.2.3. Electron tunneling takes place between the adjacent uncharged QDs [6]. Several such QDs form tunneling paths linking the metal gate to the Si substrate (Fig. 5.2.3a). The charging and discharging of the QDs takes place under the influence of voltage. If some QDs in a tunneling path are charged up, then the tunneling path is blocked by the charged QDs. The current path thus disappears (Fig. 5.2.3b). The current conduction of the MOS structure is determined by the tunneling paths [6, 7]. A direct observation of this is the comparative I-V characteristics of control (blank) and QD sample (Fig 5.1.3 and 5.2.4). Therefore, the change of the current conduction is only the reflection of the disappearing/appearing of the tunneling paths due to the charge/discharge in the QDs [6].

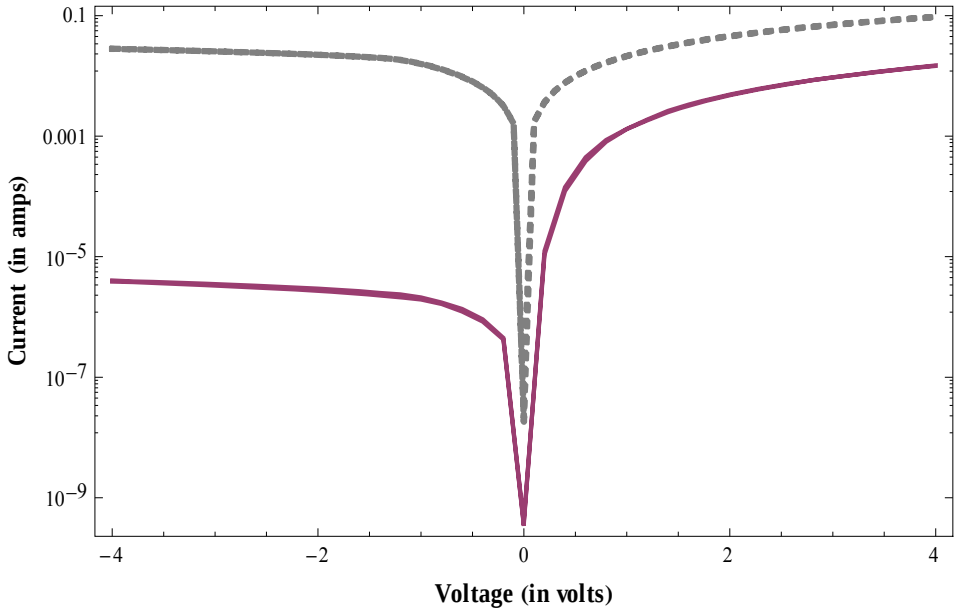

Fig. 5.2.4: I-V plot for Control (w/o QDs; Dotted line) and 5 min QD oxidation sample (thick line)

5.3 Memory Effect

A primary method of observing memory effect is through hysteresis. Hysteresis is observed when the influence of the previous "history" of a body on its subsequent response by exhibiting a lag. Simply put, a system with memory has hysteresis. Hysteresis measurements were performed for all the samples (except 0 min oxidation) for this project. Depending on the oxide thickness and existence of QDs hysteresis was observed. Nanocrystal based memory is gaining much attention due to its ability to store charge at very low currents [1, 6, 7]. One of the secondary purposes of the project is study this memory effect in nanocrystals. Hysteresis measurement involves performing forward and backward voltage sweeps. Hysteresis in a MOS capacitor can be observed in the depletion region. The primary target samples to observe this is 5 min and 30 min because QDs in these samples are partially oxidized and accommodate tunneling (and QD

charging) unlike 90 min oxidation samples. 90 min oxide sample is of no interest as it already exhibits MOS Capacitor like characteristics confirming complete oxidation of the QDs.

Hysteresis measurements were performed on the 5 min sample. There is no observable hysteresis for the 5 min sample due to very thin tunneling oxides. The plot in the accumulation shows drop in capacitance both for forward and reverse sweeps. As explained in the previous section (5.2), the drop can be attributed to tunneling that is present in this operative regime i.e. accumulation. The accumulation region is crucial to hysteresis (for n-type), as the electrons accumulate near the dielectric. This has been explained in the earlier section.

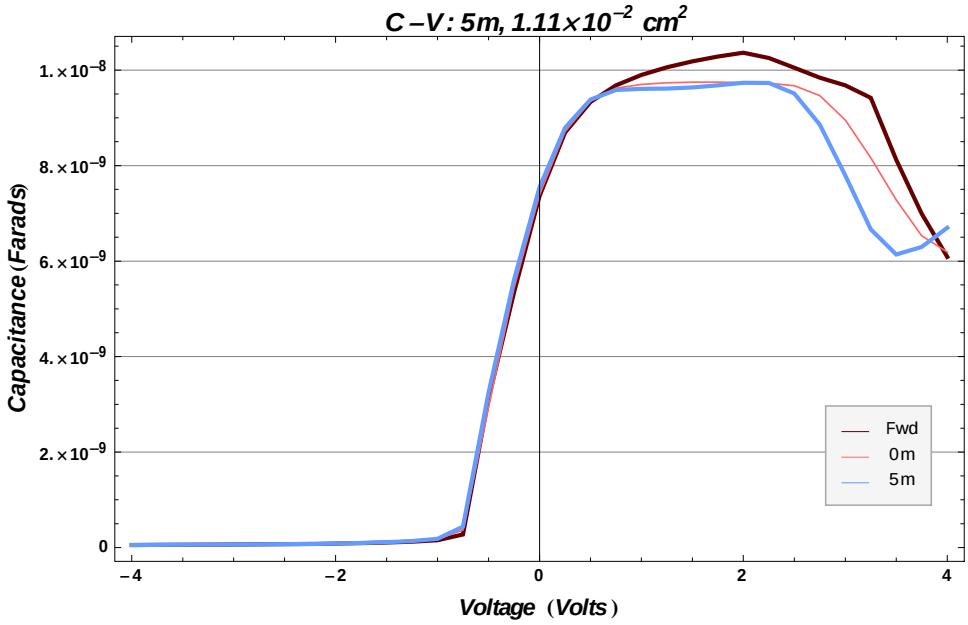

Fig. 5.3.1: Hysteresis measurement for 5 min oxide sample

In the accumulation regions, the QD pathways assist in tunneling [6, 7]. Capacitance drop can be directly attributed to tunneling—direct tunneling. Both 5 min and 30 min samples lie in the direct tunneling regime. The tunnel oxide for 5 min oxidation sample is thin enough to facilitate direct tunneling. It is easier for electrons to tunnel through the oxide than pass through QDs. With the

existence of high tunnel currents in the direct tunneling regime, any existence of hysteresis or memory effect can be negated.

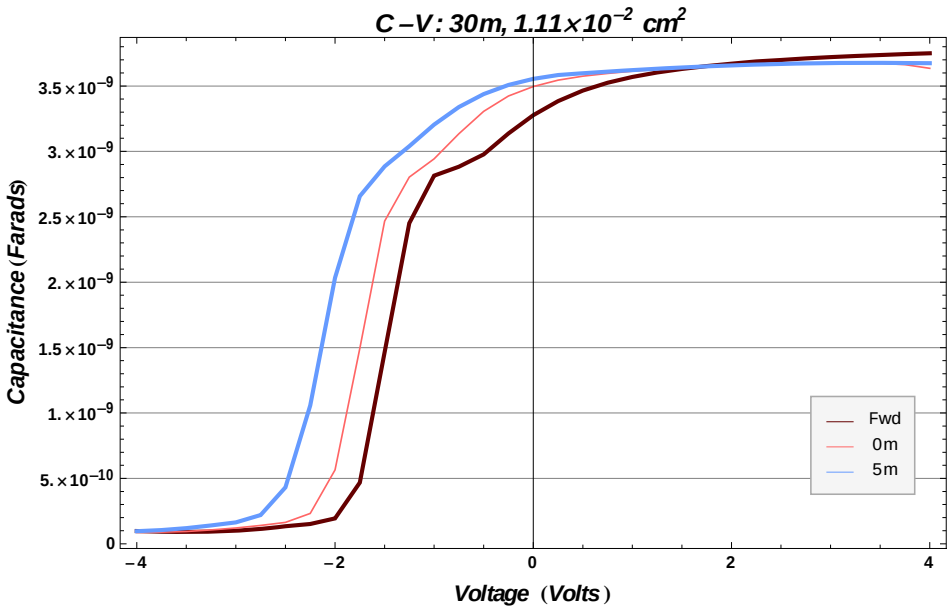

Fig. 5.3.2: Hysteresis for 30 min oxidation sample

The 30 min oxidation sample shows near perfect hysteresis. There is a noticeable shift of the curve (reverse sweep; accumulation to inversion) in the depletion region. This directly indicates charging of the QDs (Fig 5.2.4). This hysteresis result is concurrent with results obtained from literary sources [1, 6, 7, 8, 9] confirming charging of QDs in the oxide.

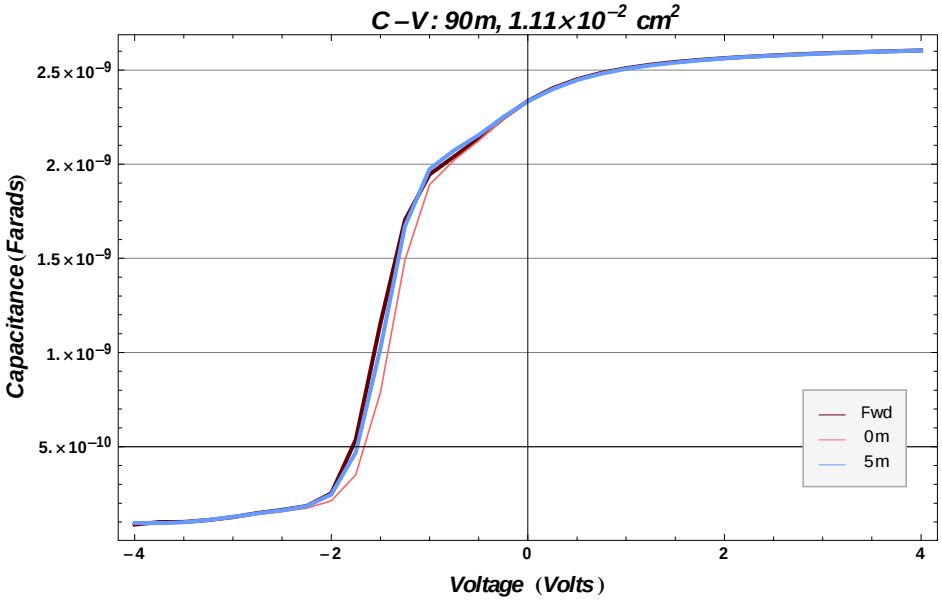

Fig. 5.3.3: Hysteresis for 90 min oxidation sample

Hysteresis measurements were performed for 90 min oxidation sample. There is no observable hysteresis for this sample. In previous discussion, it has been confirmed (through electrical characterization) that the QDs are mostly (if not completely) oxidized. Lack of any hysteresis shifts in the curve confirms the absence of QDs, indicating that they were completely oxidized. Lack of hysteresis is also an indication of lack of mobile charge present in the oxide which can exist during oxide growth. This affirms the authenticity of hysteresis measurements in other samples (primarily 30 min oxidation).

5.4 Stress Measurements

Voltage stress measurements were performed on the samples. The device is first swept forward (-4V to 4V; inversion to accumulation). As soon as it reaches 4V, a 4V current is passed through the device for a selected period of time: 1 min, 2 mins, 3 mins, and 5 mins. A reverse sweep (4V

to -4V; accumulation to inversion) is performed immediately after the selected time period. A hysteresis shift is observed for each stress measurement. However, the shift saturates after 3 mins. Looking at Fig 5.3.1, the 5 min (dotted) and 3 min curves overlap. The hysteresis observed in 0 min sweep indicates the charging of QDs due to charge trapping. The subsequent shifts are indicative of presence of slow traps [38-41].

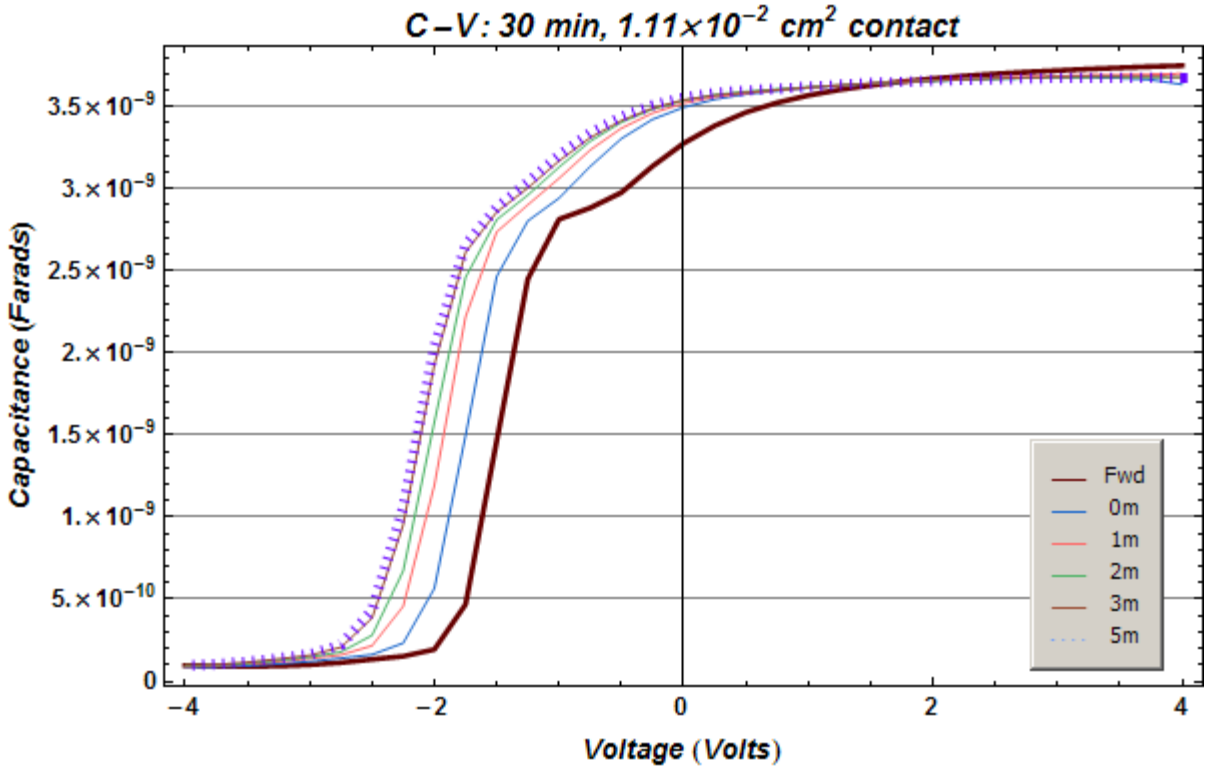

Fig. 5.4.1: Progression of hysteresis curves under time stress

Chapter 6: SUMMARY

Si nanocrystals show a strong potential as a future of flash memory. Extensive research is underway to understand the performance, fabrication and memory characteristics of Si NCs. A proper deposition technique has to be devised in order to commercialize this nanocrystal memory technology. Ion Implantation appears to be the deposition technique of choice for Si nanocrystals; CVD has also been used, albeit to a lesser extent. Mist deposition is used as vehicle for depositing the colloidal Si QD solution. In this project, characterization of MOS capacitors embedded with Si QDs has been performed. The main novelty of the project is the oxidation dependent size variation of Si QDs which is shown using electrical characterization, I-V and C-V. Memory effects, through hysteresis measurements, are observed and matched with the results from other studies.

The kinetics of Si QD oxidation growth is also studied. Not much literature or information is available in this area. Si QDs oxidize slower than planar Si primarily due to interfacial and compressive stresses. The slower oxidation of Si QDs has been demonstrated with the use of C-V measurements, where capacitance is lower for pre-oxidized Si wafer with QDs than the capacitance of oxidized wafers post QD deposition for the same time. Tunneling current dependence on tunnel oxide thickness has also been demonstrated.

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