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STUDIES OF THIN SILICON OXIDES AND HIGH-K MATERIALS FOR GATE DIELECTRICS IN METAL-INSULATOR-SEMICONDUCTOR STRUCTURES

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ABSTRACT

The development of a gate stack system (dielectric, electrode, and their compatibility with plasma etching processes and the scaled complementary metal oxide semiconductor [CMOS] integrated circuit [IC] process flow) presents major materials and processing challenges as IC industry approaches the sub-100 nm technology generation by the year 2006 and beyond. The continually shrinking gate-oxide thickness, necessitated by the requirement of higher gate capacitances for high drive current, results in direct tunneling and excessive leakage currents in metal-oxide-Si field-effect transistors (MOSFETs). To obtain high gate capacitance and inhibit tunneling, relatively thick insulators of high dielectric constants (high-k) are needed in place of gate oxides in MOSFETs. The research in this thesis will cover a series of issues related to the scaling of submicron devices.

In the first part of this thesis we examined the plasma-process induced damages in thin-gate oxide MOSFETs and its identification and characterization through electrical measurements. We found that, with the aggressive shrinking of oxide thickness around and below 50Å, conventional transistor parameter measurements such as threshold voltage (V_{th}), transconductance (G_m) and subthreshold swing (S) failed to resolve differences in devices with variable degree of plasma-process induced damage. We demonstrated that in these thin-oxide MOSFETs the gate leakage current (I_g) is the only transistor parameter which can detect plasma-processing induced changes in oxide charge and interface states. These results are interpreted in terms of the strong dependence of I_g

on trap-assisted tunneling which dominates conduction in oxides within the studied thickness regime.

In subsequent studies, thin-gate oxide MOS capacitors and MOSFETs were subjected to Fowler-Nordheim (FN) stress and Hot-Carrier (HC) stress, respectively, and tested with deep level transient spectroscopy (DLTS) to monitor trap generation during plasma process as well as during device operation. Charge states in SiO_2 and Si/ SiO_2 interface states were observed under different FN stress temperatures and their causes were attributed to carrier injection during the stress. For the first time bulk Si defects are reported to be generated by FN stressing on thin gate oxides which raises a serious concern of carrier mobility in channel region of corresponding MOSFETs. During HC stress, we found that HC stress in thin-oxide transistors promotes interface damage while oxide charge trapping becomes less significant. The observed degradation is no longer localized near the drain side.

In the second part of the thesis, we focus our studies on the electrical properties of high-k gate stack systems. Different high-k dielectrics, $SrTa_2O_6$, $ZrSiO_4$, ZrO_2 and HfO_2 prepared by liquid source misted chemical deposition, and TiO_2 prepared by chemical vapor deposition were used as the insulators in metal-insulator-Si (MIS) capacitors which were examined using CV/IV and DLTS. It is revealed, for the first time, that the accumulation capacitance of the MIS with the high-k dielectric is strongly dependent on the measuring temperature and frequency. The capacitance dependence on temperature in the MIS with the high-k dielectric is seen to proceed in an opposite direction to that of MOS capacitors while the capacitance dependence on frequency in the MIS is

significantly larger than that of MOS capacitors. An equivalent circuit model is proposed and the discrepancy is explained by the impedance contributions from a thin and low quality interfacial layer, between the high-k dielectric and the Si substrate, often inadvertently incorporated during the high-k dielectric growth. These observations call for efforts to be put towards the careful evaluation and possible elimination of this low-quality interfacial layer from gate dielectric stacks.

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Chapter 1

An Overview of Metal-Oxide-Semiconductor (MOS) Device Scaling: Past, Present and Future

1.1 Miniaturization in CMOS

Semiconductor industry has continued to prosper and to foster the growth of multiple industries ever since early 1970s. It has grown at a very fast 15% compounded annual growth rate (CAGR), with semiconductor sales reaching $160B in 1998, representing 16% of the total electronic equipment sales ($900B). Without any doubt, semiconductor industry has become the main driving force for the new information age. At the center of this sustained growth, resides the unique factor that has made the semiconductor industry successful: decrease in device feature size have provided improved functionality at a reduced cost. The first commercial microprocessor, the 4004 invented by Intel in 1971, contained a mere 2300 transistors and performed about 60,000 calculations in a second. Three decades later, and at the same or even lower cost, Intel Pentium III and AMD Athlon microprocessors run at 500M-1G Hz, have more than 22 million transistors performing hundreds of millions of calculations each second [1].

Complementary metal-oxide-Si (CMOS) technology has become the dominant very-large-scale-integrated (VLSI) circuit technology and its dominance has permitted the industry to focus primarily on scaling. Device linear features have indeed decreased at a rate of ~ 70% every three years throughout most of the industry's relatively short history. Moreover, acceleration to a 2-year cycle has been experienced in the most recent years. Cost per function has simultaneously decreased at an average rate of ~ 25-30%/year/function [2]. In 1965, Gordon Moore, the founder of Intel Inc., predicted that the number of transistors on a chip would quadruple every 36 months. He further updated his prediction in 1985 and reduced the cycle to 24 months. It is interesting how CMOS scaling has strictly followed this law for the last thirty years of its development.

The promise of CMOS scaling is to speed up the device while at the same time increase the integration density to lower the overall cost. This is made possible by continuous miniaturization of transistor's dimensions, e.g. shorten the channel length to reduce the carrier traveling time from drain to source, reduce the gate oxide thickness, minimize the transistor area, etc. This is also made possible by the development of many new processing technologies, such as extreme UV, e-beam and X-ray lithographies. Over the years, silicidation processes were added to CMOS processing sequence so as to lower the sheet resistance of the poly-Si electrode and source/drain regions. Lightly-doped drain (LDD) and double diffused drain (DDD) structures have been developed to improve the transistor robustness to hot carrier induced degradation [3]. Barrier metals and W-Plugs were added to the Al-alloy interconnection process flow for improved reliability.

According to the Semiconductor Industry Association (SIA) predictions, the expected transistor gate length reaches 250nm (50Å oxide thickness) in 1998-1999, 180nm (25 Å oxide thickness) in 2001, 130nm in 2004 and eventually 100nm in 2007. The first two phases have already been achieved, whereas the shorter gate lengths are currently within reach. The reduction of transistor channel length reduces the carrier traveling time between source and drain, thus improves the device speed. Meanwhile, the reduction of gate oxide thickness is necessary to maintain the device scaling, e. g. threshold voltage and capacitance. However, it appears that the fundamental limits of the materials constituting the building blocks of the planar CMOS process will be reached soon, and the physics behind device operation will begin to change to accommodate quantum physics effects. Present research focuses on two important questions. The first question is what is the impact of ultra-thin gate oxide (<50Å) on device fabrication and operation? The second is, given the role of the oxide in device characteristics, what is the ultimate limit of oxide thickness reduction?

1.2 Ultra-thin Gate Oxides: Properties, Issues, Problems and Scaling Limitations

Two of the most significant properties that are inherent to the ultra-thin gate oxides are the direct tunneling current and a new failure mechanism referred to as soft-breakdown. In the metal-oxide-Si (MOS) structure with 50Å or above oxide thickness, when a constant current is injected into the oxide, the conduction mechanism is Fowler Nordheim (FN) tunneling. In this mechanism electrons are injected across a triangular barrier at the SiO_2-gate or SiO_2/Si substrate [4, 5]. FN tunneling usually occurs during

device fabrication, especially during plasma based depositions or etching processes. Damage to devices induced by FN current flow is very well studied [6]. However, below 50Å, a new type of conduction mechanism in the oxide comes into play. This mechanism is direct tunneling which is well above the level of Fowler-Nordheim tunneling at similar applied biases. This is because the film thickness is reduced to the point at which electrons can tunnel directly from cathode to anode and no longer require the effective barrier thinning that is necessary for the F-N conduction mode [7, 8].

The large tunneling current poses a fundamental limitation on the scaling of oxide thickness. While it may be at a negligible level compared with the ON-state current of a device, it will directly have an effect on the overall standby power. For a total active gate area of $0.1cm^2$, chip standby power limits the maximum tolerable gate leakage current to the order of $1\text{-}10A/cm^2$, which occurs for gate oxides in the range of 15-18Å [9]. Moreover, the quantum tunneling current, especially in the large area devices that are often used in process control and reliability circuits may totally obscure the leakage from breakdown. Also, the large gate current renders some characterization techniques, such as threshold voltage, transconductance measurement, and even quasi-static capacitance-voltage (CV) measurement less accurate and less reliable [10].

In spite of the above disadvantages associated with thin oxides, it is also found out that using ultra thin oxides comes with some advantages too. For example, it is observed that plasma induced damage in the ultra-thin gate oxide transistor is much less severer than that in thicker gate oxide transistor. It is well known that the plasma induced damage arises from the stressing of the gate oxide, thereby resulting in increased

interface defect density, in shifted device parameters and in degraded device density [6]. In the past, it has been firmly established that damage from plasma processing increases with the reduction of gate oxide thickness, from 20nm to 8nm [11], or to 4nm [12]. When the gate oxide is reduced beyond these thicknesses, however, better gate oxide reliability is reported as a result of the direct tunneling current. It has been suggested that plasma charging damage will no longer pose a severe threat to the thin gate oxide once it is scaled below 3 nm [13]. A possible explanation here is that injected electrons gain energy as they travel in the oxide and they need to travel a certain distance beyond which their energy is high enough to create charge-trapping defects. An ultra-thin oxide may not be thick enough to accommodate such a distance. Also in a very thin oxide an electron may travel ballistically (without scattering or collisions) [14,15]: this means that there will be less collisions between electrons and atoms, and therefore fewer number of generated defects. Moreover, some of the charge trapped in these few defects will be easily swept off by the high electric field in the gate oxide during the process [16]. However, we should point out that at this point the results are not yet conclusive, recent reports indicate that high level of plasma damage is observed in 2nm-thick oxides.

Soft-breakdown is another issue that is unique to ultra-thin oxide MOS devices. It is observed as an increase in the low-level leakage current, but not as a catastrophic failure [17,18]. It becomes more prevalent the thinner the oxide and for oxides stressed at lower voltages. An ultra-thin oxide device (25Å) exhibiting soft-breakdown shows no abrupt voltage drop, no abrupt current jump, even no increase in low-voltage leakage current. The only indication of the soft breakdown is an increase in gate noise [19]. The

device with soft breakdown can operate normally in some applications, but soft breakdown could be detrimental in any analog or flash memory system [20]. Also, due to the lack of a sharp transition in the increasing leakage current, it is often difficult to define soft-breakdown and distinguish it from catastrophic breakdown in ultra-thin gate oxides. Combining this with the high tunneling leakage, the ultra-thin gate dielectrics under temperature and bias stressing show increase in stress-induced leakage currents (SILC) and soft-breakdown characteristics well in advance of the true hard breakdown/wear-out. The implications being that there are no well defined criteria for the gate-dielectric failure in the sub 50Å thickness range.

There are also other issues related to the ultra-thin oxides. Among these issues is the standard formula for oxide lifetime prediction which would no longer provide accurate estimate on the mechanism that causes the oxide to fail. One test on the low SILC measurement leads to the conclusion that the reliability of 2.2 nm gate oxide at 25°C has reached an unacceptable level.

All of the above issues and problems associated with ultra thin gate oxides have resulted in the presently accepted limit for the CMOS scaling of 100 nm gate length, or 15 Å gate oxide thickness. Further investigations on this limitation are currently in progress utilizing gate oxides as thin as 13 Å [21]. These investigations include "dynamic' gate tunneling leakage, loss of inversion layer charge, carrier mobility degradation and the temperature dependence of all these variables.

1.3 High-k Materials for Gate Dielectrics in MOS Structures

Traditional scaling, which has been at the heart of the semiconductor industry for the last 30 years, is indeed beginning to show the fundamental limits of the materials constituting the building blocks of the planar CMOS process. However, new materials can be introduced in the basic CMOS structure to replace and/or augment the existing ones to further extend the device scaling approach. Since the assimilation of these new materials into the modified CMOS process gives the device physicist and the circuit designer improved electrical performance similar to the historical trends, this new regime is often identified as “equivalent scaling’. It is expected that these new materials will provide a viable solution to extending the limits of the planar CMOS process for the next 5 to 10 years. Examples of the introduction of these new materials are; using copper to replace aluminum to reduce the resistivity, or using low dielectric constant materials as surrounding dielectrics to reduce coupling between CMOS interlayers [22].

To break the 100nm-feature-size/15Å-thick-oxide barrier, the most significant step is the introduction of high dielectric constant (high-k) materials. As discussed in the previous sections, the shortening of transistor channel length leads to the corresponding scaling of gate area as well as gate oxide thickness in order to maintain the same transistor parameters such as gate threshold voltage and capacitance, which is proportional to the gate area and dielectric constant while inversely proportional to the gate thickness. If the reduction of the gate dioxide thickness is to reach its limit at ~ 15 Å, the alternative way might be to look for new materials that offer higher dielectric constants. *Table 1–1* shows the electrical properties of a few promising candidates. With

a high dielectric constant (k) a thick gate dielectric layer (≥ 200 Å) gives an appropriate capacitance value equal to that of a thin equivalent oxide thickness (EOT) which is usually in the range of 5-15Å. Thus the required dielectric capacitance obtained by making oxide thickness thinner is alternatively achieved in a much thicker but proportionately higher k dielectric. The advantage of using the relatively thick high k dielectrics is in the elimination of direct tunneling and soft-breakdown. High k materials, therefore, present excellent candidates for the replacement of the traditional SiO_2 gate oxide.

If a high-k material is to replace SiO_2 as a gate dielectric, in addition to high dielectric constant (k>25), this high k material must have a reasonable energy gap (>4eV), a barrier height relative to Si greater than 1V or at least greater than the supply voltage V_d to be used with the dielectric, a low leakage current (no Frenkle-Poole, F-P, i.e., trap-assisted tunneling or other defects degrading dielectric reliability), a low interface state density (D_{it}) and a low bulk dielectric charge. Furthermore the high k material must have no or minimal capacitance-voltage hysteresis effects, no more than an atomic layer of oxide at the silicon/dielectric interface, excellent thermal stability, and high process immunity to hot carrier effects [23,24]. In brief these high k materials must possess all the excellent qualities that had qualified Si/SiO_2 system and gave it the monopoly over all MOS structure devices. These qualities are over and above that of high k.

We can break the high-k materials listed in *Table 1–1* into four groups. The first group consists of Si_3N_4 and Al_2O_3. These two dielectrics have relatively low k value

compared to the other materials. However, they are very well studied and can be easily integrated into the conventional CMOS process. Some might regard them as an "extension" of SiO_2 but they are also a necessary segue to the high-k era, given the difficulties faced in choosing a suitable high-k dielectric [25]. Well-controlled nitridated films of 15Å thickness have already been reported. The second group consists of Ta_2O_5, TiO_2 and $BaSrTiO_3$. Their k values are highest among all dielectrics. However, thermodynamic studies indicate that Ta and Ti are not thermodynamically stable on silicon and thus form an interfacial layer. This interfacial layer is shown, later in this thesis, to greatly degrade the EOT value. Moreover, the interaction of these two materials with the polysilicon or metal gate electrode is of a large concern [26]. The third group consists of other types of binary oxides such as La_2O_3, HfO_2, ZrO_2, who have been proven to be thermodynamically stable on silicon. However, these materials are often efficient diffusers of oxygen therefore post-deposition annealing in an oxidizing ambient can easily cause the formation of interfacial layers [27]. The last group is comprises mainly silicides such as $HfSi_xO_y$, $ZrSi_xO_y$, $SrTaO_6$ or $ZrSiO_4$. These multi-component oxides are compatible with and stable on silicon substrate.

Up until now, none of the above materials has emerged as the most likely candidate to meet all of the complex and stringent requirements associated with processing, device performance and reliability. Most research has been focused on the different growth technologies of the high-k dielectrics. Chemical vapor deposition (CVD) and metal-organic CVD (MOCVD) are still most commonly used on some of the materials. Ion-beam sputtering can produce $SrTiO_3$ films with well-crystallized and void-

free structures. RF magnetron sputtering, laser ablation, and electron cyclotron resonance plasma-assisted RF sputtering all have been tried in growing high-k materials [28]. Molecular Beam Epitaxy (MBE) and Atomic Layer Deposition (ALD) are also used to precisely control the growth of high-k dielectrics. One of the promising reports comes from the thermal oxidation of amorphous La to directly form La_2O_3 dielectric layer. The resulting capacitor has 33Å La_2O_3 layer with EOT of 4.8Å and a k-value of 27. It also has low leakage current 0.06A/cm^2 at ~1V and high breakdown field of 13.5MV/cm [23]. The thermal oxidation method used here is very similar to the conventional thermal SiO_2 growth in comparison with CVD or sputtering deposited gate dielectrics. Recently, Ruzyllo's group at Penn State developed a liquid source misted chemical deposition (LSMCD) technique in which the liquid metal-organic precursors is atomized and deposited in a controlled amount in the form of sub-micron mist droplets onto the wafer surface at room temperature and atmospheric pressure [29].

Buffer layers are usually used between the Si and the high k dielectric. Jet vapor-deposited (JVD) nitride film or NH_3/NO nitrided films are reported to improve the interface quality, reduce the stress, and suppress the inter-diffusion between Si and the high-k dielectric. However, the results are far from being conclusive. MOS capacitors (MOSCAPs) and MOS field-effect transistors (MOSFETs) with thin HfO_2 dielectrics and n^+ polycrystalline silicon (poly-Si) gate electrodes can be made without any barrier layer but they require rapid thermal annealing (RTA) activation of the poly-Si gate instead of furnace annealing [30].

Very few studies have been conducted to show how high-k dielectric growth could affect the quality of the interface between the high-k dielectric and silicon, or the region just below the interface. As is well known, one of the major advantages of using silicon dioxide for the gate dielectric is its near perfect match with the silicon substrate. Without a high quality interface, interface states and near-interface bulk states can act as minority carrier traps that are detrimental to the MOS device operation.

The study of high k materials and the corresponding gate stack system (high-k dielectric, interfacial layers, electrode, and their compatibility with plasma processing and the CMOS process flow) still remains at the research stage and far from production line. Major breakthroughs are very much welcome and are eagerly searched for to prepare for the 100 nm technology generation fast approaching and due in the year 2006.

1.4 Thesis research scope

The first part of this thesis research is on the study of the various issues related to miniaturization and scaling of MOS structures. We focused on thin silicon dioxide that is currently in use as a gate dielectric in CMOS but is steadily reduced in thickness to meet CMOS standards. The severity of damage to the silicon dioxide induced by processing, especially plasma etching is one of the research areas addressed in this thesis. Effective ways of characterizing the thin oxide and, hence, evaluate MOSFETs and MOS capacitors performance are discussed. Subsequently, we subjected the oxide to Fowler-Nordheim and hot carrier stresses, thereby mimicking device damage by processing and/or device aging. In the second phase of this thesis research we examined a number of

high-k candidates to replace the oxide as a gate dielectric. These high-k dielectrics are investigated in terms of their dielectric, interface, leakage and breakdown properties. The interfacial layer between the high-k dielectrics and the silicon substrate, either grown intentionally or unintentionally, are examined and their effects on the electrical properties of the gate dielectric stack are analyzed in details. Also, the impact of high-k dielectrics deposition on the underneath silicon substrate is investigated in the course of thesis studies

Table 1–1: Electrical properties of some high-k candidates

Gate Dielectric	E_g (eV)	K
SiO_2	9	3.9
Si_3N_4	5	7.5
Al_2O_3	8.7	8.5-10.5
Ta_2O_5	4-4.5	20-35
TiO_2	3-3.5	30-100
$BaSrTiO_3$	*	200-300
La_2O_3	*	27
Y_2O_3	5.6	15
CeO_2	5.5	26
HfO_2	5.7	25
ZrO_2	5.8	25
$HfSi_xO_y$	6	15-25
$ZrSi_xO_y$	6	15-25
$SrZrO_3$	5.4	30
$SrHfO_3$	*	28
Sr_2TiO_4	5.2	50
L_aAlO_3	5.7	25

...

*: no reliable values are published for these parameters.

Chapter 2

Experimental Procedure: Test Structures and Electrical Characterization Methods

2.1 Test Structures

The performance of a MOS transistor is largely determined by the quality of gate dielectrics and its interface with the silicon substrate. The effective carrier mobility, which essentially determines the speed of a MOS transistor, largely depends on the density and distribution of interface/bulk/dielectric traps. Most electrical characterization techniques are focused on how to locate and identify these traps. And most characterization methods are applied on two basic types of test structures: MOS capacitors and MOS transistors.

During the early stages of the development of MOS technology, the MOS capacitor has been used as the principal test vehicle for investigating and understanding the properties of the MOS system. In fact, much of the present knowledge of the properties of this system has been acquired by small signal admittance measurements on MOS capacitors. As pointed out by Nicollian and Brews, more than 20 properties of the MOS system can be measured and monitored using MOS capacitors [31].

Unfortunately, with the continuous miniaturization of CMOS, some new effects and phenomena appear to be inherent to MOS transistor itself and can only be observed by direct characterization on the transistor. These include junction edge effects, short channel effects, hot carrier induced interface degradation and mobility degradation due to thin gate oxides [32, 33, 34]. For this reason, the characterization of the submicron MOS transistor becomes mandatory for the development of new CMOS circuits and semiconductor memories.

Does that mean the characterization techniques on the capacitor structure have lost their significance? The answer to this question is no. Let us take the case of charging damage to oxide during the gate poly-Si etching process as an example. Both of these two test structures, MOS capacitor and transistor, have their advantages and disadvantages. A transistor is a very sensitive device and requires much smaller antenna than the capacitor for the charging damage detection. However it requires additional steps to complete the fabrication after the gate poly-Si etching. Therefore, the damage caused by gate poly-Si definition etching may be obscured by subsequent processing steps. Alternatively, a capacitor can detect the charging damage directly after the gate poly-Si definition etching. On the other hand, capacitance measurements require a large antenna. Therefore, in order to obtain detailed information one needs to perform the tests on both device structures and preferably using different techniques. This is what we attempt to do in our proposed studies. We will use both MOS capacitor and transistor structures, and we will utilize a number of electrical characterization techniques.

In the following sections, we will discuss the electrical characterization techniques that are employed in our studies. The physical principles utilized in these techniques are well documented in various books and journal articles and thus will be only briefly reviewed below. We will mainly highlight the advantages and limitations of these characterization methods. We will also point out some precautions we need to take during the tests and data interpretation.

2.2 Electrical Characterization Methods

2.2.1 Transistor Parameter Measurements

There are three principal DC MOSFET parameters, threshold voltage (V_{th}), transconductance (G_m) and subthreshold swing (S). The easiest way to understand the information on the state of the MOSFET provided by these three transistor parameters is to write down their expressions using an enhanced mode n-channel device as an example [35,36]. These expressions are :.

$$V_{th} = V_{fb} + 2\Phi_f - \frac{1}{C_{ox}}(Q_d + Q_{it}) \qquad (2.1)$$

where V_{fb} is the flat-band voltage, Φ_f is the Fermi potential, C_{ox} is the oxide accumulation capacitance, and Q_d and Q_{it} are the depletion and interface charges, respectively; and

$$G_m = \frac{dI_d}{dV_g} = \left(\frac{W}{L}\right) C_{ox} V_d \frac{C_i}{C_{ox} + C_d + C_i + C_{it}} \frac{\mu_{eff}^2}{\mu_o} \qquad (2.2)$$

where I_d is the drain current, V_g the gate voltage, and V_d the drain voltage. The capacitances C_i, C_d, and C_{it} are for the insulator, depletion region, and interface, respectively. μ_{eff} is the effective mobility, μ_o is the low-field mobility (at the threshold where Q_{it}, the interface charge, is zero). W and L are the channel's width and length, respectively;

$$S = \frac{G_m}{I_d}, D_{it} = \frac{C_{ox}}{q}\left(\frac{q}{SkT} - 1 - \frac{C_d}{C_{ox}}\right) \qquad (2.3)$$

where S is the swing and D_{it} is the interface state density. q, T, and k are the electronic charge, absolute temperature, and Boltzmann constant, respectively.

As can be seen above, V_{th} reveals the polarity and quantity of charge trapped in the interface and bulk gate dielectric. G_m is proportional to the effective carrier mobility, and S is inversely proportional to the interface density.

Transistor parameter measurements are fast and informative. Cumulative probability results are usually collected from 14 to 20 devices to determine the uniformity of the transistor fabrication process. The characterization systems are easy to operate. They usually serve as in-house monitoring tools to control the quality of device fabrication. Also they are very useful tools in the characterization of stressed devices [37].

However, despite of these formulas, these three transistor parameters usually serve as visual and qualitative measures of transistor condition. The subthreshold swing,

S, is only appropriate when the interface trap density is relatively high (>$5x10^{10}$-10^{11} $eV^{-1}cm^{-2}$) thus is not adequate for the evaluation of the interface trap density in virgin MOS devices fabricated using state-of-the-art technology where D_{it} lies in the range of $5x10^{9}$-10^{10} $eV^{-1}cm^{-2}$ [38]. The transconductance G_m is strongly affected by the short channel effects that are present in submicron devices [39]. Also from the threshold voltage data, it is hard to distinguish the effects of bulk dielectric charge from those of interface traps. Moreover, it will be shown in the following chapter that one of the main conclusions of our studies is that these three transistor parameters become less sensitive in characterizing devices with ultra thin gate oxides that are thinner than 50Å [40].

2.2.2 Capacitance Voltage (CV) Measurements

Capacitance-versus-voltage (CV) measurements are the most common characterization techniques used on MOS capacitors. A quick and simple CV scan can yield doping profiles of diffusions, implants, or bulk materials. It can reveal oxide characteristics which may be influenced by oxide deposition, annealing, stress or device damage, and it can also be used to calculate interface characteristics such as interface trap density (D_{it}) and metal-semiconductor work functions [41,42]. However, we must take a few precautions when measuring and interpreting CV data, especially on VLSI capacitors. We must also note the limitations of CV measurements on ultra thin oxide capacitors as we point out in the following.

First, the voltage sweep should be performed from inversion to accumulation after a stable inversion condition is established. This insures that we obtain a correct flat

inversion capacitance instead of a slowly decreasing deep depletion capacitance [43]. Secondly, series resistance plays an increasing role in measurements performed on capacitors with extremely thin gate oxide. This is illustrated in the simple formula given below which applies to most commercial CV systems,

$$C_p = \frac{C_s}{1 + \omega^2 R_s^2 C_s^2} \qquad (2.4)$$

where C_p and C_s are the measured capacitance and actual oxide capacitance, respectively. R_s is the series resistance which originates primarily in the substrate and in the back contact between the substrate and the probe chuck. Most monitoring capacitors tend to have large areas while maintaining the same thin oxide thickness, i.e. they give much larger capacitances than the real devices. The coupling of R_s and C_s could cause a significant distortion in CV data and misleads their interpretation [44,45]. Thirdly, CV measurements are often unsuccessful on ultra thin gate oxide (<50Å) capacitors, mainly due to the large gate leakage current. Park and co-workers pointed out the difficulty of obtaining reasonable CV data on their 52Å-thick gate oxide, 40μm x 40μm capacitors, which effectively rules out the possible observation of CV shift on samples with different metal peripheral length [46].

2.2.3 Charge Pumping Measurement

The charge pumping technique was first introduced by Brugler and Jespers [47] in 1969. This technique is based on a recombination process at the Si/SiO_2 interface of a MOS transistor involving the interface states. This recombination induces a substrate current that can be directly related to the interface-state density. Ever since then, several authors have developed and presented different ways of applying this principle for the determination of the average density of interface traps [47-50], their energy distribution [51,52], and even the geometric mean value of the capture cross section for electrons and holes at these traps [50].

The major advantage of the charge pumping (CP) measurement is it can be performed directly on the actual MOS transistors instead of monitoring MOS capacitors. Not only it eliminates the extrapolation of results from capacitors to transistors, it also can detect most phenomena that are unique to the transistor system [53].

Through CP measurement, the lateral distribution of interface traps as well as the energy distribution of these states can be determined. In modern short channel devices, the channel is usually non-uniform, either from process damage or from being subjected to hot-carrier stress. CP technique enables the probing of the interface as a function of position in the non-uniform channel [54]. It is quick, relatively simple, and it can yield precise results on the damage from FN stress, radiation, and/or hot carrier stress.

2.2.4 Deep Level Transient Spectroscopy

Deep-level transient spectroscopy (DLTS) was first developed by D.V.Lang [55]. It monitors the change of capacitance transients by controlled filling and emptying of carriers from deep levels. The activation energy level, cross section and the space distribution of the traps can thus be derived from the DLTS signal. There are two basic ways to perform DLTS measurements. The traditional way is through a 'rate window': a system which produces a peak output when the time constant of the input transient corresponds to a reference time set on the instrument. This can be implemented using a double "box-car" system, a lock-in amplifier or an exponential correlator. Another way is called Fourier-transform deep level transient spectroscopy (FTDLTS) [56]. In this technique the capacitance-time transients are digitized, and the discrete Fourier coefficients are found via numerical Fourier transformation. These coefficients can be used to calculate amplitude and time constant of the transients for discrete trap levels.

The transient signal from DLTS measurement can result from traps located in the semiconductor substrate, the semiconductor-silicon interface, and in the bulk oxide region close to the semiconductor oxide interface. DLTS is the most widely used technique for the characterization of deep states in semiconductors, especially for routine material evaluation, because it presents the information in a convenient quasi-spectroscopic form that can be visually interpreted.

DLTS can be applied on both capacitor and transistor structures. In the latter case, bias and pulse voltage are applied to gate while the drain-source current is monitored instead of the capacitance. The basic principle here is still the same. The change of

current transient comes from the filling and emptying of carriers from deep levels [57-59].

There are a few limitations on the DLTS technique, however. It requires an elaborate experimental set-up using synchronized pulse sources, integrators and time averagers. It also requires a relatively large area test device to get distinguishable capacitance/current signal. Also, each DLTS scan requires much longer time (0.5-1 hour) than a routine IV/CV/CP measurement (a few minutes) therefore it is not realistic to use it to produce statistical data. Because of that, there have been very few reports on its application on VLSI devices [60]. On the other hand, the DLTS technique offers a wealth of information that is not possible to get from other characterization techniques.

2.3 Measurement Equipment

A 4142B Hewlett-Packard Semiconductor Parameter Analyzer was used to measure transistor parameters which included V_{th}, S, the leakage current (I_g, measured at a gate voltage V_g=2V), and maximum transconductance (G_m), which is hereafter referred to as transconductance for brevity. Probability plots were then generated from the data with each plot containing results from at least 12 transistors. Charge pumping measurements were performed using a Wavetech 20 MHz Frequency Generator and the 4142B HP Parameter Analyzer. The CV and DLTS measurements were done using a Keithley system and a Bio-Rad DL8010 Fourier-transform DLTS system, respectively.

Chapter 3

Thin Gate Oxides : (I) Plasma Induced Damage and Damage Detection

3.1 Introduction

Any device parameter that is sensitive to oxide charge and interface traps can be used to monitor the degradation of MOSFETs. The threshold voltage (V_{th}), maximum transconductance (G_m) and subthreshold swing (S) are the three traditional transistor parameters which are commonly used in device characterization. For more than three decades, these three parameters were used as indicators of process-induced damage to MOSFETs [61,62,64]. However, in this chapter we demonstrate that V_{th}, G_m and S cease to be effective in monitoring plasma-induced damage in very thin gate oxide (≤65Å) MOSFETs.

In this chapter, we examined the plasma-induced damage aspects in 65Å-thick and 45Å-thick gate-oxide MOSFETs. These devices were fabricated using a 0.35μm full CMOS process flow and subjected to damage from different plasma processes, e.g., contact or via etching. We found out that V_{th}, G_m and S measurements revealed very little to no information with respect to process induced damage in these devices. Even charge pumping (CP) measurement, one of the most sensitive characterization methods, was not able to probe process-induced damage aspect in these very thin gate-oxide devices. In contrast, we clearly establish that gate leakage current (I_g) becomes a very sensitive

parameter which could be reliably used in assessing damage to thin gate oxide MOSFETs.

3.2 Device Fabrication and Test Structures

The n-channel MOSFETs used in this study were fabricated on 200 mm boron-doped (~$10^{17}cm^{-3}$) epitaxial silicon substrates using the SEMATECH 132AZ mask set [69]. The channel length and width for these transistors were 0.35 and 5.0μm, respectively. The thickness of the gate oxide, grown at 900°C in dry O_2 ambient, was either 65Å or 45Å. The poly-Si gate definition etching, the contact etching and the metal etching employed a Cl_2/HBr, a CHF_3/CF_4 and a $BCl_3/N_2/Cl_2$ based chemistries, respectively. All etching processes were performed using commercial reactive-ion-etching and transformer coupled plasma tools. After metallization, all transistors were given annealing in forming gas (6% H_2 and 94% N_2) at 400 °C for 30 minutes.

Four test modules, Type I, II, III and IV, were used in this study. These modules differ in oxide thickness and/or vulnerability to damage from a certain plasma process, as given in *Table 3–1*. Each module comprises transistors that had different antenna ratios (ARs). Here AR refers to the area ratio between poly-Si field oxide, metal 1 pad, or metal 2 pad coverage and gate-oxide coverage, depending on the plasma process examined. The ARs used were 5770, 14470 and 62220. The number of via holes in Type I and IV modules, and the number of contact holes in Type I module were 58×58 (the number of holes is given as a product of two numbers to emphasize the rectangular geometry of the via or contact hole arrays with a total number of holes that is equal to the product). In

Type II and III modules, the number of contact and via holes were kept at a minimum of 2×2 to minimize the corresponding damage. In Type III sample, the area of metal 1 interlayer was also kept as minimum to reduce the damage from metal 1 process. All modules had the same size of metal 2 pad.

3.3 Experimental Results

Figure 3.1 shows V_{th} and S for Type I module (45Å-thick gate-oxide) with different antenna ratios (AR=5770, 14470 and 62220 at poly-Si, metal 1 and metal 2 etch steps). No significant differences can be seen in both V_{th} and S for different ARs. The percentage distributions of data for different AR are similar. The maximum median variations in V_{th} and S, as a function of AR, are less than 5 mV and 0.2 mV/dec., respectively. G_m for this Type I module (not shown) also yields a similar pattern to V_{th} and S: no observable changes in G_m with AR. In essence, none of the three parameters, V_{th}, S and G_m, has been able to discern differences in damage from different ARs. However, it is currently very well established that charging damage clearly increases with increasing AR [66, 70]. We reiterate that this Type I module is designed such that it would be subjected to the highest charging damage from the poly-Si etch and the two metal etches. During the poly-Si gate definition and the metal etching processes, the poly-Si or metal pads attached to the thin gate oxide act as charge collecting electrodes, which will impose a stress voltage across the oxide and Si/SiO_2 interface. This voltage increases with increasing pad area that is proportional to the AR, and results in a Fowler-Nordheim (FN) tunneling current flow through the thin oxide. The larger the AR, the

higher the stress voltage and current across the oxide and consequently the higher the damage to the MOSFET [62, 64-66, 70]. It is not likely that reducing the oxide thickness would totally eliminate this damage [66]. We can only assume that the damage is so low that V_{th}, G_m, S can no longer reveal its dependence on AR.

The I_g probability plots for the same Type I MOSFETs are shown in *Figure 3.2*. Even when a logarithmic scale is used as in *Figure 3.2* , the dependence of I_g on AR is very clear. The transistors with the largest AR (62220) yield the largest leakage currents (a median current of 10^2~10^3 nA), while transistors with the smallest AR (5770) have leakage currents only in the range of ~1nA. The differences in I_g are up to three orders of magnitude. As explained before, this is what we would expect from these transistors – the larger AR a transistor has, the more damage it incurs during the plasma processing. Measurements on other modules in this 45Å-oxide wafer were performed and all results showed similar patterns: larger AR yielded larger I_g, while no clear shifts in V_{th}, G_m and S could be observed. Therefore we may reasonably conclude that, at least for the 45Å gate-oxide devices, I_g is a more sensitive parameter than V_{th}, G_m and S in monitoring plasma-induced damage in the MOSFETs.

Figure 3.3 shows the I_g data from measurements on Type II, III and IV modules (all with oxide thickness of 65Å) with two different ARs (AR=5770, 62220). Two general trends can be observed. First, for transistors in the same module but with different ARs, those with larger ARs yield larger I_g. This is exactly what we found in type I module. Second, for different modules, I_g(IV) > I_g(II) > I_g(III) where the Roman numbers between brackets indicate the type. Type IV module is sensitive to damage from metal 1,

via and metal 2 etch steps since transistors bear charging antennas for each one of these processes. Therefore, expectedly, this module must be the most damaged as witnessed by the largest I_g. Type II module was primarily sensitive to metal 1 etch damage. Although this module employed a small metal 2 AR to reduce the damage from metal 2 etching, the size of metal 2 pad, which is kept the same for all modules, is still large enough to induce significant additional damage during the metal 2 process. Hence, Type II module shows an intermediate I_g between that of Type IV and Type III. Type III module, however, employed a minimum area of metal 1 inter-pad that is much smaller than the metal 2 pad. Therefore it only experienced damage during the metal 2 process. Consequently, I_g becomes the smallest one. Here again I_g is able to differentiate between slight changes in the degree of damage for different modules.

Figure 3.4 shows the I_g dependence on AR for Type III module. It is interesting to note here that in spite of the very low leakage current (~pA), it is still possible to observe the AR dependence of I_g. The small I_g in this module strongly implies that Type III module suffered the least damage during the whole process.

We now move on to study the other three transistor parameters V_{th}, G_m, S in the 65Å-thick gate-oxide devices and see if they exhibit similar patterns to those in *Figure 3.3* . *Figure 3.5* shows V_{th} and G_m for Type II, III and IV modules with different ARs. The results in *Figure 3.5* are the median values from probability curves of sets of 12 devices. G_m, for different modules and ARs, does not reveal any differences. When AR = 5770, all three modules have roughly the same G_m (~141μS), whereas when AR increases to 62220, the difference in G_m between the three modules is still less than 3 μS. As for

V_{th}, we notice that it decreases with increasing AR, which indicates positive charge buildup in the oxide. However, unlike I_g, we are not able to find any correlation between the three modules, and the variance in V_{th} is less than 4%, or 25 mV. We also note that there is no significant change in S (not plotted) for different modules and different ARs. Charge pumping (CP) measurement was used to detect the damage aspects in the 65Å-thick oxide modules. *Figure 3.6* shows typical CP curves for Type III module with AR=5770 and 62220. As can be seen, the two curves of the Type III module almost overlap with each other. Repeated CP measurements on the same Type III modules in different locations in the wafer show that differences in CP current with different ARs are less than 5%. We also performed CP measurements on Type II and IV modules. At AR=5770, Type II yields slightly higher CP current peak than Type III, as shown in Fig 3.6. When AR further increases, the height of the CP current peak increases but is quickly undermined by the high leakage current tail. No CP curve could be obtained in Type IV due to the high gate leakage current even at low AR. Higher CP peak indicate more damage in the transistor, especially at the Si/SiO_2 interface. The CP data in Fig 3.6 enables us to draw the following conclusions: (1) just like V_{th}, G_m and S, CP is unable to resolve interface damage dependence on AR in lightly damaged Type III module; and (2) from CP it is possible to observe differences in damage degree between the different modules. Our CP data agrees with I_g measurements in that the Type IV module was the most damaged, whereas Type III was the least damaged.

3.4 Discussion

We have shown that the gate leakage current I_g is a very sensitive parameter to monitor the quality of thin gate-oxide MOSFETs. It can differentiate between damage aspects from different plasma processes, as well as the damage dependence on antenna ratio. Longer plasma process with harsher processing conditions and larger AR in a processed device results in more damage, which is correlated to larger I_g. Traditional transistor parameters V_{th}, G_m and S are no longer good characterization parameters as the gate oxide becomes too thin (≤65Å). In our experiments, these three parameters failed or partially failed to give sufficient information regarding damage from plasma processing. On the other hand, charge pumping measurement, which is believed to be extremely sensitive to defect states at Si/SiO_2 interface and in the channel region of MOSFETs, is also not informative in the case of ultra-thin oxides, since it did not reveal the AR dependence in lightly damaged samples (Type III), and it failed when gate leakage current became large.

It should be noted that all of our measurements were performed on thin gate-oxide (45Å and 65Å) devices, i.e., results of the type presented in section (III) are the consequence of continuously shrinking the oxide thickness in submicron MOSFETs. In fact, our previous work on relatively thick oxide (≥90Å) devices did not call for the importance of I_g [70]. In 90Å-thick gate-oxide MOSFETs, I_g was very small within the range of 100 $fA/\mu m^2$ or less, thus it could hardly be used to distinguish damage between different samples. Our results also showed that, in 90Å-thick oxide MOSFETs, measurements of V_{th}, G_m and S were capable of bringing out the damage dependence on

ARs. Due to the hydrogen passivation of defects during post-metal annealing, the shifts of these parameters as a function of AR were extremely small, nonetheless these shifts were still observable [70]. However, when the oxide becomes thinner (≤65Å), these shifts become less and less significant, as shown in our previous figures. Comparing V_{th} in *Figure 3.1* with V_{th} in *Figure 3.5* , we notice that shifts in V_{th} with different AR are much smaller in 45Å-thick gate-oxide samples (5mV) than in 65Å-thick gate-oxide samples (25mV). This is also the case with shifts in G_m and S.

The observation of very small to no change in V_{th}, G_m and S in thinner oxide devices may indicate that, for the same process flow, the AR related damage in the thinner oxide at least would not be as significant as that in thicker oxide. This is consistent with the well-known large tolerance of thin oxides to current stress and the fact that the plasma stress current does not increase very much with reducing the oxide thickness. It has been recently proposed that plasma can be considered as an imperfect current source with the current somewhat modified by the gate electrode voltage [66]. Injected electrons gain energy as they travel in the oxide and they need to travel a certain distance beyond which their energy is high enough to create charge-trapping defects. An ultra-thin oxide may not be thick enough to accommodate such a distance. Also in a very thin oxide an electron may travel ballistically (without scattering or collisions) [71, 72]: this means that there will be less collisions between electrons and atoms, and therefore fewer amount of generated defects. Moreover, some of the charge trapped in these few defects will be easily swept off by the high electric field in the gate oxide during the process. Needless to say that most of the Si/SiO_2 interface and bulk oxide states will be

passivated after the post-metal annealing. Since V_{th}, G_m and S are essentially affected by charge within the gate oxide and interface, less charge states lead to less sensitivity of these parameters.

The gate leakage current I_g, on the other hand, benefits from the oxide being very thin, since large leakage current I_g through the oxide can be measured even at low applied electric field (≤ 3V). This is due to direct tunneling (DT) which would only happen in thin oxide devices [67, 73]. The mechanism of the stress induced DT current has already been very well studied [71-75]. DT effectively increases the magnitude of the gate current, making it more observable. More important, this DT current appears to be trap-assisted, i.e. it can use bulk oxide states and interfacial states as hopping sites, and it also reflects the barrier (field) distortion caused by trapped negative or positive oxide charges [74]. In other words, the change of the gate leakage current I_g is an indication of change in damage aspects.

3.5 Conclusion

Based on the results from measurements on 65Å and 45Å thick oxide MOSFETs with different ARs, we have demonstrated that the gate leakage current I_g is a very sensitive parameter to monitor the quality of ultra-thin gate-oxide devices. It can differentiate between the damage aspects from different plasma processes, as well as the damage dependence on AR. Also, it can detect a slight change in oxide charge and interface states because of its dependence on trap-assisted tunneling through the thin oxide. Longer plasma processing and larger AR both result in more damage, which are

reflected in larger I_g. Traditional transistor parameters V_{th}, G_m and S were found ineffective in characterizing plasma process induced damage in ultra-thin gate-oxide device. These parameters failed or partially failed to resolve differences in devices with variable degree of damage. We have also shown that I_g measurement in ultra-thin gate-oxide devices becomes more sensitive in discerning damage than charge pumping.

Table 3–1: Test Modules

Module	Oxide thickness (Å)	Damage profile
Type I	45	Antenna employed at poly-Si gate, Metal 1 and Metal 2 etch steps, AR=5770, 14470 or 62220, Contact holes = 58×58
Type II	65	Antenna employed at Metal 1 etch step only, AR=5770, 14470 or 62220, Contact Holes = 2×2
Type III	65	Antenna employed at Metal 2 etch step only, AR=5770, 14470 or 62220, Contact Holes = 2×2
Type IV	65	Antenna employed at both Metal 1 and Metal 2 etch steps, AR=5770, 14470 or 62220, Contact Holes = 58×58

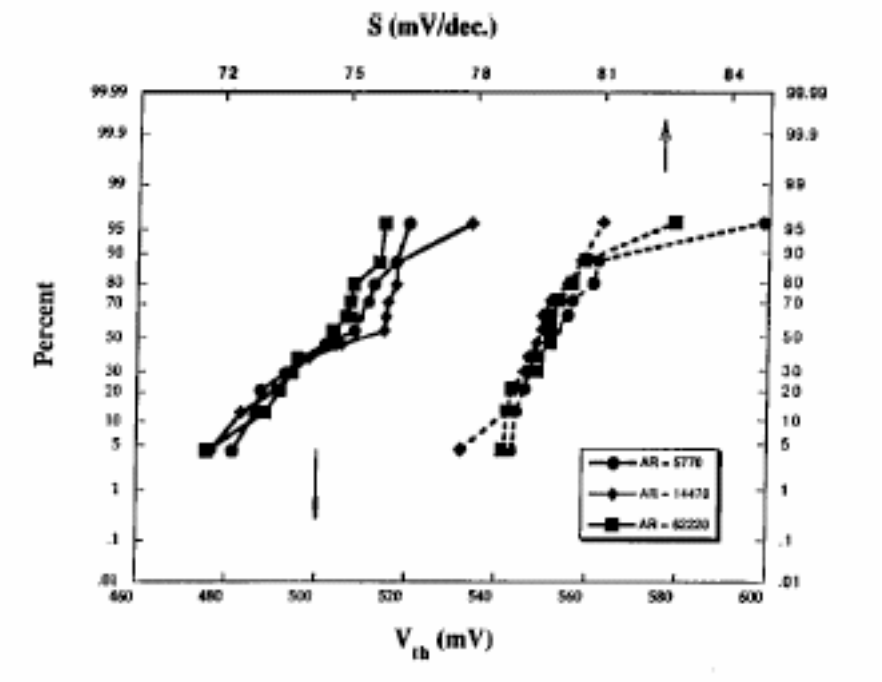


Figure 3.1: The threshold voltage V_{th} and subthreshold swing S plots for Type I module (45Å-thick gate-oxide, antennas employed at poly-Si gate, metal 1 and metal 2 etch steps with AR=5770, 14470 and 62220)

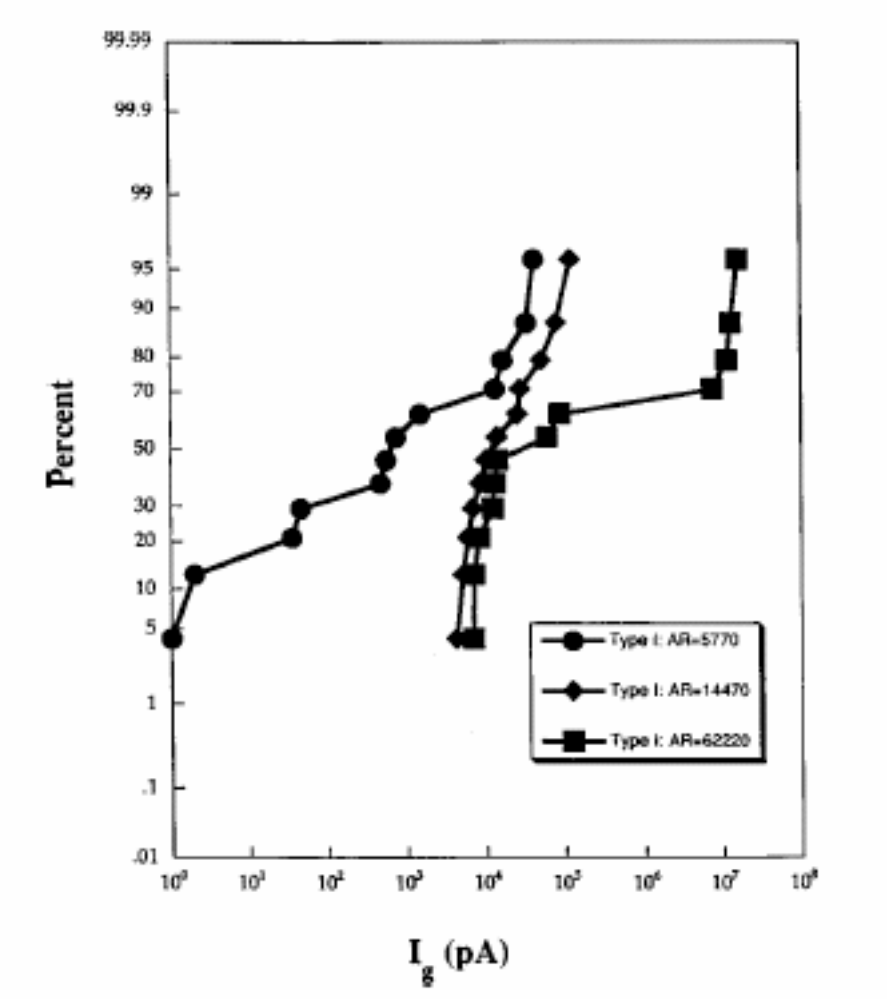


Figure 3.2: The gate leakage current I_g plot for Type I module (45Å-thick gate-oxide, antennas employed at poly-Si gate, metal 1 and metal 2 etch steps with AR=5770, 14470 and 62220)

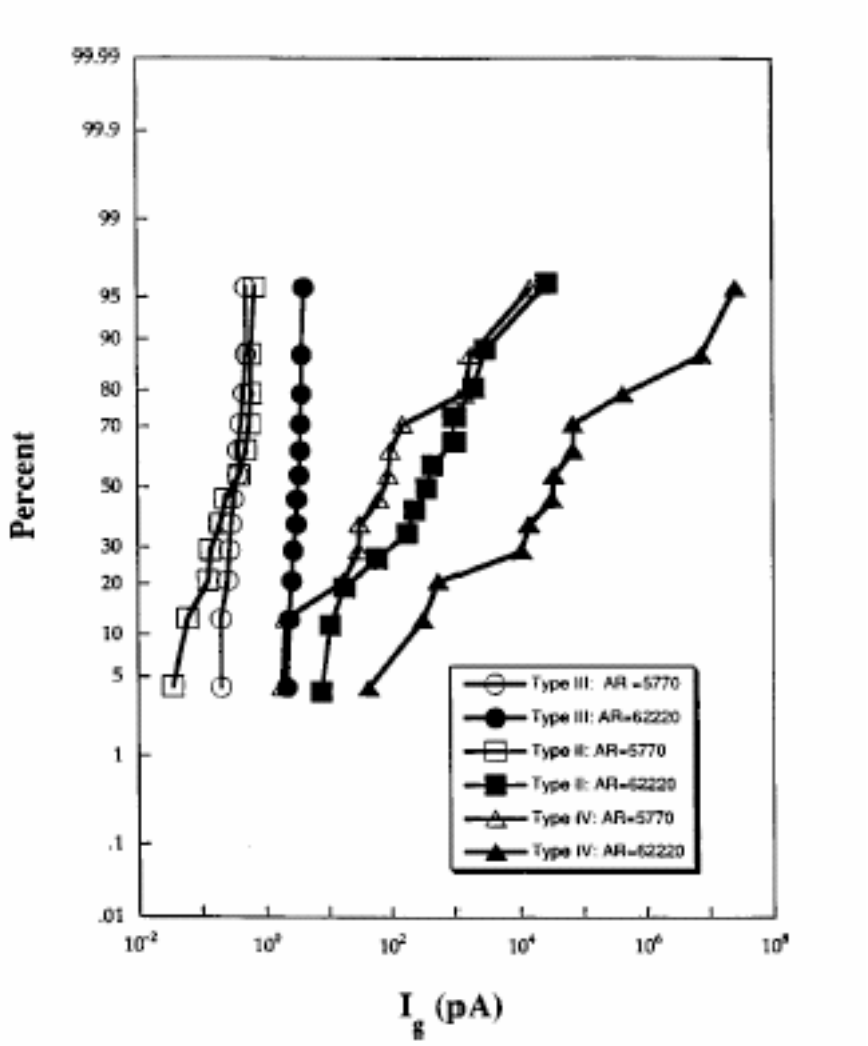


Figure 3.3: The gate leakage current I_g plots for Type II, III and IV modules (65Å-thick gate-oxide devices)

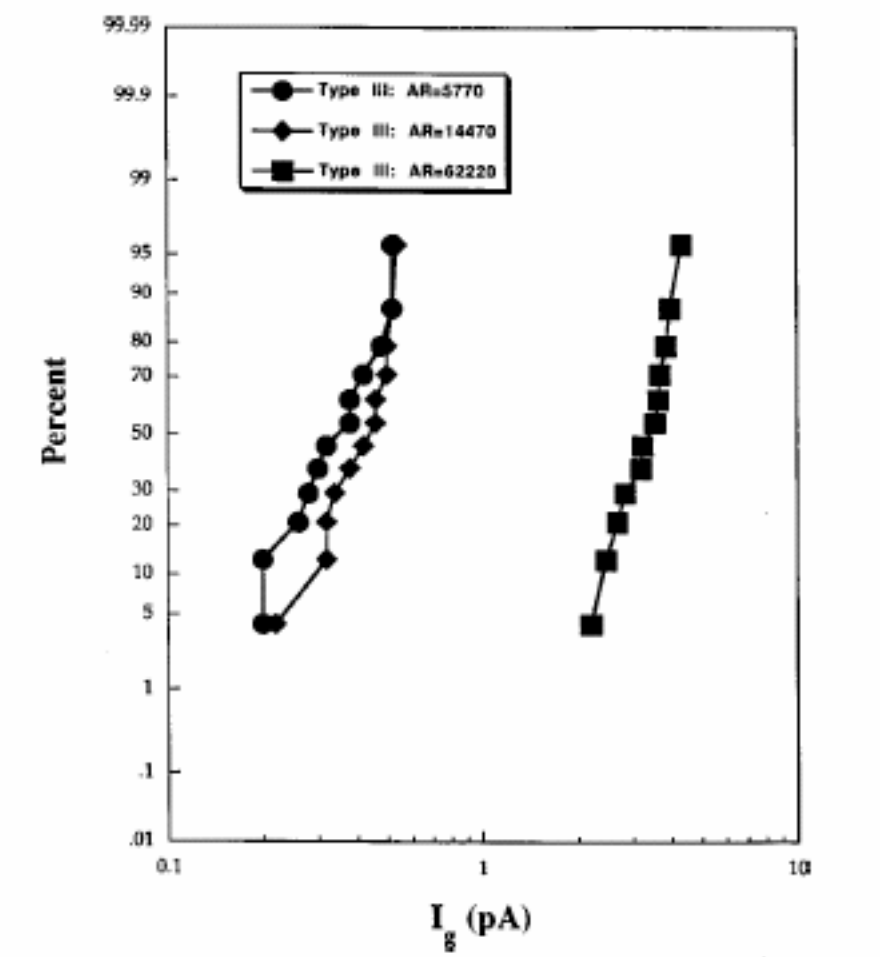


Figure 3.4: The gate leakage current I_g plots for Type III module (65Å-thick gate-oxide, antennas employed at metal 2 process only with AR=5770, 14470 and 62220)

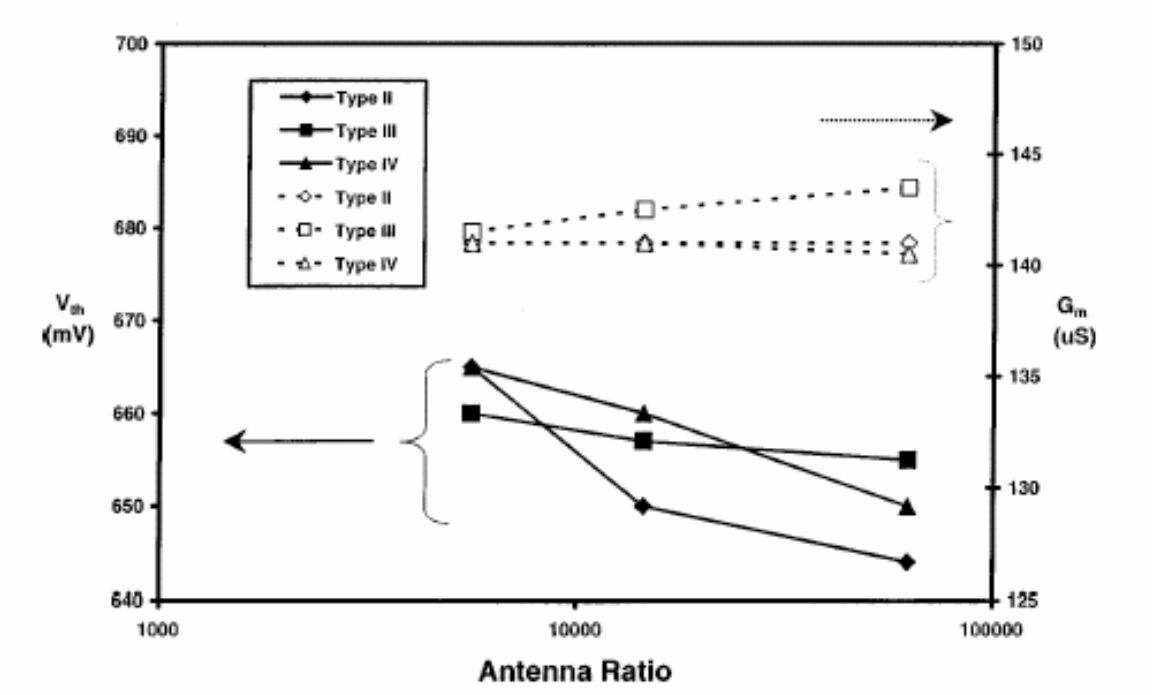


Figure 3.5: The threshold V_{th} and transconductance Gm plots for Type II, III and IV modules (65Å-thick gate-oxide). The mean values from corresponding probability curves were plotted here as a function of antenna ratios (AR=5770, 14470 and 62220).

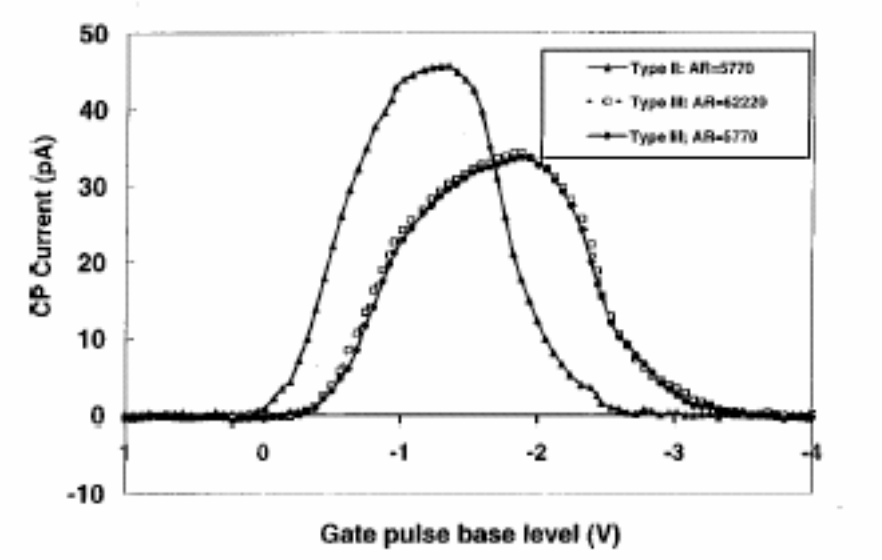


Figure 3.6: The charge pumping curves for Type II module (AR=5770) and Type III module (AR=5770,62220). The measurement conditions were: reverse-bias-voltage V_{rev} = 0V, voltage-pulse height V_{pulse} = 2.2V and frequency f = 1 MHz.

Chapter 4

Thin Gate Oxides : (II) Fowler-Nordheim Stress Reliability

4.1 Introduction

We have shown in the preceding chapter that leakage current is the most sensitive transistor parameter for the characterization of plasma charging damage in thin oxides. Other transistor parameters are shown to be ineffective in probing this damage in the thin oxides. However the information derived from I_g is very limited and a detailed study of the very thin gate oxides requires the use of more elaborate techniques such as the one utilized in the study presented in this chapter.

Plasma charging and the ensuing gate oxide and oxide/Si interface damage are major reliability concerns for submicron complementary metal-oxide-silicon (CMOS) technologies [76-78]. Fowler-Nordheim (FN) stress tests on thin gate oxides are frequently used to assess the reliability of metal-oxide-silicon (MOS) structures, and to determine the nature of the mechanisms responsible for the degradation of their characteristics [79].

During FN stress, degradations in metal-oxide-silicon field-effect transistor (MOSFET) characteristics are, predominantly, attributed to the generation of charged defects in the bulk gate oxide, and at the SiO_2/Si interface. Charged defects in the gate oxide will shift the threshold voltage in the MOSFET, whereas interface traps will affect

both the threshold voltage and the minority carrier mobility. It has also been suggested that interface trap generation during device operation may lead to oxide breakdown [79]. However, bulk Si traps in the channel region just beneath the SiO_2/Si interface, if generated by FN stress, can be detrimental to the minority carrier lifetime.

In this chapter we examine trap generation by FN stress in MOS capacitor structures. These MOS structures were fabricated using a full 0.5μm CMOS process flow. The study of the traps was carried out using capacitance-voltage (CV) and deep-level transient spectroscopy (DLTS) measurements. We report on positive charge accumulation in the bulk gate oxide and trap generation at the SiO_2/Si interface. The positive charge and interface traps are all induced by the FN stress. More importantly, we demonstrate that FN stress is able to induce bulk Si traps just beneath the SiO_2/Si interface.

4.2 On the Device Structures and the Experimental Procedure

The MOS capacitors used in this study were fabricated on 200 mm boron-doped ($\sim 10^{17} cm^{-3}$) epitaxial silicon substrate using the SEMATECH 132 Z mask set for a 0.5μm CMOS process [80]. All capacitors were fabricated using the full 0.5μm CMOS process up to and including metal 1 processes as well as post metal 1 annealing at 400°C in forming gas (94% N_2 and 6% H_2) ambient. The nominal dimensions of the n^+-polycrystalline silicon (poly-Si) gate were 0.5μm × 80μm, and the 90 Å-thick gate oxide (SiO_2) was thermally-grown at 900°C in dry O_2 ambient. The poly-Si gate definition

etching employed a Cl_2/HBr-based chemistry, whereas the contact etching employed a CHF_3/CF_4 based chemistry and the metal 1 etching used a $BCl_3/N_2/Cl_2$ chemistry. All etching processes were performed using commercial reactive-ion-etching and transformer coupled plasma tools.

Directly after processing, CV and DLTS measurements were performed to find defect densities and defect states in the MOS capacitor. Upon the completion of measurements in the as-processed capacitors, they were then subjected to constant-voltage FN stress and subsequently both CV and DLTS measurements were performed again to find changes in defect densities and states. The FN stress condition was -12 V on the gate for 30s duration at temperatures between 50 K and 300K. The CV and DLTS measurements were done using a Bio-Rad DL8010 Fourier-transform DLTS system. The DLTS measurement conditions were: (i) the capacitor was held at a zero-bias steady state; (ii) a filling pulse of 40ms width and height (V_p) in the range -2 V to -6 V; and (iii) a temperature scan rate of 0.5 K/s to 1 K/s. In the DLTS measurements, either the temperature was scanned from 350 K down to 60 K or from 60 K up to 350K. In the former scan the temperature of the FN-stressed capacitor was raised to 350K before the DLTS measurement was performed, whereas in the latter scan the temperature was brought down to 60 K directly after the FN stress and then followed by DLTS measurement from 60 K to 350 K. The CV measurements were performed between accumulation and inversion modes of the MOS capacitor for a gate voltage sweep between -6 V and +4 V. All CV measurements were performed at room temperature.

4.3 Experimental Results

Figure 4.1 shows a typical CV scan in the MOS capacitor before (solid line) and after (dotted line) FN stress. This CV scan was taken in a capacitor that was FN stressed at 300K. As can be seen from *Figure 4.1*, the CV curve is shifted in the negative direction of the gate voltage as a result of the FN stress. The shift of the flat-band voltage induced by the FN stress is calculated as -0.5 V. This is an indication of a positive charge build-up in the bulk gate oxide and at the SiO_2/Si interface induced by the FN stress. We estimated the total positive-charge build-up to be ~10^{-7} C/cm^2 which corresponds to an areal defect density of ~10^{12} cm^{-2}. Similar CV curve shifts and defect densities were observed to be induced by the FN stress at all stress temperatures between 50 K and 300 K.

No DLTS peaks were observed in any of our MOS capacitors before the application of FN stress. Since the resolution of the DLTS system is ~10^{-6}, the defect concentration in the bulk Si of the unstressed capacitors should be well below 10^{11} cm^{-3}. *Figure 4.2* shows the DLTS signal taken in a capacitor that was stressed at 300 K. A broad peak which is ~70 K wide and centered at 280 K is observed. This peak, hereafter referred to as H(0.55), corresponds to a band of closely spaced hole traps of 0.2 eV width and centered at 0.55 eV above the top of the valence band (E_v). Different pulse heights were used to examine the spatial distribution of H(0.55). Two different DLTS spectra, taken under the same conditions except for V_p of -2V and -6V, are shown in *Figure 4.2* . Clearly the DLTS signal's intensity, height and width are independent of the pulse height, which indicates that this DLTS signal is associated with hole traps located at the SiO_2/Si interface.

The same interfacial hole trap H(0.55) can also be seen in capacitors stressed at 250 K, 200 K and 150 K. *Figure 4.3* shows the relative density of H(0.55) estimated from $\Delta C/C$, where ΔC is the height of the H(0.55) DLTS peak and C is the capacitance taken at the temperature of the peak. As shown in *Figure 4.3* , the concentration of H(0.55) drops significantly as the stress temperature is lowered to 200 K and 150 K. When the stress temperature is further lowered to below 150K, H(0.55) is no longer detected.

Figure 4.4 shows the DLTS spectrum obtained in a capacitor stressed at 150 K. It is inferred from higher temperature stress that H(0.55) still exists at the high temperature end of the spectrum shown in *Figure 4.4* however poorly resolved. But it is apparent from *Figure 4.4* that a new peak E(0.35) appears at ~135 K. This new peak corresponds to an electron trap located at 0.35eV below the bottom of the conduction band (E_c). From *Figure 4.4* , it can also be seen that the E(0.35) signal intensity changes with different pulse heights (V_p = -2V, -3V), which is a characteristic of a bulk trap [78]. This indicates that this electron trap is located in the Si substrate.

Up until now, all the DLTS signals discussed above are not affected in any way by the direction of the temperature scan; i.e., different temperature scan directions always yield the same spectrum. An interesting spectral feature, however, appears in the DLTS spectra on capacitors stressed at 100 K. As can be seen in *Figure 4.5*, now the DLTS signal depends on the temperature scan direction. In the 300 K to 60 K temperature scan (solid line), the familiar E(0.35) signal is seen, however in the 60 K to 300 K temperature scan E(0.35) decreases in intensity and a new electron trap, denoted as E(0.30) and located at 0.30 eV below E_c, emerges. Similar to E(0.35), the E(0.30) signal varies in

intensity with pulse height and is, therefore, located in the substrate. It is also observed that $\Delta E(0.30) \sim -\Delta E(0.35)$, where $\Delta E(0.35)$ and $\Delta E(0.30)$ are changes in the trap density of E(0.35) and E(0.30), respectively, as the direction of the temperature scan is reversed. This effect was found to be completely reversible: each one of the two characteristic spectra could be exactly reproduced, provided that measurement was performed in the appropriate direction of temperature scan. These are signatures of a defect that is configurationally bistable: i.e., the defect has two stable configurations and each one of the two configurations is associated with one of the electron traps E(0.35) and E(0.30) [82].

Figure 4.6 shows the DLTS spectra taken on the capacitor stressed at 50 K. An electron trap E(0.37), located at 0.37eV below the conduction band, is seen in the Si substrate while E(0.35) and E(0.30) are seemingly absent. This trap is only detected when the capacitor is stressed at 50 K and subsequently measured from 50 K to 300 K (solid line): the capacitor's temperature remained at 50 K prior to the DLTS scan. However when the capacitor's temperature is raised to 300 K upon the completion of the DLTS scan the defect that gives rise to E(0.37) can no longer be detected. This is clearly demonstrated by the absence of the E(0.37) signal in the dotted DLTS spectrum of *Figure 4.6* which is taken from 300 K down to 60 K.

4.4 Discussion

During the stress electrons are injected from the poly-Si gate into the bulk gate oxide and are swept by the electric field towards the SiO_2/Si interface. In the meantime,

holes from the p-type Si substrate are attracted to the SiO_2/Si interface and into the bulk gate oxide. However since the effective hole mobility in the oxide could be as low as ~10^{-11} $cm^2/V \cdot S$, holes in the gate oxide move much slower than electrons which have significantly higher mobility. Therefore, the probability of holes being trapped at and near the SiO_2/Si interface region of the gate oxide is very high. This would result in the positive charge build-up observed by CV measurements.

The electrons, on the other hand, are accelerated by the stress field of ~10 MV/cm (a constant voltage of -12 V on a 90Å-thick oxide). As they arrive at the SiO_2/Si interface electrons can acquire energies that may reach a few eVs above the SiO_2 conduction band edge. These energetic electrons will collide with Si, O or H atoms at the interface, thus, generating electrically active defects at the SiO_2/Si interface [83, 84]. These defects comprise dangling bonds at Si and/or O interfacial atomic sites which result from Si-O or Si-Si bond breakage by accelerated electrons. Also the accelerated electrons may cause the release of hydrogen, via Si-H or O-H bond breakage, from interface defects passivated by hydrogen during post metal 1 annealing [85]. However, it has been shown that the release of hydrogen from passivated interface defects needed low-level FN stress applied for only very short duration of ~5 S [76, 77]. In this study H(0.55) is not detectable when the FN stress duration is below 20 S. This excludes Si-H and O-H bond breakage as a possible defect generation mechanism. Since accelerated electron interaction with Si-O or Si-Si is thermally activated its severity is expected to increase with increasing temperature. This is clearly demonstrated in *Figure 4.3* where the H(0.55) DLTS signal is seen to increase in intensity as the stress temperature increases.

We note that this H(0.55) band does not include the P_b center which is known to give rise to an electron trap at E_c-0.25 eV and a hole trap at E_v+0.30 eV [86].

One interesting features of H(0.55) is its location at mid-gap. This suggests that traps within H(0.55) can act as efficient recombination centers which would have an adverse effect on minority carrier (electron) lifetime in the capacitor. This is particularly important since the MOS capacitor fabricated on p-type substrate simulates what would happen in similarly stressed n-channel MOSFET where the current carriers in the channel are electrons (minority carriers).

There appears to be at least two distinct bulk silicon defects produced by the low temperature (<200 K) FN stress (*Figure 4.4, Figure 4.5 and Figure 4.6*). From the DLTS measurement conditions it is estimated that these defects are located within depths of 600Å to 1000Å below the SiO_2-Si interface. This region corresponds to what would be the channel in a similarly processed n-channel MOSFET.

Stressing at T= 150 K gives rise to two electron traps E(0.30) and E(0.35) which, based on our observations, are associated with a configurationally bistable defect. Defects in solids which display bistable electronic properties are of major importance. Examples of these defects include the EL2 and DX centers in GaAs and AlGaAs [87, 88] and a number of radiation-produced and Fe-related defects in silicon [89-91]. Bistability occurs whenever the stable configuration of a defect changes with its charge state and a certain energy barrier exists for conversion from one configuration to the other.

The third bulk electron trap is E(0.37), which is observed in capacitors stressed at 50K. This defect can no longer be detected after warming the capacitors to 300 K. In fact

E(0.37) is not stable at temperatures higher than 100 K. As can be seen in *Figure 4.6*, E(0.37) is a broad and irregular peak of about 60 K in width and centered at 150 K.

It should be noted that the bulk electron traps are only observed after the FN stress. These traps are associated with defects that are, presumably, formed by interactions of the energetic electrons that make it through the interface with the Si substrate. These interactions result in the formation of self interstitials and vacancies. The interstitials are mobile at temperatures as low as 4.2 K [92], while the vacancies are stable at temperatures in the range of 70 K to 150 K [93]. It is, hence, reasonable to suggest that the bulk silicon defects observed in our study are both vacancy related.

The isolated single vacancy is stable at 50 K and it starts to be mobile and tends to anneal out above 70 K in p-type Si [92]. This is very similar to the temperature stability of E(0.37) observed in this study. Moreover, the vacancy is known to give rise to an electron trap at E_c-0.4 eV which is suggested to correspond to the charge-state transition (0/-) within the defect [90]. This energy position is also very close to E(0.37). We, therefore, associate E(0.37) with the isolated vacancy defect [92-94]. The bistable defect giving rise to E(0.30) and E(0.35) is tentatively associated with a boron-vacancy pair [95]. This association was based on the temperature at which it is generated as well as its thermal stability.

4.5 Conclusion

FN-stress induced carrier traps on n^+-poly-Si/90Å-thick SiO_2/Si substrate capacitor structures, fabricated using a 0.5 μm CMOS process flow, have been studied by CV and DLTS measurements. The results obtained are summarized in the following:

(i) For FN stress temperatures between 50 K and 300 K, positive charge build-up was observed to take place in the bulk gate oxide and at the SiO_2/Si interface.

(ii) For FN stress temperatures between 150 K and 300 K, a broad DLTS signal centered at E_v+0.55 eV was observed to be induced by the stress. The signal comprises a band of hole traps located at the SiO_2/Si interface.

(iii) For FN stress temperatures below 150 K, two electron traps in bulk silicon 600 Å to 1000Å below the SiO_2/Si interface were observed to be generated by the stress. This is the first time that FN stress is reported to directly affect this region which would be the channel in a corresponding n-channel MOSFET. One of these traps is configurationally bistable and gives rise to two electronic states at 0.30 eV and 0.35 eV below E_c. This defect is seen to be induced by FN stress at 150 K and 100 K, and is absent in capacitors stressed below 100 K. The second defect, associated with an electronic state at 0.37 eV below E_c, is observed following FN stress at 50 K only.

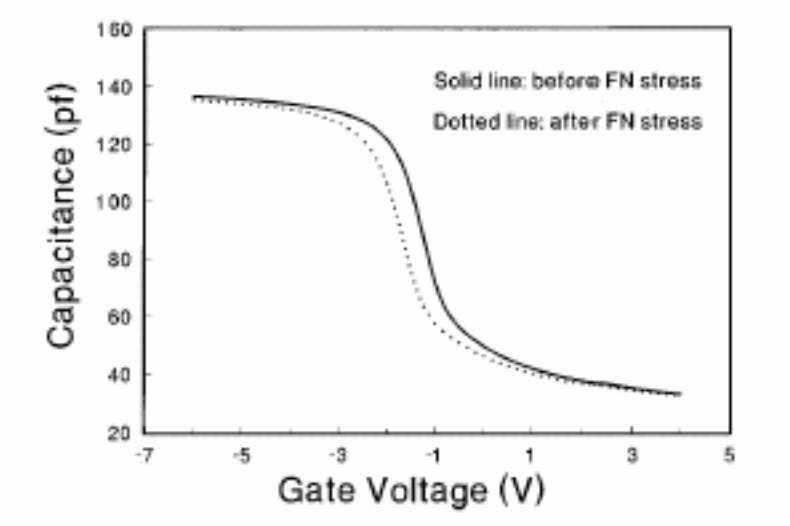


Figure 4.1: CV spectra on a MOS capacitor before and after FN stressed at 300 K. The solid line is the CV curve measured before FN stress while the dotted line is the one measured after FN stress.

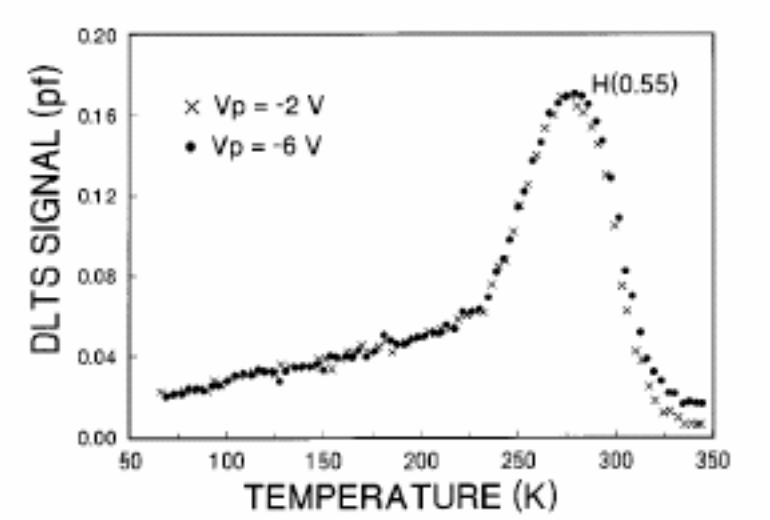


Figure 4.2: : DLTS spectra taken in temperature scans from 350 K down to 60 K in a capacitor that was FN-stressed at 300 K. The spectra were taken at a filling pulse V_p of -2V and -6V in a zero-biased capacitor

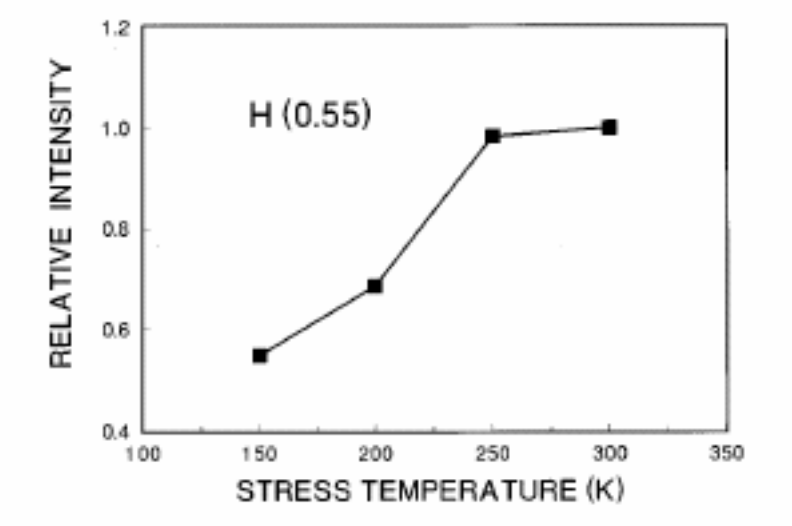


Figure 4.3: The relative intensity of H(0.55) DLTS signal as a function of the FN stress temperature.

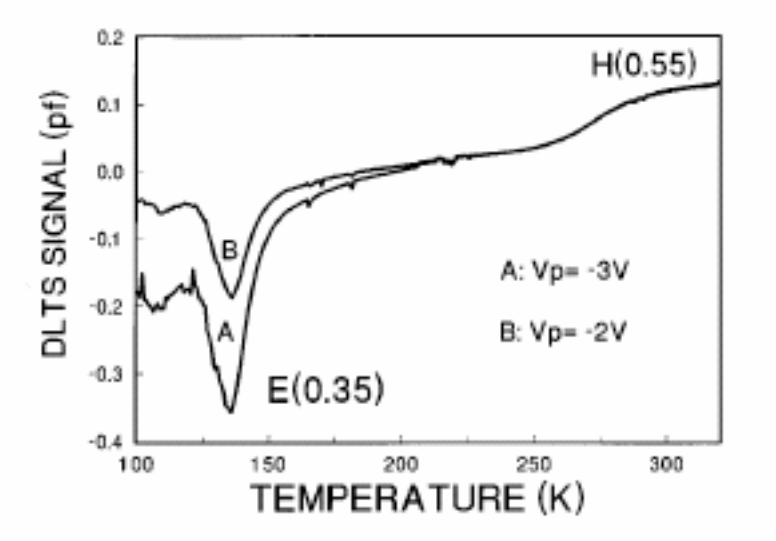


Figure 4.4: The DLTS spectra taken in a zero-biased capacitor at a filling pulse of -2V and -3V with temperature scan from 320 K down to 60 K. Prior to taking the DLTS spectrum the capacitor was FN-stressed at 150 K and subsequently warmed up to 320 K.

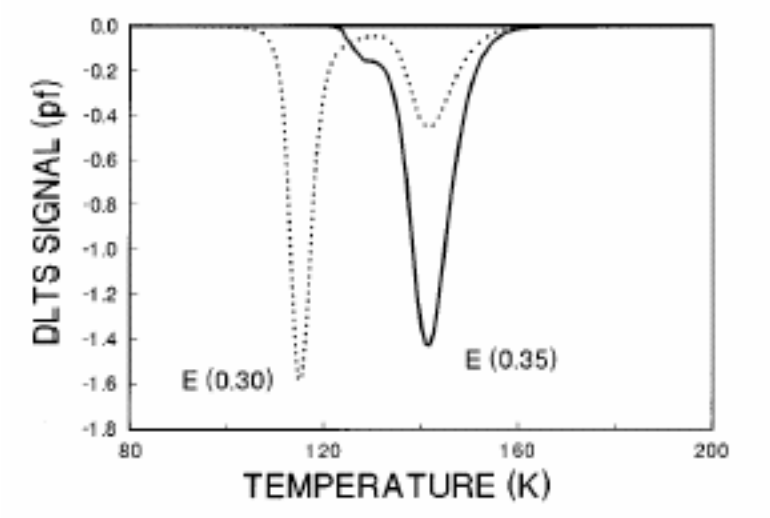


Figure 4.5: The DLTS spectra of different temperature scan directions taken in a zero-biased capacitor at a filling pulse of -4V. The capacitor was stressed at 100 K before the DLTS measurement and subsequently warmed up to 300 K. The solid line spectrum was taken in a temperature scan from 300 K to 60 K, whereas the dotted line spectrum was taken immediately after the completion of the solid line spectrum in a reverse temperature scan from 60 K up to 300 K. Only the spectral region 80 K to 200 K is shown here.

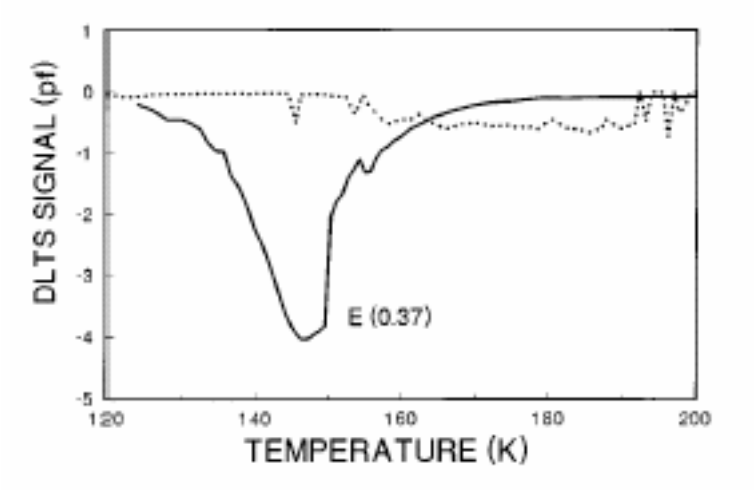


Figure 4.6: The DLTS spectra measured in a zero-biased capacitor at a filling pulse of -4V in a temperature scan from 60 K to 300 K (solid line) followed immediately by another DLTS measurement with a temperature scan from 300 K to 60 K (dotted line). Only the spectra between 200 K and 120 K is shown. Prior to taking the solid line DLTS spectrum the capacitor was FN-stressed at 50 K and subsequently measured from 60 K to 300 K.

Chapter 5

Thin Silicon Dioxide: (III) Hot Carrier Stress Reliability

5.1 A Brief Overview of Hot Carrier Induced Damage on Thin Oxide MOSFETs

5.1.1 Hot Carrier Stress Induced Damage

Ever since the introduction of MOSFETs in the mid 1960s, thanks to tremendous progress in lithography technologies, the channel length used in the state-of-the-art CMOS IC technology has been reduced by a factor of 0.7 every 3 years, allowing more and more complex functions on the chip. Five years ago, the 0.5μm channel length was still an industrial standard, while nowadays MOSFETs with 0.25μm and 0.18μm channel length are widely used. This channel length reduction of the MOSFETs has led to an increase of the switching current (essentially inversely proportional to the channel length), and thus to an increase in the circuit speed [96]. However, the power supply voltage has not been able to keep up with this minimization. External power supply is usually still kept at 5.0V while internal power supply has been reduced to only 3.3V or 2.5V. This results in increasing high electrical field in the drain region of the transistor, giving rise to the so-called *"hot-carrier induced reliability problems"* [97]**.**

5.1.2 The Physics of Hot-Carrier Interactions

During the device operation or fabrication, the gate bias V_g is usually smaller or close to the drain bias V_d. The inversion layer at the drain side is, therefore, much weaker than that at the source side, which causes the majority of drain-source voltage to drop near the drain region. The corresponding electrical field can be as high as 10^4 V/cm and the traveling carriers can gain high kinetic energy ~ kT_e with the thermal temperature T_e in the range of 1000-10000 K. These carriers are, hence, called 'hot carriers' (HCs) [97]. Some of these hot carriers will inevitably generate electron-hole pairs through impact ionization. Depending on the polarity and magnitude of the bias, these new electrons/holes can either be collected by the substrate and the drain, or overcome the Si/SiO_2 barrier and be injected into the oxide, thereby creating interface and oxide traps during the process.

There are ≅Si-OH, ≅Si-O-Si≅, and ≅Si-Si≅ bonds in the SiO_2-Si system, whether the fabrication uses H_2 annealing, grows SiO_2 in the HCI gas, or adopts a dry-wet-dry process. During the hot carrier induced degradation, hot carriers will break the above bonds and form $\cong Si^+$ and $(SiO)^+$ positive traps at the interface as well as $\cong Si^+$ inside the bulk oxide. In addition, by breaking ≅Si-O-Si≅ and ≅Si-Si≅ bonds, hot holes can also form the interface states $O_3 \cong Si$ and $Si_3 \cong Si$ [98], and hot electrons can form the neutral positive charge traps Si_2O, SiO and Si_2O_3, as well as the neutral negative charge traps Si_3 $\cong Si\text{-}O^+$ and $O_3 \cong Si\text{-}O^+$ [99, 100]. Whether these neutral traps serve as negative or positive charge centers will depend on whether they capture electrons or holes.

Generally speaking, it requires more energy to create new interface traps than to charge already existing traps. In the first case, hot carriers need to have enough energy to jump over an interface potential barrier and break a Si-O, Si-Si, Si-H or a Si-OH bond. In the latter case, however, hot carriers only have to acquire enough kinetic energy to overcome the interface barrier (instead of breaking a bond) and be trapped in the SiO_2 by already existing traps (no trap generation) [101].

5.1.3 Characterization and Prevention of Hot Carrier Damage

There are a few approaches to reducing hot-carrier degradation in scaled MOS devices. These approaches are : 1) development of hot-carrier resistant device structures such as LDDs (lightly doped drains where part of the drain voltage is dropped in a relatively lightly doped drain extension not covered by the gate), DDDs (double diffused drains), and GOLDs (gate-drain overlapped LDDs [102]) and 2) reduction of power supply voltage. The first approach increases the process complexity while the second one must overcome a low-speed problem. Another new approach is to make good use of AC (alternating current) effects, including the duty ratio [103].

However, it is not still easy to predict the degree of the HC induced degradation. The physical dimension of MOS transistors, the existing defects from different processing, the relative electric field between drain and gate, all of these can affect the amount and energy of hot carriers, thus affect the subsequent interface/oxide trap creation. This makes the characterization and modeling of hot carrier induced damage quite difficult. The detailed mechanisms that lead to oxide degradation are still

controversial, and it is still not possible to predict the degradation of a MOSFET by simulation.

5.2 On the Experimental Procedure

The p- and n -channel MOSFETs used in this study were fabricated on 200 mm epitaxial silicon substrates using the SEMATECH 132AZ mask set. The channel length and width for these transistors were 0.35μm. The thickness of the gate oxide, grown at 900°C in dry O_2 ambient, was 65Å or 45Å. The poly-Si gate definition etching, the contact etching and the metal etching employed a Cl_2/HBr, a CHF_3/CF_4 and a $BCl_3/N_2/Cl_2$ based chemistries, respectively. All etching processes were performed using commercial reactive-ion-etching and transformer coupled plasma tools. After metallization, all transistors were given annealing in forming gas (6% H_2 and 94% N_2) at 400 °C for 30 minutes. More on the experimental procedure used are given in Chapter 2 of this thesis.

5.3 Experimental Results and Discussion

5.3.1 Threshold Voltage and Maximum Transconductance

Hot carrier injection into the gate oxide and oxide/Si interface in a MOSFET is primarily affected by the ratio of the gate voltage (V_g) to the drain voltage (V_d), the gate

voltage polarity, as well as the potential barrier for carrier injection from Si into the oxide. The potential barrier is 4.8 eV for holes and 3.2 eV for electrons. Hence, in what follows we evaluate the changes in V_{th} and G_m brought about by hot carrier stress using different gate voltage and drain voltage combinations and polarities. Also the transistor type is very important in determining the hot carrier induced damage to the oxide and interface as we will discuss below. Up until now, research is focused on n-channel MOSFET (NMOS) transistors since they are believed to be more prone to hot carrier induced damages [97, 105-107]. However, recent reports have shown that in deep sub-micron p-channel MOSFET (PMOS) transistors, the HC degradation mechanism becomes more complicated, e.g, in addition to mainly oxide-charge generation, interface traps become much more significant [108, 109]. Therefore, most of the results and discussion presented in this section will focus on the effects observed in PMOS transistors. Parallel tests have also been performed on similar NMOS transistors and the results will be discussed where it is considered necessary.

Figure 5.1 shows the threshold voltage V_{th} and maximum transconductance G_m measurement results on PMOS transistors subjected to HC stress with gate bias V_g ranging from 1/8 V_d up to V_d. Each HC stress was applied for a 10 s period. To ensure the HC stress conditions are comparable in samples with different oxide thickness, V_d was selected as -8V for PMOS transistors with 65 Å-thick gate oxides and -5V for PMOS transistors with 45 Å-thick gate oxides. This way the substrate currents during the stress were at the same level in transistors with both values of gate oxide thicknesses. The x-axis in *Figure 5.1* shows the ratio of V_g/V_d, whereas the y-axis represents the percentage

changes of V_{th} or G_m after the HC stress. The values plotted for changes in V_{th} and G_m are the mean values in cumulative plots obtained from measurement results made on more than 10 transistors.

From *Figure 5.1* , in both PMOS transistors with 45 Å-thick or 65 Å-thick gate oxides, when V_g is between 1/8 V_d and 1/2 V_d, V_{th} decreases while G_m increases after HC stress. The maximum degradations of V_{th} and G_m take place at V_g/V_d between 0.2 and 0.4. When V_g is biased above 1/2 V_d, the changes in both V_{th} and G_m become smaller and finally tail off at V_g/V_d approaching 1.The degradation in PMOS transistors with 45 Å-thick oxides occurring after HC stress is significantly less severer than that in PMOS transistors with 65 Å-thick oxides.

From *Figure 5.1* one observes two distinctly different trends in V_{th} and G_m. In the first trend which occurs at low V_g with $V_g/ V_d < 0.4$ the magnitude of V_{th} decreases, whereas G_m increases with the HC stress. In the second trend, however, the picture is somewhat reversed at higher V_g and $V_g/V_d \geq 0.4$ where V_{th} increases slightly with no significant change in G_m, especially at V_g approaching V_d. There are two types of carrier injection in PMOS under different gate bias: electron injection occurs at low V_g level while hole injection occurs at V_g close or equal to V_d. At low V_g the electron gate current is at its peak, and is mainly responsible for creating negative charge states in the oxide by electron trapping, as well as interface states through bond breaking [104]. This kind of electron trapping or interface traps result in channel shortening, hence increase drain current (thus increase G_m), and indirectly decrease $|V_{th}|$, all of these effects are witnessed in *Figure 5.1.* When $V_g>1/2$ V_d, the gate current mainly consists of hot holes. However,

the degradation from hole injection is less severer. This can be due to a high barrier height in the Si/SiO_2 interface, lower mobility in the oxide layer, shorter mean-free path in the silicon, or a combination of the three. We, therefore, see the less degradation in the higher V_g bias range of *Figure 5.1* . We also note that in PMOS with gate oxide thickness of 45 Å we observed a positive shift in V_{th} when $V_g = V_d$. This is likely caused by the creation of positive oxide charge buildup when the hole injection is at peak value: this same observation was previously made by a different group [105].

The substrate current was monitored during the HC stress, as shown in *Figure 5.2*. It is clear from comparing *Figure 5.1 and Figure 5.2* that the degradation of transconductance G_m relates to the amplitude of the substrate current. They both reach their peak values between V_g/V_d between 1/3 and 1/2 and drop in values at lower or higher V_g bias. The shift of G_m can be caused by oxide charge traps and/or interface states. Notice that at V_g/V_d at 1/3 to 1/2, the gate current consists of both hot electrons and holes. A commonly adopted assumption is that the hole injection can cause positive charge trapping in the oxide close to the $Si\text{-}SiO_2$ interface, which acts as the precursor to--and transforms into--an interface state when an electron is injected into the oxide and trapped on this site [106].

The results of similar HC stress experiments on n-channel MOSFETS (NMOS) are shown in *Figure 5.3*. In these experiments changes observed in V_{th} are insignificantly (< 0.5%) small and are considered to be within the experimental error in determining V_{th}. However, much larger changes, up to ~ 25%, are observed in G_m are shown in *Figure 5.3*. The highest degradation in G_m occurs below $V_g/V_d < 0.5$ and becomes smaller when

V_g/V_d approaches 1. These results are consistent with earlier observations on HC stressed NMOS [105-107]. The absence of observable effects on V_{th} indicates that most of the HC degradation is, presumably, within the drain region of the channel and the oxide and that the majority of the bulk gate oxide is not appreciably affected.

Although charged oxide traps and interface states can be monitored using changes in V_{th} and G_m induced by the HC stress, it is often very difficult to separate the effects of oxide traps and interface states on these two transistor parameters. A more elaborate measurement method such as charge pumping provides more insight into interface states and enables the distinction between interface and bulk oxide carrier traps. The following section presents and discusses post-HC-stress charge pumping results obtained in our PMOS and NMOS transistors.

5.3.2 Charge Pumping (CP) Results and Analysis

In the event of HC stress most MOSFETS are not stressed uniformly over the entire channel. The degradation will be rather localized in the channel, mostly near the drain. The traditional transistor parameters, namely V_{th}, G_m, and S are not well suited for the study of such non-uniform degradation. For a uniformly damaged transistor, a shift of the V_{th} directly indicates a change in the oxide charge, and a change of the sub-threshold swing S suggests a corresponding change in the interface trap density D_{it} across the channel. However, for a non-uniformly degraded transistor, the analyses of these parameters become much more complicated, e.g. a change in S can also be caused by a localized fixed oxide charge in addition to changes in D_{it}. Therefore, the use of charge

pumping (CP) becomes important in understanding and analyzing the HC induced damage to our transistors [110].

Figure 5.4 shows the charge pumping results on the PMOS transistors in which the gate oxide thickness is 45 Å or 65 Å. The CP plots shown were obtained in PMOS devices subjected to HC at different V_g. When $V_g/V_d = 1/8$, the CP current is much higher than that measured in the unstressed (virgin) PMOS and the peak charge pumping current, I_p, is almost an order of magnitude higher than that in the virgin PMOS. I_p starts to decreases when V_g is biased closer to the drain voltage during the HC stress. In the PMOS with the oxide thickness of 65 Å the decrease of I_p is monotonous as V_g/V_d increases and approaches 1, whereas in the PMOS with the 45 Å thick gate oxide I_p decreases with increasing V_g/V_d beyond 1/8 and reaches its minimum value at $V_g/V_d = 6/8$, I_p then turns around and slowly increases again as V_g/V_d increases above 6/8. Moreover, in the PMOS with the 65 Å-thick oxide the CP current curve is much broader and its peak/edge shifts significantly towards positive base voltage, V_{base}, when V_g is at its lower end, increasing from $V_{base} = 0.4V$ at $V_g/V_d = 1$ to $V_{base} = 1.5V$ at $V_g/V_d = 2/8$. Such a shift is not present in the PMOS with the 45 Å-thick oxide. Instead, we see an extra shoulder of the CP current when V_g/V_d is at 1/8 and 3/8.

From CP it is possible to find out the spatial distribution of the interface carrier traps across the channel by intentionally floating the drain or the source connections during the measurement. *Figure 5.5* shows the CP results of such measurements on PMOS transistors with 45Å-thick gate oxide HC stressed at $V_g/V_d = 7/8$ (*Figure 5.5* a) and $V_g/V_d = 1/8$ (*Figure 5.5* b). The results of three measurement schemes are shown: (i)

drain, source and substrates tied together and jointly grounded, (ii) the drain and substrate grounded while the source is left floating, and (iii) the source and substrate grounded while the drain is left floating. In the case with $V_g/V_d = 7/8$, shown in *Figure 5.5* (a), I_p increased from 60pA (curve 4) to 230pA (curve 1) after the HC stress. No or very little shift in V_{base} is observed for the CP current. Floating the source (curve 3) or the drain (curve 2) during the CP measurement does not affect the shape of the CP current curve. In contrast, in *Figure 5.5*, I_p increases to 540pA (curve 4) after a HC stress at $V_g/V_d = 1/8$. More importantly, however, is the large "shoulder" appearing at higher V_{base} values. This shoulder is also present in CP measurements taken with a floating source, and the CP curves obtained with substrate, drain and source grounded, and with source floating are exactly identical. The CP curve with the drain floating (curve 2) is markedly different in this PMOS : the shoulder, which was present in the grounded source-drain-substrate and in the floating-source CP schemes, is now absent with the drain floating during the CP measurement. A sharp and abrupt drop in the CP current at the high V_{base} is seen. To understand these features in our CP results we will analyze CP current output for a hypothetical case of a non-uniformly damaged channel in a PMOS.

Figure 5.6 shows typical CP current observed in a non-uniformly degraded channel in a PMOS [110]. More specifically, the CP current in *Figure 5.6* is more typical of a channel with two distinctly degraded regions. Region I of the channel has a length of L_1, a threshold voltage V_{th1}, and an interface state density D_{it1}. Region II has a length of L_2 and is characterized by a threshold voltage V_{th2} and interface state density D_{it2},. The assumption made in *Figure 5.6* is that region II is more degraded than region I which

translates in terms of the threshold voltage as $V_{th2} > V_{th1}$. Curves I and II of *Figure 5.6* represent the separate CP contributions of regions I and II, respectively.

When $V_{FB1}-\Delta V_A<V_{base}<V_{FB2}-\Delta V_A$, and $V_{th1}<V_{base}+\Delta V_A<V_{th2}$ (ΔVA is the pulse height), region I is pulsed from weak accumulation to inversion. Meanwhile, region II stays in inversion. In this case only region I contributes to the CP current and Curve III = Curve I. However, when $V_{FB2}-\Delta V_A<V_{base}<V_{th1}$, and $V_{base}+\Delta V_A>V_{th2}$, both region are pulsed from accumulation to inversion during the CP measurement and, therefore, Curve III = Curve I+ Curve II. In this case the resultant CP curve III is highly unsymmetrical and possesses a clear shoulder towards its higher V_{base} edge. Finally, when $V_{th1}<V_{base}<V_{th2}$, and $V_{base}+\Delta V_A>V_{th2}$, region I stays in accumulation and does not contribute any CP current. Meanwhile, region II is pulsed from accumulation to inversion, and since region I is switched off ($V_{th1}<V_{base}$), the only source that can supply recombination holes to region II is the drain. If the drain is connected during the CP measurement, the CP current curve III = Curve II at $V_{base}>V_{th1}$. However, if the drain is left floating no holes will be supplied to region II and the CP current will be abruptly cut off at $V_{base}>V_{th1}$, as shown in Curve IV.

The hypothetical PMOS transistor CP output analyzed above is, apparently, very similar to our results in *Figure 5.4* and *Figure 5.5.* The implications are, hence, that our PMOS transistor with the thinner (45 Å) gate oxide is non-uniformly degraded by the HC stress when Vg/Vd ~ 1/8. This non-uniform degradation may arise from two degraded regions along the device channel with the region adjacent to the drain being the highly degraded. This degradation takes the form of negative charge buildup therein. The PMOS

transistor with the thicker gate oxide of 65 Å are not similarly degraded : HC stress is seen to uniformly damage the interface across the entire channel in these transistors. Seemingly this is also the case with the PMOS transistors with the 45 Å-thick gate oxide at V_g/V_d approaching unity.

Figure 5.7 shows the CP results of a 'double stress' test performed on the PMOS transistors. In *Figure 5.7* the stress sequence starts with a 10 s HC stress at $V_g/V_d = 2/8$ followed by a 10 s HC stress at $V_g/V_d = 1$, whereas in *Figure 5.8* the stress sequence is reversed. The CP measurements on the transistors were performed before the application of the stress, after the application of the first stress, and after the application of the second stress. In *Figure 5.7*after first stress at $V_g/V_d = 2/8$, the CP current increases with a broad shoulder expanding into the positive base voltage side as discussed earlier. After the second stress at $V_g/V_d = 1$, the CP current further increases with no apparent further extension or contraction in the shoulder region on the higher side of V_{base}. The intention in these experiments is to explore the possibility of the second HC stress curing some of the effects of the first stress. Particularly, the negative charge buildup in the drain side created by the first stress may be significantly compensated by possible hole injection during the second HC stress, thereby causing a contraction in the shoulder of the CP curve. Clearly this did not happen. Instead more interface traps are formed by the second stress as witnessed by the higher I_p. The CP results in *Figure 5.8* are more or less similar to those in *Figure 5.7* indicat*ing* that the sequence of the stress does not affect the overall outcome.

The total number of interface traps in the channel is proportional to the maximum of the recorded CP substrate current I_{cp}, while the threshold voltage and the flat-band voltage, which are determined by the fixed oxide charges and the charges in the interface traps, can be directly extracted from the edge of the curves [47-50]. An increase in the level of the CP current in the above stress cases is, therefore, an indication of an increase of the interface trap density after HC stress. A shift of the curve peak/edge towards more positive base voltages is indicative of a net negative charge buildup in the oxide or near the SiO_2/Si interface. These findings are consistent with the previous V_{th} results shown in *Figure 5.1*.

From the results of V_{th} and G_m in *Figure 5.1*, the PMOS transistors with 45 Å-thick gate oxide show less damage than the PMOS transistors with the 65 Å-thick oxide as a result of HC stress. Also from *Figure 5.4*, I_{cp} for PMOS transistors with the two different gate oxide thicknesses, I_{cp} for transistors with the thicker oxide show a much larger shift towards positive base voltage side during the CP measurements. This is an indication of more negative charge buildup induced by the HC stress near the drain edge of these transistors. Overall one may conclude that the PMOS transistors with the thinner gate oxides are more tolerant to degradation induced by HC stress. This may be attributed to the direct tunneling in the thinner oxide transistors, which causes less carrier trapping and collision, e.g. trapped electrons can easily tunnel out of the oxides. The interface trap density, on the other hand, is similar in HC stressed transistors with different gate oxide thicknesses. This is because interface states are, presumably, generated by bond breakage

at the Si/SiO_2 interface which proceeds with the same probability irrespective of the gate oxide thickness.

It is worthwhile to point out that we also observed similar results in NMOS transistors that were subjected to hot carrier stress. Examples of the results observed are given in *Figure 5.9*. As in PMOS maximum degradation takes place at low gate voltages and most stress-induced traps are localized near the drain side.

5.4 Summary

In this chapter, we have examined the HC stress induced damage on PMOS transistors under different gate bias. The maximum degradation takes place at stress conditions where the drain and gate voltages relate according to $0<V_g<1/3V_d$. Both, negatively-charged oxide traps and interface states are created by hot electrons and holes. Most of the HC induced degradation is located at the drain side of the device. However, when the gate bias is at or close to drain bias, the HC damage consists of interface states that are distributed evenly along the PMOS channel. It is also observed that the nature of the HC induced damage changes when the gate oxide is scaled down: in the transistors with 45 Å-thick gate oxide, the principal damage has switched from oxide charge trapping to interface damage, and the damage is no longer localized near the drain side of the PMOS.

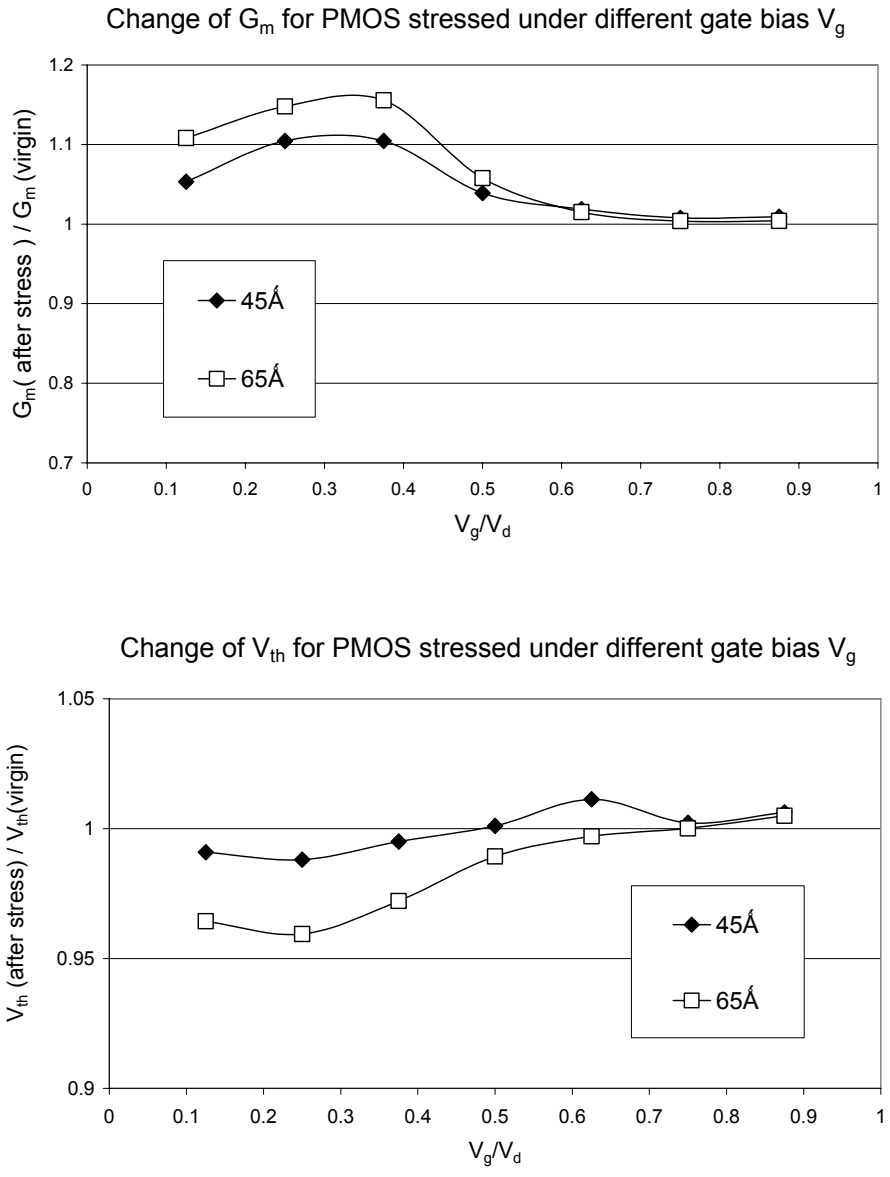


Figure 5.1: Threshold voltage and maximum transconductance results for PMOS samples under different HC stress conditions. (t=10 s, V_d=-8V for transistors with 65Å-thick gate oxide, t=10 s, V_d=-5V for transistors with 45Å-thick gate oxide, the gate bias V_g varies from 1/8 V_d to V_d)

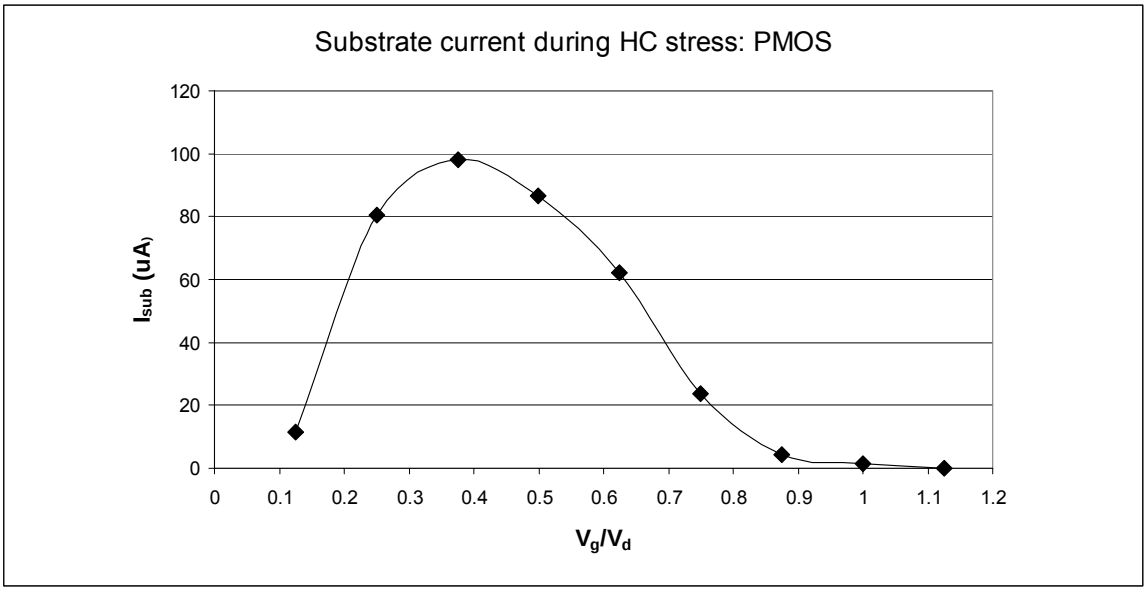


Figure 5.2: Substrate current for PMOS transistor with 45 Å-thick gate oxide during HC stress under different gate bias V_g,

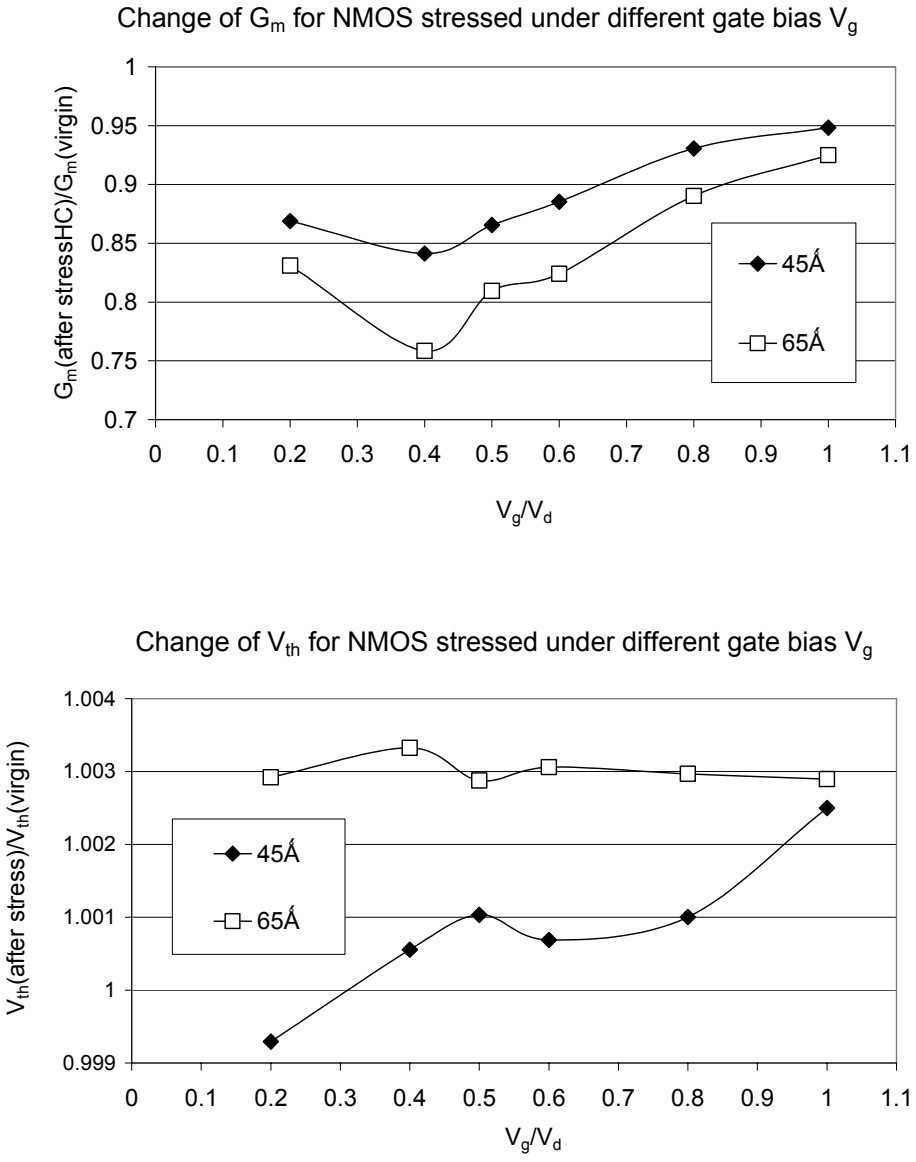
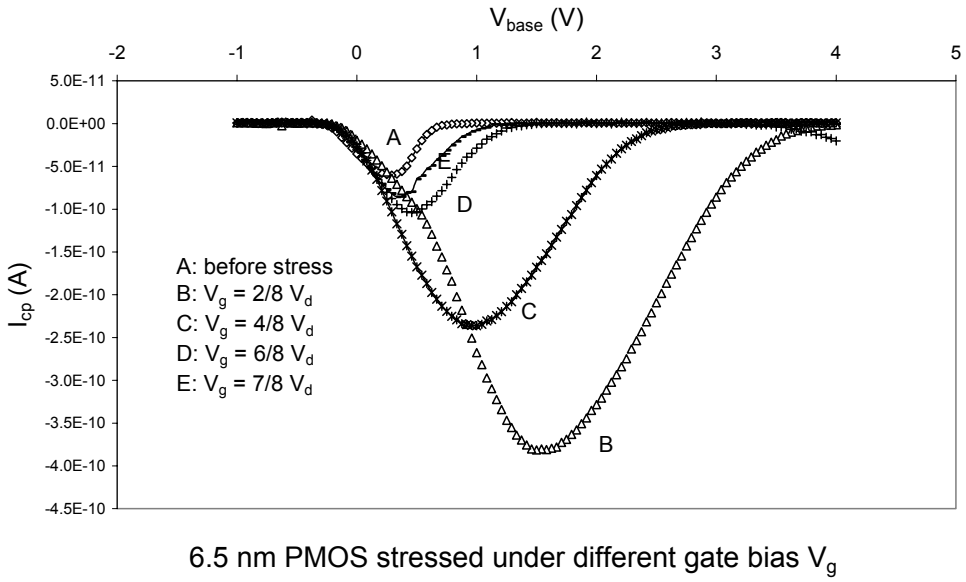
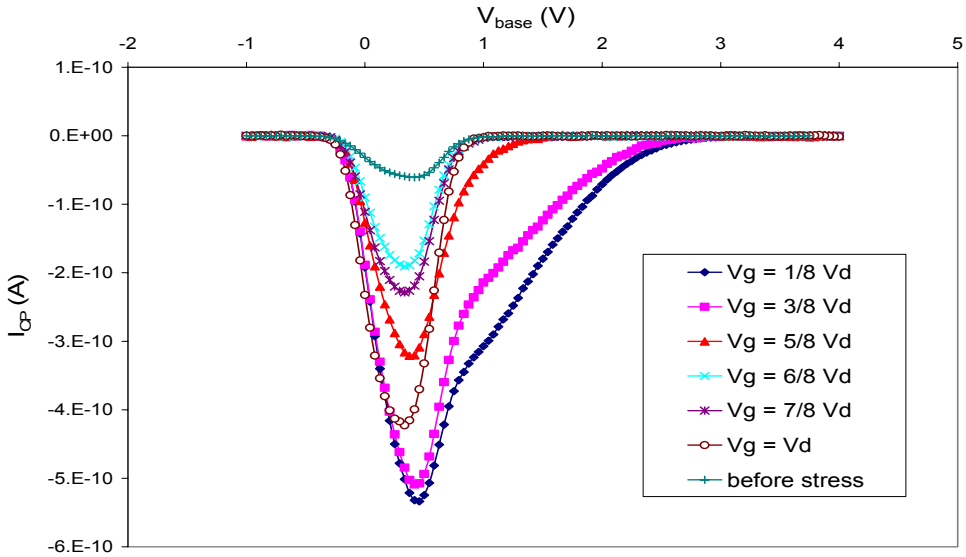


Figure 5.3: Threshold voltage and maximum transconductance results for NMOS samples under different HC stress conditions. (t=10 s, V_d=5V for transistors with 65Å-thick gate oxide, 3.5V for transistors with 45Å-thick gate oxide, the gate bias V_g varies from 1/5 V_d to V_d)



6.5 nm PMOS stressed under different gate bias V_g



4.5 nm PMOS stressed under different gate bias V_g

Figure 5.4: CP results on PMOS transistors with different oxide thickness. The HC stress condition were t = 10 s, V_d=-8V for samples with 65Å-thick gate oxide, V_d=-5V for samples with 45Å-thick gate oxide, V_g varies from 1/8 V_d to V_d.

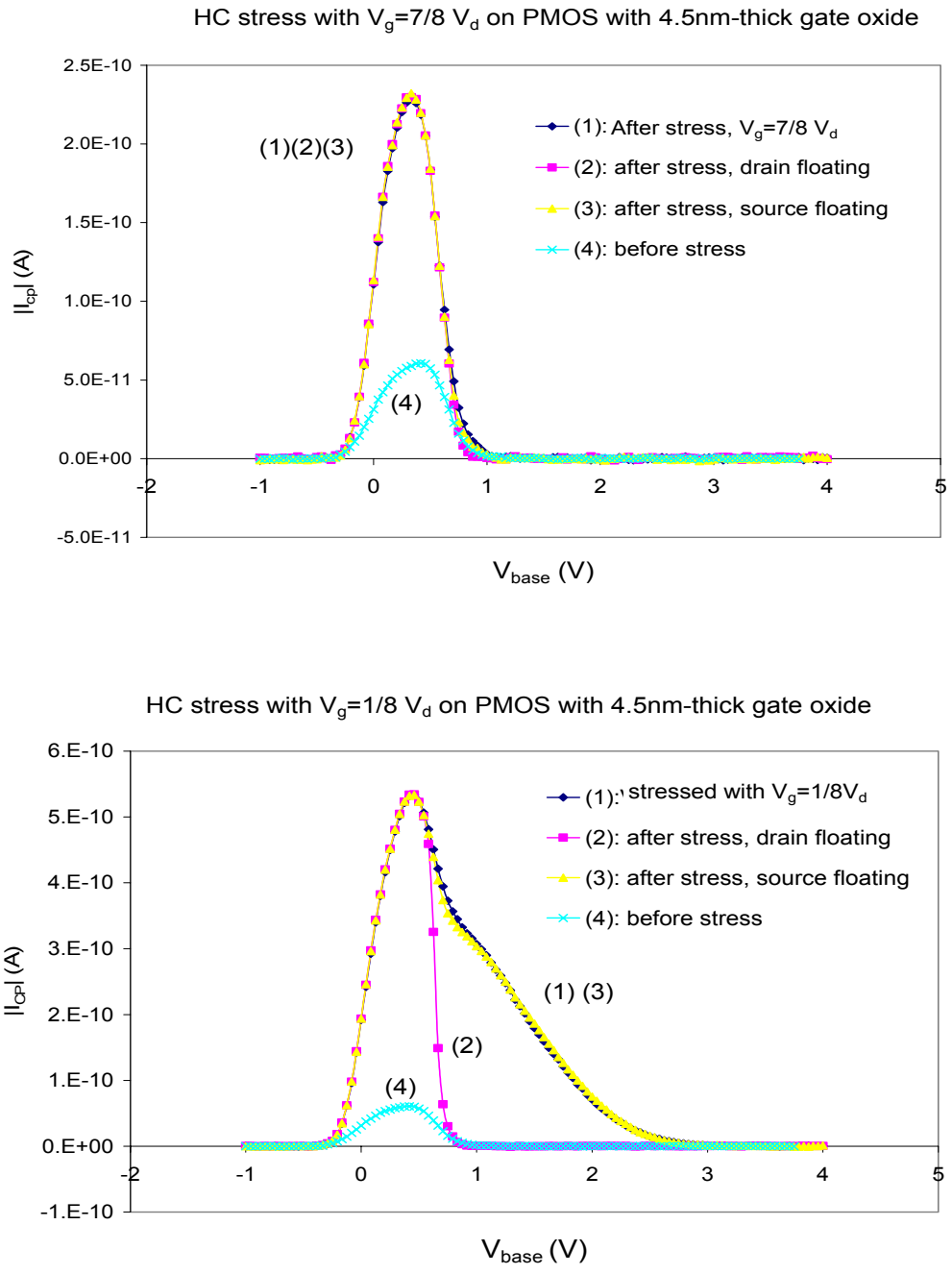


Figure 5.5: CP measurement on PMOS transistors with 45 Å-thick gate oxide under different source/drain configuration (Absolute I_{cp} current value is used in this plot)

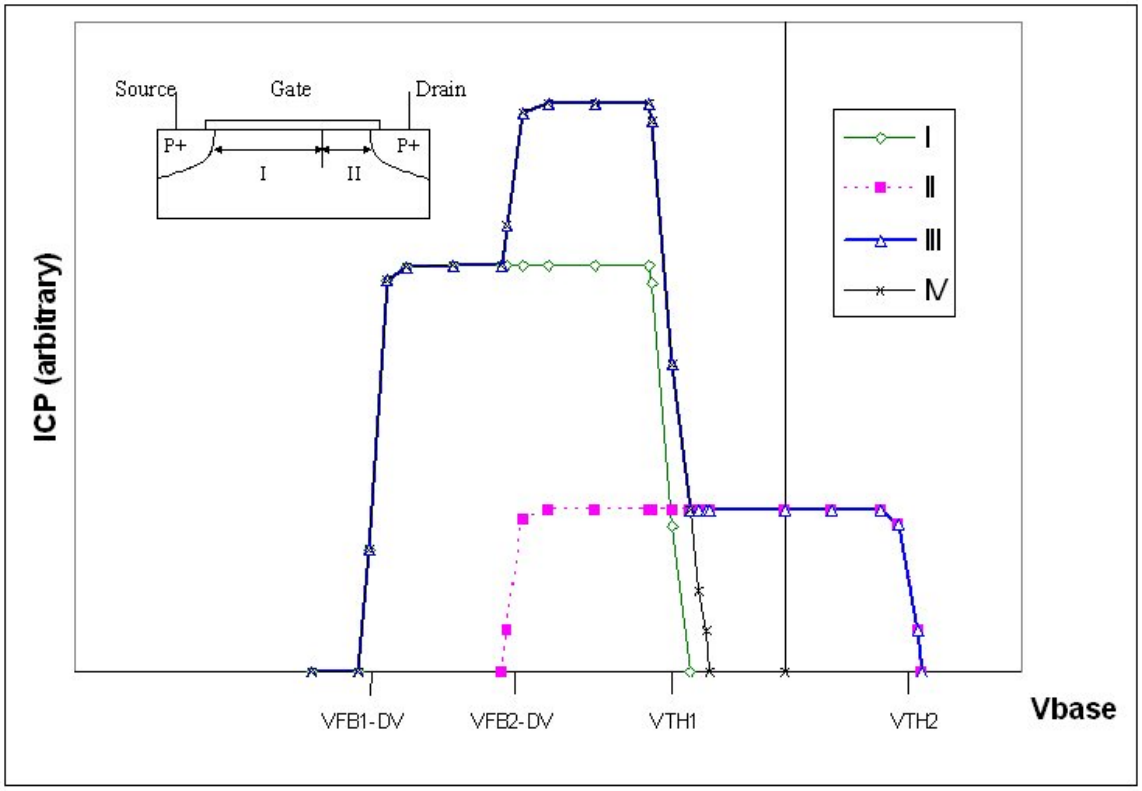


Figure 5.6: Charge Pumping curves for a PMOS transistor with nonuniformly distributed degradation. Region I of the channel is not degraded, Region II has negative trapped charge and increased interface trap desity. Curve I: CP curve of region I; Curve II: CP curve of region II; Curve III: CP curve of the whole transistor; Curve IV: CP curve of the whole transistor with drain side floated. DV is the pulse height ΔV_A

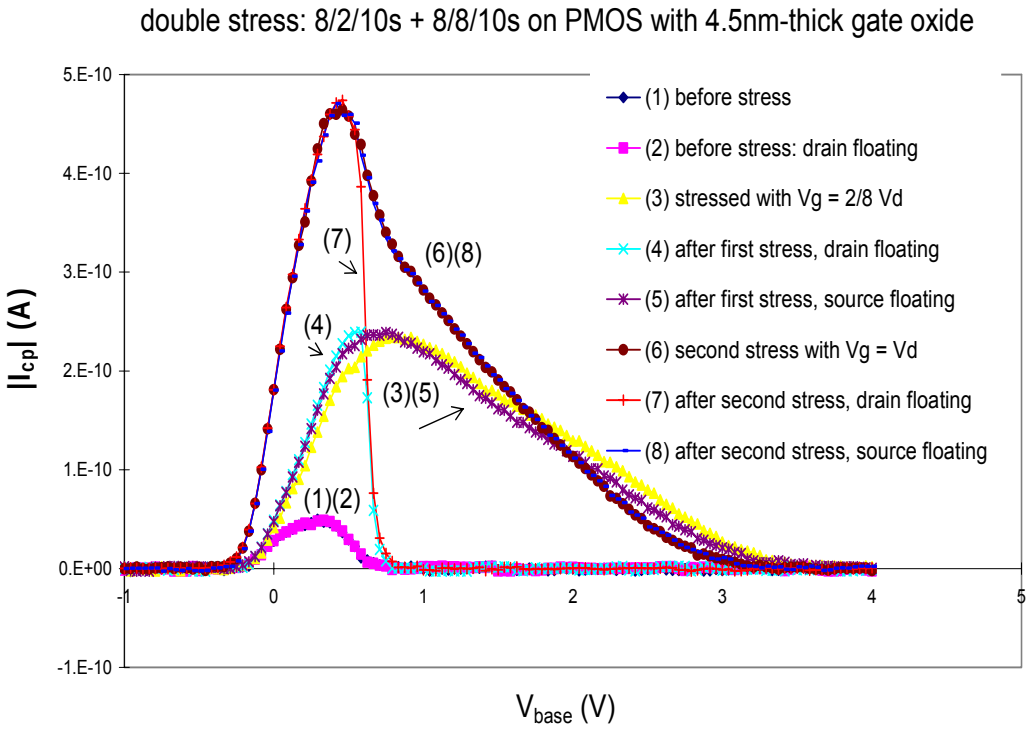


Figure 5.7: CP measurement on PMOS transistors with 45Å-thick gate oxide. Sample was first subjected to 10 s HC stress with V_g=2/8 V_d, after CP tests, it was then subjected to another 10 s HC stress with V_g=V_d. Different source/drain configurations were adopted during the CP tests as indicated in figure. (Absolute I_{cp} value is used in this plot)

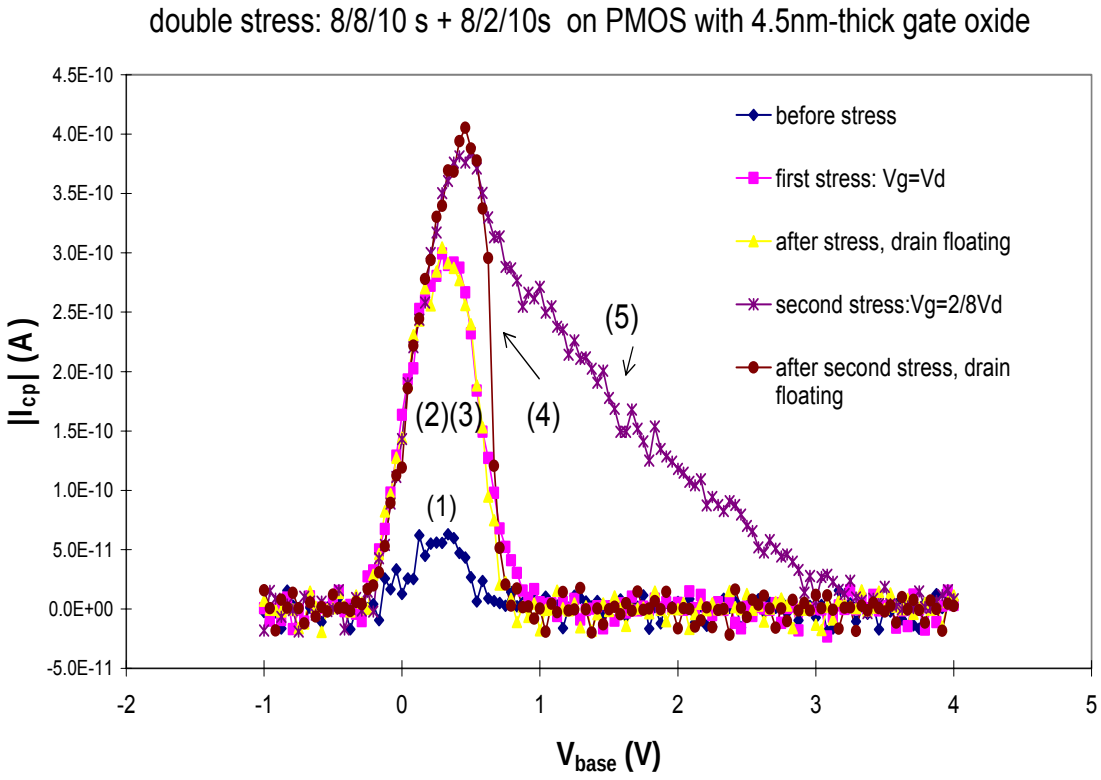


Figure 5.8: CP measurement on PMOS transistors with 45Å-thick gate oxide. Sample was subjected to 10 s HC stress with $V_g=V_d$, after CP tests, it was then subjected to another 10 s HC stress with $V_g=2/8V_d$. Different source/drain configurations were adopted during the CP tests as indicated in figures. (Absolute I_{cp} value is used in this plot)

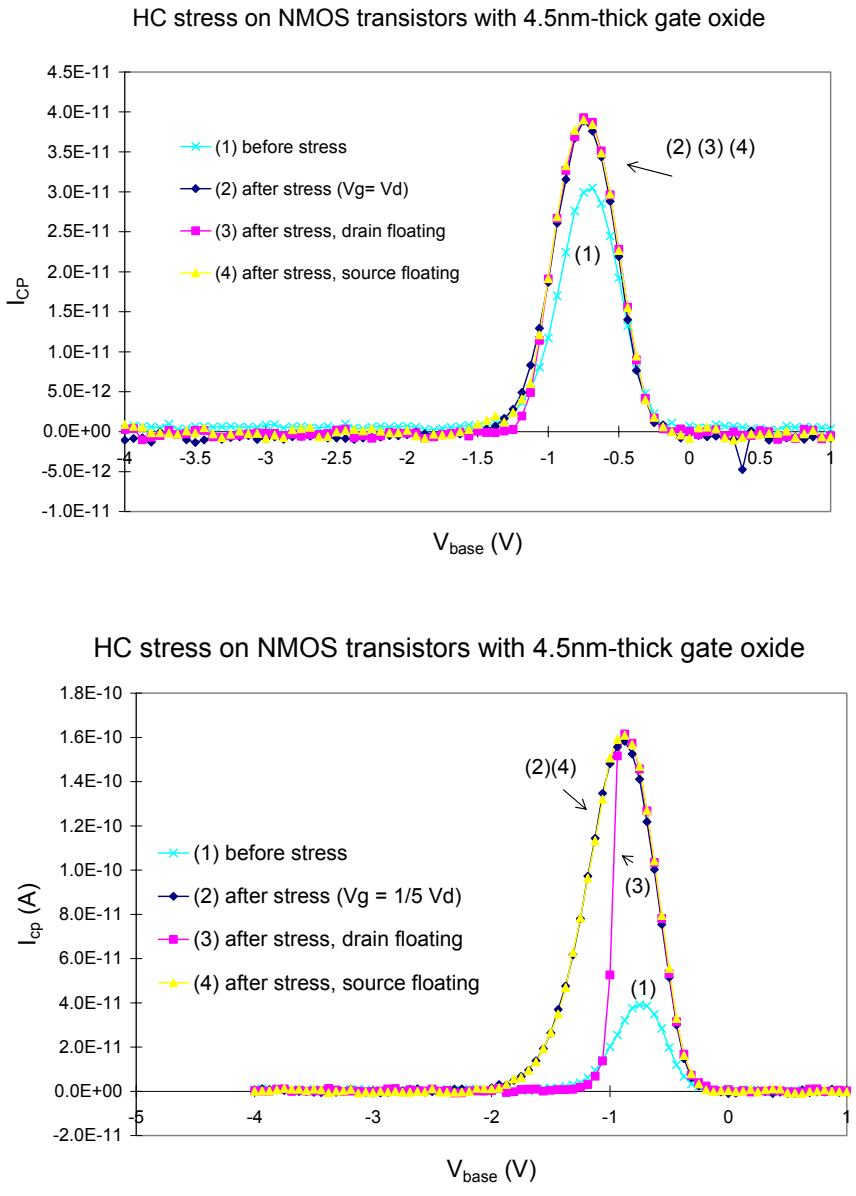


Figure 5.9: CP results on NMOS transistor with 45 Å-thick gate oxide thickness. (a) Sample was subjected to HC stress of 10 s, $V_g=V_d$; (b) sample was subjected to HC stress of 10 s, $V_g=1/5\ V_d$. CP measurements were performed with drain floating, source floating, respectively in both cases

Chapter 6

Electrical Studies of Selected Metal/High-k Gate Dielectric/Si Material Systems

6.1 Introduction

The ever increasing CMOS miniaturization makes it necessary to use high dielectric constant (high-k) materials to replace thermally-grown silicon dioxide as gate dielectrics in the gate stack systems of MOSFETs. However, one of high-k dielectric processing challenges is to control the forming of an interfacial layer between the high-k dielectric and the silicon substrate. Thermodynamic stability requires that high-k materials like TiO_2 and Ta_2O_5 react with the underneath silicon and form silicate layer during the material deposition [111]. Other materials, such as HfO_2 and ZrO_2, although are thermodynamically stable on silicon, may introduce interfacial layers during post-deposition annealing in oxygen ambient [112]. The interfacial layer may be composed of SiO_2 or/and various silicates, depending on the high-k dielectrics chemistry and process conditions [111-114]. Since it usually has a thickness of 10 to 30 Å and k values below 10, the interfacial layer imposes a severe limit on the effective oxide thickness effective oxide thickness (EOT) of the gate dielectric. Although it is possible to eliminate this interfacial layer by direct deposition of metal layer (Hf, La) on the silicon substrate

followed by low temperature or rapid thermal annealing (RTA) re-oxidation process, this process usually results in dielectrics with high leakage current and interface state density (D_{it}). Moreover, post-deposition annealing can still introduce an interfacial layer and, thereby, nullify all interfacial layer elimination efforts [112,115].

Based on the preceding discussion several research groups, therefore, focus on reducing the thickness of this interfacial layer. One common practice is to perform an NH_3- or NO-based nitridation step before the metal deposition. It has been reported that this intentionally grown interfacial layer with sufficient nitrogen concentration is able to suppress further reaction between metal and silicon substrate and to inhibit metal diffusion into the substrate during the deposition and subsequent annealing process: thus silicon surface nitridation may result in a favorable and smaller EOT [116]. Moreover, this nitridated silicon interfacial layer is believed to be able to reduce the interface trap density D_{it} and leakage current density [117]. In contrast, there are reports showing that NH_3 nitridation degrades the high-k stacks by incorporating hydrogen in the oxides which significantly increases electron trapping and thus reduces the carrier mobility in the channel region of the MOSFET [118,119].

For these reasons we found it necessary to thoroughly examine the electrical effects of this nitridated interfacial layer on the high-k dielectric stack systems. Different high-k dielectrics, $SrTa_2O_6$, $ZrSiO_4$, and HfO_2 prepared by liquid source misted chemical deposition [29] and TiO_2 layers prepared by chemical vapor deposition were used in our study. We will be showing that, besides the thickness, the quality of this interfacial layer can greatly impact the EOT of the high-k stack systems. Careful analysis of the

capacitance-voltage results is emphasized and the appropriate use of these results in the estimation of effective k values and EOTs is demonstrated and critically discussed. We will also discuss the role of this nitridated layer in preventing the occurrence of carrier traps at the Si/high-k interface and in the silicon bulk.

In the last part of this chapter, we would also try to address another important issue during the high -k material deposition: the possible cross contamination between high-k materials growth and traditional silicon dioxide growth. As we discussed earlier in Chapter 1, one of the most important requirements on a replacement gate dielectric is compatibility with conventional CMOS process.

6.2 On the Experimental Procedure

$SrTaO_6$ and $ZrSiO_4$ layers were deposited onto p-type (100) Si wafers of 2- 15 Ω cm resistivity using the liquid source misted chemical deposition (LSMCD) technique [29]. The LSMCD tool used in the depositions belongs to professor Ruzyllo's group and is housed in Penn State's Nanofabrication facility. Prior to the high-k deposition, the wafers were treated with anhydrous HF/methanol to remove native oxide. Following the native oxide removal some of the wafers were also subjected to UV/Cl_2 and UV/NO exposures to remove fluorine on Si surface and to grow a thin layer of nitridated oxide. After the high-k deposition, the wafers were subjected to a 20-minute 200 °C anneal and several pulses of 3-sec 700 °C spike anneal in oxygen to solidify the film. The gate electrodes for the capacitor structures were made of e-beam evaporated Pt and had areas

of $1x10^{-4}$ to $1x10^{-2}$ cm^2. For comparison reasons, a 1000 °C thermally-grown 200-Å-thick gate oxide metal-oxide-Si (MOS) capacitors were made on p or n-type Si substrates.

The TiO_2 sample preparation began with a backside boron implantation (60Kev, $3.5x10^{15}cm^{-3}$) of a p-type wafer. After RCA and piranha clean, the residual oxide was stripped using buffered HF. Prior to TiO_2 deposition, NH_3-nitridation of the Si surface was performed on most wafers at 750–850°C resulting in a 20–30 Å-thick nitridated silicon layer. Following nitridation MOCVD (500 ºC, 1 Torr) was used to deposit TiO_2 layers at a rate of 8Å/min. The sample was then annealed at 650°C in O_2. A 2000 Å thick platinum film was sputtered on the TiO_2 layer as a metal gate in the resulting metal-Insulator (high-k dielectric)-Si (MIS) capacitor. Finally post metallization annealing was performed at 450ºC in a H_2 ambient.

High resolution transmission electron microscopy (HRTEM) was used to measure the deposited dielectric layer thickness. Both $SrTaO_6$ and $ZrSiO_4$ were found to be 5.0-7.4nm thick on a nitridated interfacial layer which was 2.0nm thick. TiO_2 samples had varying dielectric thicknesses, which are listed in *Table 6–1.* In TiO_2 samples without pre-deposition NH_3-nitridation the interfacial layer thickness was about 2.0nm to 3.0 nm, whereas in samples with NH_3-nitridation, the interfacial layer thickness was reduced to 1.0-2.0 nm. Secondary ion mass spectrometry (SIMS) of these same TiO_2 wafers used in this study indicated that the interfacial layer in the TiO_2 wafers consisted of a $TiSi_xO_y$ mixture whose composition changes over the width of the interfacial layer, and also consisted of nitrogen in the samples subjected to the nitridation [120]. It was also found

that the thickness of the interfacial layer was relatively independent of the high-k dielectric film thickness [119].

Electrical characterizations were carried out on the MIS capacitors, incorporating the high-k and nitridated layer dielectric stack as well as on the MOS structures. Standard capacitance-voltage (CV) measurements were performed in the temperature range 50 K to 300 K and at frequencies between 100 kHz and 1 MHz. Deep level transient spectroscopy (DLTS) was used to probe the trap profile in the silicon/high-k dielectric interface and in the underneath silicon substrate, using a BIORAD DLTFS 8010 system. The measurement conditions were: (i) the capacitor was held at a steady depletion state; (ii) a filling pulse of 40 ms width and varying pulse height (V_p); (iii) a measurement period (T_w) of 200 ms; and (iv) a temperature scan rate of 0.5 K/s to 1 K/s.

6.3 Experimental Results and Discussion

6.3.1 Accumulation Capacitance Dependence on Temperature and Frequency

A common method to determine the EOT is that using the equivalent circuit shown in *Figure 6.1* (b) when the MIS capacitor with high-k dielectric stack is biased in accumulation. The capacitance C_s in the figure represents the serial combination of the high-k dielectric capacitance, C_{HK}, and the interfacial layer capacitance, C_{il}. The resistance R_s includes that of the Si substrate as well as the back contact and cable resistances, which is usually in the range of 100 to 500 Ω. Since most modern capacitor

meters utilize a parallel circuit model as shown in *Figure 6.1* (a). Eq. 6.1, relates C_s to the actual measured accumulation capacitance C_p according to

$$C_p = \frac{C_s}{1 + R_s^2 C_s^2 \omega^2} \qquad (6.1)$$

where ω is the measurement frequency. EOT is, hence, simply estimated using $EOT = \frac{k\varepsilon_0}{C_s} A$, where k=3.9 is the dielectric constant for silicon dioxide and A is the electrode area.

However, we found out that the accumulation capacitance C_p in the MIS capacitors with high-k gate dielectrics has very strong dependence on CV measurement temperature and frequency. Consequently, one deduces that EOT as derived above varies with temperature and frequency. This was observed to be the case for all measured MIS capacitors, whether the high-k dielectric was $SrTa_2O_6$, $ZrSiO_4$ and HfO_2 grown by LSMCD or chemical vapor deposited TiO_2. This was also observed to be the case in capacitors made on wafers with surfaces that were nitridated or not.

The temperature dependence of MIS capacitance is illustrated in *Figure 6.2* and the inset on the right-hand side. The CV measurements taken on a MIS capacitor with $SrTa_2O_6$ as the high-k give an accumulation capacitance of ~ 400 pF at 300 K which increases to ~ 900 pF at 50 K. The percentage change in the accumulation capacitance of the MIS capacitor was 120 % as the measurement temperature decreases from 300 K to 50 K. The dependence of the accumulation capacitance on temperature is much stronger and more pronounced above 150 K. At 100 K and below there appears to be no change in capacitance. However, the deep depletion capacitance in the MIS capacitor does not

follow the same trend in temperature as that of the accumulation capacitance (see the inset of *Figure 6.2*). At an applied voltage of 1.0 V the measured capacitance decreases from ~ 15 pF at 300 K to ~ 11 pF at 50 K, i.e. it decreases with decreasing temperature.

The frequency dependence of the accumulation capacitance on the measurement frequency is shown in *Figure 6.3* for the MOS capacitors and MIS capacitors with $SrTa_2O_6$ gate dielectrics. The measurements are all taken at 300 K and at measurement frequencies of 1M Hz and 100 kHz. The MOS accumulation capacitance shows no or very little dependence on the frequency. Meanwhile the MIS accumulation capacitance exhibits a significantly strong dependence on frequency: the accumulation capacitance almost doubled when the frequency is decreased from 1 MHz to 100 kHz.

The strong dependences of accumulation capacitance on measurement temperature and frequency in high-k dielectric capacitors are significantly different from what we observed in the conventional MOS structures made of SiO_2. In a well-behaved MOS structure, the measured accumulation capacitance C_p has a very small dependence on measurement frequency. Typically, in Si wafers with doping concentration ~ 10^{15} cm^{-3}, R_s ~ 100 to 500 Ω and C_s ~ 10^{-10} to 10^{-11} F for the gate area we used: this implies that in the frequency range 10^3 to 10^6 Hz $(\omega R_s C_s \omega)^2 << 1$ and the change in the measured capacitance C_p should not be more than 10% [121]. This is consistently the case in the MOS capacitor as shown in *Figure 6.3*. However this is very much unlike what happens in the MIS capacitor where a change in measurement frequency between 100 kHz and 1 MHz change resulted in almost a 100 % change in C_p (*Figure 6.3*). Also, in the conventional MOS capacitor, the measured accumulation capacitance C_p decreases as the

temperature decreases (*Figure 6.4*). This is because the series resistance R_s rapidly increases with decreasing temperature due to the exponential decrease in free carrier concentration in the Si substrate. In contrast, in the MIS capacitor with the high-k gate dielectric stack the accumulation capacitance C_p increases with decreasing temperature, which is completely opposite to the case in the MOS capacitor (*Figure 6.2*).

6.3.2 Estimation of EOT from CV Data

Based on the results shown in the previous section, one needs to carefully interpret the CV data in MIS capacitors with a high-k gate dielectric and the use of these results in estimating EOT. We initially took a very simplified analysis approach in which the equivalent circuit for the MIS is assumed to include capacitance series contributions from the high-k dielectric and the interfacial layers as shown in *Figure 6.1* (b). We will, hence, discuss the implications of this simple model and subsequently proceed to discuss a more general equivalent circuit.

The capacitance C_{il} in the equivalent circuit is that of the interfacial layer and the capacitance C_{HK} is that of the high-k dielectric. C_s is related to C_{il} and C_{HK} through Eq. 6.2 below

$$\frac{1}{C_s} = \frac{1}{C_{HK}} + \frac{1}{C_{il}} \qquad (6.2)$$

Using $EOT = \frac{k\varepsilon_0}{C_s} A$, Eq. 6.2 can be rewritten as

$$EOT = \frac{3.9}{k_{HK}} d_{HK} + \frac{3.9}{k_{il}} d_{il} \qquad (6.3)$$

where the d's and k's refer to the thicknesses and the dielectric constants of the high-k dielectric and interfacial layers, respectively. By plotting EOT versus the deposited dielectric film thickness d_{HK} one can calculate k_{HK} from the slope of the resulting straight line, and k_{il} from its intercept provided that the interfacial layer thickness d_{il} is kept constant and obtained through other means such as transmission electron microscopy (TEM). *Figure 6.5* shows a family of such straight lines obtained from CV results on MIS capacitors with TiO_2 as the high-k dielectric. The thickness of the high-k dielectric was varied between 20 Å and 280 Å and the CV measurements were taken between 50 K and 300 K.

Similar to what we have seen earlier in *Figure 6.2*, the accumulation capacitance C_s in a MIS capacitor with a high-k dielectric, such as TiO_2, increases with decreasing temperature. Since EOT is inversely proportional to C_s, for a MIS with a certain TiO_2 thickness, EOT becomes smaller the lower the temperature. *Figure 6.5* shows C_s in the TiO_2-based MIS capacitors does not change significantly below 150 K. We also observe that at TiO_2 thicknesses below 50 Å EOT is no longer linearly dependent on TiO_2 thickness. This is attributed to the high leakage current at these TiO_2 dielectric thicknesses, which tend to yield an apparently lower capacitance values. In the MIS

capacitors with TiO_2 thicknesses above 50 Å, the measured leakage current densities are well below 10^{-5} A/cm^2 and independent of measurement temperatures which yield flat accumulation capacitance curves and reliable C_s values. We, therefore, estimated the dielectric constants and the layer thicknesses from CV results obtained in MIS capacitors with thicknesses larger than 50 Å.

In spite of the different EOT values obtained at different CV measurement temperatures, the slopes of EOT versus d_{HK} of TiO_2 remain the same. These slopes yield a calculated k_{TiO2} value of ~ 46, which is consistent with reported data on these same TiO_2 films studied independently by other groups [119]. As we pointed out earlier the slope is independent of the CV measurement temperature and so is k_{TiO2}. The intercepts of the extrapolated straight lines with the EOT-axis, however, are different for different CV measurement temperature. But from Eq. 6.3 we observe that the intercept is proportional to d_{il}/k_{il}. Since d_{il} is the same (20 Å) in all capacitors, irrespective of the measurement temperature, one derives a temperature dependent dielectric constant for the interfacial layer, k_{il}. According to our estimation k_{il} varies from a value of 5 at 300K to 11 at 150K and below. This is a large variation in k_{il} which implies that the dielectric strength of the interfacial layer is significantly degraded by increasing temperature and the interfacial layer becomes considerably leaky.

6.3.3 Analysis of Accumulation Capacitance

In the TiO_2 and $SrTa_2O_6$ MIS capacitors, the nitridated interfacial layer is formed from the inter-diffusion and reaction with Si of Ti /Ta atoms since these two metals are

thermodynamically instable on silicon substrates. The composition of this interfacial layer is most likely of the form $TiSi_xO_y$ or $TaSi_{x'}O_{y'}$ with the fractions x, x', y, and y' gradually changing over the depth and width of the layer [111,119]. In $ZrSiO_4$ structures, although no silicide layer may form during the dielectric deposition stage, an interfacial SiN_xO_y layer is still formed due to the efficient diffusion of oxygen through $ZrSiO_4$ during post deposition oxygen annealing. The presence of nitrogen in the layer comes from the already nitridated silicon surface prior to the $ZrSiO_4$ deposition. However, a limited formation of thin silicide layers or isolated silicide islands is not entirely excluded. Overall the chemistries of these interfacial layers may be quite complex and can be best described as a mixture of SiO_2, silicide and nitridated Si. Needless to say, with such uncontrolled and lower quality interfacial layer one would expect a large density of interface states between this layer and the Si substrate underneath. Indeed a number of reports exist in the literature indicating that high densities of interface states are very common in high-k dielectrics/Si interfaces [118,119]. In addition to the traps at the interface the bulk of the interfacial layer is expected to have large densities of bulk traps as well.

Conduction in bulk dielectrics is primarily carried out via electric-field assisted charge carriers hopping between empty and vacant defect electronic states. This conduction mechanism is referred to as hopping conduction and is promoted by larger densities of defect electronic states in the dielectric [122]. Hopping conduction increases with temperature and the applied field frequency. Given the uncontrolled growth conditions of the interfacial layers in the MIS capacitors and the possibility of the

presence of high levels of interface and bulk traps in these layers, the level of hopping conduction in these layers is expected to be very high. We, hence, need to modify our equivalent circuit for the accumulation capacitance of the MIS to reckon with the possibility of high conduction across the interfacial layer at high temperatures and high frequencies. Therefore the equivalent circuit for the MIS capacitor in accumulation is modified as shown in *Figure 6.1* (c)

The circuit in *Figure 6.1* (c) includes a capacitance C_{HK} contributed by the high-k dielectric, an admittance contributed by a leaky interfacial layer, which is a parallel combination of a capacitance C_{il} and a finite resistance R_{il}, as well as the substrate resistance, R_s. The circuit analysis gives for the measured accumulation capacitance, C_p,

$$C_p = \frac{C'}{1+\omega^2 R'^2 C'^2} \qquad (6.4)$$

where

$$C' = \frac{C_{HK} C_{il}^*}{C_{HK} + C_{il}^*} \quad and \quad R' = R_s + R_{il}^* \qquad (6.5)$$

and

$$C_{il}^* = \frac{1+\omega^2 R_{il}^2 C_{il}^2}{\omega^2 R_{il}^2 C_{il}} \quad and \quad R_{il}^* = \frac{R_{il}}{1+\omega^2 R_{il}^2 C_{il}^2} \qquad (6.6)$$

At very low temperatures (≤ 100 K) the hopping conductivity of the interfacial layer is very low and, hence, R_{il} is large: from Eq. 6.6, and as R_{il} becomes large R_{il}^{*} becomes small and $C_{il}^{*} \rightarrow C_{il}$. Therefore, at the low temperature limit $R' \approx R_s$ and the measured capacitance, C_p, becomes comparable to the series combination of C_{HK} and C_{il}, i.e., $C_p \approx \frac{C_{HK}C_{il}}{C_{HK}+C_{il}}$. At high temperatures (>> 300 K), on the other hand, R_{il} is small and so is R_{il}^{*} and $R' \approx R_s$, however C_{il}^{*} is large and C' approximates C_{HK}. Hence, the measured capacitance at the high temperature limit becomes comparable to the high-k dielectric capacitance ($C_p \approx C_{HK}$). It is apparent from the preceding arguments that for both high and low values of R_{il}, occurring at extremely low and high temperatures, respectively, R_{il}^{*} is very small and, accordingly, $R' \approx R_s$ at extremely low and high temperatures. However, from Eq. 6.6 it can be shown that R_{il}^{*} attains a maximum value of $\frac{1}{2\omega C_{il}}\left(\sim 10^4\,\Omega\right)$ which occurs at $R_{il} = \frac{1}{\omega C_{il}}\left(\sim 10^4\,\Omega\right)$. This value for R_{il} is typical for lossy dielectrics at intermediate temperatures in the neighborhood of 300 K. At these intermediate temperatures, $R' \approx R_{il}^{*} \approx \frac{1}{2\omega C_{il}}$ causes $\omega^2 R'^2 C'^2 \sim 1$ in the denominator of Eq. 6.4 and thereby causes the value of the measured capacitance, C_p, to drop.

In the preceding discussion it is assumed that C_{HK} is not significantly changed within the somewhat narrow temperature range (50 K to 300 K) of these experiments; the implication is that k_{HK} remains constant. We could not find any reports in the literature

for the temperature dependence of k in the high-k dielectrics used in these studies. Nonetheless, k for similar dielectrics, such as Al_2O_3, SrZrO, $Ln_2Ti_2O_7$, are reported to increase with decreasing temperature. However, this increase occurs only at very high frequencies in the GHz range and even then, this increase is reported to be less than 10% within the range 300 K to 50 K [123]. In section (6.3.1) the effects of the interfacial layer are regarded as purely capacitive and interpreted as a change in C_{il} resulting from the change in k_{il}. In this section, however, an equivalent picture in which the change in k_{il} is viewed in terms of the resistance R_{il} which results in a higher k_{il} when small, and results in a lossy capacitor with low k_{il} when large.

We now turn our attention to the accumulation capacitance dependence on ω for a given temperature. This dependence is contained in the second term $\omega^2 R'^2 C'^2$ in the denominator of Eq. 6.4. R_{il} decreases with frequency as the hopping conductance in the interfacial layer increases with frequency. It is predicted that the dependence of hopping conductance on frequency is of the form ω^n where $0 < n < 1$ [124]: this causes a $\omega^{2(1-n)}$ power increase with frequency for $\omega^2 R'^2 C'^2$ in the denominator of Eq. 6.4. The net effect will be the observed decrease in the accumulation capacitance with the measurement frequency as we observed in *Figure 6.3*.

6.3.4 The Effects of Nitridation on the Substrate/Interface

From the above discussion, it is clear that in addition to the thickness of the interfacial layer its quality too can have an appreciable impact on the overall capacitance and EOT. The other two issues of importance with respect to the interfacial layer are its

effects on the interface states at the Si substrate and its effects in protecting the Si substrate underneath from impurity metal diffusion from the high-k dielectrics. These two issues are addressed in the results discussed in this section.

Figure 6.6 shows the CV and IV measurements taken on the MIS capacitors with TiO_2 layer (samples I and F). Both samples I and F have the same thickness of 120 Å while only sample I was deposited on the pre-deposition NH_3 nitridated Si. From TEM results sample I has its interfacial layer thickness of (20Å) reduced by 30% compared to the thickness of the interfacial layer (27Å) in sample F. Both MIS capacitors yield similar accumulation capacitance and, hence, similar EOT. In the capacitor with the nitridation layer (sample I) a negative shift in the CV curves indicates the buildup of positive charge in the gate dielectric and at the interface with Si. This clearly indicates that the inclusion of the interfacial nitride layer has degraded the gate dielectric and interface quality. This observation is similar to earlier findings by other research groups that the addition of a nitride layer to the gate dielectric stack may not be always beneficial to the interface [125]. From *Figure 6.6* we see no improvement of EOT of the MIS capacitor brought about by Si surface nitridation before the high-k dielectric deposition. The leakage current densities for MIS capacitors with both samples I and F are ~ 10^{-6} A/cm^2 at an applied voltage of 2V.

Figure 6.7 shows the DLTS spectra measured on three MIS capacitors with different TiO_2 layers thickness (samples I, K, and M). Two DLTS peaks, hereafter labeled as H1 and H2, are observed. Both correspond to hole traps. H1 exists in all three samples with similar characteristics, i.e. with a peak location in temperature at ~ 156K

and with an energy state in the Si band gap centered at 0.29eV above the top of the valence band (E_v). The energy state is determined from the Arrhenius plot of the emission rates versus reciprocal temperature at which the DLTS peak occurs. The intensity of signal H1 increases slightly with the gate dielectric thickness. The trap density N_t, calculated from the DLTS signal intensity indicates N_t (H1) ranges from $1.9x10^{13}cm^{-3}$ to $5x10^{13}cm^{-3}$ in three samples. H2, however, does not have a fixed position in temperature. It shifts towards higher temperatures and increases in intensity as the thickness of the layer TiO_2 increases. By applying various pulse voltage heights, the spatial location of both traps, H1 and H2 are determined as between 500 Å and 1000 Å below the oxynitride/silicon interface.

Figure 6.8 shows a comparison between DLTS in TiO_2 MIS capacitors with and without nitridation (samples I and F). Unlike all other TiO_2 samples, no H1 (0.29) trap is observed in sample F which is the one without NH_3 pre-deposition nitridation. Instead, it only has a broad spectrum with a peak location close to H2. The magnitude of this peak, a.k.a, the corresponding trap density, is about half of the trap density in sample I and the trap's spatial location is similar to H2, which is also about 500 to 1000 Å below the Si/TiO_2 interface. In conclusion, sample F appears to be less damaged than sample I from the DLTS results.

From above DLTS results, two main hole traps H1 and H2 were detected in the bulk Si in TiO_2 based MIS capacitors. H1 (0.29 eV) shows up in all but samples without nitridation and its density increases slightly with increasing deposited TiO_2 thickness. Therefore it is reasonable to associate its origin to the extra nitridation step instead of the

TiO_2 deposition. The slight increase of the trap intensity is likely due to the subsequent longer duration of TiO_2 deposition process in thicker samples. H2 has no fixed location, and the corresponding trap concentration increases with the TiO_2 deposition thickness. It is not possible to distinguish its origin from DLTS data alone. However, it is clear that the nitridation layer failed to prevent the growth of H2, which is most likely created during the dielectrics deposition stage. In fact, samples with nitridation step appear more damaged than the samples without. Both traps H1 and H2 are within a depth of only 1000 Å from the interface which suggests that their presence will adversely affect carrier mobility in channels of metal-oxide-Si field-effect transistors.

6.3.5 Contamination to Si from High-k Dielectric Deposition

The purpose of the experiments reported in this section is to examine possible contamination to MOS capacitors resulting from a hypothetical CMOS process that utilizes MOS structures and MIS structures with high-k gate dielectrics. P-type silicon wafers of 2-15 Ω-cm resistivity were used in this experiment. These wafers were first subjected to in-situ gas-phase Si surface cleaning treatments in the same LSMCD chamber that is often used to grow high-k dielectrics [29]. After the cleaning, the valve that releases the high-k precursor module (ZrO_2 or HfO_2 in our case) was opened briefly for 1-2 minutes, during which period a small amount of high-k dielectric molecules were deposited on the silicon surface. These molecules would possibly form isolated ZrO_2/HfO_2/silicides islands or isolated sites. The wafers were then moved out of the LSMCD chamber and went through a 950°C thermal process to grow 15-16nm thick

oxide layer. Aluminum dots were deposited afterwards to form MOS capacitors with gate area of $1x10^{-2}$ cm^2. CV, IV and DLTS measurements were performed on these MOS capacitors using the same measurements conditions as those described above.

Most of the results from CV and IV measurements appear to be well within the same range for both structures: the ZrO_2-contaminated capacitor and the HfO_2contaminated capacitor, as shown in *Table 6–2.* And they are also comparable with conventional SiO_2 capacitors with similar structures. However, we observed significant shift of CV curves towards negative voltage direction in both contaminated capacitors, indicating positive charge buildup in the gate oxide and interface. *Figure 6.9* and *Figure 6.10* show the probability plots of flat-band voltages (V_{FB}) for both samples with median values of ~ -1.4V. Both samples were then subjected to 400°C, 30 min forming gas (4% H_2, 96% N_2) furnace anneal. After anneal, V_{FB} of ZrO_2-contaminated structures seems to recover back to around -0.8V (*Figure 6.10*), while V_{FB} of HfO_2-contaminated MOS capacitors splits into two groups, one group remains at -1.4V and the other group at -0.8V (*Figure 6.9*).

DLTS measurements were performed on both samples, before and after forming gas anneal, to probe the trap profile at the Si/SiO_2 interface and the substrate beneath. DLTS measurements were performed on MOS capacitors located in different regions of the wafer. No specific spectral trends were observed as function of location on the wafer. This is an indication of non-uniform contamination across the wafer.

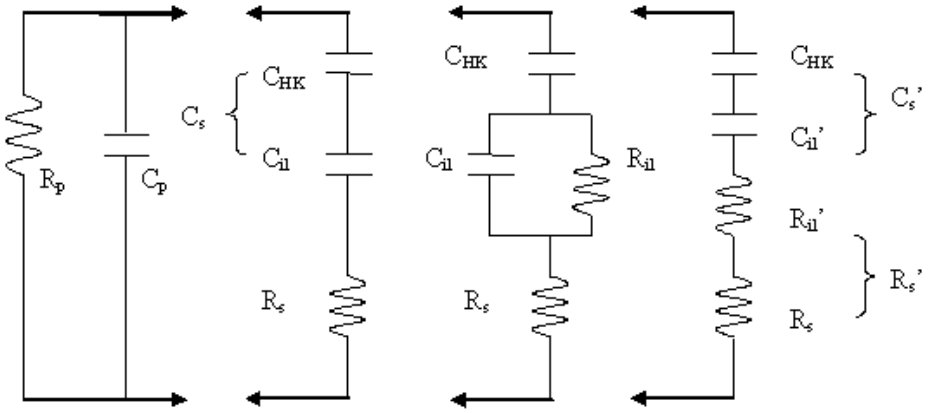
In HfO_2 contaminated samples, however, two groups of DLTS spectra can be distinguished . These are shown in *Figure 6.11* and *Figure 6.12*. In the DLTS spectra

collected from HfO_2 contaminated samples in *Figure 6.11, and Figure 6.12* we see a positive DLTS peak H3 which arises from a hole trap, and a negative DLTS peak E1 which is associated with an electron trap. Both peaks occur in temperature around 150K. The hole trap H3 is only observable under pulse voltages between -1V and -4V, when the capacitor is pulsed into accumulation region, and its intensity peaks at V_p=-2V. Combining the DLTS with CV results, one concludes that H3 is located very close to, about 500-1000 Å beneath the SiO_2/Si interface. The electron trap E1, however, shows up as early as the filling pulse reaching V_p=2V, when the capacitor is still pulsed into the depletion region. The DLTS peak E1 continues to be present until V_p=-4V. The absence of E1 for Vp between -1V and -3V is, presumably, due to the overlap with a much stronger H3 signal. E1, therefore, has large spatial distribution extending from Si/SiO_2 interface deeper into Si substrate. However, we note that not all capacitors in HfO_2contaminated samples show H3 peak during the DLTS tests : as *Figure 6.12* shows, in some of the samples only E1 trap can be detected. On ZrO_2-contaminated sample, a broad positive DLTS peak is observed for all capacitors across the wafer, although the magnitude of the peak varies with the location (*Figure 6.13*).

The conditions chosen for the forming gas anneal are typical of those used in post-metallization anneal (PMA) in CMOS to find out whether traps arising from contamination would be eliminated by the annealing. This turned out not to be the case and H3 and E1 were both present in the HfO_2-contaminated Si after the annealing. This was also the case with the broad DLTS signal observed in the ZrO_2-contaminated Si.

6.3.6 Summary

It is observed that the accumulation capacitance of MIS structures with high-k gate dielectrics has a strong dependence on the CV measurement temperature and frequency. This is explained as arising from impedance contributions from a low quality interfacial layer between the high-k dielectric and the Si substrate. The fact that the presence of this layer is observed to lower room temperature accumulation capacitance of the MIS structure necessitates that efforts must be put towards its elimination in the gate dielectric stack. Moreover, the presence of this layer must be reckoned with in determining EOT in the MIS. It is also observed that the presence of the interfacial layer does not play any effective role in improving the gate dielectric/Si interface and the underneath bulk Si qualities.



(a) Capacitance Meter

(b) (c) (d) high-k stack system Equivalent circuit

Figure 6.1: Equivalent circuits in accumulation region in MIS with a high-k gate stack system.

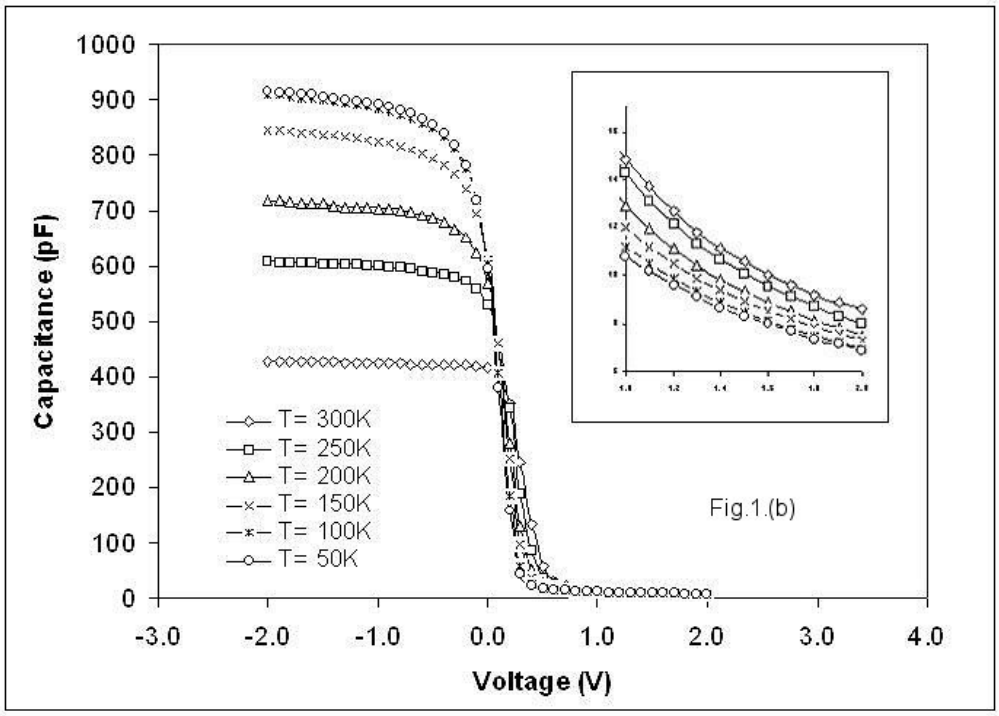


Figure 6.2: CV curves for 5.0nm $SrTa_2O_6$ /p-type Si capacitor measurement at different temperatures. The inset shows capacitance measured between +1V to +2V (deep depletion region)

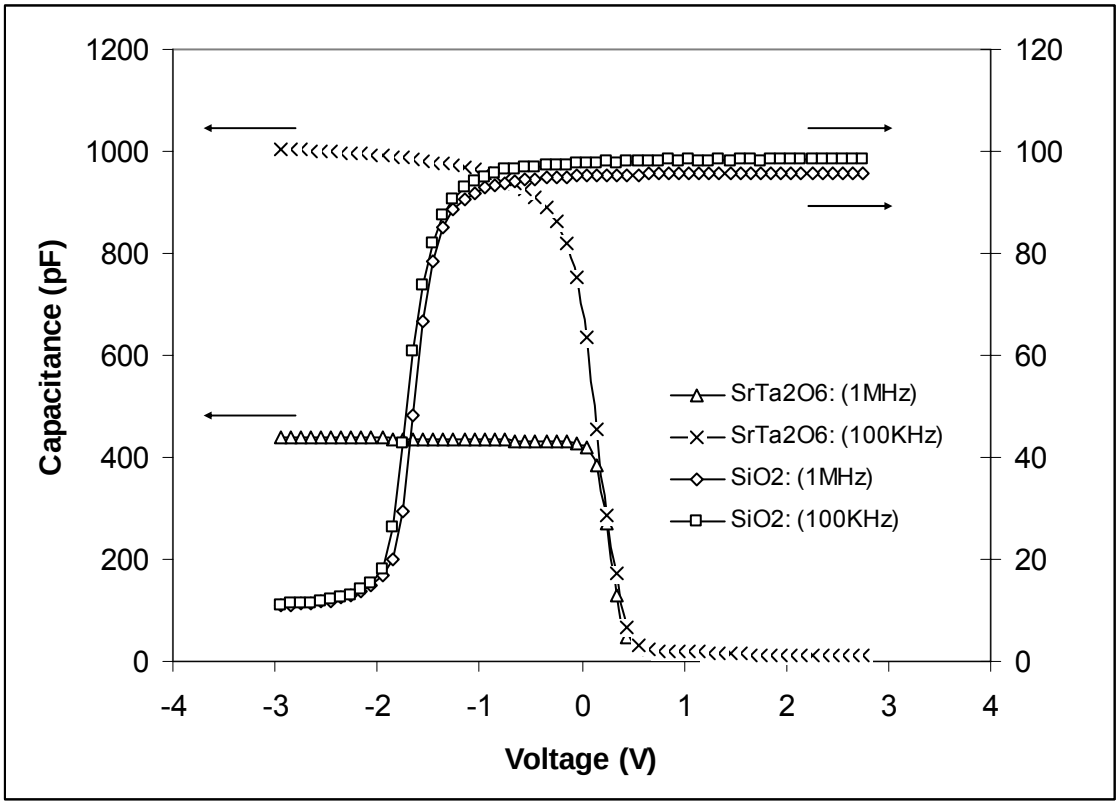


Figure 6.3: CV curves for both SiO_2/n-type Si MOS capacitor and $SrTa_2O_6$ /p-type Si MIS capacitor structures measured at different frequencies (1M Hz and 100k Hz).

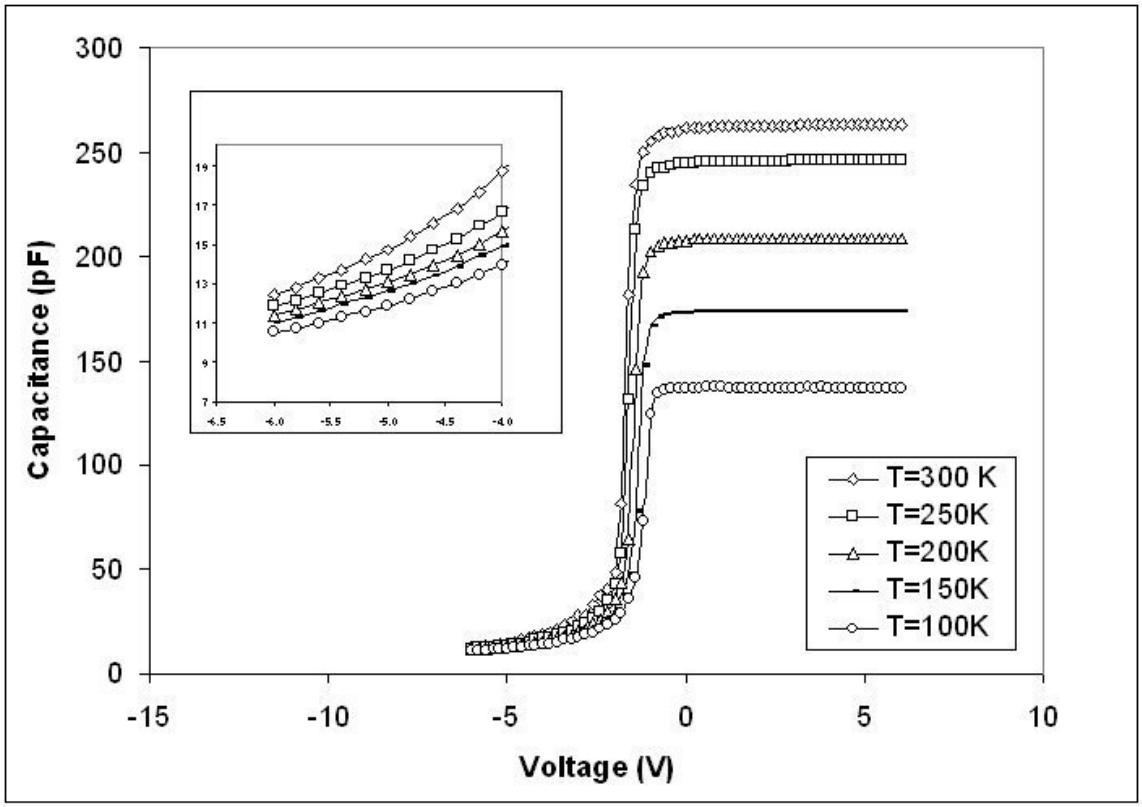


Figure 6.4: CV curves for 20 nm SiO_2/n-type Si MOS capacitor structure measured at different temperatures. The inset shows capacitance between -6.5V to -4 V (deep depletion region)

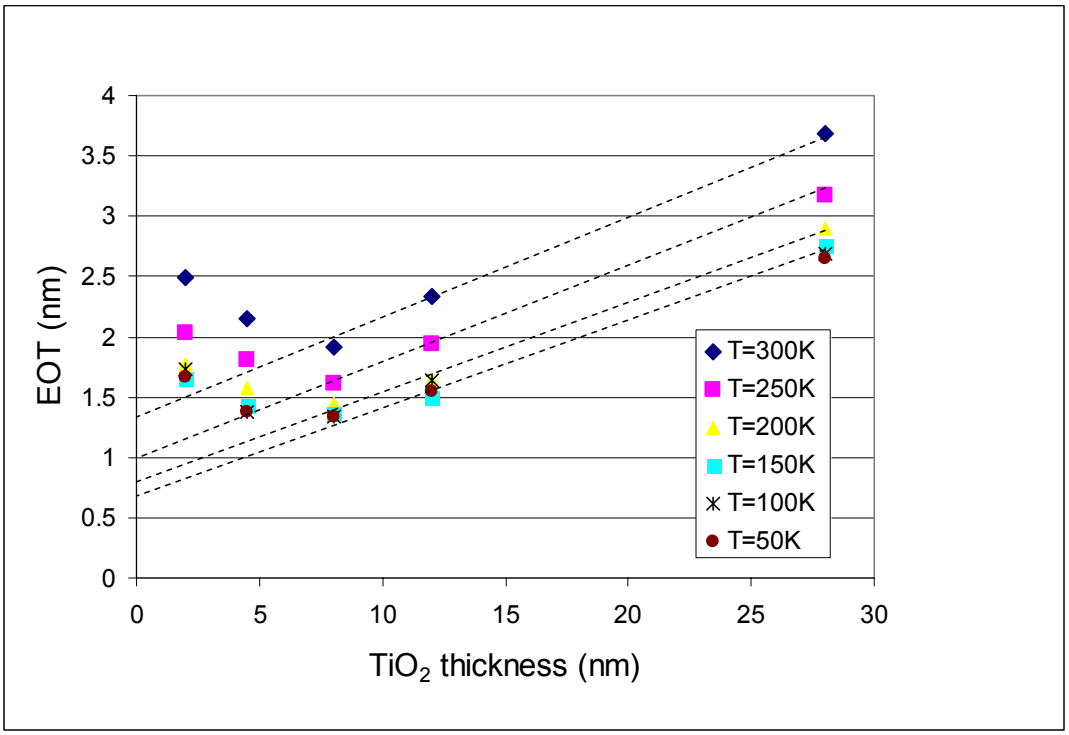


Figure 6.5: Equivalent oxide thickness (EOT), in a MIS capacitor with a TiO_2 gate dielectric on nitridated silicon as a function of the deposited thickness of the TiO_2 and CV measurement temperature.

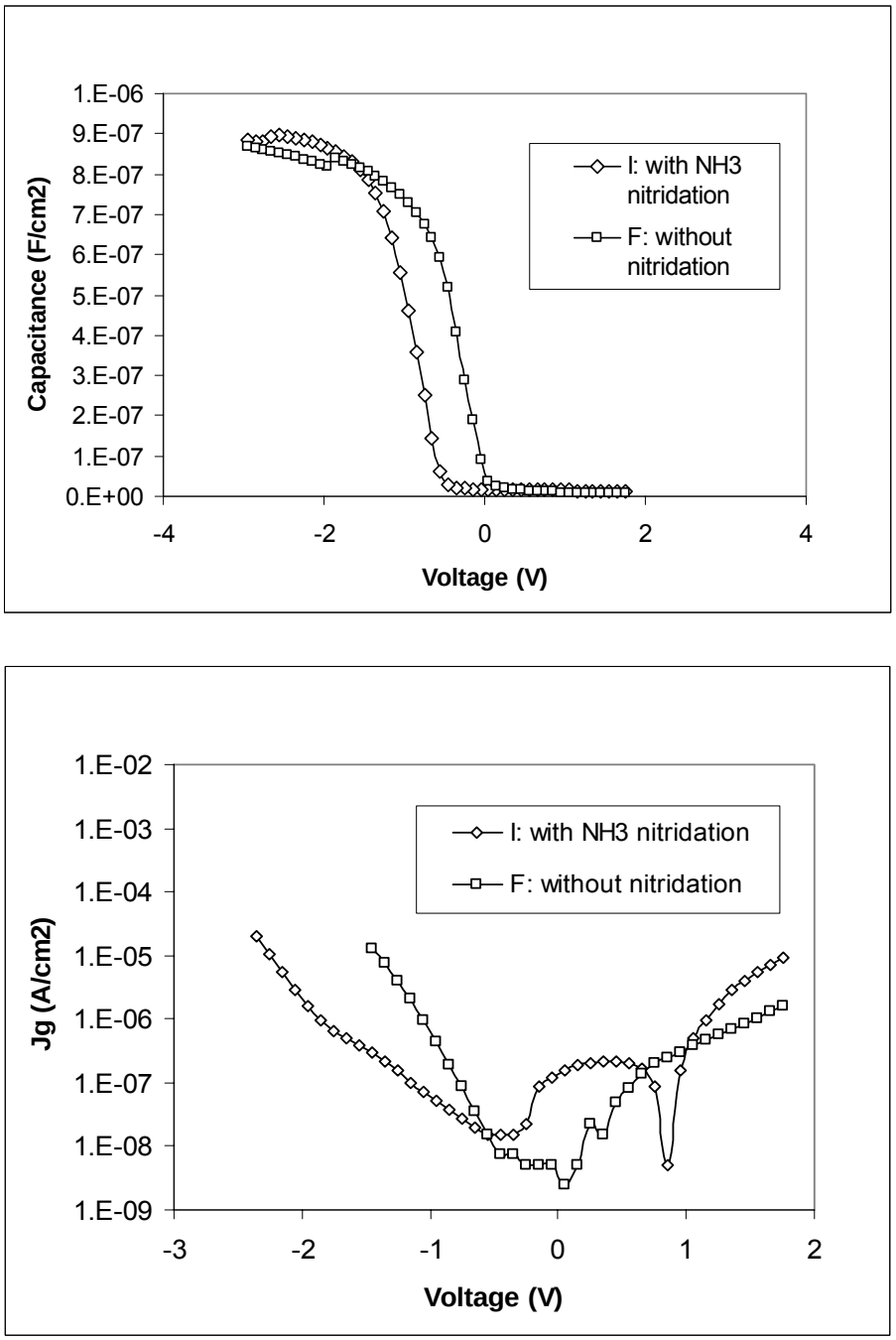


Figure 6.6: CV and IV curves for Sample I (12 nm-thick TiO_2 gate oxide with NH_3-nitridation) and Sample F (12 nm-thick TiO_2 gate oxide without NH_3-nitridation).

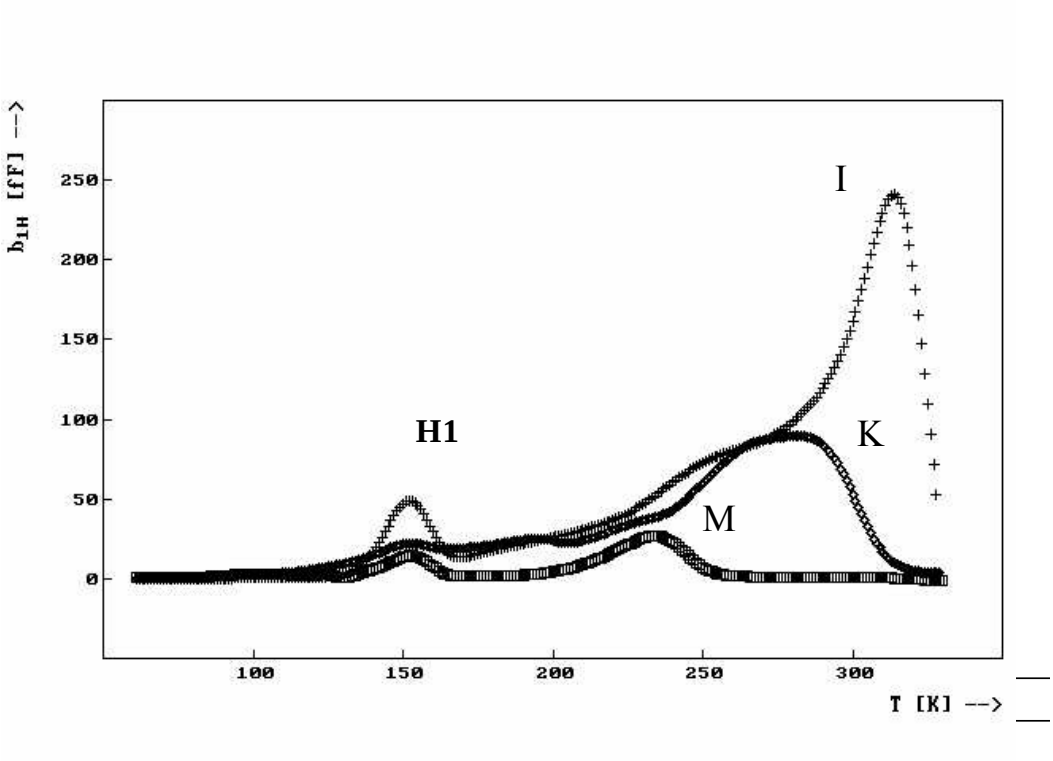


Figure 6.7: DLTS results on capacitor samples with different TiO_2 gate dielectric thicknesses. Sample I has TiO_2 thickness of 12 nm, while sample K and M have TiO_2 thicknesses of 8 nm and 2 nm, respectively. The DLTS measurement condition is reverse bias of V_r=0.5V and pulse height of V_p=0V for all three spectra.

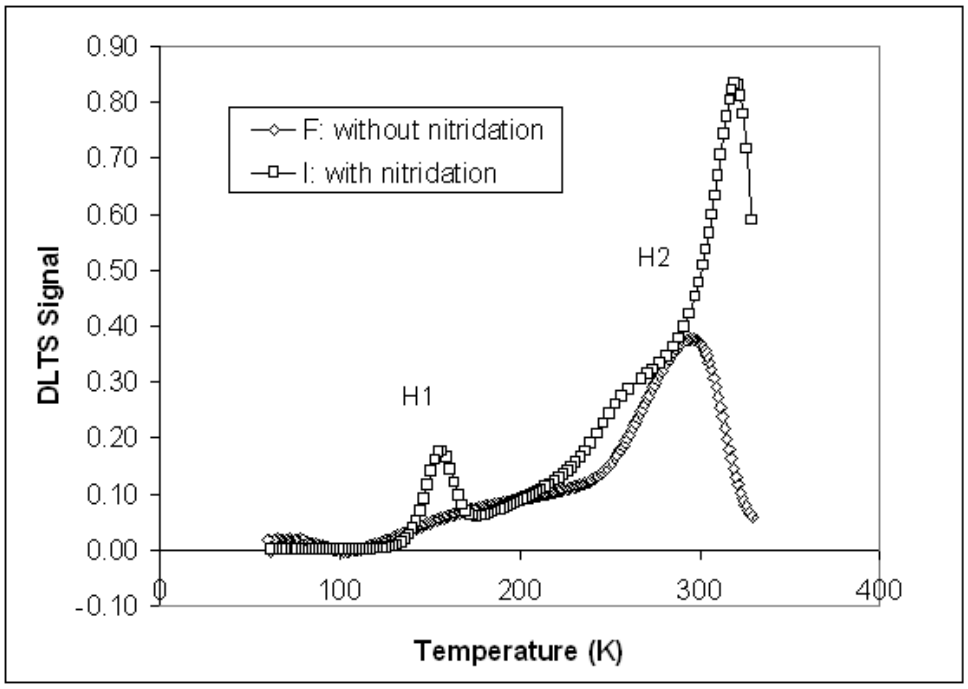


Figure 6.8: DLTS spectra on capacitors subjected to pre-deposition NH_3 nitridation (sample I) and samples without pre-deposition nitridation (F). Both samples are of similar TiO_2 gate oxide thickness (12nm).

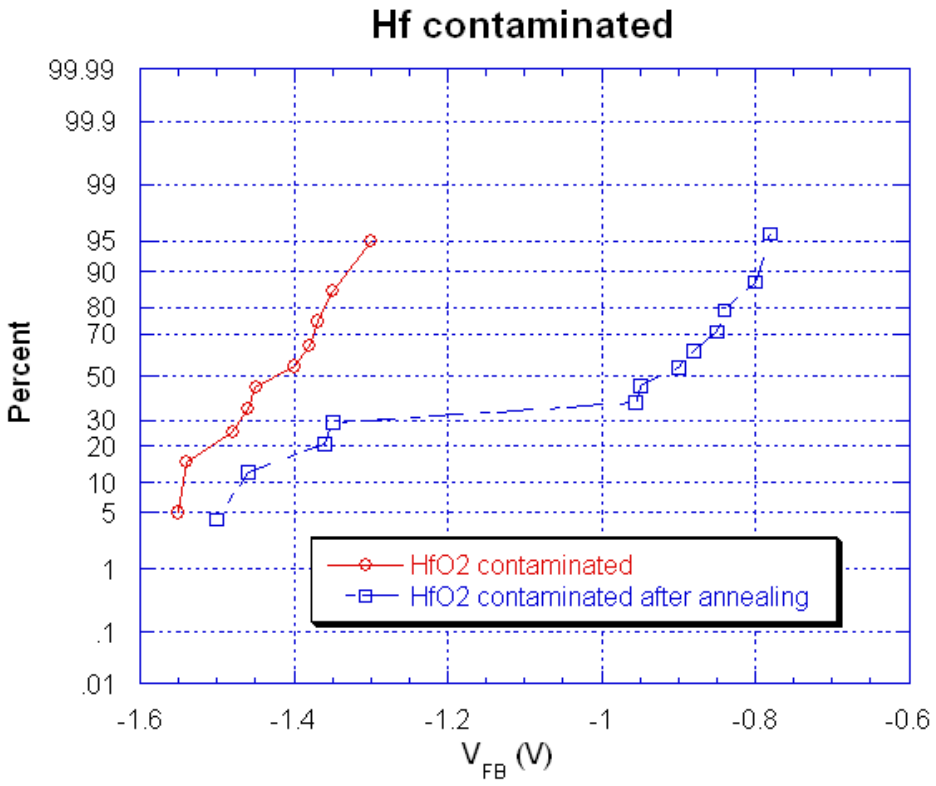


Figure 6.9: Probability plots of flat-band voltages for HfO_2 contaminated samples before and after forming gas anneal. The data were collected from 10-12 structures. The anneal condition is T=400°C and t = 30 mins.

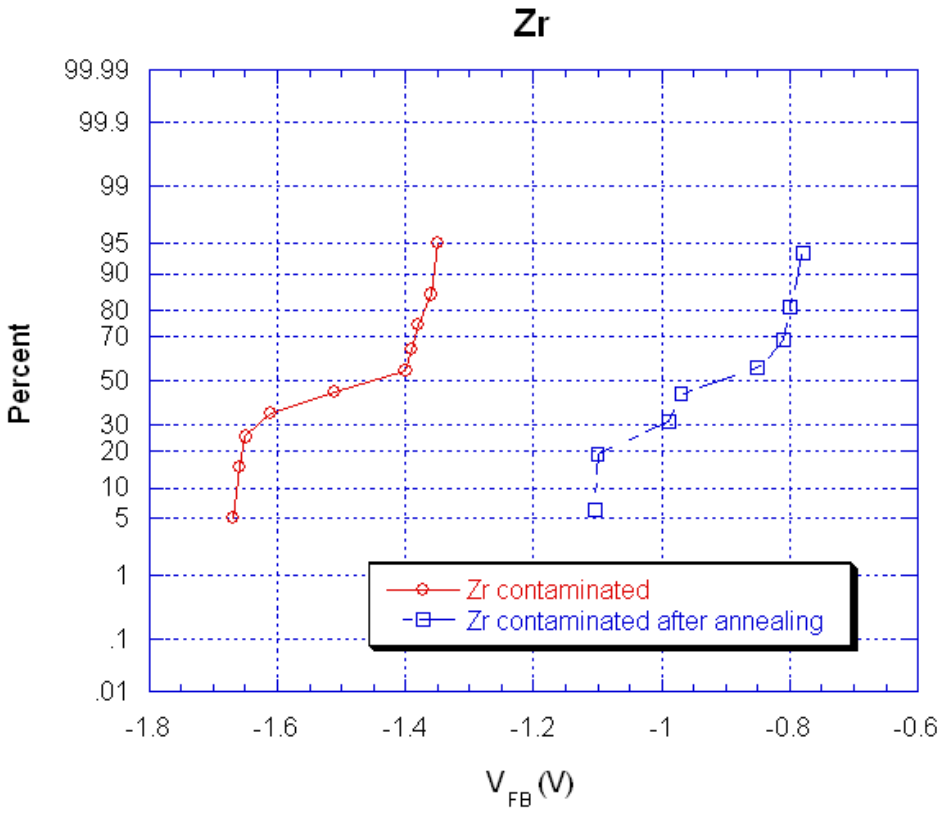


Figure 6.10: Probability plots of flat-band voltages for ZrO_2 contaminated samples before and after forming gas anneal. The data were collected from 8-10 structures. The anneal condition is T=400°C and t = 30 mins.

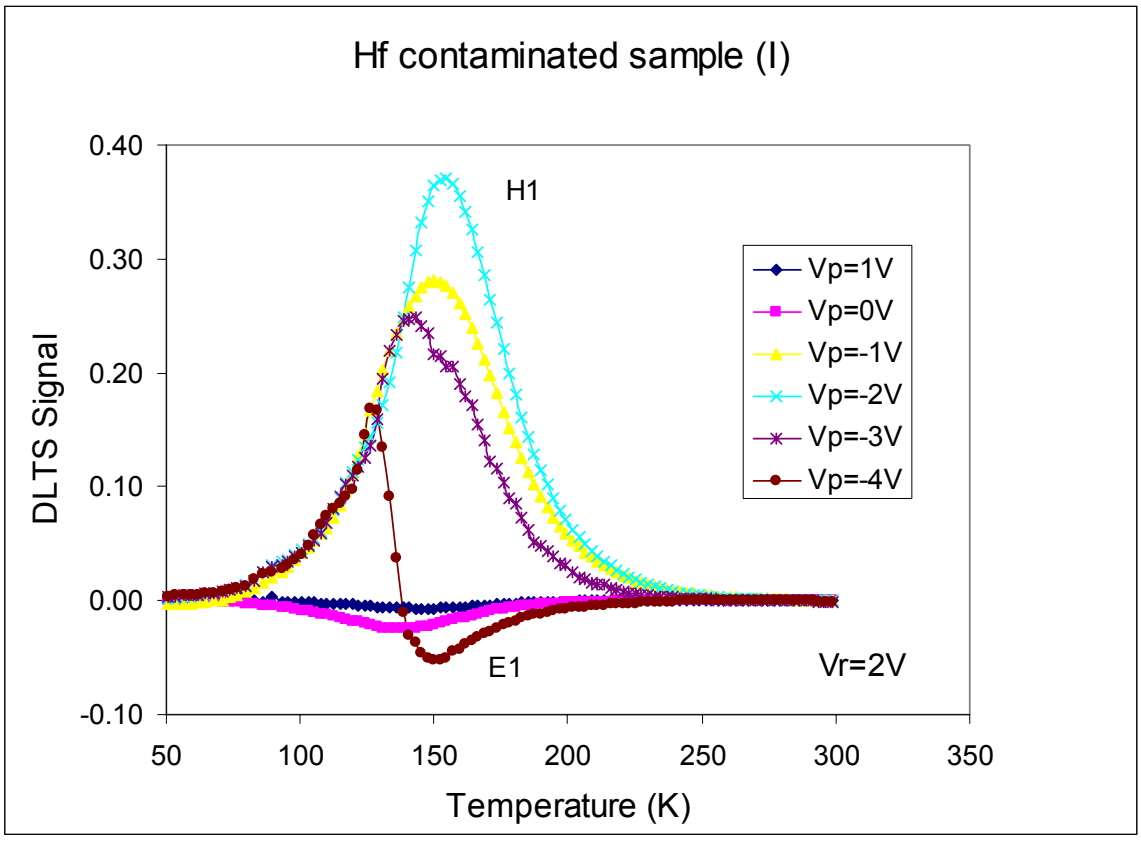


Figure 6.11: A typical DLTS spectra on HfO_2 contaminated capacitors after forming gas anneal (400°C, 30mins). The measurements were performed under reverse bias of 2V and various pulse height from -4V to 1V.

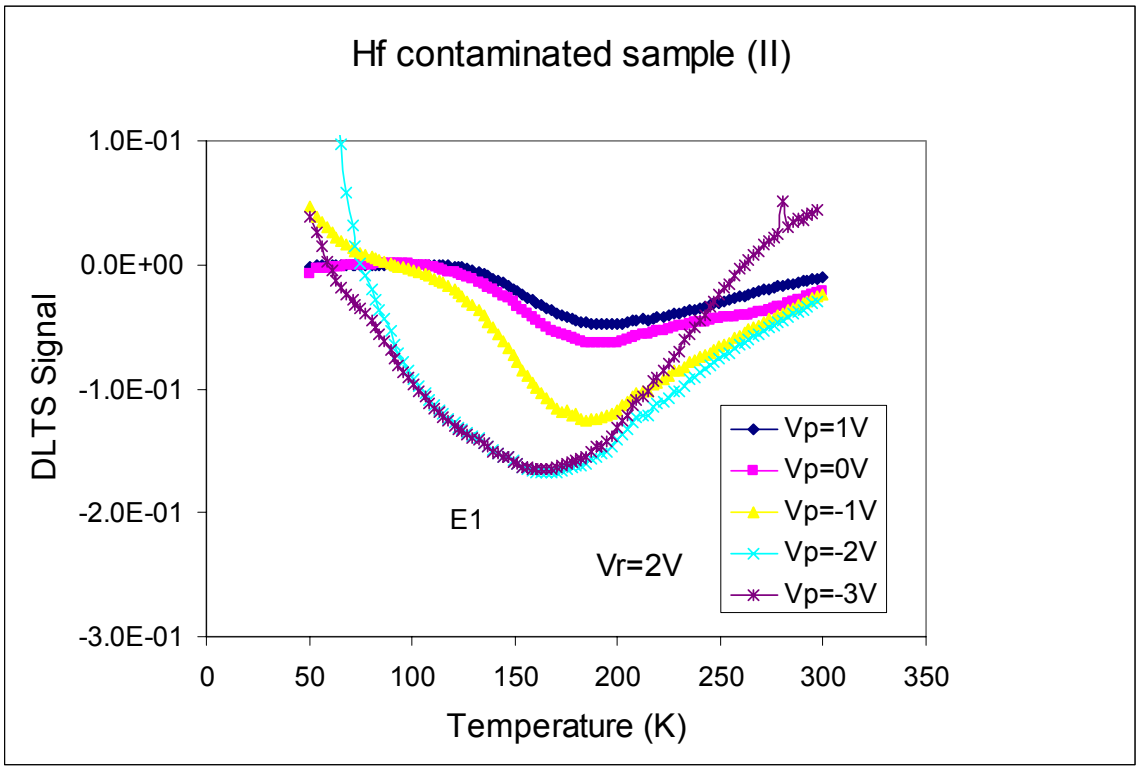


Figure 6.12: Another typical DLTS spectra on HfO_2 contaminated capacitors after forming gas anneal (400°C, 30mins). The measurements were performed under reverse bias of 2V and various pulse heights from -4V to 1V.

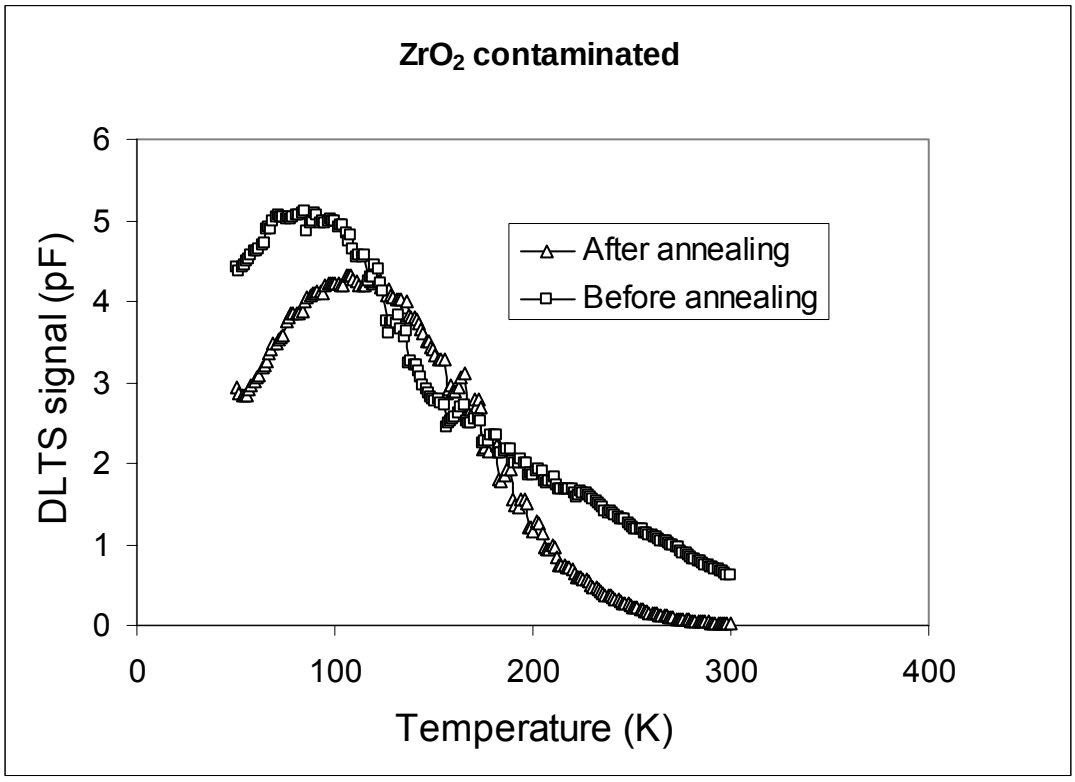


Figure 6.13: DLTS spectra on ZrO_2 contaminated samples before and after forming gas anneal (400°C, 30min). The measurement used reverse bias of V_r= 2V and had pulse height of V_p=-2V.

Table 6–1: TiO_2 sample list

Sample Code	C	I	K	L	M	F*
TiO2 thickness (Å)	280	120	80	45	20	120

*All samples but F were treated with NH_3 nitridation (850°C, 5min) prior to the TiO_2 deposition.

Table 6–2: Summary of CV/IV measurements on the contamination samples

* courtesy of Dong-oh Lee in Electrical Engineering dept., Penn State University

Sample	T_{ox} (nm)	D_{it} ($cm^{-2}eV^{-1}$)	J@-5V (A/cm^2)	E_{bd} (MV/cm)
SiO_2/HfO_2	15.5	$2.2x10^{11}$	$8x10^{-8}$	7.7
SiO_2/ZrO_2	16.3	$2.6x10^{11}$	$7.1x10^{-8}$	7.4

Chapter 7

Conclusion

The research reported in this thesis is concerned with gate dielectrics in metal-oxide-Si (MOS) capacitor and MOS field-effect transistor (MOSFET) structures. In the first part of the thesis we have focused on thin silicon dioxide (SiO_2) that is currently in use as a gate dielectric in CMOS but is steadily reduced in thickness to meet CMOS standards. In the second part we have examined a number of high-k dielectric options for replacing the oxide as a gate dielectric. We have collaborated with three research groups, Plasma-Etch Damage group in SEMATECH, the group of professor S. Campbell of the University of Minnesota, and the group of professor J. Ruzyllo at Penn State University. The first group assisted with the fabrication of the test structures involving the thin gate oxide MOSFETs. The latter two groups, however, assisted with the deposition of some selected high-k dielectrics and we have subsequently carried out detailed investigations of the electrical properties and reliabilities of these dielectrics and their interfaces with Si. The outcome of this research is highlighted in the following sections of this chapter. The final section in this chapter gives some suggestions for future studies.

7.1 On the Thin Gate Oxides

7.1.1 Gate Leakage Current as the Only Sensitive Transistor Parameter for Plasma-Processing Induced Damage in Thin Gate-Oxide MOSFETs

- Thin gate-oxide (SiO_2 of thickness 65Å-thick or 45Å) MOSFETs were fabricated using a 0.35μm full CMOS process flow developed and carried out by SEMATECH. Damage to the MOSFETs caused by different plasma processing steps, was studied using transistor parameter measurements as well as charge pumping. The parameters measured included gate leakage current (I_g) , threshold voltage (V_{th}), maximum transconductance (G_m), and subthreshold swing (S) measurements, and charge pumping measurement.
- Traditional transistor parameters V_{th}, G_m and S, which are often used as indicators of the qualities of MOSFETs of somewhat thicker gate oxides (≥ 100 Å), are found to be ineffective in characterizing plasma process induced damage in ultra-thin gate-oxide devices. V_{th}, G_m and S are not able to resolve differences in devices with variable degree of damage.
- The gate leakage current, on the other hand, is shown to be a very sensitive measure of the thin-gate-oxide MOSFETs condition. It is demonstrated that in these ultra-thin-oxide MOSFETs I_g is the only transistor parameter, which can detect plasma-processing induced changes in oxide charge and interface states. In the latter case I_g is shown to be even more sensitive than charge

pumping, which is generally regarded as the most powerful technique of measuring interface states in MOSFETs.

- These results are interpreted in terms of the strong dependence of I_g on trap-assisted tunneling which dominates conduction in oxides within the studied thickness regime

7.1.2 Trap Generation in SiO_2/Si Interface and in Bulk Si by Fowler-Nordheim Stressing of Thin-Gate-Oxide Capacitor Structures

- MOS capacitor structures, fabricated using a 0.5 μm CMOS process flow, were studied using capacitance-voltage (CV) and Fourier-transform deep-level transient spectroscopy (DLTS) measurements. In order to examine the gate-oxide's Fowler-Nordheim (FN) stress reliability the capacitors were measured before and after the application of FN stress.
- FN stress at temperatures between 50 K and 300 K is observed to give rise to positive charge build-up in the bulk gate oxide and at the SiO_2/Si interface. Meanwhile DLTS reveals the presence of interface and bulk Si traps induced by the FN stress at temperatures between 50 K and 300 K, p.
- A band of hole traps are observed at the SiO_2/Si interface following FN stressing at temperatures between 150 K and 300 K.

- In bulk Si, however, and at depths between 600 Å and 1000Å below the SiO_2/Si interface, a configurationally bi-stable defect associated with two electron traps is observed to accompany FN stressing below 150 K.
- This is the first time that bulk Si defects are reported to be generated by FN stressing on thin gate oxides. Considering that the depths below the interface where the defects are measured are within what would be the channel in a corresponding MOSFET, these defects could be detrimental to carriers' lifetimes in the channel.

7.1.3 Hot Carrier (HC) Stress Effects

- HC stress induced damage on p-channel MOSFETs (PMOS) was studied under different gate and drain bias conditions using transistor parameter (V_{th}, G_m and S), and charge pumping measurement.
- In relatively thick gate-oxide PMOS the maximum degradation from HC stress is found to take place at stress conditions corresponding to $0<V_g<1/3V_d$. Both negatively charged oxide traps and interface states are created by hot holes. Most of the HC induced degradation is located at the drain side of the PMOS, however when the gate bias is at or close to drain bias, the HC damage consists of interface states that are distributed evenly along the PMOS channel.

- The nature of the HC induced degradation changes when the gate oxide is scaled down : in transistors with 45 Å-thick gate oxide HC stress promotes interface damage and damage from oxide charge trapping becomes less significant. Also the HC degradation is no longer localized near the drain side of the PMOS.

7.2 On the High-k Gate Dielectrics

7.2.1 The Temperature and Frequency Dependence of Accumulation Capacitance in MIS structures with High-k Dielectrics

- Different high-k dielectrics, $SrTa_2O_6$, $ZrSiO_4$, and HfO_2 prepared by liquid source misted chemical deposition, and TiO_2 prepared by chemical vapor deposition were used as the insulators in metal-insulator-Si (MIS) capacitors which were examined using CV.
- It is revealed, for the first time, that the accumulation capacitance of the MIS with the high-k dielectric is strongly dependent on the measurement temperature and frequency. The capacitance dependence on temperature in the MIS with the high-k dielectric is seen to proceed in an opposite direction to that of MOS capacitors. On the other hand, the frequency dependence of the accumulation capacitance of the MOS capacitors is insignificant : this is in contrast to the frequency dependence of the accumulation capacitance in the MIS with the high-k dielectric, which is observed to be rather strong.

- Analysis of the CV results indicates that these observations are explained in terms of impedance contributions from a thin and low quality interfacial layer, between the high-k dielectric and the Si substrate, inadvertently incorporated during the high-k dielectric growth.
- These observations call for efforts to be put towards the elimination of low-quality interfacial layers from gate dielectric stacks.

7.2.2 The Effects of Pre-High-k-Deposition Substrate-Nitridation

- TiO_2 layers prepared by chemical vapor deposition were examined using CV, DLTS measurements. The objective was to examine the effects of pre-deposition nitridation of the Si substrate on the properties of the gate dielectric stack.
- Contrary to previous reports, our results show that the presence of the interfacial layer does not play any effective role in improving the high-k dielectric/Si interface as well as it does not protect bulk Si underneath from impurity diffusion during the high-k dielectric deposition. This latter conclusion is supported by our observations of DLTS carrier traps, which are tentatively ascribed to impurity-related defects.

7.3 Suggestions for Future Work

The evolution of semiconductor industry has been progressing at such a rapid pace that today's standard VLSI technology can be easily outclassed by a more advanced technology next year. New materials and new processing methods and tools are currently developed faster than one can imagine. In this thesis, we have examined capacitors and transistors with various gate dielectrics of different dimensions and prepared using several growth techniques. However, there is a need to continue the type of studies reported in this thesis in order to achieve the following objectives :

- The development of a much shorter list of IC-compatible high-k candidates with dielectric properties as close as possible to those of the thermal oxide. Currently a large number of high-k dielectrics are proposed and large research efforts are put on examining them : these efforts are better focused on only selected few.
- More elaborate and detailed characterization of the short-listed high-k dielectrics. The detailed characterization may include electron spin resonance, which could give a much more clearer picture of charge trapping in the bulk of the high-k dielectric as well as at its interface with Si.
- The incorporation of high-k dielectrics in full process flow MOSFET test structures that may be used for device level and circuit level performance and reliability assessments.

BIBLIOGRAPHY

1. Www.zdnet.com/zdnn/special/javascript/futurecpu/futurecpu.html, "Processors: Past, Present and Future"

2. International Technology Roadmap for Semiconductors, Semiconductor Industrial Association, (1999)

3. J.J.Sánchez, K.K.Hsueh, T.A.DeMassa, IEEE Trans. El. Dev., Vol ED-36, p1125, (1989)

4. M.Lezlinger, E.H.Show, J. Appl. Phys., Vol 40, No.1, p 278, (1969)

5. J.J.O'Dwyer, J.Appl.Phys, Vol 40, p 3887, (1969)

6. S.J.Fonash, C.R.Viswanathan, Y.D.Chan, Solid State Technology, p99, July (1994)

7. A. Ghetti, A. Hamad, P.J.Silverman, H. Vaidya, N. Zhao, Simulation of semiconductor Processes and Devices, SISPAD International Conference p 239 – 242, (1999)

8. X Liu, J Kang, R Han, Solid-State and Integrated Circuit Technology, 1998. Proceedings, p 432 –434, (1998)

9. S-H.Lo, D.A.Buchanan, Y.Taur, W.Wang, IEEE El. Dev. Lett., Vol 18, p209, (1997)

10. Donggun Park and Chengmin Wu, IEEE Electron Dev. Lett., Vol 19, No. 1, P. 1, January (1998)

11. A.Joshi, et al, IRPS, pp.300, (1996)

12. M.Alai, S.Jacobs, S.Ahmed, S.H.Chern, and P.McGregor, Int. Symp. Plasma Process-Induced Damage, p7, (1997)

13. D.Park, M.Kennard, Y.Melaku, N.Benjamin, T.J.King, C.Hu, Plasma Process-Induced Damage, 1998 3rd InternationalSymposium, p 56 –59, (1998)

14. D.J.DiMaria, T.N.Thesis, J.R.Kirtley, F.L.Pesavento, D.W.Dong and S.D. Brorson: J.Appl.Phys. **57**, 1214, (1985)

15. T.N.Thesis, D.J.DiMaria, J.R.Kirtley and D.W.Dong: Phys.Rev.Lett. **52**, 1445, (1984)

16. J.Jiang, O.O.Awadelkarim and J.Werking, J. Vac. Sci. Vol 16, p734, (1997)

17. S-H Lee, B-J Cho, J-C kim, S-H Choi, IEDM Technical Digest, p605, (1994)

18. M.Depas, T.Nigam, M.heyns, IEEE Trans. El. Dev., Vol 43, p 1499, (1996)

19. B.E.Weir, etc, IEDM Technical Digest, p 73, (1997)

20. T.Sakura, H.Utsunomiya, Y.Kamakura, K.Taniguchi, Electron Devices Meeting, 1998. IEDM '98 Technical Digest, p183 –186, (1998)

21. B.Yu, H.Wang, C. Riccobene, Q.Xiang and M.R.lin, 2000 symposium on VLSI technology Digest of Technical Papers

22. Y.Nishi and J.W.McPherson, Proceeding of 7th IPFA, (1999)

23. Y.H.We, M.Y.Yang, A.Chin, W.J.chen, C.M.Kwei, IEEE El. Dev. Lett., Vol 21, p341, (2000)

24. H.Huff, D.Brady, M.Gilmer, P. Zeitzoff, Sematech Technology Transfer, (1998)

25. Tak H..Ning, Semocpnductor Fabtech, 13th ed. p287, (2000)

26. G.B.Alers, Applied Physics Lett., Vol 73, p1517,(1992)

27. H.Lee, etc, Appled Phyisics Lett., Vol 76. p436, (2000)

28. C.J.Peng and S.B.Krupanidhi, Appl. Phys.lett., Vol60 (20), p 2478, (1992)

29. J.Ruzyllo, D.-O.Lee, P.Roman and M.Horn, IEEE/SEMI Advanced Semiconductor manufacturing Conference, p71, (2001)

30. L.Kang, Y.Jeon, K.Onisi, B.Lee, W.Qi, R.Nieh, S.Gopalan and J.lee, IEEE 2000 symposium on VLSI Technology Digest of Technical Papers, p 44, (2000)

31. E.Nicollian and J.R.Brews, MOS physics and Technology, Wiley, New York, Chapter 2 (1982)

32. Tomasz Brozek, Thin oxide films in MOS technology, MOS 12 tutorial, Motorola inc. May 15, (1998)

33. A.Acovic, M.Dutrit and M.Ilegems, Proc. Workshop on Low Temp. Semicond. Electron., Burlington, VT, 118-122 (1989)

34. A Acovic, G L Rosa and Y.C. Sun, Microelectronics & Reliability, p 845, July (1996)

35. R.S.Muller and T.I.Kamins, Device Electronics for Integrated Circuits, John Wiley, New-York, (1986)

36. G. Ghibaudo, Phys. Stat. Solidi (a), 95, p 323, (1986)

37. O.O.Awadelkarim, S.J.Fonash, P.I.Mikulan and Y.D.Chan, J.Appl, Phys, 79(1), p 517, (1996)

38. C.Nguyen-Duc, G.Ghibaudo, F.Balestra, Phys. State. Sol (a), 126, p553, (1991)

39. H.Haddara, Characterization methods for submicron MOSFETS, Kluwer Academic Publishes, (1995)

40. H.Shin and C.Hu: Semicond. Sci. Technol. **11**, 463 (1996)

41. T.J.Mego, Reseach & Development, 86, May (1987)

42. E.H.Nicollian, J.R.Brews, "MOS physics and Technology,' Wilet, New York, (1982)

43. P.Blood and J.W.Orton, "The Electrical Characterization of Semiconductors: Majority Carriers and Electron States", Academic Press, (1992)

44. T.J.Mego, Solid State Technology, P 163, May (1990)

45. Barton J. Gordon, Solid State technology, P 57, January (1993)

46. Donggun Park and Chengmin Wu, IEEE Electron Dev. Lett., Vol 19, No. 1, P. 1, January (1998)

47. J.S.Brugler and P.G.A. Jespers, IEE Trans. Electron Devices, Vol, ED-16, P.297, (1969)

48. G. Groeseneken, H.E. Maes, N. Beltran and R.F.De Keersmaecher, IEEE Trans. El. Dev., ED-31, p.42, (1984)

49. P.Heremans, J. Witters, G. Groeseneken, H.E. Maes, IEEE Trans, EL. Dev., ED-36, p.1318, (1989)

50. Daniel Bauza, Yves Maneglia, IEEE Tran. El. Dev. Vol 44, No 12, p 2262, (1997)

51. U.Cilingiroglu, Solid State Electron., Vol.28, p.1127, (1985)

52. W.L.Tseng, J.Appl.Phys., Vol.62, p.591, (1987)

53. W.V. Backensto and C.R.Viswanathan, Proc. IEE, Vol 128, pt.1, p.44, (1981)

54. Mario G. Ancona, N.S. Saks, D. Mccarthy, IEEE Trans. El. Dev., Vol 35, p 2221, (1988)

55. D.V.Lang, J.Appl.Phys. 45,3023 (1974)

56. S.Weiss and R. Kassing, Solid State Elctronics, Vol 31, No 12, p 1733, (1988)

57. B.W. Wessels, J. Appl. Phys., 47, pp. 1131 (1976)

58. J.A.Borsuk and R.M.Swanson, IEEE Trans. Electron Dev., ED-27, p 2217, (1980)

59. Y.Tokuda and A.Usami, Japan J.Appl. Phys., 22, p 371, (1983)

60. J.Jiang, O.O.Awadelkarim, Y.D.Chen Journal of Vacc. Sci. Vol,16 p734 (1997)

61. T.Gu, M.Okandan, O.O.Awadelkarim, S.J.Fonash, J.F.Rembetski, P.Aum, and Y.D.Chan: IEEE Electron Device Lett. **15**, 48 (1994)

62. T.Gu, O.O.Awadelkarim, S.J.Fonash, and Y.D.Chan: IEEE electron Device Lett. **15**, 396 (1994)

63. S.Fang and J.McVittie : IEEE Electron Device Lett. **13**, 288 (1992)

64. S.J.Fonash: J. Electrochem. Soc., **137**, 3885 (1990)

65. H.Shin, N.Jha, X.Qian, G.Hills, C.Hu: Solid State Technol. **36** (8), 29 (1993)

66. H.Shin and C.Hu: Semicond. Sci. Technol. **11**, 463 (1996)

67. J.Maserijian and N.Zamani: J.Appl.Phys. **53**, 559 (1982)

68. G.W.Yoon, A.B.Joshi, J.Kim and D.-L.Kwong, IEEE Electron Devices Lett. **EDL-14**, 231 (1993)

69. SEMATECH Technology Transfer 132AZ Module List (1995)

70. O.O.Awaldelkarim, S.J.Fonash, P.I.Mikulan and Y.D.Chan: J.Appl.Phys. **79** (1), 517 (1996)

71. D.J.DiMaria, T.N.Thesis, J.R.Kirtley, F.L.Pesavento, D.W.Dong and S.D. Brorson: J.Appl.Phys. **57**, 1214 (1985)

72. T.N.Thesis, D.J.DiMaria, J.R.Kirtley and D.W.Dong: Phys.Rev.Lett. **52**, 1445 (1984)

73. L.K.Han, H.H.Wang, J.Yan and D.L.Kwong: Electron Lett. **31**, No. 14, 1202 (1995)

74. Mikihiro Kimura and Tadahiro Ohmi: J.Appl.Phys. **80** (11), 6360 (1996)

75. Mikihiro Kimura and Tadahiro Ohmi: J.Appl.Phys. **80** (11), 6360 (1996)

76. T.Gu, M.Okandan, O.O.Awadelkarim, S.J.Fonash, J.F.Rembetski, P.Aum, and Y.D.Chan: IEEE Electron Device Lett. EDL 15, 48 (1994)

77. T.Gu, O.O.Awadelkarim, S.J.Fonash, and Y.D.Chan: IEEE electron Device Lett. EDL 15, 396 (1994)

78. . S.Fang and J.McVittie : IEEE Electron Device Lett. EDL 13, 288 (1992)

79. D.J.Di Maria, E Cartier, and D.Arnold: J.Appl.Phys. 73, 3367 (1993)

80. SEMATECH Technology Transfer " Phase 3 plasma etch damage assesment", Vol.2, Module test information, schematics, and layout drawings, 92010921 A-ENG., (1992)

81. D.V.Lang, J.Appl.Phys. 45,3023 (1974)

82. A.chantre, and D.Bois: Phys.Rev. B31,7979 (1985)

83. O.O.Awaldelkarim, S.J.Fonash, P.I.Mikulan, M.Ozaita, and Y.D.Chan: Microelectronic Engineering 28, 47 (1995)

84. O.O.Awadelkarim, S.J.Fonash, P.I.Mikulan, and Y.D.Chan: J.Appl.Phys.79, 517 (1996)

85. E.Cartier, J.H.Stathis, and D.A.Buchanan: Appl. Phys. Lett., 63, 1510 (1993)

86. E.H.Poindexter: Z.Phys.Chem.Neue Folge 151,165 (1987)

87. D.V.Lang in: "Deep Centers in Semiconductors". ed. S.T.Pantelides, (Gordon and Breach, New York). Chapter 7, (1986)

88. S.Markram-Ebeid in : "Deep Centers in Semiconductors". ed. S.T.Pantelides, (Gordon and Breach, New York). Chapter 6, (1986)

89. S.K.Lai: J.Appl.Phys. 54, 2540 (1983)

90. L.W.Song, X.D.Zhan, B.W.Benson, and G.D.Watkins: Phys.Rev.Lett.60, 460 (1988)

91. S.K.Bains, and P.C.Banbury: J.Phys. C18, L 109 (1985)

92. G.D. Watkins: Phys.Rev.B12, 5824 (1975)

93. G.D.Watkins in: "Radiation Effects on Semiconductor Components", eds. F.Cambou, Ch.Fert, and J.Lagasse, Jounees d'Electronique, Toulouse, p.A1 (1967)

94. L.C.Kimerling in : "Radiation Effexts in Semiconductors", eds. N.B.Urli and J.W.Corbett, (Institute of Physics, London), p.221. (1977)

95. A.Chantre: Phys.Rev. B32. 3687, (1985)

96. J.Frey, IEEE Circuits & Devices Magazine, p 31, (1991)

97. A. Acovic, G. Rosa and Y-C Sun, Micorelectronics and Reliability, p845, (1996)

98. C.C.Hsu, L.K.Wang, M.R.Wordeman, T.H.Ning, IEEE El. Dev. Lett., Vol 10, p327, (1989)

99. J.Mitsushasi, S.Nakao, T.Matsukawa, IEDM'86 Technical Digest, p386, (1986)

100. J.Maserjian, J.Vac.Sci.Technol. Vol 20(3), p743, (1982)

101. M.V.Fischetti, J.Appl.Phys, Vol 57(8), p2860, (1985)

102. J.J.Sánchez, K.K.Hsueh, T.A.DeMassa, IEEE Trans. El. Dev., Vol ED-36, p 1125, (1989)

103. E.Takeda, Microelectron. Reliab., Vol 33, p 1687, (1993)

104. Y.Nissan-Cohen, IEEE El. Dev. Lett., Vol. EDL-7, p 561, (1986)

105.] B.S.Doyle, M.Bourcerie, C.Bergonzoni, R.Benicchi, A.Bravis, K.R.Mistry and A.Boudou, IEEE Tran. El. Dev, vol 37, No 8, p 1869, (1990)

106. P.heremans, R.Bellens, G.Groeseneken, H.E.Maes, IEEE Trans. El. Dev. Vol ED-35, p 2194, (1988)

107. B.S.Doyle, M.Bourcerie, C.Bergonzoni, R.Benicchi, A.Bravis, K.R.Mistry and A.Boudou, IEEE Tran. El. Dev, vol 37, No 3, p 744, (1990)

108. R.Woltjer, G M.Paulzen, H.G.Pomp, H. Lifka and P.H.Woerlee, IEEE tran. El. Dev, vol42, No.1 p 109, (1995)

109. B.S.Doyle and K.R.Mistry, IEEE Tran. El. Dev, vol 40, No.1 p152, (1993)

110. P. Heremans, J.Witters, G.Groeseneken and H.E.Maes, IEEE. Tran. El. Dev, vol 36, No7, p 1318, (1989)

111. G. B. Alers, D. J. Werder, Y. Chabal, H. C. Lu, E. P. Gusev, E. Garfunkel, T. Gustafsson, and R. S. Urdahl, Appl. Phys. Lett. Vol 73, p1517 (1998)

112. B. H. Lee, L. Kang, R. Nieh, W. Qi, and J. C. Lee, Appl. Phys. Lett. Vol 76, p1926 (2000)

113. J.S.Suehle, E.M.Vogel, M.D.Edelstein, C.A.Richter, A.V.Nguyen, I.Levin, D.L.Kaiser, H.Wu, and J.B.Bernstein, 6th International Symp. on PPID, p90, (2001)

114. M.Coper, M.Gribelyuk, E.Gusev, Appl. Phys. Lett., Vol 76, p436 (2000)

115. Y.H.Wu, M.Y.Yang, A.Chin, W.J.Cen and C.M.Kwei, IEEE Elec. Dev. Lett., Vol 21, No7, p341, (2000)

116. H.Huff, D.Brady, M.Gilmer, P. Zeitzoff, Sematech Technology Transfer, (1998)

117. H.F.Luan, S.J.Lee, C.H.Lee, S.C.Yong, Y.L.Mao, Y.Senzaki, D.Roberts, and D.L.Kwong, IEDM, p99, (1999)

118. Karamcheti, V.H.C.Watt, H.N.Al-Shareef, T.Y.Luo, G.A.Brown, M.D.Jackson and H.R.Huff, Semiconductor Fabtech, 12th ed. p207 (2000)

119. T.Ma, S.A.Campell, R.Smith, N.Hoilien, B.He, W.L.Gladfelter etc, IEEE, Tran, Elec. Dev, Oct, (2001)

120. S. Campbell : Private communications.

121. B.J.Gordon, Solid State Tech., p57, Jan. (1993)

122. A.K.Jonscher, Proceedings of the 13th session of the Scottish universities summer school in physics", ed. P. G. Le Comber and J. Mort, NY Academic, p 329 (1973)

123. Takano Katsuyoshi, Electronic Ceramics (in Japanese), Sept. (1991)

124. J.C. Dyre, Journal of Non-Crystalline Solids, Vol135, p219, (1991)

125. P.J.Wright, A.kermani, and K.C.Saraswat, IEEE transaction on Electron Devices, V37, p 1836 (1990)

126. L.M.Terman, Solid-State Electron. Vol5, p285 (1962)

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Journal Publications

- J.Jiang, O.O. Awadelkarim, " On the capacitance of metal/high-k dielectric material stack/silicon structure", Solid-State Electron 46, 1991-1995 (2002)
- J.Jiang, O.O.Awadelkarim, and J.Werking " Gate leakage current: A sensitive characterization parameter for plasma-induced damage detection in ultrathin oxide submicron transistors", Journal of Vacuum Science Technology, A 16(3), May/jun (1998)
- J.Jiang, O.O.Awadelkarim and Y.D.Chan, " A Study of Carrier-trap Generation by Fowler-Nordheim Tunneling Stress on Polycrystalline-Silicon/SiO_2/Silicon Structures", Solid State Electronics, V.41, No.1, p41 (1997)
- J.Jiang, O.O.Awadelkarim and Y.D.Chan, " Fowler-Nordheim Stressing of Polycrystalline Si/SiO_2/Si Structures: Observation of Stress induced Defects in the Oxide, Oxide/Si interface, and in Bulk Silicon", Journal of American Vacuum Society, V.16, p734 (1997)