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**ENGINEERING HOLE INJECTION AND TRANSPORT IN LOW-DIMENSIONAL
MATERIAL TRANSISTORS**

A Dissertation in
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by

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ABSTRACT

In response to the slowdown in transistor footprint scaling, and the increasing computational demands, advanced device development for high-performance and low-power logic applications has routed towards stacking of complementary Silicon (Si) nanosheets. However, traditional Si technology is reaching a tipping point owing to its thickness scaling limitations. Alternative device geometries proposed to reduce leakage while improving electrostatics require materials with beyond-Si capabilities. The utilization of novel, inherently-low-dimensional, semiconducting channel materials with superior electronic properties such as 2D Transition Metal Dichalcogenides (TMDs) and 1D Carbon Nanotubes (CNTs) have been proposed to extend the technology roadmap beyond Si. Conversely, innovative approaches to integrate memory and logic functionalities are worth exploring to address computation demands by tackling data-transfer bottlenecks. Furthermore, always-ON, edge devices, connected across platforms in this digital age, pose a serious security threat. Hence, a ground-up makeover in the next-generation of electronics powered by beyond-Si TMD materials is implemented through a single logic transistor capable of integrating memory, sensing, and security primitives.

However, for beyond-Si-CMOS technology the need for enhancing p-type (hole) transport in 2D field-effect transistors (FETs) is identified as a critical yet challenging aspect. Tungsten Diselenide and Molybdenum Diselenide are proposed as promising 2D channel materials due to the more favorable Fermi-level pinning behavior near valence band edge. Techniques such as work-function engineering with the use of Palladium and contact interface optimization with the incorporation of Selenium, are explored to statistically improve hole injection efficiency. Following this strategy, a 3X reduction in contact resistance is achieved, down to $16 \text{ k}\Omega \mu\text{m}$.

Further, the research delves into threshold voltage engineering of p-type 2D channels using electrostatic modulation, gate dielectric optimization, and charge transfer oxide capping to achieve precise control over threshold voltage. Oxides of Molybdenum, Tungsten, and Germanium are studied in detail for their charge transfer mechanisms into the TMD channel. A large range in threshold voltage is achieved to modulate device behavior between high-performance and low-power operation with current switching ratio over 8 orders in magnitude.

Precise layer engineering strategies are also elaborated, aiming to refine the transport properties of p-type transistors through uniform bilayer growth and layer functionalization techniques. Monolayer oxidation by plasma treatment of bilayer WSe₂ channel with Palladium contacts, reduces contact resistance by 9X whereas functionalization by annealing in NO environment reduces contact resistance down to 3.5 k Ω μ m while maintaining current switching ratio over 6 orders in magnitude. Following this, an approach to achieving high-performance p-type 2D FETs is completed.

Finally, interface characterization in 1D CNT channels is discussed, presenting methods to mitigate interface defects by post-process annealing. Furthermore, temperature-dependent impedance analysis is employed to assess defect densities across the semiconductor energy gap. This concludes by underscoring the importance of interface characterization in all-interface devices such as devices on low-dimensional channel materials. This work aims to highlight the potential of low-dimensional materials for beyond-Si-CMOS logic.

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-Albert Einstein

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I dedicate this thesis to my beloved family

Mama Ji, Papa Ji, and Gaurav

Chapter 1

Introduction

The term “semiconducting” was first used in 1782 by Alessandro Volta before the Royal Society in London when he came across certain materials that discharged electricity in a non-zero amount of time by touching their surfaces with an electrometer.^{1,2} He went on to start a new field to experimentally study electrical properties of different materials. Humphry Davy, a British chemist, and the father of electrochemistry discovered that the resistivity of several metallic elements such as Cu, Ag, Sn, Pb, Fe, and Pt increased with temperature and following that, Michael Faraday, who knew about Davy’s experimental methods, for the first time, observed the opposite trend for a number of other materials, specifically Ag_2S . This material was very puzzling indeed and kept researchers busy for about 120 years.^{3,4}

Later on, the change of resistivity with irradiation was reported on Selenium and yet there was no clear understanding of the electronic phenomenon in materials. Ferdinand Braun, in 1874, discovered the rectification properties from a junction between a metal and metal sulfide the understanding of electrons as charged particles by J. J. Thomson was demonstrated following that in 1897. Although the problem of charged carriers in conductors was solved and the temperature dependence of resistivity for metals was made clear by Paul Drude, no understanding could be developed for the inverse dependence of resistivity with temperature for the anomalous set of materials that were studied by Michael Faraday. Johann Koenigsberger attempted to explain this anomaly by postulating that free electrons were a result of disassociation of atoms into fixed ions and mobile electrons and related the electron concentration in any given material to the change in temperature with a disassociation factor. However, a physical mechanism was still lacking. He termed the class of materials into “metals”, “insulators”, and “variable conductors.” The German scientist also demonstrated with the help of experiments that the disassociation factor in “variable

conductors” depended on the purity and defectivity of the material. Later on, in 1931, the band theory of this new class of material was developed by Alan Wilson. Thus, fundamentally, Koenigsberger’s semiconductor theory of disassociation energy was supported by the understanding of an energy gap that separates the sea of electrons from the sea of “holes”, the concept for which was introduced during the same time by Werner Heisenberg. The models for potential barriers and metal-semiconductor junctions were then developed in 1938 by Walter Schottky and Neville F. Mott. By 1942, the theory of thermionic emission was also developed by Hans Bethe. This marked the start of an exciting phase of discoveries to not only understand semiconductor materials but to also understand where they could fit in the consumer market.^{5,6}

Until the early 1950s, the field of semiconductors was looked down upon due to the lack of supported applications since the crystals obtained were very “dirty” and did not yield any results that were reproducible. This changed after the fabrication of the first junction “transistor” by William Shockley, John Bardeen, and Walter Brattain in 1951, shown in Figure 1-1a.⁷⁻⁹ The 1956 Nobel Prize in Physics was awarded for the discovery of semiconductors and the invention of the transistor effect. Following the invention of the transistor, the semiconductor industry took off very rapidly and had already reached a scale of \$100 million by 1957. This invention revolutionized the world as we see it today and led to the possibility of many more inventions. The first chip to have ever been fabricated was in 1959 and consisted of two transistors, some resistors, and capacitors. This chip, consisting of a bipolar planar integrated circuit was co-invented by Jack Kilby and Robert Noyce in 1959, shown in Figure 1-1b, leading to the dawn of the era for integrated circuits. In 1963, Frank Wanlass and Chih-Tang Sah invented the first complementary transistor logic.^{10,11} A figure from the patent is displayed in Figure 1-1c.¹² The advancement in the production of integrated logic circuits led to very large-scale integration (VLSI: 100,000 to 10,000,000 electronic components on a chip) and ultra large-scale integration (ULSI: >10,000,000 electronic components on a chip). There are many that are not named here

and have made a very significant contribution to bringing semiconductors into the market.

Several journal publications, patents, conferences from motivated individuals with a constant desire to understand and fierce market competition from semiconductor industry leaders led to the beginning of the Digital Revolution as we know it today. This Digital Revolution has seen the rise a rapid advancement in the functionality that these semiconductor chips offer and today these chips/wafers are capable of running an incomprehensible number of instructions parallelly. This has led to the establishment of a new Artificial Intelligence (AI) Revolution, which, we witness today, is capable of bringing in many more advancements not only in the way we perceive and utilize information but also how we create new information. Figure 1-1d shows an image of the largest single semiconductor wafer fabricated with the greatest number of transistors packed on a chip till date. Cerebras's Wafer Scale Engine, as they call it, can run a cluster worth of supercomputers on a single "large" chip, has about 900,000 cores, and is the fastest AI processor today.¹³ Figure 1-1e shows the most recently announced graphical processing unit (GPU) architecture from NVIDIA packs 208 billion transistors to run the latest generative AI models with increased energy efficiency.¹⁴ Finally, the most advanced computer processor from Apple, the M3 Max (Figure 1-1f), packs 92 billion transistors and runs on the latest commercially available transistor technology, the TSMC 3nm gate all around (GAA) structure.¹⁵ Although, it may seem like the transistor density on the chip is off the roof already and will soon saturate as the dimensions reach the physical limits, one who has witnessed the capability of semiconductors to power some of the most intricate generative AI models so powerfully and yet efficiently will only say that the best is not anywhere near.

COVID-related chip shortage that resulted in at least \$240 billion loss to the country's GDP in 2021. To resolve the supply-demand challenges and to effectuate and accelerate the leading-edge domestic semiconductor production, the bipartisan CHIPS for America Act was formulated.¹⁸ Although, foreign semiconductor producers retaliated to the surging chip demands by heavily investing in the U.S. on resources, manufacturing, and talent, there was a dire need for America to be self-reliant in producing more sophisticated and advanced semiconductor equipment for future electronic needs. As it is well known that the best time to plant a tree is twenty years back, similarly, now is the right time to invest in semiconductor fabrication facilities as it requires several years to build and set up. The CHIPS Act will boost semiconductor research, development, and manufacturing efforts to ensure the American leadership in an innovation that forms the basis of national defense, communication, automotive, exploration, consumer industries.

Current State of Logic and Computation

Transistors are a building block for any electronic equipment that we see around us. These electronics that are now the backbone of many sectors such as healthcare, manufacturing, automotive, and internet communication, make our day-to-day lives smarter, safer, and convenient. Both memory for data storage and logic for data computation have resulted in a continuous and rapid advancement in technology around us. This has further been made possible due to the continuous scaling of physical dimensions of a transistor on the electronic chip to achieve higher density which translates to making the chip more powerful and capable of higher data storage. However, scaling physical dimensions alone has not triggered this rapid growth. The success of the semiconductor industry has relied on continuous improvement in a variety of scientific fields of study such as material science, physics, chemistry, mathematics, and being

able to engineer each of these aspects has been equally important. Moreover, the economic and logistic limitations along with competitive pricing to instigate and meet consumer demands has fostered a continuous growth in the field.

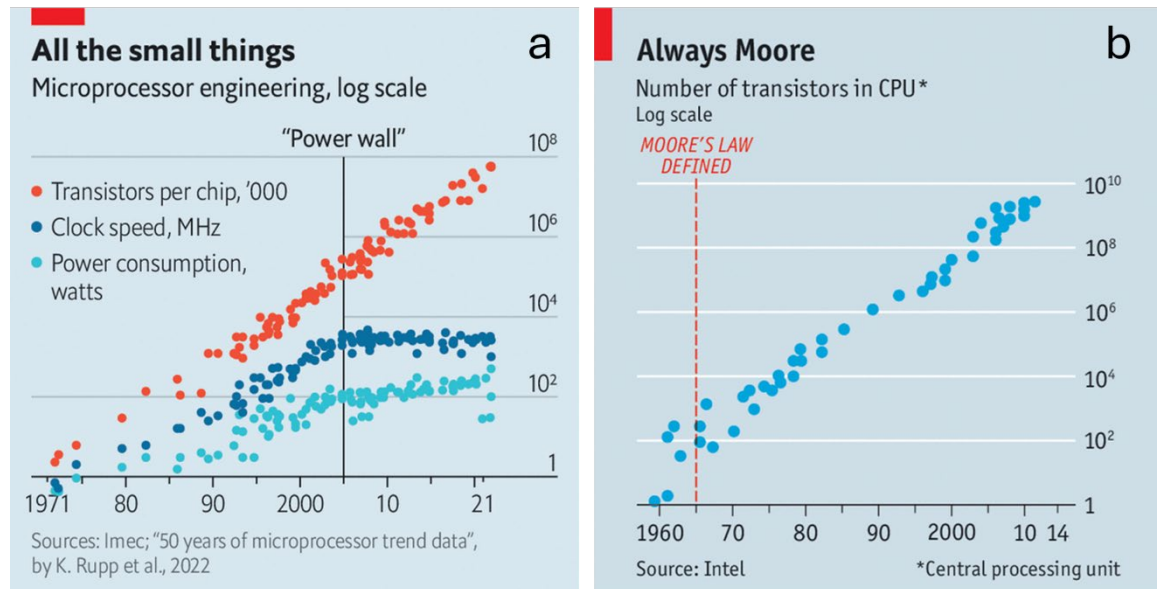


Figure 1-2: Trends in Microprocessor Evolution: a) The multi-faceted progression of microprocessor engineering over five decades, depicted on a logarithmic scale. The plot illustrates the exponential increase in transistor count per chip (red dots), a leveling off of clock speeds in MHz (blue dots) since hitting the “power wall”, and the concurrent plateau in power consumption in watts (light blue dots), reflecting efficiency improvements in microprocessor design. Data sourced from imec and “50 years of microprocessor trend data” by K. Rupp et al., 2022. b) A logarithmic scale visualization of Moore's Law, showing the steady increase in the number of transistors on central processing units (CPUs) from 1960 to the present (blue dots), underscoring the law's prediction of transistor count doubling approximately every two years. Data sourced from Intel. Image reproduced from *The Economist*.

Parallel advancement in manufacturing technology has made it fruitful in achieving the expectations from predictive trends that govern the powerfulness and pricing of electronic chips with every passing generation. One such law is termed the Dennard Law of Scaling, after Robert Dennard, which states that as transistors are physically scaled down in a generation, the power consumption of the chip that accommodates these transistors must remain constant from the previous generation, pictorially demonstrated in Figure 1-2a.^{19,20} The term “power wall”, as also

referred to in the figure denotes the point of time when the Dennard Law of Scaling failed, as a result of the increase in power consumption due to leakage and clock speeds could not keep up. This can be combined with another law that is famously known as the Moore's Law, after Gordon Moore, who predicted that the number of transistors on a chip would double every two years with minimal increase in cost, illustrated in Figure 1-2b.²¹ Collectively called the Koomey's Law, it stated that the performance capability of a chip would double every 18 months. Around 2006, it was found that the development could not keep up with Dennard's Law since the scaled physical dimensions imparted leakage issues which led to increased power consumption. Although the transistor count on the chip continues to double, the inability to increase clock frequencies for higher performance caps further improvement. However, overclocking resulted in an evolution of multicore processors to continue improvement in performance.

Memory is another essential component for computing alongside logic. A similar evolution in memory design for efficient memory-write, -erase, -read, -rewrite, and longevity of data storage has occurred over several decades. Cathode ray tubes, magnetic drums, delay lines, floppy disks, and hard disk drives; all of these played an important role towards our understanding and assessment of memory architecture until we finally developed the flash memory which helped make memory smaller, lighter, and affordable by implementing the MOS technology. However, there was still a recognizable difference in the speed at which memory read and write took place compared to that of the logic computation module. This led to the memory and logic modules being separated and linked by data communication buses. Hence, this form of separated memory and logic architecture came to be known as the von Neumann architecture and established itself as the convention.²² As computing efficiency is becoming a challenge, advancements in architecture and packaging are being looked at as the avenues for innovation. Even minute amount of energy loss and time delay is becoming more and more critical. The constant data transfer for concurrent storage and compute between the separated modules is

resulting in additional compute latency and costing additional energy. This requires a bottom-up reformation in the individual nodes of the edge computing architecture, which can therefore be achieved through material discovery, device innovation, and non-von Neumann computing alternatives.²³⁻²⁵ Additionally, these data collection and computation nodes are required to be highly secure which is possible by embedding additional security protocols into hardware components. Inspirations can also be drawn from the highly parallel, distributed, energy efficient, and adaptive, biological immune system, to conceive efficient and low-power, in-sensor and near-sensor computing alternatives.

Need for Material Innovation

Physical limitations in the most dominant and widely studied semiconducting material, Silicon (Si), led to the investigation of alternative semiconducting channel materials that could potentially replace Si. Field effect transistors (FETs) fabricated on Si when scaled in different device components faced the following issues: i) increasing bandgap due to quantum confinement, ii) roll-off in switching threshold voltage and disproportionate scaling of supply voltage, iii) carrier velocity saturation, iv) increasing leakage current across the contacts, v) worsened subthreshold switching behavior, vi) increased tunneling current density across the dielectric, vii) degradation in the carrier mobility due to scattering, and viii) heat dissipation issues.²⁶⁻²⁸ Furthermore, scaling gate length to keep up with FET scaling expectation requires a thinner channel for better electrostatic control.²⁹ To overcome the above limitations, alternative channel materials to Si, such as Ge, III-V compounds provide excellent transport properties. However, electrostatic control at scaled dimensions still remains a challenge. Low-dimensional materials that are inherently thin along with excellent electronic properties have provided an avenue for continued exploration of an alternative to Si. Low-dimensional materials such as two-

dimensional (2D) materials and one-dimensional materials (1D) are some of the most widely explored candidates and have been evaluated to retain their electronic properties when confined in one or two dimensions respectively.³⁰⁻³² Moreover, they possess unique mechanical properties such as high tensile strength, high intrinsic thermal conductivity, and high strain resilience making them suitable for non-rigid, flexible advanced consumer electronic products.

Two-dimensional Materials

Two-dimensional (2D) materials have gained substantial interest for their promising electrical properties as channel materials in FETs.³³⁻³⁵ They exhibit weak van der Waals (vdW) bonds between layers, allowing for easy exfoliation of atomically thin layers from their respective bulk crystals. Due to their naturally thin dimension, they can be thinned down to a single atomic layer and still have no degradation in their electronic properties unlike other bulk semiconducting materials. Additionally, their ultra-thin and inert nature allows for excellent electrostatic gate control for large scale integrations. Scaling down the 2D field effect transistors is relatively easier to achieve in comparison with the conventional bulk materials because of higher-resilience to the “short-channel effects”. While the first demonstration of 2 nm Si-based nanosheet technology by IBM was impressive, thickness scaling of Si remains a challenge without compromising the performance.³⁶ The absence of dangling bonds in these materials can potentially help achieve better interface for better electrostatic control. Figure 1-3a shows a plethora of 2D materials that have been explored with varying bandgaps. These materials, depending on the bandgap, material composition, and configuration, can be utilized as metals, semiconductors, and even insulators.

After the first report of exfoliated monolayer Graphene on SiO₂, with mobility as high as $\sim 10,000 \text{ cm}^2/\text{Vs}$ was published in 2004, Graphene received great attention as a channel material.^{37,38} Higher than predicted mobility values have also been achieved ($\sim 100,000 \text{ cm}^2/\text{Vs}$)

by passivating and gating the layered graphene with hexagonal boron nitride (h-BN) which prevents any surface scattering by phonons. Due to the absence of a bandgap, a much less ON/OFF ratio with graphene field effect transistors makes it less suitable for digital logic applications. Although novel electronic switching devices have been proposed that fundamentally introduce a bandgap by narrowing the graphene into graphene nanoribbons or utilize tunneling based transport in graphene FETs, scalability remains a question.³⁹⁻⁴¹ Another class of 2D materials that have attracted immense attention are transition-metal dichalcogenides (TMDs).⁴² TMDs consist of layered hexagonal transition metal (M) atoms sandwiched between two layers of chalcogen (X) atoms with a general formula of MX_2 . Figure 1-3b shows a characteristic image of the atomistic structure as well as the bonding in a 2D TMD monolayer with another monolayer. Layered and stacked heterostructures of 2D materials have reportedly been shown to demonstrate exotic superconducting and semiconducting behavior at different twist angles.^{43,44} Additionally, based on their energy band alignment, they show intrinsic n-type (MoS_2 , WS_2 etc.), p-type (BP), and ambipolar (WSe_2 , MoSe_2 , MoTe_2) transport properties.⁴⁵ Doping these materials to tune the electronic transport has also been demonstrated but has achieved limited success in terms of scalability. Due to quantum confinement effects, electronic properties in these TMDs depend on the number of layers. This can cause variability among devices fabricated on flakes. With development in wafer-scale, low temperature synthesis of TMD materials using chemical vapor deposition (CVD), metal organic chemical vapor deposition (MOCVD), and physical vapor deposition (PVD), TMD materials have been brought much closer to being compatible with large-scale semiconductor processing standards.

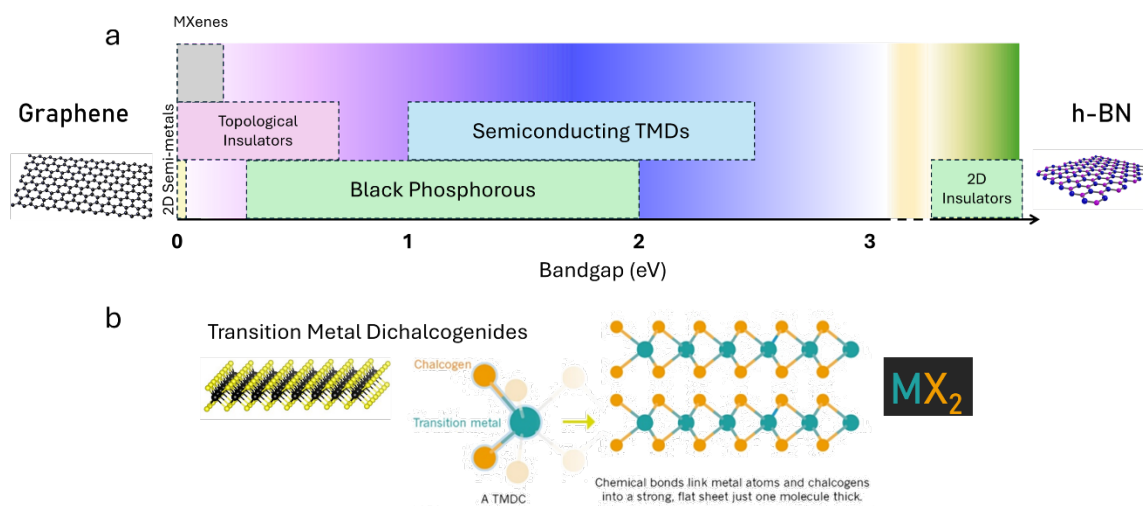


Figure 1-3: Landscape of Two-Dimensional (2D) Materials: This figure illustrates the spectrum of 2D materials categorized by their electrical properties. Starting from conductive graphene on the left, the gradient transitions through topological insulators, semiconducting transition metal dichalcogenides (TMDs), and black phosphorus, to insulating materials on the right. Insets show atomic-scale representations: a) Graphene's honeycomb lattice, known for its exceptional conductivity and strength, b) A layered structure of TMD with the transition metal sandwiched between two chalcogen atoms in MX_2 configuration. The chemical bonds between metal and chalcogen atoms result in a strong, flat atomically thin sheet. This diversity underpins the potential of 2D materials to revolutionize electronics, with each material offering distinct advantages for specific applications, ranging from transparent conductors to semiconductors for flexible electronics.

One-dimensional Materials

One-dimensional (1D) materials exist in the form of nanotubes (NTs) or nanowires (NWs) and can range in diameter without any restriction in lengths.⁴⁶ Their physical structure allows for quantum confinement in two dimensions and results in interesting optical and electronic properties. Materials such as ZnO NWs, III-V NWs, Carbon Nanotubes (CNTs) offer very high carrier mobilities along with cylindrical geometry for optimum electrostatic control making them promising candidates for channel materials in advanced logic devices. Different materials offer different energy bandgaps making them ideal for detection and emission of light in different wavelength spectrum. These 1D materials are gaining extensive interest in the field of

photovoltaics, light emitting diodes (LEDs), photodetectors allowing for integration on non-rigid substrates.^{47,48}

Out of the many 1D materials, CNTs are the most widely explored semiconductors.^{49,50} These vary by the number of cylindrical layers and are distinguished as single-wall CNTs (SWCNTs) and multi-wall CNTs (MWCNTs) and their diameters can range from 1 nm to 100 nm, both shown in Figure 1-4a.⁵¹ These materials can be simply understood as a wrapped-around sheet of Graphene. Furthermore, the chirality of the CNTs also determines their physical structure. Chirality is used to define reflection symmetry. The chiral symmetry in a 1D SWCNT is illustrated for better understanding in Figure 1-4b.⁵² A chiral object is one whose mirror reflection cannot be superimposed onto itself. SWCNTs can be either chiral or achiral, where achiral CNTs are further divided into armchair and zigzag configuration CNTs. Of these different CNTs, zigzag CNTs seem to be the most interesting since they can be either metallic or semiconducting depending on their band structure and the diameter of the CNT determines the bandgap but not the chirality. Their alternating coexistence as metallic and semiconducting makes them essentially unique since they can be used as interconnects or in the FET semiconducting channel.

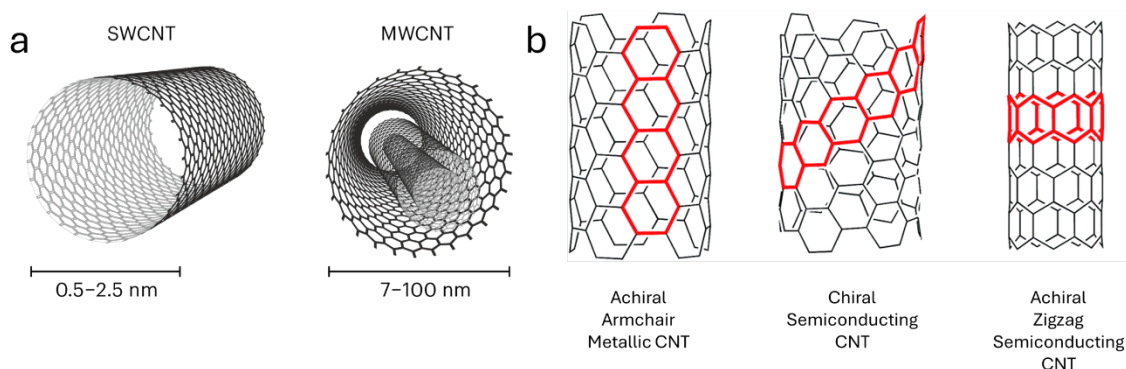


Figure 1-4: Structural Diversity and Chirality in Carbon Nanotubes (CNTs): a) A single-walled CNT with its characteristic cylindrical structure, and a multi-walled CNT, illustrating the concentric assembly of multiple CNT layers. b) Three distinct chiral vectors (red) of CNTs, achiral armchair, achiral zigzag, and chiral structures, each determining the electronic properties of the

nanotubes, such as metallic or semiconducting behavior. The chirality of CNTs is crucial for their integration into electronic devices, as it directly influences conductivity and band structure, parameters essential for the design of advanced nanoelectronic applications.

Transistors on Low-dimensional Materials

Due to their excellent electronic properties, high surface area, and high mechanical strength, a plethora of applications in wearable and flexible electronics for biochemical sensing have already been investigated.⁵³ Their limitless reach in academia, defense laboratories, and industries as a testbed to carry out exploratory research has made them mature for realizing large-scale applications. More importantly, world-known semiconductor foundries and manufacturers have started investigating on the electronic properties for these low-dimensional materials to be used as semiconducting channel in place of Si or to complement Si, the most studied and established material. Corporate research and pathfinding labs in Taiwan Semiconductor Manufacturing Company (TSMC), Intel, Samsung, Applied Materials, Apple are among the top companies that have considered investing in extending the logic roadmap with low-dimensional channel materials.^{54,55} Transistors, as explained earlier are a fundamental building block of any electronic component. Transistors built on these low-dimensional materials stand to not only continue the trend of Moore's Law but also to provide pathways to overcome the physical and technical limitations faced by Si-based devices.^{56,57} Hence, the development of transistors on low-dimensional materials is not merely an academic pursuit; it is a necessity to meet the evolving demands of technology that is becoming ever more integrated into the fabric of daily life.⁵⁸

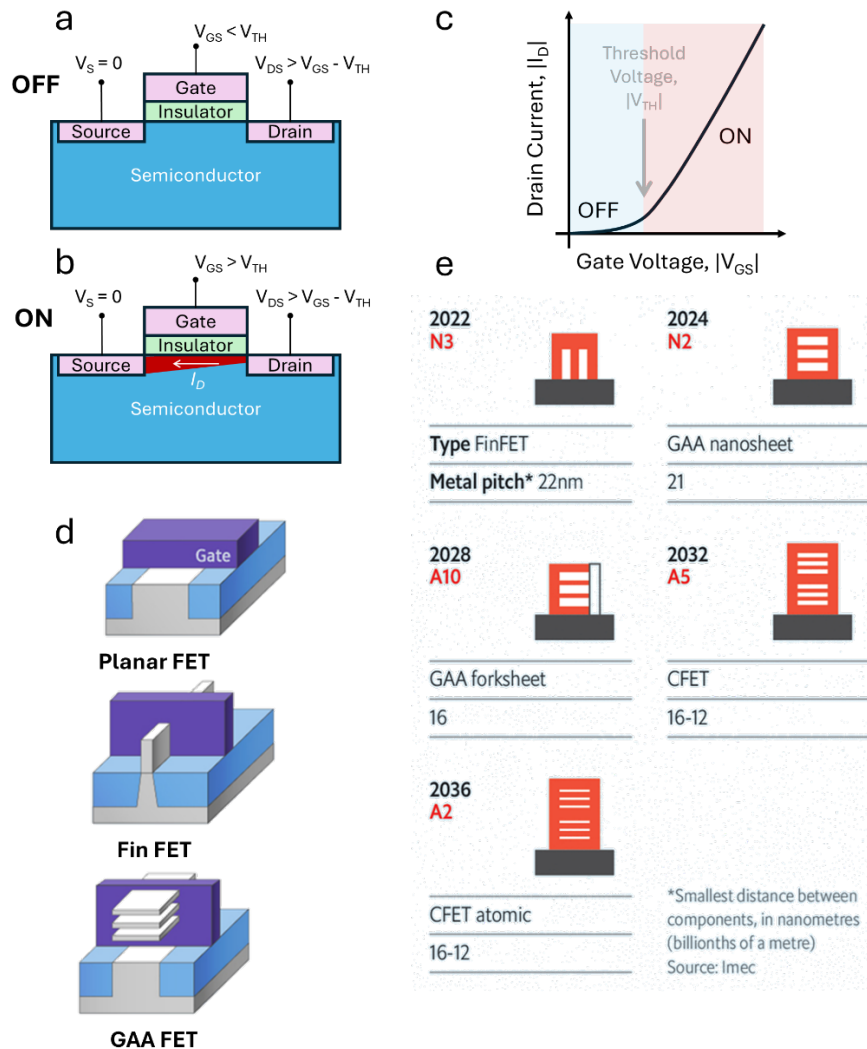


Figure 1-5: Transistor Structure and Design Evolution: a) Three-terminal Metal Oxide Semiconductor Field-effect Transistor (MOSFET) device structure in its planar geometry in the logical '0' or 'OFF' state, b) MOSFET in the ON state with the carriers injected from the source terminal, transported to the drain terminal, under the presence of a lateral field. The electrostatic modulation of the conductive channel is influenced by the transverse field applied at the gate terminal which switches the device to logical '1' or 'ON' state, c) Current-voltage characteristics of the MOSFET show the minimum potential that must be applied to the gate terminal, determined by the MOSFET's threshold voltage (V_{TH}), to switch the device from the 'OFF' state to the 'ON' state. d) The evolution and scaling trends in transistor technology from planar structure to traditional FinFET structures to more advanced Gate-All-Around (GAA) nanosheet configurations. e) A timeline displays transistor scaling milestones, with each bar representing a significant step in the reduction of feature sizes, moving towards smaller and more efficient transistor architectures with finer metal pitches. Data source: imec.

Traditional transistor, short for Metal-oxide Semiconductor Field-effect Transistor (MOSFET) is the cornerstone of modern microelectronic devices.^{26,59,60} MOSFET is a three-terminal device comprising of gate, source, and drain terminals, as depicted in Figure 1-5a. The MOSFET's ability to switch between "ON" and "OFF" states, more conventionally referred to as the binary logic states, "1" and "0", with minimal power consumption, along with higher scalability and lower footprint, has been the key criteria for its development. The switching of the MOSFET is triggered by the minimal electrostatic potential applied at the gate terminal (gate-to-source voltage, V_{GS} must be greater than the MOSFET threshold voltage, V_{TH}), thereby tuning conductivity of the so-called channel that lies between the source and drain terminals. Figure 1-5b shows a planar MOSFET in the ON state with the conduction path due to the flow of electrons from source to drain, depicted in red, allowing I_D current to flow. This logical electronic switch is electrically characterized by current-voltage characteristics, shown in Figure 1-5c, depicting the transition from OFF state to the ON state at the switching threshold voltage. Every generation of the FET has succeeded the previous one with breakthroughs in material innovation, design, and processing advancement. The criteria for an advancement to be worthy of a new generation used to be defined by the Dennard Law of Scaling until early 2005. Following that, advancements in material discovery such as the high-k metal gate leading to minimal switching power, next-generation uniaxial strained Silicon leading to improved mobility, tri-gate/fin-FET to gate-all-around (GAA) structures resulting in higher electrostatic control, and the latest tech high-NA (numerical aperture) EUV (extreme ultraviolet) lithography advancing patterning to an amazingly small and crisp level.⁶¹⁻⁶³ The evolution in device structure of a MOSFET for better performance and better electrostatic control has been shown in Figure 1-5d. Following the implementation of the GAA FET, many more generations of FET structures have been proposed that utilize the epitaxial growth of Si on amorphous interlayers to stack channel in three dimensions and further reduce the device footprint. This has been shown in Figure 1-5e.

To better understand the fundamental operation of a MOSFET, it becomes useful to first sketch the idea of a MOS capacitor (MOSCAP) structure, since it helps explain the electrostatics of the gate without bringing in the aspect of lateral transport in the channel. In this section, the fundamental operation of MOSFET is explained after the basis of various semiconductor devices is established with the help of MOS structure.

Metal Oxide Semiconductor (MOS) Structure

MOS structure comprises of metal gate electrode, an insulating oxide layer, and a semiconducting material (Si substrate), as depicted in Figure 1-6a. The metal gate is typically made from highly conductive materials like aluminum or polysilicon, while the insulating layer is usually silicon dioxide (SiO_2) or silicon nitride (Si_3N_4). The semiconductor substrate can be either p-type or n-type, depending on the desired characteristics of the MOSCAP. The device may be considered to be under zero bias or under the application of a finite bias. General relations of charge neutrality may be used to study the charge distribution across the MOS structure. Any charge present in the semiconductor may be integrated until the edge of its interface with the insulator. The insulator is devoid of any charge, given that it is free of any defects. The metal, abundant of charge, although rejects volume charge but allows the charge to be present at the interface with the insulator. The two charge distributions depicted in Figure 1-6b on either side of the interface, $-Q_s$ in the semiconductor and Q_g at the gate/insulator interface therefore satisfy the overall charge neutrality. Field lines emerge from the sheet charge at the metal/insulator interface and terminate at the charge in the semiconductor. As a result, there is no field deep inside the semiconductor or the metal. However, the electric field in the insulator, ϵ_{ins} , is finite and is given by,

$$\epsilon_{ins} = -\frac{Q_s}{\epsilon_{ins}}$$

where ϵ_{ins} is the permittivity of the insulator. Electric field, ϵ_{ins} , is uniform inside the insulator since we have considered an ideal, defect-free insulator. The dissimilar materials stacked together exhibit different permittivity hence, the electric field is discontinuous. The continuity of the electric displacement vector helps obtain the normal components of the electrical field on both sides of the interface, given by,

$$\epsilon_s \epsilon_s = \epsilon_{ins} \epsilon_{ins}$$

The relationship between the electric field and charge in the semiconductor is given below as,

$$\epsilon_s = -\frac{Q_s}{\epsilon_s}$$

Electric field in the structure is shown in Figure 1-6c. The electrostatic potential drop across the structure (Figure 1-6d), also denoted as the built-in potential, ϕ_{bi} , given as the sum of the potential drop in the semiconductor (ϕ_s) and the potential drop in the insulator (ϕ_{ins}). Hence,

$$\phi_{bi} = \phi_s + \phi_{ins}$$

We can now calculate the potential drop across the insulator since the field in the assumed ideal insulator is uniform.

$$\phi_{ins} = \epsilon_{ins} t_{ins}$$

where t_{ins} defines its thickness and the capacitance of the insulator is, as we know it,

$$C_{ins} = \frac{\epsilon_{ins}}{t_{ins}}$$

Therefore, the built-in potential across the MOS structure is,

$$\phi_{bi} = \phi_s - \frac{Q_s}{C_{ins}}$$

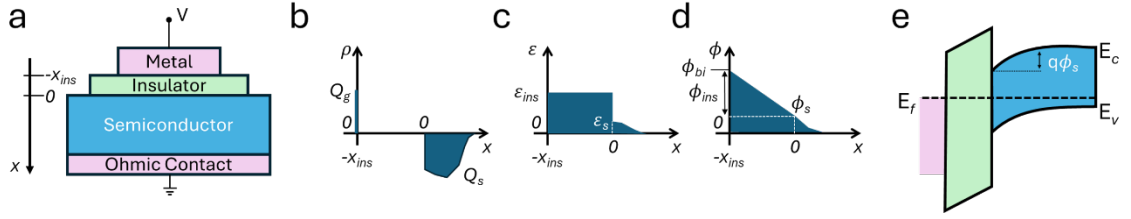


Figure 1-6: Metal Oxide Semiconductor (MoS) Fundamentals under Zero Bias: a) Device schematic of a MOS structure with the respective coordinate system pointing into the semiconductor and the origin being at the insulator/semiconductor interface. b) Distribution of volume charge density in space shows that the charge density in the semiconductor extends to some depth from the interface and the integrated charge density in the semiconductor is Q_s balanced by some charge at the gate metal/insulator interface, Q_g , c) electric field in the MOS stack, d) electrostatic potential profile across the MOS structure denoting a total potential drop ϕ_{bi} , e) total band bending inside the semiconductor is given by the surface potential, ϕ_s .

Hence, this applies to any MOS structure at any given bias. This helps us illustrate band-bending in MOS physics, as shown in Figure 1-6e. Analyzing the charge distribution and electric field displacement through the structure can be useful to obtain the potential difference across any given interface. In this way, the total band-bending in the semiconductor is $q\phi_s$.

MOS structure Capacitance-Voltage Characteristics

Band diagrams for a MOS structure (Figure 1-7a) are the most optimum way to explain the different regimes of operation. Under the flatband condition, no electric field exists in all three materials and there is no exchange of charge across any junction. Thus, the free electron level, commonly referred to as the vacuum level is the same and the Fermi level of the entire system is in equilibrium. The Fermi level, defined by the Fermi-Dirac statistics, gives the probability of occupancy of an electronic state at a given energy level to be exactly one-half. Flatband voltage (V_{fb}) in a MOS device, given by,

$$V_{fb} = (\phi_m - \phi_s) - \frac{Q_{ins}}{C_{ins}}$$

where ϕ_m is the work function of the gate metal, ϕ_s is the work function of the semiconductor, Q_{ins} is the equivalent charge in the insulator, and C_{ins} is the capacitance of the insulator, both normalized per unit area. The contribution of Q_{ins} for extremely low t_{ins} in modern VLSI devices is meager and therefore, the flatband voltage is nothing but the difference in the work function of the gate metal and the semiconductor.

The MOS structure operates in several distinct regimes, depending on the applied gate voltage (V_G). These regimes are characterized by the distribution of charges in the semiconductor and the formation of different types of layers at the semiconductor-insulator interface. For each regime of operation, the charge distribution schematic has been provided along with the energy band diagram corresponding to the situation in a MOSCAP structure with a p-type semiconductor. The capacitance-voltage (C-V) characteristics can be seen in Figure 1-7k. One can refer to each mode of operation while analyzing the device charge distribution schematic, band diagram, and C-V curve, simultaneously.

1. **Accumulation:** (Figure 1-7b, g) When a negative voltage is applied to the gate of a p-type MOS structure (or a positive voltage in a n-type), majority carriers (electrons in n-type, holes in p-type) accumulate at the semiconductor-insulator interface because they are mobile, thus forming an accumulation layer, as a result of the electric field in the insulator. Once in accumulation, the accumulation charge only increases linearly as a function of the applied gate voltage. In this regime, the capacitance of the stack is as high as the capacitance of the insulator capacitance, C_{ins} since the semiconductor capacitance in accumulation is large.
2. **Flatband:** (Figure 1-7c, h) The flatband condition occurs when the applied gate voltage exactly cancels out the built-in potential differences within the MOS structure, making the energy bands in the semiconductor flat. The flatband voltage, V_{fb} , is an important

parameter as it provides information about the work function difference between the gate metal and the semiconductor, as well as the charge within the insulator or at the interface.

3. **Depletion:** (Figure 1-7d, i) As the gate voltage becomes less negative in a p-type (or less positive in an n-type) MOS structure, the majority carriers are repelled from the surface, leaving behind a depletion region devoid of free charge carriers. This region is now filled with immobile ionized donors in p-type (or acceptors in n-type) semiconductors. The capacitance decreases because the depleted semiconductor capacitance, C_d , adds series capacitance to C_{ins} . The change in the built-in potential across the structure determines the length of the depletion region.
4. **Threshold:** (Figure 1-7e) The transition from the depletion regime to the onset of strong inversion is marked by the threshold voltage (V_{th}). This is a critical parameter for MOS devices, indicating the gate voltage required to create a significant inversion layer at the semiconductor surface.
5. **Inversion:** (Figure 1-7f, j) If the gate voltage is more positive in a p-type MOS structure (or more negative in an n-type), it eventually inverts the semiconductor surface, creating a thin layer of minority carriers (holes in n-type, electrons in p-type) at the semiconductor surface. This inversion layer behaves similarly to a semiconductor of the opposite type, forming a p-n junction at the interface. In the strong inversion regime, the capacitance approaches the C_{ins} again, as the inversion layer has a large capacitance. This is achieved by further increasing the gate voltage so that the concentration of minority carriers at the semiconductor surface is greater than or equal to the concentration of majority carriers in the bulk.

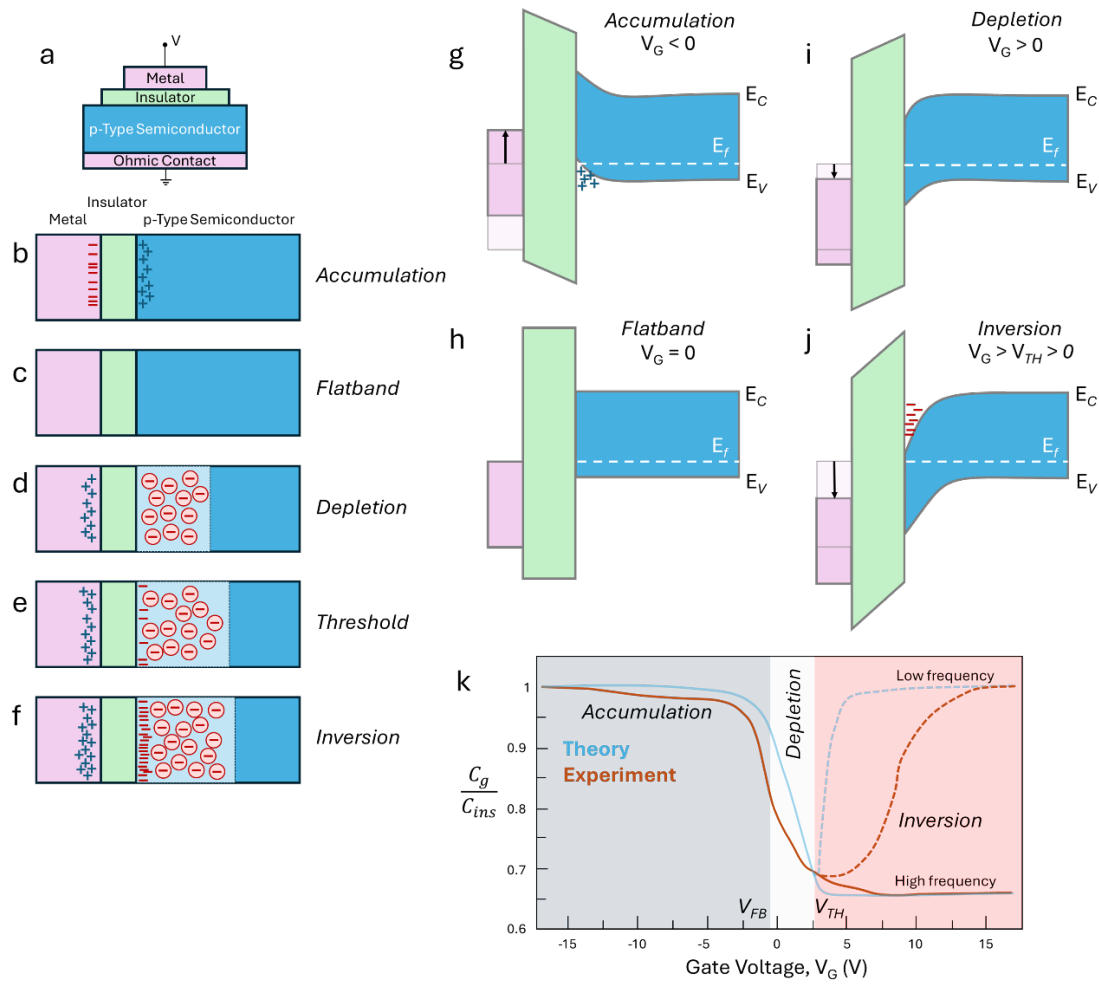


Figure 1-7: Device Physics of a Basic MOS structure under Bias: a) Device schematic of a MOS capacitor structure with a p-type semiconductor and b-f) illustrations of the charge distribution under the application of varying bias along with the corresponding energy band diagrams in g-j). For a small negative voltage applied to the gate metal, the structure is in b, g) accumulation and as the bias is increased, c, h) flatband situation is reached when there is no potential difference across the structure, further increasing the gate voltage causes the d, i) depletion region to widen until the device reaches e) threshold, beyond which there is an f, j) inversion layer formed in the semiconductor surface closer to the insulator and the device is in inversion. k) Capacitance-voltage (C-V) characteristics of a typical MOS structure denoting different regimes at low and high frequencies of small signal voltage.

However, in experimental C-V curves, several deviations from the ideal theoretical behavior can be observed due to various factors, including:

1. Interface trap states: The presence of interface trap states at the semiconductor-oxide interface can lead to a stretching out of the C-V curve in the depletion region, known as

the "distortion" or "hump" in the C-V curve. This distortion is caused by the exchange of charge carriers between the semiconductor and the interface trap states as the surface potential changes.

2. Oxide trapped charges: Fixed oxide charges or mobile oxide charges can shift the entire C-V curve along the voltage axis, indicating the presence of an effective oxide charge.
3. Polysilicon depletion effects: In MOSCAP structures with polysilicon gates, the depletion of the polysilicon gate at high frequencies can lead to a deviation from the ideal C_{ins} in the accumulation and inversion regions.
4. Minority carrier generation: In the depletion region, the generation of minority carriers can lead to a deviation from the ideal C-V curve, particularly at high frequencies.

A MOS structure is a true capacitor, and an equivalent circuit can be used to explain the MOS electrostatics behavior, as demonstrated in Figure 1-8.⁶⁴ Device parameters such as threshold voltage, flatband voltage, insulator and interface properties, and semiconductor doping levels can be extracted. Furthermore, it can also be used to study the non-idealities in the device induced from process-related or uncontrolled variations. Capacitance is defined as the change of charge resulting from small changes in voltage applied as an AC voltage and is given by,

$$C = \frac{dQ}{dV} \text{ and } C = \frac{1}{1/C_{ins} + 1/C_s}$$

Capacitance of a MOS structure is the sum of insulator capacitance (C_{ins}) and semiconductor capacitance (C_s) in series. Hence, the total capacitance of the structure varies depending on the regime of operation. For the below equations, q is the electron charge, k is the Boltzmann's constant and T is the temperature (300 K unless otherwise specified).

In the accumulation regime, when bias voltage, $V < V_{fb}$

$$C \cong C_{ins} \frac{1}{1 + \frac{2kT}{q(V_{fb} - V)}}; C_s \cong \frac{q}{2kT} C_{ins} (V_{fb} - V)$$

When the flatband condition is met at $V = V_{fb}$,

$$C \cong C_{ins} \frac{1}{1 + C_{ins} \frac{L_D}{\epsilon_s}}; C_s \cong \frac{\epsilon_s}{L_D}$$

where L_D is defined as the Debye length denoting the extent of distance over which electrostatic perturbations can be experienced.

When the device is in depletion, i.e., when $V_{fb} < V < V_{th}$,

$$C \cong \frac{C_{ins}}{\sqrt{1 + 4 \frac{V - V_{fb}}{\gamma^2}}}; C_s \cong \frac{\epsilon_s}{W_D}$$

where γ is the body factor given by $\gamma = \frac{1}{C_{ins}} \sqrt{2\epsilon_s q N_A}$ and N_A is the concentration of acceptor ions given for the case of a p-type semiconductor. Depletion width, W_D , is the extent of the semiconductor devoid of any mobile charge. Maximum depletion width is given by, $W_{D,max} = \sqrt{\frac{2\epsilon_s \Psi_B}{q N_A}}$. Surface potential of semiconductor at $V = V_{th}$ is $\Psi_B = \frac{kT}{q} \ln \frac{N_A}{n_i}$, where n_i is the intrinsic carrier concentration. This capacitance is of utmost importance to study the subthreshold performance of the MOS device and an assumption that $V = V_{th}$ can be made.

When the device is in inversion, for $V > V_{th}$,

$$C \cong C_{ins} \frac{1}{1 + \frac{2kT}{q(V - V_{th})}}; C_s \cong C_{inv} + C_d$$

where C_{inv} is the inversion layer capacitance.

The above explanation holds valid for the MOS structure measured at low frequencies. At high frequencies, the device operation changes. The carriers in the semiconductor are expected to respond to the changing AC voltage. In accumulation, the majority carriers that have accumulated

near the surface and the AC response is easier due to the constant source of majority carriers from the Ohmic contact. The time for this process is limited by the slower of the two components, namely the dielectric relaxation time or the RC time constant of the MOS structure. Since this is a fast phenomenon, the accumulation regime remains unaffected by the change in frequency. For the case of depletion, the majority carrier concentration requires modulation at the edge of the depletion regime as compared to at the surface. Similar to the previous case, depletion regime also remains unaffected by the change in frequency. However, in the inversion regime, in order for the minority carriers to respond to the high frequency AC signal, more minority carriers need to be generated in the semiconductor itself, which is limited by the generation time constant, or commonly known as the minority carrier response time, which is relatively slow. In this regime, the thickness of the depletion region stays the same. The closest region where the AC modulation to satisfy the electrostatics can take place is therefore at the edge of the depletion region. Hence, it can be concluded that, at high frequencies, the inversion capacitance of a MOS structure is equal to the depletion capacitance.

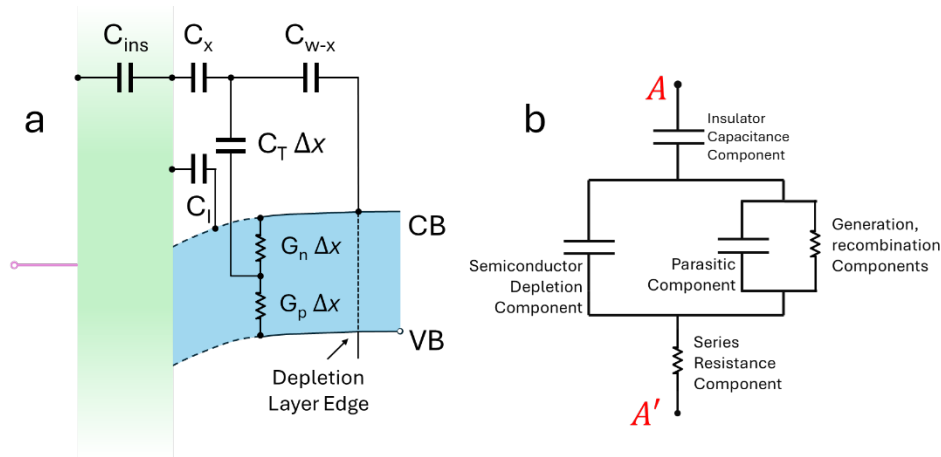


Figure 1-8: Equivalent circuit of a MOSCAP structure: a) Equivalent circuit for a MOSCAP structure considering the generation and recombination factors at a width of Δx into the depletion layer at a distance x from the semiconductor surface. On the right, in blue, is the semiconductor with the band edges denoted by conduction band (CB) and valence band (VB) for a p-type Si. Measurement terminals are indicated by circles. For a single level interface trap state, the capacitance C_{w-x} will be replaced by the depletion semiconductor capacitance, C_x (also, depletion

capacitance), and $C_T\Delta x$, $G_n\Delta x$, and $G_p\Delta x$ shall be replaced by C_T , G_n , and G_p . b) Equivalent circuit for a single-level interface trap state situation with capacitive and resistive trap components, given the semiconductor is in depletion.

Metal Oxide Semiconductor Field Effect Transistor (MOSFET)

MOSFET is the building block for modern VLSI devices and memory systems.⁶⁵⁻⁶⁷ It is required to be a unipolar device with a single type of majority carrier flowing across the source and drain contacts, in the channel, the conductivity of which can be electrostatically tuned by the gate. A conventional planar Si MOSFET is fabricated by doping two n⁺ regions in a p-type substrate (or two p⁺ regions on an n-type substrate) separated by a characteristic channel length (L_{ch}), to form an n-type channel (or a p-type channel), followed by the formation of a gate oxide on top of the channel with a gate metal deposited on top. The MOSFET can be considered as two p-n junctions connected back-to-back with the device known to work with low leakage currents. Its operation is based on the principles of operation of a MOS structure. When a large positive (or negative) gate voltage is applied to the gate metal, the excess of majority carriers, electrons (or holes) at the surface of the Si form a conductive path for current to flow across the ion-implanted/doped source and drain regions given a voltage difference exists across the source and drain terminals. Source terminal is considered as the reference terminal grounded at $V_S = 0$ V. Hence, gate voltage (V_{GS}) and drain voltage (V_{DS}) are applied with reference to the grounded source terminal. Current is measured at all three terminals and is denoted as drain current (I_D), source current (I_S), and gate current (I_G). Although current is only measured at a given terminal and not in reference to another terminal unlike voltage, drain current is interchangeably denoted with I_{DS} and drain voltage is interchangeably denoted with V_D .

The operation of a MOSFET can be simplified using a water reservoir analogy.⁶⁷ Two source and drain contacts depicted by water reservoirs separated by the channel such that the flow of water from one reservoir to the other is restricted by a gate barrier that can be lowered or raised. When the barrier is above the minimum height (threshold, V_{th}) that allows water to flow across, there will be no flow of water (carriers) and the device is understood to be in the cut-off regime, because $V_{GS} < V_{th}$. When the barrier is lowered and the barrier height is below the water level in both source and drain reservoirs, the flow of water over the barrier is determined by the barrier height. By applying a $V_{DS} > 0$, a positive electric field is induced across the source and drain terminals, and this results in the drift of majority carriers in the inversion layer from one reservoir to the other. This case corresponds to the linear or triode regime of device operation. In this case, $V_{GS} > V_{th}$ and $V_{GD} > V_{th}$. Now, if the barrier height is lower than the water level in the source reservoir but above the water level in the drain reservoir, the flow of water is independent of the water level in the drain reservoir with respect to the water level in the source reservoir. This is related to the saturation regime of device operation. In this case, $V_{GS} > V_{th}$ but $V_{GD} < V_{th}$. The electric field in the channel is only affected by the applied V_{GS} and not by V_{DS} because as the velocity of the carrier increases along the channel, the carrier simply drops down into the drain reservoir and the inversion layer in “pinched off” near the drain end of the channel. This is also a very important regime of device operation because it is in this regime that the MOSFET can be operated as an amplifier.

In the context of MOSFET operation, the Fermi-Dirac distribution plays a crucial role in determining the carrier concentration and their energy distribution, which are vital for understanding how carriers are injected across barriers within the device. It is also crucial in analyzing carrier injection across barriers, such as from the source to the channel in a MOSFET. The Fermi-Dirac distribution is a fundamental principle in quantum statistics that describes the probability of occupation of energy states by fermions (particles like electrons that follow the

Pauli exclusion principle) in a system at thermal equilibrium. The distribution is given by the formula:

$$f(e) = \frac{1}{1 + e^{-\frac{(E-E_F)}{kT}}}$$

where $f(e)$ is the probability of occupation of an energy state E , E_F is the Fermi energy level, which is the chemical potential at absolute zero temperature, k is the Boltzmann's constant, and T is the temperature in Kelvin.

Injection efficiency across a potential barrier (like the source/channel barrier in a MOSFET) depends on the barrier height relative to the Fermi level and the thermal energy of the carriers, as denoted in Figure 1-9a for electrons and in Figure 1-9b for holes. Carriers must have enough energy to overcome the potential barrier created by the gate voltage and the built-in potential of the device. At non-zero temperatures, carriers can be thermally excited to higher energy states. The probability of finding an electron with enough energy to cross the barrier is given by the tail of the Fermi-Dirac distribution at energies above the barrier height. In an n-type MOSFETs, a positive V_{GS} can lower the potential barrier for electrons from the source to the inversion layer, aligning the Fermi level of the source closer to or even above the conduction band edge at the interface. The Fermi-Dirac distribution helps predict the proportion of electrons with sufficient energy to cross over and contribute to the current.

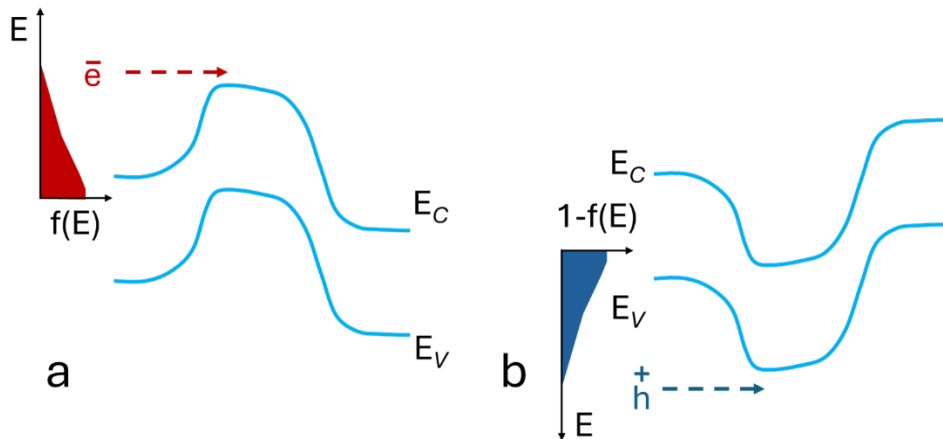


Figure 1-9: Energy band diagram across the MOSFET barrier. Band diagrams depicting injection of Fermion over the barrier in the direction of source to drain for a) electrons, b) holes.

MOSFET Current-Voltage Characteristics

Transfer Characteristics of a MOSFET: The transfer characteristics of a MOSFET, shown in Figure 1-10a, entail how the drain current (I_D) varies as a function of the gate-to-source voltage (V_{GS}) while keeping the drain-to-source voltage (V_{DS}) constant. This characteristic is crucial for understanding how effectively a MOSFET can be turned on and off with changes in gate voltage.

- **Subthreshold Region:** Below the threshold voltage (V_{TH}), the MOSFET is technically "OFF," but a small subthreshold leakage current still flows due to carrier diffusion. This current exponentially increases as V_{GS} approaches V_{TH} .
- **Above Threshold Region:** When V_{GS} exceeds V_{TH} , a strong inversion layer forms, and the channel becomes highly conductive. The current increases sharply and then gradually levels as V_{GS} increases further. This part of the curve is almost linear initially (ohmic region) and then plateaus (saturation region) depending on the value of V_{DS} .

Output Characteristics of a MOSFET: The output characteristics of a MOSFET, shown in Figure 1-10b, describe how the drain current (I_D) varies with the drain-to-source voltage (V_{DS}) for different levels of gate-to-source voltage (V_{GS}). These characteristics are important for determining the operating state of the MOSFET (cut-off, linear, or saturation) and its efficiency and power handling capabilities.

In the linear regime of the device operation, as V_{GS} exceeds V_{th} , the conductive channel forms, and at low V_{DS} , the MOSFET behaves like a resistor. The current flowing from the source to drain (I_D) is directly proportional to V_{DS} and can be given by the following equation,

$$I_D = \mu_{eff} C_{ins} \frac{W}{L} (V_{GS} - V_{th}) V_{DS}$$

where μ_{eff} is the effective carrier mobility in the inversion layer, W is the channel width, L is the channel length. The above equation applies when the V_{DS} is small. For the case of large V_{DS} , the equation is,

$$I_D = \mu_{eff} C_{ins} \frac{W}{L} \left((V_{GS} - V_{th}) V_{DS} - \frac{V_{DS}^2}{2} \right)$$

The saturation regime of the device must be studied differently for the case of a long-channel device and a short-channel device. For the case of a long-channel device, when V_{DS} exceeds V_{GS} , the potential difference between the gate and the substrate is different across the length of the channel. The potential difference is reduced near the drain side of the channel leading the channel to be “pinched-off” as explained earlier with the water reservoir analogy. At that bias, $V_{DS} > V_{DS,sat} \approx V_{GS} - V_{th}$, the device behaves as a square law device with the saturation current given by,

$$I_{D,sat} = \mu_{eff} C_{ins} \frac{W}{2L} (V_{GS} - V_{th})^2$$

For the case of a short-channel device, one can assume that the drift velocity of carriers (v_d) saturates above a certain critical electrical field (ϵ_c) where saturation velocity ($v_{d,sat}$) can be given as,

$$v_{d,sat} = \mu_{eff} \epsilon_c$$

The following formula helps determine if the channel is long, given,

$$L \gg \frac{\mu_{eff} V_{DS}}{v_{d,sat}}$$

Hence, the saturation current for a short-channel MOSFET can be given as,

$$I_{D,sat} = WC_{ins} v_{d,sat} (V_{GS} - V_{th})$$

It is important to mention that transport in low-dimensional materials is more complicated than hence the above equations derived from conventional Si MOSFETs don't fully apply. Velocity overshooting is a phenomenon experienced by carriers that are injected in low-dimensional channels although possess high mobility but also experience high fields at the beginning of the channel leading them to scatter in the channel.

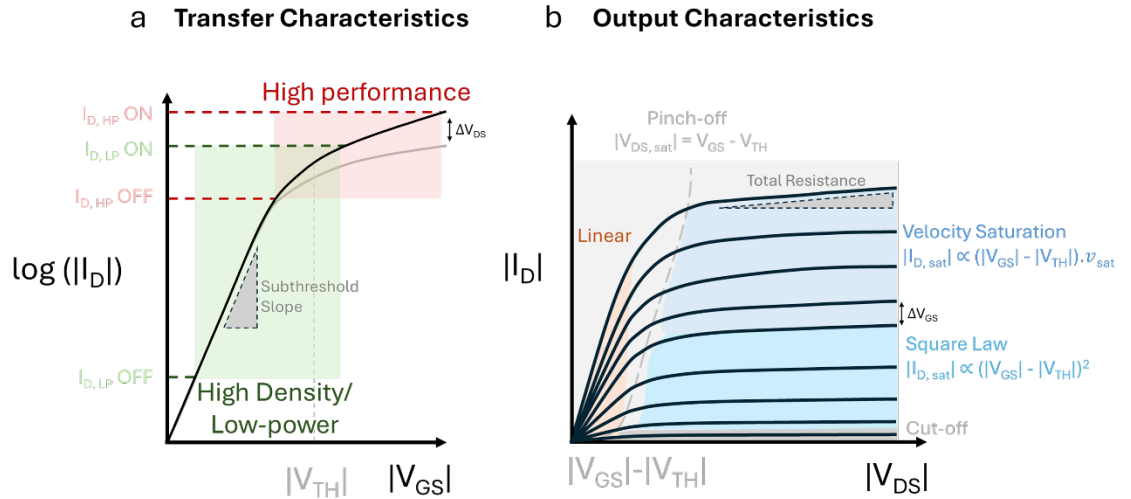


Figure 1-10: Basic Electrical Characterization of MOSFET: a) Transfer Characteristics of the MOSFET in the logarithmic scale where the current is measured on the drain (I_D) terminal while sweeping the voltage across the gate and source (V_{GS}) terminals while applying a constant voltage across the drain terminal and source (V_{DS}) terminals. Device performance metrics are labelled for

high-performance and high-density/low-power device operation. b) Output characteristics of the MOSFET plotted in the linear scale where the measured I_D is plotted with respect to varying V_{DS} for discretely varying V_{GS} . Different regions of operation are shaded for better understanding.

Below V_{th} , the MOSFET does not entirely turn OFF. In subthreshold regime, a small value of current flows in the channel due to carrier diffusion, characterized by an exponential dependence on $V_{GS} - V_{th}$. The subthreshold leakage current is a key concern for modern electronics as it determines the static power consumption of any IC. The presence of a large barrier to current flow unable to restrict thermal diffusion of carriers across and the presence of a finite diffused charge even under the application of a small electric field is the reason behind the subthreshold current. Current equation can now be given as,

$$I_D = \mu_{eff} C_{ins} \frac{W}{L} (m - 1) \left(\frac{kT}{q} \right)^2 e^{q(V_{GS} - V_{th})/mkT}$$

Here, m is given as the body factor. It equals,

$$m = 1 + \frac{C_s}{C_{ins}}$$

for which, C_s is the semiconductor capacitance and C_{ins} is the insulator capacitance. The subthreshold regime of operation is characterized by the exponential switching in the device given by the subthreshold slope, SS, which is the number of millivolts of change in V_{GS} for a decade order of change in I_D . The theoretical limit of SS is 60 mV/decade. SS can thus be related to m with the following equation,

$$SS = m \frac{kT}{q} \ln 10 = 2.3m \frac{kT}{q} \text{ (V/dec)}$$

Hence, $m > 1$ and we hit the theoretical switching limit of 60 mV/dec. Practically, other non-ideal parasitic capacitance primarily from interface traps (C_{IT}) can haunt also the device switching and hence, the updated equation for the body factor, m , can be as follows,

$$m = 1 + \frac{C_s}{C_{ins}} + \frac{C_{IT}}{C_{ins}}$$

Equations to relate the OFF ($I_{D,OFF}$) and ON ($I_{D,ON}$) currents to the threshold voltage, V_{th} , are important to be discussed and are therefore given below.

$$I_{D,OFF} = I_D(V_{GS} = 0; V_{DS} = V_{DD}) \propto e^{-qV_{th}/mkT}$$

$$I_{D,ON} = I_D(V_{GS} = V_{DS} = V_{DD}) \propto (V_{DD} - V_{th})^\alpha, 1 < \alpha < 2$$

From this, it looks like by varying just V_{th} , one can achieve high ON current and exponentially low OFF current. However, V_{th} is a key parameter that requires engineering. Threshold voltage, V_{th} , is given by the following equation,

$$V_G = \phi_m - \phi_s + \psi_s - \frac{Q_S(\psi_s)}{C_{ins}} - \frac{Q_{IT}(\psi_s)}{C_{ins}} - \frac{Q_F}{C_{ins}} - \frac{\chi_m}{t_{ins}} \frac{Q_m}{C_{ins}}$$

where, ϕ_m and ϕ_s are the work function of the gate metal and semiconductor, ψ_s is the surface potential of the semiconductor, Q_S is the charge at the semiconductor surface, Q_{IT} is the interface trap charge as a function of the surface potential, Q_F is the concentration of fixed charge in the insulator, Q_m is the concentration of mobile charge in the stack, with the charge centroid given by χ_m , thickness of the insulator given by t_{ins} , and insulator capacitance given by $C_{ins} = \epsilon_{ins}\epsilon_{vacuum}/t_{ins}$. When the device is biased in threshold, i.e., at $V_{GS} = V_{th}$, surface semiconductor potential, ψ_s equals twice the bulk semiconductor potential, ψ_B , such that $\psi_s = 2\psi_B$. Thus, this helps understand the several intricacies in engineering the V_{th} of the MOSFET. After having covered the basics of the device operation, we set the criteria for an ideal MOSFET to be a device that exhibits high ON current, low leakage OFF current, ideal (60 mV/dec) and rapid switching behavior.

Objectives and Dissertation Organization

This thesis entitles transistor stack engineering and device development for high-performance computing as well as low-power logic using two-dimensional (2D) channel

materials, specifically transition metal dichalcogenides (TMDs), as novel semiconductor materials with the potential to replace conventional semiconducting channels due to their superior electronic and optical properties at scaled dimensions. The thesis also covers device improvement using another low-dimensional channel material, namely, carbon nanotubes (1D), introduced earlier as promising channel candidates for logic advancement.

Chapter 2 details the current state of logic and computation. Advanced logic and computing techniques that have been proposed are introduced and the memory-logic data transfer bottleneck is explained, where the memory and logic are physically separated. Following the introduction to traditional von Neumann computing, the contradictory scheme of non-von Neumann computing is explained where memory and logic are combined on the same device platform, enhanced with optical sensing and hardware security capabilities. The chapter then transitions to discuss the key driving forces and requirements for advanced logic and computing in the next decade. With the impending end of Moore's Law and the slowing of transistor scaling, new materials and device architectures are needed to continue the relentless pursuit of increased performance and energy efficiency.

The core requirements for advanced logic transistors, including the need for both high-performance n-type and p-type field-effect transistors (FETs) to enable complementary metal-oxide-semiconductor (CMOS) logic, are highlighted. While significant progress has been made in demonstrating n-type FETs using materials like molybdenum disulfide (MoS_2), the development of high-performance p-type 2D FETs remains a significant challenge. The chapter then hints towards the key performance goals from IRDS, highlights the area of improvement, and motivates for the development in p-type 2D FETs.

Chapter 3 focuses on engineering p-type electrical contacts to 2D channel materials, a crucial aspect for realizing high-performance p-type transistors. Various techniques are explored, including work-function engineering, where the metal work function is tuned to pin closer to the

semiconductor's valence band edge for efficient hole injection; metallization-induced strain analysis, which involves specialized transmission electron microscopy (TEM) analysis to study strain induced onto the semiconductor; and contact interface optimization, where the metal-semiconductor interface is optimized by incorporating a high work-function, low-damage Selenium for even more efficient hole injection.

In Chapter 4, the emphasis shifts to engineering the threshold voltage of p-type 2D channels. Strategies such as electrostatic modulation through gating, where external electric fields are applied to modulate the channel's carrier concentration; gate dielectric engineering, which involves optimizing the dielectric material and thickness to improve electrostatic control; and charge transfer doping, where dopants are introduced to modulate the channel's carrier concentration, are discussed to overcome the challenges associated with achieving desired threshold voltages in 2D material-based transistors.

Chapter 5 presents layer engineering techniques to improve p-type transport. Layer-controlled growth and dependence on transport is assessed, followed by stacking of 2D layers to form the channel and look for transport improvement, layer modification by plasma treatment and annealing for surface functionalization is discussed, highlighting the potential for high-performance enhancement through bilayer growth, monolayer dopant introduction by stacking, and surface treatment. Therefore, the need to study the surface and interface in more detail is underscored.

Chapter 6 delves into interface characterization in FETs on 1D channel materials. The analysis of interface defects using 1D FETs as a testbed, where techniques like bias and frequency dependent impedance characterization help estimate defect concentration as well as their energetical position along the bandgap of the channel. This highlights the challenges involved with low-dimensional channel materials in interface trap state identification and suggests a methodology to estimate defects farther and closer to band edges.

Finally, Chapter 7 presents the conclusion and future work. A summary of the key findings and contributions of the research is provided, along with suggestions for future research directions. Specific steps toward realizing an ideal p-type 2D FET are outlined, including the use of buffer layers to improve the semiconductor-dielectric and semiconductor-contact interface, strained, wrap-around contacts to achieve efficient charge injection, extension doping to modulate and lower injection resistances into the channel, and optimal dielectric interfaces and dielectric quality to minimize defects and improve electrostatic control.

Chapter 2

Advanced Logic and Computing

*Part of this chapter has been reproduced from: **Secure Electronics Enabled by Atomically Thin and Photosensitive Two-Dimensional Memtransistors.** Aaryan Oberoi, Akhil Dodda, He Liu, Mauricio Terrones, and Saptarshi Das, *ACS Nano* **2021** 15 (12), 19815-19827, DOI: 10.1021/acsnano.1c07292*

The semiconductor industry has been the driving force behind the rapid technological advancements witnessed over the past few decades. Guided by industry standards and technology roadmaps, such as those outlined by the International Roadmap for Devices and Systems (IRDS), the relentless pursuit of performance and energy efficiency has fueled the continuous scaling of transistor dimensions.⁶⁸ This scaling has been governed by Moore's Law, which predicted a doubling of transistor density approximately every two years.²¹

Through the years, the industry has successfully transitioned from micron-scale transistor nodes to deep sub-micron nodes, with the latest commercial technologies reaching the 5 nm node and beyond. This incredible scaling has been accompanied by significant innovations in transistor architecture, materials, and fabrication processes. The conventional planar metal-oxide-semiconductor field-effect transistor (MOSFET) has evolved into three-dimensional structures, such as FinFETs and gate-all-around (GAA) architectures, to improve electrostatic control and mitigate short-channel effects.⁶⁹

Despite these advancements, the industry is rapidly approaching the fundamental limits of transistor scaling, and the era of Moore's Law is nearing its end. As a result, there is a pressing need for disruptive innovations in materials, device architectures, and computing paradigms to sustain the historic pace of performance and energy efficiency improvements.

Traditional computing architectures have been based on the von Neumann model, the central processing unit (CPU) performs logical operations on data retrieved from memory, with the two components connected via a data bus. While this approach has been the backbone of modern computing, it suffers from an inherent bottleneck known as the "memory wall". The physical separation of logic and memory, coupled with the ever-increasing data transfer requirements, has led to a significant performance and energy efficiency penalty, limiting the overall system performance. This chapter introduces an unconventional computing technique that integrates memory and logic together. Following that, to meet the immediate needs of the logic industry, FETs based on low-dimensional materials are proposed and a quick overview on current state of logic with low-dimensional materials is discussed.

von Neumann Computing

The von Neumann architecture, proposed by John von Neumann in 1945, is based on the fundamental principle of separating logic and memory into distinct physical units.²² This separation has been the backbone of modern computing systems, enabling the development of complex and powerful processors capable of executing a wide range of operations.

Logic and Memory

In the von Neumann model, the memory unit, typically implemented using random access memory (RAM) or other storage technologies, holds both the program instructions and the data being processed. The CPU and memory are connected through a data bus, facilitating the transfer of instructions and data between the two units. This architecture has several advantages, including the ability to execute a wide range of algorithms by simply modifying the program

instructions stored in memory. However, the "von Neumann bottleneck" or the "memory wall" is a major downside as processing power demand is increasing. As processors become faster and more powerful, the data transfer rates between the CPU and memory become increasingly limited, leading to a significant performance penalty.

Understanding Digital Logic

A CMOS inverter is a fundamental building block in digital electronics, consisting of a PMOS and an NMOS transistor configured in a push-pull manner. The CMOS inverter operates with complementary states where when one transistor is "ON," the other is "OFF," allowing for effective digital switching with very low power dissipation. The schematic of a CMOS inverter is given in Figure 2-1a. In a CMOS push-pull configuration, the source of the pull-up PMOS is connected to the supply voltage (V_{DD}) whereas its drain is connected to the output. Similarly, the pull-down NMOS has its drain connected to the output while its source is grounded. The gates of both the transistors are shorted and the input is fed through them. To better understand the operation of a CMOS inverter, the output characteristics of both the transistors is overlaid on top of each other, as shown in Figure 2-1b. The voltage transfer characteristics (VTC) of a CMOS inverter, schematically represented in Figure 2-1c, describe how the output voltage varies with input voltage. When V_{input} is low, the NMOS is linear while the PMOS is in saturation. This allows the current to pass through the PMOS transistor which is ON and hence V_{output} is equal to the supply voltage, V_{DD} . This condition is labelled as point 'A'. Now, when V_{input} further increases, both devices are above threshold and in saturation mode, labelled as point 'B'. Hence, a slight change increase in V_{input} can result in the PMOS transistor to be OFF further resulting in V_{output} to be grounded since the NMOS transistor is now ON. This slight increase in V_{input} can

result in a very large switching in V_{output} with a very high gain, labelled as point 'C'. Further increase in V_{input} leads to PMOS reaching the linear regime of operation and pulling down the output to ground through NMOS, labelled by point 'D'. The critical part of the VTC curve where V_{input} is around $V_{DD}/2$. Both NMOS and PMOS are partially conducting, which results in a rapid transition in V_{output} from high to low. This point is also where the gain of the inverter is highest, and it's sensitive to variations in the threshold voltages of the transistors. Ideally, the switching threshold V_M of the CMOS inverter, where $V_{input} = V_{output}$, is around $V_{DD}/2$.

The logic unit, or the CPU, is responsible for executing a series of fundamental logical operations, such as AND, OR, NOT, and XOR, on binary data. These operations form the basis of digital logic circuits, which are the building blocks of modern processors. By combining these basic operations in intricate ways, complex algorithms and computations can be performed. Digital logic circuits are designed using Boolean algebra, which provides a mathematical framework for describing and manipulating binary values. These circuits are typically implemented using electronic components such as transistors, which act as switches to control the flow of electric current based on the input logic values.

The fundamental logic gates, such as AND, OR, and NOT gates, are the basic building blocks of digital logic circuits. The AND gate performs a logical conjunction, outputting a logic '1' only when all input values are '1'. The OR gate performs a logical disjunction, outputting a logic '1' if any of the input values is '1'. The NOT gate, also known as an inverter, simply inverts the input logic value. More complex logic functions can be realized by combining these basic gates in various configurations. For example, the XOR (exclusive OR) gate, which outputs a '1' when the input values are different, can be constructed using a combination of AND, OR, and NOT gates. Similarly, advanced arithmetic and logical operations, such as addition, multiplication, and logical shifts, can be implemented using intricate arrangements of these

fundamental gates. Digital logic circuits are designed to be highly reliable and operate with well-defined truth tables, ensuring predictable and deterministic behavior. This reliability is crucial for the proper execution of algorithms and computations in modern computing systems.

The fundamental logic gates are typically implemented using complementary metal-oxide-semiconductor (CMOS) technology, which utilizes both n-type and p-type metal-oxide-semiconductor field-effect transistors (MOSFETs). CMOS logic circuits offer several advantages over other logic families, making them the predominant choice for modern digital logic design. The use of complementary n-type and p-type MOSFETs allows for efficient implementation of logic gates with low static power consumption. When one type of transistor is on and conducting, the other type is off, minimizing the flow of direct current and reducing power dissipation. CMOS technology also provides high noise immunity, thanks to the well-defined logic levels and the ability to drive relatively large capacitive loads. Additionally, CMOS circuits are highly scalable, allowing for continued miniaturization and performance improvements as transistor dimensions shrink with each new technology node.

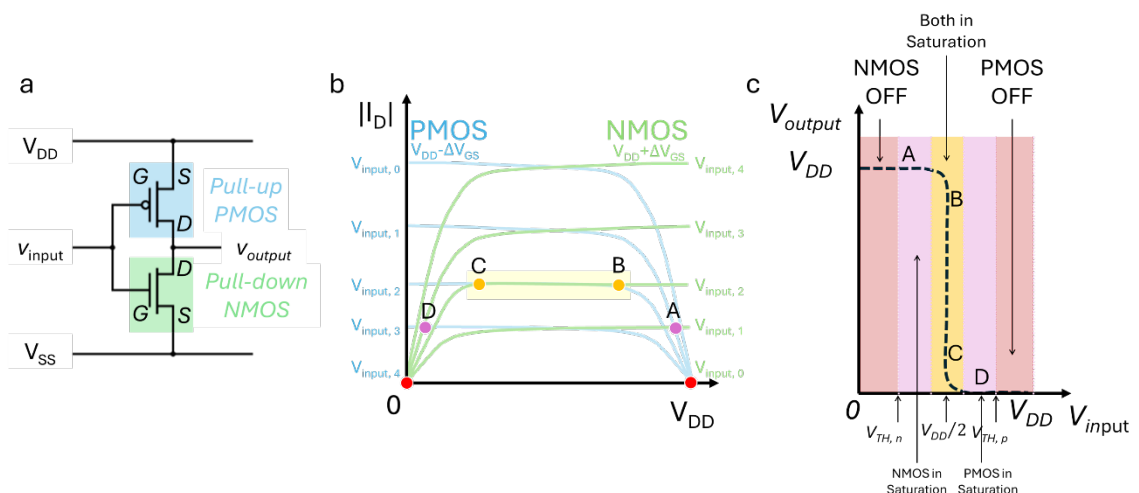


Figure 2-1: Complementary Metal Oxide Semiconductor (CMOS) Fundamentals: a) Circuit schematic of the CMOS Inverter where the source of the p-type MOSFET (PMOS) is connected to the supply voltage (V_{DD}) as the pull-up unit whereas source of the n-type MOSFET (NMOS) is connected to the ground (V_{SS}) as the pull-down unit. b) PMOS and NMOS output characteristics superimposed on top of each other to identify the steady state operations of the CMOS inverter.

The input voltages are labelled alongside each curve and the intercepts A, B, C, D correspond to the c) voltage transfer characteristics (VTC) where V_{output} is plotted against V_{input} color coded to identify the switching intercept points.

The complementary nature of CMOS logic gates is essential for realizing complex digital circuits. For example, the CMOS implementation of the inverter, a fundamental building block, comprises a p-type MOSFET and an n-type MOSFET connected in series. When the input is logic '1', the n-type transistor is on, and the p-type transistor is off, pulling the output to ground (logic '0'). Conversely, when the input is logic '0', the n-type transistor is off, and the p-type transistor is on, connecting the output to the supply voltage (logic '1'). By combining these complementary CMOS logic gates in intricate ways, designers can construct complex digital circuits, such as arithmetic logic units (ALUs), control units, and memory elements, enabling the realization of modern microprocessors and other digital systems.

Understanding Digital Memory

The memory unit, on the other hand, is responsible for storing both the program instructions and the data being processed. Traditional memory technologies, such as dynamic random-access memory (DRAM) and static random-access memory (SRAM), are based on the storage and retrieval of binary data. One of the most widely used non-volatile memory technologies is the floating-gate memory cell, schematic shown in Figure 2-2a. A floating-gate memory cell forms the basis of NAND and NOR flash memories. In a floating-gate memory cell, the storage element consists of a floating gate electrode, typically made of polysilicon, surrounded by an insulating oxide layer. The presence or absence of electrons stored on this floating gate determines the logic state ('1' or '0') of the cell. The floating gate is electrically isolated, and electrons are injected onto or removed from it through various mechanisms, such as hot carrier injection or Fowler-Nordheim tunneling. The stored charge in the floating gate

modulates the threshold voltage (V_{TH}) of the associated MOSFET, enabling the read operation to determine the logic state by sensing the current flow. The carriers responsible for electrostatic screening can tunnel either from the channel or can be injected from the control gate itself. The operating mechanism is demonstrated in Figure 2-2b and Figure 2-2c, respectively. The read state of the device is determined by the carrier type in the floating gate. Furthermore, the floating gate metal can be replaced by an amorphous oxide to utilize the trap states in the defective oxide for electrostatic screening.

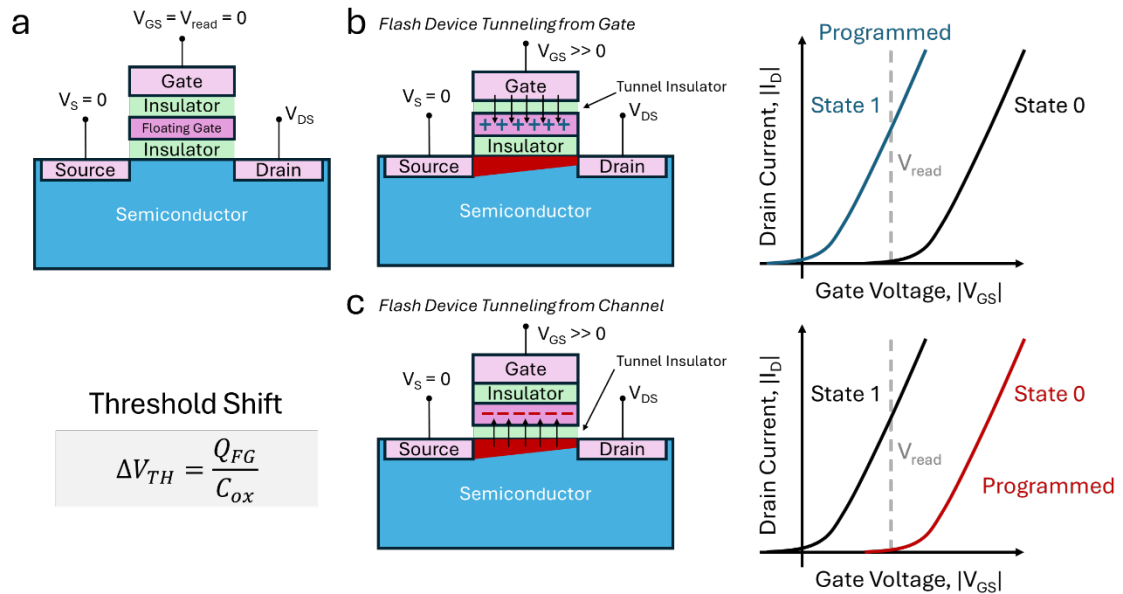


Figure 2-2: Floating Gate Flash Memory Device: a) Device schematic of a typical flash memory device in the read state with a floating gate metal sandwiched between the tunneling insulator and gate insulator. Charge injected into the floating gate causes electrostatic screening thereby resulting in threshold voltage shifts, given by the formula for ΔV_{TH} . b) Flash memory device with tunneling insulator layer present next to the control gate metal, allowing for charge to be injected from the control gate. Carrier type injected determines the threshold shift direction and allows the device to switch between two binary memory states for the ‘write’ process. For a given V_{read} , the device is programmed to a state ‘1’ when the threshold is ‘low’ and state ‘0’ when the threshold is ‘high’. Corresponding threshold shift is depicted alongside. c) Flash memory device with tunneling insulator layer present right above the channel allowing charge to be injected from the channel, resulting in the device to be programmed. Corresponding transfer characteristics after programming are given alongside.

NAND flash memory, widely used in solid-state drives (SSDs) and other storage devices, arranges the floating-gate cells in a dense array, with multiple cells connected in series, allowing for high storage density and cost-effectiveness.^{70,71} NOR flash memory, on the other hand, connects the cells in parallel, sacrificing density for faster random-access times, making it suitable for code storage applications. Another type of non-volatile memory technology is the charge-trap memory, which stores charge in discrete traps within a dielectric layer, rather than a continuous floating gate.⁷² This architecture offers advantages in terms of scalability, reliability, and lower operating voltages compared to traditional floating-gate cells. In addition to non-volatile memories, volatile memory technologies like DRAM and SRAM are widely used for main memory and cache memory in computing systems. DRAM stores data as charge on a capacitor, while SRAM uses bistable latching circuits to store each bit of data.

These memory technologies have undergone significant advancements in terms of density, speed, and energy efficiency, enabling the development of increasingly powerful computing systems. However, the industry is actively exploring emerging non-volatile memory technologies, such as resistive random-access memory (RRAM), phase-change memory (PCM), and magnetoresistive random access memory (MRAM), to overcome the scaling limitations of traditional memory architectures.⁷³

Non-von Neumann Computing

With several billion smart devices predicted to be connected to the internet this year alone, the boom on the Internet of Things (IoT) ecosystem has been the greatest success story known.⁷⁴ Increasing use cases for easy-to-use sensors along with its amalgamation with artificial intelligent (AI) systems, has extensively enabled remote, real-time insights, thus providing real-time and autonomous, decision-making capabilities. Following this, colossal amounts of data

were being generated from mostly unsecure devices which required high power and large communication bandwidth for data acquisition and communication with cloud for processing purposes. Further, the financial costs and energy expenditure required to operate these cloud servers was only rising. To tackle these challenges, edge computing harnessed the “in-device computing” capability for better and real-time predictive analysis, by moving the IoT devices to the edge thus reducing bandwidth, latency, energy expenditure, and operating costs.⁷⁵ However, state-of-the-art edge devices are still bound by the von Neumann bottleneck that physically separates the memory and computing units. With conventional computing algorithms still being implemented, edge computing simply relocates the burden of energy, storage, and computing inefficiency from cloud to edge devices. This requires a bottom-up reformation in the individual nodes of the edge computing architecture, which can therefore be achieved through material discovery, device innovation, and non-von Neumann computing alternatives. Figure 2-3 compares the two computing schemes side-by-side. Additionally, these data collection and computation nodes are required to be highly secure which is possible by embedding additional security protocols into the hardware components. Inspirations can also be drawn from the highly parallel, distributed, energy efficient, and adaptive, biological immune system, to conceive efficient and low-power in-sensor and near-sensor computing alternatives. Thus, an area and energy-efficient platform utilizing the capabilities offered by 2D materials, for sensing, security, storage, and computing for next generation of edge devices is proposed.

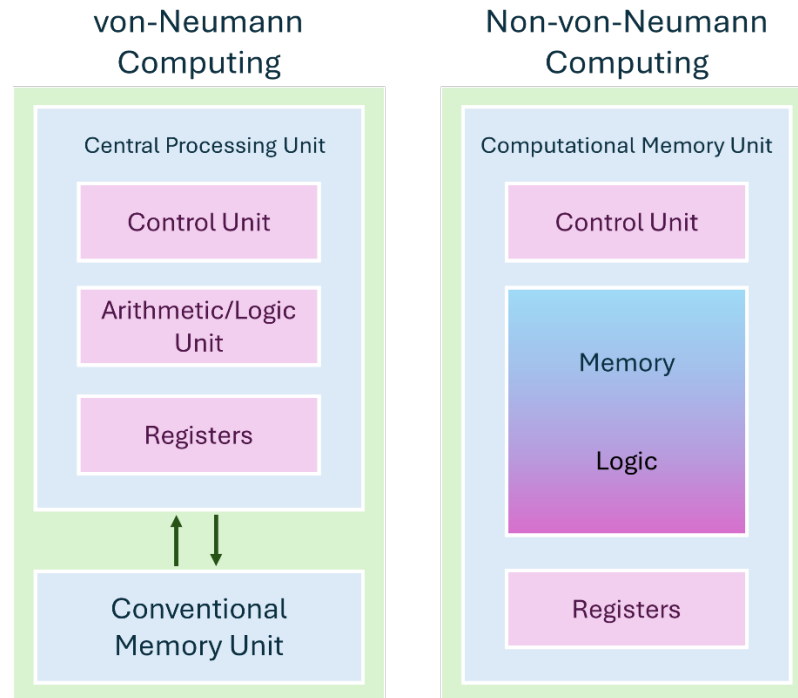


Figure 2-3: Contrasting Computing Architectures: a) von-Neumann architecture is depicted, highlighting its characteristic separation of the Central Processing Unit, from the Conventional Memory Unit, illustrating the data transfer bottleneck between them. b) Non-von-Neumann architecture integrates computational memory with the Control Unit, Memory, and Logic in a unified Computational Memory Unit, indicating the removal of the bottleneck and enabling parallel data processing and storage.

Combined Memory, Sensing, Security, and Logic

The limitations of the von Neumann architecture have led researchers to explore alternative computing paradigms that can overcome the memory bottleneck by combining logic, memory, and sometimes sensing and security functions within the same device platform.²³ One promising approach is the development of multi-functional electronic blocks that can perform these diverse operations within a single integrated unit.⁷⁶ A prime example of such a multi-functional device is a charge trapping transistor based on two-dimensional (2D) channel materials with photo-responsive properties.^{77,78} In this architecture, the 2D channel material, such as a

transition metal dichalcogenide (TMD) or a thin film of carbon nanotubes, acts as both the transistor channel and a photosensor, enabling light detection and conversion in addition to traditional transistor operations.

The charge trapping capability of the gate dielectric stack in these transistors allows for non-volatile storage of information, effectively integrating memory functionality within the same device.²⁵ By modulating the trapped charge distribution, the transistor's threshold voltage can be altered, enabling the implementation of multi-level analog memory states to further enable neuromorphic computing primitives. This allows for integration of memory on top of logic.⁶⁷

Furthermore, the inherent optoelectronic properties of the 2D channel materials can be leveraged for sensing and imaging applications, enabling the integration of sensing capabilities within the same device platform.⁷⁹ This multi-functional integration has the potential to significantly reduce the complexity and footprint of traditional imaging and sensing systems, which typically require separate photodetectors and readout electronics.

Additionally, the unique or non-ideal material properties and device characteristics of 2D transistors can be exploited for hardware security applications, such as physical unclonable functions (PUFs) and true random number generators (TRNGs).^{80,81} The stochastic nature of charge trapping and de-trapping events, combined with the inherent material variations and defects in 2D materials, can provide a rich source of entropy for generating unpredictable and unclonable security keys.

By integrating logic, memory, sensing, and security functions within a single multi-functional device, this approach has the potential to overcome the von Neumann bottleneck, reduce system complexity, and enable new applications that leverage the unique properties of 2D materials and emerging device architectures. In the following sections, the integrated memory and sensing functionality of 2D materials will be utilized combining it with the logic operation on a 2D FET.

2D Analog Memtransistor

A "memtransistor" refers to a type of electronic device that combines the properties of a transistor with memory functionality. This term is often associated with devices that leverage memristive properties (memory + resistor) within a transistor-like structure, allowing the device not only to switch and amplify signals like a traditional transistor but also to retain state information, effectively acting as a form of non-volatile memory. Memtransistors can perform the dual roles of signal processing (like a transistor) and data storage (like a memory cell). This combination is highly beneficial for reducing the footprint of circuits on chips, leading to more compact and potentially more efficient integrated circuits. The charge storage phenomenon in a non-floating gate type device will be discussed to explain the operating principle of the 2D memtransistor utilized.

Charge Trapping in a 2D FET

Another interesting approach to realizing memory capabilities is through the exploitation of charge trapping phenomena in FETs based on 2D materials like MoS₂, WS₂, etc. Due to the extremely thin nature of these materials, their properties are strongly affected by their interfacial environment. Moreover, the lack of an ideal dielectric to 2D materials like Silicon dioxide (SiO₂) is to Silicon, makes it all the more challenging to obtain an ideal transistor performance. However, these non-idealities can be leveraged, turning the unfavorable trap states at 2D-dielectric interface for logic into favorable charge storage centers enabling threshold voltage modification that is applicable for non-binary, analog state memory where the memory criteria requirements are far more relaxed and yet show remarkable superiority to traditional computing techniques for next-generation electronics. Researchers have explored various strategies to

optimize these criteria in 2D FET-based analog memory devices.⁸² For instance, the use of engineered dielectric stacks with tailored trap distributions can enhance the number of memory states and improve retention characteristics.⁸³ Additionally, innovative programming schemes, such as incremental pulse programming or quasi-non-volatile operation, can be employed to increase endurance and memory ratio.⁸⁴ By carefully designing and optimizing memory designing parameters, 2D FET-based memory devices can pave the way for highly efficient and robust neuromorphic computing systems, leveraging the unique properties of 2D materials and their interfaces.

In a typical 2D FET structure, the semiconducting channel is interfaced with a high-k dielectric material, such as hafnium oxide (HfO_2) or aluminum oxide (Al_2O_3), which serves as the gate insulator. At the 2D semiconductor-dielectric interface, as well as within the dielectric itself, there exist a distribution of charge trapping sites arising from various defects from inherent growth-induced defects or impurities to processing or fabrication induced device variations. Charge trapping mechanisms may be divided into two categories depending on the origin of the trapped charge, namely, a) channel carrier trapping, b) injected charge trapping. By applying appropriate programming voltages to the gate terminal, either carriers in the channel can be pulled into these trapping sites or charges from the gate can be injected into these trapping sites, modulating the electrostatic potential and the effective threshold voltage of the FET. Trapped charges result in screening of electric fields applied at the gate terminal and this leads to threshold voltage shifts. The charge trapping sites may be defects in the semiconducting channel, defects at the semiconductor-dielectric interface, shallow-level and deep-level trap states in the gate dielectric, or even a physically introduced metal floating gate or defective insulator stacked into the gate dielectric. Following this, the trapped charge distribution can be precisely controlled, enabling the storage of analog values based on the resulting threshold voltage shifts.

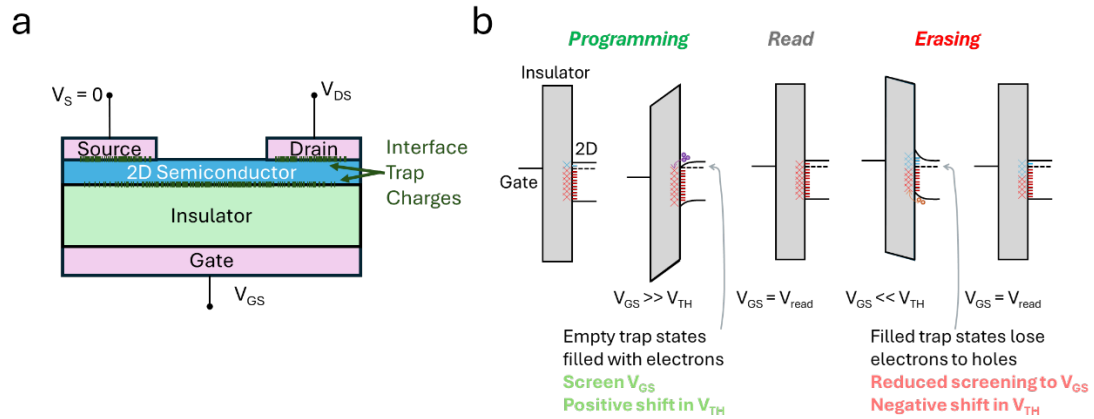


Figure 2-4: Charge Trapping in 2D FETs: a) Device schematic of a 2D contact-gated FET highlighting the presence of interface trap states at the interface of the 2D semiconducting film with the insulator as well as the contacts. b) Energy band diagrams along the MOS direction showing the population and depopulation of trap states accessible above the Fermi level that result in programing and erasing cycles in non-floating gate, purely trap-assisted memory devices.

Figure 2-4a shows a device schematic of a 2D FET with the 2D TMD film transferred onto a back-gate substrate with an insulating dielectric, often an amorphous oxide grown using atomic layer deposition (ALD). The source and drain contact metals are work-function engineered to tune the polarity of the transport in the 2D TMD film. Due to the ultra-thin nature of the TMD film, defects can be created at any point of the processing step. Defects from mechanical strain during film transfer, polymer residue from lithography and etching processes, and defects from metal evaporation can all lead to variations in electronic properties. Moreover, pre-existing defects in the insulator stack and inherent defects in the TMD film can lead to variations in properties that demand extensive characterization. These defects, although unfavorable, can instead be exploited and the generated properties can be utilized to mimic the stochastic behaviors of imperfections around us.

The resultant properties of a 2D TMD FET with an unoptimized interface and insulator stack can still provide charge trapping capabilities. Since the charge trapping centers are non-uniform and can sometimes be localized to certain areas in the channel or contacts, their charge-holding capabilities can be variable and dependent on many parameters. Yet, from a functional

memory device standpoint, the variability in threshold voltage of the device occurring from the screening of the channel electrostatic potential due to an unaccountable and unlocatable number of trapped charges in the can result in a non-binary number of memory states. These responsible traps may be located anywhere close to the interface or even slightly deep into the insulator itself. The programming and erasing of memory states by charge storage in these traps can be explained with the help of energy band diagrams along the gate electrostatic direction as shown in Figure 2-4b. For the sake of understanding, we will consider an n-type MoS₂ semiconducting channel on an amorphous aluminum oxide (Al₂O₃) insulator. On the application of a large positive voltage to the back gate metal, we pull the bands down and the Fermi level of MoS₂ is close to the conduction band edge. Traps in the interface of the semiconductor and Al₂O₃ energetically located above the Fermi level that were empty are suddenly filled with electrons from the channel. Now these electron capture sites screen potential across the insulator and cause an increase in the threshold voltage. Similarly, when a large negative voltage is applied, the trapped carriers are now lost to the channel causing the threshold to shift leftwards.

This analog storage capability can be leveraged for implementing synaptic weight updates in artificial neural networks, where the synaptic weights are encoded as the stored charge levels until they have to be updated again for training.⁸⁵⁻⁸⁷ The non-volatile or near non-volatile nature of the trapped charges allows for persistent storage, while the ability to incrementally modify the charge distribution through the application of programming pulses enables efficient weight update mechanisms akin to biological synaptic plasticity.^{24,88} Hence, the charge trapping phenomena at the 2D semiconductor-dielectric interface can be exploited for realizing multi-level memory cells, where multiple distinct charge states can be programmed and read, increasing the storage density compared to traditional binary memory cells.

Analog Memory Criteria

For analog memory based on charge trapping phenomena in 2D FETs to be viable, several key criteria must be met. These criteria help benchmark the memory performance in order to compare with other similar charge trapping memory devices. FETs with monolayer MoS₂ as the channel material are fabricated on a 50 nm Al₂O₃ insulator with Pt/TiN/p++-Si back gate metal. Monolayer MoS₂ is synthetically grown using metal organic chemical vapor deposition (MOCVD) technique and transferred onto the back-gate substrate. The device schematic is given in Figure 2-5a. Transfer characteristic sweeps are measured after the application of a back-gate ($V_{GS} = V_{write}$) programming pulse of varying amplitude from 5 V to 21 V with a pulse duration of 100 ms. With the application of every programming voltage, the device characteristics shift until a point where any higher programming voltage to the back-gate seems detrimental to the device itself. The post-programming device characteristics are shown in Figure 2-5b. Similarly, an erase pulse of opposite polarity can be applied to reverse the shift in transfer characteristics. The magnitude of charge injected/trapped may be estimated from the threshold shift equation in Figure 2-5. The threshold voltage (V_{TH}) may be further determined using the iso-current method, by measuring the gate voltage for which the device current is 10 nA. Note that the magnitude of programming and erase pulses are different, and this corresponds to the energy band alignment of the MOS stack as well as the energetic location of the traps. We now characterize the MoS₂ memtransistor's capabilities. Figure 2-6 represents the key criteria along with denoting the metrics of a MoS₂ memtransistor device exhibiting 4 memory states.

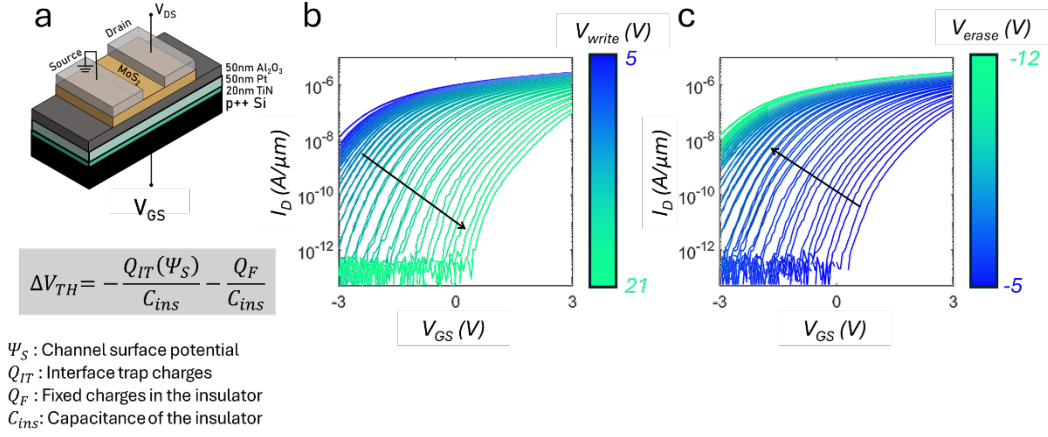


Figure 2-5: 2D Analog Memtransistor: a) Device schematic of a 2D FET with MoS₂ as the channel material, Ni/Au source/drain contact metal, fabricated on a 50 nm thin Al₂O₃ dielectric with Pt/TiN/p++-Si as the back gate metal. The equation for threshold voltage now includes the term that is responsible for the additional interface trap charge and fixed charge in the dielectric. b) Transfer characteristic sweeps of the 2D MoS₂ FET after the application of an increasing magnitude of programming/write voltage to the back gate, $V_{GS} = V_{write}$. Rightward shift in the threshold voltage (V_{TH}) is observed as the magnitude of the write voltage increases from 5 V to 21 V. c) Transfer characteristic sweeps of the 2D MoS₂ FET after the application of an erase voltage, $V_{GS} = V_{erase}$, opposite in polarity to V_{write} . In this case, a leftward shift in V_{TH} is observed owing to the release of electrons from the interface trap states.

The memory criteria can be classified as follows:

1. **Number of Memory States:** The ability to reliably store and distinguish between multiple analog charge levels is crucial for implementing multi-level memory cells and synaptic weight storage. The number of distinct memory states that can be programmed and read determines the precision and storage density of the memory cell. At a $V_{GS} = V_{read}$, four stable memory states can be identified and the measured current at $V_{read} = 0$ V can be used to categorize the different memory states.
2. **Memory Ratio:** The memory ratio, defined as the ratio of the maximum to minimum conductance (or threshold voltage) states, is a key figure of merit for analog memory cells. A larger memory ratio translates to a wider dynamic range and improved signal-to-noise ratio, enabling more reliable multi-level storage and computation. Depending on the application, the memory ratio may be desired. For the case of the MoS₂

memtransistor, a memory state is set apart from another state by one orders of magnitude of change in current. It is also important to note that the memory ratio criteria are dependent on the number of desirable memory states.

3. Retention: The trapped charge levels must exhibit long-term non-volatile retention, ensuring that the stored information is not lost over time. Charge retention is heavily influenced by the quality of the dielectric stack, the trap energy levels, and the operating conditions. The longevity of a given state in the MoS₂ memtransistor was tested for about 50 s and memory stability is established based for the 4 distinguishable states. This retention in charge trapping based memory devices is dependent on the trap time constant and the physical and energetic location of the trap.
4. Endurance: The memory cell must withstand a large number of programming and erase cycles without significant degradation in performance. This endurance requirement is particularly important for applications like neuromorphic computing, where frequent weight updates are necessary during training and inference. For the case of MoS₂ memtransistor characterized above, the re-programmability is tested thrice over 4 distinct memory states.

Although more stringent characterization techniques are necessary, here, the 2D memtransistor's capability to store charge is briefly characterized. Later on, this capability will be utilized to store necessary information and its usefulness as a security-enabled transistor will be explored.

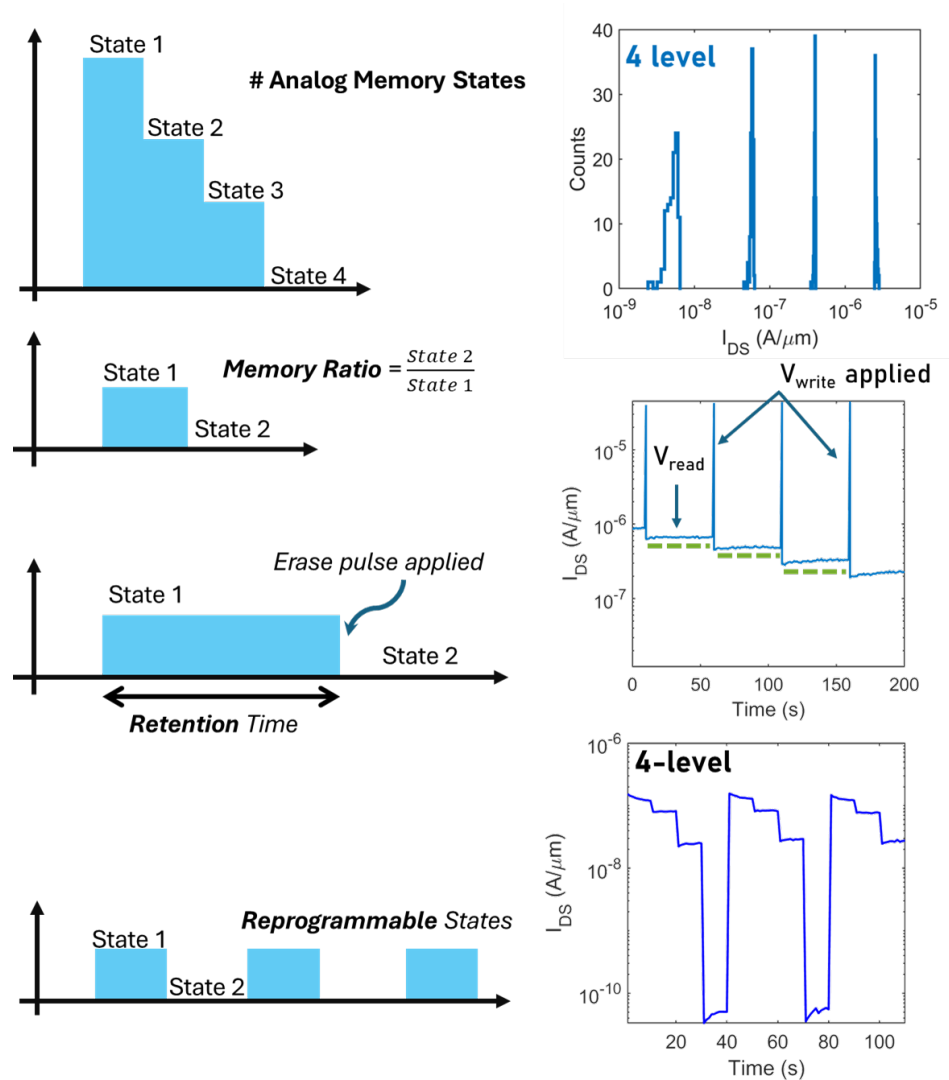


Figure 2-6: Analog Memory Criteria: For an analog memory cell to be viable and to further benchmark and compare with alternative memory solutions, the four criteria must be identified, namely, the number of analog memory states, the ratio or memory window between each state, the retention time for each state, and the re-programmability of the state over several read and write cycles.

2D Photoresponsive FET

Sensing is indispensable for the Internet of Things ecosystem that includes intelligent transport system, general manufacturing, medical imaging, machine vision, security and

surveillance, scientific discoveries, and many others. Traditional optical image sensors are power hungry, limiting their deployment in remote and resource constrained locations such as deep sea, deep space, and inaccessible geological locations. Research on reducing the power consumption and improving the active pixel area has been restricted to Silicon (Si) and with innovation in materials, alternative materials can be identified to either replace or accompany the current trends in low-power imaging applications. One of the widely known 2D semiconducting materials, MoS₂, has known to exhibit excellent electronic and optoelectronic properties^{77,89-91}. The indirect to direct bandgap transition from multilayer to monolayer MoS₂ confirmed by photoluminescence characterization shows great potential in optoelectronic applications for in-memory sensing and image acquisition⁹². Yin et al. first reported the photoresponsivity on exfoliated monolayer MoS₂ FET⁷⁸. Many studies have reported their understanding of the photogeneration mechanism in monolayer MoS₂⁹³⁻⁹⁵, however these studies utilize monochromatic light from laser for photoexcitation, thus ignoring the use case scenarios in real world applications where incident light is often diffusive. It is therefore important to study the response of MoS₂ phototransistor to diffusive light sources of three primary colors, red, green, and blue for practical application purposes. Lee et al. demonstrated the applicational capability of MoS₂ phototransistor beyond a simple unit photodetector for use as an imaging pixel⁹⁶. Their MoS₂ based imager was programmed to mechanically scan a 2D image placed in front of light projected from LED. In their demonstration, the scanning procedure and output image were produced in simulation using LabVIEW and the imaging pixel constituted of exfoliated MoS₂ FET. Several developments in the large area growth of high quality 2D materials have occurred in the recent past^{91,97,98} and the photodetection capabilities of FETs on these materials have been studied⁹⁹⁻¹⁰². However, any comparison with state-of-the art technologies, especially pertaining to the energy benefits of using these ultra-thin photodetectors, still lacks. Hence, it becomes important to experimentally characterize and benchmark the photoresponse of large area grown MoS₂ FET against state-of-

the-art Si-based PN photodiode (PD) and extrapolate this understanding to analyze the energy benefits of an image acquisition platform made up of MoS₂ phototransistors.

Photoresponse in Monolayer MoS₂

The indirect-direct bandgap transition in monolayer MoS₂ enables many applications in the field of photonics and optoelectronics. Initial studies on the optoelectronic capabilities of monolayer MoS₂ have been performed on exfoliated monolayers derived from single crystal flakes. Since exfoliation is not a viable approach for technological commercialization due to limitations in scalability, this study explores solutions with large-area growth of monolayer MoS₂. Synthesis of large area monolayer MoS₂ films is done using the scalable metal organic chemical vapor deposition (MOCVD) technique. High electrical performance is seen due to low carbon contamination and uniform crystallinity achieved as a result of high-temperature epitaxial growth using H₂S chalcogen precursor. Post-synthesis, PMMA assisted wet transfer process is employed to transfer monolayer MoS₂ from the sapphire substrate to the fabrication substrate, following which back-gated field effect transistors (FET) are fabricated. The back-gated FET stack comprised of atomic layer deposition (ALD) grown 50 nm Al₂O₃ on Pt/TiN/p⁺⁺-Si. Device schematic of the MoS₂ FET is shown in Figure 2-7a. The channel of the MoS₂ FET is 1 μm in length and 5 μm in width. More details about the growth process and device fabrication can be referred from our previous studies^{91,101,103}. Figure 2-7a shows the output characteristics i.e., source to drain current (I_{DS}) versus applied drain voltage (V_D) for different back gate voltages (V_{BG}) for the monolayer MoS₂ FET. The device ON current reaches about $\approx 20 \mu\text{A} / \mu\text{m}$ at $V_D = 5 \text{ V}$. Figure 2-7c and Figure 2-7d show the transfer characteristics in the logarithmic scale and linear scale, respectively, i.e., I_{DS} versus V_{BG} for a given V_D . The fabricated photodetector shows very high ON/OFF current ratio in the order of $\approx 10^7$, a subthreshold slope of 288 mV/dec.

The carrier mobility was extracted from the peak transconductance and was found to be $\approx 12 \text{ cm}^2/\text{Vs}$ as shown in the mobility characteristics, as shown in Figure 2-7e. A very low gate leakage current $\approx 1 \text{ pA} / \mu\text{m}$ is attributed to the high quality of the gate oxide and near-zero hysteresis window, shown in Figure 2-7f.

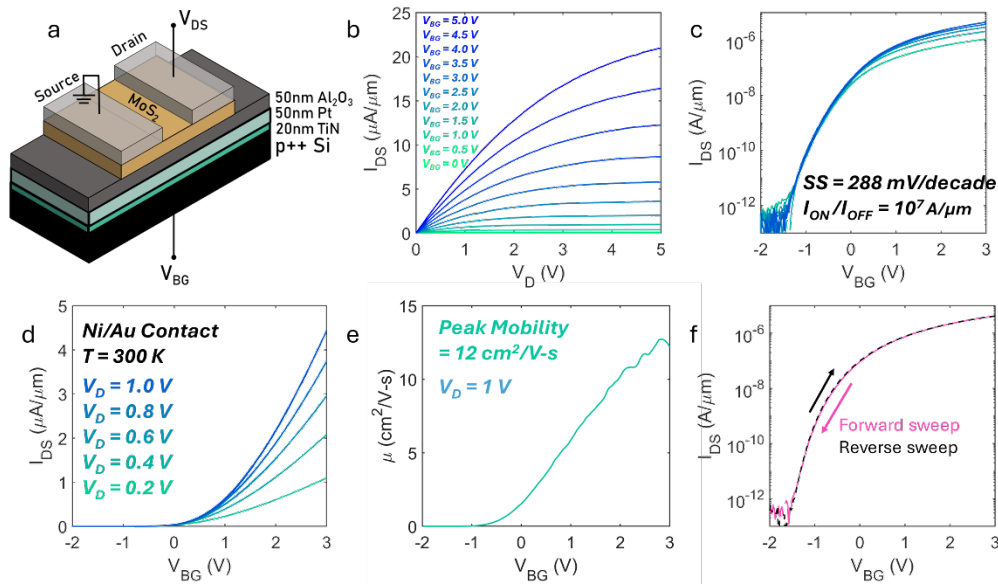


Figure 2-7: 2D MoS₂ FET Electrical Characterization: a) Device schematic of the back-gated MoS₂ memtransistor, b) Output characteristics of the long channel MoS₂ device with ON current reach up to 20 $\mu\text{A}/\mu\text{m}$ and the drain current showing the saturation regime, c) corresponding logarithmic scale transfer characteristics of the device and a subthreshold slope of 288 mV/dec, d) linear scale transfer characteristics of the device showing Schottky-limited performance, e) field effect electron mobility extracted using transconductance method and a peak mobility value of 12 $\text{cm}^2/\text{V-s}$, f) dual sweep transfer characteristics hinting to a clean interface with insulating 50 nm Al₂O₃.

As stated earlier, the traditional approach of assessing the photoresponse of a material makes use of lasers to tune the incident power and wavelength. To increase the application reliability of the MoS₂ FET for image acquisition in real life scenarios, it is important to characterize the material's photoresponse to diffused light which is supported with the use of light emitted diodes (LEDs) of varying colors. We measure the response of our MoS₂ phototransistor to varying LED intensities by choosing the V_{LED} corresponding to the subthreshold region of the LED characteristics. The diode characteristics are shown in Figure 2-8.

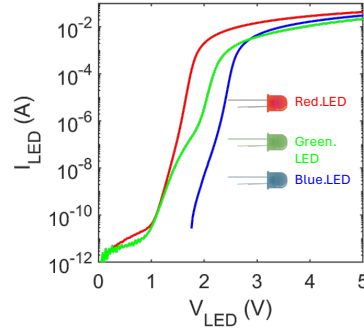


Figure 2-8: Light Emitting Diode (LED) Characteristics: Output characteristics of LEDs of varying colors used in the photodetector measurements.

Photocurrent (I_{PH}) is extracted by subtracting the output current $I_{DS,dark}$ under no illumination from the $I_{DS,light}$ measured under different illumination intensities (V_{LED}). Figure 2-9a, Figure 2-9b, and Figure 2-9c show the experimental photocurrent characteristics measured for red, green, and blue illumination respectively. As the illumination intensity increases with increasing V_{LED} , the photocurrent also increases. When light from red LED ($\lambda_{red} \approx 650 - 700 \text{ nm}$), green LED ($\lambda_{green} \approx 500 - 550 \text{ nm}$) and blue LED ($\lambda_{blue} \approx 450 - 500 \text{ nm}$) is incident on the MoS₂ phototransistor, electron-hole pairs are generated since the energy incident from the LED light source is greater than the bandgap of monolayer MoS₂ ($\approx 1.84 \text{ eV}$). Under the application of drain bias ($V_D = 1 \text{ V}$), the photoexcited carriers drift towards the respective metal electrodes. This results in an additional current generated due to the photoexcited carriers and adds to the dark current in the device. In the ON-state, very less change in photocurrent is noticed because the additionally generated photocurrent is obscured by the high dark current in that regime. The dark current can be significantly reduced by operating the device in the subthreshold and OFF state. However, in the OFF state, the interface trap states between Al₂O₃ and MoS₂ recombine with the photoexcited carriers causing a reduction in the photocurrent. The dangling Al-O bonds at the surface result in the trap states that follow a Fermi-Dirac distribution. This requires us to choose an optimum gate voltage range to enhance the photoresponse in the

MoS₂ FET. Photogating effect can be further explained with sweep rate dependent hysteresis measurement. Widening in the hysteresis window under LED illumination for increasing pulse width of $t_p = 10 \text{ ms}$ (Figure 2-9d), $t_p = 100 \text{ ms}$ (Figure 2-9e) and $t_p = 1000 \text{ ms}$ (Figure 2-9f), is direct evidence that photogating effect is playing a dominant role in the photocurrent generation in the MoS₂ phototransistor.

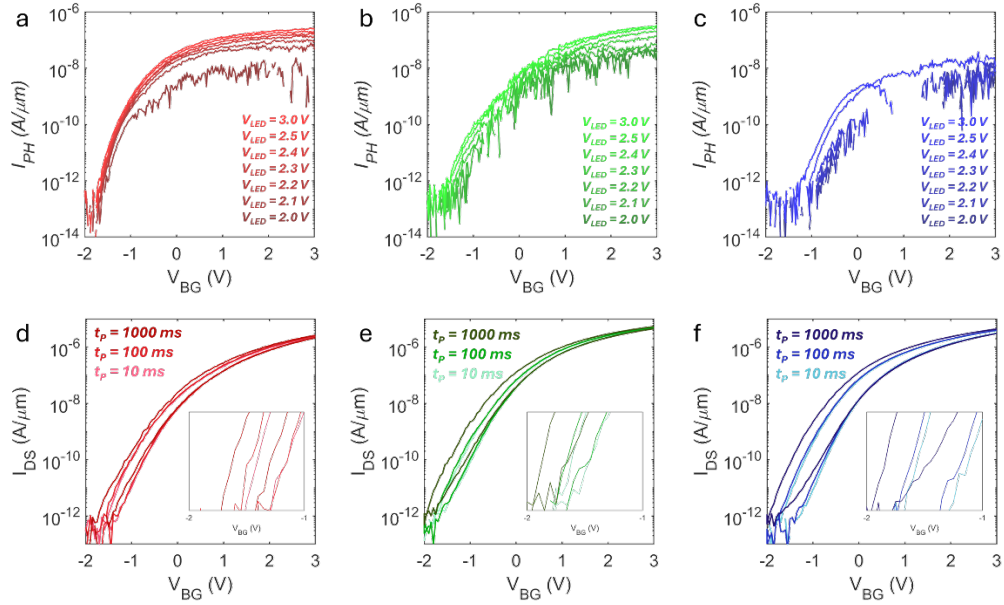


Figure 2-9: MoS₂ FET Photocurrent Characterization: Device photocurrent, I_{PH} , calculated as the difference in the device current, I_{DS} , with and without illumination with varying LED intensities varied as LED bias, V_{LED} for a) red, b) green, and c) blue LEDs. Hysteresis window widening observed in the transfer characteristics of the device with increasing measurement step duration under constant LED illumination. This denotes that a higher pulse duration allows photogenerated carriers to access border traps in the oxide that are not otherwise accessible with fast measurements. The measurement for d) red, e) green, and f) blue LEDs shows that the response to blue LED is the highest since the hysteresis window shown in the inset suffers most shift for the case of blue LED.

MoS₂ Image Sensor

Figure 2-10 elucidates the detection threshold and energy benefits of the proposed MoS₂ image sensor based on MoS₂ phototransistor. For comparison, we have used a commercially

available Si PN PD to benchmark the detection threshold and energy expenditure of our MoS₂ based image sensor. Figure 2-10a shows the photoresponse characteristics i.e., I_{PD} versus V_{PD} for the Si PD under different illumination intensities of red (top), green (middle) and blue (bottom) LEDs. Similarly, the cross correlation (CC) between the photoresponse for an MoS₂ phototransistor and the LED input signal is calculated and demonstrated in Figure 2-10b along with the dependence on the back-gate bias. The reverse bias diode current increases in magnitude with increasing V_{LED} . Figure 2-10c shows a comparison of the signal-to-noise ratio (SNR) measured for the MoS₂ image sensor and a commercially available Si PD. The SNR is plotted for varying V_{LED} and V_{BG} . For each of the red, green, and blue LED light sources, a periodic signal of 5 Hz was applied, and the output current response from the MoS₂ image sensor was measured at different gate voltages for increasing illumination intensities. Again, the SNR increases monotonically with V_{LED} and shows a non-monotonic trend along the applied gate voltage V_{BG} . The gate voltage can be optimized to achieve high photoresponse based on the operating regime of the device. Due to slight threshold variation between the detectors corresponding to red, green, and blue LEDs, the highest SNR for a given V_{LED} differs in the three cases. Figure 2-10d shows the total energy consumed by the MoS₂ phototransistor in detecting the 5 Hz periodic signal. The energy consumed monotonically decreases with negative V_{BG} corresponding to the subthreshold and OFF state of the MoS₂ image sensor. Although the SNR for the Si PD is relatively higher, our MoS₂ image sensor can detect low intensity signals at energy expenditure of tens of picojoules. Energy expenditure to detect the same signal on Si PD is calculated to be in the range of hundreds of nano Joules each for red, green, and blue LED light sources. Interestingly, the monolayer MoS₂ based single-pixel image sensor shows an energy benefit of 1000x of magnitude against the Si PD. The response of the MoS₂ image sensor to red, green, and blue LED light sources already indicates a high spectral range in the visible region. The MoS₂ phototransistor exhibits a high

electron carrier mobility and low dark current noise (pA) in the subthreshold optical detection regime making it an ideal candidate for low noise photodetection.

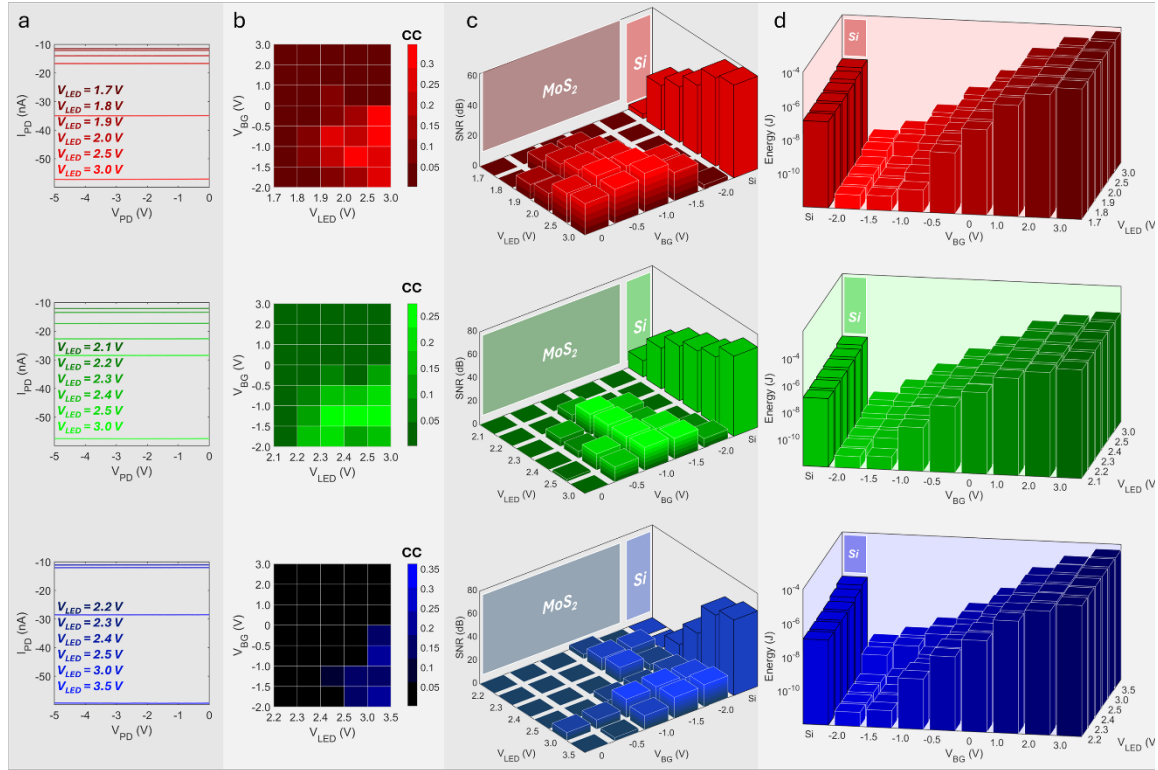


Figure 2-10: MoS₂ Image Sensor and Silicon Photodiode Benchmarking: a) Photoresponse characteristics i.e., I_{PD} versus V_{PD} for the Si photodiode under different illumination intensities for red (top), green (middle) and blue (bottom) colors of LEDs, b) Cross-correlation (CC) is measured to see the photoresponse current, I_{PH} , against the increasing LED bias range (V_{LED}) measured on the MoS₂ image sensor as a function of the gate bias, V_{BG} , for red, green, and blue LEDs. This is measured to assess the optimal range of detection for the MoS₂ photodetector, c) Signal-to-noise (SNR) ratio extracted from the power spectral density for both MoS₂ image sensor and Si photodiode for different illumination intensities of red, green, and blue LEDs. Although, Si photodiode shows a higher SNR, the tunability that the MoS₂ image sensor provides in terms of the range of operation with the dependence on gate bias voltage, V_{BG} , can be beneficial, d) Energy expenditure in detection is calculated from the fast Fourier transform of the photoresponse of the MoS₂ and Si photodetectors to the pulsing signal at a given frequency, This is repeated for different back-gate voltages and for different intensities of red, green, and blue colors of LEDs.

Sensitivity (S) is an important optoelectronic characteristic for a photodetector and is defined as the ratio of the photocurrent I_{PH} to the luminous flux intensity L_ϕ . Figure 2-11a shows the sensitivity of the MoS₂ image sensor as a function of V_{BG} and V_{LED} . We have used the Si PD to calibrate L_ϕ . Sensitivity of Si PD is known from its rating ($S = 9 \text{ nA/lx}$) and its reverse biased photocurrent characteristics can be used to extract L_ϕ . The sensitivity for the MoS₂ image sensor far exceeds the rated sensitivity of the Si PD. However, high dark current in the ON state makes signal detection difficult. In the subthreshold and OFF state of the MoS₂ image sensor, despite its low sensitivity, signal detection is possible owing to the exponentially lower dark current compared to Si PD. For this reason, we believe that SNR is a better metric to rate the photodetection capabilities of our MoS₂ image sensor. Frequency dependent measurements for the MoS₂ image sensor are presented for different V_{BG} in Figure 2-11b. As seen from the figure, the peak SNR does not change significantly with higher frequencies proving the high speed photodetection capability of the MoS₂ image sensor. The technique for extraction of SNR for the phototransistor has been detailed earlier.¹⁰³ Detection of higher frequency optical pulses is limited by the rate of hole trapping/de-trapping at the MoS₂/Al₂O₃ interface. Hence for higher frequencies of input signal, SNR degradation is expected. The non-monotonic trend along the V_{BG} axis is due to the photogating effect. The scalability of a sensor over a large area is mainly dependent on the device-to-device variation in the as-fabricated chip. Figure 2-11c shows the statistics of the device characteristics on our as-fabricated chip. Minimal variation in the characteristics is a result of excellent material growth and device fabrication. Inset in Figure 2-11c shows a histogram of the SNR and minimal variation is observed. Finally, the fast Fourier transform of the time-varying signal from the MoS₂ image sensor at varying frequencies of input LED signal, shown in Figure 2-11d, suggests that the MoS₂ image sensor is capable of signal detection in the kHz frequency range. Next, we test the image acquisition capability of the MoS₂ based single pixel

image sensor and model a multi-pixel demonstration highlighting the energy benefits against commercial Si PD.

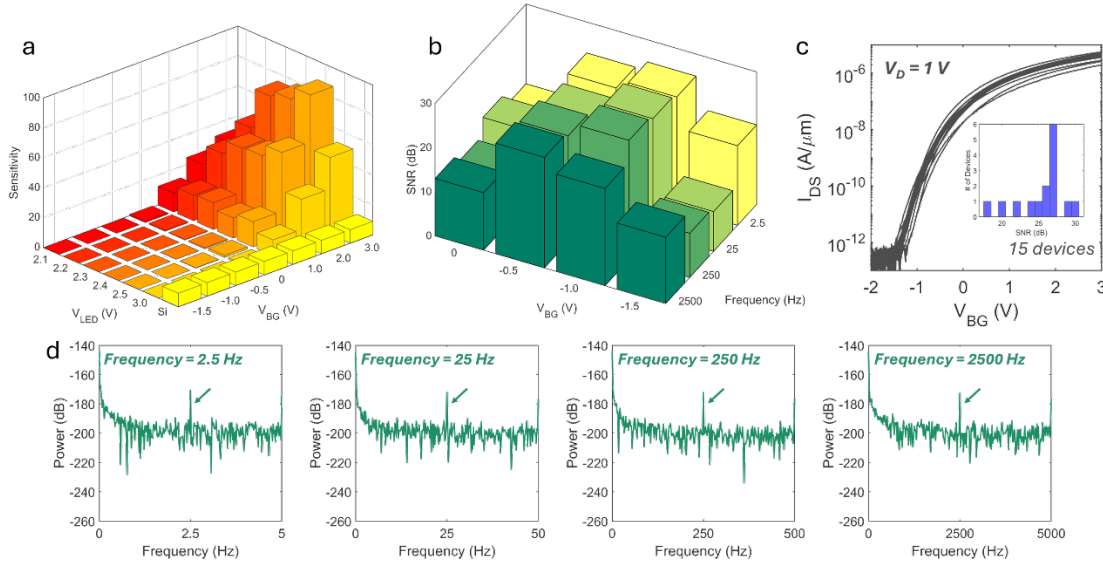


Figure 2-11: Figures of Merit for MoS₂ Image Sensor: a) Sensitivity of the MoS₂ image sensor compared with that of Si photodiode measured across the gate bias range and for different LED intensities, b) Signal-to-Noise Ratio (SNR) calculated from the power spectral density of the fast Fourier transform calculated on the output photoresponse of the MoS₂ image sensor for varying frequencies of LED pulses denotes the range of photodetection speed, c) Transfer characteristics statistics of 15 MoS₂ FETs that are characterized for image sensing show very less variability in device performance as well as in the SNR (inset) to an input signal, d) Power Spectral density of the fast Fourier transform of the time-varying signal denoting the detected signals of LED pulse signals.

Multi-pixel MoS₂ Image Sensor

Figure 2-12 elucidates the energy benefits of the MoS₂ image sensor for image acquisition applications based on the photoresponse model developed for MoS₂ and Si PD.

Figure 2-12a shows the input image of size 25 X 25 pixels in the red, green and blue channels with pixel intensities (0 – 255) scaled to LED current values (100 nA – 5 μA) and sequentially fed to the respective red, green, and blue LED light sources. The current response from each

device corresponding to red, green and blue channel input is recorded in its subthreshold regime ($V_{BG,red} = -0.65\text{ V}$, $V_{BG,green} = -0.75\text{ V}$, $V_{BG,blue} = -0.75\text{ V}$) and is scaled back to intensity values (0 – 255) shown in Figure 2-12b. The current I_{DS} corresponding to input pixel was normalized to map I_{PH} to pixel intensities. Corresponding color gradients are very clearly visible from the red, green, and blue colormaps of output photocurrent I_{PH} denoting the high photoresponsive nature of the MoS₂ image sensor. Pixelation in the output image is a result of the inherent device stochasticity in the subthreshold regime.

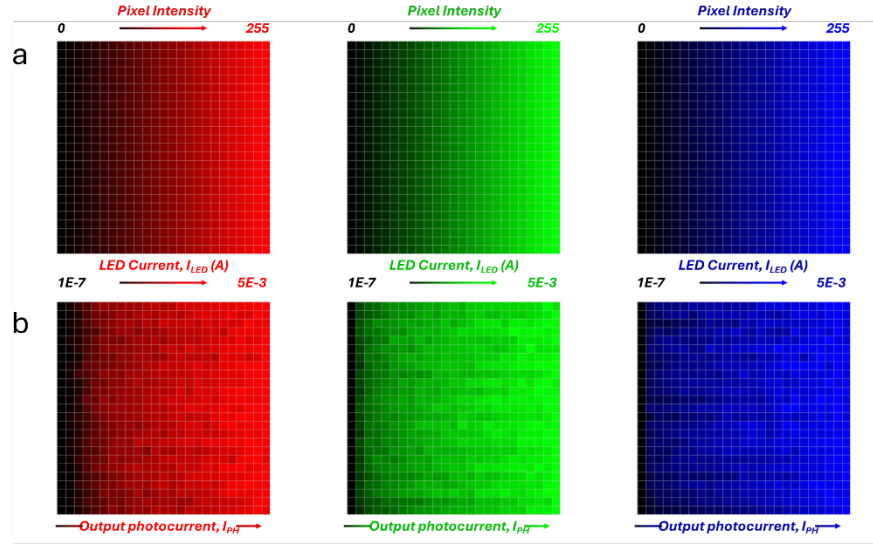


Figure 2-12: MoS₂ Image Sensing Array: a) Image depicting the LED current ramp for red, green, and blue colors is given as input to the MoS₂ image sensor. The LED current is mapped to the pixel intensity and a 25x25 image is generated as the input image. b) Similarly, the output photocurrent from the MoS₂ image sensor is remapped to the pixel intensity and the image is reconstructed. The reconstructed image response from the MoS₂ image sensor very well reflects the input image from the dark to brighter shades.

We have also developed a model for a multi-pixel demonstration of the MoS₂ image sensor and to better validate the energy benefits against commercial Si PD. The transfer characteristics of the MoS₂ device is captured using the Virtual Source Model (Lundstrom *et al.*)⁵⁸, shown in Figure 2-13a. The LED output characteristics for red, green, and blue colors are captured using an empirical relationship that relates the input voltage V_{LED} to the output current

I_{LED} . The modeled LED output characteristics for the red, green, and blue LEDs are shown in Figure 2-13b. Furthermore, the photoresponse of the Si PD and the MoS₂ image sensor are modeled using empirical relationships and curve fitting, as shown in Figure 2-13c and Figure 2-13d.

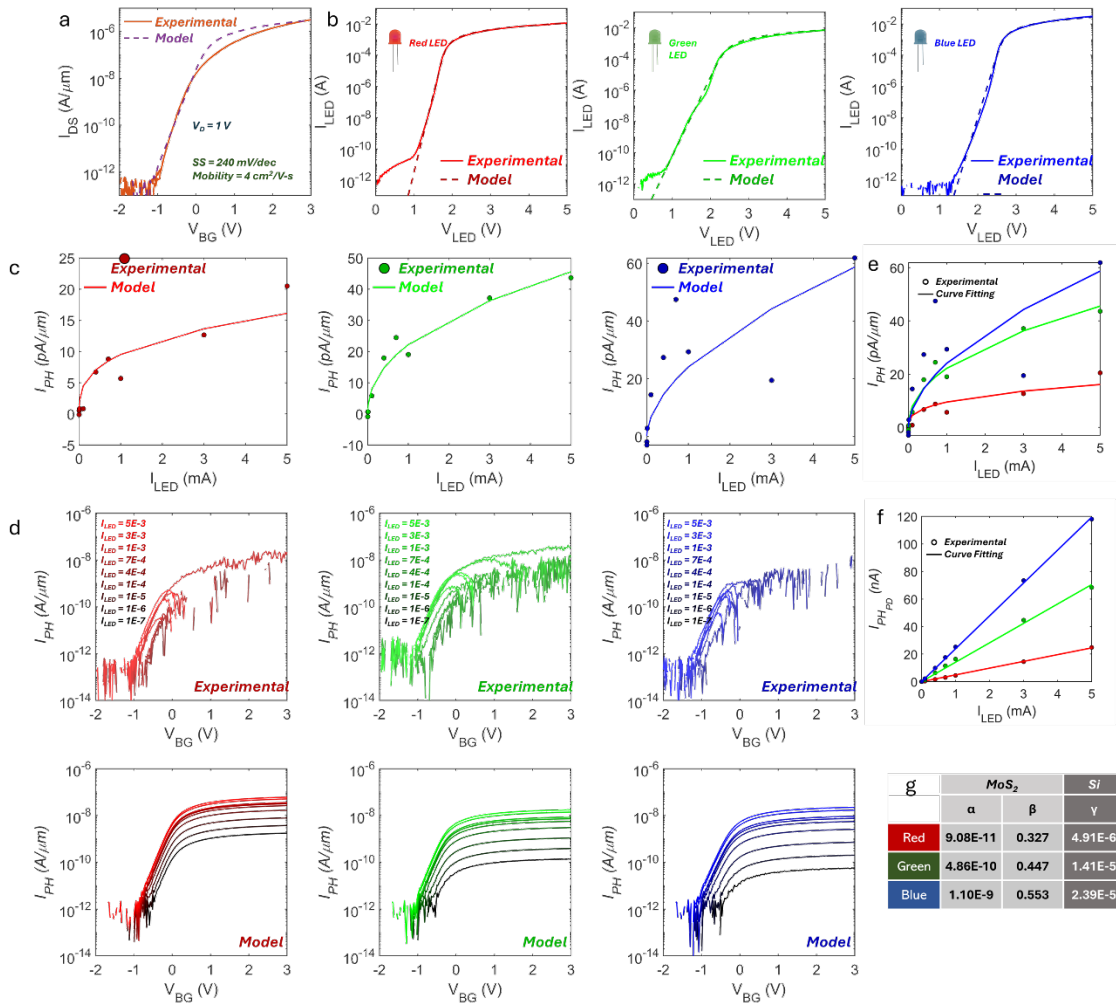


Figure 2-13: Modeling the MoS₂ Image Sensor: a) The MoS₂ FET characteristics are simulated using the Virtual Source Model and a good agreement between the experimental and simulated device characteristics is obtained, b) LED characteristics are modeled using an empirical relationship, c) Photocurrent I_{PH} variation with increasing LED intensities with an LED input current are modelled and curve fit, and a power-law curve fit is obtained for each of the red, green, and blue LEDs, d) Photocurrent I_{PH} is also modelled using a combination of the semi-empirical Virtual Source Model along with an empirical relationship on the LED current dependence to obtain a match in the subthreshold device regime, e) Curve-fitted parameters for MoS₂ photocurrent and LED current. The LED current is semi-empirically modelled with the equation $I_{LED} = I_{ON}$,

$\text{fit} \cdot \log(1 + \exp(q \cdot (V_{\text{LED}} - V_{\text{LED, TH}}) / (m_{\text{LED, fit}} \cdot k_B \cdot T)))$ and the conductance in the MoS₂ channel is calculated as $G_{\text{photo}}(\text{MoS}_2) = \alpha \cdot (I_{\text{LED}})^\beta$ which is then added to the device conductance shown in a), f) Photodiode current follows linearly with increasing LED current and is mapped using the equation $G_{\text{photo}}(\text{Si}) = \gamma \cdot (I_{\text{LED}})$, g) Final fitting parameters are presented in the table for both MoS₂ and Si photodetectors.

After having mapped the photoresponse from the MoS₂ image sensor, Si PD and developed an empirical relationship to relate the LED current to the photocurrent, we can estimate the energy consumed for each of the photodetectors. Colored dots in Figure 2-13e indicate the extracted I_{PH} in response to varying intensities of red, green, and blue LED inputs. Figure 2-13f shows the extracted photocurrent from the Si PD (I_{PHPD}) corresponding to the same LED intensities. For the case of MoS₂ image sensor, I_{PH} follows a power law dependence with I_{LED} , while the I_{PHPD} shows a linear dependence with I_{LED} . Solid lines in Figure 2-13e and Figure 2-13f represent the curve fitted photoresponse showing a power law curve fit ($I_{PH} = \alpha I_{LED}^\beta$) in the former case and a linear fit ($I_{PHPD} = \gamma I_{LED}$) in the latter. The values for α , β and γ are tabulated in Figure 2-13g. Now, a complete image acquisition model is developed where each pixel intensity is fed to a multi-pixel MoS₂ image sensor model. This is used to simulate the deployment scenario of both the photodetectors and compare the energy consumption between the two. The input image to the model is shown in Figure 2-14a. Output current I_{PH} and I_{PHPD} is scaled back to pixel intensity values and the reconstructed image is shown in Figure 2-14b and Figure 2-14c respectively. The total energy expenditure for a multi-pixel demonstration of MoS₂ image sensor is found to be at least 1000X lower than that of Si PD. As can be seen from the output image, there is very little loss in the image quality and spatial features, however this has got more to do with the integration and image reconstruction, most of which requires peripheral circuits.

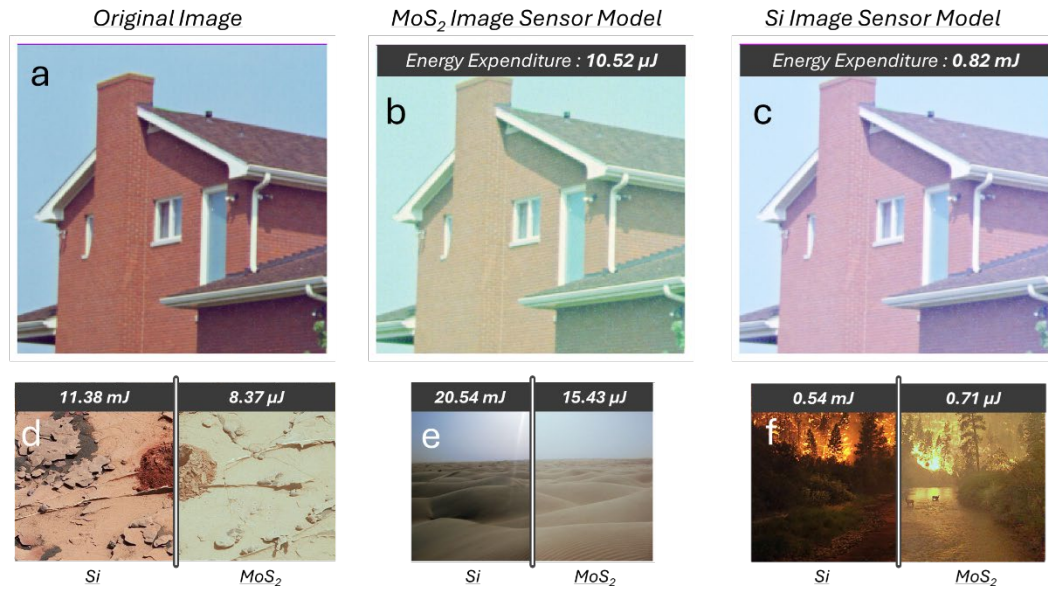


Figure 2-14: MoS₂ Image Sensor Deployment Scenario: a) Input image to the model simulating the output response b) from an array of MoS₂ image sensors and c) from an array of Si photodiodes. The energy consumption from the MoS₂ image sensor array is very minimal as compared to that of Si photodiode owing to the low dark current in the MoS₂ device in the subthreshold regime of operation. Other scenarios present the scenarios where the MoS₂ image sensor will be particularly useful due to lower energy requirements effective in resource constrained environments such as for d) space exploration, e) environment monitoring, and f) forest fire detection.

The ultra-low power detection in the MoS₂ image sensor is due to the subthreshold, low-noise operation and can be utilized for image sensing applications in resource constrained environments. Although the images obtained from the MoS₂ image sensor lose contrast, this can be improved by increasing the dynamic range of the image sensor. The dynamic range can be improved by improving the extent of current saturation for higher intensities. The Si PD outperforms the MoS₂ image sensor when it comes to contrast due to its linear output response to increasing light intensities compared to a saturating power law curve in case of MoS₂ image sensor. However, the deployment of such sensors will be beneficial in areas that demand constant monitoring and do not have electrical connectivity through power lines. Some more images from resource constrained environments are fed into the model to compare the energy values of the two

as shown in Figure 2-14d-f. There may not be a need to collect highly detailed contrast information of the environment if the image sensor is responsive to rapid changes in the scene, a capability which has already been demonstrated in the previous section. Hence, both cases where environmental scenes are subject to dynamic change (thunderstorms, wildfires etc.) and a sudden change (tsunamis, flashfloods etc.) can be detected on the MoS₂ image sensor with very little energy expenditure.

Secure Memtransistors

Introduction to Hardware Security

Breaches in hardware security are becoming more pervasive in the semiconductor industry raising major concerns to the government, businesses, and consumers.¹⁰⁴⁻¹⁰⁷ Compromised hardware chips pose a serious threat to the economy of a country and to the safety of its people. They impact the security and reliability of a wide range of electronic systems used in defense, transportation, communication, healthcare, and manufacturing across the globe.^{108,109} Recent reports have suggested an alarming increase in the hardware security threats, including piracy of hardware intellectual property (IP), reverse engineering, cloning, recycling, and remarking.¹⁰⁹⁻¹¹¹ These problems are further aggravated with the increasing nodes in an always-connected internet of things (IoT) ecosystem.⁷⁴ Due to the highly globalized integrated circuit (IC) fabrication process, an attacker in the supply chain may steal information, add Trojan, or even distribute compromised chips through unauthorized channels. IC manufacturing is likely to continue being outsourced to reduce costs and increase profits, thus breeding security concerns; therefore, hardware security must be a critical design consideration alongside device performance, reliability, and power consumption for any existing or emerging technology.

While silicon-based complementary metal oxide semiconductor (CMOS) technology offers hardware security solutions,^{107,108,112,113} these are often inconclusive, inadequate, and energy and area inefficient. Furthermore, the demise of dimension-scaling of silicon-based CMOS, computing bottleneck enforced by von Neumann architectures, and new requirements imposed by resource-limited IoT edge devices and sensors necessitates alternative approaches based on unconventional and multifunctional materials and devices.^{104,112,114} Tremendous progress has been made in the field of memristors for security applications. Security primitives based on stochastic switching mechanism in memristors are often power-hungry and also require additional CMOS-based peripheral circuitry.¹¹⁵⁻¹¹⁹ Although energy challenges have been mitigated in the article by Wen *et al.*,¹²⁰ small current ratio originating from the defects requires extensive peripheral read-out circuitry using CMOS technology to differentiate bits. On the other hand, memtransistor is a three-terminal device that allows electrostatic gate control to modulate the resistance across the device in addition to the non-volatile programming capability. Any peripherals can be made using MoS₂ FETs and hence the need for a hybrid design can be eliminated. Furthermore, MoS₂ memtransistors are optically active allowing integration of sensing with compute and storage.

Here, we introduce atomically thin and photosensitive memtransistor technology based on monolayer MoS₂ as a non-von Neumann computing platform to offer comprehensive, low-power, and area efficient security solutions. In short, we combine growth- and fabrication-related imperfections introduced in monolayer 2D film manifesting in device-to-device variation with gate-tunable persistent photoconductivity and analog electrical programmability to enable bottom-up implementation of diverse security primitives on a single chip. We demonstrate 2D memtransistor-based physically unclonable function (PUF), anticounterfeit measures, optical watermarks, and camouflaged devices and circuits to ensure authentic use of ICs, prevent IC recycling, stop IC reverse engineering, and protect IPs, respectively. Our bottom-up

implementation of an all-in-one hardware security platform can offer protection to IoT edge devices and future generations of microelectronic systems.

The motivation behind the use of 2D memtransistor technology is multifold: while the recent demonstration of 2 nm silicon-based nanosheet technology by IBM is impressive, thickness scaling of silicon remains a challenge without compromising the performance. Atomically thin two-dimensional (2D) layered semiconductors such as transition metal dichalcogenides (TMDCs) are $\sim 10\times$ thinner at their monolayer limit (~ 0.7 nm) compared to state-of-the-art silicon fin structures (~ 6 nm) and promises to offer better channel-to-dielectric interfaces owing to the absence of dangling bonds in transistor geometries. Recent report of scalable fabrication of ultra-scaled transistors ($L_{CH} \sim 10$ nm) on chemical vapor deposition (CVD) grown MoS_2 with considerably low hysteresis, high ON current (~ 560 A/m), and low subthreshold swing (~ 120 mV/dec) shows good promise in order to meet the requirements set forth by the International Roadmap of Devices and Systems (IRDS).¹²¹ A long-standing concern on high contact resistance of 2D transistors has also been mitigated earlier this year for MoS_2 .¹²² In addition, circuit, and architecture level demonstrations of digital, analog and radio frequency (RF) electronics based on 2D transistors are already available¹²³⁻¹²⁷ and emerging applications such as neuromorphic, optoelectronic, straintronic, and biomimetics exploiting sensing, computing, and storage capabilities of 2D transistors have also been reported.^{85,88,100,101,103,128,129} However, one fundamental question that is yet to be addressed is that whether the emerging 2D material-based hardware infrastructure can offer adequate resilience to the rampant security vulnerabilities experienced by current silicon technology.^{130,131} If so, what properties of 2D materials and devices can be exploited to better support various security schemes?

2D Hardware Security Platform

Figure 2-15a visually summarizes the security needs, potential solutions, and how our 2D memtransistor-based non-von Neumann hardware platform exploits material and device level properties and phenomena to accomplish the same. 2D memtransistor were fabricated using large area CVD-grown monolayer MoS₂ on a back-gate memory stack comprising of 50 nm ALD-grown Al₂O₃ on Pt/TiN/p⁺⁺-Si with non-volatile and analog programming capability (see *Methods* sections for more detail of material synthesis and device fabrication). First, device-to-device variation in a large population of 2D memtransistors (Figure 2-15b) is exploited to construct high entropy PUFs that can be used as secure keys for IC authentication. Next, long-term retention and analog programmability of 2D memtransistors (Figure 2-15c) is utilized for designing anticounterfeit measures such as electronic counter and clock to track the number of usages and the age of the chip, respectively, to identify recycled and remarked ICs. The same capability is expanded for camouflaging device and circuit functionalities to protect ICs against reverse engineering. Finally, the phenomenon of gate-tunable persistent photoconductivity of 2D memtransistors (Figure 2-15d) is used to design hardware watermarks as defense against IP piracy/theft.

a Non-von Neumann 2D memtransistor based comprehensive hardware security

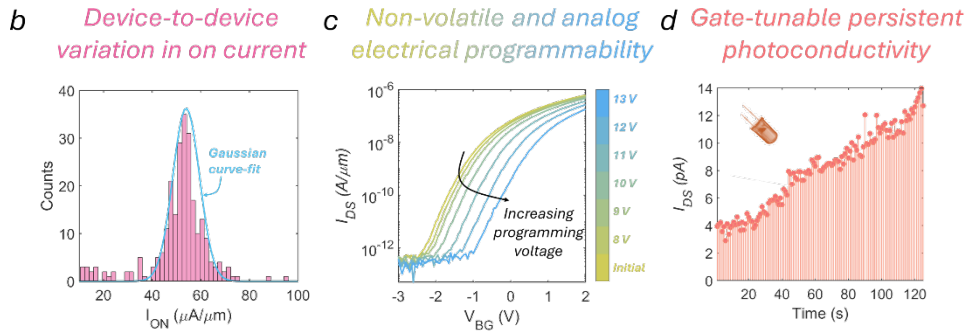
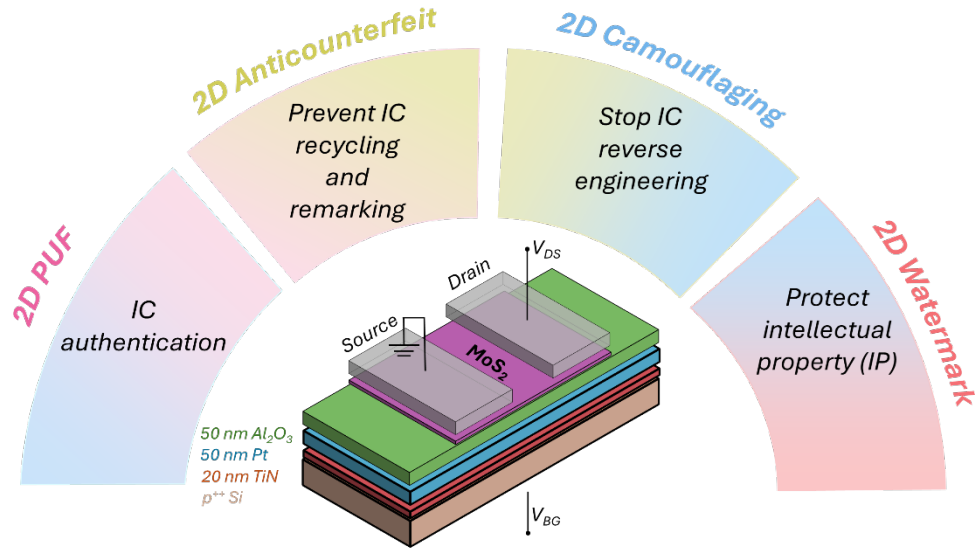


Figure 2-15: 2D memtransistor-based non-von Neumann hardware security platform: a) Visual summary of functional capabilities of our non-von Neumann 2D memtransistor fabricated using large area CVD-grown monolayer MoS₂ on a back-gate stack comprising of 50 nm ALD-grown Al₂O₃ on Pt/TiN/ p^{++} -Si with non-volatile and analog programming capability. b) Device-to-device variation in on-current among large memtransistor population is exploited for the construction of high entropy PUFs that can be used for IC authentication. c) Analog programmability and long-term retention are utilized for designing anticounterfeit measures such as electronic counter and clock to track the number of usages and the age of the chip, respectively, to identify recycled and remarked ICs. This programmability of 2D memtransistor is also used for camouflaging device functionalities to protect against IC reverse engineering. d) The phenomenon of gate-tunable persistent photoconductivity is exploited for the design of hardware watermarks as defense against IP piracy or theft.

Note that several demonstrations on memristor based crossbar arrays have utilized the process variations and inherent stochasticity for device authentication and random number generation.¹³²⁻¹³⁵ Hybrid memristor-CMOS circuits have been used to demonstrate PUFs with

higher attack resilience, lower hardware overhead, and lower energy consumption.^{136,137} Similarly hybrid memristor-CMOS circuit models have been proposed to obfuscate IC layouts using polymorphic gates and cyclic-locking schemes.¹³⁸ Models of chaotic memristive systems using Chua circuits have also been demonstrated for encryption and secure communication.^{139,140} While promising, two-terminal memristor-based non-von Neumann platforms are limited in computational capability and require CMOS peripherals and sensors, which increases area and energy overhead. In contrast our proposed three-terminal memtransistor technology with the added feature of photosensitivity owing to the use of monolayer 2D materials offer stand-alone and holistic solution for in-memory computing and sensing, which is critical for achieving diverse and energy and area efficient security solutions.

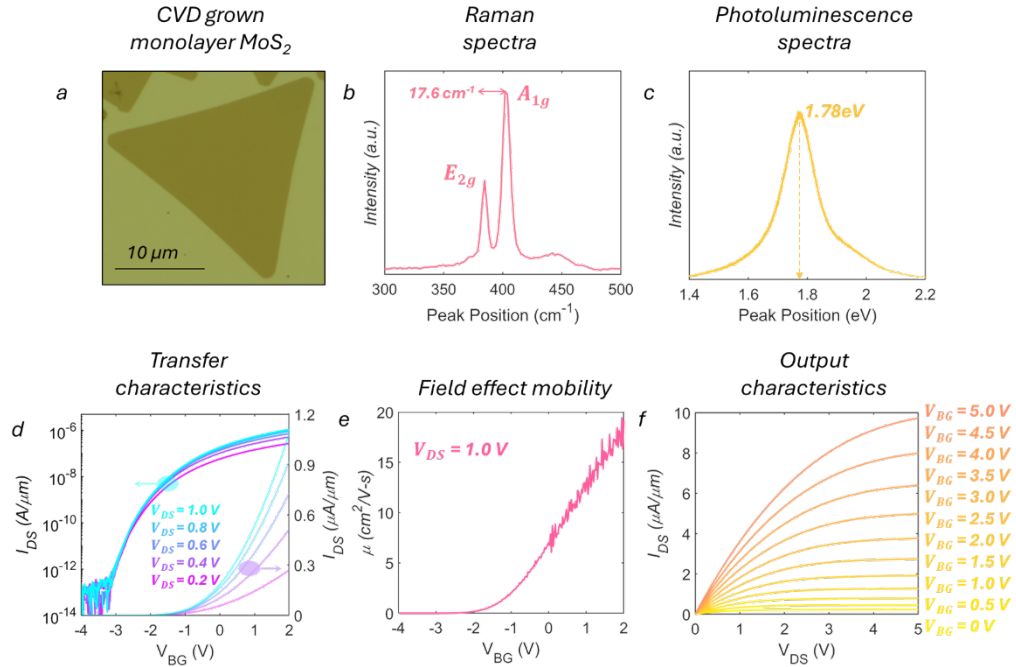


Figure 2-16: Fabrication and characterization of monolayer MoS₂ memtransistors: a) Optical image, b) Raman spectra, and c) photoluminescence (PL) spectra of post-transfer monolayer MoS₂ obtained using a 488 nm LASER at room temperature. Raman peak separation of 17.6 cm⁻¹ between the characteristics A_{1g} and E_{2g} peaks and PL peak observed at 1.78 eV confirms monolayer MoS₂. d) transfer characteristics, e) field effect mobility (μ), and h) output characteristics of a representative MoS₂ memtransistor with 5 μ m channel length (L), 5 μ m channel width (W) and 40 nm Ni/40 nm Au as the source and drain contacts. The device shows an ON/OFF current ratio of

$\sim 10^6$, subthreshold slope (SS) of ~ 250 mV/decade, threshold voltage (V_{TH}) of ~ -0.5 V, peak μ of ~ 20 cm²V⁻¹s⁻¹, and on current of ~ 10 μ A/ μ m for $V_{BG} = 5$ V and $V_{DS} = 5$ V. These results indicate that the performance of our CVD grown MoS₂ memtransistors are at par with the recent literature and comparable to exfoliated single crystal flakes.

As mentioned earlier, MoS₂ used in this study was grown by salt-assisted CVD. Post-synthesis, the film is transferred onto the gate dielectric stack by PMMA-assisted wet transfer process.¹⁴¹ Figure 2-16a shows the optical image of monolayer MoS₂. The transferred film quality was assessed *via* Raman and photoluminescence (PL) spectra using a 488 nm LASER at room temperature as shown in Figure 2-16b and Figure 2-16c. Raman peak separation of 17.6 cm⁻¹ between the characteristics A_{1g} and E_{2g} peaks and PL peak observed at 1.78 eV confirms monolayer MoS₂. Figure 2-16d shows the transfer characteristics in linear and logarithmic scale where the source to drain current (I_{DS}) is plotted as a function of the back-gate voltage (V_{BG}) measured at different drain voltages (V_{DS}). The *n-type* characteristics can be attributed to electron injection due to the metal Fermi level pinning close to the conduction band being consistent with the previous studies on metal-semiconductor interface.^{90,142} The MoS₂ memtransistor shows an ON/OFF current ratio of $\sim 10^6$, subthreshold slope (SS) of ~ 250 mV/dec and low gate leakage owing to the high quality of the gate dielectric, semiconducting material and contact interfaces. The threshold voltage (V_{TH}) was extracted using iso-current method at $I_{DS} = 100$ nA/ μ m and found to be ~ -0.5 V. Figure 2-16e shows the field effect mobility (μ) extracted from transconductance ($g_m = \frac{dI_{DS}}{dV_{BG}}$) with peak value of ~ 20 cm²V⁻¹s⁻¹. Figure 2-16f shows the output characteristics of the memtransistor *i.e.*, I_{DS} versus V_{DS} measured at different V_{BG} . The on current reached ~ 10 μ A/ μ m for $V_{BG} = 5$ V and $V_{DS} = 5$ V. The above results indicate that the performance of our CVD grown MoS₂ memtransistors are at par with the recent literature and comparable to exfoliated single crystal monolayer flakes. With basic material and device characterization

performed, we now discuss the realization of different security primitives based on these MoS₂ FETs.

2D Physically Unclonable Function

Maintaining a record of each IC using a unique identification key can prevent overproduced ICs from being remarked and sold by an adversary. PUFs are one of the most widely known security primitives for key authentication and IC fingerprinting. PUFs rely on variation in the physical characteristics of the devices such that the architecture-level output generates an ID which is unique to that IC. The electronic circuit gives the output response of the hardware to specific inputs, referred to as challenges. Together, the input to the PUF and the excitation output, is called a challenge-response pair (CRP). Pappu *et al.* reported PUF using unique speckle patterns generated by scattering of light from a liquid medium with suspended nanoparticles.¹⁴³ Uncontrollable and unavoidable physical process variations that exist in silicon CMOS fabrication have also been used to generate unique signatures for IC authentication.^{144,145} Arbiter PUFs, ring oscillator PUFs and SRAM PUFs are the most popular silicon based PUFs. However, the major drawback for silicon based PUFs is their low entropy owing to limited device-to-device variation, which is a direct consequence of otherwise flawless foundry process. This necessitates additional circuitry to compensate for reduced randomness adding energy and area overheads.

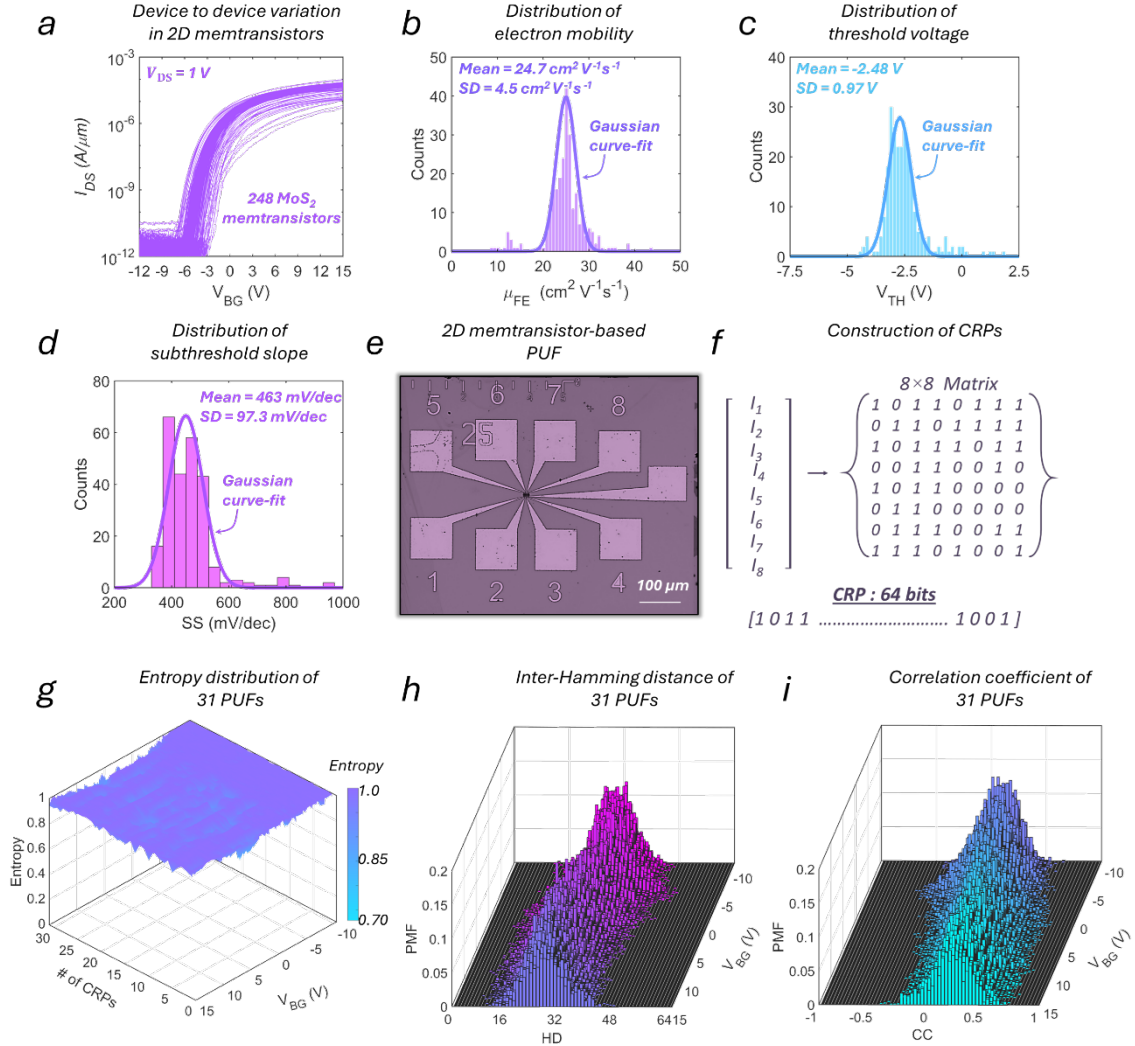


Figure 2-17: 2D memtransistor-based physically unclonable function (2D-PUF): a) Transfer characteristics of 248 identical memtransistors with $L = 1 \mu\text{m}$, $W = 2 \mu\text{m}$. The origin of device-to-device variation can be ascribed to factors like growth defects, sulfur vacancies, transfer-related strain, polymer residues, absorbed water molecules, etc. Histograms of b) μ_{FE} , c) V_{TH} , and d) SS extracted from these 248 memtransistors with a mean of 24.5 cm²V⁻¹s⁻¹, -2.48 V, and 463 mV/decade and standard deviation of 4.5 cm²V⁻¹s⁻¹, 0.97 V, and 97.3 mV/decade. e) Optical image of a representative 2D memtransistor-based PUF comprising of an array of 8 memtransistors. f) Construction of CRP. $V_{DS} = 1$ V and $V_{BG} = 0$ V are used as challenge and I_{DS} values obtained from 8 memtransistors are used to construct the response. Each I_{DS} value is converted to an 8-bit binary sequence, and the bit sequences obtained from 8 memtransistors are concatenated to construct a 64-bit CRP. This procedure is then repeated to obtain a total of 31 CRPs or PUFs from 248 memtransistors. g) Entropy of 31 PUFs at different V_{BG} . h) Histogram of hamming distance (HD) and i) correlation coefficient (CC) among 465 ($^{31}C_2$) pairs of CRPs measured at different V_{BG} . Mean entropy of ~ 0.95 , mean HD ~ 28 and mean CC ~ 0.1 are very close to their ideal values of 1, 32, and 0, respectively, confirming that the CRPs are uniform, unique, and uncorrelated and suggesting that the CVD-grown MoS₂ offers a random source for the construction of 2D memtransistor-based PUF.

Acknowledging the above-mentioned limitations in conventional silicon-based PUFs, we demonstrate a 2D memtransistor-based PUF, by exploiting the intrinsic device-to-device variation in our large area CVD grown monolayer MoS₂. Figure 2-17a shows the transfer characteristics of 248 identical memtransistors measured with $V_{DS} = 1$ V. The observed device-to-device variation can be ascribed to variation in different intrinsic/extrinsic parameters such as μ_{FE} , V_{TH} , SS , contact resistance *etc.* arising from factors like growth defects, sulfur vacancies, transfer-related strain, polymer residues, adsorbed water molecules, *etc.* Figure 2-17b-d, respectively show the histogram of μ_{FE} , V_{TH} , SS extracted from these 248 memtransistors with a mean of $24.5 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$, -2.48 V, and 463 mV/decade and standard deviation of $4.5 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$, 0.97 V, and 97.3 mV/decade . Clearly, these device parameters follow random Gaussian distributions. Leveraging these variations associated with the memtransistors, we construct PUFs. Figure 2-17e shows the optical image of a representative 2D memtransistor-based PUF comprising of an array of 8 memtransistors. $V_{DS} = 1$ V and $V_{BG} = 0$ V are used as challenge and I_{DS} values obtained from 8 memtransistors are used to construct the response. Each I_{DS} value is converted to an 8-bit binary sequence, and the bit sequences obtained from 8 memtransistors are concatenated to construct a 64-bit CRP as shown in Figure 2-17f. This procedure is then repeated to obtain a total of 31 CRPs or PUFs from 248 MoS₂ memtransistors.

To assess the efficacy and randomness associated with the generated CRPs, we have employed various statistical metrics such as entropy, hamming distance (HD), and correlation coefficient (CC). Entropy is defined as a measure of randomness or unpredictability associated with the cryptographic keys which are computed based on the equation below:

$$E = -[p \log_2 p + (1 - p) \log_2 (1 - p)]$$

Here, p is the probability of finding either a 1 or a 0 in a bit sequence. Ideally, we would expect $p = 0.5$, for ensuring maximum entropy of unity. Figure 2-17g shows the entropy of 31 PUFs at different V_{BG} . We observed that the PUFs demonstrates a mean entropy of ~ 0.95 , which

is very close to the ideal value of 1, implying that the generated CRPs are random. HD is another key measure that defines the number of bit substitutions required to transform one CRP to another. Ideally, a HD that equals to half the bit length ensures a maximum uniqueness of about 50%, *i.e.*, for a 64-bit sequence, ideal $HD = 32$. Figure 2-17h shows the histogram or probability mass function (PMF) of the calculated HD among 465 ($^{31}\text{C}_2$) pairs of CRPs measured at different V_{BG} . We observed that the CRPs demonstrates mean HD of ~ 28 close to the ideal value of 32, confirming their uniqueness. Finally, we compute CC , which determines the strength and statistical relationship between two CRPs. For CRPs to be an independent and identically distributed random variable, the CC must be equal to 0. Figure 2-17i shows the histogram or PMF of the calculated CC among 465 pairs of CRPs measured at different V_{BG} . The mean CC was found to be ~ 0.1 . Once again, this reassures us that the generated CRPs are identically distributed and uncorrelated. The read-out energy for each PUF was found to be ~ 1 nJ calculated using $\sum_{i=1}^8 I_{DS,i} V_{DS} \tau_{read}$, where $\tau_{read} = 100$ μs , and the footprint for each PUF was 16 μm^2 . In order to strengthen our claim, we have developed a virtual source (VS) model to capture the device-to-device variation in MoS_2 memtransistor shown in Figure 2-18a. Using the VS model, and the mean and standard deviation values extracted from the experimental data, 64,000 memtransistor were simulated to construct 1000 CRPs. These 1000 CRPs exhibited mean entropy of ~ 0.98 , mean $HD = 32$, and $CC = 0$. Clearly, the mean entropy is ~ 0.98 , which is close to the ideal value of 1 as can be seen from Figure 2-18b. Figure 2-18c-d show the histogram of the hamming distance (HD) and correlation coefficient (CC) among the $^{1000}\text{C}_2$ pairs of CRPs with mean values of 32 and 0, respectively. Hence, our results confirm that the CRPs generated from our 2D memtransistor-based PUFs meets the entropy/randomness expectation necessary for their implementation as cryptographic primitives in next generations of microelectronic ICs.

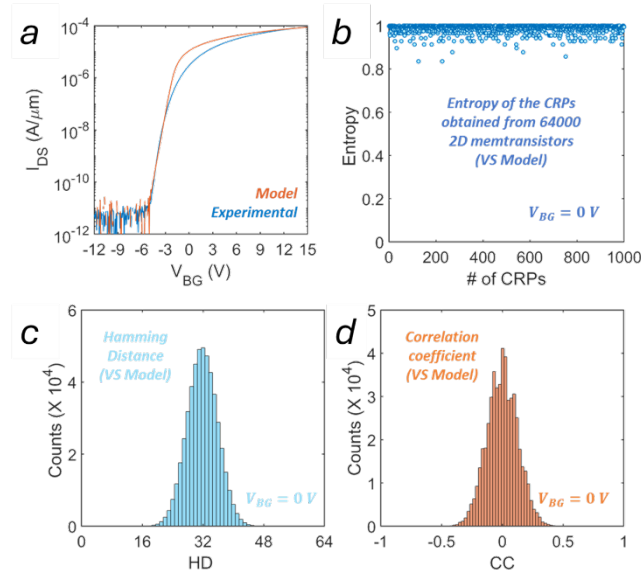


Figure 2-18: Empirical model for 2D memtransistor-based PUF: a) Experimentally measured (solid blue line) and simulated (red solid line) transfer characteristics of a representative 2D memtransistor with a channel length, $L = 1 \mu\text{m}$, and width, $W = 2 \mu\text{m}$, measured at a drain voltage, $V_{DS} = 1 \text{ V}$. Simulation results for the distribution of b) entropy, c) hamming distance (HD), and d) correlation coefficient (CC) for 1000 CRPs extracted from 64000 2D memtransistors obtained using the VS model. 2D memtransistor based PUF show near ideal entropy of ~ 0.98 , HD of 32 and CC of 0.

Electrically Programmable 2D Clock for Anticounterfeit

Counterfeit ICs are a growing concern for the semiconductor industry. During the assembly of ICs onto the printed circuit board low-quality counterfeit ICs may enter the supply chain. These ICs are classified into several categories, *i.e.*, recycled, remarked, defective, cloned, forged, tampered, and over-manufactured and are primarily collected from the electronic waste or in an illicit market to be sold as new. According to a report by Senate Armed Services Committee,¹⁴⁶ more than a million suspect counterfeit electronic components are present in several US military hardware, including military airplanes, helicopters, missile, and electronic warfare systems.^{147,148} Since counterfeit ICs often do not meet the performance standards or lifetime requirements, their use can result in catastrophic failure of electronic components in

mission critical applications and can cost human lives. Anti-counterfeiting is a defense against counterfeit ICs, which involves either counterfeit detection or counterfeit avoidance or both. Counterfeit detection methods mostly involve extensive study of device reliability including electromigration, negative bias temperature instability (NBTI), hot carrier injection, and time-dependent dielectric breakdown (TDBB), which bear the signature of aging devices.¹⁴⁹ On the other hand, counterfeit avoidance measures include physical unclonable functions (PUFs),¹⁴⁴ secure split test (SST),¹⁵⁰ hardware metering (HM),¹⁵¹ and electronic chip ID (ECID).¹⁵² More recent developments include DNA markings¹⁵² and use of nanorods (NR)¹⁵³ to detect cloned, recycled, and remarked counterfeit ICs. While these advancements are impressive, counterfeit detection and avoidance measures are considered to be still in their infancies, which offers tremendous scope for innovation in this field.

Here we introduce the concept of electronic counter and clock to track the usage and age of a chip, respectively, as measures for counterfeit detection by exploiting electrical programmability of our 2D memtransistor. Figure 2-19a shows monotonic shift in the device characteristics as a result of the application of different numbers (N_p) of positive programming voltage pulses of magnitude $V_{write} = 8$ V each for a duration of $t_{write} = 100$ μ s. Note that positive V_{BG} enforce electron accumulation

in the 2D channel that can be captured by the trap-states inside the oxide leading to the observed positive shift in V_{TH} in the post-programmed device characteristics. Figure 2-19b shows the retention of post-programmed device conductance values (G_F), read at $V_{BG} = V_{read} = 0$ V for 100 s corresponding to different N_p for $V_{write} = 8$ V and $t_{write} = 100$ μ s. G_F values were found to be constant, indicating non-volatile memory retention. This attribute of our 2D memtransistor can be used to construct an electronic counter or hardware metering device by associating each authentication of the chip with the application of one programming pulse to the device. As the chip continues to be used, the metering device keeps counting the total number of usage or N_p ,

which can be revealed by measuring G_F . In fact, each hardware module/architecture/circuit within a given chip can be associated with individual counters to track their respective usage without adding significant area overhead due to smaller footprint offered by a single device-based counter.

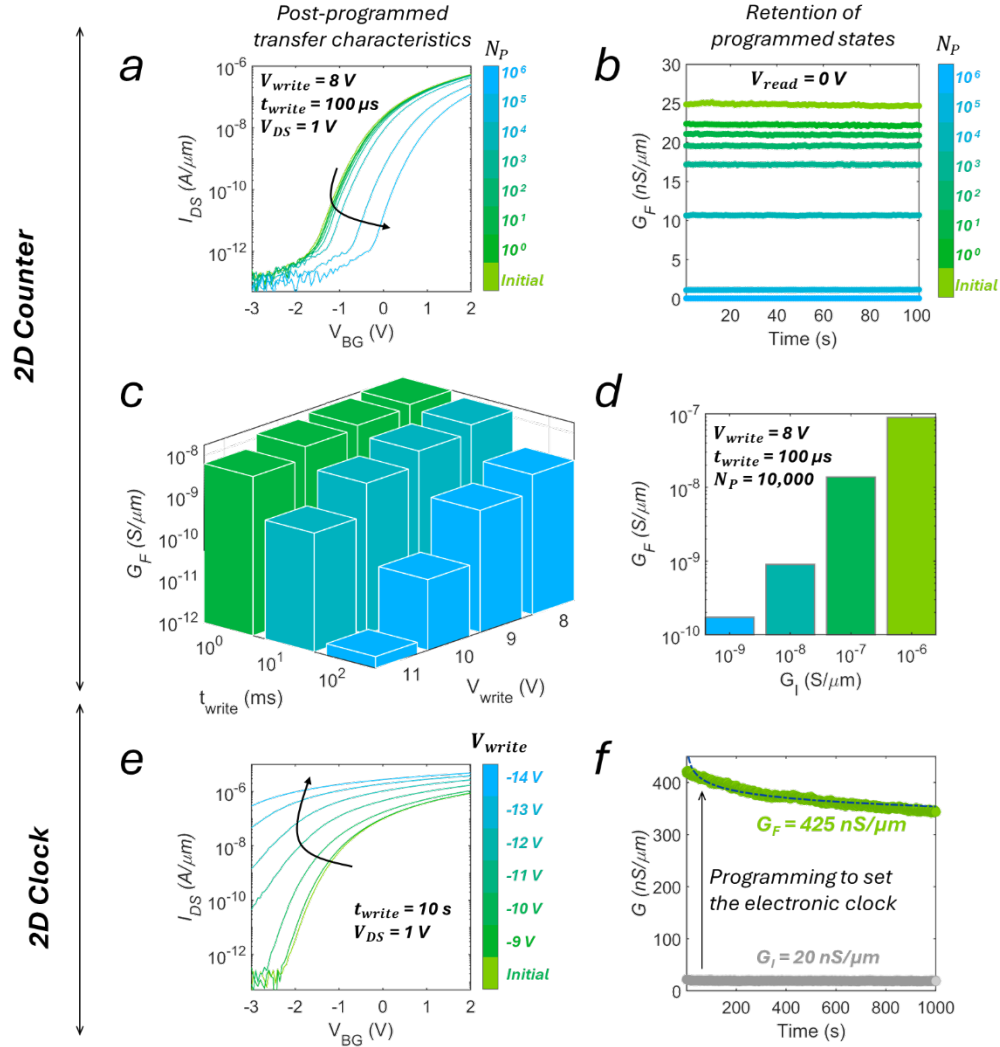


Figure 2-19: 2D memtransistor-based anticounterfeit measures: An electronic counter to track the number of usages of the chip is constructed by associating each authentication of the chip with the application of one programming pulse ($N_p = 1$) to the back-gate terminal of our MoS₂ memtransistor. a) Transfer characteristics of a memtransistor after the application of $N_p = 10^0, 10^1, 10^2, 10^3, 10^4, 10^5$, and 10^6 positive programming voltage pulses of magnitude $V_{write} = 8 V$ each for a duration of $t_{write} = 100 \mu s$. b) Retention of post-programmed device conductance values (G_F), read at $V_{BG} = V_{read} = 0 V$ for 100 s corresponding to different N_p in (a). G_F values were found to be constant, indicating non-volatile memory retention. c) G_F as a function of V_{write} and

t_{write} for same $N_P = 1000$. d) Dependence of G_F on the initial conductance (G_I) of the device for same N_P , V_{write} and t_{write} . Only from prior knowledge of G_I , V_{write} , and t_{write} , and by measuring G_F the usage of the chip, N_P can be determined allowing the manufacturer/chip-designer to obfuscate the counting scheme and usage information from illicit parties and prevent tampering/resetting of the counter. An electronic clock for tracking the age of the chip is constructed by programming the memtransistor using reverse polarity of the back-gate voltage, i.e., negative V_{write} . e) Transfer characteristics of a memtransistor after the application of different magnitude of negative V_{write} for $t_{write} = 10$ s. f) Temporal evolution of post-programmed G_F , which was found to follow a slow power-law decay. Only from the prior knowledge of G_F , and by measuring $G(t)$, the age of the chip can be revealed.

In addition, our hardware metering device based on 2D memtransistor offers features, which can be exploited to prevent reverse engineering of the counting scheme as well as conceal the usage information from untrustworthy users. For example, Figure 2-19c shows G_F as a function of V_{write} and t_{write} for same $N_P = 1000$. Here, the memtransistor's programmability aspect is utilized, as was introduced earlier. We cover some more detail on the programming magnitude and programming duration in Figure 2-20 with the pre- and post-programmed transfer characteristics. As expected, higher V_{write} and longer t_{write} leads to more electron trapping and hence greater positive shift in V_{TH} and lower G_F . Similarly, we found that G_F depends on the initial conductance (G_I) of the device for same N_P , V_{write} and t_{write} as shown in Figure 2-19d. Therefore, without having a prior knowledge of G_I , V_{write} and t_{write} it is difficult to predict N_P allowing the manufacturer/chip-designer to obfuscate the counting scheme and usage information from illicit parties. It also prevents adversaries from resetting the counter as well. Counters embedded in every chip can be assigned unique combinations of G_I , V_{write} and t_{write} and the information can be maintained in a secure database by trustworthy parties so that if and when needed the information can be revealed to prevent recycling of used ICs. Programming energy expenditure (E_P) per use for different V_{write} calculated using $E_P = \frac{1}{2} C_G V_{write}^2$, where C_G is the gate capacitance. E_P is found to be miniscule, in the order of few pico Joules, highlighting the energy efficiency of the proposed counterfeit detection scheme.

We also propose a natural clock based on the same 2D memtransistor to track the age of the chip independent of its usage. Here, we exploit analog programmability of the device using reverse polarity of the back-gate voltage, *i.e.*, negative V_{write} . Figure 2-19e shows the transfer characteristics of the device after the application of different magnitude of negative V_{write} for $t_{write} = 10$ s. Negative shift in V_{TH} indicate trapping of holes or equivalently release of electrons from the trapped states inside Al_2O_3 . Figure 2-19f shows the temporal evolution of post-programmed G_F , which was found to follow a slow exponential decay described empirically using Eq. 1.

$$G(t) = G_F \left(\frac{t}{\tau} \right)^{-\gamma} \quad [1]$$

Where, $\tau = 1$ s and $\gamma = 0.05$ are fitting parameter. From prior knowledge of G_F , and by measuring $G(t)$, the age of the chip can be revealed. For example, in the present case, the measured $G(t)$ will be $170 \mu S/\mu m$ after 1 year. Without any information on G_F , it is highly unlikely that the illicit recycler can reset the clock to make the chip appear as new. Furthermore, multiple clocks can be embedded in the same chip, each programmed at different G_F by using different V_{write} and t_{write} . This information can be maintained in a secure database, similar to the case of the counters, and can be revealed to end users to prevent recycling of remarked ICs. Additionally, for both the counter and the clock, the programming terminal can be made inaccessible to the end users eliminating the possibility that the attacker can reset either of them.

Nevertheless, our demonstration of electronic counter and clock based on 2D memtransistor offers a robust counterfeit avoidance mechanism that utilizes simple trapping/detrapping phenomena in gate-oxide instead of relying on complex circuits and/or extensive device reliability analysis used by current technologies. Additionally, it allows the chip manufacturer to embed a maximum license usage/period by predefining a threshold conductance for the electronic counter/clock such that the chip ceases to operate after the number of uses or

the age of the chip has reached the maximum value set by the manufacturer. Therefore, the device can not only serve to detect counterfeit but also avoid it by stopping to function beyond its maximum use/age.

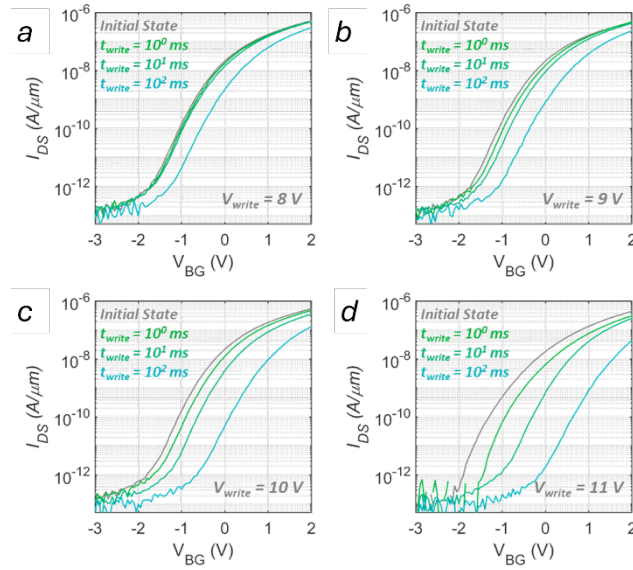


Figure 2-20: Dependence of programming voltage and programming pulse duration on the electrical programmability of 2D memtransistor: Initial and post-programmed transfer characteristics for increasing gate voltage bias a) $V_{\text{write}} = 8 \text{ V}$, b) 9 V , c) 10 V , and d) 11 V for $N_p = 1000$ pulses of varying t_{write} .

Optically Programmable 2D FET for IP Watermarking

In addition to counterfeiting, IP infringement is another rapidly proliferating crisis for the IC industry accounting for ~\$4 billion loss, annually. Claiming the rightful ownership of an IP in the court of law requires secret hardware signatures or watermarks that are incontestable *i.e.*, extremely unlikely to be present by coincidence in a pirated IC. A considerable amount of work has been done on IC watermarking using algorithmic constraints at various stages of logic and physical synthesis. However, most watermarking approaches focus on developing models at the circuit/architecture level¹⁵⁴⁻¹⁵⁶ and none exploit exclusive capabilities at the material and device

level. For example a recent work involve the use of nanowire-based polymorphic gates for IP protection.¹⁵⁶ While promising, these watermarks are area and energy inefficient.

Here, we propose an innovative watermarking strategy by exploiting the optical photoresponse of our 2D memtransistor. Note that monolayer MoS₂ exhibits a direct bandgap of ~ 1.8 eV making it sensitive to visible spectrum of light. Figure 2-21a shows the transfer characteristics of a representative MoS₂ memtransistor measured under different illumination intensities (I_{LED}) using a blue light emitting diode (LED). Photocarriers are generated in the MoS₂ channel, which under the applied V_{DS} drift towards the respective electrodes adding photocurrent to the already existing dark current in the device. With increasing I_{LED} the photocurrent increases and so does the channel conductance. This phenomenon is true for any phototransistor with a photoactive semiconducting channel including silicon. However, what makes our MoS₂ memtransistor different and enables us to develop watermarks is the phenomenon of persistent photoconductivity due to photogating effect. In most photosensitive transistors, the conductance returns to the dark state or pre-illumination level after the illumination ceases. However, in MoS₂ memtransistor the conductance persists beyond the removal of the optical stimuli depending on the biasing of the device during illumination. Figure 2-21b-c show transfer characteristics of the MoS₂ memtransistor measured in dark after a $t_{op} = 10$ s exposure to blue LED with the device biased in the on-state ($V_{OP} = 2$ V) and the off-state ($V_{OP} = -4$ V) during the illumination, respectively. While there is no significant change in the post-illumination characteristics for $V_{OP} = 2$ V, it shows a monotonic negative shift with increasing I_{LED} for $V_{OP} = -4$ V.

In MoS₂ memtransistor, trap states capable of capturing photogenerated carriers are available in the amorphous gate-oxide (due to growth imperfections of the ALD), in the MoS₂ channel (due to sulfur vacancies originating from the CVD growth), or even at the MoS₂/oxide interface (due to adsorbed organic/inorganic molecules during the wet-transfer process used for

the device fabrication). Note that the negative shift in the threshold voltage (V_{TH}) of MoS₂ memtransistor after illumination in the off state is a clear indication of excess positive charge at and near the MoS₂/Al₂O₃ interface. This suggests that photogenerated holes are captured by the trap states or equivalently electrons are released from the trap states through recombination with the photogenerated holes.

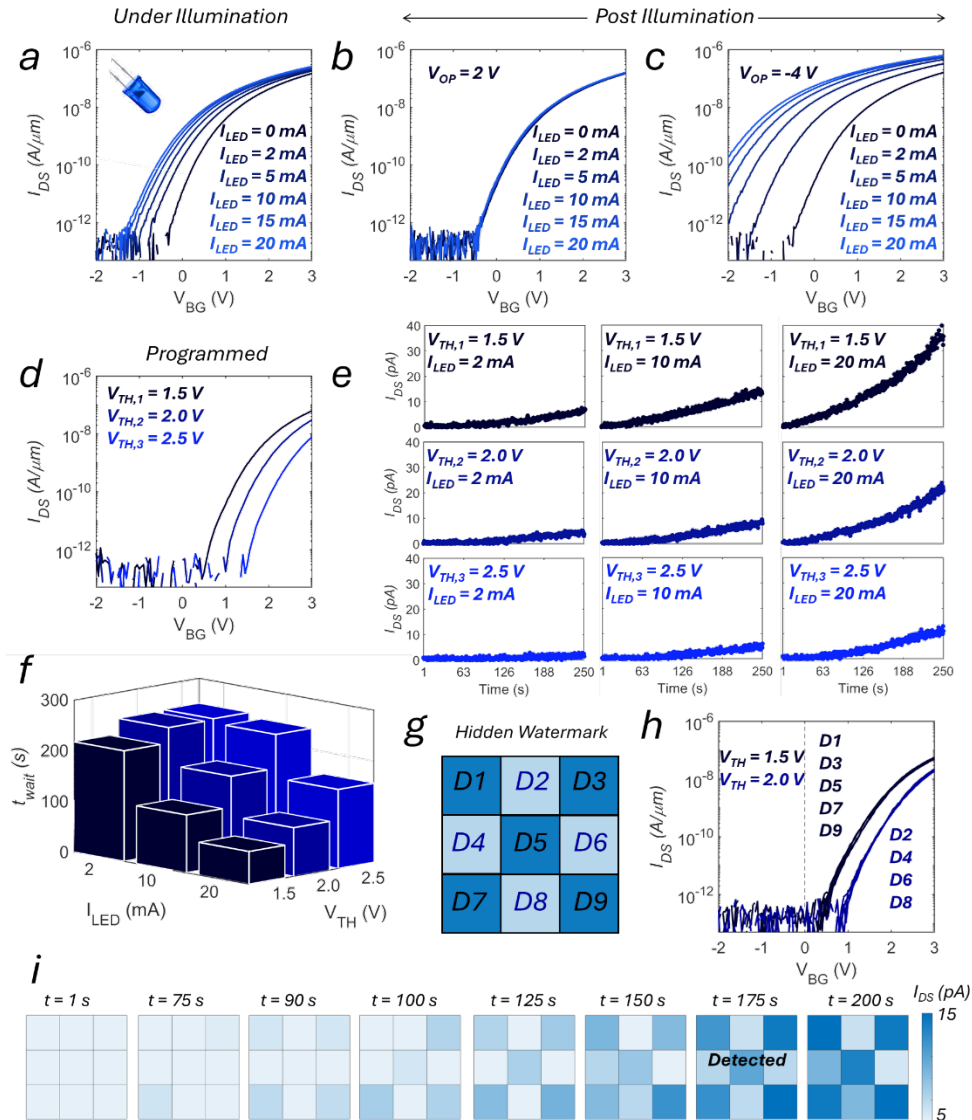


Figure 2-21: 2D memtransistor-based watermark: Transfer characteristics of a representative memtransistor measured a) under illumination and in dark after illumination in b) on-state ($V_{OP} = 2$ V) and c) off-state ($V_{OP} = -4$ V) with blue light emitting diode (LED) of different intensities (I_{LED}) for $t_{OP} = 10$ s. d) Transfer characteristics of MoS₂ memtransistor, electrically programmed

to obtain different V_{TH} . e) Temporal evolution of the photoresponse of the device measured at $V_{read} = 0$ V, under the illumination of a blue LED with different I_{LED} . Clearly, the wait time (t_{wait}) to observe finite photocurrent in the device i.e., $I_{DS} > I_{TH}$, where I_{TH} is a predefined threshold, increases with increasing V_{TH} and decreases with increasing I_{LED} . f) t_{wait} extracted for $I_{TH} = 5$ pA as a function of V_{TH} and I_{LED} . g) The phenomenon of gate-tunable persistent photoconductivity is used to hide a 3×3 digital watermark using 9 memtransistors. Each pixel corresponds to one device. h) Devices D1, D3, D5, D7, and D9 are programmed with $V_{TH} = 1.5$ V and devices D2, D4, D6, and D8 are programmed at $V_{TH} = 2$ V. Note that the initial current measured at $V_{read} = 0$ V for all devices are the same, hiding the watermark. i) Watermark is revealed after $t_{wait} \sim 175$ s by exposing the devices to blue illumination.

To design the watermark, first, we show that pre-illumination state of the device has profound impact on persistent photoconductivity. Figure 2-21d shows the transfer characteristics of the same memtransistor, electrically programmed to obtain different V_{TH} . Figure 2-21e shows the corresponding temporal evolution of the photoresponse of the device measured at $V_{read} = 0$ V, under the illumination of a blue LED with different I_{LED} . Clearly, the wait time (t_{wait}) to observe finite photocurrent in the device i.e., $I_{DS} > I_{TH}$, where I_{TH} is a predefined threshold, increases with increasing V_{TH} and decreases with increasing I_{LED} . Figure 2-21f shows t_{wait} extracted for $I_{TH} = 5$ pA as a function of V_{TH} and I_{LED} . We use this feature to hide a 3×3 digital watermark using 9 MoS₂ memtransistors as shown in Figure 2-21g. Each pixel corresponds to one device. Devices D1, D3, D5, D7, and D9 are programmed with $V_{TH} = 1.5$ V and devices D2, D4, D6, and D8 are programmed at $V_{TH} = 2$ V as shown in Figure 2-21h. During illumination, each device is measured at a gate voltage of $V_{BG} = V_{read} = 0$ V. Note that at $V_{read} = 0$ V, both set of devices are in the off state. As a result, the measured current at $V_{read} = 0$ V is the measurement noise floor which is in the range of $\sim$ pA. Hence, the watermark is not revealed through simple electrical measurements. Here we assume that the gate-terminal of these devices is made inaccessible to the end user restricting an attacker to measure the device transfer characteristics. However, when IP authentication is requested, the watermark can be revealed by illuminating the devices and measuring the I_{DS} by applying $V_{DS} = 1$ V as shown in Figure 2-21i. The watermark is revealed after $t_{wait} \sim 175$ s. Our watermark offers multiple layers of security:

1) the reverse engineer is unlikely to be aware of the use of persistent photoconductivity for the design of the watermark, 2) the watermark remains concealed even if electrical measurements are performed in dark, 3) each chip can be assigned a unique $N \times N$ watermark patterns with N being a large number, and 4) for any given watermark the V_{TH} values used can be different concealing the t_{wait} . Note that, it is also possible to create $N \times N$ analog watermarks by assigning different V_{TH} values to each of the N^2 devices.

Programmable 2D Circuit Camouflaging

Reverse engineering is another major security threat to the IC industry.^{107,157-160} Reverse engineers have been successful in extracting even device level details from an IC with very limited resources.¹⁶¹ For example, tri-gate technology used in Intel's 22nm Xeon processor was revealed by reverse engineers.¹⁶¹ Camouflaging is a hardware obfuscation technique that can hide the device/circuit functionality from reverse engineers.¹⁵⁷⁻¹⁶⁰ Inspired from nature, where animals camouflage to survive from predators or find preys, IC camouflaging make the devices/circuits look alike but differ in functionalities. State-of-the art camouflaging techniques involve fabrication of dummy contacts or alteration of channel doping to obfuscate the threshold voltage of the device.¹⁶²⁻¹⁶⁶ While there are many proposals for IC camouflaging, most schemes have been implemented and tested at the simulation level with limited experimental demonstrations. Here, we exploit electrical programmability of our MoS₂ memtransistors to obfuscate device and circuit level functionalities.

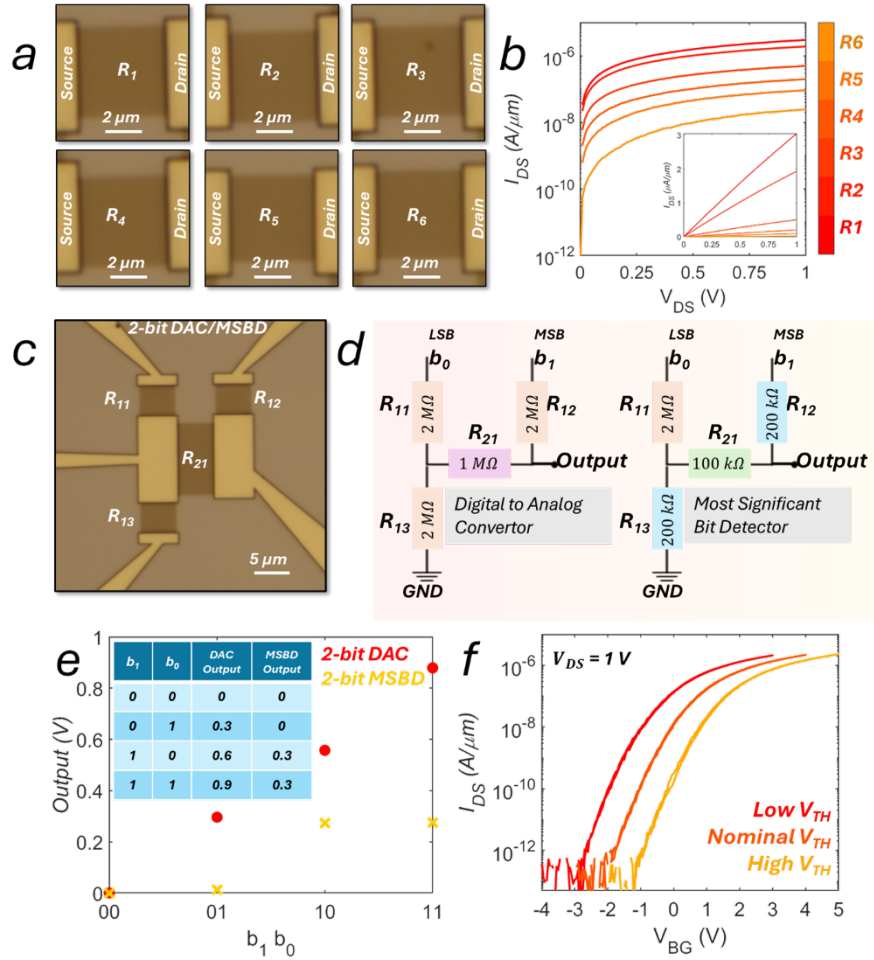


Figure 2-22: 2D memtransistor-based camouflaging: a) Optical images and b) corresponding I_{DS} versus V_{DS} characteristics of $N = 6$ monolayer MoS_2 -based resistors. In spite of visual similarity, the resistors differ by ~ 3 orders of magnitude in their resistance values since they are programmed accordingly, allowing their obfuscation from reverse engineers. c) Optical image and d) circuit schematic of a R-2R ladder digital to analog convertor (DAC) circuit for converting 2-bit digital input ($b_1 b_0$) into corresponding analog output (V_{out}) using camouflaged MoS_2 -based resistors. Also given alongside is a circuit schematic of a most-significant bit detector (MSBD) circuit. Note that the width of the horizontal resistor (R_{21}) is designed to be double compared to the width of the vertical resistors (R_{11} , R_{12} , and R_{13}) to make the circuit appear like a R-2R ladder, which can be used as a digital to analog converter (DAC). e) V_{out} obtained for different combinations of $b_1 b_0$ (00, 01, 10, 11). When the resistors are programmed such that $R_{11} = R_{12} = R_{13} = 2R_{21}$, the circuit functions like a DAC. However, when $R_{11} = 2\ \text{M}\Omega$, $R_{12} = R_{13} = 200\ \text{k}\Omega$, and $R_{21} = 100\ \text{k}\Omega$, V_{out} is high only when the most significant bit, i.e., $b_1 = 1$. In other words, the circuit behaves like a MSBD. This shows that camouflaged MoS_2 resistors can be used to successfully obfuscate analog circuit functionality. f) Low V_{TH} (LVT), nominal V_{TH} (NVT), and high V_{TH} (HVT) memtransistors based switches that can be used to camouflage a wide variety of logic gates. Although an attacker can easily identify a switch from the layout, the V_{TH} of the switch remains opaque, making the configuration secure.

Figure 2-22a shows the optical images of $N = 6$ monolayer MoS₂-based resistors and Figure 2-22b shows their corresponding I_{DS} versus V_{DS} characteristics. Although the resistors look visually identical, their resistance values differ by ~ 3 orders of magnitude since they are programmed accordingly using the back-gate terminal. These camouflaged resistors can serve as dummy contacts to obscure circuit functionalities. For example, Figure 2-22c-d, respectively, show the optical image and circuit schematic of a camouflaged R-2R ladder based digital to analog convertor (DAC) circuit (*left*) for converting 2-bit digital input (b_1b_0) into corresponding analog output (V_{out}). Figure 2-22d (right) shows the circuit schematic of a most significant bit detector (MSBD) which is very identical to the DAC circuit except with different set of resistance values. Note that the width of the horizontal resistor (R_{21}) is designed to be double compared to the width of the vertical resistors (R_{11} , R_{12} , and R_{13}) to make the circuit appear like a R-2R ladder, which can be used as a digital to analog converter (DAC). This is indeed true when $R_{11} = R_{12} = R_{13} = 2R_{21} = 2 \text{ M}\Omega$ as shown Figure 2-22e. Table inset in Figure 2-22e shows the output for a DAC circuit as well as the camouflaged MSBD circuit. V_{out} obtained for different combinations of b_1b_0 (00, 01, 10, 11) represents their analog equivalence.

However, when these resistors are programmed such that $R_{11} = 2 \text{ M}\Omega$, $R_{12} = R_{13} = 200 \text{ k}\Omega$, and $R_{21} = 100 \text{ k}\Omega$, V_{out} is high only when the most significant bit, *i.e.*, $b_1 = 1$. In other words, the circuit behaves as a most significant bit detector (MSBD). For this circuit, whenever the most significant bit is high, V_{out} is also high, else it is set to low. This shows that camouflaged MoS₂ resistors can be used to successfully obfuscate analog circuit functionality.

Programmable MoS₂ memtransistors can also serve as threshold voltage defined switch for digital circuit camouflaging. As shown in Figure 2-22f, MoS₂ memtransistor-based switches can be programmed in one of the three states, low V_{TH} (LVT), nominal V_{TH} (NVT), and high V_{TH} (HVT). The switch conducts when programmed at LVT and stops conducting when programmed

at HVT. When these LVT and HVT switches are used in conjunction with regular switch with NVT, it is possible to camouflage a wide variety of logic gates.¹⁶⁷ Although an attacker can easily identify a switch from the layout, the V_{TH} of the switch remains opaque, making the configuration secure.

Computing for the Next Decade

While novel computing paradigms like non-von Neumann architectures and neuromorphic computing offer intriguing prospects for overcoming the limitations of traditional von Neumann systems, the immediate priority for the semiconductor industry remains the relentless pursuit of performance and energy efficiency improvements through continued transistor scaling and innovation. Despite the significant advancements in transistor architecture and fabrication processes, the industry is rapidly approaching the fundamental limits of scaling imposed by the physical properties of conventional Si. As transistor dimensions shrink into the sub-nanometer regime, issues such as excessive leakage currents, short-channel effects, and resistivity limitations become increasingly pronounced, hindering further performance and power efficiency gains.

Consequently, the development of promising new channel materials has emerged as a critical imperative for sustaining the historical cadence of logic node advancement and enabling the next generation of high-performance computing systems. While the exploration of non-traditional computing techniques continues to push the boundaries of what is possible, the immediate focus of the semiconductor industry remains firmly fixed on the development of the advanced logic nodes through the exploration of alternative materials and their integration into high-performance, energy-efficient logic. This focus is driven by the pressing need to overcome

the impending limitations and meet the demands of the ever-growing computational needs of modern applications.

In the subsequent sections, the current state of 2D and 1D material-based logic transistors, highlighting the progress made, the challenges faced, and the potential solutions being explored to realize their promise will be discussed.

Key Requirements for Advanced Logic

Semiconductor production is devoted to digital logic that satisfies requirements for two major device types, namely, a) high-performance (HP), and b) high-density (HD)/low-power logic. More Moore technology roadmap from The International Roadmap for Devices and Systems (IRDS) sets technology targets with device design and performance specifications. Several considerations in terms of speed, performance, density, cost, and readiness level are assessed in the report from year to year. This helps engineers and scientists design devices that can keep up with historical trends at reduced cost and power while packaging more denser components. These requirements are driven by the demands for computational performance, energy efficiency, and functional density across a wide range of applications, from high-performance computing (HPC) and data centers to mobile and Internet of Things (IoT) devices.

To maintain performance at reduced voltages, past scaling efforts have concentrated on supplementary enhancements, including the incorporation of strain in the channel, the application of stress boosters, the adoption of high-k metal gates, the reduction of contact resistance, and the optimization of electrostatics. These measures aim to offset the diminution in gate drive as the supply voltage decreases, a crucial adjustment for the demands of high-performance mobile applications. Although FinFET device architecture has especially helped keep up with the roadmap through improved electrostatics and fin depopulation (increasing fin height to reduce

number of fins), the reduction of parasitics will continue to be the dominating knob for performance improvement as the device structure progresses towards gate-all-around (GAA) also referred to as lateral nanosheet, and furthermore towards complementary stacked nanosheet (CFET) geometry.^{42,62,69,168}

As device architectures undergo transformation, associated modules are anticipated to adapt accordingly. This evolution could involve a shift in channel materials from Si to alternatives such as SiGe, Ge, 2D TMD materials, and carbon nanotubes (CNT). Similarly, the contact module may transition from silicides to innovative materials that offer reduced Schottky barrier heights (SBH), alongside the adoption of wrap-around contact integration approaches to expand the contact surface area. As predicted in the IRDS report, a transition to GAA architecture is already underway, with leading foundries incorporating the best of the GAA device architecture to meet their customer demands. What has brought us to this ultimate GAA switch is the limitation in the fin width scaling among many other challenges in power and area scaling. All-in-all, the GAA adoption is much more complicated.¹⁶⁹ On the flip side, the reintroduction of effective width as a knob has eased the complexity for analog circuit designers, although it is unlikely foundries will allow this variable since implementing device models for processing of a single device structure is already extremely challenging.¹⁷⁰ Projected device architectures will provide fully-depleted and fully-inverted (volume inversion) channels. Complementary FETs (CFETs) where lateral GAA FETs will evolve with increase NS stacking count and reduce proximity of p-type and n-type channels, finally being stacked on top of each other and further reducing device cell footprint.¹⁷¹

High-mobility channel requirement will remain a driving factor. Although materials like Ge and III-V show tremendous promise, the benefits of high drive current with gate scaling seem limited due to velocity saturation. However, further scaling in gate length results in ballistic transport which increases injection velocity due to reduced effective mass and therefore results in

higher drive current. This although comes at the cost of increased leakage since a low carrier effective mass can lead to tunneling across source and drain, thereby leading to higher static power dissipation. While a rigorous analysis of the device parameters will be necessary to enjoy the benefits of alternative high mobility materials, theoretical predictions suggest degradation in mobility from thinning down of channel in beyond GAA structures for enhanced electrostatics. TMD materials that are inherently thin and less prone to surface scattering effects are predicted to maintain high mobility with very high carrier effective mass, thereby proving ideal for low-power logic. To meet high-performance demands, 1D CNTs as channel materials also provide some potential owing to their relatively small bandgap, and cylindrical structure.

With the progression of technology scaling, the **parasitic capacitance** between the gate and source/drain terminals of the device is expected to rise. This aspect becomes increasingly critical, surpassing the impact of channel capacitance loading, especially within the standard cell context. The effect is further amplified in GAA structures due to the unutilized space between stacked devices. Emphasis should be placed on developing low- κ spacer materials and potentially even air spacers, which must maintain high reliability and etch selectivity for source/drain (S/D) contact formation. **Current drive per footprint** is another key metric that will be set to achieve high performance goals as stacking NS with GAA structures reduces overall footprint. Parasitic capacitance and series resistance will need to be tackled simultaneously. One of the obvious routes to increasing current drive will be to improve **channel electrostatics**. Equivalent oxide thickness scaling, interface trap density reduction are possible routes for conventional materials.

Alternatively, 2D TMD materials and 1D CNTs offer the benefit of a fully interfacial device, once again due to their extremely thin/cylindrical nature. Interface trap density reduction is an ongoing challenge due to the absence of an ideal and scalable dielectric integration with TMDs. In conventional Si technology, the distance between individual stacked devices is required to be minimized while keeping space for dielectric and threshold-determining gate metal so as to

minimize parasitics between gate and source/drain contacts. However, threshold-determining factors for 2D TMDs/1D CNTs are yet to be fully understood. Other sources of **leakage current** such as punch through (source to drain leakage from under the channel) are minimized with 2D TMD materials due to their large carrier effective mass and isolated structure. Leakage source/drain tunneling currents, although much higher in 1D CNT, the requirements for their application in HP devices are much more relaxed. **Process and material variations** in conventional Si technology leading to threshold and drive current variations are more issues that will need to be tackled and their root cause being channel doping, surface roughness, channel thickness variations will need further optimization. This problem too has necessitated the need for undoped channel materials and an improvement in epitaxial growth as well as deposition techniques. In order to maintain high electrostatics and mobility in the proposed 2D TMD and 1D CNT materials, passivation techniques will be necessary that do not introduce any further variations.

In the Table 1-1, Electrical Performance Targets such as the key electrical targets for future nodes will be first identified from the IRDS report.^{172,173}

Electrical Performance Targets

Table 1-1: Electrical Performance Targets from Future Technology Nodes (Sourced from IRDS)

Year of Production	2025	2028	2031
Node Label	"2 nm"	"1.5 nm"	"1.0 nm"
3D Integration Scheme	Stacking	Stacking	3DVLSI
Logic Device Structure	Lateral GAA	Lateral GAA CFET-SRAM	Lateral GAA (3D) CFET-SRAM-3D
LOGIC DEVICE ELECTRICAL SPECS			
Power Supply Voltage - Vdd (V)	0.65	0.65	0.60
Subthreshold slope (mV/dec) - HP (mV/dec)	72	70	70
Subthreshold slope (mV/dec) - HD (mV/dec)	67	67	65
V _{t,sat} at I _{off} =10nA/um - HP (mV)	165	165	164
V _{t,sat} (mV) at I _{off} =100pA/um - HD (mV)	271	268	268
Effective mobility (cm ² /V.s)	100	80	60
R _{sd} (Ohms.um)	257	245	232
Ballisticity.Injection velocity (cm/s)	9.00E+06	9.00E+06	9.00E+06
V _{dsat} (V) - HP	0.101	0.108	0.144

<i>V_{dsat} (V) - HD</i>	0.101	0.108	0.144
<i>I_{on} (uA/um) at I_{off}=10nA/um - HP</i>	787	851	753
<i>I_{on} (uA/device) at I_{off}=10nA/um - HP</i>	170	184	157
<i>I_{on} (uA/um) at I_{off}=100pA/um - HD</i>	602	656	551
<i>I_{on} (uA/device) at I_{off}=100pA/um - HD</i>	130	142	115

Shifting the focus from solely pursuing far-reaching unconventional computing techniques to addressing the foundational challenges in 2D TMD materials provides a balanced, risk-mitigated, and immediately impactful approach to advancing technology nodes for the future. While the allure of groundbreaking computing paradigms is undeniable, the semiconductor industry must ensure that it continues to invest in the material science breakthroughs that underpin all electronic devices. This strategy ensures continuous improvement in technology capabilities and readiness for future innovations. Thus, transitioning from the broader technological needs and advancements in computing, sensing and security, it is clear that the development of advanced semiconductor materials is crucial. While significant progress has been made in the development of n-type FETs using 2D TMDs, the development of p-type FETs has lagged behind.^{90,91,123,174-179} This imbalance limits the full potential of complementary logic circuits using novel materials, which we saw earlier, require both n-type and p-type devices to function optimally.¹⁸⁰

Chapter 3

Engineering p-Type Contacts to 2D TMD Channels

*Part of this chapter has been reproduced from: **Toward High-Performance p-Type Two-Dimensional Field Effect Transistors: Contact Engineering, Scaling, and Doping.** Aaryan Oberoi, Ying Han, Sergei P. Stepanoff, Andrew Pannone, Yongwen Sun, Yu-Chuan Lin, Chen Chen, Jeffrey R. Shallenberger, Da Zhou, Mauricio Terrones, Joan M. Redwing, Joshua A. Robinson, Douglas E. Wolfe, Yang Yang, and Saptarshi Das, *ACS Nano* **2023** 17 (20), 19709-19723, DOI: 10.1021/acsnano.3c03060*

n-Type field effect transistors (FETs) based on two-dimensional (2D) transition metal dichalcogenides (TMDs) like MoS₂ and WS₂ have come closer to meeting the requirements set forth in International Roadmap for Devices and Systems (IRDS).^{142,174,175,178,181,182} However, *p*-type 2D FETs are dramatically lagging behind in meeting performance standards. Here, we investigate an approach to contact engineering and channel length (L_{ch}) scaling to achieve high-performance *p*-type FETs based on synthetic WSe₂. Using electrical measurements backed by atomistic imaging and rigorous analysis, Pd was identified as the favorable contact metal for WSe₂ owing to better epitaxy, larger grain size, and higher compressive strain leading to lower Schottky barrier height. While the ON-state performance of Pd-contacted WSe₂ FETs were improved by $\sim 10\times$ by aggressively scaling L_{ch} from 1 μm down to ~ 20 nm, ultra-scaled FETs were found to be contact limited with contact resistance extracted to be 40 k Ω μm . To reduce the contact resistance further, the introduction of a high-work function Selenium (Se) buffer layer is explored as a means to rectify anionic vacancies and safeguard the TMD layers during processing, which markedly enhances fabrication yield and reduces performance variability. This

study innovates by incorporating a Pd-Se contact mixture formation as a lower resistance p-type contact with median contact resistance measured down to 17 k Ω μ m.

Work-function Engineering to Achieve p-Type Electrical Contacts

The absence of *p*-type transport in 2D TMDs can be ascribed to the phenomenon of Fermi level pinning (FLP) at the metal/semiconductor (MS) junction resulting in large Schottky barrier (SB) heights for hole injection into the valence band (E_V).¹⁸³ For MoS₂, the FLP is near the conduction band (E_C),⁹⁰ whereas for WSe₂ the FLP is near the middle of the bandgap¹⁸⁴ as shown in Figure 3-1a-b, respectively.¹⁸⁵ While low work function metals such as Sc, Bi, etc. can give rise to small SB height for electron injection (ϕ_{SB-N}) leading to high-performance *n*-type 2D FETs,^{90,122} the SB height for hole injection ($\phi_{SB-P} = E_G - \phi_{SB-N}$) is large enough to prevent adequate hole injection even when high work function metals such as Ni, Pd, Pt, etc. are used for MoS₂ FETs. For monolayer MoS₂, this situation is aggravated owing to larger E_G of ~ 1.8 eV compared to multilayer flakes with $E_G \sim 1.2$ eV. Therefore, it is not surprising that there has been no report of hole conduction in large area grown monolayer MoS₂. In contrast, midgap FLP in WSe₂ makes the hole injection relatively easier although at the cost of severe loss in the ON-state performance (I_{ON}) since tunneling injection through the SB is less efficient compared to Ohmic injection.¹⁸⁶ Therefore, while WSe₂ is a better choice for *p*-type 2D FETs, the MS interface for WSe₂ must be improved, i.e., R_C must be significantly reduced to achieve high-performance.

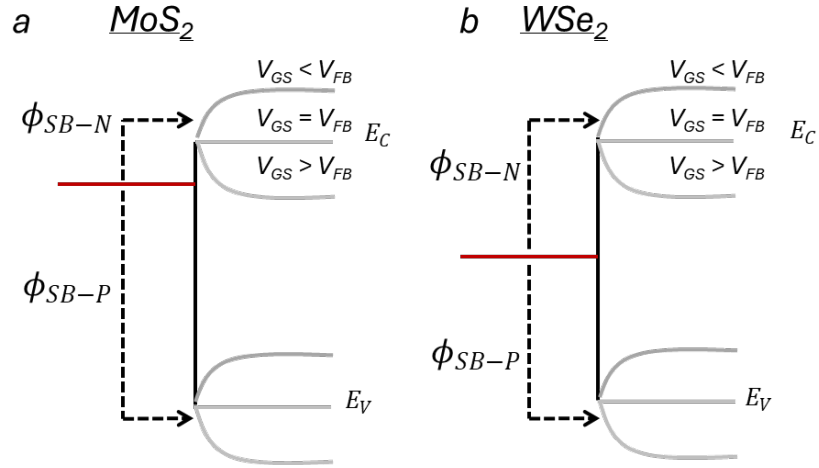


Figure 3-1: Fermi-level pinning (FLP) in MoS_2 and WSe_2 : a) For monolayer MoS_2 , the FLP is closer to the conduction band (E_C) irrespective of the metal work function, resulting in a tall Schottky barrier (ϕ_{SB-P}) to hole injection. This makes hole injection difficult and hence development of p-type FETs on MoS_2 is extremely challenging. b) For WSe_2 , the situation is more relaxed and FLP is closer to the middle of the bandgap with most metals. This results in a lower ϕ_{SB-P} , thereby facilitating hole injection. Although, presence of ϕ_{SB-P} still limits the ON-state performance due to high contact resistance, WSe_2 provides as a favorable choice for p-type 2D FETs.

Recent studies have suggested that beyond MIGS, the MS interface can be significantly impacted by the fabrication technique used for the contact deposition. For example, by avoiding radiative heating of the substrate during metal evaporation and by optimizing the deposition conditions, Wang *et al.* were able to achieve damage-free van der Waals (vdW) contact between exfoliated WSe_2 and high work function metals such as Pd and Pt.¹⁸⁷ They were also able to realize p-type WSe_2 FETs with R_C of $3.3 \text{ k}\Omega \mu\text{m}$, and saturation currents in excess of $10 \mu\text{A}/\mu\text{m}$. In another report, Kwon *et al.*¹⁸⁸ used a selenium buffer layer to achieve interaction- and defect-free vdW contacts between a range of metals and exfoliated 2D TMDs reinstating the Schottky–Mott rule with a near ideal FLP factor of ~ 0.9 . Using this approach, they also demonstrated p-type WSe_2 FETs with vdW Au contacts exhibiting R_C of $1.25 \text{ k}\Omega \mu\text{m}$. Another report suggested the use of Ru contacts and reported high ON currents up to $50 \mu\text{A}/\mu\text{m}$, low OFF currents.¹⁸² However, Ru itself is unstable and may be difficult to reproduce. Another report performed self-aligned doping using the O_2 -doping process technique and demonstrated high-performance p-type

FETs.¹⁷⁶ Transferred printing of pre-deposited contacts is yet another approach that can preserve the vdW interface between the metal and the 2D materials and eliminate doping, strain and interfacial roughness compared with evaporated metal contacts.¹⁸⁹ For example, Liu *et al.*¹⁹⁰ demonstrated R_C of $5 \text{ k}\Omega \mu\text{m}$ for p -type FETs made using exfoliated and ultra-clean WSe₂ monolayers based on transferred metal contacts embedded within h-BN. Similar approach was adopted by Kong *et al.*¹⁹¹ to demonstrate doping-free complementary WSe₂ FETs with Au contacts. In a more recent study, vdW epitaxy and random crack formation were exploited to achieve vdW contact between large area grown metallic VSe₂ and semiconducting bilayer WSe₂.¹⁹² By using this process, a 20-nm-long and 1.3-nm-thick p -type FET was fabricated with record low- R_C of $0.50 \text{ k}\Omega \mu\text{m}$ and record high ON-state current of $1.72 \text{ mA}/\mu\text{m}$. Note that vdW contacts have also been realized for MoS₂,^{189,193} however, p -type FETs with acceptable performance have only been demonstrated for WSe₂, highlighting the importance of developing this material for future technology nodes. Furthermore, since most of the above-mentioned studies are based on exfoliated and single-crystal WSe₂ flakes, it is important to realize high-quality synthetic WSe₂ and implement the fundamental insights gained from the previous studies to achieve high-performance p -type 2D FETs. In addition, the impact of aggressive channel length scaling must be investigated and strategies for high-performance operation must be developed.

To identify the appropriate contact metal, bilayer WSe₂ FETs were fabricated using high work function metals such as Ni, Pd, and Pt as the source/drain contact electrodes. However, metal work function is not the only factor that determines the performance p -type FETs. Instead, as discussed earlier, metallization induced damage, interfacial epitaxy, strain etc. can play a more critical role in achieving high-performance p -type FETs.^{187,194} Therefore, it is important to optimize the metal evaporation conditions to reduce deposition-induced damage and maintain as clean an interface as possible between various metals and WSe₂. For our study, all metals were

deposited using electron beam (e-beam) evaporation with the evaporation rate initialized to 0.5 Å/s to lower the kinetic impact of the metal atom on to the TMD interface and to allow longer time for metal atom to settle after being evaporated from the crucible. TEM and STEM experiments were performed to characterize the averaged grain sizes and epitaxy quality of the metals deposited on the WSe₂, as well as the resultant in-plane elastic strain on the WSe₂. Figure 3-2a shows STEM-HAADF images for the bilayer WSe₂ films with 5 nm of Ni, Pd, and Pt contacts viewed down the c-axis. It is clearly seen that all the metal films are nanocrystalline, while the morphology and grain size differ significantly in different metals. Figure 3-2b shows the average grain size for Ni, Pd, and Pt. It is interesting to note that Ni has the smallest average grain size despite its lower boiling point. Metal grain size and grain orientation can play an important role in determining the specific contact resistivity of MS interfaces as larger grain sizes can minimize carrier scattering at the grain boundaries and vary metal work function.^{195,196} Therefore, the increased grain size on the Pd will enable a lower electrical resistivity and better contact performance.

Figure 3-2c shows the SAED patterns for Ni-, Pd-, and Pt-coated WSe₂ film, where we found that the [001] direction of the WSe₂ is always parallel to the [111] zone axis of Ni, Pd, and Pt. Figure 3-2d shows single crystal simulation of the SAED patterns of the Ni-, Pd-, and Pt-coated WSe₂ film, with the metal and the WSe₂ on the [111] and [001] zone axes, respectively. In addition, the $\{1\bar{2}0\}$ planes of WSe₂ are aligned such that they are parallel with the $\{2\bar{2}0\}$ planes of the Ni, Pd or Pt. The significant matching between Figure 3-2c and Figure 3-2d implies that the grains of the metal films are highly textured, and there exists an epitaxy correlation between the deposited metal and the WSe₂. Figure 3-2e shows the SAED patterns after the transformation from the Cartesian coordinate to the polar coordinate system. In these special plots, the diffraction disks within the same plane family will align on the same vertical line, while the parallel planes will align on the same horizontal line. Figure 3-2f shows the enlarged view of the boxed regions

in Figure 3-2e, showing that the $\{1\bar{2}0\}$ planes of WSe_2 are indeed parallel with the $\{2\bar{2}0\}$ planes of the metal as their corresponding diffraction peaks are aligned on the same horizontal lines. To quantitatively compare the epitaxy quality of different metals on WSe_2 , we performed a series of fitting on the white-dash vertical lines in Figure 3-2e, to get the averaged full-width at half maximum (FWHM) for the $\{2\bar{2}0\}$ peaks of metal. The FWHM represents the angular spread of the $\{2\bar{2}0\}$ peaks. The higher the FWHM, the lower the epitaxy quality. The comparison results are summarized in Figure 3-2g, showing Pt manifests the best epitaxy quality and the Ni the worst. In all cases, the FWHM is small, indicating that most of the grain boundaries in the metal films are small angle grain boundaries.

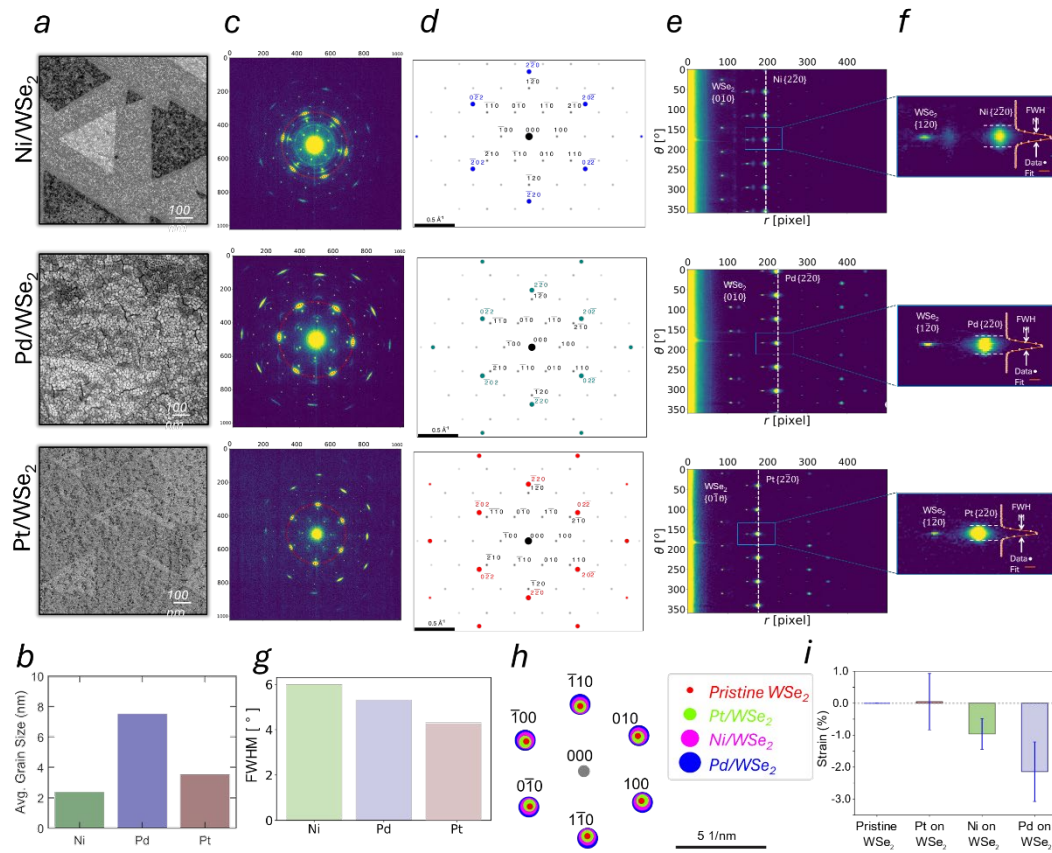


Figure 3-2: TEM characterization of the grain size, epitaxy, and strain at metal/ WSe_2 contact interfaces: a) STEM-HAADF images for the bilayer WSe_2 films with 5 nm of Ni, Pd, and Pt contacts viewed down the c-axis. b) Average grain size for Ni, Pd, and Pt. c) SAED for Ni-, Pd-,

and Pt-coated WSe₂ film, where WSe₂ is on [001] and Ni, Pd, and Pt are on [111] zone axes, respectively. Elliptical fitting is performed to correct the stigmatism in diffraction. d) Single crystal simulation of the SAED of the Ni-, Pd-, and Pt-coated WSe₂ film. e) SAED after the transformation from the Cartesian coordinate to the polar coordinate system. Note that the diffraction disks within the same plane family will align on the same vertical line. f) Enlarged view of the boxed regions in (e). The Inset shows the fitting of the FWHM for the Ni (220), Pd (220) and Pt (220) peaks. g) Comparison of the averaged FWHM for, Ni-, Pd-, and Pt-coated WSe₂. h) Overlay of the first order diffraction spots for pristine and Ni-, Pd-, and Pt-coated WSe₂, where the off-centering clearly indicates the magnitude of strain in the samples. i) The averaged in-plane hydrostatic strain for Ni, Pd, and Pt-coated WSe₂ measured from the SAED patterns. The strain is tensile if it is positive.

In addition to the epitaxy quality, we analyzed the in-plane strain based on the SAED patterns with a [001] zone axis. Figure 3-2h shows the overlay of the first order diffraction spots for pristine and Ni-, Pd-, and Pt-coated WSe₂, where the off-centering clearly indicates the magnitude of strain in the samples. The averaged in-plane hydrostatic strain caused by different metals are compared in Figure 3-2i, showing that the strain is small tensile for Pt, medium compressive for Ni and large compressive for Pd. A complementary strain analysis for Pd based on the HRTEM images is provided in Figure 3-3. Note that strain can tune the electronic band structure of WSe₂ and thereby influence the carrier transport underneath the contacts.¹⁹⁷⁻²⁰¹ For example, using *ab initio* density functional theory, Kumar, *et al.*¹⁹⁷ predicted that the bandgap of bilayer TMDCs can be reduced by applying mechanical strains and tuning interlayer distance. Later Nayak, *et al.*²⁰¹ have experimentally demonstrated monotonic bandgap reduction resulting in semiconductor-to-metal transition in multilayer MoS₂ subjected to out-of-plane uniaxial stress of ~20 Gpa. Strain can also influence carrier mobility, MS interfacial properties such as MIGS, and the SB height, all of which can impact R_c and hence the FET performance. As we will elucidate next, using transport measurements, FET performance is the superposition of many factors that influence the MS interface including metal work function, metal epitaxy, metal-induced strain, etc.

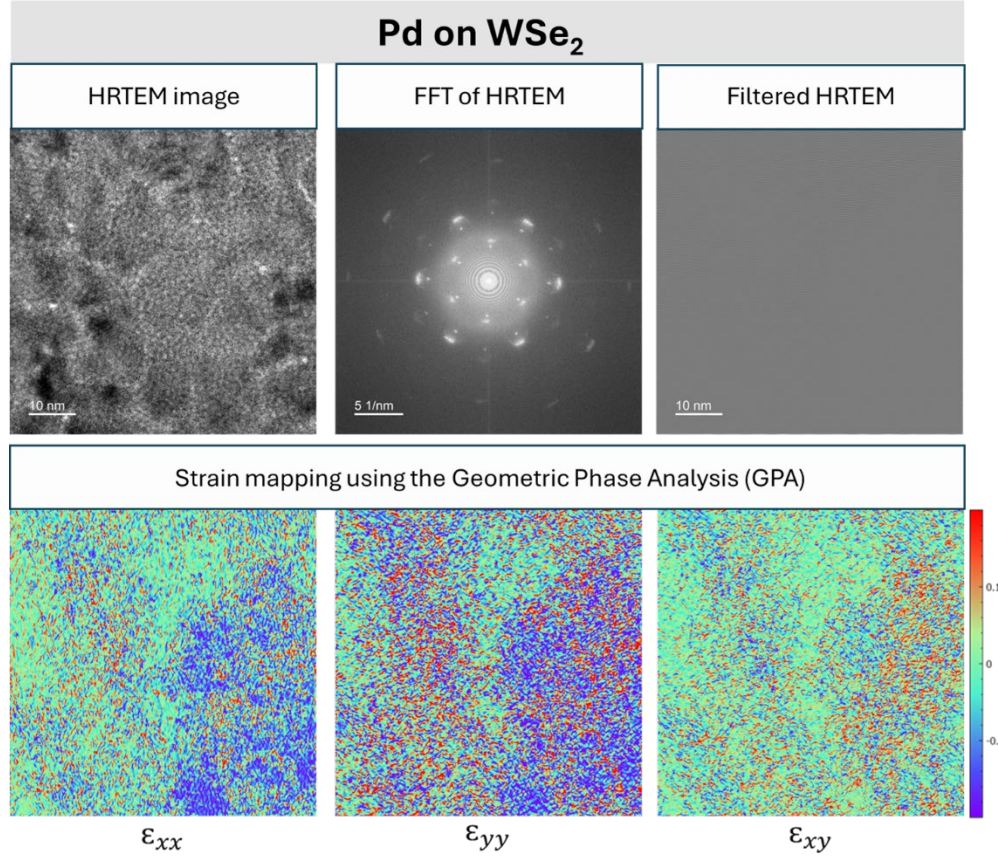


Figure 3-3: Strain map for Pd on WSe₂: The fast Fourier transform (FFT) of the HRTEM image was performed, showing the structural information in the reciprocal space. The following inverse-FFT of the characteristic peaks for WSe₂ enabled the formation of a filtered HRTEM image showing only the lattice fringes WSe₂. Strain mapping using the geometric phase analysis (GPA) was performed based on filtered HRTEM image to reveal the in-plane normal strain in x direction ϵ_{xx} , normal strain in y direction ϵ_{yy} , and the shear strain ϵ_{xy} , respectively.

Figure 3-4a-c show the transfer characteristics, i.e., source-to-drain current (I_{DS}) while sweeping V_{BG} for $V_{DS} = 1$ V for ~20-50 bilayer WSe₂ FETs with Ni, Pd, and Pt as the source/drain metal contacts, respectively. The L_{ch} for all of these devices were 1 μm . For each contact metal type, the best performing device, i.e., the device with highest p -branch ON currents ($I_{DS,P}$) measured at $V_{BG} = -5$ V is marked in bold while the other devices are shaded. Figure 3-4d-h, respectively, show box plots for $I_{DS,P}$ measured at $V_{BG} = -5$ V, field-effect hole mobility ($\mu_{FE,P}$) extracted from peak-transconductance, threshold voltage, $V_{TH,P}$, extracted at an iso-current of 1 nA/ μm , subthreshold slope (SS_P) extracted over two orders of magnitude change in I_{DS} , and the

extracted SB heights (ϕ_{SB-P}) for hole injection for the Ni, Pd, and Pt contacted bilayer WSe₂ FETs. The upper and lower arms of the rectangular boxes denote the 75th and 25th percentiles, respectively. Maximum and minimum values for the distribution are spanned by the line limits. Some key observations can be made from these results. Ni contacted devices show lower median *p*-branch ON currents ($I_{DS,P,median}$) of ~ 6.3 nA/ μ m, more negative median threshold voltage ($V_{TH,P,median}$) of ~ -1.4 V, higher median subthreshold slope ($SS_{P,median}$) of ~ 1.2 V/decade, and lower median field-effect hole mobility ($\mu_{FE,P,median}$) of ~ 0.008 cm²V⁻¹s⁻¹. The relatively poor performance of Ni-contacted bilayer WSe₂ FETs can be primarily attributed to larger $\phi_{SB-P,median}$ of ~ 0.68 eV for the Ni contacts compared to ~ 0.42 eV and ~ 0.49 eV for Pd and Pt contacts, respectively. This is expected since Ni has slightly lower work function (5.04 – 5.35 eV) compared to Pd (5.2 – 5.6 eV) and Pt (5.1 – 5.9 eV). Also note that the Fermi level of Ni pins near the middle of the bandgap of WSe₂, which is evident from more ambipolar transfer characteristics observed for Ni in comparison to Pd and Pt. The higher device-to-device variation among Ni contacted WSe₂ FETs is likely related to relatively poorer epitaxy between Ni and WSe₂ as evident from Figure 3-4e.

Interestingly, Pd and Pt have very similar work functions as well as very similar epitaxy as shown in Figure 3-4e, however, Pd-contacted devices clearly outperforms Pt-contacted devices with better $I_{DS,P,median}$ of ~ 55 nA/ μ m, more positive $V_{TH,P,median}$ of ~ -0.07 V, more consistent SS_P , higher $\mu_{FE,P,median}$ of 0.22 cm²V⁻¹s⁻¹, and lower $\phi_{SB-P,median}$ of ~ 0.42 eV. This clearly indicates that the higher compressive strain induced by Pd contact as shown in Figure 3-4g may play an important role in determining the FET performance. As mentioned earlier, higher strain can lead to an increase in carrier mobility in WSe₂ underneath the contacts as well as reduction in the SB height.²⁰² Both can contribute to reduction in R_C and hence higher overall performance as observed from the transport experiments. Figure 3-4i shows a qualitative comparison using a

spider plot for Ni/WSe₂, Pd/WSe₂, and Pt/WSe₂ contact interfaces accounting for the metal work function, grain size, epitaxy, metal-induced compressive strain, resulting SB height, and FET performance captured through $I_{DS,P}$. It is clear that a single microscopic factor alone is insufficient to determine the optimal MS interface. Instead, contact quality and FET performance is a superposition of many factors, which necessitates a comprehensive investigation presented in this work. Based on rigorous analysis of atomistic images, diffraction patterns, and transport measurements, it can be stated that the higher work function of Pd in conjunction with better epitaxy, larger grain size, and higher metal induced compressive strain can lead to lower SB height and optimal performance for WSe₂ *p*-type FETs. The “champion” Pd-contacted WSe₂ device could achieve an $I_{DS,P}$ of ~ 440 nA/ μm for $n_s \sim 1.4 \times 10^{13} \text{ cm}^{-2}$ and $V_{DS} = 1$ V. In the following section, we will scale L_{ch} from 1 μm down to 20 nm for Pd-contacted WSe₂ FETs to boost their performance.

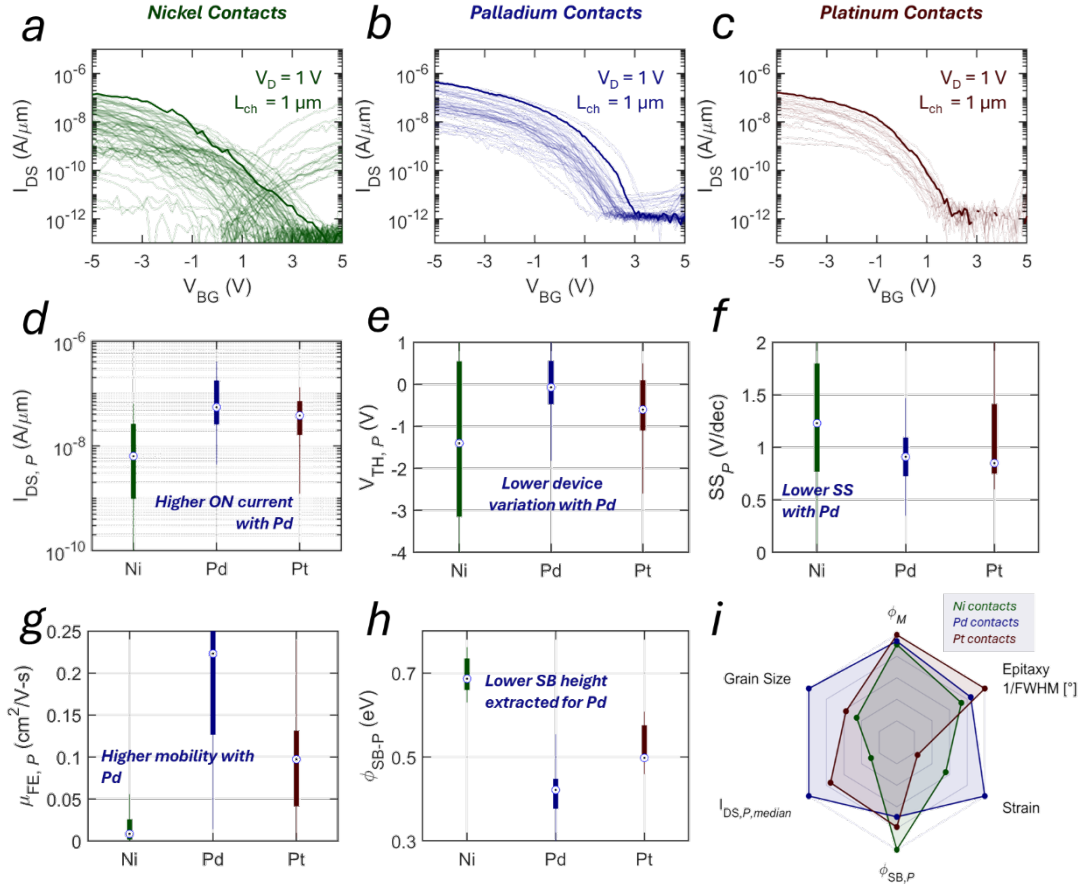


Figure 3-4: Contact engineering for WSe₂ FETs: Transfer characteristics, i.e., source-to-drain current (I_{DS}) while sweeping V_{BG} for $V_{DS} = 1$ V for ~20-50 bilayer WSe₂ FETs with a) Ni, b) Pd, and c) Pt as the source/drain metal contacts. The L_{ch} for all devices were 1 μ m. For each contact metal type, the best performing device, i.e., the device with highest p-branch ON currents ($I_{DS,P}$) measured at $V_{BG} = -5$ V is marked in bold while the other devices are shaded. Box plots for d) $I_{DS,P}$ measured at $V_{BG} = -5$ V, e) field-effect hole mobility ($\mu_{FE,P}$) extracted from peak-transconductance, f) threshold voltage, $V_{TH,P}$, extracted at an iso-current of 1 nA/ μ m, g) subthreshold slope (SS_P) extracted over two orders of magnitude change in $I_{DS,P}$, h) the extracted SB heights (ϕ_{SB-P}) for hole injection for the Ni, Pd, and Pt contacted bilayer WSe₂ FETs. The upper and lower arms of the rectangular boxes denote the 75th and 25th percentiles, respectively. Maximum and minimum values for the distribution are spanned by the line limits. i) Comprehensive and qualitative analysis of Ni, Pd, and Pt with WSe₂ denoted using a spider plot, showing Pd to cover the largest area. This highlights that contact engineering is a rather superposition of multiple factors, all of which are investigated here.

Contact Limited at Aggressively Scaled Channel Lengths

Channel length scaling is one of the most obvious ways to enhance the performance of WSe₂ FETs. We have developed a two-step nanolithography process as described in the **Appendix** section to fabricate aggressively scaled WSe₂ FETs with L_{ch} down to 20 nm. Figure 3-5a-b show representative SEM images and corresponding transfer characteristics of several WSe₂ FETs measured at $V_D = 1$ V with $L_{ch} = 1$ μ m, 100 nm, 50 nm, and 20 nm respectively. Figure 3-5c shows the box plot for $I_{DS,P}$ measured at $V_{BG} = -7$ V for different L_{ch} . Note that, as expected, $I_{DS,P,median}$ reaches ~ 670 nA/ μ m at $L_{ch} = 100$ nm which is $\sim 7\times$ increase from ~ 90 nA/ μ m at $L_{ch} = 1$ μ m. However, $I_{DS,P,median}$ increases to ~ 900 nA/ μ m when L_{ch} is further scaled down to 20 nm, i.e., five-fold reduction in physical length yields only $\sim 1.3\times$ improvement in the ON state performance, suggesting that Pd-contacted WSe₂ FETs are limited by R_C . Similar results have also been reported for contact-limited *n*-type MoS₂ FETs at ultra-scaled channel lengths.^{203,204} Figure 3-5d shows the total resistance, R_T , extracted for $n_s = 10^{13}$ cm⁻², as a function of L_{ch} . R_T follows the expected trend and plateaus for $L_{ch} < 100$ nm. Using the traditional linear extrapolation method, R_C is extracted to be 365 k $\Omega\mu$ m. Dependence of R_C on n_s is shown in Figure 3-5e. The observed monotonic decrease in R_C with increasing n_s can be attributed to the electrostatic thinning of the SB tunneling distance (λ_{SB}). We would like to remind the reader that λ_{SB} is determined by the smaller of the two band-bending lengths, the screening length (λ_{scr}) arising from the gate electrostatics as given by **Eq. 1a**, and the width of the depletion region at the MS interface (W_D), which depends on the semiconductor doping (N_D) (**Eq. 1b**).

$$\lambda_{scr} = \sqrt{t_{ox} t_{body} \epsilon_{ox} / \epsilon_{body}} \quad [1a]; \quad W_D \approx \sqrt{2 \epsilon_{body} \phi_{SB-P} / q N_D} \quad [1b]$$

In Eq. 1, ϵ_{ox} and t_{ox} are, respectively, the permittivity and thickness of the gate dielectric, and ϵ_{body} is the permittivity of the semiconducting channel. The semiconductor

industry has mostly relied on scaling W_D to reduce R_C through degenerate doping of Si underneath the contacts since FLP occurs for metal-silicide junctions as well.²⁰⁵ Additionally, the silicon channel underneath the contacts is deprived of electrostatic gate control in conventional top-gated device geometry (Figure 3-6a). However, in the absence of degenerate doping of TMDs, the 2D community has primarily exploited the back-gated device geometry to reduce R_C through electrostatic thinning of λ_{SB} (Figure 3-6b).

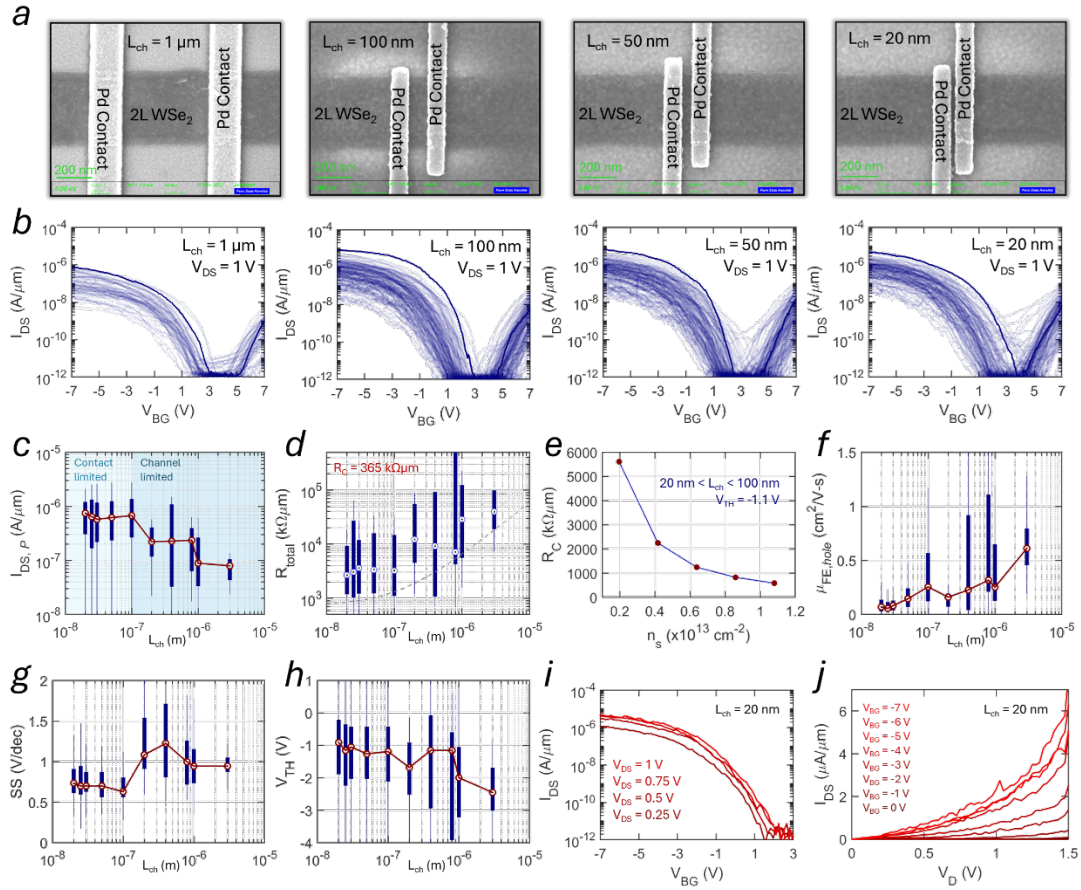


Figure 3-5: Aggressively scaled p-type WSe₂ FETs: a) Representative scanning electron microscope (SEM) images and b) corresponding transfer characteristics of several WSe₂ FETs measured at $V_D = 1$ V with $L_{ch} = 1$ μ m, 100 nm, 50 nm, and 20 nm, respectively. c) Box plot for $I_{DS,P}$ measured at $V_{BG} = -7$ V for different L_{ch} . $I_{DS,P,median}$ reaches ~ 1 μ A/ μ m at $L_{ch} = 100$ nm which is $\sim 10\times$ increase from ~ 100 nA/ μ m at $L_{ch} = 1$ μ m. d) The total resistance, R_T , extracted for $n_s = 10^{13}$ cm⁻², as a function of L_{ch} . Using the traditional linear extrapolation method, R_C is extracted to be 365 k $\Omega\mu$ m. e) Dependence of R_C on n_s . The impact of aggressive L_{ch} scaling on f) $\mu_{FE,P}$, g) SS_P and h) $V_{TH,P}$. i) Transfer and j) output characteristics for the best performing p-type

WSe₂ FET with aggressively scaled L_{ch} of 20 nm. $I_{DS,P,max}$ reaches $\sim 2 \mu A/\mu m$ for $V_D = 1$ V and $V_{BG} = -7$ V.

The impact of aggressive L_{ch} scaling on $\mu_{FE,P}$, SS_P and $V_{TH,P}$ are shown in Figure 3-5f-h, respectively. As expected, $\mu_{FE,P}$ is severely limited by R_C when extracted from ultra-scaled devices.²⁰⁶ However, for longer L_{ch} , $\mu_{FE,P,median}$ was found to be $0.6 \text{ cm}^2 V^{-1} s^{-1}$, whereas $\mu_{FE,P,max}$ can reach $\sim 2.2 \text{ cm}^2 V^{-1} s^{-1}$. We also noted an abrupt change in $SS_{P,median}$ from 1 V/decade to 630 mV/decade for $L_{ch} < 200 \text{ nm}$. We attribute this change to the average grain size of our synthetic WSe₂, which is on the order of $\sim 200 \text{ nm}$. Since adsorbates or residues arising from the fabrication process flow have greater propensity towards grain boundaries, longer devices are more prone to carrier trapping and worsening of SS_P . A similar trend is observed for $V_{TH,P,median}$, which is relatively constant at ~ 1.2 V for $L_{ch} < 200 \text{ nm}$ but shows a steady decrease for $L_{ch} > 200 \text{ nm}$ and reaches ~ -2.45 V at $L_{ch} = 3 \mu m$. Since charges trapped at the grain boundaries can lead to unintentional doping of the channel material, we believe the trend observed for $V_{TH,P}$ can also be correlated to the grain size of synthetic WSe₂. Finally, Figure 3-5i-j, respectively, show the transfer and output characteristics for the best performing WSe₂ FET with aggressively scaled L_{ch} of 20 nm. $I_{DS,P,max}$ reaches $\sim 2 \mu A/\mu m$ for $V_{DS} = 1$ V and $V_{BG} = -7$ V.

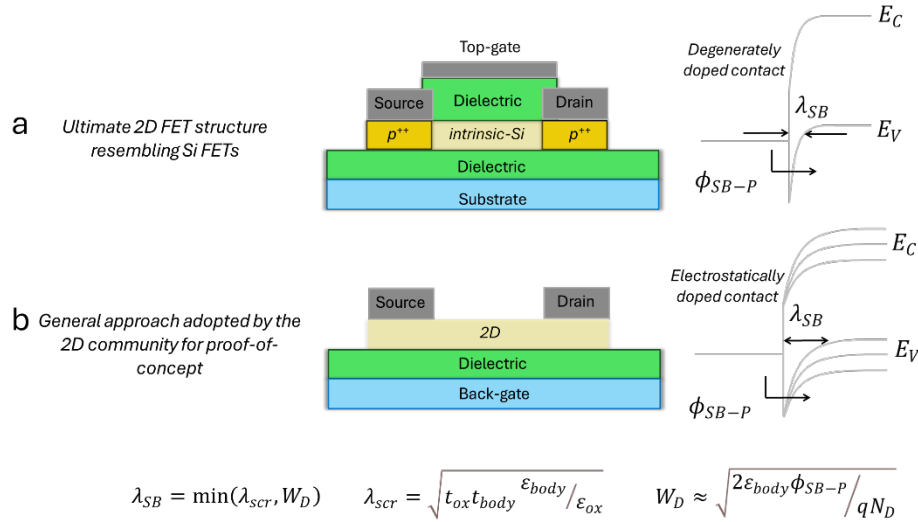


Figure 3-6: Impact of device geometry on contact resistance: a) Conventional top-gated device geometry with degenerately doped source/drain contact regions. b) Back-gated device geometry widely used by the 2D community to enable electrostatic gating of the 2D channel underneath the contacts to compensate for the absence of degenerate doping capability.

Contact Interface Engineering

The ultrathin nature of TMD films, coupled with their vulnerability to damage during processing and device fabrication has underscored the value of employing buffer and sacrificial layers to safeguard interfaces and preserve material properties. For TMD channel materials, the device's performance and characteristics are intrinsically governed by the properties of the interfaces. Unlike traditional bulk semiconductors, where the channel region extends deep into the material, in low-dimensional 2D systems, the channel is confined to an atomically thin layer. Consequently, the interface between the channel and the surrounding materials, such as the gate dielectric, contacts, or encapsulation layers, becomes the defining feature that dictates the device's behavior.

For 2D TMDs or graphene, the channel is essentially a surface, making the interface with the gate dielectric and the contact regions critically important. The quality of this interface can significantly impact various device parameters, including carrier mobility, contact resistance, subthreshold swing, and electrostatic control. Imperfections, defects, or unintended doping at the interface can lead to Fermi-level pinning, charge trapping, and scattering phenomena, ultimately degrading the device's performance. Traditional metallization techniques such as sputtering, or e-beam evaporation often involve the direct impact of hot, high-energy metal atoms on the surface of atomically thin 2D film.²⁰⁷⁻²⁰⁹ For robust multilayer materials, this impact is generally benign or even beneficial, helping to create a strong metal-semiconductor interface. However, 2D TMD films are extremely delicate and sensitive. The high kinetic energy impact from conventional metallization techniques can create defects, dislodge atoms, or even puncture the ultra-thin layers, severely degrading the electrical and mechanical properties of the material. Moreover, the high deposition heat can cause changes in the material structure, such as reconstruction of the lattice, desorption of surface atoms or even unintended strain, as we studied earlier, which can alter the electronic properties of the 2D materials. Some metals tend to chemically react with the TMD surface to form metal chalcogenides and this can also impede electronic performance. Therefore, while conventional metallization techniques have served the semiconductor industry well for traditional materials, their application to 2D TMD films requires careful consideration and adaptation to preserve the unique properties of these promising materials. The use of van der Waals contacts has been debated however there are several scalability challenges when it comes to growth of such in-situ growth of metals directly on the TMD semiconducting films or transfer of metals to avoid FLP from physical process-induced damage. It is unclear if the van der Waals forces that predominantly govern the physical properties of 2D materials favor the formation of strong bonds with metals deposited using conventional techniques. Weak adhesion with the TMD film can also lead to high contact resistance, proving inefficient for carrier injection.

Low-melting Point Contact Metals

Using low melting point contact metals is a strategic approach to mitigate the damage caused by conventional metallization techniques when fabricating contacts on delicate 2D TMDs.^{193,210} This method offers several advantages that help preserve the integrity and enhance the functionality of 2D materials in electronic devices, particularly for creating effective electrical contacts. The use of low melting point metals often involves softer deposition processes and reduced risk of thermal stress that can modify the TMD's inherent properties.^{174,175} However, their chemical stability and back-end-of-line (BEOL) compatibility (>400 °C) are also important points to keep into consideration. Their higher malleability in comparison with high-melting point metals can also allow them to coat the TMD surface more conformally thereby ensuring a large contact surface area. Hence, these metals can help in minimizing thermal, chemical, and mechanical stresses during contact formation.

In/Pd Contacts to WSe₂

In a report by Wang et al., the use of Indium as the contact metal was proposed and the metal formed an mixture with the Palladium metal deposited on the WSe₂ film.²¹⁰ This mixed metal contact was the first to be proposed for p-type FETs and was inspired from the development by Kumar *et al.* on MoS₂ for n-type FET using a stack of Indium and Gold.¹⁷⁸ The devices were shown to exhibit a lower contact resistance and the high-resolution TEM images justified the clean van der Waals contact formation. A similar approach during the fabrication of back-gated FETs on WSe₂ that is grown using MOCVD technique. Devices with In/Pd stack were compared with the devices with bare Pd contacts. Figure 3-7a shows the transfer characteristics of the devices with unoptimized Pd contacts whereas Figure 3-7b shows that for devices with In/Pd

contacts. Deposition of In was carried out using e-beam evaporation in a different chamber followed by Pd evaporation and this may have resulted in slight oxidation of In. Interestingly, both sets of devices show distinct threshold voltages as well as subthreshold switching characteristics. The chip with In/Pd contacted devices show a higher yield, possibly due to the contact interfacial layer. Overall, the devices with In/Pd contacts tend to achieve a higher drive current. The results, although inconclusive, present an interesting approach to introducing contact interfacial layers. The inherent property of the metal also plays an important role in the choice of contact metal to the 2D film. Therefore, the oxidizing ability of In and the reliance on e-beam evaporation still presents doubt on the e-beam induced radiative damage to the TMD film. Furthermore, since most low-melting point metals such as In, Bi, have a low work-function, they are more suitable as n-type contacts. We now demonstrate a unique approach to using a low-melting point, high work-function metal as an ideal p-type contact to WSe₂.

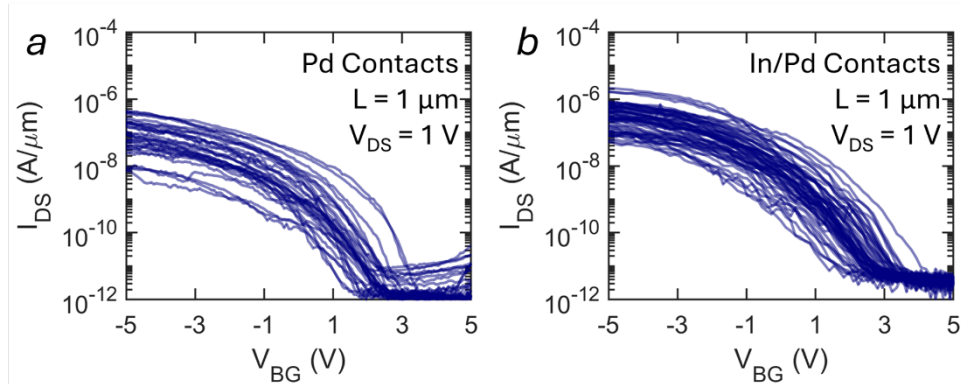


Figure 3-7: Low-melting Point Contact Metals for WSe₂ FETs: Transfer characteristics of monolayer WSe₂ FETs with a) Pd and b) In/Pd as source/drain metal contacts. The L_{ch} for all devices were $1 \mu\text{m}$. The incorporation of Indium metal allows slightly higher performance and fabrication yield. However, the median current values remain the same. Moreover, due to the low melting point of In, the post-processing of the substrate, such as annealing, is restricted.

Se/Pd Contacts to WSe₂

One such metal with a high work function and a low-enough melting point is a chalcogen buffer layer of Selenium (Se), introduced between WSe₂ and the Palladium (Pd) contacts which is shown to notably reduce contact resistance down to 17 k Ω μ m. The combined use of bilayer WSe₂ along with Se buffer layer not only provides interface protection but also markedly improves yield and lowers variability. The dependence of performance on channel length, previously masked by high contact resistance, becomes more apparent following this approach.

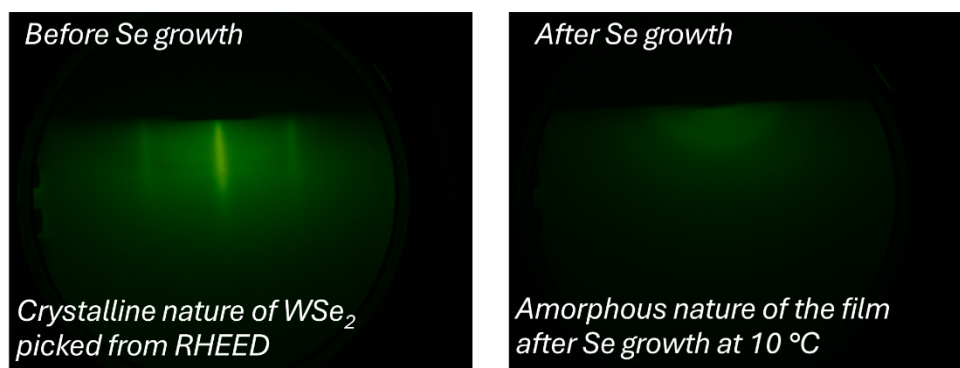


Figure 3-8: Growth of Amorphous Se: Reflection high-energy electron diffraction (RHEED) images confirming amorphous nature of Se before and after growth using molecular beam epitaxy (MBE).

In order to study device behavior with contact interface optimization, we incorporate a 10 nm Se buffer layer into our device fabrication process. This Se layer is deposited via molecular beam epitaxy (MBE) directly onto the WSe₂ films, which have been transferred to a high-k dielectric substrate, under room-temperature and ultra-high vacuum (UHV) conditions to ensure a pristine interface. Figure 3-8 shows the amorphous nature of the MBE grown Se interlayer on WSe₂ confirmed with Reflection High-energy Electron Diffraction (RHEED) images. Device fabrication proceeds as described as discussed in the prior section. The Se layer, characterized by its dull red appearance, gradually loses its color through each step of the fabrication process, ultimately vanishing after the annealing step. This transformation is indicative of the Se layer's

reduction, a necessary step to prevent the formation of a current shorting path across the device. Vacuum annealing is introduced to eliminate the Se layer above the channel region. Given that Se is blanket-coated onto the WSe_2 , the Se beneath the contacts diffuses into the Pd, driven by its vapor pressure and temperature differential, and forms an mixture with Pd. This interaction is visualized in the comparative AFM images of Pd/ WSe_2 and Pd/Se/ WSe_2 stacks provided in Figure 3-9a and Figure 3-9b, respectively, where the Se-interlayered sample exhibits additional grain formation due to the Se-Pd bonding at the elevated temperatures from Pd evaporation.

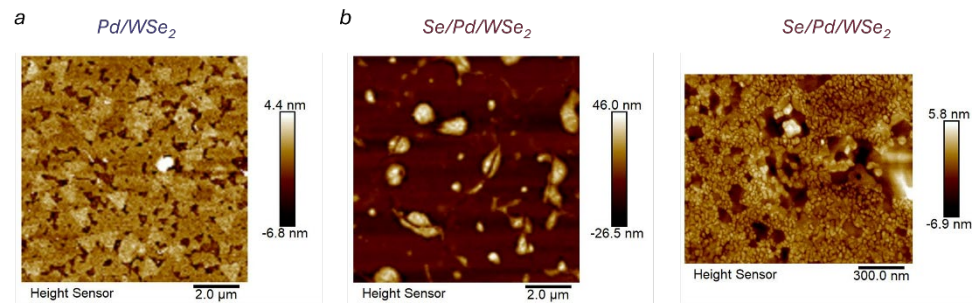


Figure 3-9: Atomic Force Microscopy (AFM) of Mixed-contact interface: A comparison of the topology of the Pd film with and without the presence of the interlayer Se. With 10 nm of Pd directly sitting on WSe_2 , a very conformal coating is formed whereas with the 10 nm Se interlayer and the sample having gone through vacuum annealing, small grains are spotted under the AFM. This may be small grains of nanocrystals that are the resultant of bonding between Pd and Se. When a smaller area is scanned, small grains of certain morphology are observed.

The higher work function of Se, compared to Pd, facilitates a more favorable alignment with the valence band of the channel, enhancing hole injection efficiency. The below- V_{TH} improvement may be attributed to the vacancy-fulfilling ability of Se interlayer in WSe_2 . Furthermore, Se serves as a low-impact barrier to minimize Fermi-level pinning caused by defect creation from high melting point metals. While Se itself is not suitable as a contact metal due to its low melting point, the final work function of the Pd-Se mixture, influenced by the atomic ratio of its constituents, is higher than that of pure Pd. This adjustment in work function leads to enhanced hole injection properties. Figure 3-10a illustrates the device schematics before and after

processing on a Se-coated substrate, highlighting the incorporation of Se interlayer contacts in the WSe₂ FET fabrication.

To elucidate the chemical composition and bonding behavior within the contact region following Pd deposition, we employed X-Ray Photoelectron Spectroscopy (XPS). Drawing on insights from previous studies, we aimed to understand the contact composition's depth-dependent characteristics, which—beyond Fermi level pinning—play a crucial role in defining contact resistance.^{211,212} Figure 3-10b-c present the depth-profiled XPS spectra for the contact metals, Pd and Se, where the initial nanometers of sputtering reveal distinct peaks for Pd and Se 3d 5/2 and 3d 3/2 due to spin-orbit splitting, indicating potential Pd-Se bonding within the stack. The atomic concentration at various depths in the contact stack was estimated by accounting for the relative sensitivity factor, which reflects the probability of ejecting an electron from an atom based on its atomic structure. This analysis offers a glimpse into the composition of the contact/WSe₂ interface and the metal layer's contribution to the work function. Selenium's presence throughout the contact stack, as shown in Figure 3-10e, from the surface to the interface with the 2D material, suggests Se's incorporation through the Pd metal.

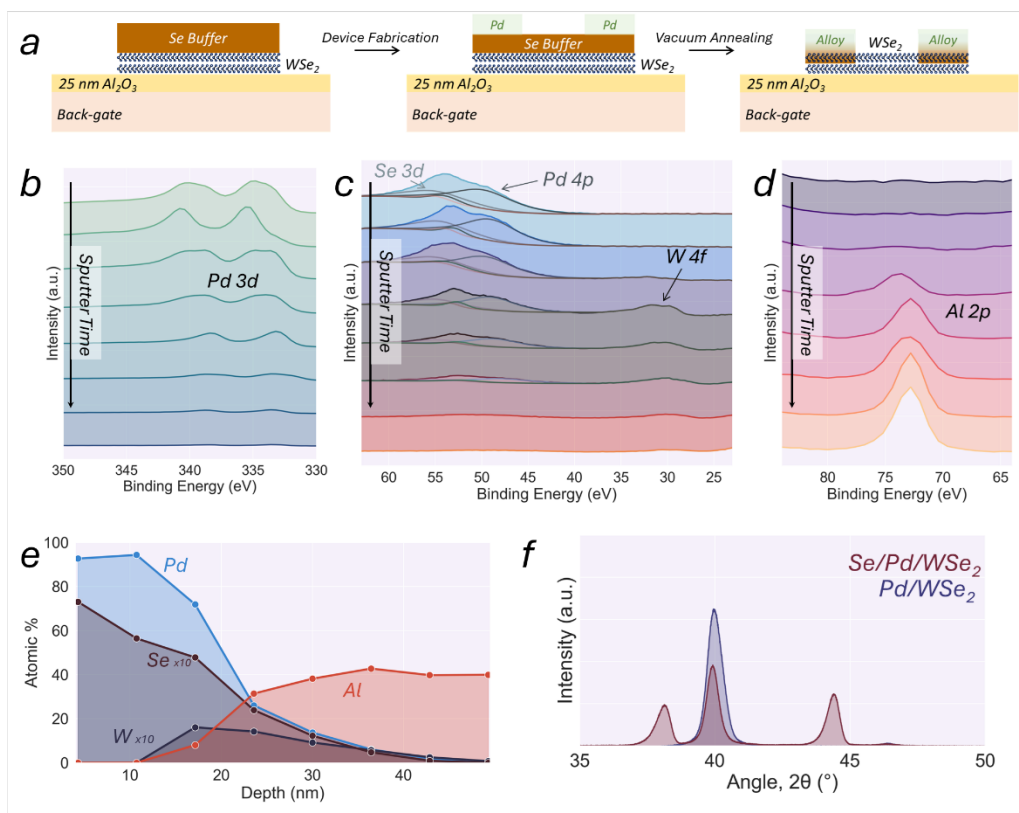


Figure 3-10: Contact Buffer Layer and Alloy Formation: Selenium buffer layer is introduced with the intention to protect the underlying TMD from processing-induced damage. a) Schematic of the process to incorporate Se is displayed. Depth profiled X-Ray Photoelectron Spectroscopy (XPS) emissions of the contact metals, b) Pd 3d, c) Se 3d, W 4f and Pd 4p and d) Al 2p. Palladium and Selenium, but no tungsten is detected from the outer surface down to an estimated depth of 16 nm when W appears. Additional appearing peaks are due to the formation of crystalline Se from the high deposition temperature of Pd; shoulders present in Se peaks point toward Pd incorporation, and potential bonding of the Pd-Se metals. Below the WSe_2 layer, we detect Al and O (not shown) from the Al_2O_3 layer. e) The atomic concentration at each sputtering time in the contact stack can be estimated by considering the relative sensitivity factor. Elemental/bonded Se seems to be present throughout the contact stack and reduces with the same intensity as Pd. As the reduction of intensity is approached, signal from W and Se (bonded to W) starts to emerge and quickly drops due to the ultra-thin nature, before any signal from the substrate starts to be picked. f) X-Ray Diffraction (XRD) is performed to determine the nature of the contact stack. Sample with the Se interlayer shows a crystalline Se peak confirming the formation of an alloy with Pd.

X-Ray Diffraction (XRD) is utilized to study the nature of the contact metal formed with and without the Se buffer layer. Previously, XRD was used to determine the n-type alloyed contact to MoS_2 and confirm its back end of the line (BEOL) compatibility.¹⁷⁸ Figure 3-10f reveals the XRD patterns for a Pd / 100% Bilayer WSe_2 / Si substrate stack with and without a 10

nm Se interlayer. The Se-interlayered stack exhibits a discernible crystalline Se peak, possibly resulting from the thermal effects of Pd evaporation or the vacuum annealing step aimed at removing the Se interlayer. An intriguing aspect of the Se/Pd stack's XRD is the appearance of shoulders on the lower angle side of crystalline Se peaks, hinting at alloy formation with Pd. This observation leads to the speculation that the Se interlayer not only acts as a soft-impact buffer but also contributes to forming a polycrystalline contact metal through alloying with Pd.

Having developed a p-type alloyed contact stack for WSe₂, we proceeded to fabricate FETs using Pd-Se contacts to assess their performance against the previously utilized, unoptimized Pd contacts on 100% bilayer WSe₂. Electrical characterization of devices with $L_{ch} = 1\ \mu\text{m}$ and $L_{ch} = 200\ \text{nm}$ are depicted in Figure **3-11a-b** showcasing significant distinctions between the unoptimized and mixed metal contacts, notably in, (i) a negative shift in V_{TH} , (ii) an improvement in SS, (iii) increased I_D at maximum V_{ov} , and (iv) reduced variation and lower I_D in n-type transport. The first two attributes primarily affect channel and interface properties, while the latter two are indicative of contact quality.

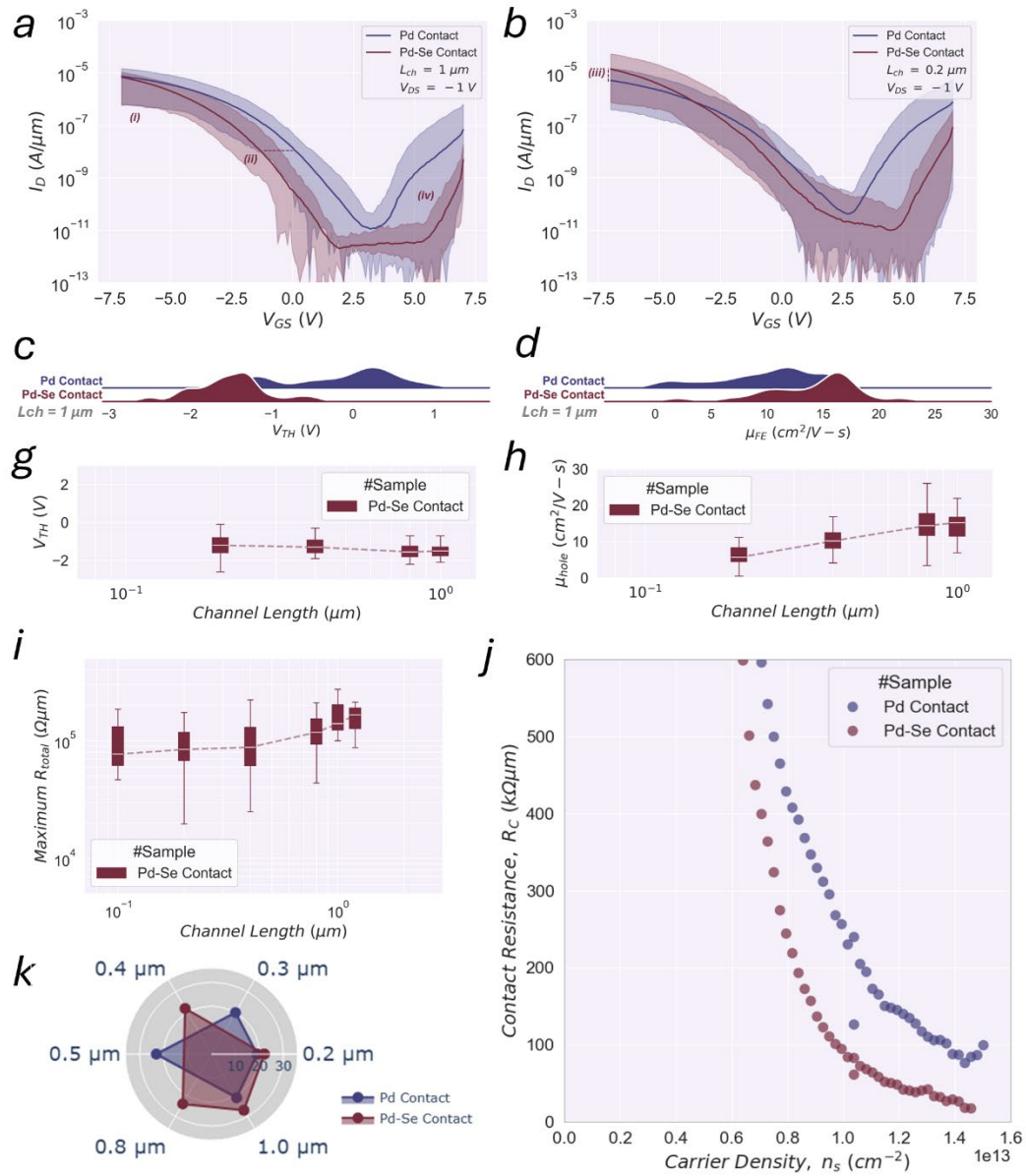


Figure 3-11: Electrical Characterization of p-Type WSe₂ FETs with Alloyed Contacts: FETs with Pd-Se alloy in the contact stack are fabricated to compare their performance against the suboptimal Pd contacts on 100% bilayer WSe₂. Transfer characteristics are plotted in the logarithmic scale for devices with a) $L_{ch} = 1 \mu m$ and b) $L_{ch} = 200 nm$, measured at $V_{DS} = -1 V$. Statistical variability of V_{TH} for c) $L_{ch} = 1 \mu m$ and d) $L_{ch} = 200 nm$ are plotted and reduced variability is observed for devices with alloyed contacts. Furthermore, similar observation is made for the plots of μ_{FE} for e) $L_{ch} = 1 \mu m$ and f) $L_{ch} = 200 nm$. g) Statistical distribution of V_{TH} is plotted for different L_{ch} ranging from 200 nm to 1 μm . V_{TH} follows a more uniform distribution across all L_{ch} and the median value is consistently found to be around -1 V. h) Statistical distribution of μ_{FE} is plotted for different L_{ch}

ranging from 200 nm to 1 μm and a dependence on the L_{ch} still points that the contacts are imperfect. Highest μ_{FE} of 27 $\text{cm}^2/\text{V-s}$ is extracted from a device with $L_{ch} = 800$ nm. Median μ_{FE} increases from 1.6 $\text{cm}^2/\text{V-s}$ to 5.6 $\text{cm}^2/\text{V-s}$ for $L_{ch} = 200$ nm where contact effects are most dominant. i) Total resistance, R_{total} , is now extracted to study the contact properties for the devices with optimized contact/semiconductor interface at the maximum overdrive voltage. A decreasing trend of R_{total} with decreasing L_{ch} suggests an improvement in the contacts. j) Contact resistance, R_C , is then extracted and compared for devices with and without alloyed contacts. Devices with alloyed contacts exhibit better gate control and a threefold reduction in R_C down to 17 $\text{k}\Omega\mu\text{m}$ is extracted. k) Yield for devices with and without contact interface optimization is shown in the polar plot. Device yield with Pd contacts is observed to be 49% while it is 65% for devices with alloyed contacts.

Subsequent analyses focused on channel properties like V_{TH} and μ_{FE} across different L_{ch} .

Figure 3-11c-d illustrate the statistical variability of V_{TH} for L_{ch} of 1 μm and 200 nm, respectively, with alloyed contacts showing a more negative, consistent V_{TH} , indicating reduced variability. This remaining variability might be attributed to the WSe_2 channel's multilayer nature, uneven strain, and grain size variation. Reasons for higher V_{TH} may be the variant electrostatics from the influence of the interface trap states at the contact/semiconductor interface or the preservation of the bilayer/multilayer material under the contacts. Figure 3-11e-f present the variability of μ_{FE} for L_{ch} of 1 μm and 200 nm, respectively. It must be stressed that it becomes difficult to decouple the benefits of the buffer layer in vacancy fulfilling of the underlying material from that of interface protection at the contact/semiconductor region since either of these effects could enhance device performance. The statistical distribution of V_{TH} and μ_{FE} are plotted for different L_{ch} ranging from 200 nm to 1 μm in Figure 3-11g-h, respectively. Notably, V_{TH} exhibits no L_{ch} dependency, with a consistent median value around -1 V. The highest μ_{FE} , 27 $\text{cm}^2/\text{V-s}$, was observed in a device with an L_{ch} of 800 nm, with median μ_{FE} increasing from 1.6 $\text{cm}^2/\text{V-s}$ to 5.6 $\text{cm}^2/\text{V-s}$ for an L_{ch} of 200 nm, where contact effects are most pronounced. This marked improvement in μ_{FE} raises questions about the technique's efficacy for material identification or the reliability of back-gated structures in estimating channel μ_{FE} .²⁰⁶ It is possible that μ_{FE} may still be constrained by interlayer scattering. A comparative analysis of V_{TH}

and μ_{FE} between unoptimized Pd deposition and mixed metal contact formation is provided in Figure 3-12a and Figure 3-12b, respectively.

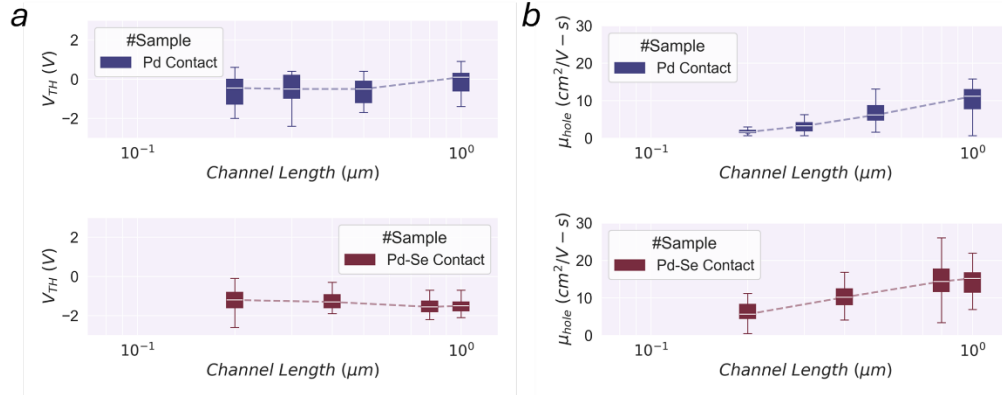


Figure 3-12: Device Parameter Comparison and Channel Length Dependence: a) Side-by-side comparison of threshold voltage, V_{TH} , extracted using the iso-current method at $I_{D,iso} = 10$ nA/ μm with and without alloyed contacts. Evidently, a smaller distribution across all L_{ch} are observed. b) Similarly, comparing the μ_{FE} values for the two cases, it is observed that devices with shorter L_{ch} are less impacted than for the case of Pd evaporated contacts.

We now investigate the effects on contact properties of the FETs by computing the total resistance (R_{total}) at maximum overdrive voltage, illustrated in Figure 3-11i. A comparative analysis of R_{total} for devices, with and without alloyed contacts at maximum overdrive as well as for identical carrier densities (n_s), is presented in Figure 3-13. The extrapolated R_{total} values, obtained using the y-intercept method at the same overdrive voltage, facilitate a direct comparison of R_C across devices, as depicted in Figure 3-11j. For devices with unoptimized Pd contacts on 100% bilayer WSe₂, R_C begins to diverge at higher n_s values, exceeding $1.4E13$ cm⁻², with the lowest recorded R_C at 63 k $\Omega\mu m$ for $n_s = 1.48E13$ cm⁻². In contrast, devices with alloyed contacts exhibit a significant reduction in R_C , reaching as low as 17 k $\Omega\mu m$ at $n_s = 1.45E13$ cm⁻², marking over a threefold improvement in R_C . This enhanced gate control, resulting in reduced R_C at comparatively lower n_s values, can be attributed to the diminished interface trap states across all interfaces with WSe₂, a consequence of the Se interfacial layer's presence.

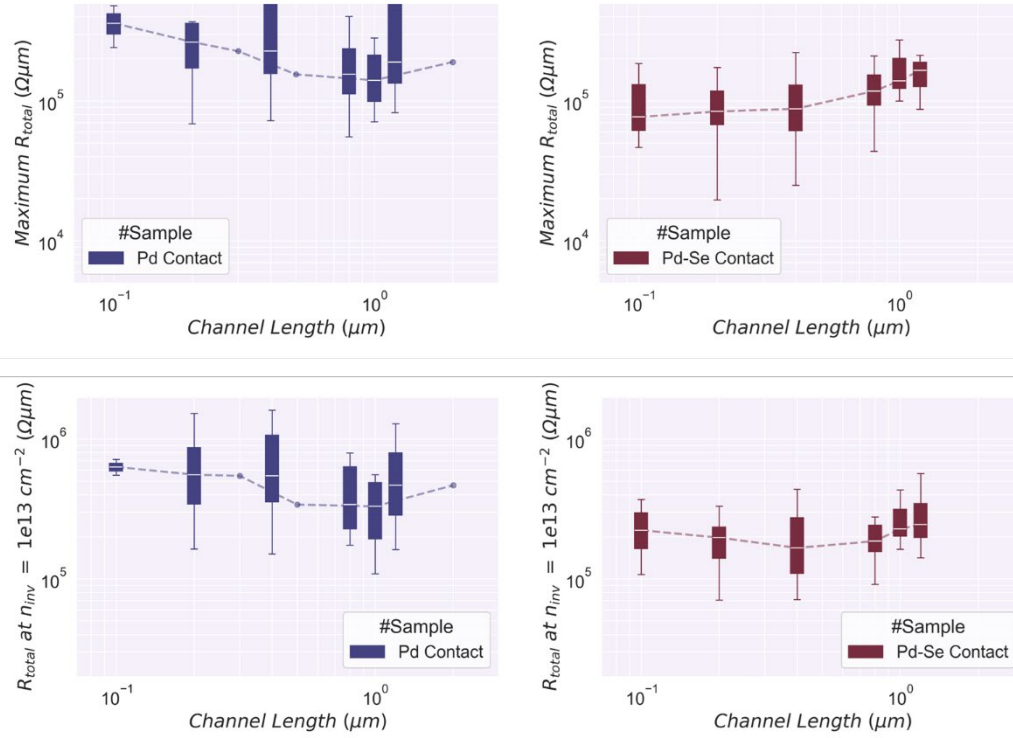


Figure 3-13: Total Resistance Comparison and Channel Length Dependence: Side-by-side comparison of total resistance, R_{total} , at maximum negative gate bias, $V_{\text{GS}} = -7 \text{ V}$, and R_{total} at a given carrier concentration in the channel, $n_s = 1\text{E}13 \text{ cm}^{-2}$ for two different contact schemes, namely evaporated Pd contacts and Se interlayer alloyed contacts. Comparing the R_{total} , it is observed that devices with alloyed contacts show a scaling dependence on the L_{ch} whereas for Pd contacts, R_{total} tends to increase in the opposite manner due to high R_{C} . Similarly, for R_{total} measured at $n_s = 1\text{E}13 \text{ cm}^{-2}$, less variation along with lower values R_{total} in is observed signaling that R_{C} has been reduced. However, the median R_{total} seems to plateau with lower R_{C} is still impeding current injection and further improvement is needed.

Device yield with suboptimal Pd contacts was found to be 49% which was improved to 65% with the introduction of Se buffer layer, as depicted in Figure 3-11k. This improvement was assessed based on criteria such as low gate leakage currents, non-shortcd source-drain contacts, and effective gate control during subthreshold operation. Hence, this section underscores the critical role of the Se interfacial layer in metal evaporation processes, leading to alloy formation and subsequently enhancing hole injection efficiency.

Aiming to further improve hole transport in WSe₂ FETs and achieve threshold tunability, we employed threshold engineering on the WSe₂ FETs. This involved dual gating, varying back gate dielectric, and use of oxide capping films on the WSe₂ channel, thus covering possible routes for further enhancement in device performance.

Chapter 4

Engineering Threshold of p-Type 2D TMD Channels

One of the critical challenges in realizing high-performance p-type field-effect transistors (FETs) based on two-dimensional (2D) channel materials lies in the precise control and engineering of the device's threshold voltage (V_{TH}). In convention bulk MOS technology, the threshold voltage is defined as the minimum gate bias required to create an inversion layer and allow substantial current flow between the source and drain terminals. However, in a fully depleted transistor, where the channel is a thin semiconductor film or 2D material layer, the entire body is depleted of majority carriers at sufficiently large gate voltages. In this case, the threshold voltage is defined as the gate voltage at which the depleted channel becomes conductive due to the formation of a conductive path or accumulation of carriers.

More specifically, for a p-type ultra-thin 2D FET, V_{TH} corresponds to the gate voltage at which the valence band edge at the channel center aligns with the Fermi level, allowing hole conduction. The threshold voltage in fully depleted devices is highly sensitive to the channel thickness, dielectric constant, and the work function difference between the gate metal and the semiconductor channel.^{213,214} Precise control of these parameters is crucial for engineering the desired threshold voltage in ultra-thin-body or 2D channel transistors. Additionally, in fully depleted devices, short-channel effects like drain-induced barrier lowering (DIBL) can significantly impact the threshold voltage, making proper device scaling and optimization even more critical for maintaining good electrostatic integrity and performance.^{204,215} In conclusion, threshold voltage plays a pivotal role in governing the device's switching characteristics, leakage currents, and overall performance.

Importance of Threshold Voltage Engineering

In the realm of complementary metal-oxide-semiconductor (CMOS) logic circuits, the integration of both n-type and p-type FETs with well-engineered threshold voltages is essential for achieving optimal device operation, energy efficiency, and robust circuit functionality [52]. Specifically, for p-type 2D FETs, precise threshold voltage engineering is crucial for the following reasons:

1. **Leakage Current Control:** Proper threshold voltage tuning is vital for minimizing leakage currents in the off-state, which directly impacts the static power consumption and overall energy efficiency of the device. Excessive leakage currents can lead to increased power dissipation, heating, and potential reliability issues.
2. **Drive Current Optimization:** The on-state drive current, which determines the switching speed, transconductance, and ultimately the performance of the FET, is strongly influenced by the threshold voltage. Achieving the desired drive current requires careful engineering of the threshold voltage to ensure sufficient overdrive while maintaining acceptable off-state leakage.
3. **Electrostatic Integrity:** As device dimensions scale down, maintaining excellent electrostatic control over the channel becomes increasingly challenging due to short-channel effects. Optimizing the threshold voltage can help mitigate these effects, such as DIBL and subthreshold swing degradation, ensuring proper switching behavior and preventing undesirable leakage paths.
4. **Circuit Design and Integration:** For seamless integration into CMOS logic circuits, the threshold voltages of both n-type and p-type FETs must be carefully engineered to ensure proper logic level shifting, noise margins, and overall circuit performance. Mismatched

threshold voltages can lead to logic failures, signal degradation, and increased power consumption.

5. Analog/RF Applications: Beyond digital logic, p-type 2D FETs with precisely tuned threshold voltages are essential for analog and radio-frequency (RF) applications, where the transistor's transconductance, linearity, and noise performance are critical.

Achieving precise threshold voltage control in p-type 2D FETs is particularly challenging due to the unique material properties and device physics associated with these emerging channel materials. Factors such as band structure, effective mass, and contact resistance can also impact the threshold voltage characteristics, necessitating innovative engineering strategies tailored to the specific 2D material system.

Electrostatic Modulation by Gating

Electrostatic doping through the application of external electric fields has emerged as an effective strategy for threshold voltage engineering in p-type 2D FETs based on transition metal dichalcogenides (TMDs) like WSe_2 . Unlike conventional substitutional doping, which can disrupt the 2D lattice structure, electrostatic doping allows for precise control over the carrier type and concentration without introducing structural defects. In one approach, locally gated regions, referred to as side polarity gates (PGs), have been employed to induce p-type or n-type transport in WSe_2 channels. By applying appropriate bias voltages to these side PGs, the Fermi level of the WSe_2 channel can be electrostatically modulated, effectively shifting the threshold voltage, and enabling reconfigurable p-type or n-type operation in a single device. This technique has been demonstrated in exfoliated WSe_2 and other TMDs like MoTe_2 , paving the way for logic and neuromorphic applications.

Electrostatic doping has also been extensively explored in dual-gated FET structures, where both a global back gate and a local top gate are used to modulate the channel's carrier concentration and threshold voltage. This approach has been particularly valuable for studying optoelectronic and photovoltaic effects in TMDs, as it allows for precise control over the device's operating regime and carrier transport properties. However, the fabrication of dual-gated FETs on large-area grown TMD materials has been challenging due to issues such as charge transfer doping from high-k dielectrics, energetic alignment of trap states at the TMD/dielectric interface, and threshold voltage variations.²¹⁶⁻²¹⁹ Post-process annealing techniques have been reported to help regain electrostatic control in dual-gated MoS₂ FETs, but a thorough understanding of the underlying mechanisms is still lacking.²²⁰

It is difficult to control the doping concentration, which is key for threshold voltage engineering in FETs. Moreover, achieving both p- and n-type FETs using same large area-grown TMD material remains elusive. Several articles have demonstrated side polarity gates (PGs) as means of achieving n-type and p-type transport from WSe₂²²¹⁻²²⁴. In an article by Thakar *et al.*²²⁵, a single reconfigurable circuit was demonstrated using exfoliated WSe₂ on h-BN where local-back, and side PGs were employed for bias-induced doping to perform logic and neuromorphic operations. Chen *et al.* reported reconfigurable p- and n-type FETs with excellent device performance on exfoliated MoTe₂ using local-back and side PGs for electrostatic doping²²⁶. Several such articles on exfoliated and synthetic WSe₂ have demonstrated electrical tunability using electrostatic doping technique for application in optoelectronics and photovoltaics²²⁷⁻²³⁰. In another article by Groenendijk *et al.*, dual-gated FET was fabricated on exfoliated, multilayer WSe₂ to demonstrate photovoltaic and photo thermoelectric effects²³¹. However, fabricating dual-gated FETs has been extremely challenging on large-area grown TMD material. Large threshold variations in FET performance resulting either from charge transfer doping from high-k dielectrics onto TMD film, or, from the energetic alignment of trap states at the TMD/dielectric

interface, limit dual-gate FET fabrication on TMD materials. Post-process N_2 or Ar/H_2 annealing has been reported to help regain electrostatic control on dual-gated MoS_2 FET, however, a thorough understanding is still lacking. Recent report from imec on establishing a process flow for fabricating high-performance dual-gated MoS_2 FETs is a step forward¹⁸¹. Even though, these reports are very relevant in making TMD-based CMOS logic possible, the use of exfoliated WSe_2 , $MoTe_2$, and h-BN limits the application scope. Recently, Dorow *et al.* demonstrated high-performance FETs based on monolayer CVD-grown WSe_2 with 90 nm SiO_2 as back-gate oxide²³². Furthermore, these devices were top gated with Hf seed/ 5 nm HfO_2 and Al seed/ 6 nm of Al_2O_3 to enhance the p- and n-branch of the device characteristics. However, application of very high global back-gate biases of opposite polarity makes it challenging for CMOS integration on the same substrate. Nevertheless, demonstration of both p- and n-type FETs based on a single TMD material that is synthetically grown and the FETs fabricated on the same substrate, has remained challenging for a long time. While significant progress has been made, the realization of complementary p-type and n-type FETs on the same large-area grown TMD material and substrate remains a challenge, hindering the development of TMD-based CMOS logic circuits.²³³ Overcoming this hurdle through innovative electrostatic doping techniques and interface engineering strategies is a crucial step toward enabling high-performance p-type 2D FETs for advanced logic applications.

Here, we introduce tri-polarity gated (TPG) WSe_2 FETs to achieve unipolar p- and n-type transport. We first characterize the material properties to validate the high-quality and crystalline nature of our large-area WSe_2 obtained using metal organic chemical vapor deposition (MOCVD) technique. We then study dual-gated (DG) WSe_2 FETs for different biasing configurations for the back-gate (BG) and top-gate (TG). We observed ambipolar transport in TG WSe_2 FETs even when the back-gate is biased to limit either n- or p-type carrier injection underneath the contacts confirming two-path carrier injection theory, i.e., body and edge injection proposed in the

literature. Finally, we demonstrate how TPG WSe₂ FETs can be biased to achieve *p-i-p* and *n-i-n* configurations leading to unipolar p- and n-type characteristics. We also realize a CMOS inverter using two TPG WSe₂ FETs. For reasons discussed above, several limitations to achieve unipolar electron and hole transport from the same TMD material have been addressed with TPG WSe₂ FETs. Although polarity gating is a well-known technique, no prior demonstration on large-area grown, ultra-thin TMD channel has been shown. Our proposed approach of electrostatically doping large-area WSe₂ provides with a possible approach to not only determine transport type on the same transistor but also engineer the threshold, thus further advancing CMOS capabilities at ultra-thin channel dimensions as suggested by TSMC's perspective article²⁹. Challenges in terms of device performance and yield are still open and require collective and significant effort.

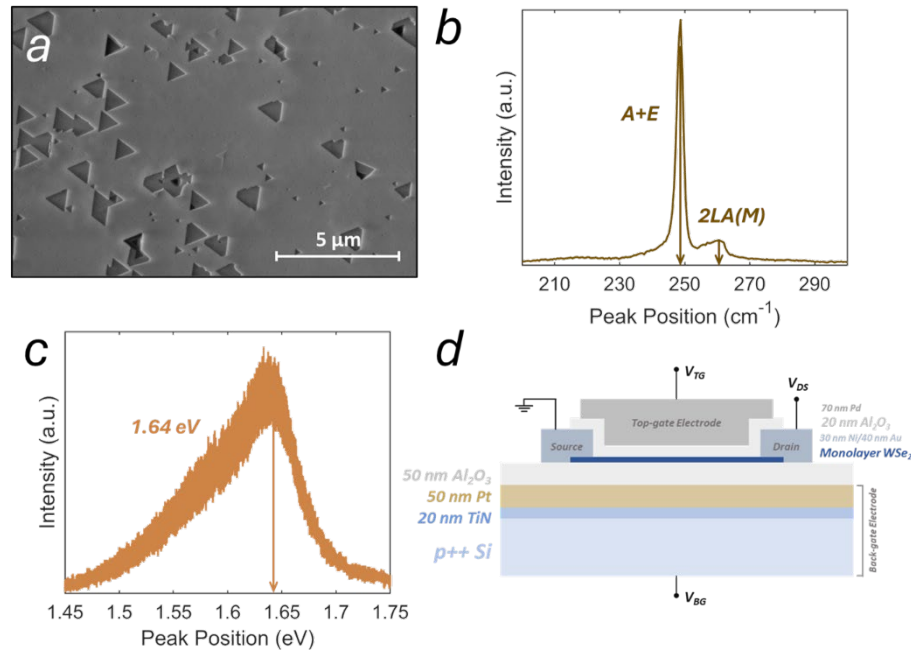


Figure 4-1: Monolayer WSe₂ Material Characterization: a) Scanning electron microscope (SEM) image of the MOCVD grown monolayer WSe₂ on epitaxial c-Al₂O₃. Fully coalesced monolayer film growth, with some bilayer island formation is observed. b) Raman spectra of the monolayer WSe₂ film, which demonstrates peaks at 249.1 cm⁻¹ and 260.9 cm⁻¹ nm corresponding to characteristic A+E and 2LA(M) Raman modes of WSe₂. c) photoluminescence (PL) spectroscopy shows an expected optical band gap of around 1.64 eV for monolayer WSe₂. d) Schematic representation of a monolayer dual-gated (DG) WSe₂ FET device with atomic layer deposition

(ALD) grown 50 and 20 nm Al_2O_3 as the back- and top-gate dielectric and 30 nm/40 nm Pt/TiN and 70 nm Pd as the back- and top-gate electrode. The source/drain contact electrodes were 30 nm Ni/ 40 nm Au.

Monolayer WSe_2 was grown epitaxially on c-plane sapphire (Cryscore Optoelectronic Ltd, 99.996%) substrates at 800 °C via metal organic chemical vapor deposition (MOCVD) technique in a custom-designed, vertical cold-wall reactor reported elsewhere^{234,235}. The surface morphology of the films is evaluated with Verios G4 scanning electron microscope (SEM) with the accelerating voltage of 2 keV as shown in Figure 4-1a; a fully coalesced monolayer film is observed, with islands of bilayer growth. Optical properties are studied with Horiba Labram HR Evolution VIS–NIR Raman system with a 532 nm laser wavelength at 0.5 mW power. Figure 4-1b shows the Raman spectra of the film, which demonstrates peaks at 249.1 cm^{-1} and 260.9 cm^{-1} nm; these peaks corresponds to characteristic A+E and 2LA(M) Raman modes of WSe_2 , where the absence of the interlayer mode at 309 cm^{-1} further confirms the monolayer nature of the films^{236,237}. Moreover, photoluminescence (PL) spectroscopy, as given in Figure 4-1c, shows an expected optical band gap of around 1.64 eV for monolayer WSe_2 .

All WSe_2 FETs were fabricated on conventional silicon substrate. For back-gate electrode a stack of 20 nm/50 nm TiN/Pt is sputter deposited on Si substrate followed by atomic layer deposition (ALD) of 50 nm of Al_2O_3 as the back-gate oxide at 200 °C. Monolayer WSe_2 film is wet-transferred onto the back-gated stack, spin-coated with A6 PMMA and patterned with e-beam lithography to define the channel width. The remaining WSe_2 is etched away using sulfur hexafluoride (SF_6) plasma under 5 °C for 30 s. Another e-beam lithography step is employed to pattern source/drain contact regions on positive bilayer photoresist stack of methyl methacrylate (MMA) and A3 PMMA. Post-develop in MIBK/IPA solution for 60 s/45 s, contact electrode stack of 40 nm nickel (Ni) and 30 nm gold (Au) is deposited using e-beam evaporation. Lift-off is performed by immersing the metal-coated sample in acetone followed by IPA. For top-gate

fabrication, a thin 1 nm seed layer of aluminum (Al) is evaporated using e-beam to allow uniform growth of 20 nm of top-gate oxide, Al_2O_3 by ALD at 150 °C. Lower temperature ALD growth prevents underlying WSe_2 nanosheet from degradation. Finally, the sample is spin coated with MMA/PMMA and patterned with e-beam lithography to define top-gate electrode. Post-develop, 70 nm of palladium (Pd) was e-beam evaporated as top-gate electrode, which was followed by lift-off with acetone and IPA. Figure 4-1d, shows the schematic of a DG WSe_2 FET. Electrical measurements were performed using Keysight B1500 parameter analyzer inside Lake Shore and FormFactor 12000 probe stations.

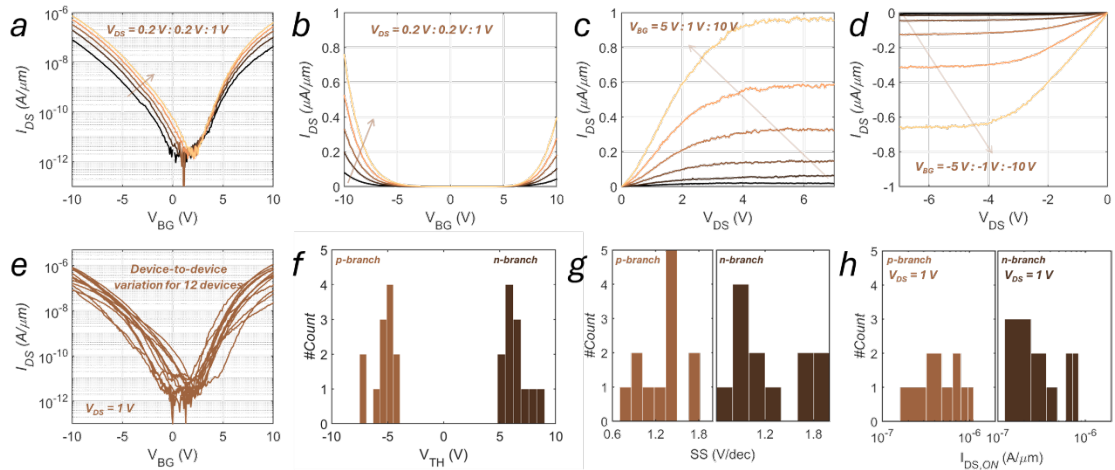


Figure 4-2: Electrical Characterization of Ambipolar WSe_2 FETs: Transfer characteristics, i.e., drain current (I_{DS}) versus back-gate voltage (V_{BG}) for different source to drain voltage (V_{DS}) in a) logarithmic and b) linear scale of a monolayer WSe_2 FET. Output characteristics, i.e., I_{DS} versus V_{DS} for c) positive V_{BG} and d) negative V_{BG} . e) Device-to device variation in the transfer characteristics of 12 WSe_2 FETs. Histogram plots showing the device-to-device variation in f) threshold voltage (V_{TH}), g) subthreshold slope (SS), and h) on-current extracted for both n- and p-branches across these 12 devices.

Figure 4-2a-b, show the transfer characteristics of a back-gated WSe_2 FET with channel length $L_C = 1 \mu\text{m}$, and channel width of $W = 5 \mu\text{m}$, in the logarithmic and linear scale respectively. The drain to source current (I_{DS}) is measured at varying source to drain voltages (V_{DS}) from 0.2 V to 1.0 V, in 200 mV increments, while the back-gate voltage (V_{BG}) is swept

from 10 V to -10 V. High current ON/OFF ratio of $\sim 10^6$ at $V_{DS} = 1$ V, is observed for both electron and hole branch. Electron and hole mobility values are extracted from the transfer characteristics using peak transconductance method and are found to be ~ 1.5 and $2.5 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$, respectively. Output characteristics, i.e., I_{DS} versus V_{DS} for varying V_{BG} is plotted for both n- and p-branch in Figure 4-2c-d, respectively. Due to pinning of metal Fermi level at the midgap, carrier injection is mostly Schottky barrier-limited for both electron and hole transport, as evident from the output characteristics, which has also been reported in other works²³⁸⁻²⁴⁰. The device ON current, I_{DS} reaches 980 nA/ μm at $V_{DS} = 6$ V and 660 nA/ μm at $V_{DS} = -6$ V for n- and p-branch, respectively. The inversion charge carrier density in the n-branch is calculated and found to be $\sim 2.43 \times 10^{12} / \text{cm}^2$ while for the p-branch, it is found to be $\sim 2.54 \times 10^{12} / \text{cm}^2$. Here, the inversion carrier density, Q_{inv} , is calculated using the formula $Q_{inv} = C_{ox}(V_{BG} - V_{TH,p/n})$, where C_{ox} is the oxide capacitance given as the ratio of oxide dielectric constant and oxide thickness, $V_{TH,p/n}$, is the threshold voltage calculated using iso-current method at $I_{DS} = 10$ nA/ μm for both the n- and p-branch and is found to be $V_{TH,n} = 7.8$ V and $V_{TH,p} = -7.7$ V, respectively, and $V_{BG} = \pm 10$ V is the voltage applied to the back-gate for the device to operate in the ON state of the n- and p-branch, respectively. Device-to-device variation is captured by measuring transfer characteristics of 12 devices across the substrate, as shown in Figure 4-2e. Histogram plots showing the device-to-device variation in threshold voltage, subthreshold slope (SS), and on-current extracted for both n- and p-branches across these 12 devices are shown in Figure 4-2f-h, respectively.

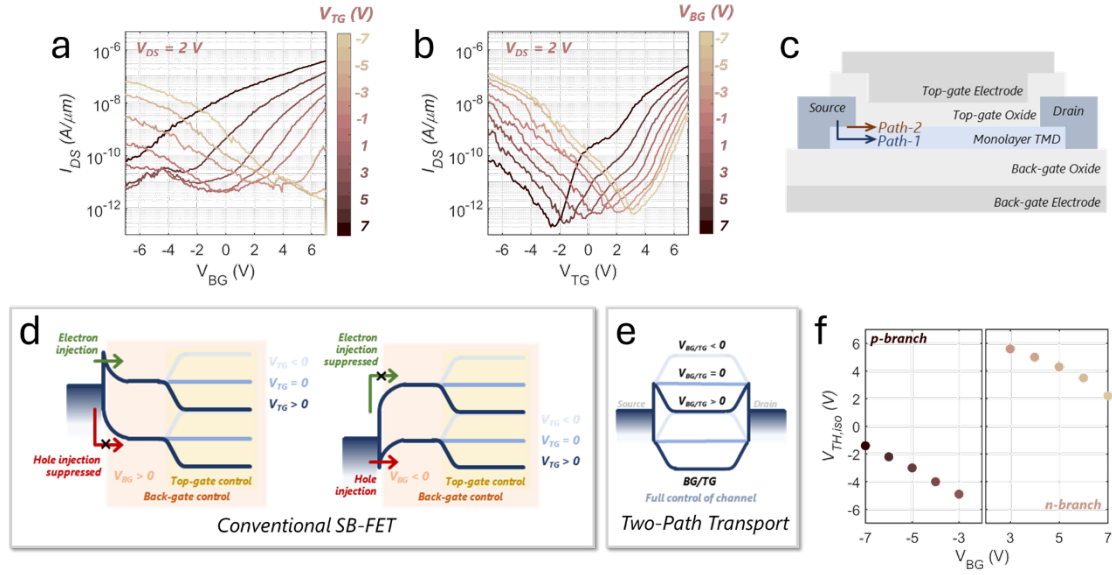


Figure 4-3: Dual-gate WSe₂ FETs: a) Back-gate transfer characteristics for $V_D = 2$ V for discretely varying top-gate voltage, V_{TG} . The electron and hole branches are completely suppressed for $V_{TG} < -3$ V and $V_{TG} > 3$ V, respectively, despite V_{BG} being swept between ± 7 V. This is expected since the TG 20 nm thick Al₂O₃ has $\sim 2.5\times$ better electrostatic control of the channel. b) Top-gate transfer characteristics of the WSe₂ FET when V_{TG} is swept from -7 V to 7 V for discretely varying V_{BG} between -7 V and 7 V, for $V_{DS} = 2$ V. Unlike the BG, the TG has no electrostatic access to the WSe₂ channel underneath the contacts and is therefore unable to control the band movement or Schottky barrier at the Ni/WSe₂ contact interface. The ambipolar transport in the TG transport characteristics is understood by invoking a secondary path for carrier injection. c) Device schematic showing the two-path transport in our DG WSe₂ FET as an extension to the conventional Schottky-barrier FET model. Here, two separate carrier injection paths were modelled: 1) carrier injection from metal to the 2D channel underneath the contact, or body injection and 2) carrier injection from the edge of the contact to the adjacent channel, or edge injection. d) Energy band diagrams for the conventional SB-FET model. When V_{BG} is positive (negative), hole (electron) injection into the channel underneath the contacts is prohibited. e) Energy band diagram for the extended two-path model. Here the SB for the edge injection can be controlled by both TG and BG. f) Tunability of $V_{TH,p/n}$ for the TG WSe₂ FET using V_{BG} .

Figure 4-3a shows the BG transfer characteristics for $V_D = 2$ V for discretely varying top-gate voltage, V_{TG} . Clearly, polarity and magnitude of V_{TG} allow for the modulation of $V_{TH,n}$ and $V_{TH,p}$. Also note that the electron and hole branches are completely suppressed for $V_{TG} < -3$ V and $V_{TG} > 3$ V, respectively, despite V_{BG} being swept between ± 7 V. This is expected since TG Al₂O₃ is 20 nm thick, whereas BG Al₂O₃ is 50 nm thick allowing the TG $\sim 2.5\times$ better electrostatic control of the channel. In other words, electrons (holes) induced by positive

(negative) V_{TG} must be compensated by equivalent negative (positive) V_{BG} before any hole (electron) transport can be observed. Next, we would like to discuss some interesting observations in DG WSe₂ FETs. Figure 4-3b shows the TG transfer characteristics of the WSe₂ FET when V_{TG} is swept from -7 V to 7 V for discretely varying V_{BG} between -7 V and 7 V, for $V_{DS} = 2$ V. Note that the TG stack shown in Figure 4-3c is patterned to overlap with the source and drain contact regions to ensure TG control of the entire monolayer WSe₂ channel. However, unlike the BG, the TG has no electrostatic access to the WSe₂ channel underneath the contacts and is therefore unable to control the band movement or Schottky barrier at the Ni/WSe₂ contact interface. Yet, we observe ambipolar transport in the TG transfer characteristics irrespective of V_{BG} . This carrier injection anomaly can be explained by invoking a secondary path for carrier injection. In a report by Prakash *et al.*²⁴¹, a novel two-path model is proposed as an extension to the conventional Schottky-barrier FET model. Here, two separate carrier injection paths were modelled: 1) carrier injection from metal to the 2D channel underneath the contact, or body injection and 2) carrier injection from the edge of the contact to the adjacent channel, or edge injection as shown in the device schematic in Figure 4-3c. For the conventional SB-FET model, when V_{BG} is positive (negative), hole (electron) injection into the channel underneath the contacts is prohibited based on the band diagrams shown in Figure 4-3d. While TG has no control on the carrier injection at the Ni/WSe₂ contact interface underneath the channel, it can modulate the barrier for carrier injection from the edge of the Ni contact to the WSe₂ channel. Hence, carrier injection for a DG WSe₂ FET can be simply explained by incorporating the two-path transport as shown in the band diagrams in Figure 4-3e. As such, the ambipolar feature is preserved in the TG transfer characteristics irrespective of the magnitude and polarity of V_{BG} . However, since V_{BG} has electrostatic access to the entire channel, $V_{TH,p/n}$ can be tuned using V_{BG} as seen in Figure 4-3f. Here, $V_{TH,p/n}$ for the n- and p-branch are extracted from iso-current method for $I_{DS} = 1$ nA/ μ m.

Figure 4-4 shows few other DG WSe₂ FET characteristics where ambipolar characteristics are preserved in TG transfer characteristics and statistically confirms two-path injection.

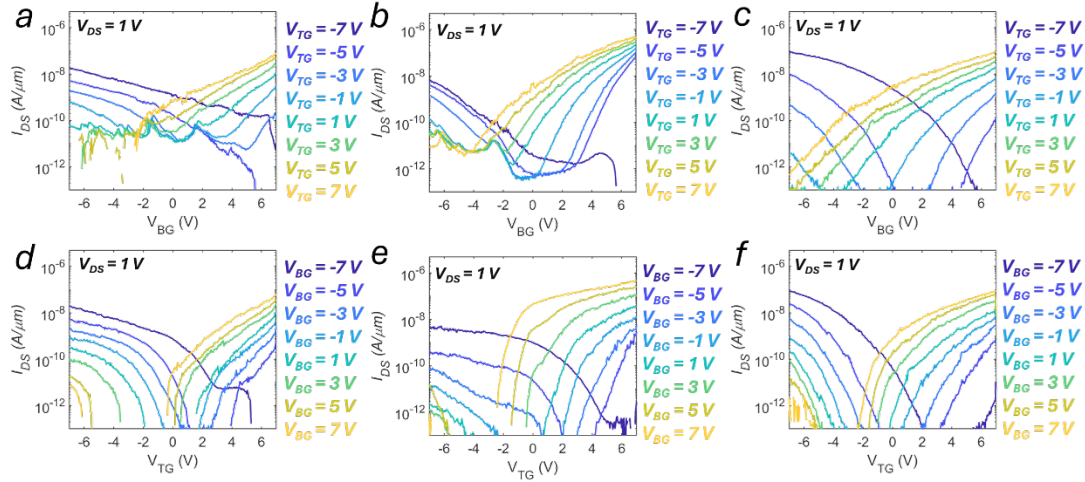


Figure 4-4: Statistical evidence in three top-gated WSe₂ FETs confirming two-path carrier injection: a-c) Back-gate transfer characteristics of three WSe₂ FETs measured at $V_D = 1$ V for discretely varying V_{TG} . As expected, the electron and hole branches are completely suppressed for $V_{TG} < -3$ V and $V_{TG} > 3$ V, respectively. d-f) Top-gate transfer characteristics measured at $V_D = 1$ V for discretely varying V_{BG} , corresponding to the above three FETs showing ambipolar transport behavior. This confirms and validates the two-path injection phenomenon which preserved the ambipolar transport in top-gated WSe₂ FETs.

From the above observations and discussion, it is clear that in order to achieve unipolar FET transfer characteristics, the edge injection must be suppressed at the metal/2D semiconductor contact interface. This is accomplished by using a tri-polarity gated (TPG) WSe₂ FET achieving *n-i-n* and *p-i-p* doping profile using gate electrostatics. Figure 4-5a-b, respectively show the schematic and false-colored scanning electron microscope (SEM) image of the proposed TPG WSe₂ FET structure with two PGs integrated on top of a BG WSe₂ FET. The two PGs are shorted to the same contact pad and supplied with a bias of V_{PG} . These PGs are responsible for controlling the edge injection at the metal/2D semiconductor contact interface. Figure 4-5c-d demonstrate the capability of our TPG WSe₂ FET to function as a unipolar p- and n-type FET, respectively. For $V_{PG} < 0$ V and $V_{BG} = 0$ V, a *p-i-p* doping profile is achieved. Applying $V_{BG} < 0$ V

reduces the barrier height for hole injection in the intrinsic region and thereby creates a continuous p-type channel between the source and the drain contacts. In contrast, applying $V_{BG} > 0$ V lowers the barrier for electron injection in the intrinsic region but it is incapable of compensating for the barrier for electron injection introduced near the contacts through electrostatic p-type doping by applying $V_{PG} < 0$ V. Thinner (20 nm) oxide dielectric used for the PG compared to the thicker (50 nm) BG dielectric makes it more difficult for the BG to have electrostatic control of the doped regions. A similar situation arises for $V_{PG} > 0$ V and $V_{BG} = 0$ V, except for the fact that an *n-i-n* doping profile is established. Therefore, applying $V_{BG} > 0$ V enables electron transport, whereas hole transport remains suppressed for $V_{BG} < 0$ V. In both cases, $V_{TH,p/n}$ can be adjusted using the magnitude of V_{PG} . Figure 4-6 shows the transfer characteristics of few TPG WSe₂ FETs where edge injection at the metal/2D semiconductor contact interface is controlled to achieve unipolar transport behavior in WSe₂ FETs.

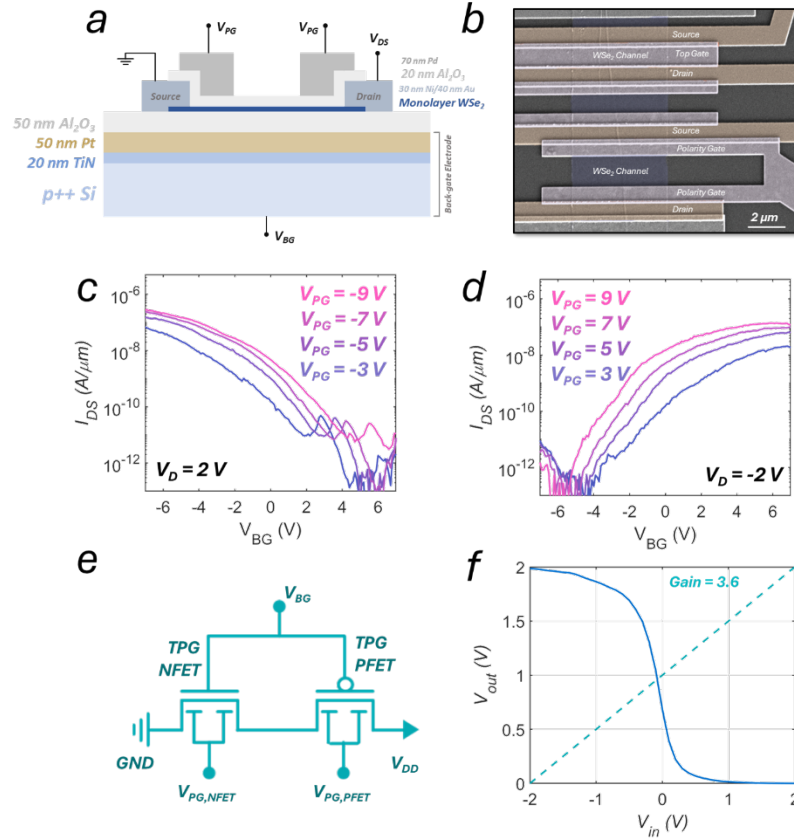


Figure 4-5: Tri-polarity gated (TPG) FETs to build a CMOS Inverter: a) Device schematic and b) false-colored scanning electron microscope (SEM) image of tri-polarity gated (TPG) WSe₂ FET structure with two polarity-gates (PGs) integrated on top of a BG WSe₂ FET. The two PGs are shorted to the same contact pad and supplied with a bias of V_{PG} . These PGs are responsible for controlling the edge injection at the metal/2D semiconductor contact interface. Unipolar c) p-type and d) n-type device operation is demonstrated using the TPG WSe₂ FET. For $V_{PG} < 0$ V and $V_{BG} = 0$ V, a p-i-p doping profile is achieved. Applying $V_{BG} < 0$ V reduces the barrier height for hole injection in the intrinsic region and thereby creates a continuous p-type channel between the source and the drain contacts. In contrast, applying $V_{BG} > 0$ V lowers the barrier for electron injection in the intrinsic region but it is incapable of compensating for the barrier for electron injection introduced near the contacts through electrostatic p-type doping by applying $V_{PG} < 0$ V. Thinner TG dielectric (20 nm) used for the PG compared to the thicker BG dielectric (50 nm) makes it more difficult for the BG to have electrostatic control of the doped regions. Similarly, for $V_{PG} > 0$ V and $V_{BG} = 0$ V, as shown in d), a n-i-n doping profile is achieved. Thus, by applying $V_{BG} > 0$ V enables electron transport, whereas hole transport remains suppressed for $V_{BG} < 0$ V. Moreover, $V_{TH,p/n}$ can be adjusted using the magnitude of V_{PG} . e) Schematic of a CMOS inverter using TPG FETs. f) Output (V_{out}) versus Input (V_{in}) characteristics of our 2D CMOS inverter. The peak gain of the WSe₂ CMOS inverter is calculated using the formula dV_{out}/dV_{in} and is found to be ~ 3.6 .

Finally, we realize a CMOS inverter, which is a fundamental logic unit for any integrated circuit, using our TPG WSe₂ FETs. Here, we integrate two TPG WSe₂ FETs, such that one of

them is biased to operate as an n-type FET and the other as a p-type FET. Although resistive-load based inverters using only n-type TMDs have been demonstrated, it comes at a cost of increased power consumption and lower noise margin; thus, CMOS inverters are desired^{123,242}. Figure 4-5e-f, respectively, show the schematic and input (V_{in}) versus output (V_{out}) characteristics of our 2D CMOS inverter. Note that the input voltage, $V_{in} = V_{BG}$, is common to both n- and p-type WSe₂ FETs and is swept from -2 V to 2 V. Also note that, $V_{DD} = 2$ V is applied to the source terminal of the p-type WSe₂ FET, whereas the source terminal of the n-type WSe₂ FET is connected to the ground. The output (V_{out}) is obtained at the common drain terminal of the two WSe₂ FETs. Fixed voltages $V_{PG,PFET} = -7$ V and $V_{PG,NFET} = +7$ V are applied to the respective PGs of the p- and n-type WSe₂ FETs.

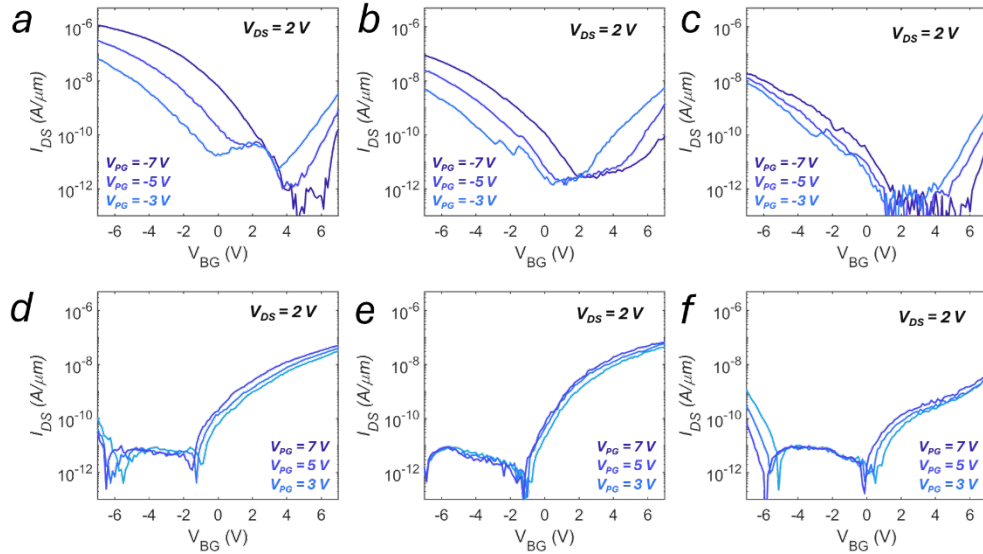


Figure 4-6: Back-gated transfer characteristics of three tri-polarity gated (TPG) WSe₂ FETs: Each TPG WSe₂ FET is integrated with two polarity-gates (PGs) on top, to primarily control edge injection at the metal/2D semiconductor contact interface. Unipolar a-c) p-type and d-f) n-type device operation is demonstrated using three TPG WSe₂ FETs for varying V_{PG} , measured at $V_D = 2$ V.

Figure 4-7a-b show the transfer characteristics of the p- and n-type modulated TPG WSe₂ FETs that constitute the CMOS inverter in Figure 4-5f. The peak gain of the WSe₂ CMOS

inverter is calculated using the formula dV_{out}/dV_{in} and is found to be ~ 3.6 . This demonstration highlights the potential use of WSe₂ in beyond-Si CMOS logic. To the best of our knowledge, this is the first demonstration of a 2D CMOS inverter using the same large-area grown TMD material integrated on the same substrate. We acknowledge that the device performance of our WSe₂ FETs can be further improved through the reduction in grain boundaries and defects in the WSe₂ films by the optimization of MOCVD growth, damage-free and clean transfer of as-grown film onto the target device fabrication substrate, as well as through contact engineering, use of high-k dielectric, and scaling of device dimensions^{126,127,243,244}.

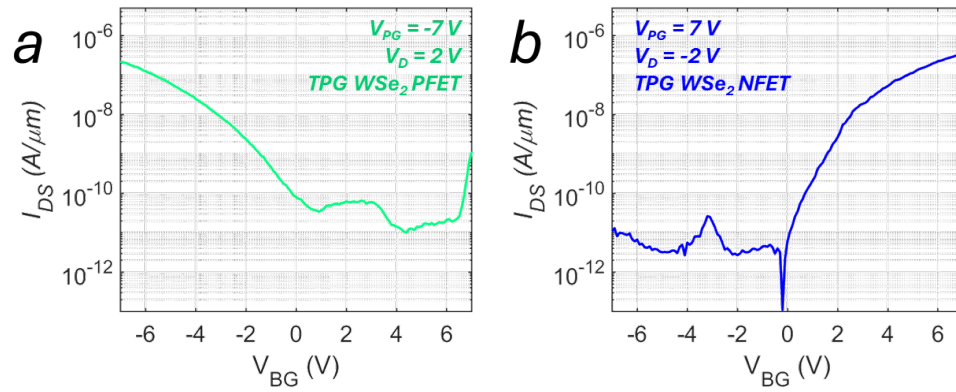


Figure 4-7: Transfer characteristics of two TPG WSe₂ FETs constituting a CMOS Inverter: Fixed voltages $V_{PG, PFET} = -7$ V and $V_{PG, NFET} = +7$ V are applied to the respective PGs of the a) p- and b) n-type WSe₂ FETs to obtain the inverter characteristics shown in Figure 4-5.

In this work, DG and TPG FETs are fabricated and studied based on MOCVD-grown monolayer WSe₂. We found that both Pt bottom gate with 50 nm ALD-grown Al₂O₃ and Pd top gate with 20 nm ALD grown Al₂O₃ enable excellent electrostatic control of the WSe₂ channel, enabling both electron and hole transport. However, in a DG FET, it is challenging to obtain unipolar FET characteristics owing to carrier injection at the edges of metal/2D semiconductor contact interface despite the use of BG to eliminate either electron or hole injection into the channel underneath the contacts. However, by using side PGs, it is possible to obtain *p-i-p* and *n-*

i-n doping profile leading to unipolar p- and n-type WSe₂ FETs. Finally, TPG WSe₂ FETs were used to realize a 2D CMOS inverter on the same substrate.

Gate Dielectric Dependence

The choice of gate dielectric material and its properties can significantly impact the threshold voltage of p-type 2D FETs through various mechanisms, including:

1. **Dielectric Constant (κ -value):** The dielectric constant of the gate insulator material plays a crucial role in determining the electrostatic control over the channel. A high- κ dielectric material can provide stronger capacitive coupling between the gate and the 2D channel, leading to more effective modulation of the channel's carrier concentration and, consequently, the threshold voltage [64]. For example, hafnium oxide (HfO₂) with a relatively high dielectric constant (theoretical $\kappa \approx 25$) can offer improved electrostatic control compared to traditional silicon dioxide (SiO₂) (theoretical $\kappa \approx 3.9$), potentially enabling lower operating voltages and better subthreshold swing in 2D FET.^{216,245}
2. **Interface Dipole Formation:** The interface between the gate dielectric and the 2D channel material can give rise to dipole formation, which can significantly shift the threshold voltage. The dipoles can originate from factors such as metal-induced gap states, structural distortions, or charge transfer across the interface.
3. **Charge Trapping and Fixed Charges:** Defects and impurities within the gate dielectric material can act as charge trapping sites, leading to the accumulation of fixed charges. These trapped charges can modulate the effective electric field experienced by the channel, influencing the threshold voltage.

4. **Band Alignment and Fermi-Level Pinning:** The band alignment between the gate dielectric and the 2D channel material can play a role in determining the degree of Fermi-level pinning at the interface.

By carefully selecting and engineering the gate dielectric material, its dielectric constant, interface properties, and band alignment, one can effectively tune the threshold voltage of p-type 2D FETs to achieve the desired device characteristics and performance targets. Carrier transport dependence on the dielectric interface has notable implications and has been well studied for the case of n-type FETs.^{214,246,247} However, their dependence on the p-type FET operation has not been statistically looked into.

Here, we identify a favorable back-gate dielectric from among HfO₂, Al₂O₃, ZrO₂, and AlN and study its dependence on the p-type transport. Use of a variety of 3D insulators, both amorphous and crystalline, to 2D channels has been widely demonstrated for n-type 2D FETs. Moreover, the use of high-k dielectrics to achieve low equivalent oxide thickness (EOT) for comparing technological relevance of 2D channels has also provided concrete evidence for high-k dielectric integration in 2D logic. However, theoretical predictions of these values for the purpose of identification of optimum dielectrics to 2D TMDs do not / cannot always tell the complete story that is observed from experimental results. The dielectric interface properties are the trickiest to predict and so is its impact on the transport mechanism. Interface properties can affect device switching behavior such as threshold voltage (V_{TH}), subthreshold slope (SS) and for the case of contact-gated FETs such as ours, it also has a significant impact on the above-threshold parameters such as ON current (I_D at $V_G - V_{TH} > 0$). We use HfO₂, ZrO₂, Al₂O₃, and AlN, grown using atomic layer deposition (ALD) technique and evaluate each of them on the basis of electronic performance of p-type 2D WSe₂ FETs.

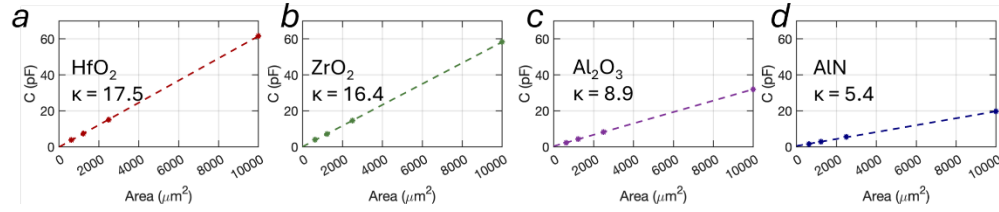


Figure 4-8: Dielectric Constant Extraction: Capacitance measurements on increasing contact pad areas of capacitor structures that sandwich 25 nm of a) HfO_2 , b) ZrO_2 , c) Al_2O_3 , and d) AlN .

First, the dielectric constant of each of the dielectrics is extracted from the measured capacitance of metal-insulator-metal (MIM) structures. Figure 4-8a-d shows the extracted capacitance value from the four given dielectrics for varying capacitor structure area. The dielectric constant (κ) values are found to be 17.4 for HfO_2 , 14.1 for ZrO_2 , 8.9 for Al_2O_3 , and 5.4 for AlN .

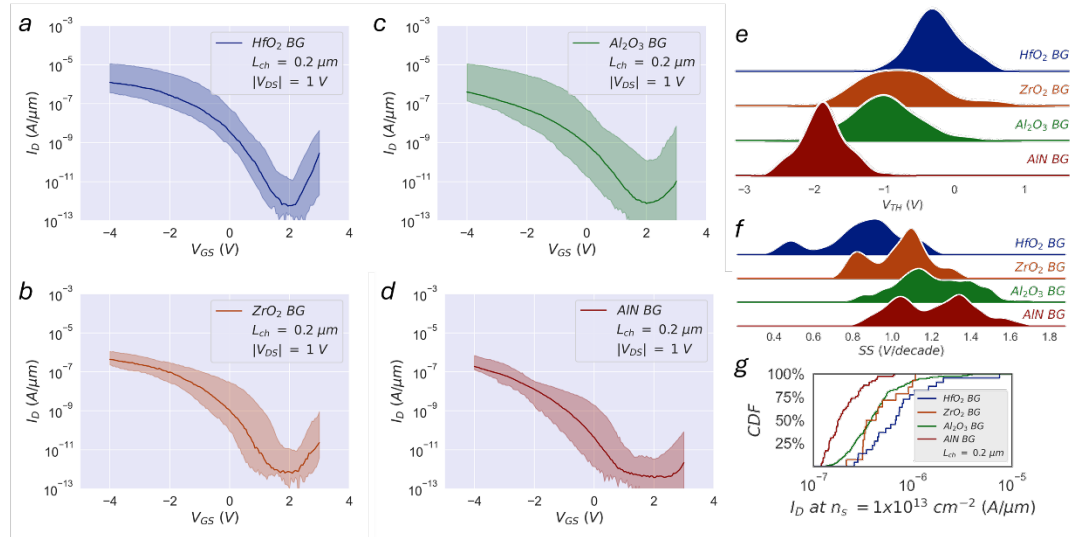


Figure 4-9: Back-gate Dielectric Dependence on WSe_2 FET Performance: Logarithmic scale transfer characteristics of WSe_2 FETs on a) 25 nm of HfO_2 , b) 25 nm ZrO_2 , c) 25 nm Al_2O_3 , d) 25 nm AlN , with a channel length of $0.2 \mu\text{m}$, measured at a drain bias of 1 V. The solid line indicates the median current value from all the devices whereas the shaded bands indicate the distribution covering the results from all the devices. e) Gaussian distribution comparing the V_{TH} on all substrates showing a trend in the mean V_{TH} varying from 0 V to -2 V. Here, doping from the dielectric can be roughly estimated and it shows that HfO_2 least n-type dopes the WSe_2 from the back f) Gaussian distribution of subthreshold slope (SS) of all devices on a given dielectric show that devices on HfO_2 have the best switching characteristics however they follow a wide distribution and is divided into three distinct bands. A similar case is observed for rest of the

dielectrics. g) Cumulative Distribution Function (CDF) plot shows the measured device current (I_D) extracted at a given carrier concentration of $n_s = 1 \times 10^{13} \text{ cm}^{-2}$, show the probability that the current extracted at this specified carrier concentration falls below a certain value.

Figure 4-9a-d shows the transfer characteristics of the devices on the four given dielectric substrates, namely, HfO_2 , ZrO_2 , Al_2O_3 , and AlN , with a channel length of $0.2 \text{ } \mu\text{m}$, measured at a drain bias of 1 V . The solid line indicates the median current value from all the devices whereas the bands indicate the spread of the measured current across all the devices. Evidentially, the bands from different substrates show a variation in switching threshold, V_{TH} . Figure 4-9e shows a Gaussian distribution of the V_{TH} on all given substrates. Devices on HfO_2 and ZrO_2 show a less negative V_{TH} as compared to devices on Al_2O_3 and AlN . Devices on HfO_2 and AlN are less spread out indicating lower device to device variation. However, the number of functional devices on each substrate varies due to fabrication or processing issues. Overall, devices on Al_2O_3 show the highest yield. Increasing the dielectric constant (κ) of the gate insulator increases the gate capacitance (C_{ins}). A higher C_{ins} reduces the voltage drop across the oxide for a given charge density in the channel, leading to a decrease in V_{TH} . This is beneficial for reducing the power consumption of the device and for enabling lower voltage operations, which is crucial for scaling down device sizes in integrated circuits. From the trend in V_{TH} , we observe a clear dependence on the κ . We now extract the subthreshold slope (SS) from the devices on each of the substrates. Figure 4-9f shows the Gaussian distribution plot for SS and observe a decreasing trend in SS with increasing dielectric constant, κ . A large device to device variation causes the distribution to spread out and this is primarily due to the dielectric quality. The high SS may be correlated to the large interface trap state density at the semiconductor/dielectric interface. We will now compare the output current of the devices on each of the substrates extracted at a given carrier concentration to do a fair comparison of the dielectrics and identify the ideal choice for further development. Figure 4-9g shows the plot of current (I_D) extracted at a given carrier

concentration of $n_s = 1 \times 10^{13} \text{ cm}^{-2}$ as a cumulative distribution function (CDF) for four given dielectrics. A CDF plot for this context will show the probability that the current extracted at this specified carrier concentration falls below a certain value. The x-axis typically represents current levels, and the y-axis represents the cumulative probability. HfO_2 and ZrO_2 , being high- κ materials show higher currents as compared to Al_2O_3 and AlN , given that they provide better gate control, thus, higher drive currents. Al_2O_3 and AlN on the other hand, exhibit curves towards lower drive currents or with less steep slopes, indicating a broader distribution of current outcomes. Although HfO_2 as the dielectric to WSe_2 seems to be the ideal choice, the low yield on this substrate defies the purpose for statistical assessment for other device parameters, primarily, contact resistance. Since Al_2O_3 produces the highest yield, we use Al_2O_3 for all other p-type FET optimization on WSe_2 .

Oxide Capping Layers for Surface Charge Transfer

In addition to engineering the gate dielectric material, researchers have explored the incorporation of thin oxide capping layers as an effective strategy for modulating the threshold voltage in p-type 2D FETs. These capping layers, typically deposited on top of the 2D channel material, can induce significant changes in the device's electronic properties and carrier transport characteristics through surface charge transfer doping and the formation of interfacial dipoles, enabling threshold voltage tunability.

Surface charge transfer doping is a phenomenon where charge carriers (electrons or holes) are transferred between the 2D channel material and the capping layer, effectively modulating the channel's carrier concentration and Fermi level position. This charge transfer can be driven by the work function difference between the two materials or by the formation of charge transfer complexes at the interface.²⁴⁸⁻²⁵⁰ The effectiveness of these oxide capping layers in

modulating the threshold voltage is highly dependent on the specific 2D material system, the deposition techniques, and the interface quality. Careful material selection, process optimization, and interface engineering are crucial for maximizing the benefits of these capping layers and achieving the desired threshold voltage characteristics in p-type 2D FETs. Additionally, the stability and environmental sensitivity of these capping layers must be considered for practical device applications.

The complexity of accurately gauging V_{TH} for ultra-thin TMD materials stems from their sensitivity to environmental changes, which can be affected by various factors such as processing conditions, material quality, residue, and free charge, compounded by a scarcity of comprehensive statistical analyses. In this section, we employed 5 nm thin oxide capping layers to modulate V_{TH} of WSe₂ FETs. The first oxide film, WO₃, is formed by thermal annealing the WSe₂ channel to naturally oxidize the top layer into the native oxide. The second film, MoO_x is deposited via thermal evaporation of high purity MoO₃, and the third film, GeO₂ is initially deposited as Ge and subsequently annealed in air at 225 °C for 15 mins. Prior to electrical characterization, these films were analyzed for stoichiometry and bonding using XPS, with their valence band edges estimated through Ultraviolet Photoelectron Spectroscopy (UPS) to assess band alignment with WSe₂. Then, electrical characterization results show the dependence of variation, V_{TH} , μ_{FE} , and R_C on the channel lengths (L_{ch}). Finally, device characterization is performed to reach higher n_s at maximum V_{ov} , setting a benchmark for p-type 2D FETs.

Figure 4-10a illustrates the process for V_{TH} engineering in mixed contact, bilayer WSe₂ channel FETs, employing oxide capping.^{176,251,252} Figure 4-10b-d show the XPS results, depicting the stoichiometry of the films formed atop a 10 nm Au film on a Si substrate, chosen to minimize oxidation interference from the underlying TMD. The **Appendix** section provides a comprehensive description of sample preparation for XPS and UPS analyses. Samples with all three films were prepared to investigate stoichiometry changes with and without annealing, with

further details available in the **Appendix**. These samples were prepared on top of a thin and stable film of metallic Au sitting on Si/SiO₂ substrate to prevent oxygen migration from underlying films.

For WSe₂-based samples (Figure 4-10b), uncapped samples revealed characteristic W 4f and Se peaks, with a minor presence of oxidized tungsten (likely WO₃) in unannealed samples. Post-annealing, a decrease in total W and Se content was observed alongside oxidized W and a low binding energy Se 3d peak at 53.6 eV. Mo-based samples (Figure 4-10c) exhibited O/Mo ratios consistent with MoO_x ($x \sim 2.9$), though XPS quantification alone couldn't confirm sub-stoichiometry. There was no evidence of reduced Mo valence states in the Mo 3d core level spectra.²⁵³ XPS valence band spectra indicated the valence band maximum was 3.1 eV in good agreement with previous studies.²⁵⁴ This value was 3.3 eV, also in line with previous work. The valence band spectra contained weak band at ~1.0-1.5 eV that has been previously attributed to oxygen vacancies.^{253,255,256} Small amounts of Au are observed due to the signal from under the 10 nm MoO_x film. Ge-based samples (Figure 4-10d) showed both oxidized and metallic germanium post-annealing, with a noticeable Au presence suggesting thinner Ge films, indicating full stoichiometry of Ge and WSe₂ films post-O₂ annealing, while MoO_x films remained slightly non-stoichiometric.

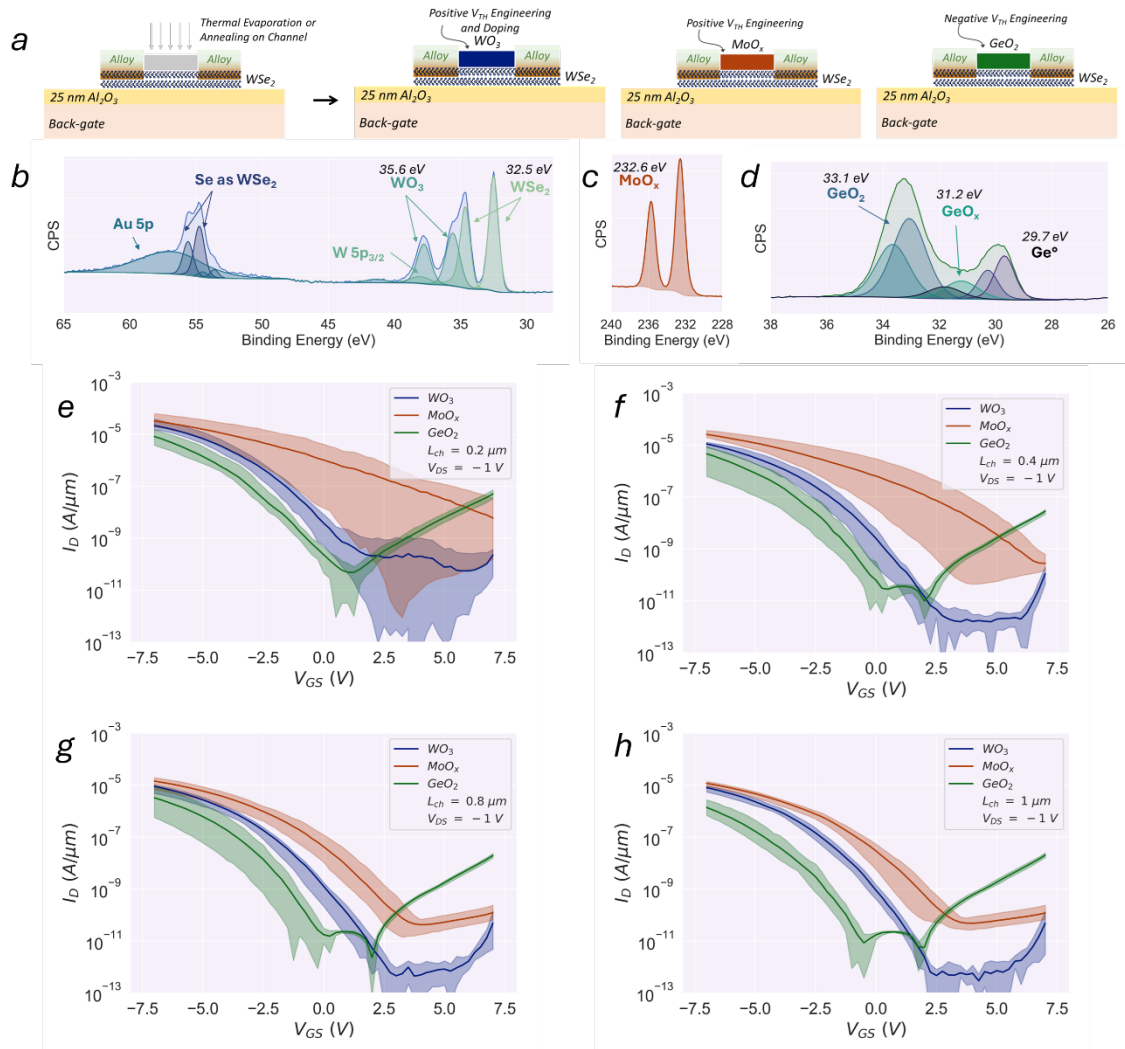


Figure 4-10: Threshold-engineered p-Type WSe₂ FETs: a) Device schematic of the mixed contact, bilayer WSe₂ channel FET and the process for achieving V_{TH} engineering. X-Ray Photoelectron Spectroscopy (XPS) is performed to study the composition of WO₃, MoO_x, and GeO₂ after annealing in the presence of O₂ for 30 minutes at 225 °C in a Rapid Thermal Annealing (RTA) chamber. b) Uncapped WSe₂-based samples show the characteristic W 4f and Se peak confirming the presence of WSe₂. A signal from oxidized W at 35.6 eV and from an unknown low binding energy Se 3d peak at 53.6 eV is noted confirming the presence of WO₃ film. b) Presence of MoO_x is confirmed by the characteristic peak at 232.6 eV. Furthermore, O/Mo ratios and Mo 3d peak shapes appear consistent with MoO_x where x is ~2.9. d) Mixtures of oxidized and metallic germanium for Ge-based samples were detected with the peak for stoichiometric GeO₂ presence detected at 33.1 eV. Electrical characterization is performed on the mixed contact, bilayer WSe₂ FETs capped with WO₃, MoO_x, and GeO₂ for L_{ch} = e) 200 nm, f) 400 nm, g) 800 nm, and h) 1 μm, with all devices measured at V_{DS} = -1 V. Devices capped with MoO_x and WO₃ show a rightward V_{TH} shift whereas devices capped with GeO₂ show a leftward V_{TH} shift.

UPS helped estimate the position of valence band maxima (VBM). For samples with MoO_x , VBM was estimated to be between 2.8 and 3.0 eV. These same gap states observed by XPS were detected by UPS at 1.3 eV. For the other two oxides, WO_3 and GeO_2 , the presence of Au complicated the determination of the VBM because of the signal at the Fermi edge from Au. An approximate value of 0.83 eV was estimated as the VBM for WO_3 , whereas for annealed GeO_2 , VBM was estimated to be 0.97 eV, much higher than that of the unannealed Ge sample further proving the formation of a non-conductive oxide. Steps used to extract VBM from UPS are shown in Figure 4-11.

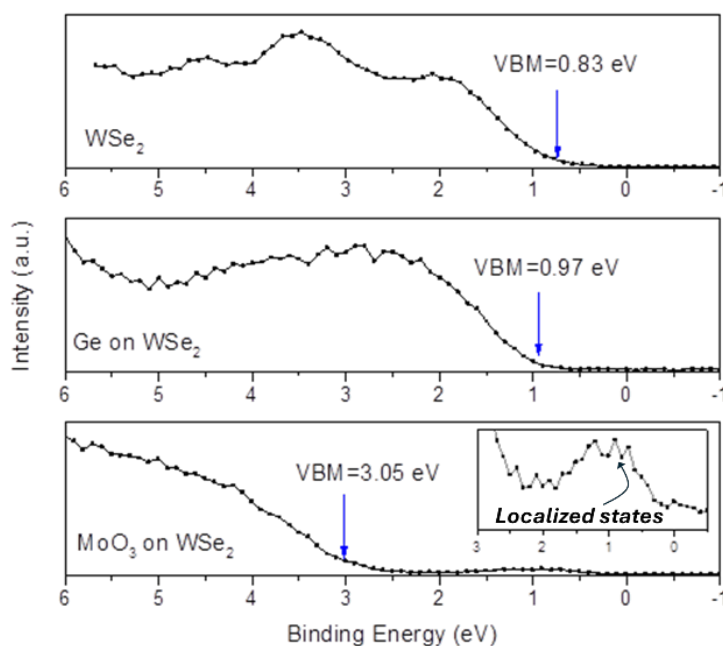


Figure 4-11: Valence Band Maxima (VBM) Extraction from X-ray Photoelectron Spectroscopy (XPS): XPS is performed to analyze the surface of WO_3 , MoO_3 , and GeO_2 films and valence band maxima (VBM) is extracted for the three cases. Presence of localized states in MoO_3 at ~ 1.2 - 1.3 eV suggests the presence of defects in the oxide that may be contributing to the additional charge in the channel which corresponds to the large shift in V_{TH} as well as a higher minimum I_D measured in the positive gate bias, V_{GS} regime.

Electrical characterization revealed distinct transfer curve distributions for WSe₂ FETs with different oxide caps, particularly in V_{TH} shifts, as displayed in Figure 4-10e-h for L_{ch} varying from 200 nm to 1 μ m. MoO_x and WO₃ capped devices exhibited a rightward V_{TH} shifts, while GeO₂ capped devices showed leftward V_{TH} shifts, reintroducing ambipolarity in WSe₂. Although MoO_x capped devices displayed higher ON currents for comparable V_{ov} , an increase in the OFF current was also observed, with notable variation for the below- V_{TH} regime for shorter L_{ch} devices, attributed to the MoO_x's high electron trapping nature. The loss of electrostatic gating or the large shift in V_{TH} for the devices capped with MoO_x at short L_{ch} has been observed earlier.^{252,257} In reports where native oxide formation introduced the shift in V_{TH} , it was attributed to the additional trap charges resulting in degrading SS or shifting V_{TH} , whereas in other reports where MoO_x was evaporated on top of the channel, the loss of gating was attributed to high hole doping capability of the oxide film.^{249,252,258,259} Unlike the other two oxide films, MoO_x film interestingly exhibits localized acceptor states that lie within the electronic bandgap of WSe₂, as supported by evidence from XPS and UPS shown in Figure 4-12.

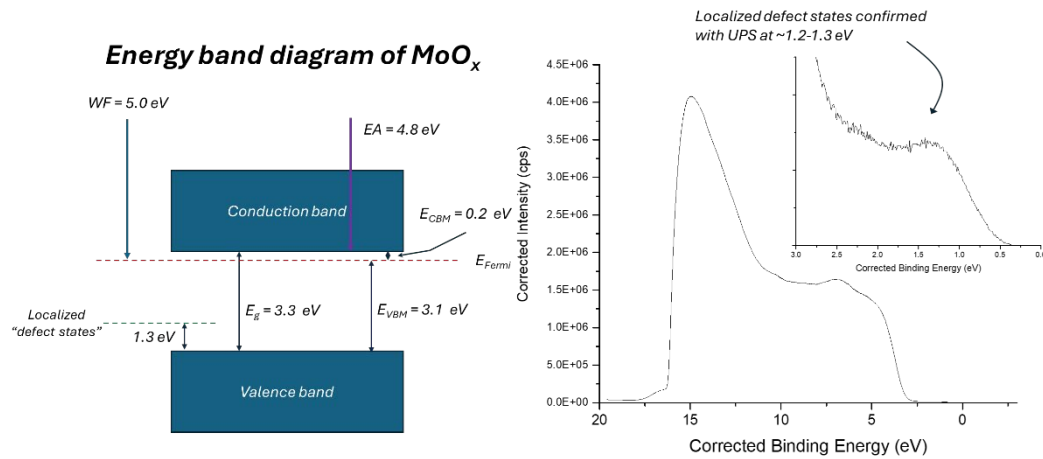


Figure 4-12: Defect Energy Level Estimation: Ultraviolet photoelectron spectroscopy (UPS) results of MoO₃ confirm the presence of localized defect states in the entirety of the MoO₃ film. Furthermore, valence band maxima (VBM) can be extracted from the slope of the binding energy curve at low energies. This helps estimate the band alignment of MoO₃. The MoO_x band structure is determined by combining the VBM and gap state information from XPS and UPS along with

work function (UPS). All measurements were acquired sequentially on the same sample in the same surface science cluster tool. The conduction band minimum was determined by difference $E_g - E_{VBM}$.

Device metrics such as V_{TH} and μ_{FE} are derived from the transfer characteristics for $L_{ch} = 1 \mu m$ given in Figure 4-10h. The variation in V_{TH} , depicted in Figure 4-13a spans from -5 V with GeO_2 capping to 2 V with MoO_x capping, enabling the tunability of device operation between depletion and enhancement mode. Devices capped with MoO_x exhibit an elevated μ_{FE} , as illustrated in Figure 4-13b. The change in carrier density (ΔN) is inferred from the shift in V_{TH} (ΔV_{TH}) observed between devices featuring a bilayer channel with mixed metal contacts and those subjected to the film oxidation process, providing insights into the impact of oxide capping on device performance. Carrier density difference is plotted in Figure 4-13c. It is calculated from the following equation:

$$\Delta N = C_{ox} \frac{\Delta V_{TH}}{q}$$

A positive ΔN may denotes hole doping whereas a negative ΔN denotes electron doping. For devices capped with MoO_x , the substantial variability in V_{TH} with L_{ch} complicates the estimation of ΔN . At the largest L_{ch} , ΔN is roughly estimated to be $+5E12 \text{ cm}^{-2}$ with an average value of $+1E13 \text{ cm}^{-2}$ across different L_{ch} . In contrast, WO_3 capping results in a modest change in ΔN , approximately $+1E12 \text{ cm}^{-2}$. The notable effect of WO_3 capping is the pronounced suppression of electron transport and a decrease in OFF current, potentially due to bandgap widening as the channel transitions from bilayer to single layer, without compromising ON-state performance in the p-type branch. GeO_2 capping leads to a negative ΔN of $-4E12 \text{ cm}^{-2}$, aligning with the leftward shift in V_{TH} . Contact resistance (R_C) was analyzed for FETs with each oxide type post- V_{TH} modification, plotted in Figure 4-13d. With additional oxidation and WO_3 formation did not significantly alter R_C . MoO_x capping did not impact the R_C from $17 \text{ k}\Omega\mu m$ at $n_s = 1.3E13 \text{ cm}^{-2}$, positioning as more suitable for high performance applications compared to

WO₃. GeO₂ capping resulted in an R_C of 90 k $\Omega\mu\text{m}$ at $n_s = 9.3\text{E}12\text{ cm}^{-2}$, offering slightly better performance than WO₃ for the same n_s , albeit with a more pronounced electron transport branch. It must be noted that R_C is extracted by extrapolating from the median of the R_{total} values. Lower R_C values may be extracted when extrapolating with minimum of R_{total} values. Furthermore, large variation in characteristics can also result in noisy and erroneous extraction of R_C , hence, for MoO_x, the R_{total} data for the shortest $L_{ch} = 200\text{ nm}$ was ignored. To leverage our FET stack with its thick dielectric layer, we applied larger gate voltages (V_{GS}) to achieve higher n_s and thereby enhance I_D through improved hole transport.

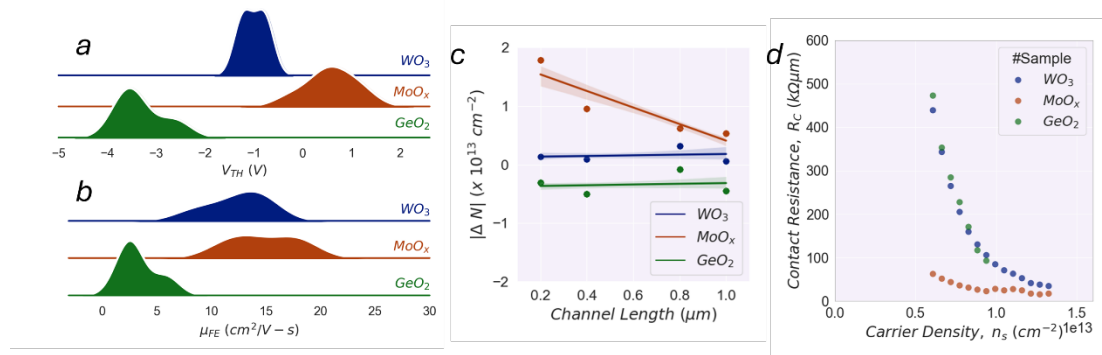


Figure 4-13: Performance Metrics of Oxide-capped WSe₂ FETs: a) Threshold voltage, V_{TH} , extracted from the transfer characteristics for the longest $L_{ch} = 1\text{ }\mu\text{m}$ shows a distinct distribution in the range from -5 V to 2 V, providing with tunability in device operation between depletion mode and enhancement mode device operation. Devices capped with MoO_x achieve a positive V_{TH} with mean around 0.75 V and devices capped with GeO₂ achieve a negative V_{TH} with mean around -3.5 V, whereas devices with WO₃ show only a slight shift in mean V_{TH} . b) Field-effect mobility, μ_{FE} , estimated from the device characteristics with WO₃ and MoO_x show almost no difference confirming that the oxide capping films do not impact transport, however, a sudden drop is noticed for the devices capped with GeO₂ due to lower peak transconductance value. c) Change in channel carrier density (ΔN), is estimated from the change in V_{TH} . ΔN extracted for devices with MoO_x capping shows a large variation and a minimum value of $+5\text{E}12\text{ cm}^{-2}$ is extracted, while devices with GeO₂ capping show a $-4\text{E}12\text{ cm}^{-2}$ change in carrier density due to V_{TH} leftward shift. d) Contact resistance, R_C , is extracted from the FETs. Devices capped with WO₃ exhibit R_C of 34 k $\Omega\mu\text{m}$ at $n_s = 1.3\text{E}13\text{ cm}^{-2}$. Devices with MoO_x capping exhibit R_C of 17 k $\Omega\mu\text{m}$ at the same $n_s = 1.3\text{E}13\text{ cm}^{-2}$. However, a lower R_C for lower n_s is noted in comparison to the devices with the devices with no capping layer. GeO₂ capping yields an R_C of 90 k $\Omega\mu\text{m}$ at a lower $n_s = 9.3\text{E}12\text{ cm}^{-2}$.

Output characteristics for devices with $L_{ch} = 200$ nm are shown in Figure 4-14a-c for the three different oxides. Devices employing MoO_x capping exhibit the highest ON current of up to $160 \mu\text{A}/\mu\text{m}$ at a $V_{GS} = -12$ V and a $V_{DS} = -1.5$ V. Devices capped with WO_3 and GeO_2 demonstrate comparable ON current performances, up to $85 \mu\text{A}/\mu\text{m}$. Figure 4-14d shows the linear scale transfer characteristics of the devices with the three oxide caps measured at $|V_{DS}| = 1$ V. Figure 4-14e shows the logarithmic scale transfer characteristics of the highest performing FET with MoO_x capping. The device reaches a maximum ON current of $\sim 200 \mu\text{A}/\mu\text{m}$ at a $V_{GS} = -14$ V while maintaining a switching ratio of about 7 orders of magnitude. With this, we demonstrate that p-type FETs on WSe_2 are potentially suitable for both high-performance as well as low-power CMOS logic, by tailoring the V_{TH} and $I_{D,max}$ through the choice of oxide capping.

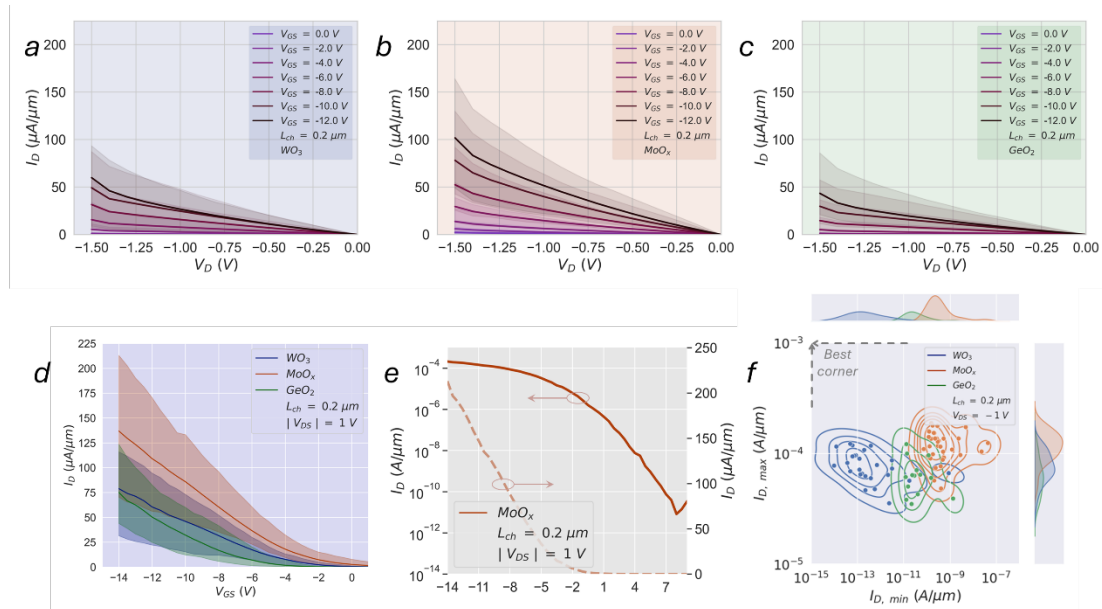


Figure 4-14: High Performance p-Type WSe_2 FETs: Output characteristics for devices with $L_{ch} = 200$ nm for devices with a) WO_3 , b) MoO_x , and c) GeO_2 . Devices with MoO_x capping achieve highest ON current of up to $160 \mu\text{A}/\mu\text{m}$ for the highest $V_{GS} = -12$ V and a $V_{DS} = -1.5$ V. d) Linear scale transfer characteristics of the devices with the three different oxide films measured at $|V_{DS}| = 1$ V. e) Logarithmic and linear scale transfer characteristics of the highest performing FET with MoO_x capping measured at $|V_{DS}| = 1$ V which achieves over $200 \mu\text{A}/\mu\text{m}$ with an $I_{D,max}/I_{D,min}$ ratio of $\sim 1\text{E}7$. f) Plot of $I_{D,max}$ against $I_{D,min}$ shows the distribution of all 200 nm FETs with

different oxide capping layers. Devices with MoO_x achieve a relatively low $I_{D,\max}/I_{D,\min}$ between $1\text{E}4$ and $1\text{E}6$ compared to devices with WO_3 , which achieve a ratio between $1\text{E}9$ and $1\text{E}10$.

As depicted in Figure 4-14f, devices with different caps are assessed for ratio of the maximum to minimum measured current, $I_{D,\max}/I_{D,\min}$. It must be noted that the OFF current in our case is limited by the measurement tool capability and is termed as $I_{D,\min}$. The distribution among the devices is depicted by the contour plot in the main figure and the small gaussian distribution given alongside both the axes.

Finally, V_{TH} tunability of our p-type FETs is explored by employing a oxide capping layers to the bilayer, mixed contact p-type FETs. Through the utilization of three distinct oxide caps— WO_3 , MoO_x , and GeO_2 —each demonstrating unique attributes that influence charge concentration within the semiconductor channel, we tailor device operation and applicability in both high-performance as well as low-power operation. MoO_x is recommended for high-performance p-type FET applications due to its efficacy, while WO_3 and GeO_2 are proposed for V_{TH} engineering, maintaining low OFF currents suitable for low-power applications. Furthermore, we highlight the importance of surface charge films with localized defects engineered to control FET performance, offering a comprehensive approach to p-type FET optimization.

We will now systematically reveal the superiority of 100% coalesced bilayer WSe_2 films over non-uniform bilayer coverage as a key requirement for improved p-type FET performance. We will also investigate the effect of bilayer coverage on the transport properties of p-type WSe_2 2D FETs while also detailing the steps to achieve bilayer synthesis.

Chapter 5

Engineering 2D TMD Layers for Improved p-Type Transport

*Part of this chapter has been reproduced from: **Toward High-Performance p-Type Two-Dimensional Field Effect Transistors: Contact Engineering, Scaling, and Doping.** Aaryan Oberoi, Ying Han, Sergei P. Stepanoff, Andrew Pannone, Yongwen Sun, Yu-Chuan Lin, Chen Chen, Jeffrey R. Shallenberger, Da Zhou, Mauricio Terrones, Joan M. Redwing, Joshua A. Robinson, Douglas E. Wolfe, Yang Yang, and Saptarshi Das, *ACS Nano* **2023** 17 (20), 19709-19723, DOI: 10.1021/acsnano.3c03060*

High device to device variability, high contact resistance, and the absence of an ideal dielectric to 2D FETs hinder their potential for High Volume Manufacturing (HVM).^{260,261} To date, large-scale, high-performance CMOS demonstrations have primarily utilized MoS₂ and WS₂ for n-type FETs and development of p-type 2D FETs is still underway. The lower conduction band minima (CBM) and optimal band gap and band alignment of WSe₂ makes it a promising candidate for p-type FETs, however this exploration on the scalability has only been made possible through significant advancements in large-area growth techniques.^{142,238,262-266} Controlled growth and engineering of device parameters such as contact resistance and threshold voltage remain crucial for their realization in advanced 2D logic. In this study, we follow a material-device co-optimization strategy to underscore bilayer growth for high-performance as well as low-power logic.²⁶⁷ We systematically reveal the superiority of 100% coalesced bilayer WSe₂ films over non-uniform bilayer coverage as a key requirement for improved p-type FET performance. We also investigate the effect of bilayer coverage on the transport properties of p-type WSe₂ 2D FETs while also detailing the steps to achieve bilayer synthesis. Further, we study the role of layer modification by annealing and plasma treatments in oxygen and nitric oxide

environments. We also introduce pre-oxidized layer of Tungsten Oxide at the interface and see the benefits from interface optimization. Finally, we demonstrate high-performance p-type 2D WSe₂ FETs on high- κ dielectric achieving ON current up to 300 $\mu\text{A}/\mu\text{m}$.

Controlled Bilayer Growth of WSe₂

WSe₂ films were synthesized on 2-inch c-plane sapphire substrates using a metal-organic chemical vapor deposition (MOCVD) system within the 2D Crystal Consortium Materials Innovation Platform (2DCC-MIP) at Penn State. By maintaining constant growth conditions, we modulated the WSe₂ layer thickness by varying the deposition time from 20 to 30 minutes. This approach yielded a progressive increase in bilayer coverage from 50% to a complete 100%, with the emergence of multilayer islands across the substrates. Detailed growth parameters are documented in the **Appendix** section.

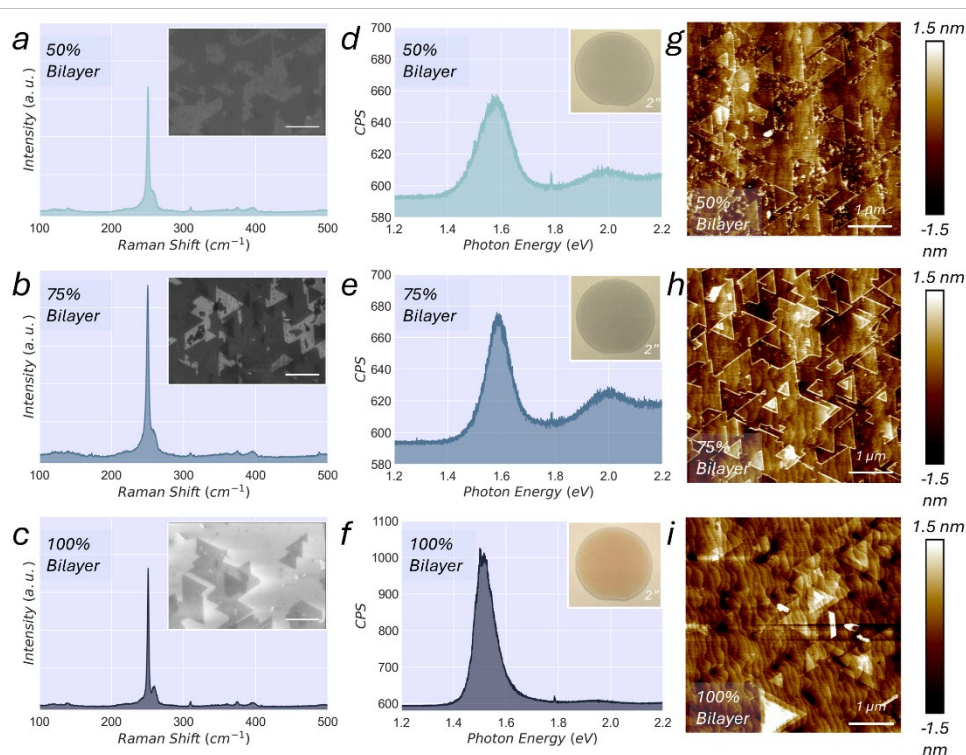


Figure 5-1: Material Characterization of Synthetic Bilayer WSe₂: a-c) Raman characterization of the WSe₂ films on Sapphire show the characteristic peak at 250 cm⁻¹ for all the three samples and an additional peak roughly 10 cm⁻¹ above the characteristic peak shows its prominence with increasing conformality in 100% bilayer WSe₂, as seen in c). Inset SEM images in a-c) show progressively increasing bilayer coverage of WSe₂ on Sapphire and a clear observance of the domain size and orientation can be made. These inset images follow a scale bar of 1 μm. d-f) Photoluminescence (PL) spectra of WSe₂ shows a gradual red shift in the peak position referring to a reduction in the optical bandgap of WSe₂. Inset images in d-f) represent optical images of wafer scale WSe₂ growth performed on 2-inch wafers and a slight variation in contrast from 50% to 100% bilayer coverage is observed. g-i) Atomic Force Microscopy (AFM) performed on the center of the growth wafers of WSe₂ further proves the presence of few bilayers in the sample with 50% bilayer coverage, gradually increasing with 75% coverage, and fully coalescing to form 100% bilayer WSe₂ with islands of multilayer.

Raman and photoluminescence (PL) spectra of as-grown WSe₂ films are depicted in Figure 5-1a-f. The measurement was taken within a N₂-ambient glovebox by Witec Alpha-300 Apyron system, with 532 nm laser (4 mW power). Raman spectra shows the characteristic peak at 250 cm⁻¹ for all the three samples. While other TMDs have characteristic and separate E_g and A_g vibrational modes, WSe₂ vibrational modes are degenerate and therefore overlap at the given laser wavelength.^{237,268,269} PL, on the other hand, shows distinct differences between the samples.

Measured for the 50% and 75% bilayer are single layer regions, with additional quenching in the 75% sample as opposed to the 50%, due to the more homogeneous nature of the sample.²⁷⁰ The 100% bilayer sample shows an enhanced emission compared to that of the single layer, which previous reports have indicated could be due to reduced valley to valley scattering with the addition of strain.²⁷¹ With increasing layers of WSe₂, a red shift in the peak position is observed with increasing layers, denoting a reduction in the bandgap of the WSe₂. However, WSe₂ is exceptionally complex because the minimum energy transition not being equal to the minimum optically allowed transition.^{270,272,273}

Increasing bilayer coverage of WSe₂ flakes can be seen in the SEM images in the inset of Figure 5-1a-c. Insets of Figure 5-1d-f show optical images of the 2" wafers for increasing layer coverage. Atomic Force Microscopy (AFM) is used to study the conformality of the lateral growth and the evolution of the domain sizes with growth times, Figure 5-1g-i. These results further prove the gradual increase of bilayer domains coverage from 50% up to full 100% bilayer WSe₂ with multilayer islands.

p-Type WSe₂ FETs with Pd contacts and Dependence on Bilayer Coverage

WSe₂ films, synthesized via MOCVD, were transferred onto a trio of substrates using a wet transfer technique. The substrates comprise of p⁺⁺-Si/TiN/Pt as the global back gate and 25 nm Al₂O₃ as the gate dielectric. The channel patterning of WSe₂ and the deposition of 40 nm/30 nm thick Pd/Au source and drain electrodes were achieved through electron beam lithography and evaporation techniques, respectively. An illustrative device schematic is presented in the inset of Figure 5-2a.

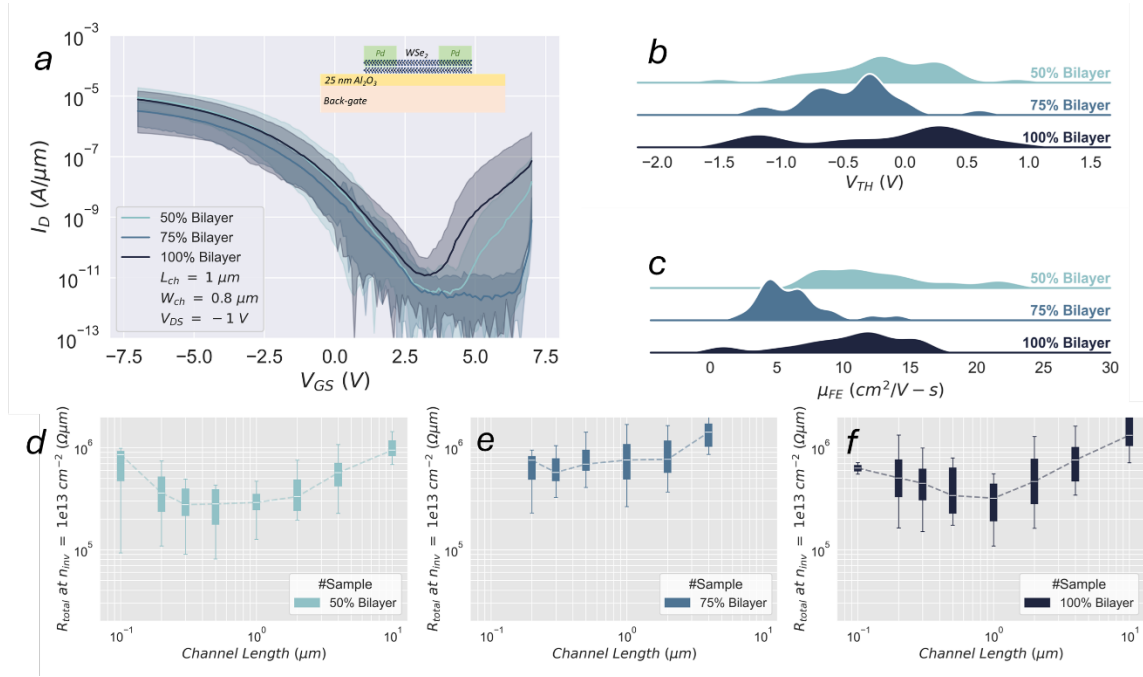


Figure 5-2: Electrical Characterization of p-Type WSe₂ FETs: Back-gated field-effect transistors (FETs) are fabricated on 25 nm Al₂O₃ as the gate dielectric with Pt/TiN/p++-Si as the gate metal. Varying coverage of bilayer WSe₂ are transferred to three different substrates and are then used as channel material while high work-function Pd, capped with Au, are used for source-drain contacts. a) Transfer characteristics of the FETs with $L_{ch} = 1 \mu\text{m}$, measured at $V_{DS} = -1 \text{ V}$, are plotted in the logarithmic scale with the solid line depicting the median transfer curve and the bands depicting the range of the distribution for all the devices. Device schematic is presented in the inset of a). b) Threshold voltage, V_{TH} , is extracted using the iso-current method at $I_{D,iso} = 10 \text{ nA}/\mu\text{m}$ and compared among devices on different channel types. Devices on 100% bilayer WSe₂ show a larger variation as compared to the other two channel types which follow a mean $V_{TH} = -0.25 \text{ V}$. c) Field-effect mobility, μ_{FE} , extracted from the peak transconductance method is estimated. Mean μ_{FE} is extracted to be 12, 6, and $10 \text{ cm}^2/\text{V-s}$ from the three channel types, respectively. d-f) Total resistance, R_{total} , extracted from the three channel types for L_{ch} ranging from 100 nm to $10 \mu\text{m}$ with increasing bilayer coverage as shown in d), e), and f) respectively. R_{total} is extracted for the same carrier density, $n_s = 1\text{E}13 \text{ cm}^{-2}$, and its distribution is represented in a box plot. Solid white line inside the box denotes the median value and box bounds denote the 25th and 75th percentile of the dataset, with line bounds denoting the minimum and maximum values in the dataset.

Electrical characterization of the 3-terminal FETs consistently revealed predominant p-type behavior across all samples. The output current (I_D) is measured at the drain, under a -1 V bias across the drain-source terminals (V_{DS}). The device's switching capabilities are assessed by varying the gate-to-source voltage (V_{GS}), with the drain current indicating hole transport under negative gate bias and electron transport under positive gate bias. Figure 5-2a delineates the

transfer characteristics for devices with a channel length (L_{ch}) of 1 μm , categorized by channel type, represented in the legend. Approximately 20-25 devices per channel type were analyzed, with the spread of their transfer characteristics depicted by semi-transparent bands, and the median performance highlighted with solid lines. The analysis will henceforth focus on the median solid lines for performance insights, while the distribution bands will help elucidate variations that may be stemming from fabrication or growth processes. Devices with 50% and 100% bilayer coverage exhibited comparable p-type conduction, yet the latter also demonstrated noticeable n-type conduction. Conversely, the substrate with 75% bilayer coverage showed a slight reduction in p-type conduction and significantly diminished n-type conduction.

The susceptibility of single layer WSe_2 to surface defects, such as Se vacancies or substitutions, is a critical factor, potentially arising during synthesis, processing, or device fabrication stages. According to density functional theory (DFT) analyses, Se defect sites tend to align closer to the conduction band edge of WSe_2 , potentially enhancing electron transport and introducing variability in FET performance.^{194,217,218,266,274-276} In contrast, 100% bilayer coverage, featuring multilayer WSe_2 islands, could potentially exhibit bulk-like properties. These include elevated carrier mobility due to minimized grain boundary effects and enhanced defect resilience, attributed to the thicker material structure and reduced surface defect impact.

Quantifying defects in WSe_2 films presents a significant challenge, as material characterization techniques tend to alter the sample's inherent properties. Consequently, we focus on analyzing the transport behavior across the three channel types, underpinned by a detailed examination of the electrical data.

Our analysis extends to the device and material parameters derived from the transfer characteristics, which are important in assessing the p-type FETs' performance. We determine the threshold voltage (V_{TH}), which serves as a critical indicator of the transistor's activation voltage, using the iso-current method at a set current of 10 nA/ μm . As depicted in Figure 5-2b, V_{TH} trends

towards more negative values with increased bilayer coverage, suggesting that the multilayer domains necessitate stronger electrostatic control due to charge screening effects. The distribution's multimodal nature possibly reflects the variability in material coverage and layering across the FET channels. It is however important to note that even as layer thickness increases, it has minimal impact on the switching behavior of the FETs.

Further, we evaluate the field-effect hole mobility (μ_{FE}) employing the peak transconductance approach for devices across all substrates, as illustrated in Figure 5-2c. Devices with 50% coverage exhibit the highest μ_{FE} . However, an increase in coverage to 75% leads to a decline in μ_{FE} , potentially due to Coulombic scattering. While Smithe et al. reported negligible impact of small bilayer islands on μ_{FE} , the generalizability of this finding to other TMDs and the observed reduction in μ_{FE} with up to 75% bilayer coverage remain unexplained.²⁷⁷ It is plausible that at significant but incomplete bilayer coverage, the interspaces between domains act as grain boundaries, thereby hindering charge transport. At 100% bilayer coverage, μ_{FE} displays a wide range, with some devices showing markedly low values. Although μ_{FE} is inherently a material characteristic, its dependency on transconductance during extraction could lead to overestimations, particularly in contact-gated devices.^{206,278} Notably, at the highest carrier densities, devices with 100% bilayer coverage channel surpass those with partial bilayer presence, indicating that either metal contact-induced damage, enhanced carrier supply in fully bilayer samples, or reduced current crowding might be more influential factors at elevated carrier concentrations.

It is also crucial to analyze the resistances that impede the carrier injection. This evaluation is done by first measuring the total resistance of the device at a specific overdrive voltage, ensuring a consistent basis for comparison. This is done by reading I_D for any device at the same n_s which is chosen to be $1\text{E}13\text{ cm}^{-2}$. Sheet carrier density is given by the following equation,

$$n_s = qC_{ox}(V_{GS} - V_{TH})$$

where, q is the carrier charge, C_{ox} is the oxide capacitance calculated as the ratio of the oxide dielectric constant and oxide thickness and $V_{GS} - V_{TH}$ can be referred to as the additional overdrive voltage, V_{ov} , required to achieve charge accumulation. We employ statistical box plot representations to analyze the data, with each plot illustrating the median value as a solid white line within the box, the 25th and 75th percentiles as the box boundaries, and the whiskers extending to the dataset's minimum and maximum values, as demonstrated in Figure 5-2d-f. These plots reveal that the total resistances (R_{total}) of devices across all three channel types are remarkably similar, as deduced from the inverse relationship of Ohm's law with the drain current (I_D) at a predetermined overdrive voltage. The non-linear correlation of the R_{total} on the L_{ch} suggests a significant contribution of contact resistance (R_C) on carrier injection into the channel.¹⁴² Further investigation into the contact resistance, R_C , relative to the channel types is depicted in Figure 5-3a, where R_C values are derived using the Y-intercept method from R_{total} for L_{ch} ranging between 100 nm and 10 μm . The data indicates that channels with 50% and 100% bilayer coverage exhibit R_C values of approximately 82 $\text{k}\Omega\mu\text{m}$ and 64 $\text{k}\Omega\mu\text{m}$ at a carrier density of $n_s = 1.4\text{E}13 \text{ cm}^{-2}$, respectively. All channel types achieve similar n_{inv} values suggesting decent gate control. However, the devices on channels with 75% bilayer coverage demonstrates a higher R_C of 126 $\text{k}\Omega\mu\text{m}$ at the same n_s .

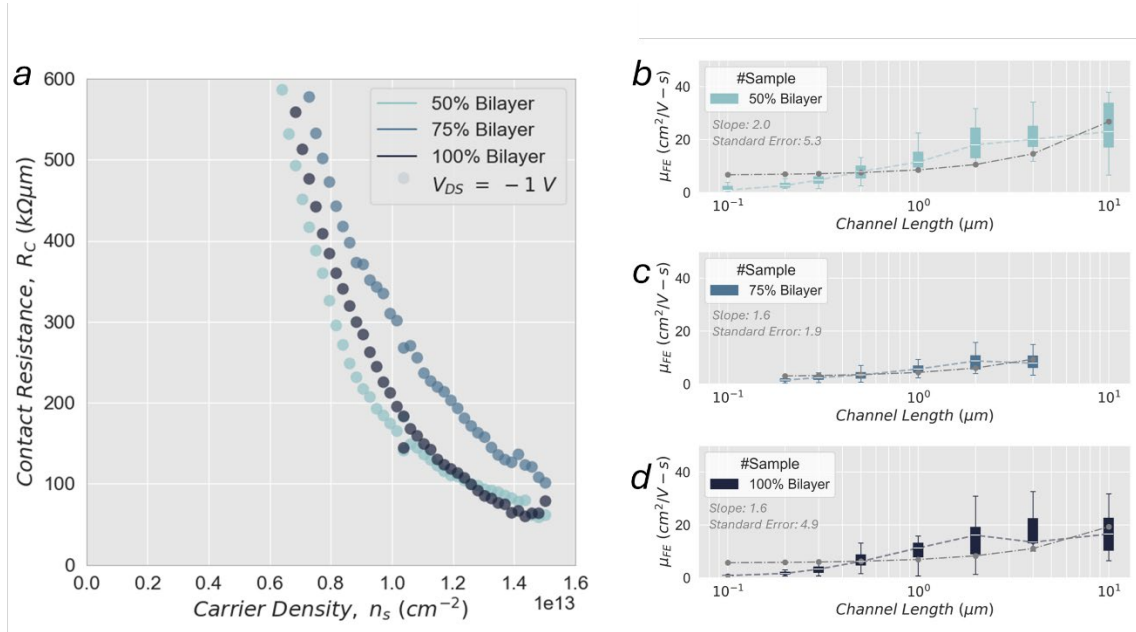


Figure 5-3: Contact Resistance and Mobility Dependence on Channel Length: a) Contact resistance, R_C , is extracted from R_{total} . Devices on 100% bilayer WSe₂ exhibit R_C of 64 $k\Omega\mu m$ at $n_s = 1.4E13 cm^{-2}$, whereas devices on 50% bilayer WSe₂ exhibit R_C of 82 $k\Omega\mu m$ for the same n_s . B-d) Channel properties are further investigated with the plots of μ_{FE} against L_{ch} .

The relationship between the field-effect hole mobility (μ_{FE}) and L_{ch} is also explored in Figure 5-3b-d. The variation of μ_{FE} with L_{ch} could potentially lead to ambiguous conclusions regarding the channel material's quality, as it is influenced by other factors, including the pronounced effect of surface roughness scattering on mobility in layered materials.^{40,279} Interestingly, the devices showed a dependence on the channel width, particularly in the n-type characteristics. Devices with longer width and shorter length showed the highest n-type branch and as the channel length increased, the n-type branch reduced. Following this, the devices with the least n-type conduction would be to design a channel area with short width and long channel, however, the fabrication yield for low width devices is very poor. Figure 5-4 shows the device characteristics for varying widths, lengths, and coverage of WSe₂.

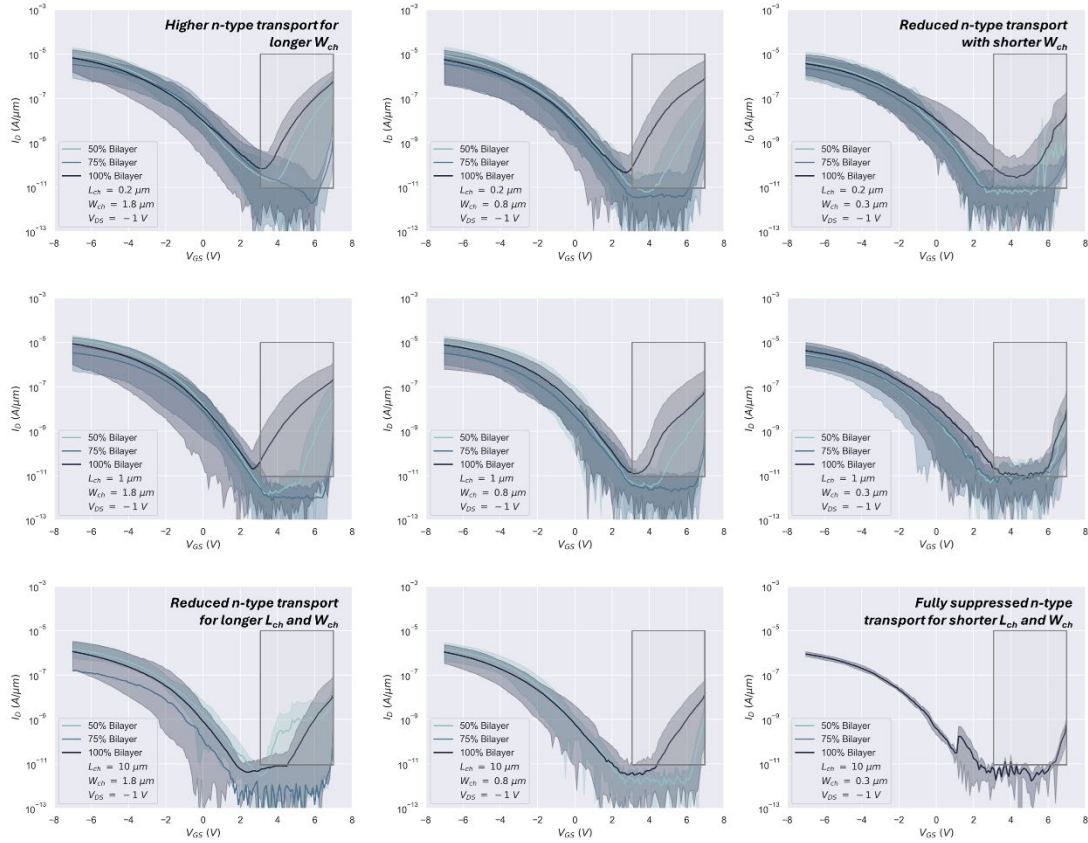


Figure 5-4: Width dependent transfer characteristics for varying thicknesses of WSe₂: An increase in the n-type branch is observed with increasing channel width, W_{ch} . As the channel length, L_{ch} , is reduced along with W_{ch} , n-type transport is almost completely suppressed. This may be correlated to the larger surface area of the channel prone to defects caused during metal evaporation leading to metal-induced gap states (MIGS). This can result in local variations under the contact from Fermi-level pinning.

Based on the discussed results, we identify the channel with 100% bilayer coverage of WSe₂ to be the promising candidate for further development of p-type 2D FETs. We will now identify that the μ_{FE} extracted from contact gated FETs cannot be used as the sole discerning parameter in material identification due to the dependence on the contact quality. In the subsequent section, we aim to further enhance the performance of p-type WSe₂ FETs through contact engineering.

Multilayer WSe₂ and MoSe₂ FETs

Many TMDs exhibit a transition from a direct bandgap in monolayer form to an indirect bandgap in multilayer form. This shift generally involves a reduction in the bandgap energy. In multilayer configurations, TMD films maintain high charge carrier mobilities, though generally lower than their monolayer forms because the presence of multiple layers can also influence the scattering mechanisms of charge carriers. Multilayer TMDs are mechanically more robust compared to their monolayer counterparts. They also tend to have enhanced thermal stability and improved thermal conductivity due to increased layer interactions. Moreover, multilayer TMDs are highly suitable for FETs where high current capacity and stability are required. For the above reasons, we explore p-type FET development on multilayer channels of WSe₂.

Although it can be favorable for p-type FET development, multiple layers in the channel can partially screen the electric field from the gate. This screening effect reduces the influence of the gate voltage on the channel, especially for the layers further from the gate dielectric interface. This leads to a poor subthreshold slope or even a poor ON-OFF ratio in FETs as can be seen in Figure 5-5a-c. With increasing layer thickness, there is no improvement in p-type performance that is observed. These FETs were fabricated on a 10 nm thin Al₂O₃ dielectric with local Ni back-gate. Multi-step transfer process of monolayer MOCVD-grown WSe₂ was carried out to stack layers on top of each other. Due to the loss of electrostatic control, multilayer WSe₂ does not show potential for p-type FET development.

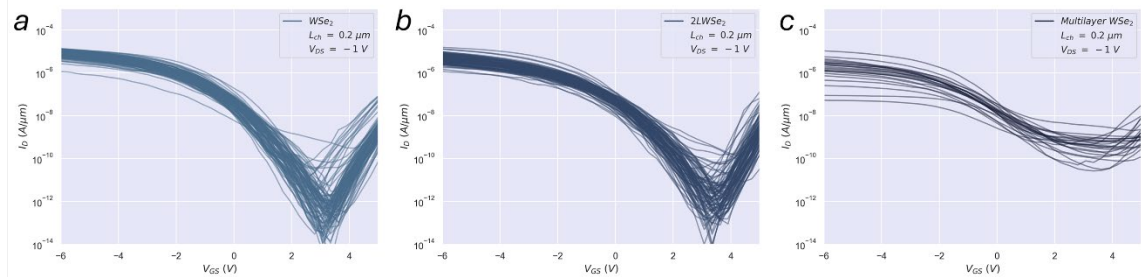


Figure 5-5: Layer Dependent Transport in WSe₂ FETs: FETs were fabricated on local back-gated substrates with 10 nm Al₂O₃ as the dielectric and Ni as the back-gate electrode with channel length of 0.2 μ m and the transfer characteristic sweeps were performed at $V_{DS} = 1$ V. Logarithmic scale transfer characteristics of Pd contacted FET on c) few bilayer WSe₂ showing dominant p-type conduction with ON-OFF ratio, b) double transferred few bilayer WSe₂ showing similar performance and slight reduction in subthreshold characteristics, and c) quadruple-transferred few bilayer WSe₂ which begins to show loss of gating, and degradation in ON-OFF ratio.

Another TMD candidate to develop p-type FETs is Molybdenum Diselenide

(MoSe₂).^{262,280,281} This material offers the same advantage as WSe₂ in that it has a relatively higher valence band maxima than MoS₂ which allows for hole injection despite Fermi level pinning near conduction band. Similar to WSe₂, MoSe₂ also exhibits a transition from an indirect to a direct bandgap as it is thinned down to a monolayer, with the bandgap of monolayer MoSe₂ being around 1.55 eV. The slightly smaller bandgap compared to WSe₂ can influence its electronic and optical properties, potentially offering advantages in applications requiring lower energy photon absorption and emission. While MoSe₂ generally has lower mobility for holes compared to WSe₂, it still maintains respectable levels that are adequate for many electronic applications. The slightly lower mobility can sometimes be compensated for by other factors such as stability or ease of growth. Both MoSe₂ and WSe₂ exhibit good environmental stability, but MoSe₂ tends to be slightly more resistant to oxidation than WSe₂. Although slightly less common as p-type compared to WSe₂, MoSe₂ can still be engineered to exhibit good p-type characteristics. Research into optimizing the contact engineering and surface treatments can enhance its p-type performance, making it a viable alternative.

Here, we tested the electrical performance of MoSe₂ grown using chemical vapor deposition (CVD) on SiO₂ substrate. Large-area grown MoSe₂ was transferred using the wet-transfer process. Since the film was not coalesced, the domains were star-shaped and very clearly visible optically as can be seen in Figure 5-6a. In some cases, the film folded into itself during the transfer process, leading to multilayer formation, shown in Figure 5-6b. Following that, the

channel was isolated from the rest of the flake and contacts were patterned using e-beam lithography and Pd contacts were deposited. The channel length in this case is $0.2\ \mu\text{m}$. On comparing the electrical results on both the devices, we observe a stark difference in the p-type branch. Device on multilayer MoSe₂ reached an I_{DS} of $1\ \mu\text{A}/\mu\text{m}$. Although further characterization may be useful, the presence of an n-type branch limits further development.

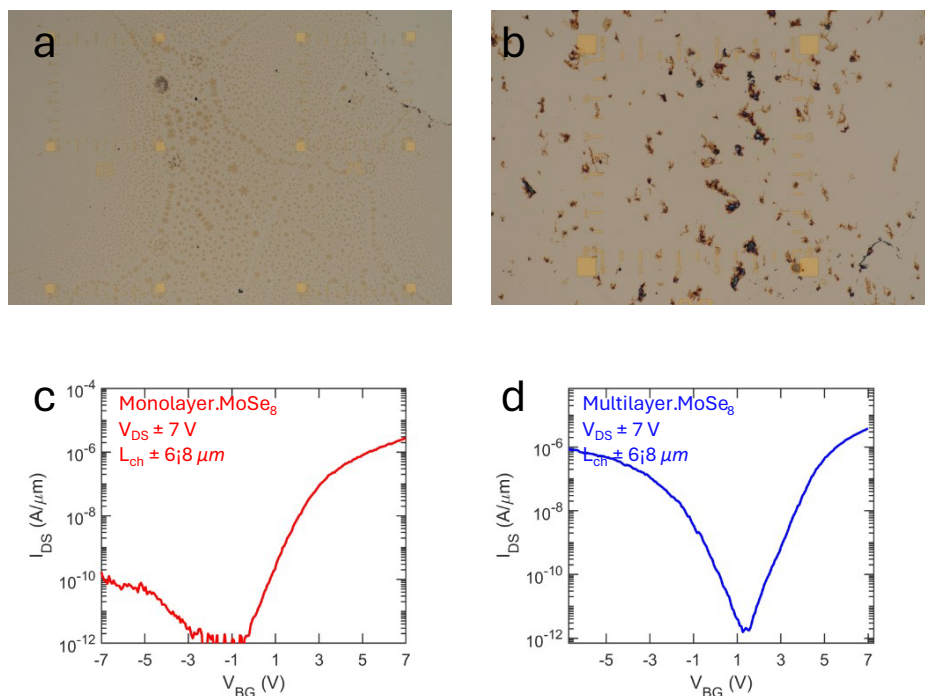


Figure 5-6: Layer Dependent Transport in MoSe₂ FETs: Optical image of as-transferred CVD grown a) monolayer MoSe₂ flakes, b) Multilayer, folded MoSe₂ flakes on back-gate substrate with 25 nm Al₂O₃ as the dielectric. Logarithmic scale transfer characteristics of Pd contacted FET on c) monolayer MoSe₂ showing dominant n-type conduction, and d) multilayer MoSe₂ showing enhanced p-type conduction. The channel length is $0.2\ \mu\text{m}$ and the devices were biased at $V_{DS} = 1\text{ V}$.

Transition Metal Oxide Layer Doping

In the chapter on contact engineering p-type FETs on WSe₂, it was noted that the ON-state performance of Pd-contacted WSe₂ FETs was although improved by aggressively scaling

L_{ch} from 1 μm down to ~ 20 nm, ultra-scaled FETs were still contact limited. By scaling L_{ch} to ~ 20 nm $I_{DS,P,median}$ was improved by $\sim 10\times$ to ~ 890 nA/ μm from the unoptimized Pd contacts shown in Figure 3-5. We also found that the contact resistance (R_C) dominates for aggressively scaled Pd contacts to WSe₂ devices with $L_{ch} < 200$ nm. The contact resistance (R_C) extracted using the conventional transfer-length method (TLM) was found to be ~ 360 k Ω μm for carrier concentration (n_s) of $\sim 1 \times 10^{13}$ cm⁻². To reduce R_C and improve $I_{DS,P}$, we exploited a surface charge transfer doping (SCTD) strategy where the top-layer of bilayer WSe₂ channel was converted into WO_xSe_y using a self-limiting oxidation process. The monolayer WO_xSe_y enables *p*-type doping of the underlying monolayer WSe₂, which not only increases the median value for $I_{DS,P}$ by another $\sim 5\times$ to ~ 4 $\mu\text{A}/\mu\text{m}$ but also improves the metal-semiconductor interface and reduces R_C by $\sim 9\times$ to ~ 40 k Ω μm . A “champion” *p*-type WSe₂ FET with Pd contacts and monolayer WO_xSe_y dopant layer was able to achieve I_{ON} as high as ~ 10 $\mu\text{A}/\mu\text{m}$ for $L_{ch} = 20$ nm while maintaining a current on/off ratio of $>10^5$. We also show the applicability of our *p*-type SCTD technique to other 2D materials such as MoS₂, MoTe₂, and MoSe₂.

Monolayer Dopant by Layer Reduction from Bilayer WSe₂

In order to unlock the full potential of aggressively scaled WSe₂ FETs, it is critical to reduce R_C . As demonstrated in Figure 3-6, thinning of λ_{SB} using electrostatic gating alone is insufficient for the realization of a low- R_C contact to WSe₂ in spite of optimization of the contact metal. However, further reduction is possible through the introduction of doping. Here, we exploit SCTD using monolayer *p*-type dopants to demonstrate significant performance enhancement for aggressively scaled WSe₂ FETs. Note that several previous reports have suggested the use of transition metal oxides (TMOs) as *p*-type dopant for TMDs. For example, Chuang *et al.*²⁸² demonstrated *p*-type MoS₂ FETs by depositing sub-stoichiometric molybdenum

trioxide as a charge transfer interlayer between Pd contact and the semiconducting MoS₂ channel. It is also possible to convert TMDs into their corresponding TMOs using methods such as annealing in air, ozone (O₃) treatment, or exposure to O₂ plasma. In our previous study,²⁸³ we have realized *p*-type 2D FETs based on exfoliated MoS₂, WSe₂, MoTe₂, MoSe₂, and WS₂ by controllably transforming top few layers of multilayer TMD flakes into their corresponding TMOs. In a similar study based on exfoliated WSe₂ flakes, Pang *et al.*²⁸⁴ used atomistic imaging to show that the oxidation process can occur laterally and can spread beyond the channel area being exposed to underneath the contacts. Finally, Choi *et al.*²⁸⁵ demonstrated that large area grown monolayer WSe₂ transferred onto monolayer graphene could be controllably oxidized using UV-O₃ leading to improved carrier mobility in graphene.

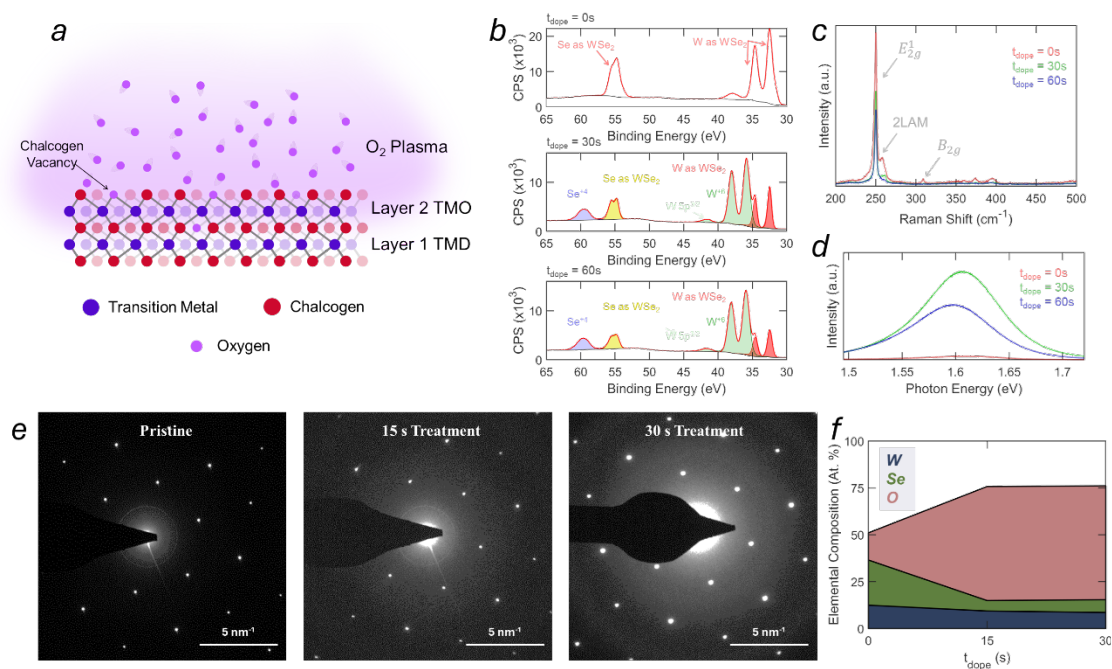


Figure 5-7: Monolayer *p*-type dopant for WSe₂ FETs: a) Schematic of a self-limiting oxidation process that converts the top-layer of the bilayer WSe₂ into sub-stoichiometric WO_xSe_y, which in turn *p*-dopes the remaining monolayer WSe₂. b) X-ray photoelectron spectroscopy (XPS), c) Raman, and d) photoluminescence (PL) spectrum of pristine bilayer WSe₂ and after the sample was treated with oxygen plasma for a total duration of 30 s and 60 s. e) SAED for the pristine and post O₂ plasma treated bi-layer WSe₂ film viewed down its *c*-axis. f) Elemental content is mapped from

a small portion in the bilayer WSe₂ film, and its composition is studied with increasing oxygen plasma duration. Clearly, the oxygen content of the film increases during the plasma treatment.

Here, we adopt the above-mentioned strategy and demonstrate a self-limiting oxidation process that converts the top-layer of the bilayer WSe₂ into sub-stoichiometric WO_xSe_y, which in turn *p*-dopes the remaining and underlying monolayer WSe₂ as shown schematically in Figure 5-7a. Figure 5-7b-d, respectively, show the XPS, Raman, and photoluminescence (PL) spectrum of pristine bilayer WSe₂ and after the sample was treated with oxygen plasma for a total duration of 30 s and 60 s. In Figure 5-7b, the XPS of the virgin film shows only W 4f and Se 3d peaks due to the presence of WSe₂. The Se:W is consistent with WSe₂ at the value of 2.0. At 30 sec and 60 sec, we see evidence of an increasing proportions of both W⁶⁺ and Se⁴⁺ and increase in oxygen. These observations are consistent with the presence of WO₃ and SeO₂ or WO_xSe_y. In the Raman spectrum shown in Figure 5-7c, the *B*_{2g} mode found at ~310 cm⁻¹ confirms that the pristine film consists of more than one layer prior to the O₂ plasma treatment. This peak disappears after 30 s of O₂ plasma treatment, indicating that the top layer of WSe₂ was oxidized. Some reduction in the intensity of the degenerate *E*_{2g}¹ peak and the 2LAM was noted, but their presence implies that the bottom layer of WSe₂ remains after 30s of oxygen plasma treatment. Subsequently, 60 s of oxygen plasma treatment causes a further reduction in the intensity of the *E*_{2g}¹ peak while the 2LAM becomes nearly indistinguishable from the noise floor. Photoluminescence spectra in Figure 5-7d shows that the intensity of the A excitonic peak increases significantly after 30 s of oxygen plasma treatment, which may be a result of the WSe₂ film transitioning from bilayer to monolayer. Furthermore, it is evident that 60 s of oxygen plasma treatment causes degradation of the A excitonic peak intensity which is accompanied by a slight reduction in the peak position, i.e., the photon energy where the peak reaches its maximum intensity.

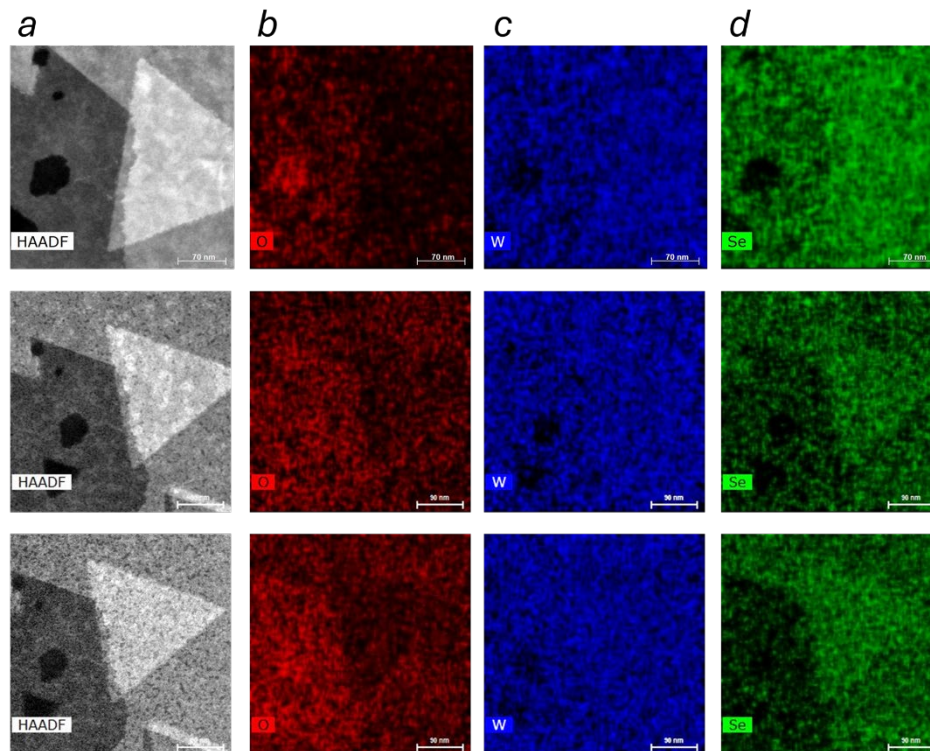


Figure 5-8: Qualitative HRSTEM analysis of WSe₂ film with increasing oxygen plasma treatment: a) HRSTEM images of WSe₂ film with bilayer islands clearly showing the impact of oxygen plasma treatment on the film. Element mapping with EDS is performed for b) oxygen, c) tungsten, and d) selenium showing increase in oxygen concentration and reducing selenium concentration providing further evidence for the formation of an amorphous layer of WO_xSe_y.

Figure 5-7e show the SAED patterns for the pristine and post O₂ plasma treated bi-layer WSe₂ film viewed down its c-axis. The film shows progressive reaction with oxygen species as a function of plasma exposure time. Slight amorphization of the film is apparent from the diffraction patterns, for which diffraction spots appear more diffuse and the amorphous halo at the center of the patterns appears to grow. Also, the film evolves to form a landscape of monolayer, bilayer, and multi-layer regions at the nm scale. Additionally, Figure 5-8 shows the EDS maps as a function of the O₂ plasma exposure time. Clearly, the oxygen content of the films increases during the plasma treatment. Figure 5-7f shows the evolution in elemental composition mapped with EDS from a bilayer region in the WSe₂ film. The oxygen content in the pristine sample is highest within a hole in the film, which suggests that the oxygen signal originates from

residual oxygen on the lacey carbon film on the TEM grid, not from the film itself. After the oxygen plasma treatment, the hole disappears in the oxygen map, and the oxygen content is more uniform across the film, indicating that the oxygen is present within the film after treatment. This suggests that WO_xSe_y is formed across the entire film during exposure to oxygen plasma.

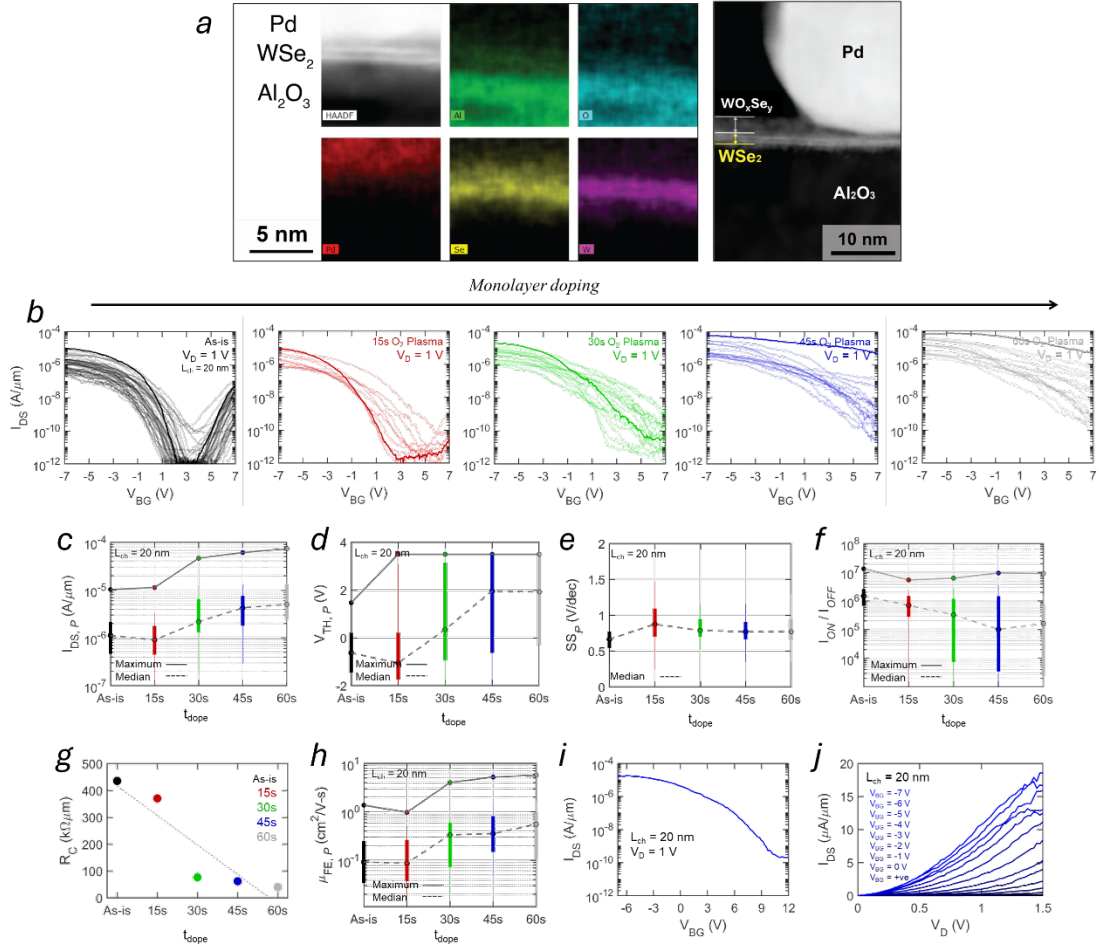


Figure 5-9: High-performance WSe_2 FETs with monolayer dopant: a) Cross sectional HRTEM image and the corresponding EDS elemental mapping of the contact region for a post oxygen plasma-treated p-type WSe_2 FET. b) Transfer characteristics of as fabricated WSe_2 FETs with $L_{\text{ch}} = 20$ nm and after exposure to O_2 plasma for $t_{\text{dope}} = 15, 30, 45$ and 60 seconds. The device with highest $I_{\text{DS,P}}$ measured at $V_{\text{BG}} = -7$ V is marked in bold while the other devices are shaded. Note that the electron branch is severely suppressed even after 15 s of plasma treatment. Box plots for c) $I_{\text{DS,P}}$ measured at $V_{\text{BG}} = -7$ V, d) extracted $V_{\text{TH,P}}$ at an iso-current of 100 nA/μm, e) SS_P for two orders of magnitude change in I_{DS} , and f) current on/off ratio ($I_{\text{ON/OFF}}$) as a function of t_{dope} across all WSe_2 FETs with $L_{\text{ch}} = 20$ nm. g) Extracted R_C values before and after O_2 -treatment. Clearly, with increasing exposure time, R_C improves by $\sim 10\times$ from ~ 435 kΩμm to ~ 40 kΩμm. This

indicates that the oxidation process can laterally extend to underneath the contacts leading to an improved interface between Pd and WSe₂. h) Extracted $\mu_{FE,P}$ as a function of L_{ch} before and after the self-limiting oxidation of bilayer WSe₂. An increase in $\mu_{FE,P,median}$ is observed across all scaled L_{ch} values. i) transfer and j) output characteristics of the best performing p-type WSe₂ FETs with $L_{ch} = 20$ nm.

Figure 5-9a shows the cross-sectional STEM-HAADF image and the corresponding EDS elemental mapping of the contact region for a post oxygen plasma-treated p-type WSe₂ FET. An amorphous layer of WO_xSe_y can be seen on top of crystalline WSe₂ channel. Figure 5-9b shows the transfer characteristics of as fabricated WSe₂ FETs with $L_{ch} = 20$ nm and after exposure to O₂ plasma for $t_{dope} = 15, 30, 45$ and 60 seconds, respectively. The device with highest $I_{DS,P}$ measured at $V_{BG} = -7$ V is marked in bold while the other devices are shaded. Note that the electron branch is severely suppressed even after 15 s of plasma treatment. Figure 5-9b-e, respectively, show the box plots for $I_{DS,P}$ measured at $V_{BG} = -7$ V, extracted $V_{TH,P}$ at an iso-current of 10 nA/ μ m, SS_P for two orders of magnitude change in I_{DS} , and current on/off ratio (I_{ON}/I_{OFF}) as a function of t_{dope} across all WSe₂ FETs with $L_{ch} = 20$ nm. The increasing trend in $I_{DS,P}$ in Figure 5-9b and $V_{TH,P}$ in Figure 5-9c are observed until a total exposure time of 45s. A total of $\sim 5\times$ increase in $I_{DS,P,median}$ and $\sim 7\times$ increase in $I_{DS,P,max}$ and a shift of ~ 2.5 V in $V_{TH,P,median}$ are observed. However, at 60 seconds of exposure, there is no further improvement in $I_{DS,P,median}$ or change in $V_{TH,P,median}$ indicative of self-limiting oxidation of the top-layer of bilayer WSe₂. Note that there is a slight increase in the $SS_{P,median}$ from ~ 660 mV/decade to ~ 770 mV/decade as seen in Figure 5-9d between the pristine and 15 s O₂ plasma treated WSe₂ FETs, which can be attributed to the higher affinity of adsorbents towards amorphous and sub-stoichiometric WO_xSe_y leading to more interface trap states.

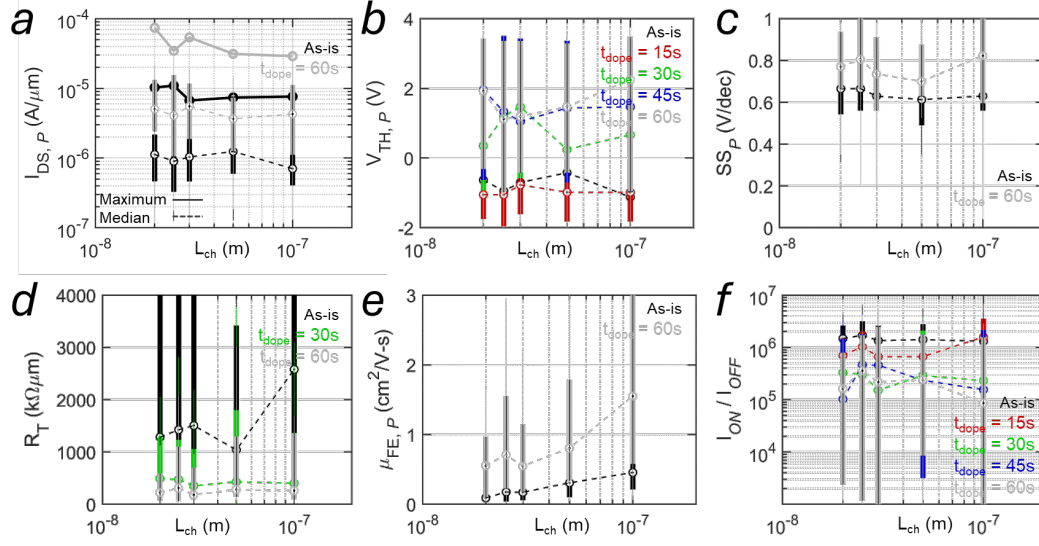


Figure 5-10: Impact of doping on scaled WSe₂ FETs: a) Box plot for $I_{DS,P}$ measured at $V_{BG} = -7$ V for $V_D = 1$ V as a function of L_{ch} before and after 60s of oxygen plasma treatment. b) Box plot for $V_{TH,P}$ as a function of L_{ch} with increasing t_{dope} . $V_{TH,P,median}$ is observed to steadily increase for all L_{ch} . c) Box plot for SS_P as a function of L_{ch} before and after $t_{dope} = 60$ s. $SS_{P,median}$ shows a ~ 200 mV/decade increase. d) Box plot for R_T as a function of L_{ch} before and after $t_{dope} = 30$ and 60s. $R_{T,median}$ reduces from ~ 1280 k $\Omega\mu m$ to ~ 220 k $\Omega\mu m$ after $t_{dope} = 60$ s for $L_{ch} = 20$ nm. e) Box plot for $\mu_{FE,P}$ as a function of L_{ch} before and after $t_{dope} = 60$ s. An increase in $\mu_{FE,P,median}$ is observed after $t_{dope} = 60$ s across all scaled L_{ch} . For $L_{ch} = 100$ nm, $\sim 3X$ increase in $\mu_{FE,P,median}$ reaching ~ 1.5 cm²V⁻¹s⁻¹ after doping is observed. f) Box plot for I_{ON}/I_{OFF} as a function of L_{ch} with increasing t_{dope} .

The decrease in the median value of I_{ON}/I_{OFF} from $\sim 1.5 \times 10^6$ to $\sim 1.6 \times 10^5$ seen in

Figure 5-9e is a direct consequence of more positive $V_{TH,P}$ and increased SS_P . Figure 5-10 shows similar analysis done for different L_{ch} . Figure 5-9f shows the extracted R_C values before and after O₂-treatment. Clearly, with increasing exposure time, R_C improves by $\sim 10\times$ from ~ 435 k $\Omega\mu m$ to ~ 40 k $\Omega\mu m$. This indicates that the oxidation process can laterally extend to underneath the contacts leading to an improved interface between Pd and WSe₂, which agrees with previous findings. Figure 5-9g shows the extracted $\mu_{FE,P}$ as a function of L_{ch} before and after the self-limiting oxidation of bilayer WSe₂. An increase in $\mu_{FE,P,median}$ is observed across all scaled L_{ch} values. For $L_{ch} = 100$ nm, $\sim 3X$ increase in $\mu_{FE,P,median}$ from ~ 0.45 cm²V⁻¹s⁻¹ to ~ 1.5

$\text{cm}^2\text{V}^{-1}\text{s}^{-1}$ after doping is observed. Finally, Figure 5-9h-i, respectively, show the transfer and output characteristics of the best performing *p*-type WSe₂ FETs with $L_{\text{ch}} = 20 \text{ nm}$. It is important to note that the device completely turns OFF when V_{BG} is swept to 12 V. $I_{\text{DS},\text{p}}$ reaches $\sim 16 \mu\text{A}/\mu\text{m}$ for $V_{\text{D}} = 1.0 \text{ V}$ at $V_{\text{BG}} = -7 \text{ V}$. Stability of the scaled and doped *p*-type WSe₂ FETs is demonstrated in Figure 5-11. Figure 5-9j shows the corresponding output characteristics of the best performing *p*-type WSe₂ FET. Non-linear current-voltage dependence is observed due to the SB-limited nature of the contacts.

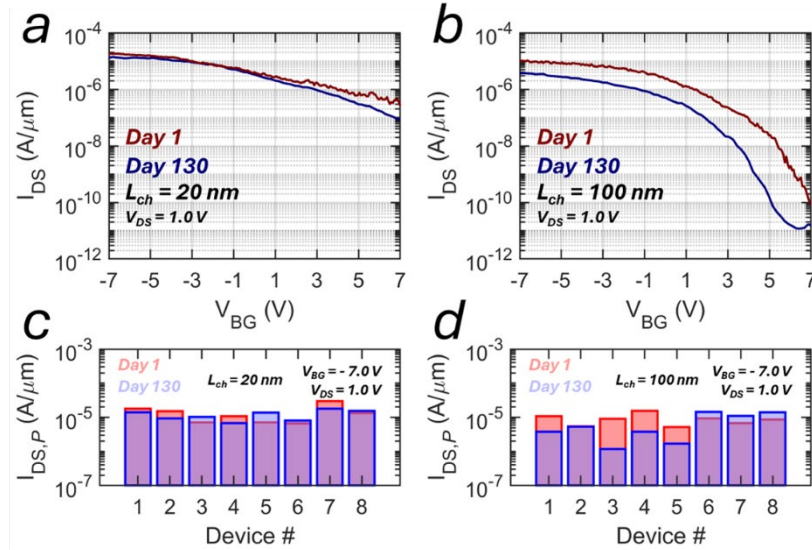


Figure 5-11: Air-stability of doped-WSe₂ p-type FETs: Transfer characteristics of *p*-type WSe₂ FETs that were doped for the maximum duration of $t_{\text{dope}} = 60 \text{ s}$, measured at $V_{\text{DS}} = 1 \text{ V}$ for devices with a) $L_{\text{ch}} = 20 \text{ nm}$ and b) $L_{\text{ch}} = 100 \text{ nm}$ respectively. The transfer curves in blue denote the measurement performed immediately after the channel was exposed with O₂ plasma whereas the transfer characteristics in red denote the measurement performed after the devices were left in ambient for 130 days. Slight decrease in ON current is noticed from device statistics for c) $L_{\text{ch}} = 20 \text{ nm}$ and d) $L_{\text{ch}} = 100 \text{ nm}$ with greater decrease observed for $L_{\text{ch}} = 100 \text{ nm}$ which corresponds to the greater channel area exposed.

Figure 5-12a-b show the transfer characteristics for pre- and post-O₂ plasma treated FETs based on exfoliated multilayer MoS₂ and large area MOCVD grown three-layer (3L) MoS₂, respectively. These MoS₂ FETs were fabricated with Ni contacts and with 50 nm Al₂O₃ as the

gate dielectric. Clearly, no p -type transport is observed in the as-fabricated device characteristics. However, the p -branch emerges after treatment with mild O_2 plasma. We were able to achieve $I_{DS,P}$ of $\sim 50 \text{ nA}/\mu\text{m}$ for the exfoliated multilayer MoS_2 and $\sim 40 \text{ nA}/\mu\text{m}$ for the MOCVD grown 3L MoS_2 . Note that it is difficult to suppress the n -type transport in MoS_2 due to the phenomenon of metal Fermi-level pinning near the conduction band of MoS_2 . We also test the self-limiting oxidation based doping strategy on FETs fabricated on large area CVD grown few layer MoSe_2 contacted with Pd on 25 nm Al_2O_3 as the gate dielectric as shown in Figure 5-12c. Here, upon exposure to O_2 plasma, slight improvement in p -type transport is observed and significant reduction in the n -branch is noted. Exposure for longer duration resulted in damage to the multilayer MoSe_2 FETs. Finally, the SCTD strategy is tested on exfoliated multilayer MoTe_2 with Pd contacts and 50 nm of Al_2O_3 as the gate dielectric as shown in Figure 5-12d. Since MoTe_2 is known to be very prone to oxidation, we perform only a mild UV- O_3 treatment to test the strategy. Even slight exposure causes the top few layers to convert to their native oxide and introduces p -type doping for the MoTe_2 channel underneath. However, it becomes difficult to turn the device OFF likely due to degenerate doping.

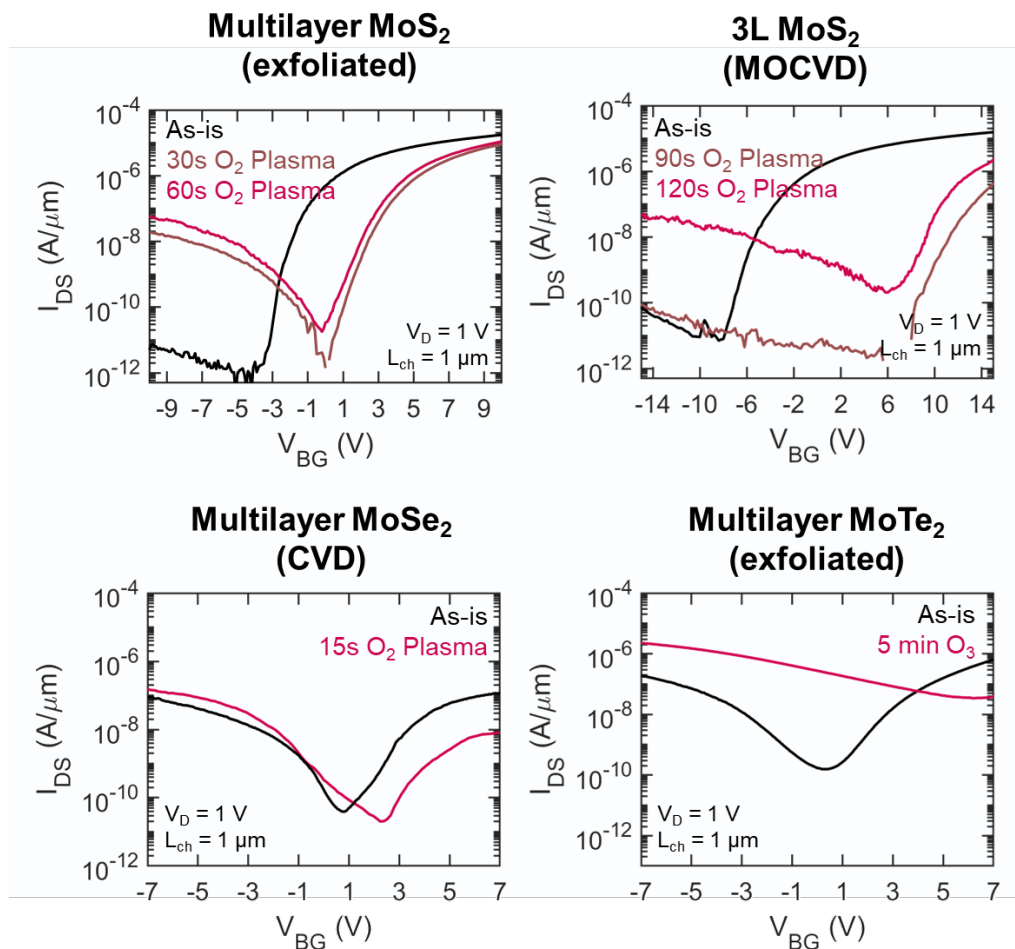


Figure 5-12: Monolayer p-type doping for various TMDs: As-fabricated and post-doping transfer characteristics of FETs based on a) exfoliated multilayer MoS₂, and b) large area grown three-layer (3L) MoS₂ with Ni contacts on 50 nm of Al₂O₃ as gate dielectric. c) As-is and post-doping transfer characteristics of large area grown, multilayer MoSe₂ with Pd contacts on 25 nm of Al₂O₃ gate dielectric. d) As-is and post-doping transfer characteristics of FET on multilayer, exfoliated MoTe₂ with Pd contacts on 25 nm Al₂O₃ gate dielectric. A mild UV-O₃ treatment was used for MoTe₂ owing to its greater propensity for oxygen.

To overcome this, we also pattern the side areas of the channel close to the contacts such that we create a $p^+ - i - p^+$ doping profile as shown in Figure 5-13.

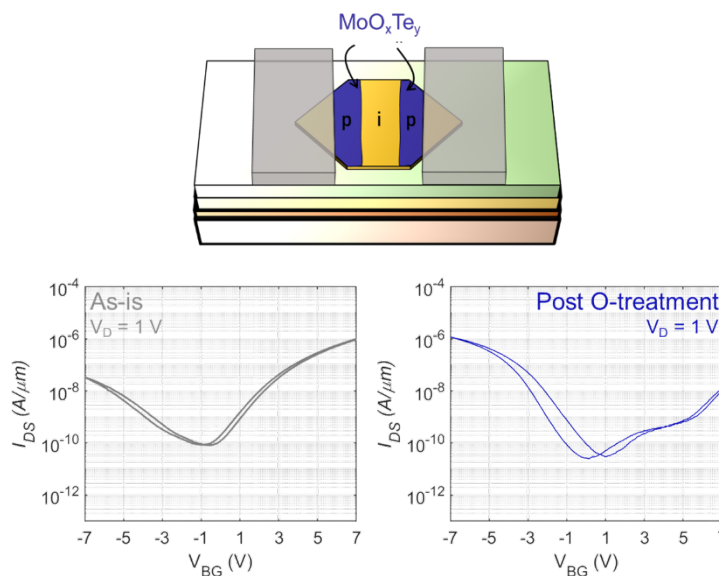


Figure 5-13: Selective profile doping of MoTe₂ FET. As-is MoTe₂ FET characteristics showing ambipolar transport. Selective doping and R_C reduction near contacts from oxygen-based doping. Since MoTe₂ is prone to oxidation, even slight exposure causes the top few layers to convert to their native oxide (MoO_xTe_y) which tends to dope the MoTe₂ channel underneath. Owing to the small bandgap of MoTe₂, it becomes difficult to turn the device OFF after the device is degenerately doped p-type. Selective patterned doping of side regions near contacts to create a p⁺-i-p⁺ doping profile helps switch the MoTe₂ FET OFF.

We also explored alternative oxidation processes for the *p*-type SCTD doping. Figure 5-14a shows electrical characterization of FETs based on exfoliated multilayer WSe₂ with Pd contacts fabricated on 50 nm of Al₂O₃ as gate-dielectric before and after treatment with UV-Ozone (O₃). Similarly, Figure 5-14b shows another exfoliated multilayer WSe₂ FET with the same structure and physical dimension, before and after annealing in O₂ atmosphere. In both cases, as-fabricated FETs show ambipolar characteristics with a dominant n-type transport. Device exposed to O₃ for 25 mins shows a slight improvement in p-branch ON current (~5X) with I_{DS} reaching 5 nA/μm, whereas device annealed at 250 °C in O₂ atmosphere show a major improvement in the ON current (~1000X) with I_{DS} reaching 10 μA/μm.

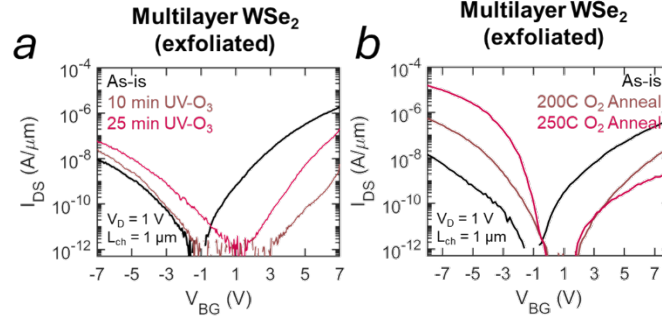


Figure 5-14: Other oxidation approaches for monolayer doping: a) FET on exfoliated, multilayer WSe₂ with Pd contacts fabricated on 50 nm of Al₂O₃ is treated with mild UV-Ozone (O₃) exposure for $t_{\text{dope}} = 10$ mins and $t_{\text{dope}} = 25$ mins. Slight improvement in $I_{DS,P}$ is observed whereas $I_{DS,N}$ is reduced by ~ 3 orders of magnitude. b) Another FET with a similar device structure and physical dimension is annealed in O₂ atmosphere. In both cases, as-fabricated FET performance shows ambipolar characteristics with a dominant n-type transport. Device annealed at 250 °C show a major improvement in the ON current ($\sim 1000\times$) with $I_{DS,P}$ reaching 10 μ A/ μ m.

The oxidation of the top layer of a bilayer WSe₂ FET to form WO_xSe_y presents an interesting approach to engineering the electrical properties of 2D TMD devices. This technique leverages the inherent properties of the WSe₂ and the oxidized derivatives to modify the electronic environment at the top channel interface. By transforming the top layer into WO_xSe_y, the device benefits from the increased stability and potential p-type doping from the oxide, which could enhance hole transport. However, this process is not without its challenges. The oxidation can induce damage to the underlying WSe₂ channel, potentially leading to defects that adversely affect carrier mobility and overall device performance. The presence of these defects can increase scattering or carrier trapping sites, thus lowering the mobility and eventually drive current of the device. Additionally, the oxidation with O₂ plasma which induces channel defects can also degrade the electrostatic control of the channel leading to poor switching behavior. Moreover, these channel defects can cause high leakage currents across source and drain contacts. To address the limitations observed in the in-situ oxidation of the top WSe₂ layer, we now explore an alternative strategy: the introduction of a pre-oxidized WSe₂ film underneath the channel. This

approach aims to harness the benefits of the oxide interface while mitigating the direct impact on the channel material itself.

Monolayer Dopant Introduction at Channel Interface

Following the challenges associated with less-controlled oxidation and the oxidation of underlying channel, we now explore an alternative strategy of introducing a monolayer dopant at the back interface of the TMD channel. A pre-oxidized WSe₂ layer is introduced beneath the conducting TMD channel, both WSe₂ and MoSe₂. This method seeks to leverage the benefits of doping while minimizing the detrimental impacts on the electrostatics. The approach also seeks to potentially increase the drive current without compromising the material integrity.

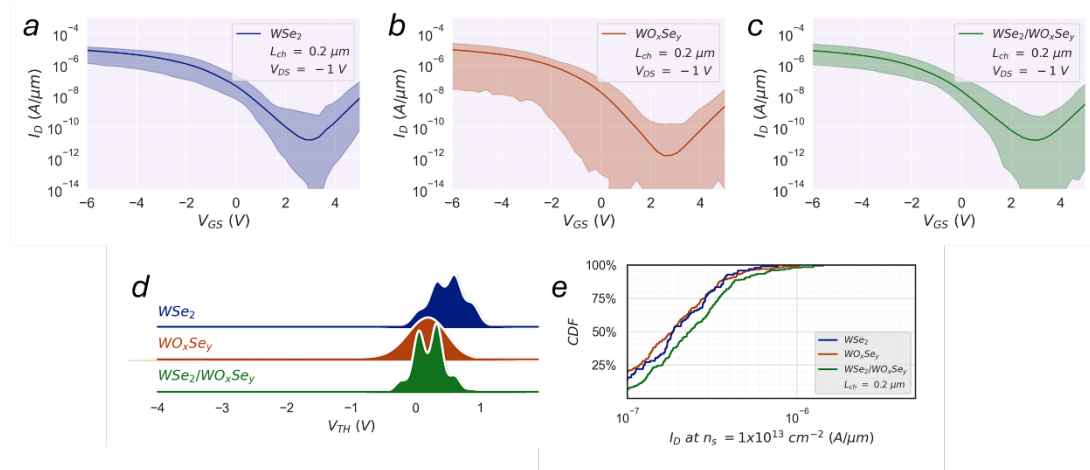


Figure 5-15: Monolayer Dopant Interface to WSe₂ FET: Monolayer dopant of WO_xSe_y was first transferred onto the target substrate and pre-oxidized before subsequent WSe₂ FET fabrication. Three types of channel combinations were obtained, namely, pristine monolayer WSe₂, oxidized WO_xSe_y, and monolayer WSe₂ stacked on WO_xSe_y and devices were fabricated on each of these. Logarithmic scale transfer characteristics of devices with channel length of 0.2 μ m on a) pristine monolayer WSe₂, b) partially oxidized WO_xSe_y, and c) monolayer WSe₂ stacked on WO_xSe_y show a dependence on the OFF current and n-type conduction. Due to partial oxidation of the underlying WSe₂ film into WO_xSe_y, many devices still show decent n-type conduction, although several devices on WO_xSe_y, show OFF current below 1 pA and no n-type conduction hinting towards the doping of WSe₂. d) Threshold voltage, V_{TH} extracted from the transfer characteristics show a slight negative shift. e) Cumulative distribution function (CDF) plot of the output current, I_D , extracted

for a carrier concentration n_s of $1\text{E}13\text{ cm}^{-2}$ and compared across all channel types shows that the WSe_2 channel with the interfacial layer of WO_xSe_y exhibits relatively high performance.

Monolayer WSe_2 was grown using MOCVD technique and was wet-transferred onto a local back-gate substrate with 10 nm Al_2O_3 dielectric and Ni gate metal. The substrate was then treated with O_2 plasma for 30 s at 50 W of power and 500 mTorr of pressure, followed by an O_2 anneal step in the rapid thermal anneal (RTA) chamber for 15 minutes at 250°C to ensure complete oxidation of this layer into WO_3 which will serve as the bottom interface layer. Another monolayer film of WSe_2 was transferred on top covering only a portion of the pre-oxidized WO_xSe_y . CVD grown MoSe_2 was also transferred onto the same substrate such that only a portion of MoSe_2 islands would sit on the pre-oxidized film. Channel isolation and device fabrication steps proceeded as usual. The Pd metal deposition process was optimized such that a long enough idle time was given to the sample after every 100 Å of Pd was e-beam evaporated at $3\text{e-}6$ Torr. This idle time was implemented to maintain low pressure and low temperature of the substrate inside the process chamber. Following the deposition of 40 nm of Pd metal, 30 nm of Pt metal was also deposited to allow contact pad's resilience to probing. Finally, five sets of devices were identified based on the following materials in their channel: i) WSe_2 , ii) WO_xSe_y , iii) WSe_2 on WO_xSe_y , iv) MoSe_2 , and v) MoSe_2 on WO_xSe_y . Figure 5-15a-c shows the transfer characteristics of the FETs on WSe_2 , WO_xSe_y , and WSe_2 stacked on WO_xSe_y . Interestingly, from Figure 5-15b, the material did not fully oxidize, and most devices retained semiconducting properties. The reduction in the OFF current and higher device to device variation compared to the transfer characteristics in Figure 5-15a tells us that the underlying pre-oxidized WSe_2 material was only partially oxidized. Figure 5-15d shows the variation in threshold voltages (V_{TH}) across all devices on each of the three channel types. It can be concluded that the introduction of WO_xSe_y results in a slightly negative V_{TH} shift. We also compare the output current, I_D , for a given carrier concentration n_s of $1\text{E}13\text{ cm}^{-2}$. This is displayed as a cumulative distribution function (CDF) plot,

and it is observed that the devices consisting of WO_xSe_y at the back interface of the monolayer WSe_2 channel. The large variation across the devices in the subthreshold regime of Figure 5-15e can be attributed to the partial oxidation of the underlying WSe_2 . Partially oxidized WSe_2 can result in bilayer islands of WSe_2 leading to the degraded electrostatic control of the channel.

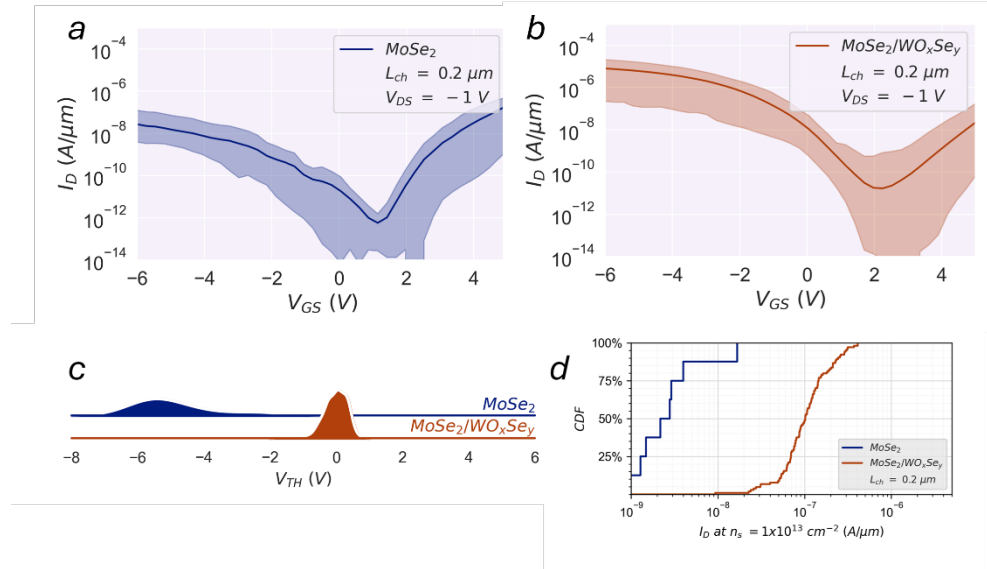


Figure 5-16: Monolayer Dopant Interface to MoSe_2 FET: Monolayer dopant of WO_xSe_y was introduced as an interfacial layer to MoSe_2 FETs. Devices were fabricated on 10 nm Al_2O_3 with Ni back-gate and Pd source/drain contacts. Two types of channel combinations were obtained, namely, pristine monolayer MoSe_2 , and monolayer MoSe_2 stacked on WO_xSe_y . Logarithmic scale transfer characteristics of devices with channel length of $0.2 \mu\text{m}$ on a) pristine monolayer MoSe_2 and b) monolayer MoSe_2 stacked on WO_xSe_y show a significant difference in the p-type conduction. A 100X increase in the p-type branch is noted owing to the underlying WO_xSe_y . Increase in p-type branch is expected to be from the underlying partially oxidized WO_xSe_y , since no change in n-type conduction is observed. c) Threshold voltage, V_{TH} is also extracted from the transfer characteristics. d) Cumulative distribution function (CDF) plot of the output current, I_D , extracted at an iso- n_s -extracted carrier concentration of $1 \times 10^{13} \text{ cm}^{-2}$ shows an overall performance increase.

We apply the same approach to modulating the electrical performance of the MoSe_2 channel. Figure 5-16a shows the transfer characteristics of the pristine MoSe_2 FETs. These devices show ambipolar behavior with a higher n-type conduction branch, measured to be around $I_D = 5 \times 10^{-7} \mu\text{A}/\mu\text{m}$, at $V_{GS} = +5 \text{ V}$. However, the p-type branch current at maximum overdrive voltage is only $I_D = 5 \times 10^{-8} \mu\text{A}/\mu\text{m}$. In the presence of the underlying WO_xSe_y layer, we observe a

100X increase in the p-type branch current but no reduction in the n-type branch current, shown in Figure 5-16b. This leads us to believe that there is parallel conduction path from the underlying interfacial layer. The large shift in the V_{TH} for the p-type branch is shown in Figure 5-16c. Similarly, the CDF plot in Figure 5-16d shows the iso- n_s -extracted device current I_D for devices with and without the underlying interfacial WO_xSe_y .

Another interesting approach to doping the TMD channel was reported by Fang *et al.* by annealing the WSe_2 FET in the presence of NO_2 .²⁸⁶ The chemisorption of NO_2 molecules on exfoliated bulk crystal of WSe_2 resulted in heavy hole doping into the channel. Another paper from the same research group detailed the covalent functionalization of NO_2 molecules onto the top layer of exfoliated WSe_2 material.²⁸⁷ By X-ray Photoelectron Spectroscopy (XPS), the position of Fermi-level was determined and was noted to move beyond the valence band edge suggesting a case of degenerate doping. More recently, this technique was tested on large-area grown monolayer WSe_2 by Chiang *et al.* and a large increase in p-type conduction branch was observed after a high temperature annealing step in NO_x environment.²⁸⁸ Record high ON current performance up to $300 \mu A/\mu m$ and contact resistance down to $950 \Omega \mu m$ was reported. However, the variability in the electrical characterization results was high and the doped device performance did not scale with channel dimensions. A similar study from the same group was presented by Lan *et al.* and even higher ON currents up to $750 \mu A/\mu m$ were reported for the p-type WSe_2 FETs setting another high-performance 2D p-type FET record.²⁸⁹ Here, the semiconducting monolayer WSe_2 channel was sandwiched between a pre-oxidized layer of WO_xSe_y and another layer of WSe_2 that was oxidized with O_2 plasma post-device fabrication. In our approach, we statistically studied the impact of NO_x anneal on contact-engineered and layer-engineered bilayer WSe_2 FETs. Monolayer WSe_2 was transferred on 25 nm Al_2O_3 with Pd contacts and FETs with 200 nm channel length were fabricated with Pd contacts.

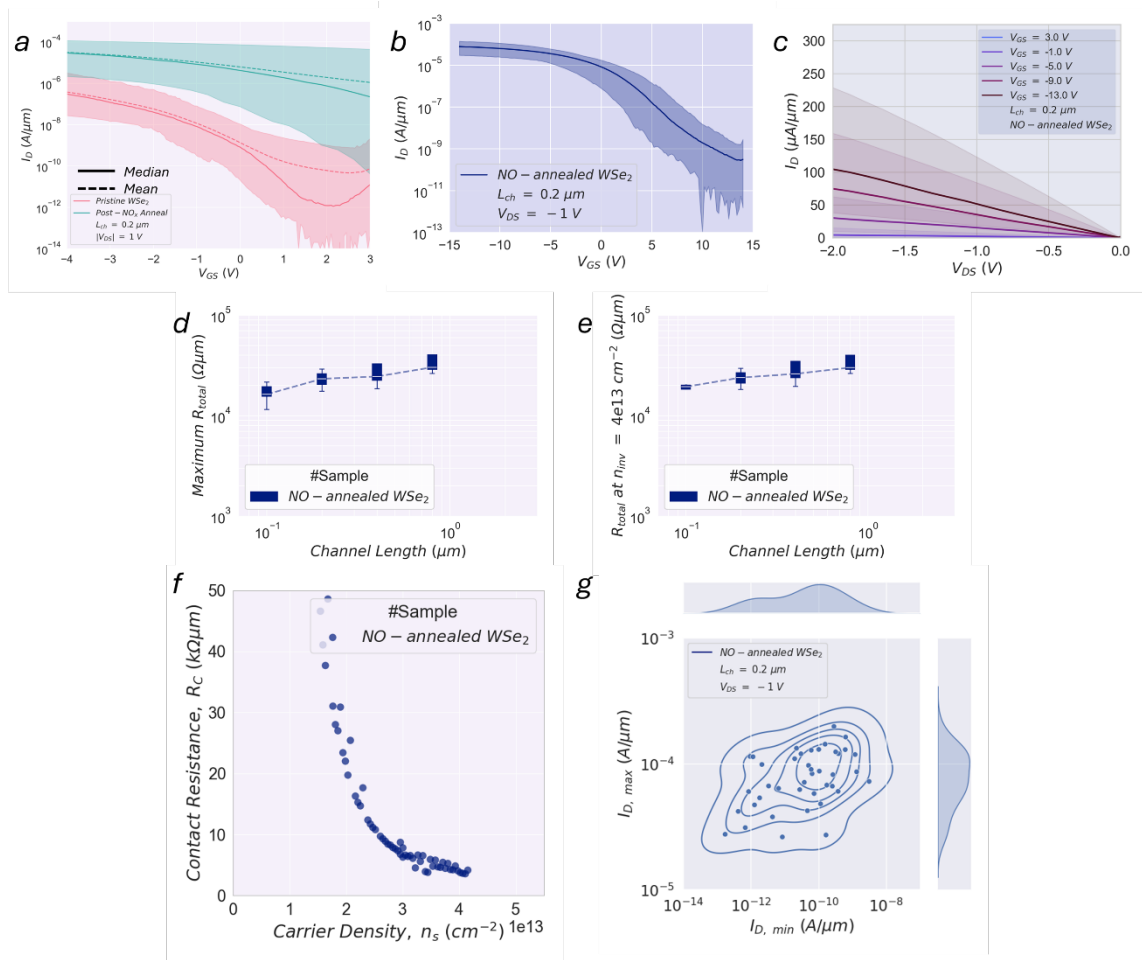


Figure 5-17: NO_x Anneal Layer Modification for High-performance p-Type FET: a) Logarithmic scale transfer characteristics of FETs on few bilayer WSe₂ with 25 nm Al₂O₃ as the gate dielectric, measured pre- and post-NO_x anneal at a drain bias, V_{DS} of +1 V. A 100X increase in the ON current at $V_{GS} = -4$ V was observed owing to the threshold shift channel functionalization with NO_x molecules. b) Transfer characteristics of bilayer WSe₂ FETs along the full sweep range on 25 nm Al₂O₃ after O₂ and NO_x anneal. c) Output characteristics show high ON currents up to 200 $\mu\text{A}/\mu\text{m}$ at $V_{GS} = -13$ V and $V_D = -2$ V. d) Total resistance, R_{total} , is extracted from the current at $V_{GS} = -14$ V along with e) iso- n_s -extracted R_{total} for $n_s = 4\text{E}13 \text{ cm}^{-2}$. f) Contact resistance, R_C , is extracted by extrapolating from the R_{total} for every n_s and is estimated to be as low as 3.5 k $\Omega \mu\text{m}$. g) ON/OFF ratio or the ratio of the maximum measured current ($I_{D, max}$) to the minimum measured current ($I_{D, min}$) is extracted to be at least six orders of magnitude. However, some devices lose complete gating either due to large shift in threshold or a possible phase transition in the channel material itself.

Figure 5-17a shows the pre- and post-NO_x anneal transfer characteristics measured at a drain bias, V_{DS} of +1 V. A 100X increase in the ON current at $V_{GS} = -4$ V was observed owing to the threshold shift beyond the measurement range. To combine the doping effects from oxidation

and nitric oxide anneal, we utilized the bilayer WSe₂ sample treated with O₂ anneal to convert the top layer into WO₃. Devices on this sample were contacted with Pd-Se. The detailed results from this sample after O₂ anneal have been presented in Figure 4-10. Figure 5-17b shows the transfer characteristics of the WSe₂ FETs with the gate voltage, V_{GS} , swept from -14 V to +14 V. The devices experience a huge positive shift in V_{TH} . Output characteristics, in Figure 5-17c, for these devices show very high ON current performance up to 200 $\mu\text{A}/\mu\text{m}$ at $V_{GS} = -13$ V and $V_D = -2$ V. Figure 5-17d shows the total resistance, R_{total} , extracted from the current at the maximum overdrive voltage i.e. $V_{GS} = -14$ V. Some dependence on the channel length is exhibited. Now, we can also calculate the R_{total} for a given carrier density such as $n_s = 4\text{E}13 \text{ cm}^{-2}$, shown in Figure 5-17e. We also extract the contact resistance, displayed in Figure 5-17f, R_C , by extrapolating from the R_{total} for every given channel carrier density, n_s , determined by the gate voltage overdrive. The dependence of performance on channel length, previously masked by high contact resistance, becomes more apparent following this approach. By NO_x annealing, the contact resistance is further reduced down to 3.5 $\text{k}\Omega \mu\text{m}$, thereby tuning the top-channel interface by doping which was previously reported to be effective.^{288,289} The ON/OFF ratio or the ratio of the maximum measured current ($I_{D,max}$) to the minimum measured current ($I_{D,min}$) can also be extracted as done previously when the devices were capped with oxides for threshold-engineering (Figure 5-17f). Our doped WSe₂ FETs therefore achieve over 200 $\mu\text{A}/\mu\text{m}$ with ON/OFF ratios up to 10⁶.

Finally, we fabricate another set of WSe₂ FETs on a high- κ dielectric stack of HfO₂ and expose them to NO_x anneal environment with the motive to achieve high-performance p-type 2D FET operation. Figure 5-18a shows the transfer characteristics of all the devices with channel length of 200 nm measured before and after NO_x anneal. A 100X increase in ON current is observed and all devices reach at least above 100 $\mu\text{A}/\mu\text{m}$. However, due to large shift in V_{TH} , the

OFF current is increased. Figure 5-18b shows the output characteristics for one of the highest performing devices. This device reaches up to 300 $\mu\text{A}/\mu\text{m}$ at a $V_{GS} = -8\text{ V}$, measured at a drain bias of -1.5 V. Hence, we conclude that although the NO_x top layer surface functionalization provides a promising approach to achieving high-performance p-type 2D FETs. There are still a few challenges that need to be addressed in terms of scalability, CMOS-compatibility, and variability. The outlook for further p-type FET development has been outlined in the **Future Outlook** section.

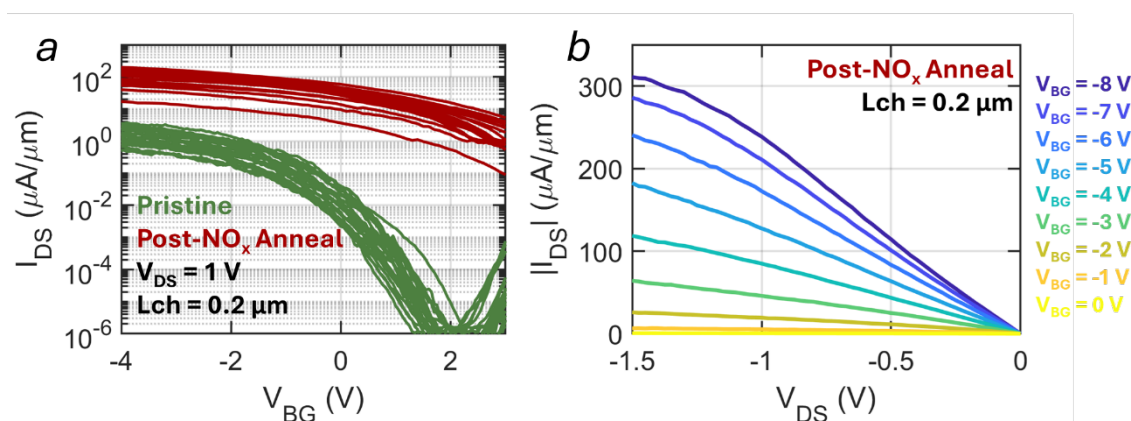


Figure 5-18: NO_x Anneal Layer Modification on high- κ HfO_2 : a) Transfer characteristics of WSe_2 FETs with channel length of 0.2 μm measured before and after NO_x anneal at a drain bias of 1 V shows a 100X increase in ON current with most devices measuring a drive current of at least 100 $\mu\text{A}/\mu\text{m}$. B) Output characteristics from the highest performing NO_x annealed, Pd contacted, few bilayer WSe_2 FET. This device reaches up to 300 $\mu\text{A}/\mu\text{m}$ at a $V_{GS} = -8\text{ V}$, measured at a drain bias of -1.5 V showing promise for high-performance p-type 2D FET with WSe_2 .

The layer engineering functionalization of WSe_2 using full coverage of bilayer material followed by O_2 and NO_x annealing techniques represents a significant advancement in the modification and control of material properties for enhanced device performance. Substrate treatment with O_2 and NO_x has proven effective in altering the electronic properties of WSe_2 either by introducing oxygen-related defect states that can modulate the band structure or by covalently bonding the NO molecule to the top layer of the channel, both of which can improve the p-type conduction.

The insights gained from these layer modification techniques underscore the importance of precise surface engineering in 2D “surface-only” semiconductors. By manipulating the surface states and chemical composition, we can significantly influence the overall electronic properties and reactivity of 2D materials. Such advancements pave the way for more sophisticated interface engineering strategies, essential for the next generation of electronic devices.

Chapter 6

Engineering and Characterizing Interface to 1D CNT Channel

Part of this chapter has been reproduced from: S. Li et al., "High-performance and low parasitic capacitance CNT MOSFET: 1.2 mA/ μ m at VDS of 0.75 V by self-aligned doping in sub-20 nm spacer," 2023 International Electron Devices Meeting (IEDM), San Francisco, CA, USA, 2023, pp. 1-4, doi: 10.1109/IEDM45741.2023.10413827.

Motivation

Building upon the foundational knowledge acquired from surface functionalization of WSe₂, this chapter in the thesis delves into the engineering and characterization of interfaces, employing one-dimensional carbon nanotubes (CNTs) as a testbed. This approach aims to explore the complex interactions at the interface of hybrid structures that combine low-dimensional semiconductors with conventional bulk device components such as insulator and contact metal. In 1D channel materials like carbon nanotubes (CNTs), the channel is a quasi-one-dimensional structure with a high surface-to-volume ratio. The interface between the CNT and the surrounding dielectric or contact materials plays a crucial role in determining the device's characteristics. Defects, adsorbates, or improper interface engineering can result in increased scattering, reduced carrier mobility, and poor electrostatic control, limiting the device's potential. Interface engineering for low-dimensional channel materials involves various strategies, such as the careful selection of dielectric materials, surface treatments, encapsulation techniques, and contact engineering.²⁹⁰ The goal is to create a high-quality interface that minimizes defects, prevents unintended doping, and facilitates efficient carrier transport while maintaining excellent electrostatic control.

Characterizing and understanding these interfaces is equally important for optimizing device performance and enabling future scaling. Various analytical techniques, including electrical characterization methods (e.g., low-frequency noise measurements, capacitance-voltage measurements), spectroscopic techniques (e.g., X-ray photoelectron spectroscopy, Raman spectroscopy), and microscopy techniques (e.g., scanning probe microscopy, transmission electron microscopy), can provide insights into the interface properties, defect densities, and charge transport mechanisms.

By mastering interface engineering and characterization for low-dimensional channel materials, the true potential of these emerging materials for high-performance electronic devices can be unlocked.

Introduction

Carbon nanotubes (CNTs) possess unique mechanical as well as electrical properties with a one-dimensional structure consisting of just Carbon atoms exposed onto the surface. They have the highest electrical and thermal conductivity among all materials, can be semiconducting, and also exhibit a high surface to volume ratio due to their cylindrical structure making them potential candidates for transistors. Reports of ballistic electron transport along lengths of CNT have triggered interest for their potential in the next generation of electronic devices.⁵⁶ CNTs have been studied widely for over two decades and the great amount of scientific understanding has led us to believe that their establishment involves a highly complex synthesis and fabrication process which yields a strong correlation to the electronic properties, such as the alignment, the bandgap dependence on the diameter, and their extremely sensitive interface to the surrounding environment.^{291,292} Despite the challenges, there has been remarkable progress in the growth,

fabrication, and high-performance demonstration on CNTs, making them a suitable candidate as channel material in scaled, high-performance transistors beyond Silicon technology.^{49,50,293-296}

Complementary digital MOSFETs with localized extension doping, computer system with a single instruction set, and modern microprocessor architectures have been realized, fully built using CNTs as the channel materials.²⁹⁷⁻²⁹⁹ Although significant advancements have been reported, the fundamental understanding of a CNT MOSFET has been primarily limited to transport measurements. Since CNTs exhibit an inert surface, free of dangling bonds, growth of dielectrics for wrap-around gate-all-around geometry is complex. The inert surface of these low-dimensional materials limits their interface quality and further impacts transport. Furthermore, the inherent channel defects cannot be neglected. A combination of these traps in the channel, at the interface, and in the dielectric can lead to degraded transport and poor electrostatic control of the channel. A major reason for the success of any electronic technology node is the superior quality of the Si/SiO₂ interface. An interface state trap density less than $1\text{E}10\text{ cm}^{-2}\text{ eV}^{-1}$ is expected from production quality Si MOSFETs. Switching to high- κ dielectric increases the interface trap density to between $1\text{E}11 \sim 1\text{E}12\text{ cm}^{-2}\text{ eV}^{-1}$. Hence, the goal for any alternative channel technology to be viable, a low interface trap density is a given necessity.³⁰⁰

Conductance Method for Interface Trap Estimation

Capacitance-voltage (C-V) characterization is an efficient way of studying the interface properties.^{64,301} For a MOS structure, static and differential capacitances may be derived. Since the charge in the semiconductor can vary nonlinearly depending on the applied bias, differential capacitance holds more importance. This is derived from small-signal measurements that superimpose a small signal AC voltage onto the applied gate bias. The capture and emission of mobile carriers by the interface trap states leads to generation and recombination events that

influence the interface trap impedance, which can be measured with the help of equivalent circuits. This is done so by extracting the necessary parameters from the conductance and capacitance across the MOS structure. The conductance method is a well-known technique to extract the interface trap density, capture probability, and capture time constant of the traps. Among the small-signal methods, it is considered to be the most accurate and due to its convenience, it is extensively used in assessing chemical changes to interface traps from annealing and other processes.^{290,302,303}

Changes in interface trap state occupancy are introduced by changing the gate bias, which changes the position of the Fermi-level. Trap states located above the Fermi-level are empty while those located below the Fermi-level are full. Through the conductance method, the small variations in the trap occupancy resulting in small AC signal variations that move the band edges toward or away from the Fermi-level located about a few kT/q on either side. Due to this small signal variation to the band edges, an energy loss is detected due to the capture and emission of majority carriers. This energy loss takes place at all frequencies except when all trap states have sufficient time to respond (very low frequencies) or when trap states cannot respond (very high frequencies). During the positive half cycle of the AC signal, the conduction band edge is closer to the semiconductor Fermi level and the average electron energy is high however at frequencies where an energy loss occurs, the interface trap states respond slowly to this variation and follow the AC signal with a certain lag. In this situation, there are trap states below the Fermi level that are still empty and the filling of these low energy trap states with the electrons that have a higher average energy in the semiconductor until the ensemble of electrons reach the same average energy. This energy loss is given away as heat through phonons. Similarly, in the negative half cycle of the AC signal, there are filled trap states above the Fermi level for which the electrons have a higher average energy than the average energy of electrons in the semiconductor. Hence, energy is needed to emit electrons from the trap states into the conduction band of the Silicon and

this is provided by phonons. These electrons occupy the tail end of the Fermi-Dirac distribution and raise the average energy of the electrons in the semiconductor until the original average energy is achieved through loss of energy in the form of heat. This energy loss that occurs on both halves of the AC cycle is measured as an equivalent parallel conductance, G_{pm} . The emission and capture of electrons in these trap states take place as usual however each trap state retains the electron for a definite time, defined as the trap time constant, τ_p . Hence, there will be a characteristic interface trap capacitance, C_{IT} , associated to this. At any given frequency of the AC signal applied to the gate, there will be a loss associated to the speed of capture and emission of the interface traps. This is dependent on the capture probability. The above also depends on the interface trap density, D_{IT} , near the Fermi-level which is proportional to the gate bias. Hence, by combining the loss at all frequencies and biases, the capture probability as well as the interface trap density can be estimated corresponding to the position in the semiconductor's bandgap. The interface trap level density and the capture time constant can be derived from the measured impedance for a MOS structure with semiconducting, network CNT as the channel. For a simplistic case, we assume that all interface trap levels are identical, and the equivalent circuit of a MOS structure has been shown in Figure 1-8a. In depletion, the equivalent circuit can be simplified to Figure 1-8b.

CNT MOS Structure Impedance Analysis

In this work, we implement the conductance-based interface characterization technique to estimate the interface trap density over the energy bandgap of semiconducting, network CNT channel, extract capture time constants, and finally extract the channel carrier density. It is noted that the introduction of a post-process annealing helps in reducing the D_{IT} to an acceptable limit. Finally, we summarize the results and lay a path forward to underscore the need for an aligned

CNT channel to prevent percolation paths and junctions in network CNTs. Figure 6-1a shows the cross-section device schematic of a top-gated CNT MOSFET structure with network and CNTs, a scanning electron microscopy (SEM) image for which is shown in Figure 6-1b. The semiconductor CNT purification and device fabrication was carried out on a Quartz substrate in the same way as it has been described in Zhang *et al.*²⁹⁸ The device was fabricated using a contact-first process with the top-gate dielectric constituting of a 1.2 nm thin low-temperature nanofog layer of AlO_x which is intended as the seed layer for the growth of high- κ 5 nm HfO_2 . The low-temperature nanofog AlO_x prevents surface damage and forms a conformal coating that preserves the underlying CNT from high- κ dielectric growth.²¹⁷ For source/drain contact metal, Pd is used, whereas Pt is used as the top-gate contact metal. The device gate length is $L_g = 2 \mu\text{m}$, gate width, W_g is $310 \mu\text{m}$, and the extension region is $0.6 \mu\text{m}$.

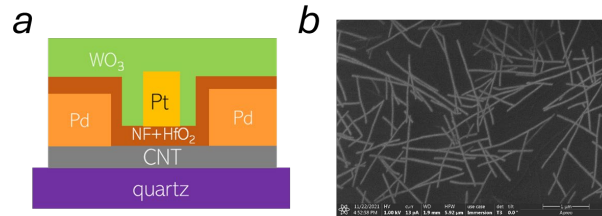


Figure 6-1: Carbon Nanotube (CNT) MOSFET: a) Cross-section of the top-gated CNT MOSFET, b) Scanning Electron Microscopy (SEM) image of the channel region with network of 99.99% purified CNTs

Electrical characterization was performed on MPI Semiautomatic Prober with Keysight B1500A parameter analyzer. The dual-sweep transfer characteristics of a top-gated CNT MOSFET are shown in Figure 6-2a for the device measured in the gate voltage, V_G , ranging from -1 V to +1 V, with the drain contact biased at $V_D = -0.05$ V. The gray line indicates the device current measured at the drain terminal (I_D), red line indicates the gate current, I_G . The device achieves an ON/OFF ratio of 5 orders of magnitude and shows predominantly n-type characteristics. The subthreshold slope (SS) of the device is extracted to be 102 mV/dec with a

threshold voltage, V_{TH} around 0 V, extracted using the iso-current method. The D_{IT} value can be extracted from the SS using the formula below,

$$D_{IT} = \left(\frac{SS}{0.06} - 1 \right) \frac{C_{ox,model}}{q}$$

where $\frac{SS}{0.06}$ gives the band movement factor m , C_{ox} is the modeled oxide capacitance which is 2.98×10^{-10} F/m, and q is the electronic charge. This yields D_{IT} with the unit of $\text{eV}^{-1} \text{ m}^{-1}$. A D_{IT} value for this device is found to be $0.21 \text{ eV}^{-1} \text{ nm}^{-1}$, equivalent to $4.61 \times 10^{12} \text{ eV}^{-1} \text{ cm}^{-2}$. This conversion considers the circumference of the CNTs given the total length. Transconductance is extracted from the device current and plotted in Figure 6-2b.

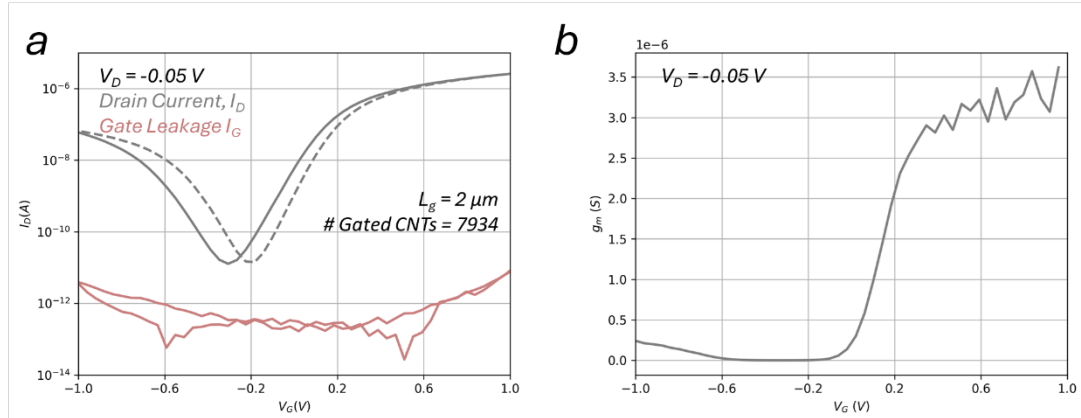


Figure 6-2: Electrical Characterization of CNT MOSFETs: a) Dual-sweep transfer characteristics of the device, b) Transconductance (g_m) extracted over gate bias sweep

Next, we examine the capacitance and conductance measurements of the device in room temperature and in ambient. Measurements were performed using an LCR meter E4980A. The device under test was considered to be one side of the MOSFET structure with the one of the source/drain contact pad connected to the “low” terminal and the gate contact pad connected to the “high” terminal of the LCR meter. Figure 6-3a shows the measured circuit for the device under test. Parallel equivalent circuit measurements are preferred since the expected capacitance values are very low and the elements exhibit high impedance. The measured parallel capacitance

and conductance are swept over gate bias for each given frequency as well as swept over a low to high frequency range for each given bias. The frequency or bias is consequently increased without any reset pulse thus maintaining the state from the previous measurement. Zero-open and zero-short calibration structures were used to de-embed parasitics.

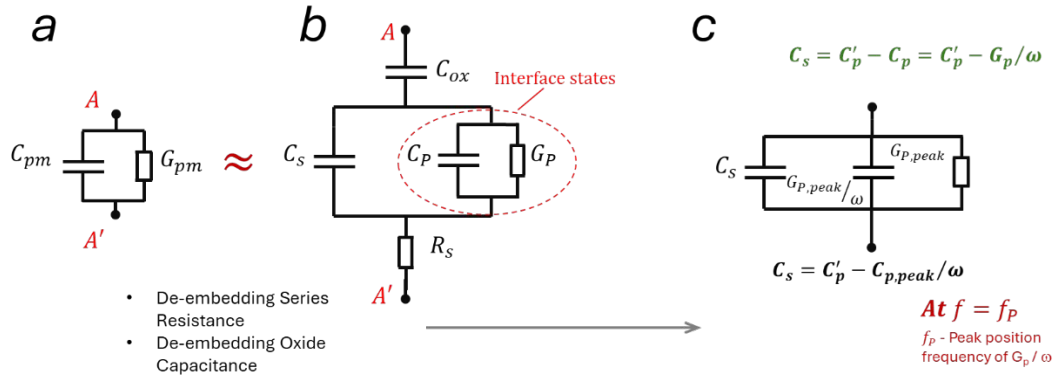


Figure 6-3: CNT MOS Structure Equivalent Circuit: a) Parallel equivalent measured circuit, and b) the actual equivalent circuit in depletion considering the series resistance (R_s), oxide capacitance (C_{ox}), and the interface trap state capacitive (C_p) and conductive (G_p) components with the semiconductor capacitance (C_s) in parallel. c) Final equivalent circuit after de-embedding through a series of impedance-admittance conversions.

Plot of measured parallel capacitance (C_{pm}) and measured parallel conductance (G_{pm}) versus bias are shown in Figure 6-4a-b. Angular frequency, ω , is $2\pi \times$ frequency. We observe frequency dependent dispersion in the electron accumulation regime (positive V_G) from the C-V curves and this may correspond to the distributed RC network in the channel due to the network CNT junctions and not to the defects.[ref] Our understanding of the junctions from randomly oriented network CNTs is limited. The frequency-dependent dispersion in the depletion regime is due to the interface trap defects. For this reason, we proceed with the analysis. The ambipolarity nature of the device makes the analysis complicated and hence the effect of opposite carriers (negative V_G), accumulation of holes is also considered. As the gate voltage is swept to positive,

the CNT channel is populated with electrons; when the gate voltage is swept to negative, the CNT channel is populated with holes; the channel is depleted of charge around -0.5 V.

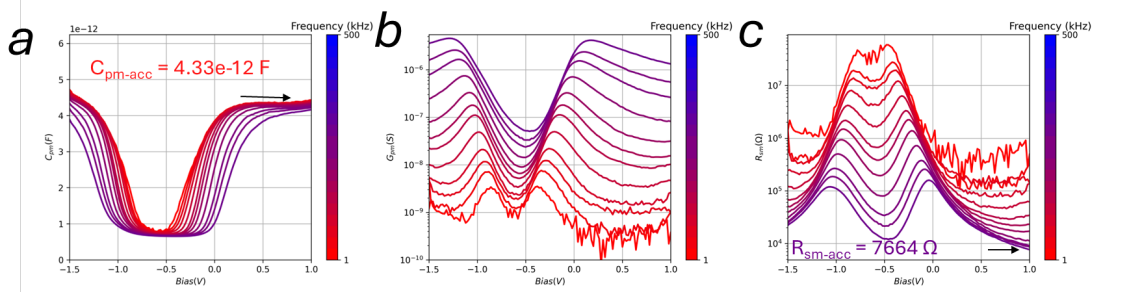


Figure 6-4: Capacitance-Conductance sweeps over varying bias: a) Measured capacitance (C_{pm}) across the MOS structure plotted for frequencies ranging from 1 kHz to 500 kHz. The semiconducting channel is ambipolar as seen from transport measurements, b) measured conductance (G_{pm}) swept over bias for different frequencies, and c) extracted series resistance (R_{sm}) gives an estimate of the maximum $R_{sm, acc}$.

The conductance method is now implemented. The ungated region of the CNT channel along with the Schottky contacts give rise to a large amount of series resistance, R_{sm} . This value of R_{sm} is extracted when the device is biased in accumulation. We extract R_{sm} using the following equation relating the measured bias sweeps of G_{pm} and C_{pm} ,

$$R_{sm} = \frac{G_{pm}}{G_{pm}^2 + \omega^2 C_{pm}^2}$$

Figure 6-4c shows the extracted R_{sm} and the value in accumulation is found to be $R_{sm, acc} = 7664 \Omega$. This underlines the need to de-embed the high series resistance. Now, we extract the factor of series resistance, a , with the following equation,

$$a = G_{pm} - (G_{pm}^2 + \omega^2 C_{pm}^2) R_{sm}$$

We study the capacitance and conductance measurements over frequency sweeps now since our analysis will correspond to the impedance loss identified at any given frequency. Thus, the corrected capacitance, C_C , and corrected conductance, G_C , can be estimated from,

$$C_c = \frac{(G_{pm}^2 + \omega^2 C_{pm}^2) C_{pm}}{a^2 + \omega^2 C_{pm}^2}, \quad G_c = \frac{(G_{pm}^2 + \omega^2 C_{pm}^2) a}{a^2 + \omega^2 C_{pm}^2}$$

Now that we have de-embedded the series resistance and obtained the corrected values of conductance and capacitance, we will proceed to the de-embedding step of gate oxide capacitance, C_{ox} . The final value of the parasitic component that will be used for the extraction of D_{IT} post de-embedding of R_{sm} and C_{ox} is given by,

$$G_P/\omega = \frac{\omega C_{ox}^2 G_c}{G_c^2 + \omega^2 (C_{ox} - C_c)^2}$$

while the capacitance value after the de-embedding steps is given by,

$$C_s + C_p = \frac{\omega^2 C_c C_{ox}^2 - \omega^2 C_c^2 C_{ox} - G_c^2 C_{ox}}{G_c^2 + \omega^2 (C_{ox} - C_c)^2}$$

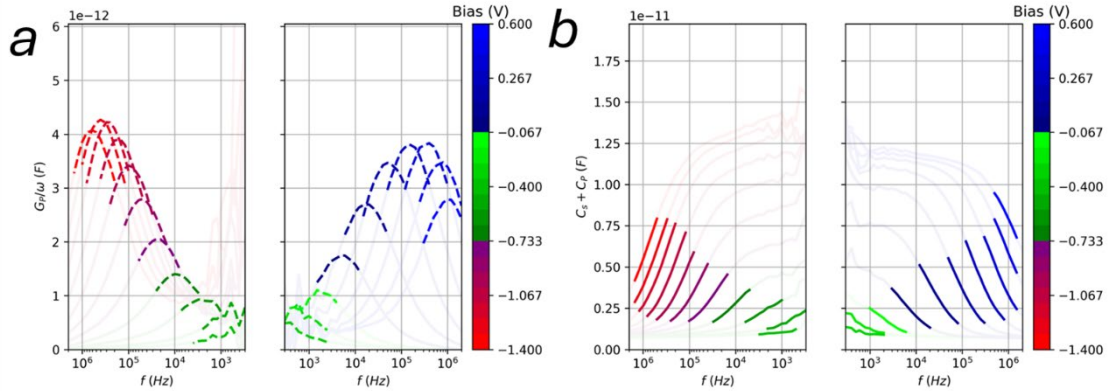


Figure 6-5: De-embedded parasitic components versus frequency: a) Measured de-embedded G_P/ω showing the presence of conductance peaks in both bias ranges owing to the ambipolarity of the channel. The dotted range indicates the range 1/5 and 5X on either side where $\left[G_P/\omega\right]_{f=f_{peak}}$. b) Sum of semiconductor capacitance (C_s) and parasitic capacitance (C_p) calculated after de-embedding of R_{sm} and C_{ox} . C_s provides the trap energy and CNT carrier density for the bias at which a G_P/ω peak is observed using a standard density of states CNT model.

Both corrected capacitive components are plotted in Figure 6-5. Figure 6-5a shows G_P/ω versus frequency with the dotted lines indicating the limits 1/5 and 5X limits of the frequency

where $\left[G_P/\omega\right]_{f=f_{peak}}$. The corresponding range for the sum of semiconductor capacitance and parasitic capacitance, $C_s + C_p$, is also shown. The faded lines indicate the rest of the curve for each of the two cases. These limits will later be useful to extract the interface trap state density and energy gap location, respectively. This capacitance $C_s + C_p$ constitutes of the semiconductor capacitance in depletion as well as the parasitic capacitance. The accumulation capacitance, $C_{pm,acc}$, is extracted from C_{pm} versus gate bias plot. The following steps are employed to extract the gate capacitance from the modeled capacitance considering the cylindrical structure of the CNT channel network,

$$\text{Simulated } C'_{ox} = 2.98\text{E-}10 \text{ F/m}$$

$$\text{Simulated } C'_{acc} = 1.93\text{E-}10 \text{ F/m}$$

$$\text{Measured } C_{pm,acc} = 4.33\text{E-}12 \text{ F}$$

Total Length, L_{tot} , can be approximated by taking the ratio of the $C_{pm,acc}$ and C'_{acc} . We find L_{tot} to be $2.28\text{E-}2$ m following which we calculate the oxide capacitance as C_{ox} as $C'_{ox} \times L_{tot}$, found to be $6.68\text{E-}12$ F. The linear density of the CNTs, N , across the channel can be the ratio of the L_{tot} and the $L_{average}$, where $L_{average}$ is the average length of each CNT connecting the source to the drain. $L_{average}$ is approximated to be the gate length, L_g , divided by the cosine of the average orientation angle i.e. $\cos \alpha$, where $\alpha = 45^\circ$. The total number of CNTs in the channel can therefore be calculated. Hence, number of CNTs in the channel, N , is found to be 7934 and the density of CNTs is N/W_g , found to be ~ 25 CNTs per μm .

Next, we extract the interface trap density, D_{IT} , by first evaluating for ξ at ξ_{peak} and obtain the peak value of the de-embedded parasitic component, G_P/ω , given as $\left(G_P/\omega\right)_{f=f_{peak}}$.

Hence,

$$D_{IT} = \left(G_P/\omega\right)_{f=f_{peak}} [f_D(\sigma_s)q]^{-1}$$

where $f_D(\sigma_s)$ is denoted as the universal function given by the plot shown in Figure 6-6a.

The value of standard deviation of band bending, given by σ_s , is derived from the plot in

Figure 6-6b. Here, the ratio of $\left[G_P/\omega\right]_{f=5 \times f_{peak}}$ or $\left[G_P/\omega\right]_{f=0.5 \times f_{peak}}$ to the peak value

$\left[G_P/\omega\right]_{f=f_{peak}}$ is used to extract the value of σ_s . To extract the value of the trap time constant, τ_P ,

we use the relation,

$$\tau_P = \frac{\xi_{peak}}{\omega_{peak}}$$

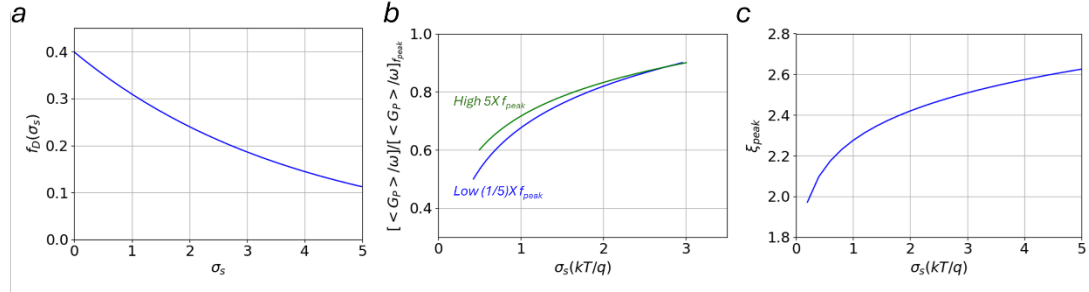


Figure 6-6: Additional Fit Functions for Analysis: a) Universal function $f_D(\sigma_s)$ versus standard deviation of band-bending (σ_s), b) Ratio of $\left(G_P/\omega\right)$ and $\left(G_P/\omega\right)_{f=f_{peak}}$ to calculate the σ_s . c) Plot of $\xi_{peak} = \omega_{peak} (c_{peak} N_A) e^{v_s}$ as a function of σ_s , where c_{peak} is the capture probability, N_A is the carrier density, and v_s is the carrier thermal velocity. ξ_{peak} is calculated and is used to calculate interface trap response time (τ_P). .

The extraction of ξ_{peak} is based on its dependence on the σ_s , shown in Figure 6-6a.

Hence, the calculation of D_{IT} and τ_P , in principle, only require two points on a G_P/ω curve, one at the peak of de-embedded parasitic component and the other extracted at 1/5 or 5X of the peak value. In most cases, the estimation of D_{IT} is simplified and the value for $f_D(\sigma_s)$ is used as 0.4 extracted for $\sigma_s = 0$ from the Figure 6-6c. Now, we use the de-embedded capacitance value at the peak frequency to extract the position of the D_{IT} in the energy gap. For this, we use a model to estimate the value of semiconductor capacitance (C_s) under depletion. Figure 6-7a shows the

modeled semiconductor capacitance along the CNT bandgap that when subtracted from $C_s + C_p$ and thus G_p/ω can be obtained. The bandgap of the CNT depends on the diameter and is extracted from the relationship below,

$$E_g = 2 \times \frac{a_{C-C}}{CNT \text{ diameter}}$$

where, a_{C-C} is the atomic distance between the C atoms (1.42 Å). Given the diameter of the CNT in our channel is 1.45 nm, the bandgap E_g is approximated as 0.55 eV. Finally, in Figure 6-7b the extracted D_{IT} (stars) shows a value of $\sim 3 \text{ eV}^{-1} \text{ nm}^{-1}$ located $\sim 60 \text{ meV}$ from the conduction band edge and similarly for electrons, the D_{IT} value is roughly the same and found to be $\sim 50 \text{ meV}$ from the valence band edge for holes. As we move closer to middle of the bandgap, the D_{IT} value also decreases, a characteristic of the trap distribution in semiconducting channels. The semiconductor capacitance (C_s) (circles) is extracted from the difference of $C_s + C_p$ and G_p/ω at f_{peak} , normalized to the total length, L_{tot} and given in the same figure. The characteristic trap time constant (τ_p) is shown in Figure 6-7c. Carrier density (Figure 6-7d) can also be extracted from the DOS CNT model and correlated to the extracted semiconductor capacitance from impedance measurements. It is noteworthy that room temperature impedance measurements within a typical frequency range between 1 kHz and 1 MHz provide trap related data within 30-100 meV of the band edge. For 3D semiconductors, an energy range around 250 meV below conduction band or above valence band edges is typically accessed by room temperature conductance. This different behavior is tentatively attributed to the 1D nature of the system. The capture length $\sigma_{n,p}$ (in 3D “capture cross section”, e.g. 10^{-14} cm^2) in the 1D system is very short ($\leq 1 \text{ fm}$). Now, we introduce an annealing step in the process flow. A forming gas anneal is performed on the device stack after the ALD growth of the dielectric stack. Notably, a significant reduction in the D_{IT} is observed. Figure 6-8a shows the transfer characteristics before and after annealing. The subthreshold switching characteristics show a major improvement from

142 mV/dec to 81.6 mV/dec. Figure 6-8b shows the reduction in the D_{IT} close to the middle of the bandgap, which corresponds to the subthreshold regime of device operation. We extract the D_{IT} from both of the impedance measurements in three regions of the band gap and from transport measurements near the supposedly subthreshold regime in the transfer characteristics that correspond to near mid gap. This is shown in the form of a bar plot in Figure 6-8c. No change is observed near the band edges while the region corresponding to the mid gap has $\sim 1\text{E}12\text{ eV}^{-1}\text{ cm}^{-2}$ reduction.

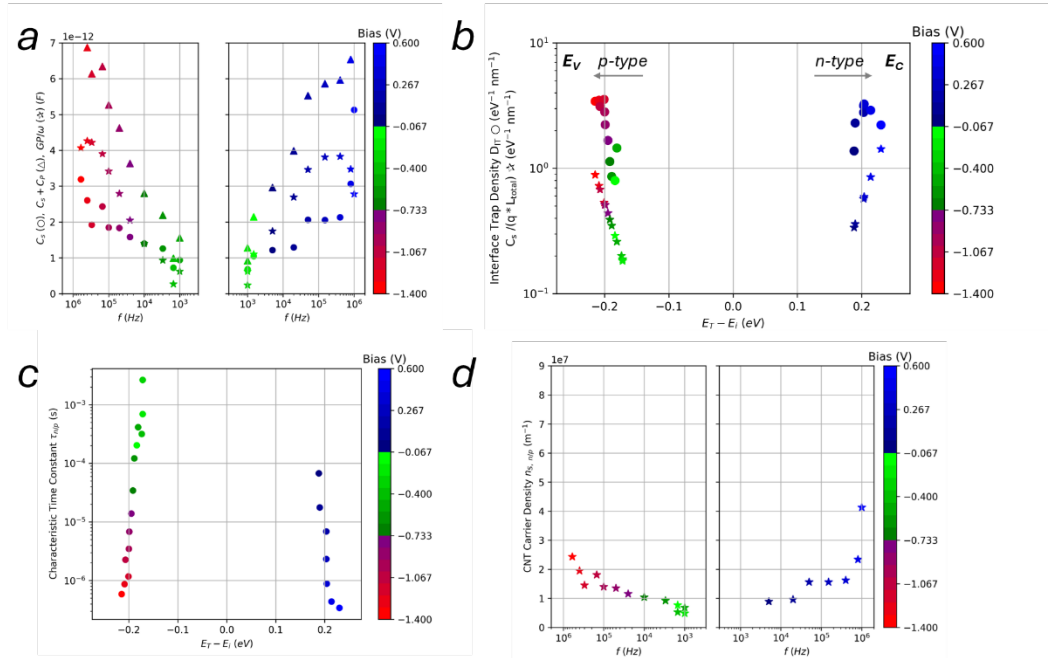


Figure 6-7: Interface Trap Characterization: a) Plot of G_p/ω , $C_s + C_p$, and C_s calculated at $f = f_{peak}$, b) Interface trap density (D_{IT}) estimated across the CNT bandgap with E_T denoting the trap level and E_I denoting the intrinsic Fermi level position. The D_{IT} ranges from $2.5\text{ eV}^{-1}\text{ nm}^{-1}$ near the left band edge (valence band) for holes to $7\text{e-}1\text{ eV}^{-1}\text{ nm}^{-1}$ approaching the mid gap region. Similarly, D_{IT} for electrons near right band edge (conduction band) is calculated. c) Characteristic Trap Time Constant (τ_p) over the energy gap range. d) Carrier density (n_s) in the CNT channel obtained from the impedance measurements tells the carriers present in the channel uninfluenced by the traps.

Temperature dependent study is also performed to identify the location of trap states near the band edges. Carrier density in the channel is extracted (Figure 6-9a) using a top-of-barrier

charge CNT density of states model that is utilized to map the semiconductor capacitance (C_s) which is used to estimate the defect density in the band gap. Figure 6-9b shows the interface trap states located very close to the band edge can now be accessed since the Fermi-level moves closer to the band edge at lower temperatures. The measurements were carried out in a Lakeshore CRX-VF probe station that allowed for temperatures as low as 10 K. Interestingly, the ratio of C_s to D_{IT} increases as the temperature is lowered.

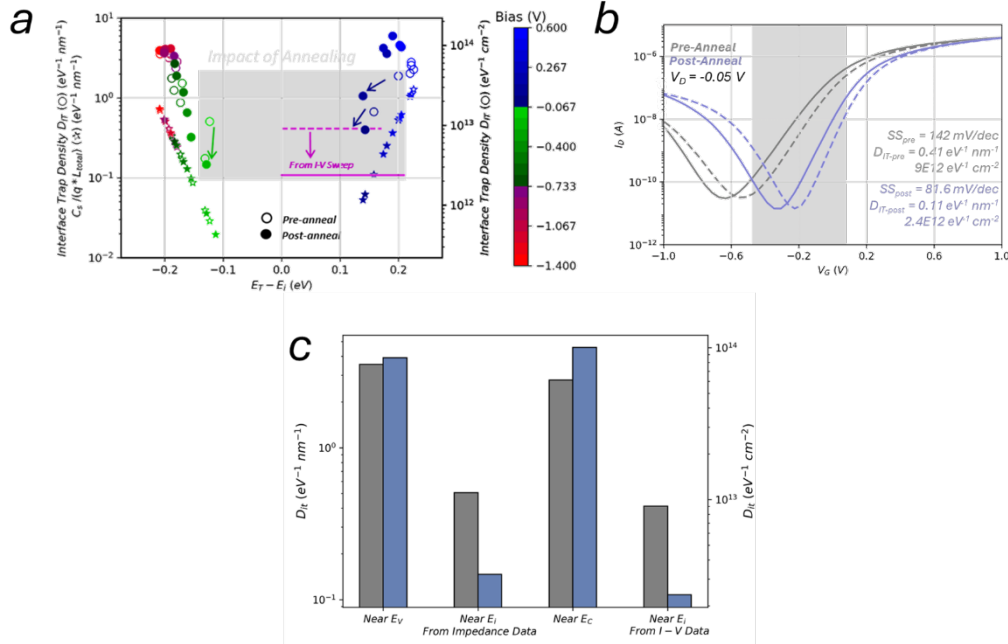


Figure 6-8: Interface Trap Reduction: a) Interface trap density (D_{IT}) estimated across the CNT bandgap for a device before and after Forming Gas anneal. The D_{IT} pre-anneal for electrons at least 150 meV from the conduction band edge is reduced by $0.4 \text{ eV}^{-1} \text{ nm}^{-1}$ post-anneal. The dark shaded region indicates the region of impact in the energy gap from annealing. The pink lines show the calculated D_{IT} from the transfer characteristics and its projected reduction after annealing. c) Transfer characteristics for the respective devices show a reduction in the subthreshold slope (SS) and a rightward shift in threshold voltage (V_{TH}) from annealing. Furthermore, D_{IT} extracted from the SS also shows a reduction of about $0.3 \text{ eV}^{-1} \text{ nm}^{-1}$. d) Bar plot comparing the D_{IT} extracted from impedance measurements as well as transport measurements in three different regions of the CNT energy gap.

Finally, we conclude by underlining the need to perform the same analysis on a device with aligned CNTs. Although aligned CNT channel currently faces a challenge with only 66.67%

purity i.e. the devices on aligned CNTs show a semi-metallic behavior since channel is a mix of semiconducting and metallic CNTs, the measured capacitance gets severely affected. Moreover, the gate-first over the contact-first process would prove to be more useful since the channel would not see any process residue and an ultra-clean semiconductor/oxide interface can be expected. Temperature dependent results at higher temperatures will help extract the defect density levels near mid gap region and could be correlated more strongly to the transport measurements.

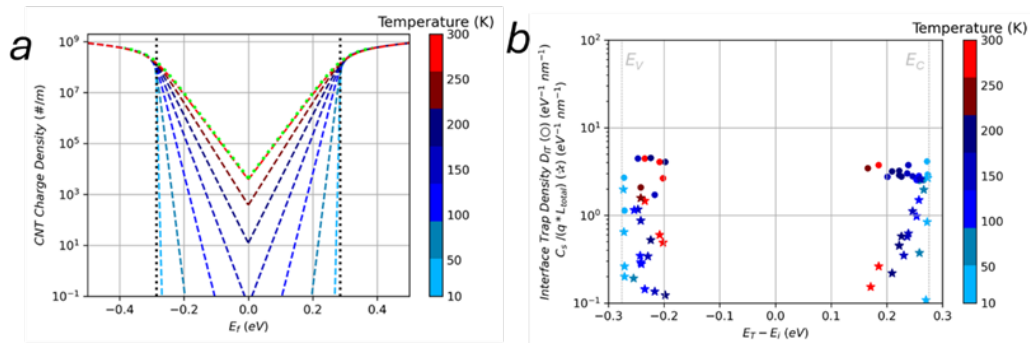


Figure 6-9: Interface Trap State Temperature Dependence: a) CNT charge density (N) calculated for varying temperatures using the CNT DOS model. The temperature dependence plays a role in the position of Fermi level which would be essential to study the interface trap location in the energy gap. b) Interface trap density (D_{IT}) estimated across the CNT bandgap different bias points and at different temperatures shown by the color identifier. As temperature is lowered, trap density closer to the band edges can be extracted with more confidence.

In summary, a comprehensive methodology to characterize the interface is established on 1D CNT based MOSFETs and the approach can very well be extended to other low-dimensional channel material based MOSFETs. Using the conductance method, we identify a large interface trap density in the structures and identify post-processing techniques to reduce the same. Our results further indicate the need for aligned CNTs and cleaner processes in fabrication.

Future Work

Several avenues for development in FETs on low-dimensional materials are yet to be explored. In this chapter, the possible routes to gaining control over p-type 2D FET performance are briefly explained.

- **Synthesis of 2D TMDs on amorphous materials:** Synthesis of the low-dimensional material will remain the most critical part in device exploration. Their growth on amorphous substrates shall hold importance since transfer of films is just not scalable.³⁰⁴ The direction towards confined area growth is promising although the challenges in its implementation in stacked nanosheet structures are yet to be explored.
- **Purification of aligned CNTs:** The presence of junctions in network semiconducting CNT channel hinders further development and process optimization. There is a need for a scalable synthesis process of aligned CNTs with high purity of semiconducting CNTs. Semi-metallic CNTs in the channel can influence the measured capacitance and provide a direct conduction path making it non-applicable for logic.
- **Buffer Layers to preserve channel properties:** TMD films are inherently thin, and their electronic benefits over conventional bulk semiconducting channels bear fruit only when their thickness is retained to few atomic layers. At bulk dimensions, Coulombic scattering, electrostatic screening results in poor conductivity as well as degraded switching. However, reducing its thickness leads to challenges associated with preserving intrinsic material properties. Hence, introduction of buffer layers into the process will tend to optimize device performance. In some cases, damage to the semiconducting film may pose as a benefit and that may although be shadowed by the interface encapsulation, it will thus provide evidence and scope for tunability. These layers may be introduced for multi-bridge channel assembly for stacked nanosheet structures or to assist in transfer. In

either case, their reactivity with the channel material must be minimal. Moreover, the gate-first process must be developed where the channel material does not see any process residue from contact metallization. This will help study the pristine interface properties.

- **Strain and Thermal Stress from Contacts:** As we have studied in Chapter 2, the effect of contact evaporation process plays a key role in determining device behavior. The strain induced from the metallization process as well as the thermal stress the TMD film experiences during the high-kinetic bombardment of metal atoms in e-beam evaporation must be studied in detail and its statistical dependence on the electronic properties of the film must be assessed. As we also determined from the holistic approach on contact engineering that compressive strain is beneficial for hole injection, its introduction with minimal damage can be a route forward. This may be achieved by confined area growth and heteroepitaxy growth near contact regions as a means of strain booster.
- **Wrap-around de-pinned Contacts:** Since the contact geometry for the TMD stacked nanosheet will be C-shaped contacts that wrap around the nanosheet, their growth and implementation must be ascertained.³⁰⁵ Growth of high work function as well as high strain contact materials must be developed using industry scalable processes. Atomic Layer Deposition (ALD) or Chemical Vapor Deposition (CVD) alternatives must be explored and the wettability and coating ability of the TMD film must be maximized.
- **Surface Functionalization in Oxidative Environments:** As studied in Chapter 5, layer engineering to improve performance by coalescing TMD domains so as to prevent origins of carrier scattering as well as functionalizing top layers with covalent molecules to controllably dope the underlying film shall remain critical. Preserving the changes from the oxidative environments such as post-anneal capping steps will need to be identified. Tests for air stability although important may not be critical for readiness assessment since capping layers can reduce film sensitivity. Moreover, functionalization techniques

will need to make sure of CMOS process compatibility by confined channel plasma exposures or sequential in the process flow.

- **Controlled Extension Doping:** 2D TMD based devices will need to evolve from contact-gated structures to local channel gated structures to be realizable, practical, and less affected by parasitics. This will shoot up the extension resistance and lead to poor injection. Developing techniques to dope or strain extension/spacer regions will be necessary going forward.
- **Clean and High- κ Dielectric Interface:** As observed in Chapter 4 and 7, the effects of interface can be significant in defining the transport behavior. Growth of dielectric on an inert surface such as that of TMD can be challenging and interface protection from high-temperature processes will be required. The interface challenge will be demanding since low-temperature process leads to a defective surface or bulk properties. Hence, encapsulation with van der Waals insulating materials such as hexagonal Boron Nitride, Calcium Fluoride, Strontium Titanate, etc. will be necessary as well as the use of high- κ dielectrics for low-power and high-performance logic. Interface characterization will be key to predicting subthreshold device performance and measurement techniques discussed in Chapter 7 help with that.
- **Dielectric Environment:** The dielectric environment that the TMD film experiences not only determines its switching properties but there are reports discussing the influence of the dielectric environment on the bandgap of the TMD.^{213,306} This will be important to realize sooner or later when dielectric interfacial layers can be introduced with the intention to not only reduce surface phonon scattering, but also introduce bandgap fluctuations for graded junctions, potential barriers etc.
- **Defect-band Modulation:** Interestingly, the defect bands in capping layers can be optimized such that they benefit device performance by carrier donation or acceptance

into/from the channel. As explored in Chapter 4, the capping layers can provide an additional knob to modulate the device switching behavior making it applicable either for low-power logic or high-performance computing or both. In order to pursue this, detailed material characterization will be required, and a ground-up analysis of the material structure and behavior will need to be understood.

Conclusion

In conclusion, this thesis represents a comprehensive exploration into the development of key transistor components utilizing novel low-dimensional materials that are potential candidates for channel material in advanced logic nodes. From delving into the basics of today's electronic devices to realizing the impact of the CHIPS Act on fostering innovation and further towards dissecting the nuances of von Neumann and Non-von Neumann computing paradigms, it navigates through the capability of 2D TMD based FETs in integrating logic, memory, and security into a single electronic device. Central to this narrative is the elucidation of the urgent need to mitigate challenges and harness the potential of low-dimensional materials, to meet the computing demands of tomorrow. Herein, each transistor component such as the contact, insulator, channel, interface is engineered for improvement. Owing to the limited scientific understanding of p-type transport in 2D FETs, significant fulfillments in engineering p-type contacts, modulating device threshold, and maintaining clean interfaces in TMD channels are documented, offering statistical perspectives on p-type 2D transistor development. Contacts to WSe_2 are explored and a reduction in contact resistance from $40 \text{ k}\Omega \mu\text{m}$ by work-function modulation to $16 \text{ k}\Omega \mu\text{m}$ by contact interface optimization is achieved. Using oxide capping layers, threshold voltage modulation is achieved without any negative impact on channel properties. Layer engineering by growth optimization, layer modification by plasma treatment, and covalent functionalization by annealing provides alternative route to improving device performance thereby achieving a contact resistance of $3.5 \text{ k}\Omega \mu\text{m}$ on p-type WSe_2 FETs. The thesis culminates in an examination of the interfaces with 1D CNT channels, shedding light on the need for interface characterization. This work attempts to contribute to the vast body of existing knowledge systematically and positively on 2D transistor development and aims to guide researchers towards further improvement in p-type 2D FETs, with the ultimate aspiration that the

insights derived from within may one day underpin the electronic advancements of a timeline that is reigned by the unconfined potential of the strictly confined low-dimensional materials.

Appendix A

2D Film Growth and FET Fabrication

Film Growth and Transfer

Monolayer MoS₂ Growth CVD

This material was used in Chapter 2: Secure Memtransistors

MoS₂ was grown by a salt-assisted CVD method. NaBr (Alfa Aesar, 99%) was grounded into a fine powder with a mortar and pestle, then mixed with MoO₃ in a 10:1 ratio by weight. For growth of monolayer films, 2 mg of the salt/oxide mixture was placed in the bottom of a ceramic boat and a piece of SiO₂ (300nm)/Si substrate was placed facing down over the mixture, with ~2 mm of space between the mixture and substrate. 100 mg of sulfur powder (Alfa Aesar, 95%, 300 mesh) was used as the sulfur source. The growth substrate is placed at the centre of the 1-inch diameter horizontal tube furnace (Lindberg/Blue M), while the sulfur powders were placed upstream and outside of the furnace. The synthesis condition was as follows: the tube was flushed with 400 sccm of Ar for 20 min, then the flow was reduced to 100 sccm. The furnace was then heated to 800°C in 20 min and then held for 5 min. The sulfur powder was independently heated to 220°C in 5 min and held for 5 min, while the furnace was kept at 800°C.

Monolayer WSe₂ Growth MOCVD

This material was used in Chapter 4: Electrostatic Modulation by Gating

The pristine, epitaxial WSe₂ films are grown on c-plane sapphire (Cryscore Optoelectronic Ltd, 99.996%) substrates at 800 °C via MOCVD in a custom-designed, vertical cold-wall reactor

reported elsewhere.^{1,2} The surface morphology of the films is evaluated with Verios G4 scanning electron microscope with the accelerating voltage of 2 keV and optical properties are studied with Horiba Labram HR Evolution VIS–NIR Raman system with the 532 nm laser wavelength at 0.5 mW power. Raman spectroscopy demonstrates peaks around 249.1 cm^{-1} and 260.9 cm^{-1} nm that corresponds to characteristic A+E and 2LA(M) Raman modes of WSe₂ where the absence of the interlayer mode at 309 cm^{-1} further confirms the monolayer nature of the films.^{3,4} Moreover, photoluminescence spectroscopy shows an expected optical band gap around 1.65 eV for monolayer WSe₂.

Bilayer WSe₂ Growth CVD

This material was used in Chapter 3: Work-function Engineering to Achieve p-Type Electrical Contacts and Chapter 5: Transition Metal Oxide Layer Doping

The growth of WSe₂ thin films on c-plane sapphire substrates was carried out at 800 °C at 400 Torr in a home-built vertical cold-wall chemical vapor deposition system and at 850-1000 °C at 200 Torr in a horizontal cold wall system for approximately one hour. The tungsten hexacarbonyl (W(CO)₆) (99.99%, Sigma-Aldrich) source was kept inside stainless-steel bubbler where the temperature and pressure of the bubbler were held at 30-37 °C and 650-730 Torr, respectively. Mass flow controllers are used to supply H₂ to the bubbler to transport W(CO)₆ precursor into CVD. In the vertical system, the flow rate of the H₂ gas through the bubbler is maintained at constant 8 sccm (standard cubic centimeters per minute) which resulted in a W(CO)₆ flow rate of 9.0×10^{-4} sccm at the outlet of the bubbler. H₂Se (99.99%, Matheson) gas is supplied from a separate gas manifold and introduced at the inlet of the reactor at a constant flow rate of 60 sccm. In the horizontal system, the W(CO)₆ flow rate was 3.1×10^{-3} sccm and the H₂Se flow rate was 75 sccm.

Layer-controlled WSe₂ Growth MOCVD

This material was used in Chapter 3: Contact Interface Engineering, Chapter 4: Oxide Capping Layers for Surface Charge Transfer, and Chapter 5: Controlled Bilayer Growth of WSe₂

The MOCVD system is equipped with a cold-wall horizontal reactor with an inductively heated graphite susceptor with gas-foil wafer rotation.³⁰⁷ Tungsten hexacarbonyl (W(CO)₆) with the purity $\geq 99.9\%$ (trace metals basis) is purchased from Sigma-Aldrich, LLC was used as a metal precursor. Hydrogen Selenide (H₂Se) was used as a chalcogen gaseous precursor. Hydrogen (H₂) was used as a carrier gas. C-plane sapphire with a 2" diameter and a nominal $\pm 0.2^\circ$ miscut towards the M-axis was used for all growths. The W(CO)₆ powder was maintained at 30 °C and 400 torr in a stainless-steel bubbler. The synthesis of WSe₂ is based on a multi-step process, consisting of nucleation, ripening, and lateral growth steps, described previously.²³⁴ WSe₂ samples were nucleated for 30 s at 850 °C, then ripened for 10 min at 850 °C and 10 min at 1000 °C, and then grown at 1000 °C for a specific time. During the lateral growth, the tungsten flow rate was set as 3.8×10^{-3} sccm and the chalcogen flow rate was set as 75 sccm while the reactor pressure was kept at 200 torr. Then, the WSe₂ film was annealed under H₂ and H₂Se ambient for 10 min and the H₂ and H₂Se ambient was maintained for 8 min as the chamber was cooled down to provide additional time for metal adatom diffusion and to reduce selenium vacancies.

Substrate	WSe ₂ Growth on 2" C-plane sapphire				Post Growth Annealing
	Pre growth Annealing	Nucleation	Ripening	Lateral Growth	
2" C-plane Sapphire	H ₂ 850 C 10 mins	30s @ 850C; 14 sccm through W(CO) ₆ bubbler, 75 sccm H ₂ Se	10min @ 850C, 10min @ 950C, 75 sccm H ₂ Se	20-30 min @ 950C, 7 sccm through W(CO) ₆ bubbler, 75 sccm H ₂ Se	H ₂ +H ₂ Se 75 sccm 950 C 10 mins

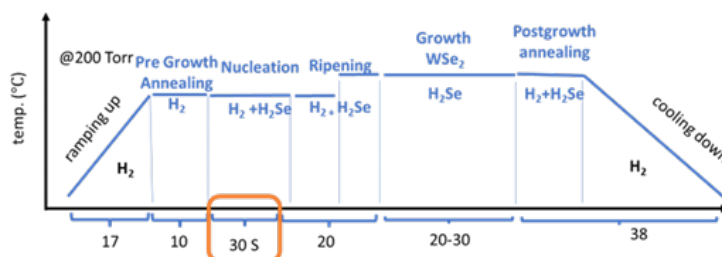


Figure A-1: Growth flow chart for controlled bilayer growth of WSe₂

Monolayer MoSe₂ Growth CVD

This material was used in Chapter 5: Multilayer WSe₂ and MoSe₂ FETs

Two solutions were prepared by dissolving AHM ((NH₄)₆Mo₇O₂₄, Alfa Aesar, purity of 99.999%; 0.05 g) and sodium cholate hydrate (0.2 g) into DI water (10 mL), respectively. Freshly mixed solutions (30uL AHM solution mixed with 300uL sodium cholate hydrate solution) were spin-coated onto a clean SiO₂ (300 nm)/Si substrate (3000 rpm, 1 min). Subsequently, the precursor-coated substrate was loaded in the center of a quartz reaction tube, and selenium powder was placed in an alumina boat located upstream. During synthesis, the furnace was first ramped up to 800 °C in 30 min and then held at 800°C for 15 min for growth. Simultaneously, the selenium powder was vaporized at 375 °C during the 15 minutes of growth stage, allowing the selenization of the spin-coated precursors. Ultra-high purity Ar gas was used for purging the tube before and during the ramping up process. 100sccm Ar/H₂ mix (85%Ar, 15%H₂) was used during the 15 minutes of growth at 800°C. After the growth finished, the carrier gas was switched back to pure Ar, letting the monolayer samples naturally cool down to room temperature.

WSe₂ film transfer to target substrates

To fabricate the WSe₂ field-effect transistors, the bilayer WSe₂ film was first transferred from the sapphire growth substrate to the global back-gated Al₂O₃/Pt/TiN/p⁺⁺-Si substrate using a polymethyl-methacrylate (PMMA)-assisted wet transfer process. First, the WSe₂ film on the sapphire substrate was spin-coated with PMMA and baked at 150 °C for 2 min to ensure good PMMA/WSe₂ adhesion. The corners of the spin-coated film were scratched using a razor blade and immersed inside a 2 M NaOH solution kept at 90 °C. Capillary action caused the NaOH to be preferentially drawn into the substrate/film interface due to the hydrophilic nature of sapphire and the hydrophobic nature of WSe₂ and PMMA, separating the PMMA/WSe₂ film from the sapphire substrate. The separated film was then fished from the NaOH solution using a clean glass slide and rinsed in three separate water baths for 15 min each before finally being transferred onto the target substrate. Subsequently, the substrate was baked at 50 °C and 70 °C for 10 min each to remove moisture and promote film adhesion, thus ensuring a pristine interface, before the PMMA was removed using acetone immersion over-night and the film was cleaned with IPA.

E-beam Lithography and Channel Isolation Etch

Features < 100 nm

The ultra-scaled devices were fabricated using a two-step ebeam lithography process, where the scaled source-drain contact terminals were patterned, evaporated, and lifted-off in the first step using a single layer ebeam photoresist, followed by the second step which involved patterning, evaporation, and lift-off of large contact pads shorted to the scaled source/drain terminals for access and measurements. ZEP 520A 1:1 is used as the photoresist in the first step. Prior to resist spinning, the sample is dipped in Surpass 4K for 60 s, rinsed in DI water, and baked

at 100 °C for 1 min. This is done to improve the adhesion of the photoresist to the substrate that contains exposed metal alignment markers. The sample is then spin-coated at 5000 RPM for 45 s and baked at 180 °C for 3 min. The sample is then exposed using ebeam lithography. The ultra-scaled patterns exposed in the first step are developed using a cold-develop process involving organic solvent n-amyl acetate chilled to -10 °C (3 min) and then rinsed in IPA for 60 s. Post the develop process, 20 nm of palladium is evaporated using e-beam evaporation, which now serves as contacts to the WSe₂. Remaining metal on the photoresist is lifted-off with immersion in acetone for 30 min. The sample is then immersed in Photo Resist Stripper 3000 (PRS 3000) heated at 60 °C on a hotplate for 15 mins to completely remove the resist. Higher adhesion of the resist to the substrate can make it difficult to strip the resist, thus requiring the use of a pipette or a purge bottle to purge with acetone or PRS 3000 depending on the solvent used. Following the resist removal, the sample is rinsed with IPA for 10 min. For the second step, contact pads are again defined using ebeam lithography. Now, the sample is spin coated with methyl methacrylate (MMA) followed by A3 PMMA. E-beam lithography is used to pattern the large access pads that overlap with the ultra-scaled source and drain contacts on the WSe₂ channel. The sample is developed using a 1:1 mixture of MIBK/IPA for 60 s and pure IPA for 45 s. Next, 40 nm of palladium and 30 nm of gold are deposited using e-beam evaporation. Finally, a lift-off process is performed to remove the evaporated palladium/gold except from the source/drain patterns by immersing the sample in acetone for 30 min followed by IPA rinse for another 10 min.

Features > 100 nm

To define the source and drain contacts, the sample was then spin coated with methyl methacrylate (MMA) followed by A3 PMMA. E-beam lithography was again used to pattern the source and drain contacts. The sample was then developed using a 1:1 mixture of MIBK/IPA for 60 s and pure IPA for 45 s. Next, 40 nm of palladium and 30 nm of gold were deposited using e-

beam evaporation. Finally, a lift-off process was performed to remove the evaporated palladium/gold except from the source/drain patterns by immersing the sample in acetone for 30 min followed by IPA rinse for another 10 min.

Channel Definition

To define the channel regions for the WSe₂ FETs, the substrate was spin-coated with PMMA and baked at 180 °C for 90 s. The resist was then exposed via an electron beam (e-beam) and developed using a 1:1 mixture of 4-methyl-2-pentanone (MIBK) and IPA. The bilayer WSe₂ film was subsequently etched using a sulfur hexafluoride (SF₆) reactive ion etch chemistry at 5 °C for 30 s. Next, the sample was immersed in acetone overnight and cleaned with IPA to thoroughly remove the photoresist.

Contact Deposition

Nickel, Palladium, and Platinum

Metal evaporation was done in a Ferrotec Temescal F-2000 evaporator with a standard fixture that allows for a substrate to source crucible distance of at least 50 cm. Radiative damage is prevented during ramp-up process by closing both the substrate and crucible shutters until a stable deposition rate is achieved. It is important to note that the shutters cannot fully protect the substrate and the metal atoms can still find alternative pathways to get to the substrate from the open sides. For our scaled device fabrication (< 100 nm), we limit the metal contact thickness to 20 nm. Since also use a lower deposition rate, i.e., 0.5 Å/s, hence a back-of-the-envelope calculation from the methods suggested by Wang et al., suggests a ~340 kJ irradiation energy ($85\text{ mA} \times 10\text{ kV} \times 400\text{ s}$) on the substrate from Pd metal evaporation. This, however, is very much dependent on the chamber conditions. The reason for the choice of a low deposition rate is

to have better adhesion of the contacts with the substrates since the fabrication involves a lift-off process. Using higher deposition rate for scaled device fabrication leads to a very poor contact adhesion yield. Another point worth noting is that, in the cited article, the authors have only fabricated long channel devices (> 100 nm) and the high deposition rate process is favored. The dependence on base vacuum pressure is a very interesting topic and has been looked into in great detail¹⁷⁹. However, the findings have been difficult to reproduce by other researchers in the community and have not produced exceedingly impressive results. It is also justifiable that at low pressures in the chamber, the kinetic energy of the metal atoms is reduced due to the reduction in the effective mean free path of a metal atom being excited and leaving the crucible. We use a base vacuum pressure of 3×10^{-6} which is maintained throughout the evaporation process. The temperature of the chamber is monitored to be around $18^\circ\text{C} - 19^\circ\text{C}$. Substrate temperature may however be different and may also depend on the chamber conditions. Moreover, the initial 4 – 5 nm (100 s of deposition duration) of evaporated metal film plays a key role in deciding the interface properties, thus deciding the device behavior. An additional idle time (~ 10 minutes) is set to allow the system to cool down post-deposition. Another point worth noting is that ebeam evaporation of thin films at higher deposition rates usually results in patchy films with non-uniform coverage and imperfections along the thickness. Allowing elongated durations of idle time between deposition steps could also result in variation of surface chemistry of the underlying 2D material affected by the contents of the process chamber. All-in-all, a high-level understanding of the damage resulting from contact metal evaporation is not possible due to a convolution of various factors at the nanoscale. Hence, in our proposed methods, we perform a thorough study of the interface between the metal contact and the 2D material with the help of STEM imaging, where we extract the grain size of the metal films, calculate the type of strain imparted on WSe_2 , and study the epitaxy relationship between the three metals namely, Ni, Pd, and Pt.

Selenium Interlayer to Palladium

Selenium deposition and annealing under ultra-high vacuum (UHV) was done in a model R450 molecular beam epitaxy system (MBE) manufactured from DCA Instruments, Oy in Finland at a background pressure in the low 10^{-9} Torr range. The chip temperature during Se deposition was 10°C as measured by a thermocouple on the backside of the sample holder stage. Set at a constant rotation of 3 rpm, the chip was exposed to a Se flux equivalent to a rate of $0.1 \text{ \AA/s}$ generated by a simple Knudsen effusion cell for about 15 min to coat the chip with a 10-nm-thick amorphous Se film. The Se flux and rate was determined prior to deposition using a Quartz Crystal microbalance device Eon from Colnatec calibrated by physical film thickness measurements using X-ray reflectivity. During the UHV anneal, the chip was not exposed to any molecular flux in the MBE system, solely heated to 250°C (as measured by the sample stage thermocouple behind the chip) for 1 h with heating and cooling ramp rates of $10^{\circ}/\text{min}$. Following that, metal evaporation was done in a Ferrotec Temescal F-2000 evaporator with a standard fixture that allows for a substrate to source crucible distance of at least 50 cm. We also use a lower deposition rate, i.e., $0.5 \text{ \AA/s}$. The reason for the choice of a low deposition rate is to have better adhesion of the contacts with the substrates since the fabrication involves a lift-off process. We use a base vacuum pressure of 3×10^{-6} which is maintained throughout the evaporation process. The temperature of the chamber is monitored to be around $18^{\circ}\text{C} - 19^{\circ}\text{C}$. Substrate temperature may however be different and may also depend on the chamber conditions.

Top-gate Metal Fabrication

A thin 1 nm seed layer of aluminum (Al) is evaporated using e-beam to allow uniform growth of 20 nm of top-gate oxide, Al_2O_3 by ALD at 150°C . Lower temperature ALD growth prevents underlying WSe_2 nanosheet from degradation. Finally, the sample is spin coated with

MMA/PMMA and patterned with e-beam lithography to define top-gate electrode. Post-develop, 70 nm of palladium (Pd) was e-beam evaporated as top-gate electrode, which was followed by lift-off with acetone and IPA.

Electrical characterization

Transport Measurements

Lake Shore CRX-VF probe station and Keysight B1500A parameter analyzer were used to perform the electrical characterization at room temperature in high vacuum ($\approx 10^{-6}$ Torr). Electrical characterization of the fabricated devices was also performed using a semi-automated Formfactor 12000 probe station in atmospheric conditions also with a Keysight B1500A parameter analyzer. Characterization of CNT FETs were performed in room temperature on MPI Semi-automated Probing tool along with B1500A. Fast pulse measurement unit B1530A was also programmed as and when it was necessary.

Impedance Measurements

Impedance measurements of CNT MOS structures were carried out in room temperature on MPI Semi-automated Probing tool along with B1500A and LCR meter E4980A and at low-temperature on a Lakeshore CRX-VF probe station. Lock-in amplifier and Picoprobe setup was used for ultra-low capacitance measurements. Fast pulse measurement unit B1530A was also programmed as and when it was necessary.

Material Characterization

Raman and PL Characterization

Raman and photoluminescence (PL) spectra were taken using a Witec Alpha-300 Apyron system within a N₂-ambient glovebox with ~5ppm of O₂ and H₂O. Single point Raman and PL spectra were taken using the 100X objective at a 4mW laser power for 30s and 3 accumulations and 5s and 2 accumulations. Raman and PL spectra spot scans were performed with a laser power of wavelength 532 nm.

Atomic Force Microscopy (AFM) Characterization

Bruker Icon II is used to perform AFM analysis with RTespa tips for contact mode study.

XRD characterization

X-Ray Diffraction is done with a PANAnalytical X'Pert 2 Diffractometer with a Cu-K α source. Samples are first aligned to the (400) silicon peak to ensure orientation in the z direction, then measured in a 2θ - ω scan through a $\frac{1}{2}''$ slit to reduce the amount of out of plane noise in the data.

Oxide XPS characterization

XPS experiments were performed using a Physical Electronics VersaProbe III instrument equipped with a monochromatic Al K α x-ray source ($h\nu = 1,486.6$ eV) and a concentric hemispherical analyzer. Charge neutralization was not utilized. The binding energy axis was calibrated using sputter cleaned Cu (Cu 2p_{3/2} = 932.62 eV, Cu 3p_{3/2} = 75.1 eV) and Au foils (Au 4f_{7/2} = 83.96 eV). Measurements were made at a takeoff angle of 45° with respect to the sample surface plane. This resulted in a typical sampling depth of 3-6 nm (95% of the signal originated

from this depth or shallower). Quantification was done using instrumental relative sensitivity factors (RSFs) that account for the x-ray cross section and inelastic mean free path of the electrons. On homogeneous samples major elements (>5 atom%) tend to have standard deviations of $<3\%$ while minor elements can be significantly higher. The analysis size was $\sim 200\mu\text{m}$ in diameter. Sputtering used a 2 kV Ar^+ ion beam. The estimated sputter rate was 4.3 nm/min.

Ultraviolet Photoemission Spectroscopy (UPS) Characterization

UPS measurements were made within the VersaProbe III XPS at a takeoff angle of 90° (normal to the sample surface) using He I (21.22 eV). Samples were grounded using a gold foil sandwiched with a copper clip to ensure the films were well grounded. The sample was biased -5V during UPS measurements to permit collection of the secondary electron cutoff (SECO) region used for work function determination. The UPS spectral intensities were corrected for the weak contributions from He I $^\alpha$ (23.09 eV), He I $^\beta$ (23.75 eV) and He $^\gamma$ (24.05 eV) photons that are generated during the He-discharge.³⁰⁸

Valence Band Maxima (VBM) Extraction

VBM were determined by both XPS and UPS using a linear extrapolation of the leading edge of valence band spectrum to the background.

Transmission electron microscopy (TEM)

The sample for characterizing the cross-section of the device was prepared by an FEI Helios nanofab 660 focus ion beam (FIB) following the general TEM sample preparation process with a final cleaning at 1 kV. To get the strain condition in c-plane, the 5 nm metal (Ni or Pt or Pd) was directly deposited on the WSe_2 /sapphire substrate to get the metal (Ni or Pt or Pd)/ WSe_2 /sapphire. Same to the process of transferring WSe_2 to target substrates, the PMMA-

assisted wet transfer process was used to transfer metal (Ni or Pt or Pd)/WSe₂ onto the Quantifoil® TEM Substrate (658-200-CU-100, Ted Pella) for the further TEM characterization. The analysis of the strain and FWHM on the SAED patterns were based on the py4DSTEM framework³⁰⁹. STEM-HAADF was performed using an aberration-corrected ThermoFisher Titan³ G2 60-300 with monochromator and X-field emission gun source at an accelerating voltage of 80 kV and the EDS mapping was performed in the same TEM at an accelerating voltage of 80 kV. The convergence semi-angle used for STEM imaging was 25 - 30.0 mrad and the collection angle range of the HAADF detector was 42-244 mrad. Selected area electron diffraction (SAED) spot patterns were collected using a ThermoFisher Talos F200X transmission electron microscope at an accelerating voltage of 200 kV. The SAED simulations were performed using the SingleCrystal 4 software.

Text Paraphrase and Image Generation

Large language models such as ChatGPT and Claude AI were employed to enhance the quality of the text along with paraphrasing for improved readability.^{310,311} c DALL.E and Adobe Illustrator were used for image generation purposes.^{312,313}

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VITA

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Aaryan Oberoi was born in Allahabad, India and later moved to Bangalore, India during his primary schooling. He graduated from Amrita Vishwa Vidyapeetham, Bangalore Campus with a Bachelor of Technology in Electronics and Communications Engineering (First Class with Distinction) in 2019. In the final semester of his undergraduate studies, he went to Pennsylvania State University for an internship in Prof. Saptarshi Das's research group. After that, he joined Prof. Saptarshi Das's group as a doctoral student in the Fall of 2019. His doctoral research focused on developing non-von Neumann computing primitives inspired from neuromorphic algorithms in the first two years of his doctoral studies. In the next three years he focused on improving the performance of p-type electrical contacts to 2D materials. During his doctoral research, he co-authored 13 peer-reviewed journal and conference articles. Following his PhD degree, he will work on leading-edge Silicon devices in the semiconductor industry.