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MAGNETIC RESONANCE OBSERVATIONS OF DEFECTS INVOLVED IN BIAS TEMPERATURE INSTABILITIES AND STRESS INDUCED LEAKAGE CURRENTS IN HfO_2 AND SiO_2 BASED METAL-OXIDE-SILICON STRUCTURES

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ABSTRACT

This study examines underlying physical mechanisms involved in two very important reliability problems in SiO_2 based and HfO_2 based metal-oxide-silicon technology: the negative bias temperature instability (NBTI) and an important aspect of low-voltage stress induced leakage currents (LV-SILC). A combination of conventional electron spin resonance (ESR), electrically-detected magnetic resonance including spin dependent recombination (SDR) and spin dependent tunneling (SDT), and electrical measurements have been utilized to study variously processed samples in an attempt to understand the specific defects and the roles that they play in these reliability problems.

After a brief introduction and background, chapter 3 discusses a newly developed means to perform SDT on ultra-thin oxides which we call energy-resolved spin dependent tunneling and is used to directly determine the energy levels of K centers involved in LV-SILC in nitrided SiO_2 devices. In chapter 4, a newly developed ESR technique which we call on-the-fly ESR is utilized to study the triggering mechanisms of NBTI in pure SiO_2 devices. Chapter 5 utilizes SDR measurements on SiO_2 based structures and attempts to examine the role that fluorine plays in suppressing NBTI in pure SiO_2 devices while doing little to suppress NBTI in nitrided SiO_2 devices. Chapter 6 presents a conventional ESR and SDR study which attempts to identify the electronic and physical nature of pre-existing trapping centers in the SiO_2 like interfacial layer region of HfO_2 based devices which are thought to play important roles in limiting the performance and reliability of these structures.

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LIST OF ABBREVIATIONS

ALD	atomic layer deposition
DC-IV	direct current gate controlled diode recombination current versus voltage
DOS	density of states
EB ISSG	etch back in-situ steam generated oxide
EDMR	electrically-detected magnetic resonance
EOT	equivalent oxide thickness
ER-SDT	energy-resolved spin dependent tunneling
ESR	electron spin resonance
IC	integrated circuit
ISSG	in-situ steam generated oxide
LV-SILC	low-voltage stress induced leakage current
MOS	metal-oxide-silicon
MOSFET	metal-oxide-silicon field-effect-transistor
NBTI	negative bias temperature instability
NBTS	negative bias temperature stress
nMOSFET	n-channel metal-oxide-silicon field-effect-transistor
PBTI	positive bias temperature instability
pMOSFET	p-channel metal-oxide-silicon field-effect-transistor
SDR	spin dependent recombination
SDT	spin dependent tunneling
SILC	stress induced leakage current
SRH	Shockley-Read-Hall

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This dissertation is dedicated to the memory of

Thomas B. Ryan

December 27, 1922 – August 28, 2008

and

Elizabeth A. Ryan

June 14, 1924 – June 24, 2008

Chapter 1

INTRODUCTION

Over the last several decades, our society has witnessed the incredible growth and global impact of the microelectronics industry. This is in a large part due to the availability of new integrated circuits (ICs) which perform better than their predecessors just a few years old. The increase in processing power of ICs has been accomplished through the down-scaling of individual circuit components, in particular, the metal-oxide-silicon field-effect-transistor (MOSFET). By reducing the physical size of the individual MOSFETs, the switching time is reduced and hence the device performs faster. With smaller devices, engineers are also able to manufacture ICs with a higher density of MOSFETs in a given area, dramatically increasing the potential processing power. Moore's law [1], first proposed in 1965 and later revised in 1975, predicts that the number of transistors per IC (and hence the processing power) will approximately double every two years; remarkably, this has been true for over 40 years.

Much of this success is due to the remarkable nature of the Si/SiO_2 system which displays outstanding quality and reliability. For much of the history of microelectronics, Si/SiO_2 has been the essential building block. Until recently, MOSFET down-scaling (in particular the thinning of the SiO_2 gate oxide) has been accomplished almost unimpeded. Now, as SiO_2 based gate dielectrics approach 1nm in thickness, the fundamental physical limits of the SiO_2 based gate dielectric are being pushed [2]. Excessively high gate leakage currents and the exacerbation of reliability limiting phenomena along with the physical limitations of the dielectric have threatened to halt Moore's law [2]. In the last

decade, engineers have devised ways to overcome the limitations of conventional SiO_2 gate dielectrics by replacing them with a different material, one with a higher dielectric constant than pure SiO_2 (the so called high-k dielectrics) [2].

An analysis of the capacitance of a MOSFET gate stack is useful in understanding the advantages of MOSFET down-scaling. The easiest way to visualize this is by modeling the MOSFET gate stack as a simple parallel plate capacitor whose capacitance per unit area (C) is given by:

$$C = \frac{k\varepsilon_0}{t}, \tag{1.1}$$

where k is the dielectric constant of the dielectric, ε_0 is the permittivity of free space, and t is the thickness of the dielectric (i.e. the separation of the parallel plates). Over the last 40-plus years, MOSFET down-scaling has reduced the "t" of equation (1.1) to yield a higher gate capacitance per unit area which results in a higher switching speed of the device [3]. As mentioned previously, the SiO_2 based gate dielectrics cannot be made any thinner due to its electrical, physical, and reliability limitations [2]. Thus, the only other parameter which can be controlled is the dielectric constant (k) of the insulating material. Increasing "k" in equation (1.1) results in a higher capacitance for a given dielectric thickness. Perhaps more importantly, implementing a high-k dielectric allows for an equivalent capacitance with a physically thicker film. The physically thicker film will drastically reduce leakage currents while maintaining electrical equivalency [2]. For example, replacing a 1nm thick SiO_2 ($k \approx 4$) oxide with a dielectric of $k \approx 20$ would allow for a film about 5nm thick with an equivalent capacitance. Typically, this is expressed as an equivalent oxide thickness (EOT) [2]; the 5nm high-k film would have an EOT of 1nm.

The first "high-k dielectric" has been around for quite some time: nitrided SiO_2 in which nitrogen is incorporated into SiO_2 [4]. The nitridation scheme results in a modest increase of the dielectric constant of the SiO_2. Nitrided SiO_2 could theoretically have a dielectric constant as high as 7.5 (pure Si_3N_4) but typically, the nitrogen content is held around 10% resulting in a dielectric constant of about 4 - 4.5 compared to k = 3.9 for pure SiO_2 [4]. This small increase in dielectric constant helps to alleviate some of the device scaling issues previously mentioned. Perhaps more importantly, nitrided SiO_2 also has the added advantage of reducing boron penetration into the gate stack which can lead to threshold voltage shifts and decreased reliability [4]. Although the nitrided SiO_2 approach has been widely utilized and works remarkably well, a much larger gain in dielectric constant is needed to allow Moore's law to continue for device generations to come.

Many studies have been performed to determine the most suitable replacement of SiO_2 and nitrided SiO_2 gate dielectrics [2, 5-7]. Of these potential replacements, it seems that hafnium based dielectrics will be the MOSFET gate dielectrics of the near future. Intel Corporation and IBM Corporation have both announced (or started) full scale production of 45nm node microprocessors containing hafnium based gate dielectrics [8, 9]. This is arguably the biggest change to high performance MOSFETs in the history of metal-oxide-silicon (MOS) technology.

In early studies of high-k device research, the range of potential replacement dielectrics explored was great [2, 5-7] and most studies focused on improving device performance [2, 3, 5]. Now that there is a widespread consensus on what the replacement dielectric will be (hafnium based) and high quality devices are feasible, high-k research

now includes reliability studies of hafnium based devices. As of now, no comprehensive study relating atomic-scale defect structure to device degradation reliability issues has been performed.

Although it seems that state-of-the-art high performance ICs (for example microprocessors) will be made with high-k hafnium based dielectrics, pure SiO_2 and nitrided SiO_2 are still important gate dielectric materials for many applications [4]. Despite a large amount of work, important reliability issues are not yet fully understood and are a source of widespread controversy in these devices [10].

1.1 Bias Temperature Instabilities

The negative bias temperature instability (NBTI) and the positive bias temperature instability (PBTI) are device degradation phenomena occurring as a result of moderate gate bias at elevated temperatures. NBTI is manifested as a shift in threshold voltage as well as a degradation in saturation drive current following the application of significant negative gate bias and elevated temperature to p-channel MOSFETs (pMOSFETs) [10]. PBTI manifests itself in a similar manner following the application of significant positive gate bias at elevated temperatures in n-channel MOSFETs (nMOSFETs) [11]. It's important to note that in SiO_2 based devices, PBTI is not a major source of concern [12]. However, both NBTI and PBTI are believed to be major reliability limiting phenomena in HfO_2 based devices [11, 13, 14].

Although the phenomena have been observed and studied in conventional SiO_2 and nitrided SiO_2 devices for several decades [15] the exact mechanisms and defects responsible for NBTI induced device degradation are still topics of widespread

controversy [10, 16, 17]. However, it is generally accepted that following a negative bias temperature stress (NBTS), interface trap generation and/or charge build up in the bulk of the oxide is the source of the device degradation [10, 16, 17]. The specific role each plays is still a major source of controversy. Examining a simple expression for the threshold voltage of a pMOSFET is an easy way to visualize the potential sources of NBTI threshold voltage degradation:

$$V_T = \phi_{MS} - \frac{Q_{ot}}{C_{OX}} - \frac{Q_{it}}{C_{OX}} - 2\phi_F - \frac{\left|\sqrt{4\varepsilon_S \phi_F q N_D}\right|}{C_{OX}}, \qquad (1.2)$$

where V_T is the threshold voltage, ϕ_{MS} is the metal-semiconductor work function difference, Q_{ot} is the oxide charge, C_{OX} is the oxide capacitance, Q_{it} is the interface charge, ϕ_F is the difference between the bulk Fermi level and intrinsic level, ε_S is the permittivity of silicon, q is electronic charge, and N_D is the substrate doping level [18]. Assuming the substrate doping (N_D) and oxide capacitance (C_{OX}) remains constant during a NBTS, only a change in oxide charge (Q_{ot}) or interface charge (Q_{it}) can explain the observed shift in threshold voltage [18]. Although this simple exploration reveals that interface state generation and/or oxide charge generation is the source of the threshold voltage shift, the specific roles that each plays is still a major source of controversy and confusion [10, 16, 17].

Traditionally, NBTI has been explained in terms of some type of reaction-diffusion model [10, 16, 17]. Although the reaction-diffusion model generally makes physical sense, many variations of this general idea exist and certain aspects of NBTI are not well explained [16]. A complete picture explaining a wide range of circumstances is

not available. In the general reaction-diffusion model, a reaction takes place during a NBTS which depassivates a silicon-hydrogen bond at the Si/SiO_2 interface [10, 16, 17]. A Si/SiO_2 interface state (apparently a P_b center in pure SiO_2 devices [19, 20]) is created and the hydrogenic species diffuses into the gate stack as an oxide charge; this process leads to the observed shift in threshold voltage and degradation of drive current [10, 16, 17]. The observation of NBTI recovery [21, 22], a process in which much of the NBTI damage disappears, is explained as the reversal of this process. When the NBTS is removed, some of the hydrogenic species diffuse back to the interface and repassivate the interface states [10, 16, 17]. It should be noted that NBTI recovery has only recently been observed [21, 22] and is perhaps the most challenging aspect of NBTI. Recent studies of NBTI recovery [21-24] call into question the validity of conclusions drawn in earlier NBTI studies in which recovery was not accounted for. Additionally, recovery cannot be fully explained by the reaction-diffusion model. As noted by Grasser *et al*., the reaction-diffusion model predicts a universal recovery phenomena nearly independent of the hydrogenic species involved [16]. Additionally, in contrast to some experimental studies [25-28], Grasser *et al*. [16] note that the reaction-diffusion model fails to predict recovery which depends on gate bias, temperature and process conditions.

Recent conventional electron spin resonance (ESR) observations of Fujieda *et al.* [19] on simple Si/SiO_2 capacitors and electrically-detected magnetic resonance (EDMR) observations of Campbell *et al.* [20, 29, 30] on fully processed transistors suggest that NBTI is dominated by Si/SiO_2 interface states (P_b centers) in pure SiO_2 structures. When subject to very severe NBTS conditions, Campbell *et al.* [20, 29, 30] also observed E' centers generated. Although their experimental observations are somewhat tenuous,

Campbell *et al.* suggest that E' centers could trigger the NBTI process via an E' center/P_b center hydrogen exchange [20, 29, 30]. This general idea, that NBTI is caused by an E'/P_b center hydrogen exchange triggered by hole capture at an E' site, has been expressed by Lenahan [31, 32] who provides simple thermodynamics based arguments to this effect. The experimental results of Conley *et al.* [33, 34] clearly demonstrate that multiple E'/P_b center reactions are thermodynamically and kinetically possible. Figure 1.1 provides schematic drawings of the two types of interface states commonly found in (100) Si/SiO_2, the P_{b0} (top) and P_{b1} (bottom) centers [35]. Both P_{b0} and P_{b1} centers are silicon dangling bond defects in which the central silicon atom is back-bonded to three other silicon atoms. Both defects are located precisely at the Si/SiO_2 interface. Figure 1.2 illustrates schematic drawings of two E' centers commonly found in pure SiO_2: a neutral oxygen vacancy (top) and a positively charged oxygen vacancy (bottom) [35]. E' centers are silicon dangling bond defects in which the central silicon atom is back-bonded to three oxygen atoms.

Lenahan [31, 32] notes that the correlation between Si/SiO_2 P_b centers and E' oxide defects frequently observed in ESR studies of variously processed Si/SiO_2 samples may be relevant to NBTI degradation. Figure 1.3a schematically illustrates an Si/SiO_2 interface before (1.3a) and after (1.3b) oxide stressing. The interface of 1.3a is typical of oxides which received a forming gas anneal following thermal oxidation of SiO_2; Si/SiO_2 P_b interface states are hydrogen passivated. Lenahan [31, 32] argues that if the oxide stress generates a large number of E' oxide defects (figure 1.3b), and if the bonding energies of the Si-H bond at the hydrogen passivated P_b center and a Si-H bond at a hydrogen passivated E' center are about the same, the illustration of figure 1.3b is

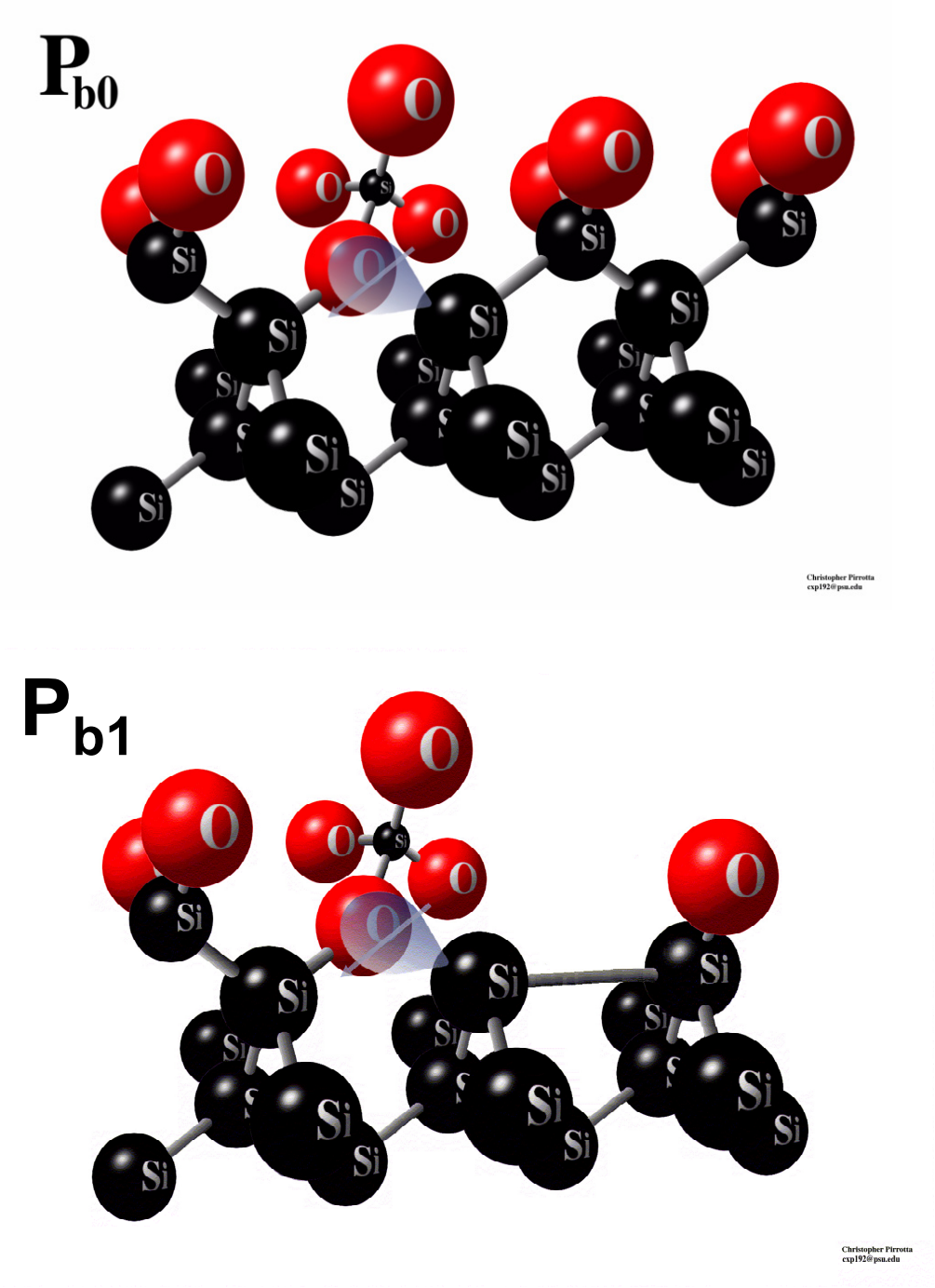

Figure 1.1: Schematic drawings of P_{b0} (top) and P_{b1} (bottom) Si/SiO_2 interface states. P_{b0} and P_{b1} defects dominate interface trapping in (100) Si/SiO_2. Both are silicon dangling bond defects in which the central silicon atom is back-bonded to three other silicon atoms.

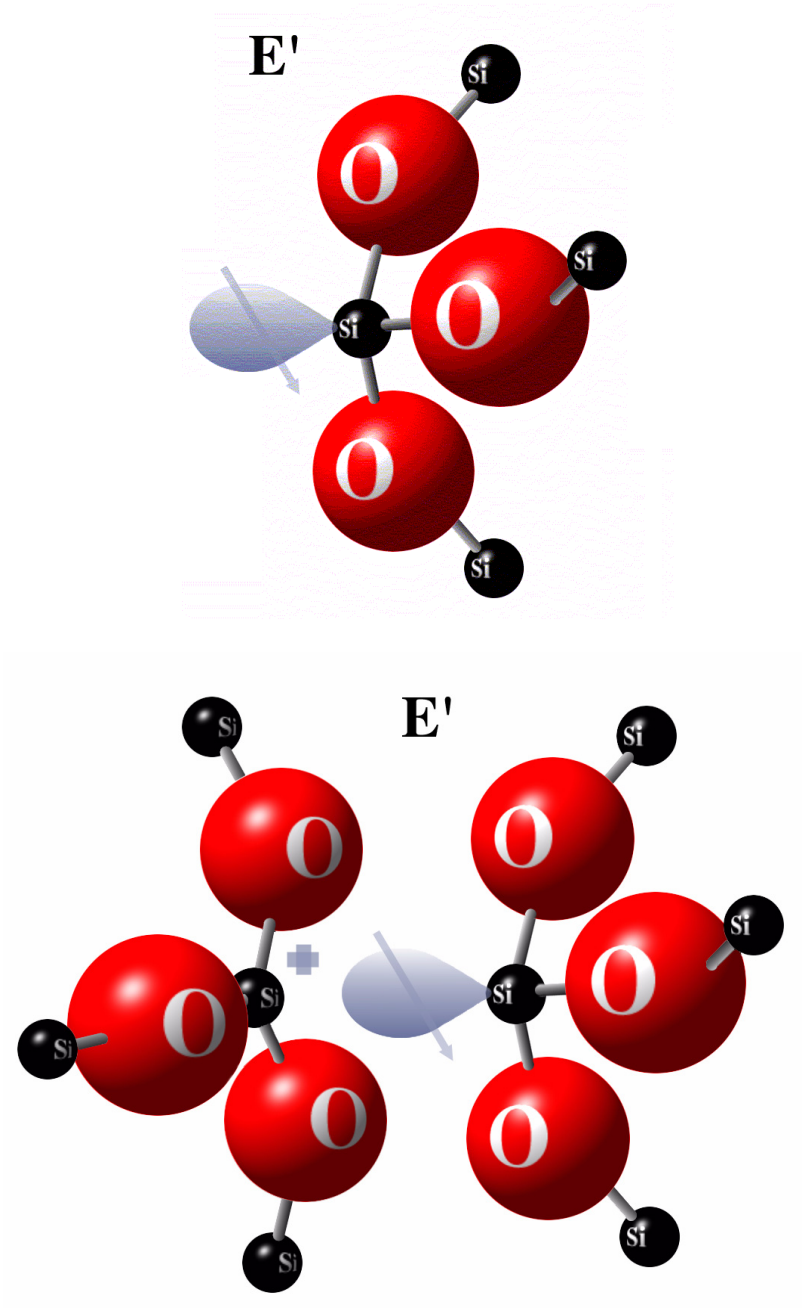

Figure 1.2: Schematic drawings of two E' centers commonly found in pure SiO_2; a neutral oxygen vacancy (top) and a positively charged oxygen vacancy (bottom). E' centers dominate charge trapping in pure SiO_2 dielectrics. They are silicon dangling bond defects in which the central silicon atom is back-bonded to oxygen atoms.

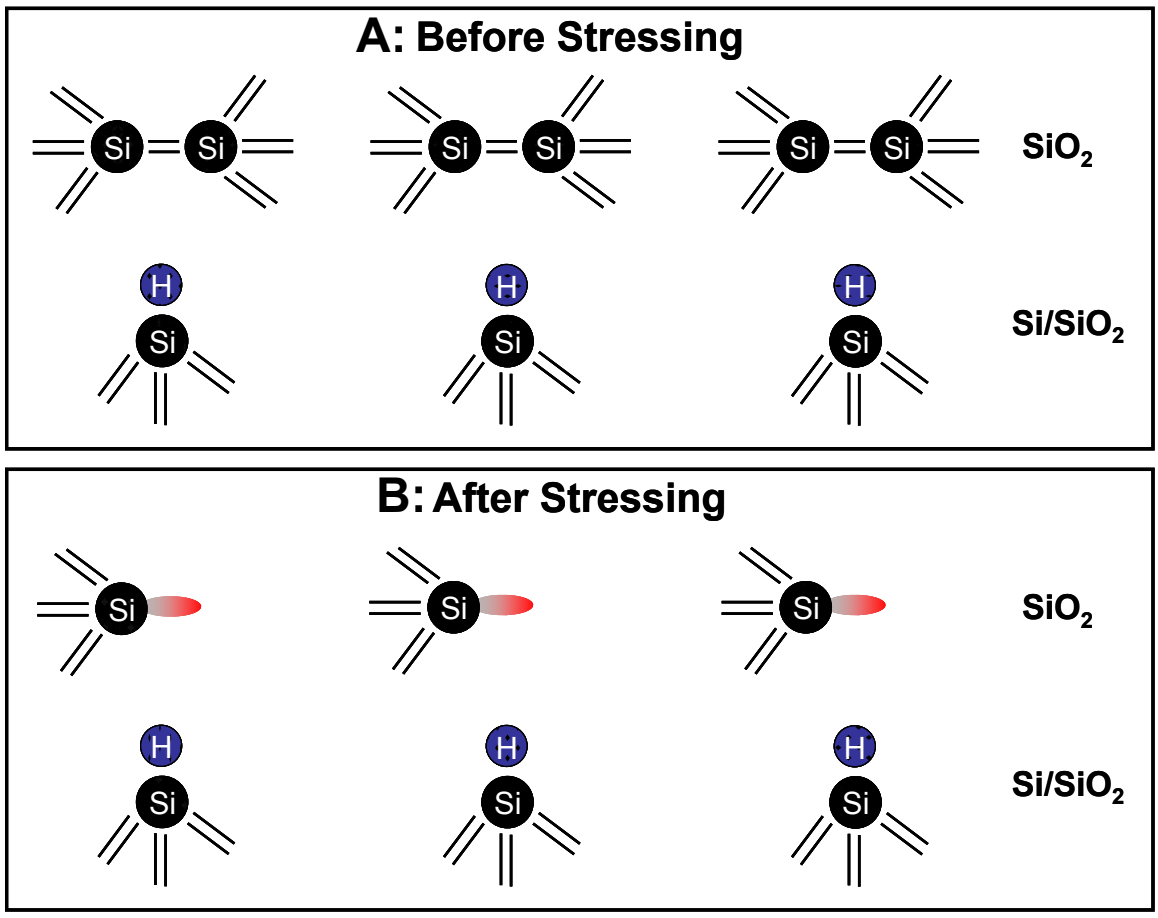

Figure 1.3: Two simplified illustrations of the Si/SiO_2 interface. (a) A perfect interface prior to stressing in which all P_b center precursors are hydrogen passivated. (b) After oxide stressing which created large numbers of E' centers in the oxide. Note that the post-stressing illustration (b) is thermodynamically unstable.

thermodynamically unstable (i.e. completely hydrogen passivated P_b centers in the vicinity of completely unpassivated E' centers is thermodynamically unstable). Lenahan argues that the Gibbs free energy of the system:

$$G = H - TS, \tag{1.3}$$

where H is enthalpy (sum of energy plus pressure times volume), T is absolute temperature, and S is entropy, would be lowered if some hydrogen from the passivated P_b centers transfers to some of the unpassivated E' centers in the oxide [31, 32]. This hydrogen transfer would cost little energetically and thus little enthalpy since the two bond energies are roughly equal [31, 32].

However, the hydrogen transfer would greatly increase the entropy of the system; since the entropy of the system is defined as

$$S = k \ln(\Omega), \tag{1.4}$$

where k is Boltzmann's constant and Ω is the number of microscopic configurations responsible for the macroscopic system, the configurational entropy would increase from $k \ln(1)$ for the case of figure 1.3b to $k \ln(M)$, a large increase, if one hydrogen was transferred from any of the M hydrogen passivated P_b center sites to an unpassivated E' center site [31, 32]. The removal of a second hydrogen would lead to a configurational entropy of $k \ln[(M)(M-1)/2]$ and so on for additional removal of hydrogen. Additionally, the configurational entropy due to the unpassivated E' centers would increase from $k \ln(1)$ to $k \ln(N)$, a large increase, if one hydrogen were added to any of the N unpassivated E' center sites [31, 32]. This is schematically illustrated in figure 1.4.

Thus, the simple statistical thermodynamics arguments of Lenahan indicate that the transfer of hydrogen from passivated interface states to unpassivated oxide defects is

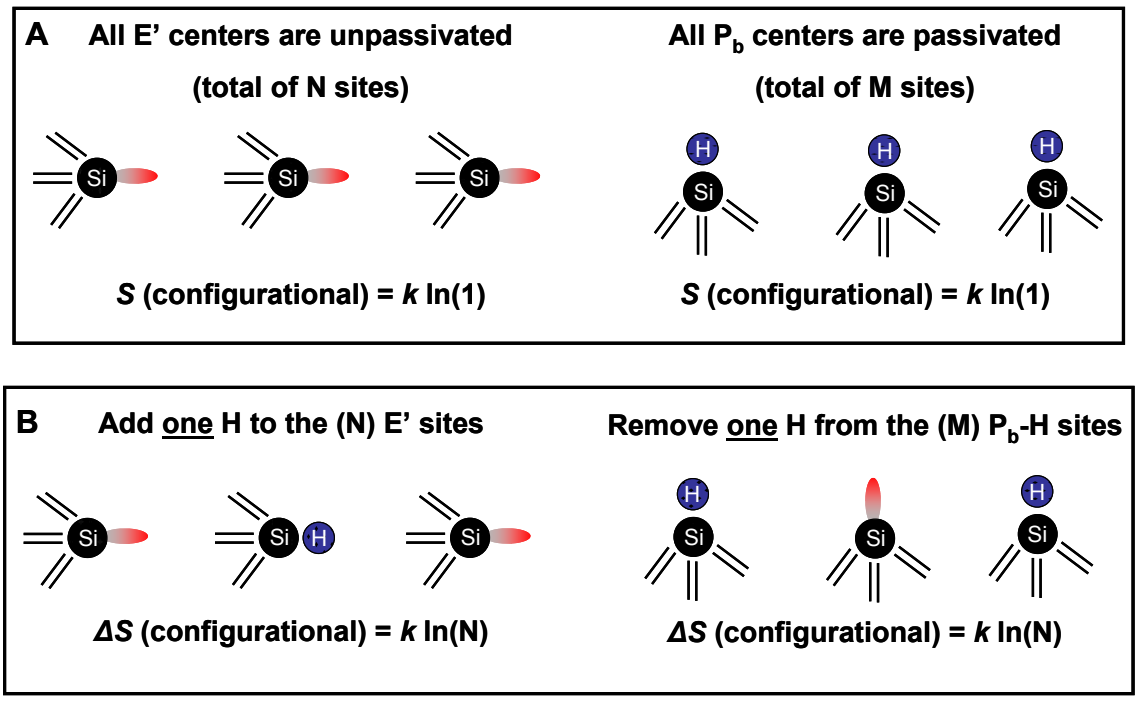

Figure 1.4: (a) A schematic illustration of an oxide with N unpassivated E' center sites and M hydrogen passivated P_b center sites. In both cases, the configurational entropy, S, is given by k ln(1). (b) A schematic illustration of the effect of transferring one hydrogen from a passivated P_b center site to an unpassivated E' center site. In both cases, there is a large increase in the configurational entropy.

thermodynamically favored and provides a very plausible explanation for the triggering mechanisms of NBTI.

Quite recently, Grasser *et al.* [36] have developed a comprehensive quantitative two-stage model for NBTI in pure SiO_2 devices based on the ideas expressed by Campbell *et al.* [29, 30] and Lenahan [31, 32] in which NBTI is triggered by inversion layer hole capture at an E' center precursor site (a neutral oxygen vacancy). In the model proposed by Grasser *et al*., the NBTI degradation process is initiated (stage one) when inversion layer hole capture occurs at E' precursor sites (neutral oxygen vacancy) [36]. The hole capture leads to positively charged E' centers (paramagnetic defects observable with ESR) in the oxide, similar to the schematic drawing provided in figure 1.3b. In stage one, the system is in a recoverable state where the positively charged E' center can very quickly emit a hole leading to full recovery back to the precursor state. Grasser *et al*. argue that this recoverable charge trapping state is responsible for NBTI recovery in which much of the damage very quickly heals once the NBTI stress is removed [36]. However, if the NBTI stress is maintained, the system can also proceed to stage two of the model (permanent degradation). Following the arguments of Lenahan [31, 32] discussed above, Grasser *et al.* note that the large number of unpassivated E' centers in the vicinity of hydrogen passivated P_b interface states in stage one is thermodynamically unstable. The oxide silicon dangling bonds (E' centers) created in the stage one process triggers the creation of P_b centers through the P_b/E' hydrogen exchange process discussed above [36]. This leads to a poorly recoverable P_b interface state and the transferred hydrogen essentially "locks in" the positive charge on the E' center site (rendering it diamagnetic and unobservable with ESR). The positively charged E' center and the

newly created P_b interface state is consistent with much of the NBTI literature [10, 16, 17] suggesting the degradation is due to interface state generation and oxide charge build up, the magnetic resonance observations of Campbell *et al*. [20, 29, 30] and Fujieda *et al*. [19] who indicate that NBTI is dominated by interface state generation, and the somewhat tenuous arguments of Campbell *et al*. [20, 29, 30] who suggest that E' centers play an important role in NBTI degradation.

The comprehensive quantitative model of Grasser *et al.* [36] explains NBTI degradation over a wide range of bias voltage and stress temperature, the observed asymmetry between stress and recovery, and the strong sensitivity to bias and temperature during recovery. Perhaps more importantly, the model attributes recovery to charge trapping/detrapping, a tunneling mechanism, which accurately predicts the very fast experimentally observed recovery phenomena [21-24]. Since the reaction-diffusion model relies on diffusion of hydrogenic species (a much slower process than tunneling) to account for recovery, it predicts a much slower recovery which is incompatible with experimental observations [21-24]. Additionally, the model predicts that paramagnetic E' centers will be present during stress and will very quickly recover upon removal of stress [36]. However, prior to this work the existence and role of these E' centers had not yet been conclusively demonstrated.

As mentioned previously, Campbell *et al.* were only able to report somewhat tenuous E' experimental observations in NBTI stressed devices [29, 30]. This is so for two reasons. First, and most importantly, the EDMR technique of spin dependent recombination (SDR) used [37, 38] does not permit observations at significant negative bias; the stress biasing conditions must be altered so that electron and hole quasi Fermi

levels are split more or less symmetrically about the intrinsic Fermi level at the Si/SiO_2 interface. Secondly, SDR is only marginally adequate for E' center detection because only those E' centers very close to the interface can contribute to SDR. Conventional ESR does permit E' center detection at any gate bias if the center is positively charged. Chapter 4 discusses this in more detail where we utilize our newly developed on-the-fly ESR technique to perform ESR measurements during NBTI stressing of MOS structures. The newly developed technique permits a recovery free glimpse into the dynamics of NBTI and our results provide insight into the E'/P_b center NBTI triggering mechanisms discussed above.

An additional source of NBTI confusion is that NBTI is enhanced when nitrogen is incorporated in the SiO_2 gate dielectric [39]. Although the reasons for the nitrogen enhancement of NBTI phenomenon is not yet fully understood, recent progress has been made in identifying the atomic-scale defects involved in nitrogen enhanced NBTI. Campbell *et al.* [40] utilized EDMR measurements to study NBTI in plasma nitrided SiO_2 devices. Although the range of processing explored was very limited (one set of plasma nitrided SiO_2 devices), the study of Campbell *et al.* [40] demonstrates that, at least in some samples, the dominating NBTI defects in plasma nitrided devices are fundamentally different than those of conventional pure SiO_2 (P_b centers). They provide evidence that the dominating NBTI defect in their plasma nitrided devices is the K center and is physically located in the near interface region (close, but not precisely at, the Si/dielectric interface) [40]. K centers are silicon dangling bond defects in which the central silicon is back-bonded to nitrogen atoms. K centers dominate charge trapping in pure Si_3N_4 films. A schematic drawing of a K center is provided in figure 1.5.

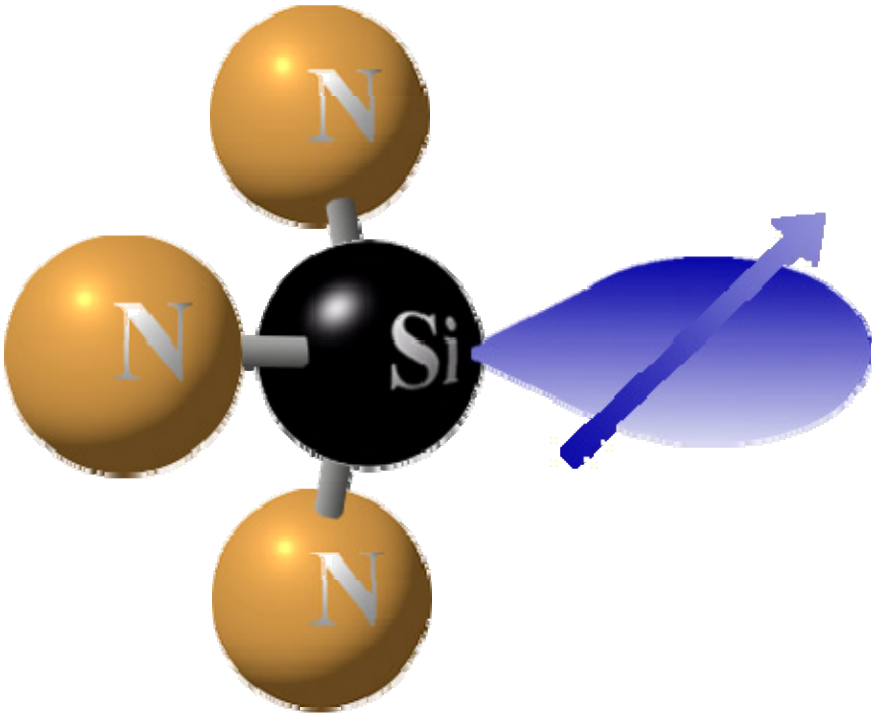

Figure 1.5: Schematic drawing of the K center which dominates charge trapping in pure Si_3N_4 and some nitrided SiO_2 dielectrics. The K center is a silicon dangling bond defect in which the central silicon atom is back-bonded to nitrogen atoms.

Campbell *et al.* [40] speculate that since K centers can be hydrogen passivated [41], the reaction-diffusion model involving hydrogen liberation from a defect site is the likely mechanism for the NBTI response they observe. (The results of this dissertation provide an alternative explanation.) Campbell *et al.* [40] also note that variation in plasma nitridation profiles in the gate stack may lead to the conflicting reports of NBTI generated interface and/or bulk traps. Depending on the nitridation profile, K center precursors could be present very near the interface, or further away in the bulk of the oxide. Following NBTS, the K centers very near the interface would behave as interface states while the ones further into the bulk would behave more as bulk traps. However, in the very thin oxides (2.3nm EOT) Campbell *et al.* [40] studied, the line between purely interface and purely bulk trapping centers is blurred. In chapter 3, we utilize a newly developed technique called energy-resolved spin dependent tunneling (ER-SDT) to directly determine the density of states (DOS) of these K center defects in ultra-thin plasma nitrided oxide devices.

Another interesting aspect of NBTI is the role that fluorine plays in reducing the severity of NBTI degradation. Several studies have shown that when fluorine is incorporated into thicker SiO_2 devices, the NBTI degradation is reduced [42, 43]. The most likely explanation for this observation is that silicon-fluorine bonds are stronger than silicon-hydrogen bonds [44-46]. If interface defects are passivated with fluorine instead of hydrogen, during an NBTS the stronger silicon-fluorine bonds are not broken as easily as silicon-hydrogen bonds. However, studies have shown that fluorine incorporation in nitrided SiO_2 devices has little or no effect on the NBTI response [47]. Campbell *et al.* suggest that fluorine still replaces hydrogen at the interface, but since the

dominating NBTI defects in nitrided SiO_2 are likely near interface K centers, the fluorine does not passivate the K center precursors resulting in little or no change in the NBTI response [48]. Chapter 5 discusses fluorine's role in more detail where SDR measurements are utilized to identify the atomic-scale role that fluorine plays in NBTI.

Although progress has recently been made in identifying the atomic-scale defects responsible for NBTI in conventional SiO_2 and nitrided SiO_2 based devices [20, 29, 40], very little is known about the NBTI/PBTI defects and mechanisms in HfO_2 based devices. As previously mentioned, unlike conventional SiO_2 based devices [10], PBTI is also a problem in HfO_2 based devices [13, 14]. Several studies involving purely "electrical" measurements have observed NBTI and PBTI in HfO_2 based MOSFETs [13, 14, 49, 50]. These studies suggest that the roles of interface and bulk charge trapping in HfO_2 NBTI are similar to those observed for NBTI in SiO_2 based devices. However, some controversy remains regarding the origins of PBTI in these devices. PBTI degradation is thought to be due to defects formed in the interfacial layer region during stress or a combination of interfacial layer defect formation and pre-existing defect charge trapping in the interfacial layer and/or the bulk HfO_2 [11, 14, 51-54]. The nature of defects in HfO_2 is discussed in section 1.3 of this chapter. Cochrane *et al.* [55] were the first to apply the EDMR technique of SDR to study the physical nature of atomic-scale defects involved in NBTI in HfO_2 based MOSFETs. They found that the NBTI generated defects in HfO_2 MOSFETs are different than those observed in SiO_2 devices. Cochrane *et al.* [55] suggest that near interface E' like centers are the dominating NBTI induced defects opposed to purely interface and bulk trapping centers. As previously mentioned, this may be the source of controversy [10, 16, 17] regarding the roles of

interface and bulk trapping centers as near interface traps (sometimes called switching traps or border traps) can have characteristics of both interface and bulk trapping centers. Chapter 6 discusses the role of these interfacial layer defects in greater detail where we utilize conventional ESR and SDR measurements to identify the physical and electrical nature of these defects.

1.2 Stress Induced Leakage Currents

Stress induced leakage current (SILC) is a device degradation phenomenon occurring as a result of excess gate oxide electric field [4, 56-59]. SILC is manifested as a continuous increase in gate leakage current and eventual oxide breakdown (an electrical short through the gate oxide) during the application of high oxide electric fields [4, 56-59]. Aggressive gate oxide scaling has exacerbated SILC in recent years and poses a serious concern for future gate oxide scaling [4, 56-59]. Additionally, SILC poses a major limitation to MOSFET power efficiency since excess gate leakage currents are essentially wasted energy. SILC is also a major concern with regard to non-volatile floating gate memory data retention times, as stored information (charge stored on a floating gate) can leak off the floating gate and be lost [60, 61].

SILC is believed to arise from an oxide wear out process in which defect centers are generated in the oxide and/or interface as a result of the electric field stress [4, 56-59]. The increased concentration of defect centers leads to an increase in gate leakage current due to trap assisted tunneling. For thicker oxides (greater than about 3.5nm) SILC related trap assisted tunneling is thought to be an inelastic tunneling process [62, 63] which proceeds through neutral electron traps in the oxide (likely oxygen vacancies otherwise

known as E' centers in SiO_2 dielectrics [58, 64-68]) [69, 70]. However, when the gate oxide thickness is scaled down below about 3.5nm, SILC related trap assisted tunneling is thought to be an elastic (or low loss inelastic) process which proceeds through an interface trap to interface trap tunneling mechanism [71-73]. This process is usually referred to as low-voltage SILC (LV-SILC) because the SILC current is usually only observed at low sense (gate) voltages within a volt or two of flat band conditions [71, 72]. Additionally, Nicollian *et al*. suggest that LV-SILC is only observed when the energy states of the interface defects are within the same range of electrostatic potential, supporting the idea that LV-SILC is due to interface trap to interface trap tunneling [71, 72].

Figure 1.6 schematically illustrates the basic idea of SILC for a "thick" dielectric (figure 1.6a) and a "thin" dielectric (figure 1.6b). When a constant voltage stress is applied to an MOS gate stack, defect centers are continuously generated in the oxide. Again, these defects are very likely E' centers for the case of SiO_2 stacks [58, 64-68]. When enough of these defects are generated, a leakage path can form between the gate contact and the substrate in which electrons can tunnel from one defect to another through the oxide. When the gate oxide is scaled down below about 3.5nm (figure 1.6b), the same situation occurs, but in this case, the electron does not need to make multiple "jumps" to work its way through the oxide. In the LV-SILC interface trap to interface trap model proposed by Nicollian *et al.* [71, 72], interface defects are created during stress, and an electron can tunnel from an interface defect near the gate contact directly to an interface defect at the Si/SiO_2 interface. Since the Si/SiO_2 interface states can respond

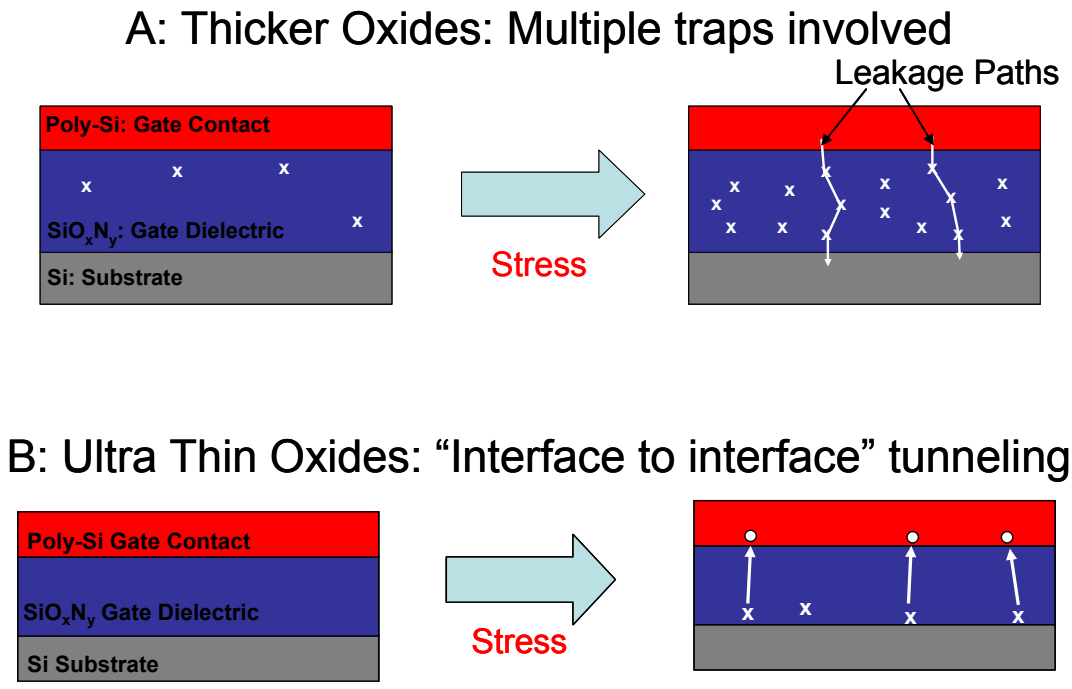

Figure 1.6: Schematic illustration of SILC in "thick" (a) and "thin" (b) dielectrics.

electrically to the substrate Fermi level position, LV-SILC can be turned on and off by modulating the gate bias.

As mentioned previously, ESR studies strongly suggest that neutral electron traps, probably E' centers, are the defects likely responsible for SILC in thicker SiO_2 oxides [74-76]. In thinner SiO_2 oxides, P_b centers located directly at the Si/SiO_2 interface are likely generated during stress, and in addition to defects already within the highly defective poly-silicon gate contact are the defects likely responsible for LV-SILC. Chapter 3 discusses the mechanisms of LV-SILC in greater detail.

1.3 The Nature of Defects in Hafnium Based Dielectrics

Si/dielectric interface traps are one of the most important defects that reduce the performance of MOSFET devices. Si/dielectric interface traps are in direct contact with the MOSFET channel and can reduce the channel conductance and the overall performance of the device [77]. One of the primary reasons conventional Si/SiO_2 has proved to be so successful is the excellent quality of the Si/SiO_2 interface [5]. Through proper processing, it is quite possible to achieve interface state densities of 10^{10} $cm^{-2}eV^{-1}$ or less [77]. As mentioned previously, early studies of high-k based MOS devices focused mainly on reducing the interface state density. Interface states were, until fairly recently, of the upmost importance because it was not uncommon to have unacceptably high interface state densities (10^{11}-10^{12} $cm^{-2}eV^{-1}$) [78-84].

Early ESR studies performed a few years ago by several independent groups on Si/HfO_2 structures identified the dominating Si/dielectric interface states as silicon dangling bond centers identical to or very similar to the Si/SiO_2 P_b center family of

defects [80, 85-89]. The P_b center family of defects dominate interface trapping in conventional Si/SiO_2 devices [35]. All P_b centers are high p-character silicon dangling bond defects located precisely at the Si/dielectric boundary [35]. In all cases, the central silicon atom is back-bonded to three other silicon atoms [35].

Kang *et al.* were the first to identify interface states in (111) Si/HfO_2 structures using ESR [86]. By measuring the defect spectra g tensor, Kang *et al.* observed that the dominating interface states in (111) Si/HfO_2 are silicon dangling bond centers located precisely at the Si/dielectric interface which are almost, but not quite identical to, the P_b centers commonly observed in (111) Si/SiO_2 [90-92]. Kang *et al*. noted that the components of the g tensor, $g_{\parallel}$ and $g_{\perp}$, were shifted to a value slightly above that of the Si/SiO_2 P_b [86]. Stesmans *et al.* extended the studies of Kang *et al.* to include the more technologically relevant (100) Si/HfO_2 system [80]. They observed Si/dielectric interface states which were essentially identical to the P_{b0} and P_{b1} centers commonly found in (100) Si/SiO_2. Later, Pribicko *et al.* observed P_{b0} and P_{b1} like centers in fully processed metal gate (100) Si/HfO_2 MOSFETs using SDR [89]. Recent work by Triplett *et al.* more closely examined interface states in (100) Si/HfO_2 and found that, as Kang *et al*. had observed earlier, the g tensor components for their observed interface defect spectra are almost identical (though $g_{\perp}$ is slightly higher) to those of conventional Si/SiO_2 P_b centers [93].

As high-k dielectric research has progressed, researchers have devised processing techniques to reduce the density of interface states in Si/HfO_2 devices to acceptable densities. Of particular importance is the HfO_2 deposition technique, preparation of the silicon substrate (interfacial layers), and post-deposition anneals. Unlike SiO_2 which can

be thermally grown, HfO_2 must be deposited. Early in HfO_2 research, a wide variety of deposition techniques were explored including physical vapor deposition [79, 82, 84, 94-96], chemical vapor deposition [80, 93, 97, 98], and atomic layer deposition (ALD) [78-81, 86, 99-103]. Today, ALD is arguably the preferred method for depositing ultra-thin layers of HfO_2 on silicon [3, 104]. ALD allows for atomic layer control of the HfO_2 layer which results in an extremely uniform and high quality HfO_2 film. Typically, the silicon substrate is prepared by growing a very thin (of order 1nm) SiO_2 interfacial layer prior to ALD deposition [3, 104]. The SiO_2 interfacial layer is used to improve the nucleation of HfO_2 during ALD deposition as well as to improve the electrical properties of the Si/dielectric interface [3, 104-106]. The SiO_2 interfacial layer is not necessarily good for the development of Si/HfO_2 MOSFETs and will be discussed in further detail. Post-deposition treatments of the gate stack have been shown to improve the quality of the interface as well. Post-deposition forming gas (hydrogen/nitrogen) [80, 86, 94, 107], nitrogen [101] and ammonia [97] anneals have been shown to be quite effective at reducing the interface state density to reasonable levels.

Ideally, it would be preferable to have an Si/HfO_2 interface void of any interfacial layers (for example, HfO_2 deposited on hydrogen terminated silicon) [5, 108]. This would yield the maximum gate stack capacitance possible for the high-k dielectric. Studies have suggested that despite the most stringent preparation techniques, a thin layer of native SiO_2 will grow between the silicon and the HfO_2 which can result in a very poor quality interface [5]. Some researchers have suggested that it is nearly impossible to achieve a Si/HfO_2 interface without some native oxide growth of SiO_2 occurring after any extended period of time [5]. Robertson suggests that this is not due to a thermodynamic

instability, but rather oxygen diffusion through the HfO_2 and subsequent oxidation of the silicon during post-deposition annealing [5].

Accepting the presence of a SiO_2 interfacial layer has proved to be the best way to overcome its limitations; if the interfacial layer is unavoidable, it should be created intentionally. By intentionally creating the SiO_2 interfacial layer, it can be made of the highest possible quality opposed to the generally poor quality of the native SiO_2 growth. Since the Si/HfO_2 interface is of subpar quality, having the high quality SiO_2 interfacial layer eliminates the problems associated with oxidation of the silicon substrate through oxygen diffusion [5] and poor HfO_2 ALD nucleation on bare silicon [105]. It also makes the actual Si/dielectric interface a Si/SiO_2 interface, whose properties are arguably the primary reason for the success of the microelectronics industry.

Despite this seemingly easy "quick fix", the SiO_2 interfacial layer has its drawbacks. First, and perhaps the most obvious drawback, is that even a very thin SiO_2 interfacial layer will add to the gate oxide thickness and quickly use up the allocated EOT for a particular device design. Thus, it is imperative to control the SiO_2 interfacial layer thickness very carefully. Secondly, the interfacial layer introduces a "new" type of defect which was not previously of concern in conventional Si/SiO_2. Several studies have suggested that when HfO_2 is deposited on a thin SiO_2 interfacial layer, the HfO_2 will leach oxygen from the interfacial layer to an extent highly dependent on processing [88, 99, 109]. Using a variety of analytical and electrical measurements, Bersuker *et al.* [88] argue that this process renders the SiO_2 interfacial layer oxygen deficient (sub-stoichiometric) with a large density of oxygen vacancies present in the SiO_2 interfacial layer which is consistent with other recent literature. Scopel *et al.* [110] calculated that it

is energetically favorable to form oxygen vacancy defects in the SiO_2 by compensation than in the HfO_2. Wang *et al.* [111] argue that oxygen deficient HfO_2 absorbs oxygen from the SiO_2 interfacial layer creating the oxygen vacancies in the SiO_2. Bersuker *et al.* [99] demonstrated that high temperature processing generates electrically-active defects in the interfacial layer of HfO_2 MOSFETs, consistent with oxygen vacancy formation. Young *et al.* [112, 113] and Heh *et al.* [114, 115] have also shown that in addition to bulk trapping, near interface traps are important reliability limiting defects as well.

ESR measurements by Triplett *et al.* [93], Stesmans *et al.* [116], and Ryan *et al.* [109] all support the suggestions of oxygen deficient silicon centers (E' centers) in the interfacial layer. The authors of these studies [93, 109, 116] have suggested that these defects sites are similar to E' centers which are commonly observed in stressed SiO_2 [35, 117-121]. As mentioned previously, Cochrane *et al.* [55] utilized SDR to observe NBTI induced defects in HfO_2 MOSFETs. They suggest a dominating role of NBTI generated near interface E' like centers in HfO_2 MOSFETs. Cochrane *et al.* [55] also suggest a weak coupling of an E' like site and a nearby hafnium atom which is consistent with work by Van Benthem *et al.* [122] who observed individual hafnium atoms in the interfacial layer of HfO_2 structures. As mentioned previously, chapter 6 discusses these interfacial layer defects in greater detail.

It's worthwhile to note that the dielectric constant of the interfacial layer SiO_2 is sometimes observed to be much higher than expected [83, 88, 99, 100, 112, 114]. Studies have suggested that the higher than expected dielectric constant is due to the high density of oxygen vacancies in the interfacial layer [88, 99, 114]. Bersuker *et al.* [88] suggest that the density of oxygen deficient silicon sites can be as high as 10^{19} cm^{-3} in the

interfacial layer, resulting in a sub-stoichiometric SiO_x interfacial layer. These observations are supported by first principle simulations of Giustino and Pasquarello [123] who reported that the dielectric constant of the sub-stoichiometric SiO_x interfacial layer can be as high as 6 or 7. Although helpful in achieving a high quality interface, the inclusion of a SiO_2 interfacial layer presents "new" defects which are of importance to reliability issues.

Unlike conventional Si/SiO_2, several studies have suggested a dominating role for bulk charge traps in the HfO_2 of Si/HfO_2 devices [14, 94, 124-126]. HfO_2 is much more susceptible to intrinsic pre-existing traps than its SiO_2 counterpart [127, 128]. Lucovsky [127] attributes this to the higher ionic bonding character and higher atomic coordination number for the oxide which makes it a poor glass former (hard to keep amorphous during processing). Robertson [128] also suggests that this makes for an oxide which is not able to relax and "repair" defects easily. Studies of the electrical properties of HfO_2 films support this idea. For example, Zafar *et al.* [14, 125] reported threshold voltage shifts in HfO_2 nMOSFETs and attributed the shift to trapping of charge at pre-existing defect sites, likely in the bulk of the HfO_2. Gusev *et al.* [126] also reported that at low stress voltages, charge trapping occurred at pre-existing defect sites in HfO_2 MOSFETs. In conventional Si/SiO_2, bulk charge trapping is usually only of concern after the device has been stressed in some way. Typically, in SiO_2 based MOSFETs, the associated defects are of the E' center family of defects.

Limited ESR studies have experimentally studied bulk charge traps in HfO_2 MOS structures [129, 130]. It should be noted that the observation of these defects has proved to be quite difficult with ESR and a complete picture is yet to be had. Using a corona ion

method which allowed for the flooding of the dielectric with electrons or holes, Kang *et al.* [129] were the first to observe oxygen vacancies and oxygen interstitials in ALD HfO_2 on silicon. Paramagnetic centers quite similar to the oxygen interstitial have been widely studied in many materials including bulk samples of ZrO_2 [131-142]. Kang *et al.* [129] noted that the observed g tensor values for the HfO_2 spectra were very similar to those reported for oxygen interstitials in bulk samples of ZrO_2 [135-138]. Kang *et al.* [129] suggest that since hafnium and zirconium are very similar chemically, the close correspondence in g tensor values provides further evidence that their spectra is due to an HfO_2 oxygen interstitial. Signals quite similar to the likely HfO_2 oxygen vacancy observed by Kang *et al.* [129] have been reported in bulk ZrO_2 [135-138, 142] and recently in bulk HfO_2 systems [142, 143] as well. Again, the authors argue that the similarities in hafnium and zirconium suggest that the observed defects are due to an oxygen vacancy in HfO_2. Additionally, recent theoretical calculations of g tensor values for oxygen vacancies in HfO_2 by Ramo *et al.* [144] are in fairly close agreement with the reported experimental values of Kang *et al.* [129] and further support their argument that the observed signal is due to an oxygen vacancy. The observation of the oxygen vacancy and the oxygen interstitial being the dominating intrinsic HfO_2 bulk charge traps are further supported by several theoretical studies which have suggested that the primary intrinsic bulk defects in HfO_2 (and the very similar ZrO_2) are the oxygen interstitial and oxygen vacancy [145, 146]. Using a variety of modeling techniques and assumptions, the atomic-scale structure and electronic properties of these defect sites has been calculated by Foster *et al.* [145, 146], Xiong *et al.* [147, 148], and Kralik *et al.* [149].

Chapter 2

EXPERIMENTAL METHODS

2.1 Electron Spin Resonance

ESR is an analytical technique which utilizes unpaired electrons to provide chemical and physical information about a paramagnetic center [150, 151]. Thus, it is especially well suited, and is undoubtedly the most powerful tool available, for studying the structure of trapping centers in MOS structures.

An electron is a charged particle with intrinsic angular momentum; qualitatively it can be thought of as a spinning negative charge which has an associated magnetic moment [150]. When a sample with unpaired electrons is placed in a large magnetic field, the electron's magnetic moment can either precess about or precess against the magnetic field. Although this model is not exactly correct, it can qualitatively be thought of as the electron's magnetic moment lining up parallel (precessing about) or anti-parallel (precessing against) to the applied magnetic field. The orientation of the electrons (parallel or anti-parallel) correspond to two energy levels known as the Zeeman levels [150]. The energy difference between the Zeeman levels increases linearly with increasing magnetic field strength as shown in figure 2.1.

In ESR, a microwave frequency alternating magnetic field is also applied to the sample. When the energy of the microwave frequency alternating field equals the energy difference between the Zeeman levels (ΔE), resonance occurs. During resonance, transitions between the Zeeman levels can occur which can be qualitatively thought of as an electron "flipping" its spin vector along with its associated spin magnetic moment.

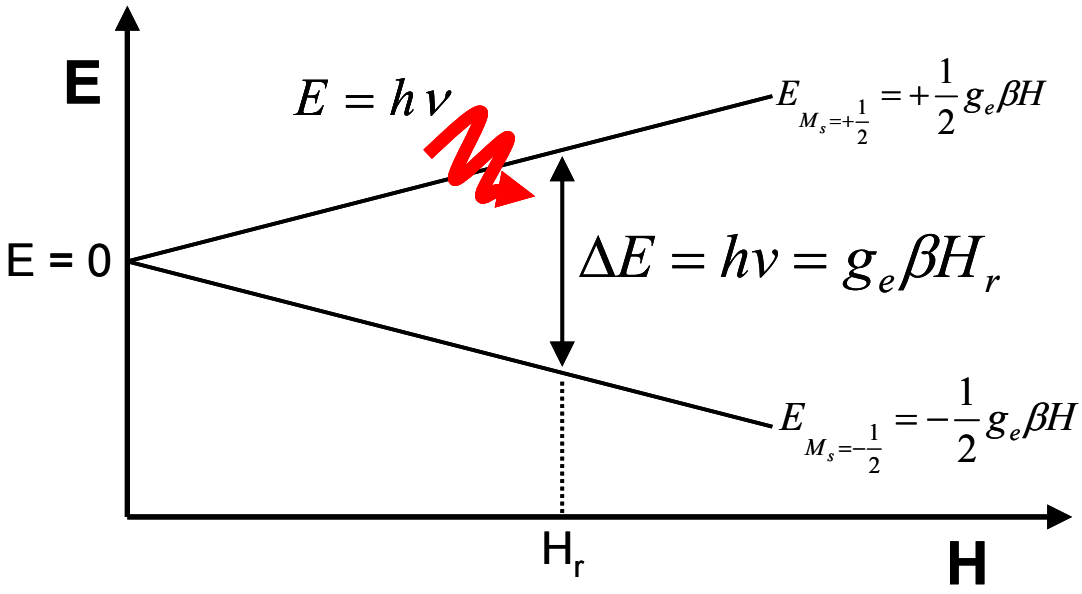

Figure 2.1: Illustration of the Zeeman energy levels for the simplest case of free electrons.

Resonance is detected by recording the reflected microwave power which monitors the net change in energy from the electron's spin "flipping".

For the simplest case, a free electron, the ESR resonance condition is defined as:

$$h\nu = g_e \beta H \quad , \tag{2.1}$$

where h is Planck's constant, ν is the frequency of the second oscillating magnetic field, g_e is the free electron g value (≈ 2.002319) , β is the Bohr magneton, and H is the external magnetic field at resonance. Typically, the external magnetic field strength is around 3400 which corresponds to an oscillating magnetic field frequency in the X-band microwave regime (~9.5 GHz). Deviations from equation (2.1) due to spin-orbit coupling and electron-nuclear hyperfine interactions often lead to considerably more complex resonance conditions than the simple case described in equation (2.1) and therefore provide much more useful structural information about a paramagnetic center and its surroundings.

The first interaction which alters the resonance condition of equation (2.1) is called spin-orbit coupling. Spin-orbit coupling is due to a moving electron interacting with the electric field produced by a nuclear charge [151]. The Bohr model provides a qualitative (and only qualitative) explanation of spin-orbit coupling [35]. It describes an electron traveling around the nucleus in a circular orbit, much as the Earth orbits the Sun. If an observer were to stand on the electron, it would appear that the nucleus was in a circular orbit around the electron (the same argument is true for the Earth/Sun system). Figure 2.2 schematically illustrates this argument. In this model, the nucleus generates a small magnetic field which is proportional to the orbital angular momentum of the

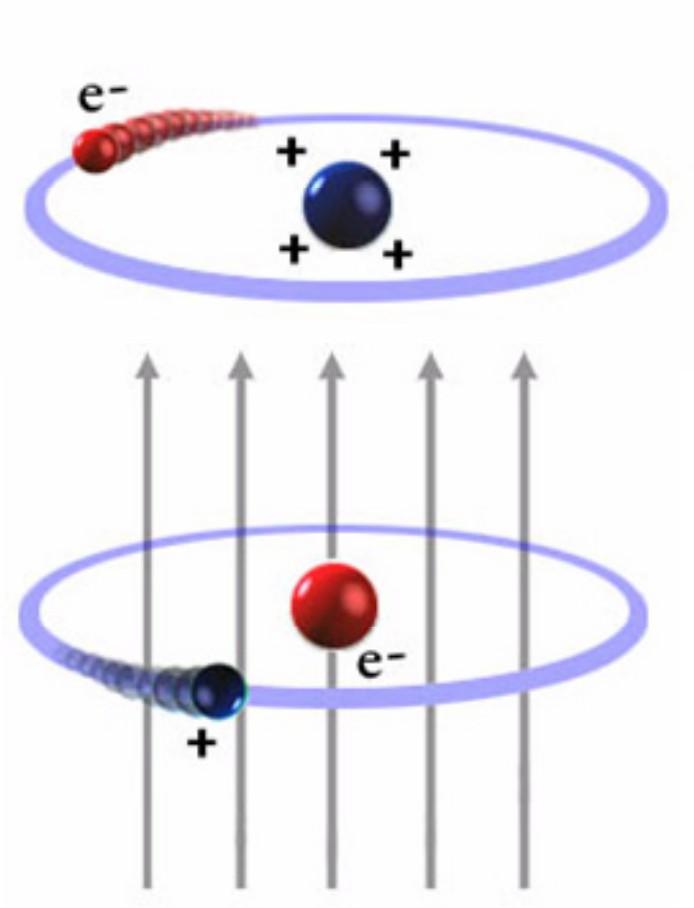

Figure 2.2: Schematic illustration of the spin-orbit coupling effect. From the electron's reference frame, the nucleus appears to orbit around the electron.

electron [35]. The greater the nuclear charge and orbital angular momentum quantum number, the greater the spin-orbit coupling.

Spin-orbit coupling is included in the resonance condition by replacing the free electron g (g_e) with a matrix usually taken to be the second rank tensor g_{ij}. Simply put, the g depends upon the defect's structure and orientation with respect to the applied magnetic field. Information about a defect's structure is determined from the g tensor; it is essentially a defect "fingerprint" [35].

The symmetry of the tensor implies symmetry in the paramagnetic center. Second order perturbation theory allows for a first order calculation of the g tensor components for simple defects encountered in this study [35, 150, 151]:

$$g_{ij} = g_e \delta_{ij} + 2\lambda \sum_k \frac{\langle db | L_i | k \rangle \langle k | L_j | db \rangle}{(E_k - E_{db})}, \qquad (2.2)$$

where g_e is the free electron g value, δ_{ij} is the Kronecker delta function, λ is the spin-orbit coupling constant, L_i and L_j are angular momentum operators with respect to the i and j directions of the center's axis system, db corresponds to the dangling bond ground state, k corresponds to excited states, and E_k and E_{db} are the energies associated with the excited states and ground state of the paramagnetic center.

The second interaction which alters the simple resonance condition of equation (2.1) is the electron-nuclear hyperfine interaction. Electron-nuclear hyperfine interactions arise from the interaction of unpaired electrons with nearby nuclei possessing a magnetic moment [35]. Some nuclei relevant to MOS technology that possess magnetic moments are ^{29}Si (spin ½), ^{1}H (spin ½), ^{19}F (spin ½) and ^{14}N (spin 1).

Equation (2.3) is a modified version of equation (2.1) that includes the electron-nuclear hyperfine interaction:

$$h\nu = g\beta H + M_I A\,, \tag{2.3}$$

where M_I is the nuclear spin quantum number and A is the hyperfine tensor. For an axially symmetric paramagnetic center with a specific orientation of its symmetry axis with respect to the magnetic field (given by the angle θ), g and A are defined as [35]:

$$g = \left(g_{II}^2 \cos^2\theta + g_{\perp}^2 \sin^2\theta\right)^{1/2}, \tag{2.4}$$

$$A = \left(A_{II}^2 \cos^2\theta + A_{\perp}^2 \sin^2\theta\right)^{1/2}. \tag{2.5}$$

Equations (2.3-2.5) provide an easy means to evaluate g and hyperfine tensors for axially symmetric defects in a crystalline environment. (Many defects of interest have this symmetry.) To visualize the orientation dependence of certain centers, consider simple silicon dangling bond defects located precisely at the interface of Si/SiO_2. Since the silicon substrate is crystalline in nature, the dangling bonds point in specific crystallographic directions. The ESR pattern therefore changes as one rotates the sample with respect to the applied magnetic field. For a dangling bond defect in the bulk of SiO_2, all defect orientations are equally likely, since SiO_2 is amorphous in nature. Thus, simple rotation mapping of a defect's g value can sometimes provide vital information about the defect's location in a structure comprised of crystalline and non-crystalline materials.

For conventional ESR, which has a sensitivity of order 10^{10} total defects, sample requirements dictate large area (~1cm^2) blanket capacitor structures with very limited conductive material present (for example, no metal contacts). Thus, conventional ESR is

not especially well suited for studying fully processed devices. However, ESR has the advantage of being able to probe defects in the entire gate stack (including interface, near interface, and bulk traps) [35]. It is also possible to perform fairly accurate "spin counting" in ESR through the use of a spin standard which allows one to count the number of defects in a given sample. Without any gate contact, it is still possible to apply oxide bias to an ESR sample utilizing the corona ion "gateless" biasing technique [152]. This allows for a "virtual" gate in which the desired oxide bias can be achieved (a Kelvin probe can be utilized to monitor the gate voltage).

2.2 Spin Dependent Recombination

Magnetic resonance studies of device instabilities would ideally be carried out on fully processed devices. Conventional ESR, with a sensitivity of about 10^{10} total spins, is not nearly sensitive enough for studies of fully processed devices. Fortunately, the EDMR technique of SDR (which is at least 10^7 times more sensitive than conventional ESR) allows for ESR measurements in fully processed devices while circumventing the conventional ESR sample requirements and sensitivity limitations [37, 38, 153].

SDR utilizes the principles of ESR as well as the Shockley-Read-Hall (SRH) model for recombination [154, 155] and the Pauli exclusion principle. In the SRH model, a conduction electron is captured by a deep level defect. Then, the defect site captures a hole; the electron and hole recombine and the process can repeat indefinitely (hole capture can occur first). The Pauli exclusion principle states that two electrons cannot occupy the same orbital if their spin quantum numbers are equal.

In SDR, a fully processed MOSFET is configured as a gate controlled diode to ensure that the substrate current is dominated by recombination through interface states [156]. The MOSFET is then placed in a large magnetic field and, as with the case of conventional ESR, unpaired electrons residing on deep level defects tend to align parallel or anti-parallel to the applied magnetic field. If a deep level defect and a conduction electron have the same spin quantum number, recombination cannot occur because it is forbidden by the Pauli exclusion principle. When the ESR resonance condition, equation (2.3), is satisfied, the deep level defect's electrons are "flipped" which increases the probability of a conduction electron and deep level defect having opposite spin quantum numbers. Thus, the probability of a recombination event occurring is increased which in turn increases the recombination (substrate) current. This is schematically illustrated in figure 2.3. In SDR, resonance is detected by monitoring the change in the recombination (substrate) current and the resonance condition of SDR is the same as conventional ESR as described by equation (2.3). Again, information about the defect's structure and chemistry is gained from the g tensor.

As mentioned previously, the key advantage of using SDR is that one is able to perform ESR measurements on fully processed devices. Thus, the samples utilized in SDR are much more technologically relevant than the large area samples of ESR. With SDR, one can obtain valuable ESR information and easily relate them to actual device parameter shifts. However, SDR can only probe defects a short way (~1nm) into the gate stack which limits the technique to studying interface and near interface defects. Direct spin counting is not possible with SDR, so the direct current gate controlled diode recombination current vs. voltage (DC-IV) measurement (discussed in section 2.4) is

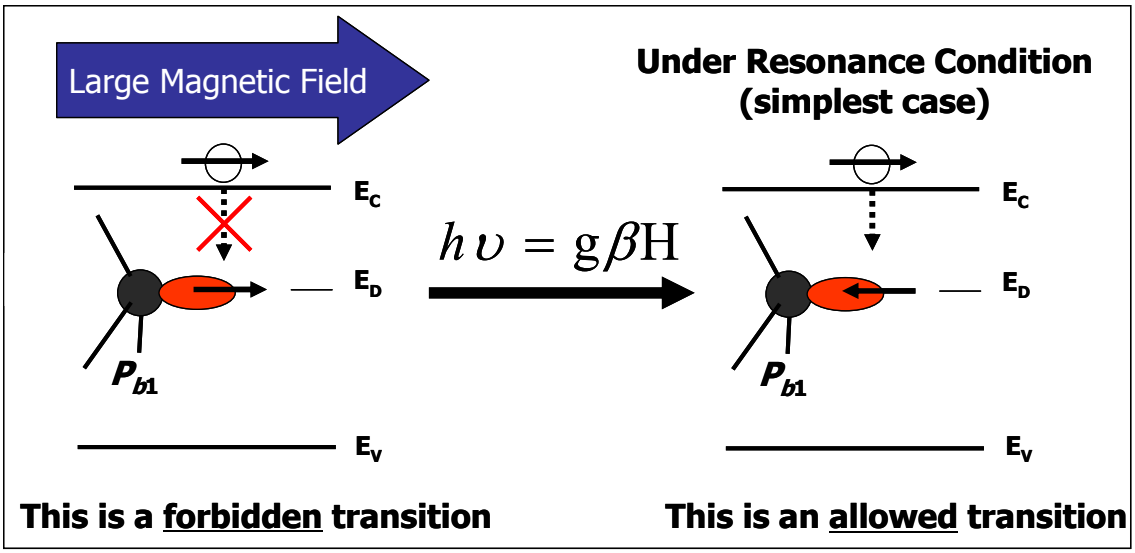

Figure 2.3: Schematic illustration of the basic idea behind SDR. The device recombination (substrate) current is modified due to an ESR induced spin-flipping.

usually performed in parallel to SDR for monitoring the interface state density. Additionally, SDR is severely limited by excess gate leakage currents when the oxide thickness is reduced to below about 2nm.

Figure 2.4 illustrates a simple schematic diagram of a typical SDR spectrometer. A MOSFET is mounted on a special adapter such that its electrical contacts can be accessed while being placed in a microwave resonant cavity. This allows for the MOSFET to be configured as a gate controlled diode and enables the monitoring of the substrate current. The cavity is situated in a large magnetic field. Helmholtz coils are mounted on the cavity which applies a small AC magnetic field to the sample and allows for a phase/frequency detection scheme to be utilized. The substrate current is fed into a preamplifier and a lock-in amplifier. The lock-in output is recorded as the large magnetic field is swept through resonance.

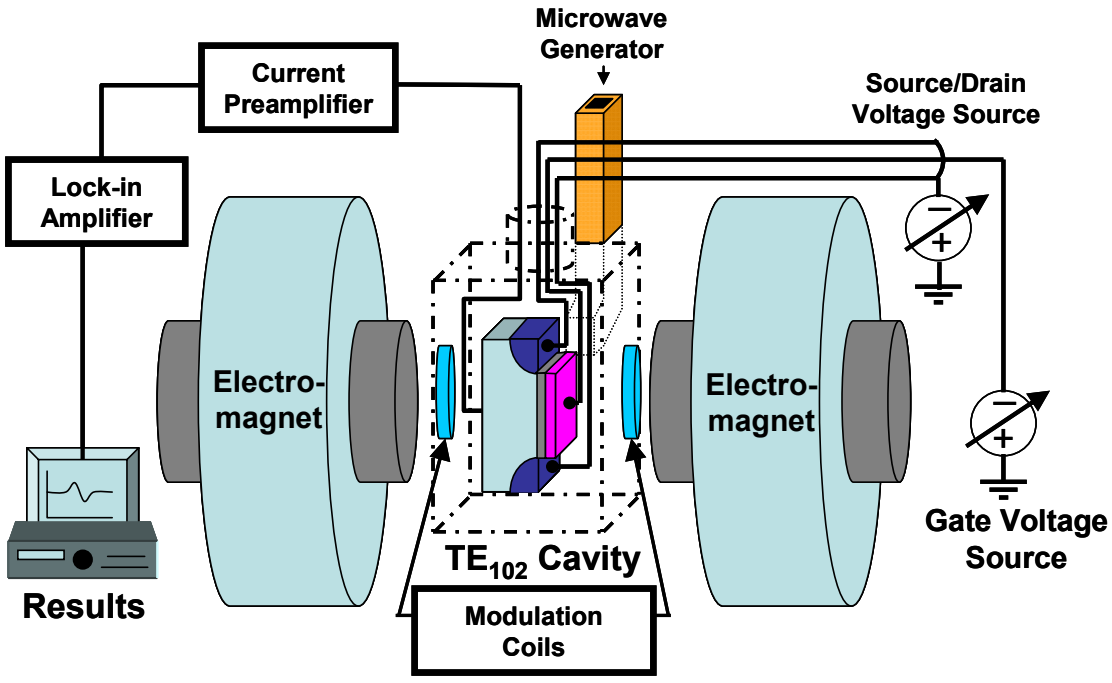

Figure 2.4: Schematic illustration of an SDR spectrometer.

2.3 Spin Dependent Tunneling

The principles of spin dependent tunneling (SDT) are very similar to those of SDR, except that in SDT, one monitors a spin dependent tunneling current. In the simplest model for trap assisted tunneling, an electron can tunnel from one defect to another and eventually work its way through the gate oxide. Similar to the case of SDR, when one applies a large magnetic field to the system, unpaired electrons in the sample tend to line up parallel or anti-parallel to the applied magnetic field. If the tunneling electron and the oxide defect have the same spin quantum number, the tunneling event is forbidden. When the ESR resonance condition is satisfied, the oxide defect flips its spin orientation, and the tunneling event becomes allowed. This process is schematically illustrated in figure 2.5. In SDT, resonance is detected by monitoring the gate tunneling current as a function of magnetic field. Again, the resonance condition is described by equation (2.3) and information about the tunneling defect's structure is determined from the g tensor. Very few studies have reported on SDT to date and have involved only very coarse qualitative information about energy levels [157], quite low signal-to-noise ratios [158], and, in one case, a difficult to deconvolute mixture of SDT and SDR [48]. This work demonstrates a simple, much improved approach to SDT called energy-resolved SDT (ER-SDT), which allows one to directly link the analytical power of magnetic resonance to defect energy levels [159]. The simplicity of the technique and the robust character of the response make it, at least potentially, of widespread utility in the understanding of defects important in solid state electronics. This improved approach to SDT is discussed in detail in chapter 3.

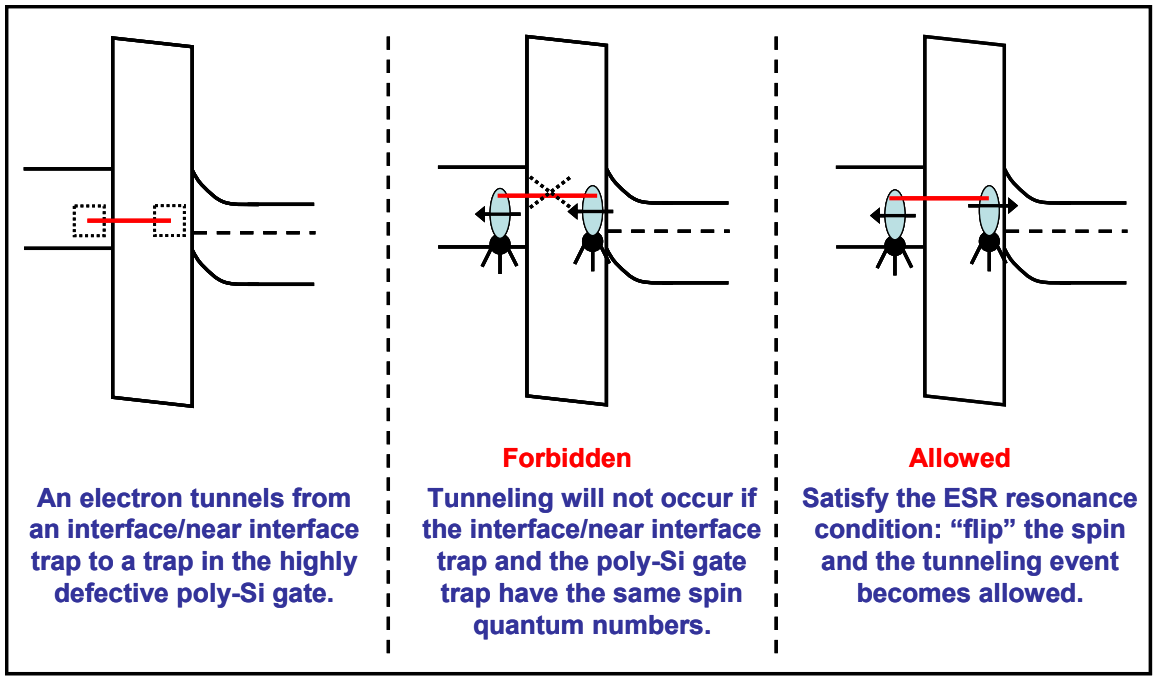

Figure 2.5: Schematic illustration of the basic principles behind SDT. The trap assisted tunneling current associated with gate leakage current is modified due to an ESR induced spin-flipping.

2.4 Gate Controlled Diode

One of the most important device parameters to track in MOS reliability problems is the interface state density (D_{it}). The DC-IV method is a quick and reliable way to track the interface state density in MOSFETs [156, 160]. In the DC-IV measurement, a MOSFET is configured as a gate controlled diode; a small forward bias (V_F) is applied to the shorted source/drain contacts and the source/drain to substrate current (I_{sub}) is monitored as a function of gate bias [156, 160]. As the gate bias is swept, the source/drain to substrate current displays a characteristic peak.

Fitzgerald and Grove [156] showed that the peak in substrate current corresponds to a peak in recombination current through interface states. They also showed that the change in current from base line amplitude to the peak amplitude (ΔI_{sub}) is proportional to the interface state density which is described by:

$$\Delta I_{sub} = \frac{1}{2} q n_i \sigma_s v_{th} D_{it} A q |V_F| \exp\left(\frac{q|V_F|}{2kT}\right), \tag{2.6}$$

where q is electronic charge, n_i is the intrinsic carrier density, σ_s is the geometric mean of the electron and hole capture cross section of the defect, v_{th} is the thermal velocity, A is the gate area of the MOSFET, k is Boltzmann's constant, and T is the absolute temperature. Note that an important limitation of the DC-IV method is that the change in substrate current is proportional to the geometric mean capture cross section of the defect. One would have to assume a geometric mean capture cross section when dealing with a yet to be determined defect center.

Chapter 3

DETERMINATION OF K CENTER DENSITY OF STATES VIA ENERGY-RESOLVED SPIN DEPENDENT TUNNELING SPECTROSCOPY

In this chapter, we report on a very simple and much improved approach to SDT which we call energy-resolved SDT (ER-SDT) which exploits advantages provided by extremely thin dielectrics. Our observations introduce a simple method to link point defect structure and energy levels in a very direct way in materials of great technological importance. The enormous difference between the very high capacitance of the thin dielectric and the much lower capacitance of the silicon depletion layer allows a modest applied voltage to sweep through most of the silicon band gap with very little net potential drop across the dielectric. The approach yields direct information about defect energy levels and provides magnetic resonance spectra with excellent sensitivity.

The dielectrics chosen for the study are plasma nitrided SiO_2 films which are quite widely utilized in essentially state-of-the-art ICs. Deep level defects were generated within these films by subjecting them to high electric fields. The defect generating conditions were chosen because they represent the circumstances under which an important instability in present day ICs occurs: LV-SILC. Our ER-SDT results strongly suggest that LV-SILC is dominated by K center defects in ultra-thin (1.2nm EOT) nitrided SiO_2 MOS devices. Using ER-SDT, we extract information about the electronic levels of the K centers. Since the K center is thought to dominate NBTI in nitrided oxide devices [20, 40, 48], these observations are also important with respect to nitrided oxide NBTI degradation.

3.1 Experimental Details

ER-SDT measurements were carried out at room temperature utilizing a custom-built spectrometer consisting of a Resonance Instruments 8330 series X-band microwave bridge with a TE_{102} microwave cavity and a four-inch electromagnet controlled by a very stable magnetic field controller. The magnetic field was calibrated with conventional ESR measurements using a strong pitch spin standard. The ER-SDT samples utilized are 1.2nm EOT plasma nitrided SiO_2 p-type MOS capacitors with p^+ poly-silicon gates. The very high p^+ doping of the gate effectively pins the gate Fermi energy very close to the gate silicon valence band edge. The gate areas were $\approx 10^4 \mu m^2$. Deep level defects were generated in the dielectrics by room temperature stressing of 2.2V for 10^4 seconds. Gate tunneling current vs. gate voltage (I_G-V_G) measurements were made before and after stress to monitor the change induced by trap assisted tunneling.

3.2 Results and Discussion

Figure 3.1 illustrates I_G-V_G measurements in a device before and after it was subjected to a high electric field stress. At first glance, the pre- and post-stress curves are virtually identical. Figure 3.2 illustrates $\Delta J/J_0$ vs. V_G for the capacitor from the measured I_G-V_G curves of figure 3.1. Here, J_0 is the gate current density pre-stress and ΔJ is the gate current density post-stress (J_t) minus J_0. The $\Delta J/J_0$ vs. V_G plot illustrates the difference between the I_G-V_G curves before and after stress due to a trap assisted tunneling current in the post-stress I_G-V_G measurement of figure 3.1 [71]. The peak of this curve (V_G = 0.35V) corresponds to the maximum fractional contribution of trap assisted tunneling current, not the maximum trap assisted tunneling current, as direct

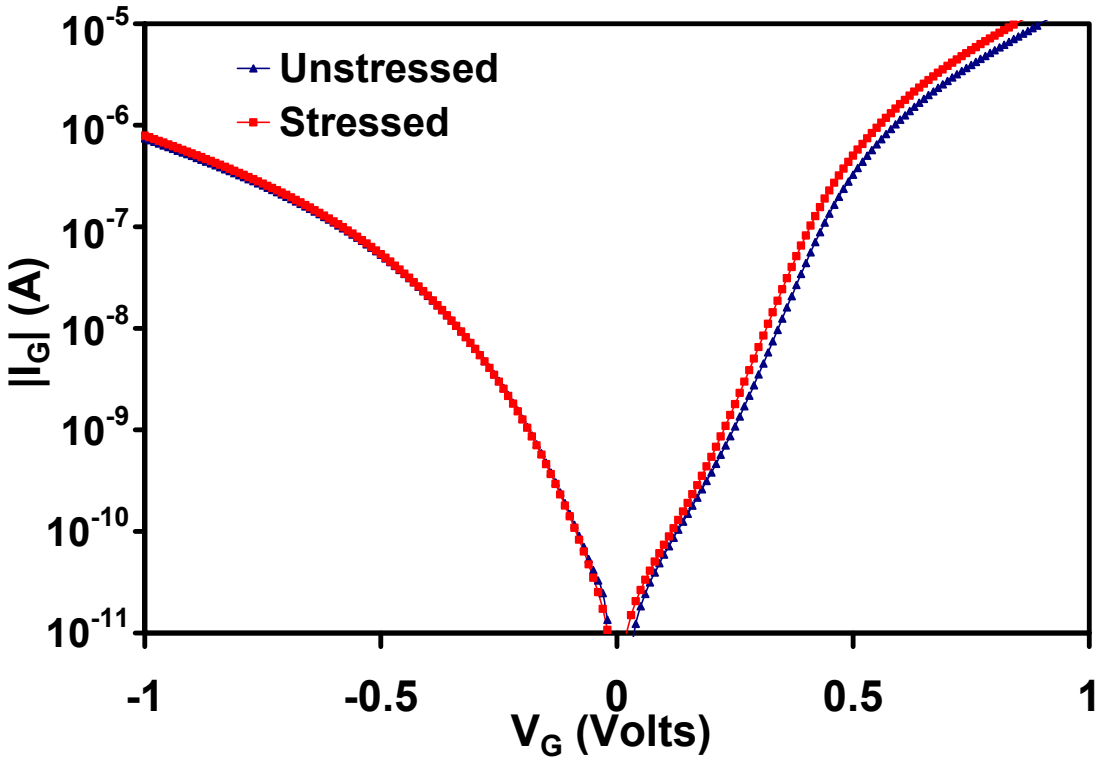

Figure 3.1: I_G-V_G curves before and after high electric field stressing.

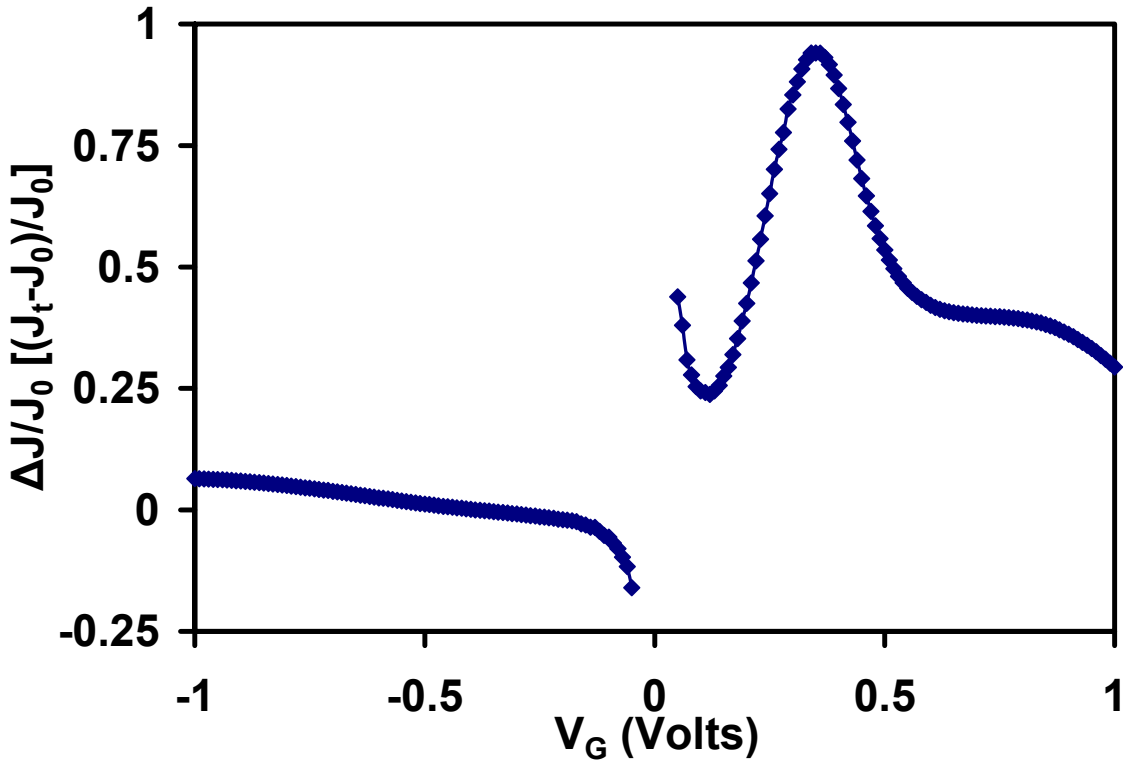

Figure 3.2: $\Delta J/J_0$ vs. V_G where J_0 is the gate current density pre-stress and ΔJ is the gate current density post-stress (J_t) minus J_0. The peak in the curve is caused by a trap assisted tunneling current in the stressed I_G-V_G measurement of figure 3.1.

tunneling is increasing exponentially with voltage. At higher voltages the current is dominated by direct band to band tunneling which overwhelms the trap assisted tunneling current. Values for $\Delta J/J_0$ around $V_G = 0V$ are not included because the amplitude of the currents are below the detection limit of the I_G-V_G measurements.

Figure 3.3 illustrates a representative ER-SDT measurement taken with V_G biased to correspond to the peak in the $\Delta J/J_0$ curve in figure 3.2 ($V_G = 0.35V$). In this figure, the measurement was made with the Si/dielectric interface normal parallel to the applied magnetic field (0°). The spectrum is a single line with a g of 2.0030 ± 0.0002 and a line width of about 15G.

Figure 3.4 illustrates the ER-SDT spectrum with the sample rotated 90 degrees from the measurement of figure 3.3. In this measurement, the Si/dielectric interface normal is perpendicular to the applied magnetic field (90°). The fact that the spectrum does not change when the sample is rotated strongly suggests that the defects are located in an amorphous material. If the defects existed at specific orientations, as they would in a crystalline environment or were precisely at the Si/dielectric interface, the g value would almost certainly change as the sample is rotated in the magnetic field. For example, the g values of the dominating interface defects in conventional Si/SiO_2, P_b centers, change considerably as the sample is rotated in the magnetic field [35]. The defects observed in this study do not follow such a pattern, ruling out a direct role for Si/dielectric P_b centers in the spin dependent trap assisted tunneling process. The magnetic field orientation independence, the zero crossing g value of 2.0030, and the 15G line width of the observed defect spectrum are all consistent with the K center found in Si_3N_4 and some SiO_xN_y films [48, 161, 162]. When the K center is paramagnetic, a

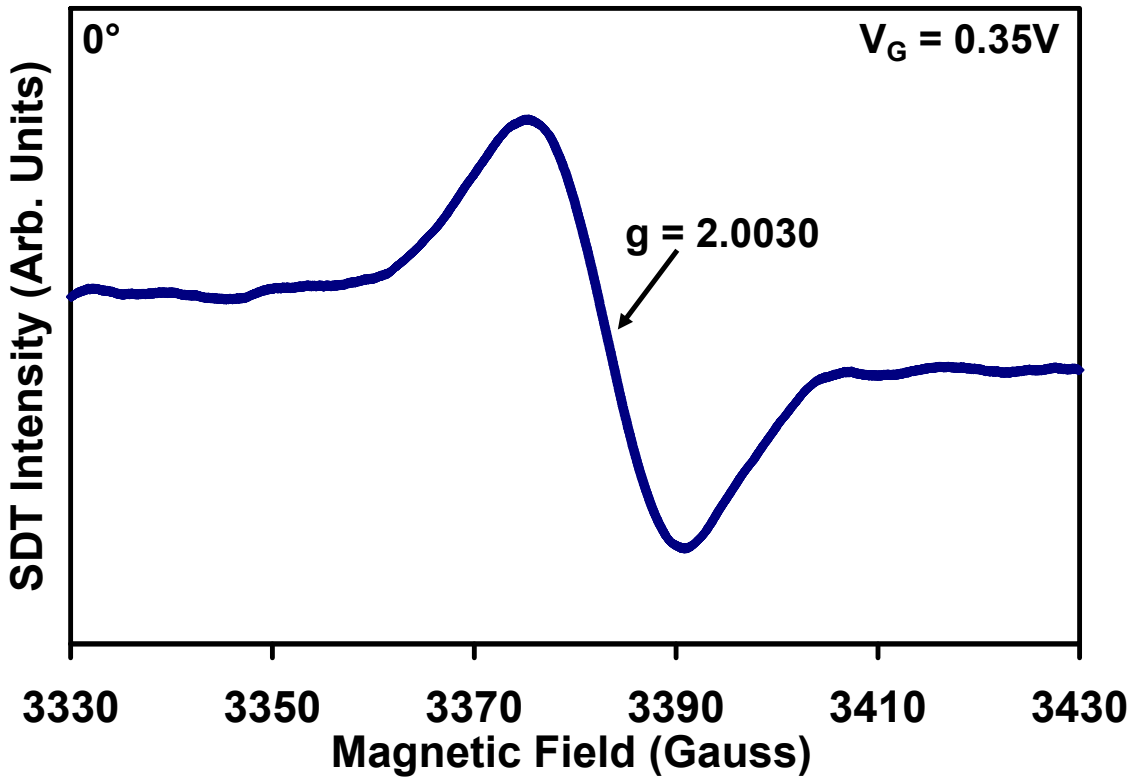

Figure 3.3: Representative ER-SDT measurement taken with V_G biased to correspond to the peak in the $\Delta J/J_0$ curve of figure 3.2 (V_G = 0.35V). The measurement was taken with the magnetic field parallel to the Si/dielectric interface normal. The zero crossing g = 2.0030 ± 0.0002.

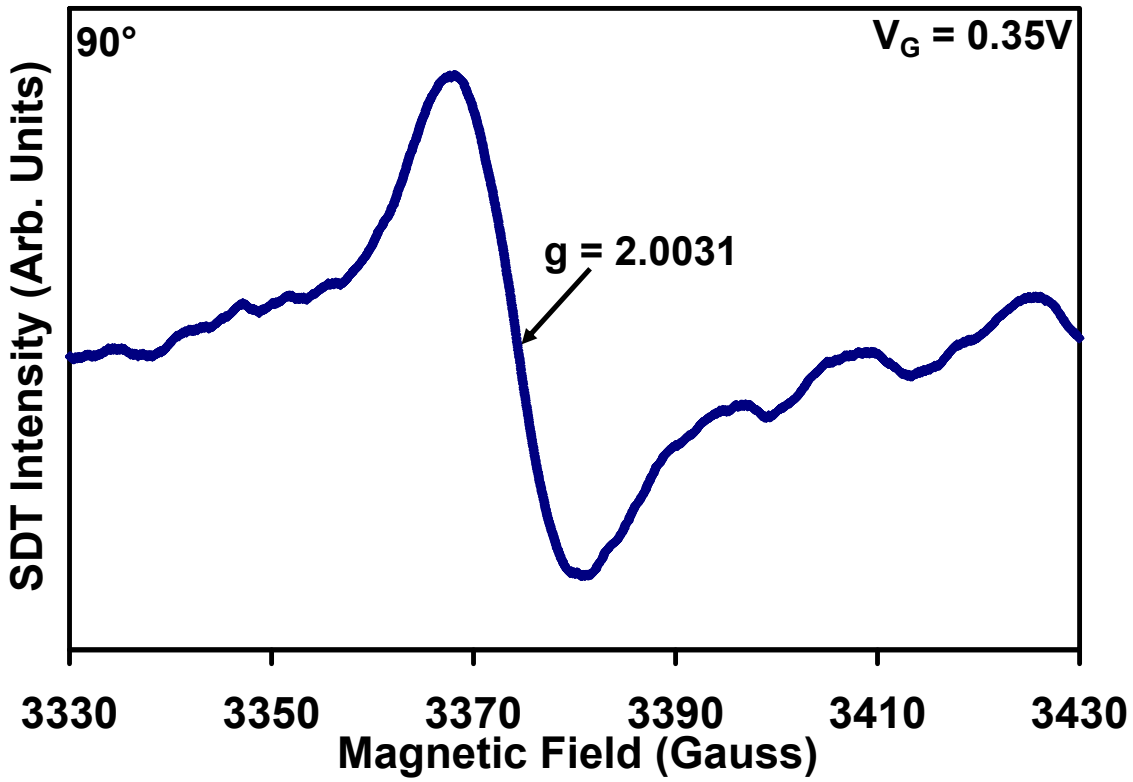

Figure 3.4: In this trace, the sample is rotated in the magnetic field so that the Si/dielectric interface normal is perpendicular to the magnetic field. Note that the spectrum zero crossing g does not change, within experimental error, from the g with the interface normal parallel to the magnetic field as shown in figure 3.3.

single electron occupies a high p-character wave function in a silicon atom back-bonded to three nitrogen atoms [162, 163]. The K center is responsible for trapping in conventional Si_3N_4 films [161].

Figure 3.5 illustrates a comparison between the normalized ER-SDT intensities as a function of V_G (a) and the $\Delta J/J_0$ vs. V_G (b) plot of figure 3.2. The normalization of figure 3.5a is achieved by dividing the spin dependent modification to the tunneling current (ΔI_{SDT}) by the total DC current (I). The $\Delta I_{SDT}/I$ response very closely follows the characteristic trap assisted tunneling peak of figure 3.5b, a very strong indication that we are observing spin dependent trap assisted tunneling current due to the defects largely responsible for the tunneling current.

In an attempt to delineate between the spin dependent trap assisted tunneling current and the direct tunneling current, figure 3.6 shows the spin dependent modification to the tunneling current (ΔI_{SDT}) as a function of V_G. It peaks at about 0.5V, indicating that, as one would expect, the peak at $V_G = 0.35V$ in $\Delta I_{SDT}/I$ (figure 3.5a) is shifted downward because direct tunneling overwhelms the trap assisted tunneling process at higher bias. Since the direct tunneling is not spin dependent, the ER-SDT response is not affected by the large direct tunneling current response which overwhelms the "electrically" measured trap assisted tunneling current at higher bias.

Figure 3.7 illustrates the poly-Si/SiO_xN_y/crystalline-Si band diagram for the device at three quite different biasing conditions: $V_G = 0$, 0.55, and 1.0V. For simplicity of presentation, only two levels of a single dielectric trap are included in diagrams. (These band diagrams were calculated using the Boise State band diagram program [164].) Note first that there is very little band bending in the dielectric at any of the

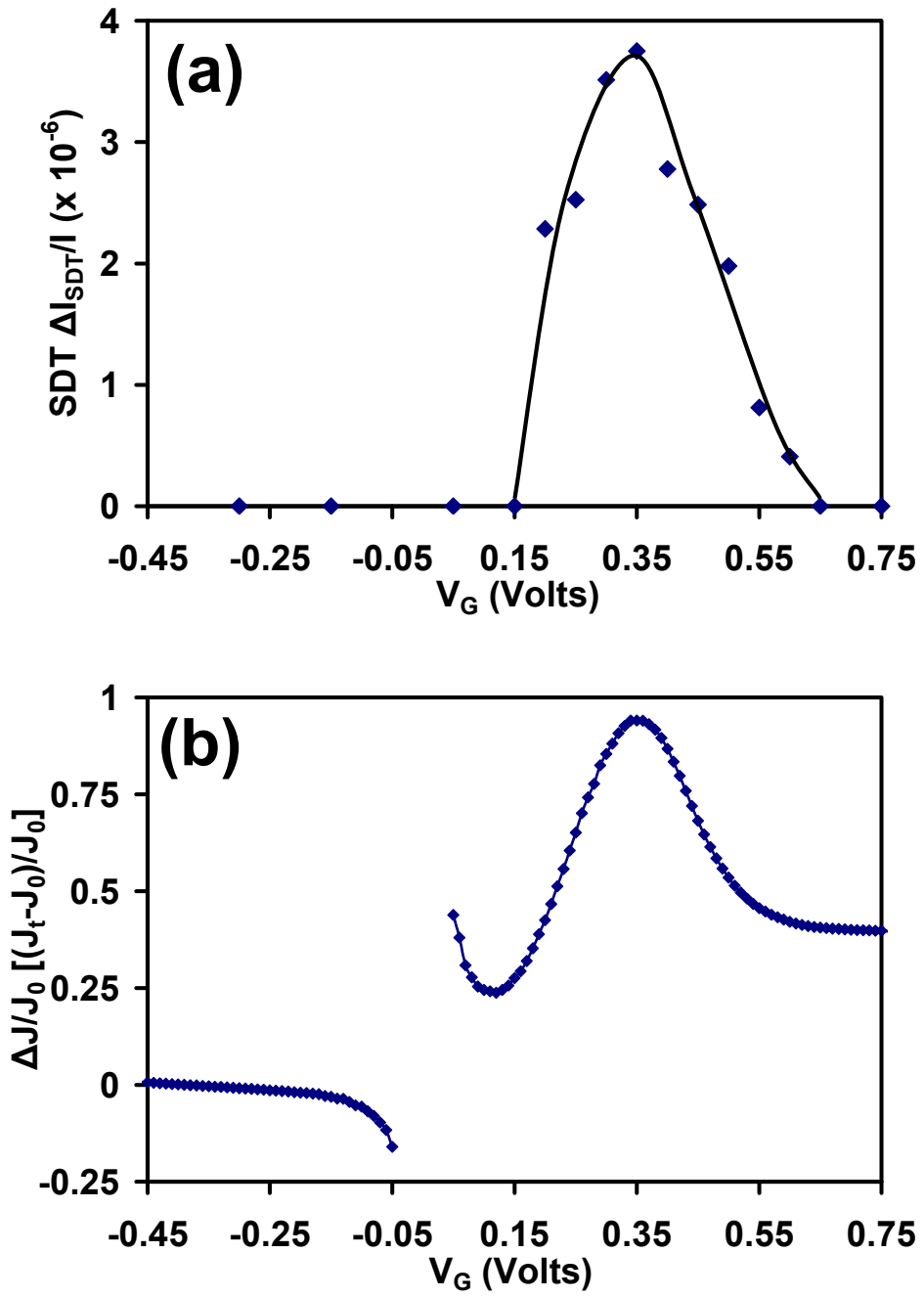

Figure 3.5: Comparison between the normalized ER-SDT intensities as a function of V_G (a) and the $\Delta J/J_0$ vs. V_G (b) plot of figure 3.2. The normalization of figure 3.5a is achieved by dividing the spin dependent modification to the tunneling current (ΔI_{SDT}) by the total DC current (I). The ER-SDT response ($\Delta I_{SDT}/I$) very closely follows the characteristic trap assisted tunneling peak of (b).

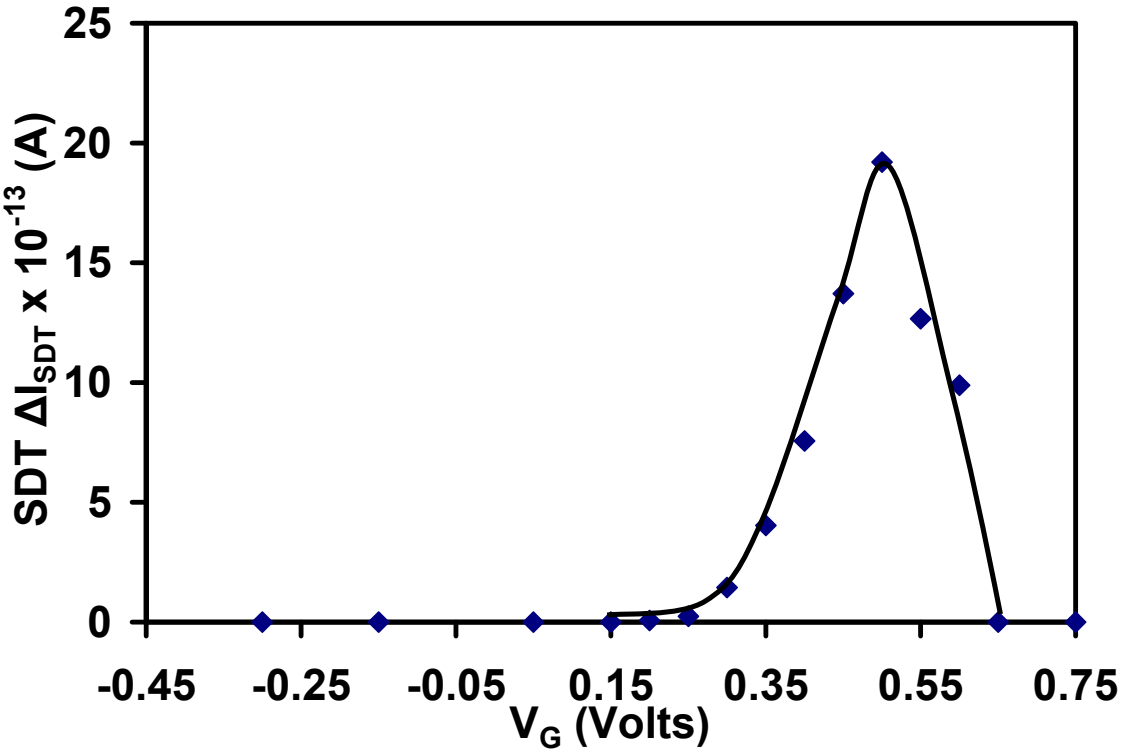

Figure 3.6: ER-SDT spin dependent modification to the tunneling current (ΔI_{SDT}) as a function of V_G. Note that it peaks at about $V_G = 0.5V$ indicating the peak at $V_G = 0.35V$ in the ER-SDT $\Delta I_{SDT}/I$ of figure 3.5a is shifted downward because direct tunneling overwhelms the trap assisted tunneling process at higher voltages.

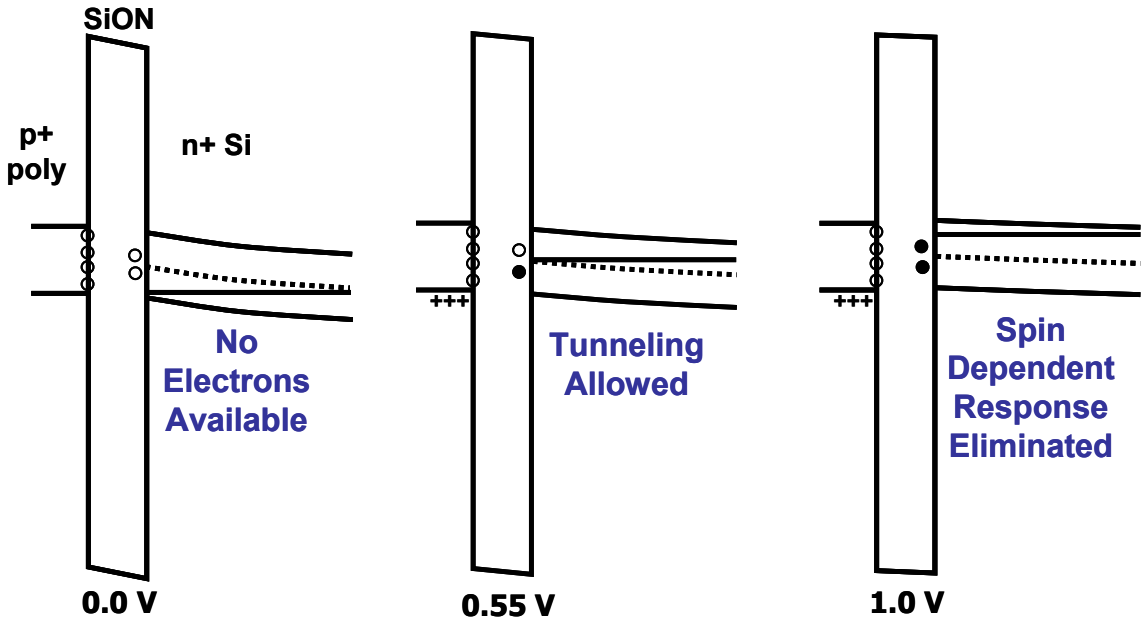

Figure 3.7: Energy band diagrams for the sample at three different values of gate bias. Note that the only plausible explanation for the tunneling current must involve electron tunneling through defects with levels corresponding to the range of the silicon band gap. The simplified sketch illustrates two dielectric defect levels, consistent with the experimental result.

illustrated biasing levels. The dielectric is so thin that the relationship between the crystalline-Si/dielectric Fermi level and the defect energy level is nearly independent of the physical position of the defect with respect to the crystalline-Si/dielectric interface. This is so because of the enormous difference between the capacitance of the 1.2nm EOT dielectric and the much thicker silicon depletion region. Nearly all the voltage appears across the silicon. Figure 3.6 shows that the ER-SDT response appears at a V_G of about 0.2V, peaks at 0.5V, and has completely disappeared at about 0.65V. At $V_G = 0.2V$, where ER-SDT appears, the crystalline-Si/dielectric Fermi level is 0.26eV above the silicon valence band edge. At $V_G = 0.65V$, where the ER-SDT disappears, the Fermi level is about 0.68eV above the silicon valence band edge. This narrow response must reflect a narrow distribution in K center levels.

An explanation of the response can be gleaned from a brief consideration of the physics of spin. The ER-SDT process, like all EDMR processes, must involve a pair of spins initially separated physically. One of the spin sites is a K center. K centers, especially those nearest the crystalline-Si/dielectric boundary, can act like interface traps in that, as the Fermi level is advanced from the valence band edge toward the conduction band edge, the empty dangling bond trap levels (+/0) will accept an electron as the Fermi level crosses the relevant energy. This process is not spin dependent whether or not it involves paramagnetism at the K center site because it does not involve paramagnetism from the valence band. However, once the K center is rendered paramagnetic, interactions of the K center site with another paramagnetic site would be spin dependent and thus susceptible to ER-SDT. Should the K center accept an additional electron, it would be rendered diamagnetic again, insensitive to the ER-SDT process.

Consider tunneling of an electron from a paramagnetic K center site to another paramagnetic site in the (highly defective) poly-silicon gate. The process would be allowed only if the unpaired electron spins have opposite spin quantum numbers. If the two sites had electron spins with the same spin quantum number, the tunneling process would be forbidden (Pauli exclusion principle). However, if the K center electron spin were to be "flipped" via ESR, the previously forbidden tunneling event would be allowed. Thus, magnetic resonance could modulate such a tunneling process. The ER-SDT process would thus "turn on" when the Fermi level crosses the energy level corresponding to the first K center electron (+/0) transition which places one electron in the defect's dangling bond orbital. Figure 3.8a, a replotting of the results of figure 3.6 in which V_G is replaced by the position of the Fermi level, indicates that the ER-SDT response begins to appear with the Fermi level at about 0.26eV above the valence band edge. The process peaks with the Fermi level at about 0.54eV. Very crudely speaking, the energy range of 0.26eV to 0.54eV would correspond to the range of energy over which the K centers accept the first electron (+/0 transition). The ER-SDT response drops from 0.54eV to below our detection limit at 0.68eV. So, to a rough approximation, the energy range of 0.54eV to 0.68eV corresponds to the range of energy over which the K centers accept the second electron (0/- transition).

To a very crude approximation, we could approximate the collective K center DOS by the absolute value of the derivative $d\Delta I_{SDT}/dE_F$. This is illustrated in figure 3.8b. The cartoons of figure 3.8c illustrate the spin states (and charge) of the K centers. We can understand how this is so by first considering an array of precisely identical defects which have precisely identical energy levels. This array of defects would have a DOS as

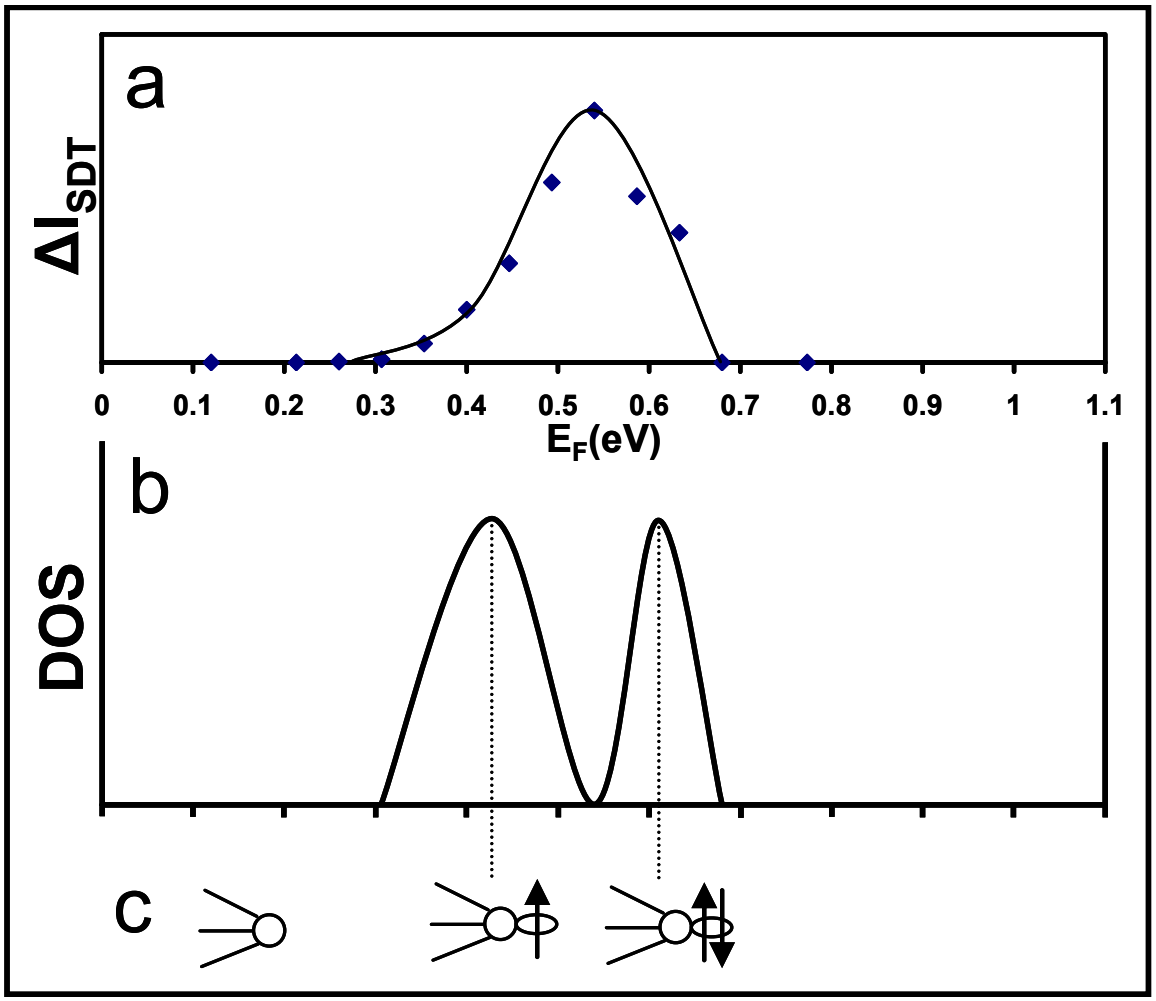

Figure 3.8: (a) The ER-SDT response as a function of interface Fermi level position, (b) a crude schematic representation of K center density of states, and (c) a cartoon representation of the charge states of the K centers.

illustrated in figure 3.9. Figure 3.10a illustrates a more physically reasonable DOS in which each of the levels is broadened to take into account disorder. If the Fermi level is below the (+/0) level, the defect's unoccupied dangling bond orbital does not have an electron to contribute to the tunneling. The defect is also diamagnetic (no unpaired electron) and cannot take part in magnetic resonance. Thus, with the Fermi level below the (+/0) level, no ER-SDT signal can be observed.

However, if the Fermi level crosses the (+/0) level of some of the K centers, these centers can contribute to the tunneling and are paramagnetic and do take part in magnetic resonance. Therefore, the ER-SDT response begins to turn on as the Fermi level crosses the lower (+/0) levels and increases as long as the Fermi level continues to cross these levels. However, as the Fermi level begins to cross the (0/-) level, the orbitals begin to accept a second electron and become negative. When this happens, the centers lose their paramagnetism and can no longer take part in magnetic resonance, so the ER-SDT response is reduced. The ER-SDT response drops to zero when all of the K centers accept the second electron. This ER-SDT response is illustrated in figure 3.10b.

Figure 3.10c illustrates the derivative of the ER-SDT amplitude vs. energy response of figure 3.10b. Notice that the maximum on the left side of the trace occurs at the same energy as the (+/0) peak in figure 3.10a. This is so because the increase in ER-SDT amplitude vs. energy will be greatest at the lower peak of the curve in figure 3.10a. Analogously, since the rate of decrease in ER-SDT amplitude vs. energy will occur at the (0/-) peak, the minimum on the right will occur at that (0/-) energy. Thus, the absolute value of the derivative shown in figure 3.10d is a fairly good first order representation of the defect DOS.

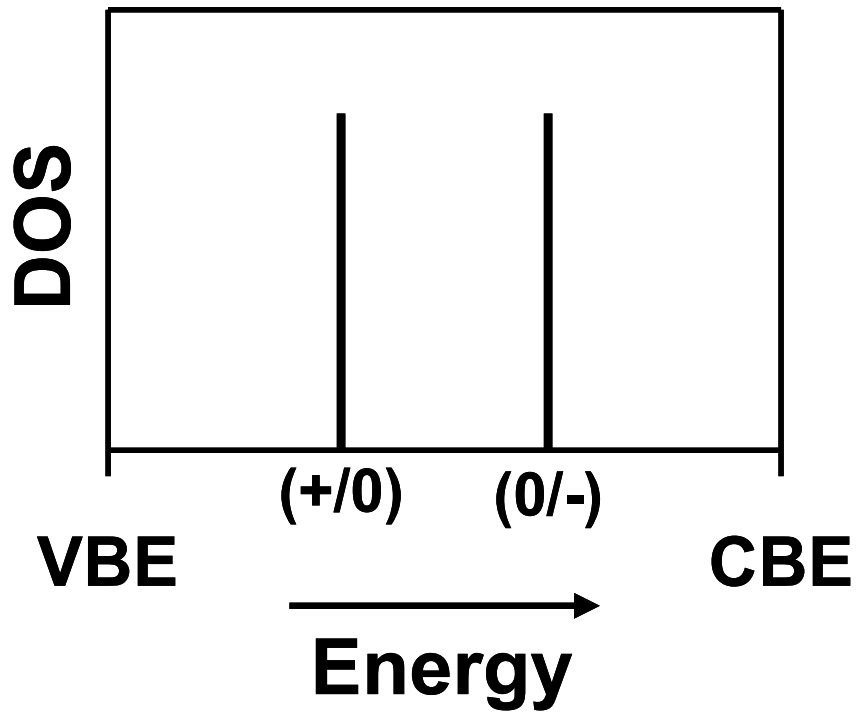

Figure 3.9: Schematic illustration of the density of states for an array of precisely identical defects with precisely identical energy levels between the valence band edge and the conduction band edge.

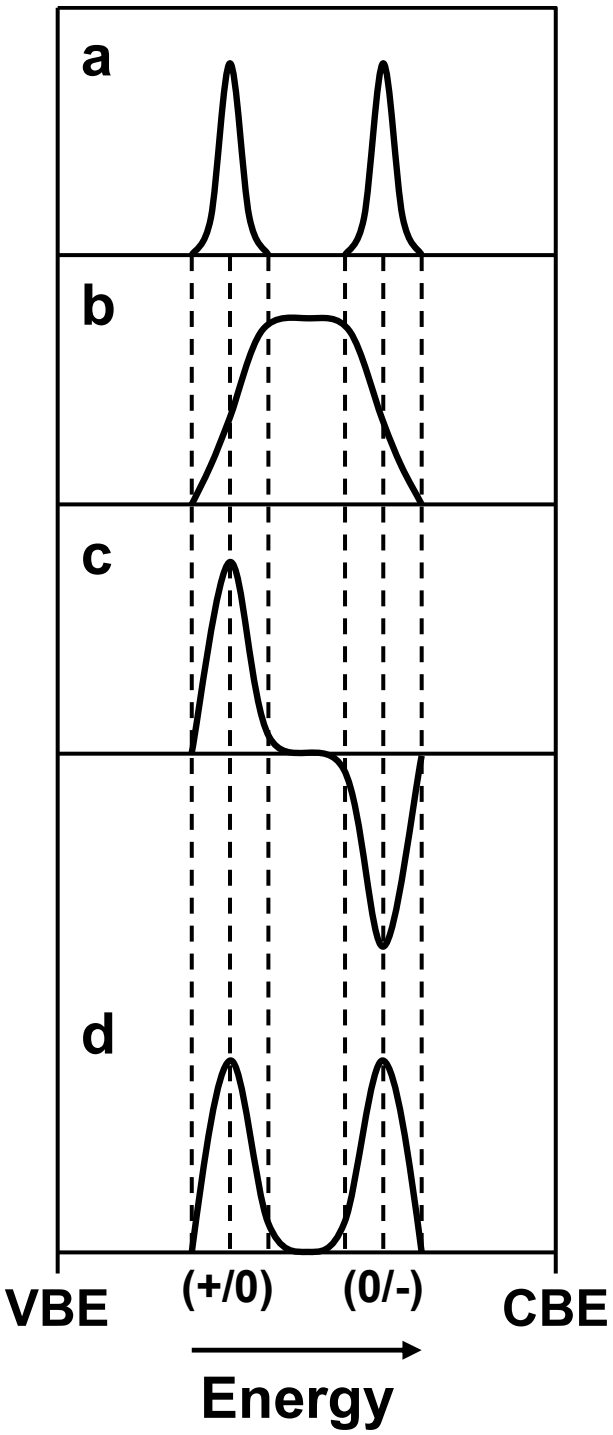

Figure 3.10: (a) A more physically reasonable density of states in which each of the levels of figure 3.9 is broadened to take into account disorder. (b) The ER-SDT response from the levels of (a). (c) Schematic illustration of the derivative of the ER-SDT amplitude vs. energy response of (b). (d) The absolute value of the derivative (c). The plot illustrated in (d) is, as discussed in the text, an approximation of the defect density of states.

It is important to point out that this absolute value of the derivative is only a first order representation of the actual DOS. If the (+/0) and (0/-) transition peaks overlap, the absolute value of the derivative will incorrectly indicate a zero in the DOS between the two peaks. Also, the tunneling transmission probability from the K centers to defects in the poly-silicon gate will not be precisely constant throughout the energy range (about 0.4eV) over which the ER-SDT is observed. However, the transmission probability will vary relatively slowly over the energy range. Consider the WKB approximation as a very crude predictor of the tunneling transmission coefficient (T) from a trap close to the crystalline-Si substrate/dielectric interface to a defect close to the poly-Si/dielectric interface:

$$T \cong \exp\left\{-2\left(\frac{2m^*\phi}{\hbar^2}\right)^{\frac{1}{2}} d\right\} \exp\left\{-2\left(\frac{2m^*\phi}{\hbar^2}\right)^{\frac{1}{2}}\left(\frac{qEd}{4\phi}\right) d\right\}, \tag{6.1}$$

where m^* is the effective mass of the electron which we take to be about $0.5m_e$, ϕ is the difference in energy between the interface Fermi level and the dielectric conduction band edge at the interface, $\hbar$ is Planck's constant divided by 2π, E is the dielectric electric field, d is the dielectric thickness, and q is electronic charge. Over the range in energy in which ER-SDT is observed, T varies by approximately a factor of three. However, for the distance between the peaks in the absolute value of the derivative (about 0.17eV), the variation in T is much smaller, about 30%. Thus, our experimental evaluation of the DOS is very crude but should provide a fairly accurate measure of the average (+/0) and (0/-) transition levels.

Note that this very crude representation is correct to the extent that the average energy of the first (+/0) transition is almost certainly higher than 0.26eV and the average

energy of the (0/-) transition is almost certainly lower than 0.68eV but above 0.54eV. As mentioned previously, this approximation is illustrated in figure 3.8b. The cartoons of figure 3.8c illustrate the charge and spin states of the K centers. Figure 3.8b indicates that the K center electron-electron correlation energy is quite small, roughly 0.2eV. This result is semi-quantitatively consistent with estimates made for the K center in Si_3N_4 [165]. These results and their interpretation are qualitatively consistent with ideas of Nicollian *et al.* [71, 72] who developed a model for LV-SILC based on interface trap to interface trap tunneling.

As mentioned previously, most EDMR studies have utilized SDR. Lepine was first to address potential models for SDR [38]. He envisioned a process in which two spins interact essentially in an instantaneous collision; in his model, the size of the effect is limited by the product of the polarization of the two spin systems; that of a charge carrier and that of a paramagnetic deep level defect. Under the circumstances of our measurements, the product of the polarization of two spin systems would be approximately 10^{-6}. In a Lepine like process then, the maximum possible effect would be a current change of about one part in one million. Kaplan, Soloman, and Mott proposed an SDR model in which they envisioned a coupling between a pair of spins for a finite time [37]. The model of Kaplan *et al.* [37] could be consistent with a much larger effect. Figure 3.11 illustrates the magnitude of the ER-SDT resonance as a function of microwave power. The effect clearly exceeds 10^{-6} at the highest power levels available to us; the effect is clearly far from saturated at our highest power level. This indicates two things: (1) the ER-SDT response reported in this study probably involves a mechanism more like that described by Kaplan *et al.* [37] than that of Lepine [38].

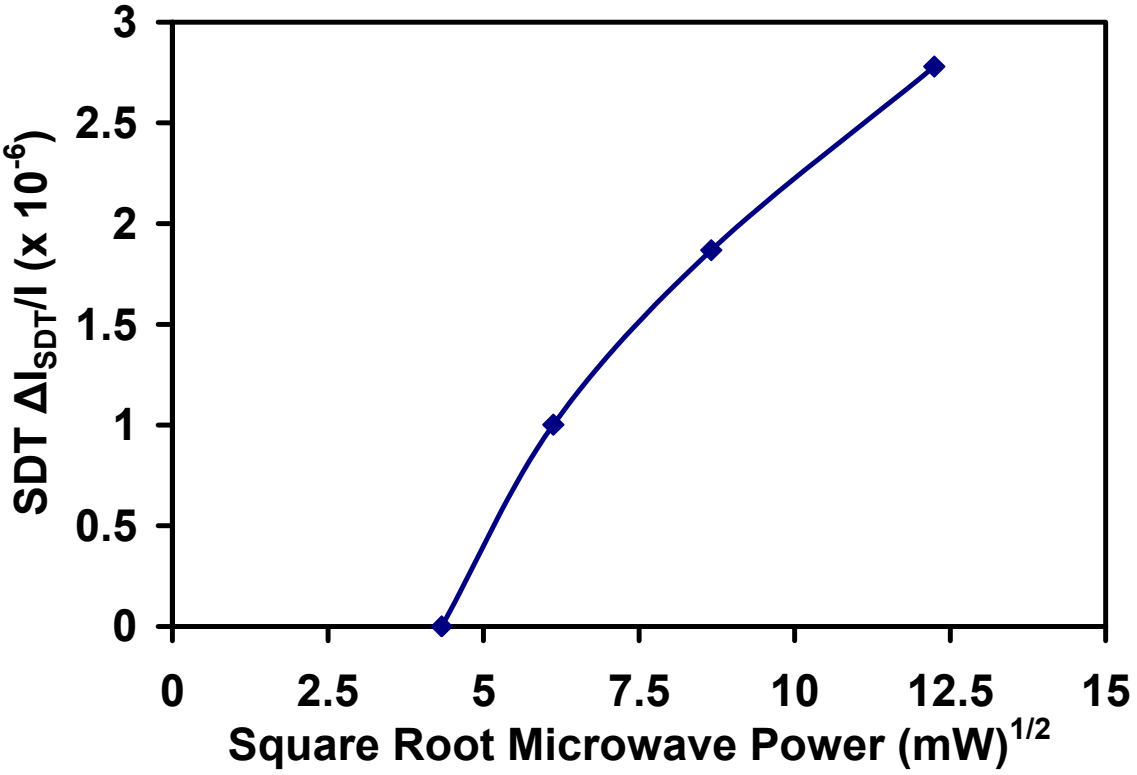

Figure 3.11: ER-SDT signal intensity ($\Delta I_{SDT}/I$) vs. square root of microwave power. Note that the signal intensity does not saturate at the highest power level available in our measurements. This indicates that far higher sensitivities are possible. (The amplitude would continue to grow if the power level could be increased further.)

(2) Since the sensitivity in our measurements is already high and the response is far from maximized at the highest level of power available to us, the sensitivity of the technique is potentially quite high.

3.3 Summary

In summary, the very simple ER-SDT measurement offers the capability to directly link the analytical power of magnetic resonance with defect energy levels. Our results on 1.2nm EOT plasma nitrided SiO_2 MOS devices strongly indicate that LV-SILC is dominated by K center defects. By exploiting the very high capacitance of the thin dielectric and the much lower capacitance of the silicon depletion region, we approximate the K center DOS.

One could envision extending this ER-SDT approach to more complex device structures, different materials, and thicker dielectrics. One could also envision extending this approach to quantum computing as it provides a simple sensitive method for magnetic resonance which could, at least in principle, be utilized at temperatures low enough to assure quite long spin lattice relaxation times [166].

Chapter 4

WHAT TRIGGERS THE NEGATIVE BIAS TEMPERATURE INSTABILITY?

In this chapter, we utilize a newly developed means to perform on-the-fly ESR measurements of NBTI defect generation. As mentioned earlier, the very fast recovery phenomenon complicates NBTI measurements and must be accounted for if stress conditions are altered prior to or during a measurement. Since our on-the-fly ESR approach permits ESR measurements without the alteration or removal of stress conditions, it provides a unique means to observe NBTI degradation void of any recovery contamination. We demonstrate that elevated temperature (100°C) and modest negative polarity oxide electric field (<5MV/cm) generate ESR spectra of E' oxide defects. (These defects are holes trapped in oxygen vacancies.) When similar measurements are made at elevated temperature and no oxide bias, E' center spectra are not observed. When ESR measurements are made with identical negative oxide bias at room temperature, E' center spectra are not observed. Furthermore, we demonstrate that the E' center spectrum disappears, a recovery phenomenon, when the NBTI stressing condition is removed. These observations indicate that NBTI is triggered by inversion layer hole capture at an E' precursor site (an oxygen vacancy) which then leads to the depassivation of nearby interface states (P_b centers). These results are consistent with and fully support the qualitative arguments of Campbell *et al*. [29, 30], Lenahan [31] and the comprehensive quantitative two-stage model proposed by Grasser *et al*. [36].

4.1 Experimental Details

The samples used in this study are simple Si/SiO_2 blanket capacitor structures with 49.5nm thermally grown SiO_2 oxides. The samples received a forming gas anneal following thermal oxidation. ESR measurements were performed before, during, and after the samples were subjected to a NBTS of V_G = -25V at 100°C. On-the-fly ESR measurements were performed by first applying negative gate bias via corona ions and then loading the biased samples into a heated quartz dewar situated inside the ESR microwave resonance cavity. The gate bias was monitored before and after stress with a Kelvin probe. ESR measurements were made on a commercially available Bruker Instruments X-band spectrometer with a TE_{104} microwave cavity and a calibrated weak pitch spin standard. Some measurements also utilized a calibrated SiO_2 E' standard [167].

4.2 Results and Discussion

Figure 4.1 illustrates pre-stress ESR spectra for the forming gas annealed sample (bottom trace) and a nearly identical sample which did not receive a forming gas anneal (top trace) at identical spectrometer gain. The spectrometer settings used were chosen to permit the observation of both P_b and E' defects and are not optimized for either defect. The sample which did not receive the forming gas (top trace) displays three spectra with g = 2.0063 (P_{b0} Si/SiO_2 interface states), g = 2.0036 (P_{b1} Si/SiO_2 interface states), and g = 2.0006 (E' oxide defects). The sample which did receive the forming gas anneal (bottom trace) displays a much weaker signal with g = 2.0069 which is consistent with a low density of Si/SiO_2 P_{b0} centers. The second integral of the ESR signal is proportional to

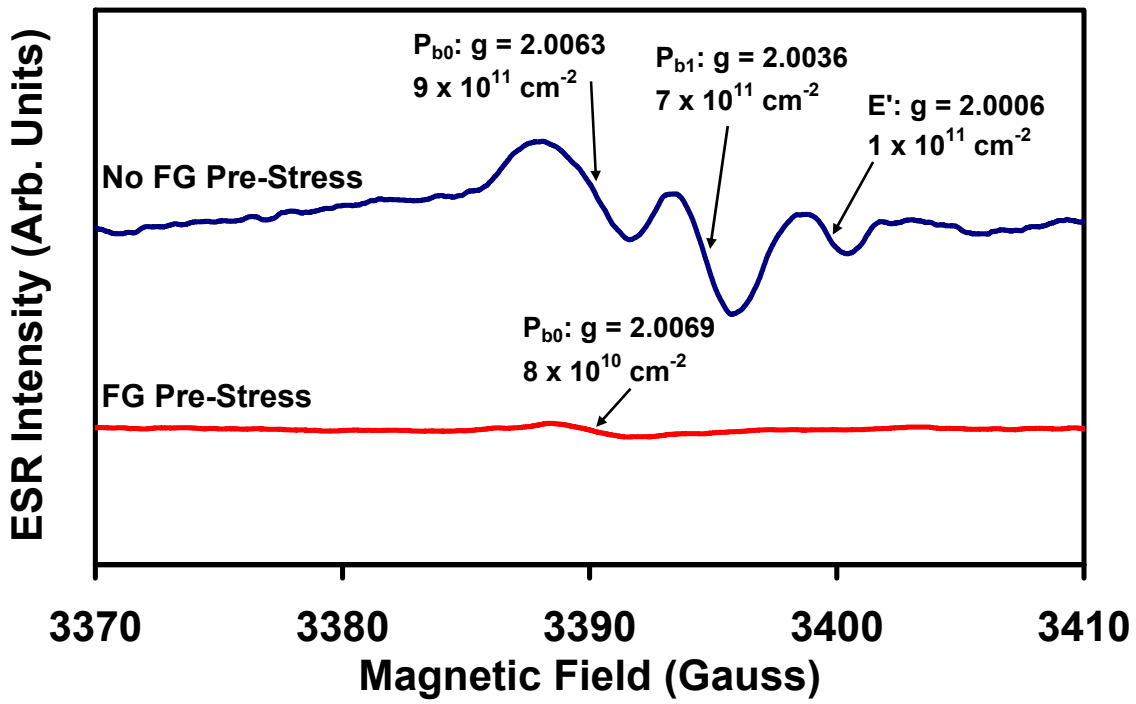

Figure 4.1: Comparison of pre-stress ESR spectra plotted with identical spectrometer gain for the sample treated with forming gas (bottom trace) and a nearly identical sample which was not treated with forming gas following oxidation (bottom trace). As expected, the sample which received the forming gas anneal is of much higher quality.

the number of defects present and, as expected, the forming gas annealed sample has far fewer defects present pre-stress. Since Si/SiO_2 samples which did not receive forming gas anneals are not technologically relevant, only results taken on the sample which did receive the forming gas anneal are shown in the remainder of this chapter.

Figure 4.2 illustrates three ESR traces taken at room temperature for the sample with forming gas. The top trace was taken on the as-processed sample, the middle trace was taken with the sample biased with -25V at room temperature, and the bottom trace taken after removing the negative bias. The room temperature corona bias of -25V (middle trace) does not result in an increase of interface states (P_b centers) or oxide defects (E' centers). It does, of course, suppress the P_{b0} signal because these defects are interface traps and can respond to the substrate silicon Fermi level [168]. (The negative bias renders most of the P_{b0} centers positive and diamagnetic.) Figure 4.3 illustrates three ESR traces taken at zero volts bias for the sample. The top trace was taken on the as-processed sample at room temperature, the middle trace was taken with the sample at elevated temperature (100°C), and the bottom trace taken after returning the sample to room temperature. The elevated temperature at zero volts bias (middle trace) does not result in an increase of interface states or oxide defects.

Figure 4.4 illustrates three ESR traces taken before (top trace), during (middle trace) and after (bottom trace) NBTI stressing. As mentioned previously, in the pre-stress case (top trace) we observe a weak spectrum consistent with Si/SiO_2 P_{b0} centers. During NBTI stress, we observe the clear generation of Si/SiO_2 P_{b1} centers ($g = 2.0034$) and SiO_2 E' centers (2.0006). Upon removal of the stress, the $g = 2.0006$ E' center signal

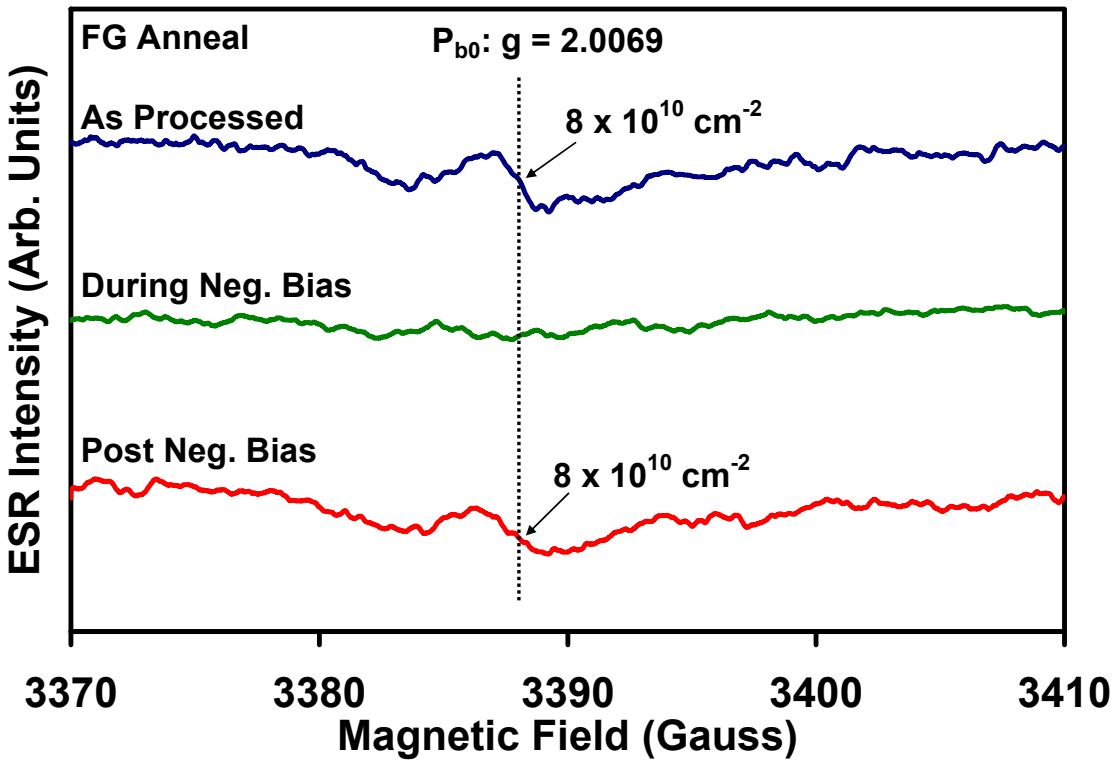

Figure 4.2: Room temperature ESR traces taken on the sample which received a forming gas anneal as-processed (top trace), with -25V bias (middle trace), and after removal of negative bias (bottom trace). Note that the negative bias alone does not generate additional P_b interface states or E' defects.

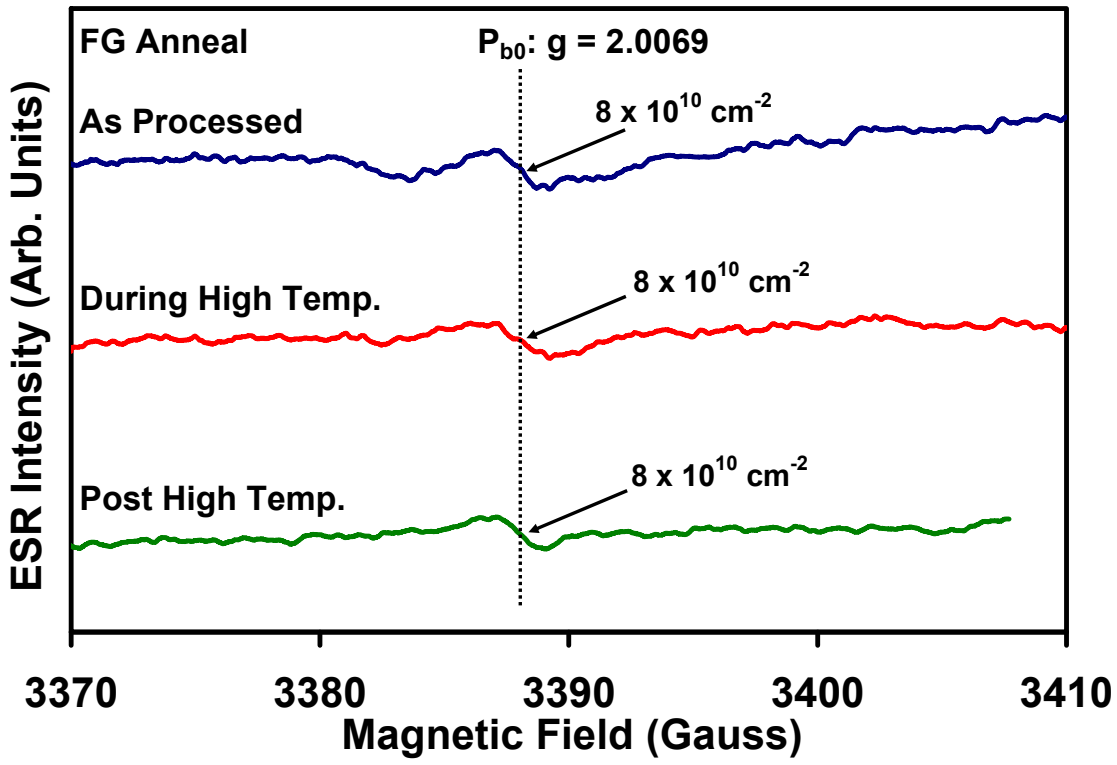

Figure 4.3: Three ESR traces for the sample which received the forming gas anneal as-processed (top trace), with zero volts bias at 100°C (middle trace), and after cooling the sample back to room temperature (bottom trace). Note that the elevated temperature alone does not generate additional P_b interface states or E' defects.

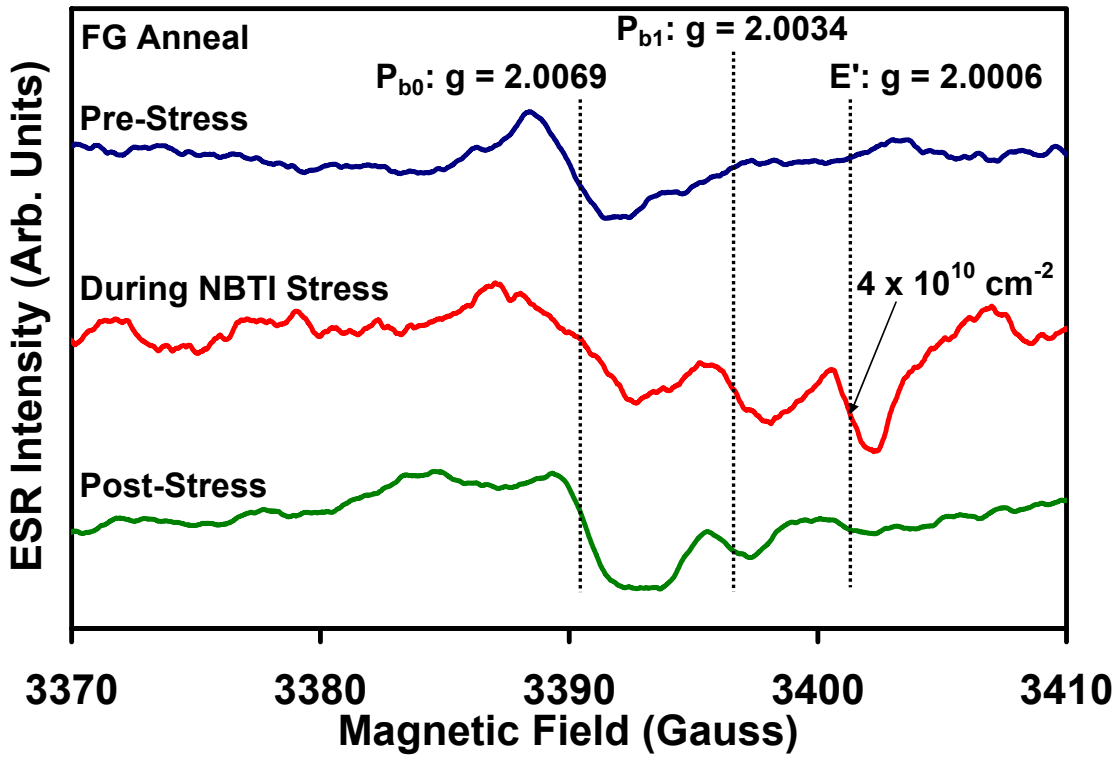

Figure 4.4: Three ESR traces for the sample which received the forming gas anneal. Note the clear generation of an E' signal during NBTI stress (middle trace), as well as P_{b1} center generation, and the nearly complete recovery of the E' defects post-stress (bottom trace).

completely recovers while some of the P_{b1} centers remain. This result clearly demonstrates that E' centers are generated during NBTI stress and very quickly recover upon removal of the stress; that is, positively charged oxygen vacancy sites are generated during stress and very quickly recover.

As mentioned previously, the spectrometer settings used in figures 4.1-4.4 were chosen to permit the observation of both Si/SiO_2 P_b centers and SiO_2 E' centers and are not optimized for either defect; the E' center density is underrepresented in these traces. (There is a significant difference in E' and P_b spin lattice relaxation times which leads to this underrepresentation [117].) In an attempt to further demonstrate that E' centers (positively charged oxygen vacancy sites) are present during NBTI stressing, figure 4.5 shows three ESR traces taken on the forming gas annealed sample before (top trace), during (middle trace) and after NBTI stressing (bottom trace). In this figure, the spectrometer settings are optimized for the observation of E' centers. When NBTS stressing is applied (middle trace), a clear signal with $g_{\parallel}=2.0016$ and $g_{\perp} = 2.0006$ appears which is characteristic of an E' center. Upon removal of the NBTI stress (bottom trace), the E' signal completely recovers. Figure 4.6 further demonstrates the identification of this signal as due to an E' center by comparing the during NBTI stress spectra of figure 4.5 (top trace) with that of a commercially available E' standard (bottom trace) [167]. Note the close correspondence between the g values and the line shapes which are characteristic to this type of defect.

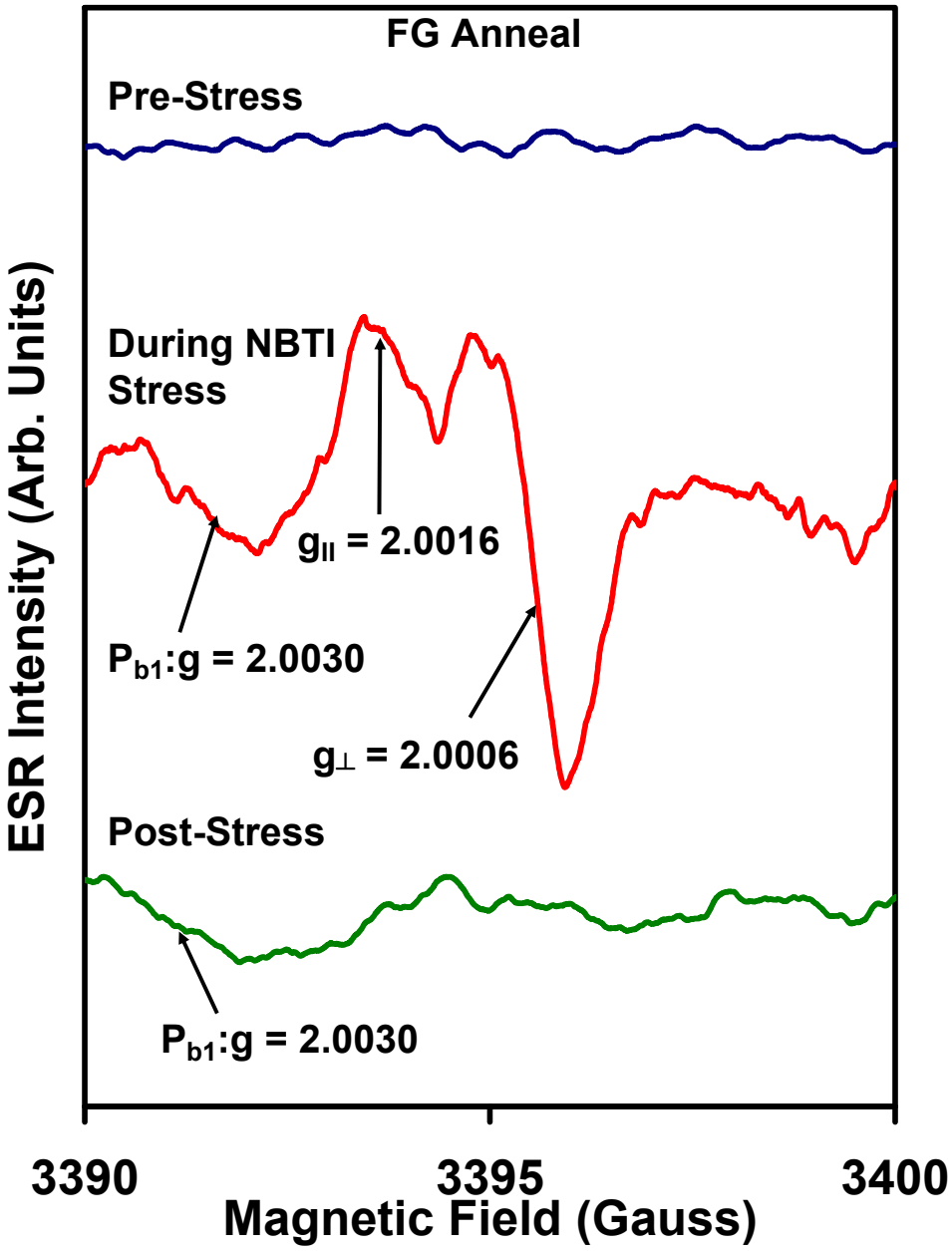

Figure 4.5: Three ESR traces taken on the sample which received the forming gas anneal. In these traces, the spectrometer settings are optimized to observe E' centers. Note the clear generation of an E' spectrum during stress (middle trace) and its subsequent recovery post-stress (bottom trace).

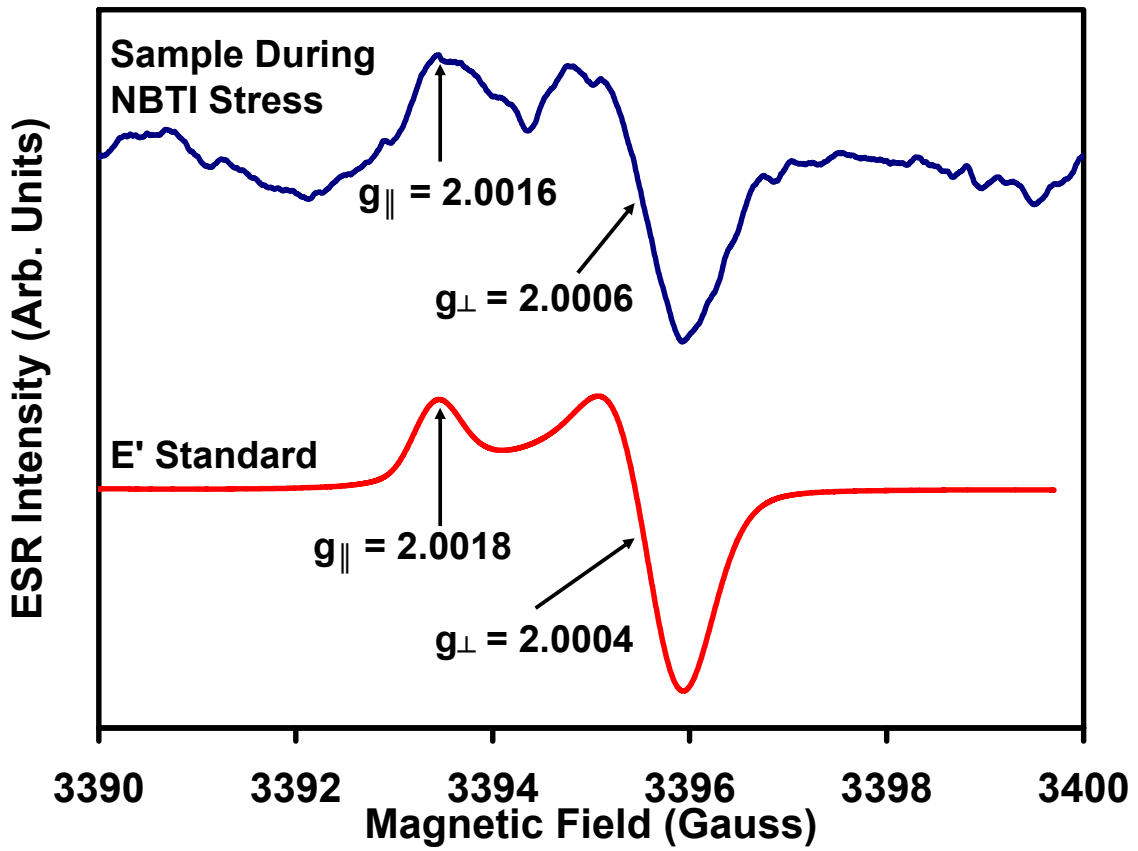

Figure 4.6: Comparison of the forming gas annealed sample during NBTI stress from figure 4.5 (top trace) and a commercially available E' standard (bottom trace). The standard sample signal-to-noise is much higher because the standard has orders of magnitude more E' centers. Note the close correspondence between the g values and line shapes. The gain of the sample trace is approximately 10,000 times larger that used for the E' standard; all other spectrometer settings are identical. (Note that the precision of g is ± 0.0002.)

4.3 Summary

In summary, we present results which demonstrate that E' centers are generated in Si/SiO_2 MOS structures when subjected to modest negative oxide bias at elevated temperature. We further demonstrate that these E' centers recover once the stressing conditions are removed. Only the combination of negative oxide bias and elevated temperature results in E' center generation. These results are consistent with and strongly support the suggestions of Campbell *et al.* [29, 30] and Lenahan [31] as well as the more recent comprehensive two-stage model proposed by Grasser *et al.* [36] in which NBTI is triggered by the tunneling of electrons from a neutral E' center precursor to unoccupied valence band states.

Chapter 5

THE ROLE FLUORINE PLAYS IN SUPRESSING THE NEGATIVE BIAS TEMPERATURE INSTABILITY

In this chapter, we use SDR measurements to directly observe the atomic-scale effects of fluorine on NBTI response in fully processed 7.5nm fluorinated SiO_2 MOSFETs. DC-IV measurements demonstrate a correlation between the SDR results and device parameter degradation (interface state generation). We compare the results to virtually identical pure SiO_2 MOSFETs which serve as a good comparison for our observations in fluorinated SiO_2 devices. Our results clearly demonstrate that fluorine incorporation generally suppresses NBTI degradation compared to pure SiO_2 oxides, consistent with earlier studies [42, 43]. Additionally, our results show that fluorine can effectively passivate Si/SiO_2 P_{b0} center precursors and much less effectively passivates Si/SiO_2 P_{b1} center precursors. Thus, P_{b1} centers dominate the NBTI response of these fluorinated SiO_2 devices. This is important because P_{b0} and P_{b1} centers have significantly different DOS and thus the narrower P_{b1} DOS distribution will likely result in a larger threshold voltage shift in proportion to the total number of P_{b1} states, meaning a higher percentage of P_{b1} centers will likely be positively charged when the pMOSFET device is turned on. This larger effect per defect is of course more than compensated by the smaller total number of P_{b1} centers. Additionally, our observations help explain why fluorine reduces NBTI damage in pure SiO_2 devices but does very little to help reduce NBTI in nitrided oxide devices. In nitrided oxide devices, NBTI is not dominated by

Si/dielectric P_b centers [48], and thus the fluorine incorporation does not passivate the defect precursors.

5.1 Experimental Details

We compare the effects of NBTS on conventional pure SiO_2 devices and very similar fluorinated SiO_2 devices. Both types of devices are large area (~40,000μm^2) pMOSFETs with identical gate oxide thickness (7.5 nm) and device geometry. Three differently processed sets of fluorinated devices were used. SDR and DC-IV measurements were made before and after identical NBTS sequences (V_G = -5.7 V at 140°C for 250,000 seconds). Following NBTS, all devices were subjected to a temperature quench step in which the gate bias stress was maintained as the device was brought to room temperature over approximately 4 minutes. We have found this to be fairly effective at "locking-in" NBTI induced damage, rendering it observable in the SDR/DC-IV measurements [29]. SDR measurements were made at room temperature on a custom-built X-band spectrometer and were calibrated using a strong pitch spin standard.

5.2 Results and Discussion

Figures 5.1 and 5.2 illustrate representative pre- and post- NBTS DC-IV curves for the pure SiO_2 device (figure 5.1) and a representative fluorinated SiO_2 device (figure 5.2). The peak in the post-NBTS DC-IV curve, which scales with interface state density (D_{it}), is nearly an order of magnitude smaller in the fluorinated case (figure 5.2). Following the analysis of Fitzgerald and Grove [156] and assuming a mean capture cross section of $\sigma = 2 \times 10^{-16} cm^2$, D_{it} values were extracted. For pure SiO_2 (figure 5.1), $D_{it} = 7 \times 10^9$ cm^{-2} eV^{-1}

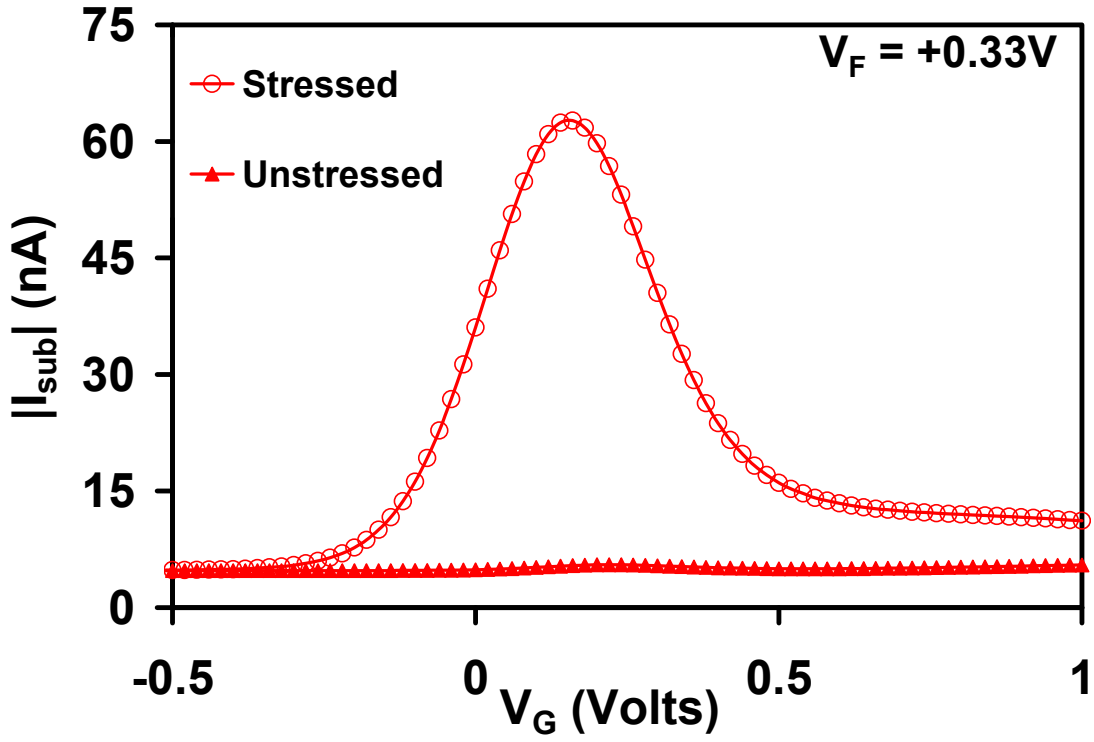

Figure 5.1: Representative pre- and post- NBTS DC-IV curves for the pure SiO_2 devices.

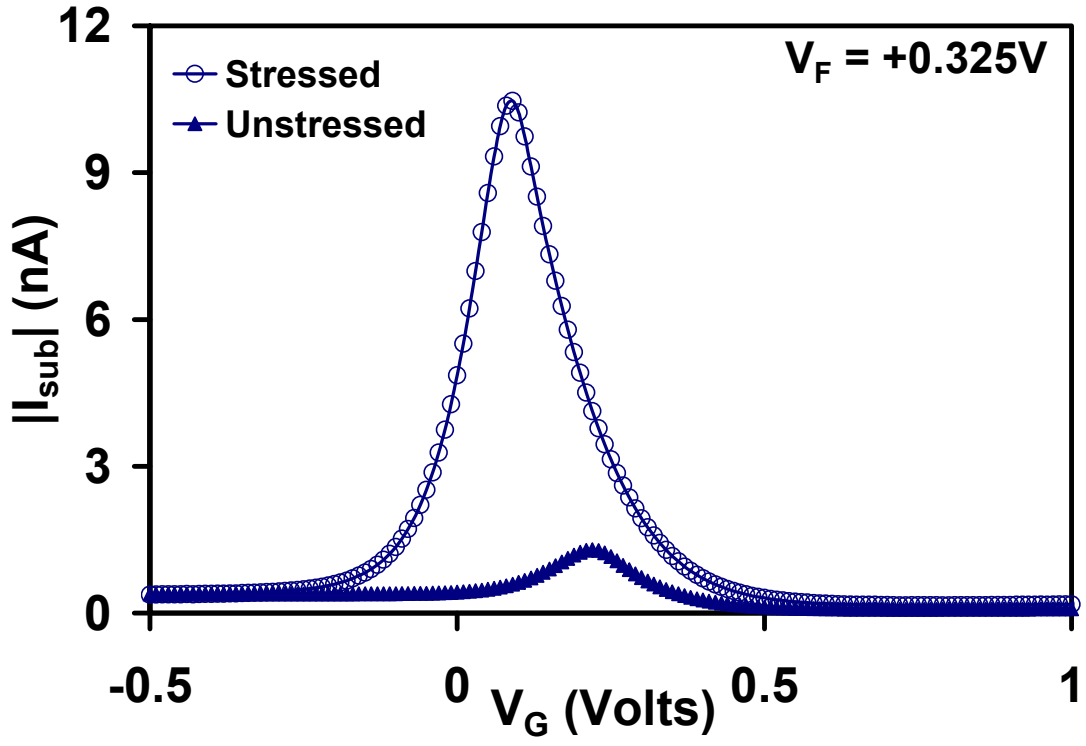

Figure 5.2: Representative pre- and post- NBTS DC-IV curves for the fluorinated SiO_2 devices. Note the decreased amplitude of the peak compared to the pure SiO_2 curve of figure 5.1. The smaller post-NBTS D_{it} for the fluorinated devices was consistently observed in our study.

for pre-NBTS and 5 x 10^{11} cm^{-2} eV^{-1} for post-NBTS. For the representative fluorinated SiO_2 sample (figure 5.2), D_{it} = 8 x 10^{9} cm^{-2} eV^{-1} for pre-NBTS and 9 x 10^{10} cm^{-2} eV^{-1} for post-NBTS. The reduction in post-NBTS D_{it} of figure 5.2 (compared to the nearly identical pure SiO_2 sample) was observed in all three sets of fluorinated SiO_2 devices in our study. This is consistent with other reports indicating less NBTI damage in fluorinated SiO_2 devices [42, 43].

Figures 5.3 (pure SiO_2) and 5.4 (fluorinated SiO_2) illustrate SDR traces of the two post-NBTS devices utilized in figures 5.1 and 5.2. In these traces the magnetic field is parallel to the (100) Si/SiO_2 interface normal. Pre-NBTS defect spectra were below the detection limit of the spectrometer. Note that in these figures, the spectrometer gain for the pure SiO_2 trace (figure 5.3) is much lower than the fluorinated SiO_2 trace (figure 5.4). Figure 5.3 exhibits two somewhat overlapping signals with g values of 2.0057 and 2.0031 which are, respectively, due to Si/SiO_2 P_{b0} and P_{b1} centers [35, 169]. Note that figure 5.3 is representative of NBTI SDR results on many essentially pure SiO_2 pMOSFETs, as reported earlier [20]. The figure 5.4 trace exhibits a significantly different and much weaker single line spectrum with a g of 2.0026 which is consistent with a P_{b1} center. Note also the somewhat broader width of the signal of figure 5.4. This may indicate the presence of nearby fluorine nuclei [151].

Although the device of figure 5.4 is very similar structurally and was stressed identically as the pure SiO_2 device of figure 5.3, their NBTI response is very different. For the case of the representative fluorinated device, there is no indication of P_{b0} center generation following NBTS. This observation suggests that the incorporation of fluorine

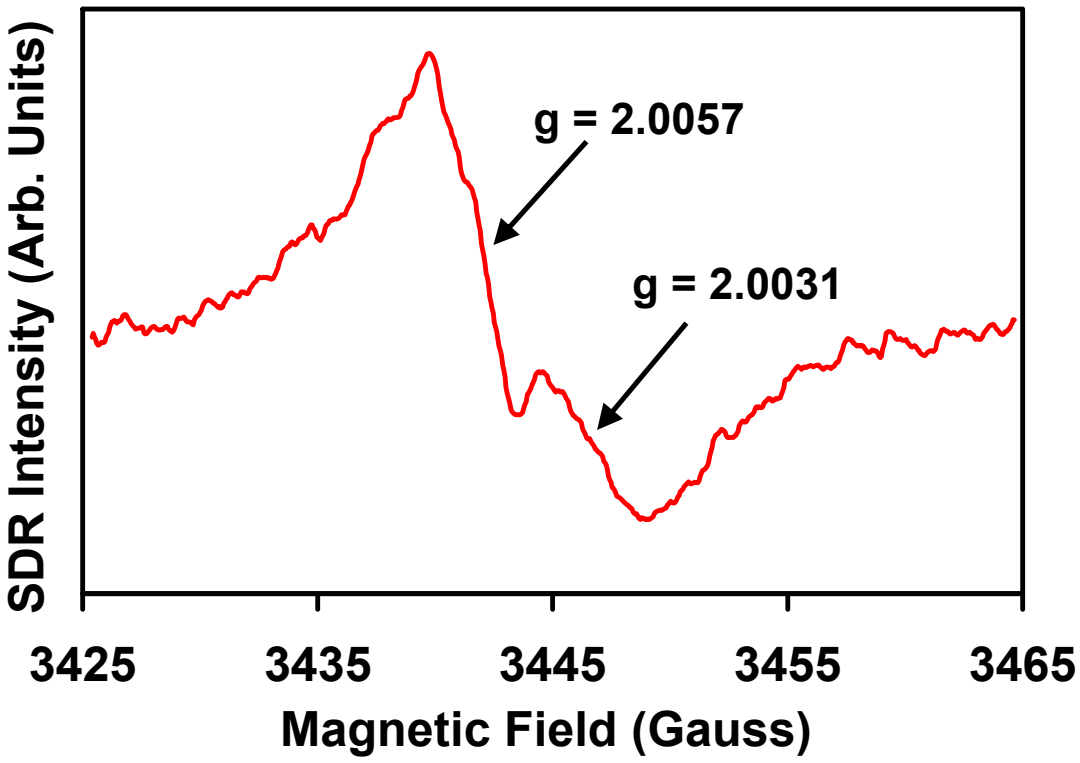

Figure 5.3: Post-NBTS SDR traces for the pure SiO_2 device of figure 5.1. The two signals are due to P_{b0} (g = 2.0057) and P_{b1} (g = 2.0031) Si/SiO_2 interface defects. Note that this data is representative of NBTI SDR results on many essentially pure SiO_2 pMOSFETs, as reported earlier.

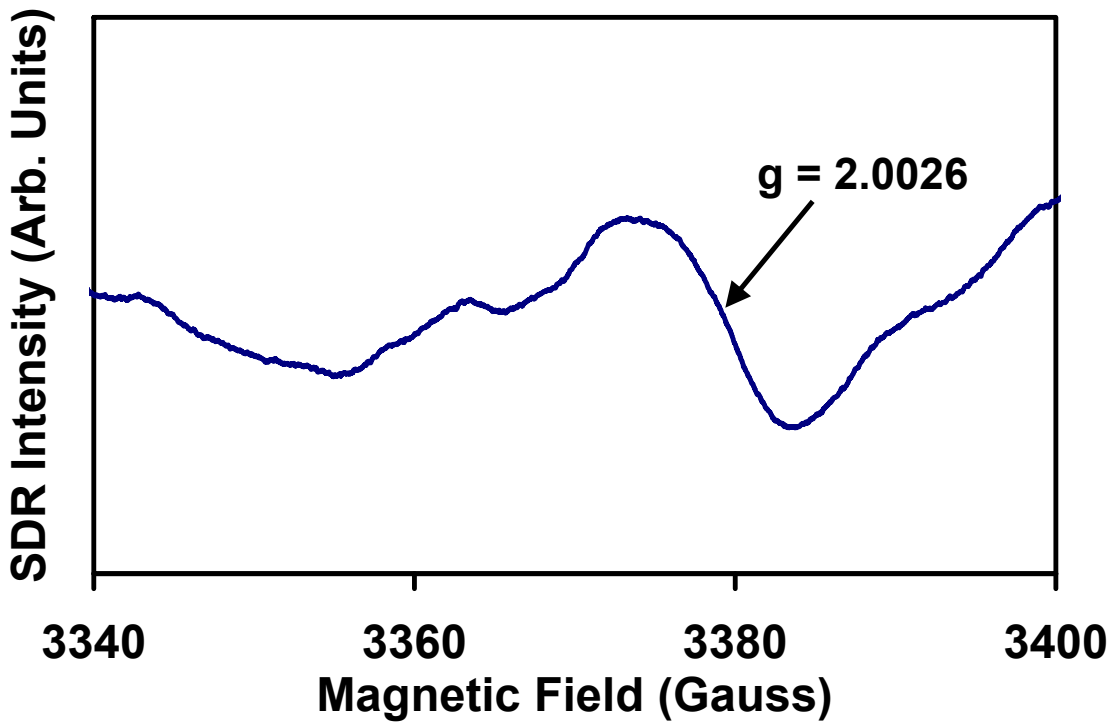

Figure 5.4: Post-NBTS SDR traces for the fluorinated SiO_2 device of figure 5.2. The signal is consistent with a P_{b1} Si/SiO_2 interface defect. The gain is much higher and the sweep width is greater to compenstate for the much weaker and somewhat broadened signal.

can selectively passivate P_{b0} precursors. That is, it is more effective at passivating the P_{b0} precursors.

Figures 5.5 and 5.6 illustrate (weak) post-NBTS SDR traces for the two remaining somewhat differently processed fluorinated SiO_2 devices. Again, pre-NBTS defect spectra are below the detection limit of the spectrometer. Although the signal-to-noise ratios are low, the same qualitative pattern appears: a much weaker SDR signal at $g \approx 2.003$ (which is consistent with P_{b1} center generation) and an absence of spectra expected for P_{b0} defects. Again, the larger width of the signal may indicate the presence of nearby fluorine nuclei [151]. DC-IV measurements (not shown) for the device from figure 5.5 indicate pre-NBTS $D_{it} = 2 \times 10^{10}$ cm^{-2} eV^{-1} and post-NBTS $D_{it} = 1 \times 10^{11}$ cm^{-2} eV^{-1}. For the device from figure 5.6, pre-NBTS $D_{it} = 1 \times 10^{10}$ cm^{-2} eV^{-1} and post-NBTS $D_{it} = 1 \times 10^{11}$ cm^{-2} eV^{-1}.

As mentioned previously, these results indicate that fluorine incorporation can effectively passivate P_{b0} center precursors, but less effectively passivates P_{b1} center precursors. This would help to explain the diminished interface state generation observed in other recent reports of NBTI stressed fluorinated devices [42, 43].

Additional SDR measurements on more complex fluorinated high-k based memory structures reveal that the defects observed (possibly P_{b1} like) are not identical to those commonly observed in conventional Si/SiO_2. Much broader SDR spectra (observed in both fluorinated SiO_2 and high-k devices with the magnetic field parallel to the (100) normal) suggest the presence of nearby fluorine. (Fluorine has a spin ½ magnetic moment which would broaden or split the spectrum.) The magnetic field orientation dependence of these defects also suggests that they are coupled to fluorine.

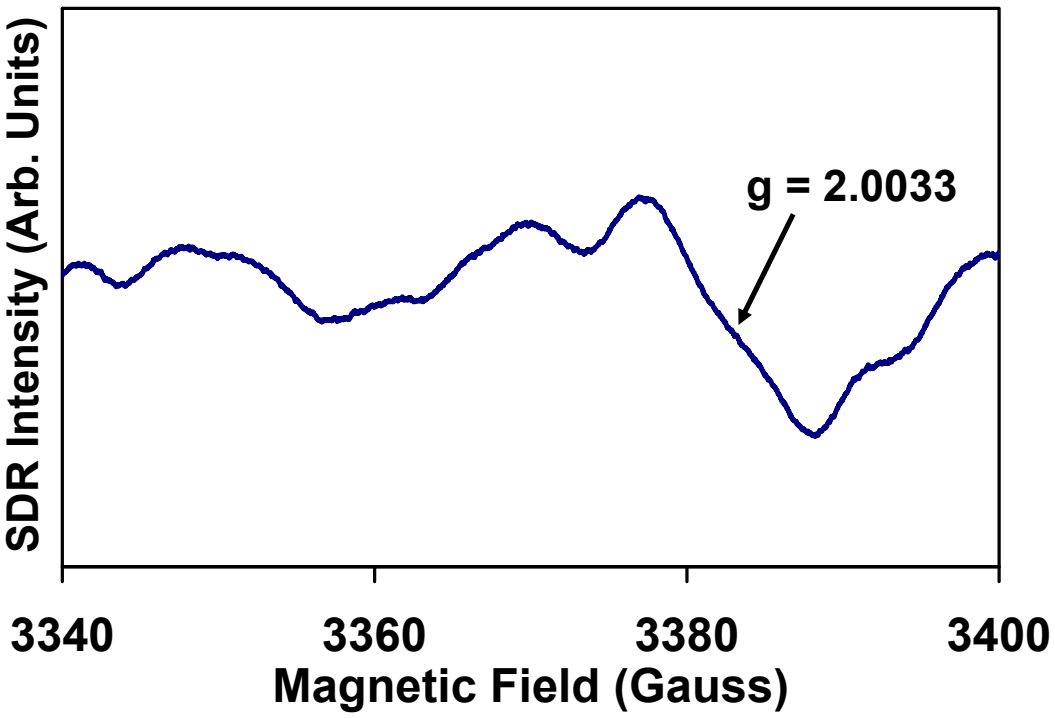

Figure 5.5: Post-NBTS SDR trace of a second somewhat differently processed fluorinated SiO_2 device. The qualitative pattern is identical: a weak P_{b1} signal and an absence of P_{b0} signal.

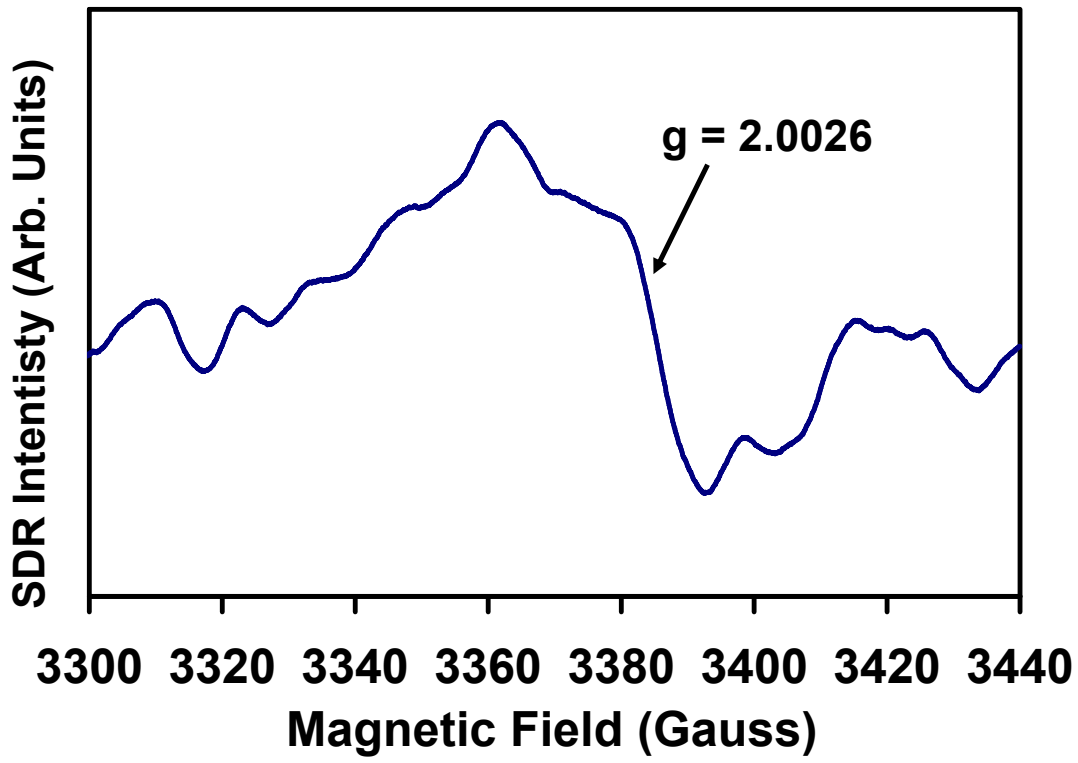

Figure 5.6: Post-NBTS SDR trace of a third somewhat differently processed fluorinated SiO_2 device. Note the much greater breadth of the signal; this may indicate the presence of nearby fluorine nuclei.

Rotating the magnetic field perpendicular to the (100) normal (figure 5.7) splits the spectrum into two lines, suggesting the presence of spin ½ nuclei.

P_{b0} and P_{b1} defects are the two variants of defect centers that dominate interface trapping at (100) Si/SiO_2 boundaries and are responsible for a wide range of MOS instability and performance issues [20, 35]. These defects are apparently responsible for the commonly observed increase in D_{it} following NBTI stressing of pure SiO_2 devices [19, 20]. The main differences between them are in the dangling bond axis of symmetry [35, 169] and their electronic DOS [168, 170]. A schematic illustration of P_{b0} and P_{b1} DOS is provided in figure 5.8.

P_{b0} centers have a broadly peaked DOS centered about midgap with an electron correlation energy of about 0.7eV [170]. The P_{b1} levels are much more narrowly distributed, with a DOS skewed towards the lower half of the band gap [168]. Since these defects have significantly different DOS, our results may be useful in modeling NBTI response in fluorinated oxide devices. The narrower P_{b1} DOS distribution will likely result in a larger shift in threshold voltage in proportion to the total number of P_{b1} states. That is, a higher percentage of P_{b1} centers will likely be positively charged when the pMOSFET is turned on. This larger effect per defect is, of course, more than compensated by the smaller total number of P_{b1} centers. The result also helps to explain why fluorine reduces NBTI damage in pure SiO_2 devices, but not in some nitrided devices; in nitrided devices, NBTI is not dominated by P_b centers [20].

Our results may also help to explain fluorine's role in reducing the effects of hot carrier damage and improving radiation hardness. Nishioka *et al.* [171] and Wright *el al*. [46] examined the effects of fluorine on hot electron response in fluorinated MOS devices.

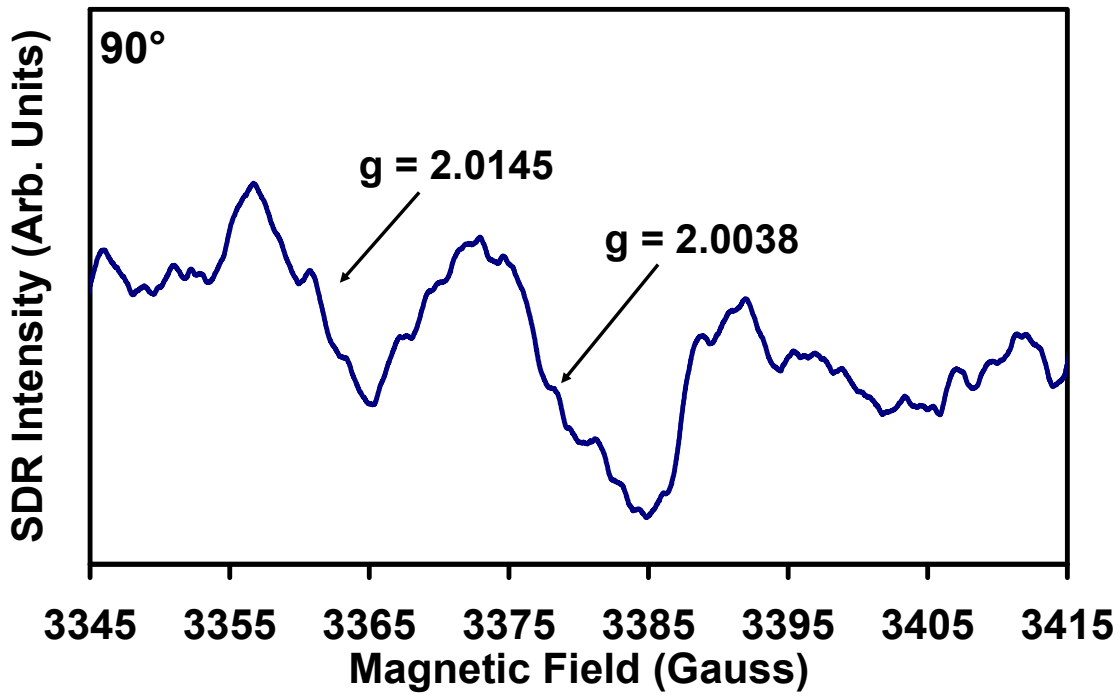

Figure 5.7: SDR trace of the more complex high-k based memory structure with the sample rotated 90° in the magnetic field. The two-line spectrum strongly suggests the defect is coupled to fluorine and demonstrates that the spectrum is not due to simple P_{b0} or P_{b1} centers. The low field line resonance condition would correspond to a g = 2.0145, far too high for any P_b center. The two lines suggest coupling with fluorine which has a spin ½ nucleus.

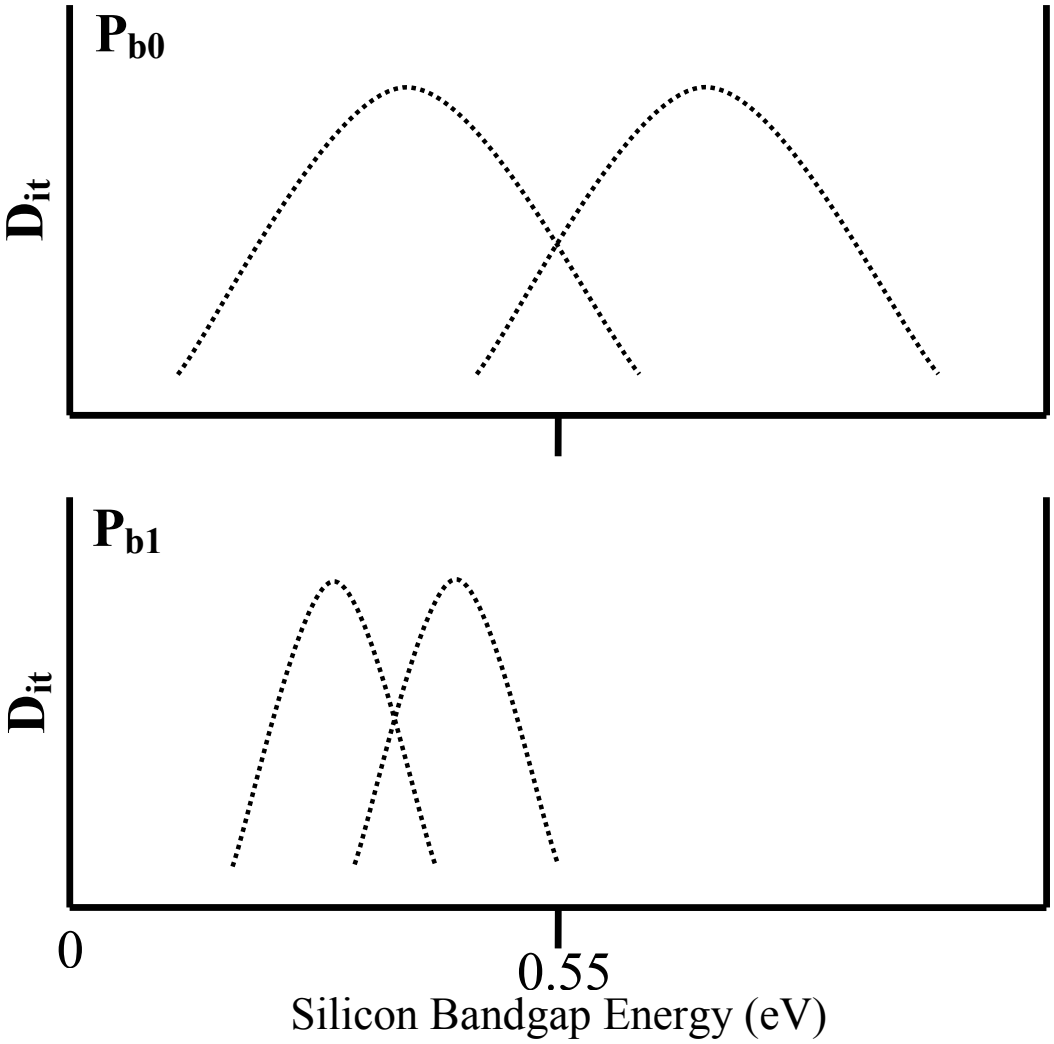

Figure 5.8: Schematic illustration of P_{b0} (top) and P_{b1} (bottom) density of states. P_{b0} and P_{b1} are the dominating interface states in pure Si/SiO_2 MOS devices.

Both studies show that fluorine incorporation leads to a more robust interface in which interface state generation is reduced compared to hot electron stressed pure SiO_2 devices. They suggest that the stronger silicon-fluorine bond (compared to silicon-hydrogen) or bond strain relief may be responsible for the improved interface response. Wang *et al.* [172] and da Silva *et al.* [173] showed that fluorine incorporation can improve the radiation hardness of SiO_2 MOS devices resulting in a reduced interface state density following irradiation. Again, these authors argue that the stronger silicon-fluorine bond may be responsible for the improved radiation hardness. Our results clearly indicate that fluorine more effectively passivates P_{b0} centers but is less effective at passivating P_{b1} centers in NBTI stressed devices. It is very likely that a similar phenomenon occurs in hot carrier stressed and irradiated devices resulting in a more robust interface. As has been noted in some of the earlier fluorine literature, these results make sense in terms of the relative strengths of silicon-hydrogen and silicon-fluorine bond energies. Pauling estimated the strength of the silicon-hydrogen bond to be approximately 295 KJ $mole^{-1}$ and the strength of the silicon-fluorine bond to be much larger, 510 KJ $mole^{-1}$ [174].

5.3 Summary

In summary, we present results which demonstrate that the incorporation of fluorine can diminish NBTI degradation in agreement with other recent work [42, 43]. Although the pure SiO_2 control devices are virtually identical to the fluorinated SiO_2 devices, their NBTI response is dramatically different. Our results strongly indicate that fluorine incorporation in the SiO_2 effectively passivates P_{b0} center precursors but much less effectively passivates P_{b1} center precursors. As a result, P_{b1} centers dominate the

resulting NBTI induced defect spectra. (The small effect is a decidedly tougher interface for NBTI.) Since these two defects have significantly different DOS, our results may be useful for modeling fluorinated oxide NBTI response. Our results also suggest that fluorine nuclei are present near these defects. Additionally, our results help to explain why fluorine reduces NBTI damage in pure SiO_2 devices, but not in some nitrided oxide devices; in nitrided oxide devices, NBTI is not dominated by P_b centers but rather K center defects [40, 48, 175] which likely cannot be fluorine passivated.

Chapter 6

THE NATURE OF INTERFACIAL LAYER DEFECTS IN Si/HfO_2 MOS STRUCTURES

Recent studies clearly indicate that near Si/dielectric trapping centers (that is, centers within the SiO_2 like interfacial layer region) play important roles in Si/HfO_2 device instabilities. In this chapter, we utilize conventional ESR measurements to characterize large process dependent variations of paramagnetic defect centers in the near Si/dielectric interfacial layer region of Si/SiO_2/HfO_2 blanket films prepared to replicate the thermal cycles of HfO_2 based MOSFET device processing. We also utilize SDR measurements to characterize similar defects in fully processed metal gate HfO_2 MOSFETs.

In a study involving several processing variations, we find large differences in the densities of two (likely) E' centers in the near Si/dielectric interfacial layer region. The presence, sometimes in very high densities, of E' defects in the Si/dielectric interfacial layer region supports the idea that the interfacial layer is not stoichiometric SiO_2, but rather an oxygen deficient silicon rich dielectric. This conclusion is in agreement with earlier studies [88, 99] which suggested that HfO_2 deposited on a SiO_2 layer would leach oxygen from the interfacial layer to an extent highly dependent upon processing details.

Additionally, specially prepared Si/HfO_2 blanket structures were prepared to study the electronic properties and structure of this presumed oxygen deficient silicon site in the interfacial layer. Previous studies [55, 93, 109, 116] on HfO_2 films lacked adequate sensitivity to perform extensive high-resolution ESR measurements on this

defect in ultra-thin HfO_2 films. The simply processed structures discussed herein were specifically designed to yield a strong spectra associated with the oxygen deficient silicon in the interfacial layer region. The much stronger signal in these samples gave the additional sensitivity required to perform fairly extensive ESR measurements (orientation dependence, oxide biasing, and saturation measurements) reported herein.

6.1 Experimental Details

In this chapter, two sets of HfO_2 samples where utilized. Sample set 1 consisted of HfO_2 deposited via ALD with a tetrakis(ethylmethylamino)hafnium precursor with ozone on eight-inch (100) silicon substrates to a thickness of 3nm. Special ultra-high resistivity substrates ($\rho > 10^3 \Omega$-cm) were utilized to facilitate ESR sensitivity. HfO_2 deposition was performed on two types of a thin SiO_2 interfacial layer: a chemical oxide of about 1.1nm resulting from the O_3 treatment of the silicon substrate and an in-situ steam generated (ISSG) SiO_2 (2nm) which was etched back to approximately 1.1nm (EB ISSG). All samples in this set received a standard forming gas anneal prior to HfO_2 deposition. This sample set also includes a comparison of no post-HfO_2 deposition anneal and post-HfO_2 deposition N_2 (700°C/60s) and N_2 (1000°C/10s) annealed samples as well as a comparison of samples with and without a 10nm thick TiN cap deposited prior to post-HfO_2 deposition annealing. (The TiN cap was etched off prior to ESR measurements.) In one case, the HfO_2 was deposited in a way that produced an oxygen deficient HfO_2 film. The measurements involve comparisons to two Si/SiO_2 "control" samples consisting of O_3 generated SiO_2 (1nm) and EB ISSG SiO_2 (1.1nm). No HfO_2 was deposited on the SiO_2 control samples.

Sample set 2 consisted of HfO_2 deposited via magnetron sputtering at room temperature to a thickness of 509nm on ultra-high resistivity ($\rho > 10^3$ Ω-cm) (100) silicon substrates in an oxygen deficient atmosphere (prepared by J. Robertson of Cambridge University). Although the total dielectric is very thick, these samples were chosen to provide an interfacial layer in which the defects associated with the E' like oxygen deficient silicon centers observed in sample set 1 (and other previous studies [55, 93, 109, 116]) are present in very high numbers close to the Si/dielectric boundary. These high numbers allowed for much higher resolution ESR measurements to be made. In order to maintain the sensitivity of the ESR measurements, no metal gate was utilized for oxide biasing. Instead, these measurements were performed utilizing the corona ion "gateless" biasing technique which allowed for ESR measurements on bare oxides with varying polarities of oxide bias.

ESR measurements were performed at room temperature using a Bruker Instruments X-band spectrometer with a TE_{104} double microwave cavity and a calibrated weak pitch spin standard. Although the densities of E' defects per unit volume are quite high in some samples, the paramagnetic defect densities per unit area are low because the SiO_2 thickness is so small, resulting in relatively modest precision even with extensive signal averaging. Nevertheless, the signals were adequate for meaningful comparisons with accuracy better than a factor of two in absolute number and about +/- 10% in relative number. SDR measurements were made at room temperature on a custom-built X-band spectrometer and were calibrated using a strong pitch spin standard.

6.2 Results and Discussion

We find narrow ESR signals with zero crossing g values between g = 2.0004 and g = 2.0025 in most of the samples investigated. In Si/SiO_2 systems, narrow ESR lines with zero crossing g values in the 2.0004 to 2.0025 range have typically been linked to E' centers [35]. We find striking processing induced differences in the densities of the two E' defects.

Figure 6.1 compares ESR traces taken on three samples with identical sample area and spectrometer settings. All three samples involved 3nm of HfO_2 deposited on the EB ISSG SiO_2 interfacial layer. Sample (a) received no post-deposition anneal, sample (b) received both the 700°C and 1000°C N_2 anneals, and sample (c) had a 10nm thick TiN capping layer deposited prior to receiving both high temperature N_2 anneals. Although little appears in trace (a), trace (b) exhibits clear signals at g = 2.0036 and g = 2.0005 which are assigned to P_{b1} (g = 2.0036) like Si/dielectric interface traps and E_γ' (g = 2.0005) like oxide traps which are commonly observed in conventional Si/SiO_2 systems [35]. The sample (b) spectra represent defect densities of 7×10^{10} cm^{-2} and 4×10^{10} cm^{-2} for P_{b1} and E' respectively. Trace (c) exhibits a very strong signal at g = 2.0025 representing a defect density of 8×10^{11} cm^{-2}. (Note that, since the SiO_2 layer is only about 1nm thick, this corresponds to a volume density of about 10^{19} cm^{-3}.) In conventional Si/SiO_2 systems, signals with zero crossing g values near 2.002 have been linked to an E' variant, most often the E_δ' center [35]. It is not certain the signal observed here is due to an E_δ' center. However, it is fairly certain that the g = 2.0025 signal is due to <u>some</u> type of oxygen deficient silicon (E') defect. For this reason, the signal at g = 2.0025 will simply be referred to as an E' variant. Comparison of traces (a)

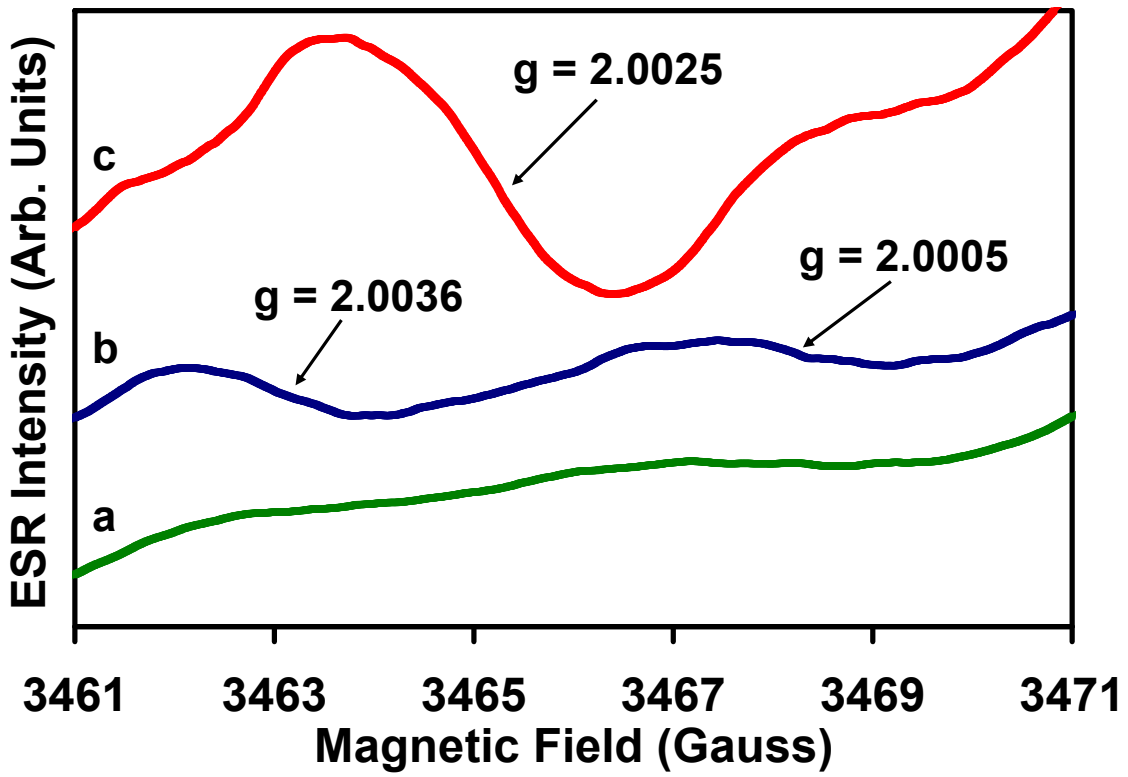

Figure 6.1: Comparison of three very similarly processed samples: (a) 3nm HfO_2 deposited on EB ISSG SiO_2, (b) a sample identical to (a) except that it received a 700°C and 1000° N_2 post-deposition anneal, and (c) a sample identical to (b) except that it had, in addition, a 10nm thick TiN cap deposited prior to N_2 annealing.

and (b) suggest that the high temperature anneal alone enhances the generation of E_γ' and P_{b1} like defects. Comparison of traces (b) and (c) suggests that the presence of a metal cap during the annealing process clearly has a very large effect on the defect chemistry of these samples, leading to a much higher density of oxygen deficient silicon centers.

Figure 6.2 compares three second derivative ESR traces also all taken on samples with identical areas and spectrometer settings. Samples (a) and (b) are "controls" in that (a) consists of the O_3 grown SiO_2 interfacial layer with no HfO_2 deposited, and (b) consists of a sample with the same O_3 grown SiO_2 interfacial layer with 3nm of near stoichiometric HfO_2. The sample from trace (c) involves the deposition of an oxygen deficient layer of HfO_2 (fabricated by significantly reducing the time of the O_3 oxidation cycle during the ALD process) on the 1.1nm chemical oxide film obtained by the O_3 treatment of the silicon substrate. There are no observable signals in traces (a) and (b) but trace (c) exhibits two clear signals at g = 2.0024 (E' variant) and g = 2.0005 (E_γ') with respective densities of $9 \times 10^{11} cm^{-2}$ and 2×10^{11} cm^{-2}. This suggests that the HfO_2 layer can remove oxygen atoms from the near Si/dielectric SiO_2 interfacial region.
We also observe E' variant defect spectra somewhat similar to those in the blanket HfO_2 samples using very sensitive SDR measurements on fully processed MOSFETs. Our SDR measurements were made on MOSFETs with HfO_2 based gates stacks nearly identical to the previously discussed HfO_2 blanket structures. The devices exhibit an SDR signal with a g value of $g \approx 2.0024$; a representative trace is shown in figure 6.3. These SDR signals are likely due to defects related to the g = 2.0025 defects seen with conventional ESR. (The difference in the measured g values 2.0029 versus 2.0025 is

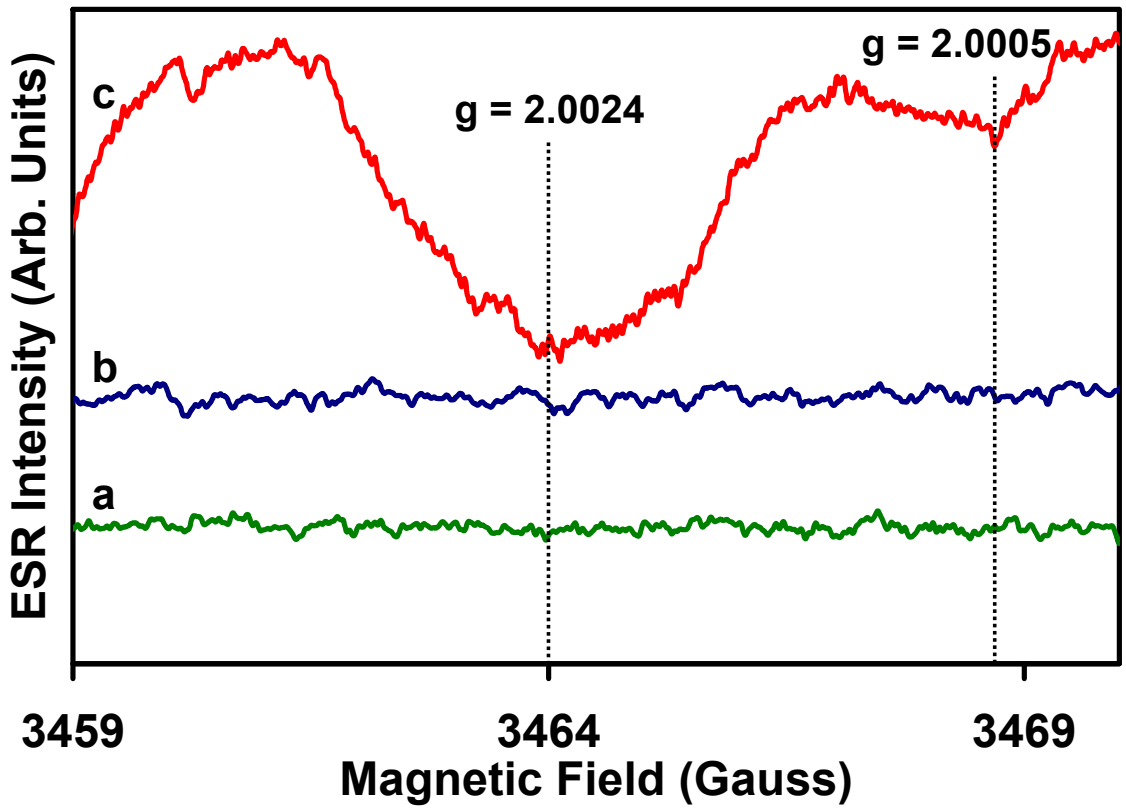

Figure 6.2: Three second derivative ESR traces of (a) control 1nm O_3 SiO_2, (b) 3nm HfO_2 deposited on 1nm O_3 SiO_2, and (c) oxygen deficient HfO_2 deposited on 1nm O_3 SiO_2. Note that the deposition of the oxygen deficient HfO_2 film grossly increases the densities of the two E' like signals.

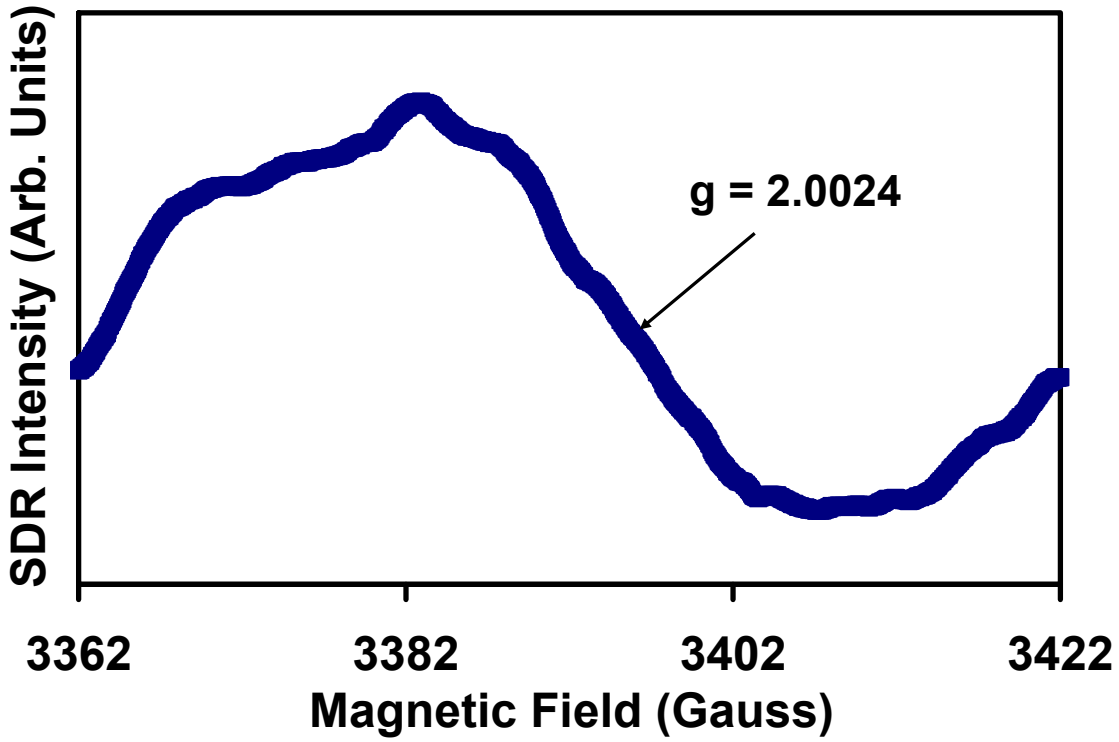

Figure 6.3: Representative SDR trace on a fully processed metal gate HfO_2 MOSFET. Note the appearance of a (much broader) SDR signal at a g value (2.0024) which is, within experimental error, equal to those observed in the conventional ESR measurements.

within experimental error.) The much broader SDR lines indicate that the defects are not identical. The broad lines may indicate that the defects observed in SDR are due to oxygen deficient silicons near a hafnium atom. Because hafnium nuclei are relatively large and outer shell electrons associated with hafnium atoms would have some *d* character, it is likely that a nearby hafnium atom would tend to broaden the SDR spectrum because of the likely large spin-orbit coupling effect.

The SDR observation is important for two reasons. (1) SDR is only sensitive to recombination center defects located at or very near the Si/dielectric interface [153], suggesting that these signals are due to defects very near the Si/dielectric interface (in the interfacial layer region). (2) SDR is only sensitive to electrically-active defects [37, 38, 153]. The simple fact that these g = 2.0024 defects can be observed with SDR indicates that they are electrically-active.

The observation of E' or E' like centers in the near Si/dielectric interfacial region is of considerable technological significance. A very thin "interfacial transition layer" dielectric is widely reported to be present in HfO_2 based MOS structures [88, 99]. The chemical nature and electronic properties of this layer are, as yet, poorly understood. The observation of E' centers in unstressed samples quite strongly suggests that the interfacial layer region is oxygen deficient and silicon rich. The presence of E' or E' like defects may also be an important reliability problem. The E' family of defects clearly dominates many performance limiting roles in conventional Si/SiO_2 technologies [35].

These results are consistent with suggestions in the recent literature. Scopel *et al.* [110] calculated that it is energetically more favorable to form oxygen vacancy defects in SiO_2 by compensation than in HfO_2. Wang *et al.* [111] argue that oxygen deficient HfO_2

absorbs oxygen from the SiO_2 interfacial layer creating oxygen vacancies in the SiO_2. Bersuker *et al.* [88] demonstrated that high temperature processing generates electrically-active defects in the interfacial layer of TiN/HfO_2 based MOSFETs, consistent with oxygen vacancy formation. Recently, Triplett *et al.* [93] also reported an ESR signal at g = 2.0024 in unstressed HfO_2/SiO_2 samples. Stesmans and Afanas'ev [116] report ESR measurements on Al_2O_3, ZrO_2, and HfO_2 on Si/SiO_2 structures. Although they did not observe E' centers in any samples prior to stressing, they found that vacuum ultraviolet irradiated ZrO_2/SiO_2 samples exhibit an order of magnitude more E' centers than either the Al_2O_3/SiO_2 or HfO_2/SiO_2 samples and noted that in HfO_2/SiO_2 samples, higher annealing temperatures resulted in an increase of vacuum ultraviolet generated signals at g = 2.0005 but a decrease of the signal at g = 2.0024.

As mentioned previously, studies from other groups and the work presented above on sample set 1 lacked adequate sensitivity to perform fairly extensive high-resolution ESR measurements on this interfacial layer defect in ultra-thin HfO_2 samples. In sample set 2, we have utilized simply processed Si/HfO_2 structures specifically designed to yield a strong spectra associated with the oxygen deficient silicon in the interfacial layer region (the defects associated with the $g \approx 2.0025$ spectra discussed above). The much stronger signal in these samples gave us the additional sensitivity required to perform fairly extensive ESR measurements including orientation dependence, oxide bias, and microwave saturation reported below.

Figure 6.4 illustrates a series of ESR traces taken with varying angles between the applied magnetic field and the (100) silicon surface normal. As the sample is rotated in the magnetic field, the line shape of the observed signal changes. The direction of the

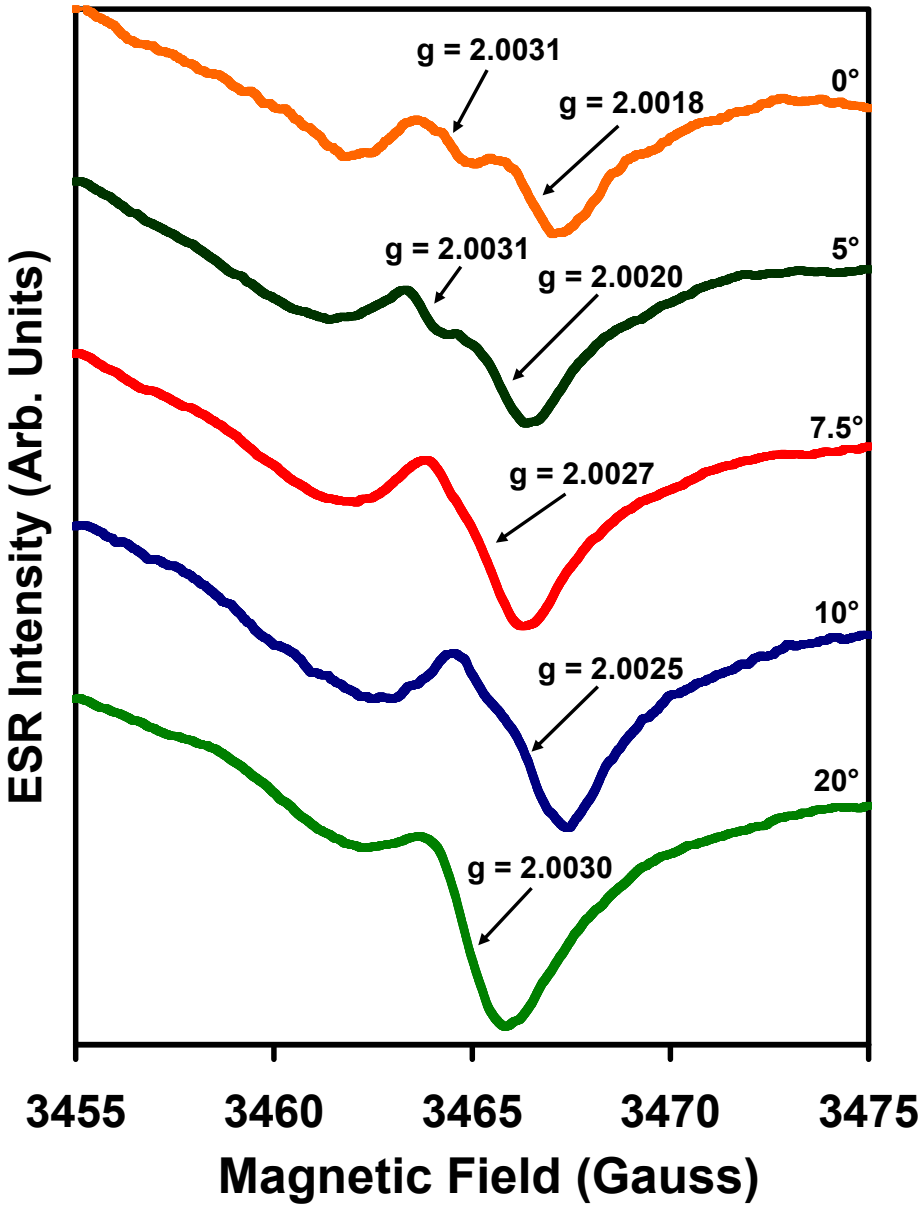

Figure 6.4: ESR vs. sample orientation. Note the change in line shape as the sample is rotated in the applied magnetic field. The defect cannot reside in a purely amorphous or non-textured polycrystalline matrix.

magnetic field matters. This shows that the observed defect cannot reside in a purely amorphous or non-textured polycrystalline matrix. If it did, the applied magnetic field orientation could not change the line shape. Based on this orientation data alone, the possibility that the defect resides directly at the Si/dielectric interface can be eliminated (Si/dielectric P_b centers are not the source of this spectra). If this were the case, the orientation dependence would exhibit a g tensor close to those typically observed for the P_b family of defects [92, 176]. It does not have such a g tensor. As mentioned previously, our group [55, 109] and at least two other groups [93, 116] have reported spectra similar to those reported here (narrow lines with $g \approx 2.002$ and with much lower resolution) in other Si/HfO_2 structures with much thinner (3-5nm) dielectrics. The authors of these studies have suggested that the defects involve oxygen deficient silicons and are located within the interfacial layer region. This is certainly a very strong possibility in this case as an oxygen deficient silicon back-bonded to oxygens located very close to the silicon substrate would almost certainly have a zero crossing $g \approx 2.002$ [35]. It should be noted that since we were forced to utilize somewhat different Si/HfO_2 films to obtain the required resolution and sensitivity, our observations only demonstrate with certainty that the defects are not in an amorphous matrix in these samples. Nevertheless, based on the highly similar ESR spectra, the results strongly suggest this would be the case in thin dielectrics as well.

Figure 6.5 illustrates a series of ESR traces taken with zero, +30V, and -30V applied gate bias. At zero volts bias (trace 1) we observe a signal with a zero crossing g = 2.0017 corresponding to a paramagnetic defect density of 3.1×10^{12} cm^{-2}. When identical measurements are made with positive (trace 2) or negative (trace 3) bias, the

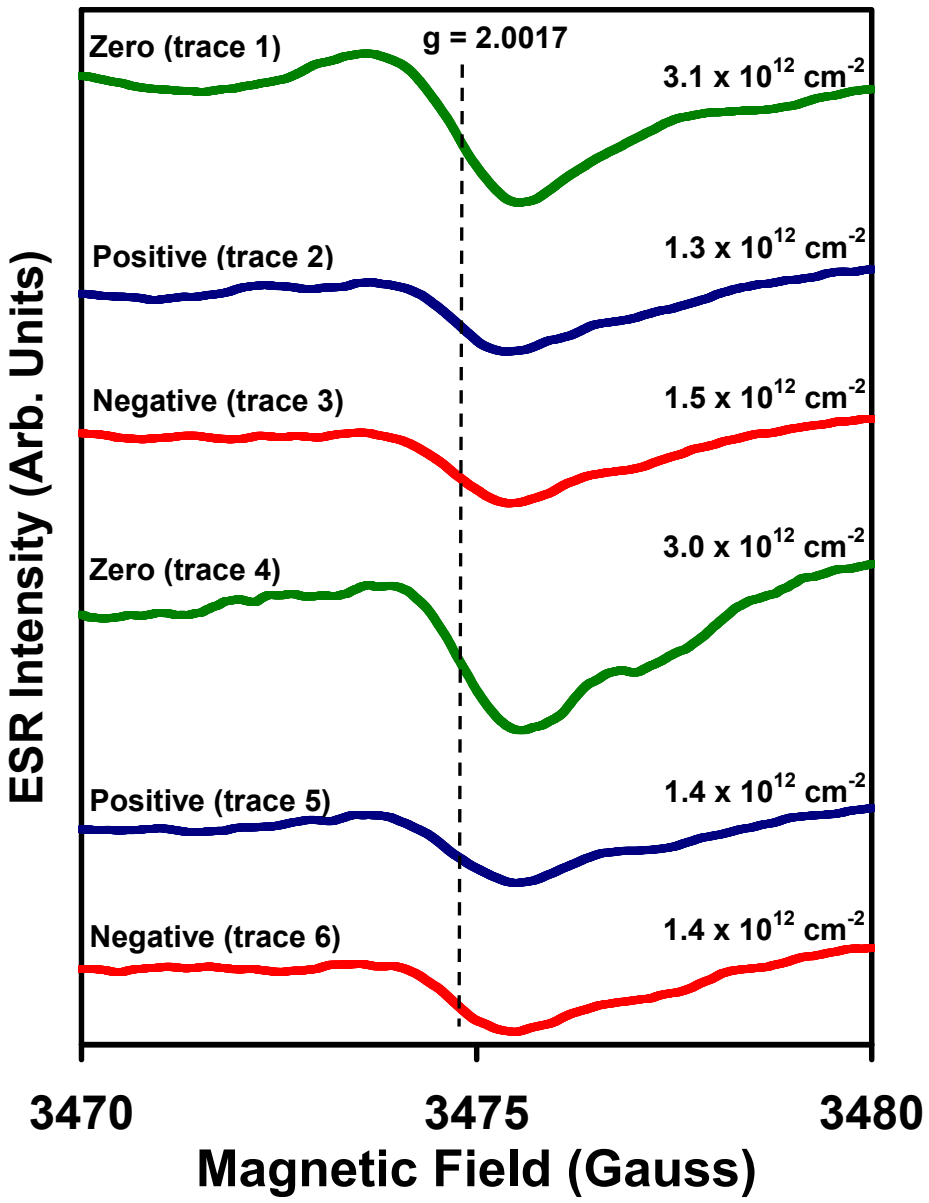

Figure 6.5: ESR vs. applied gate bias. Note the amplitude modulation as a result of biasing. The defect acts as both an electron and hole trap.

signal intensity decreases by about a factor of two (corresponding to paramagnetic defect densities of about 1.4 x 10^{12} cm^{-2} in both cases). Removing the applied bias (trace 4) restores the signal to its original amplitude. Traces 5 and 6 illustrate the factor of two decrease in signal amplitude with a repetition of the positive or negative bias. This repeatable signal amplitude modulation pattern caused by the applied bias shows that the defect acts as both an electron and hole trap "communicating" with the silicon Fermi level. This electronic response can be explained as follows (schematically illustrated in figure 6.6): without bias, the observed defects are neutral and have an odd number of electrons (paramagnetic and ESR active); when positive (negative) bias is applied the defect captures an electron (hole) rendering an even number of electrons on the defect site (diamagnetic and ESR inactive). This repeatable amplitude modulation response also shows that the defects must be located very close to the Si/dielectric interface. They must be close enough to "communicate" electrically with the silicon (they cannot be located in the bulk of the HfO_2). Following the arguments of Oldham *et al*. [177] for E' centers in pure SiO_2 (assuming pure SiO_2 should give a reasonable estimate), only defects within a few nanometers of the interface can participate in the charge capture during the time scale of our measurements (hundreds of seconds). This places the defect within the Si/dielectric interfacial layer region of these (rather thick) samples as previously reported [55, 93, 109, 116].

Figure 6.7 illustrates the results of a series of ESR measurements made with varying levels of applied microwave power on the sample defect and that of a commercially available E' standard (oxygen vacancy in pure SiO_2). As the power level is increased, the intensity of the E' standard increases until about 0.25mW. Beyond this,

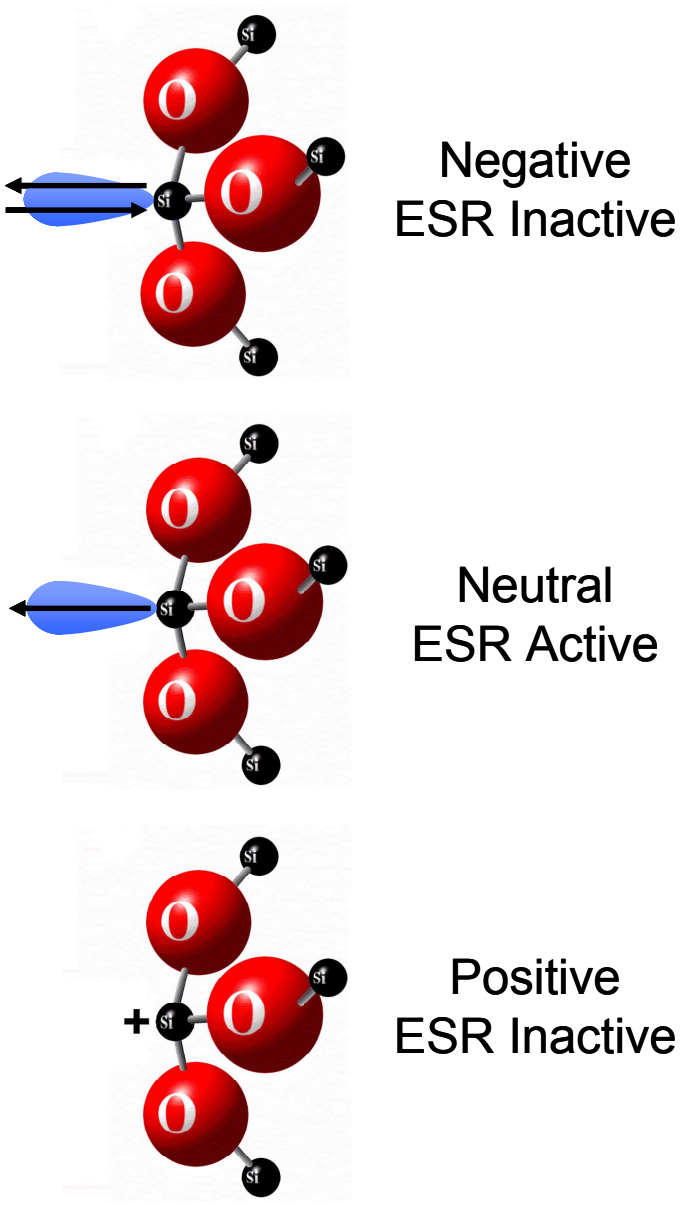

Figure 6.6: Schematic diagram illustrating the effects of gate biasing on the defects ESR response. Note that the defect may be more complex. (It likely involves a nearby hafnium atom.)

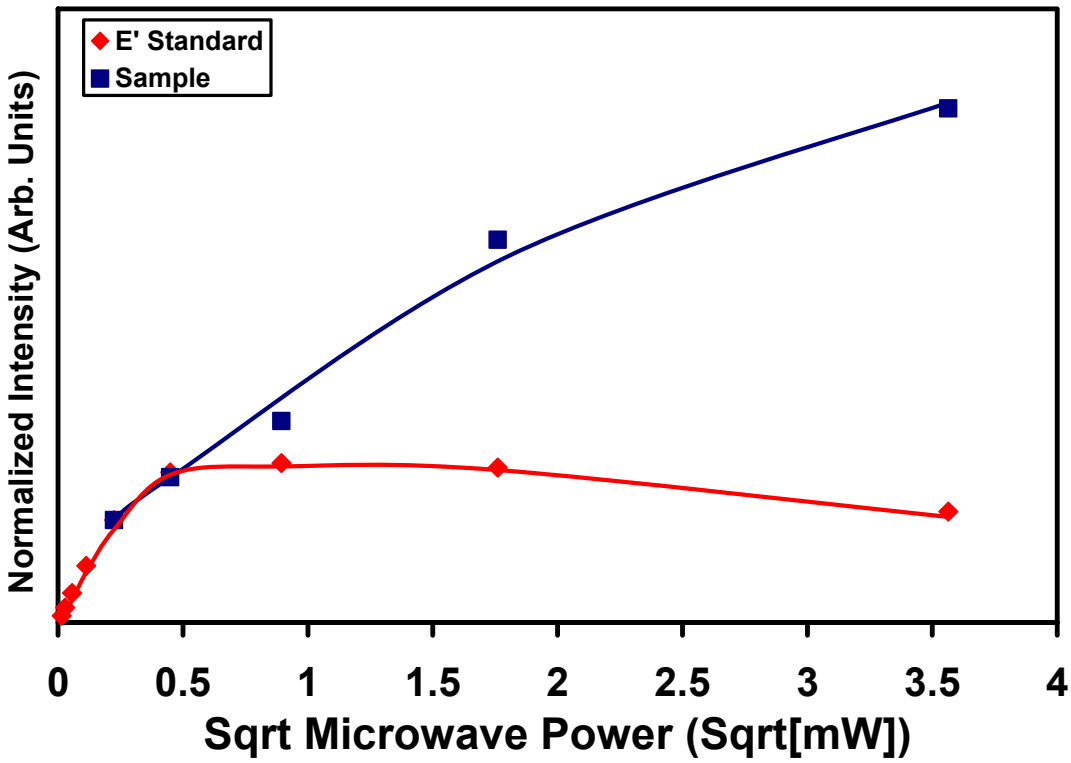

Figure 6.7: Normalized intensity for the sample and an E' standard. The sample defect's T_1 is much shorter than a conventional E' center suggesting a coupling to a hafnium atom.

the spin system is saturated and the signal intensity decreases with increasing microwave power. For the case of the HfO_2 sample, the signal intensity continues to increase without much saturation past 12.7mW. This indicates that, for the case of the HfO_2 samples, the room temperature spin lattice relaxation time, T_1, of the oxygen deficient silicon defect is much shorter than that of the E' standard [151, 178]. E' centers in pure SiO_2 generally exhibit quite long spin lattice relaxation times (of order 200μs) [178]. The significantly shorter T_1 observed here indicates that something not present in pure SiO_2 must be present near these defects. Paramagnetic sites involving transition metal impurities typically have quite short T_1 times at room temperature [151]. Since hafnium atoms are the only obvious impurity and are transition metal atoms, the results of figure 6.7 are at least strongly suggestive of some sort of (weak) coupling between an E' like site and a nearby hafnium atom. Van Benthem *et al.* [122] reported observations of individual hafnium atoms in the Si/dielectric interfacial layer of 3nm HfO_2 samples; this result is consistent with a possible coupling of E' centers and hafnium atoms in the interfacial layer.

6.3 Summary

In summary, we present results which strongly suggest that oxygen deficient silicon centers exist in the near Si/dielectric interfacial layer region of Si/HfO_2 structures. Our results suggest that the densities of oxygen deficient silicon centers (E' centers) in the interfacial layer region of HfO_2/SiO_2 based MOS devices can be very high and are strongly processing dependent. The very strong process dependence suggests that the number of these defects may be reduced to acceptably low levels with appropriate

processing chemistry. Additionally, we show that depositing oxygen deficient HfO_2 significantly increases the density of the oxygen deficient silicon centers in the interfacial layer region, supporting the arguments of Bersuker *et al*. who suggest that these defects are created through an HfO_2 oxygen leaching mechanism [88, 179]. The simple fact that these defect centers are observable with SDR indicates that they are indeed electrically-active and can participate in lifetime limiting reliability problems such as NBTI/PBTI and SILC.

Additional results on the specially prepared samples illustrate the power of utilizing ESR measurements and corona techniques in identifying the physical and electrical nature of trapping centers in HfO_2 based structures. Although our measurements required the use of specially prepared samples significantly different from ultra-thin ALD HfO_2 based device structures, very similar though much weaker defect spectra have been observed in samples much more closely resembling modern gate stacks [93, 109, 116]. This close similarity strongly suggests that our major findings (summarized below) could potentially be applicable to those structures. (1) These defect centers are not in a purely amorphous or non-textured polycrystalline matrix. (2) They are very near the Si/dielectric interface. (3) They are clearly electrically-active and act as both electron and hole traps. (4) They are likely coupled to hafnium atoms.

Since the spectra observed in this study are very similar to those observed in other studies, the defects involved are therefore likely present in a wide variety of HfO_2 device structures. Their presence could limit the performance and reliability of HfO_2 based MOSFETs.

Chapter 7

CONCLUSIONS

In this work, very sensitive magnetic resonance measurements have been utilized to study the atomic-scale defects associated with important device reliability problems in modern day microelectronics. Although this work provides significant insight into these problems, more work is needed to develop a complete and fundamental understanding.

In chapter 3, LV-SILC was investigated in ultra-thin nitrided SiO_2 MOS devices with a newly developed approach to SDT which we call ER-SDT. The ER-SDT technique offers the capability to directly link the analytical power of magnetic resonance with defect energy levels. We find that LV-SILC is dominated by K center defects in these devices, and by exploiting the very high capacitance of the thin dielectric and the much lower capacitance of the silicon depletion region, we approximate the collective K center DOS. Since K centers are thought to dominate trapping in pure Si_3N_4 and some nitrided SiO_2 dielectrics [48, 161, 162], our results are useful for not only LV-SILC, but other issues in which K centers participate (such as nitrided oxide NBTI).

In chapter 4, NBTI in pure SiO_2 was investigated with our newly developed on-the-fly ESR technique. The technique permits a recovery free glimpse into the dynamics of NBTI defect generation by allowing one to perform ESR measurements during NBTI stress. We find that E' centers are generated in Si/SiO_2 MOS structures when subjected to modest negative oxide bias at elevated temperature. Furthermore, these E' centers disappear, a recovery phenomenon, once the stressing conditions are removed. This result is consistent with NBTI being triggered by the tunneling of electrons from a neutral

E' center precursor to unoccupied valence band states, fully consistent with the ideas of Campbell *et al.* [29, 30], Lenahan *et al.* [31], and the recent two-stage model proposed by Grasser *et al.* [36].

In chapter 5, the role fluorine plays in suppressing NBTI in pure SiO_2 devices while doing little to suppress NBTI in nitrided SiO_2 devices was investigated using SDR measurements. Additional DC-IV measurements demonstrate a direct correlation between actual device parameter degradation (interface state generation) and magnetic resonance spectra. We find that the NBTI response of fluorinated SiO_2 devices and nearly identical pure SiO_2 devices is dramatically different. Our results strongly suggest that fluorine incorporation can suppress the generation of P_{b0} centers but does little to suppress P_{b1} center generation during NBTI stressing. That is, fluorine can effectively passivate P_{b0} center precursors, but much less effectively passivates P_{b1} center precursors. Thus, P_{b1} centers dominate the NBTI response of fluorinated SiO_2 devices. Since these defects have significantly different DOS [168], our results may prove useful in modeling NBTI response in these dielectrics. Additionally, our results suggest a coupling between P_{b1} centers and nearby fluorine atoms. Lastly, our results provide a fundamental reason that fluorine incorporation does little to suppress NBTI in nitrided SiO_2 devices; NBTI in nitrided SiO_2 devices is not dominated by interface state generation but rather near interface K center defects [20, 40, 48]. It is likely that fluorine cannot passivate the K center precursors.

In chapter 6, interfacial layer region defects in Si/HfO_2 based MOS structures were studied using conventional ESR and SDR measurements. We find that oxygen deficient silicon centers (E' centers) can be present in very high densities in the SiO_2 like

interfacial layer region of these structures. Conventional ESR measurements on a variety of essentially state-of-the-art HfO_2 films on silicon demonstrate the very strong processing dependence of the interfacial layer defects. SDR measurements on fully processed HfO_2 MOSFETs demonstrate that these interfacial layer defects are electrically-active and can thus limit the performance of these devices. Our results support and are fully consistent with the idea that the deposition of HfO_2 on a thin SiO_2 interfacial layer will create these defects through an oxygen leaching process [88, 99, 179]. Additional conventional ESR measurements on specially prepared HfO_2 dielectrics demonstrate that the interfacial layer defects are not in a purely amorphous matrix , are located very near the Si/dielectric interface, are clearly electrically-active and can act as both electron and hole traps, and they are likely coupled to hafnium atoms. Since the spectra observed in this study are very similar to spectra observed in several other studies [93, 109, 116], the interfacial layer defects identified here are likely present in a wide range of HfO_2 device structures and thus potentially play an important role in limiting the performance and reliability of HfO_2 MOSFETs.

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APPENDIX: NON-TECHNICAL ABSTRACT

The most important building block of microelectronics is an electronic switch called the metal-oxide-silicon field-effect-transistor (MOSFET). By applying a voltage, current flowing through the MOSFET can be turned on or off. This binary operation (on or off) is the basis of modern computing. If many MOSFETs are hooked together in a certain way, logic operations can be performed which can process information. Modern microprocessors can easily contain hundreds of millions of individual MOSFETs all working together to accomplish the computer user's desired task.

Over the last several decades, our society has witnessed the incredible growth and global impact of the microelectronics industry. This is largely due to the availability of new hardware which performs faster than its predecessors just a few years old. The key idea behind making ever faster hardware is to decrease the size of the individual MOSFETs. By making the MOSFETs smaller, they can be turned on and off faster, and more MOSFETs can be crammed into a given area.

Unfortunately, the shrinking of MOSFETs over the years has exacerbated several reliability and fundamental physical limitations. These problems have threatened to halt the development of future increases in computing power. Despite many years of work (in some cases decades), many of these problems are not yet fully understood. In order to preserve the trend of faster computing, a fundamental understanding of these issues must be a top priority.

The work reported herein investigates two of the most important reliability problems in modern microelectronics called the negative bias temperature instability

(NBTI) and stress induced leakage current (SILC). Using highly sensitive magnetic resonance techniques, this work has investigated the atomic-scale imperfections associated with NBTI and SILC. By understanding the root causes, this work attempts to develop a fundamental understanding of these problems with the hope that they can be ameliorated in future generations of hardware.

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