The Pennsylvania State University

The Graduate School

College of Engineering

**ATOMIC-SCALE DEFECTS INVOLVED IN THE NEGATIVE BIAS TEMPERATURE**

**INSTABILITY IN SIO$_2$ AND PLASMA-NITRIDED OXIDE BASED pMOSFETs**

A Thesis in

Engineering Science and Mechanics

by

Jason P. Campbell

Submitted in Partial Fulfillment
of the Requirements
for the Degree of

Doctor of Philosophy

August 2007

The thesis of Jason P. Campbell was reviewed and approved* by the following:

Patrick M. Lenahan
Distinguished Professor of Engineering Science and Mechanics
Thesis Adviser
Chair of Committee

S. Ashok
Professor of Engineering Science

Jerzy Rużyłło
Professor of Electrical Engineering

Michael T. Lanagan
Associate Professor of Engineering Science and Mechanics

Anand T. Krishnan
Reliability Engineer – Texas Instruments
Special Member

Judith A. Todd
Professor of Engineering Science and Mechanics
P.B. Breneman Head of the Department of Engineering Science and Mechanics

*Signatures are on file in the Graduate School.

**ABSTRACT**

This study examines the atomic-scale defects involved in a metal-oxide-silicon field-effect-transistor reliability problem called the negative bias temperature instability (NBTI). NBTI has become the most important reliability problem in modern complementary-metal-oxide-silicon technology. Despite 40 years of research, the defects involved in this instability were still undetermined prior to this work. We combine DC gate-controlled diode measurements of interface state density with two very sensitive electrically detected magnetic resonance measurements called spin-dependent recombination and spin-dependent tunneling. An analysis of these measurements provides an identification of the dominating atomic-scale defects involved in NBTI in pure $SiO_2$- and plasma-nitrided oxide-based devices. (The fundamental mechanism behind NBTI's enhancement due to the addition of nitrogen had previously been a mystery.)

Our results in pure $SiO_2$ devices indicate an NBTI mechanism which is dominated by the generation of $P_{b0}$ and $P_{b1}$ interface state defects. ($P_{b0}$ and $P_{b1}$ are both silicon dangling bond defects in which the central silicon is back bonded to three other silicon atoms precisely at the $Si/SiO_2$ interface.) This observation is consistent with what most NBTI researchers have assumed. However, our observations in plasma-nitrided oxide devices contradict what most NBTI researchers had previously assumed.

We demonstrate that the dominating NBTI-induced defect in the plasma-nitrided devices is fundamentally different than those observed in pure $SiO_2$-based devices. Our measurements indicate that the new plasma-nitride NBTI-induced defect's physical location extends into the gate dielectric. The defect participates in both spin-dependent recombination and spin-dependent

tunneling. Our spin-dependent recombination results strongly indicate that the plasma-nitrided defect has a density of states which is more narrowly peaked than that of $P_b$ centers and is near the middle of the band gap. The high sensitivity of our spin-dependent tunneling measurements allow for an identification of the physical and chemical nature of this defect through observations of $^{29}$Si hyperfine interactions. The defects are silicon dangling bonds in which the central silicon is back bonded to nitrogen atoms. We call these NBTI-induced defects $K_N$ centers because of the similarities to the K centers observed in silicon nitride. (The silicon nitride K center is also a silicon dangling bond in which the silicon atom is back bonded to nitrogen atoms.) The defect identification in plasma-nitrided devices helps to explain (1) NBTI's enhancement in plasma-nitrided devices, (2) conflicting reports of NBTI induced interface states and/or bulk traps, and (3) fluorine's ineffectiveness to reduce NBTI in plasma-nitrided devices. Our measurements also allow for observations of the atomic-scale defects involved in NBTI recovery.

# Table of Contents

**LIST OF FIGURES**

## LIST OF TABLES

# LIST OF ABBREVIATIONS

CMOS          complementary metal-oxide-silicon

DC-IV         direct current gate-controlled diode recombination current versus voltage

$D_{it}$      interface state density ($\#/cm^2$ eV)

EDMR          electrically-detected magnetic resonance

EOT           equivalent oxide thickness

ESR           electron spin resonance

FAMOS         floating-gate avalanche-injection metal-oxide-silicon

$I_{SUB}$     device substrate current

KSM           Kaplan, Solomon, Mott model for spin-dependent recombination

MNOS          metal-nitride-oxide silicon

NBTI          negative bias temperature instability

NBTS          negative bias temperature stress

nMOS          n-channel metal-oxide-silicon

pMOS          p-channel metal-oxide-silicon

pMOSFET       p-channel metal-oxide-silicon field-effect-transistor

PNO           plasma-nitrided oxide

SRH           Shockley, Read, Hall model for recombination

SDR           spin-dependent recombination

SDT           spin-dependent tunneling

UIS           uninterrupted stress

$V_T$         device threshold voltage

$V_F$         bias applied to the source-drain to substrate junction

# ACKNOWLEDGMENTS

First and foremost, I would like to thank Dr. Patrick Lenahan for giving me the opportunity to work in his laboratory. His patience and guidance is directly responsible for every educational and professional achievement I have attained. All of my research abilities are due entirely to his influence. Without his watchful eye, I would not be the researcher I am today. He is the best scientist I have ever met.

I would also like to thank my committee members, Dr. Ashok, Dr. Rużyłło, Dr. Lanagan, and Dr. Krishnan, for excellent guidance throughout my graduate and undergraduate studies.

I would not be able to deal with the rigors of graduate school without my contemporaries in Dr Lenahan's laboratory: Andy Kang, Nate Bohna, Dave Meyer, Morgen Dautrich, Shane Yerkes, Jason Ryan, Corey Cochrane, Aaron Rape, Brad Bittel, and Ted MacDonald. You have all been in the trenches with me, at some point or another, and for that I am grateful.

The quality and impact of this research has been greatly enhanced by the patience and guidance of both Drs. Anand Krishnan and Srikanth Krishnan at Texas Instruments. They have had an amazing impact on this work. I am grateful for all of their comments, suggestions, and friendship.

I want to thank Drs. Phil Kraus and Khaled Ahmed at Applied Materials Inc. for the opportunity to work in their research group. They have provided excellent guidance and friendship throughout my graduate studies.

I want to thank my parents for being constant supporters of all my endeavors. My greatest accomplishment in life will be to continually make them proud.

Lastly, I want to thank my wife, Gwennie. She has been my biggest supporter and is the love of my life. Her understanding and support has made all of my graduate work possible. I am forever grateful that I have found her and cannot wait to start the next chapter of our lives together.

**Chapter 1**

**INTRODUCTION**

One of the most remarkable characteristics of the Si/SiO$_2$ system is that it displays an outstanding reliability response. Transistors fabricated using the Si/SiO$_2$ system can be scaled to extremely small dimensions to enhance the performance while still maintaining high reliability. However, aggressive gate oxide scaling, less aggressive operating voltage scaling and the addition of nitrogen to the gate dielectric have exacerbated a major reliability concern called the negative bias temperature instability (NBTI). NBTI manifests itself as a negative threshold voltage (V$_T$) shift and degradation in drive current in pMOSFET devices subject to negative gate biases at elevated temperatures. These NBTI-induced parameter shifts eventually lead to circuit failure. Predictions of NBTI-limited lifetimes must be accurate to ensure that the circuit will function for a known period of time. The accuracy of the NBTI lifetime predictions depend on a detailed understanding of the NBTI mechanism. Despite nearly forty years of research, a fundamental understanding of NBTI is still incomplete.

This incomplete understanding involves, among other things, widespread disagreement regarding the origin of the threshold voltage shift (interface states and/or bulk traps).[1-5] Defining the roles of NBTI-induced interface states and/or bulk traps has proven difficult, in part, because some of the NBTI damage is not permanent.[6,7] Some of the damage recovers very quickly[6,7], with significant recovery occurring in microseconds after the negative bias temperature stress (NBTS) is removed.[8] This rapid recovery is difficult to capture using conventional electrical characterization techniques and often obscures the relative balance of interface states and/or bulk traps.[5,9] A particularly important issue is the effect of the addition of nitrogen to the SiO$_2$ gate dielectric. Nitrogen is often added to the gate dielectric. The nitrogen increases the dielectric

constant, allowing a thinner dielectric to provide an equivalent capacitance; this reduces the gate

leakage current and allows for further scaling. Also, in p-channel devices, the addition of

nitrogen blocks boron (used for the poly-silicon gate doping) from penetrating into the oxide.

Unfortunately, the addition of nitrogen to the gate dielectric also greatly increases NBTI

damage.[10,11] Nitridation is thought to somehow enhance NBTI by altering the relative densities

of interface states and/or bulk traps.[5,12] Although the enhancement is almost universally

observed, a fundamental understanding of the nitrogen-induced NBTI enhancement on interface

state/bulk trap generation is still undetermined.

In this work, we have utilized a unique combination of electrical and magnetic resonance

measurements to study the atomic-scale defects involved in NBTI. We employ DC gate-

controlled diode recombination current (DC-IV)[13,14] measurements to monitor NBTI-induced

changes in device interface state density ($D_{it}$). These electrical measurements are combined with

very sensitive electrically-detected magnetic resonance (EDMR) measurements which allow for

the identification of specific NBTI-induced atomic-scale defects. The combination of these two

types of measurements (DC-IV and EDMR) provides a direct correlation between the NBTI-

induced electrical damage and the generation of specific atomic-scale defects.

Magnetic resonance techniques are the only measurements with the analytical sensitivity

and power to examine the physical and chemical nature of the defects involved in NBTI.[5,12,15]

One of these magnetic resonance techniques, conventional electron spin resonance (ESR), was

first utilized by Fujieda *et al.* to examine the atomic-scale defects involved in NBTI.[16] However,

their experiments involved large area (~1cm$^2$) blanket dielectric capacitor structures on p-type

substrates.[16] We have circumvented[17-21] the sample requirements of conventional ESR (large area

and simple processing) by utilizing two very sensitive (EDMR) techniques called spin-dependent

recombination (SDR) and spin-dependent tunneling (SDT). These measurements rely on ESR-induced changes in device currents. Thus, the atomic-scale defects identified in these measurements are directly linked to NBTI-induced degradation in fully processed devices. It should be noted that our SDT measurements represent only the third time this technique has been reported and the first time this technique has been utilized to study reliability problems.

This work has resulted in the development of a fundamental understanding of the atomic-scale defects involved in NBTI in both pure-$SiO_2$ and plasma-nitrided oxide (PNO) based devices. In the pure-$SiO_2$ devices, our results indicate that NBTI is dominated by the generation of $P_{b0}$ and $P_{b1}$ interface state defects. $P_{b0}$ and $P_{b1}$ defects are both interfacial silicon dangling bond defects in which the central silicon is back bonded to three other silicon atoms precisely at the $Si/SiO_2$ interface.[22-25] The observation of NBTI-induced $P_{b0}$ and $P_{b1}$ defects is relatively consistent with what most NBTI experts assumed (interface state generation via hydrogen depassivation of silicon dangling bonds at the $Si/SiO_2$ interface). These results are also consistent with much of NBTI "reaction-diffusion" literature.[1,5,26,27] The reaction-diffusion model predicts that NBTI is dominated by a hydrogen depassivation of $P_b$ centers at the $Si/SiO_2$ interface and the reaction rate is controlled by hydrogenic diffusion away from the interface.[1,5,26,27]

However in PNO devices, our observations were inconsistent with what most NBTI experts assumed. Our results clearly show that, in these devices, *NBTI generates a new defect* (not $P_{b0}$ or $P_{b1}$).[18,20] Extensive measurements have allowed for a detailed examination of this new defect's: (1) physical location within the gate stack, (2) simultaneous participation in spin-dependent recombination and spin dependent tunneling processes, (3) density of states, (4) and physical and chemical identity. Our observations help provide an explanation for NBTI's nitrogen enhancement and also help explain the conflicting reports of the dominance of NBTI-

induced interface states and/or bulk traps. This defect identification also helps explain fluorine's ineffectiveness in reducing NBTI in nitrided devices.

This work represents a significant contribution to the NBTI field. It is the first comprehensive experimental examination of the atomic-scale mechanisms governing NBTI in SiO$_2$ and PNO devices. Our results have allowed for the validation of some NBTI models and call into question others. Our NBTI results are thoroughly discussed throughout chapters 3-5 of this thesis. The remainder of this chapter provides a short explanation of the origins of the NBTI-induced parameter shifts as well as a brief history of the NBTI phenomenon.

## 1.1 The Origins of NBTI

An examination of the simplest transistor operation equations is useful to illustrate the origins of the characteristic NBTI $V_T$ shift. The threshold voltage of a pMOSFET is given by [28]

$$V_T = V_{FB} - 2\phi_F - \frac{|Q_{SC}|}{C_{ox}}$$

(1.1)

where $V_{FB}$ is the voltage required for the flat band condition, $\phi_F$ is the difference between the bulk Fermi level and intrinsic level, $|Q_{SC}|$ is the magnitude of the maximum space charge in the depletion region, and $C_{ox}$ is the oxide capacitance. $|Q_{SC}|$ and $V_{FB}$ are given by

$$|Q_{SC}| = \left|\sqrt{4\varepsilon_s \phi_F q N_D}\right|$$

(1.2)

$$V_{FB} = \phi_{MS} - \frac{Q_{ot}}{C_{OX}} - \frac{Q_{it}}{C_{OX}}$$

(1.3)

where $\varepsilon_s$ is the permittivity of silicon, q is the electronic charge, $N_D$ is the substrate doping density, $\phi_{MS}$ is the metal semiconductor workfunction difference, $Q_{ot}$ is the oxide fixed charge density, and $Q_{it}$ is the interface trapped charge density. Combining (1.1)-(1.3) yields expression (1.4) for the threshold voltage of a pMOSFET [28]

$$V_T = \phi_{MS} - \frac{Q_{ot}}{C_{OX}} - \frac{Q_{it}}{C_{OX}} - 2\phi_F - \frac{\left|\sqrt{4\varepsilon_s\phi_F qN_D}\right|}{C_{OX}} \tag{1.4}$$

Assuming that the substrate doping ($N_D$) and the oxide capacitance ($C_{OX}$) are both constant during a given negative bias temperature stress (NBTS) condition, the observed shift in threshold voltage ($\Delta V_T$) must arise from a change in the numbers of oxide and/or the interface trapped charges ($\Delta N_{ot}$ and $\Delta N_{it}$) [28]. This simple examination is in agreement with a very large body of NBTI research which has shown that oxide ($N_{ot}$) and interfacial defects ($N_{it}$) are indeed responsible for the NBTI-induced degradation. However, the role of each type of defect is still actively debated.

In an NBTI measurement, a device is subject to a negative bias temperature stress (NBTS) condition which is designed to approximate "real world" circuit operation at an accelerated rate (higher voltage and temperature). A typical NBTI characterization subjects pMOSFETs to various NBTS conditions while monitoring shifts in device parameters ($\Delta V_T$ or $\Delta I_d$) or defect densities ($\Delta N_{ot}$ or $\Delta N_{it}$) as a function of stressing time. These degradation trends can then be used to empirically predict the NBTI-limited circuit lifetimes. The poorly understood details that govern these lifetime extractions are an extremely important barrier to the research and development of integrated circuit technology.

## 1.2 A Brief History of the NBTI Phenomenon

Surprisingly, NBTI is not a newly observed phenomenon. In 1967, Deal *et al.* provided the first report on the "fast state" ($N_{it}$) and "slow state" ($N_{ot}$) positive charge build-up in MOS devices subject to negative gate biases at elevated temperatures (300-450°C).[29] Deal noted that this charge build-up was "not an extraneous contamination such as sodium ions, but (was) a phenomenon intrinsically connected with the Si/SiO$_2$ interface."[29] This positive charge build-up was even shown to impact very early floating-gate avalanche-injection metal oxide silicon (FAMOS) read-only memory in 1971.[30] The observations in FAMOS memory were consistent with those of Deal in that the charge decay "corresponded to that of positive-charge buildup at the Si/SiO$_2$ interface."[30] Further experimental evidence of interface state and oxide charge generation after NBTS (250-300°C) was reported throughout the early 1970's.[31,32]

The first comprehensive effort to understand and model the NBTS-induced positive charge buildup was by Jeppson *et al.* in 1977.[26] In this pioneering article, the authors utilize split-CV measurements to monitor the oxide charge and interface state generation at NBTS conditions (25-125°C, 4-7MV/cm) consistent with metal-nitride-oxide-silicon (MNOS) operating conditions [26] rather than the higher temperatures explored in earlier studies.[29-32] Jeppson *et al.* suggest that the NBTI-induced generation of interface traps "cannot be formed unless the atomic structure is changed at the interface".[26] A reaction-diffusion model was proposed to explain their observations.[26] In their model, an chemical reaction takes place at the Si/SiO$_2$ interface in which a hydrogenous species is depassivated from a silicon atom at the interface and leads to the formation of (1) an interface state (2) an oxide charge and (3) a hydroxyl group.[26] The hydroxyl group is assumed to diffuse through the oxide and limit the extent to which the interface reaction

proceeds.[26] Jeppson's analysis leads to a power law time dependence ($t^n$) of the generation of interface states with n = ¼.[26] Jeppson also noted that the NBTI damage was only semi-permanent and slowly recovered when the NBTS was removed.[26] The model fit their data as well as the data of many other contemporary researchers. Despite some ambiguity in the exact mechanisms involved in Jeppson's model, it became accepted as the leading explanation for NBTI in the $SiO_2$-based devices of the time. In fact, the power law (n = ¼) dependence on transistor parameter shifts became the distinguishing feature denoting NBTI.

Due to the adoption of faster, relatively NBTI-immune, nMOS device technology in the late 1970's and early 1980's, NBTI research slowed almost to a halt.[1] In the late 1980's and early 1990's NBTI remerged as a reliability issue with the adoption of CMOS integrated circuits.[1] In 1991, Blat *et al.* re-examined the NBTI phenomenon and were the first to argue that NBTI requires holes at the interface.[33] Also in 1991, Doyle *et al.* examined both NBTI and hot carrier (HC) reliability degradation.[34] They found that the major difference between the two phenomena is the temperature activation.[34] At high temperatures, HC degradation becomes less important due to interactions between hot carriers and phonons while the effects of NBTI become more important.[34] However, at that time, HC degradation was the major reliability concern and NBTI was viewed as a minor problem.

At the turn of the century, NBTI became a subject of renewed interest. La Rosa *et al.* [35] and Thewes *et al.* [36] further examined Doyle's work on NBTI and HC degradation. The work of both groups strongly suggested that, due to CMOS scaling, NBTI's importance would increase in future generations of integrated circuits.[35,36] A series of papers in 1999 and 2000 by Kimizuka *et al.* reintroduced NBTI as a major reliability concern for the very near future.[10,11] In these studies, Kimizuka *et al.* demonstrated that the common practice of incorporating nitrogen into the gate

oxide greatly enhances NBTI degradation in ultrathin gate dielectrics.[10] This creates quite a dilemma because the nitrogen incorporation, which retards boron penetration, reduces gate leakage, and improves hot carrier immunity also acts to enhance NBTI degradation [10,11].

With a renewed focus on NBTI, the reliability literature was flooded with various (sometimes poorly thought out) theories to explain the origins of NBTI. Several studies linked NBTI to boron penetration in the gate dielectric,[37,38] but this was later proved unlikely.[39] Some research even linked NBTI to ultrathin gate oxide tunneling currents;[38,40] however, this conjecture was also found to be incorrect.[11,41,42] In the initial scramble to reduce NBTI problems, reliability engineers' first empirical process modifications involved the same tricks used to abate HC damage. Several studies showed that fluorine incorporation suppressed NBTI degradation.[41,43-47] However, the incorporation of too much fluorine was found to enhance boron penetration, which helps NBTI, but sacrifices device performance.[47] Deuterium post-oxidation anneals were also found to reduce NBTI.[10,16,48] Since the deuterium anneal replaces interfacial Si-H bonds with stronger Si-D bonds, the NBTI improvement suggests a link between NBTI degradation and Si-H bond dissociation.[10,16,49-51] Despite a large volume of work on the origins of the nitrogen-enhanced NBTI effect,[4,5,10,16,39,43,47,52-61] the enhancement mechanism has still proved quite elusive.

The reliability community was recently upended again by several examinations of NBTI recovery. Although Jeppson[26] had shown that the NBTI damage does exhibit recovery, Ershov[6] *et al* and many of the 2003 International Reliability Physics Symposium (IRPS) proceedings papers[62-65] clearly showed that NBTI recovery takes place over a very short time scale. The consequence of this "recoverable" NBTI degradation calls into question the validity of much of the previous NBTI work. It was shown that recovery was "contaminating" all of the

contemporary NBTI measurements and analysis.[6] Most NBTI characterizations had involved periodic interruptions of the NBTS to make either a threshold voltage or drain current measurement. The measurement contamination occurs during these stress interruptions and alters the measured parameter shifts. More importantly, if the time delay between stress and measure is not controlled, the NBTI lifetime predictions can be quite inaccurate.[6] Consequently, NBTI recovery has become a major topic in the last few years.

Rangan *et al.* were the first to explore the recovery effect using the uninterrupted stress (UIS) technique.[7] In the UIS measurement, a small bias is applied to the drain, the gate is held at the stressing voltage, and the drain current is monitored as a function of time ($I_{d,lin}$ conditions).[7] In this technique, the stress and measurement are performed simultaneously; hence, there is no delay confounding the characterization.[7] Rangan *et al.* also showed that the recovery mechanism has an associated temperature activation.[7] A device subject to NBTS at room temperature or below will recover nearly to its original state; while a device stressed at a higher temperature displays less recovery.[7] Rangan proposed that the NBTI degradation is due to interface states ($N_{it}$) and that recovery involves the repassivation of Si-H bonds at the interface.[7] The higher temperature NBTS was thought to  harden or "lock-in" the degradation by allowing the depassivated hydrogenous species to either (1) diffuse farther away from the interface or (2) form a stable hydrogenous species unavailable for repassivation.[7] The recovery effect, while perplexing in origin, served as a circuit reliability lifetime extension.[2,5-7,63,66-68] Since recovery takes place very quickly after stress removal, AC circuit recovery during normal operation is possible. The NBTI breakthroughs of 2003 not only anointed NBTI as *the* major reliability problem in modern device structures, but also reminded most of the community that a fundamental understanding is lacking.[69]

The challenge of recovery as a metric, involves it's characterization, and it's implications to "real world" circuit operation. Many authors have altered their techniques to either minimize measurement delay[3,7] or, at the very least, keep the delay constant[5,6] (which inserts a systematic error). The details of the recovery mechanism are still hotly debated. There are essentially two factions of researchers that believe recovery is due to either interface state ($N_{it}$) repassivation[1,2,5,7,60,65-67,70-74] or fixed oxide charge ($N_{ot}$) annihilation via hole de-trapping events.[3,4,75-79] It has been suggested that this discrepancy is due to measurement delay;[72] however, a solid explanation for the disparity is yet to be established. The various nitrogen incorporation techniques have also compounded this disagreement because the addition of nitrogen is known to create $N_{ot}$.[1,4,59,78] Recently, researchers have been able to circumvent recovery and find that the NBTI degradation follows a power law with exponent n=1/6.[2] Subsequent (recovery-free) reports have reported a nearly universal n=1/6 power law time dependence.[5,8,9]

Recent work has shown that the stressing conditions must be chosen carefully so as to not involve secondary mechanisms.[70,73,80-82] NBTS at excessive gate bias or temperature has been shown to generate an increased rate of $N_{ot}$, due to substrate hole injection through impact ionization.[70,73,80-82] The increased $N_{ot}$ generation leads to erroneously high power law time slopes (n) and further complicates lifetime extraction and confounds comparisons between different research groups.[70,73,80-82]

The newest NBTI literature also includes a renewed modeling effort and an emphasis on NBTI-induced $N_{it}$. Most modeling efforts explore variations of the original reaction-diffusion theory put forth by Jeppson[26] and later refined by Ogawa.[27] The modified reaction-diffusion model assumes that the NBTI threshold voltage shift is due almost entirely to the generation of

Si/SiO$_2$ interface states by the hydrogenic depassivation of Si-H bonds.[1,2,26,27] The degree to

which this reaction occurs is limited by the diffusion of the hydrogenic species away from the

interface.[1,2,26,27] It is thought that the interface state generation process is catalyzed by the capture

of inversion layer holes at the Si/SiO$_2$ interface.[1,83,84] The hole capture is thought to weaken Si-H

bonds and aid in Si-H dissociation.[1,83,84] Despite the fact that this important catalyzing step is

often unquestioningly accepted, the hole capture mechanism is often ignored in much of the

reaction-diffusion literature.[1,53,57,82,85,86] The hydrogenic species that is liberated from the

interface is also a topic of debate. Quite a few researchers model this phenomenon with the Si-H

dissociation involving a hydrogen ion (H$^+$) or proton.[57,86-88] Despite a large body of literature that

invokes H$^+$ species, this idea has been refuted by several studies.[1,2,5,7,27,74,89] The n=1/6 power

law dependence (which is nearly universally observed when recovery is minimized) is explained

within the reaction-diffusion framework by invoking a <u>neutral</u> molecular (H$_2$) or atomic

hydrogen species [1,2,5,7,27,66,67,70,73,80-82]. NBTI recovery is also predicted within this framework as

the reverse of the Si-H dissociation in which the hydrogenic species repassivates the interface

states (N$_{it}$) [1,2,5,66,67,70]. This model fits quite well with the contemporary (no measurement delay)

data.  By virtue of its starting assumptions, this model also supports the idea that interface states

(N$_{it}$) play dominating roles in NBTI degradation and recovery [1,2,5,66,67,70].

Other researchers believe that NBTI is not explained by the reaction diffusion theory.[4,78]

Instead, they propose that the threshold voltage shift is due to the generation of both interface

states as well as bulk traps.[4,78] In this model, there is also the assumption that interfacial Si-H

bond depassivation is catalyzed by an inversion layer hole capture event.[4,78] However, in this

NBTI model, the hydrogenic species is thought to diffuse far away from the interface and not

participate any further in recovery.[4,78] The threshold voltage recovery is, instead thought to occur, by detrapping of holes from the generated bulk traps.[4,78]

     As is illustrated throughout this brief NBTI history, there are quite a few controversies that permeate the literature. The fundamental understanding of NBTI provided by our measurements allows for an examination, and in some cases, a good explanation for, the root causes of these NBTI controversies.

# Chapter 2

# EXPERIMENTAL METHODS

## 2.1 The DC-IV Technique

The DC-IV technique is a DC current versus voltage measurement that is performed on a

MOSFET configured as a gate-controlled diode (source and drain contacts are shorted).[13,14]

Shorting the source and drain forms a diode between the source/drain and substrate. With this

diode slightly forward biased, a measurement of the device substrate current as a function of gate

voltage yields a peak in the substrate current.[13,14] This peak in substrate current is dominated by

recombination current through interface states.[13,14] Varying the gate voltage changes the surface

potential and consequently, the relative populations of charge carriers present at the interface.

The peak in substrate current occurs at the gate voltages which correspond to relatively equal

populations of electrons and holes at the interface (depletion).[13,14] The substrate current is at a

minimum at gate voltages corresponding to unequal populations of electrons and holes at the

interface (accumulation and inversion).[13,14] This concept is schematically illustrated in figure 2.1.

A quantitative derivation of the current versus voltage behavior was first presented in a

later series of papers by Fitzgerald and Grove.[13,90] In this derivation, *the peak in the gate*

*controlled diode measurement was related to the interface state density* ($D_{it}$) in a very

straightforward manner. Fitzgerald and Grove's derivation begins by assuming that the

recombination or generation events, in silicon, occur at deep level defects within the silicon band

gap and that the process can be described by the Shockley, Read, Hall (SRH) model[91,92] for

recombination-generation. Figure 2.2 schematically illustrates the SRH model. In this model, the

**Recombination Current via Interface Defects**

$\mathbf{I}_{sub}$

$\Delta I_{sub}$

$\mathbf{V_G}$

SiO$_2$     SiO$_2$     SiO$_2$

p$^+$   p$^+$    p$^+$   p$^+$    p$^+$   p$^+$

n-type Si     n-type Si     n-type Si

**Inversion**     **Depletion**     **Accumulation**
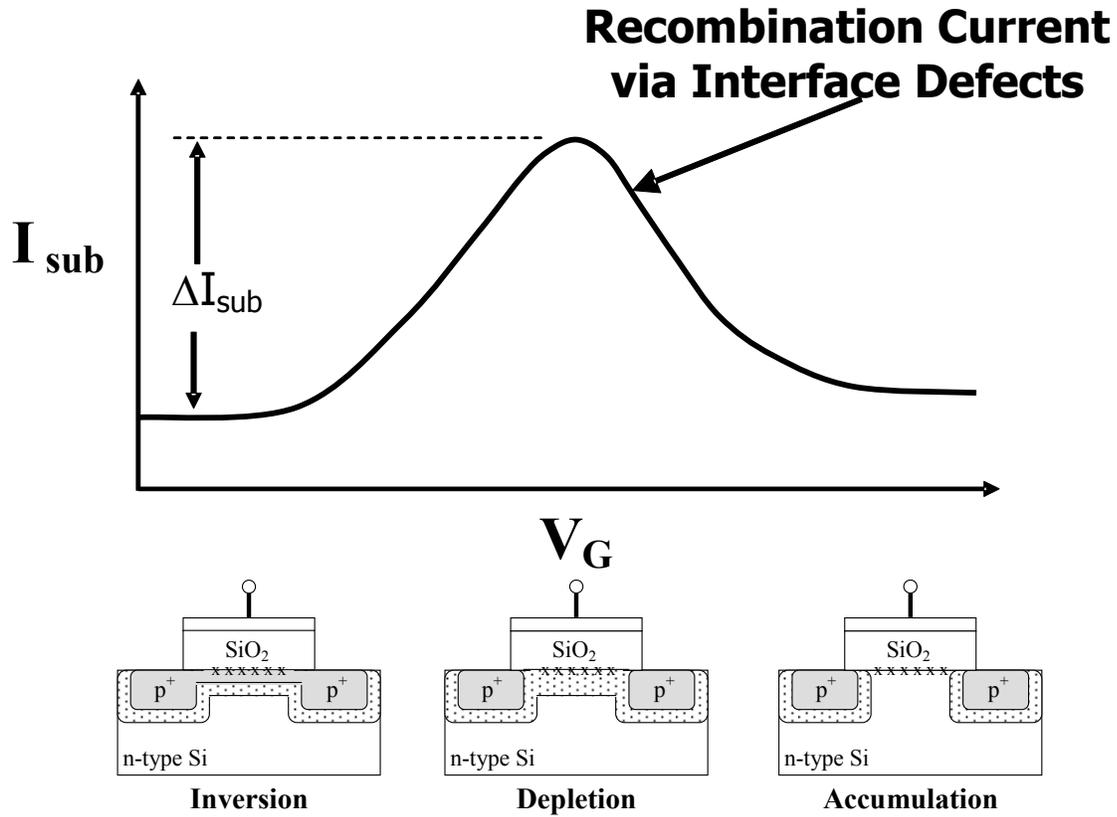
Figure 2.1: Schematic representation of the DC-IV measurement. In the case of a slightly forward biased source/drain to substrate diode, sweeping the gate voltage results in a peak in the substrate current due to recombination through interface states. This peak should occur at gate voltages which provide equal numbers of electrons and holes at the location of most of the recombination centers, the Si/dielectric interface.
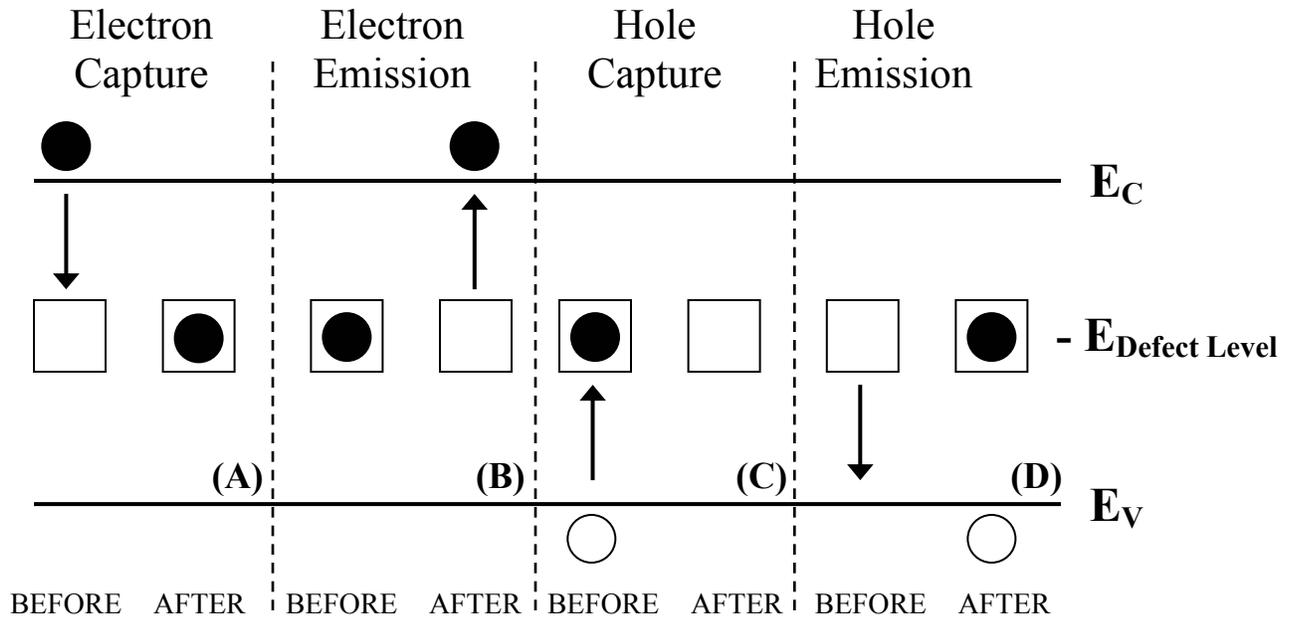
Figure 2.2: Schematic illustration of the Shockley, Read, Hall (SRH) model for recombination.

recombination-generation process is most efficient for deep level traps and can occur in one of the following four processes: (A) electron capture, in which an electron from the conduction band falls into a deep level and is trapped, (B) electron emission, in which a trapped electron is emitted from a deep level trap to the conduction band, (C) hole capture, in which a hole in the valence band is captured in a deep level trap that already contains an electron, and (D) hole emission, in which a trapped hole is emitted from a deep level trap to the valence band. (These processes can occur indefinitely and can also occur in reverse order.) When the SRH model is applied to a gate-controlled diode structure, Fitzgerald and Grove[13] showed that the substrate recombination current ($I_{SUB}$) is given by:

$$I_{SUB} = Aq\sigma_s v_{th} \left[ \int_{E_V}^{E_C} \frac{D_{it}(E)dE}{p_S + n_S + 2n_i \cosh\left(\frac{E - E_i}{kT}\right)} \right] \left[ p_S n_S - n_i^2 \right] \tag{2.1}$$

where A is the effective gate area, q is the electronic charge, $\sigma_s$ is the geometric mean of the electron and hole capture cross sections, $v_{th}$ is the thermal velocity of electrons, $E_C$ and $E_V$ denote the energies of the conduction and valence band edges respectively, $D_{it}(E)$ is the interface state density as a function of energy between $E_C$ and $E_V$, $p_S$ and $n_S$ are the hole and electron concentrations at the surface, $n_i$ is the intrinsic number of carriers, E is the energy level of the surface recombination centers, $E_i$ is the intrinsic Fermi level, k is Boltzmann's constant, and T is temperature. $p_S$ and $n_S$ for a pMOS device are given by

$$p_S \cong \frac{n_i^2}{N_D} \exp\left(\frac{-q\phi_s}{kT}\right) \exp\left(\frac{q|V_F|}{kT}\right) \tag{2.2}$$

$$n_S \cong N_D \exp\left(\frac{q\phi_s}{kT}\right) \tag{2.3}$$

16

where $N_D$ is the substrate doping, $\phi_S$ is the surface band bending, and $V_F$ is the forward bias applied to the source/drain to substrate junction. Note that increasing $V_F$ increases the number of minority carrier holes ($p_S$) available for recombination (in a pMOS device).

With the assumptions of an energy independent capture cross section and energy independent $D_{it}$ near mid gap, Fitzgerald and Grove[13] showed that equation (2.1) can be approximated by

$$I_{SUB} = \left(\frac{1}{2}\right) q n_i \sigma_S v_{th} D_{it} A q |V_F| \exp\left(\frac{q|V_F|}{2kT}\right) \quad \text{for } |V_F| > kT/q \qquad (2.4).$$

This equation allows for a straightforward extraction of interface state densities based on the peak in the substrate current. The energy window in which recombination occurs is controlled by $V_F$ and scales as approximately $q|V_F|$. The implications of changing $V_F$ and the recombination energy window to the DC-IV measurement are discussed in detail in chapter 4.


## 2.2 Electron Spin Resonance (ESR)


Since both of the EDMR techniques (SDR and SDT) used in this study are governed by ESR theory, it is useful to first examine the basic principles of this technique. ESR measurements are sensitive to unpaired electrons.[15,93,94] Since an electron is a charged particle with intrinsic angular momentum, it can qualitatively (and only qualitatively) be thought of as a negatively charged particle which is spinning on an axis.[15,93,94] In this qualitative picture, the spinning charged particle produces a magnetic field and an associated magnetic moment. In the absence of any external magnetic fields, these magnetic moments are randomly oriented.[93,94] However, the application of a large external magnetic field tends to align any unpaired electrons

such that the electron's magnetic moments align either parallel (spin-up, $M_S = +\frac{1}{2}$) or anti-parallel (spin-down, $M_S = -\frac{1}{2}$) to the applied field.[93,94] This polarization of the electrons splits the energy of the spin system into two different levels.[15,93,94] This is known as the Zeeman effect.[93,94] At thermodynamic equilibrium, the lower energy level is more populated and corresponds to the spin-up state.[15,93,94] The higher energy level corresponds to the spin-down state.[15,93,94] The Zeeman energy splitting is illustrated in figure 2.3.

In addition to the external (polarizing) magnetic field, a second high frequency (microwave) electromagnetic field is also applied to the system. If the product of Planck's constant and the high frequency field (hv) equals the Zeeman splitting, resonance can occur.[15,93,94] At resonance, the electrons can absorb energy and "flip" spin orientation. For the simplest case, the resonance condition is described as[15,93,94]:

$$h\nu = g_e \beta H \qquad\qquad (2.5)$$

where $h$ is Planck's constant, $\nu$ is the frequency of microwaves added to the spin system, $g_e$ is the free-electron g-value (g = 2.002319), $\beta$ is the Bohr magneton, and $H$ is the large applied magnetic field. The resonance described in equation (2.5) is for an isolated unpaired electron. In practice, the local environment of the unpaired electron changes the resonance condition. For systems relevant to this research, the deviations from the resonance condition are almost entirely due to spin-orbit coupling and electron-nuclear hyperfine interactions.[15,93,94]

### 2.2.1 Spin-orbit Coupling

Spin-orbit coupling alters the resonance condition of equation (2.5) by the addition of an effective local magnetic field due to the electron's orbital angular momentum about the nucleus.[15,93,94] This can be *qualitatively* described using the Bohr atomic model in which
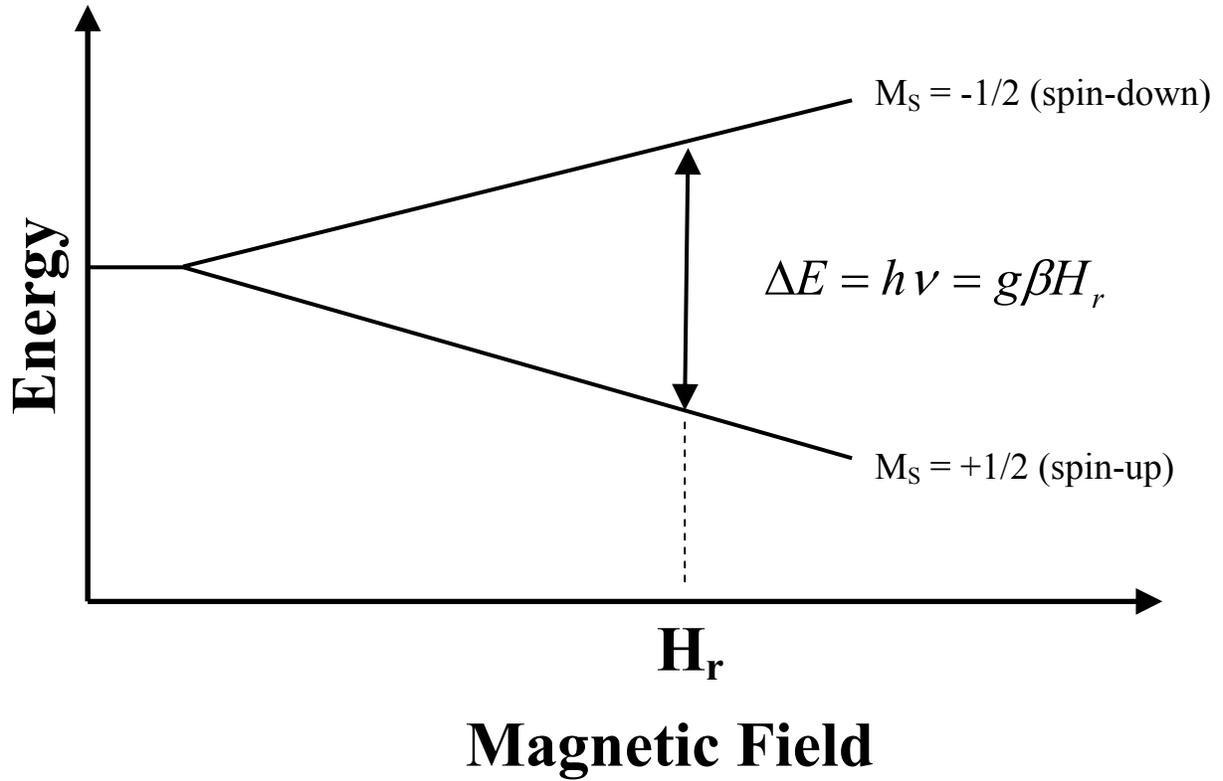
Figure 2.3: Schematic representation of Zeeman splitting for the simplest case of unpaired electrons.

electrons orbit the nucleus in a circular path.[15,93,94] Even though the electron is "orbiting the nucleus", from the perspective of the electron, the positively charged nucleus appears to orbit the electron. The circular orbit of the positively charged nucleus about the electron generates an additional local magnetic field. This alters the resonance condition for any electron "orbiting" a nucleus (for example, an electron trapped in the dangling bond of a point defect). The spin-orbit coupling effect is included in the resonance condition by replacing the free-electron ($g_e$) with the g-matrix, $g_{ij}$.[15,93,94] The g-matrix is also often referred to as a second rank tensor or g-tensor.[15,93,94] A second order time independent perturbation theory calculation gives $g_{ij}$ as[15,93,94]:

$$g_{ij} = g_e \delta_{ij} - 2\lambda \sum_{n,n\neq 0} \frac{\langle 0|L_i|n\rangle\langle n|L_j|0\rangle}{E_n - E_0} \tag{2.6}$$

where $\delta_{ij}$ is the Kronecker delta, $\lambda$ is the atomic spin-orbit coupling constant, $|0\rangle$ represents the electron's ground state, $|n\rangle$ represents an excited state, $L_i$ and $L_j$ are angular momentum operators appropriate for the x, y, or z directions, $E_0$ is the energy of the ground state and $E_n$ is the energy of the excited state.

As shown in equation (2.6), the $g_{ij}$ values of an electron trapped in a dangling bond of a point defect will deviate from $g_e$ as excited states are mixed with the ground state.[15,93,94] In practice, these deviations help to identify the structure of these point defects. The $g_{ij}$ is essentially a second rank tensor which reflects a defect's symmetry.[15,93,94] In the case of axially symmetric defects (where z is the symmetry axis) $g_{zz}$ is denoted as $g_\parallel$ and $g_{xx} = g_{yy}$ are denoted as $g_\perp$.[15,93,94] Here, $g_\parallel$ is the g-value measured when the applied magnetic field is parallel to the defect's symmetry axis, $g_\perp$ is the g-value measured when the applied magnetic field is perpendicular to the defect's symmetry axis.

## 2.2.2 Electron-Nuclear Hyperfine Interactions

Another important source of deviation from the resonance condition is due to electron-nuclear hyperfine interactions.[15,93,94] This occurs when an unpaired electron is located close to a nearby *magnetic* nucleus. The important magnetic nuclei involved in this study include silicon and nitrogen. Silicon naturally occurs as 95.3% (no magnetic nucleus) and 4.7% $^{29}$Si (spin ½ magnetic nucleus).[93,94] Nitrogen naturally occurs as essentially 100% $^{14}$N which has a spin 1 magnetic nuclei.[93,94] A spin ½ magnetic nucleus has two possible orientations in the applied magnetic field while a spin 1 magnetic nucleus has three possible orientations in the applied magnetic field.[15,93,94]

An unpaired electron nearby a nucleus with a net magnetic moment experiences an additional local magnetic field due to the nuclear magnetic moment.[15,93,94] This local field splits the Zeeman levels into $(2I + 1)$ additional states, where I is the nuclear spin.[93,94] This results in $(2I + 1)$ additional resonant lines at $(2I + 1)$ magnetic field values centered about the original resonant field.[93,94] The Zeeman splitting and resonance spectra for a nucleus with spin ½ are illustrated in figure 2.4. Note that all of the resonance transition arrows in figure 2.4 all correspond to the same energy, corresponding to one value of $h\nu$. Thus, when a system is subject to microwave irradiation of a frequency, $\nu$, the additional electron-nuclear hyperfine spectra occur at different applied fields.
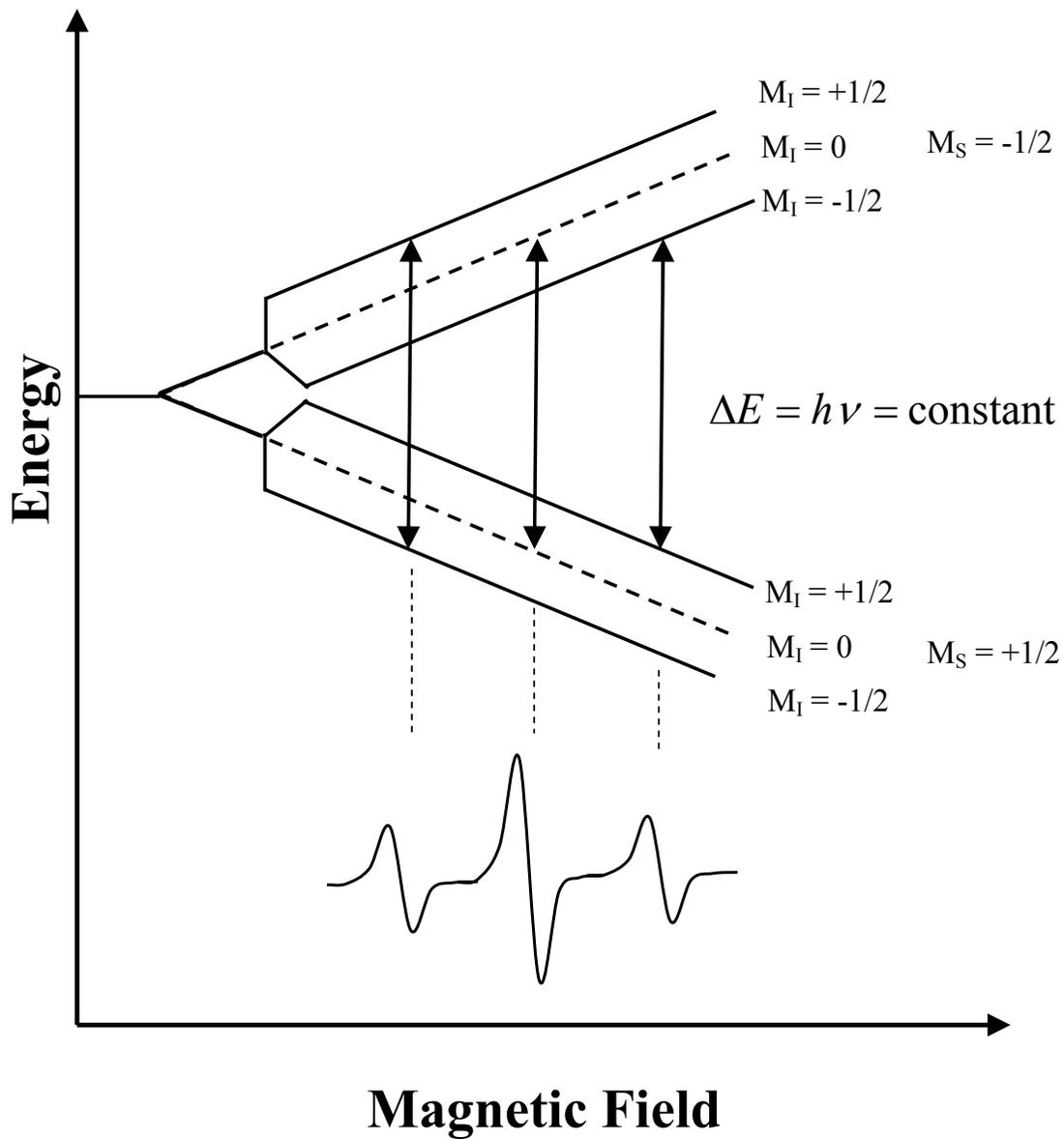
Figure 2.4: Schematic illustration of the Zeeman splitting which is altered by the presence of a nearby magnetic nucleus with spin (I = ½). The diagram also schematically illustrates the expected spectrum due to this nuclear hyperfine splitting.

As discussed above, the electron-nuclear hyperfine interaction alters the resonance condition by introducing an additional local magnetic field. If a single magnetic nucleus is involved with the unpaired electron, this altered resonance condition is given by[15,93,94]:

$$H = \frac{h\nu}{g\beta} + m_I A \qquad (2.7)$$

where $m_I$ is the nuclear spin quantum number, and $A$ is the electron-nuclear hyperfine matrix. It is important to note that not all nuclei have a magnetic moment. If no magnetic nuclei are present, the $m_I A$ term is zero.[15,93,94] The electron-nuclear hyperfine interaction (A) is can be expressed in terms of an isotropic ($A_{iso}$) and an anisotropic ($A_{aniso}$) component. The isotropic component, called the Fermi contact interaction is given by:[15,93,94]

$$A_{iso} = \frac{8\pi}{3} g_N \beta_N |\psi(0)|^2 \qquad (2.8)$$

where $g_N$ and $\beta_N$ are respectively, the g and Bohr magneton of the nucleus, and $|\psi(0)|^2$ is the unpaired electron probability at the nucleus. Since only an s-type wave function has a non-zero probability at the center of the nucleus, $A_{iso}$ is a measure of the s-character of the unpaired electron's wave function.[15,93,94] The anisotropic component is given by:

$$A_{aniso} = \frac{2}{5} g_N \beta_N \left\langle \frac{1}{r^3} \right\rangle \qquad (2.9)$$

where $\langle 1/r^3 \rangle$ is the expectation value over, in this case, a 3p orbital. The anisotropic component is a measure of the p-character of the unpaired electron's wave function.[15,93,94] The geometry of a p orbital dictates that the magnetic field interaction with an unpaired electron in a p type orbital should be anisotropic. That is, the interactions are different if the magnetic field is aligned parallel or perpendicular to the symmetry axis of the p-orbital.)

We assume that the wave function for an unpaired electron trapped in a dangling bond orbital consists of a linear combination of atomic orbitals (3s and 3p for the defects relevant to this study).[15] $A_{iso}$ and $A_{aniso}$ can be theoretically calculated for 100% 3s and 100% 3p wave functions respectively.[15,93,94] A comparison of the measured $A_{iso}$ and $A_{aniso}$ values with these calculated values gives a rough estimate of the s- and p-character of a defect's dangling bond wave function.[15,93,94] Additionally, the summation of the defect's s- and p-characters is a measure of the unpaired electrons localization to that dangling bond orbital.

Fortunately, the $A_{iso}$ and $A_{aniso}$ components of the hyperfine interaction can be related to the *measurable* interactions with the field parallel ($A_\parallel$) and perpendicular to ($A_\perp$) the unpaired electron's orbital symmetry axis. These relations are given by:[15,93,94]

$$A_{iso} = \frac{(A_\parallel + 2A_\perp)}{3} \tag{2.10}$$

$$A_{aniso} = \frac{(A_\parallel - A_\perp)}{3} \tag{2.11}$$

The electron-nuclear hyperfine modification to the resonance condition provides an extremely useful tool to determine information about a point defect's physical and chemical nature. This electron nuclear hyperfine interaction is used in this study to *identify the nature of the dominating NBTI-induced defect in PNO devices*.[17]

**2.2.3 The Electron Spin Resonance Spectrometer**

A schematic diagram of the ESR spectrometer is shown in figure 2.5. The spectrometer consists of three main components. The first is an electromagnet, which is used to apply the polarizing magnetic field which aligns any unpaired electrons in the sample under study. It is important that this magnetic field is extremely uniform and well controlled over the volume of the sample. The second component of the spectrometer is the microwave generator. To induce a resonance, the sample under study must be subject to microwave irradiation (this provides the necessary energy (hv) to allow spin flipping). The microwaves are typically generated using a klystron or Gunn diode source.[93,94] The third component of the spectrometer is the microwave cavity or resonator. The resonator's geometry allows for an efficient coupling of the microwave irradiation to the sample under study.[94] Typical ESR measurements involve X-band microwave irradiation (8-10 GHz) coupled to either $TE_{102}$ or $TE_{104}$ resonators at a magnetic field of approximately 3500 Gauss. These components provide the necessary hardware to induce a resonance; however, the resonance must also be detected. The detection scheme in ESR involves a microwave detector diode and a lock-in amplifier.[94] The microwave detector diode is placed in the microwave circuit and measures the reflected microwave power exiting the resonator. Changes in the reflected power indicate microwave absorption, or resonance. This absorption is monitored using a lock-in amplifier. The lock-in amplifier provides phase and frequency sensitive detection which vastly improves the sensitivity of this measurement. The lock-in detection scheme requires that the magnetic field is modulated at a known phase and frequency. This magnetic field modulation is provided by Helmholtz coils on the walls of the resonator. In practice, a sample is placed in the resonator and the microwave irradiation is critically coupled to the sample at some constant frequency. The reflected power is then monitored as a function of
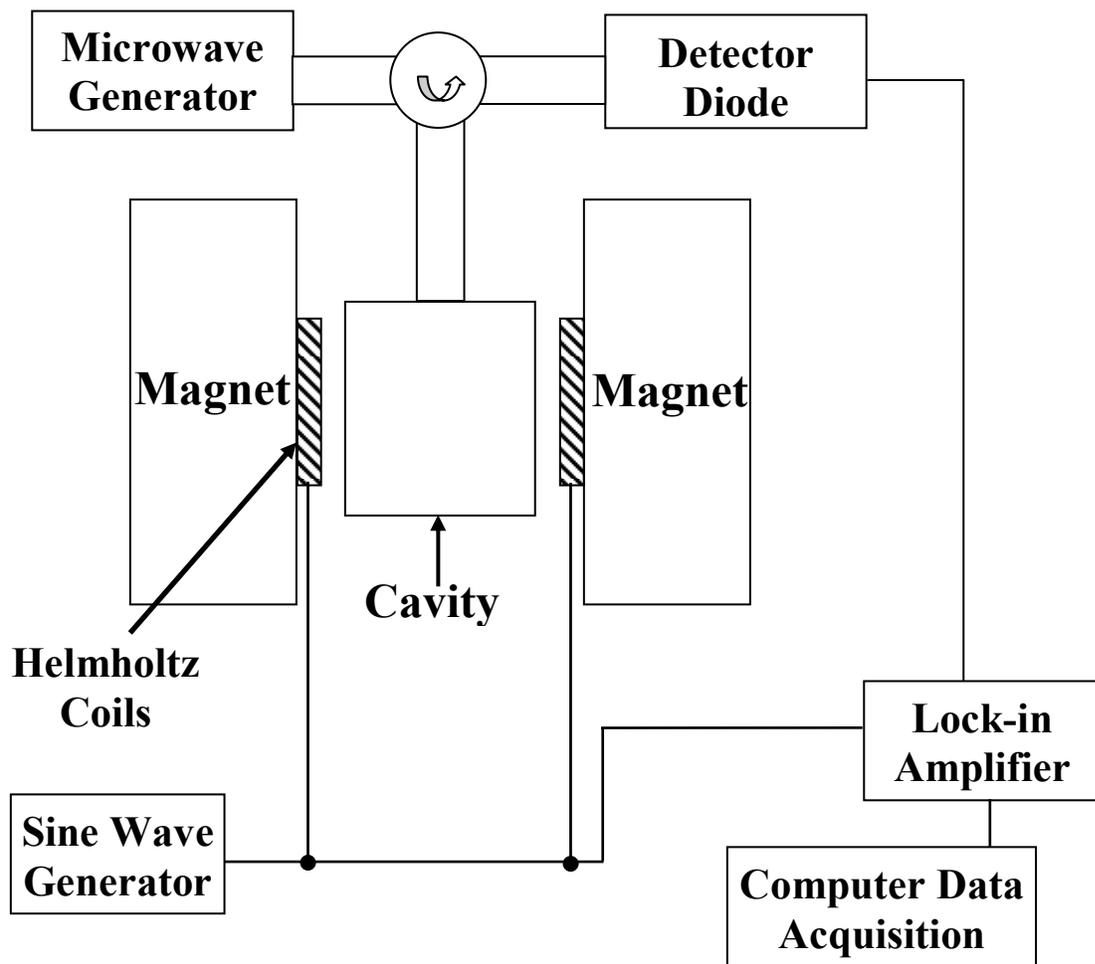
Figure 2.5: Schematic diagram of an ESR spectrometer.

magnetic field. When this technique is applied to MOS systems, the sensitivity ($10^{10}$ spins/Gauss of line width) requires fairly large area (~ 1 cm$^2$) sample sizes. The requirement that the sample under study be critically coupled to the microwave adds an additional upper limit on sample area and composition. To ensure that the microwave circuit is not loaded, the amount of conductive material (silicon substrates, metal or poly-Si gate layers) must be limited. Samples with known "spin" concentrations and g-values can be used to calibrate the field and frequency of the system which allows for measurements of the g and A "tensors" of a sample under study.

## 2.3 Spin-dependent Recombination (SDR)

Spin-dependent recombination (SDR) is an electrically detected ESR technique first demonstrated by Lepine in 1972.[95] In SDR, the samples under study include fully processed devices. The ESR induced spin flipping acts to modify device recombination current. The modification to this recombination current is measured as a function of magnetic field. This results in an ESR-like spectrum which is due to the deep level defects participating in recombination. This technique provides an extremely large increase in sensitivity over ESR and allows for measurements in fully processed devices.[23]

A brief, only qualitatively correct, explanation of SDR provided by Lepine[95] is useful in understanding our measurements. The Lepine model for SDR is schematically illustrated in figure 2.6. Lepine's model[95] combines both the Shockley-Read-Hall (SRH) model[91,92] for recombination and the Pauli exclusion principle. A SRH recombination event occurs when a conduction electron is captured by a deep level defect and then a hole is captured at the same defect site. (The recombination sequence could also be reversed.) In SDR, a transistor is biased

so that the source/drain to substrate current is dominated by recombination through interface defects (this corresponds to the peak in the DC-IV[13,14]). The device, thus configured, is placed in a large slowly varying DC magnetic field which partially polarizes the spins of the conduction electrons, holes, and deep level defects. If a deep level defect and a charge carrier have the same spin orientation, the Pauli exclusion principle forbids charge capture by the deep level defect because the electrons must have different spin quantum numbers to occupy the same orbital. When a paramagnetic deep level's electron spin resonance condition is satisfied, the defect's electron spins are "flipped." Flipping the spins increases the probability of opposite spin orientations between deep level defects and charge carriers, thus increasing the recombination current. This increase in recombination current, which is spin dependent, is what is measured in SDR.

Lepine's model provides simple insight into the physics governing SDR but predicts a spin dependent change in the recombination current of approximately 1 part in $10^6$ at the fields and temperatures utilized in our study.[95] SDR experiments can show a current change of approximately 1 part in $10^4$ or larger.[23,96] A frequently more accurate (but more complex) description of SDR has been proposed by Kaplan, Solomon, and Mott (KSM).[97] KSM extends Lepine's model to consider the coupling of two spins prior to the actual recombination events.[97] Once coupled, the two spins can either recombine or dissociate, but not recombine with other electrons and holes.[97] The KSM model assumes that recombination mostly involves singlet pairs (pairs in which the electrons have opposite spin orientation without the help of magnetic resonance).[97] The triplet (pairs in which the electrons have the same spin orientation) recombination rate is assumed to be negligible.[97] If resonance occurs while the two electrons are coupled, the triplet becomes a singlet and recombination occurs. The size of SDR effect
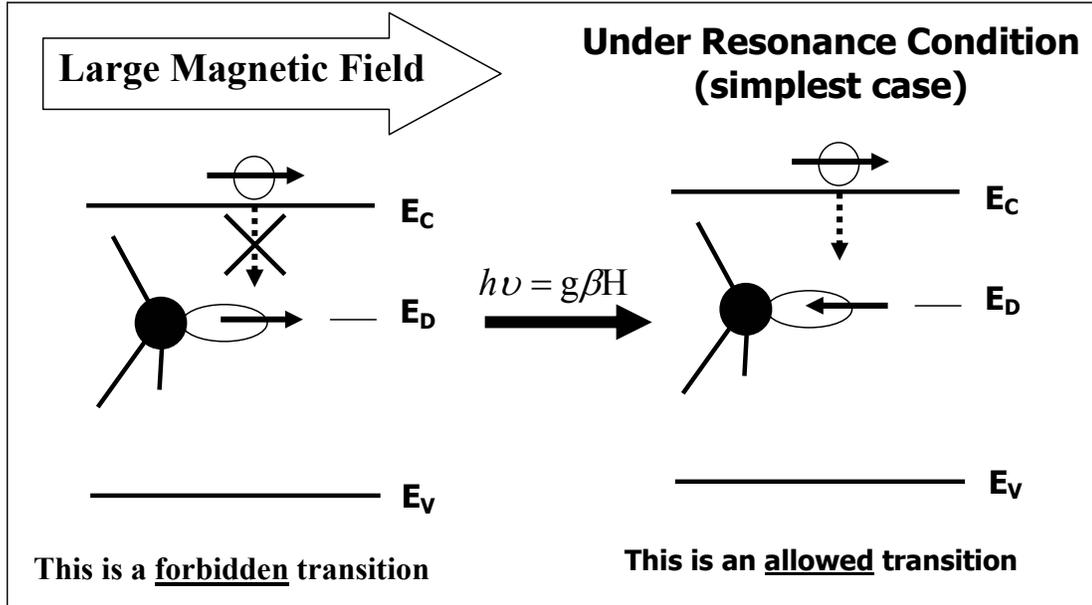
Figure 2.6: Schematic illustration of Lepine's model for SDR. In this model, device substrate current is modified due to (1) an ESR induced spin-flipping event and (2) the Pauli exclusion principle.

predicted by KSM is relatively large[97] and is more nearly consistent with experimental data on most devices than the Lepine model. In the KSM model, the size of the SDR effect depends upon the relationship between the coupling time of the pair and the spin-lattice relation time, or $T_1$.[97] The KSM analysis leads to the prediction of an SDR effect that is (to first order) magnetic field independent.[97] In other words, the magnetic field polarization of unpaired electrons has little effect on the recombination. It should be noted that the original KSM model assumes a coupling between conduction band and valence band electrons and holes.[97] In reality, the coupling is generally between a conduction or valence band charge carrier and a deep level defect.[96,98] The details of these SDR models and their relevance to MOS devices are discussed elsewhere.[96,98]

## 2.4 Spin-dependent tunneling (SDT)

SDT is very similar to SDR with the difference being that in SDT, one measures a *tunneling* current which is spin-dependent. There is very little in the literature regarding SDT measurements.[99,100] In the SDT measurement, a device is biased so that the substrate current is dominated by a trap assisted tunneling current through the gate dielectric. The device, thus configured, is placed in a large slowly varying DC magnetic field which partially polarizes the spins of the electrons, holes, as well as the spins of paramagnetic deep level defects participating in trap-assisted tunneling in the dielectric. If, for example, an unpaired electron in the tunneling defect and a gate valence electron both have the same spin orientation, the Pauli exclusion principle forbids a tunneling event through the center. However, satisfaction of the resonance condition can "flip" the spin orientation of the unpaired electron in the tunneling center and increases the probability of opposite spin orientations between tunneling center and gate valence

30

electrons, thereby increasing the tunneling current. The increase in trap-assisted tunneling current, which is spin-dependent, is what is measured in SDT.[99,100] While the details of the SDT mechanism in this study are not fully determined, our observations[17,18] are consistent with spin-dependent trap-assisted tunneling through "near-interface" defects. This mechanism is discussed in more detail in chapter 4.

## 2.5 The SDR/SDT Spectrometer

A schematic illustration of an SDR/SDT spectrometer is shown in figure 2.7. The schematic is remarkably similar to the ESR schematic of Figure 2.5. The differences include the sample types and detection schemes. In SDR and SDT, a fully processed transistor is critically coupled to the microwaves. The spin-dependent modification to the device recombination (tunneling) current is what is detected in SDR (SDT). This current is detected with the help of a current to voltage converter/pre-amplifier and the lock-in detection scheme. This measurement apparatus allows for very high sensitivity measurements. The SDR sensitivity can, under some circumstances, reach as little as $10^3$ paramagnetic defects.[23]
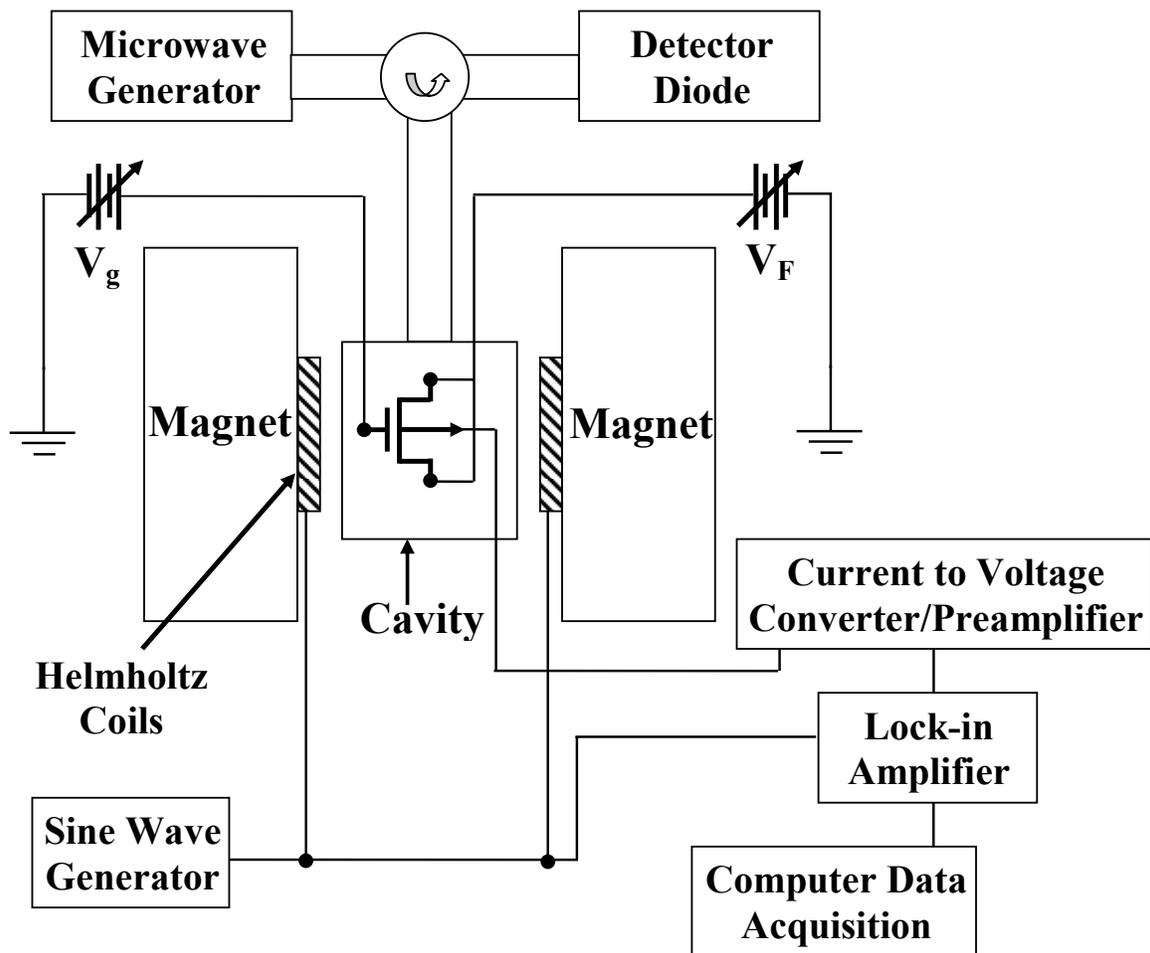
Figure 2.7: Schematic diagram of an SDR/SDT spectrometer.

# Chapter 3

## NBTI IN PURE SiO$_2$-BASED pMOSFETs

In this chapter, SDR measurements are utilized to directly observe the atomic-scale defects associated with NBTI in fully processed *pure SiO$_2$* devices.[19-21,101,102] (Here, "pure" indicates that the dielectrics are SiO$_2$ with only hydrogen present as a significant impurity.) We also correlate the SDR defect observations with DC-IV measurements[13,14] of NBTI-induced interface state density. The combination of DC-IV and SDR measurements is a useful tool to link specific atomic-scale defects to the device electronic properties. Our measurements in this chapter detail the correlation of NBTI-induced interface state generation to the generation of P$_{b0}$ and P$_{b1}$ interfacial silicon dangling bonds.[19-21,101,102] (P$_{b0}$ and P$_{b1}$ are both silicon dangling bond defects in which the central silicon atom is back bonded to three other silicon atoms precisely at the Si/SiO$_2$ interface.) Our results clearly show that NBTI is dominated by the generation of these P$_{b0}$ and P$_{b1}$ interface defects.[19-21,101,102] After a perhaps too harsh NBTS we also note the observation of E′ center oxide defects.[19-21,102] Our results do not allow for a definitive understanding of the E′ center's role in NBTI, but suggest that they may be involved in the catalyzing inversion layer hole capture process.[19-21,102]

## 3.1 Experimental Details

Our examination of NBTI in SiO$_2$ devices includes two different types of pure SiO$_2$-based pMOSFETs. The first type involves large area ($\approx$ 41,000 $\mu$m$^2$) 7.5nm SiO$_2$ devices

provided by Texas Instruments. The devices are fabricated in a gated-diode configuration where the source and drain are shorted together. The second type of devices involves very large area ($\approx$ $1 \times 10^6$ $\mu m^2$) 48 nm $SiO_2$ power pMOSFETs provided by Austria Microsystems. The gate dielectrics for these devices were formed using a 20 minute wet oxidation at 900°C followed by a 20 minute dry oxidation at 900°C. The oxidation steps were followed by a $N_2$ anneal at 925°C. These devices involve a large gate overhang that extends over a lightly doped region. This device layout slightly alters the DC-IV characteristic curves, but still allows for SDR observations of NBTI-induced atomic scale defects. Both types of devices were subject to various NBTS conditions. Following stress, all of the devices were subject to a temperature quench in which the stressing temperature is reduced to room temperature over approximately 4 minutes while the gate bias stress is maintained. We have been found this method to be fairly effective at "locking-in" the NBTI-induced damage, rendering it observable in the SDR/DC-IV measurements.[19] Interface state densities were monitored using the DC-IV measurement.[13,14] NBTI-induced changes in the DC-IV derived interface state density were correlated to SDR measurements detailing the generation of specific defect structures. X-band (~9.5GHz) SDR measurements were made at room temperature with a custom-built SDR/SDT spectrometer based on a Resonance Instruments 8330 series microwave bridge and a $TE_{102}$ microwave cavity. SDR measurements were calibrated using a strong pitch spin standard and an EIP 535 frequency counter. All DC-IV and SDR measurements in this chapter were made with +0.33V applied to the source/drain to substrate diode. The examination of NBTI in pure $SiO_2$ devices will begin with DC-IV and SDR measurements on the 7.5 nm devices and then proceed to the 48 nm power devices.

## 3.2 NBTI in 7.5nm SiO$_2$ pMOSFETs

7.5 nm SiO$_2$ devices were subject to an NBTS of -5.7V at 140°C for 250,000 seconds. Pre- and post-NBTS gate controlled diode DC-IV measurements are shown in figure 3.1. It is clear that the NBTS induces a large increase the peak substrate current which scales with D$_{it}$. Following the analysis of Fitzgerald and Grove[13], D$_{it}$ values were extracted for pre-NBTS (7 x 10$^9$ cm$^{-2}$eV$^{-1}$) and post-NBTS (5 x 10$^{11}$ cm$^{-2}$eV$^{-1}$) using a mean capture cross-section of $\sigma_s$ = 2 x 10$^{-16}$ cm$^2$. Figure 3.2 illustrates the corresponding pre- and post-NBTS SDR traces with the magnetic field vector perpendicular to the (100) surface. The interface state density in the unstressed device is below the SDR detection limit. After NBTS, we observe the generation of two strong signals at g = 2.0057 ± 0.0003 and g = 2.0031 ± 0.0003. The observed g-values at this magnetic field orientation allows us to attribute the g = 2.0057 signal to P$_{b0}$ centers and the g = 2.0031 signal to P$_{b1}$ centers. We note that the size of the SDR effect ($\Delta I/I \approx$ 5 x 10$^5$) is consistent with the KSM model.[97]
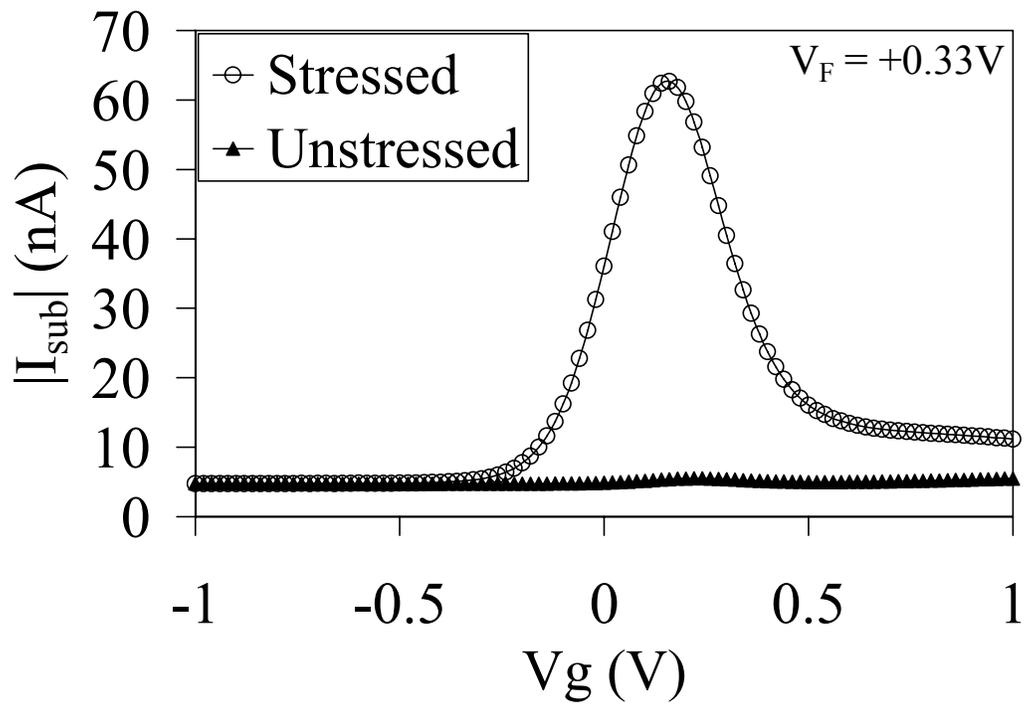
Figure 3.1: Gate controlled diode DC-IV measurements on a 7.5nm pMOSFET before and after the application of NBTS (-5.7V at 140°C for 250,000 seconds).
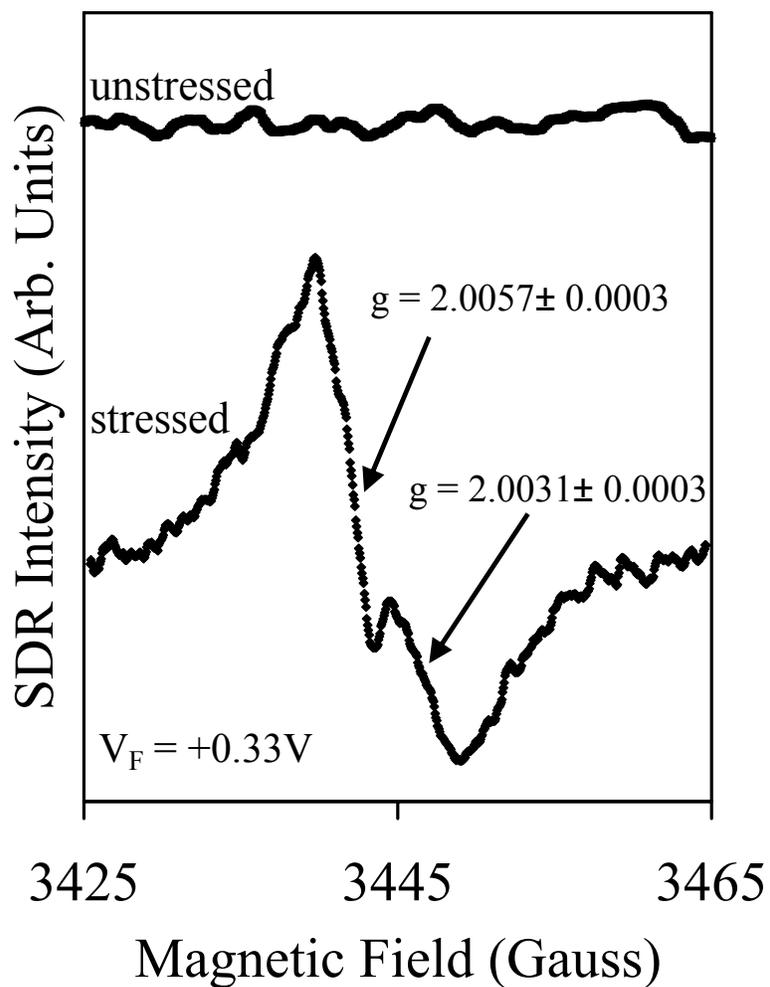
Figure 3.2: SDR traces of 7.5nm pMOSFETs with the magnetic field vector perpendicular to the (100) surface both before and after the application of NBTS (-5.7V at 140°C for 250,000 seconds).

$P_{b0}$ and $P_{b1}$ defects are both silicon dangling bond defects in which the central silicon atom is back-bonded to three other silicon atoms precisely at the $Si/SiO_2$ boundary.[15,22-25,103,104] Figure 3.3 illustrates a schematic drawing of $P_{b0}$ and $P_{b1}$ centers. The main differences between the two defects are in the dangling bond axes of symmetry[15,22,23,25,103,104] and electronic densities of states.[24,105-108] The $P_{b0}$ dangling bond orbital points along the <111> directions[15,22,23] while the $P_{b1}$ dangling bond orbital points along the <211> directions.[25,103,104] The observation of NBTI-induced $P_{b0}/P_{b1}$ defects is consistent with regard to the defects' densities of states.[15,105,106,108,109] Both the (111) Si $P_b$ center and (100) Si analog, the $P_{b0}$ center, have a broadly peaked density of states centered about mid-gap with the "+/0" and "0/-" transitions separated by about 0.7eV.[24,106,108] Utilizing conventional ESR measurements, Campbell et al. showed[105] (figure 3.4) that that the $P_{b1}$ has a considerably different density of states with the "+/0" and "0/-" transitions separated by only a few tenths of an eV and shifted toward the lower part of the gap. These experiments involved ESR measurements as a function of corona bias applied to the gate dielectric.[105] Varying the corona bias alters the position of the Fermi energy in the silicon, and therefore allows one to measure the density of states as a function of corona bias. Unfortunately, a precise quantitative comparison of the corona bias to the Fermi energy level is not available in this case. However, much earlier conventional ESR work[24,106-110] showed that the $P_b$ and $P_{b0}$ amplitude peaks at about mid-gap and drops to small fraction of the mid-gap amplitude when the Fermi level is close to either the valence or conduction band edge. These earlier studies (on thick $SiO_2$ structures with higher defect densities) did involve comparisons of Fermi energy and $P_b$ amplitude. Our conclusions, with regard to the $P_{b1}$ density of states, rely on these earlier observations of the $P_b$ and $P_{b0}$ densities of states. The newer observations of figure 3.4 clearly
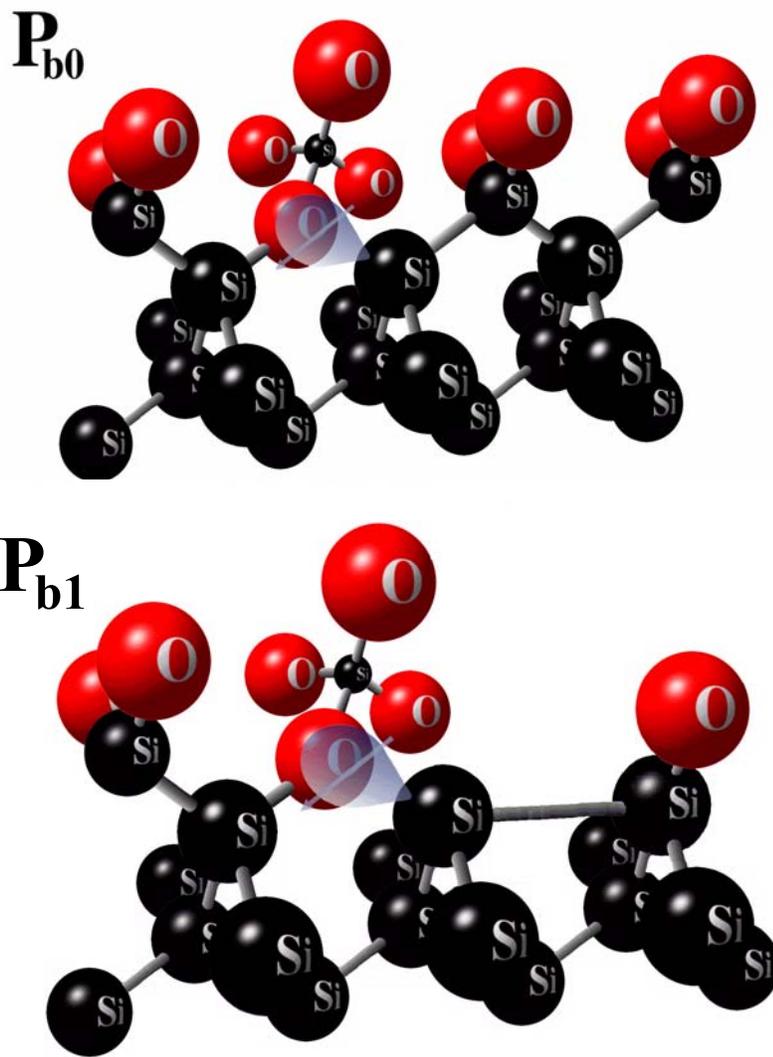
Figure 3.3: Schematic Drawing of the $P_{b0}$ and $P_{b1}$ Si/SiO$_2$ interface defects.
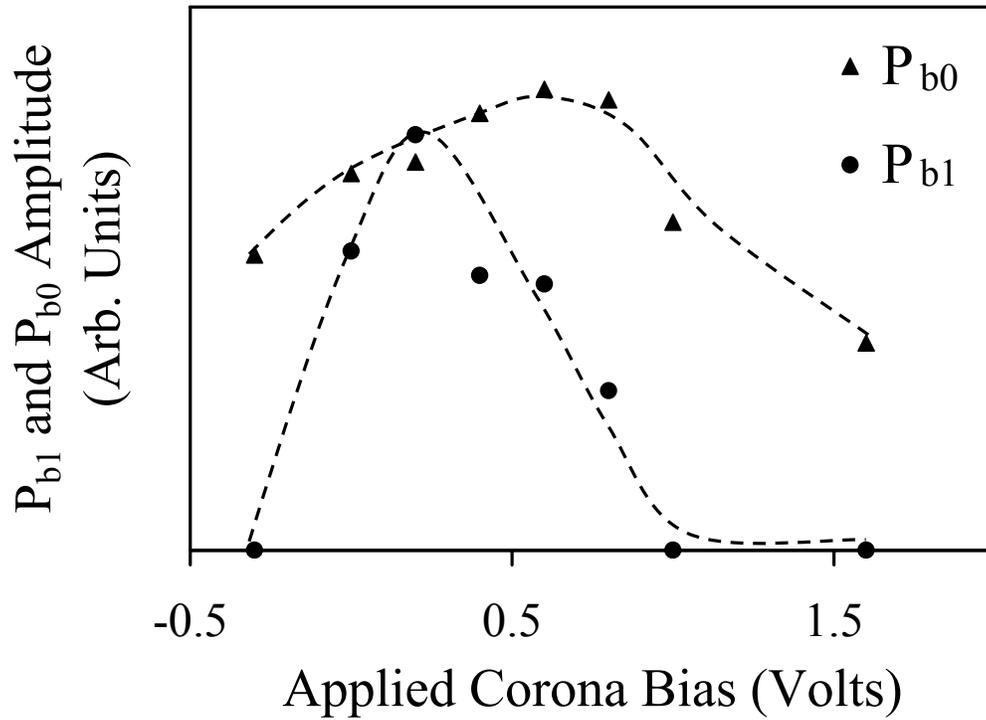
Figure 3.4: ESR derived $P_{b0}$ and $P_{b1}$ signal amplitudes as a function of applied corona bias. The plot indicates that the $P_{b1}$ density of states is narrower than the $P_{b0}$ and is skewed toward the lower part of the silicon band gap. The dashed lines are included as merely a guide for the eye.

show that the $P_{b1}$ distribution is considerably narrower than that of the $P_{b0}$ and also clearly shows that the distribution is shifted to the lower part of the band gap.[105] A schematic illustration of the $P_{b0}$ and $P_{b1}$ densities of states is illustrated in figure 3.5.[105]

Figure 3.6 illustrates the NBTI-induced $P_{b0}$ and $P_{b1}$ SDR signal amplitudes as a function of gate bias. The dashed lines are only a guide for the eye. Figure 3.6 clearly illustrates that both $P_{b0}$ and $P_{b1}$ centers have significant densities of states near midgap; a result at least qualitatively consistent with the broad density of states indicated in figure 3.4. The correspondence in gate voltage between the DC-IV peak (figure 3.1) and the SDR amplitude peaks (figure 3.6) provides further support to the concept that the dominating NBTI-induced defects in these $SiO_2$-based devices are $P_{b0}$ and $P_{b1}$ centers.
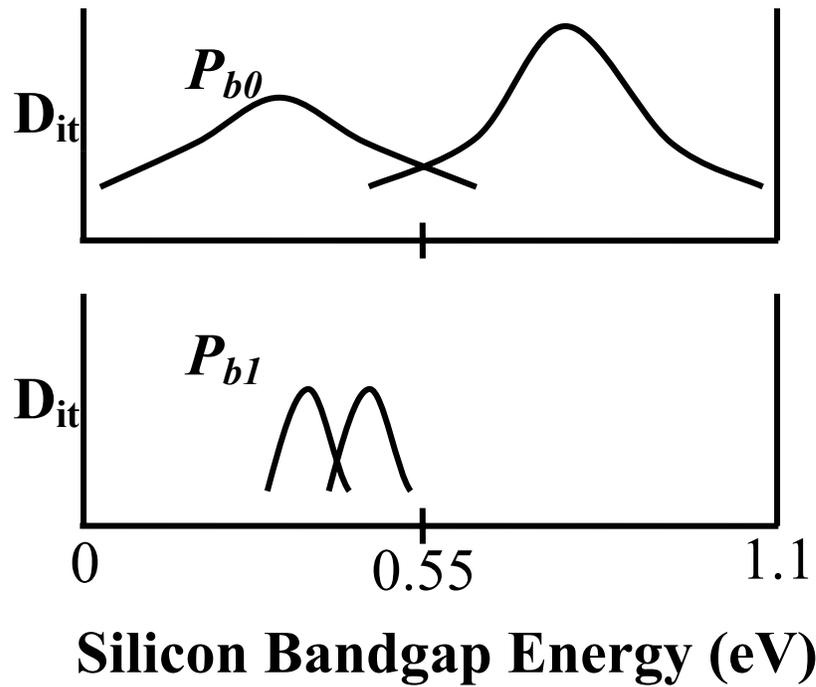
Figure 3.5: Schematic representation of the density of states of the $P_{b0}$ and $P_{b1}$ defects as a function of band-gap energy. The sketches provide only a crude semi-quantitative representation. The important points to note in this illustration are that the $P_{b1}$ density of states distribution is significantly narrower than that of the $P_{b0}$ density of states and that this distribution is almost certainly skewed toward the lower part of the Si band gap.
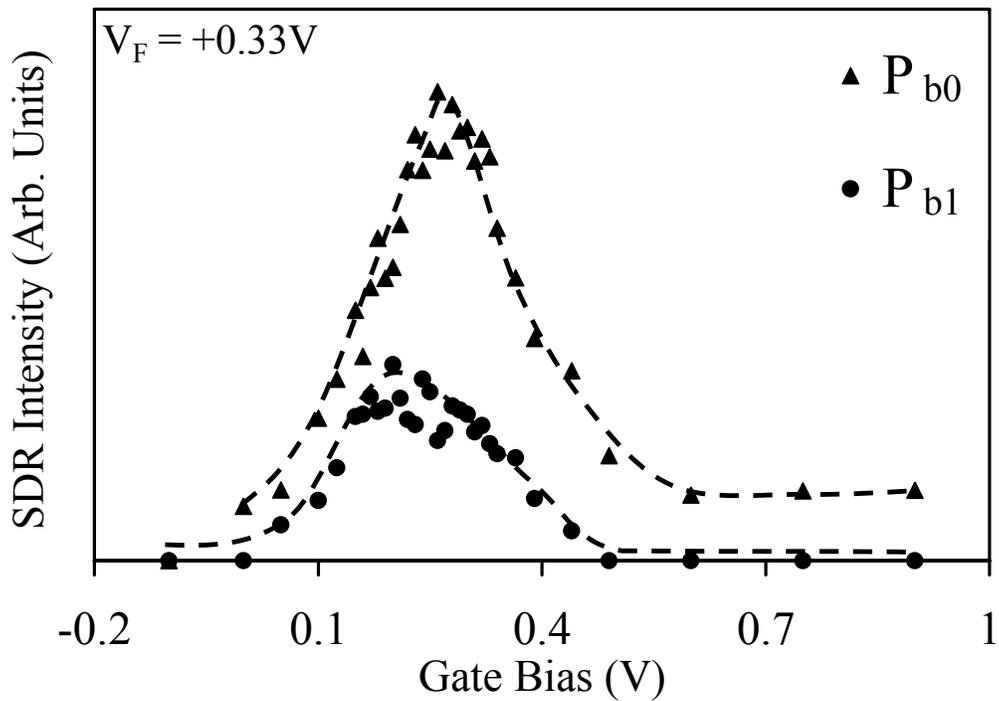
Figure 3.6: SDR derived $P_{b0}$ and $P_{b1}$ signal amplitudes as a function of applied gate bias for the 7.5nm pMOSFET subject to NBTS (140°C for 250,000 seconds with -5.7V on the gate contact). The dashed lines are included as merely a guide for the eye. In these measurements, the magnetic field vector is perpendicular to the (100) surface.

As discussed above, the assignment of $P_{b0}$ and $P_{b1}$ defects as the NBTI-induced defects in these $SiO_2$ devices is consistent with the observed NBTI-induced negative shift in threshold voltage. Figure 3.7 schematically illustrates, for a pMOS device biased in inversion, both the $P_{b0}$ and $P_{b1}$ centers would be positively charged. The $P_{b0}/P_{b1}$ defects would result in the expected NBTI-induced shift in threshold voltage. The fairly high densities of interface states seen in this study could account for quite significant threshold voltage shifts. Thus, our results are consistent with the idea that $P_{b0}/P_{b1}$ defects could be responsible for most of the NBTI threshold voltage shift in comparable devices (thicker $SiO_2$-based devices).
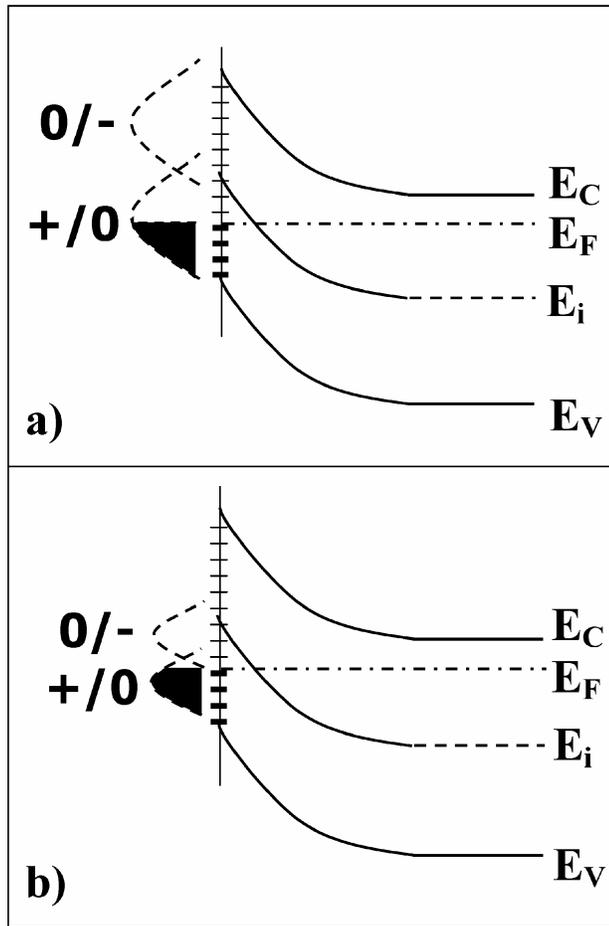
Figure 3.7: Schematic representations of the a) $P_{b0}$ and b) $P_{b1}$ density of states for p-type MOS capacitor biased in inversion.

In an effort to further investigate the defects associated with NBTI, another 7.5 nm device was subject to a higher temperature NBTS condition (-5.7V at 200°C for 20,000 seconds). The pre- and post-NBTS gate controlled diode DC-IV measurements are shown in figure 3.8. Again, it is clear that the NBTS induces a large increase in the peak substrate current and interface state density. The Fitzgerald/Grove analysis[13] yields a pre-NBTS $D_{it}$ of 7 x $10^9$ cm$^{-2}$eV$^{-1}$ and a post-NBTS $D_{it}$ of 7 x $10^{11}$ cm$^{-2}$eV$^{-1}$ assuming a mean capture cross-section of $\sigma_s$ = 2 x $10^{-16}$ cm$^2$.

Figure 3.9 illustrates the corresponding pre- and post-NBTS (-5.7V at 200°C for 20,000 seconds) SDR spectra with the magnetic field perpendicular to the (100) surface. Similar to the 140°C stressing case, we observe both $P_{b0}$ and $P_{b1}$ interface defect signals (g = 2.0060 ± 0.0003, and g = 2.0033 ± 0.0003 respectively). Within experimental error, the observed $P_{b0}$ and $P_{b1}$ g-values are the same as in the 140°C NBTS. In addition, we almost certainly observe a third signal (close to our sensitivity limit) at g = 2.0007 ± 0.0003. We attribute this signal to an E′ center oxide defect. E′ defects are oxygen vacancy centers or single silicon dangling bonds.[15] In both cases, the resonance measurements are sensitive to an unpaired electron in one or more silicon atom orbitals in which the silicon is back-bonded to oxygen atoms in the oxide. Figure 3.10 illustrates a schematic drawing of a neutral E′ symbol. The E′ centers (or any bulk dielectric defects) observed in an SDR measurement must be located very near the Si/SiO$_2$ interface because only "near-interface" oxide defects would be able to interact with the interface traps to alter the recombination current.[96,98] Since we are only observing the "near interface" E′ centers, the fact that the E′ signal is much weaker than the $P_{b0}$ and $P_{b1}$ signals does not necessarily indicate that the E′ density is significantly lower than the $P_{b0}$/$P_{b1}$ defects. There may be more E′ centers distributed further into the oxide.
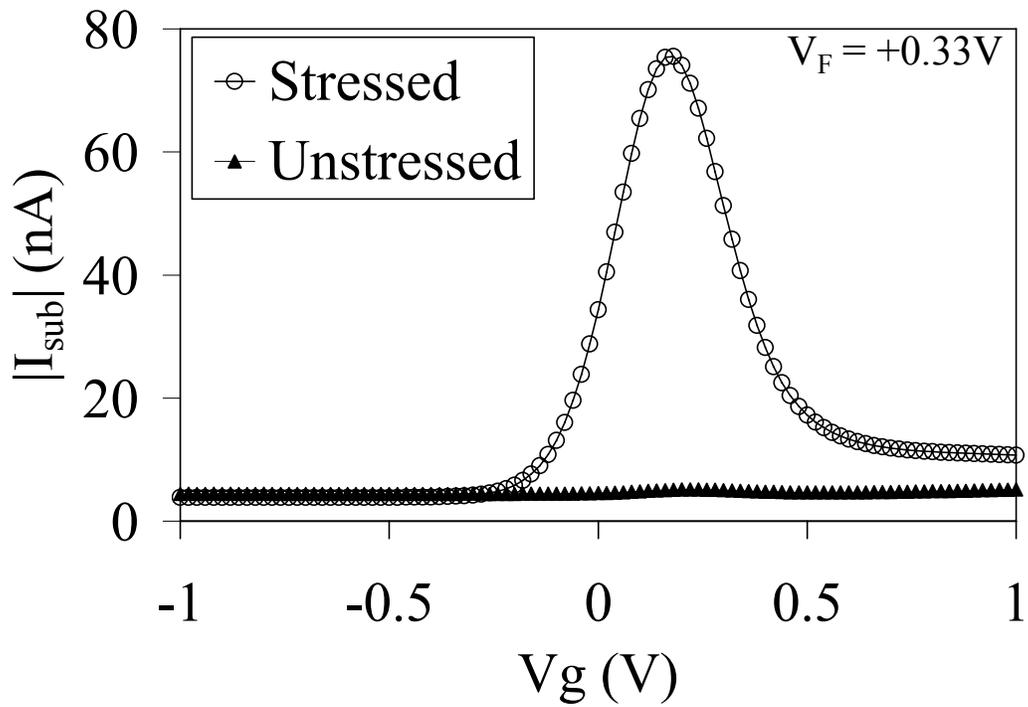
Figure 3.8: Gate controlled diode DC-IV measurements on a 7.5nm pMOSFET before and after the application of NBTS (-5.7V at 200°C for 20,000 seconds).
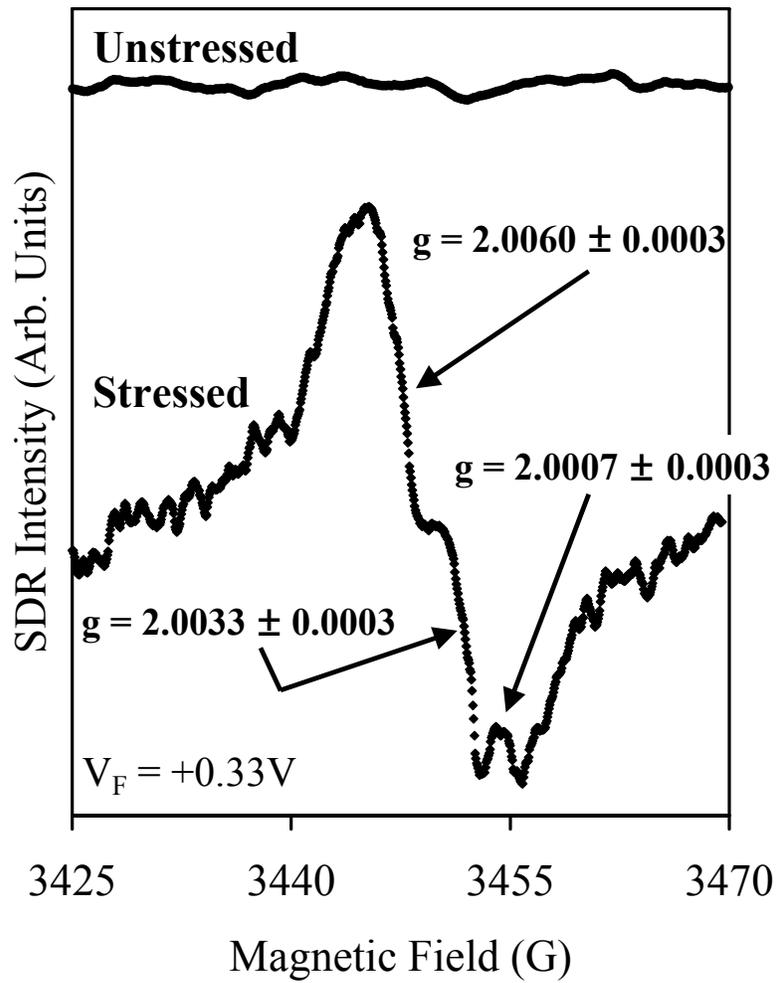
Figure 3.9: SDR traces of 7.5 nm pMOSFETs with the magnetic field vector perpendicular to the (100) surface both before and after the application of NBTS (-5.7V at 200°C for 20,000 seconds).
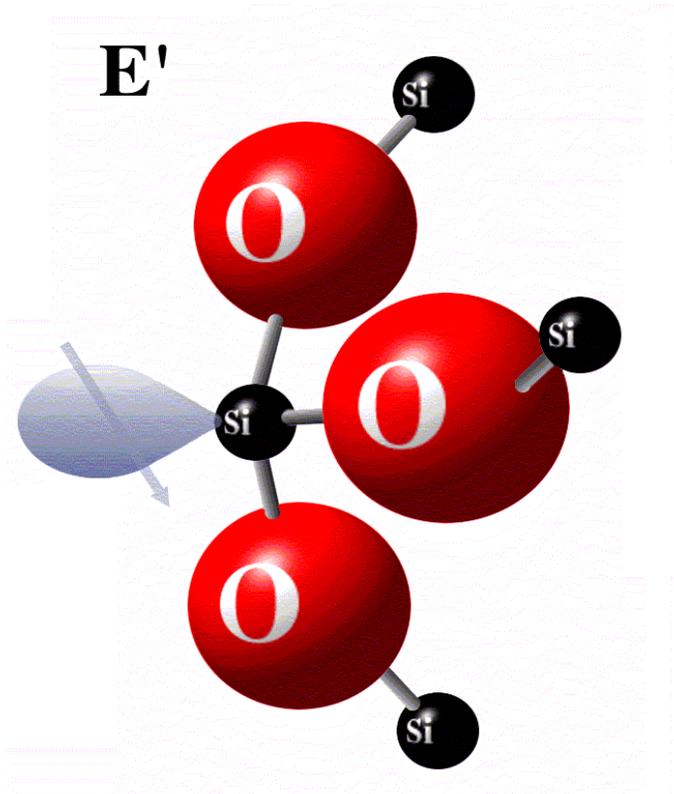
Figure 3.10: Schematic representation of a neutral E' center oxide defect.

At this time, we are not able to conclusively determine the role of E′ defects in NBTI. Since we are only able to detect the E′ signal in the devices subjected to the harsher stressing condition (-5.7V, 200°C for 20,000 seconds), we cannot rule out the possibility that, under these circumstances, the E′ centers have been generated via hot hole oxide injection[71] (inconsistent with the NBTI phenomenon). Nevertheless, our E′ observations suggest that they may play an important role in NBTI. It is worth noting that E′ centers have levels near the middle of the $SiO_2$ band gap; at energies appropriate for hole capture from the silicon inversion layer.[111] There is extensive experimental evidence indicating that E′ centers can capture holes.[15,112] There is also clear experimental evidence that, after hole capture, E′ centers can "crack" molecular hydrogen; a process which could lead to Si-H bond dissociation at the Si/dielectric boundary.[112] As mentioned above, most NBTI theories involve the capture of an inversion layer hole which then leads to $Si/SiO_2$ interface Si-H dissociation.[1,2,26,27] Although our E′ center results must be viewed with some skepticism, they do suggest a potential path in which an inversion layer hole capture event can lead to eventual $Si/SiO_2$ Si-H bond breaking.

### 3.3 NBTI in 48nm $SiO_2$ Devices

We have also examined the NBTI response in some much thicker pure $SiO_2$ power transistors. These devices also exhibit a similar NBTI response as observed in the 7.5nm $SiO_2$ devices. These devices were subject to a NBTS condition of -25V at 175°C for 100,000 seconds. Figure 3.11 shows both the pre- and post-stress DC-IV characteristic curves. The geometry of these devices (gate extension over lightly doped regions) results in two DC-IV peaks.[113] The DC-IV double peak has been reported in the literature for devices with lightly doped regions.[113] The DC-IV peak at $V_G = -0.5V$ is associated with interface states located near the center of the

50
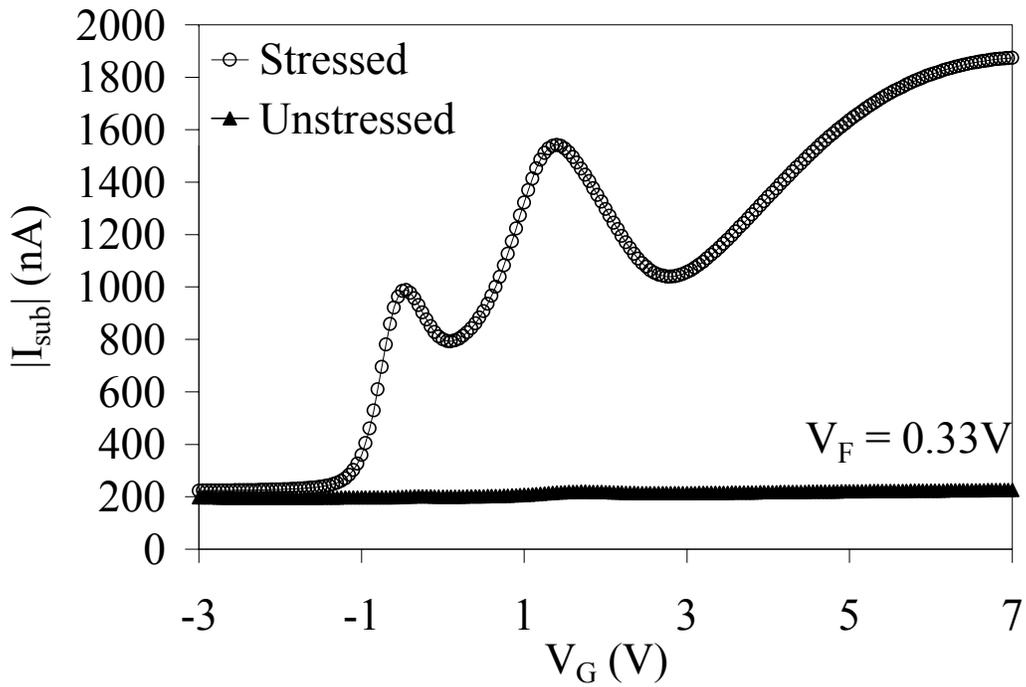
Figure 3.11: Gate controlled diode DC-IV measurements on a 48 nm power pMOSFET before and after the application of NBTS (-25V at 175°C for 100,000 seconds). The double peak in the DC-IV characteristics is consistent with the devices geometry. These devices include lightly doped regions adjacent to the source and drain. This results in two different depletion regions corresponding to two different peaks in the DC-IV curve.

channel while the DC-IV peak at $V_G = 1.4V$ is associated with interface states in the drift regions adjacent to the source and drain.[113] Austria Microsystems has performed processing simulations for these devices which indicate that the lightly doped regions on both the source and drain sides of the pMOSFET account for a large part of the channel region. This is also indicated by the relative sizes of the two DC-IV peaks. After NBTS, we observe an increase in both of these substrate current peaks. The Fitzgerald and Grove analysis[13] leads to pre-NBTS $D_{it} = 6 \times 10^9$ $cm^{-2}eV^{-1}$ and $D_{it} = 8 \times 10^9$ $cm^{-2}eV^{-1}$ for the $V_G = -0.5$ and $V_G = 1.4V$ peaks, respectively. Post-NBTS, we observe an increase in substrate current peaks which correspond to $D_{it} = 2 \times 10^{11}$ $cm^{-2}eV^{-1}$ and $D_{it} = 4 \times 10^{11}$ $cm^{-2}eV^{-1}$ for the $V_G = -0.5$ and $V_G = 1.4V$ peaks, respectively. All the extracted $D_{it}$ values assume a mean capture cross-section of $\sigma_s = 2 \times 10^{-16}$ $cm^2$.

Figure 3.12 illustrates the corresponding SDR measurements for $V_G = -0.5V$ and $V_G = +1.4V$ with the magnetic field aligned parallel to the <100> surface normal. The interface state density in the unstressed device is below our SDR detection limit. After NBTS, we observe the generation of a strong signal at $g = 2.0056 \pm 0.0003$ for $V_G = 1.4V$ and $V_G = -0.5V$. The observed g-value at this magnetic field orientation indicates that this signal is due to $P_{b0}$ centers. We note that the same defect signature is observed with $V_G = 1.4V$ and $V_G = -0.5V$. This is an indication that NBTI generates the same defects in the channel and lightly doped interface regions of the device.

Figure 3.13 illustrates the $P_{b0}$ SDR signal amplitudes as a function of gate bias as well as the DC-IV characteristic curve for the post-NBTS pMOSFET of figures 3.11 and 3.12. The close correspondence in gate voltage between the peaks in DC-IV and SDR measurements is another
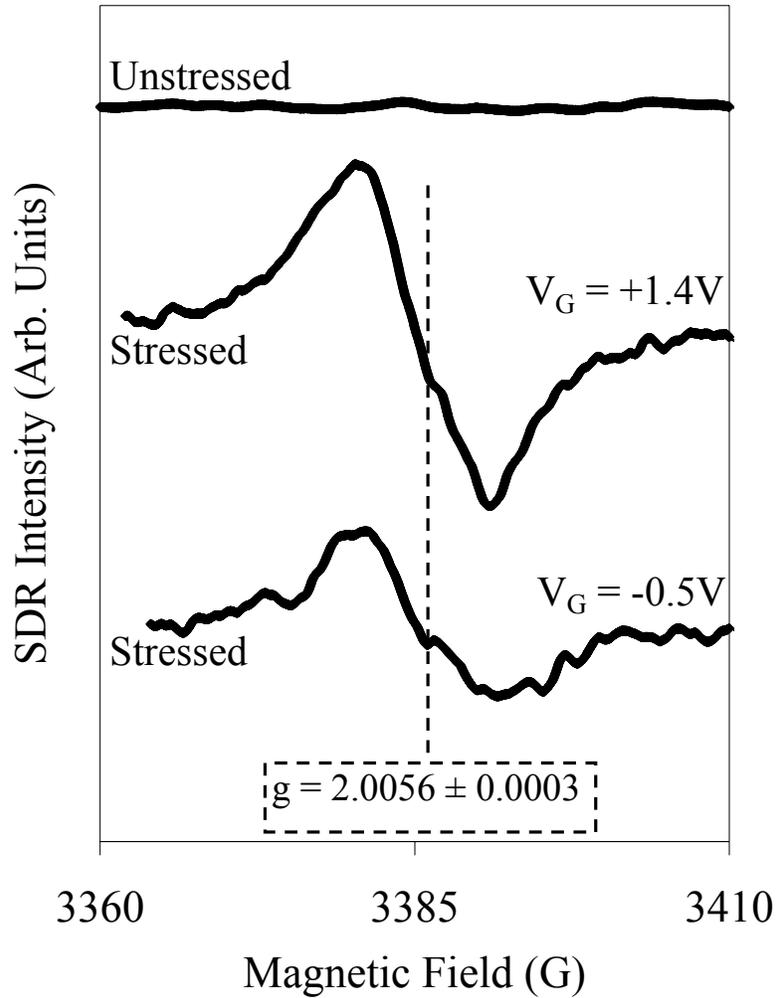
Figure 3.12: SDR traces of 48nm pMOSFETs with the magnetic field aligned parallel to the <100> direction both before and after the application of NBTS (-25V at 175°C for 100,000 seconds). We observe the same defect with the gate voltage corresponding to each of the two DC-IV peaks ($V_G$ = 1.4V and $V_G$ = -0.5V).
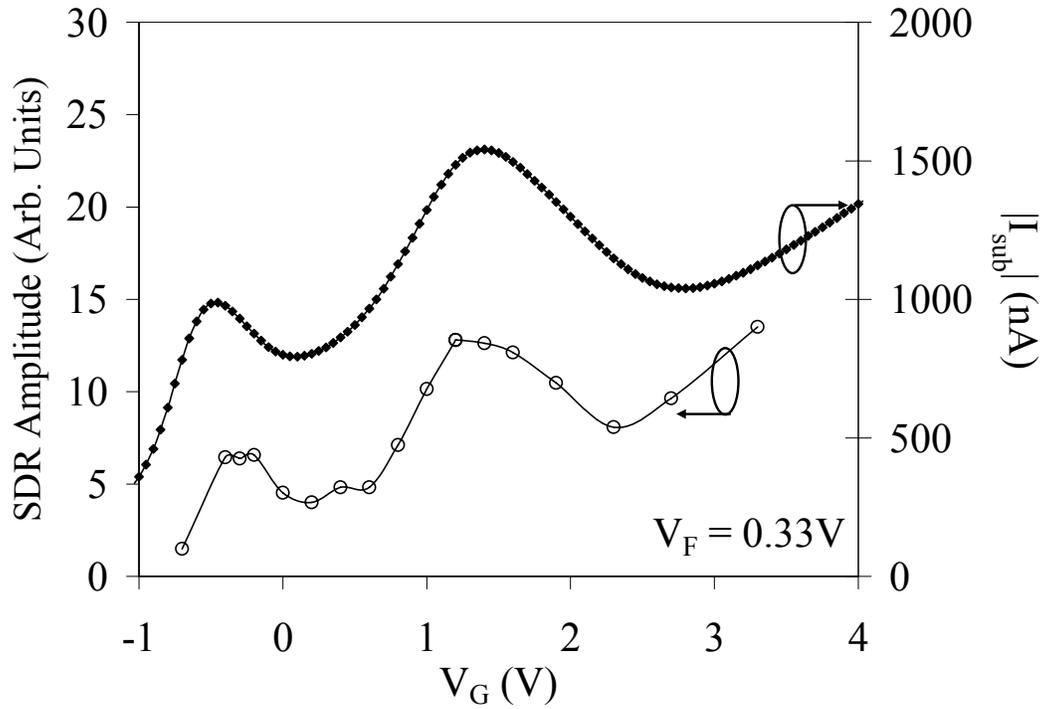
Figure 3.13: SDR signal amplitude (lower curve) and DC-IV derived substrate current (upper curve) as a function of gate bias for the 48 nm pMOSFET subject to an NBTS of -25V at 175°C for 100,000 seconds. The close correspondence between these two measurements is a strong indication that the defects observed in SDR are the same defects monitored in the DC-IV measurement.

indication that the $P_{b0}$ defects dominate the electronic NBTI-induced interface state density response.

From these observations, we conclude that the NBTI response in the 48nm pMOSFETs is dominated by $P_{b0}$ interface state generation. It is somewhat interesting that we observe both $P_{b0}$ and $P_{b1}$ defects in the 7.5nm devices but only $P_{b0}$ defects in the 48nm devices. The presence of $P_{b0}$ and $P_{b1}$ defects at the Si/SiO$_2$ interface is thought to be a result of strain relief. However, the reasons for the preferential generation of one of these defects in some devices is not understood.

### 3.4 Summary

In both the 7.5nm and 48nm SiO$_2$ pMOSFETs, DC-IV measurements indicate that the NBTI response is dominated by the generation of relatively large densities of interface states. The corresponding SDR measurements identify these NBTI-induced interface states as $P_{b0}$ and $P_{b1}$ defects in the 7.5nm devices and $P_{b0}$ defects in the 48nm devices. Thus, our observations for these SiO$_2$ devices indicate that NBTI is more consistent with the reaction-diffusion model in which the response dominated by interface state generation.[1,2] Our observation of NBTI-induced E′ centers suggests that they may have some role in the catalyzing inversion layer hole capture. However, since unrealistically harsh NBTS was required to observe the E′ centers, it is not possible to conclude with certainty that they play a role under technologically relevant conditions.

# Chapter 4

## NBTI IN PLASMA-NITRIDED OXIDE (PNO) pMOSFETs

This chapter discusses SDR and SDT magnetic resonance measurements utilized to directly observe the atomic-scale defects of NBTI in fully processed 2.3 nm PNO devices.[17,18,20] We compare the SDR and SDT measurements with DC-IV observations of NBTI-induced changes in interface state densities as well as trap-assisted tunneling current measurements. We also make measurements on 7.5 nm pure $SiO_2$ devices, which serve as a good comparison for our observations in the 2.3 nm PNO devices. Our results definitively identify the dominating atomic-scale defect in the 2.3 nm PNO devices as a $K_N$ center (not a $P_{b0}$ or $P_{b1}$ center).[17,18] $K_N$ centers are silicon dangling bond defects in which the central silicon is back-bonded to three other nitrogen atoms.[17] The $K_N$ centers are in the "near-interface" region of the dielectric and have a fairly narrow peaked effective density of states near the middle of the band gap.[18] We find that NBTI-induced $K_N$ centers participate in both spin-dependent recombination and tunneling processes.[18] This is an indication that the same defect can act like an interface state and a bulk dielectric tunneling center.[18] These collective observations may help explain why the addition of nitrogen enhances the NBTI phenomenon. They may also explain why NBTI experts can report conflicting views on the roles of NBTI-induced interface states and bulk traps. Finally, this deeper understanding of the NBTI-induced atomic-scale defects may help to explain fluorine's ineffectiveness in reducing NBTI in nitrided devices.

## 4.1 Experimental Details

This study involves both 7.5nm $SiO_2$ and 2.3nm equivalent oxide thickness (EOT) PNO large area pMOSFETs (~40,000 $\mu m^2$). Since the NBTI-induced atomic-scale defects are fairly well understood in the thicker $SiO_2$ devices[19-21], we use them as a control to compare and contrast the thinner PNO devices. The $SiO_2$ devices were subject to an NBTS of -5.7V at 140°C for 210,000 seconds. The PNO devices were subject to an NBTS of -2.6V at 140°C for 180,000 seconds. Interface state densities ($D_{it}$) were monitored using DC-IV measurements.[13,14] In the DC-IV measurement, the source and drain contacts are shorted while the source/drain to substrate diode is forward biased.[13,14] The substrate current is then monitored as a function of gate bias ($V_G$).[13,14] Fitzgerald and Grove showed that when the substrate current is dominated by recombination through interface states, the DC-IV characteristic curve displays a peak in the substrate current.[13] The difference between this peak and baseline substrate current scales with the interface state density, $D_{it}$. The energy window in which recombination occurs is controlled by $V_F$. As will be shown in the following sections, variations in the SDR and DC-IV recombination energy window provide a deeper understanding of the defects involved.

X-band (~9.5GHz) SDR and SDT measurements were made at room temperature with a custom-built SDR/SDT spectrometer based on a Resonance Instruments 8330 series microwave bridge and a $TE_{102}$ microwave cavity. SDR/SDT measurements were calibrated using a strong pitch spin standard and an EIP 535 frequency counter. Immediately following the stress, each device was subject to a post-NBTS temperature quench step. This step involves cooling the device to room temperature (over the span of several minutes) while the negative stressing bias is

maintained. We have found this method to be fairly effective at "locking-in" the NBTI-induced damage, rendering it observable in SDR/SDT.[20] Also, to ensure that further recovery was minimal during subsequent measurements, all DC-IV, SDR, and SDT measurements were taken at least 4 hours post-NBTS/temperature quench. The details of the SDR phenomena and SDT phenomenon are discussed in Chapter 2.

**4.2 Comparison of NBTI in 7.5 nm SiO$_2$ and 2.3 nm PNO pMOSFETs: Different Defects**

Figure 4.1 illustrates the pre- and post-NBTS DC-IV characteristic curves for a 7.5nm SiO$_2$ and a 2.3nm EOT PNO-based pMOSFET. In the 7.5nm SiO$_2$ device (figure 4.1a), NBTS clearly generates an increase in the peak substrate current corresponding to an increase in D$_{it}$. The Fitzgerald and Grove analysis[13] leads to a pre-stress D$_{it}$ $\approx$ 6 x 10$^9$ /cm$^2$eV and a post-stress D$_{it}$ $\approx$ 4 x 10$^{11}$ /cm$^2$eV assuming a mean capture cross section of $\sigma_s$ = 2 x 10$^{-16}$ cm$^2$. In the 2.3nm PNO device (figure 4.1b) NBTS also generates an increase in peak substrate current and D$_{it}$. Fitzgerald and Grove derived D$_{it}$ values were not extracted for these devices because of the uncertainty in the mean capture cross-section. However, we note an approximately one order of magnitude increase in the peak substrate current which should correspond to approximately one order of magnitude increase in D$_{it}$. It is clear that NBTS generates a very large increase in D$_{it}$ in both the SiO$_2$ and PNO devices. We note that the shapes of the DC-IV characteristic curves for the SiO$_2$ and PNO devices are somewhat different. The SiO$_2$ DC-IV curve is consistent with recombination while the PNO DC-IV is due to both recombination and tunneling; tunneling dominates at the most positive gate voltages. As one would anticipate, the PNO tunneling

component is most dominant when the source/drain to substrate diode forward bias ($V_F$) is reduced to near zero or zero. (In this case, the recombination current is turned off.)

Figure 4.2 illustrates post-NBTS magnetic resonance results for the 7.5nm $SiO_2$ and 2.3nm PNO-based devices with the magnetic field parallel to the <100> surface normal. The spectrometer settings in each case are optimized to yield the true line shape of the spectra. In this figure, SDR spectra are plotted as a function of g-value to illustrate differences in NBTI-induced defects in the $SiO_2$ and PNO devices. NBTS in 7.5nm $SiO_2$-based devices generates two SDR signals at g = 2.0059±0.0003 and g = 2.0033±0.0003 corresponding to $P_{b0}$ and $P_{b1}$ Si/$SiO_2$ interface defects respectively.[21] The $P_{b0}$ and $P_{b1}$ defects have been shown to be the dominating interface defects in Si/$SiO_2$ systems under many circumstances[15] and have also been shown to play a large role in NBTI in thicker $SiO_2$-based devices.[16,19-21] We note that the size of the SDR signal for $SiO_2$ device ($\Delta I/I \approx 5x10^5$) is more consistent with the KSM model[97] for SDR. In 2.3nm PNO-based devices, NBTS generates a much broader ($\approx$ 14G wide) SDR signal at g = 2.0020±0.0003. Measurements (not shown) with spectrometer settings optimized to observe narrower signals within the broad g = 2.0020 signal revealed no other components. If $P_{b0}$/$P_{b1}$ centers were present in significant quantities in the PNO-based devices, the overlapping $P_{b0}$/$P_{b1}$ signal would be observed to the left (higher g-value) of the apparently symmetric g = 2.0020 signal. It is clear that this is not the case. Thus, NBTS in thinner PNO-based devices generates this new defect at g = 2.0020 to such an extent that any $P_{b0}$/$P_{b1}$ generation is completely obscured. From these DC-IV/SDR measurements, it is clear that NBTI generates different defects in the PNO devices. The following sections of this manuscript examine the electronic properties and physical identity of this NBTI-induced center in the PNO devices.
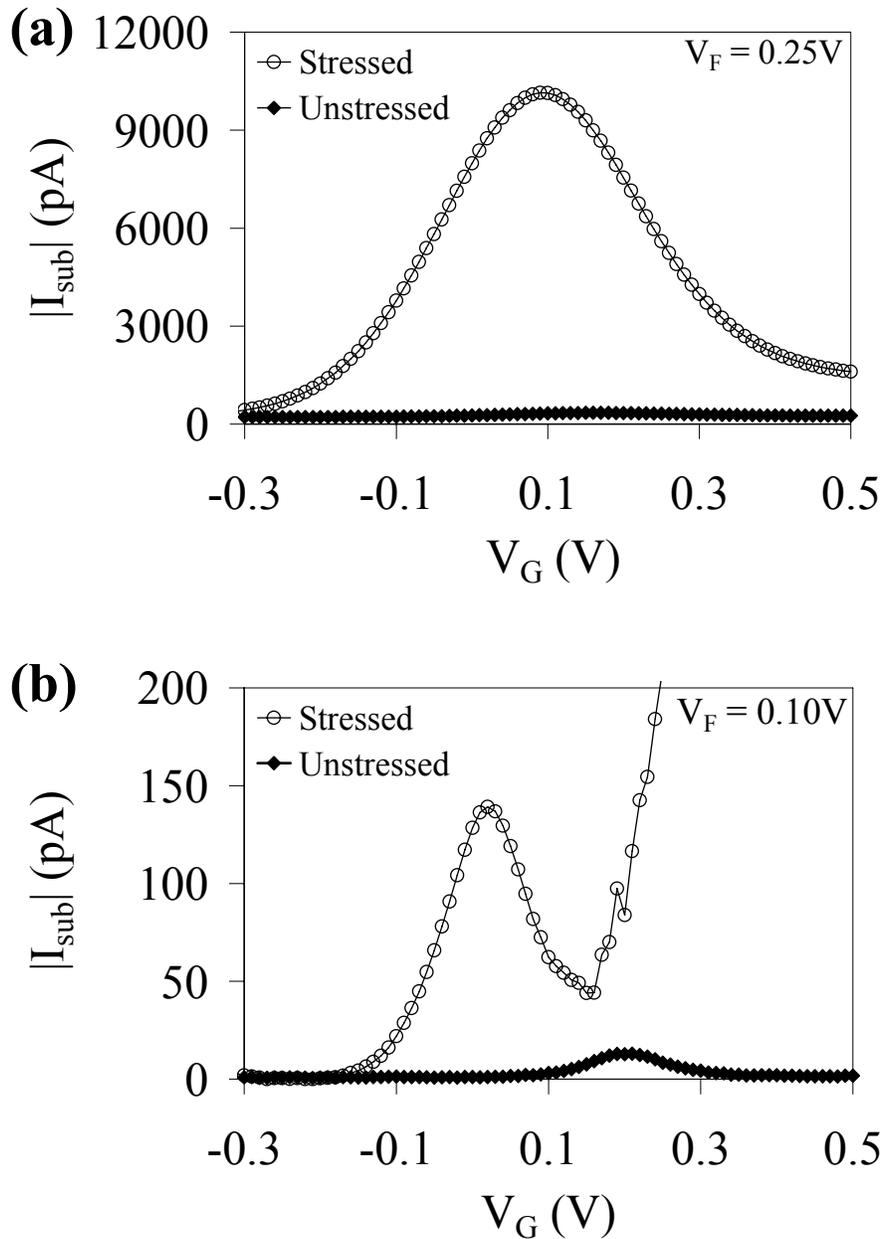
Figure 4.1: Pre- and Post-NBTS DC-IV measurements on (a) 7.5nm $SiO_2$ pMOSFET (-5.7v at 140°C for 210,000 seconds) and (b) 2.3nm PNO pMOSFET (-2.6V at 140°C for 180,000 seconds).
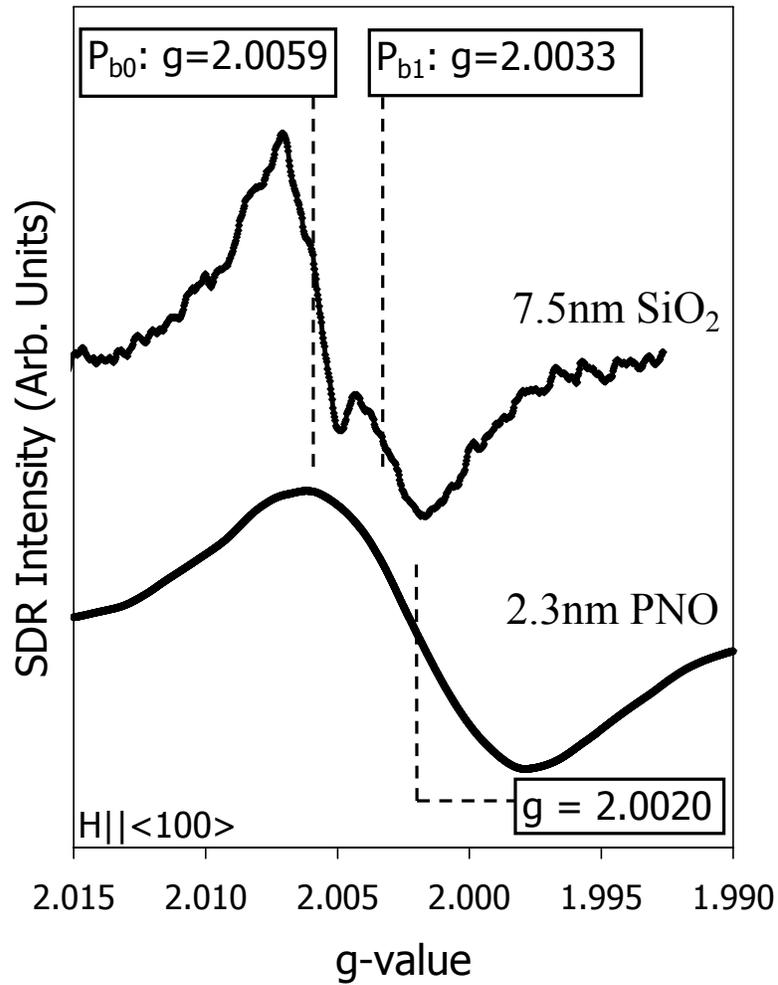
Figure 4.2: Optimized SDR traces of NBTI-induced defects in 7.5nm $SiO_2$ and 2.3nm PNO-based devices as a function of g-value. NBTI generates different defects in $SiO_2$ and PNO devices.

## 4.3 PNO Defect: Physical Location

The relationship between a defect's experimentally observed g-value and the orientation of the applied magnetic field is an indication of the defect's local environment. Figure 4.3 illustrates the g-value versus device orientation with respect to the applied magnetic field for the $P_{b0}$ center as well as for the new PNO defect. In this figure, $\theta$ is defined as the angle between the magnetic field vector and the <100> surface normal. Figure 4.3(a) illustrates the $P_{b0}$ g-value orientation dependence adapted from earlier ESR work.[110] The $P_{b0}$ signal splits into three lines (each corresponding to a <111> direction) that are clearly a function of orientation (anisotropic).[110] If a defect was located precisely at the interface, one would expect it to have an orientation dependent g-value because of the long range order present precisely at the interface.[15,93] The  would reflect the symmetry of the defect.[15,93] Rotation of the device in the magnetic field changes the alignment of the local magnetic field experienced by the defect relative to the applied field. This alters the defect's resonance condition resulting in an anisotropic g-value.[15,93] Figure 4.3(b) illustrates the g-value orientation dependence of the NBTI-induced g = 2.0020 signal in the PNO devices. The g = 2.0020 signal's g-value is independent of the device orientation (isotropic). If a defect was located in an amorphous dielectric, one would expect the defect to have an equal distribution in all orientations.[15,93] In this case, rotation of the device in the magnetic field alters the local magnetic fields of all the defects, but the total effect would be on average zero, resulting in an unchanging g-value.[15,93] Therefore, our observation of an isotropic g = 2.0020 (figure 4.3(b)) is a strong indication that the dominant NBTI-induced defect in the PNO devices is located within the amorphous dielectric. However, the NBTI-induced increase in both the DC-IV peak and the SDR spectrum indicates that this defect is
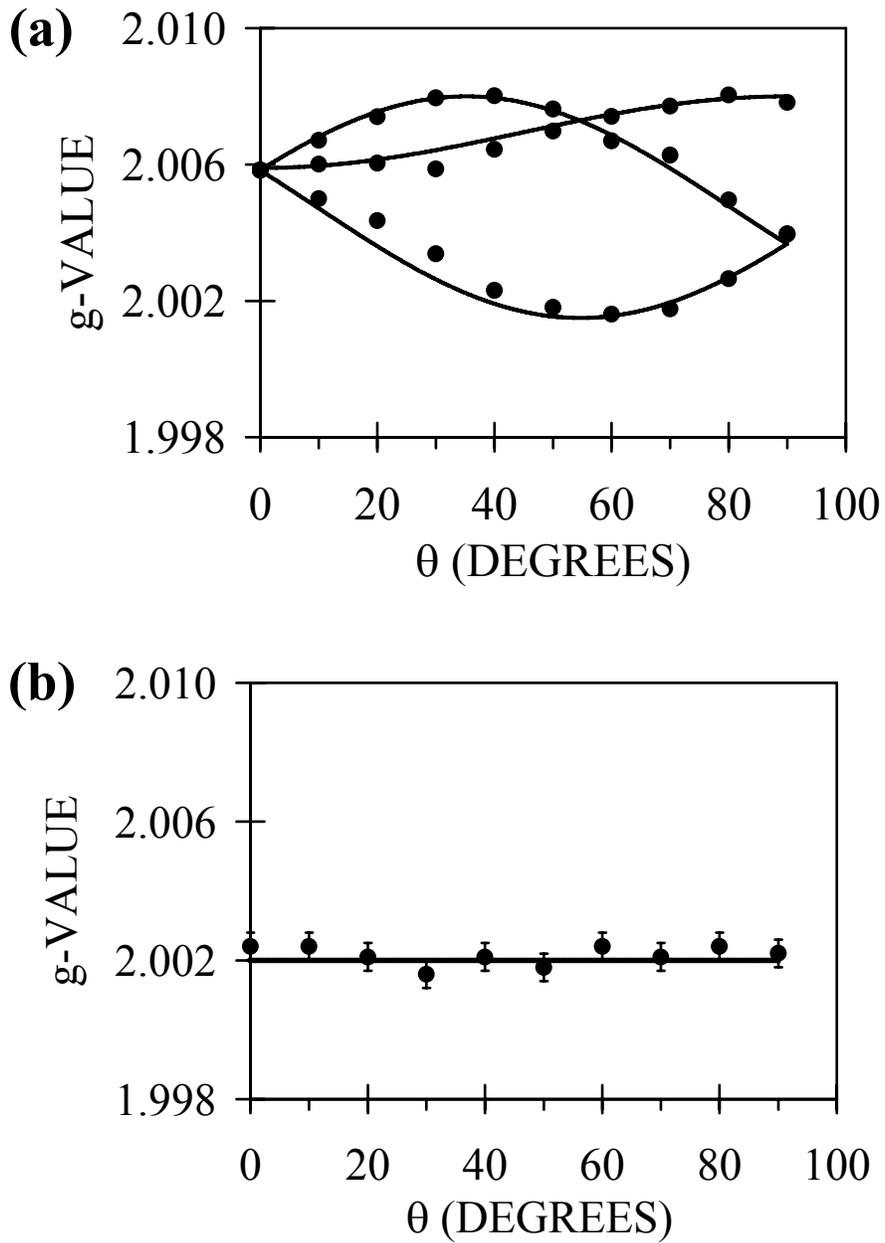
Figure 4.3: (a) Adapted ESR g-value angular dependence for the Si/SiO$_2$ P$_{b0}$ interfacial defect [Ref. 111] and (b) SDR g-value angular dependence for the NBTI-induced 2.3nm PNO defect. The PNO defect's isotropic g-value is an indication that the defect is physically located in the "near-interface" region.

located close enough to the interface to participate in recombination. Therefore, we conclude that the defect is located within the dielectric but close (probably ≤ 1nm) to the interface (the "near-interface" region). However, we also note that in these 2.3 nm PNO devices, the "near-interface" region may account for a large percentage of the gate dielectric.

## 4.4 PNO Defect: Participation in SDR and SDT

This section examines the impact of the source/drain to substrate forward bias ($V_F$) on the EDMR sensitivity of the PNO defect. We find that increased sensitivity is linked to the PNO defect's participation SDT. The effects of $V_G$ on the SDT and SDR phenomena are also explored.

Figure 4.4 illustrates the post-NBTS magnetic resonance spectra for a 2.3nm pMOSFET taken with $V_F$ = -0.2V and $V_F$ = +0.2V. In these measurements, the magnetic field is parallel to the <100> surface normal. Both spectra clearly show the generation of the same PNO defect (≈ 14G wide signal at g = 2.0020 ± 0.0003). The spectrometer gain for the $V_F$ = -0.2V spectrum is 100 times larger than the gain of the $V_F$ = +0.2V spectrum. Magnetic resonance measurements utilize microwave irradiation to satisfy the ESR resonance condition. In these measurements, the microwaves induce a (+0.2V) bias between the source/drain to substrate diode. When a source/drain to substrate bias ($V_F$) of -0.2V is applied to compensate for the microwave-induced biasing, the diode is completely turned off and the device substrate current is only the tunneling current. Thus, the spectrum observed with $V_F$ = -0.2V is a spin-dependent tunneling current

through the gate dielectric. However, when $V_F = +0.2V$ the source/drain to substrate diode is turned on (sufficient numbers of interfacial electrons and holes) and the device substrate current is orders of magnitude larger, the current is dominated by recombination. Thus, the spectrum observed with $V_F = +0.2V$ corresponds to spin-dependent recombination current through interface traps. The observation of the same defect signature at $V_F = -0.2V$ and at $V_F = +0.2V$ indicates that *the same defect participates in both spin-dependent tunneling and spin-dependent recombination*.

To further examine the role of the PNO defect in SDT and SDR phenomena, we have made extensive SDT/SDR measurements as a function of $V_F$. These measurements are shown in figure 4.5(a) as the normalized SDR and SDT amplitudes as a function of $V_F$. The normalization is achieved by dividing the spin-dependent modification to the tunneling and recombination currents ($\Delta I$) by the non-spin-dependent DC current (I). We observe that the $\Delta I/I$ response steadily increases as $V_F$ is decreased. The largest $\Delta I/I$ effect is seen for $V_F \leq -0.2V$. As discussed above, for these values of $V_F$ the source/drain to substrate diode is turned off and the observed spectrum is dominated by SDT. For larger positive values of $V_F$, the source/drain to substrate diode is turned on and the observed spectrum is dominated by SDR. In an attempt to delineate between SDR and SDT, figure 4.5(b) plots the modification to the spin-dependent currents ($\Delta I$) as a function of $V_F$. The $\Delta I$ response is relatively constant for negative values of $V_F$ and increases sharply for positive values of $V_F$. Unlike $\Delta I/I$, the $\Delta I$ of the SDT current should be nearly independent of $V_F$ (it should only depend upon the gate voltage). Therefore, the increase in $\Delta I$ for positive values of $V_F$ is due to an increase in SDR current. Thus, the spin-dependent current is dominated by tunneling for negative values of $V_F$ and by recombination for larger positive values of $V_F$. It is difficult to determine the exact transition between SDT and SDR. However,
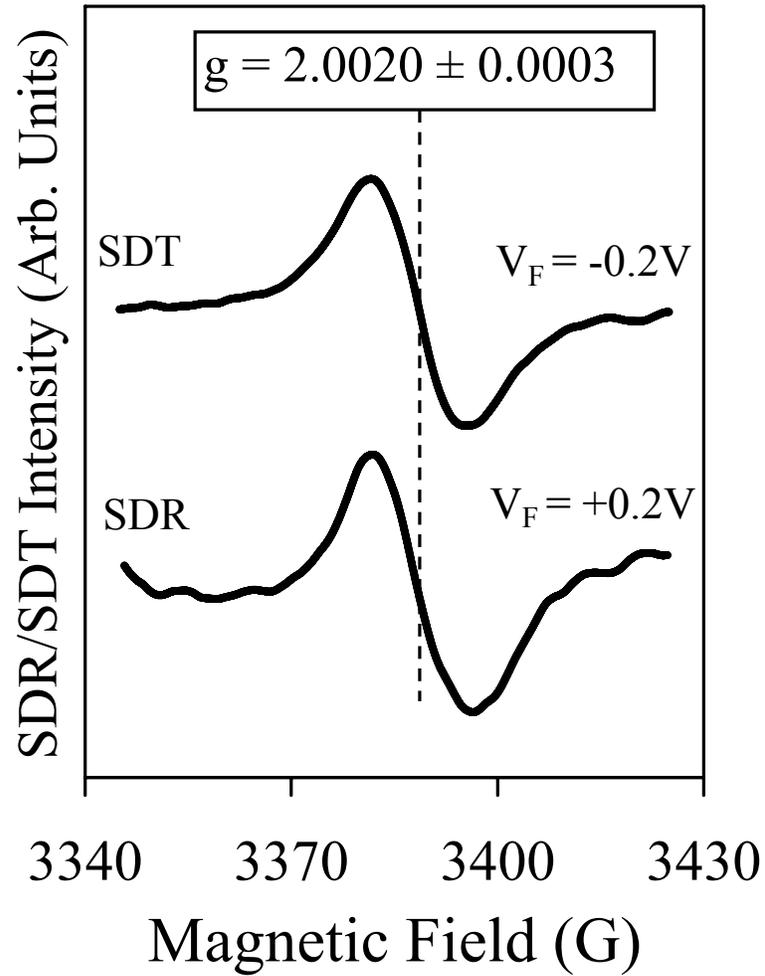
Figure 4.4: SDT ($V_F = -0.2V$) and SDR ($V_F = +0.2V$) spectra of PNO defect. Both measurements clearly show the generation of a single dominating signal at g = 2.0020. The spectrometer gain is 100 times greater for the $V_F = -0.2V$ spectrum.
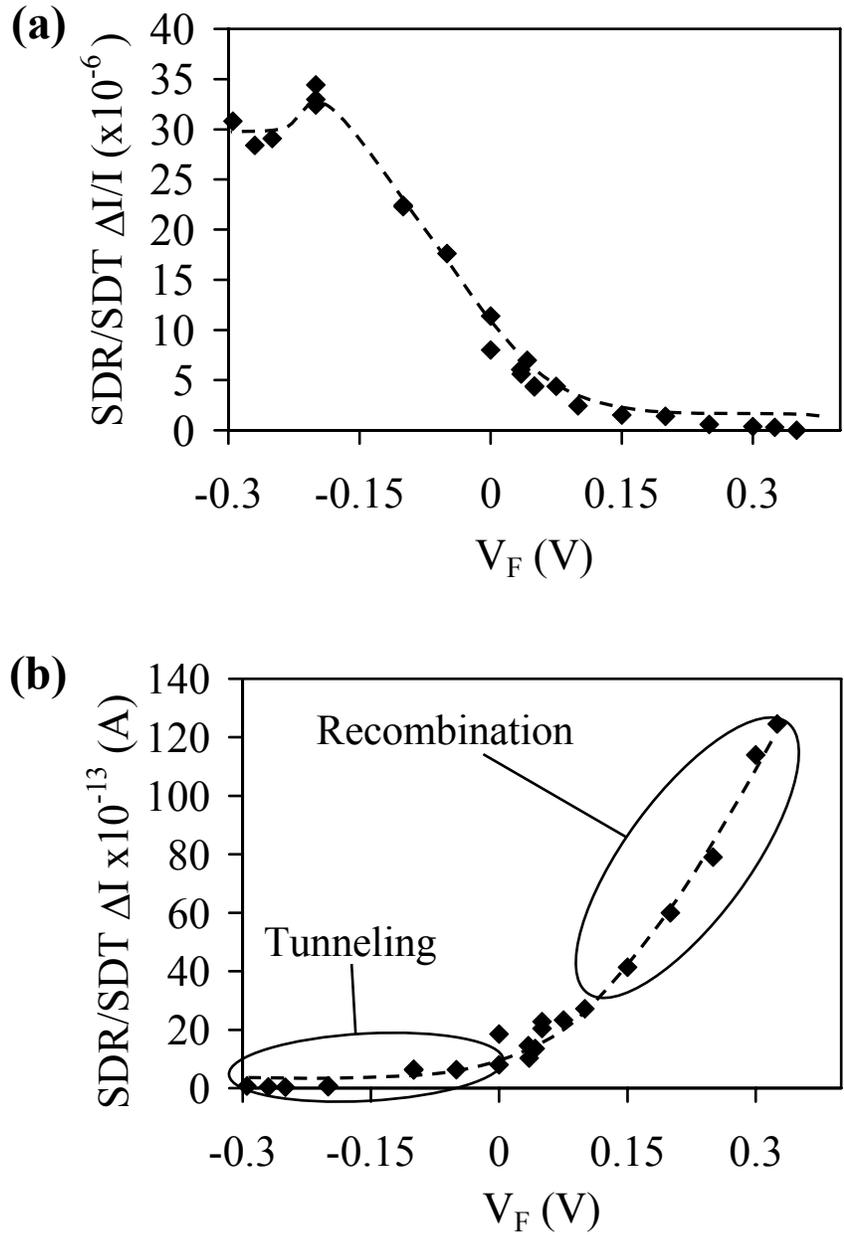
Figure 4.5: (a) Normalized size of the SDR and SDT effect for the PNO defect as a function of $V_F$. The normalization is plotted as the modification to the SDR/SDT current ($\Delta I$) divided by the DC source/drain to substrate diode current (I). (b) The modification to the SDR/SDT current ($\Delta I$) as a function of $V_F$. These figures illustrate that the PNO defect clearly participates in both SDT and SDR phenomena.

since the $\Delta I$ value increases dramatically as $V_F$ is increased ($\approx$ 25x larger at $V_F = +0.1$, $\approx$ 60x larger at $V_F = +0.2V$, and $\approx$ 120x larger at $V_F = +0.3V$), we somewhat arbitrarily take SDT as the dominant mechanism for $V_F < +0.1V$ and SDR as the dominant mechanism for $V_F > +0.1V$. Although our approach to separating the relative contributions of SDT and SDR is imprecise, we believe the argument is conclusive.

We have also examined the effect of $V_G$ on the SDR and SDT phenomena. Figure 4.6 illustrates the SDR ($V_F = +0.2V$) and SDT ($V_F = -0.2V$) $\Delta I/I$ responses as a function of gate voltage ($V_G$). Since interface recombination is largest in a depletion region (equal numbers of electrons and holes at the interface)[13,90], the SDR $\Delta I/I$ should be largest for the gate voltages corresponding to a depleted channel. The SDR $\Delta I/I$ should be at a minimum when $V_G$ corresponds to an accumulated or inverted channel (unequal numbers of electrons and holes at the interface). This is exactly what we observe. The SDR $\Delta I/I$ is broadly peaked near depletion ($V_G \approx +0.45V$) and is consistent with the expected SDR behavior. However, the SDT $\Delta I/I$ response is different; it is a narrower function of $V_G$ and exhibits negative $\Delta I/I$ values. Since SDT should only occur when $V_G$ bends the bands to an energetically favorable alignment of tunneling trap levels, one would expect the $\Delta I/I$ response to be narrower for SDT than for SDR. The negative $\Delta I/I$ values correspond to a reversal in the measured SDT signal polarity and sign of the DC current. We interpret this reversal in SDT signal polarity to a band alignment favorable for a reversal in direction of the SDT current.
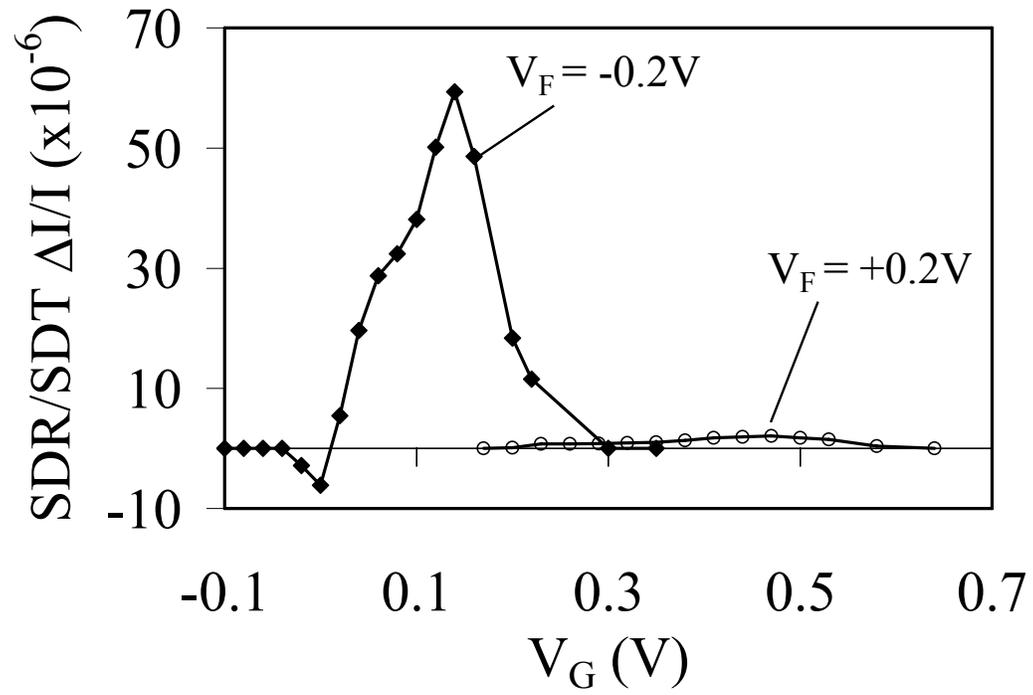
Figure 4.6: Normalized size ($\Delta I/I$) of the SDR and SDT effects as a function of $V_G$ for $V_F = +0.2V$ and $V_F = -0.2V$.

Figure 4.7 illustrates the device tunneling ($V_F = -0.2V$) and recombination ($V_F = +0.2V$) currents along with the SDT ($V_F = -0.2V$) and SDR ($V_F = -0.2V$) $\Delta I$ responses of the PNO defect as a function of $V_G$. We observe that the peak in the device tunneling current closely corresponds to the peak SDT $\Delta I$ response (figures 4.7(a) and (b)) and that the peak in the device recombination current closely corresponds to the peak in the SDR $\Delta I$ response (figures 4.7 (c) and (d)). This correspondence is another strong indication that the PNO defect acts as both the dominant tunneling center and interface state in these devices.

It is important to note that the maximum size of the SDT effect ($\Delta I/I \cong 6 \times 10^{-5}$) is much larger than the SDR effect ($\Delta I/I \cong 2 \times 10^{-6}$) observed in these PNO samples. The increased size of the SDT effect provides a considerable improvement in measurement sensitivity over SDR. Also, the $\Delta I/I$ SDT value we measure is likely smaller than what we would observe if more microwave power were available in our system because the signal amplitude is still increasing linearly at the maximum available microwave power (150mW) of the spectrometer. Large SDR effects are typically explained in terms of a pairing two spins (KSM model).[97] In this case, the spins would be the charge carriers and the deep level defects spins. The size of the observed SDT effect is more consistent with that predicted by a KSM-like model in which there is a pairing between tunneling charge carriers and charge carriers trapped in PNO defect tunneling centers. However, the size of the observed SDR effect is smaller than the size predicted by the KSM model and smaller than most SDR measurements reported in the literature.[96] The size of the SDR effect in the PNO devices is more consistent with that predicted by the Lepine[95] model for SDR in which recombination occurs without a pairing of spins. This implies that when the PNO defect is participating in interfacial recombination, there is little coupling between conduction or valence
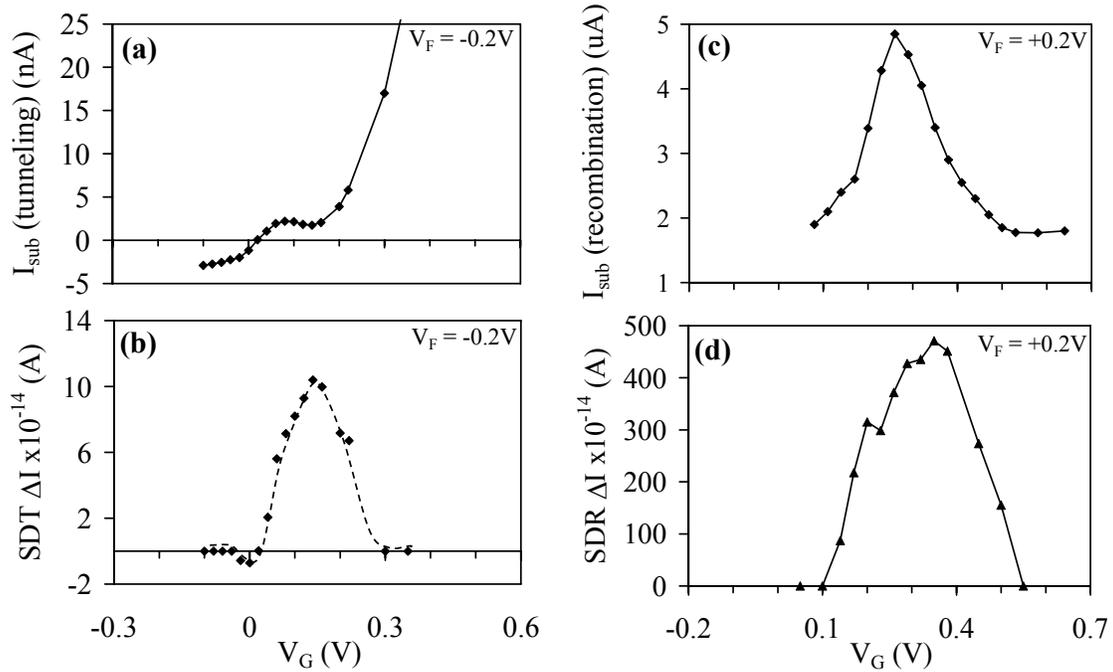
Figure 4.7: DC substrate currents and modifications to the spin-dependent currents ($\Delta I$) for SDT with $V_F$ = -0.2V (a) and (b) and for SDR with $V_F$ = +0.2V (c) and (d). The close correspondence between the peaks in the substrate currents and $\Delta I$ values is an indication that the PNO defect dominates both the device tunneling centers (a) and (b) and interfaces states (c) and (d).

band charge carriers and deep level interfacial defect spins prior to the actual recombination event. This correspondence between the PNO defect's recombination response and the Lepine model may be consistent with the fact that the PNO defects are not located at the interface.

Considering that the PNO devices' gate dielectrics are relatively thin (2.3nm), it is possible that the SDT mechanism involves an interface trap to interface trap tunneling mechanism similar to that proposed by Nicollian[114] to describe low-voltage stress-induced leakage currents. We have already shown that the PNO defects are physically located not at the interface, but in the "near-interface" region of the dielectric. Therefore, we speculate that our SDT measurements involve a spin-dependent trap-assisted variation of the interface state to interface state tunneling mechanism which involves tunneling through the gate dielectric through NBTI-induced PNO "near-interface" defects.

## 4.5 PNO Defect: Density of States

We have shown that large variations in $V_F$ can change the nature of the observed spin-dependent current from tunneling to recombination. However, restricting $V_F$ to values in which SDR is the dominant mechanism ($V_F \geq +0.1V$) also allows for a very useful comparison between the thicker $SiO_2$ and thinner PNO devices. Since SDR is a spin-dependent modification to the DC-IV measurement and $V_F$ controls the DC-IV recombination energy window, or the energy range over which interface traps may contribute to the effect, differences in the size of the SDR effect as a function of $V_F$ reflect differences in the densities of states of thee different defects in these two types of devices.

Figure 4.8 illustrates the size of the post-NBTS SDR effect as a function of source/drain to substrate forward bias ($V_F$) for the $SiO_2$ and PNO devices. For the 7.5nm $SiO_2$ devices, the SDR derived $\Delta I/I$ is broadly peaked at $V_F \approx +0.25V$. This relatively weak dependence on $V_F$ is consistent with a *relatively* flat density of states near the middle of the band gap. This is so because increasing $V_F$ increases the energy window in which recombination occurs.[13] If the density of states near the middle of the band gap is *relatively* flat (like that expected in an interface dominated by $P_{b0}$ and $P_{b1}$ defects), increasing $V_F$ allows more interface states to participate in the recombination process. Thus, the size of the SDR effect (seen via $\Delta I/I$) increases. This behavior continues until $V_F$ is large enough that the source/drain to substrate forward bias diffusion current overwhelms the recombination current and the denominator in $\Delta I/I$ dominates. Thus, for an interface that is dominated by defects with a relatively flat density of states ($P_{b0}/P_{b1}$), the SDR $\Delta I/I$ should be broadly peaked as a function of $V_F$. (Note that our conclusions here are qualitative to semi-quantitative in detail; the combined $P_{b0}$ and $P_{b1}$ density of states is not precisely flat but a *relatively* flat distribution.) However, the SDR $\Delta I/I$ response is quite different for the PNO devices. In the PNO case, $\Delta I/I$ steadily decreases as $V_F$ is increased. This is consistent with a narrower density of states fairly near the middle of the band gap. Following the arguments above, if the density of states near the middle of the band gap is narrowly peaked, increasing $V_F$ beyond a point, approximately corresponding to the peak width,
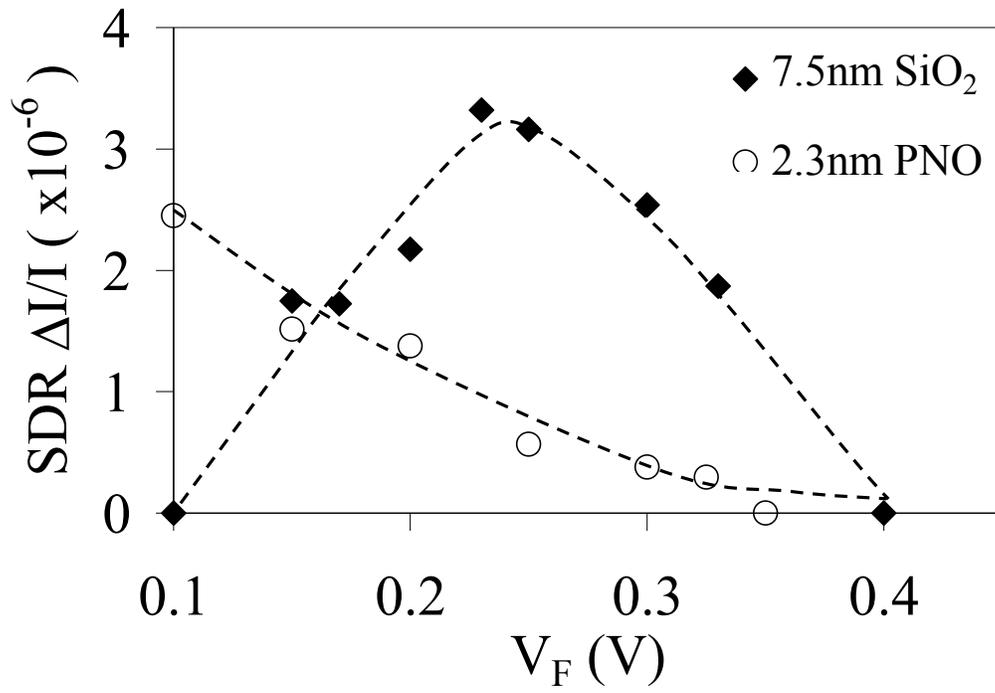
Figure 4.8: Normalized size ($\Delta I/I$) of the SDR effect as a function of $V_F$ for the $SiO_2$ and PNO devices. The different responses indicate different densities of states.

does not increase the number of defects participating in recombination (the number of defects in essentially constant). Instead, increasing $V_F$ only increases the forward bias diffusion current and the denominator of the $\Delta I/I$ term dominates. Thus, for an interface with a narrowly peaked density of states near the middle of the band gap, the SDR $\Delta I/I$ should steadily decreases as $V_F$ is increased.

Since our SDR measurements utilize a spin-dependent modification to the DC-IV measurement, DC-IV theory is useful in understanding this result.[13,14] Using the Shockley-Read-Hall model for recombination, Fitzgerald and Grove[13] showed the DC-IV substrate current ($I_{sub}$) is given by:

$$I_{SUB} = Aq\sigma_s v_{th} \left[ \int_{E_V}^{E_C} \frac{D_{it}(E)dE}{p_S + n_S + 2n_i \cosh\left(\frac{E-E_i}{kT}\right)} \right] \left[ p_S n_S - n_i^2 \right] \tag{4.1}$$

where $p_S$ and $n_S$ are the hole and electron concentrations at the surface, E is the energy level of the surface recombination centers, $E_i$ is the intrinsic Fermi level, and $E_C$ and $E_V$ are the energies of the conduction and valence band edges. $p_S$ and $n_S$ for a pMOS device are given by

$$p_S \cong \frac{n_i^2}{N_D} \exp\left(\frac{-q\phi_S}{kT}\right) \exp\left(\frac{q|V_F|}{kT}\right) \tag{4.2}$$

$$n_S \cong N_D \exp\left(\frac{q\phi_S}{kT}\right) \tag{4.3}$$

where $N_D$ is the substrate doping and $\phi_S$ is the surface band bending. Note that increasing $V_F$ between the source/drain to substrate p/n junction increases the number of minority carrier holes ($p_S$) available for recombination (in a pMOS device). An examination of the integral in equation

(4.1) helps explain the $V_F$-derived active recombination window. For $|E-E_i|$ values small enough to ensure that the $p_S+n_S$ term is greater than the $2n_i\cosh[(E-E_i)/kT]$ term, the denominator of the integral is nearly constant and relatively small. However, as $|E-E_i|$ increases, the $\cosh[(E-E_i)/kT]$ term blows up and overwhelms the $V_F$ derived $p_S+n_S$ term. This can be thought of as effectively closing the recombination window. Careful analysis of the integrand of equation (4.1) using equations (4.2) and (4.3) leads to an effective DC-IV and SDR recombination energy window of $\sim q|V_F|$, centered about the middle of the band gap.

Computer simulations of the DC-IV recombination current using equations 4.1-4.3 were carried out for various values of $V_F$ and various densities of states. By dividing the simulated DC-IV peak current by the baseline substrate current, an analogous $\Delta I/I$ behavior is observed. Figure 4.9(a) illustrates the simulated $\Delta I/I$ behavior for a 7.5nm gate oxide with a flat density of states through the gap. Figure 4.9(b) illustrates the simulated $\Delta I/I$ behavior for a 2.3nm gate oxide with a very narrowly peaked density of states centered about the middle of the gap. The insets of both figures show the simulated densities of states. The similarities between simulated $\Delta I/I$ (figure 4.9) and measured SDR $\Delta I/I$ (figure 4.8) suggests a common origin. The DC-IV derived $D_{it}$ values as a function of $V_F$ for the $SiO_2$ and PNO devices are also consistent with this trend. $D_{it}$ values, averaged over the energy window, for the $SiO_2$ device (figure 4.10(a)) are approximately constant as $V_F$ is increased while the $D_{it}$ values, averaged over the energy window, for the PNO devices (figure 4.10(b)) decreases as $V_F$ is increased. This trend is what one would anticipate from our above analysis.

Recently, Krishnan et al.[5] and Stathis et al.[59] have reported results which suggest different NBTI-induced density of states in $SiO_2$ and PNO-based devices. Stathis et al.[59] speculate that the addition of nitrogen changes the dangling bond structure of the NBTI-induced
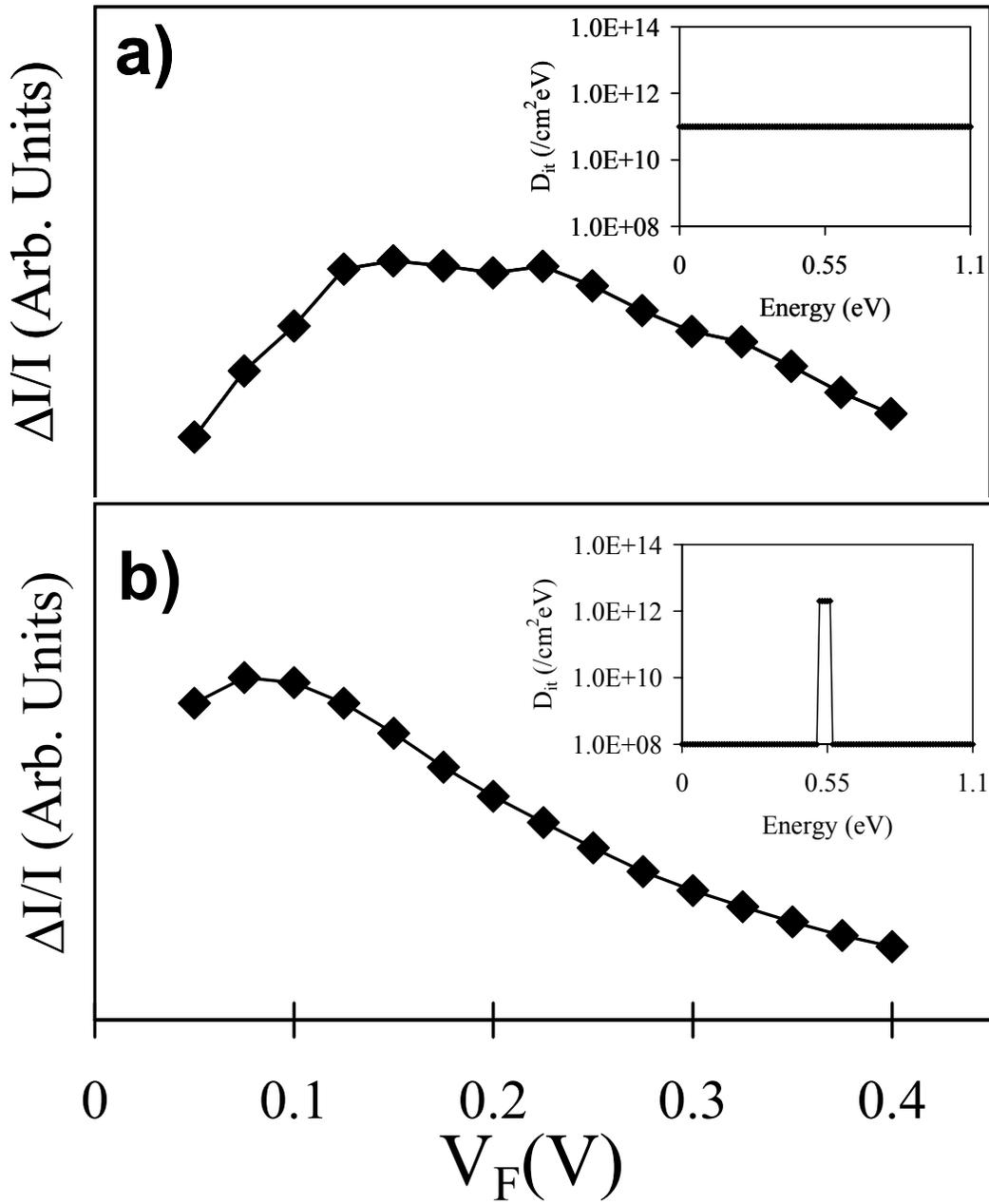
Figure 4.9: Simulated ΔI/I DC-IV recombination current as a function of $V_F$ for (a) 7.5nm $SiO_2$-device with a flat density of states through the gap and (b) 2.3nm PNO device with a very narrow density of states centered about the middle of the gap. The figure insets show the simulated densities of states in each case.
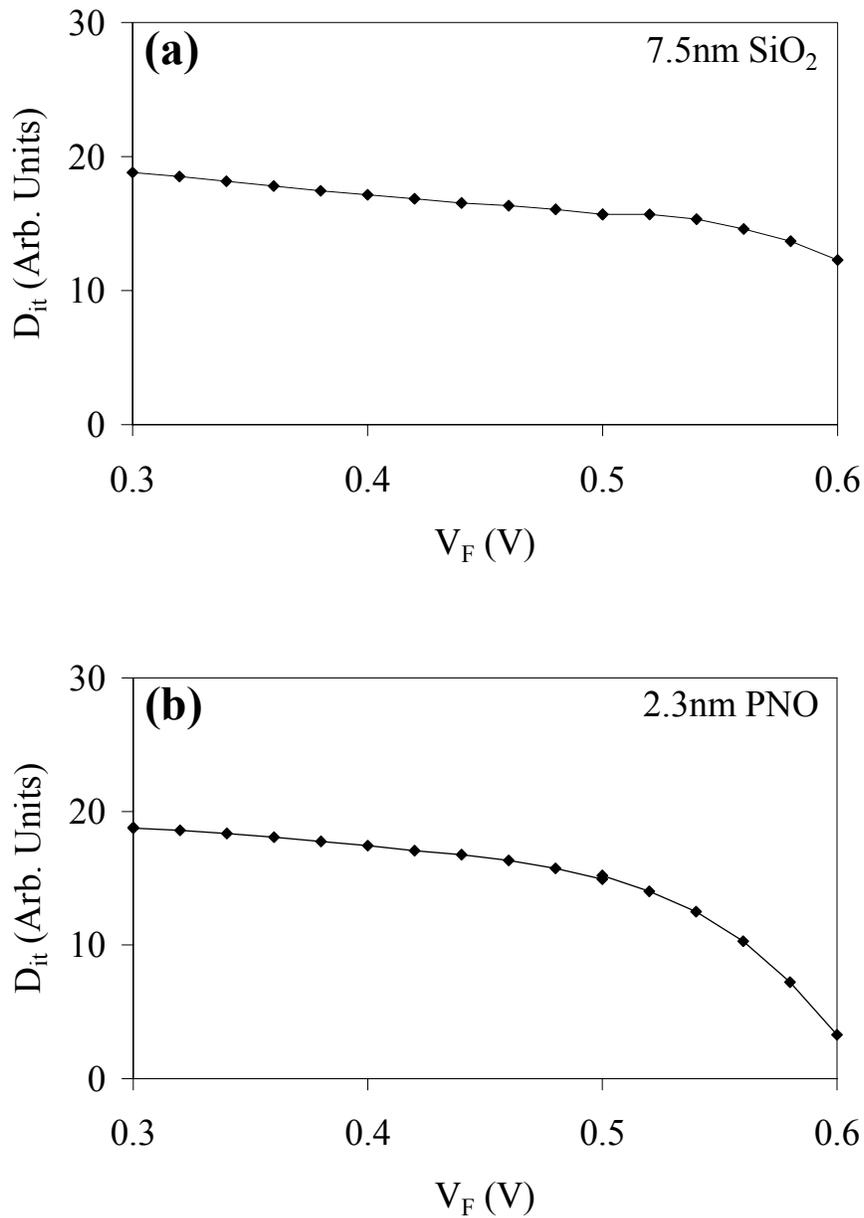
Figure 4.10: DC-IV derived average $D_{it}$ values over the energy window for the (a) $SiO_2$ and (b) PNO devices as a function of source/drain to substrate diode forward bias ($V_F$). The $D_{it}$ values were obtained from DC-IV measurements and equation (1). As $V_F$, and the recombination energy window, increases, $D_{it}$ for the $SiO_2$ device is essentially constant while $D_{it}$ for the PNO device decreases. This is consistent with the PNO defect having a narrowly peaked density of states.

defects. Our observations are consistent with this conclusion. (However, in detail, our conclusions differ with regard to density of states.) Our observations directly demonstrate that there are different dangling bond defects in PNO- and $SiO_2$-based devices and, as discussed in the next section, the PNO defects involve silicon atoms coupled to nitrogen atoms. Our observations also suggest a narrower density of states for the PNO defect than the $P_{b0}/P_{b1}$ defects in $SiO_2$ devices. Figure 4.11 illustrates a schematic representation of the density of states of NBTI-induced defects in thicker $SiO_2$ and thinner PNO-based devices. ESR measurements indicate that the $P_{b0}/P_{b1}$ composed density of states in thicker $SiO_2$ systems approximately corresponds to the schematic sketches of figure 4.11(a).[24,25,103,105-109] The $P_{b0}/P_{b1}$ effective density of states would be the summation of the $P_{b0}$ and $P_{b1}$ defect levels yielding a *relatively* flat density of states near the middle of the band gap as schematically shown in figure 4.11(b). Densities of states qualitatively similar to this pattern are typically reported in measurements of Si/$SiO_2$ interface traps.[115] Our results strongly suggest that the PNO defect has a narrower density of states near the middle of the band gap (figure 4.11(c)). (The schematic sketch does not show the PNO defect trap levels extending into the dielectric for simplicity of presentation.) These measurements cannot distinguish between donor or amphoteric nature of the defects. However, the observation of a very narrow density of states and the known shift in threshold voltage are both consistent with, but do not prove, that NBTI-induced defects in thin nitrided devices have a narrow donor level, as has been suggested recently.[5]

**Silicon Bandgap Energy**
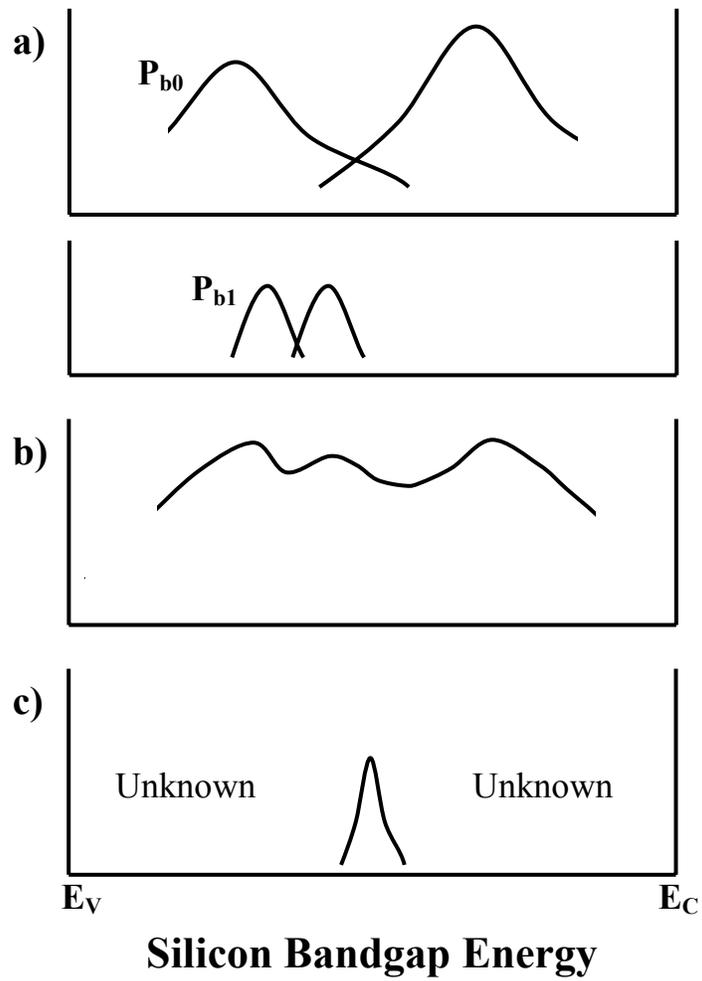
Figure 4.11: Schematic representation of the (a) Si/SiO$_2$ P$_{b0}$ and P$_{b1}$ interface defect densities of states and (b) the effective P$_{b0}$/P$_{b1}$ density of states illustrating the relatively flat distribution near the middle of the band gap. (c) Illustrates a schematic representation of the PNO defect's density of states near the middle of the band gap.

## 4.6 PNO Defect: $^{29}$Si Hyperfine Identification (K$_N$ centers)

The high sensitivity observed in the SDT measurement provides the means to examine the local environment of the PNO defect via hyperfine interactions with nearby magnetic nuclei. Figure 4.12 illustrates the wide scan post-stress SDT spectra ($V_F = 0.0V$) of the PNO defect with the magnetic field perpendicular to the (100) surface of the device. Extensive signal averaging plus the enhanced sensitivity of SDT has allowed for the observation of two weak satellite lines as well as a third small signal shifted $\approx$ 45G below the central line. While the identity of the third smaller signal is not yet known, the observation of the two satellite side peaks and the g = 2.0020 central signal provides the necessary information to identify the physical and chemical nature of the PNO defect.

Both of the weak satellite lines have a peak-to-peak width of approximately 25G and are virtually identical in amplitude. The low field line is 183G below the central line and the high field line is 166G above the central line (349G splitting). Each of the side peaks have an integrated intensity of $\approx$ 2% of the dominant central signal. The relative sizes of the central signal and side peaks *unequivocally identifies the NBTI-stressed defect as a silicon dangling bond*. Most silicon nuclei (95.3%) are not magnetic; however, a small fraction (4.7% $^{29}$Si) are magnetic and have a nuclear spin of ½.[93] Thus, nearly all (95.3%) of the silicon dangling bond spectrum would appear as a single dominant signal while a small fraction (4.7%) of the silicon dangling bond spectrum would appear as two satellite side peaks. Each of these satellite side peaks would appear as $\approx$ 2.3% of the integrated intensity of the central signal. Within experimental error, this is exactly what is observed for the PNO defect. (No other element could provide this 2.3% / 95.3% pattern.
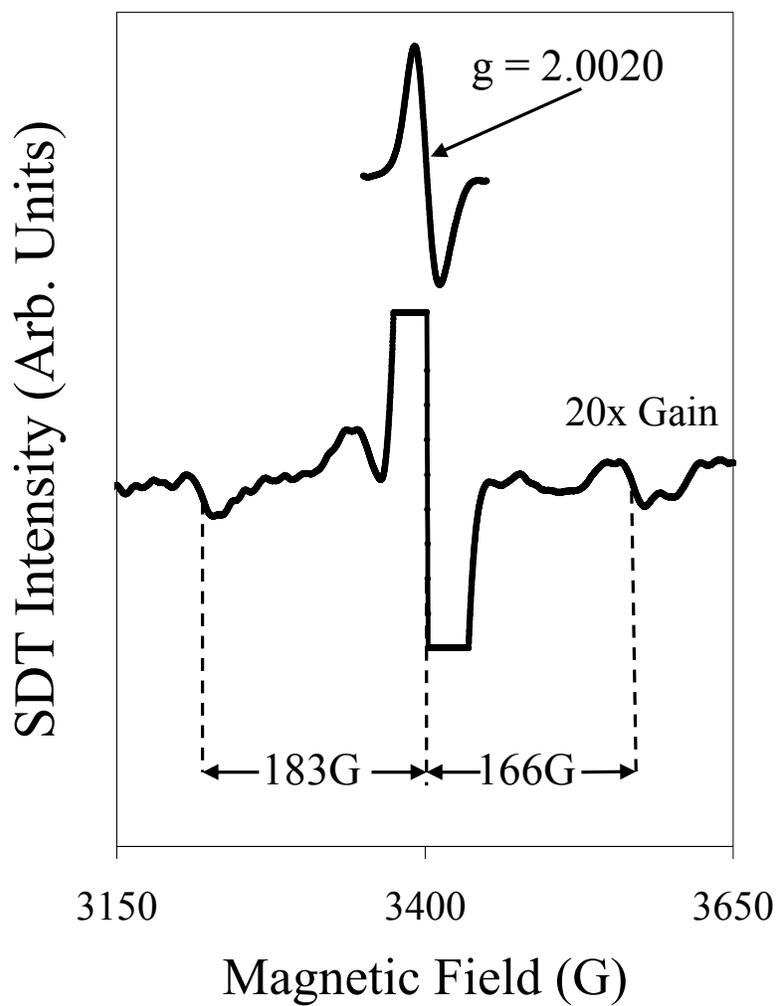
Figure 4.12: Wide scan SDT spectra of the PNO defect. Increased spectrometer gain (20x) and extensive signal averaging reveals two [29]Si hyperfine side peaks.

The small asymmetry in the hyperfine side peak splitting occurs when the electron-nuclear interaction is large.[93] The asymmetry can be calculated by the Breit-Rabi correction: $\delta \approx (\Delta H)^2 / 4H_0$, where $\delta$ is the asymmetry, $\Delta H$ is the hyperfine splitting, and $H_0$ is the resonant field without the nuclear interaction.[93] The observed hyperfine asymmetry (8.5G) is consistent with a calculated Breit-Rabi correction ($\Delta H = 349G$ at $H_0 = 3400G$) of $\delta \approx 9G$.

The hyperfine interaction is generally expressed in a three by three matrix, A, often called the hyperfine "tensor".[93] For a defect with axial symmetry, the parallel ($A_{\parallel}$) and perpendicular ($A_{\perp}$) components of this "tensor" can be related to the defect's electronic wave function in terms of an isotropic ($A_{iso}$) and anisotropic ($A_{aniso}$) component. $A_{iso}$ and $A_{aniso}$ are measures of the s- and p-character of the defect's wave function respectively.[93] Our observations allow for a moderately accurate measurement of $A_{iso}$ and a very crude estimate of $A_{aniso}$.[93,116] For the ideal case, $A_{iso}$ and $A_{aniso}$ are given[116] by

$$A_{iso} = \Delta H - \frac{1}{2} A_{aniso} \qquad (4.4)$$

$$A_{aniso} = \frac{2}{3} (\text{hyperfine line width}) \qquad (4.5)$$

The exact contributions of the anisotropic hyperfine coupling to the width of the hyperfine lines is difficult to determine because of additional broadening due to super-hyperfine interactions with second nearest neighbor nitrogen atoms which each have a nuclear magnetic moment and a nuclear spin of 1.[93,116] However, a rough upper limit on the hyperfine line width is given by the measured peak-to-peak line width (25G) while a rough lower limit is given by difference between the measured hyperfine line width and the central signal line width (25G - 14G = 11G).

This analysis yields a rather crude $A_{aniso} \approx (2/3)(11 \text{ to } 25G) \approx 12\pm5G$, and a more precise $A_{iso} = 349G - (12/2) = 343G$.

The s-character and p-character of the observed defect can be roughly estimated by comparing the measured $A_{iso}$ and $A_{aniso}$ values with the $A_{iso}$ and $A_{aniso}$ values calculated for 100% 3s and 100% 3p silicon wave functions.[93,116] The calculated $A_{iso}$ for a 100% 3s silicon wave function and $A_{aniso}$ for 100% 3p silicon wave function are 1639.3G and 40.75G respectively.[93] The measured $A_{iso} = 343G$ indicates that the s-character of the NBTI-stressed defect is about $343G/1639.3G \cong 21\%$, while the measured $A_{aniso} = 12\pm5G$ indicates that the p-character of the NBTI-stressed defect is of order $12\pm5G/40.75G \approx 29\pm12\%$. The sum of the s- and p-contributions to the defect's electronic wave function, or localization, is $50\pm12\%$. Note that this is a <u>very rough</u> estimate.

Table 4.I compares the measured center line width, g-value, and hyperfine line splitting of the PNO defect with other silicon dangling bond defects ($P_{b0}$, E′, and K centers) which might conceivably be present in these devices. As discussed above, $P_{b0}$ defects are interfacial silicon dangling bond defects in which the central silicon is back bonded to three other silicon atoms.[15,22-24,103] They, along with the closely related $P_{b1}$ defects, account for most of the Si/SiO$_2$ interface states in SiO$_2$ MOSFETs.[15,22-24,103] E′ centers are oxide silicon dangling bond defects in which the central silicon is back bonded to oxygen atoms.[117] They dominate the electronic properties of irradiated and high-field stressed SiO$_2$.[15,112,117] K centers are silicon dangling bond defects found in silicon nitride in which the central silicon is back bonded to nitrogen atoms.[116,118] They dominate charge trapping in Si$_3$N$_4$ films.[116,118,119] An examination of Table I reveals that the NBTI-stressed defect spectrum and the K center spectrum are very similar. Thus,

| | Centerline Width (G) | g-value* | Hyperfine Splitting (G) |
|---|---|---|---|
| $P_{b0}$ [23] | $\cong 3$ | 2.0059 | 105 |
| $E'_{\gamma}$ [50] | $\cong 2$ | 2.0005 | 424 |
| K center [49] | $\cong 14$ | 2.0028 | 358 |
| NBTI Defect ($K_N$ center) | $\cong 14$ | 2.0020 | 349 |

*For the E′, K, and $K_N$ centers this the simple zero-crossing g-value; but for $P_{b0}$, it represents the g at a specific magnetic field orientation . In these measurements, H ∥ <100> surface normal.

Table 4.1: Measured magnetic resonance parameters of important silicon dangling bond defects. The K center and $K_N$ center parameters are nearly the same.

we conclude that the PNO defect is a silicon dangling bond in which the silicon is back bonded to nitrogen atoms that we refer to as $K_N$ for NBTI.

The differences between the $K_N$ and K center spectra are small but clearly larger than experimental error. These small deviations are likely due to slightly different bonding environments and probably the larger band gap in the PNO dielectric. In $Si_3N_4$, the K center's nitrogen atoms are bonded almost exclusively to silicon atoms[116,118], while the SiON $K_N$ center's nitrogen atoms may be bonded to one or more oxygen atoms. This small change in second-nearest neighbor bonding and possibly the larger band gap (the gap in $Si_3N_4$ is about 5 eV) are very likely responsible for the small deviations we observe between the K and $K_N$ centers.

## 4.7 $K_N$ center: Implications to NBTI

### 4.7.1 Nitrogen-enhanced NBTI

The presence of the $K_N$ center in PNO devices indicates that fundamental differences in the dielectric chemistry strongly influence the electronic properties of the interface and near-interface regions. The bonding mismatch between Si and $SiO_2$ is almost certainly the main reason that $P_{b0}/P_{b1}$ defects exist. At a typical $Si/SiO_2$ interface, $P_{b0}/P_{b1}$ defects are passivated with hydrogen atoms. The relatively easy dissociation of the hydrogen atoms from $P_b$ precursors is thought to drive the interface defect generation in NBTI.[1,5,26,27] Our observations are certainly consistent with this mechanism of in thicker $SiO_2$-based devices.[19-21] However, this is not the

case in the thinner PNO-based devices. Since $P_{b0}/P_{b1}$ defects were not observed post-stress, the plasma-nitridation process must preferentially create large numbers of $K_N$ center precursors. (It is possible that weaker $P_{b0}/P_{b1}$ signals may be buried under the $K_N$ signal.) The presence of large numbers of $K_N$ precursors is presumably the main reason why nitridation so strongly enhances the NBTI response. Since it is known that K centers can be hydrogen passivated[120], it is reasonable to speculate that NBTS liberates hydrogen from the $K_N$ centers in much the same way that it is liberated from $Si/SiO_2$ $P_{b0}/P_{b1}$ defects. A hydrogenic depassivation mechanism would likely be subject to the same Reaction-Diffusion kinetics as has been proposed for thicker pure $SiO_2$-based devices. This may be likely the reason that much of NBTI theory correctly predicts aspects of the NBTI response in thin nitrided devices with only slight modifications.[12]

### 4.7.2 NBTI-induced Interface States vs. Bulk Traps

The observation of $K_N$ centers in both SDR (participation in interfacial recombination) and SDT (participation in tunneling) demonstrates that $K_N$ centers can act as both interface states and "near-interface" dielectric tunneling centers. Variations in the plasma-nitridation processing are thought to control the nitrogen profile within the gate dielectric.[121] We speculate that variations in the nitrogen profile (and the consequent proximity of the $K_N$ centers to the Si/SiON interface) are a major source of conflicting conclusions regarding NBTI-induced interface states and fixed oxide charge generation. If the PNO processing creates $K_N$ center precursors very near the interface, a post-NBTI electrical analysis would indicate interface state generation. But, if the PNO processing creates $K_N$ center precursors in the "near-interface" or bulk dielectric regions, a

post-NBTI electrical analysis would likely indicate some combination of interface state and bulk dielectric defect generation. So, it is possible for the same defect to be responsible for seemingly different aspects of the NBTI degradation. (In a 2.3nm gate dielectric, it may be difficult to distinguish between "near-interface" and "bulk" dielectric defects.)

### 4.7.3 NBTI: Fluorine Incorporation

Our $K_N$ defect observations may also help explain somewhat puzzling observations regarding fluorine's impact on NBTI. In thicker $SiO_2$ devices, fluorine incorporation is thought to "toughen up" the interface by replacing the weaker hydrogen passivation of $P_b$ centers (Si-H) with a stronger fluorine passivation (Si-F).[122,123] The stronger passivation is thought to be the reason that fluorine incorporation reduces NBTI in thicker $SiO_2$ devices.[43,44] However, the same fluorine incorporation in nitrided devices is observed to have little or no effect on NBTI.[124] The realization that NBTI in PNO devices creates $K_N$ defects (not primarily interfacial $P_b$ centers) may help explain this. The introduction of fluorine in nitrided devices probably does replace some interfacial Si-H bonds with Si-F bonds. However, interfacial Si-H depassivation does not dominate NBTI in these devices. If the fluorine incorporation in nitrided devices does not passivate the dominating NBTI-induced defects, it will not be effective in suppressing NBTI.

## 4.8 Summary

We have employed purely electrical DC-IV measurements as well as SDR and SDT magnetic resonance measurements on 7.5nm $SiO_2$ and 2.3nm PNO pMOSFETs. Our results indicate that the dominating NBTI-induced defects in the $SiO_2$ and PNO devices are different. NBTI in $SiO_2$ devices is dominated by $P_{b0}$ and $P_{b1}$ Si/$SiO_2$ interfacial silicon dangling bond defects. NBTI in the PNO devices is dominated by $K_N$ centers. Our measurements show that the $K_N$ centers are located in the "near-interface" region and they participate in both SDR and SDT phenomena. (The "near-interface" region could be a large fraction of a 2.3nm oxide.) An examination of the $K_N$ defects SDR versus $V_F$ response strongly suggests that the $K_N$ defects have a narrowly peaked density of states around the middle of the silicon band gap. The realization that $K_N$ defects (not $P_b$ centers) dominate NBTI in the PNO devices may help explain: (1) NBTI's enhancement in nitrided devices, (2) conflicting reports of NBTI induced interface states and/or bulk traps, and (3) fluorine's ineffectiveness to reduce NBTI in nitrided devices.

## Chapter 5

## ADDITIONAL NBTI OBSERVATIONS: RECOVERY AND ACTIVATION ENERGY

In this chapter, we utilize SDR and DC-IV measurements as a function of time to examine the role of these atomic-scale defects in NBTI recovery.[20] We also make NBTI activation energy measurements of defect generation by monitoring the degradation in the linear drain current $I_{d,lin}$ as a function of stressing time.[20]

Our SDR and DC-IV measurement approach is not fast enough to observe the entire NBTI recovery phenomenon which begins microseconds after the stress is removed. However, the fact that recovery continues for at least $10^5$ seconds after stress removal,[7,9] allows for a qualitative SDR/DC-IV examination of the atomic scale defects involved in NBTI recovery. We present DC-IV and SDR measurements in pure $SiO_2$ and PNO devices which show that NBTI recovery results in a reduction in interface state density and a corresponding reduction in the density of the atomic-scale defects observed in SDR. In pure-$SiO_2$ devices, we observe that the $D_{it}$ recovery is accompanied by a reduction in $P_{b0}$ defect density. In PNO devices, we observe that the $D_{it}$ recovery is accompanied by a reduction in $K_N$ center density.

We also present activation energy measurements (of defect generation) on $SiO_2$ and PNO devices. Despite our earlier observations which show that different defects dominate NBTI in these two types of devices, we observe that the activation energies are, within experimental error, the same.

## 5.1 Experimental Details

Our NBTI recovery measurements involve pure-$SiO_2$ and PNO devices. The $SiO_2$ devices are very large area ($\approx 1x10^6$ $\mu m^2$) 48 nm $SiO_2$ power pMOSFETs provided by Austria Microsystems. These devices are the same as those discussed in chapter 3. The PNO devices are large area ($\approx 41,000$ $\mu m^2$) 2.3nm EOT PNO pMOSFETs provided by Texas Instruments. These devices are the same as those discussed in chapter 4. In these recovery experiments, the devices were subject to a NBTS condition followed by a temperature quench step. The temperature quench reduces the temperature of the device to room temperature over the span of approximately 4 minutes while the gate bias is maintained. This step is thought to "lock-in" the NBTI damage[7] rendering it observable in the DC-IV and SDR measurements. DC-IV and SDR measurements were taken pre-NBTS as well as a function of time post-NBTS/temperature quench. Recovery is observed as a reduction in the DC-IV derived $D_{it}$ and SDR signal amplitude (which is proportional to defect density). This approach allows for a crude investigation of the specific atomic-scale defects involved in NBTI recovery.

Our activation energy measurements involved 1$\mu$m x10 $\mu$m 2.7 nm pure $SiO_2$ and 2.3nm EOT PNO pMOSFETs provided by Texas Instruments. Activation energies of defect generation were extracted using the uninterrupted stress technique.[7] In this technique the device linear drain current, $I_{d,lin}$, is monitored ($V_d$ = -50mV) as a function of time while the gate bias is kept at the stressing voltage. This allows for a (nearly) recovery-free examination of the activation energy of defect generation. The activation energies were extracted after 6000 seconds of NBTS.

**5.2 NBTI Recovery in 48 nm SiO$_2$ pMOSFETs**

48 nm SiO$_2$ devices were subject to an ex-situ NBTS of -25V, 150°C for 100,000 seconds. Following the NBTS and temperature quench step, both SDR and DC-IV measurements were taken over a period of approximately 2 weeks. In all measurements, the source/drain to substrate junction is biased at +0.26V.

Figure 5.1 illustrates the DC-IV measurements for the unstressed device as well as measurements taken 600 seconds and 1.2 x 10$^6$ seconds post-NBTS/temperature quench. Since the NBTS/temperature quench was applied ex-situ, 600 seconds elapsed before the device was loaded into the spectrometer and the first DC-IV measurement was complete. Consequently, the 600 second measurement was the first measurement taken post NBTS/temperature quench (the 1.2 x 10$^6$ second measurement was the last measurement taken). As discussed in chapter 3, the geometry of these devices (gate extension over lightly doped regions) results in two DC-IV peaks. The DC-IV peak at $V_G$ = -0.5V is associated with interface states located near the center of the channel while the DC-IV peak at $V_G$ = 1.5V is associated with interface states in the drift regions adjacent to the source and drain. For both gate voltages, it is clear that NBTS generates an increase in the peak substrate current which corresponds to an increase in D$_{it}$. The Fitzgerald and Grove analysis[13] leads to pre-NBTS D$_{it}$ = 6 x 10$^9$ cm$^{-2}$eV$^{-1}$ and D$_{it}$ = 8 x 10$^9$ cm$^{-2}$eV$^{-1}$ for the $V_G$ = -0.5 and $V_G$ = 1.5V peaks, respectively. Post-NBTS (600 second measurement), we observe an increase in peak substrate current which correspond to D$_{it}$ = 2 x 10$^{11}$ cm$^{-2}$eV$^{-1}$ and D$_{it}$ = 3 x 10$^{11}$ cm$^{-2}$eV$^{-1}$ for the $V_G$ = -0.5 and $V_G$ = 1.5V peaks, respectively. All the extracted D$_{it}$ values assume a mean capture cross-section of $\sigma_s$ = 2 x 10$^{-16}$ cm$^2$. After 1.2 x 10$^6$ seconds of

Figure 5.1: DC-IV measurements taken pre- and post-NBTS (-25V, 150°C, for 100,000 seconds). The 600 seconds curve denotes the DC-IV measurement taken 600 seconds after the temperature quench step. The $1.2 \times 10^6$ seconds curve denotes the DC-IV measurement taken $1.2 \times 10^6$ seconds after the temperature quench step.

recovery (approximately 2 weeks) the $D_{it}$ corresponding to the $V_G = -0.5V$ peak exhibits little to no recovery, while the $D_{it}$ corresponding to the $V_G = +1.5V$ peak recovers approximately 20%.

Figure 5.2 illustrates the corresponding SDR measurements for the unstressed device, the *first measurement completed* post NBTS/temperature quench ($9 \times 10^3$ seconds), and the last measurement ($1.2 \times 10^6$ seconds). These SDR measurements were taken with the magnetic field aligned parallel to the <100> surface normal. The SDR measurements were taken with $V_G = 1.5V$ (not $V_G = -0.5V$) because of the improvement in SDR sensitivity corresponding to this voltage (see chapter 3). We observe that NBTS clearly generates a dominating signal at $g = 2.0058 \pm 0.0003$ which we attribute to $P_{b0}$ defects. The $P_{b0}$ signal amplitude (proportional to the number of defects) decreases by approximately 20% between the first and last measurements.

Figure 5.3 illustrates the (a) DC-IV derived $D_{it}$ and (b) SDR signal amplitudes as a function of time post-NBTS/temperature quench. We observe that the $V_G = -0.5V$ peak displays little or no $D_{it}$ recovery. At this time, we do not understand why this is so. We speculate that the geometry of the device is such that recovery occurs quicker near the center of the channel (perhaps faster than is captured in my first DC-IV measurement). We observe that the $V_G = +1.5V$ peak recovers approximately 20%. This reduction in interface state density is accompanied by a 20% recovery in $P_{b0}$ defect density. This correlation between $D_{it}$ and $P_{b0}$ recovery strongly suggests a common origin.
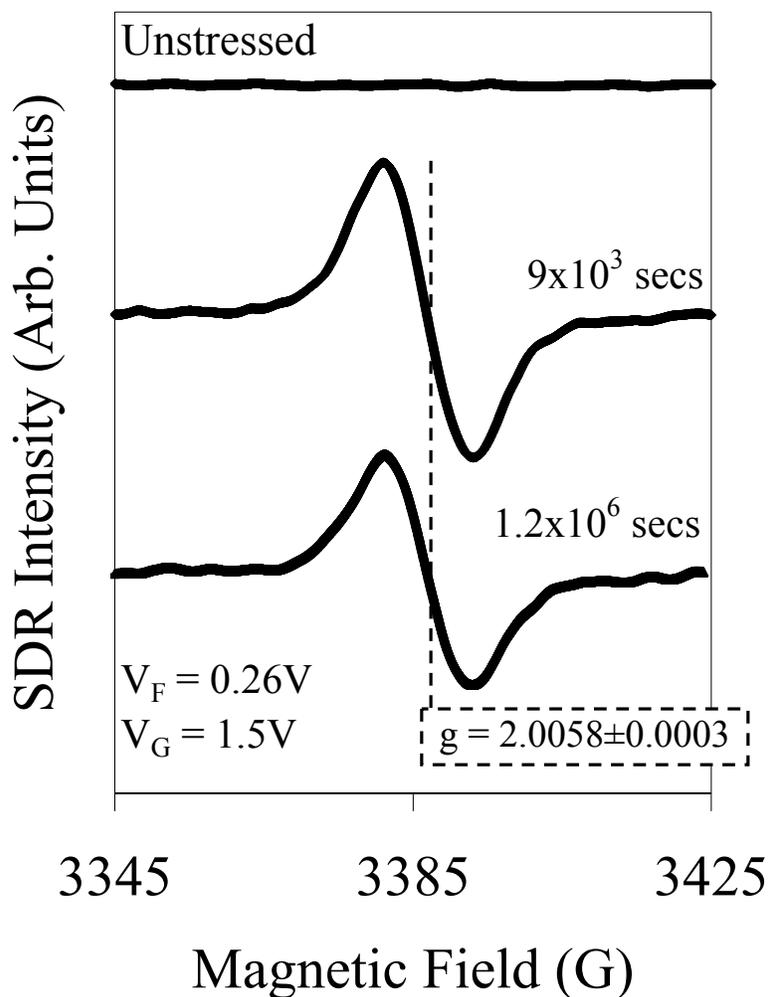
Figure 5.2: SDR spectra taken both pre- and post-NBTS (-25V, 150°C, for 100,000 seconds). After stress we note the generation of a strong g = 2.0058 ± 0.0003 signal corresponding to $P_{b0}$ defects. The 9 x $10^3$ seconds curve denotes the SDR measurement completed after 9 x $10^3$ seconds post- temperature quench. The 1.2 x $10^6$ seconds curve denotes the SDR measurement completed 1.2 x $10^6$ seconds after the temperature quench step. These spectra correspond to the $V_G$ = 1.5V DC-IV peak.
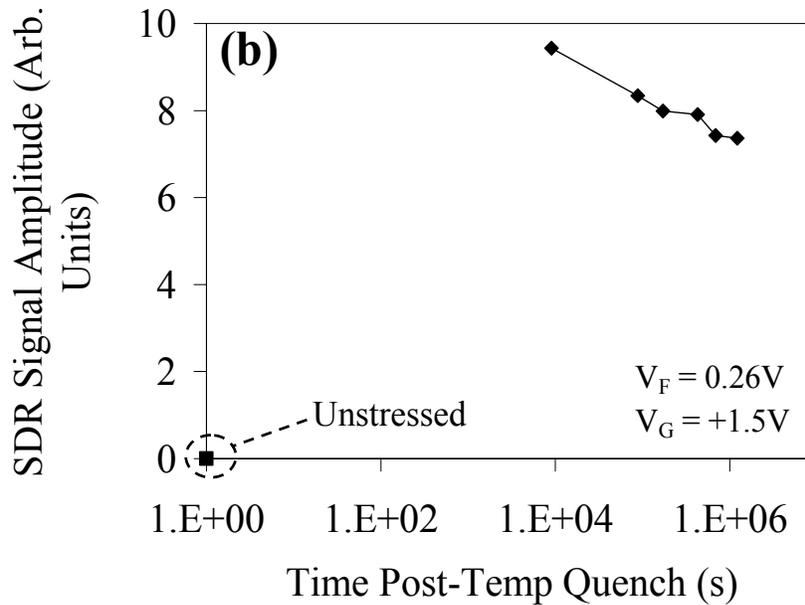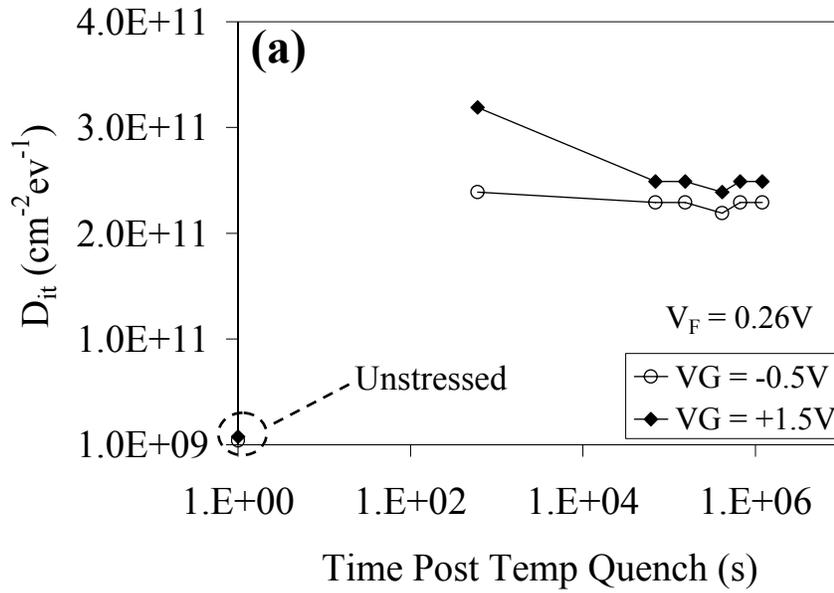
Figure 5.3: (a) DC-IV derived $D_{it}$ values on the stressed devices as a function of time post temperature quench. The $D_{it}$ values were tracked for both the $V_G = -0.5V$ DC-IV peak (essentially no recovery), as well as the $V_G = 1.5V$ DC-IV peak ($\approx 20\%$ recovery). (b) SDR signal amplitude (scales with $P_{b0}$ defect density) on the stressed devices as a function of time post temperature quench. We observe that the SDR signal amplitude (and $P_{b0}$ defect density) recovers $\approx 20\%$ recovery over the course of two weeks.

## 5.3 NBTI Recovery in 2.3 nm PNO pMOSFETs


Although we observe a correlation in $D_{it}/P_{b0}$ recovery, the bulk of the recovery process occurs faster than our measurement time.[7,9] Alternatively, we can reduce the delay between stress and measurement by performing the NBTS and temperature quench in-situ (hot air is piped into the spectrometer's microwave cavity via an evacuated quartz dewar to provide the elevated temperature). We utilized this in-situ stressing scheme to further investigate recovery in the PNO devices over a somewhat shorter time scale.

Figure 5.4 illustrates DC-IV characteristic curves taken pre- and post-NBTS (-2.8V 140°C for 10,000 seconds) as well as during the recovery process ($V_F = 0.33V$). The NBTS generates a large increase in $D_{it}$ (approximately an order of magnitude). A subsequent DC-IV measurement after ~5 hours of SDR measurement shows a reduction in $D_{it}$ associated with recovery. In an attempt to induce further recovery, the device was then subjected to a 24-hour bake (150°C with 0V on the gate electrode). A DC-IV measurement post-bake shows only a modest amount of recovery. We believe that the lack of significant post-bake recovery is due to the temperature quench post-NBTS. Thus, the NBTI-induced damage is, to some degree, "locked-in" when cooling to room temperature and is relatively unaffected by additional high temperature treatments.[7] Figure 5.5 illustrates the corresponding SDR measurements ($V_F = 0.33V$) taken with the magnetic field aligned parallel to the <100> direction at various post-NBTS time-steps. The NBTS generates a signal at $g = 2.0020 \pm 0.0003$ which corresponds to a $K_N$ center.[17] The amplitude of the $K_N$ center signal (which is proportional to the number of defects) decreases with time post NBTS. Figure 5.6 summarizes the $D_{it}$ and SDR signal intensity
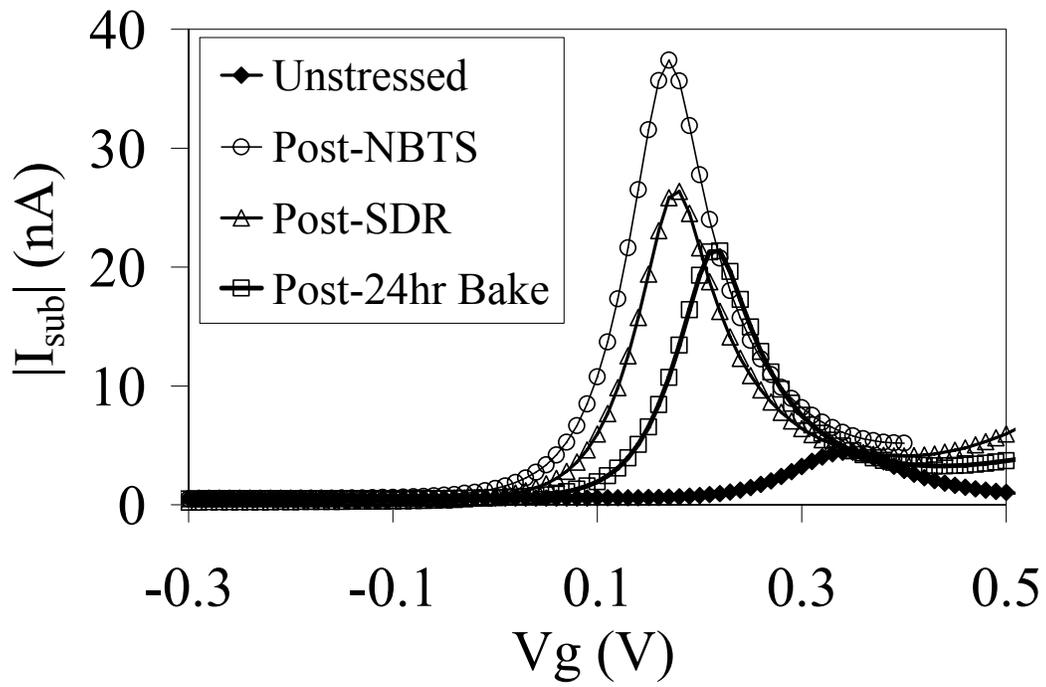
Figure 5.4: DC-IV measurements of 2.3nm PNO pMOSFET pre- and post-NBTS (-2.8V at 140°C for 10,000 seconds) as well as post-SDR measurement and post-24hr bake (150°C with 0V on the gate electrode). This indicates that $D_{it}$ exhibits a recovery process post NBTS. (source/drain to substrate voltage = 0.33V)
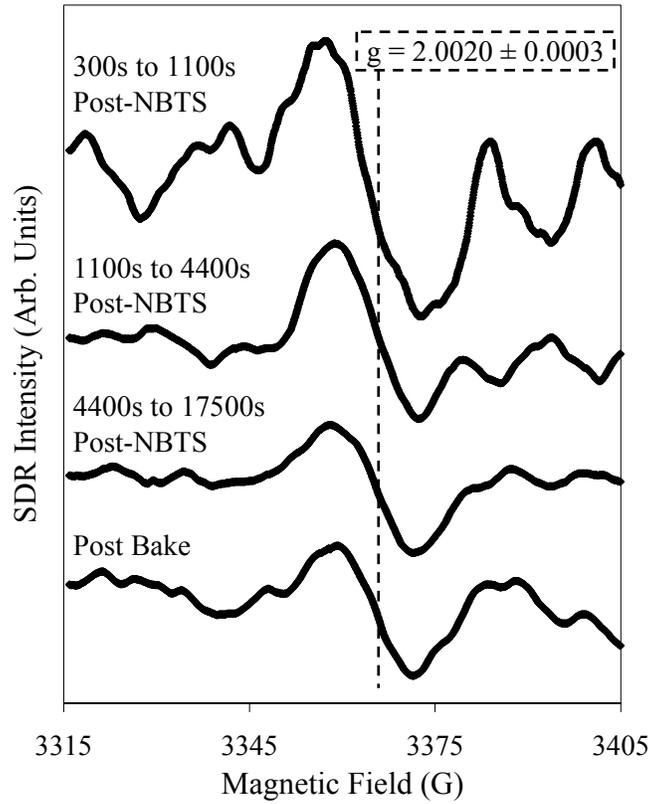
Figure 5.5: SDR traces of 23Å PNO pMOSFET post-NBTS (-2.8V at 140°C for 10,000 seconds) at various time steps which shows that the $K_N$ center density exhibits NBTI recovery. (Signal size scales with the density of defects.)
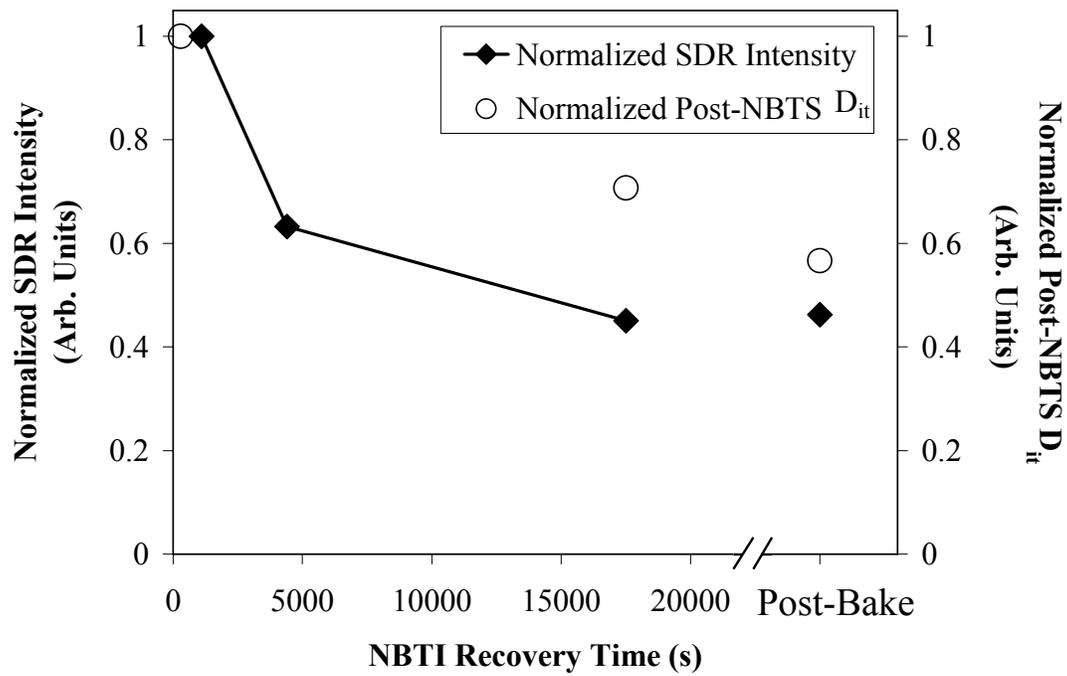
Figure: 5.6: Normalized SDR signal amplitude and normalized post-NBTS Dit as a function of NBTI recovery time illustrating the NBTI recovery process qualitatively tracks with the density of the $K_N$ centers

recovery. Since the observed $K_N$ center signal shows a recovery behavior that qualitatively scales with the observed $D_{it}$ degradation, these results are a strong indication that this defect is involved in the NBTI recovery process in these devices.

## 5.4 NBTI Activation Energy in 2.7nm SiO$_2$ and 2.3nm PNO pMOSFETs

Figure 5.7 illustrates an Arrhenius plot of both 2.7 nm SiO$_2$ and 2.3 nm PNO devices stressed at -3.3V for 6000 seconds. Activation energies are extracted by monitoring the degradation in $I_{d,lin}$ using the uninterrupted stress methodology. The extracted NBTI activation energies are observed to be time-independent and are essentially equivalent (0.11-0.12 eV). Note that these values actually correspond to the product of the activation energy and n, where n is the power law time exponent of degradation. Assuming n~1/6, the true activation energy is approximately 0.66-0.72eV. These values are consistent with those reported for hydrogenic diffusion through SiO$_2$.[125] The similarity in the extracted activation energies is contrary to reports that show that the activation energy is different for SiO$_2$ and PNO devices.[57,126] The equivalence is consistent with the idea that the rate limiting step involves the diffusion of species to and/or from the atomic defects. This result is therefore consistent with the recent work of Alam *et al.*[1] as well as the very recent work of Varghese *et al.*[74] who have proposed that the activation energies for SiO$_2$ and PNO devices should be equivalent because the activation energy is essentially determined by the diffusing species. Regardless of the fundamental difference in NBTI-induced atomic-scale defects in SiO$_2$ and PNO devices, our observations strongly suggest that the diffusing (presumably hydrogenic) species is the same in both SiO$_2$ and PNO devices.
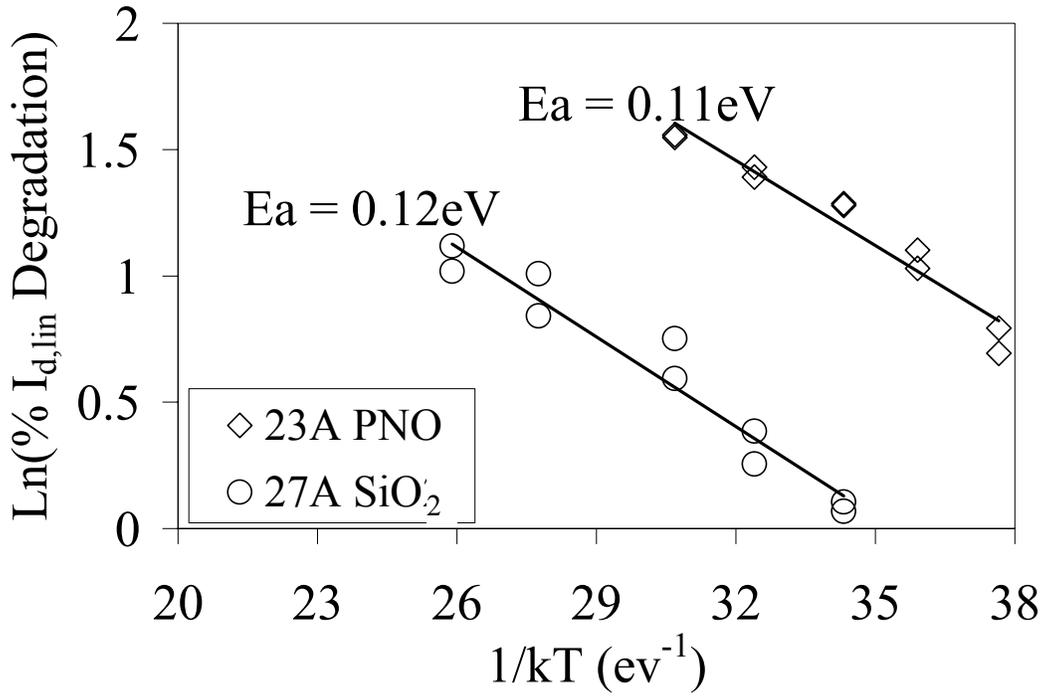
Figure 5.7: Arrhenius plot for SiO$_2$ and PNO pMOSFETs stressed at -3.3V for 6000 seconds. Activation energies are extracted by monitoring the degradation in I$_{d,lin}$ using the uninterupted stress methodology. Both devices are found to have essentially the same activation energies.

## 5.5 Summary

We report DC-IV and SDR measurements taken as a function of time during NBTI recovery that allow for a qualitative observation of the atomic scale defects involved in NBTI recovery in $SiO_2$ and PNO devices. In 48 nm $SiO_2$ devices, the DC-IV recovery in $D_{it}$ is accompanied by a recovery in $P_{b0}$ defect density. In PNO devices, the DC-IV recovery in $D_{it}$ is accompanied by a recovery in $K_N$ center defect density. These observations suggest an NBTI recovery mechanism that involves $P_{b0}$ and $K_N$ repassivation in $SiO_2$ and PNO devices respectively. Despite these fundamental differences in dominating NBTI-induced defects in $SiO_2$ and PNO devices, we measure activation energies (of defect generation) that appear to be the same. This strongly suggests that the rate limiting step is diffusion and that the, presumably hydrogenic, diffusing species is the same in both $SiO_2$ and PNO devices.

# Chapter 6

## CONCLUSIONS

In this work, we have utilized a unique combination of electrical and magnetic resonance measurements to study the atomic-scale defects involved in NBTI. We employ DC-IV measurements to monitor NBTI-induced changes in device interface state density. These electrical measurements are combined with two very sensitive EDMR measurements called SDR and SDT which allow for the identification of specific NBTI-induced atomic-scale defect populations. The combination of these two types of measurements (DC-IV and EDMR) provides a direct correlation between the NBTI-induced electrical damage and the generation of specific atomic-scale defects. This work has resulted in a fundamental understanding of the atomic-scale defects involved in NBTI and has led to a deeper understanding of the NBTI phenomenon in both pure-$SiO_2$ and PNO devices.

In both 7.5nm and 48nm pure-$SiO_2$ pMOSFETs, DC-IV measurements indicate that the NBTI response is dominated by the generation of relatively large densities of interface states. The corresponding SDR measurements identify these NBTI-induced interface states as $P_{b0}$ and $P_{b1}$ defects in the 7.5nm devices and $P_{b0}$ defects in the 48nm devices. These observations are consistent with what most NBTI experts assumed (interface state generation via hydrogen depassivation of silicon dangling bonds at the $Si/SiO_2$ interface). These results are also consistent with much of NBTI "reaction-diffusion" literature.[1,5,26,27] The reaction-diffusion model predicts that NBTI is dominated by a hydrogen depassivation of $P_b$ centers at the $Si/SiO_2$ interface and the reaction rate is controlled by hydrogenic diffusion away from the interface.[1,5,26,27] After a

high temperature NBTS (a conditions which may be too harsh for technological relevance), we also note the observation of E′ center oxide defects. Our observation of NBTI-induced E′ centers suggests that they may have some role in the catalyzing inversion layer hole capture. However, since a harsh NBTS was required to observe the E′ centers, it is not possible to conclude with certainty that they play a role under technologically relevant conditions.

However, in 2.3nm PNO devices, our observations were inconsistent with what is generally assumed in the NBTI literature. Our results clearly show that, in these devices, *NBTI generates a new defect* (not $P_{b0}$ or $P_{b1}$). SDT measurements have allowed us to identify this defect as a $K_N$ center. Our measurements show that the $K_N$ centers are located in the "near-interface" region and they participate in both SDR and SDT phenomena. (The "near-interface" region could be a large fraction of a 2.3nm oxide.) An examination of the $K_N$ defects SDR versus $V_F$ response strongly suggests that the $K_N$ defects have a narrowly peaked density of states around the middle of the silicon band gap. The realization that $K_N$ defects (not $P_b$ centers) dominate NBTI in PNO devices may help provide an explanation for NBTI's nitrogen enhancement. Our results also help explain the conflicting reports of the dominance of NBTI induced interface states and/or bulk traps. Finally, the $K_N$ center identification helps explain fluorine's ineffectiveness in reducing NBTI in nitrided devices. It should be noted that our SDT measurements represent only the third time this magnetic resonance technique has been reported in the literature and the first time this technique has been utilized to study reliability problems.

Our DC-IV and SDR measurement approach has also allowed for a qualitative examination of atomic-scale defects involved in NBTI recovery in $SiO_2$ and PNO devices. In 48 nm $SiO_2$ devices, the DC-IV recovery in $D_{it}$ is accompanied by a recovery of $P_{b0}$ defect density. In PNO devices, the DC-IV recovery in $D_{it}$ is accompanied by a recovery in $K_N$ center defect

density. These observations suggest an NBTI recovery mechanism that involves $P_{b0}$ and $K_N$ repassivation in $SiO_2$ and PNO devices respectively.

Our observations clearly show that there are fundamental differences in the dominating NBTI-induced defects in $SiO_2$ and PNO devices. Despite these differences, we measure the same activation energies (of defect generation) in both $SiO_2$ and PNO devices. This strongly suggests that the rate limiting step in the NBTI degradation process is diffusion and that the, presumably hydrogenic, diffusing species are the same in both $SiO_2$ and PNO devices.

This body of work represents a significant contribution to the NBTI field. It is the first comprehensive experimental examination of the atomic-scale mechanisms governing NBTI in fully processed $SiO_2$ and PNO devices. Our results have allowed for the validation of some aspects of NBTI models and rule out one widely held assumption that $P_b$ centers dominate NBTI in PNO devices. Our observations regarding NBTI and the $K_N$ center were not generally anticipated in the literature. Our $K_N$ center observations have been limited to the PNO processing used to fabricate these devices. Our observations may not be universally applicable. The introduction of nitrogen via other methods (thermal nitridation, $NH_3$ annealing, etc…) could conceivably result in the generation of different NBTI-induced defects. The universality of our observations can only be determined with absolute certainty through further experiments examining variously processed nitrided devices. However, it seems likely that, at least to first order, the thermodynamics that govern the introduction of nitrogen to the $SiO_2$ network will result in the generation of $K_N$ center precursors (over a wide range of processing variations).[127] It is nevertheless also virtually certain that processing variations will result in variable $K_N$ center and presumably the nitrogen center densities. Our hope is that the deeper understanding provided by these measurements will allow for processing changes which will act to ameliorate NBTI.

A large portion of this research was spent trying to limit the effects of tunneling current. In thin gate dielectrics, the tunneling current overwhelms the SDR and limits the sensitivity of the measurement. Consequently, we initially limited our experiments to thicker gate dielectrics (less tunneling). However, the realization that tunneling can be an asset has really changed the approach of the later part of this work. SDT has proved to be an extremely sensitive tool to probe the atomic-scale defects involved in NBTI. The technique permits this in very thin gate dielectrics. The ability to examine the atomic scale defects in ultra-thin gate dielectrics allows for a stronger link between our research and the problem observed in technologically relevant devices.

The SDT technique also has logical applications to other device instabilities. For example, the fundamental mechanisms of stress-induced leakage current (SILC) and soft-breakdown in gate oxides are still undetermined. SDT measurements would absolutely identify the atomic scale defects involved in these processes. (The will probably be very similar to the defects we observed due to NBTI.)

The next generation of CMOS technology will likely include the replacement of $SiO_2$ with a high-k dielectric. These dielectrics are known to have bias temperature instability problems and high densities of shallow electron traps. The application of SDR/SDT techniques would allow for a fundamental understanding of the defects involved in these technologically important materials systems.

## REFERENCES

[1]   M. A. Alam and S. Mahapatra, Microelectron. Rel., **45** (1), pp. 71-81 (2005)

[2]   S. Chakravarthi, A. T. Krishnan, V. Reddy, C. F. Machala, and S. Krishnan, *Proc. IEEE Int. Reliability Phys. Symp.*, pp. 273-282 (2004)

[3]   M. Denais, A. Bravaix, V. Huard, C. Parthasarathy, G. Ribes, F. Perrier, Y. Rey-Tauriac, and N. Revil, *Proc. IEEE Int. Electron Devices Meet.*, pp. 109-112 (2004)

[4]   V. Huard, M. Denais, and C. Parthasarathy, Microelectron. Rel., **46** (1), pp. 1-23 (2006)

[5]   A. T. Krishnan, C. Chancellor, S. Chakravarthi, P. E. Nicollian, V. Reddy, A. Varghese, R. B. Khamankar, and S. Krishnan, *Proc. IEEE Int. Electron Devices Meet.*, pp. 705-708 (2005)

[6]   M. Ershov, S. Saxena, H. Karbasi, S. Winters, S. Minehane, J. Babcock, R. Lindley, P. Clifton, M. Redford, and A. Shibkov, Appl. Phys. Lett., **83** (8), pp. 1647-1649 (2003)

[7]   S. Rangan, N. Mielke, and E. C. C. Yeh, *Proc. IEEE Int. Electron Devices Meet.*, pp. 341-344 (2003)

[8]   H. Reisinger, O. Blank, W. Heinrigs, A. Muhlhoff, W. Gustin, and C. Schlunder, *Proc. IEEE International Reliability Physics Symposium*, pp. 448-453 (2006)

[9]   T. Grasser, W. Gos, V. Sverdlov, and B. Kaczer, *Proc. IEEE Int. Reliability Phys. Symp.*, pp. 268-280 (2007)

[10]  N. Kimizuka, K. Yamaguchi, K. Imai, T. Iizuka, C. T. Liu, R. C. Keller, and T. Horiuchi, *Proc. Symp. on VLSI Technol.*, pp. 92-93 (2000)

[11]  N. Kimizuka, T. Yamamoto, T. Mogami, K. Yamaguchi, K. Imai, and T. Horiuchi, *Proc. Symp. on VLSI Technol.*, pp. 73-74 (1999)

[12]  A. E. Islam, G. Gupta, S. Mahapatra, A. T. Krishnan, K. Ahmed, F. Nouri, A. Oates, and M. A. Alam, *Proc. IEEE Int. Electron Devices Meet.*, pp. 329-332 (2006)

[13]  D. J. Fitzgerald and A. S. Grove, Surf. Sci., **9**, pp. 347-369 (1968)

[14]  A. Neugroschel, C. T. Sah, K. M. Han, M. S. Carroll, T. Nishida, J. T. Kavalieros, and Y. Lu, IEEE Trans. Electron Devices, **42** (9), pp. 1657-1662 (1995)

[15]  P. M. Lenahan and J. F. Conley, J. Vac. Sci. Technol., B, **16** (4), pp. 2134-2153 (1998)

[16]  S. Fujieda, Y. Miura, M. Saitoh, E. Hasegawa, S. Koyama, and K. Ando, Appl. Phys. Lett., **82** (21), pp. 3677-3679 (2003)

[17]  J. P. Campbell, P. M. Lenahan, A. T. Krishnan, and S. Krishnan, *submitted to Applied Physics Letters*, pp.  (2007)

[18]  J. P. Campbell, P. M. Lenahan, A. T. Krishnan, and S. Krishnan, *Proc. IEEE Int. Reliability Phys. Symp.*, pp. 503-510 (2007)

[19]  J. P. Campbell, P. M. Lenahan, A. T. Krishnan, and S. Krishnan, IEEE Trans. Device Mater. Rel., **6** (2), pp. 117-122 (2006)

[20]  J. P. Campbell, P. M. Lenahan, A. T. Krishnan, and S. Krishnan, *Proc. IEEE Int. Reliability Phys. Symp.*, pp. 442-446 (2006)

[21]  J. P. Campbell, P. M. Lenahan, A. T. Krishnan, and S. Krishnan, Appl. Phys. Lett., **87** (20), pp. 204106 (2005)

[22]  K. L. Brower, Z. Phys. Chem., Neue. Folge, **151**, pp. 177-189 (1987)

[23]  J. W. Gabrys, P. M. Lenahan, and W. Weber, Microelectron. Eng., **22** (1-4), pp. 273-276 (1993)

[24]  E. H. Poindexter, G. J. Gerardi, M. E. Rueckel, P. J. Caplan, N. M. Johnson, and D. K. Biegelsen, J. Appl. Phys., **56** (10), pp. 2844-2849 (1984)

[25] A. Stesmans, B. Nouwen, and V. V. Afanas'ev, Phys. Rev. B, **58** (23), pp. 15801-15809 (1998)

[26] K. O. Jeppson and C. M. Svensson, J. Appl. Phys., **48** (5), pp. 2004-2014 (1977)

[27] S. Ogawa and N. Shiono, Phys. Rev. B, **51** (7), pp. 4218-4230 (1995)

[28] D. K. Schroder and J. A. Babcock, J. Appl. Phys., **94** (1), pp. 1-18 (2003)

[29] B. E. Deal, M. Sklar, A. S. Grove, and E. H. Snow, J. Electrochem. Soc., **114** (3), pp. 266-274 (1967)

[30] D. Frohman-Bentchkowsky, IEEE J. Solid-State Circuits, **6** (5), pp. 301-306 (1971)

[31] A. Goetzberger, A. D. Lopez, and R. J. Strain, J. Electrochem. Soc., **120** (1), pp. 90-96 (1973)

[32] M. Nakagiri, Jpn. J. Appl. Phys., **13** (10), pp. 1610-1617 (1974)

[33] C. E. Blat, E. H. Nicollian, and E. H. Poindexter, J. Appl. Phys., **69** (3), pp. 1712-1720 (1991)

[34] B. S. Doyle, B. J. Fishbein, and K. R. Mistry, *Proc. IEEE Int. Electron Devices Meet.*, pp. 529-532 (1991)

[35] G. La Rosa, F. Guarin, S. Rauch, A. Acovic, J. Lukaitis, and E. Crabbe, *Proc. IEEE Int. Reliability Phys. Symp.*, pp. 282-286 (1997)

[36] R. Thewes, R. Brederlow, C. Schlunder, P. Wieczorek, A. Hesener, B. Ankele, P. Klein, S. Kessel, and W. Weber, *Proc. IEEE Int. Electron Devices Meet.*, pp. 81-84 (1999)

[37] T. Yamamoto, K. Uwasawa, and T. Mogami, IEEE Trans. Electron Devices, **46** (5), pp. 921-926 (1999)

[38] M. Makabe, T. Kubota, and T. Kitano, *Proc. IEEE Int. Reliability Phys. Symp.*, pp. 205 (2000)

[39] C. H. Ang, C. M. Lek, S. S. Tan, B. J. Cho, T. P. Chen, W. H. Lin, and J. Z. Zhen, Jpn. J. Appl. Phys., Part 2, **41** (3B), pp. L314-L316 (2002)

[40] M. Houssa, C. R. Parthasarathy, V. Huard, N. Revil, E. Vincent, and J. L. Autran, *Proc. IEEE Int. Integrated Reliability Workshop*, pp. 133-134 (2002)

[41] D. Y. Lee, H. C. Lin, W. J. Chiang, W. T. Lu, G. W. Huang, T. Y. Huang, and T. Wang, *Proc. Int. Symp. on Plasma- and Process-Induced Damage*, pp. 150-153 (2002)

[42] S. Tsujikawa, Y. Akamatsu, H. Umeda, and J. Yugami, *Proc. IEEE Int. Reliability Phys. Symp.*, pp. 28-34 (2004)

[43] C. H. Liu, M. T. Lee, C.-Y. Lin, J. Chen, K. Schruefer, J. Brighten, N. Rovedo, T. B. Hook, M. V. Khare, S.-F. Huang, C. Wann, T.-C. Chen, and T. H. Ning, *Proc. IEEE Int. Electron Devices Meet.*, pp. 861-864 (2001)

[44] T. B. Hook, E. Adler, F. Guarin, J. Lukaitis, N. Rovedo, and K. Schruefer, IEEE Trans. Electron Devices, **48** (7), pp. 1346-1353 (2001)

[45] Y.-H. Lee, N. Mielke, B. Sabi, S. Stadler, R. Nachman, and S. Hu, *Proc. IEEE Int. Electron Devices Meet.*, pp. 353-356 (2003)

[46] D. Y. Lee, T. Y. Huang, H. C. Lin, W. J. Chiang, G. W. Huang, and T. Wanga, J. Electrochem. Soc., **151** (2), pp. G144-G148 (2004)

[47] T. Sasaki, F. Ootsuka, H. Ozaki, T. Hoshi, M. Tomikawa, M. Yasuhira, and T. Arikado, Jpn. J. Appl. Phys., Part 1, **43** (4B), pp. 1837-1842 (2004)

[48] J.-S. Lee, J. W. Lyding, and K. Hess, *Proc. IEEE Int. Reliability Phys. Symp.*, pp. 685-686 (2004)

[49] K. G. Cheng, K. Hess, and J. W. Lyding, IEEE Electron. Dev. Lett., **22** (9), pp. 441-443 (2001)

[50] K. G. Cheng, K. Hess, and J. W. Lyding, IEEE Electron. Dev. Lett., **22** (5), pp. 203-205 (2001)

[51] J. W. Lyding, K. Hess, and I. C. Kizilyalli, Appl. Phys. Lett., **68** (18), pp. 2526-2528 (1996)

[52] S. S. Tan, T. P. Chen, C. H. Ang, Y. L. Tan, and L. Chan, Jpn. J. Appl. Phys., Part 2, **41** (10 A), pp. 1031-1033 (2002)

[53] J. Ushio, T. Maruizumi, and K. Kushida-Abdelghafar, Appl. Phys. Lett., **81** (10), pp. 1818-1820 (2002)

[54] C. H. Liu, H.-S. Lin, Y.-Y. Lin, W.-T. Chang, C.-S. Hsiung, C.-C. Hsu, A. Y. Liang, J. Chen, Y. J. Chang, F.-T. Liou, M. G. Chen, T. M. Pan, C. J. Kao, K. T. Huang, S. H. Lin, Y. C. Sheng, J. H. Lee, M. Huang, S. Huang-Lu, W. Y. Hsieh, P. W. Yen, S. C. Chien, and Y. T. Loh, *Proc. IEEE Int. Reliability Phys. Symp.*, pp. 268-271 (2002)

[55] J. Ushio, K. Watanabe, K. Kushida-Abdelghafar, and T. Maruizumi, Appl. Surf. Sci., **216** (1-4), pp. 258-263 (2003)

[56] S. S. Tan, T. P. Chen, C. H. Ang, and L. Chan, Appl. Phys. Lett., **82** (2), pp. 269-271 (2003)

[57] S. S. Tan, T. P. Chen, J. M. Soon, K. P. Loh, C. H. Ang, and L. Chan, Appl. Phys. Lett., **82** (12), pp. 1881-1883 (2003)

[58] S. S. Tan, T. P. Chen, C. H. Ang, and L. Chan, IEEE Electron. Dev. Lett., **25** (7), pp. 504-506 (2004)

[59] J. H. Stathis, G. LaRosa, and A. Chou, *Proc. IEEE Int. Reliability Phys. Symp.*, pp. 1-7 (2004)

[60] Y. Mitani, *Proc. IEEE Int. Electron Devices Meet.*, pp. 117-120 (2004)

[61]   T. B. Hook, R. Bolam, W. Clark, J. Burnham, N. Rovedo, and L. Schutz, Microelectron. Rel., **45** (1), pp. 47-56 (2005)

[62]   W. Abadeer and W. Ellis, *Proc. IEEE Int. Reliability Phys. Symp.*, pp. 17-22 (2003)

[63]   G. Chen, K. Y. Chuah, M. F. Li, D. S. H. Chan, C. H. Ang, J. Z. Zheng, Y. Jin, and D. L. Kwong, *Proc. IEEE Int. Reliability Phys. Symp.*, pp. 196-202 (2003)

[64]   M. Ershov, R. Lindley, S. Saxena, A. Shibkov, S. Minehane, J. Babcock, S. Winters, H. Karbasi, T. Yamashita, P. Clifton, and M. Redford, *Proc. IEEE Int. Reliability Phys. Symp.*, pp. 606-607 (2003)

[65]   S. Tsujikawa, T. Mine, K. Watanabe, Y. Shimamoto, R. Tsuchiya, K. Ohnishi, T. Onai, J. Yugami, and S. i. Kimura, *Proc. IEEE Int. Reliability Phys. Symp.*, pp. 183-188 (2003)

[66]   M. A. Alam, *Proc. IEEE Int. Electron Devices Meet.*, pp. 345-348 (2003)

[67]   A. T. Krishnan, V. Reddy, S. Chakravarthi, J. Rodriguez, S. John, and S. Krishnan, *Proc. IEEE Int. Electron Devices Meet.*, pp. 349-352 (2003)

[68]   M. F. Li, G. Chen, C. Shen, X. P. Wang, H. Y. Yu, Y.-C. Yeo, and D. L. Kwong, Jpn. J. Appl. Phys., **43**, pp. 7807-7814 (2004)

[69]   A. T. Krishnan, *Proc. IEEE Int. Reliability Phys. Symp. Tutorial Notes*, pp. (2004)

[70]   S. Mahapatra, P. B. Kumar, and M. A. Alam, IEEE Trans. Electron Devices, **51** (9), pp. 1371-1379 (2004)

[71]   D. Varghese, S. Mahapatra, and M. A. Alam, IEEE Electron. Dev. Lett., **26** (8), pp. 572-574 (2005)

[72]   T. Yang, C. Shen, M. F. Li, C. H. Ang, C. X. Zhu, Y. C. Yeo, G. Samudra, and D. L. Kwong, IEEE Electron. Dev. Lett., **26** (10), pp. 758-760 (2005)

[73]  S. Mahapatra, M. A. Alam, P. B. Kumar, T. R. Dalei, D. Varghese, and D. Saha, Microelectron. Eng., **80**, pp. 114-121 (2005)

[74]  D. Varghese, D. Saha, S. Mahapatra, K. Ahmed, F. Nouri, and M. Alam, *Proc. IEEE Int. Electron Devices Meet.*, pp. 701-704 (2005)

[75]  M. Denais, V. Huard, C. Parthasarathy, G. Ribes, F. Perrier, N. Revil, and A. Bravaix, IEEE Trans. Device Mater. Rel., **4** (4), pp. 715-722 (2004)

[76]  V. Huard and M. Denais, *Proc. IEEE Int. Reliability Phys. Symp.*, pp. 40-45 (2004)

[77]  B. Zhu, J. S. Suehle, and J. B. Bernstein, *Proc. IEEE Int. Reliability Phys. Symp.*, pp. 689-670 (2004)

[78]  V. Huard, M. Denais, F. Perrier, N. Revil, C. Parthasarathy, A. Bravaix, and E. Vincent, Microelectron. Rel., **45** (1), pp. 83-98 (2005)

[79]  V. Huard, C. R. Parthasarathy, and M. Denais, *Proc. IEEE Int. Integrated Reliability Workshop*, pp. 5-9 (2005)

[80]  S. Mahapatra and M. A. Alam, *Proc. IEEE Int. Electron Devices Meet.*, pp. 505-508 (2002)

[81]  S. Mahapatra, M. A. Alam, P. B. Kumar, T. R. Dalei, and D. Saha, *Proc. IEEE Int. Electron Devices Meet.*, pp. 105-108 (2004)

[82]  S. Mahapatra, P. Bharath Kumar, and M. A. Alam, *Proc. IEEE Int. Electron Devices Meet.*, pp. 337-340 (2003)

[83]  B. Tuttle and C. G. Van de Walle, Phys. Rev. B, **59** (20), pp. 12884-12889 (1999)

[84]  C. G. Vandewalle and R. A. Street, Phys. Rev. B, **49** (20), pp. 14766-14769 (1994)

[85]  K. Kushida-Abdelghafar, K. Watanabe, J. Ushio, and E. Murakami, Appl. Phys. Lett., **81** (23), pp. 4362-4364 (2002)

[86]  J. M. Soon, K. P. Loh, S. S. Tan, T. P. Chen, W. Y. Teo, and L. Chan, Appl. Phys. Lett., **83** (15), pp. 3063-3065 (2003)

[87]  S. S. Tan, T. P. Chen, J. M. Soon, K. P. Loh, C. H. Ang, W. Y. Teo, and L. Chan, Appl. Phys. Lett., **83** (3), pp. 530-532 (2003)

[88]  S. Zafar, J. Appl. Phys., **97** (10), pp. 103709 (2005)

[89]  S. Ogawa, M. Shimaya, and N. Shiono, J. Appl. Phys., **77** (3), pp. 1137-1148 (1995)

[90]  A. S. Grove and D. J. Fitzgerald, Solid-State Electron., **9**, pp. 783-806 (1966)

[91]  R. N. Hall, Phys. Rev., **87** (2), pp. 387-387 (1952)

[92]  W. Shockley and W. T. Read, Phys. Rev., **87** (5), pp. 835-842 (1952)

[93]  J. A. Weil, J. R. Bolton, and J. E. Wertz, *Electron Paramagnetic Resonance: Elementary Theory and Practical Applications*. John Wiley & Sons, New York, NY, (1994)

[94]  J. E. Wertz and J. R. Bolton, *Electron Spin Resonance: Elementary Theory and Practical Applications*. McGraw-Hill, New York, (1972)

[95]  D. J. Lepine, Phys. Rev. B, **6** (2), pp. 436-441 (1972)

[96]  M. A. Jupina and P. M. Lenahan, IEEE Trans. Nucl. Sci., **36** (6), pp. 1800-1807 (1989)

[97]  D. Kaplan, I. Solomon, and N. F. Mott, Journal De Physique Lettres, **39** (4), pp. L51-L54 (1978)

[98]  P. M. Lenahan and M. A. Jupina, Colloids Surf., **45**, pp. 191-211 (1990)

[99]  Y. Miura and S. Fujieda, Jpn. J. Appl. Phys., Part 1, **40** (4B), pp. 2840-2843 (2001)

[100]  J. H. Stathis, Appl. Phys. Lett., **68** (12), pp. 1669-1671 (1996)

[101]  J. P. Campbell, P. M. Lenahan, A. T. Krishnan, and S. Krishnan, *Proc. IEEE Int. Integrated Reliability Workshop*, pp. 118-120 (2004)

[102]   J. P. Campbell, P. M. Lenahan, A. T. Krishnan, and S. Krishnan, *Proc. IEEE Int. Integrated Reliability Workshop*, pp. 1-4 (2005)

[103]   T. D. Mishima and P. M. Lenahan, IEEE Trans. Nucl. Sci., **47** (6), pp. 2249-2255 (2000)

[104]   T. D. Mishima, P. M. Lenahan, and W. Weber, Appl. Phys. Lett., **76** (25), pp. 3771-3773 (2000)

[105]   J. P. Campbell and P. M. Lenahan, Appl. Phys. Lett., **80** (11), pp. 1945-1947 (2002)

[106]   G. J. Gerardi, E. H. Poindexter, P. J. Caplan, and N. M. Johnson, Appl. Phys. Lett., **49** (6), pp. 348-350 (1986)

[107]   P. M. Lenahan and P. V. Dressendorfer, J. Appl. Phys., **54** (3), pp. 1457-1460 (1983)

[108]   P. M. Lenahan and P. V. Dressendorfer, J. Appl. Phys., **55** (10), pp. 3495-3499 (1984)

[109]   P. M. Lenahan and P. V. Dressendorfer, Appl. Phys. Lett., **41** (6), pp. 542-544 (1982)

[110]   Y. Y. Kim and P. M. Lenahan, J. Appl. Phys., **64** (7), pp. 3551-3557 (1988)

[111]   E. P. O'Reilly and J. Robertson, Phys. Rev. B, **27** (6), pp. 3780-3795 (1983)

[112]   J. F. Conley, P. M. Lenahan, H. L. Evans, R. K. Lowry, and T. J. Morthorst, J. Appl. Phys., **76** (5), pp. 2872-2880 (1994)

[113]   B. B. Jie, M. F. Li, C. L. Lou, W. K. Chim, D. S. H. Chan, and K. F. Lo, IEEE Electron. Dev. Lett., **18** (12), pp. 583-585 (1997)

[114]   P. E. Nicollian, M. Rodder, D. T. Grider, P. Chen, R. M. Wallace, and S. V. Hattangady, *Proc. IEEE Int. Reliability Phys. Symp.*, pp. 400-404 (1999)

[115]   E. H. Nicollian and J. R. Brews, *MOS (Metal Oxide Semiconductor) Physics and Technology*. John Wiley & Sons, New York, (1982)

[116]   P. M. Lenahan and S. E. Curry, Appl. Phys. Lett., **56** (2), pp. 157-159 (1990)

[117] D. L. Griscom, E. J. Friebele, and G. H. Sigel, Solid State Commun., **15** (3), pp. 479-483 (1974)

[118] W. L. Warren and P. M. Lenahan, Phys. Rev. B, **42** (3), pp. 1773-1780 (1990)

[119] D. T. Krick, P. M. Lenahan, and J. Kanicki, J. Appl. Phys., **64** (7), pp. 3558-3563 (1988)

[120] V. J. Kapoor, R. S. Bailey, and H. J. Stein, J. Vac. Sci. Technol., A, **1** (2), pp. 600-607 (1983)

[121] P. A. Kraus, K. Ahmed, T. C. Chua, M. Ershov, H. Karbasi, C. S. Olsen, F. Nouri, J. Holland, R. Zhao, G. Miner, and A. Lepert, *Proc. Symp. on VLSI Technol.*, pp. 143-144 (2003)

[122] T. P. Ma, J. Vac. Sci. Technol., A, **10** (4), pp. 705-712 (1992)

[123] P. J. Wright and K. C. Saraswat, IEEE Trans. Electron Devices, **36** (5), pp. 879-889 (1989)

[124] Y. Mitani, M. Nagamine, H. Satake, and A. Toriumi, *Proc. IEEE Int. Electron Devices Meet.*, pp. 509-512 (2002)

[125] M. L. Reed and J. D. Plummer, J. Appl. Phys., **63** (12), pp. 5776-5793 (1988)

[126] S. S. Tan, T. P. Chen, C. H. Ang, C. M. Lek, W. Lin, J. Z. Zheng, A. See, and L. Chan, *Proc. Int. Symp. on Plasma- and Process-Induced Damage*, pp. 146-149 (2002)

[127] T. Maruizumi, J. Ushio, and M. Miyao, J. Non-Cryst. Solids, **246** (1-2), pp. 73-82 (1999)

APPENDIX: NON-TECHNICAL ABSTRACT

Modern society's thirst for electronics is sustained by the ability to fabricate *reliable* integrated circuits. All integrated circuits rely on the transistor as the fundamental building block. The transistor can be thought of as a light switch (it can be turned "on" or "off"). Linking many of these "switches" together can form a path of decision making or logic. This logic controls the operation of modern electronics (computers, cell phones, etc.) In order for the logic in these modern electronics to function properly, the transistors must function *reliably*.

The reliability of these transistors is most threatened by a problem called the negative bias temperature instability. This instability manifests itself as gradual shift in transistor threshold voltage at conditions (negative gate bias and moderately elevated temperature) that, unfortunately, occur in many electronic devices. Using the light switch analogy, the shift in transistor threshold voltage is equivalent to a shift in the light switch's on/off transition point. If the on/off transition changes, the logic that relies on this switching fails, and the computer or cell phone using this logic becomes useless.

Prior to this research, the fundamental mechanisms governing the negative bias temperature instability were unknown. The urgency of this problem has recently increased because the common practice of adding nitrogen to the transistor (which improves the transistor performance) also acts to enhance the negative bias temperature instability.

In this work, very sensitive magnetic resonance measurements have been utilized to observe specific atomic-scale defects which are involved in the negative bias temperature instability. Atomic scale defects are imperfections or errors that occur in the materials that compose the transistor structure. This work shows that the negative bias temperature instability in conventional silicon/silicon dioxide transistors is caused by bonding errors (silicon dangling

bonds in which the silicon is bonded to three other silicon atoms) at the interface between these two materials. However, the addition of nitrogen to these transistors causes different bonding errors (silicon dangling bonds in which the silicon atoms are bonded to three other nitrogen atoms) located very close to but not precisely at the interface. The difference in these bonding errors is the reason why the negative bias temperature instability is enhanced with the addition of nitrogen. Despite nearly forty years of research on this instability, an understanding of the atomic-scale imperfections that are responsible for the shift in the "on/off" transition has been lacking. This work provides a better understanding of how the instability occurs and allows for a better prediction of the "lifetime" of a transistor.

<div align="center">

**VITA**
**Jason P. Campbell**

</div>

**Place of Birth:** Wilkes-Barre, PA – 12/04/1978

**Education:**  B.S. Engineering Science with Honors: The Pennsylvania State University- 5/01
Ph.D. Engineering Science and Mechanics: The Pennsylvania State University

**Honors:**  IEEE International Reliability Physics Symposium "Outstanding Paper" (2006)
Penn State College of Engineering Deans Fellowship (2001 - 2003)
Schreyer Honors Scholar (1998 - 2001)
Tau Beta Pi, National Engineering Honor's Society

**Professional Activities:**
International Integrated Reliability Workshop (IRW): Vice-Poster Chair (2005), Vice-Discussion Group Chair (2006), Technical Program Committee (2005-2007), NBTI Discussion Group Leader (2005)

**18 Publications (7 Refereed Journal Publications, 2 Journal papers in internal review, and 9 Conference Proceedings):**

P.M. Lenahan, J.P. Campbell, A.Y. Kang, S.T. Liu, R.A. Weimer, *IEEE Trans. Nuc. Sci.*, **48**, 2101 (2001)

P.M. Lenahan, A.Y. Kang, and J.P. Campbell, *Proceedings of the International Workshop on the Physics of Semiconductor Devices,* V Kumar and PK Basu editors, Allied Publishers, New Delhi, pp. 608-615 (2001)

P.M. Lenahan, J.J. Mele, J.P. Campbell, A.Y. Kang, R.K. Lowry, D. Woodbury, S.T. Liu, and R. Weimer, *Proceedings of the IEEE International Reliability Physics Symposium*, pp. 150-155 (2001)

P.M. Lenahan, N.A. Bohna, J.P. Campbell, *IEEE Trans. on Nuc. Sci.*, **49**, 2708 (2002)

J.P. Campbell and P.M. Lenahan, *Appl. Phys. Lett.,* **80**, 1945 (2002)

P.A. Kraus, T.C. Chua, A. Rothschild, F.N. Cubaynes, A. Veloso, S. Mertens, L. Date, T. M. Bauer, K. Z. Ahmed, J.P. Campbell, F. Nouri, J. Cruse, R. Schreutelkamp, and M. Schaekers, *Proceedings of the 205th Meeting of the Electrochemical Society*, 2004

J.P. Campbell, P.M. Lenahan, A.T. Krishnan, and S. Krishnan, "Atomic Scale Defects Involved in NBTI", *IEEE International Integrated Reliability Workshop Final Report*, pp. 118-120 (2004)

T.G. Pribicko, J.P. Campbell, P.M. Lenahan, W. Tsai, and A. Kerber, *Appl. Phys. Lett.*, **86**, 173511 (2005)

J.P. Campbell, P.M. Lenahan, A.T. Krishnan, S. Krishnan, *Appl. Phys. Lett.*, **87**, 204106 (2005)

J.P. Campbell, P.M. Lenahan, A.T. Krishnan, and S. Krishnan, "Observations of NBTI-induced Atomic Scale Defects", *IEEE International Integrated Reliability Workshop Final Report,* pp. 1-4 (2005)

J.P. Campbell, P.M. Lenahan, A.T. Krishnan, and S. Krishnan, *Proceedings of the IEEE International Reliability Physics Symposium*, pp. 442-447 (2006) **\*\*Awarded Outstanding Conference Paper\*\***

J.P. Campbell, P.M. Lenahan, A.T. Krishnan, S. Krishnan, *IEEE Trans. Device and Materials Rel.,* **6**, 117 (2006)

C.J. Cochrane, P.M. Lenahan, J.P. Campbell, G. Bersuker, and A. Neugroschel, *IEEE International Integrated Reliability Workshop Final Report*, pp. 11-15 (2006)

C.J. Cochrane, P.M. Lenahan, J.P. Campbell, G. Bersuker, and A. Neugroschel, *Appl. Phys. Lett.*, **90**, 123502 (2007)

J.P. Campbell, P.M. Lenahan, A.T. Krishnan, and S. Krishnan, *Proceedings of the IEEE International Reliability Physics Symposium*, pp. 503-510 (2007)

J.P. Campbell, P.M. Lenahan, A.T. Krishnan, S. Krishnan, awaiting Texas Instruments approval for submission to Applied Physics Letters (2007)

J.P. Campbell, P.M. Lenahan, A.T. Krishnan, S. Krishnan, awaiting Texas Instruments approval for submission to Journal of Applied Physics (2007)

**J.P. Campbell has first-authored 7 oral presentations, 1 poster presentation, and co-authored an additional 24 presentations at national and international conferences**