The Pennsylvania State University
The Graduate School
Department of Materials Science and Engineering

DESIGN OF SHALLOW AND THERMALLY STABLE
CONTACTS ON ANTIMONIDE-BASED SEMICONDUCTORS

A Thesis in
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by
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This dissertation addresses the development of shallow and thermally stable metallizations for Sb-based compound semiconductors for high speed, low power electronic devices. The factors that influence the contact resistance, thermal stability, and shallowness of the ohmic contacts to p-InGaSb were investigated. These contacts are important for the base of a 6.2 Å heterojunction bipolar transistor. A non-alloyed low resistance Pd/W/Au (2/50/145 nm) ohmic contact prepared using an (NH₄)₂S rinse treatment was developed with a specific contact resistance of $5.9 \times 10^{-7} \, \Omega \, \text{cm}^2$. Tungsten serves as a diffusion barrier. Gold lowers the metal sheet resistance, which we have found both experimentally and through modeling to influence contact resistance measurements, and palladium is used to make intimate contact at the metal/semiconductor interface. It was observed by cross-sectional transmission electron microscopy that the (NH₄)₂S rinse treatment effectively minimizes the thickness of any residual dielectric layer on the semiconductor, leading to a reduction in the specific contact resistance. In addition, the specific contact resistances of various metal/W/Au (2/50/145 nm) contacts were compared, and the (NH₄)₂S rinse is found to partially relieve Fermi level pinning at the contact/p-InGaSb interface. Cross-sectional transmission electron microscopy reveals that the Pt/W/Au contacts have better thermal stability than Pd/W/Au contacts, with the Pt/W/Au contacts remaining shallow even after they are aged at 250 °C for 3 days.

The thermal stability of various gate metallizations on InAs/AlGaAsSb/InAs heterostructures with and without the InAs cap removed was also investigated. These
metallizations are important for high electron mobility transistors fabricated from the antimonide based compound semiconductors. The W/Au gate was found to be a good candidate for making stable contacts directly to AlGaAsSb. The Ti/Pt/Au (50/50/100 nm) and Co/Si/Co/Si/Co metallizations are more thermally stable on InAs than other metallizations tested. It was observed by the cross-sectional transmission electron microscopy that a degradation in the current-voltage characteristics is associated with the metal/InAs reactions, and a proposed energy band diagram was used to explain the degradation mechanism.
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Chapter 1

INTRODUCTION AND METAL/SEMICONDUCTOR CONTACT

1.1 General Background

The lattice matched 6.1 – 6.2 Å antimonide based compound semiconductors (ABCS), including ternary and quaternary alloys, are currently of interest for optoelectronics and high speed, low power electronic devices. The potential applications include low voltage photoconductive detectors for environmental sensing,[1],[2] mid infrared lasers in the wavelength region from 1 - 5 µm,[3],[4] low noise amplifiers (< 1dB), and low voltage, high frequency integrated circuits (ICs) for analog to digital converters used in digital oscilloscopes, digital cameras and CD players[5]. Recently, Sb-based ICs with an enhanced cut-off frequency in excess of 200 GHz and a 1/10 reduction in power consumption compared to the InP-based devices were reported by all DARPA’s ABCS program participants (Hughes Research Laboratory, Rockwell Scientific and Northrop Grumman Space Technology).[6] The improved performance is attributed to the superior properties of the ABCS.

The properties of the ABCS and other selected semiconductors are listed in Table 1.1.[7],[8] Although Sb-based semiconductors have lower melting points compared to nitrides, carbides, and other semiconductors, higher carrier mobility (77,000 cm²/V s for InSb, 33,000 cm²/V s for InAs, 5000 cm²/V s for GaSb, and 4600 cm²/V s for InP at 300 K) raises the operation frequency.[9] In contrast to the applications for the wide
bandgap semiconductors, the smaller energy bandgap of ABCS (0.36 eV for InAs and 0.17 for InSb) also reduces the turn on voltages, leading to lower power consumption. Inspection of Fig 1.1 reveals that the range of the lattice parameter for the Sb-based binary semiconductors is from 5.65 Å (for GaAs) to 6.48 Å (for InSb), which presents difficulty to avoid formation of dislocations during the heterostructure growth. This can be accomplished by employing the ternary and quaternary Sb-based semiconductors, in which the adjustment of the composition in the ternary or quaternary ABCS alters the lattice parameters along with the energy bandgap and carrier mobility.
Table 1.1: Selected properties of semiconductors at $T = 300 \text{ K}$.[7],[8]

<table>
<thead>
<tr>
<th>Semiconductor</th>
<th>Bandgap (eV)</th>
<th>Electron/Hole Mobility (cm²/V s)</th>
<th>Static Dielectric Constant</th>
<th>Lattice Constant (Å)</th>
<th>Density (g/cm³)</th>
<th>Melting Point (K)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Si</td>
<td>1.12</td>
<td>1400/470</td>
<td>11.7</td>
<td>5.43095</td>
<td>2.328</td>
<td>1685</td>
</tr>
<tr>
<td>Diamond</td>
<td>5.45</td>
<td>1900/1600</td>
<td>5.5</td>
<td>3.57</td>
<td>3.5</td>
<td>~ 4000</td>
</tr>
<tr>
<td>3C-SiC</td>
<td>2.3</td>
<td>800/40</td>
<td>9.7</td>
<td>4.36</td>
<td>3.5</td>
<td>&gt; 2100</td>
</tr>
<tr>
<td>6H-SiC Hexagonal</td>
<td>3.03</td>
<td>400/100</td>
<td>9.7</td>
<td>$a = 3.081$</td>
<td>3.2</td>
<td>&gt; 2100</td>
</tr>
<tr>
<td>InN Wurtzite</td>
<td>1.89</td>
<td>3200/15</td>
<td>15.3</td>
<td>$a = 3.544$</td>
<td>6.81</td>
<td>1373</td>
</tr>
<tr>
<td>AlN Wurtzite</td>
<td>6.2</td>
<td>135/14</td>
<td>8.5</td>
<td>$a = 3.111$</td>
<td>3.23</td>
<td>3273</td>
</tr>
<tr>
<td>GaN Wurtzite</td>
<td>3.39</td>
<td>1000 bulk/30</td>
<td>9</td>
<td>$a = 3.189$</td>
<td>6.15</td>
<td>&gt; 1973</td>
</tr>
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<td>GaAs</td>
<td>1.42</td>
<td>8000/340</td>
<td>12.8</td>
<td>5.6533</td>
<td>5.32</td>
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<td>6.0959</td>
<td>5.619</td>
<td>980</td>
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<tr>
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<td>6.0584</td>
<td>5.66</td>
<td>1215</td>
</tr>
<tr>
<td>InP</td>
<td>1.35</td>
<td>4600/150</td>
<td>12.5</td>
<td>5.8693</td>
<td>4.787</td>
<td>1330</td>
</tr>
<tr>
<td>InSb</td>
<td>0.17</td>
<td>77000/1000</td>
<td>17.9</td>
<td>6.4794</td>
<td>5.775</td>
<td>798</td>
</tr>
<tr>
<td>AlAs</td>
<td>2.16</td>
<td>1200/400</td>
<td>10.1</td>
<td>5.6622</td>
<td>3.81</td>
<td>1870</td>
</tr>
<tr>
<td>AlSb</td>
<td>1.6</td>
<td>200/420</td>
<td>14.4</td>
<td>6.1355</td>
<td>4.218</td>
<td>1330</td>
</tr>
</tbody>
</table>
Heterojunction bipolar transistors (HBT) and high electron mobility transistors (HEMT) in particular are therefore promising for high speed low power device applications. From the device design point of view, the contact resistance (voltage drop across metal/semiconductor interface) and the lifetime of the contacts are critical parameters. The contacts must be shallow and thermally stable, not consuming many tens of nanometers of semiconductor, to avoid inadvertently contacting underlying layers of a device. The ideal contact remains shallow not only during processing and packaging, but also during long-term operation of the device. Hence, the major objective of this thesis is the development of shallow, thermally stable ohmic contacts to p-In$_{0.25}$Ga$_{0.75}$Sb (for the base of an HBT) and gate metallizations on Al$_{0.80}$Ga$_{0.20}$As$_{0.16}$Sb$_{0.84}$/InAs and InAs/Al$_{0.80}$Ga$_{0.20}$As$_{0.16}$Sb$_{0.84}$/InAs (for HEMTs) when the semiconductor layers to be contacted are less than 50 nm thick.

Fig 1.1: Bandgap as a function of lattice parameter for III-V semiconductors. (Data for plot taken from [7])
This thesis describes studies of the shallow, thermally stable ohmic contacts to p-
In$_{0.25}$Ga$_{0.75}$Sb and gate metallizations to Al$_{0.80}$Ga$_{0.20}$As$_{0.16}$Sb$_{0.84}$/InAs and 
InAs/Al$_{0.80}$Ga$_{0.20}$As$_{0.16}$Sb$_{0.84}$/InAs (for HEMTs). This work includes the use of metal-III-
V phase equilibria to select candidates for non-reactive contacts. Aging of the 
metallizations was performed because of the need for processing and packaging at 250 
°C, while 100 °C was selected for some accelerated aging studies to simulate devices in 
operation. The electrical parameters of contact resistance or leakage current density, as 
well as the reaction depth, were taken into consideration and evaluated.

1.2 Metal/Semiconductor Contacts

When an intimate metal/semiconductor (M/S) contact is made, it can provide 
either a rectifying Schottky contact or an ohmic contact. Schottky contacts exhibit 
rectifying I-V characteristics with low levels of current at reverse bias, and current flows readily across the M/S interface at forward bias. Conversely, ohmic contacts have linear 
or quasi-linear I-V characteristics at both forward and reverse biases with a low specific 
contact resistance ($\rho_C$), which is the area-independent resistance at the interface between 
the metal and the semiconductor.

1.2.1 Schottky Barriers

When a metal and a semiconductor contact each other, the Fermi level ($E_F$) at the 
semiconductor surface can either shift with the contact metal (Schottky-Mott theory), or
remain fixed independent of the metal work function due to surface states (Bardeen limit).\[10\]

1.2.1.1 Schottky-Mott Limit

The Schottky-Mott limit describes a barrier height for current transport at the M/S interface when the Fermi level position near the semiconductor surface is unpinned. In other words, no surface/interface states are present at the M/S interface. The Fermi level is the energy level at which electrons have a 50% probability of occupancy of a state.\[11\] The potential difference between the conduction band ($E_C$) and the vacuum level is the electron affinity of the semiconductor ($\chi_s$), and the energy difference between vacuum level and the Fermi level is the work function ($\Phi_m$). Fig 1.2 (a) shows the energy band diagram of a metal with a larger work function than that of an n-type semiconductor. When the metal and semiconductor are separated from each other, both are electrically neutral. After they contact to each other, the two Fermi levels are forced into coincidence. Electrons then pass from the semiconductor to the metal, leading to a region depleted of electrons. Hence, band bending occurs at the surface of the semiconductor with a depletion width ($W$), and a barrier for electron transport from the metal to the semiconductor is formed at the interface ($\Phi_{bn}$), as shown in Fig 1.2 (a). The energy barrier is known as Schottky barrier, and is approximately the difference between the metal work function and the electron affinity at the semiconductor surface.

$$\Phi_{bn} = \Phi_m - \chi_s \quad \text{Eq 1.1}$$
Similarly, Fig 1.2 (b) shows the energy band diagram of a metal with a smaller work function than that of a p-type semiconductor. After they contact to each other, holes are transported from the semiconductor to the metal, leading to band bending downward at the semiconductor surface. A barrier for hole transport from the metal to the semiconductor is formed at the interface ($\Phi_{bp}$), and can be estimated by Eq 1.2,

$$\Phi_{bp} = E_g + X_s - \Phi_m$$  \hspace{1cm} Eq 1.2

where $E_g$ is the bandgap of the semiconductor.

The above discussion shows that the metal work function is a function of the barrier height, and one could employ Eq 1.1 or Eq 1.2 to design a metal contact to an n-type or a p-type semiconductor, respectively. However, an ideal M/S interface is difficult...
to achieve experimentally. Surface oxides, contamination, or even the metallization process itself could produce the surface states on the semiconductor, which could consequentially lead to a barrier height that is almost independent of the contact metals.

1.2.1.2 Bardeen’s Model

Fig 1.3 shows the metal/p-type semiconductor contact in the presence of the dielectric layer, and a continuous distribution of surface states at the dielectric layer/semiconductor interface is characterized by a neutral level $\Phi_o$. In the absence of surface states, the positive charge on the metal surface ($Q_m$) must be equal and opposite to the negative charge in the depletion region ($Q_d$) due to the uncompensated acceptors to maintain charge neutrality. Similarly, in the presence of the surface states ($Q_{ss}$),

$$Q_m + Q_d + Q_{ss} = 0.$$ \hspace{1cm} Eq 1.3

As shown in Fig 1.3, if the neutral level of the interface states is lower than $E_F$, the interface contains a net negative charge, which leads to a smaller $Q_d$ compared to that in the absence of surface states. Consequentially, the width ($w$) of the depletion region will be decreased along with the amount of the band bending (proportional to $w^2$) and the barrier height, i.e., pushing $\Phi_o$ toward $E_F$. In this case, the barrier height is no longer dependent on the metal work function, and is approximately the difference between the energy bandgap and the neutral level, as given by[10]

$$\Phi_b = E_g - \Phi_o.$$ \hspace{1cm} Eq 1.4
1.2.2 Ohmic Contacts

In the limiting case of the Schottky-Mott limit, a contact metal must be chosen with a work function equal to the electron affinity of the semiconductor in order to obtain a low resistance ohmic contact to an n-type semiconductor. On the other hand, for an low resistance ohmic contact to a p-type semiconductor, the metal work function must be approximately equal to the sum of the band gap and the electron affinity of the semiconductor. However, in the presence of surface states, the choice of the metal influences the barrier height less strongly. Therefore, other methods must be explored to achieve ohmic behavior.

There are three basic types of conduction mechanisms for carrier transport across the interface between metals and semiconductors: thermionic emission (TE), field emission (FE), and thermionic-field emission (TFE). For semiconductors with low doping concentrations, the depletion width is relatively large and the conduction across the interface is normally dominated by thermionic emission (TE), with the carriers

Fig 1.3: Metal/semiconductor contact with surface states.
thermally excited over the barrier. Assuming a low to moderately doped n-type semiconductor, the I-V relationship is given by Eq 1.5.[10],[12]

\[ J = A^* T^2 \exp\left(-\frac{q\Phi_b}{kT}\right)[\exp\left(\frac{eV}{kT}\right) - 1], \]  

Eq 1.5

where \( k, q, \) and \( A^* \) are the Boltzmann constant, elementary charge, and the effective Richardson constant, respectively. In addition, the specific contact resistance is defined as the reciprocal of the derivative of current density with respect to voltage evaluated at zero bias.

\[ \rho_c = \left(\frac{\partial J}{\partial V}\right)^{-1} \bigg|_{V=0} \]  

Eq 1.6

With Eq 1.5 and Eq 1.6 we can derive the specific contact resistance for TE dominated carrier transport mechanism.[12]

\[ \rho_c = \frac{k}{qA^* T} \exp\left(\frac{q\Phi_b}{kT}\right) \]  

Eq 1.7

For a heavily doped semiconductor, the depletion width is sufficiently narrow at the interface. Consequentially, tunneling probabilities become high and the field emission mechanism (FE) will dominate. The I-V relationship is then

\[ J \approx J_{OF} \exp\left(\frac{qV}{E_{00}}\right), \]  

Eq 1.8

where

\[ J_{0F} = \frac{\pi A^* T}{kC_1 \sin(\pi kT C_1)} \exp\left(-\frac{q\Phi_b}{E_{00}}\right), \]  

Eq 1.9
and

\[ C_1 = (2E_{00})^{-1} \ln\left[ \frac{-4(\Phi - V)}{\xi} \right], \quad \text{Eq 1.11} \]

where \( N_d \) is the donor impurity density, \( m^* \) is the effective mass, \( \varepsilon_s \) is the semiconductor dielectric constant, and \( \xi = E_C - E_F \). The specific contact resistance can be written as [12]

\[
\rho_c = \left( \frac{A^*\pi q}{k \sin(\pi C_t k T)} \exp\left( \frac{q\Phi_b}{E_{00}} \right) - \frac{A^* q}{C_1 k^2} \exp\left[ \frac{-q\Phi_b}{E_{00}} \right] \right) + C_1 q \xi \right)^{-1}, \quad \text{Eq 1.12}
\]

In Eq 1.8, Eq 1.9, and Eq 1.12, the tunneling currents are exponentially increased with \( \sqrt{N_D} \), and a low specific contact resistance could be obtained for a highly doped semiconductor at low temperatures.

The third mechanism is thermionic-field emission (TFE) for intermediate doping ranges. It is a combination of thermionic emission (TE) and field emission (FE) with an I-V relationship of

\[
J \approx J_{OTF} \exp\left( \frac{qV}{E_0} \right), \quad \text{Eq 1.13}
\]

where

\[
J_{OTF} = \frac{A^* T \sqrt{\pi E_{00} q(\Phi_b - V - \xi)}}{k \cosh(E_{00} / k T)} \exp\left( \frac{-q\xi}{kT} - \frac{q}{E_0} (\Phi_b - \xi) \right), \quad \text{Eq 1.14}
\]

\[
E_0 = E_{00} \coth(E_{00} / k T), \quad \text{Eq 1.15}
\]
These transport regimes can be distinguished by the comparison of a characteristic energy, $E_{00}$, with the thermal energy ($kT$). The characteristic energy $E_{00}$ is expressed in Eq 1.9. When $kT \gg E_{00}$, thermionic emission dominates. The dominant current transport mechanism is thermionic emission, thermionic-field emission, and thermionic-field emission when $kT \gg E_{00}$, $kT \approx E_{00}$, and $kT \ll E_{00}$, respectively.[12]

From Eq 1.7, the specific contact resistance ($\rho_c$) of a lightly doped semiconductor can vary exponentially with the barrier height. For a heavily doped semiconductor, the specific contact resistance varies exponentially with the factor $(\sqrt{\Phi_b / N_d})$, as shown in Eq 1.14. However, in practice, it is difficult to measure the real specific contact resistance. This is because experimentally the specific contact resistance measurement includes a portion of the metal immediately above the M/S interface, a part of the semiconductor below that interface, and any dielectric layer at the interface.[7] Therefore, control of contamination, surface oxides, M/S reactions, or interfacial defects is required for obtaining an ideal interface condition.
Chapter 2

HIGH ELECTRON MOBILITY TRANSISTORS AND HETEROJUNCTION BIPOLAR TRANSISTORS

In this chapter, the main components for high speed, low power devices are introduced. Metallizations should exhibit low leakage currents for the gate of the high electron mobility transistors (HEMTs) and ohmic contacts for the heterojunction bipolar transistors (HBTs). In addition, good control of the M/S reaction is needed for the metallizations to HEMTs and HBTs because the voltage drop across the M/S interface and the thickness of these layers are critical for device performance. Hence, shallow, thermally stable contacts are required to avoid inadvertently contacting underlying layers during device processing, packaging, and operation.

2.1 High Electron Mobility Transistors

The high electron mobility transistor (HEMT) was developed from the basic concept of field effect transistors, in which the contacts are fabricated on the source, gate, and drain. The source and drain require low resistance ohmic contacts for carrier flow in and out of the HEMT. The applied bias on the gate controls current in the channel layer, and the barrier layer is made sufficiently thin so that it is totally depleted under equilibrium conditions by the built-in potential associated with the gate contact.[13] Fig 2.1 shows a cross section of AlGaAs/GaAs material system that was the first HEMT developed[13],[14]. It consists of a heavily doped $n$-AlGaAs layer on top of an undoped
AlGaAs spacer followed by an undoped GaAs channel layer and a semi-insulating GaAs substrate. Due to the Fermi level line-up to establish thermal equilibrium at the junction, the carrier transport occurs between AlGaAs/GaAs, which consequentially causes the energy band bending at the heterojunction interface for both sides, as shown in Fig 2.2. Electrons pass from the AlGaAs (wide bandgap semiconductor) to GaAs (narrow bandgap semiconductor) and holes transport in the opposite direction, resulting in the AlGaAs upward and GaAs downward band bending at the interface. Therefore, a confined quantum well with high density of electrons is formed at the interface in the GaAs channel, and is referred to as a 2-dimensional electron gas (2-DEG).

Fig 2.1: A typical AlGaAs-GaAs HEMT.
The electrons in the 2-DEG are physically separated from the impurities so that the impurity scattering effect is reduced, resulting in an enhanced electron mobility and effective velocity under an electric field. The electron density in the 2-DEG can be controlled by the applied gate voltage, as described by Eq 2.1.13

\[ n_s = \frac{\varepsilon}{q(d + \Delta d)}(V_g - V_{th}), \]  

Eq 2.1

where \( \varepsilon \) is the permittivity of the \( n \)-AlGaAs, \( d \) is the thickness of the doped and undoped AlGaAs layer, and \( V_g \) is the applied gate voltage. \( V_{th} \) is the threshold voltage given in Eq 2.2.13

\[ V_{th} = \Phi_b - \Delta E_C - \frac{qN_{d}d_{d}^{2}}{2\varepsilon} + \Delta E_{FO}. \]  

Eq 2.2

\( \Phi_b \) is the Schottky barrier height, \( d_d \) is the thickness of the doped AlGaAs, \( \Delta d \) and \( \Delta E_{FO} \) are correction factors (in the AlGaAs-GaAs system \( \Delta d \sim 80\text{Å} \) and \( \Delta E_{FO} \sim 0 \)).13
As indicated in Eq 2.1, the electron density in the 2-DEG is proportional to the inverse function of the barrier layer thickness \((1/d)\). Hence, the thickness of the barrier layer has to be sufficiently thin in order to have a high electron density in the 2-DEG. Furthermore, for the operation of HEMTs, the I-V characteristics can be written as
\[ I_D = \frac{e\mu W}{2L(d + \Delta d)} \{2(V_g - V_{th})V_{DS} - V_{DS}^2 \}, \]  

Eq 2.3

where \(L\) is the channel length, \(\mu\) is the permeability, and \(V_{DS}\) is the source to drain voltage. When sufficient \(V_{DS}\) is applied to reach the carrier saturation velocity, Eq 2.3 becomes
\[ I_D(sat) = \frac{eW}{2L(d + \Delta d)}(V_g - V_{th} - V_0)V_{sat}. \]  

Eq 2.4

\(V_{sat}\) is the saturation velocity, \(V_0 = L\ E_s\), and \(E_s\) is the electric field in the channel to produce the saturation velocity.

The above discussion shows that to achieve maximum performance of the HEMT, despite bandgap engineering of the heterostructures, high quality metallizations for the gate on the HEMT is a key component. This becomes evident from Eq 2.1, Eq 2.3 and Eq 2.4, in which a thin barrier layer is desired for high electron density in 2-DEG, and the gate voltage is a critical component for controlling electron density in the 2-DEG and drain currents. An unwanted voltage drop, created by a high leakage current at the gate, or thickness change of the barrier layer due to the M/S reactions, can greatly degrade the performance. Therefore, to develop high speed, low power dissipation devices, shallow and thermally stable gate metallizations with low leakage currents are required.
### 2.2 Heterojunction Bipolar Transistors

A heterojunction bipolar transistor (HBT) consists of three separately doped regions with two pn junctions that are sufficiently close to interact with each other. Fig 2.3 shows a typical npn HBT structure and the corresponding band diagram with a very heavily doped (n++) emitter, moderately doped (p+) base, and lightly doped (n) collector.[13] Metallizations are required on the emitter, base, and collector for operation.

When an electric field is applied at the emitter-base (E-B) junction, electrons are injected from the emitter across the junction into the base, and create excess minority carriers in the base. Simultaneously, a separate electric field is applied across the base-collector (B-C) junction to remove or minimize the minority carriers at the edge of the B-C junction, and the electric field sweeps the electrons toward the collector, generating a high velocity of electrons in the collector.

![Fig 2.3: An npn HBT structure and energy band diagram.](image)

For the device performance, the base current ($I_B$) and the collector current ($I_C$) are a function of the B-E voltage ($V_{BE}$) by[7]
where \( R_B \), \( R_E \), and \( n \) are the base resistance, emitter resistance, and ideality factor, respectively. The logarithm of the \( I_B \) or \( I_C \) against \( V_{BE} \) plot is called a Gummel plot. For an \( I_B-V_{BE} \) Gummel plot, the base current usually has two linear regions. A linear fit applied to the low voltage region yields a slope of \( \ln(\frac{q}{nkT}) \), for which the E-B space charge region dominates. At intermediate voltages, the slope of the linear fit is \( \ln(\frac{q}{nKT}) \) with \( n = 1 \), which is the same as the ideality factor in the \( I_C-V_{BE} \) Gummel plot, and the B-C space charge region dominates.\[15\]

As described above, E-B and B-C junctions determine the performance of HBTs, and the width of the base needs to be smaller than the minority carrier diffusion length in order for electrons to diffuse through the base without recombination with majority holes in the base region. As a result, shallow, thermally stable ohmic contacts to the base layer of a HBT are particularly important for low power dissipation and high speed operation.
3.1 Literature Review

Semiconductor alloys containing GaSb, including In$_{0.25}$Ga$_{0.75}$Sb, are currently of interest for optoelectronic devices as well as high frequency, low power electronic devices.[16] While there are no reports to our knowledge on ohmic contacts to p-InGaSb, studies of ohmic contacts to p-GaSb have been described by several authors. Ohmic contacts to p-GaSb are easily obtained due to Fermi level pinning near the valence band edge, and specific contact resistances below $10^{-7}$ Ω cm$^2$ have been reported by Tadayon et al. for Au/p-GaSb contacts annealed at 200 °C for 60 s.[17] These contacts retained a low resistance when held at 100 °C for 10 h, but they degraded when annealed at 250 °C for 60 s, conditions even milder than those that Milnes et al.[18] found lead to degradation of Au/p-GaSb contacts (350 °C for 30 h). Both findings are consistent with the work of Piotrowska et al.[19], who report poor metallurgical stability of Au and Au-based contacts to GaSb. In fact, Piotrowska et al. observed a 100 nm thick reaction layer using transmission electron microscopy after Au (Zn) contacts to p-GaSb were annealed for only 3 min at 180 °C. Furthermore, after Au contacts were annealed at 300 °C, a reaction layer 750 nm thick was measured using Rutherford backscattering spectroscopy.[19]
Milnes et al. have reported significantly improved stability in the electrical performance of Ag/p-GaSb contacts compared to Au/p-GaSb contacts.\cite{18} Their Ag/p-GaSb ohmic contacts with a specific contact resistance of $5 \times 10^{-6}$ Ω cm$^2$ were stable for at least 30 h at 350 °C. Of course, desirable electrical behavior does not guarantee that a contact is shallow, and in a later study of Ag/n-GaSb contacts by Li and Milnes, the formation of Ag-Ga and Ag-Sb phases were observed by x-ray diffraction even after annealing for only 10 s at 400 °C.\cite{20} A comparably low specific contact resistance of $5.8 \times 10^{-6}$ Ω cm$^2$ was reported by Vogt et al. for Au/Pt/Ti/p-GaSb ohmic contacts, although the resistance increased greatly after the contacts were annealed at 450 °C for 90 s.\cite{21} Using transmission electron microscopy, however, they also observed a rough interface in Ti/GaSb contacts annealed at 200 °C for 2 h, which is undesirable for a shallow contact.\cite{21} The same group later reported Au/Pd/p-GaSb contacts with as-deposited specific contact resistances ranging from $3 \times 10^{-6}$ – $2.9 \times 10^{-7}$ Ω cm$^2$.\cite{22} This contact reproducibly provided lower resistance than did Ti/Au, Pt/Au, Ni/Au and Au contacts. Annealing did not improve the electrical performance of the Pd/Au contacts, and their thermal stability was not discussed.

In some cases, shallow contacts that do not consume many tens of nanometer of semiconductor are required to avoid inadvertently contacting underlying layers of a device. Since low-resistance ohmic contacts to p-GaSb have previously been formed without annealing, non-annealed contacts might be considered for these applications; however, the contacts will generally still be subjected to heat treatment during subsequent device processing and packaging. Therefore, this approach does not ensure that the contact will remain shallow when it is packaged, and it furthermore may not remain
shallow during long-term operation of the device. To avoid any reaction when the contacts are stressed, a contact in thermodynamic equilibrium with the semiconductor could instead be chosen, but this approach also has a potential drawback: a moderate reaction between the metal and semiconductor is often beneficial for lowering the interfacial resistance and more importantly for improving the reproducibility of the contacts. Since III-Sb surfaces oxidize fairly readily, this concern is likely to be particularly important for contacts to p-In$_{0.25}$Ga$_{0.75}$Sb.

The importance of the pre-metallization surface treatment for contacts to p-GaSb is illustrated by previous work, in which Tadayon et al. reported that contacts prepared using (1:1) HCl:H$_2$O for 30 s, followed by (1:1) buffered HF:H$_2$O for 30 s, yielded a reduced specific contact resistance compared to the same contacts prepared using H$_2$SO$_4$ solutions. Numerous studies have been reported on the surface passivation of p-GaSb. Dutta et al. observed that Schottky diodes treated with HCl followed by either (NH$_4$)$_2$S$_x$ solution or RuCl$_3$ solution exhibited reduced leakage currents compared to diodes treated with only HCl, and Liu et al. used x-ray photoelectron spectroscopy to examine GaSb surfaces treated with different etchants and rinsing solutions, identifying chemistries that provided reduced levels of oxygen at the semiconductor.

The Fermi level position for p-III(Ga,In)Sb semiconductors is known to be pinned near the valence band maximum due to a high level of surface states, which could be associated with a thin oxide layer, defects on the semiconductor surface, or defects induced by metal deposition. Therefore, the effect of the surface preparation on Fermi level pinning at the metal/p-InGaSb interface is examined. Cross-
sectional transmission electron microscopy (TEM) is also employed to examine the shallowness of the contacts before and after aging.

### 3.2 Experimental Procedure

Contacts were prepared on a 500 nm thick Be doped p-type In$_{0.25}$Ga$_{0.75}$Sb epilayer with a carrier concentration of $1.8 \times 10^{18}$ cm$^{-3}$ and mobility of 275 cm$^2$/Vs at 300K. The InGaSb film was grown on a 1.3 μm thick AlSb buffer layer on a semi-insulating GaAs (100) substrate. Samples were cleaved into 5 × 5 mm pieces and soaked in acetone and methanol for 5 minutes each, rinsed in de-ionized (DI) water, and then blown dry with compressed N$_2$ to remove organic contamination. Photolithography was performed to prepare circular transfer length method (CTLM) patterns for measuring specific contact resistance. Gap spacings of 2, 4, 8, 14, 20, 30, and 50 μm were used. Next, the samples were subjected to (1:1) HCl:H$_2$O for 30 s and then (1:1) HF:H$_2$O for 30 s to remove surface oxides followed by a rinse in DI water[17]. The samples were then promptly loaded into a vacuum chamber with a base pressure of 10$^{-7}$ Torr, and the films were deposited by DC magnetron sputtering. After deposition, samples were soaked in acetone and methanol with ultrasonic agitation to remove the photoresist, rinsed with DI water, and blown dry with compressed N$_2$. Current-voltage (I-V) characteristics were measured after deposition and after each heat treatment using a Keithley 236 source-measure unit in current sweep mode with 2 probes positioned on each contact (one for sourcing current and one for measuring voltage). Heat treatment was performed in a tube furnace under flowing UHP N$_2$ gas. Some contacts were sealed in quartz tubes at a pressure of 10$^{-4}$ Torr
(vacuum) before heat treatment. Gap spacings were measured using scanning electron microscopy for the CTLM calculations, and the reaction depth on a variety of samples was studied by performing Auger electron spectroscopy (AES) depth profiles. An area of approximately 100 µm² was sampled in each depth profile. Four point probe measurements were also performed to measure the sheet resistance of the metals used in the contacts. In this case, the metals were deposited on 2.5 cm × 5 cm SiO₂ (1 µm)/Si substrates. Cross-sectional transmission electron microscope (TEM) specimens were prepared from samples that were bonded face-to-face with an adhesive that was cured at 100 °C for 90 min. The samples were sliced, mechanically thinned, and ion milled in a Fischione 1010 ion mill to achieve electron transparency. Cross-sectional TEM was performed using a JEOL 2010F field-emission TEM. A Digital Instruments Dimension 3100 atomic force microscope (AFM) was used to measure the etch step of (NH₄)₂S solutions on p-InGaSb.

### 3.3 Design of a Shallow, Thermally Stable Ohmic Contact to p-Type InGaSb

The development of a shallow, thermally stable ohmic contact to p-In₀.₂₅Ga₀.₇₅Sb is described in this section. Contacts with single or double metal layers were initially tested (Pd, W, Pd/W, and W/Au). The Auger electron spectroscopy (AES) depth profiling was employed to study the thermal stability of the contacts, and the effect of the metal sheet resistance was modeled and measured.
3.3.1 Preliminary Results

Preliminary experiments compared Pd, W, Pd/W and W/Au contacts. Linear I-V curves were obtained after deposition and again after heat treatment for all samples studied in this work. The contact resistances of the as-deposited and annealed samples are listed in Table 3.1. Low resistance Pd contacts were observed as deposited with good reproducibility among 6 samples. The average contact resistance of the as-deposited Pd (100 nm)/p-InGaSb contacts is 0.21 Ω mm. The average contact resistance of two samples was reduced to 0.15 Ω mm after annealing at 150 °C for 1 h in N₂. More severe annealing at 200 °C for 1 h provided similar results, while an increase in contact resistance to 0.24 Ω mm was observed after the samples were annealed at 250 °C for 1 h.
Table 3.1: Comparison of different metal contacts to p-In$_{0.25}$Ga$_{0.75}$Sb.

<table>
<thead>
<tr>
<th>Annealing Condition</th>
<th>Apparent specific contact resistance (Ω cm$^2$)</th>
<th>Contact Resistance (Ω mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Pd (100 nm)</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>As-deposited (Average of 6 samples)</td>
<td>$(3.2 \pm 0.8) \times 10^{-6}$</td>
<td>$0.21 \pm 0.05$</td>
</tr>
<tr>
<td>150 °C, 1 h, N$_2$ (Average of 2 samples)</td>
<td>$(1.7 \pm 0.6) \times 10^{-6}$</td>
<td>$0.15 \pm 0.03$</td>
</tr>
<tr>
<td>200 °C, 1 h, N$_2$ (Average of 2 samples)</td>
<td>$(2.0 \pm 0.4) \times 10^{-6}$</td>
<td>$0.15 \pm 0.03$</td>
</tr>
<tr>
<td>250 °C, 1 h, N$_2$ (Average of 2 samples)</td>
<td>$(3.8 \pm 1.3) \times 10^{-6}$</td>
<td>$0.24 \pm 0.09$</td>
</tr>
<tr>
<td><strong>W (100 nm)</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>As deposited (Average of 2 samples)</td>
<td>$(3.6 \pm 0.0) \times 10^{-3}$</td>
<td>$10.4 \pm 1.01$</td>
</tr>
<tr>
<td>200 °C, 1 h, N$_2$</td>
<td>$(4.1 \pm 1.0) \times 10^{-4}$</td>
<td>$9.07 \pm 1.93$</td>
</tr>
<tr>
<td>+ Au (100 nm) post anneal</td>
<td>$(3.9 \pm 0.4) \times 10^{-6}$</td>
<td>$0.20 \pm 0.02$</td>
</tr>
<tr>
<td><strong>Pd/W (10/90 nm)</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>As deposited (Average of 4 samples)</td>
<td>$(1.3 \pm 0.1) \times 10^{-4}$</td>
<td>$2.06 \pm 0.14$</td>
</tr>
<tr>
<td>200 °C, 1 h, N$_2$ (Average of 2 samples)</td>
<td>$(1.0 \pm 0.1) \times 10^{-4}$</td>
<td>$1.85 \pm 0.19$</td>
</tr>
<tr>
<td>+ Au (100 nm) post anneal (Average of 2 samples)</td>
<td>$(1.4 \pm 1.2) \times 10^{-6}$</td>
<td>$0.12 \pm 0.10$</td>
</tr>
<tr>
<td><strong>W/Au (100/100 nm)</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>As deposited (Average of 2 samples)</td>
<td>$(3.7 \pm 1.6) \times 10^{-5}$</td>
<td>$0.97 \pm 0.40$</td>
</tr>
<tr>
<td>250 °C, 1 h, N$_2$ (Average of 2 samples)</td>
<td>$(4.5 \pm 2.5) \times 10^{-6}$</td>
<td>$0.34 \pm 0.16$</td>
</tr>
</tbody>
</table>
An apparent specific contact resistance of $3.2 \times 10^{-6} \, \Omega \, \text{cm}^2$ was extracted for the as-deposited Pd contact using the CTLM analysis, but this value and the other apparent specific contact resistance values in Table 3.1 were found to be artificially high due to the influence of the metal sheet resistance, as will be examined in more detail later. The specific contact resistance is used to describe an interfacial resistance at the metal/semiconductor interface, but the metal sheet resistance is assumed to be zero when using the conventional CTLM for extracting the specific contact resistance. The contact resistance, on the other hand, is an important device parameter that depends not just on the specific contact resistance but also on the semiconductor sheet resistance, metal sheet resistance, and contact geometry, and the contact resistance values reported in this paper are accurate even when the metal sheet resistance is not negligible.

AES depth profiles were carried out to examine the reaction depth of a Pd/p-InGaSb contact after deposition and after annealing at 150 °C for only 30 min in N₂, as shown in Figs 3.1 (a) and (b). Even for the as-deposited condition, a signal from Sb was observed on the sample surface, but little interdiffusion between the Pd and InGaSb was detected. After the anneal, interdiffusion between Pd and InGaSb was more pronounced, and In, Ga and Sb were present throughout the Pd layer. Based on the Pd-Ga-Sb phase diagram, even more extensive reaction is anticipated with more severe annealing, which predicts that PdGa and Sb will ultimately form in these contacts.[30] Although the Pd contacts exhibit a low resistance with good reproducibility both in our study and in the study of Au/Pd/p-GaSb contacts conducted by Vogt et al.[22], they may not remain shallow. According to the Pd-Ga-Sb phase diagram[31], if a 100 nm Pd film is annealed
on GaSb until thermodynamic equilibrium is achieved, 386 nm of GaSb will be consumed.

On the other hand, Liu and Mohney\cite{31,32} have estimated the phase equilibria in the metal-Ga-Sb and metal-In-Sb systems and have identified W as a candidate for a

![Graph](image)

**Fig 3.1:** AES depth profiles of a Pd (100 nm)/InGaSb contact (a) as deposited and (b) after annealing at 150 °C for 30 min in N2.

On the other hand, Liu and Mohney\cite{31,32} have estimated the phase equilibria in the metal-Ga-Sb and metal-In-Sb systems and have identified W as a candidate for a
contact in thermodynamic equilibrium with both GaSb and InSb. To test this prediction, AES depth profiles were collected for 100 nm thick W films on InGaSb after deposition and after annealing at 300 °C for 3 h in N₂, as shown in Figs 3.2 (a) and (b). In these profiles, no detectable interdiffusion between the W contact and InGaSb was observed, despite the fact that they were annealed under much more severe conditions than the Pd contact discussed above. Therefore, W (100 nm) was next tested as an ohmic contact. When the W contacts were fabricated, however, a much higher contact resistance was measured (10.4 Ω mm) compared to the Pd contacts. Annealing at 200 °C for 1 h in N₂ did little to improve the first of these contacts, resulting in a contact resistance of 9.07 Ω mm after annealing directly at 200 °C for 1 h in N₂. In an attempt to better engineer a shallow, low resistance ohmic contact to p-InGaSb, Pd/W (10/90 nm) contacts were next studied.
A thin Pd layer (10 nm) was deposited on p-InGaSb, followed by a 90 nm W layer. The average contact resistance for the 4 as-deposited Pd/W contacts was 2.06 $\Omega$ mm, which is much greater than that of the Pd (100 nm) contacts but less than that of W (100 nm). Annealing these contacts at 200 °C for 1 h in N$_2$ provided only a modest

Fig 3.2: AES depth profiles of a W (100 nm)/InGaSb contact (a) as deposited and (b) after annealing at 300 °C for 3 h in N$_2$. 

A thin Pd layer (10 nm) was deposited on p-InGaSb, followed by a 90 nm W layer. The average contact resistance for the 4 as-deposited Pd/W contacts was 2.06 $\Omega$ mm, which is much greater than that of the Pd (100 nm) contacts but less than that of W (100 nm). Annealing these contacts at 200 °C for 1 h in N$_2$ provided only a modest
improvement in the contact resistance (1.85 $\Omega$ mm). Since the Pd/W contacts exhibit a contact resistance so much greater than that of the Pd contacts, even though the same metal is in contact with the p-InGaSb, we suspected that the metal sheet resistance might be dominating the contact resistance of these contacts, as has been described in other studies.[33],[34] The influence of the metal sheet resistance on both the contact resistance and the accuracy of the extraction of the specific contact resistance was next explored, first through experiments and later by modeling.

To experimentally verify that the metal sheet resistance played an important role in the contact resistance measurements, we measured the contact resistance of the previously annealed 100 nm W contacts after deposition of a 100 nm Au overlay. The contact resistance decreased from 9.07 $\Omega$ mm to 0.20 $\Omega$ mm, as indicated in Table 3.1. We also prepared new samples in which the Au overlay was deposited on the W without breaking vacuum during the initial deposition step. In this case, the average contact resistance was 0.97 $\Omega$ mm as deposited and 0.34 $\Omega$ mm after annealing at 250 °C for 1 h in N$_2$. Finally, when a 100 nm Au overlay was added to annealed Pd/W (10/90 nm) contacts, the average contact resistance was reduced from 1.85 $\Omega$ mm to 0.12 $\Omega$ mm. These contacts provided the lowest contact resistance of all the contacts we had studied so far.

3.3.2 Design of Pd/W/Au Ohmic Contacts to p-InGaSb

Based on our preliminary work, we learned that reducing the metal sheet resistance was important for our contacts. We verified that W is a non-reactive contact on
InGaSb, while Pd reacts with InGaSb at moderate temperatures. On the other hand, Pd/W (10/90 nm) contacts capped with 100 nm of Au after annealing provide a lower resistance than similar W (100 nm) contacts. For the second set of experiments, a thin layer of Pd was to provide an intimate contact to p-InGaSb, W layers were used as diffusion barriers to protect the underlying contact from a Au cap, and the Au cap was used to lower the metal sheet resistance. A total thickness of 200 or 250 nm was used since thicker contacts can be difficult to lift off. A trade-off was expected between the thickness of the W, which will be a more effective barrier when it is thicker, and the thickness of the Au layer, which will decrease the metal sheet resistance the thicker it is deposited.

Table 3.2 lists the contact resistance for Pd/W/Au contacts of different layer thicknesses, and a Pd/Pt/Au (5/50/145 nm) contact was tested for comparison. The Pd/W/Au (2/145/100 nm) contacts were selected to minimize the consumption of InGaSb by Pd. The average contact resistance for the as-deposited Pd/W/Au (2/145/100 nm) contact was 0.47 $\Omega$ mm, while it was 0.45 $\Omega$ mm after annealing at 250 °C for 1 h. The average contact resistance for the as-deposited Pd/Pt/Au (5/50/145 nm) contact was 0.32 $\Omega$ mm, and reduced to 0.21 $\Omega$ mm after annealing for 2 h in N$_2$. On the other hand, Pd/W/Au contacts with 5 nm thick Pd layers provided much lower resistance. Three different layer thicknesses, (5/50/145 nm), (5/95/100 nm), and (5/145/100 nm), were examined in the as-deposited condition. All the I-V characteristics were linear, and good reproducibility was observed in 2 different deposition runs. In the as-deposited condition, the Pd/W/Au (5/50/145 nm) contact had the lowest contact resistance (0.08 $\Omega$ mm from an average of 3 samples), Pd/W/Au (5/145/100 nm) the second lowest (0.13 $\Omega$ mm from 3 samples), and Pd/W/Au (5/95/100 nm) contact the highest (0.24 $\Omega$ mm from 3
samples). An apparent specific contact resistance of \(2.8 \times 10^{-7} \, \Omega \, \text{cm}^2\) was calculated for the as-deposited Pd/W/Au (5/50/145 nm). Although the thick Au cap undoubtedly provides a low metal sheet resistance and lowers the resistance we measure, we have not yet determined if the metal sheet resistance still influences our measurement, so we can only assume at this point that the specific contact resistance (an interfacial parameter) is equal to or less than \(2.8 \times 10^{-7} \, \Omega \, \text{cm}^2\). Heat treatment at 250 °C in N\(_2\) was also performed. The contact resistance of Pd/W/Au (5/95/100 nm) dropped to 0.19 \(\Omega \, \text{mm}\) after 1 h, and the contact resistance of the Pd/W/Au (5/145/100 nm) contact was reduced to 0.08 \(\Omega \, \text{mm}\) after 3 h. We note that the relative performance of these three contacts could still be due to the effect of the metal sheet resistance because the thinnest metal contact (Pd/W/Au (5/95/100 nm)) provided the greatest contact resistance. We would not otherwise expect such a difference between the contacts prior to annealing since the same layer is deposited first on the semiconductor in each case. To further examine the extent to which the metal sheet resistance increases the contact resistance, modeling was performed, as described in the next section.
Table 3.2: Contact resistance and apparent specific contact resistance of Pd/W/Au contacts with different layer thicknesses.

<table>
<thead>
<tr>
<th>Annealing Condition</th>
<th>Apparent specific contact resistance (Ω cm²)</th>
<th>Contact Resistance (Ω mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pd/W/Au (2/145/100 nm)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>As-deposited (Average of 2 samples)</td>
<td>$(9.6 \pm 1.3) \times 10^{-6}$</td>
<td>$0.47 \pm 0.05$</td>
</tr>
<tr>
<td>250 °C, 1 h, N₂</td>
<td>$(8.4 \pm 0.8) \times 10^{-6}$</td>
<td>$0.45 \pm 0.04$</td>
</tr>
<tr>
<td>Pd/W/Au (5/50/145 nm)/cumulative annealing</td>
<td></td>
<td></td>
</tr>
<tr>
<td>As-deposited (Average of 3 samples)</td>
<td>$(2.8 \pm 2.4) \times 10^{-7}$</td>
<td>$0.08 \pm 0.07$</td>
</tr>
<tr>
<td>Pd/W/Au (5/95/100 nm)/cumulative annealing</td>
<td></td>
<td></td>
</tr>
<tr>
<td>As-deposited (Average of 3 samples)</td>
<td>$(1.9 \pm 0.4) \times 10^{-6}$</td>
<td>$0.24 \pm 0.02$</td>
</tr>
<tr>
<td>250 °C, 1 h, N₂</td>
<td>$(1.1 \pm 0.5) \times 10^{-6}$</td>
<td>$0.19 \pm 0.02$</td>
</tr>
<tr>
<td>Pd/W/Au (5/145/100 nm)/cumulative annealing</td>
<td></td>
<td></td>
</tr>
<tr>
<td>As-deposited (Average of 3 samples)</td>
<td>$(5.8 \pm 3.8) \times 10^{-7}$</td>
<td>$0.13 \pm 0.05$</td>
</tr>
<tr>
<td>250 °C, 1 h, N₂</td>
<td>$(5.0 \pm 3.2) \times 10^{-7}$</td>
<td>$0.12 \pm 0.04$</td>
</tr>
<tr>
<td>250 °C, 3 h, N₂</td>
<td>$(1.8 \pm 1.6) \times 10^{-7}$</td>
<td>$0.08 \pm 0.04$</td>
</tr>
<tr>
<td>Pd/Pt/Au (5/50/145 nm)/cumulative annealing</td>
<td></td>
<td></td>
</tr>
<tr>
<td>As-deposited (Average of 2 samples)</td>
<td>$(3.4 \pm 0.5) \times 10^{-6}$</td>
<td>$0.32 \pm 0.06$</td>
</tr>
<tr>
<td>250 °C, 2 h, N₂</td>
<td>$(1.4 \pm 0.5) \times 10^{-6}$</td>
<td>$0.21 \pm 0.09$</td>
</tr>
</tbody>
</table>
3.3.3 Effect of Metal Sheet Resistance on the Circular Transfer Length Method

Our analysis of the effect of the metal sheet resistance follows closely the work of Ahmad and Arora[34], who described the circular transfer length method in terms of the two-dimensional equivalent circuit shown in Fig 3.3. Here, $i_0$ is the applied current. $i_1/U$ and $i_2/V$ are the current/potential in the semiconductor and metal, respectively, which can be described in Eq 3.1 and Eq 3.2.

\[ \frac{dU(r)}{dr} = \frac{R_s}{2\pi r} i_1(r) \quad \text{Eq 3.1} \]

\[ \frac{dV(r)}{dr} = \frac{R_{sm}}{2\pi r} i_2(r) \quad \text{Eq 3.2} \]
Rs is the semiconductor sheet resistance, and R_{sm} is the metal sheet resistance. The sum of the current flowing through metal and semiconductor is the total current (Eq 3.3) and the specific contact resistance $\rho_C$ in terms of the potential drop across the contact is described in Eq 3.4.

$$i_1(r) + i_2(r) = i_0 \quad \text{Eq 3.3}$$

$$\frac{di_1(r)}{dr} = \frac{2\pi r}{\rho_C} (U - V) \quad \text{Eq 3.4}$$

From Eq 4.1 ~ 4.4 we can get the modified Bessel function.

$$r^2 \frac{d^2}{dr^2} (U - V) + r \frac{d}{dr} (U - V) - r^2 \frac{R_s + R_{sm}}{\rho_C} (U - V) = 0 \quad \text{Eq 3.5}$$

Solving the equation along with the boundary conditions $i_1(0) = 0$, $i_2(0) = i_0$, $i_1(a) = i_0$, and $i_2(a) = 0$ yields

$$U - V = \frac{R_s}{2\pi a k'} \frac{I_0(rk')}{I_1(ak')} \quad \text{Eq 3.6}$$

where $I_0$ and $I_1$ are the modified Bessel function of the first kind of order zero and one, and

$$k' = \sqrt{\frac{R_s + R_{sm}}{\rho_C}} \quad \text{Eq 3.7}$$

Moreover, substitute (U-V) in Eq 3.6 into Eq 3.4 gives

$$i_1(r) = \int \frac{2\pi r}{\rho_C} (U - V) dr = \frac{i_0 R_s}{a k'^2 \rho_C} \frac{I_1(rk')}{I_1(ak')} r \quad \text{Eq 3.8}$$

Therefore, the voltage drop across the inner contact ($V_i$) is
where \( b \) is the probe radius. In addition, we can find the expression for voltage drop across the gap (\( V_g \)) in terms of semiconductor sheet resistance (\( R_{ss} \)) as:

\[
V_g = \int_a^b \frac{R_{sm}}{2\pi r} I_2(r) dr - (U - V)|_a
\]

\[
= \left( \frac{R_{sm}}{2\pi} \ln \left( \frac{a}{b} \right) + \frac{R_s R_{sm}}{2\pi a^3 k^3 \rho_c} \frac{I_0(bk') - I_0(ak')}{I_1(ak')} \right) + \frac{R_s}{2\pi a k' I_1(ak')} \times i_0
\]  \quad \text{Eq 3.9}

Similarly, solving Eq 3.5 with the boundary condition \( i_1(a_1) = i_0, i_2(a_1) = 0, i_1(a_2) = 0, \) and \( i_2(a_2) = i_0 \), we obtain the following solutions.

\[
U - V = \frac{(R_s + R_{sm}) i_0}{2\pi a_i k'} K_0(rk') - K_1(a_i k') \]  \quad \text{Eq 3.11}

\[
i_1 = \int_{a_1}^r \frac{2\pi r(U - V)}{\rho_c} dr = i_0 - \frac{i_0 R_s}{a_i k'^2 \rho_c} \frac{K_1(rk')}{K_1(ak')} r + \frac{i_0 R_s}{k'^2 \rho_c} \]  \quad \text{Eq 3.12}

\( K_0 \) and \( K_1 \) are the modified Bessel function of the second kind of order zero and one. So that the voltage drop across the outer contact (\( V_O \)) becomes

\[
V_O = \int_{a_i}^a \frac{R_{sm}}{2\pi r} I_2(r) dr + (U - V)|_{a_i}
\]

\[
= \left( \frac{R_{sm}}{2\pi k'^2 \rho_c} \ln \left( \frac{a_i}{a_2} \right) + \frac{R_s R_{sm}}{2\pi a_i k'^3 \rho_c} \right) \times \frac{K_0(a_i k') - K_0(a_2 k')}{K_1(a_i k')} + \frac{R_s}{2\pi a_i k' K_1(a_i k')} \times i_0 \]  \quad \text{Eq 3.13}
Since the total voltage drop equals to the product of the total current \( (i_0) \) and resistance \( (R_T) \), combining Eq \( 3.9 \), Eq \( 3.10 \), and Eq \( 3.13 \), we arrived at a similar expression to that of Ahmad and Arora for the total resistance measured between a pair of contacts, \( R_T \), as given in Eq \( 3.14 \).

\[
R_T = \frac{R_{sm}}{2\pi} \ln\left(\frac{a}{b}\right) - \frac{R_{s}R_{sm}}{2\pi a k^3 \rho_C} I_0(ak') + \frac{R_{s}}{2\pi a k' I_1(ak')}
\]

\[
+ \frac{R_{ss} \ln\left(\frac{a_1}{a}\right)}{2\pi} + \frac{R_{s}R_{sm}}{2\pi a k^2 \rho_C} \ln\left(\frac{a_2}{a_1}\right)
\]

\[
+ \frac{R_{s}R_{sm}}{2\pi a k^3 \rho_C} \frac{K_0(a_2 k') - K_0(a_1 k')}{K_1(a_1 k')}
\]

The solution differs from that of Ahmad and Arora\(^{[34]} \) in the term \( R_{s}R_{sm} \ln\left(\frac{a_2}{a_1}\right)/(2\pi a k^3 \rho_C) \) (they have \( R_{sm} \ln\left(\frac{a_2}{a_1}\right)/2\pi \)). However, when the metal sheet resistance is much less than the semiconductor sheet resistance, the obtained solution simplifies to that of Ahmad and Arora\(^{[34]} \). By further assuming that the metal sheet resistance is very small and can be ignored, a simplified version of Eq \( 3.14 \) applies and is given in Eq \( 3.15 \).

\[
R_T = \frac{R_{s}L_T}{2\pi a} \frac{I_0(a/L_T)}{I_1(a/L_T)} + \frac{R_{s}L_T}{2\pi a_1} \frac{K_0(a_1/L_T)}{K_1(a_1/L_T)} + \frac{R_{ss}}{2\pi} \ln\left(\frac{a_1}{a}\right)
\]

Eq \( 3.15 \)

where \( L_T \) is the transfer length defined as

\[
L_T = \sqrt{\frac{\rho_C}{R_s}}.
\]

Eq \( 3.16 \)

For a given true value of the specific contact resistance, we can input the semiconductor sheet resistance and metal sheet resistance into Eq \( 3.14 \) to arrive at a value for \( R_T \) for each gap spacing. We can then take calculated resistances and fit them to
Eq 3.15, which neglects the metal sheet resistance during the CTLM calculation, to extract the apparent specific contact resistance we would calculate if we neglected the metal sheet resistance. Alternatively, we can use the calculated $R_T$ values to arrive at the contact resistance in $\Omega$ mm that would be measured for a given specific contact resistance, semiconductor sheet resistance, and metal sheet resistance.

For the case of the as-deposited Pd/W/Au (5/50/145 nm) contact, the apparent specific contact resistance was $2.8 \times 10^{-7} \ \Omega \ cm^2$. Using the metal sheet resistance we measured on a composite Pd/W/Au (5/50/145 nm) film deposited on an insulating substrate, $0.37 \ \Omega/\square$, and the semiconductor sheet resistance of $300 \ \Omega/\square$, the true specific contact resistance could be as low as $1.2 \times 10^{-9} \ \Omega \ cm^2$ (too low for us to accurately measure). This calculation demonstrates that the metal sheet resistance is very important for the Au/W/Pd/p-InGaSb contacts we have measured.

Simulations are plotted in Fig 3.4 to further demonstrate the effect of the metal sheet resistance on the apparent specific contact resistance. The true specific contact resistance corresponds to the value obtained with a zero metal sheet resistance. Assuming that the true specific contact resistance is $1.0 \times 10^{-7} \ \Omega \ cm^2$, the semiconductor sheet resistance is $300 \ \Omega/\square$ (the case in our study), and the metal sheet resistance is $0.5 \ \Omega/\square$ (or $0.1 \ \Omega/\square$), the apparent specific contact resistance becomes $9.8 \times 10^{-7} \ \Omega \ cm^2$ (or $2.0 \times 10^{-7} \ \Omega \ cm^2$). The metal sheet resistance has to be less than $0.012 \ \Omega/\square$ in order to obtain an error in the apparent specific contact resistance of no more than 10 % when using the simpler Eq 3.15 for extracting the specific contact resistance. As shown in the Fig 3.4, the influence of the metal sheet resistance is not as strong for higher values of the true
specific contact resistance, but an effect is observed even when the true specific contact resistance is $1.0 \times 10^{-5} \, \Omega \, \text{cm}^2$. If the semiconductor thickness were reduced to 1/10 of the thickness used in our study (reduced to 50 nm), as would be typical for the base of an HBT, the semiconductor sheet resistance would increase by approximately one order of magnitude to $3000 \, \Omega/\square$. If the true specific contact resistance were then $10^{-7} \, \Omega \, \text{cm}^2$, a metal sheet resistance of $< 0.04 \, \Omega/\square$ would allow an error in the apparent specific contact resistance of less than 10%. Thus, the metal sheet resistance has a greater effect on the CTLM measurement in the case of a lower semiconductor sheet resistance.

![Graph](image.png)

**Fig 3.4**: Apparent specific contact resistance as a function of metal sheet resistance. The semiconductor sheet resistance is $300 \, \Omega/\square$.

We can also examine the problem by calculating the effect of the metal sheet resistance on the contact resistance. **Fig 3.5** shows the contact resistance as a function of metal sheet resistance for a given true specific contact resistance of $10^{-7} \, \Omega \, \text{cm}^2$ and for semiconductor sheet resistances of 300 and 3000 $\Omega/\square$. The contact resistance is $0.055 \, \Omega$.
mm for a true specific contact resistance of $1 \times 10^{-7} \ \Omega \ \text{cm}^2$ and semiconductor sheet resistance of $300 \ \Omega/\square$ if the metal sheet resistance is assumed to be zero, but for metal sheet resistances of $0.5 \ \Omega/\square$ and $0.1 \ \Omega/\square$, the contact resistances are calculated to be $0.17 \ \Omega \ \text{mm}$ and $0.08 \ \Omega \ \text{mm}$, respectively. A metal sheet resistance of $< 0.02 \ \Omega/\square$ is necessary for obtaining an increase in contact resistance of less than 10 %. On the other hand, when the semiconductor sheet resistance is $3000 \ \Omega/\square$ and the true specific contact resistance is $10^{-7} \ \Omega \ \text{cm}^2$, the contact resistance is calculated to be $0.17 \ \Omega \ \text{mm}$ when the metal sheet resistance is assumed to be zero, and a metal sheet resistance of $< 0.07 \ \Omega/\square$ is required to avoid an increase in the contact resistance of more than 10 %.

Fig 3.5: Contact resistance as a function of metal sheet resistance for a true specific contact resistance of $1 \times 10^{-7} \ \Omega \ \text{cm}^2$ with semiconductor sheet resistances of 300 and 3000 $\ \Omega/\square$.

Finally, the relationship between the real specific contact resistance, metal sheet resistance, semiconductor sheet resistance, and the apparent specific contact resistance is
plotted in Fig 3.6. These simulations demonstrate that the effect of the metal sheet resistance is less severe as the real specific contact resistance increases. The metal sheet resistance also exerts a greater influence with decreasing semiconductor sheet resistance. The simulations also demonstrate that a very low metal sheet resistance is required for our ohmic contacts to p-InGaSb in order to measure an accurate specific contact resistance and to achieve the lowest possible contact resistance. On the other hand, our measurements are actually impacted by the large size of our contacts (100 µm radius). Much smaller contacts are often used in actual devices, making the effect of the metal sheet resistance less severe. For example, we could repeat our calculations for a contact with a radius of only 10 microns. For a true specific contact resistance of $10^{-7} \, \Omega \, \text{cm}^2$ and a semiconductor sheet resistance of 300 $\Omega/\square$, a metal sheet resistance as high as 0.11 $\Omega/\square$ would result in an error of only 10% when the apparent specific contact resistance was extracted using Eq 3.15. (This metal sheet resistance is much greater than the 0.012 $\Omega/\square$ value calculated for the 100 µm radius contacts.) Similarly, a metal sheet resistance of 0.22 $\Omega/\square$ could be tolerated before the contact resistance would increase by 10%.
Fig 3.6: 3-dimensional plot for the metal sheet resistance effect on apparent specific contact resistance with the real specific contact resistance of $1 \times 10^{-5}$, $1 \times 10^{-6}$, and $1 \times 10^{-7}$ Ω cm$^2$. 

Real $\rho_c = 1 \times 10^{-5}$ Ω cm$^2$

Real $\rho_c = 1 \times 10^{-6}$ Ω cm$^2$

Real $\rho_c = 1 \times 10^{-7}$ Ω cm$^2$
The discussion above could lead one to wonder if the differences in contact resistance among all of our different samples were due to differences in the metal sheet resistance. A pair of two samples, however, demonstrates that the metal in contact with the p-InGaSb is also still important. When we compare the Pd/W/Au (5/95/100 nm) contact and W/Au (100/100 nm) contact, we do not expect a great difference in the metal sheet resistance, but the contact resistances were 0.24 Ω mm for the as-deposited Pd/W/Au (5/95/100 nm) contact and 0.97 Ω mm for the as-deposited W/Au (100/100 nm) contacts. This result provides evidence that the 5 nm thick Pd layer inserted in our contacts lowers the resistance at the metal/semiconductor interface.

3.3.4 Thermal Stability of the Tungsten Barriers

The thermal stability of the low resistance Pd/W/Au ohmic contacts was next examined following heat treatment at 125 °C and 250 °C in evacuated quartz tubes, and at 250 °C in flowing N$_2$ gas. For the Pd/W/Au contact with the thinnest W layer (5/50/145 nm), aging in evacuated quartz tubes resulted in no obvious degradation after 24 h, although intermixing of the metal layers was observed after annealing at 250 °C for 1 h in N$_2$. A change in appearance from the original smooth, gold colored surface to a rough, silver-colored surface was observed. This difference in behavior when the contacts were aged in the two different environments was unexpected but was reproducible, and any possible differences in the temperatures to which the two samples were exposed can be ruled out because the heat treatment was performed in the same furnace. The difference might be due to enhanced degradation of the contact due to the accelerated loss
of Sb from the InGaSb in an open system (flowing N₂ gas), as has been observed in Au/GaSb and Au/InSb by Pugh and Williams[35], or it might instead be due to enhanced interdiffusion in a N₂ ambient.[36],[37] Ohkawa et al.[36] observed that the interdiffusion of Au/Co/Si at 350 °C for 15 min was significantly slower in forming gas (N₂-H₂ 0.01:1) than in dry N₂. Chang and Yeh[37] also observed that the interdiffusion of Au/Ni/Cu/SiO₂ at 350 °C was slowest in forming gas (N₂-H₂ 9:1) among the ambients of forming gas, hydrogen, and N₂-O₂ (4:1).

After the Pd/W/Au contact with the thinnest W layer (5/50/145 nm) was aged for 67 h in a sealed quartz tube, part of the sample surface remained the original Au color, and part exhibited a rough silvery surface similar to that of the intermixed sample annealed in N₂ for 1 h. The AES depth profiles of the as-deposited condition, as well as the smooth and rough areas on the surface of the sample aged for 67 h, are shown in Fig 3.7, 3.8, 3.9, respectively. For the smooth Au colored area of the aged contact (Fig 3.8), no change is observed in the AES depth profile compared to the as-deposited condition of Fig 3.7. However, for the rough silver-colored area, In, Ga, and Sb were detected in the metal layers, and Au was detected throughout the contact (Fig 3.9). Hence, the degradation of the surface morphology notified us of the non-uniformity of the contact and intermixing of the metal layers (Pd/W/Au) and p-InGaSb, which occurs severely once the W diffusion barrier fails. Although the contact resistance does not increase, the contact is no longer shallow after the W barrier fails. Au penetrates deeply into the semiconductor Thermal stability tests under milder annealing conditions were also performed. The same layer structure was aged at 125 °C in vacuum for 15 days, and
no degradation was observed in either the apparent specific contact resistance or the surface morphology.

Fig 3.7: AES depth profile of the Pd/W/Au (5/50/145 nm) contact as deposited.
Fig 3.8: AES depth profile of a smooth Au spot on the Pd/W/Au (5/50/145 nm) contact aged at 250 °C for 67 h in vacuum.

Fig 3.9: AES depth profile of a rough, silvery spot on the Pd/W/Au (5/50/145 nm) contact aged at 250 °C for 67 h in vacuum.
Similar experiments were performed on contacts with thicker W layers, and their contact resistance is plotted in Fig 3.10 as a function of time held in N₂ at 250 °C. AES depth profiles showed no mixing of the W and Au layers in the Pd/W/Au (5/95/100 nm) contacts after 1 h in N₂ or Pd/W/Au (5/145/100 nm) contacts after 100 h in N₂, similar to the depth profile shown in Fig 3.7. In fact, in all cases in this study for which the contact remained smooth and gold colored, the depth profiles looked like the profile in Fig 3.7, except that some contacts had thicker W layers than others. On the other hand, rough silver colored areas appeared on the contact surface, and significant mixing of the Pd/W/Au (5/95/100 nm) and Pd/W/Au (5/145/100 nm) contacts was observed, after aging at 250 °C in N₂ for 2 h and 150 h, respectively. Not surprisingly, the thickest W layer served effectively as a diffusion barrier to Au for the longest time.

![Graph showing contact resistance of Pd/W/Au contacts of different layer thicknesses aged at 250 °C in N₂.](image)

**Fig 3.10:** Contact resistance of Pd/W/Au contacts of different layer thicknesses aged at 250 °C in N₂.
In order to estimate the lifetime of the contacts, aging of the Pd/W/Au (5/50/100 nm), (5/95/100 nm), and (5/145/100 nm) contacts and a Pd/Pt/Au (5/50/145 nm) contact was performed at elevated temperatures in sealed quartz tubes. The failure of the barrier layers was determined by a change in the surface morphology or the color of the top surface, and the results are listed in Table 3.3.

Table 3.3: Failure time of the Pd/W/Au contacts at 200 °C, 250 °C, and 300 °C. (Average of four samples in each condition).

<table>
<thead>
<tr>
<th>(L)</th>
<th>(t) Failure Time (days)</th>
</tr>
</thead>
<tbody>
<tr>
<td>W Thickness (nm)</td>
<td>200 °C</td>
</tr>
<tr>
<td>50</td>
<td>44.50 ± 2.00</td>
</tr>
<tr>
<td>95</td>
<td>187.75 ± 7.00</td>
</tr>
<tr>
<td>145</td>
<td>263.50 ± 7.00</td>
</tr>
<tr>
<td>Pd/Pt/Au (5/50/145 nm)</td>
<td></td>
</tr>
</tbody>
</table>

The degradation in the surface morphology of the Pd/Pt/Au (5/50/145 nm) contacts was observed after aging for 18 h (0.75 day) in vacuum. On the other hand, no degradation in the surface morphology was observed after the Pd/W/Au (5/50/100 nm) contacts were aged for 3 days, and surface roughening was observed after 4 days aging, as listed in Table 3.3, which suggests that W is more promising for use as a diffusion barrier.

For the finite system to the Fick’s laws, the solution for the average concentration \( \overline{C} \) is[38]

\[
\frac{\overline{C} - C_S}{C_i - C_S} = \frac{8}{\pi^2} \exp\left(-\frac{t}{\tau}\right)
\]

Eq 3.17
where \( C_S \) is the surface concentration, \( C_i \) is the initial Au concentration in the W matrix, \( t \) is the time, and

\[
\tau = \frac{4L^2}{\pi^2 D(T)}.
\]

Eq 3.18

\( L \) is the thickness of the W barriers, and \( D(T) \) is the diffusivity of Au in W matrix at a temperature (T). The fractional concentration term in Eq 3.17 is required to determine the diffusivity but is unknown, and the solution for semi-infinite systems is often used for estimating diffusivity and activation energy for the failure of a thin barrier layer.[39] Therefore, the solution for the semi-infinite system is used, as described below.

Assuming that the Au in-diffusion is the rate limiting step for the degradation in the surface morphology, and the Au cap is thick enough to remain at a constant concentration on the W surface before the failure of the W barrier, the relationship between concentration profile and annealing time can be approximately expressed by[38]

\[
C(x, t) = C_S + (C_0 - C_s) \text{erf} \left( \frac{x}{2\sqrt{D(T) \times t}} \right).
\]

Eq 3.19

where \( C(x,t) \) is the concentration of Au at the diffusion time and distance \( x \), \( C_S \) is the surface concentration, and \( C_0 \) is the initial Au concentration in the W matrix, which is zero in our case. Eq 3.19 is then reduced to:

\[
D(T) = \frac{x^2}{4t[\text{erf}^{-1} \left( \frac{C(x,t) - C_S}{2C_S} \right)^2]}.
\]

Eq 3.20
Assuming that the fractional concentration term is a constant at the failure time for the W barriers when the distance \( x \) is equal to the thickness of the W barriers \( L \), it can be observed from Eq 3.20 that the diffusivity can be determined by a plot of \( x^2 \) vs. \( t \). Moreover, the relationship between the diffusion coefficient and temperature follows the Arrhenius equation.[38]

\[
D(T) = D_0 \times \exp\left(\frac{-Q}{kT}\right) \tag{Eq 3.21}
\]

where \( D_0 \) is the pre-exponential factor, and \( k \) and \( Q \) are the Boltzmann constant and activation energy, respectively. Therefore, by equating Eq 3.20 and Eq 3.21, the activation energy for the failure of W barriers can be extracted by plotting \( x^2/t \) verses \( 1/kT \). The result is shown in Fig 3.11.
Fig 3.11: $x^2/t$ as a function of $1/kT$ for 50 nm, 95 nm, and 145 nm thick W barriers.
It can be observed from Fig 3.11 that the estimated activation energies for 50 nm, 95 nm, and 145 nm thick W barriers at the temperature range of 300 – 250 °C are higher than those in the temperature range of 250 – 200 °C. This suggests that the activation energy for W barrier failure is dependent on the annealing temperature. Despite the possible variations in the experiment, such as samples heating up during sealing in quartz tubes, vacuum condition, or W thickness, the failure mechanism associated with temperature dependence of the Au in-diffusion rate and the elemental out-diffusion rate from the InGaSb, In, Ga, and Sb, might also change. In addition, sometimes a change in the high-diffusivity paths (grain boundary diffusion and lattice diffusion) by the heating treatment may cause the non-linear temperature dependence of the apparent diffusion coefficient.[38] Similar observations were made for Ag[38] and Cu-TiB₂[40] systems, in which the heat treatment leads to the structural change (for Ag[38]) or the composition change in the diffusion barriers (for TiB₂[40]), and the non-linear temperature dependence of the apparent diffusion coefficient was observed.

### 3.3.5 Summary

Based on preliminary studies of the contact resistance and thermal stability of Pd, W, Au single and multi-layer contacts, a low resistance Au/W/Pd/p-In₀.₂₅Ga₀.₇₅Sb ohmic contact was developed, and the metallurgical and electrical factors that influence the performance of this contact were examined. Palladium is employed for making intimate contact to the p-InGaSb, and W (which is predicted to be in thermodynamic equilibrium with InGaSb) is used as a diffusion barrier to protect the semiconductor from reaction
with a Au cap. The Au layer lowers the metal sheet resistance, which turns out to be a critical parameter for achieving a low contact resistance. The contact resistance of as-deposited Pd/W/Au (5/50/145 nm) contacts is 0.08 Ω mm (corresponding to a specific contact resistance of $2.8 \times 10^{-7}$ Ω cm$^2$), while Pd/W/Au (5/145/100 nm) contacts exhibit a contact resistance of 0.13 Ω mm after deposition. Further annealing of the Pd/W/Au (5/145/100 nm) contacts at 250 °C for 3 h in N$_2$ reduced the contact resistance to 0.08 Ω mm. Both contacts were deposited on a p-In$_{0.25}$Ga$_{0.75}$Sb layer with a semiconductor sheet resistance of approximately 300 Ω/√. The thermal stability of the Pd/W/Au contacts was also examined. The contacts exhibited much better thermal stability when aged in evacuated quartz tubes than when aged at 250 °C in N$_2$, and the contacts with the thickest W layer exhibited the best performance. The Pd/W/Au (5/145/100 nm) contacts exhibited no metallurgical or electrical degradation when aged at 250 °C in N$_2$ for 100 h, while they survived for 4 months at 250 °C in sealed quartz tubes. An activation energy of 1.3 eV was observed for the Pd/W/Au (5/50/145 nm) contacts.

3.4 Sulfur Passivation for Shallow Pd/W/Au Ohmic Contacts to p-InGaSb

In this section of the thesis, the relationship between the specific contact resistance of non-alloyed Pd/W/Au ohmic contacts to p-In$_{0.25}$Ga$_{0.75}$Sb and pre-metallization surface preparations is examined. The resistance of ohmic contacts is minimized when p-InGaSb is exposed briefly to a dilute (NH$_4$)$_2$S solution. This treatment minimizes the thickness of any residual oxide or sulfide layer on the semiconductor and
avoids excessive etching of the semiconductor, which would make the contact less shallow. A specific contact resistance of $5.9 \times 10^{-7} \Omega \text{ cm}^2$ is achieved for a Pd/W/Au (2/50/145 nm) contact that consumes no more than 5 nm of InGaSb.

### 3.4.1 Effect of the Surface Treatment on the Specific Contact Resistance of the Pd/W/Au Contacts

The measured specific contact resistances for the as-deposited Pd/W/Au contacts prepared using different surface treatments are listed in Table 3.4. The “conventional surface treatment” consisted of 16.5 % HCl for 30 s followed by 1 buffered oxide etch (BOE):1 DI H$_2$O for 30 s and rinsing in DI H$_2$O. When this treatment was performed with a final step of 30 s in 21 % (NH$_4$)$_2$S, it is called the “modified surface treatment”. Specific contact resistances of $3.8 \times 10^{-7}$ and $3.0 \times 10^{-7} \Omega \text{ cm}^2$ were obtained for the Pd/W/Au (5/50/145 nm) contacts with the conventional and modified surface treatment, respectively. On the other hand, when a thinner Pd layer was used, Pd/W/Au (2/50/145 nm) contacts prepared with the modified surface treatment showed a specific contact resistance of $2.0 \times 10^{-6} \Omega \text{ cm}^2$, higher than that of either Pd/W/Au (5/50/145 nm) contact but lower than the Pd/W/Au (2/50/145 nm) contact prepared using the conventional surface treatment ($7.6 \times 10^{-6} \Omega \text{ cm}^2$). The low specific contact resistance and minimal effect of the surface treatments for the contacts with 5 nm Pd indicates that 5 nm of Pd might be thick enough to diffuse through and disperse the native oxide on the semiconductor. On the Pd/W/Au (2/50/145 nm) contact, however, the surface treatment significantly influenced the specific contact resistance, indicating that 2 nm of Pd might
be inadequate to disperse the interfacial oxide and make intimate contact to p-InGaSb, at least without further improvement in the surface preparation. However, a contact with a 2 nm Pd layer might be attractive for an ultra-shallow contact. For this reason, a study of the surface preparation was undertaken.
Table 3.4: Comparison of the specific contact resistances for the as-deposited Pd/W/Au contacts with different surface treatments.

<table>
<thead>
<tr>
<th>Contacts</th>
<th>Surface treatment</th>
<th>Specific contact resistance (Ω cm²)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pd/W/Au (5/50/145 nm)</td>
<td>Conventional surface treatment (Average of nine samples)</td>
<td>(3.8 ± 0.9) x 10⁻⁷</td>
</tr>
<tr>
<td>Pd/W/Au (5/50/145 nm)</td>
<td>Modified surface treatment (Average of three samples)</td>
<td>(3.0 ± 0.9) x 10⁻⁷</td>
</tr>
<tr>
<td>Pd/W/Au (2/50/145 nm)</td>
<td>Conventional surface treatment (Average of five samples)</td>
<td>(7.6 ± 0.4) x 10⁻⁶</td>
</tr>
<tr>
<td>Pd/W/Au (2/50/145 nm)</td>
<td>Modified surface treatment (Average of three samples)</td>
<td>(2.0 ± 0.1) x 10⁻⁶</td>
</tr>
<tr>
<td>Pd/W/Au (2/50/145 nm)</td>
<td>Conventional surface treatment + 30 min in open air</td>
<td>(4.4 ± 5.1) x 10⁻⁵</td>
</tr>
<tr>
<td>Pd/W/Au (2/50/145 nm)</td>
<td>Modified surface treatment + 30 min in open air</td>
<td>(2.1 ± 0.1) x 10⁻⁶</td>
</tr>
<tr>
<td>Pd/W/Au (2/50/145 nm)</td>
<td>Ruthenium passivation (Average of three samples)</td>
<td>(3.0 ± 0.9) x 10⁻⁶</td>
</tr>
<tr>
<td>Pd/W/Au (2/50/145 nm)</td>
<td>IPA rinse (Average of four samples)</td>
<td>(2.9 ± 1.6) x 10⁻⁶</td>
</tr>
<tr>
<td>Pd/W/Au (2/50/145 nm)</td>
<td>Sulfide rinse (Average of eight samples)</td>
<td>(5.9 ± 2.3) x 10⁻⁷</td>
</tr>
</tbody>
</table>
Besides reducing the specific contact resistance of Pd/W/Au (2/50/145 nm) contacts, the modified surface treatment also made processing the contacts easier. In a separate experiment, contacts treated with the conventional and modified surface treatments were both stored in open air for 30 min before they were loaded into the deposition chamber. As listed in Table 3.4, a specific contact resistance of $4.4 \times 10^{-5}$ Ω cm$^2$ was observed on the Pd/W/Au (2/50/145 nm) contacts prepared using the conventional surface treatment and then left in air for 30 min, while the same contacts treated using the modified surface treatment followed by aging in open air for 30 min yielded a specific contact resistance of $2.1 \times 10^{-6}$ Ω cm$^2$. Comparing the fresh and aged contacts treated with the conventional surface treatment, an order of magnitude increase in the specific contact resistance strongly suggests that the native oxide continues to grow during the 30 min the sample is left in air, greatly influencing the specific contact resistance of the Pd/W/Au (2/50/145 nm) contacts. On the other hand, contacts to the fresh and aged surfaces prepared using the modified surface treatment showed a comparable specific contact resistance, even though the p-InGaSb surfaces was exposed to air for 30 min before they were loaded into the deposition chamber, verifying that the sulfur passivation can effectively inhibit the oxide growth.

Since these results were encouraging but not satisfactory, additional surface preparations were explored. Pd/W/Au (2/50/145 nm) contacts prepared using 16.5 % HCl for 30 s followed by (1:1) RuCl$_3$(0.05 M):HCl(0.1M) for 1 min at 40 °C (ruthenium passivation); 16.5 % HCl for 30 s followed by rinsing in 2-propanol (IPA rinse); and 16.5 % HCl for 30 s followed by a rinse in 2.1 % (NH$_4$)$_2$S for 1-2 s (sulfide rinse) were compared, as listed in Table 3.4. Specific contact resistances of $3.0 \times 10^{-6}$ and $2.9 \times 10^{-6}$
Ω cm\(^2\) were observed for the Pd/W/Au (2/50/145 nm) contacts with ruthenium passivation and the IPA rinse, respectively. On the other hand, a reduced specific contact resistance of \(5.9 \times 10^{-7} \ \Omega \text{cm}^2\) was achieved on the same contacts prepared using the sulfide rinse treatment. Interestingly, Pd/W/Au (2/50/145 nm) contacts prepared using the IPA rinse yielded a reduced specific contact resistance compared to the same contacts prepared using the conventional surface treatment (\(7.6 \times 10^{-6} \ \Omega \text{cm}^2\)), which is in good agreement with findings by Liu et al.\(^{[26]}\) that a rinse in IPA leads to a reduction in oxide thickness compared to rinsing in DI water. Even better than the IPA rinse, however, was the rinse in a dilute (NH\(_4\))\(_2\)S solution (2.1 %).

Cross-sectional TEM of Pd (50 nm)/p-InGaSb contacts annealed at 100 °C for 90 min prepared using the conventional surface treatment and the sulfide rinse treatment are shown in Fig 3.12 and Fig 3.13, respectively. Thick Pd contacts are shown first instead of Pd/W/Au contacts since we have found it more difficult to image thin residual oxide layers in Pd/W/Au contacts. From top to bottom, the layers are identified as Pd, an intermediate oxide layer, an amorphous Pd-In-Ga-Sb reaction layer, and InGaSb. The presence of the amorphous reaction layer indicates that the thick Pd layer can diffuse through the native oxide on p-InGaSb and react uniformly with the semiconductor. Furthermore, the 2-3 nm thick continuous oxide layer within the contacts prepared with the conventional surface treatment indicates that there is significant oxide on p-InGaSb prior to metallization when the conventional surface treatment is used. On the other hand, only a few patches were observed at the Pd/amorphous reaction layer interface in the contacts treated with HCl followed by a (NH\(_4\))\(_2\)S rinse, as shown in Fig 3.13. It is clear that the (NH\(_4\))\(_2\)S rinse greatly reduces the amount of oxide on the semiconductor. We
furthermore observed by TEM that the sulfide rinse treatment provides intimate contact between layers, as seen in the cross-sectional TEM image of the Pd/W/Au contact (Fig 3.14). On the other hand, the modified treatment leaves behind a residual sulfide layer. This layer is visible in Fig 3.15 above the amorphous Pd-In-Ga-Sb reaction layer and can be identified using EDS. The low contact resistance achieved after the sulfide rinse treatment is attributed to the minimization of the thickness of any residual layer – sulfide or oxide – on the InGaSb surface.

Fig 3.12: Cross-sectional TEM image of a Pd(50 nm)/p-InGaSb contact prepared with the conventional surface treatment and annealed at 100 °C for 90 min.
Fig 3.13: Cross-sectional TEM image of a Pd(50 nm)/p-InGaSb contact prepared using the sulfide rinse treatment. The sample was annealed at 100 °C for 90 min.

Fig 3.14: Cross-sectional TEM image of a Pd/W/Au (2/50/145 nm) contact prepared using the sulfide rinse treatment and annealing at 100 °C for 90 min.
3.4.2 Etch Rate of (NH₄)₂S Solutions on p-InGaSb: Atomic Force Microscopy

To minimize the consumption of InGaSb, not only should reaction between the metal and semiconductor be minimized, but the etching of p-InGaSb by the pre-metallization surface preparation should be also taken into consideration. In order to ensure minimal consumption of the p-InGaSb due to the surface treatments, the etch depth of HCl and (NH₄)₂S solutions on p-InGaSb were studied at room temperature. No measurable etch step was found on the p-InGaSb surfaces treated with 18.3 % HCl for 30 min, but a step was observed on the surfaces treated with (NH₄)₂S solutions, as shown in Fig 3.16, a measured 4.0 nm etch step by 0.84 (NH₄)₂S solution for 15 min. Fig 3.17 (a) and (b) show the measured etch depth as a function of etching time, where the etching rate on p-InGaSb increases with the concentration of the (NH₄)₂S solution. Uniform etch rates were obtained for the 42, 21 and 14 % (NH₄)₂S solution, but the etch rates of the 2.1

Fig 3.15: Cross-sectional TEM image of a Pd/W/Au (2/50/145 nm) contact prepared with the modified surface treatment and annealing at 100 °C for 90 min.
% and 0.84 % (NH₄)₂S solutions appeared to gradually slow, and finally no further etching was observed after 30 min in 0.84 % (NH₄)₂S. The non-uniformity of the etch rate implies the occurrence of competing dissolution and sulfidation reactions on the surface.[41] When the concentrated solution is used, the dissolution process dominates, leading to a linear relationship between etching depth and etching time. On the other hand, when a more dilute solution is used, the etching first gradually slows and eventually stops, since the sulfide layer that forms protects the InGaSb from further etching.
Fig 3.16: AFM analysis of etch step on p-InGaSb by 0.84 % (NH₄)₂S solution for 15 min.
In summary, we found that minimization of any dielectric layer thickness before metal deposition is a key to reducing the specific contact resistance of Pd/W/Au.
(2/50/145 nm) samples. A surface treatment combining 16.5 % HCl for 30 s to remove oxides followed by a rinse in 2.1 % (NH₄)₂S for 1-2 s is effective for achieving a low specific contact resistance. The specific contact resistance was reduced from $7.6 \times 10^{-6}$ Ω cm² for the conventional surface treatment to $5.9 \times 10^{-7}$ Ω cm² for the surface treatment with the sulfide rinse.

### 3.5 Shallow and Thermally Stable Pt/W/Au Ohmic Contact to p-Type InGaSb

In the previous section, an as-deposited Pd/W/Au (2/50/145 nm) contact prepared using the (NH₄)₂S rinse treatment with a specific contact resistance of $5.9 \times 10^{-7}$ Ω cm² was developed. The reduction of the specific contact resistance for the samples prepared with the (NH₄)₂S rinse was associated with the minimization of the interfacial dielectric layer. This suggests that intimate metal/p-InGaSb contacts could be prepared using the (NH₄)₂S rinse treatment. In this work, the specific contact resistances of metal/W/Au (2/50/145 nm) contacts prepared using the conventional pre-metallization treatment are compared to samples prepared using the (NH₄)₂S rinse, and the effect of the surface preparation on Fermi level pinning at the metal/semiconductor interface is examined. Cross-sectional transmission electron microscopy (TEM) is employed to examine the shallowness of the contacts before and after aging.
3.5.1 Surface States of the Sulfur Passivated p-InGaSb Surfaces

The effect of the pre-metallization surface treatment on the specific contact resistance of the as-deposited metal/W/Au contacts was first investigated. Contacts with two nanometers of Pt, Ni, Pd, Co, Ti, or no first layer with an additional 50 nm of W and a 100 nm of Au cap were prepared using the conventional surface treatment, and the specific contact resistances are shown in Fig. 3.18. Similar contacts with 2 nm of Pt, Pd, Co, Cu, Cr, Ag, and no first layer beneath 50 nm W and 100 nm Au were prepared using the (NH₄)₂S rinse treatment, as shown in Fig. 3.19. The average specific contact resistances with the standard deviations for the contacts prepared using the (NH₄)₂S rinse treatment are listed in Table 3.5. Higher specific contact resistances were observed on the contacts prepared using the conventional surface treatment compared to those prepared with the (NH₄)₂S rinse treatment. For the contacts prepared using the conventional surface treatment, no relationship between the specific contact resistance and the metal work function of the first metal layer could be found. However, the specific contact resistance decreases with the work function of the first layer for contacts prepared using the (NH₄)₂S rinse treatment.
Fig 3.18: Average specific contact resistance as a function of the work function of the first contacting metal in metal/W/Au (2/50/145 nm) contacts prepared using the conventional surface treatment.

Fig 3.19: Average specific contact resistance as a function of the work function of the first contacting metal in metal/W/Au (2/50/145 nm) contacts prepared using the (NH₄)₂S rinse treatment.
Table 3.5: Average specific contact resistances of the metal/W/Au (2/50/145 nm) contacts.

<table>
<thead>
<tr>
<th>Contacts</th>
<th>( \rho_C (\Omega \text{ cm}^2) ) as deposited</th>
<th>( \Phi_B ) (eV) as deposited</th>
<th>( \rho_C (\Omega \text{ cm}^2) ) aged for 1 day at 250 °C</th>
<th>( \rho_C (\Omega \text{ cm}^2) ) aged for 2 days at 250 °C</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pt/W/Au</td>
<td>((4 \pm 1) \times 10^{-6})</td>
<td>0.19</td>
<td>((4 \pm 2) \times 10^{-6})</td>
<td>((4 \pm 2) \times 10^{-6})</td>
</tr>
<tr>
<td>Pd/W/Au</td>
<td>((6 \pm 2) \times 10^{-7})</td>
<td>0.13</td>
<td>((2 \pm 1) \times 10^{-6})</td>
<td>((2 \pm 1) \times 10^{-6})</td>
</tr>
<tr>
<td>Co/W/Au</td>
<td>((5 \pm 3) \times 10^{-6})</td>
<td>0.20</td>
<td>((5+6/-5) \times 10^{-6})</td>
<td>((7 \pm 7) \times 10^{-6})</td>
</tr>
<tr>
<td>Cu/W/Au</td>
<td>((2+3/-2) \times 10^{-5})</td>
<td>0.23</td>
<td>((9 \pm 5) \times 10^{-5})</td>
<td>((1 \pm 1) \times 10^{-4})</td>
</tr>
<tr>
<td>W/Au (50/145 nm)</td>
<td>((3 \pm 1) \times 10^{-5})</td>
<td>0.25</td>
<td>((3 \pm 1) \times 10^{-5})</td>
<td>((4 \pm 1) \times 10^{-5})</td>
</tr>
<tr>
<td>Cr/W/Au</td>
<td>((2 \pm 1) \times 10^{-5})</td>
<td>0.24</td>
<td>((1 \pm 1) \times 10^{-5})</td>
<td>((1+2/-1) \times 10^{-5})</td>
</tr>
<tr>
<td>Ag/W/Au</td>
<td>((6 \pm 6) \times 10^{-5})</td>
<td>0.26</td>
<td>((8+10/-8) \times 10^{-6})</td>
<td>((9+10/-9) \times 10^{-6})</td>
</tr>
</tbody>
</table>
The Schottky barrier heights of the contacts were also estimated from the specific contact resistances. Since $E_0 \sim kT$ at a temperature of 300 K and a doping concentration of $1.3 \times 10^{18}$ cm$^{-3}$, the thermionic field emission model was employed for the estimates[12], where $k$ is the Boltzmann’s constant, $T$ is the absolute temperature, and

$$E_{00} = \frac{hq}{4\pi} \left( \frac{N_A}{m^* \varepsilon_s} \right)^{1/2}.$$  \hspace{1cm} \text{Eq 3.22}

The parameters of the effective mass ($m^*$) and the permittivity of the semiconductor ($\varepsilon_s$) were adopted from the literature,[42] and $h$, $q$, and $N_A$ are Planck’s constant, the electronic charge, and the acceptor concentration, respectively. In addition, the specific contact resistance ($\rho_C$) can be expressed as a function of the barrier height ($\Phi_B$):[12]

$$\rho_C = \frac{k^2 \cosh(E_{00}/kT)}{qA^* \left[ \pi(q\Phi_B + q\xi)E_{00} \right]^{1/2} \left[ \coth(E_{00}/kT) \right]^{1/2} \times \exp \left\{ [q(\Phi_B - \xi)/E_0] + q\xi/kT \right\}},$$  \hspace{1cm} \text{Eq 3.23}

where

$$E_0 = E_{00} \coth(E_{00}/kT).$$  \hspace{1cm} \text{Eq 3.24}

$A^*$ is the Richardson’s constant, and $\xi$ is the energy difference between the Fermi level and the valence band for p-type semiconductors ($E_F-E_V$), which can be calculated using the Fermi-Dirac integral.[11] By using Eq 3.22 - Eq 3.24, the barrier heights can be extracted from the specific contact resistance for a moderately doped semiconductor.

The estimated barrier heights for the as-deposited metal/W/Au (2/50/145 nm) contacts with the (NH$_4$)$_2$S rinse treatment are listed in Table 3.5. Low values are observed for the contacts with high metal work functions (0.13 eV for the as-deposited Pd/W/Au...
contacts and 0.19 eV for the as-deposited Pt/W/Au contacts), and the opposite is found for low work function metals (0.26 eV for the as-deposited Ag/W/Au contacts and 0.24 eV for the as-deposited Cr/W/Au contacts). In addition, except for the Pd/W/Au contact, we observed a linear relationship between the barrier height ($\Phi_B$) and metal work function ($\Phi_m$) of the first contacting layer given by

$$\Phi_B = 0.48 - 0.05\Phi_m.$$  \hspace{1cm} \text{Eq 3.25}

The linear relationship, with a slope of 0.05, demonstrates that the barrier height is weakly dependent on the metal work function of the first contacting layer (Fig 3.20). For the Pd/W/Au contacts, the source for the anomalously low barrier height might be due to reaction between Pd and InGaSb, which occurs readily at 100 °C (see Fig 3.21) and may occur even at room temperature.

When the conventional pre-metallization surface treatment was used, no clear relationship between the specific contact resistance and the metal work function was found, as shown in Fig 3.18. This finding could be associated with the observation of a continuous dielectric layer at the Pd/p-InGaSb interface when using the conventional surface treatment (Section 3.4.1), which could lead to a high interface state density. On the other hand, a dependence of the specific contact resistance or barrier height on the metal work function for the contacts prepared using the (NH$_4$)$_2$S rinse treatment could be associated with the modification of the p-InGaSb surface and the absence of a dielectric layer after using the (NH$_4$)$_2$S rinse pre-metallization treatment, which could reduce the surface state density on p-InGaSb. In fact, Miyamura et al. suggested that the chalcogen atoms absorbed on Ga-terminated GaAs surfaces provide a significant reduction in
surface state density.\textsuperscript{[43]} A reduced surface state density could cause the surface Fermi level position to be partially pinned.

Aging of the metal/W/Au (2/50/145 nm) contacts was also performed at 250 °C in evacuated quartz tubes. The specific contact resistances of the Pt/W/Au, Co/W/Au, W/Au, and Cr/W/Au contacts remained the same within experimental error following 1 day at 250 °C. Conversely, degradation in the specific contact resistance was observed for the Pd/W/Au, Cu/W/Au, and Ag/W/Au contacts aged at 250 °C for 1 day in evacuated quartz tubes, as listed in Table 3.5. This is inconsistent with our previous finding that no degradation in the specific contact resistance was found before the failure of the diffusion barrier W for the Pd/W/Au (5/50/145 nm) contacts (Section 3.3.4). This difference could be due to the use of a 2 nm rather than 5 nm Pd layer. In addition, degradation in the surface morphology was observed after aging all the contacts that are

![Graph showing Schottky barrier height as a function of the work function of the first contacting metal in metal/W/Au (2/50/145 nm) contacts (neglecting Pd/W/Au).]

\textbf{Fig 3.20:} Schottky barrier height as a function of the work function of the first contacting metal in metal/W/Au (2/50/145 nm) contacts (neglecting Pd/W/Au).
listed in Table 3.5 at 250 °C for 4 days in evacuated quartz tubes, which indicates failure of the W barrier. (Section 3.3.4)

3.5.2 Shallowness of the Pt/W/Au Contacts

Cross-sectional TEM was next performed to examine the shallowness of the contacts and the changes they undergo upon aging. Fig 3.21 shows the cross-sectional TEM image of a Pd/W/Au (2/50/145 nm) contact annealed at 100 °C for 90 min in air and sectioned prior to aging. Gold, W, InGaSb and AlSb buffer layers are observed from top to bottom, and a uniform metal/p-InGaSb interface is observed. Because the reaction layer is very thin, it is difficult to distinguish it from the metal layers above it. To measure the consumption of the InGaSb epilayers, the thickness of the InGaSb epilayer with and without contact metallizations was compared. Thickness measurements were performed on images at the same magnification, and twenty measurements were taken for each image, with equal spacing between each measurement, to ensure good statistical results. In addition, the maximum InGaSb thickness, minimum InGaSb thickness, average InGaSb thickness, and the consumption of the InGaSb with standard deviations were recorded and listed in Table 3.6 to provide information on the uniformity of the interfacial reactions. Compared to the thickness of the InGaSb without metallization (blank), the Pd/W/Au (2/50/145 nm) contacts annealed for 100 °C for 90 min consumed an average of 4.6 nm of InGaSb with a standard deviation of 1.3 nm, suggesting that the interfacial reaction is uniform with a 4 nm difference between the maximum and minimum InGaSb thickness. However, a non-uniform interfacial reaction with the
formation of isolated grains was observed after the Pd/W/Au (2/50/145 nm) contact was aged at 250 °C for 1, 2, and 3 days in evacuated quartz tubes. These isolated grains were determined to consist of Pd, In, Ga, and Sb using energy dispersive x-ray spectroscopy and are shown clearly in Fig 3.22. An average consumption of 9.0 nm of InGaSb with a standard deviation of 8.5 nm was measured, and the difference between the minimum and maximum InGaSb thickness is 22.4 nm for 1 day of aging. The formation of isolated, hemispherical grains at the interface could be associated with a reduction in interfacial free energy. Consistently, more moderate interface roughening and void formation were also observed for the Pd/W/Au (5/50/145 nm) contacts aged at 250 °C for 1 h (Fig 3.23) and 1 day (Fig 3.24), respectively. The void formation may occur as a result of a large disparity between diffusion rates of the Pd and the elements from the semiconductor. We previously reported that no change was found in the specific contact resistance or the Auger depth profiles of the Pd/W/Au (5/50/145 nm) contacts before and after aging. (Section 3.3.4) Due to the fact that Auger analysis was used and relies on the detection of signals from an averaged area, and due to the possibility of interface roughening during sputtering, the interfacial reactions less than 5 nm were not readily observed in the Auger depth profiles.
Fig 3.21: Cross-sectional TEM image of a Pd/W/Au (2/50/145 nm) contact annealed at 100 °C for 90 min.

Fig 3.22: Cross-sectional TEM image of a Pd/W/Au (2/50/145 nm) contact aged at 250 °C for 1 day in an evacuated quartz tube.
Fig 3.23: Cross-sectional TEM image of a Pd/W/Au (5/50/145 nm) contact aged at 250 °C for 1 h in an evacuated quartz tube.

Fig 3.24: Cross-sectional TEM image of a Pd/W/Au (5/50/145 nm) contact aged at 250 °C for 1 day in an evacuated quartz tube.
Table 3.6: Thickness measurements (in nm) for InGaSb beneath the metal/W/Au contacts.

<table>
<thead>
<tr>
<th>Contact</th>
<th>Aging condition</th>
<th>Min/Max InGaSb Thickness</th>
<th>Average Thickness</th>
<th>Consumption of InGaSb</th>
</tr>
</thead>
<tbody>
<tr>
<td>Blank</td>
<td>100 °C/90 min</td>
<td>40.8/43.7</td>
<td>42.8 ± 0.9</td>
<td>0.0</td>
</tr>
<tr>
<td>Pd/W/Au (2/50/145 nm)</td>
<td>100 °C/90 min</td>
<td>36.4/40.8</td>
<td>38.2 ± 1.0</td>
<td>4.6 ± 1.3</td>
</tr>
<tr>
<td>Pd/W/Au (2/50/145 nm)</td>
<td>250 °C/1 day evacuated quartz tube</td>
<td>21.8/44.2</td>
<td>33.8 ± 8.4</td>
<td>9.0 ± 8.5</td>
</tr>
<tr>
<td>Pd/W/Au (5/50/145 nm)</td>
<td>100 °C/90 min</td>
<td>34.7/37.0</td>
<td>36.0 ± 0.6</td>
<td>6.8 ± 1.1</td>
</tr>
<tr>
<td>Pd/W/Au (5/50/145 nm)</td>
<td>250 °C/1 h evacuated quartz tube</td>
<td>31.1/41.6</td>
<td>35.9 ± 2.9</td>
<td>6.9 ± 3.0</td>
</tr>
<tr>
<td>Pd/W/Au (5/50/145 nm)</td>
<td>250 °C/1 day evacuated quartz tube</td>
<td>21.0/39.7</td>
<td>32.8 ± 6.4</td>
<td>10.0 ± 6.4</td>
</tr>
<tr>
<td>Pt/W/Au (2/50/145 nm)</td>
<td>250 °C/1 day evacuated quartz tube</td>
<td>36.7/40.5</td>
<td>38.7 ± 1.2</td>
<td>4.1 ± 1.5</td>
</tr>
<tr>
<td>Pt/W/Au (2/50/145 nm)</td>
<td>250 °C/3 days evacuated quartz tube</td>
<td>32.08/42.59</td>
<td>36.9 ± 2.9</td>
<td>5.9 ± 1.6</td>
</tr>
</tbody>
</table>
Similar TEM experiments were performed on the Pt/W/Au (2/50/145 nm) contacts. The Pt/W/Au (2/50/145 nm) aged at 250 °C for 1 day showed a uniform metal/p-InGaSb interface, and 4.1 nm of InGaSb was consumed. Little change was observed after the Pt/W/Au (2/50/145 nm) contacts were aged at 250 °C for 3 days, as shown in Fig 3.25. Consumption of only 5.9 nm of InGaSb was measured with a uniform reaction across the image (a standard deviation of 1.6 nm), indicating that the Pt/W/Au (2/50/145 nm) contacts remain shallow and thermally stable for 3 days at 250 °C in evacuated quartz tubes.

![Cross-sectional TEM image of a Pt/W/Au (2/50/145 nm) contact aged at 250 °C for 3 days in an evacuated quartz tube.](image)

Fig 3.25: Cross-sectional TEM image of a Pt/W/Au (2/50/145 nm) contact aged at 250 °C for 3 days in an evacuated quartz tube.

The as-deposited Pd/W/Au (2/50/145 nm) contacts exhibit extremely low resistance, which could enhance device performance. However, degradation in the specific contact resistance and an irregular reaction morphology at the interface after aging at 250 °C for 1 day were observed. Since shallow, thermally stable ohmic contacts are required for packaging and long-term operation, metals that have a slow reaction rate
with InGaSb are often favored. Hence, the Pt/W/Au contacts, which yielded a specific contact resistance of $4 \times 10^{-6} \ \Omega \ \text{cm}^2$ for the as-deposited condition, is interesting from the point of view of improved thermal stability. Uniform and shallow interfacial reactions were observed for the Pt/W/Au contacts aged at 250 °C for 3 days in evacuated quartz tubes, and no degradation in the specific contact resistance was observed after aging.

### 3.5.3 Summary

The development of a shallow, thermally stable ohmic contact to p-InGaSb is described in this chapter. The Fermi level position at the p-InGaSb surface is found to be only partially pinned after the (NH$_4$)$_2$S rinse treatment, which is linked to the sulfur passivation and absence of a dielectric layer at the interface. As-deposited Pt/W/Au (2/50/145 nm) contacts yield a specific contact resistance of $4 \times 10^{-6} \ \Omega \ \text{cm}^2$. Cross-sectional TEM verified that this contact remains shallow with a consumption of only 5.9 nm of InGaSb after the contact was aged at 250 °C for 3 days in an evacuated quartz tube. No degradation of the specific contact resistance was observed after aging at 250 °C for 3 days.
Chapter 4

GATE METALLIZATIONS ON SB-BASED HEMTS

Chapter 4 describes the design of thermally stable gate metallizations on Sb-based HEMTs. A high electron mobility transistor (HEMT) heterostructure of InAs(5 nm)/Al_{0.80}Ga_{0.20}As_{0.16}Sb_{0.84}(40 nm)/(n-)InAs(50 nm)/(n+)InAs(1 µm) was used in this study. Gate metallizations were prepared on the heterostructures both with and without the 5 nm InAs cap layer, and metallization candidates that are in thermodynamics equilibrium with InAs or AlSb were selected along with other metallizations in a study of the thermal stability. Aging of the gate metallizations was performed, and current-voltage (I-V) characteristics, XPS depth profiles, and cross-sectional TEM were compared.

4.1 Literature Review

AlSb/InAs based heterostructures are currently attractive for high speed and low power applications, and the initial development of AlSb/InAs based heterostructures has been reported.\cite{44,45} A comparison of I-V characteristics on heterostructures with different barrier layers demonstrated that the barrier layers greatly influence the current transport mechanism. The additional of Ga to the barrier layer leads to an increase in the current flowing across the barrier and improves its stability\cite{44}, whereas the addition of As or Al causes a decrease in the current transport across the barrier, which can be explained by the valence band position of the barrier layer.\cite{44,45} In addition,
modifications to the surface capping layer greatly affects the surface Fermi level pinning position. A higher leakage current was observed for diodes with an InAs cap compared to diodes with a GaSb cap.[46],[47] Hence, in our study, gate metallizations on both AlGaAsSb barriers with and without an InAs cap layer will be investigated. Citric acid[48], H₃PO₄[45], and acetic acid[49] solutions that were reported for etching InAs were evaluated in this thesis for InAs cap removal.

The effect of the gate metallizations on the leakage current was demonstrated by Bolognesi et al.[50] A reduced leakage current for the as-deposited Al gate metallizations was observed compared to Ti/Au gate metallizations. Similarly, Boos et al.[51] observed a higher leakage current for a diode with Cr/Au compared to TiW/Au (17.5/100nm) gate metallizations before heat treatment. TiW/Au metallizations showed good thermal stability from 90 °C to 300 °C for annealing durations of 1 hour. By contrast, an increase in current of one order of magnitude for Cr/Au diodes at -0.2 V was observed after aging at 150 °C. The change in the leakage current for diodes with different gate metallizations and heat treatments indicates that metal/semiconductor reactions might be the source of the degradation in the leakage current with aging.

To design a thermally stable gate metallization, thermodynamics can be used to predict metals that are not reactive on Al₀.₈₀Ga₀.₂₀As₀.₁₆Sb₀.₈₄ or InAs. However, except for tungsten[52], no elemental metal was reported to be in equilibrium with AlSb. Hence, some bimetallic contacts that are in equilibrium with AlSb might be good candidates for making thermally stable contact to Al₀.₈₀Ga₀.₂₀As₀.₁₆Sb₀.₈₄. For instance, Fig 3.1 shows a calculated Al-Co-Sb ternary phase diagram at 300 K using the Terquat program.[53] A tie-line between CoAl and AlSb indicates that CoAl is in equilibrium
with AlSb. The metallic CoAl phase also has a high melting temperature\cite{54}, and consequently it could be a good candidate for a gate metallization on AlGaAsSb. Similarly, for the metal-In-As system, Swenson\cite{55} suggested that W, Re, Os, RhIn$_3$, PdIn and PtIn$_2$ are candidates for stable contacts on InAs. In addition, other common metallizations with high conductivity, such as CoSi$_2$\cite{56}, might be employed for making thermally stable gate metallizations, since CoSi$_2$ is predicted to be stable on InAs\cite{52}.

![Phase diagram](image)

Fig 4.1: Isothermal section of the calculated Al-Co-Sb phase diagram at 300 K.

### 3.2 Preliminary Study of InAs Cap Removal

Preliminary experiments were carried out on a heterostructure of InAs/Al$_{0.80}$Ga$_{0.20}$As$_{0.16}$Sb$_{0.84}/$(n$^+$)InAs/buffer and GaAs substrate, as shown in Fig 3.2. The InAs cap was grown to protect AlGaAsSb barrier from oxidation, and an AlGaAsSb barrier was grown on top of a heavily doped InAs layer to create a 2-DEG in the InAs
channel. Effort was first focused on the selective wet etching of InAs cap off the AlGaAsSb by I-V characteristics, AFM, and XPS.

<table>
<thead>
<tr>
<th>InAs (5 nm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Al_{0.86}Ga_{0.26}As_{0.16}Sb_{0.84} (10 nm)</td>
</tr>
<tr>
<td>InAs (n+) (1 µm)</td>
</tr>
<tr>
<td>GaAs (n+) buffer and substrate</td>
</tr>
</tbody>
</table>

Fig 4.2: HEMT epitaxial layers with a 10 nm AlGaAsSb barrier layer.

### 4.2.1 Results from I-V Measurements

Aluminum contacts were deposited on the heterostructures that were etched using acetic acid:H₂O₂:H₂O (5:1:5) or citric acid:H₂O₂ (1:1) for the InAs cap removal. Preliminary results showed better Al film adhesion on the acetic acid etched surfaces, compared to the adhesion of the Al film on surfaces etched with the citric acid based solution. In addition, irreproducibility in I-V curves was observed when 351 developer was used for photolithography (Fig 3.6) Hence, future experiments were performed by using a shadow mask to fabricate Schottky dots with radius of 50 µm on a modified structure, as shown in Fig 3.4. The thickness of the AlGaAsSb barrier was increased to 40 nm thick, and a lightly doped InAs channel was used for subsequent Schottky barrier study.
Atomic Force Microscopy

AFM was performed to measure the etch step created using citric acid, acetic acid, and phosphorus acid based solutions. A rough surface with a RMS roughness of 23.2 nm was observed on the surfaces etched with citric acid:H₂O₂ (1:1) solution for 20 sec. Further soaking in acetone, methanol for 30 min each and rinsing in DI water resulted in a significant reduced RMS roughness of 3.1 nm. This suggests that the citric acid solution produced a large amount of residue on the surface, and a long degrease
cleaning step is required, i.e., acetone and methanol. The large amount of residue on the sample surface causes poor adhesion of the Al film. Therefore, further investigation of the removal of the InAs layer was focused on other etchants.

Fig. 4.5 shows the 100 µm topographic images for samples etched with H₃PO₄:H₂O₂:H₂O (1:2:40) for 20 sec, 1 min, and 5 min with scales of 500 nm, 500 nm, and 2000 nm, respectively. The average section analysis across the steps shows that step heights are 50.2 nm (etched for 20 sec), 232.5 nm (etched for 1 min), and 998.3 nm (etched for 5 min), as shown in Table 3.1. An estimation of etching rate of 199.1 nm/min (approximately equal to 3.3 nm/s) is extracted from the linear fit to the etching depth as a function of etching time, as shown in Fig. 3.5.
Fig 4.5: AFM topography image of etched steps by $\text{H}_3\text{PO}_4:\text{H}_2\text{O}_2:\text{H}_2\text{O}$ (1:2:40) for (a) 20 sec, (b) 1 min, and (c) 5 min with scales of 500 nm, 500 nm, and 2000 nm, respectively, 100 µm scan.
Similarly, 351 developer and acetic acid based solution were also tested in order to see its effect on the epilayers. As listed in Table 3.1, a step height of 155 nm was observed after etching in 351 developer for 100 min, and that of the samples treated with

<table>
<thead>
<tr>
<th>Etchant</th>
<th>Etching time</th>
<th>Height (nm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>H$_3$PO$_4$:H$_2$O$_2$:H$_2$O (1:2:40)</td>
<td>20 sec</td>
<td>50.2</td>
</tr>
<tr>
<td></td>
<td>1 min</td>
<td>232.5</td>
</tr>
<tr>
<td></td>
<td>5 min</td>
<td>998.3</td>
</tr>
<tr>
<td>351 developer</td>
<td>100 min</td>
<td>155.0</td>
</tr>
<tr>
<td>Acetic acid:H$_2$O$_2$:H$_2$O (5:1:5)</td>
<td>10 sec</td>
<td>5.0</td>
</tr>
<tr>
<td></td>
<td>45 sec</td>
<td>12.5</td>
</tr>
</tbody>
</table>

Fig 4.6: Step height as a function of etching time for H$_3$PO$_4$:H$_2$O$_2$:H$_2$O (1:2:40) solution.

Similarly, 351 developer and acetic acid based solution were also tested in order to see its effect on the epilayers. As listed in Table 3.1, a step height of 155 nm was observed after etching in 351 developer for 100 min, and that of the samples treated with
acetic acid based solution for 10 and 45 sec were approximately 5.0 nm and 12.5 nm, respectively.

In summary, the etching of the heterostructures using citric acid, acetic acid, phosphorus acid, and 351 developer were compared. Citric acid was observed to leave a stubborn residue on the surface, and a DI rinse can not remove the residue, which makes the processing difficult. A solution that yields a fast etch rate, phosphorus acid, is not recommended for selective InAs cap removal without etching AlGaAsSb. In addition, 351 developer for the photolithography is found to etch the heterostructures, so that photolithography using this solution can not be used. Acetic acid was the most promising candidate to employ in this study. It does not leave a residue on surface, and yielded a moderate etch rate.

4.2.3 X-ray Photoelectron Spectroscopy

Acetic acid:H\textsubscript{2}O\textsubscript{2}:H\textsubscript{2}O (5:1:5) solution was investigated by XPS for InAs cap removal for the gate metallization study on the AlGaAsSb layer. Fig 3.7 shows surveys on sample surface without treatment, and surfaces treated with acetic acid based solutions for 10, 20, 30, and 45 sec, for which the etch depths were measured by AFM from 5 nm (10 s) to 12 nm (45 s etch). Fig 3.7 (a) shows that the elements In, As, O, and C were observed on the surface without acetic acid treatment, which indicates the InAs capping layer is at the surface. On the other hand, on the surfaces etched for 10, 20, 30, and 45 sec, similar XPS spectra were observed with elements of Al, Ga, As, Sb, O, and C, as shown in Fig 3.7 (b). Indium was not detected on the four surfaces, which suggests that
AlGaAsSb surfaces were exposed, and the InAs channel layers underneath AlGaAsSb barrier were not detected. XPS results revealed that the InAs cap can be removed by acetic acid:H₂O₂:H₂O (5:1:5) solution treated for 10 sec without extensive etching of the AlGaAsSb.

Fig 4.7: XPS spectrums of sample surface (a) without treatment, (b) treated with acetic acid:H₂O₂:H₂O (5:1:5) for 10, 20, 30, and 45 sec.
4.2.4 Summary

Acetic acid:H₂O₂:H₂O (5:1:5), citric acid:H₂O₂ (1:1), 351 developer, and H₃PO₄:H₂O₂:H₂O (1:2:40) were investigated for InAs cap removal. Poor adhesion of Al films on the surfaces treated with citric acid based solution was first observed during contact fabrication. This can be linked to the results from AFM, where a large amount of residue was observed on the surfaces treated with the citric acid based solution. On the other hand, Al films on surfaces treated with acetic acid exhibited good adhesion. It was also found that Schottky diodes fabricated with a shadow mask with and without 351 developer treatment showed a significant increase of the current for samples exposed to 351 developer for 45 sec, as shown in Fig 3.6, which can be explained by the etching of the heterostructures by the 351 developer. Therefore, this resist/developer combination can not be used. A phosphorus acid based solution was also investigated with an estimated etch rate of 199 nm/min, which is in good agreement with prior work by Cai et al.[57], although the composition of the barrier layer is different. The etch rate of phosphorus acid based solution appears to be too fast to be used in nanoscale work since the InAs capping layer is only 5 nm thick, and the removal of AlGaAsSb is undesirable. Therefore, a good choice for InAs cap removal is the acetic acid solution. Both XPS and AFM results suggested that the 5 nm InAs cap was removed after surface treatment with the acetic acid solution for 10 sec. Hence, all the I-V characteristic measurements in this study were performed on the contacts fabricated with a shadow mask, and surface treatments of 10 sec in an acetic acid solution were used to remove the cap InAs layer whenever removal of the cap was desired.
4.3 Experimental Procedure

Samples were cleaved into 5 × 5 mm pieces followed by degreasing in acetone, methanol, and DI water for 5 min each. Large area Pd/Pt/Au (15/25/60 nm) ohmic contacts were first deposited by e-beam deposition with a deposition rate of approximate 1-2 Å/sec and annealed at 250 °C for 30 min in N₂. Next, samples were treated in acetic acid solution for 10 sec for InAs cap removal when cap removal was desired. A shadow mask with contacts with a radius of 50 µm was used for Schottky dot fabrication. I-V characteristics were measured on a four probe station, and current density was extracted for making comparisons to the work of others. Thermal stability of various gate metallizations on AlGaAsSb with and without the InAs cap were tested and compared. The temperature 250 °C was chosen to satisfy temperature requirements for packaging, and to accelerate aging to learn about long-term stability. Ultra high purity Ar, an inert gas, was employed as an annealing ambient and was passed through a high capacity gas purifier with a flow rate of 100 sccm.

4.4 Thermal Stability of Gate Metallizations on AlGaAsSb with InAs Cap Removed

Various gate metallizations were tested on AlGaAsSb with the InAs cap removed. Thermal stability of the gate metallizations were compared in terms of the I-V characteristics and XPS depth profiles.
4.4.1 Thermal Stability of Gate Metallizations on AlGaAsSb by I-V Measurement

The selected gate metallizations on AlGaAsSb (without InAs cap) are listed in Table 4.2. The I-V characteristics of the gate metallizations aged at 250 °C in UHP Ar were compared, as shown in Fig 3.8 (a)-(i). A dc magnetron sputtering system was used for W/Au gate metallizations, and e-beam deposition was used for the other gate metallizations. For the as-deposited condition, high leakage currents and symmetric I-V characteristics were observed for the Al/Co/Al/Co/Al/Co, Co/Al/Co/Al/Co/Al, Ti/Au, W/Au (100/100 nm), Co/Si/Co/Si/Co, and Co/Si/Co/Si/Co/Au gate metallizations. On the other hand, low leakage currents and asymmetric I-V characteristics were observed for the Ti/Pt/Au (5/50/100 nm), Ti/Pt/Au (50/50/100 nm) and W/Au (30/100 nm) gate metallizations. For the Ti/Pt/Au (5/50/100 nm) and Ti/Pt/Au (50/50/100 nm) gate metallizations, the current at +0.2 V is lower than that at -0.2 V. Conversely, comparing the current at -0.2 V, higher current was observed at +0.2 V on the W/Au (30/100 nm) gate metallizations.
Table 4.2: List of gate metallizations on AlGaAsSb.

<table>
<thead>
<tr>
<th>Metallizations</th>
<th>Thickness (nm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Al/Co/Al/Co/Al/Co</td>
<td>(20/13.3/20.1/13.3/20/13.3)</td>
</tr>
<tr>
<td>Co/Al/Co/Al/Co/Al</td>
<td>(13.3/20/13.3/20.1/13.3/20)</td>
</tr>
<tr>
<td>Ti/Au</td>
<td>(10/290)</td>
</tr>
<tr>
<td>Ti/Pt/Au</td>
<td>(5/50/100)</td>
</tr>
<tr>
<td>Ti/Pt/Au</td>
<td>(50/50/100)</td>
</tr>
<tr>
<td>W/Au</td>
<td>(30/100)</td>
</tr>
<tr>
<td>W/Au</td>
<td>(100/100)</td>
</tr>
<tr>
<td>Co/Si/Co/Si/Co</td>
<td>(5/28.5/5/50/11.5)</td>
</tr>
<tr>
<td>Co/Si/Co/Si/Co/Au</td>
<td>(5/28.5/5/50/11.5/100)</td>
</tr>
</tbody>
</table>
Fig 4.8: I-V characteristics of gate metallizations aged at 250 °C in UHP Ar.
For the aging study, the surface morphology of all the gate metallizations remained the same after aging. Co/Al-based metallizations showed no notable increase in the current at -0.2V after 20 days aging. However, the as-deposited Co/Al gate metallization yielded an already high reverse bias current, leading to poor device performance for Co/Al. Hence, W/Au is the most promising gate metallization tested for AlGaAsSb, and is stable at 250 °C for 3 hours in UHP Ar. The current at -0.2 V degraded and gradually increased after aging from 4 hours to 10 hours. Poorer thermal stability was

Fig 4.8: I-V characteristics of gate metallizations aged at 250 °C in UHP Ar.
observed for all other gate metallizations, where an order of magnitude increase in the current at -0.2 V was observed on all other gate metallizations aged for 2 hours.

**4.4.2 Thermal Stability of InAs/AlGaAsSb/InAs by X-ray Photoelectron Spectroscopy**

A first trial for the XPS depth profile was on the blank HEMT wafer as received, and aged at 250 °C for 24 hours in UHP Ar. The Al 2s, Sb 3d, O KLL, Ga 2p, In 3d, and As 3d peaks were recorded and a 10 sec ion gun etch interval was used for depth profiling. As shown in Fig 4.9, no change in the heterostructures was observed from the XPS depth profiles on the sample before and after aging, which suggests that the epilayers are thermally stable at 250 °C for 24 hours in Ar. In addition, the observed approximate atomic concentration in the AlGaAsSb barrier layer from all three XPS depth profiles are very close to Al$_{0.80}$Ga$_{0.20}$As$_{0.16}$Sb$_{0.84}$, which shows a good agreement with the composition provided by HRL.
4.5 Thermal Stability of Gate Metallizations on AlGaAsSb with InAs Cap

Various gate metallizations were fabricated on the AlGaAsSb layer with the InAs cap. Aging of the gate metallizations were performed at 250 °C in UHP Ar. The I-V characteristics, XPS depth profiles, and cross-sectional TEM were compared.

Fig 4.9: XPS depth profiles of InAs/AlGaAsSb/InAs (a) as received and (b) aged at 250 °C for 24 hours in UHP Ar.
4.5.1 Thermal Stability of Gate Metallizations on AlGaAsSb with InAs Cap Determined by I-V Measurement

The tested gate metallizations were listed in Table 4.3, and I-V characteristics were compared, as shown in Fig 3.9 (a)-(i). W/Au gate metallizations were deposited using dc magnetron sputtering system, and e-beam deposition was used for all the other gate metallizations. The I-V characteristics of all as-deposited gate metallizations show low current. For the as deposited condition, W/Au (100/100 nm) gate metallizations have symmetric I-V characteristics. For the Ti/Au, Ti/Pt/Au (5/50/100 nm), Ti/Pt/Au (50/50/100 nm), and W/Au (30/100 nm) gate metallizations, the current at -0.2 V is higher than that at +0.2 V. No difference in the I-V characteristics was observed for the Co/Si/Co/Si/Co with and without the Au cap. On the other hand, Al/Co/Al/Co/Al/Co, Co/Al/Co/Al/Co/Al, Co/Si/Co/Si/Co, and Co/Si/Co/Si/Co/Au gate metallizations have a higher current at -0.2 V than that at +0.2 V. Rapid degradation was observed for Al/Co/Al/Co/Al, Co/Al/Co/Al/Co/Al, Ti/Au, Ti/Pt/Au (5/50/100 nm), and W/Au (30/100 nm) after aging, but the surface morphology remained unchanged. The I-V characteristics of Ti/Pt/Au (50/50/100 nm) gate metallizations remained nearly unchanged after aging for 8 hours, but degraded after aging for 14 hours, as shown in Fig 3.9 (e). This result differs significantly from that for the Ti/Pt/Au (5/50/145 nm) gate metallizations, since rapid degradation upon aging was observed with the thinner Ti layer. Similarly, the I-V characteristics of W/Au (100/100 nm) gate metallizations in Fig 3.9 (g) showed no change after 2 hours aging, but an order of magnitude increase in the current was observed after 3 hours aging. Further degradation in the I-V characteristics was observed after aging for 5 hours, but the surface morphology
remained the same. Co/Si/Co/Si/Co and Co/Si/Co/Si/Co/Au exhibited excellent thermal stability on InAs, as shown in Fig 3.9 (h) and (i), except for an increase in the current at forward bias after 30 min aging. The I-V characteristics show Co/Si/Co/Si/Co is thermally stable for 14 hours, and degradation occurred after aging for 21 hours. Hence, the most stable gate metallizations were first Co/Si/Co/Si/Co (stable at 250 °C in UHP Ar for at least 14 hours), and second Ti/Pt/Au (50/50/100 nm) (stable at 250 °C in UHP Ar for at least 8 hours).

Table 4.3: List of gate metallizations on InAs.

<table>
<thead>
<tr>
<th>Metallizations</th>
<th>Thickness (nm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Al/Co/Al/Co/Al/Co</td>
<td>(20/13.3/20.1/13.3/20/13.3)</td>
</tr>
<tr>
<td>Co/Al/Co/Al/Co/Al</td>
<td>(13.3/20/13.3/20.1/13.3/20)</td>
</tr>
<tr>
<td>Ti/Au</td>
<td>(10/290)</td>
</tr>
<tr>
<td>Ti/Pt/Au</td>
<td>(5/50/100)</td>
</tr>
<tr>
<td>Ti/Pt/Au</td>
<td>(50/50/100)</td>
</tr>
<tr>
<td>W/Au</td>
<td>(30/100)</td>
</tr>
<tr>
<td>W/Au</td>
<td>(100/100)</td>
</tr>
<tr>
<td>Co/Si/Co/Si/Co</td>
<td>(5/28.5/5/50/11.5)</td>
</tr>
<tr>
<td>Co/Si/Co/Si/Co/Au</td>
<td>(5/28.5/5/50/11.5/100)</td>
</tr>
</tbody>
</table>
Fig 4.10: I-V characteristics of gate metallizations on AlGaAsSb with InAs cap aged at 250 °C in UHP Ar.
4.5.2 Thermal Stability of Gate Metallizations on AlGaAsSb with InAs Cap by X-ray Photoelectron Spectroscopy

Ti/Pt/Au (50/50/100 nm) and Co/Si/Co/Si/Co (5/28.5/5/50/11.5 nm) gate metallizations were investigated by XPS due to their competitive thermally stability. The Ti/Pt/Au gate metallization as deposited and aged at 250 °C for 15 hours in Ar (after degradation in the I-V characteristics) were compared, as shown in Fig 4.11. The XPS depth profiles were collected from the Au 4p, Pt 4p, Ti 2p, Al 2s, Ga 2p, Sb 3d, In 3d, As
3d, and O KLL with a 30 sec ion gun etch interval. The Ti/Pt/Au layers were observed on the sample surfaces without much mixing. The InAs cap layer was observed at the Ti/InAs/AlGaAsSb interface by an increase of the indium and arsenic signals. No significant change in the heterostructures was found after aging. However, the etch time where the position of the Ti/InAs interface was found could provide some hint as to what is occurring. The capping InAs layer is observed after approximately 480 sec etching for the as-deposited and 450 sec for the aged sample. Moreover, the AlGaAsSb layer in the aged sample is also shifted about 60 sec toward the surface, which suggests that the metal/semiconductor interface has slightly displaced after aging.
XPS depth profiles were also performed for Co/Si/Co/Si/Co gate metallizations as deposited, aged for 14 hours, and aged for 27 hours at 250 °C in UHP Ar. Co 2p, Si 2p, Al 2s, Ga 2p, Sb 3d, O KLL, In 3d, and As 3d peaks were used with a 30 sec ion gun etch interval. For the as-deposited condition, three Co layers were found in the metallization from the surface to the metal/semiconductor interface, followed by the observation of the heterostructure, as shown in Fig 4.12 (a). After aging at 250 °C for 14 hours in Ar, a
smoother depth profile for the Co and Si layers was observed in the metallization, which suggests a change in the metallization, but InAs/AlGaAsSb/InAs HEMT layers remained unchanged, as shown in Fig 4.12 (b).

Fig 4.13: XPS depth profile of Co/Si/Co/Si/Co gate metallizations on InAs/AlGaAsSb/InAs for (a) the as deposited condition, and (b) aged at 250 °C in Ar for 14 hours.

Fig 4.13 shows the depth profile for the Co/Si/Co/Si/Co gate metallizations aged at 250 °C in Ar for 27 hours to study the degradation mechanism for the I-V
characteristics. A slight change was found at the interface, compared to that for the sample aged for 14 hours. The Co and Si signals were detected further into the AlGaAsSb, which suggests that the interface mixing occurred after samples were aged for 27 hours. However, even though observations of the metal/semiconductor interfaces for Co/Si/Co/Si/Co and Ti gates as slightly displaced toward the surface were made, the interdiffusion between the metallizations and semiconductor epilayers still can not be conclusively verified due to the long sputter time and stability of the sputter rate on samples during depth profiling. Further experiments using cross-sectional TEM were performed to resolve the limit of the depth resolution.

Fig 4.13: XPS depth profile of Co/Si/Co/Si/Co gate metallizations on InAs/AlGaAsSb/InAs aged at 250 °C in Ar for 27 hours.
4.5.3 Thermal Stability of Co/Si/Co/Si/Co Gate Metallizations on AlGaAsSb with InAs Cap by Cross-Sectional TEM

Cross-sectional TEM was performed on the Ti/Pt/Au (50/50/100 nm) and Co/Si/Co/Si/Co gate metallizations in order to investigate the mechanisms for the degradations in the I-V characteristics (Fig 3.9 (e) and (i)). The as-deposited Ti/Pt/Au (50/50/100 nm) gate metallizations, Ti/Pt/Au aged for 8 hours, and aged for 15 hours were compared, as shown in Fig 4.14, Fig 4.15, and Fig 4.16, respectively. Similar results were observed for the as-deposited condition and the gate metallizations aged for 8 hours, in which layers of Ti/Pt/Au gate metallizations and InAs/AlGaAsSb/InAs HEMTs were observed from the cross-sectional TEM images. No significant change was found from the cross-sectional EDS line scans. High intensities of Ga and As in the Pt and Au layers for both conditions are believed to be artifacts due to peak overlaps between gallium, arsenic, gold and platinum. An increase in the integrated peak intensity of the indium and arsenic at about 100 nm in depth indicates the location of the InAs cap. On the other hand, for the Ti/Pt/Au (50/50/100 nm) gate metallizations aged for 15 hours (corresponding to the aging time when the failure of the I-V characteristics observed in Section 4.5.1), a change occurred at the interface between the metallization and HEMT, as shown in Fig 4.16. The InAs cap was absent, and isolated grains were measured about 10 nm in depth at the interface. Furthermore, comparing the cross-sectional EDS line scans across the interface with (Fig 4.17) and without (Fig 4.18) a grain, the isolated grains consist mostly of indium, and arsenic is found to react with titanium after 15 hours aging, which is in agreement with prior work of Swenson that TiAs is in thermodynamic equilibrium with In and InAs[58].
Fig 4.14: Cross-sectional TEM image and the corresponding EDS line scan of an as-deposited Ti/Pt/Au (50/50/100 nm) gate metallization.

Fig 4.15: Cross-sectional TEM image and the corresponding EDS line scan of a Ti/Pt/Au (50/50/100 nm) gate metallization aged at 250 °C for 8 h in UHP Ar.
Fig 4.16: Cross-sectional TEM image and the corresponding EDS line scan of a Ti/Pt/Au (50/50/100 nm) gate metallization aged at 250 °C for 15 h in UHP Ar.

Fig 4.17: Cross-sectional EDS line scan across the interface with a grain.
For the Co/Si/Co/Si/Co gate metallizations, the as-deposited Co/Si/Co/Si/Co gate metallizations, Co/Si/Co/Si/Co gate metallizations aged for 10 hours, and 27 hours were compared, as shown in Fig 3.3, Fig 3.17, and Fig 3.10, respectively. Distinct layers consisting of Co/Si/Co/Si/Co/InAs/AlGaAsSb/InAs were detected via cross-sectional EDS line scans, as shown in Fig 3.3. For the sample annealed at 250 °C for 10 hours, an increase in the thickness of the Co-rich layers in the cross-sectional TEM image due to incorporation of Si was observed for the metallizations aged for 10 hours, compared to the as-deposited condition. No change is observed at the interface between the metallization and semiconductor heterostructure. On the other hand, significant interfacial reaction between the metallizations and InAs cap was observed in the cross-sectional TEM images after aging for 27 hours, as shown in Fig 3.10. Agglomeration and grain formation consisting of a Co-Si-In-As phase were observed at the interface, as
shown in Fig 4.22. This condition corresponds to degraded electrical characteristics, as described in Section 4.5.1.

Fig 4.19: Cross-sectional TEM image and the corresponding EDS line scan of an as-deposited Co/Si/Co/Si/Co gate metallization.
Fig 4.20: Cross-sectional TEM image and the corresponding EDS line scan of a Co/Si/Co/Si/Co gate metallization aged at 250 °C for 10 h in UHP Ar.

Fig 4.21: Cross-sectional TEM image and the corresponding EDS line scan of a Co/Si/Co/Si/Co gate metallization aged at 250 °C for 27 h in UHP Ar.
4.6 Discussion

The gate metallizations associated with the degradation time at 250 °C on AlGaAsSb with the InAs cap removed and AlGaAsSb with the InAs cap are summarized in Table 3.2 and Table 3.4, respectively. W/Au gate metallizations are found to be good candidates for making thermally stable gate metallizations on AlGaAsSb without the InAs cap. Comparing W/Au (30/100 nm) and W/Au (100/100 nm), an addition of 70 nm to the tungsten barrier gives a longer thermal stability at 250 °C, which demonstrates that tungsten is effective for thermally stable gate metallizations and is in agreement with the thermodynamic prediction that W is in equilibrium with AlSb[52]. A degradation of the I-V characteristics on W/Au (100/100 nm) gate metallizations occurred after aging for 4 hours.

Fig 4.22: Cross-sectional TEM image of a Co/Si/Co/Si/Co gate metallization aged at 250 °C for 27 h in UHP Ar.
Table 4.4: Thermal stability of different gate metallizations on AlGaAsSb aged at 250 °C in UHP Ar.

<table>
<thead>
<tr>
<th>Gate metal</th>
<th>The longest aging time tested before degradation</th>
<th>Time to fail</th>
</tr>
</thead>
<tbody>
<tr>
<td>Co/Al/Co/Al/Co/Al</td>
<td>20 days</td>
<td>(no information)</td>
</tr>
</tbody>
</table>
Table 4.5: Thermal stability of different gate metallizations on InAs aged at 250 °C in UHP Ar.

<table>
<thead>
<tr>
<th>Gate metal</th>
<th>The longest aging time tested before degradation</th>
<th>Time to fail</th>
</tr>
</thead>
<tbody>
<tr>
<td>Co/Al/Co/Al/Co/Al (13.3/20/13.3/20.1/13.3/20 nm)</td>
<td>As deposited</td>
<td>30 min</td>
</tr>
<tr>
<td>Al/Co/Al/Co/Al/Co (20/13.3/20.1/13.3/20/13.3 nm)</td>
<td>As deposited</td>
<td>30 min</td>
</tr>
<tr>
<td>Ti/Au (10/290 nm)</td>
<td>As deposited</td>
<td>1 hr</td>
</tr>
<tr>
<td>Co/Si/Co/Si/Co/Au (5/28.5/5/50/11.5/100 nm)</td>
<td>34 hrs</td>
<td>40 hrs</td>
</tr>
<tr>
<td>Co/Si/Co/Si/Co (5/28.5/5/50/11.5 nm)</td>
<td>14 hrs</td>
<td>21 hrs</td>
</tr>
<tr>
<td>W/Au (30/100 nm)</td>
<td>As deposited</td>
<td>2 hr</td>
</tr>
<tr>
<td>W/Au (100/100 nm)</td>
<td>2 hrs</td>
<td>3 hrs</td>
</tr>
<tr>
<td>Ti/Pt/Au (50/50/100 nm)</td>
<td>8 hrs</td>
<td>14 hrs</td>
</tr>
<tr>
<td>Ti/Pt/Au (5/50/100 nm)</td>
<td>As deposited</td>
<td>1 hr</td>
</tr>
</tbody>
</table>
For the gate metallizations on the InAs cap, in order to compare the relationship between gate metallizations on AlGaAsSb with the InAs cap and the I-V characteristics, current densities at +2 V and -2 V are plotted as a function of aging time, as shown in Fig 4.23 and Fig 4.24, respectively. Different levels of currents were observed for the different as-deposited gates, but no relationship between metal work function and the current density is observed. This is consistent with the finding by Bolognesi et al. that the gate metallization could shift the surface Fermi level pinning position on InAs/AlSb heterostructures, and it was speculated that this observation was due to metal/InAs reactions.[50] At forward bias, the most stable gate metallization is Ti/Pt/Au (50/50/100 nm), which is stable for 8 hours at 250 °C. Cross-sectional TEM revealed that no degradation of the HEMT after aging for 8 hours. In addition, Co/Si/Co/Si/Co showed a change at the forward current after a 30 min anneal. An increase in the current after 30 min annealing was observed, and then the current was stable for 14 hours annealing before further degradation. This change after 30 min might be linked to the observation of the mixing of the Co and Si layers that was indicated by the XPS depth profiles and the cross-sectional EDS line scans. Deposition of Co/Si/Co/Si/Co layers could introduce additional metal/semiconductor Schottky barriers for carrier transport, since Si is semiconducting. The Schottky barrier due to the Co/Si/Co junction may be reduced after the Co layers are alloyed, as indicated by the XPS depth profile Fig 4.12 (b) and the cross-sectional EDS line scan (Fig 4.22). Unfortunately, the residual Si semiconductor unmixed with Co, left due to incomplete reaction between Co and Si, was unanticipated and discovered only late in this work. A semiconducting layer in the gate metallization is obviously undesirable unless it is degeneratively doped and very conductive.
At reverse bias, Co/Si/Co/Si/Co and Co/Si/Co/Si/Co/Au gate metallizations exhibited excellent thermal stability at 250 °C. The degradation in the I-V characteristics was observed after aging at 250 °C for 21 hours in UHP Ar, which is associated with the

Fig 4.23: Comparison of current density at +2 V of gate metallizations on InAs.

Fig 4.24: Comparison of current density at -2 V of gate metallizations on InAs.
interfacial reaction between Co/Si and InAs for the sample aged for 27 hours that was observed in the cross-sectional TEM (Fig 4.22). Similarly, the degradation of the Ti/Pt/Au (50/50/100 nm) gate metallizations was observed after 14 hours aging in both electrical properties and the interface morphology. Cross-sectional TEM verified that Ti is a good candidate for making a thermally stable gate metallization on InAs due to the slow reaction rate. Mixing of the titanium and arsenic at the interface and formation of isolated grains that consisted mostly of indium (Fig 4.17) were observed after aging for 15 hours. However, the Co/Si/Co/Si/Co aged for 27 hours and the Ti/Pt/Au (50/50/100 nm) aged for 15 hours did not consume all the AlGaAsSb barrier, which indicates that the degradation of the I-V characteristics may be primarily due to the consumption of the InAs cap.

Consistently, different I-V characteristics are observed on AlGaAsSb with and without the InAs cap removed, as shown in Fig 4.25 for the as-deposited Co/Si/Co/Si/Co, Fig 4.26 for the as-deposited Ti/Pt/Au (50/50/100 nm), and Fig 4.27 for the as-deposited W/Au (30/100 nm) gate metallizations. Higher leakage currents at -0.2 V were observed for the gate metallizations on AlGaAsSb with the InAs cap removed, compared to those on AlGaAsSb with the InAs cap. Furthermore, most of the degraded I-V characteristics on the HEMT with the InAs cap have comparable currents with the as-deposited I-V characteristics for the gate metallizations on the HEMT without the InAs cap. This suggests that the barrier height for current transport is altered when the InAs cap is consumed, consistent with reports that the InAs cap layer shifts the surface Fermi level pinning position of the heterostructure.[44],[47],[50],[51]
Fig 4.25: I-V characteristics of the as-deposited Co/Si/Co/Si/Co gate metallizations on AlGaAsSb with and without InAs cap.

Fig 4.26: I-V characteristics of the as-deposited Ti/Pt/Au (50/50/100 nm) gate metallizations on AlGaAsSb with and without InAs cap.
An energy band diagram for the as-grown InAs/Al$_{0.80}$Ga$_{0.20}$As$_{0.16}$Sb$_{0.84}$/InAs heterostructure is shown in Fig 4.28. The lattice constant of the Al$_{0.80}$Ga$_{0.20}$As$_{0.16}$Sb$_{0.84}$ is matched to InAs (6.05 Å).[59] The bandgap of the Al$_{0.80}$Ga$_{0.20}$As$_{0.16}$Sb$_{0.84}$ (1.51 eV) and the conduction band discontinuity between Al$_{0.80}$Ga$_{0.20}$As$_{0.16}$Sb$_{0.84}$ and InAs ($\Delta E_C = 1.20$ eV) were calculated based on the published estimates for the lattice matched Al$_x$Ga$_{1-x}$As$_y$Sb$_{1-y}$/InAs heterostructure.[59] The Fermi level pinning position is 80 meV above the conduction band energy of InAs according to Nguyen et al.[47], and electrons are confined in the InAs quantum well.

Fig 4.27: I-V characteristics of the as-deposited W/Au (30/100 nm) gate metallizations on AlGaAsSb with and without InAs cap.
For the similar case of InAs/AlSb/InAs heterostructures, when a metal contact is deposited on the InAs/AlSb/InAs, the surface Fermi level pinning position shifts upward by $\Delta E_m$, resulting in an asymmetric barrier.[44],[51]. A similar shift is shown for our InAs/Al$_{0.80}$Ga$_{0.20}$As$_{0.16}$Sb$_{0.84}$/InAs heterostructure in Fig 4.29. A Schottky barrier ($q\Phi_B$) is formed at zero bias for hole transport. For the high current observed in the samples with the surface InAs cap removed, either by chemical etching[44],[46],[47],[50] or by the metal/InAs reaction, the surface Fermi level pinning position shifts downward by $\Delta E$, leading to a reduced Schottky barrier height for hole transport ($q\Phi_B - \Delta E$), as shown in Fig 4.30. In addition, if the metallizations further react with AlGaAsSb, reactions could alter the composition of the AlGaAsSb barrier, causing a change in the valence band position of the AlGaAsSb barriers.[44],[57] Consequentially, the barrier height for hole
transport is also reduced, and increased current densities are observed for the gate metallizations on AlGaAsSb.

Fig 4.29: Schematic energy band diagram of an as-deposited gate metallization on an InAs/Al\textsubscript{0.80}Ga\textsubscript{0.20}As\textsubscript{0.16}Sb\textsubscript{0.84}/InAs heterostructure.

Fig 4.30: Schematic energy band diagram of a metal/Al\textsubscript{0.80}Ga\textsubscript{0.20}As\textsubscript{0.16}Sb\textsubscript{0.84}/InAs heterostructure with the InAs cap removed by chemical etching or metal/InAs reactions.
In conclusion, W/Au is the most promising candidate for thermally stable gate metallizations on AlGaAsSb. Co/Si/Co/Si/Co and Ti/Pt/Au (50/50/100 nm) are thermally stable gate metallizations on InAs. However, the performance of the Co/Si/Co/Si/Co and Ti/Pt/Au gates should be compared in transistors. Cross-sectional TEM confirmed that the degradation of the I-V characteristics for the gate metallizations on the HEMT with the InAs cap is associated with the consumption of the InAs cap by metal/InAs reactions. The effect of the InAs cap on the surface Fermi level pinning position is evident by comparing the I-V characteristics of the gate metallizations with and without the InAs cap, in which an downward shift in the surface Fermi level pinning position occurs when the InAs cap is either chemically etched prior to the metallization or consumed by the metal/InAs reaction. Therefore, a reduced Schottky barrier height for hole transport leads to high leakage currents for the I-V characteristics of the degraded gate on InAs/AlGaAsSb/InAs, or the as-deposited gate on AlGaAsSb/InAs with the InAs cap.
5.1 Conclusion

Design of a shallow, thermally stable ohmic contact to p-InGaSb for the base of a HBT is described in Chapter 3. An as-deposited Pd/W/Au (5/50/145 nm) contact with a specific contact resistance of $3.0 \times 10^{-7} \, \Omega \cdot \text{cm}^2$ was developed. The Au layer lowers the metal sheet resistance, which was verified to be a critical parameter for achieving a low contact resistance. Palladium is employed for making intimate contact to p-InGaSb, and W is used as a diffusion barrier to protect the semiconductor from reaction with a Au cap. In addition, the (NH$_4$)$_2$S rinse treatment, combining 16.5 % HCl for 30 s followed by a rinse in 2.1 % (NH$_4$)$_2$S for 1-2 s, was developed for making an abrupt metal/p-InGaSb interface. A shallower Pd/W/Au (2/50/145 nm) contact with the (NH$_4$)$_2$S rinse treatment yielded a reduced specific contact resistance of $5.9 \times 10^{-7} \, \Omega \cdot \text{cm}^2$ for the as-deposited condition.

While the low resistance ohmic contact was obtained on the as-deposited Pd/W/Au (2/50/145 nm) sample, this contact was no longer shallow due to the formation of isolated grains after samples were aged at 250 °C for 1 day. Hence, the specific contact resistances of as-deposited Pt/W/Au, Pd/W/Au, Co/W/Au, Cu/W/Au, W/Au, Cr/W/Au, and Ag/W/Au contacts were compared, and the (NH$_4$)$_2$S rinse treatment was found to partially relieve Fermi level pinning at the contact/p-InGaSb interface. As a result, Pt was
studied in more detail as the first contacting layer in metal/W/Au (2/50/145 nm), since it has a high work function and reacts more slowly than Pd. The Pt/W/Au (2/50/145 nm) contact yielded a specific contact resistance of $4 \times 10^{-6} \, \Omega \, \text{cm}^2$ for the as-deposited condition, which is higher than the Pd/W/Au contact, but it is interesting from the point of view of improved thermal stability. No degradation of the specific contact resistance was observed after aging at 250 °C for 3 days. It was further verified by the cross-sectional TEM that this contact remains shallow with a consumption of only 5.9 nm of InGaSb after aging at 250 °C for 3 days in an evacuated quartz tube.

Design of a shallow, thermally stable gate metallization on InAs/AlGaAsSb/InAs and AlGaAsSb/InAs HEMTs is demonstrated in Chapter 4. A W/Au gate on AlGaAsSb/InAs is thermally stable for 3 hours at 250 °C in Ar. Ti/Pt/Au (50/50/100 nm) and Co/Si/Co/Si/Co gates are thermally stable at 250 °C for at least 8 hours and 14 hours on InAs/AlGaAsSb/InAs, respectively. It was observed by cross-sectional TEM that the mixing of metals and InAs was responsible for degradation of the I-V characteristics, and a mechanism was proposed to explain the relationship between the degradation in the I-V characteristics and the consumption of the InAs cap by the metal/InAs reactions. The absence of the InAs cap may cause a downward shift in the surface Fermi level pinning position, resulting in a reduced Schottky barrier height and high leakage currents.

### 5.2 Suggested Future Work

In the gate metallization study, reduced leakage currents were observed on the diodes with the InAs cap, compared to those on the diodes without the InAs cap, which
might be associated with the Fermi level pinning position shifted by the InAs cap. Another interesting investigation would be to test the (NH$_4$)$_2$S rinse treatment on the heterostructures with and without the InAs cap. The (NH$_4$)$_2$S rinse treatment was found to reduce the density of surface states of the p-InGaSb, which causes the Fermi level pinned to be relieved. Subsequently, a metal work function dependence of the Schottky barrier height was observed. A similar effect might be observed on the InAs or AlGaAsSb surfaces treated with the sulfide rinse. However, an etch rate study of InAs or AlGaAsSb in HCl and (NH$_4$)$_2$S should first performed to minimize the semiconductor removal by chemical etching.

Finally, the Co/Si/Co/Si/Co gate showed a better thermal stability on InAs than the Ti/Pt/Au gate. However, it was observed by cross-sectional TEM that the Co/Si/Co/Si/Co gate was not completely mixed even after aging, although it was stable at least 14 h. Therefore, optimization of the Co/Si/Co/Si/Co layer thickness to avoid unreacted semiconducting Si after an initial annealing procedure might be attractive for fabricating low power, high speed HEMTs.
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   5490 (1994).


52. S. E. Mohney, unpublished calculation.


Appendix A

CALCULATION OF THE UNCERTAINTY FOR THE SPECIFIC CONTACT RESISTANCE

Assuming that a, b, c, ..., z are the measured quantities with corresponding uncertainties $S_a, S_b, S_c, ... , S_z$, respectively, and

\[ q = a - b + c - d + ... + y - z . \]  \hspace{1cm} \text{Eq A.1}

The uncertainty for the quantity ($S_q$) can be expressed as[60]

\[ S_q = \sqrt{S_a^2 + S_b^2 + S_c^2 + ... + S_z^2} . \]  \hspace{1cm} \text{Eq A.2}

For the propagation of the uncertainties in products and quotients, assuming that

\[ q = \frac{a \times b \times c}{x \times y \times z} , \]  \hspace{1cm} \text{Eq A.3}

the uncertainty in q is[60]

\[ S_q = q \times \sqrt{\left(\frac{S_a}{a}\right)^2 + \left(\frac{S_b}{b}\right)^2 + \left(\frac{S_c}{c}\right)^2 + \left(\frac{S_x}{x}\right)^2 + \left(\frac{S_y}{y}\right)^2 + \left(\frac{S_z}{z}\right)^2} . \]  \hspace{1cm} \text{Eq A.4}

In addition, if

\[ q = \frac{x}{B} , \]  \hspace{1cm} \text{Eq A.5}

where B is an exact number, then[60]

\[ S_q = \frac{S_x}{|B|} . \]  \hspace{1cm} \text{Eq A.6}
In the CTLM analysis, the individual specific contact resistance \( (\rho_C) \) is the product of the semiconductor sheet resistance \( (R_S) \) and the transfer length \( (L_T) \) square, as shown in Eq A.7.

\[
\rho_C = R_S \times L_T^2 \tag{Eq A.7}
\]

Therefore, by using propagation in products in Eq A.3 and Eq A.4, for a given uncertainty of the semiconductor sheet resistance \( (S_{RS}) \) and the transfer length \( (S_{LT}) \) that are extracted from the CTLM curve fit, the uncertainty of the individual specific contact resistance \( (S_{\rho_C}) \) can be calculated by

\[
S_{\rho_C} = \rho_C \times \sqrt{\frac{(S_{RS})^2}{R_S} + 2\frac{(S_{LT})^2}{L_T}}. \tag{Eq A.8}
\]

Moreover, when an average specific contact resistance \( (R_c) \) is calculated from more than one of the individual specific contact resistance \( (\rho_{C1}, \rho_{C2}, \rho_{C3}, \ldots, \rho_{Cn}) \)

\[
R_c = \frac{\rho_{C1} + \rho_{C2} + \rho_{C3} + \ldots + \rho_{Cn}}{n}, \tag{Eq A.9}
\]

where \( n \) is the number of the individual specific contact resistance. Using the propagation in Eq A.1, Eq A.2, Eq A.5, and Eq A.6, the uncertainty of the averaged specific contact resistance is then

\[
S_{R_c} = \sqrt{\frac{(S_{\rho_{C1}})^2 + (S_{\rho_{C2}})^2 + (S_{\rho_{C3}})^2 + \ldots + (S_{\rho_{Cn}})^2}{n}}, \tag{Eq A.10}
\]

where \( S_{\rho_{C1}}, S_{\rho_{C2}}, S_{\rho_{C3}}, \) and \( S_{\rho_{Cn}} \) are the first, second, third, and nth uncertainty of the individual specific contact resistance, respectively.
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PUBLICATIONS


