ACTIVE ENERGY HARVESTING ON PIEZOELECTRIC MATERIALS: EXPERIMENTAL DEMONSTRATION AND STANDALONE CIRCUIT IMPLEMENTATION

A Thesis in
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by
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Abstract

The need for wireless remote sensors is a fast increasing trend in many industries. The sensors need to survive without maintenance for long periods of time or indefinitely, especially for those placed in inaccessible locations. Energy harvesting using piezoelectric devices is a possible solution to this problem. There are two types of energy harvesting approaches; namely, passive and active. The passive methods are well established and have already been put into new sensor product by some companies, but the performance of the passive method is much lower than the energy potential of the piezoelectric devices.

The active energy harvest idea, which was proposed in [1] and systematically studied by Dr. Yiming Liu in [2], increases the efficiency of energy harvesting dramatically. However, instead of using a practical low-power standalone circuit to support his ideas, he performed the experiment by using a microcontroller with very high power consumption which is thousands times higher than the power generation capacity of the piezoelectric materials.

In this thesis, an improved active energy harvesting core interface is developed and the supporting standalone circuit with ultra-low power consumption is proposed. The piezoelectric PVDF is used for energy harvesting, it provides much higher power than the single-crystal material used in [2] when utilizing a multi-layer configuration. The harvested power achieved under this approach was up to 27mW at 1.4% strain, and the power consumption of the standalone active circuit was only 1.4mW.
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\begin{itemize}
  \item $S$ Strain of Piezoelectric Device
  \item $d$ Piezoelectric Constant
  \item $T$ Stress applied to Piezoelectric Device
  \item $E$ Electric field intensity
  \item $s$ Compliance
  \item $D$ Electric displacement
  \item $\epsilon$ Permittivity
  \item $Q$ Electrical Charge
  \item $Y$ Young’s Modulus
  \item $V_{OC}$ Open circuit voltage of piezoelectric device
  \item $\omega$ Resonant mechanical excitation frequency of the vibrating structure
  \item $f_s, T_s$ Switching frequency, switching period
  \item $\Delta_1$ Period in converter’s switch cycle that switch is "off" and current flows through the freewheeling diode (DCM of the flyback converter only)
  \item $l, w, t$ Length, width, thickness of the piezoelectric device
\end{itemize}
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Introduction

The contribution of this thesis is mainly based on implementing the active energy harvesting\textsuperscript{[2]} concept. Rather than focusing on analyzing and generating the equations for the active boundary control, we are interested in designing a practical actively-controlled electrical interface which will consume only a fraction of the power that can be harvested from the piezoelectric device. Through analysis and experimental demonstration, the performance of the active energy harvesting is evaluated and compared with the passive method considering the power consumption of the active supporting circuits.

1.1 Motivation and Contribution of the Thesis

In recent years, as the demand for high-performance wireless sensors is increasing in many industries, energy harvesting technology is becoming an important aspect of the future sensor development. Converting mechanical energy to electrical energy using piezoelectric materials has been the choice for many energy harvesting applications. In between the piezoelectric device and the actual electrical loads, an energy harvesting circuit is inserted as the electrical interface such that the power conditioning, impedance matching \textsuperscript{[4]} \textsuperscript{[5]} \textsuperscript{[6]} \textsuperscript{[3]} or more complicated active boundary control \textsuperscript{[1]}\textsuperscript{[7]} can be applied. Therefore well designed energy harvesting interfaces are highly desired.

There are two important aspects when designing the energy harvesting inter-
face. First, the efficiency of the electrical interface plays a key role when converting mechanical energy to electrical energy; Second, the power required by the circuits within the interface which support the energy harvesting technology is also critical, since the power generation of the piezoelectric materials is normally low. The conventional electrical interface, such as passive energy harvesting, focuses on the power conditioning concepts, which often involves AC/DC rectification followed by voltage regulation. Even though a well-designed passive interface requires only a ignorable fraction of power that can be harvesting by the piezoelectric materials, the potential of the piezoelectric energy harvesting is not achieved. Therefore, some scholars propose other approaches such as Synchronous Charge Extraction [7] and Active Energy Harvesting [2].

When properly applying the appropriate electrical boundary condition to the piezoelectric materials, more energy can be transferred to the electrical side rather than lost in the electro-mechanic couplings. However, in order to achieve this boundary control, a more complex circuit is required as well as its supplemental circuits. Unfortunately, in [2], the author did not make effort in designing such circuit, but focused instead on demonstrating the active concept. The instruments supporting the circuit are very power consuming, such much so that they are overwhelming the power that is harvested.

Therefore, an improved standalone active interface with ultra-low power consumption is proposed in this thesis, along with the improvement of the active energy harvesting core circuit. Experiments are performed for piezoelectric energy harvesting both by using a standalone active circuit and standalone passive circuit. The results show that active energy harvesting is much better than the passive methods.

1.2 Thesis Overview

Chapter 2 contains a background review of energy harvesting on piezoelectric materials. First, the piezoelectric material-polyvinylidene fluoride(PVDF) is intro-
duced, and the property and optimal configuration of the material is discussed. Then, an equivalent electric circuit model of the quasi-static energy conversion cycle of piezoelectric material is shown. Based on this model, passive and active energy harvesting methods are discussed and compared.

In Chapter 3, we start with the design of the interface for passive energy harvesting in detail, then the supporting circuits such as gate driver, duty cycle generator and control circuit are discussed separately. Then, a standalone circuit for this technique is proposed. Finally, the application of a DCM flyback converter in the active energy harvesting technique is discussed. In this chapter, we also investigate the efficiency of the interface, as well as the power loss analysis for the supporting circuitry.

Chapter 4 contains a the systematic analysis and design of the active energy harvesting technique, as well as the standalone circuit. The first part of the chapter is focused on the theoretical analysis of the active technique, then the improved active core circuit full-bridge inverter is proposed and analyzed. At the end of the chapter, the standalone circuits for the active energy harvesting, along with the DCM flyback circuit, are discussed in detail.

Chapter 5 contains an experimental demonstration of both passive and active energy harvesting using multi-layer PVDF devices. The experiment results are compared with the discussion in Chapter 3, followed by a loss analysis of the circuits. In the end the performance of the standalone active circuit is shown.

Chapter 6 concludes the work for the thesis, and proposes future work to improve the core efficiency of the circuit and further reduce the power required for the standalone circuit.
Chapter 2

Theoretical Background of Energy Harvesting

2.1 Piezoelectric Devices

2.1.1 Quasi-Static Model of Piezoelectric Materials

Piezoelectricity is a mutual coupling between mechanical strain/stress and electric field/flux density. Although the constitutive equations of piezoelectricity are expressed mostly in tensor form[8], the piezoelectric device can be described by scalar expressions provided that the direction of the mechanical stress and electric field applied to the material is fixed.[9]

\[
S = d \cdot E + s \cdot T, \\
D = d \cdot T + \epsilon \cdot E
\] (2.1)

In the case of the PVDF material that is currently being used for energy harvesting on this project, since the stress is applied along the 1-direction and the electrodes are only attached on the surface of 3-direction, more specific mathematical expressions for the constitutive properties of the material under quasi-static
conditions are given as follows.[10]

\[
S = \frac{d_{31}}{t} \cdot V + \frac{1}{Y_{11} \cdot wt} \cdot F,
\]

\[
Q = d_{31} \frac{l}{t} \cdot F + C \cdot V
\]

(2.2)

where \( S \) is the effective strain of the device, \( Q \) is the electrical charge on the electrodes of the device, \( F \) is the force exerted on the device, \( V \) is the voltage across the electrodes, \( Y \) is Young’s modulus under constant voltage, \( d \) is the general piezoelectric coefficient, \( C \) is the capacitance under constant force, \( l, w, t \) stand for effective length, width and thickness respectively, and the indices stand for the direction. The chosen model of the device is based on the quasi-static assumption, as it reveals the fundamentals of piezoelectric energy conversion without overly complex mathematical derivation.

### 2.1.2 Equivalent Electrical Model of PVDF Material

When appearing in circuit form under sinusoidal force excitation, the piezoelectric devices can be modeled as an AC current source in parallel with a capacitor, as shown in Fig 2.1.

![Electrical Model](image)

**Figure 2.1.** Electrical Model

The modeled device current is the derivative of the charge accumulated on the device. Applied to the constitute equation (2.2), it becomes

\[
I = \dot{Q} = d_{31} \frac{l}{t} \cdot \dot{F} + C \cdot \dot{V}
\]

(2.3)
By setting charge $Q$ in equation (2.2) to zero, the expression of open circuit voltage is therefore

$$V_{OC} = \frac{l}{t} \cdot \frac{d_{31}}{C} \cdot F$$

(2.4)

Notice that the open circuit is directly proportional to the applied force. By setting voltage $V$ in equation (2.2) to zero and take derivative for both sides, the expression of short circuit current is then,

$$I_{\text{short}} = \frac{l \cdot d_{31} \cdot C'}{t} \cdot \ddot{F}$$

(2.5)

The impedance of the material has only capacitive properties, so it is largely dependent on the mechanical excitation frequency; the expression of the impedance is,

$$Z = \frac{1}{\omega C}$$

(2.6)

where the capacitance $C$ is calculated as

$$C = \epsilon_{33} \frac{l \cdot w}{t}$$

(2.7)

### 2.2 Review of Energy Harvesting Techniques

#### 2.2.1 Mathematical Expression of Energy Harvesting

Converting mechanical energy to electrical energy using piezoelectric devices has been the choice for many energy harvesting applications. The energy harvesting circuit, which is the interface between a piezoelectric device and electrical load, plays a very important role in piezoelectric energy harvesting systems. The amount of energy that can be harvested is measured by the net amount of energy transferred to the electrical side. To simplify the following analysis, the magnitude and the frequency of the mechanical excitation are set to be constant, i.e. $f(t) = -F \cdot$
sin(\omega t). The average piezoelectric power converted to the electrical side is then,

\[ P_{\text{conv}} = \frac{1}{T} \int_{t_0}^{T+t_0} v(t) \cdot i(t) dt \]  \hspace{1cm} (2.8)

By substituting equation (2.2), the equation (2.8) becomes,

\[ P_{\text{conv}} = \frac{1}{T} \int_{t_0}^{T+t_0} (d_{31} \frac{l}{t} \cdot v(t) \cdot \dot{f}(t) + C \cdot v(t) \cdot \dot{v}(t)) dt \]  \hspace{1cm} (2.9)

Note that the second portion of the power conversion is zero because \( v(t) \) and \( \dot{v}(t) \) always have 90 degree difference in phase. The equation (2.9) becomes,

\[ P_{\text{conv}} = d_{31} \frac{l}{t} \cdot \frac{1}{T} \int_{t_0}^{T+t_0} v(t) \cdot \dot{f}(t) dt \]  \hspace{1cm} (2.10)

Thus the average power converted into electricity by the piezoelectric element depends both on the amplitude and phase difference between piezoelectric voltage and the first derivative of applied force. In the case of a harmonic force, the open circuit piezoelectric voltage \( V_{OC} \) is also sinusoidal, and \( v(t) \) and \( \dot{f}(t) \) and are 90° out of phase. So, the average power converted into electricity is obviously zero. When a load or the energy harvesting circuit is connected to the piezoelectric device, the phase difference between \( v(t) \) and \( \dot{f}(t) \) tends to change. Thus, the average converted power defined in equation (2.10) is not zero, but the impedance mismatch between the piezoelectric device and load directly reduces the piezoelectric voltage amplitude, which in turn reduces the power that can be harvested. Therefore maximization of the average converted power can be interpreted in this case as a compromise between the piezoelectric voltage phase shift and its amplitude reduction.

2.2.2 Energy Harvesting System

Typically, energy harvesting systems based on piezoelectric devices can be summarized to have three core components: piezoelectric devices, electric energy storage, and the power electronic interface. With other necessary components, the overall
system of energy harvesting is shown in Fig 2.2. In this chapter we will focus on designing the power electronic interface between the energy storage and piezoelectric device. The stand-alone passive approach will be emphasized first with a modified optimization of the adaptive method.

### 2.2.3 Passive Technique

A vibrating piezoelectric device differs from a typical electrical power source in that its internal impedance is capacitive rather than inductive in nature, and that it may be driven by mechanical vibrations of varying amplitude and frequency; moreover, the load impedance may change significantly. For example, the impedance of a battery varies according to its capacity. Thus a significant amount of power may be lost due to impedance mismatch without the proper interface between the source and the load. The typical passive energy harvesting technique diagram is shown in Fig 2.3.

The idea of adaptive interface circuitry, which performs the impedance match and power regulation, was introduced by Ottman. et. al. [6][3]. This harvesting circuit, as show in Fig 2.4, consists of a full-bridge rectifier with an output capacitor, an electrochemical battery, and a switch-mode DC-DC converter that...
controls the energy flow into the battery. An adaptive control technique is used to continuously implement the optimal power transfer theory and maximize the power stored by the battery.

In the following analysis, the output capacitor of the full bridge rectifier is assumed to be large enough such that the voltage $V_{rect}$ is constant. Since the exerted force is sinusoidal, assuming the voltage is constant after rectification and filtering, the corresponding polarization current can be model in similar sinusoidal form, $i_p(t) = I_p \sin(\omega t)$. The magnitude of the polarization current varies with the mechanical excitation level of the piezoelectric device, but is assumed to be relatively constant regardless of external loading. Since the voltage of the battery is constant, it becomes straightforward to maximize the output power by regulating
the current $I_{\text{out}}$ through the DC-DC converter. The DC component of the load current is provided by [6], which is

$$I_{\text{out}} = \frac{1}{T} \int_{T} i(t)dt = \frac{2I_p}{\pi} - \frac{2V_{\text{rect}}\omega C}{\pi} \quad (2.11)$$

The output power can be shown to vary with the value of the output voltage as follows:

$$P_{\text{conv}} = V_{\text{rect}} \cdot I_{\text{out}} = V_{\text{rect}} \cdot \frac{2I_p}{\pi} - \frac{2V_{\text{rect}}^2\omega C}{\pi} \leq \frac{V_{\text{OC}}^2\omega C}{\pi} \quad (2.12)$$

It can be shown that the maximum power flow occurs when the rectified voltage is half of the open circuit voltage:

$$V_{\text{rect}} = \frac{I_p}{2\omega C} = \frac{1}{2}V_{\text{OC}} \quad (2.13)$$

From an average power flow point of view, the passive approach only controls the voltage magnitude across the piezoelectric device without considering the phase shift between $v(t)$ and $f(t)$, thus a large amount of power is lost during electromechanical interactions, and only a small potion of the energy could be transferred from mechanical side to electrical side.

### 2.2.4 Active Technique

Rather than passively accepting the electrical condition generated by the mechanical excitation, i.e. piezoelectric voltage magnitude, the interface circuit could also be responsible for actively applying electrical boundary conditions, such as voltage magnitude and phase, to the piezoelectric device for each energy conversion cycle. Because of the mutual coupling of the piezoelectric devices, an optimized electrical boundary condition could effectively increase the mechanical energy flow into the energy harvester; in other words, the voltage magnitude and phase difference from the first derivative of the force can be controlled arbitrarily by the inserted electrical interface. We note that there are physical limits of piezoelectric devices, both mechanical and electrical, such as forces, and strains that might crack the device, and break-down electric field or depoling voltage.
A type of active energy harvesting, herein denoted as voltage-controlled active energy harvesting, is shown in Fig 2.5. In stages 1 and 3, the voltage across the device is kept constant by the power electronic circuitry, while the applied force changes from its maximum and minimum value. In stages 4 and 2, the power electronic circuitry charges and discharges the voltage when the force is at its maximum and minimum values. The converted energy can also be calculated from the area of either parallelogram in the electrical or mechanical domain in Fig 2.5. This in turn brings up an important point; the power electronic circuitry connected to the piezoelectric device must be capable of bidirectional power flow to implement active energy harvesting approaches. The average power converted is understood as the energy converted in one cycle multiplied by the frequency of excitation.

![Figure 2.5. Voltage Controlled Active Technique](image)

Unlike the passive approaches, active energy harvesting needs a more flexible power electronic circuit as the interface between the piezoelectric device and electric load, i.e., the power electronic interface should be capable of four-quadrant operation. In Yiming Liu’s thesis, a half bridge inverter was proposed for this purpose, but it requires both positive and negative power supply to provide the bus voltage, which is not practical when designing a standalone circuit. Thus the
full-bridge inverter is chosen as the core of the active energy harvesting circuit, which is shown in Fig 2.6.

![Diagram of full-bridge inverter](image)

**Figure 2.6.** Bidirectional full-bridge DC-DC inverter

In order to reach the electrical boundary condition, we will consider the following cycle, which is already characterized in Fig 2.5, and calculate the net electrical energy flow at each stage of the cycle.

Stage 1: Voltage is kept constant at $V_{\text{max}}$ while force changes from $F_{\text{max}}$ to $F_{\text{min}}$

$$W_1 = -d(F_{\text{max}} - F_{\text{min}})V_{\text{max}} \quad (2.14)$$

Stage 2: Voltage is changed from $V_{\text{max}}$ to $V_{\text{min}}$ while force is at $F_{\text{min}}$

$$W_2 = -\frac{1}{2}CV_{\text{max}}^2 + \frac{1}{2}CV_{\text{min}}^2 \quad (2.15)$$

Stage 3: Voltage is kept constant at $V_{\text{min}}$ while force changes from $F_{\text{min}}$ to $F_{\text{max}}$

$$W_3 = d(F_{\text{max}} - F_{\text{min}})V_{\text{min}} \quad (2.16)$$

Stage 4: Voltage is changed from $V_{\text{min}}$ to $V_{\text{max}}$ while force is at $F_{\text{max}}$. 

$$W_4 = \frac{1}{2}CV_{\text{max}}^2 - \frac{1}{2}CV_{\text{min}}^2 \quad (2.17)$$
where \( V_{\text{max}} \) and \( V_{\text{min}} \) are the maximum and minimum voltage across the piezoelectric device, \( F_{\text{max}} \) and \( F_{\text{min}} \) are the maximum and minimum force applied to the device, \( C \) is the piezoelectric capacitance, and \( W_i \) is the amount of energy flowed from or out of the piezoelectric device.

Considering the case when \( V_{\text{min}} < 0; V_{\text{max}} > 0 \), total output energy is therefore,

\[
W_{\text{out}} = d(F_{\text{max}} - F_{\text{min}})(V_{\text{max}} - V_{\text{min}}) + \frac{1}{2}C(V_{\text{max}}^2 + V_{\text{min}}^2) \tag{2.18}
\]

And the total input energy is,

\[
W_{\text{in}} = \frac{1}{2}C(V_{\text{max}}^2 + V_{\text{min}}^2) \tag{2.19}
\]

If we take the efficiency of the interface circuit into account and assume \( V_{\text{max}} = -V_{\text{min}} = \frac{1}{2}V_L \) and \( F_L = F_{\text{max}} - F_{\text{min}} \), the net harvested power is then,

\[
W_{\text{net}} = \eta W_{\text{out}} - \frac{1}{\eta} W_{\text{in}} \\
= \eta d(F_{\text{max}} - F_{\text{min}})(V_{\text{max}} - V_{\text{min}}) - \frac{1}{2}C(\frac{1}{\eta} - \eta)(V_{\text{max}}^2 + V_{\text{min}}^2) \tag{2.20}
\]

\[
= \eta dV_L F_L - \frac{1}{4}(\frac{1}{\eta} - \eta)V_L^2
\]

It can be proved that the energy harvesting is maximized when

\[
V_L = 2\frac{\eta^2}{1 - \eta^2} \frac{dF_L}{C} = 2\frac{\eta^2}{1 - \eta^2} V_{\text{OC}} \tag{2.21}
\]

Under this condition, the maximum net harvested energy becomes,

\[
W_{\text{net}} = \left( \frac{\eta^3}{1 - \eta^2} \right) CV_{\text{OC}}^2 \tag{2.22}
\]

From this expression, it is worth noticing that the efficiency \( \eta \) of the power electronic interface plays a very important role in the performance of the active energy harvesting. The ratio of active to passive energy harvesting is shown in Fig 2.7. Thus the design of active circuitry will be focused mostly on the efficiency of the power electronic interface.
Inspection of this expression reveals that the net energy can be optimized through appropriate choice of $V_L$. This optimal value is given by:

$$p = \frac{L_0 V_{VW}}{V_{VW}} \frac{L_0}{V_{VW}} \frac{L_0}{V_{VW}} \frac{L_0}{V_{VW}} \frac{L_0}{V_{VW}}$$

(19)

At this voltage level, the maximum energy harvested is given by

$$W_{max} = \frac{21F_{ac}}{V_{VW}} \frac{L_0}{V_{VW}} \frac{L_0}{V_{VW}} \frac{L_0}{V_{VW}} \frac{L_0}{V_{VW}} \frac{L_0}{V_{VW}}$$

(20)

The above function is very sensitive to the power electronic efficiency, especially when it is high, as shown in Figure 8 where the energy harvested is compared to that of the diode rectifier circuit. We note that the expression for the rectifier circuit does not take into account the efficiency of the rectifier, and hence these results are conservative. A detailed derivation of Eq. (20) is provided in an Appendix. The efficiency of power electronic converters often varies from 70% to as high as 95%.

- **Figure 2.7.** The ratio of Active to passive energy harvesting

The corresponding waveform of the voltage and the force is shown in Fig 2.8. where $F(t)$ is the sinusoidal mechanical force applied to the piezoelectric device, $V(t)$ and $I(t)$ are piezoelectric voltage and current respectively, and $P(t)$ is the power generated by the piezoelectric device. Positive $P(t)$ indicates that the power is flowing from the piezoelectric device to the electric load, and negative $P(t)$ indicates that the power is flowing into the piezoelectric device.
Figure 2.8. Active energy harvesting waveforms
Flyback-based Passive Interface
Analysis and Design

In the original publications by Ottman, et. al. [6], passive energy harvesting was achieved with a step-down converter. The step-down converter has superior performance when the input voltage is larger than the output voltage, but it does not function when the input voltage is lower than the output; moreover, if the input voltage is much higher than the output voltage, the efficiency of the step-down converter suffers. Thus, another DC-DC converter topology without such problems is desired. The transformer-isolated flyback converter is credited for its small component count and simpler control algorithm, and the power switch for the flyback converter is on the lower side of the circuit, which yields great simplification of the gate driver circuit. The passive energy harvesting interface based on flyback converter (without controller) is shown in Fig 3.1.

3.1 Steady-state Model of Flyback under Discontinuous Conduction Mode

In most cases, the power levels associated with energy harvesting is extremely low; hence the power electronic interface is required to be designed in a low-power manner. The discontinuous conduction mode (DCM) of the switched DC-DC converter is reputed for its low power performance[11] [12] [13] [14]. However, the
input and output relationship of the voltage and current is different than that of continuous conduction mode. The flyback converter can be analyzed by the

model shown in Fig 3.2. When transistor $T$ conducts, energy from the dc source $V_{in}$ is stored in the magnetizing inductance $L$ of the transformer. When the diode $D$ conducts, this stored energy is transferred to the load, with the inductor voltage and current scaled according to the turns ratio $n:1$. During subinterval 1, while
transistor $T$ conducts, the converter circuit model reduces to Fig 3.3(left). The inductor voltage $v_L$, capacitor current $i_C$, and the dc source current $i_{in}$ are given by,

$$v_L = V_{in}$$
$$i_C = -\frac{V_{out}}{R}$$
$$i_{in} = i_L$$

(3.1)

During subinterval 2, the transistor $T$ is in the off-state, and the diode conducts, the converter circuit model then reduces to Fig 3.3(right), the inductor voltage $v_L$, capacitor current $i_C$, and the dc source current $i_{in}$ are given by,

$$v_L = -nV_{out}$$
$$i_C = ni_L - \frac{V_{out}}{R}$$
$$i_{in} = 0$$

(3.2)

The current flow through the inductor $L$ and diode $D$ are sketched in Fig 3.4. The

Figure 3.4. Flyback waveform under DCM condition
principle of volt-second balance to the primary-side magnetizing inductance yields

\[
<v_L> = DV_{in} + \Delta_1(-nV_{out}) + \Delta_2(0) = 0
\]  
(3.3)

The input-output voltage relationship is then

\[
<V_{out}> = \frac{D}{n\Delta_1} V_{in}
\]  
(3.4)

By applying the principle of charge balance to the output capacitor, since there is no DC capacitor current, in this case the average output current is supplied by the diode current in one circle, which yields,

\[
<i_{out}> = <i_D> = \frac{1}{T_s} \int_0^{T_s} i_D(t)dt = \frac{V_{in}D\Delta_1 T_s}{2L} = \frac{V_{out}}{R}
\]  
(3.5)

### 3.2 Optimized Energy Harvesting Circuit under DCM Condition

The maximum power transfer theory developed for the piezoelectric element-rectifier circuit produced an expression for the optimal rectifier voltage \(V_{rect}\). The following analysis reveals that the power flow from the piezoelectric element is maximized at a constant duty cycle and, as it departs from this optimal value, the output power drops significantly. From equation (3.4) and (3.5), the output current expression is then,

\[
I_{out} = \frac{V_{in}^2 D^2 T_s}{2V_{out} n L}
\]  
(3.6)

By conservation of power for the converter (assuming losses are minimal), the output current can be expressed as a function of the input voltage and current and output voltage

\[
I_{out}V_{out} = I_{in}V_{in}
\]  
(3.7)
The input current of the converter can now be determined by equating (3.6) and (3.7),

\[ I_{in} = \frac{V_{in}D^2}{2nL_f} \]  

(3.8)

It is worth noticing that the effective input resistance of the flyback converter under DCM condition can also be determined by

\[ R_{in} = \frac{2nL_f}{D^2} \]  

(3.9)

Substituting the output current of the piezoelectric device as the input current to the converter, which is equation (2.11), and the rectifier capacitor voltage as the voltage into the converter, equation (3.8) becomes

\[ \frac{2I_p\pi}{\pi} - \frac{2V_{rect}\omega C}{\pi} = \frac{V_{in}D^2}{2nL_f} \]  

(3.10)

Solving equation (3.10), the rectifier voltage

\[ V_{rect} = \frac{I_p}{\omega C} - \frac{\pi V_{in}D^2}{4nL\omega f_s C} \]  

(3.11)

Power produced by the piezoelectric element as regulated by the converter can now be expressed as the product of the rectifier voltage (converter input voltage) and the input current

\[ P_{in} = V_{rect}I_{in} = \left( \frac{I_p}{\omega C} - \frac{\pi V_{in}D^2}{4nL\omega f_s C} \right) \frac{V_{in}D^2}{2nL_f} \]  

(3.12)

The rectifier voltage and power flow from the piezoelectric element as regulated by the flyback converter for any excitation level, as specified by the magnitude of polarization current \( I_p \), can now be determined. For this circuit, the maximization of the power flow from the piezoelectric element is considered as a function of the flyback converter’s duty cycle. Solving equation (3.10) for the duty cycle \( D \), we have

\[ D = \sqrt{\left( \frac{2I_p}{\pi} - \frac{2V_{rect}\omega C}{\pi} \right) \frac{2nL_f}{V_{rect}}} \]  

(3.13)

At peak power, the piezoelectric polarization current can be found as a function
of the optimal rectifier voltage from (2.13), substituting into (3.12), the optimal
duty cycle which results in maximum power can be determined as

\[
D_{\text{optimal}} = \sqrt{\frac{4nL\omega C}{\pi}f_s}
\]  

(3.14)

Thus in this case, the optimized constant duty cycle rather than adaptive control
will greatly reduce the complexity and power loss of the power electronic interface.
Moreover, unlike the step-down converter, the optimal duty cycle of the flyback
converter does not depend on the output voltage, so that it is valid for a wide
range of excitation.

### 3.3 Gate Driver and Duty Cycle Generator

Another attractive advantage of the flyback DC-DC converter is that its switching
device is located on the lower side of the transformer without floating ground,
so it greatly reduce the additional power loss and circuit components associated
with an isolation gate driver circuit. Unlike more conventional power electronic
circuits, the selection of a MOSFET in the ultra-low power application is extremely
dependent upon some parameters; i.e., switch-on resistance \( R_{\text{on}} \) and gate charge \( Q_g \). Considering the high-voltage and low current case, especially when using
PVDF as a piezoelectric device, the MOSFET should satisfy the peak voltage
requirement and in the meanwhile minimize the power losses such as conduction
loss and switching loss. The MOSFET gate is modeled as shown in Fig 3.5.

The function of the gate driver is essentially charging and discharging the ca-
cpacitance \( C_g \) associated with the gate. In order to reduce the gate driver losses,
we need to reduce driving voltage and operating switching frequency of the MOS-
FET. Based on those requirements, the MOSFET should be chosen with smallest
gate \( Q_g \) and threshold voltage \( V_{\text{th}} \), and the gate driver should provide enough
current to satisfy the speed requirement for the circuit associated with the gate
capacitance. Unlike the regular power MOSFET with a large gate capacitance,
we choose ZVN3320F provided by IXYS as the candidate, which is rated at 200V
and 60mA as well as a very small gate capacitance (45pF). After calculation, it
Isolated gate drive signal

Figure 3.5. Equivalent Gate Circuit

requires less than 20mA of gate driver current when working at a 5kHz switching frequency. It worth noticing that most operational amplifiers and logic chips are capable of 30~50mA driving current, thus a gate driver circuit can be omitted in this application.

In order to maximize overall efficiency of the standalone circuit, a low-power pulse-width modulator circuit was designed, and is shown in Fig 3.6. Assuming the comparator is powered by a single DC source $V_C$ and ground, which means the comparator output will be either $V_C$ or 0. The threshold voltage of the comparator is determined by the combination of resistor $R_1$, $R_2$ and $R_3$. When the output is 0V, the threshold voltage $V_+$ is

$$V_+ = \frac{R_2||R_3}{R_1 + R_2||R_3} V_C$$

(3.15)

When the output is $V_C$, then the threshold voltage is

$$V_{+2} = \frac{R_2}{R_1 + R_2||R_3} V_C$$

(3.16)

Assume the initial conditions of the capacitor are $V_{C_t} = 0$, which yields $V_{out} = V_C$. Thus the transistor $Q$ is off, the capacitor $C_t$ is charging by through resistor $R_1$. 

and $R_w$, and the time constant is $\tau_1 = (R_T + R_w)C_T$. When the voltage of the capacitor exceeds the value $V_+ = V_{+2}$, the output voltage flips ($V_{out} = 0$) and the transistor $Q$ is on. Now $V_+ = V_{+1}$, and the capacitor is discharging through resistor $R_T$. Resulting waveform of this duty cycle generator is shown in Fig 3.7. Through

![Diagram](image)

**Figure 3.6.** Duty Cycle Generator

**Figure 3.7.** Duty Cycle Generator Waveform

careful design and selection of components, especially the low power comparator,
power consumption of this circuit was reduced to 200µW. The component list is shown in Tab 3.1.

Table 3.1. Gate Driver: Component list

<table>
<thead>
<tr>
<th></th>
<th>MFG.</th>
<th>Part Number/Value</th>
<th>Count</th>
</tr>
</thead>
<tbody>
<tr>
<td>Resistor</td>
<td>Yageo</td>
<td>several</td>
<td>5</td>
</tr>
<tr>
<td>Capacitor</td>
<td>Kemet</td>
<td>0.1μF, 16V, 5%, CER</td>
<td>1</td>
</tr>
<tr>
<td>Transistor</td>
<td>NXP Semiconductors</td>
<td>NPN PDTC115ET</td>
<td>1</td>
</tr>
<tr>
<td>Comparator</td>
<td>STMicroelectronics</td>
<td>TS3021</td>
<td>1</td>
</tr>
</tbody>
</table>
Active Energy Harvesting Interface Design

As discussed in Chapter 2, the active technique is more complicated than that of passive techniques. It requires several additional circuits to operate, such as a full-bridge inverter and a bus voltage regulator, which will be discussed in detail in this chapter.

4.1 Standalone Active Circuit Design

4.1.1 Active Core Circuit

The proposed standalone circuit is powered by a single or series of rechargeable batteries without any external power supplies. The core circuit of the active technique is composed of a bidirectional full-bridge inverter as the interface between the piezoelectric device and high-voltage bus, a bus capacitor that serves as the temporary energy storage and an unidirectional DC-DC converter functioning as the bus voltage regulator. The overall system is shown in Fig 4.1.

Assume zero voltage initial condition of the bus capacitor, all MOSFETs of the full-bridge inverter are off, in this case, the bus capacitor is charged up by the body diodes of the MOSFET, which act as the full bridge rectifier. When the voltage of the bus capacitor reaches some certain level, the full-bridge inverter and the flyback converter are engaged to perform the active energy harvesting.
4.1.2 Isolated gate driver circuit design

In many power supply designs, the high-side switches are driven by an integrated gate driver IC along with isolated power supply or bootstrap circuit. However, commercially available power supplies consume significant power compared to the energy harvesting power levels. Furthermore, the application of a bootstrap circuit is ineffective at extremely low duty cycles, which are required to reduce the power loss of the MOSFET.

Therefore designing another low power, high voltage, isolated gate driver is necessary for active energy harvesting. The proposed gate driver circuit is shown in Fig 4.2, the component information is listed in Tab 4.3.

Table 4.1. Gate Driver: Component list

<table>
<thead>
<tr>
<th>Part</th>
<th>MFG.</th>
<th>Part Number/Values</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_1, R_3$</td>
<td>Yageo</td>
<td>1%,10k$\Omega$</td>
</tr>
<tr>
<td>$R_2, R_4$</td>
<td>Yageo</td>
<td>1%,10$\Omega$</td>
</tr>
<tr>
<td>$C_1, C_2$</td>
<td>Kemet</td>
<td>.01$\mu F$, 50V, 5%, CER</td>
</tr>
<tr>
<td>$Q_1 \sim Q_4$</td>
<td>IXYS</td>
<td>IXTU01N100</td>
</tr>
<tr>
<td>$T_1, T_2$</td>
<td>Coilcraft</td>
<td>FA2659-AL</td>
</tr>
<tr>
<td>$D_1 \sim D_8$</td>
<td>ON Semiconductor</td>
<td>1N5818</td>
</tr>
</tbody>
</table>

The pulse-transformers $T_1, T_2$ (refer to Tab 4.2) are used to provide high voltage isolation. Since the transformer cannot sustain a DC voltage component, the
blocking capacitors $C_1, C_2$ are placed before the primary side of the transformer so that no DC current will flow into the transformer windings. On the secondary side of the transformer, the diode rectifier changes the AC voltage to a DC voltage, which provide a constant $V_{gs}$ drive signal to the MOSFET. When the signal is low, the transformer stops working and the resistor in parallel with the gate provides a path for discharging the gate capacitance. It is worth noticing that all the components of the gate driver are passive; as a result, the power loss can be reduced greatly through careful design.

### Table 4.2. Pulse-Transformer: Coilcraft

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Turns ratio</th>
<th>Primary Inductance ($\mu H$)</th>
<th>Leakage Inductance ($\mu H$)</th>
<th>Volt-time product ($V \cdot \mu$sec)</th>
</tr>
</thead>
<tbody>
<tr>
<td>FA2659-AL</td>
<td>1:1</td>
<td>296</td>
<td>1.5</td>
<td>34.2</td>
</tr>
</tbody>
</table>

### 4.1.3 Dead-Time Generator

In order to protect the shoot-through between high and low side switches, the actual and simulink model of the dead-time generator is inserted as shown in Fig 4.3 and Fig 4.4. The dead time is provided by the $RC$ circuit and the threshold voltage of the hysteresis comparator.
Table 4.3. Gate Driver: Component list

<table>
<thead>
<tr>
<th>MFG.</th>
<th>Part Number/Value</th>
<th>Count</th>
</tr>
</thead>
<tbody>
<tr>
<td>Resistor</td>
<td>Yageo 1%,1kΩ</td>
<td>2</td>
</tr>
<tr>
<td>Diode</td>
<td>ON Semiconductor 1N5818</td>
<td>2</td>
</tr>
<tr>
<td>Capacitor</td>
<td>Kemet 0.01µF,16V,5%, CER</td>
<td>2</td>
</tr>
<tr>
<td>NOT gate</td>
<td>STMicroelectronics 74LX1G14</td>
<td>3</td>
</tr>
<tr>
<td>AND gate</td>
<td>STMicroelectronics 74LX1G08</td>
<td>2</td>
</tr>
</tbody>
</table>

Figure 4.3. Dead-Time Generator

The diode-R-C circuit at the first stage of the circuit is inserted to provide a time delay for the PWM signals. The time interval between the control signal and actual PWM signal is determined by the RC time constant, the output voltage of hysteresis NOT gate is established until the voltage of the capacitor reaches some certain value. This time delay will be the dead time in between the MOSFET switches and can be calculated as,

\[ t_{\text{dead}} = -\tau \cdot \ln \left(1 - \frac{V_{\text{th}}}{V_s}\right) \]  

where \( \tau = R \cdot C \) is the time constant of the \( RC \) pair, \( V_{\text{th}} \) is the threshold voltage of the hysteresis NOT gate, and \( V_s \) is the magnitude of the control signal. The simulation result is shown in Fig 4.5.

4.2 Loss and Power Consumption Estimation

The losses for each component of the power electronic circuit are calculated in this section and will be compared to experimental results in Chapter 5.
4.2.1 Loss of Power Electronic Circuit

The conducting state of a MOSFET is determined by the charge on its gate. To switch a semiconductor device between the on and off states, the controlling charge must be inserted and removed. The amount of power required for controlling the MOSFET is estimated in Equation (4.2).

\[
P_{gate} = f_s V_g Q_g, \quad (4.2)
\]
where $f_s$ is the switching frequency, $V_g$ is the gate driving voltage, $Q_g$ is the total gate charge of a MOSFET. Switching loss imposes an upper limit on the switching frequencies of practical converters. During the switching transitions, the transistor voltage and current are simultaneously large. In consequence, the transistor experiences high instantaneous power loss. The switching loss of the power MOSFET is estimated as

$$P_{sw} = \frac{1}{2} f_s V_{DS} I_D (t_r + t_f),$$

(4.3)

where $f_s$ is the switching frequency, $V_{DS}$ is the drain to source voltage of the device when off, $I_D$ is the current flow through the drain-source of the MOSFET when on, and $t_r, t_f$ are the voltage rise and fall time.

Conduction loss can be separated into two parts; one is resistive heat dissipation during a switch turn-on state, the other is due to the diode forward voltage drop. The on-state conduction loss of the power MOSFET is calculated as

$$P_{con} = f_s I_D^2 R_{on} t_{on},$$

(4.4)

Where $R_{on}$ is the total resistance between the source and drain during the on state, and $t_{on}$ is the turn-on time in one cycle. The power loss due to diode forward voltage drop is calculated as,

$$P_{con} = f_s V_{DS} I_D t_d,$$

(4.5)

where $t_d$ is the diode conducting time in one cycle.

Even though it is very difficult to calculate the exact power loss of the power electronics circuit, the equations (4.2)$\sim$(4.5) are intuitive references when designing the circuit and choosing components.

The switching frequency $f_s$ should be chosen low enough to reduce the power losses, which in turn, increase the core efficiency of the full-bridge inverter, but we also need to take the fundamental frequency of the piezoelectric device into account such that $f_s$ is high enough comparing to the fundamental frequency. The MOSFETs of the full-bridge inverter are key components that will affect the performance of the active energy harvesting; besides satisfying the voltage and
current rating, the parameters such as gate charge \( Q_g \), rise and fall time \( t_r, t_f \) and etc. are also critical. From equation (4.2), the energy required to turn on and turn off the MOSFET in a cycle is proportional to the control voltage \( V_g \) and the gate charge \( Q_g \). Thus a MOSFET with lower threshold voltage and smaller turn-on gate charge will be a better choice in this application. Besides, it is simpler to design a gate drive circuit by using a MOSFET with low gate charge, as discussed in Section 4.1.2.

### 4.2.2 Power Consumption of the Supporting Circuits

The objective of the supporting circuit is to perform the active energy harvesting under ultra-low power consumption condition.

**Gate Driver Circuit**

From Fig 4.2, all components of the gate driver circuit are passive. Thus the controller circuit is also responsible for providing power to the gate driver circuit besides the control signals.

The power required to drive high side MOSFETs is calculated as,

\[
P_h = \frac{2}{\eta_T} f_s Q_g V_g + \frac{V_g^2}{2 R_1}
\]

(4.6)

where \( \eta_T \) is the efficiency of the pulse-transformer

**Controller Circuit**

From Fig 4.3, the power required for the gate driver circuit is provided by the AND gate chip. As discussed in Section 3.3, the logic gate chip will provide enough power if the gate charge of the MOSFET is small enough. Therefore, the power required for controller circuits will be consist of the power consumption of the logic chips, the power required by gate driver circuit, and the power required by the duty cycle generator.

Assuming the switching frequency is at 5kHz, the universal supply voltage is 5V, the MOSFET is chosen as IXTY01N100 with 6.9nF total gate capacitance, and the parameters listed in Table 4.3. The estimated power requirement for the
standalone circuit was calculated in following part.

\[ P_{Cg} = 4 f_s Q_g V_g = 4 \times 5 \times 10^3 \times 6.9 \times 10^{-9} = 0.69 mW \]  

(4.7)

The power dissipated in the gate driver circuit composed of two parts, which are the power required by the parallel capacitor and dissipated on the parallel resistor, assuming the efficiency of the pulse-transformer is 85%:

\[ P_{Gate} = \frac{1}{\eta} \left( nCV_g^2 + \frac{V_g^2}{R} \right) = \frac{1}{85\%} \left( 2 \times 0.01 \times 10^{-6} \times 25 + \frac{25}{100 \times 10^3} \right) = 0.295 mW \]  

(4.8)

The power consumption of the logic chips was calculated as,

\[ P_{logic} = n \times V_{cc} \times I_{cc} = 5 \times 5 \times 10^{-6} = 0.025 mW \]  

(4.9)

As mentioned in Section 3.3, the power consumption of the duty cycle generator was 0.2mW. The total power requirement for the standalone circuit is:

\[ P_{total} = P_{Cg} + P_{Gate} + P_{logic} + P_{generator} = 0.69 + 0.295 + 0.025 + 0.2 = 1.21 mW \]  

(4.10)
Chapter 5

Experimental Results

This chapter first presents an experimental comparison between passive and active energy harvesting. The experimental results are also compared with the theoretical modeling developed in the previous chapter. Then, the performance of the standalone active energy harvesting circuit is presented based on same experimental platform.

5.1 Experiment Platform Configuration

5.1.1 Mechanical Excitation/Testing System

A computer-programmable material testing system (MTS Systems Corporation’s Instron 1331) is used in the following experiment to apply a sinusoidal force or displacement to a piezoelectric device. The mechanical setup is shown in Fig 5.1. A load cell measures the applied force and provides a feedback signal to the system computer so that the applied force is well-regulated. Soft plastic bars are used as sample holders for their high electrical insulation abilities. Below the device a universal joint was inserted beneath the sample holder to achieve a uniform pressure on the device. In order to satisfy the quasi-static assumption, the mechanical force frequency was set to 5 Hz, low enough that no resonance is excited in the device.
5.1.2 Piezoelectric Material Configuration

In the experiment presented in this paper, a commercial PVDF film (from Measurement Specialties, Inc.) was used for the piezoelectric material. The thickness of the material used was 24µm. The film was uniaxially stretched and corona-poled by the manufacturer. The properties of this film are provided in Table 5.1. This material has been demonstrated to withstand high strain (3%) without degrading the piezoelectric responses under quasi-static conditions[15].

Table 5.1. PVDF parameters

<table>
<thead>
<tr>
<th>24µm PVDF</th>
<th>$d_{31}(pC/N)$</th>
<th>$\epsilon_{33}(\epsilon_0)$</th>
<th>$Y(GPa)$</th>
<th>$k_{31}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>21</td>
<td>11.6</td>
<td>2.9</td>
<td>0.11</td>
<td></td>
</tr>
</tbody>
</table>

The PVDF film was then cut into rectangular pieces of 25cm x 4.2cm, with the long dimension (25cm) along the film stretching direction. Large area aluminum electrodes were deposited by a Semicore® e-beam evaporator on both sides with an effective area of 20 cm x 4 cm. In order to make the electrodes adhere well to the polymer film, the film surface was cleaned with IPA in a clean-room environment before Al was deposited. Since it is difficult to make large-volume piezoelectric
devices using a single-layer film, multilayer films were made to fabricate the piezoelectric device. There is another advantage to using multilayer piezoelectric films instead of single layer film, as this increases the total capacitance and piezoelectric constant of the device while maintaining the same open-circuit output voltage as a single-layer film. After aluminum electrodes were deposited, the films were bound together using INSULGEL® 50 soft epoxy gel. Because this gel is very soft even after it is cured, the clamping effect from the epoxy layer during vibration will be very small and can be neglected. The electrodes of different layers were connected and bound with conductive wire and silver glue. Due to the internal polarization direction of PVDF, improper connections among the electrodes of multilayer films may degrade the output voltage and power. Before the films were bound together, each film polarization was checked by using a d33 meter, and the polarization direction was marked on the margin place of each film. All the electrodes were electrically connected as positive to positive, negative to negative. In order to make it convenient during testing, the lead electrodes were arranged at the same end of the film. The Al electrodes were deposited as shown in Fig 5.2. Two types of electrodes were made during deposition. These structures make it easy to bind the positive to positive and negative to negative, and to put the same-polarity electrodes at the same side of the films.

Figure 5.2. (a) electrodes shape [top view] (b) multilayer films [cross section view].
5.1.3 Active Interface Verification using dSpace 1104 microcontroller

The test setup for the full-bridge inverter is shown in Fig 5.3. The bus voltage is regulated by an external high voltage power supply. Since the power supply does not allow current flowing back into itself, a load resistor $R_{\text{load}}$ is placed in parallel such that it is powered both by energy harvesting circuit and the power supply. By measuring the current flowing through both from the load resistor and the power supply, it is straightforward to calculate the power harvested by the piezoelectric device with Equation (5.1).

$$P_{\text{harvested}} = \left( \frac{V_{\text{sense1}}}{R_{\text{sense1}}} \right)^2 \times \left( R_{\text{load}} + R_{\text{sense1}} \right) - V \times \frac{V_{\text{sense2}}}{R_{\text{sense2}}}$$  \hspace{1cm} (5.1)

![Figure 5.3. Active System with dSpace 1104 microcontroller](image)

The operation of the active circuit is quite simple, as shown in Fig 2.8; the operations of the active techniques are discussed in Chapter 2. When the force/stress reaches its maxima, switch $Q_1$ closes and switch $Q_4$ is modulated at a constant duty cycle, while switches $Q_2$ and $Q_3$ are open; when the force/stress reaches its minima, switch $Q_2$ is closed, switch $Q_3$ is modulated at a constant duty cycle, while switches $Q_1$ and $Q_4$ are open. It is worth noticing that the power flow is bidirectional under such operations, i.e., the current flows either from the piezo-
electric device, or out of the piezoelectric device.

The active controller is implemented using a dSpace® DS1104 controller board. The board includes a Texas Instruments TMS320C32 floating-point digital signal processor (DSP), analog-to-digital (ADC) converters for sampling measurements, and pulse-width modulated (PWM) signal outputs for controlling the converter. The control algorithm was developed in MATLAB using the graphical interface Simulink and dSpace 1104 microcontroller to generate the controller code for the DSP. The controller composed of four major parts, as shown in Fig 5.4. First, an analog/digital converter was implemented which was used to measure the force or current across the piezoelectric device. The force signal, however, was fairly noisy. If the signal is directly used by the controller, the applied voltage is poorly synchronized with the mechanical force. Adding a digital or analog filter might alleviate the signal to noise ratio. Unfortunately, filters usually introduce undesirable phase shift. To solve this problem a Phase-Locked Loop (PLL) is implanted in the Simulink code. It generates an ideal sinusoidal signal in phase with the applied force, and it is then used for the controller. The phase requirement of active energy harvesting as described in previous chapters is to charge or discharge at the applied peak force. The experiment result will be shown in chapter 5.

Figure 5.4. Simulink Diagram of Active Technique
5.2 Experimental Results

5.2.1 Discontinued-Conducting-Mode Flyback Converter

Experimental data were taken to validate the passive energy harvesting approach presented in Chapter 2 and to demonstrate the operation of the energy harvesting circuitry. The flyback converter is chosen for the passive energy harvesting, as shown in Fig 3.1. The switch in the converter is a ZVN3320F N-Channel MOSFET provided by ZETEX, which is rated at 200V and 60mA. In order to reduce the switching losses, the switching frequency is set to $f_s = 2\text{kHz}$, and, as mentioned before, the mechanical excitation is set to $f = 5\text{Hz}$.

For comparison purposes, several mechanical excitation conditions were used. The design of flyback transformer parameters follows the optimized condition expressed in Chapter 2, equivalent inductance $L = 2mH$, turns ratio $n = \frac{N_p}{N_s} = 10$. Under those conditions, the optimized duty cycle is calculated as

$$D_{opt} = \sqrt{\frac{n\omega CLf_s}{\pi}} \approx 1.75\% \quad (5.2)$$

The purpose of the first experiment is to verify the optimized duty cycles under two different strain level. The input impedance of the flyback converter under different duty cycle is shown in Fig 5.5. The dashed line indicates the impedance of the piezoelectric device, the experiment result of the input impedance cross the dashed line when the duty cycle is around 1.75%, which validates the theoretical analysis. Moreover, the corresponding voltage conditions are shown in Fig 5.6. The dashed line is one half of the open circuit voltage when the strain is at 1.34%, and the dot-dashed line is one half of the open circuit voltage when the strain is at 0.81%. It is obvious that the rectified voltages reach their optimal value when the duty cycle is around 1.75%. Under the optimal condition, the net power harvested is shown in Fig 5.7. Both of the power maxima under two different strain level occur when the duty cycle is set between 1.7% and 1.8%.

The second experiment is to evaluate the performance of the flyback converter
under constant duty cycle, i.e. 1.75%. The net power harvested by the passive method under different strain levels is shown in Fig 5.9; the associated voltage condition of the piezoelectric device is shown in Fig 5.8. The available power is measured by using a matching resistor as the electric load. Recalling the optimized passive condition in Chapter 2, the maximum power generated under sinusoidal
mechanical excitation occurs when the rectified voltage is one half of the open circuit voltage, i.e., $V_{rect} = \frac{1}{2} \times V_{OC}$. It can be concluded that the optimized passive approach using a flyback converter is valid over a wide range of strain levels.
5.2.2 Bidirectional Full-Bridge Inverter for Active Energy Harvesting

In this section, we focus on evaluating the performance of the bidirectional full-bridge inverter. In order to test the inverter, a dSpace® 1104 controller card was used to implement the active control technique and provide pulse-with modulated control signals to the MOSFET gate drivers of the full-bridge converter. The power for the gate drive and control system is not included in the power path.

In order to further reduce switching losses, which will significantly reduce the performance of the active approach, the controller pulse-width modulates four MOSFETs independently, depending upon whether the voltage across the device is being increased or decreased. The MOSFET used in the full-bridge is IXTY01N100 provided by IXYS, each rated at 1000V and 100mA. In order to determine the active control activities during charging and discharging transients, a high voltage differential probe Tektronix P5200 was used to measure the voltage across the piezoelectric device, and a current probe AM 503B provided by Tektronix was used to monitor the piezoelectric current. All the signals were fed into Tektronix TDS 754D oscilloscope and the data was then imported into Matlab. For the first

<table>
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<th>Table 5.2. Instrument List</th>
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<tr>
<td>MFG.</td>
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<tr>
<td>Oscilloscope</td>
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<tr>
<td>Current Probe</td>
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<tr>
<td>Voltage Probe</td>
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<td>Microcontroller</td>
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series of tests a single-layer device was used. This device was mechanically excited so that it experienced an effective strain of 0.7%. The voltage across the device was controlled by the full-bridge inverter to transition between ±25V. The lower switches of the inverter were pulse-width-modulated at a switching frequency of 50kHz and a duty cycle of approximately 5%. The resulting measured piezoelectric voltage and current are shown in Fig 5.10. It should be noted that the charging and discharging current of the device cannot be seen in this data, due to the sampling frequency of the oscilloscope and the high-frequency nature of the current during charging and discharging. Fig 5.11 shows the current through the device at a
time scale corresponding to the pulse-width modulation of the lower MOSFETs. The gate-source voltage of the corresponding lower MOSFET is also shown (the MOSFET is on when this voltage is 15V, and is off when this voltage is 0V). Inspection of Fig 5.10 shows that the voltage and current waveforms tend to have the same sign, resulting in positive (i.e., harvested) power flow.

For the next series of experiments a four-layer PVDF device was used. The switching frequency of the inverter was changed to 5 kHz, and a duty cycle of 1% was applied to the low-side MOSFETs during the voltage transitions. The average harvested power was then determined by subtracting the power provided by the DC voltage source from the power dissipated by the DC load resistance $R_{\text{load}}$. It should be noted that, in these experiments, the power for the gate drive and control system is not included when calculating harvested energy. The power that flows from the gate driver circuitry to the inverter is only used to charge the gate capacitances of the MOSFETs, and so will not be added to the power harvested. Fig 5.12 shows the results of this harvested power as a function of the DC bus voltage for an effective mechanical strain of 0.81%. As predicted by theory, it is seen that an optimal bus voltage exists that maximizes the power harvested.

The performance of the active energy harvesting approach as a function of effective mechanical strain is shown in Fig 5.13, where it is compared to the power extracted by a passive diode rectifier circuit operating at its optimal output voltage, and to the resulting power from the diode rectifier circuit after being converted by a DC-DC converter to a desired output voltage of 1-2V. For the active data, the bus voltage was manually adjusted to its optimal value. As can be seen in the figure, the maximum power harvested by the active approach is up to 5 times higher than that with the passive approach. Based upon the chart provided in Fig 2.7, this suggests the efficiency of the full-bridge inverter circuit is approximately 78%.

In this section, we validated the full-bridge inverter for active energy harvesting without considering the power consumption of the supporting circuits which was huge. In the end, the performance of standalone circuit with ultra-low power consumption is evaluated with the circuits discussed in Chapter 4. Since the components of the full-Bridge inverter remained the same, the performance of the active energy harvesting also remained the same as shown in Fig 5.13.
The overall power consumption of the standalone circuit was measured by inserting a 33Ω current sensing resistor in series with the supply voltage. The DC voltage drop on the resistor was measured to be $V_{\text{drop}} = 9.31 \text{mV}$, thus the power consumption is calculated as

$$P_{\text{oval}} = \frac{V_{\text{drop}}}{R_{\text{sensing}}} \times V_{\text{supply}} = \frac{9.31}{33} \times 5 = 1.41 \text{mW}$$

The experimental result of the standalone circuit power consumption was very close to the estimation in Equation 4.10, which is 1.21mW.
Figure 5.9. Output Power v.s. Strain under 1.75% constant duty cycle
The active controller is implemented using a dSpace DS1104 controller board. The board includes a Texas Instruments TMS320C32 floating-point digital signal processor (DSP), analog-to-digital (ADC) converters for sampling measurements, and pulse-width modulated (PWM) signal outputs for controlling the converter. The control algorithm was developed in MATLAB using the graphical interface Simulink and the Real-Time Workshop to generate the controller code for the DSP. The controller is composed of four major parts, as shown in Figure 11.

First, an analog/digital converter is implemented which is used to sample the measured displacement of the piezoelectric device (provided by the materials testing system). This measured displacement is then fed into a phase-locked loop, which is used to generate a pure sinusoidal waveform in phase with the sampled displacement. This signal is then fed into a peak detector, which activates a PWM signal generator to enable a voltage transition across the piezoelectric device. In order to reduce switching losses, which can significantly reduce the performance of the active approach, the controller pulse-width modulates only one of the low-side MOSFETs at a time, depending upon whether the voltage across the device is being increased or decreased. The corresponding upper switch is only closed when the piezoelectric capacitance is being charged; otherwise, both of the upper switches are open. A high-impedance isolated voltage probe was used to measure the voltage across the piezoelectric device, and a Tektronix AM503B current probe was used to measure the terminal current of the device. Thirty turns of magnetic wire were wrapped through the current probe to improve the resolution of the current measurement. These probes were connected to a Tektronics TDS 754D oscilloscope.

For the first series of tests a single layer of device was used. This device was mechanically excited so that it experienced an effective strain of 0.7%. The voltage across the device was controlled by the full-bridge inverter to transition between ±25V. The lower switches of the inverter were pulse-width-modulated at a switching frequency of 50kHz and a duty cycle of approximately 5%. The resulting measured piezoelectric voltage and current are shown in Figure 12. It should be noted that the charging and discharging current of the device cannot be seen in this data, due to the sampling frequency of the oscilloscope and the high-frequency nature of the current during charging and discharging. Figure 13 shows the current through the device at a time scale corresponding to the pulse-width modulation of the lower MOSFETs. The gate-source voltage of the corresponding lower MOSFET is also shown (the MOSFET is "on" when this voltage is 15V, and is "off" when this voltage is 0V). Inspection of Figure 12 shows that the voltage and current waveforms tend to have the same sign, resulting in positive (i.e., harvested) power flow.

Figure 5.10. Energy harvesting experiment with single-layer PVDF device excited mechanically at a frequency of 5Hz and with an effective strain of 0.7%. Top: Measured voltage across piezoelectric device. Bottom: Measured current through piezoelectric device.
Figure 5.11. Energy harvesting experiment with single-layer PVDF device excited mechanically at a frequency of 5Hz and with an effective strain of 0.7%. Top: Measured voltage across piezoelectric device. Bottom: Measured current through piezoelectric device.

Figure 5.12. Harvested electric power as function of DC bus voltage for mechanical excitation of 0.81% effective strain
Figure 5.13. Harvested electrical power as a function of effective mechanical strain, active approach compared to passive diode rectifier, and passive diode rectifier with DC/DC converter
Chapter 6

Conclusions and Future Work

Throughout this thesis, two approaches have been discussed and compared. An optimized standalone passive approach using a flyback converter is developed, and the active energy harvesting method is demonstrated by using both the dSpace controller and partial standalone circuit. The passive energy harvesting with a flyback converter is capable of very high efficiency and standalone configuration, but it could only harvest a small amount of available power inherent in the piezoelectric devices. The active energy harvesting circuit controls the piezoelectric voltage, so that more power can be harvested by this approach.

As detailed theoretical analysis and experiment have shown, the performance of the active energy harvesting depends on three aspects. First, the smart PVDF materials and the configuration of the device significantly increases the energy harvesting potential. The efficiency of the full-bridge inverter plays a very important role in the power harvesting level, and the standalone supporting circuit must have low power consumption.

As the power consumption of the standalone circuit was not negligible when the strain level was low, more efficient approaches should be investigated in the future. The multilayer configuration of the device was proven to be a better approach compared to the single layer configuration, thus, multilayer devices with more layers will be developed in the near future.
Bibliography


