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ENGINEERED THIN FILMS OF PARYLENE C AS ELECTRICAL INSULATORS FOR FLEXIBLE ELECTRONICS

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Abstract

The use of a single material as a multifunctional insulator (i.e., substrate, gate dielectric, interlayer dielectric, and passivation layer) in the same device will reduce the cost and improve the sustainability of flexible devices. The major goal of this dissertation was to examine the potential use of the multifunctional insulator Parylene C as a low-κ interlayer dielectric in flexible electronics. Towards this goal, columnar microfibrous thin films (μFTFs) of Parylene C were fabricated and their electrical and mechanical properties, stability, and reliability were studied. The columnar μFTFs were fabricated using a collimated flux of Parylene-C monomers directed at an angle $\chi_v \in \{30°, 52°, 60°, 67°, 80°, 90°\}$ with respect to the substrate plane in a modified vacuum chamber using oblique angle deposition. Also, bulk Parylene-C thin films were fabricated to explore the stability of bulk Parylene C as a gate dielectric in flexible electronics. The significant results of this research are the following:

- Parylene-C columnar μFTFs can be highly porous. The porosity decreases as the deposition angle χ_v increases and lies between 0.38 and 0.56. Both the static Young's modulus and the yield strength of the Parylene-C columnar μFTFs are higher in the morphologically significant plane than in the plane normal to it. In both loading directions, static Young's moduli and yield strengths are about two orders of magnitude lower for the Parylene-C columnar μFTFs than the corresponding parameters of the bulk Parylene C, making the Parylene-C columnar μFTFs softer. The lowest relative permittivity of the fabricated Parylene-C columnar μFTFs in the 1–1000 kHz frequency range is about 70% of that of the bulk Parylene C. The static Young's moduli, yield strengths, and the relative permittivity can be correlated to the porosity, crystallinity, and the deposition angle.

- The d.c. leakage current in the Parylene-C columnar μFTFs at temperatures not exceeding 100 °C (373 K) arises from the Poole–Frenkel conduction mechanism with a barrier energy of about 0.77 eV. The a.c. conduction in the Parylene-C columnar μFTFs is attributable to small-polaron-tunneling hopping conduction and depends on the frequency f as f^s, with $s \in [0.82, 0.85]$ increasing with temperature. Also, a.c. conduction in the Parylene-C columnar μFTFs is

temperature-activated with an activation energy that decreases from 0.020 to 0.012 eV as f increases from 1 to 1000 kHz.

- Before and after the application of a constant-voltage stress (CVS), room-temperature leakage current in a metal-insulator-metal (MIM) structure incorporating Parylene-C columnar μFTF as the insulator is space-charge limited. The space charge comprises defects introduced during fabrication. No new defects are induced by the CVS. Kohlrausch–Williams–Watts relaxation can be exploited to understand transient leakage-current behavior, and characteristic times in the 3.5–3.9 s range and stretch factors in the 4.2–5.2 range were determined. These parameters suggest that carrier trapping at defects and their polarization orientation are related to space-charge formation. Moreover, capacitance dependence on time and frequency is a good indicator of the CVS-induced degradation and stability. Charge buildup in the Parylene-C columnar μFTFs is accompanied by capacitance decrease with CVS duration. Extrapolation of the capacitance-decrease dependence on CVS duration indicates that the capacitance would degrade by about 20% in 10 years.

- CVS induces charges in bulk Parylene C and its interfaces with gold and Pentacene. The net induced charge is positive and negative for, respectively, negative and positive gate bias polarity during CVS. The magnitude of the charge accumulated following positive CVS is significantly higher than that following negative CVS in the range of 4 to 25 nC cm^2. In contrast, the leakage current during the negative CVS is three orders of magnitude higher than that during the positive CVS for the same bias stress magnitude. The charge buildup and leakage current can be explained in terms of electron trapping in the bulk Parylenen-C/Pentacene interface and bulk Parylene C. Before the application of the CVS, a dielectric breakdown occurs at an electric field of 1.62 MV cm^{-1}. After the application of the CVS, the breakdown voltage decreases and the density of the trapped charges increases as the stress voltage increases in magnitude, with the polarity of the trapped charges opposite to that of the stress voltage. Trapped-charge buildup occurs in the bulk Parylene-C layer and in the proximity of the bulk Parylene-C/Pentacene interface during CVS, the magnitude and direction of the capacitance-voltage curve-shift depending on the trapping and recombination of electrons and holes in those regions.

The overall conclusion is that both mechanical and dielectric properties of the Parylene-C columnar μFTFs can be controlled by selecting χ_v appropriately. As a result, Parylene-C columnar μFTFs can be fabricated to deliver $\kappa = 2.02$, which is lower than $\kappa = 3.0$ of bulk Parylene C by 30%. Therefore, Parylene-C columnar

μFTFs are promising candidates for deployment as ultralow-κ ILDs beside their electrical stability and reliability.

Finally, the buildup of trapped charges in the bulk Parylene-C used as a gate dielectric and near the Parylene-C/Pentacene interface plays a major role in the degradation of Au/bulk Parylene-C/Pentacene structures. The first-level understanding of charge buildup in Au/bulk Parylene-C/Pentacene structures obtained will serve as the basis of future studies on the defect-generation process and the trapping of charge carriers within the insulator layer in OFETs.

Table of Contents

List of Figures

List of Tables

List of Symbols

κ	Dielectric constant or relative permittivity
C	Capacitance
t_{delay}	RC delay time
R_{m}	Resistance of a metal line
ρ	Resistivity of a metal line
ℓ	Length of a metal line
A_{m}	Cross-sectional area of a metal line
ε_o	Permittivity of vacuum
A	Top cross-sectional area of a capacitor
d	Thickness
P	Polarization
V	Voltage
f	Frequency
N	Density of electric dipoles
α_{p}	Total polarizability

χ_v	Deposition angle
χ	Tilt angle
T_s	Substrate temperature
T_m	Melting point
p	Porosity
ρ_col	Mass density of μFTF
ρ_air	Mass density of air
ρ_bulk	Mass density of bulk
$E_\parallel$	Static Young's modulus for loading along the x axis
$E_\perp$	Static Young's modulus for loading along the y axis
$YS_\parallel$	Yield strength for loading along the x axis
$YS_\perp$	Yield strength for loading along the y axis
R_p	Equivalent resistance
X_C	Equivalent reactance
V_dc	Bias voltage
V_ac	Sinusoidal voltage
T	Temperature
I_dc	DC leakage current
E_dc	DC electric field
$\Phi_\mathrm{B}^\mathrm{PF}$	Poole–Frenkel barrier energy

$\Phi_{\mathrm{B}}^{\mathrm{SC}}$	Schottky barrier energy
q_e	Elementary charge
k_B	Boltzmann constant
κ_∞	High-frequency relative permittivity
Z	Equivalent impedance
σ_{ac}	AC conductivity
σ_o	Low-frequency conductivity
B and s	Temperature-dependent parameters
τ	Characteristic relaxation time
W_H	Polaron hopping energy
Φ_{act}	Frequency-dependent activation energy
I_{m}	Transient leakage current
V_{stress}	Constant voltage applied to electrically stress a dielectric
J_{dc}	Leakage current density
I_{d}	Decaying component of leakage current
I_{L}	Steady-state component of leakage current
β	Stretch factor
E_{ext}	External electric field
E_{local}	Local electric field
C_o	Capacitance before application of constant-voltage stress

C_{s}	Capacitance after application of constant-voltage stress
δC	Relative change in capacitance
ΔC	Change in capacitance
C_{m}	Capacitance of MIS structure
C_{i}	Insulator capacitance
C_{sim}	Semiconductor-depletion-layer capacitance
ΔV	C-V curve-shift
E_{bd}	Breakdown electric field
t_{bd}	Time-to-breakdown
ΔQ_{t}	Charge buildup
Q_{m}	Charge density of mobile positive charges
Q_{b}	Charge density of charges trapped in bulk insulator
Q_{i}	Charge density of charges trapped in semiconductor/insulator interface

List of Acronyms and Abbreviations

a.c.	Alternating current
Al	Aluminum
Al_2O_3	Aluminum oxide
a-SiOC:H	Porous organosilicate
Au	Gold
CMOS	Complementary-metal-oxide-silicon
Cr	Chromium
Cu	Copper
C-V	Capacitance-voltage
CVS	Constant-voltage stress
d.c.	Direct current
DI	deionized
DMA	Dynamical mechanical analyzer
DT	Direct tunneling
EPD	Electrophoretic display

FESEM Field-emission scanning-electron microscope

FN Fowler–Nordheim tunneling

FSG Fluorinated silicon glass

IC Integrated circuit

ILD Interlayer dielectric

IoT Internet-of-Things

ITRS International Technology Roadmap for Semiconductors

I-V Current-voltage

IVT Current-voltage-temperature

KWW Kohlrausch–Williams–Watts

LCD Liquid-crystal display

μFTF Microfibrous thin film

MIM Metal-insulator-metal

MIS Metal-insulator-semiconductor

MIT Massachusetts Institute of Technology

MSP Morphologically significant plane

O-EA Organic and Printed Electronics Association

OFET Organic field-effect transistor

OLED Organic light-emitting diode

ONEL Organic and Nanostructured Electronics Laboratory

OPV	Organic photovoltaics
OTFT	Organic thin-film transistor
Parylene	Poly(para-xylylene)
PECVD	Plasma-enhanced chemical vapor deposition
PEN	Polyethylene naphthalate
PES	Polyethersulphone
PET	Polyethylene terephthalate
PF	Poole–Frenkel emission
PI	Polyimide
PMMA	Poly(methylmethacrylate)
PS	Polystyrene
PVA	Poly(vinyl alcohol)
PVD	Physical vapor deposition
PVP	Poly(vinyl phenol)
R2R	roll-to-roll
RAM	Random-access memory
RFID	Radio-frequency identification
RRAM	Resistive random-access memories
SC	Schottky emission
SCL	Space-charge-limited

Si	Silicon
SiO_2	Silicon dioxide
SPTM	Small-polaron-tunneling mechanism
STF	Sculptured thin film
SZM	Structure zone model
TAT	Trap-assisted tunneling
TDDB	Time-dependent dielectric breakdown
VLSI	Very-large-scale integration
WLAN	Wireless local-area network
WVTR	Water-vapor transmission rate

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Chapter 1
Introduction

1.1 Overview

The world of solid-state applications is growing very fast on different length scales. At small scales, electronic devices are signalling the end of Moore's law for logic integrated circuits (ICs). At large scales, the exploration of new materials and fabrication techniques are opening a wide range of opportunities for innovative applications such as flexible displays, artificial skins, photovoltaic windows, and bio-compatible implantable devices [1]. The present generation of electronic applications does not only involve inorganic devices, but also includes organic as well as hybrid organic/inorganic devices. This is due to the remarkable progress in the engineering of a variety of materials, allowing one to design and fabricate different cost-effective and high-performance electronic devices.

However, continuing research activities on electronic devices – including materials, device structures, and advanced manufacturing processes – should not only support advances in electronic technologies but also societal and environmental development. Ongoing research should contribute to improvements in health and quality of life by ensuring the best performance of health-related and environment-friendly materials and devices. Therefore, research has been focused on different materials and/or device structures to be used in novel eco-friendly and sustainable applications (Fig. 1.1).

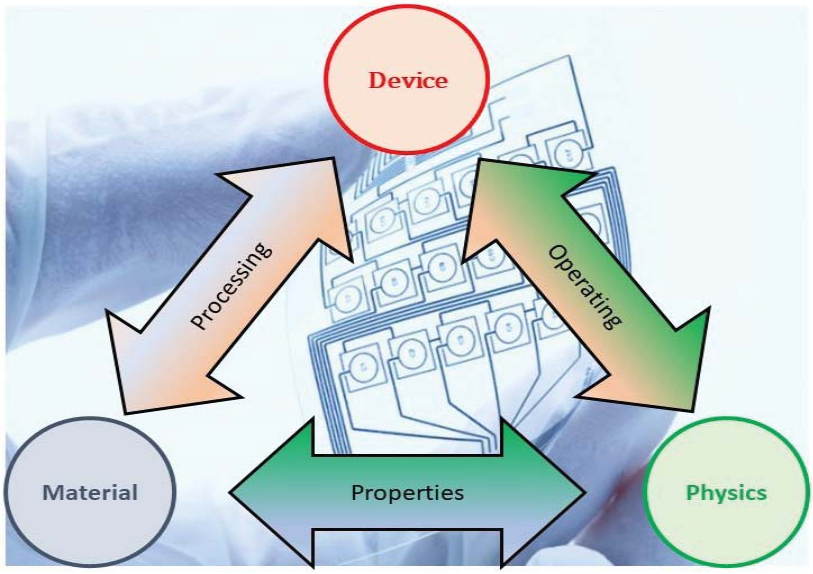

Figure 1.1. Future advances in the field of solid-state devices are dependent on the development of new multifunctional materials and novel deposition processes by fully understanding the physics behind the new material properties and device operation.

Flexible electronics have attracted interest, because of the cost-effective thin-film deposition techniques perfected and the tremendous ability to control the physical characteristics of the deposited film. Currently, solid-state lighting, photovoltaics, and bioelectronics are the areas of intense interest for the use of flexible electronics. The long-term goal is to create cost-effective, large-scale, and ultra-thin flexible devices and ICs made completely from flexible materials [1].

However, there are still some significant problems to be solved before flexible electronics find wider consumer markets and get integrated into everyday applications [1–3]. These challenges are at different levels: materials, devices, and circuits [1–3]. At the materials level, there are challenges in terms of developing and engineering insulating materials that could meet the fabrication, encapsulation, and integration requirements with minimal instability and drift in device performance [1–3]. These materials must also have the ability to be deposited uniformly and controllably over

large areas. Moreover, the chosen insulating materials should play different roles in the same flexible device, thereby reducing the number of materials used to fabricate these devices. In other words, the use of a single material as a multifunctional insulator (i.e., substrate, gate dielectric, and passivation layer) in the same device will reduce cost and improve the sustainability of flexible devices [1–4].

For decades, Parylene C has been widely used as a protection layer (i.e., encapsulation, passivation, and moisture barrier) in different medical and electronics devices [5]. However, Parylene C is not simply a protection layer. Due to its desirable mechanical and electrical properties, Parylene C also has been utilized as a flexible substrate in flexible electronics [1]. Recently, Parylene C has been proposed as a gate dielectric in organic field effect transistors (OFETs) [4]. Therefore, Parylene C is a multifunctional material that can play different roles in different electronic devices [4].

1.2 Research objectives of the dissertation

The potential use of Parylene C as a multifunctional insulator (i.e., substrate, gate dielectric, and passivation layer) in the same device will result in cost reduction and improved reliability and sustainability of flexible electronics. This is reminiscent of silicon oxide used as a gate dielectric as well as an interlayer dielectric (ILD) in conventional ICs. Therefore, the main question asked for this dissertation is whether we can engineer Parylene-C properties via a controllable deposition technique and conditions in order to use this material for different roles. For example, bulk Parylene C has been shown to function very well as a gate dielectric in organic field-effect devices [4]. Moreover, bulk Parylene C has been demonstrated to serve as an encapsulating layer as well as a substrate in flexible electronics [4].

Can we engineer the microscale morphology of Parylene C and, hence, modify its electrical and mechanical characteristics to enable its use as an ILD in flexible ICs? To

answer this question, the research reported in this dissertation addresses the changes in the electrical and mechanical characteristics introduced in Parylene C as a result of using a non-traditional method of deposition. With respect to electrical properties, this dissertation reports the lowering of the dielectric constant or relative permittivity κ of Parylene C. Also, the leakage current in Parylene C and the mechanisms responsible for charge transport were studied. In addition, the electrical stability and mechanical flexibility of the Parylene-C ILD were addressed in this dissertation.

Parylene-C columnar microfibrous thin films (μFTFs) were prepared using an oblique-angle physicochemical vapor deposition technique developed and applied at the Pennsylvania State University. The Parylene-C columnar μFTFs were examined for use in flexible electronics by studying their electrical characteristics, stability, and reliability. The research reported in this dissertation attempts to engineer κ in Parylene-C columnar μFTFs and enable their use as ILD in flexible electronics. Therefore, effects of the morphology of Parylene-C columnar μFTFs on the mechanical and dielectric properties of the film were studied. This objective was attained through a systematic study that related κ as well as porosity and mechanical flexibility to the deposition conditions of the Parylene-C columnar μFTFs. Another objective was to identify carrier-transport mechanisms in the Parylene-C columnar μFTFs by measuring leakage current in relation to temperature, and applied voltage. Determinding the reliability and electrical stress resistance of the Parylene-C columnar μFTFs by monitoring leakage current and capacitance as functions of bias stress was the third objective.

Bulk Parylene-C films, prepared using a standard chemical vapor deposition method, are vastly different from Parylene-C columnar μFTFs and are, hence, expected to have different electrical and mechanical characteristics than Parylene-C columnar μFTFs. Bulk Parylene-C films are extensively studied [4, 6–11] as gate dielectrics in organic field-effect devices. However, very little is known about the

electrical stability and reliability of bulk Parylene-C and its interfaces with organic semiconductors in these devices. This dissertation addresses this shortfall and presents results of a systematic analysis of a Au/bulk Parylene-C/Pentacene material system in terms of charge buildup, leakage current, and dielectric breakdown under constant-voltage stress.

1.3 Research plan and dissertation organization

Aiming to explore the suitability of Parylene C in flexible electronics, the research work plan was executed in the following sequence (Fig. 1.2):

1. Study the Parylene-C columnar μFTFs' morphology, porosity, flexibility, and dielectric properties in relation to the deposition angle in oblique-angle physiochemical deposition technique.

2. Identify charge transport and conduction mechanisms in Parylene-C columnar μFTFs.

3. Investigate stability and electrical-stress resistance of Parylene-C columnar μFTFs.

4. Understand the different physical phenomena of charge buildup and electrical degradation in bulk Parylene-C films.

Consequently, this dissertation is organized as follows:

- Chapter 2 contains a literature review on flexible electronics: history, materials, and applications.

- Chapter 3 describes the properties of Parylene-C as a multifunctional insulator in different applications.

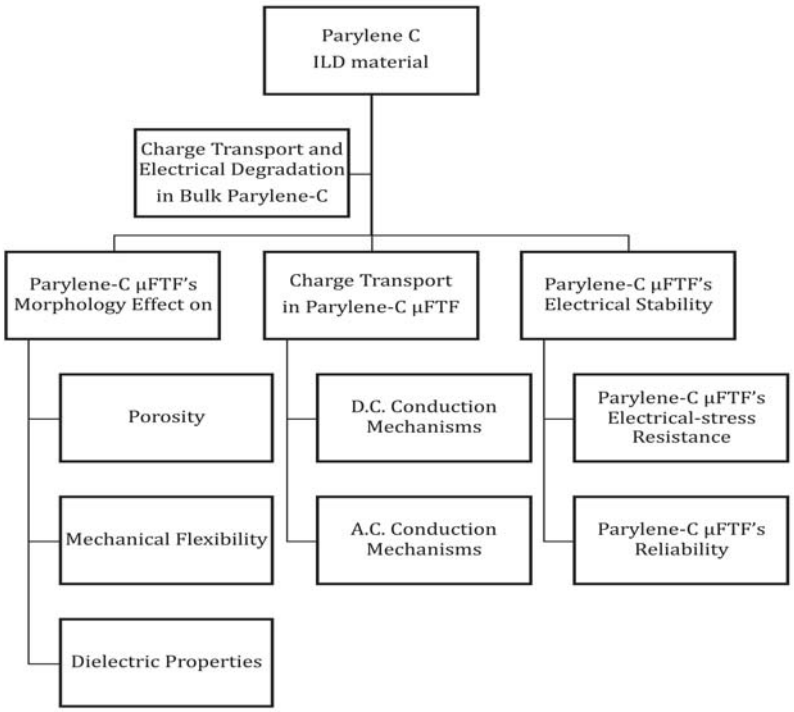

Figure 1.2. Organization flow of the objectives of this dissertation.

- An overview of ILD requirements and materials is presented in Chapter 4.
- The fabrication of Parylene-C columnar μFTFs is presented in Chapter 5.
- Characterization of the effects of morphology on the mechanical and dielectric properties of Parylene-C columnar μFTFs is described in Chapter 6.
- Chapter 7 discusses the charge transport and conduction mechanisms in Parylene-C columnar μFTFs.
- Chapter 8 discusses the effects of constant-voltage stress (CVS) on the stability of Parylene-C columnar μFTFs.
- A systematic analysis of Au/bulk Parylene-C/Pentacene structures to gain a better understanding of their degradation is reported in Chapter 9.

- The overall conclusions and directions for future work are given in Chapter 10.

1.4 List of publications resulting from this dissertation

The following journal or conference papers were published as a result of research reported in this dissertation:

1. **Ibrahim H. Khawaji**, Chandraprakash Chindam, Wasim Orfali, Osama Osman Awadelkarim, and Akhlesh Lakhtakia, "Electrical studies on Parylene-C columnar microfibrous thin films," *ECS Transactions*, vol. 69, no. 5, pp. 113–119 (2015).

2. **Ibrahim H. Khawaji**, Osama O. Awadelkarim, and Akhlesh Lakhtakia, "Studies of Parylene C microfibrous thin films electrical properties," *ECS Transactions*, vol. 75, no. 5, pp. 235–243 (2016).

3. **Ibrahim H. Khawaji**, Chandraprakash Chindam, Osama O. Awadelkarim, and Akhlesh Lakhtakia, "Dielectric properties of and charge transport in columnar microfibrous thin films of Parylene C," *IEEE Transactions on Electron Devices*, vol. 64, no. 8, pp. 3360–3367 (2017).

4. **Ibrahim H. Khawaji**, Chandraprakash Chindam, Osama O. Awadelkarim, and Akhlesh Lakhtakia, "Selectablity of mechanical and dielectric properties of Parylene-C columnar microfibrous thin films by varying deposition angle." *Flexible and Printed Electronics*, vol. 2, no. 4, art. no. 045012 (2017).

5. **Ibrahim H. Khawaji**, Osama O. Awadelkarim, and Akhlesh Lakhtakia, "Effects of constant-voltage stress on the stability of Parylene-C columnar microfibrous thin films," *IEEE Transactions on Dielectrics and Electrical Insulators*, vol. 26, no. 1, pp. 270–275 (2019).

6. **Ibrahim H. Khawaji**, Alyssa N. Brigeman, Osama O. Awadelkarim, and Akhlesh Lakhtakia, "Charge buildup and leakage current in gold/Parylene-C/pentacene capacitor under constant-voltage stress," *Microelectronics Engineering*. (submitted and under review)

7. **Ibrahim H. Khawaji**, Osama O. Awadelkarim, and Akhlesh Lakhtakia, "Parylene C as a multifunctional insulator for all-organic flexible electronics," *Proceedings of SPIE*, vol. 10968, art. no. 1096813 (2019).

Chapter 2
Review of Flexible Electronics

2.1 Introduction

For decades, the backbone of semiconductor devices has been furnished by inorganic materials such as silicon (Si) and its oxide. Texas Instruments and Fairchild Semiconductor, fabricated the first Si-based IC chip around 1960 [12]. In September 2015, the 6^{th} generation nano-scale architecture was launched in Intel Core Processors. The processor consists of more than 2.6 billion transistors on a 122.4 mm^2 die [13]. Indeed, the Si-based complementary-metal-oxide-silicon (CMOS) technology can now be considered to be well developed. Advances in nano-scale fabrication of Si-based electronics are promoted by research efforts to further miniaturize device size, increase device density in a chip, and improve device performance and reliability while reducing the production cost.

In contrast, large-scale electronics have recently attracted much interest. For example, a very important large-scale electronics application is flat-panel displays, which are lighter, thinner, and more economical than traditional cathode-ray-tube displays. Future advances in large-scale electronics are dependent on the development of new multifunctional materials and novel deposition processes [1]. Hence, a wide spectrum of new material compositions and morphologies are being explored. Researchers are currently looking for alternatives to conventional Si-based devices

with specific requirements on new materials such as transparency and flexibility [1]. For several applications, flexible materials are desirable substitutes to the traditional inorganic materials, with several emerging optical and electronic devices made using engineered flexible materials [1].

In 1994, the printed all-polymer transistor was demonstrated [17, 18]. Since then, much attention has been directed toward the development of flexible ICs on plastic substrates. In order to achieve the goal of all-organic flexible solid-state electronics, research has been focused on fundamental materials for flexible devices: conductors, insulators, and semiconductors [17, 18]. Not only have new materials been sought, but modified and even new devices architectures have been devised [17, 18]. These efforts continue to play an important role in expanding the manufacturing boundaries for flexible electronics [1].

Because they are easy to fabricate, inexpensive, and can be manufactured in large sheets, flexible materials are becoming important components of most organic devices [17, 18] such as organic thin-film transistors (OTFTs), organic photovoltaics (OPVs), and organic light-emitting diodes (OLEDs). Flexible materials are rapidly replacing conventional Si-based materials in applications requiring large-area coverage, structural flexibility, and low-temperature processing. Moreover, organic-based radio-frequency identification (RFID) tags [19] used to label and track objects automatically are attracting researchers' attention because of relatively low-cost production in comparison to their inorganic counterparts. Also, flexible sensors have been extensively fabricated for biosensors [20], mechanical sensors [21], storage devices [22], artificial skins [23], and wearable electronics [24]. Indeed, research in flexible electronics is rapidly growing.

Figure 2.1. Key applications in need for further development of organic and printed electronics [25].

2.2 Organic electronics roadmap

Organic electronics are suitable for a wide range of applications, as shown in Fig. 2.1 [25]. These devices are integrated into commercial applications such as OLED frontplanes and OTFT backplanes for displays or are integrated into promising applications such as OPVs, RFID tags, biosensors, memories, and integrated smart systems [25]. Most of these applications are either based on or integrated with OFETs. In fact, OFETs are the primary devices in flexible electronics. Moreover, OFETs have been integrated into logic circuits [28, 29], and are also strong candidates in sensing applications, as active layers can be made of organic semiconductors and organic insulators, depending on the OFET geometry [28, 29].

The market for organic electronics is mainly driven by solid-state lighting and

display technologies. Leading industrial companies such as Samsung, Philips, Sony, and LG are the top players in this market. This market will continue to grow with a projected market size of around 70 billion dollars by the year 2020 [25].

Since 2004, the Organic and Printed Electronics Association (OE-A) has been the leading international association for organics industry standards and future roadmap. The OE-A roadmap consists of all updates about new applications, materials, and processing techniques in the organic electronics industry. As shown in Fig. 2.2 [25], the 2017 OE-A roadmap is based on: operating conditions (i.e., voltage and frequency) and reliability (i.e., lifetime, efficiency, cost, and sustainability) with the ultimate goal being true flexibility (i.e. conformality, rollability, and stretchability) [25].

Therefore, flexibility is an important features for organic electronics. Flexibility can be differently interpreted by different manufacturers and users. As a mechanical characteristic, it is conveniently classified as bendability or stretchability. Also, a flexible substrate can be non-planar. Searching for flexible materials and utilizing novel fabrication methods are necessary to develop flexible electronics [1].

2.3 Applications of flexible electronics

Flexible devices are becoming a big part of our daily lives because they are inexpensive, bendable, easy to process, and can be fabricated in large areas. Flexible displays are a rapidly growing field as they can replace rigid glass panels. Numerous displays [17,18] including liquid-crystal displays (LCDs), electrophoretic displays (EPDs), and OLED displays on various polymeric substrates have been made. Paper-like displays are attractive for e-Reader [26] and e-Paper [27] applications. Artificial muscles comprising electro-optic polymers have potential applications [30] for biologically inspired robots, animatronics, and prosthetics. Flexible electronic circuits are woven or integrated onto fabric in smart textiles, a growing industry [24].

OE-A Roadmap for Organic and Printed Electronics Applications 2017

	Existing 2017	Short Term 2018-2020	Medium Term 2021-2023	Long Term 2024+	
	Rigid white OLED modules; rigid red OLEDs for automotive applications	Flexible OLEDs (color); flexible OLEDs (white)	Transparent OLEDs; flexible red OLED for automotive applications	3D OLEDs; dynamic OLED signage (segmented); long stripes; OLED in general lighting	**OLED Lighting**
OPV	Portable OPV chargers; personal electronics power supply	Large area OPV foil; OPV objects; opaque OPV for building integration	OPV integrated in building products	OPV in packaging; energy harvesting combined with storage	
	Curved OLED displays, EPD shelf-edge labels, EPD secondary displays on phones; displays for wearables	EPD wrist band; transparent displays; conformable OLCD; enhanced display integration in wearables	Curved displays for autmotive interior; integration into clothing; white goods displays	Wallpaper displays; displays in everyday objects; foldable displays	**Flexible & OLED Displays**
Electronics & Components	Printed devices: memory, RFID antenna, primary battery, active backplane; sensors: glucose, touch, temperature, humidity	Printed mobile communication devices based on antennas, light sensor; stretchable conductors / resistors; 3D touch sensors	Printed lithium ion battery; printed super caps; active touch & gesture sensors	Printed complex logic; 3D & large area flexible electronics	
	Glucose in-body sensing; pressure sensor arrays; NFC labels; hybrid RFID; HMIs (sensors)	Smart labels (discrete); HMI (embedded electronics & displays)	Human monitoring patches (single parameter, point of care, on-skin); disposable & quantitative sensors for food safety; biomedical sensors	Fully printed RFID / NFC label; ambient intelligence (connected); sensors for security (explosives)	**Integrated Smart Systems**

Figure 2.2. OA-E 2017 roadmap for organic and printed applications [25].

Flexible electronics are an essential pillar in the Internet-of-Things (IoT) technology, as device flexibility is one of the crucial features of this technology. IoT was listed as one of the top ten strategic technology trends in 2015 [31]. It refers to the network of physical objects or "things" embedded with electronics, software, and sensors to enable them to provide greater value and service by exchanging data with the manufacturers, operators, and/or other connected devices.

IoT was conceptualized by Ashton in 1999 [32]. The concept has become popular, and the vision has evolved in recent years. Sensors and communication tags are key components of IoT. They monitor the status of "things" and communicate with the "internet" to exchange information about or among "things". IoT will affect dramatically the way we live. In other words, when everyday objects are able to sense and instantly communicate with one another, major changes must occur about how and where decisions are made, and who makes those decisions.

2.4 Flexible electronics fabrication

At the present time, two main fabrication approaches are widely used in flexible electronics fabrication industry: roll-to-roll (R2R) processing and batch processing [1, 17, 18]. Although the R2R process is commonly used for low-cost applications such as polymer solar cells, it has several limitations. For instance, it is not compatible with conventional fabrication steps (e.g., alignment, vacuum deposition, and photolithography). Also, it is not preferred for low-throughput customized manufacturing because it would be difficult to justify the production cost.

The second fabrication approach is batch processing or sheet-fed processing, which is compatible with most technologies used in nanofabrication facilities. This approach can be implemented in two ways. One way is to directly deposit the flexible device on a flexible or stretchable substrate. The other is to fabricate the device on top

of a rigid substrate, such as a Si wafer or a glass substrate, and then transfer the device using a peel-off technique. The second way is commonly used to produce high-performance devices such as amorphous-Si TFTs, OFETs, and memory devices. Batch processing also allows the use of standard equipment and processes for flexible electronics.

Flexible materials are required for conduction, semiconduction, and insulation layers. Furthermore, a completely flexible electronic device often consists of active, functional, supporting and protection components, which must also be made of flexible materials [1, 17, 18].

2.5 Electrical insulators for flexible electronics

2.5.1 Mechanically flexible substrates

The substrate is the primary component affecting the device flexibility. Flexible substrates must possess appropriate mechanical, thermal, chemical, electrical, optical, and magnetic characteristics [1, 17, 18]. Most importantly, sufficient mechanical strength and flexibility to support the device are crucial for the substrates. Flexible substrates must be compatible with conventional fabrication challenges such as chemical resistance and thermal instability. In addition, the fabrication cost of the substrate is an important factor for large-area applications.

In large-area applications, traditional substrates include glass, stainless steel, paper, and plastic. Glass substrates are transparent, but are usually stiff and thick. Therefore, glass is not suitable for flexible applications that involve bending and stretching [17, 18]. In contrast, stainless-steel foil is more flexible and less stiff than glass. However, stainless steel is not transparent. Its rough surface requires additional fabrication steps such as the deposition of a buffer layer (for insulation). Also, it

is relatively thick and hard to bend. Recently, flexible metal-foil substrates less than 50-125 μm in thickness, depending on the metal, have been used for display applications [17, 18].

Polyimide (PI or Kapton™), polyethylene terephthalate (PET), polyethersulphone (PES), and polyethylene naphthalate (PEN) are recognized as suitable candidates for flexible substrates [17, 18]. These polymers are also economical. PET, PEN, and PI substrates have been employed also for their thermal properties [1, 17, 18]. They have a coefficient of thermal expansion (CTE) below 20 ppm/°C. Therefore, PEN, PET, and PI are compatible with fabrication-process temperatures of 200, 150, and 350 °C, respectively. However, PEN, PET, and PI are mostly available in bulk sheets with thicknesses in the [50, 100]-μm range and their gas and moisture permeabilities degrade with aging. A polymeric substrate with good gas and moisture permeabilities, easy manufacturability, and mechanical strength is needed for flexible electronics.

2.5.2 Protection and encapsulation materials

Although flexible electronic devices are sustainable and eco-friendly, their long-term environmental stability is vital because these systems are often designed to operate under harsh conditions for long periods [33]. One of the main fabrication challenges for flexible devices is to maintain adequate protection of the active layers from moisture and atmospheric gases [1, 17, 18]. Exposing the device to ambient conditions will lead to a degradation in device performance, as it contains active organic material layers. Therefore, an encapsulation layer is used to protect the device from ambient conditions and to prevent the active layers (semiconductors, dielectrics, or transparent conductive oxides) from charge-trapping effects induced by mechanical cracking [33]. For these reasons, there is a significant interest in polymers that can be successfully used as both substrate and encapsulation layers [4].

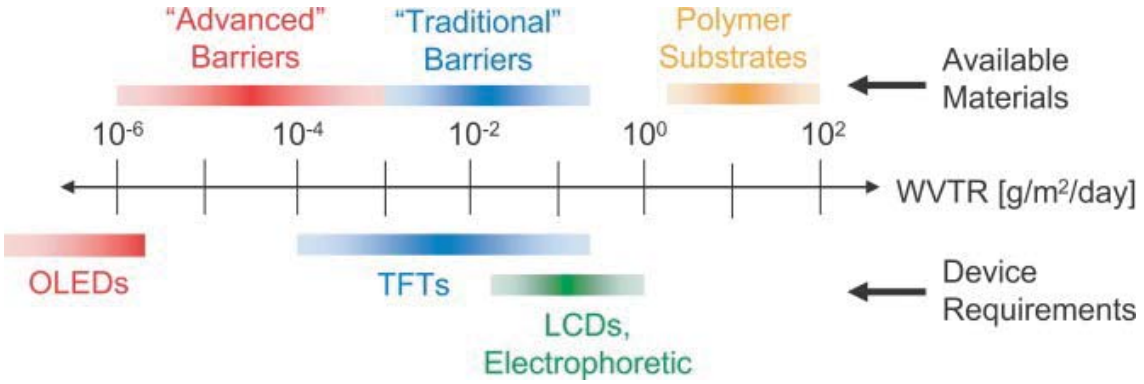

Figure 2.3. WVTR requirements for encapsulation layers suitable for flexible electronic devices [35].

PET and PEN are commonly used both as flexible substrates and encapsulation layers. These materials have a water-vapor transmission rate (WVTR) of 10^2 g/m^2/day [34]. However, the required WVTR values for flexible electronic devices, as shown in Fig. 2.3 [35], are lower by three orders of magnitude [35]. On the other hand, inorganic barriers (i.e., traditional barriers) such as silicon dioxide (SiO_2) and aluminum oxide (Al_2O_3) also have been suggested as encapsulation layers for flexible devices. Although these barriers can reduce the WVTR to about 10^{-1} g/m^2/day, these materials are brittle and can crack at even low mechanical strain during device operation. Formation of cracks in the encapsulation layer will degrade device performance.

Other approaches that have also been explored to improve barrier performance involve thicker encapsulation layers and using hybrid (i.e., organic and inorganic) multilayer structures [35]. These approaches have shown a good impact in WVTR reduction to a value about 10^{-5} g/m^2/day. However,the encapsulation layer's thickness in either approach will eventually result in a dramatic reduction of the device flexibility. Up until now, the development of the encapsulation layer in flexible electronic devices is a major challenge [34, 35].

2.5.3 Gate dielectric materials

Gate dielectrics play an important role in many electronic devices, especially in transistors. For selecting a suitable material, many characteristics must be considered. These characteristics include relative permittivity, leakage current, semiconductor-dielectric interface quality, stability, and reliability. Mainly two types of dielectric materials, inorganic and organic, are recognized as gate dielectric materials for OTFTs, OFETs, and non-volatile random-access memory (RAM).

The first type includes inorganic dielectric materials such as SiO_2 and Al_2O_3. These are commonly used in OFETs [36]. However, the deposition of these materials is costly as it involves complex processes. Also, they are not easily compatible with many types of flexible substrates, and additional processing steps are needed to overcome this handicap. Furthermore, thin films of these inorganic dielectric materials contain defects and pinholes. Another concern is that the thicknesses of these materials need to be as small as a few nanometers, in order to achieve the required degree of flexibility for flexible electronics. Therefore, high leakage current in these thin films is possible. Even though thermal annealing can be used to improve the quality of these thin inorganic dielectric materials, the flexible substrates will not be able to handle the high-temperature processes during fabrication.

The second type includes organic dielectric materials, mainly polymers. These have several advantages compared to their inorganic counterparts. Polymers are generally flexible for a wide range of thicknesses and have excellent insulating properties. Furthermore, their deposition processes are inexpensive and compatible with different flexible substrates. Polymer gate dielectrics [36] such as polystyrene (PS), polymethylmethacrylate (PMMA), poly(vinyl alcohol) PVA, and poly(vinyl phenol) PVP have been used for OFETs. However, the drawback of using these materials is that they are not compatible with standard microfabrication processes that require the use

of reactive chemicals, which limits their applications for flexible devices made on polymeric substrates.

2.6 Challenges and outstanding research in flexible electronics

There are still some significant challenges to be overcome before flexible electronics finds wider consumer markets and gets integrated into everyday applications. These challenges are at different levels: materials, devices, and circuits [2, 3]. The highlights of the challenges at each level are as follows:

- Materials – there are still challenges in terms of developing and engineering insulating materials that could meet the fabrication, encapsulation, and integration requirements with minimal instability and drift in device performance. These materials must also be possible to be deposited uniformly and controllably over large areas.

- Devices – unlike inorganic devices, the evaluation of a flexible device's performance does not only depend on operational standards but also on the degree of device's flexibility and stretchability while maintaining adequate operational standards. This amounts to saying that (i) the device performance standards are to be maintained upon the application of both electrical and mechanical stresses, and (ii) that the device is electrically and mechanically reliable and stable.

- Circuits – the compatibility and functionality of flexible circuits present major challenges when integrated into a bent, stretched, twisted or rolled-up substrate or platform. Major components of flexible circuits include the substrate, the interconnects, and the interlayer dielectrics. These components must all be

also acceptable in terms of flexibility and stretchability. For example, the active-matrix flexible display consists of OLED pixels, interconnected by ILD and integrated onto a backplane of OTFTs array on a flexible substrate.

- Reliability, stability and operational lifetime – at all three levels, fundamental studies are essential before flexible electronic become economically manufacturable.

Fundamental studies on new materials, device architectures, device stability, long-term reliability, and resistance to electrical and mechanical stresses are essential. Flexible electronics is still in its infancy, and there are enormous opportunities for high-impact research for applications that exploit low-cost manufacturing, flexibility, and large area.

Chapter 3
Parylene C as a Multifunctional Electrical Insulator

3.1 Introduction

A family of polymers collectively called parylenes [37] is commonly used in the electronics industry for moisture-banner coatings. There are many types, but only four are widely known: Parylene N, Parylene C, Parylene D, and Parylene HT [38]. Figure 3.1 illustrates the chemical formula of each of these four types of parylene [38]. Parylene N – Poly(para-xylylene) – is the basic member of this family. It is a low-loss insulator [37]. Parylene D, which has the largest monomer and two chlorine atoms in every benzene ring, possesses the same excellent physical and electrical properties as Parylene N, but with the ability to withstand higher temperatures. In Parylene Nova HT (Parylene AF-4), the newest commercially available member, the hydrogen atoms of Parylene N dimer are replaced by fluorine atoms. It is suitable for avionics applications due to its resistance to high temperatures and ultraviolet radiation. Parylene C is produced from the same dimer as Parylene N with a substitution of one chlorine atom for one of the hydrogen atoms. It has a desirable combination of electrical, mechanical, encapsulation, and thermal properties for electronic applications. Also, it is impermeable to corrosive gases [37, 38].

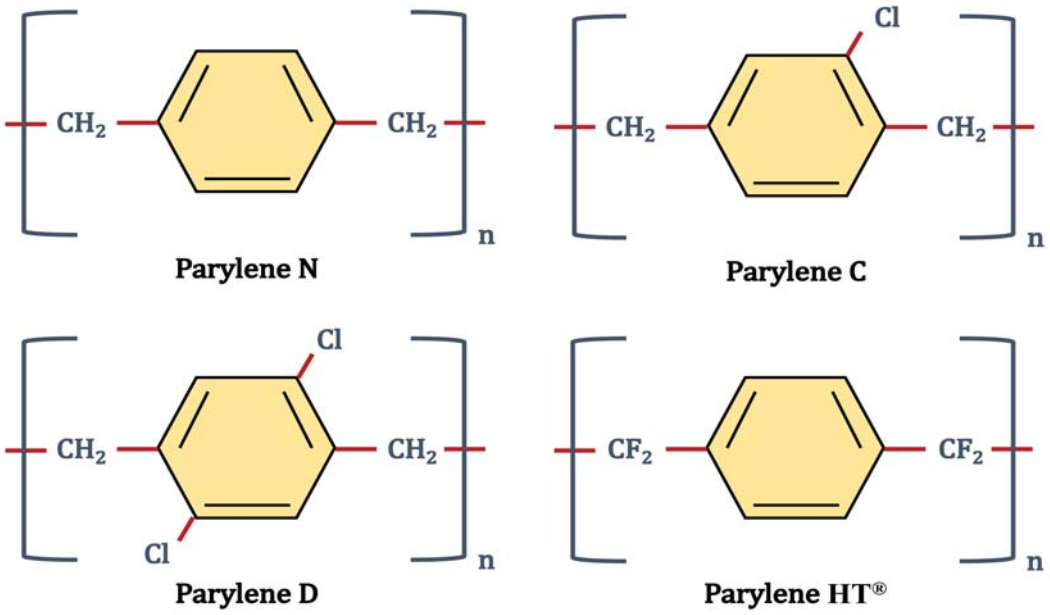

Figure 3.1. The four common types of parylene: Parylene N, Parylene C, Parylene D, and Parylene HT.

Parylene C is flexible, optically transparent, biocompatible, and with high dielectric reliability [38]. Therefore, it is used in several flexible [39], optical [40], and biomedical [41] electronic devices. Moreover, it is a medically accepted polymer, having been classified as a U.S. Pharmacopoeia Class VI polymer for medical devices [41] and being medically approved by the U.S. Federal Drug Administration for internal prostheses [39, 42]. It is widely used as a moisture-barrier coating on implantable devices such as stents, defibrillators, and pacemakers [43].

Basically, Parylene C is being extensively used in electronics for many decades as a protection layer [4] to minimize device degradation caused by exposure to oxygen and moisture. Recently, it has been used for flexible substrates, encapsulation layers, and gate dielectrics [4]. Indeed, Parylene C plays different roles in different electronic devices, as depicted in Fig. 3.2. Therefore, it has the potential to play multiple roles

in the same flexible electronic device.

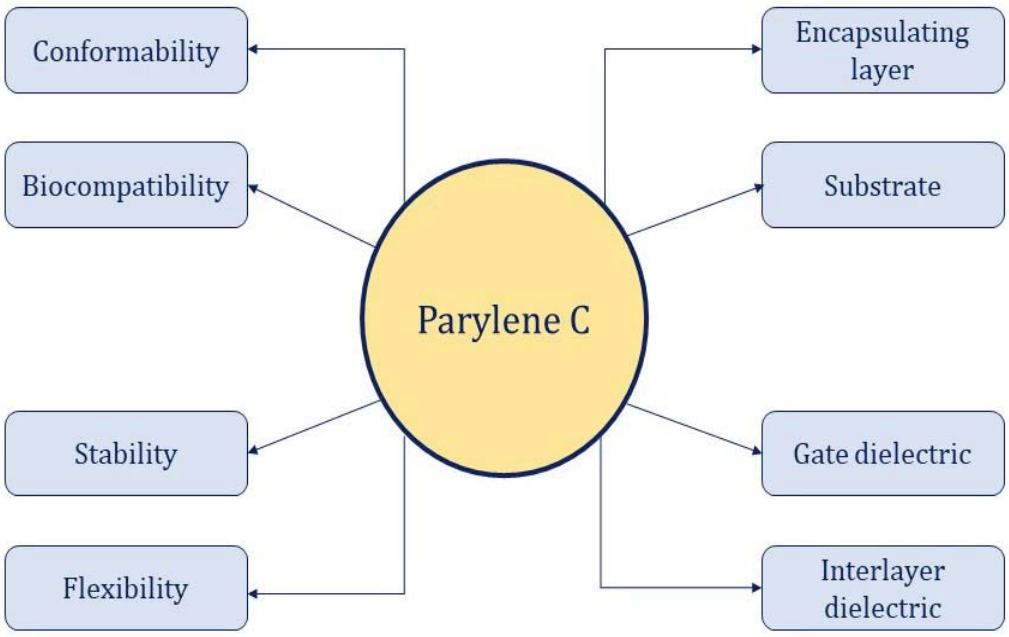

Figure 3.2. Parylene-C features and its multiple roles in different electronic devices.

3.2 Electrical, mechanical, and thermal properties of Parylene C

The electrical, mechanical, thermal, and surface properties of Parylene C are shown in Table 3.1 [38, 44–46]. It has a relative permittivity $\kappa \sim 3.0$, which is comparable to those of most common polymeric insulators [37, 38, 47, 48]. Thin films of Parylene C show insulation resistance about an order of magnitude higher than the standard of the coated circuit board test (MIL-I-46058C). This test is usually conducted at $\sim$ 65 °C and $\sim$ 90% relative humidity [38]. Uniformly thin films of Parylene C have low leakage current and high dielectric strength even at nanometer-level thicknesses [39].

These thin films of Parylene C are pinhole free and mechanically flexible [38].

Table 3.1. Electrical, mechanical, chemical, thermal, and surface properties of bulk Parylene C, PET, PI, and PEN. [38, 44–46].

		Parylene C	**PET (MYLAR 800)**	**PI (Kapton)**	**PEN (Teones)**
Electrical properties	Dielectric strength MV/cm	2.20	4.30	2.30	4.00
	Relative permittivity @ 1 MHz	2.95	3.00	3.00	2.90
	Volume resistivity Ω-cm	9×10^{16}	1×10^{18}	1×10^{17}	1×10^{17}
	Surface resistivity Ω	1×10^{14}	1×10^{16}	–	1×10^{16}
Mechanical properties	Density g/cm^3	1.29	1.39	1.42	1.36
	Tensile strength MPa	69.0	200	231	262
	Yield strength GPa	2.80	4.90	2.50	6.10
Thermal properties	Melting point °C	290	254	520	516
	Thermal expansion coefficient ppm/°C	35.0	39.0	20.0	18.0
	Thermal conductivity W/(m K)	0.08	0.15	0.12	–
Surface properties	Water absorption %	<0.1	0.8	1.8	0.3
	Gas permeability (cc mm)/(m^2 day atm)				
	N_2	0.4	0.6	3.6	–
	O_2	2.8	3.6	15	8
	CO_2	3.0	3.78	27	37
	H_2	43.3	60	150	–
	Water-vapor transmission rate g/m^2/day.	0.08	1.44	2.40	6.70

Due to softness (yield strength of 55.1 MPa and static Young's modulus of 2.76 GPa) [38], fabricability for thicknesses ranging from a few nanometers to hundreds of micrometers, and mechanical robustness, these thin films are highly suitable for flexible

electronic devices. Parylene C exhibits very little optical absorption in the visible spectral regime and is, therefore, transparent and colorless even for micrometer-scale thicknesses [38]. Because the thin films are fabricated by chemical vapor deposition (CVD), purity is high without solvent contamination that occurs when using spin-on deposition [5]. Very importantly for manufacturing operations, Parylene C can be peeled off several types of substrates [4].

Parylene C is expected to survive continuous exposure for 10 years to air at 80 °C as well as to oxygen-free atmosphere at 220 °C, based on Arrhenius extrapolation of test data [38]. The melting point of Parylene C is about 290 °C which is considered favorable for many electronic applications [38].

As a moisture and chemical barrier, bulk Parylene C is superior compared to most common polymeric insulators. The WVTR of Parylene C is comparable to other common conformal coating materials such as epoxies and polyurethanes [38]. In ASTM B117-(03) tests, circuit boards coated with Parylene C showed no corrosion or salt deposits after 144 hours of exposure to air [38]. The all-carbon structural backbone and high molecular weight make Parylene C extremely resistant to most chemicals. Also, it can resist chemical attacks when it is dipped in most organic solvents up to 150 °C [38]. Thin films of Parylene C do not swell significantly with exposure to a host of chemicals including automotive and aviation fluids [38].

Parylene C is a medically accepted polymer. It has been tested according to the biological evaluation requirements of ISO 10993 [38]. Indeed, the biocompatibility and biostability of Parylene C have been extensively demonstrated in biocompatible electronics devices for the last 40 years [5].

3.3 Parylene C in electronic applications

3.3.1 Parylene C as a flexible substrate

Parylene C has been widely used as a flexible substrate in different types of flexible electronic devices [4]. Planar OFETs with Parylene-C substrates demonstrate reversible degradation when bent with radius of curvature between 5 mm to 25 mm [4]. Also, OFETs comprising ultra-thin layers of bulk Parylene C as well as a Parylene-C substrate withstand bending with radius of curvature as low as 0.8 mm [4]. Moreover, inorganic transistors fabricated on Parylene-C substrates exhibit higher room-temperature mobility than those fabricated on SiO_2 substrates [50].

Ultra-thin and flexible transistors fabricated on a Parylene-C membrane can be wrapped around a human hair [40]. Because Parylene C is an FDA-approved and bio-friendly polymer [41], there has been significant research performed using it as a substrate for implantable neural prostheses [5, 49].

Using Parylene C as a substrate, researchers in Organic and Nanostructured Electronics Laboratory (ONEL) at Massachusetts Institute of Technology (MIT) have fabricated the thinnest (1.3 μm) and lightest (3.6 g/m^2) solar cells [51]. These devices exhibit power conversion efficiencies and fabrication yields comparable to the same solar cells fabricated on glass substrates [51].

3.3.2 Parylene C as an encapsulation material

Parylene C has the ability to cover sharp edges, crevices, and overhangs because CVD is used to deposit it [52, 53]. Therefore, Parylene C is used as an encapsulation material for many biocompatible electronic devices including implanted neural prostheses [52, 53].

Numerous published studies [5] on Parylene C have reported its biocompatibility,

biostability, low cytotoxicity, and resistance against hydrolytic degradation [5, 52]. As a result, Parylene C has been widely adapted as an encapsulation layer for bio-MEMS devices [5, 52, 54].

In a study, multiple microelectrodes protected by Parylene-C thin films were fabricated and deployed in monkey motor cortex [55]. For over four months, no changes in these microelectrodes impedance were recorded.

The compatibility of Parylene C as the encapsulation layer in different OFETs has been investigated [4]. The results show that no defects at semiconductor/encapsulation-layer interfaces are formed and, therefore, no additional charge traps are created at these interfaces.

The electrical characteristics of unprotected and protected C_{60}-based OFETs with Parylene-C encapsulation layers were studied [11]. The unprotected OFETs showed electrical degradation after only 90 min [11]. On the other hand, the Parylene-C-protected OFETs were electrically stable since the same level of degradation was observed after 12 days [11].

Parylene C has been used for the encapsulation layer in ultra-thin (2.6 μm) colloidal quantum dot light-emitting diodes that allow the alignment of red-green-blue pixels with resolutions up to 2,460 pixels per inch [56]. With Parylene C used for the substrates and encapsulation layers, the diodes performance is stable on flat, curved and convoluted surfaces under mechanical deformations such as bending, crumpling and wrinkling. These flexible diodes highlight new possibilities for integrating high-definition full-color displays in wearable electronics.

3.3.3 Parylene C as a gate dielectric

As a gate dielectric, Parylene C is compatible with different active organic semiconductors of both p- and n-types [4, 57, 60, 61]. It was introduced as a gate dielectric

in OFETs in 2000 [57]. OFETs made of a rubrene single crystals and Parylene C as a gate dielectric show high charge-carrier mobility, close to that of 10 cm^2/V s [60]. Also, flexible picene OTFTs with Parylene C as a gate dielectric exhibited field-effect hole mobility close to 1 cm^2/V s [61].

3.3.4 Parylene C: other roles in diverse applications

Parylene C has been used in different electronic devices such as wireless local-area network (WLAN) antennas, RFID tags, memories, and sensors. For example, implantable flexible antennas coated with Parylene C show good electrical performances for WLAN application [62]. The first reported waterproof inkjet-printed dual-band monopole antenna was obtained using Parylene C as the protection layer [63].

Parylene C has been used as an intermediate bonding layer and a sidewall passivation material in multi-layer homogeneous 3D ICs using post-CMOS processing protocol [64]. Also, it has been employed as an active layer in resistive random-access memories (RRAMs) for ultrafast nonvolatile [65], wearable [66], and low-power [67] memories.

High-sensitivity fiber-optic Fabry-Perot acoustic sensors based on thin Parylene-C diaphragms have been reported [68]. Also, Parylene C has been used in a chemical sensor for explosives detection [69]. As a pH sensing layer, Parylene C can be used in organic charge-modulated field-effect transistors [70]. In addition, a flexible bio-sensor based on thin Parylene C films that serve both as flexible support substrates and as active H^+-sensing membranes has been fabricated and successfully tested [71].

Chapter 4
Review of Interlayer Dielectrics

4.1 Introduction

One major goal for this dissertation was to determine the suitability of columnar microfibrous thin films of Parylene C as interlayer dielectrics (ILDs). In general, metal lines can be placed and remain electrically isolated from each other in an ILD. In present-day ICs, the ILD is also used to electrically separate closely spaced multilevel metallization of interconnect lines arranged in several levels [72]. Therefore, the ILD must possess low relative permittivity κ to eliminate or minimize cross-talk between interconnect metal lines [72].

The value of κ must be substantially lower than 3.9, which is the relative permittivity of SiO_2. Indeed, in any IC, an adequate ILD must [72]

(1) reduce the RC delay time for faster switching,

(2) reduce power dissipation,

(3) function as an electrical insulator that exhibits both extremely low leakage current and high dielectric strength

(4) provide mechanical support for the several metal layers, and

(5) help distribute thermal and shear stresses produced during processing and packaging.

All five characteristics are essential for ILDs in any IC, and more so in flexible ICs [72].

4.2 ILD properties

4.2.1 Relative permittivity

Figure 4.1 shows a schematic diagram of ILD stacks with adjacent different layers [72]. In any IC, two important parameters are the line resistance R_{m} at the two metallic ends of the interconnect and the capacitance C of the ILD material. Reducing R_{m} and/or C will effectively reduce the RC delay time $t_{\mathrm{delay}} = R_{\mathrm{m}}C$ [73]. The line resistance can be expressed as [72]

$$R_{\mathrm{m}} = \rho \left(\frac{\ell}{A_{\mathrm{m}}} \right), \tag{4.1}$$

where ρ is the resistivity of the metal line, ℓ is the length of the metal line, and A_{m} is the cross-sectional area of the metal line. The ILD capacitance is given by [72]

$$C = \kappa \varepsilon_o \left(\frac{A}{d} \right), \tag{4.2}$$

where $\varepsilon_o = 8.854 \times 10^{-14}$ F cm^{-1} is the permittivity of vacuum, A is the top cross-sectional area of the ILD capacitor, and d is the thickness of the ILD.

Equations (4.1) and (4.2) show that $t_{\mathrm{delay}} \propto \rho\kappa$. Therefore, the IC switching speed will be affected by the electrical properties of the interconnect and the ILD. Thus the selection of an ideal ILD with low κ is a key to minimize t_{delay}.

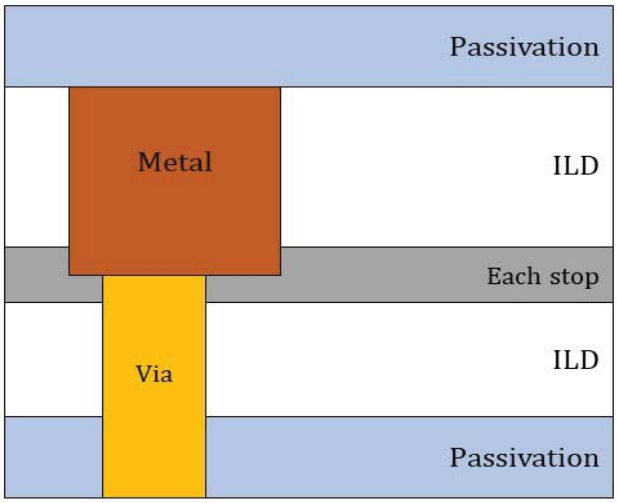

Figure 4.1. Schematic diagram of ILD stacks with adjacent layers of different materials.

The ILD capacitance also affects the consumed power [72]

$$Power \propto CV^2 f, \tag{4.3}$$

where V is the operating voltage and f is the operating frequency. One of today's major goals of IC fabrication is to enhance the power consumption efficiency. Therefore, reduction of the ILD capacitance is essential to reducing the IC power consumption.

Figure 4.2 show estimates of t_{delay} of aluminum (Al)/SiO_2 and copper (Cu)/low-κ material as metal/ILD combinations for different node technologies [74]. Indeed, the integration with a low-κ ILD and low-ρ metal will have a significant impact on the switching speed and the power consumption of the IC [72].

Reduction of R_{m} can be achieved by selecting a metal with low ρ such as Cu. As depicted in Fig. 4.3, there are two general strategies for lowering κ [75]:

(1) choose the ILD material with a chemical structure that has inherently low dielectric polarizability, and/or

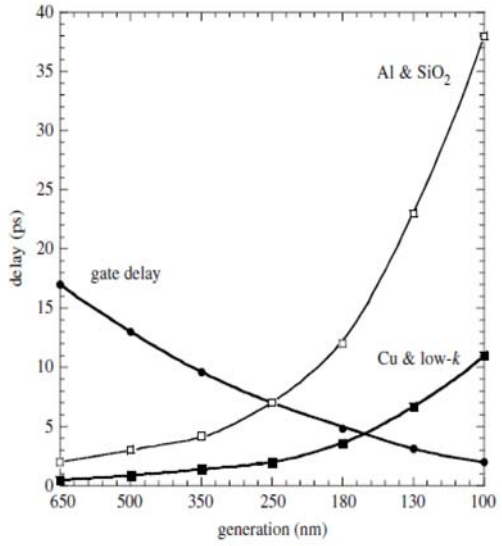

Figure 4.2. The estimated t_{delay} of gate, Al/SiO_2, and Cu/low-κ versus different node technologies. This figure is adapted from the ITRS (1999) [74].

(2) lower the density N of the electric dipoles within the ILD.

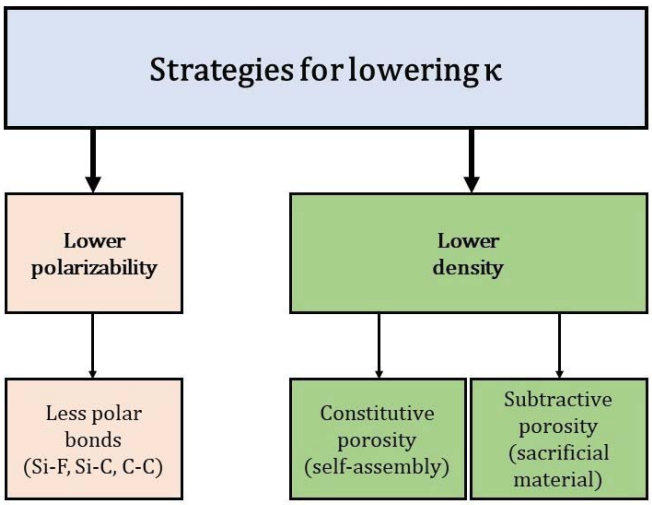

Figure 4.3. Strategies for lowering κ to develop a low-κ ILD.

When an electric field is applied across an ILD, electric dipoles are induced (i.e, di-

electric polarization is caused). As a result, the preexisting and field-induced dipoles are aligned with the applied electric field [12]. The types of dielectric polarizations are electronic, atomic or ionic, orientation, and space-charge [12]. Thus, the total polarizability α_{p} can be defined as the sum of the contributions of these polarizations. The frequency-dependent total polarizability and κ are related by the Mossotti–Clausius equation [72, 76]

$$\frac{\kappa - 1}{\kappa + 2} = \frac{4\pi}{3} N\alpha_{\mathrm{p}}. \tag{4.4}$$

It can be noticed from Eq. (4.4) that κ grows as $N\alpha_{\mathrm{p}}$ grows. The higher α_{p} and/or N, the higher is κ. Therefore, to develop or engineer a low-κ ILD, a material with low N (i.e., porous) and low α_{p} is needed.

Table 4.1 shows the electronic polarizability of different chemical bonds [72]. The polarizability of a single bond is lower than that of double bonds. However, the bond strength of double bond is higher [72]. When developing a low-κ ILD, the type of these bonds should be also considered since it plays a major role in determining both the polarizability α_{p} and the mechanical strength of the ILD material [72].

Table 4.1. Electronic polarizability and bond strength of different chemical bonds [72].

Bond	**Polarizability** $\mathbf{Å^3}$	**Bond strength** $\mathbf{kcal\ mol^{-1}}$
C–C	0.531	83
C–F	0.555	116
C–O	0.584	84
C–H	0.652	99
O–H	0.706	102
C=O	1.020	176
C=C	1.643	146
C≡C	2.036	200
C≡N	2.239	213

The second strategy aims to lower the mass density of the ILD by introducing

porosity to create a matter-free volume in the ILD material.

Generally, when two homogeneous materials of relative permittivity κ_{a} and κ_{b} are mixed together in a volume ratio $f_{\mathrm{a}} : 1 - f_{\mathrm{a}}$, where $f_{\mathrm{a}} \in [0, 1]$, the relative permitttivity κ_{ab} of the mixture must obey two reasonable constraints: [77]

$$\lim_{f_{\mathrm{a}} \to 1} \quad \kappa_{\mathrm{ab}} = \kappa_{\mathrm{a}}, \tag{4.5a}$$

$$\lim_{f_{\mathrm{a}} \to 0} \quad \kappa_{\mathrm{ab}} = \kappa_{\mathrm{b}}. \tag{4.5b}$$

Therefore, κ of any porous material with ($\kappa_{\mathrm{a}} = \kappa_{\mathrm{air}} = 1$ (air)) and bulk material ($\kappa_{\mathrm{b}} = \kappa_{\mathrm{bulk}}$) is expected to obey the restriction

$$\frac{\kappa_{\mathrm{bulk}}}{[f_{\mathrm{air}}\ \kappa_{\mathrm{bulk}} + (1 - f_{\mathrm{air}})]} \leq \kappa \leq f_{\mathrm{air}} + (1 - f_{\mathrm{air}})\, \kappa_{\mathrm{bulk}}, \tag{4.6}$$

imposed by the Wiener bounds regardless of the microstructure [78, 79]. Accordingly, we expect $\kappa < \kappa_{\mathrm{bulk}}$ for $f_{\mathrm{air}} > 0$.

4.2.2 Leakage current and insulating strength

Every ILD has a finite resistivity leading to a leakage current when a d.c. voltage is applied. The leakage current is due to conduction mechanisms which also control charge transport. Many studies [80–84] have shown that Schottky emission (SC), Poole–Frenkel emission (PF), Fowler–Nordheim tunneling (FN), direct tunneling (DT), trap-assisted tunneling (TAT), and space-charge-limited (SCL) are the most effective conduction mechanisms in dielectric materials. Figure 4.4 shows different possible conduction mechanisms inside a metal-insulator-metal (MIM) structure.

The conduction mechanisms can be classified into two types: electrode-limited and bulk-limited [81]. The electrode-limited conduction mechanisms such as SC, FN, and DT depend on the electrical properties of the electrode/insulator interface.

Bulk-limited conduction mechanisms such as PF, TAT, and SCL depend on the electrical properties of the insulator (i.e., traps' location and density). These conduction mechanisms also depend on the operating conditions such as bias voltage and temperature.

When the applied voltage keeps increasing, the ILD cannot sustain this increase in the voltage that will lead eventually to a runway current. The maximum voltage per unit thickness is called the dielectric strength or breakdown electric field E_{bd} [72], which appears to be dependent on the thickness of the ILD.

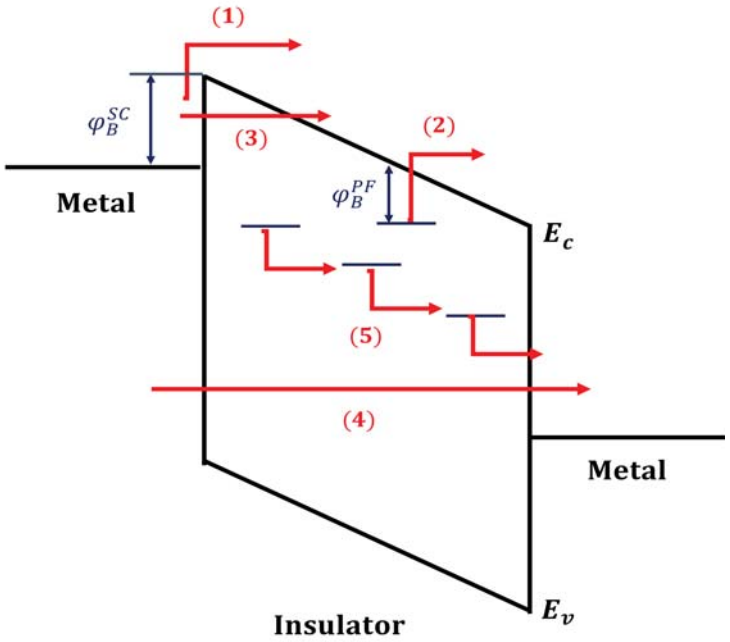

Figure 4.4. Different possible conduction mechanisms in a MIM structure: (1) Schottky emission, (2) Poole–Frenkel emission, (3) Fowler–Nordheim tunneling, (4) direct tunneling, and (5) trap-assisted tunneling. The parameters ϕ_B^{SC} and ϕ_B^{PF} are SC and PF energy barriers, respectively.

4.2.3 Mechanical and thermal properties

The development of a low-κ ILD poses two main challenges [75]. The first challenge is the deposition of a uniform and porous ILD film using approaches as the ones given in Fig. 4.3. The second challenge is the integration of this ILD film into the IC manufacturing processes. Criteria for mechanical, thermal, and chemical stabilities need to be fulfilled by the low-κ ILD material [72, 75].

The mechanical stability is needed primarily because the low-κ ILD material is expected to withstand enormous mechanical stresses during the metal integration process. For instance, Cu integration technique is called "damascene" [72] because Cu lines are embedded in the low-κ ILD and resemble damascene decorations. Then, Cu lines are polished using a chemical-mechanical polishing process that induces enormous mechanical stresses [75]. Also, the degradation of the mechanical properties of the ILD depends on porosity [72]. Therefore, the porosity of the low-κ ILD must be as low as possible to provide sufficient mechanical stability.

The ILD must also be able to endure thermal stresses due to the thermal budget of the integration process and the mismatch in the coefficients of thermal expansion. For example, a low-κ ILD is expected to withstand a high processing temperature of ~ 400°C [75]. Table 4.2 summarizes the ILD electrical, mechanical, and thermal properties of concern [72].

Table 4.2. Electrical, mechanical, and thermal requirements for ILD [72].

Electrical	**Mechanical**	**Thermal**
Low κ	Film uniformity	High thermal stability
Low dissipation	Good adhesion	Low thermal expansion
Low leakage current	Low stress	Low thermal shrinkage
High dielectric strength	High tensile modulus	High thermal conductivity
Low charge trapping	High hardness	
High reliability	Low weight loss	

4.3 Overview of interlayer-dielectric materials

In 1997, IBM and Motorola successfully introduced Cu to replace Al as the metal interconnect using very-large-scale integration (VLSI) technique [85]. This was the first attempt to reduce t_{delay} since Cu has 40% lower resistivity than Al [74]. In 2000, fluorinated silicon glass (FSG) SiOF, with $\kappa \sim 3.6$, was integrated to replace SiO_2 in the 180-nm technology node [74, 85]. The use of Cu and FSG effectively reduced t_{delay} by 50% [74, 85]. Due to size shrinking of the later technology nodes, reduction of t_{delay} has become more important. Industry and academia have worked on developing and including new materials and structures with κ lower than that of FSG [74].

In 2004, the first non-SiO_x ILD was successfully integrated into the 90-nm technology node [85]. It was organosilicate glass deposited by plasma-enhanced chemical vapor deposition (PECVD) and has $\kappa \sim 3.0$ [86–89].

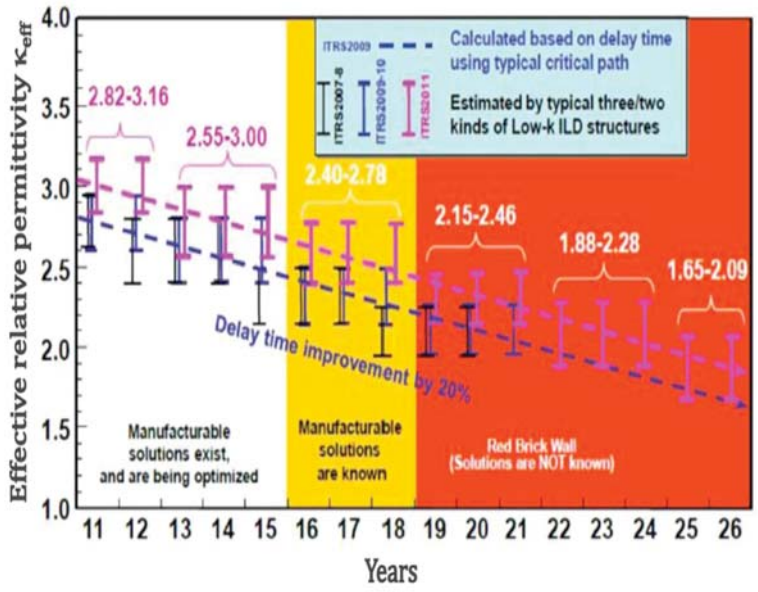

Figure 4.5. Predicted values of low κ and ultralow κ for ILDs according to the ITRS (2013) [74].

Currently, porous organosilicate thin films (a-SiOC:H) deposited also with PECVD are the dominant choice for low-κ ILD ($\kappa > 2.2$) and are also potential candidates for ultralow-κ ILD ($\kappa < 2.2$). During the deposition, sacrificial organic polymers (porogens), such as tetra methyl cyclol tetra siloxane (TMCTS) [87], are co-deposited with matrix materials, such as a silica-like matrix. The sacrificial porogens are used to create a random porous microstructure inside the material. During the curing step, most of this organic material is thermally decomposed, whereby the original occupied sites are converted into microporous/nanoporous sites. The value of κ and the quality of the thin film depend highly on the matrix materials and the porogens.

According to the International Technology Roadmap for Semiconductors (ITRS) shown in Fig. 4.5 [74], ILDs with $\kappa \sim 2.4$ can be used for the 10-nm-technology node, but ILDs with $\kappa \sim 2.3$ will be needed for the 7-nm technology node. In 2013, the ITRS community announced that ILDs with $\kappa < 2.2$ will be needed in the sub-7-nm technology node [74, 89].

Increasing porosity effectively reduces κ [90]. However, the porosity increase comes at a price. The mechanical stability of porous a-SiOC:H films will seriously degrade and probably fail during ICs fabrication [89, 91]. Tight control of both pore distribution and shape is necessary for $\kappa < 2.2$ [91], but porous a-SiOC:H films have a randomly ordered pore structure [89]. Hence, new concepts of ILD integration are being developed nowadays besides efforts to produce materials with $\kappa < 2.2$ [74,89,91].

Self-assembled materials may be useful for the next generation of ultralow-κ ILDs [91–93]. Indeed, metal-organic frameworks [92, 93], periodic mesoporous organosilicates [89, 91], and vertically aligned cylindrical pores assisted by vertically grown carbon nanotubes [94, 95] have been proposed for ultralow-κ ILDs.

Chapter 5
Parylene-C Columnar Microfibrous Thin Films

5.1 Introduction

Columnar microfibrous thin films (μFTFs) are self-assembled microstructured films that can be classified as sculptured thin films (STFs). In general, STFs constitute a distinctive class of micro/nanostructured thin films that contain nominally identical and parallel micro/nano-columns with engineered shape [96]. The STF morphology can be engineered using the oblique-angle deposition technique [97], wherein the substrate holder is rotated and/or tilted with respect to the average direction of a collimated vapor flux directed towards the substrate, the whole process taking place at a low pressure.

Different kinds of materials have been successfully fabricated as STFs [96, 98]. These include organic and inorganic materials such as oxides [99–101], nitrides [102,103], polymers [104–106], and metals [105,107,108]. The morphology of STFs can be categorized into different types such as slanted columnar, chevronic, and chiral, as shown in Fig. 5.1 [96, 98, 109]. These morphologies have been employed in various electronic [98, 110], optical [111–113], and biomedical [110] devices. Researchers in our group at the Pennsylvania State University continue to make progress in exploring and revealing the electrical, mechanical, optical, and acoustical properties of STFs [113–120].

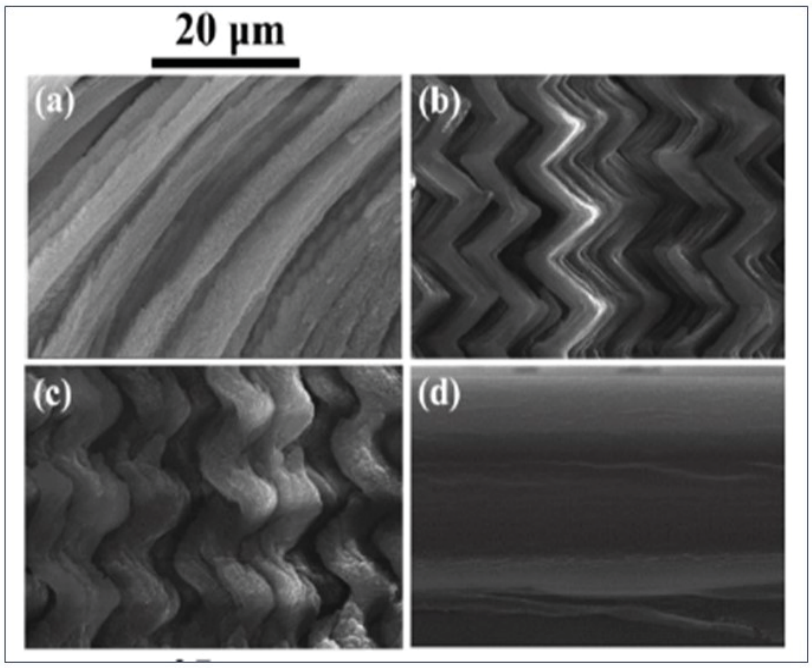

Figure 5.1. Cross-sectional images of STFs of different morphologies: (a) slanted columnar, (b) chevronic, and (c) chiral. Cross-sectional image of (d) a pinhole-free bulk thin film.Reproduced from Ref. [109].

5.1.1 Fabrication of STFs

In physical vapor deposition (PVD), a vapor flux generated from a material in a vacuum chamber is physically transferred toward a substrate on which the vapor condenses to form a solid thin film. The vapor flux can be created either thermally [106] or by bombardment by electrons [105], plasmas [102], or lasers beams [121]. Typically, the substrate is fixed during deposition.

The basic feature of the fabrication of STFs is to employ a typical PVD system with a substrate that can be tilted and/or rotated during deposition [96]. A collimated part of the vapor flux from the solid source arrives at the surface of the substrate. As a result, an assembly of parallel and shaped columns grows on the substrate [122].

As depicted in Fig. 5.2, the collimated vapor flux is directed at an angle $\chi_v \in$

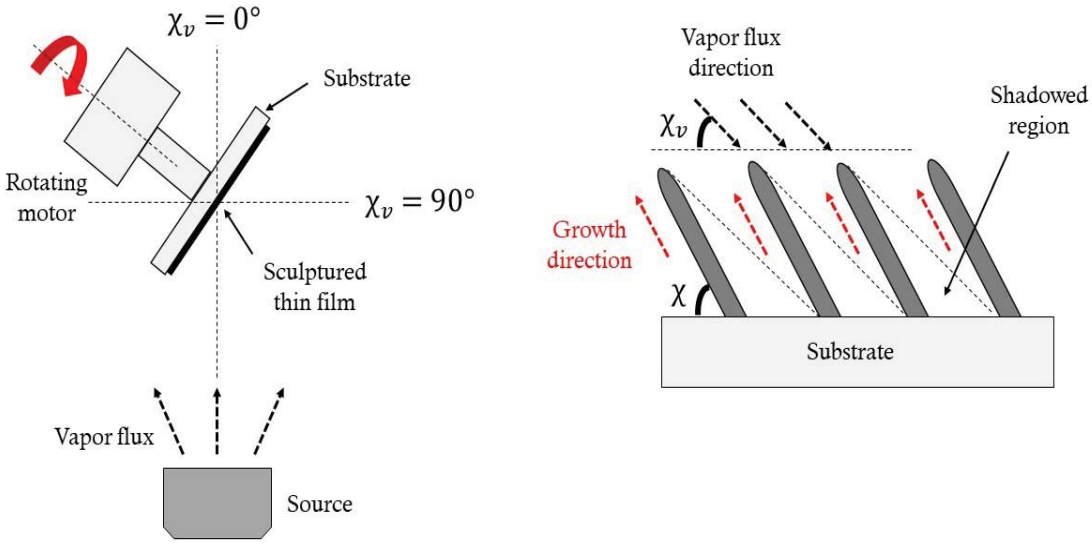

Figure 5.2. Schematic diagram represents the deposition angle and the growth direction of a slanted columnar STF. A collimated vapor flux is directed at an angle $\chi_v \in (0°, 90°]$ and the growing columns are tilted at an angle $\chi \in (0°, 90°]$.

$(0°, 90°]$ (i.e., deposition angle), and the grown columns are inclined at an angle $\chi \in (0°, 90°]$ (i.e., tilt angle) with respect to the substrate, when the substrate orientation is fixed. Generally, χ is larger than χ_v, except for $\chi_v = 90°$ (when the substrate holder is perpendicularly fixed) when $\chi = \chi_v$.

Different STF morphologies can be achieved such as slanted columnar, chevronic, or chiral, as shown in Fig. 5.1. When the substrate is tilted at a fixed χ_v but not rotated, a columnar morphology is realized [96, 123, 124]. A nematic morphology is obtained by changing χ_v as a function of time [96, 123]. By rotating the substrate, chiral morphology is realized when χ_v is fixed [96, 123]. Both rotation and tilting can be done at the same time [96].

5.1.2 Growth mechanics

As illustrated in Fig. 5.3, when a vapor flux arrives at the substrate surface, the vapor particles or atoms are either reflected or (physically) adsorbed [125, 126]. In the later case, the adsorbed clusters of atoms are called adatoms. Adatoms often move some distance tangential to the surface of the substrate (i.e., diffusion). During the diffusion process, adatoms may either desorb (i.e., release) or collide with other adatoms to form cluster called a nucleus.

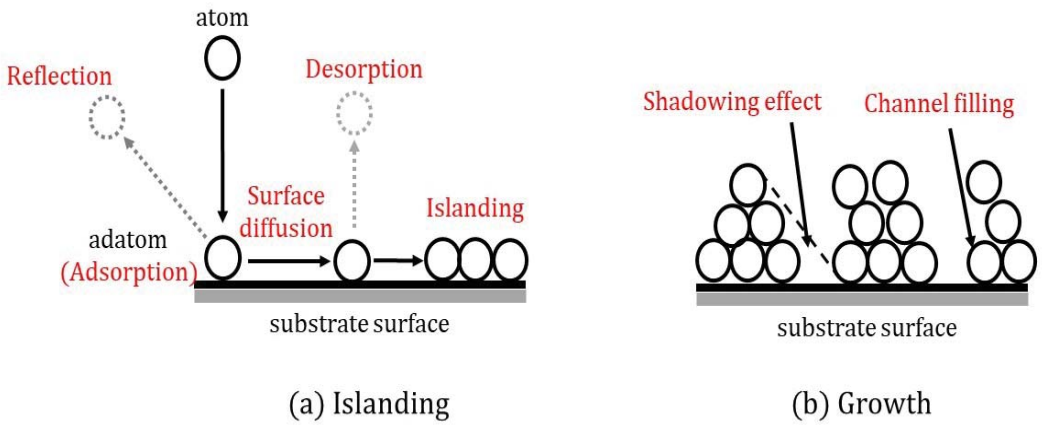

Figure 5.3. Schematic diagram of growth process of STFs.

After adsorption and collision, the adatom becomes less mobile. At this stage, the adatom tends to bond to the surface as the nuclei grow larger. When a nucleus reaches a certain size, it acts like an anchor for other adatoms. As a result, an island of bonded adatoms and gaps in between is created. Gaps between neighboring islands decrease as the film grows.

Typically, the substrate is tilted when fabricating a STF. Therefore, the accumulated adatoms effectively shadow some parts of the surface of the substrate and prevent the landing of other incoming adatoms. This process is called self-shadowing. It enhances the formation of voids and channels between islands [97, 122]. Islanding and

self-shadowing processes lead to the formation of slanted columnar morphology.

The temperature and pressure play major roles in the formation of the STF. The ratio of the substrate temperature T_s to the melting point T_m of the vaporized material affects the formation (i.e., columnar growth) of the deposited thin film, as codified in structure zone models (SZM) [97, 122]. SZMs have been extensively used to classify the morphological evolution of thin films deposited by PVD techniques [97, 122]. They provide guidelines on the evolution of thin-film morphology and its dependence on the processing parameters such as pressure and the ratio T_s/T_m [97, 122].

As the ratio T_s/T_m increases, the mobility of the adatoms increases. As a result, the surface diffusion of the adatoms increases and leads to the formation of a denser film. Therefore, the formation of STFs requires low adatom surface mobility that can be obtained by adjusting the ratio T_s/T_m for a fixed pressure.

The deposition of a STF also depends on the deposition pressure. At low pressure, the mean free path (i.e., the average distance that a particle can travel without collisions with other particles) of the atoms of the vapor flux is long. As a result, the degree of the collimation in the vapor flux is effectively enhanced. Also, this increases the surface diffusion of the adatoms.

By controlling and adjusting temperature and pressure, we can manage the influence of the adatom diffusion, which impacts the formation and growth of the STFs [96–98, 122, 125, 126].

5.2 Deposition of Parylene-C bulk and columnar μFTFs

5.2.1 Deposition of bulk Parylene-C thin film

Two types of Parylene-C films were studied for this dissertation: bulk films and columnar μFTFs. Bulk Parylene-C films are fabricated by a standard physicochemical

process known as the Gorham process [127] illustrated in Fig. 5.4. This process is used to conformally coat various solid objects or surfaces with completely pinhole-free bulk Parylene-C films for insulating purposes [38].

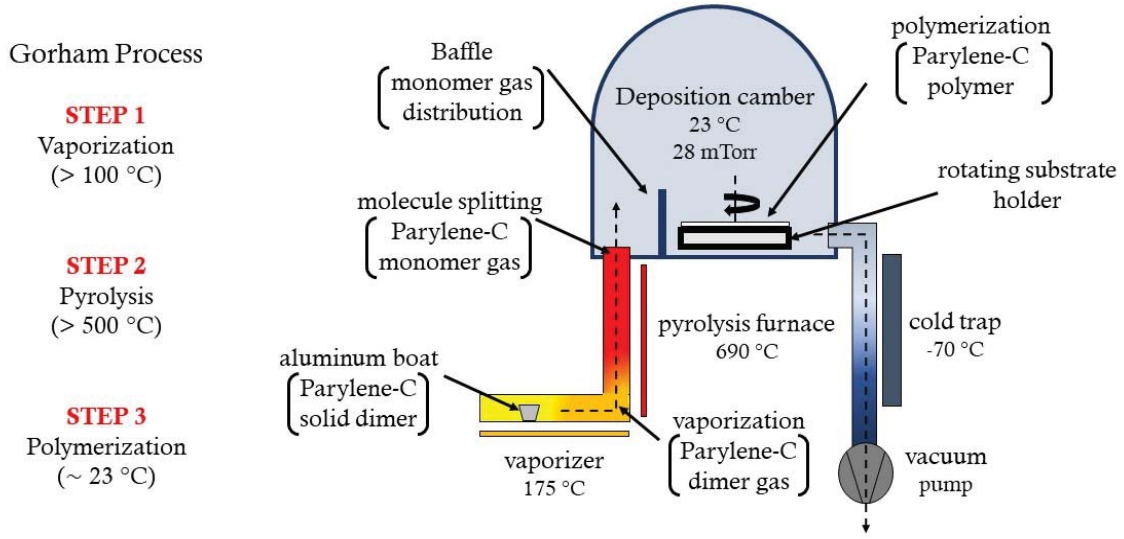

Figure 5.4. Schematic diagram of the Gorham process to deposit a bulk film of Parylene C.

The PDS 2010 Labcoater (Specialty Coatings and Systems, IN, USA) shown in Fig. 5.5(a) is often used for coating objects with parylenes [38]. In the Gorham process, a certain amount of commercially available Parylene-C dimer (980130-C-01LBE, Specialty Coatings and Systems, Indianapolis, IN, USA) is first vaporized in a vaporizer at 175 °C and then pyrolyzed into a reactive-monomer vapor at 690 °C inside a furnace. To ensure a uniform coating, the reactive-monomer vapor is passed over a baffle into a reduced-size vacuum chamber (Fig. 5.5(b)) maintained at 2.8×10^{-2} Torr. Then, the reactive-monomer vapor diffuses onto the surface of a substrate (or object) affixed to a rotating platform. The diffused monomers condense and polymerize on the exposed surfaces of the substrate to form a solid film. Bulk Parylene-C thin films of different thicknesses can be deposited by adjusting the

amount of Parylene-C dimer.

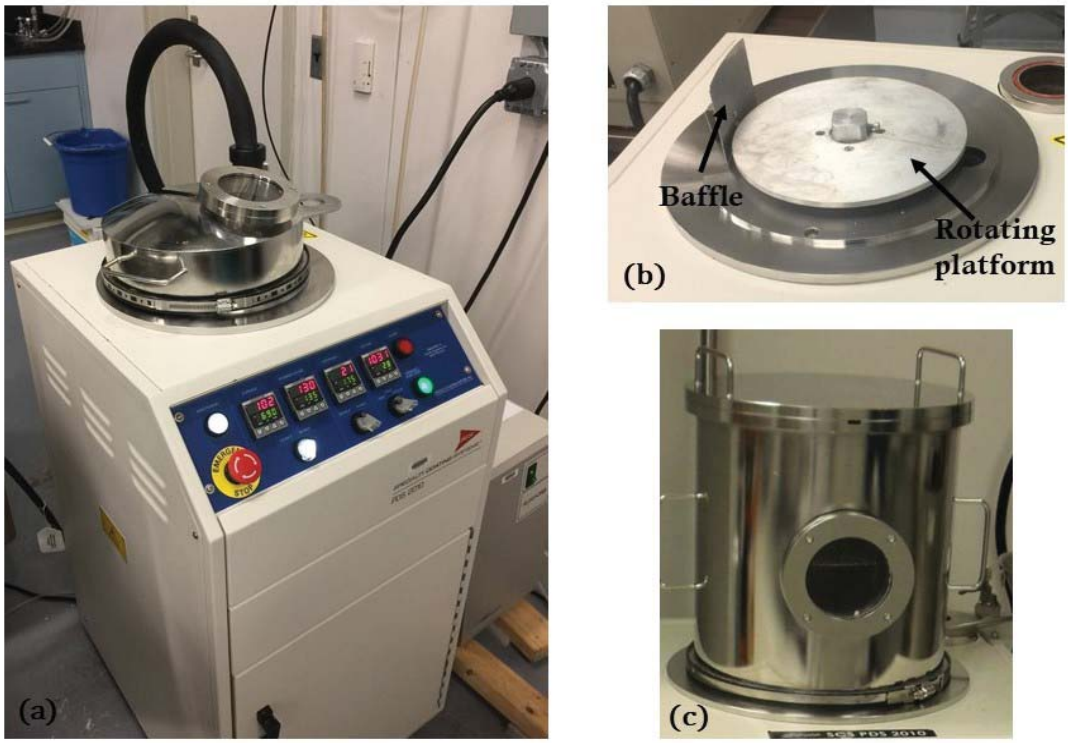

Figure 5.5. (a) PDS 2010 Parylene Labcoater (Specialty Coatings and Systems, IN, USA) using (b) a reduced-size deposition chamber or (c) a modified large-size deposition chamber.

5.2.2 Parylene-C columnar μFTFs deposition

Columnar μFTFs of Parylene C are grown using an oblique-angle variant of the standard Gorham process. Parylene-C dimer is first loaded inside the vaporizer of a modified Parylene Labcoater using the large-size chamber shown in Fig. 5.5(c). The dimer is first vaporized at 175 °C and then pyrolyzed into a reactive-monomer vapor at 690 °C inside the furnace.

Unlike for bulk Parylene-C deposition, the baffle is replaced with a nozzle. Basically, the reactive-monomer vapor provided by the furnace is non-directional, which is not

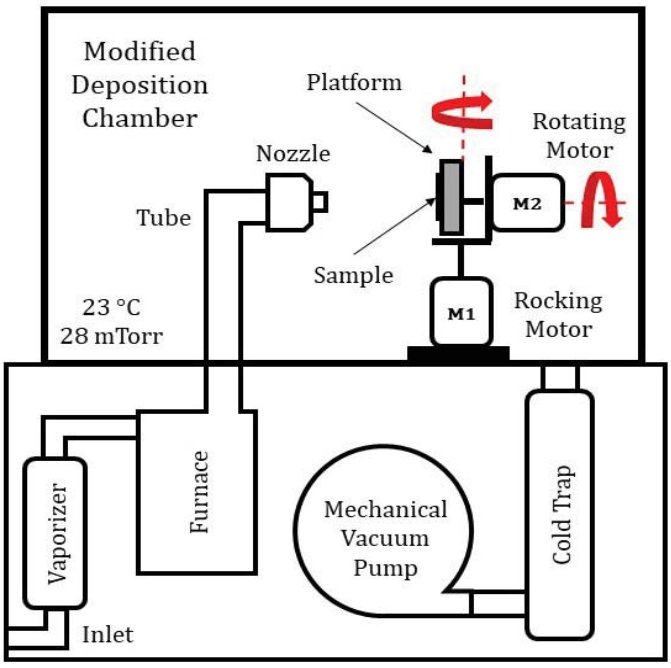

Figure 5.6. Schematic diagram of the PDS2010 Parylene Labcoater modified by incorporating a large-size deposition chamber.

compatible with the formation of STFs [96]; therefore, the nozzle is introduced to provide the essential directionality or collimation. This procedure was established by Pursel et al. [106].

The reactive-monomer vapor is collimated through a tube and released through a nozzle toward a substrate. This substrate is attached to a controllable platform in a large-size vacuum chamber of the modified Parylene Labcoater illustrated in Fig. 5.6. This vacuum chamber is also maintained at 2.8×10^{-2} Torr. When the collimated vapor flux arrives at the tilted substrate surface, self-shadowing controls the growth of the columnar μFTF , as described in Sec. 5.1.2. Columnar μFTFs of different thicknesses can be deposited by adjusting the amount of Parylene-C dimer.

5.3 Fabrication of MIS and MIM structures

P-type silicon (p-Si) substrates were ultrasonically cleaned in an ultrasonic cleaner (2200 Branson, Emerson, St. Louis, MO, USA) with acetone, deionized (DI) water, isopropyl alcohol, and DI water for 10 min each. Later, the cleaned substrates were etched for 20 min using a 1:4 mixture of hydrofluoric acid and DI water. A 150-nm-thick layer of silicon dioxide (SiO_2) was then deposited atop the p-Si substrate using a PECVD tool (P-5000, Applied Materials, Santa Clara, CA, USA). Thereafter, a 50-nm-thick adhesion layer of chromium (Cr) was deposited using a sputter tool (Desktop Pro ®, Denton Vacuum, Moorestown, NJ, USA). Next, a 150-nm-thick gold (Au) layer was sputtered on top of the Cr layer using the same tool.

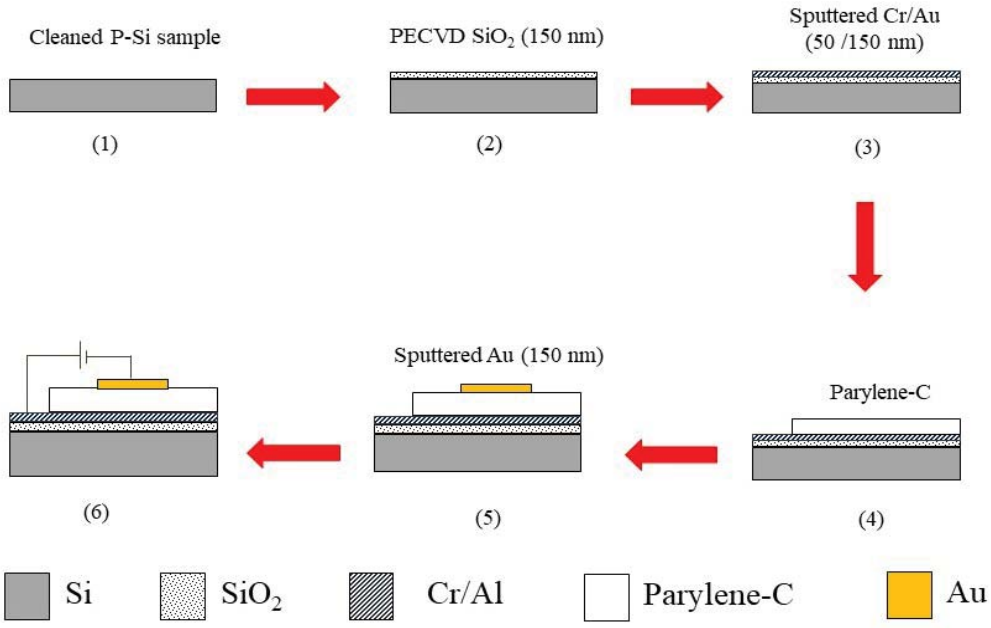

Figure 5.7. Fabrication process of an MIM structure incorporating bulk or columnar μFTF Parylene-C as an insulator.

To fabricate a MIM structure, either a bulk thin film or a columnar μFTF of

Parylene C was then deposited on top of the Au layer as an insulating thin film. During that deposition, the Au/Cr/SiO_2/p-Si structure was fixed inside the deposition chamber. To complete the MIM structure, a 150-nm-thick circular disk of Au was sputtered on top of Parylene-C layer using a mask. The area A of the circular disk was fixed at $A = 78.5$ mm^2. The Au disk at the top and the Au layer at the bottom were used as the two metal electrodes for the MIM structure. Other MIM structures were fabricated using Al layers as the two metal electrodes. The fabrication process is illustrated in Fig. 5.7.

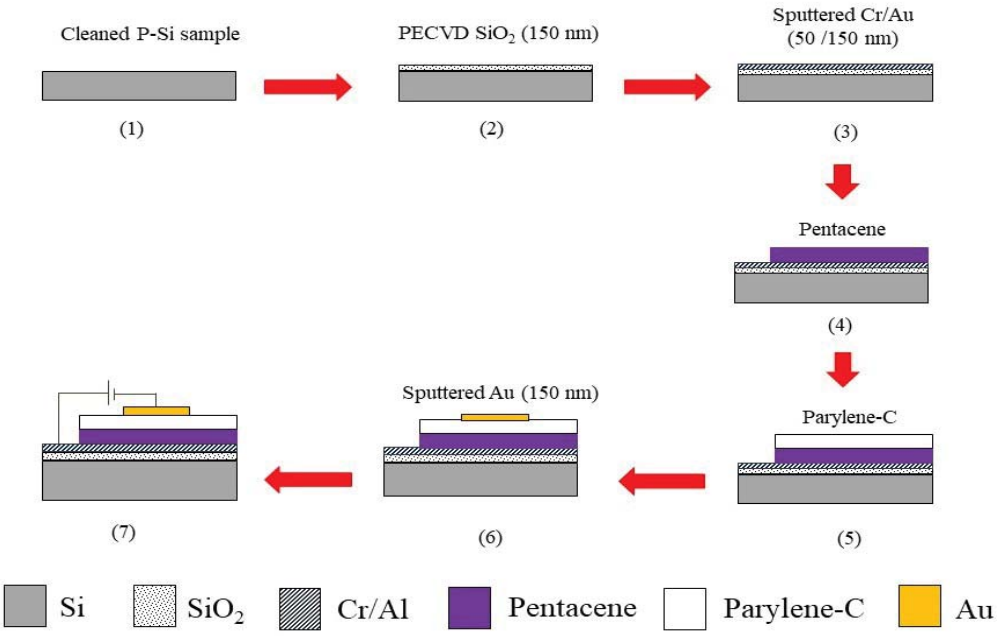

Figure 5.8. Fabrication process of an MIS structure incorporating bulk Parylene-C as an insulator.

To fabricate a MIS structure, Pentacene was purified in a gradient-temperature sublimation system (MK-5024-S, Lindberg Electric, Water-town, WI, USA) and then loaded in a tubular chamber. A thermal gradient was maintained along that chamber at about 10^{-5} Torr. The material was sublimated at 300 °C and re-condensed down

the tube at 165 °C in order to drive out impurities. A 150-nm-thick layer of purified Pentacene was then deposited atop the Au layer via vacuum thermal evaporation (Amod, Angstrom Engineering, Kitchener, ON, Canada) at a rate of 0.2 nm s^{-1}. During that process, the Au/Cr/SiO_2/p-Si structure was fixed to a rotating chuck and maintained at 0 °C in a chamber with a base pressure of 10^{-7} Torr.

An insulating layer of bulk Parylene C was deposited on top of the Pentacene/Au /Cr/SiO_2/p-Si structure. Finally, a 150-nm-thick circular disk of Au was sputtered on top of the bulk Parylene-C insulating layer using a shadow mask to form the gate of an Au/bulk Parylene-C/Pentacene structure above the Au/Cr/SiO_2/p-Si bottom structure. The area of the circular disk was set as $A = 7.1 \times 10^{-2}$ cm^2. The fabrication process is illustrated in Fig. 5.8.

In the following chapters, the suitability of self-assembled columnar μFTFs of Parylene C as ILDs is examined. The mechanical and electrical properties of Parylene-C columnar μFTFs are correlated to the porosity, crystallinity, and deposition angle. Moreover, electrical characterization using current-voltage-temperature experiments are analyzed to study the the d.c. and a.c. conduction mechanisms and charge transport in Parylene-C columnar μFTFs, and their stability under constant-voltage stress (CVS). Finally, the degradation caused by CVS is investigated to explore the stability of the bulk Parylene-C as a gate dielectric in flexible electronics.

Chapter 6
Morphology Effects on Mechanical and Dielectric Properties

6.1 Introduction

In this chapter[1], a systematic study is presented to relate κ as well as porosity p and mechanical flexibility to the deposition angle χ_v. Several Parylene-C columnar μFTFs were grown with $\chi_v \in \{30°, 52°, 60°, 67°, 80°, 90°\}$. The Parylene-C columnar μFTFs were characterized for morphology using field emission scanning electron microscope (FESEM) images, mass-density measurements to determine porosity, and measurements of static Young's moduli and yield strengths to determine flexibility. Also, MIM structures, each incorporating a Parylene-C columnar μFTF as the insulator layer, were investigated for their dielectric characteristics by measuring their capacitances.

[1]This chapter is substantially based on the following paper: Ibrahim H. Khawaji, Chandraprakash Chindam, Osama O. Awadelkarim, and Akhlesh Lakhtakia, "Selectablity of mechanical and dielectric properties of Parylene-C columnar microfibrous thin films by varying deposition angle." *Flexible and Printed Electronics*, vol. 2, no. 4, art. no. 045012 (2017).

6.2 Experimental procedure

Twenty seven p-Si substrates, 3×3 cm^2 in size, were ultrasonically cleaned, as described in Sec. 5.3, and all substrates were left overnight to dry in closed petri dishes. Every substrate was then masked using a tape to leave an unmasked central region of 2×2 cm^2 in size. A columnar μFTF with $\chi_v \in \{30°, 50°, 60°, 67°, 80°, 90°\}$ was deposited on top of each Si substrate using 3 g of Parylene-C dimer. Three replicates were made for each chosen value of χ_v. These 18 samples were used for porosity and flexibility measurements.

Also, several MIM structures, each containing a columnar μFTF as the insulator layer, were fabricated with $\chi_v \in \{30°, 60°, 90°\}$. Again, three replicates were made for each chosen value of χ_v. These nine samples were used for dielectric measurements.

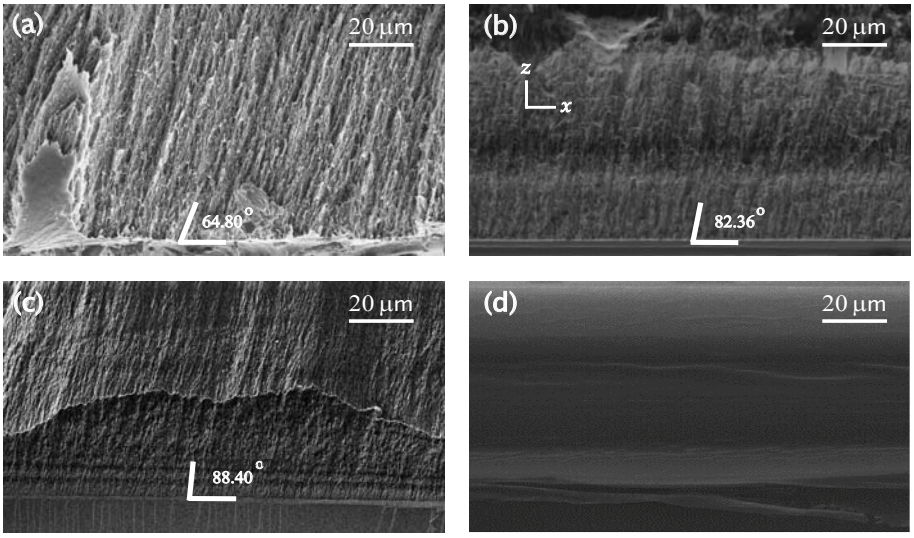

Figure 6.1. Cross-section FESEM images of the morphologically significant planes (xz plane) of Parylene-C columnar μFTFs deposited with (a) $\chi_v = 30°$, (b) $\chi_v = 60°$, and (c) $\chi_v = 90°$. Values of the tilt angle χ of the microfibers are: (a) 64.80°, (b) 82.36°, and (c) 88.40° with respect to the substrate plane (xy plane). (d) Cross-section FESEM image of a film of bulk Parylene C.

6.3 Morphology of Parylene-C columnar μFTFs

The cross-sectional morphologies of 100-μm -thick Parylene-C columnar μFTFs were examined using an FESEM (LEO 1530, Carl Zeiss, Pleasanton, CA, USA). To enhance the FESEM images by eliminating charge accumulation, the cross section of every columnar μFTF was sputtered with iridium (K575X, Emitech, Fall River, MA, USA).

Figures 6.1(a)–(c) show the FESEM micrographs of Parylene-C columnar μFTFs. In contrast with the pinhole-free film of bulk Parylene C shown in Fig. 6.1(d), every columnar μFTF is a group of parallel microfibers inclined at an angle $\chi \in (0°, 90°]$ in the xz plane with respect to the xy plane, the substrate surface plane. The plane in which the microfibers are slanted is called the morphologically significant plane (MSP) and is identified as the xz plane in Fig. 6.1(b) [114]. The microfibers are 3–5 μm in diameter and spaced 2–3 μm apart [47, 128]. The columnar μFTF must therefore by regarded as an anisotropic continuum in the context of mechanical vibrations up to a few tens of MHz in frequency [129, 130], but effectively as an isotropic continuum when used as an insulator layer for electronics [131].

Also, air occupies the inter-microfiber regions. Therefore, a columnar μFTF is a composite material comprising Parylene C and air as its constituent materials. From Figs. 6.1(a)–(c), $\chi = 64.80°,\ 82.36°$, and 88.40° when $\chi_v = 30°$, 60°, and 90°, respectively. Furthermore, χ increases and the porosity decreases with χ_v. Since the dependence of χ on χ_v is already established [128, Fig. 4], the dependence of porosity on χ_v was investigated using mass-density measurements.

6.4 Porosity of Parylene-C columnar μFTFs

The mass of the substrate was measured before and after deposition of the columnar μFTF by an analytical balance (PB303-S, Mettler Toledo, Columbus, OH, USA) with

a resolution of 0.001 g, and thus the mass of the columnar μFTF was determined. The volume of the columnar μFTF was obtained by measuring its top area and thickness.

The porosity p of every columnar μFTF was determined by calculating its mass density ρ_{col} as the ratio of its measured mass to its estimated volume. The measured thicknesses of the columnar μFTFs were found to be between 100 and 200 μm . The volume was calculated with the surface area of the columnar μFTF known to be 2×2 cm^2.

The average mass density ρ_{col} of three replicates for every selected value of χ_v is reported in Table 6.1, the standard deviation being about $\pm 5\%$ of the average values. The data indicate that ρ_{col} decreases with decreasing χ_v so that p should be higher at lower values of χ_v.

A columnar μFTF is a composite material comprising Parylene C and air. With $\rho_{air} = 1$ kg m^{-3} and $\rho_{\text{bulk}} = 1289$ kg m^{-3} as the mass densities of air and bulk Parylene C [38], respectively, the rule of mixtures [77]

$$\rho_{\text{col}} = p\rho_{\text{air}} + (1-p)\rho_{\text{bulk}} \tag{6.1}$$

can be used to determine $p \in [0, 1]$, with the assumption that the mass density of a microfiber is the same as that of the bulk material. As $\rho_{\text{bulk}} \gg \rho_{air}$, Eq. (6.1) yields

$$p = 1 - \left(\frac{\rho_{\text{col}}}{\rho_{\text{bulk}}} \right). \tag{6.2}$$

Figure 6.2 presents the estimated porosities of the Parylene-C columnar μFTFs fabricated with $\chi_v \in \{30^\circ, 52^\circ, 60^\circ, 67^\circ, 80^\circ, 90^\circ\}$. The porosity almost monotonically increases from 0.38 to 0.56 as χ_v decreases from 90° to 30°. This finding strongly supports the claim made from Fig. 6.1 that p decreases with χ_v. Therefore, the

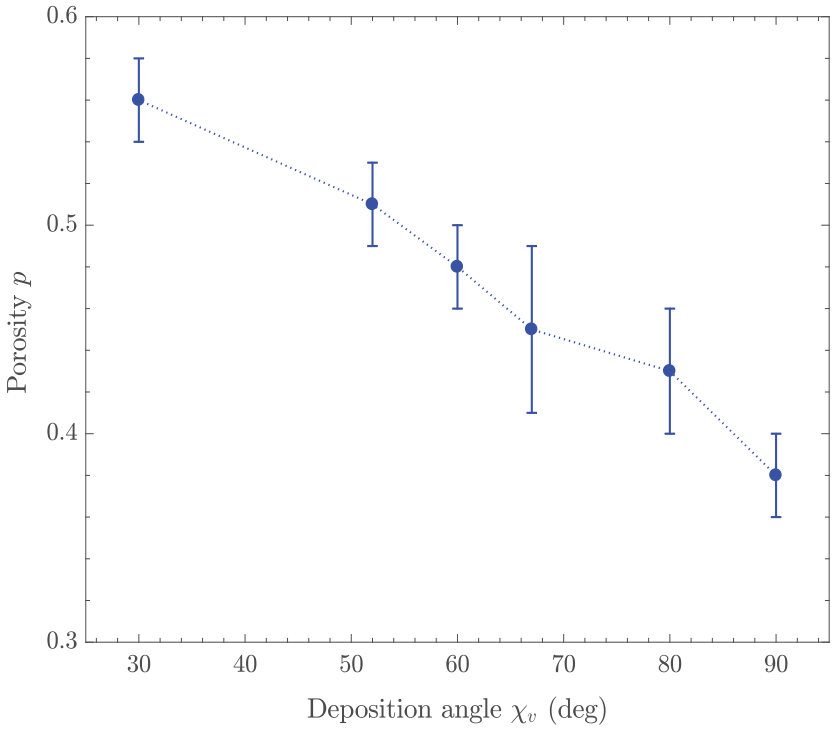

Figure 6.2. Porosity p as a function of χ_v for columnar μFTFs of Parylene C. Error bars show the variation for the three replicates for every selected value of χ_v.

porosity of a Parylene-C columnar μFTF can be selected by choosing an appropriate value of the deposition angle χ_v. Since p increases as χ_v decreases, the relative permittivity κ can be engineered [90].

6.5 Flexibility of Parylene-C columnar μFTFs

Eleven out of the 18 columnar-μFTF samples were used to determine flexibility: two samples each of $\chi_v \in \{30°, 50°, 60°, 67°, 80°\}$ and one sample of $\chi_v = 90°$. To avoid the columnar μFTF curling in the loading direction, the columnar μFTF was carefully and easily peeled off the Si substrate using a razor along either the

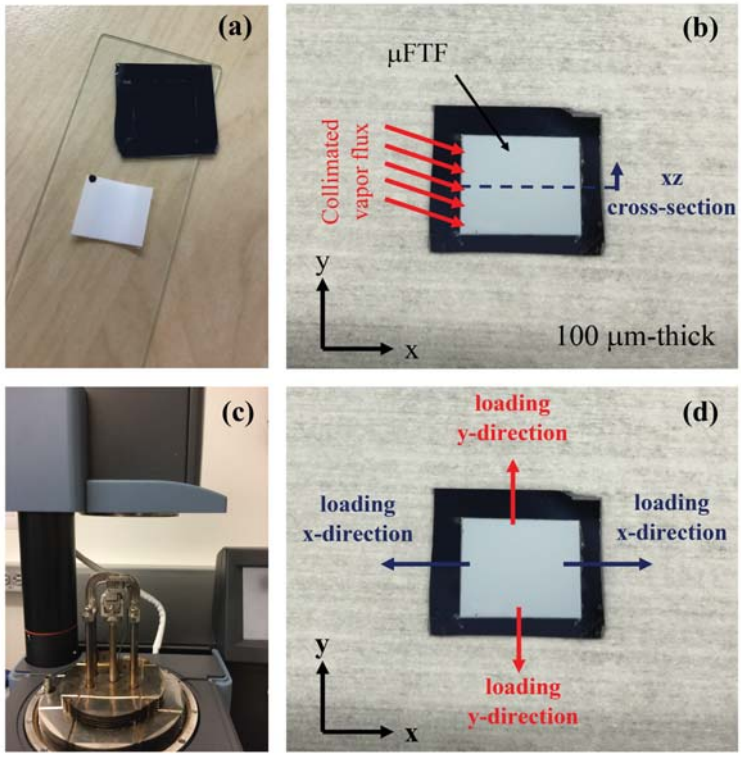

Figure 6.3. (a) Parylene-C columnar μFTF peeled off the Si substrate, (b) the xz plane with respect to the substrate plane (xy plane), (c) the tension clamp of the dynamical mechanical analyzer, and (d) loading application along either x axis or y axis in the xy plane.

x or the y axis and then used to prepare three rectangular samples, as shown in Fig. 6.3(a). The length dimension of the rectangular sample was thus aligned either along the x axis for loading at a constant strain rate along the x axis or along the y axis for loading at a constant strain rate along the y axis as shown in Fig. 6.3(d). The widths and thicknesses of these samples were measured using digital vernier calipers. After loading every rectangular sample in the tension clamp of the dynamical mechanical analyzer (DMA) (Q800, TA Instruments, Newcastle, DE, USA) presented in Fig. 6.3(c), the length of the sample was read from the DMA screen/software.

The width of every rectangular sample was found to lie between 3.0 and 5.0 mm,

the thickness between 0.1 and 0.2 mm, and the length between 6.0 and 9.0 mm. The sample was stretched at 30 μm /min upto a maximum ramp displacement of 180 μm . The values of the tensile force were measured at every 0.5 μm of displacement. The uniaxial stress and strain were determined through the accompanying software by measuring the displacement and force. Both the static Young's modulus and the yield strength of the sample were identified for a specific loading condition from the stress vs. strain curves obtained using the DMA.

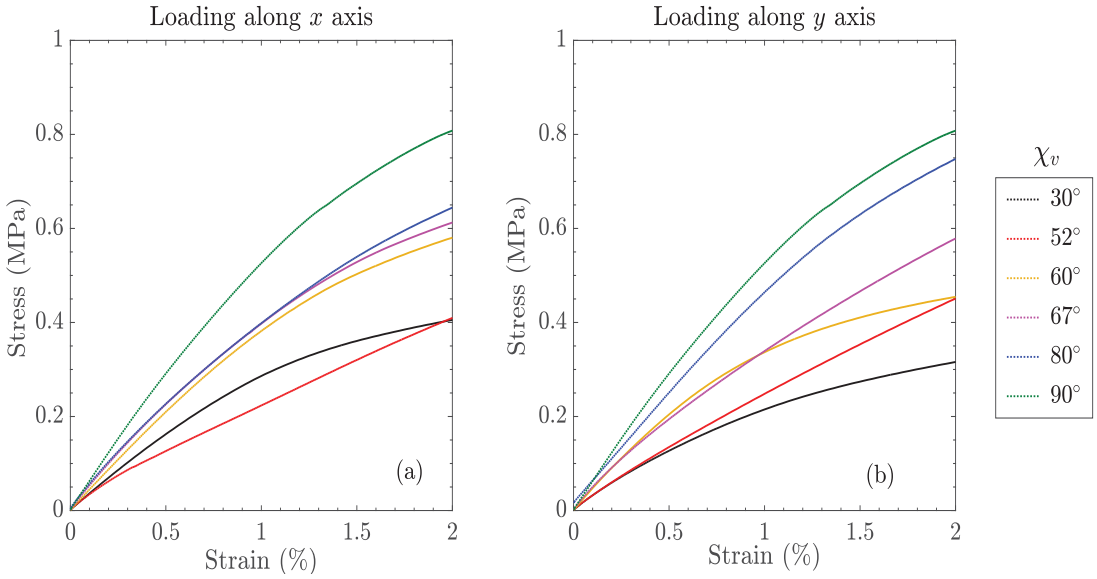

Figure 6.4. Average stress measured as a function of strain of the three replicates of Parylene-C columnar μFTFs fabricated with $\chi_v \in \{30°, 52°, 60°, 67°, 80°, 90°\}$. Loading was applied along either (a) the x axis or (b) the y axis in xy plane.

The dependences of stress on strain for loading along the x and the y axes are shown in Fig. 6.4 for $\chi_v \in \{30°, 52°, 60°, 67°, 80°, 90°\}$. The static Young's moduli ($E_{\parallel}$ and $E_{\perp}$) and the yield strengths ($YS_{\parallel}$ and $YS_{\perp}$) of the Parylene-C columnar μFTFs were determined from the stress-strain curves. The static Young's modulus was determined as the ratio of stress to strain in the linear elastic regime. In Fig. 6.4, the stress-strain curves show no well-defined yield stress points. Therefore, the yield

strength was determined as the value of stress at the intersection of the curve in linear regime and a line with slope as the value of Young's modulus and an offset of strain 0.2% [132, p. 7].

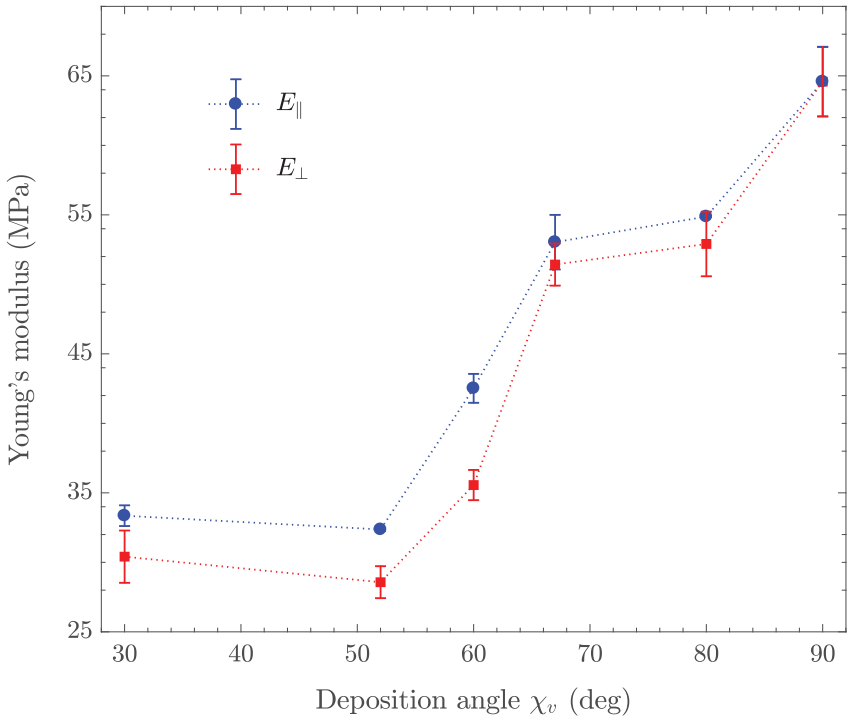

Figure 6.5. Static Young's modulus of Parylene-C columnar μFTFs for loading along the x axis (blue) and the y axis (red) in relation to the deposition angle χ_v. Error bars show the variation for the three replicates for every selected value of χ_v.

Figure 6.5 shows both the static Young's moduli of the columnar μFTFs as functions of χ_v. The Young's moduli increase with χ_v, but this trend is not followed by the samples with $\chi_v = 30°$. The values of $E_{\parallel}$ vary between 32.40 and 64.60 MPa, whereas those of $E_{\perp}$ vary between 28.60 and 64.60 MPa, as tabulated in Table 6.1. The reported values of the static Young's modulus of bulk Parylene C lie between 2.15 and 3.2 GPa [38, 133], in contrast.

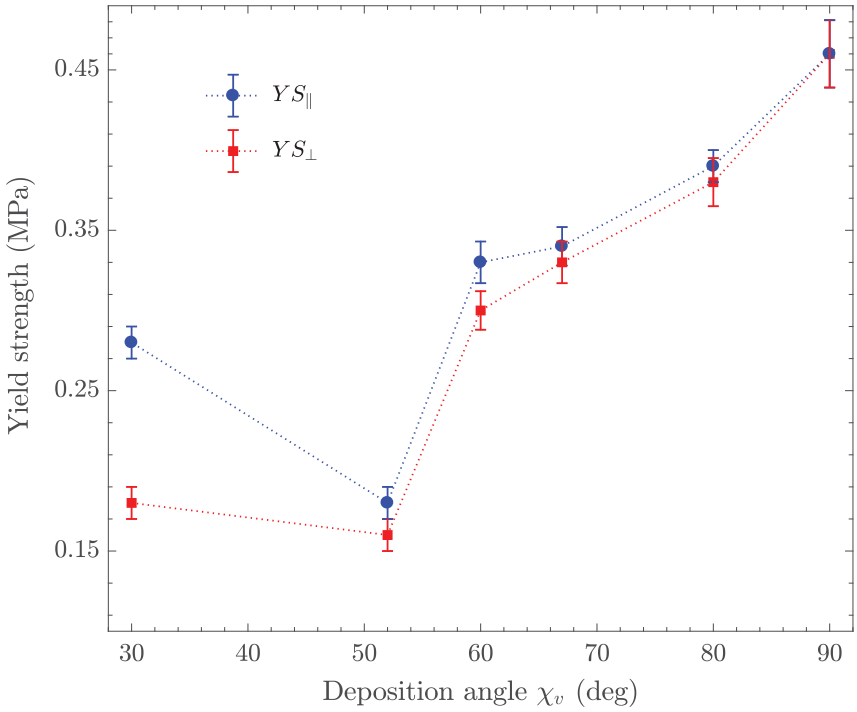

Figure 6.6. Static yield strength of Parylene-C columnar μFTFs for loading along the x axis (blue) and the y axis (red) in relation to the deposition angle χ_v. Error bars show the variation for the three replicates for every selected value of χ_v.

As shown in Fig. 6.6, the yield strength $YS_{\parallel}$ was determined to increase from 0.18 to 0.46 MPa, and the yield strength $YS_{\perp}$ from about 0.16 to 0.46 MPa, as χ_v increases from 52° to 90°. However, samples with $\chi_v = 30°$ have higher $YS_{\parallel}$ and $YS_{\perp}$ than samples with 52° of about 0.28 and 0.18 MPa, respectively. The reported yield strength of bulk Parylene C is 55.1 MPa [38].

Thus, the Parylene-C columnar μFTFs are softer than bulk Parylene C and their softness increases with χ_v. The increased softness of the columnar μFTFs can be attributed to porosity as well as to lower crystallinity than of bulk Parylene C. Whereas the columnar μFTFs have been found to be 55% to 68% crystalline with four

crystal planes, bulk Parylene C is 83% crystalline with only one crystal plane [128]. Hence, in addition to porosity, the softness of the columnar μFTFs can be attributed to the presence of more grain boundaries and low crystallinity.

The dependences of the static Young's moduli and yield strengths on χ_v can be attributed to the decrease of porosity p at higher values of χ_v reported in Sec. 6.4, except that both Young's moduli and yield strengths at $\chi_v = 30°$ do not conform to the general trend, as is evident from Table 6.1. That table also contains available data [128, Fig. 8] on the crystallinity of the columnar μFTFs vs. χ_v, the relationship between the two variables not being monotonic. As flexibility depends not only on the porosity but also on the volumetric density of grain boundaries, the relationship of the Young's moduli to the deposition angle need not be simple.

Table 6.1. Estimated values of mass density, porosity, crystallinity [128], static Young's moduli, and yield strengths of Parylene-C columnar μFTFs deposited with $\chi_v \in \{30°, 52°, 60°, 67°, 80°, 90°\}$. Measurements of the static Young's moduli and yield strengths were made with loading along either the x axis (i.e., in the MSP) or the y axis (i.e., normal to the MSP).

	Mass Density	**Porosity**	**Crystallinity** (Ref. [128])	**Young's Modulus**		**Yield Strength**	
χ_v	ρ_{col} (kg m^{-3})	p	(%)	$E_{\parallel}$ (MPa)	$E_{\perp}$ (MPa)	$YS_{\parallel}$ (MPa)	$YS_{\perp}$ (MPa)
30.0°	566	0.56	60.0	33.4	30.4	0.28	0.18
52.5°	628	0.51	57.4	32.4	28.6	0.18	0.16
60.0°	665	0.48	60.6	42.5	35.5	0.33	0.30
67.5°	711	0.45	67.7	53.1	51.4	0.34	0.33
80.0°	740	0.43	57.2	54.9	52.9	0.39	0.38
90.0°	801	0.38	61.3	64.6	64.6	0.46	0.46

According to Table 6.1, the static Young's modulus for loading along the x axis exceeds the static Young's modulus for loading along the y axis for all values of χ_v selected for this study. Such a dependence on the loading direction was expected,

based on previous results for dynamic loading [133]. During loading along the x axis, each microfiber tends to slide along its neighboring microfibers in the MSP more than when the loading is along the y axis. This leads to higher inter-microfiber friction in the xz plane than in the yz plane, leading to $E_{\parallel} > E_{\perp}$. For these columnar μFTFs, the static Young's moduli are about three times higher than the dynamic Young's moduli at room temperature [133].

Since the Parylene-C columnar μFTFs are softer (i.e., more flexible) than bulk Parylene C, the former have a greater potential for use as insulator layers in flexible electronics. However, the Parylene-C columnar μFTFs have lower yield strengths than bulk Parylene C has. For day-to-day operations, as materials are subjected to stresses within the elastic regime, the Young's moduli are of higher significance than yield strengths. Hence, for flexible electronics, Parylene-C columnar μFTFs are favorable candidates for insulator layers while bulk Parylene-C is to be preferred for substrates.

6.6 Dielectric properties of Parylene-C columnar μFTFs

To determine κ, capacitance measurements were made on nine MIM structures—three replicates each for $\chi_v \in \{30°, 60°, 90°\}$—with an LCR Meter (E4980A, Agilent Technologies, Wilmington, DE, USA) using the parallel mode of 'C-D' option. These measurements were made for 1 kHz, 10 kHz, 100 kHz, and 1000 kHz frequency at room temperature, with $V_{dc} = 1$ V and $V_{ac} = 0.1$ V applied to the sample.

According to the results discussed in Sec. 6.4 and Sec. 6.5, the morphology of Parylene-C columnar μFTFs clearly affects the mechanical properties. Since the porosity decreases as the deposition angle increases, lower values of the relative permittivity κ are expected for columnar μFTFs deposited with lower values of χ_v. In order to examine this hypothesis, capacitance measurements were performed on

nine MIM structures, each containing a Parylene-C columnar μFTF as the insulator layer.

The capacitance C of a MIM structure of area A and thickness d is given by

$$C = \kappa\varepsilon_o \left(\frac{A}{d}\right), \tag{6.3}$$

where $\varepsilon_o = 8.854 \times 10^{-12}$ F m^{-1} is the permittivity of free space. Knowing C, A, and d, one can determine

$$\kappa = \frac{Cd}{\varepsilon_o A}. \tag{6.4}$$

The average thickness of the Parylene-C columnar μFTFs was $d \simeq 83$ μm with standard deviation 0.96 μm . With $A = 78.5$ mm^2, κ was determined using Eq. (6.4) from measured values of C. Room-temperature data on κ vs. χ_v for $\chi_v \in \{30°, 60°, 90°\}$ are presented in Fig. 7.3 at 1, 10, 100, and 1000 kHz.

At all four frequencies, κ decreases with χ_v, as shown in Fig. 6.7. Also, κ decreases as frequency increases, the spectral variation of κ at low frequencies [47] being dominated by the molecular dipole polarization [12, Fig. 7.15]. As χ_v is lowered, κ decreases from 3.31 to 2.25 at 1 kHz and from 2.74 to 2.02 at 1000 kHz. These data are consistent with the decrease of κ of bulk Parylene C from 3.49 to 2.97 at frequencies ranging from 1 kHz to 1000 kHz [47].

In composite materials with semi-crystalline constituent materials, the dependences of κ on porosity and crystallinity have been correlated [134–136]. In this study, as the crystallinity of the columnar μFTFs is lower than of bulk Parylene C [128], the relative permittivity of the former is less than of the latter. Moreover, κ increases with χ_v because p reduces. Higher electrical conductivity of a columnar μFTF compared with that of the bulk material may be attributed to lower crystallinity [47]. Therefore, the lower values of κ for columnar μFTFs can be attributed to higher porosity and

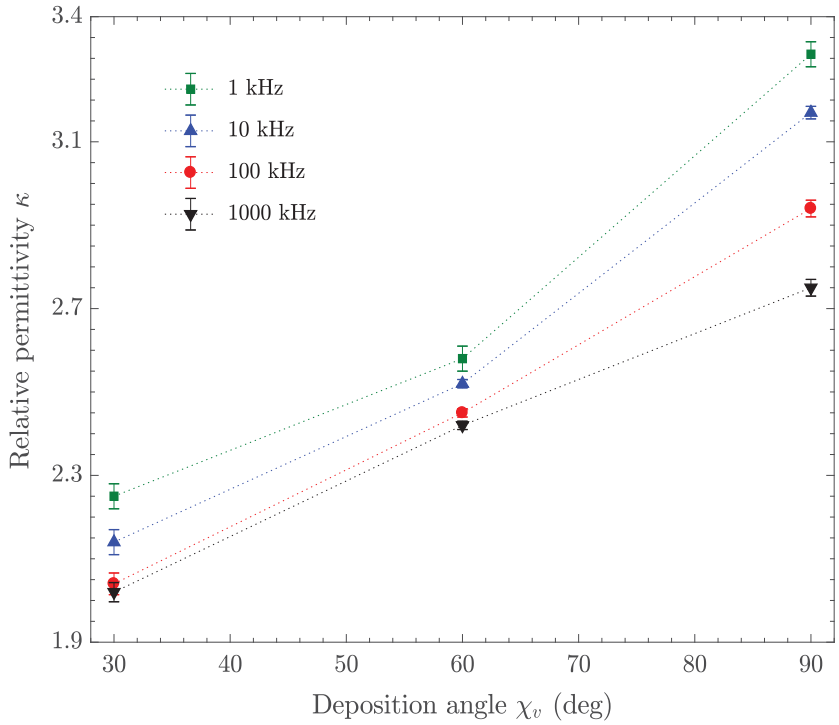

Figure 6.7. Room-temperature relative permittivity of Parylene-C columnar μFTFs in relation to the deposition angle χ_v. Error bars show the variation for the three replicates for every selected value of χ_v.

lowered crystallinity.

At 1000 kHz, as a result, $\kappa = 2.02$ of the Parylene-C columnar μFTF deposited with $\chi_v = 30°$ is significantly lower than the relative permittivity of bulk Parylene C by 30%. In 10-nm Si-based technology, κ ranging between 2.4 and 2.5 is currently suggested for ILD layers [74].

6.7 Concluding remarks

A systematic study of the effects of the morphology on the mechanical and dielectric properties of Parylene-C columnar μFTFs was performed. The Parylene-C μFTFs

were grown using the oblique-angle physicochemical vapor deposition technique wherein a collimated flux of Parylene-C monomers was directed at an angle $\chi_v \in \{30^\circ, 52^\circ, 60^\circ, 67^\circ, 80^\circ, 90^\circ\}$ onto a p-type silicon substrate.

Cross-sectional FESEM images indicated that the porosity of the columnar μFTFs increases with decreasing χ_v, and confirmation was found using mass-density measurements. The porosity of the columnar μFTFs was found to vary between 0.38 and 0.56. Subsequently, the impact of porosity on the flexibility and the dielectric properties was examined using static tension-loading experiments and capacitance measurements, respectively. The differences between the mechanical and dielectric properties of the Parylene-C columnar μFTFs and bulk Parylene C were shown to arise from the differences in their porosity and crystallinity.

The static Young's moduli and the yield strengths are lower for the Parylene-C columnar μFTFs than the corresponding parameters of the bulk counterpart by about two orders of magnitude, making the columnar μFTFs more flexible. The lowest relative permittivity of the fabricated columnar μFTFs in the 1–1000 kHz range was found to be about 70% of that of the bulk material. As the static Young's moduli, yield strengths, and the relative permittivity are functions of χ_v, Parylene-C columnar μFTFs can be engineered using χ_v for multiple roles in flexible electronics. Electrical studies of the suitability of Parylene-C columnar μFTFs as electrical insulators for flexible electronics are presented in Chapters 7 and 8.

Chapter 7

Charge Transport and Conduction Mechanisms in Parylene-C Columnar Microfibrous Thin Films

7.1 Introduction

MIM structures were fabricated, each incorporating a Parylene-C columnar μFTF as the insulator, and investigated for their current-voltage-temperature (IVT) characteristics. The Parylene-C columnar μFTF was fabricated with $\chi_v = 60°$. Measured values of leakage current as functions of temperature, frequency, and applied voltage were analyzed to identify the charge carrier-transport mechanisms in the Parylene-C columnar μFTFs. [1]

7.2 Experimental procedure

The d.c. leakage current I_{dc} was measured using a pA meter (HP 4140B, Hewlett-Packard, Palo Alto, CA, USA). The bias voltage V_{dc} was set to vary between −10 V and +10 V in steps of 1 V at a constant temperature of either 298 K, 323 K, 348 K,

[1] This chapter is substantially based on the following paper: Ibrahim H. Khawaji, Chandraprakash Chindam, Osama O. Awadelkarim, and Akhlesh Lakhtakia, "Dielectric properties of and charge transport in columnar microfibrous thin films of Parylene C," *IEEE Transactions on Electron Devices*, vol. 64, no. 8, pp. 3360–3367 (2017).

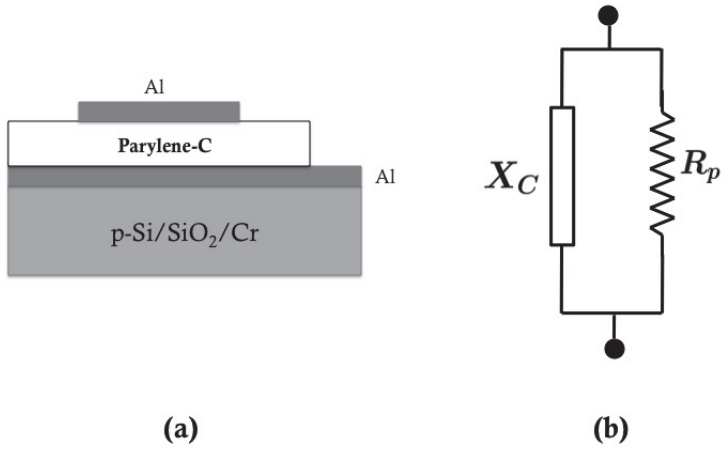

Figure 7.1. (a) Cross section of a MIM structure. (b) An equivalent circuit of the MIM structure, a capacitor C of reactance $X_{\mathrm{C}} = 1/2\pi fC$ in parallel with a resistor of resistance R_{p}, f being the frequency.

373 K, 398 K or 423 K.

The equivalent resistance R_{p} and reactance $X_{\mathrm{C}} = 1/2\pi fC$ of each MIM structure, as shown in Fig. 7.1(b), were measured with a precision LCR Meter (E4980A, Agilent Technologies, Wilmington, DE, USA) using the R_{p}–X_{C} option with the application of a bias voltage V_{dc} that was perturbed by a sinusoidal voltage $V_{\mathrm{ac}} \sin(2\pi ft)$, where f is the frequency. These measurements were made at f of either 1 kHz, 10 kHz, 100 kHz, or 1 MHz and a constant temperature T of either 298 K, 323 K, 348 K, 373 K, 398 K or 423 K with $V_{\mathrm{dc}} = 1$ V and $V_{\mathrm{ac}} = 0.1$ V.

7.3 Charge transport and leakage current

7.3.1 D.C. leakage current

Figure 7.2 presents the IVT characteristics experimentally determined for the MIM structures with the 275-μm-thick columnar μFTF as the insulator. As can be seen from Fig. 7.2(a), the d.c. leakage current $I_{\rm dc}$ increases as the temperature increases, regardless of the value of $V_{\rm dc}$ in the range $[5, 10]$ V. The increase becomes more pronounced as T increases from 373 K to 423 K. Figure 7.2(b), on the other hand, shows $I_{\rm dc}$ as a function of $V_{\rm dc}$ at fixed temperatures ranging from 298 K to 423 K. Irrespective of the polarity of $V_{\rm dc}$ in the range $[-10, 10]$ V, $I_{\rm dc}$ increases non-linearly with increasing $|V_{\rm dc}|$, especially at temperatures above 373 K.

Although a d.c. current of magnitude 10^{-13}A is considered low, HP 4140B is designed for stable and high-resolution current measurements with a maximum resolution of 10^{-15} A. Thus, the data presented in Fig. 7.2 are reliable.

D.C. electron transport in the MIM structure occurs primarily through the Poole–Frenkel (PF) mechanism when the conduction is bulk-limited [137, 138]. Schottky (SC) emission mechanism occurs when the conduction is electrode-limited [137, 138]. For the Poole–Frenkel emission mechanism, the d.c. current density [138, 139]

$$J^{\rm PF} \propto E_{\rm dc} \exp\left[\frac{q_e}{k_B T}\left(2\alpha E_{\rm dc}^{1/2} - \Phi_{\rm B}^{\rm PF}\right)\right], \tag{7.1}$$

where $E_{\rm dc} = |V_{\rm dc}|/d$ is the magnitude of the d.c. electric field, $\Phi_{\rm B}^{\rm PF}$ is the Poole–Frenkel barrier energy, $q_e = 1.6 \times 10^{-19}$ C is the elementary charge, k_B is the Boltzmann constant, $\alpha^2 = q_e/4\pi\varepsilon_o\kappa_\infty$, and κ_∞ is the high-frequency relative permittivity of the

insulator. For the Schottky emission mechanism, the d.c. current density [139]

$$J^{\mathrm{SC}} \propto T^2 \exp\left[\frac{q_e}{k_B T}\left(\alpha E_{\mathrm{dc}}^{1/2} - \Phi_{\mathrm{B}}^{\mathrm{SC}}\right)\right], \tag{7.2}$$

where $\Phi_{\mathrm{B}}^{\mathrm{SC}}$ is the Schottky barrier energy.

While the d.c. leakage current inside the Parylene-C μFTF in the MIM structure could be governed by the Poole–Frenkel mechanism, it could be governed by the Schottky mechanism at the two μFTF/metal interfaces [82,139]. As can be seen from Fig. 7.2, (i) there are clear non-linear dependences of I_{dc} on V_{dc} and (ii) I_{dc} increases with T as predicted for both emission mechanisms. As the thickness $d = 275$ μm of the Parylene-C μFTF in the MIM structure is fairly large, direct tunneling does not play any role in the leakage phenomenon. Since $\alpha E_{\mathrm{dc}}^{1/2} \sim 10^{-3}$ V is much smaller than the barrier energies, $\Phi_{\mathrm{B}}^{\mathrm{PF}} - 2\alpha E_{\mathrm{dc}}^{1/2} \simeq \Phi_{\mathrm{B}}^{\mathrm{PF}}$ and $\Phi_{\mathrm{B}}^{\mathrm{SC}} - \alpha E_{\mathrm{dc}}^{1/2} \simeq \Phi_{\mathrm{B}}^{\mathrm{SC}}$. Therefore, the dependence of I_{dc} on E_{dc} is very likely due to the Poole–Frenkel emission mechanism.

In order to validate this conjecture, the plots of (i) $\ln(J_{\mathrm{dc}}/E_{\mathrm{dc}})$ vs. $E_{\mathrm{dc}}^{1/2}$ shown in Fig. 7.3 and (ii) $\ln(J_{\mathrm{dc}}/T^2)$ vs. $E_{\mathrm{dc}}^{1/2}$ shown in Fig. 7.4 for the MIM structure containing the 275-μm-thick Parylene-C μFTF at 348 K, 373 K, and 398 K were examined; here $J_{\mathrm{dc}} = I_{\mathrm{dc}}/A$. The area A of the top electrode was fixed at 78.5 mm^2. Equation (7.2) fits the measured data with linear regression factor R-squared = 0.89, 0.77, and 0.96 at 348 K, 373 K, and 398 K, respectively, whereas Eq. (7.1) fits the measured data with R-squared = 0.99 at all three temperatures. Therefore, the Poole–Frenkel emission mechanism dominates over the Schottky emission mechanism at temperatures not exceeding ∼373 K, but that dominance fades as the temperature rises further.

Parylene C has been reported to be stable in air for 10 years at 353 K [38]. Also, while conducting X-ray diffraction experiments [128], it was found that exposure to temperature between 233 K and 398 K for 10 min did not change the crystal planes.

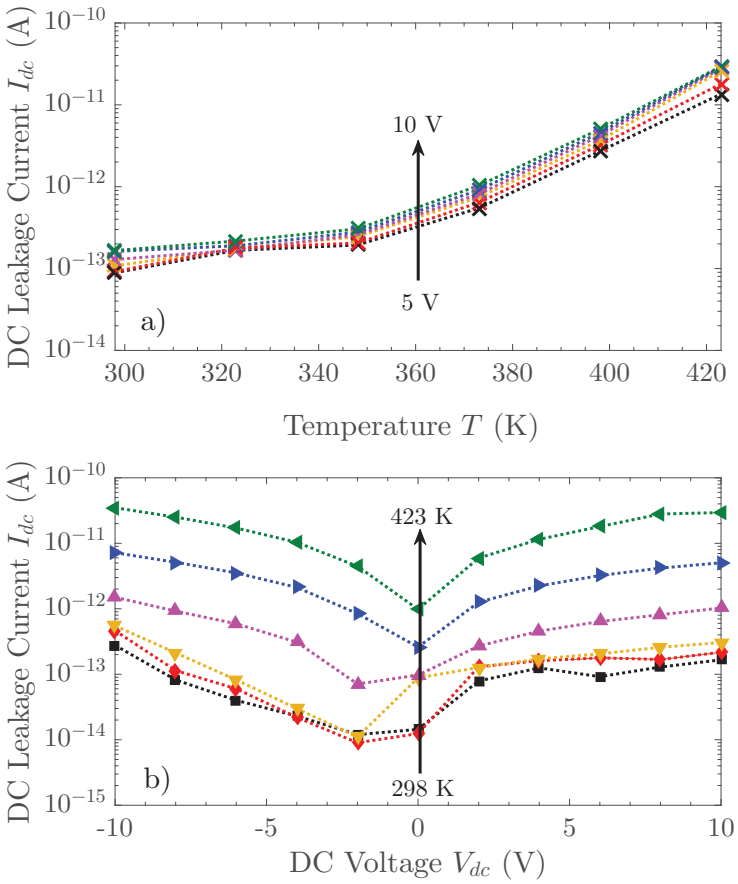

Figure 7.2. (a) Measured d.c. leakage current I_{dc} in the MIM structure containing the 275-µm-thick columnar µFTF as a function of temperature at fixed bias voltage V_{dc}: 5, 6, 7, 8, 9, and 10 V. (b) Measured values of I_{dc} in the MIM structure containing the 224-µm-thick columnar µFTF in relation to V_{dc} at fixed temperatures: 298, 323, 348, 373, 398, and 423 K.

Finally, visual examination of the samples did not evince any optical change either, so I conjecture that the microstructure is stable even for 423 K. Thus, no additional leakage mechanism is expected.

The fits of the measured data against Eq. (7.1) in Fig. 7.3 yield $\kappa_\infty = 1.16$, 2.40, and 2.37 at 348 K, 373 K, and 398 K, respectively. These values at $T = 373$ K and

398 K compare favorably with the measured relative permittivity at 1000 kHz and 298 K depicted in Fig. 6.7. Furthermore, the data in Fig. 6.7 suggest that κ may decline asymptotically to a temperature-dependent value κ_∞ with further increase of frequency.

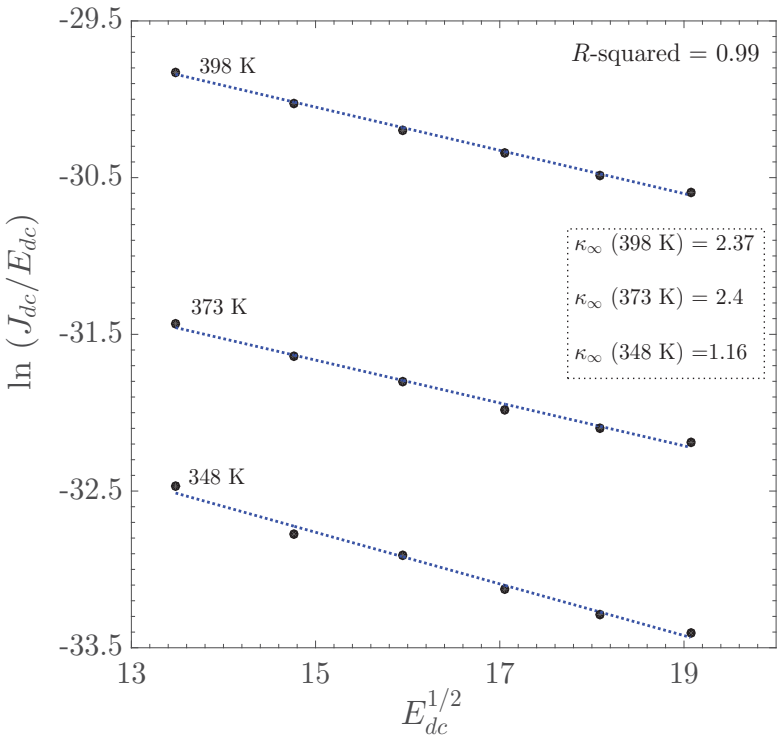

Figure 7.3. Measured values of $\ln(J_{\rm dc}/E_{\rm dc})$ plotted against $E_{\rm dc}^{1/2}$ for the MIM structure containing the 275-μm-thick Parylene-C μFTF at 348 K, 373 K, and 398 K. The units of $J_{\rm dc}$ and $E_{\rm dc}$ are A cm^{-2} and V cm^{-1}, respectively. Equation (7.1) fits the measured data with R-squared = 0.99, yielding $\Phi_{\rm B}^{\rm PF} = 0.77 \pm 0.04$ eV and the values of the κ_∞ shown at the three selected temperatures.

Since every μFTF of Parylene C is semicrystalline [128] and porous, the occurrence of defects within the sandwiched μFTF in the MIM structure is expected. As captured by the Poole–Frenkel emission theory, defects are often accompanied by localized states in the bandgap which allow for electrons to move across the film through filling and emptying these states [138]. Therefore, the conduction mechanism due to the

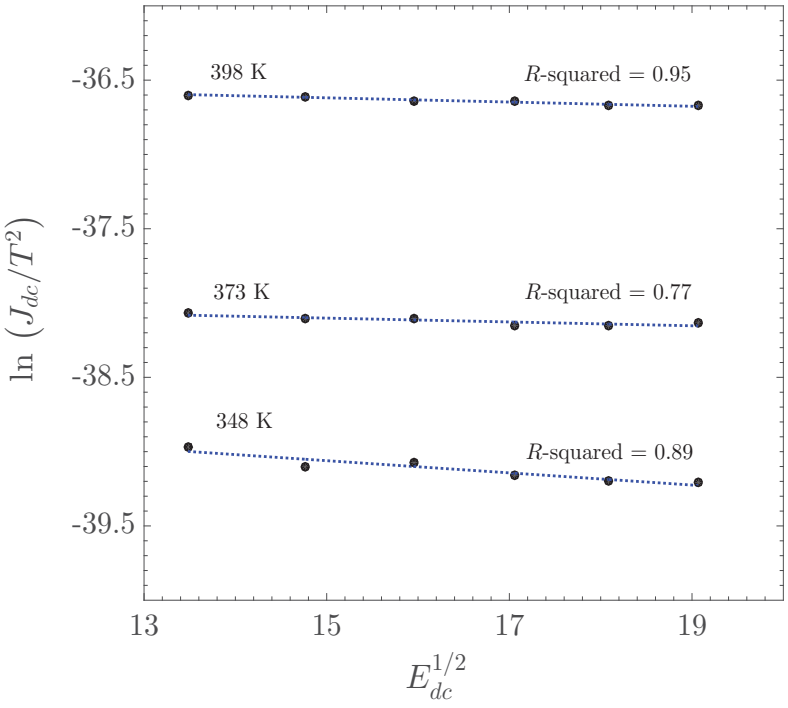

Figure 7.4. Measured values of $\ln(J_{\rm dc}/T^2)$ plotted against $E_{\rm dc}^{1/2}$ for the MIM structure containing the 275-μm-thick Parylene-C μFTF at 348 K, 373 K, and 398 K. The units of $J_{\rm dc}$ and $E_{\rm dc}$ are A cm^{-2} and V cm^{-1}, respectively. Equation (7.2) fits the measured data with R-squared = 0.89, 0.77, and 0.96 at 348 K, 373 K, and 398 K, respectively

presence of defects in a columnar μFTF is governed by the Poole–Frenkel emission.

7.3.2 A.C. leakage current

In order to understand the mechanism(s) responsible for a.c. leakage current $I_{\rm ac}$, variations of a.c. conductivity $\sigma_{\rm ac}$ with temperature and frequency needs to be analyzed. $\sigma_{\rm ac}$ was determined by measuring the resistance $R_{\rm p}$ and the reactance $X_{\rm C}$ in the equivalent circuit of the insulator layer shown in Fig. 7.1(b). These measurements were made at 1 kHz, 10 kHz, 100 kHz, and 1 MHz frequencies and at discrete temperatures between 298 K and 423 K. First, the equivalent impedance $Z(\omega) =$

$\left[R_{\rm p}^{-1} + (-jX_{\rm C})^{-1}\right]^{-1} = R_{\rm p}\,(1 + j\omega R_{\rm p}C)^{-1}$ was calculated. Next, $I_{\rm ac}$ was calculated using Ohm's law $V_{\rm ac} = I_{\rm ac}Z$. Finally, the a.c. conductivity $\sigma_{\rm ac} = (I_{\rm ac}/A)/(V_{\rm ac}/d) = (I_{\rm ac}/V_{\rm ac})(d/A)$ was extracted.

The frequency dependence of $\sigma_{\rm ac}$ computed for the 224-μm -thick Parylene-C μFTF over the selected temperature range is illustrated in Fig. 7.5(a). At every frequency, $\sigma_{\rm ac}$ of Parylene-C μFTF increases with temperature, but the temperature dependence of $\sigma_{\rm ac}$ is weak. In Fig. 7.5(b), σ_{ac} increases with frequency at all temperatures. These characteristics of $\sigma_{\rm ac}$ are observed and are similar to those of bulk polymers such as polyethylene terephthalate (PET) [141], aromatic polyimide (Kapton) [142], and Parylene C [137].

Hopping conduction is widely believed to be the most effective mechanism for explaining a.c. conduction in insulating polymers [143] and has been previously applied in studies of a.c. leakage current in bulk Parylene C [137, 140, 144]. As free charges exist in a polymeric insulator, the frequency-dependent conductivity [137]

$$\sigma(f) = \sigma_o + 2\pi f\varepsilon_o \mathrm{Im}\left[\varepsilon_{HN}(f)\right] + B(2\pi f)^s, \tag{7.3}$$

where σ_o is the low-frequency conductivity, $\varepsilon_{HN}(f)$ is the relative-permittivity contribution of the relaxation of dipoles as explained by the Havriliak–Negami model [137], and $B(2\pi f)^s$ is the high-frequency conductivity with B and s as temperature-dependent parameters. Generally, $2\pi f\varepsilon_o \mathrm{Im}\left[\varepsilon_{HN}(f)\right]$ is ignored when determining the a.c. conductivity of polymer insulators as its contribution is too small compared to the other two terms in Eq. (7.3).

In this study, relatively high frequencies ranging from 1 kHz to 1000 kHz were used. Therefore, the frequency- and temperature-dependences of a.c. conductivity can be expressed by $B(2\pi f)^s$. Thus, $\sigma_{\rm ac}$ can be represented using the Jonscher relationship [143] as $\sigma_{\rm ac} \simeq B(2\pi f)^s$. Among various mechanisms for hopping conduction, the

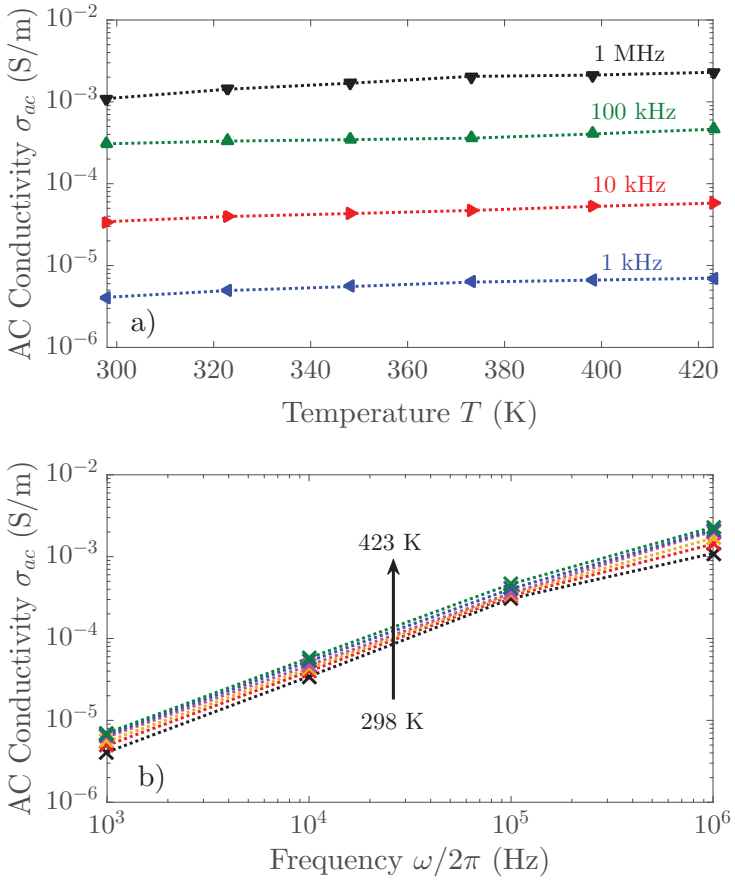

Figure 7.5. (a) AC conductivity σ_{ac} of the 224-µm-thick Parylene-C µFTF as a function of temperature at fixed frequencies: 1, 10, 100, and 1 MHz. (b) σ_{ac} as a function of frequency at fixed temperatures: 298, 323, 348, 373, 398, and 423 K.

small-polaron-tunneling mechanism (SPTM) is suggested to be a dominant mechanism in polymers [145]. SPTM predicts that

$$s = 1 - 4\left[\ln\left(\frac{1}{(2\pi f)\tau_0}\right) - \frac{W_H}{k_B T}\right]^{-1}, \tag{7.4}$$

where W_H is the polaron hopping energy and $\tau_0 \sim 10^{-13}$ s is a characteristic relaxation time on the order the vibration period of an atom [137, 146]. SPTM is reported to

dominate a.c. electron transport in bulk Parylene C as well [137].

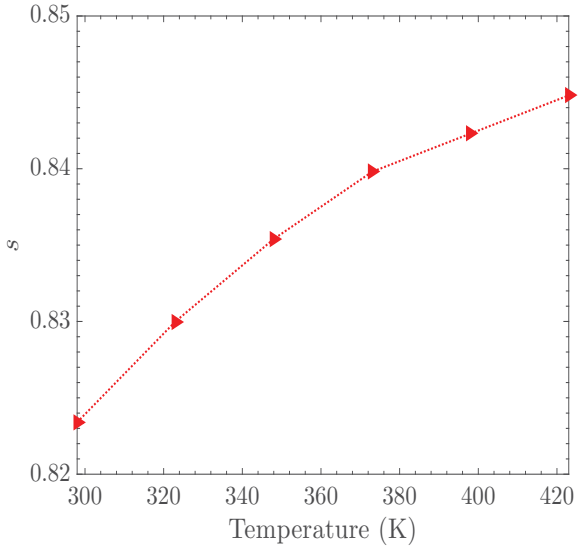

Figure 7.6. Temperature dependence of the exponent s for the 224-μm-thick Parylene-C μFTF.

After using the values of σ_{ac} presented in Fig. 7.5(b), s was determined at different temperatures by a linear-regression fit. As shown in Fig. 7.6, s increases monotonically with T. For bulk Parylene-C thin films [137], s lies between ∼0.95 and 1.00 for T between 200 and 500 K. However, within the same range of temperature, s was found to vary between 0.82 to 0.85 for columnar μFTFs. As Parylene-C columnar μFTFs are less crystalline (55-67%) than the bulk Parylene C (83.3%) [128], the disparity between the s values of bulk and μFTF forms of Parylene C can be attributed to the differences in crystallinity. Small polarons can be formed in the interfacial regions between amorphous and crystal phases or within amorphous phases [147]. Also, it can be noticed from Eq. (7.4) that the small polarons need less hopping energy W_H to overcome the potential barrier when the value of s becomes smaller. Therefore, the SPTM in Parylene-C columnar μFTFs is enhanced than in the bulk Parylene C because the latter material is less amorphous and more crystalline than the former

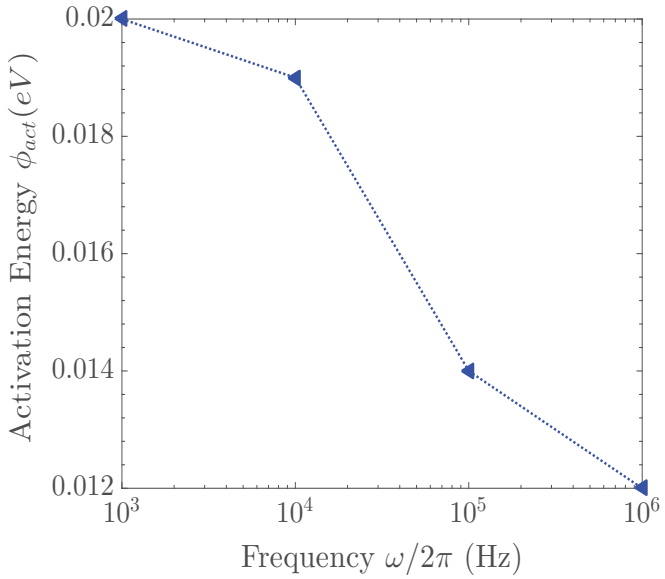

Figure 7.7. Frequency dependence of activation energy Φ_{act} for the 224-µm-thick Parylene-C µFTF.

materials.

Carrier hopping between adjacent states is enabled by a frequency-dependent activation energy $\Phi_{\text{act}}(f)$ needed to overcome the potential barrier; thus, [148–150]

$$\sigma_{\text{ac}}(f) \propto \exp\left[\frac{\Phi_{\text{act}}(f)}{k_B T}\right]. \tag{7.5}$$

Extracting $\Phi_{\text{act}}(f)$ from the values of $\sigma_{\text{ac}}(f)$ provided in Fig. 7.5(a), $\Phi_{\text{act}}(f)$ was found to decrease with frequency, as shown in Fig. 7.7. This dependence of Φ_{act} on frequency is in agreement for materials such as CdS and ZnS [150] as well as bulk Parylene C [137] in the chosen ranges of temperature and frequency. The decrease of $\Phi_{act}(f)$ with frequency is also consistent with SPTM [137, 145, 150].

7.4 Concluding remarks

The MIM structures were electrically characterized for in the [280, 420]-K temperature range and at four frequencies in the [1, 1000]-kHz range. The leakage current was studied across the Parylene-C columnar μFTFs when d.c. and a.c. voltages were applied to the MIM structures. The d.c. charge transport was determined to be attributable to the PF emission mechanism, the relevant barrier energy is 0.77 ± 0.04 eV and the high-frequency relative permittivity $\kappa_\infty \sim 2.4$ for the Parylene-C columnar μFTFs. The value of κ_∞ is in accord with the value of κ determined at 1000 kHz from capacitance measurements in Sec. 6.6. The a.c. conductivity of the Parylene-C columnar μFTFs was found to vary proportionally to $(2\pi f)^s$, with the temperature-dependent s lying between 0.82 and 0.85. The a.c. conduction in the Parylene-C columnar μFTFs can be attributed to the small-polaron-tunneling mechanism.

Chapter 8
Electrical Stability of Parylene-C Columnar Microfibrous Thin Films

8.1 Introduction

To develop reliable and stable flexible devices, it is important to understand the dominant degradation mechanisms in these devices. In general, degradation in electronic devices depends on the operation ambient as well as on the applied electrical and mechanical stresses. In addition to these factors, the reliability and stability of flexible electronic devices hinge upon the selection of appropriate materials for the substrate, active, and insulating layers.

Semi-crystalline polymers, such as Parylene C, usually contain significant concentrations of bulk and interface defects, especially after the application of electrical stress [151–153]. These defects cause instability which results in degraded film properties. Therefore, a systematic study [1] of the degradation caused by electrical stress in Parylene-C columnar μFTFs is of paramount importance before determining their suitability for applications in flexible electronics.

MIM structures incorporating Parylene-C columnar μFTFs were fabricated and

[1]This chapter is substantially based on the following paper: Ibrahim H. Khawaji, Osama O. Awadelkarim, and Akhlesh Lakhtakia, "Effects of constant-voltage stress on the stability of Parylene-C columnar microfibrous thin films," *IEEE Transactions on Dielectrics and Electrical Insulators*, vol. 26, no. 1, pp. 270–275 (2019).

electrically characterized to examine reliability and electrical-stress resistance of Parylene-C columnar μFTFs. Leakage current and capacitance were measured prior to and following the application of a CVS on the MIM structure. The leakage-current behavior was analyzed using the space-charge-limited conduction (SCLC) and Kohlrausch–Williams–Watts (KWW) relaxation function. Furthermore, the dependence of the capacitance on time and on frequency were examined as indicators of CVS-induced degradation and stability.

8.2 Experimental procedure

To measure leakage current, a Semiconductor Parameter Analyzer (HP 4155C, Hewlett-Packard, Palo Alto, CA, USA) was used. The leakage-current resolution of this instrument is 10 fA and the bias-voltage resolution is 0.2 μV. The bias voltage V_{dc} was swept from -1 V to 1 V to measure time-independent leakage current I_{dc} at room temperature.

For CVS time-dependence measurements, the transient leakage current $I_{\mathrm{m}}(t)$ was measured as a function of duration t while a constant voltage V_{stress} was being applied to it at room temperature. The chosen values of V_{stress} are 10, 30, 50, and 100 V, whereas $t \in [1, 600]$ s. A fresh MIM structure was used for every value of V_{stress}.

Capacitance measurements were carried out using a Precision LCR Meter (HP 4284, Hewlett-Packard, Palo Alto, CA, USA), while the parallel mode of 'C-D' option was selected. The resolution of the instrument is 0.01 fF. These measurements were made at frequency $f \in \{1, 10, 100, 1000\}$ kHz at room temperature with $V_{\mathrm{dc}} = 1$ V and $V_{\mathrm{ac}} = 24$ mV. The stress voltage $V_{\mathrm{stress}} = 100$ V was applied for $t \in \{0, 1800, 3000, 7200, 9000\}$ s. A fresh MIM structure was used for every period of time.

8.3 Current-voltage characterization before and after CVS

Figure 8.1 shows the d.c. leakage current I_{dc} measured at room temperature as a function of the bias voltage V_{dc} ranging from -1 V to 1 V. Reversal of V_{dc} reverses I_{dc}. The magnitude $|I_{\mathrm{dc}}|$ increases nonlinearly from 0 to 5 pA as $|V_{\mathrm{dc}}|$ increases from 0 to 1V.

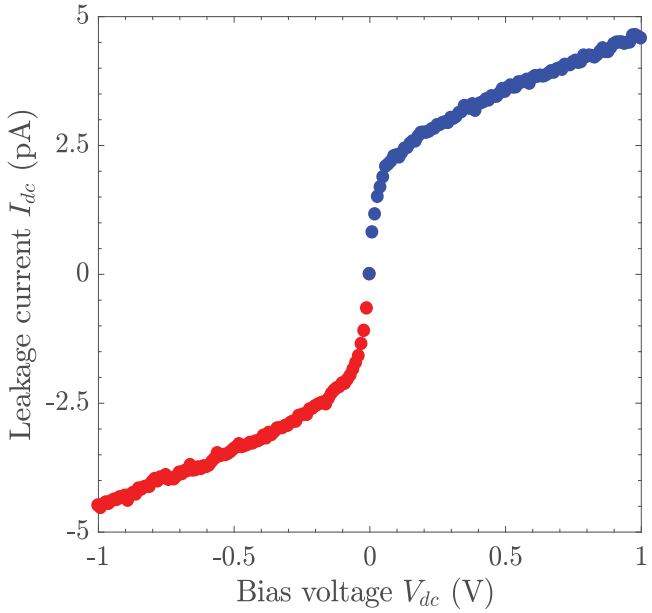

Figure 8.1. I_{dc} measured at room temperature in relation to V_{dc} before CVS application (fresh sample).

Several different conduction mechanisms have been identified in polymeric dielectric materials [80–84]. Thermionic emission including the Schottky and Poole–Frenkel mechanisms, direct and Fowler-Nordheim tunneling, and space-charge-limited current have been considered for d.c. electron transport within MIM and MIS structures. As discussed in Chapter 7, measurements of the temperature dependence of conduction in MIM structures using a Parylene-C columnar μFTF as the insulating layer have shown that conduction is dominated by Poole–Frenkel mechanism at temperatures

exceeding 350 K but not at lower temperatures. In many studies on MIM and MIS structures [81, 82, 154, 155], the power law

$$J_{dc} \propto V_{\mathrm{dc}}^{m}, \tag{8.1}$$

has been deduced for the dependence of the leakage current density J_{dc} on V_{dc}, where the exponent m is positive. At very low bias voltage, the conduction is ohmic with $m = 1$. At higher bias voltages, values of $m > 1$ suggest that conduction is space-charge limited [81, 82, 154, 155]. In the absence of electron trapping and detrapping at defects, $m = 2$ should emerge consistently with Mott–Gurney law [154]

$$J_{dc} = \frac{9}{8}\mu\varepsilon_o\kappa\frac{V_{\mathrm{dc}}^2}{d^3}, \tag{8.2}$$

where μ is the electron mobility. However, when defect concentrations in the insulator are large and electrons are trapped at defects, the space charge arising from ionized defects becomes important and m then exceeds 2 [155].

Figure 8.2 shows log-log plots of J_{dc} against V_{dc}^2 at room temperature obtained following the application of different levels of CVS. The MIM structures were stressed for $t = 600$ s with $V_{\mathrm{stress}} \in \{10, 30, 50, 100\}$ V. After the application of the CVS, the leakage current was measured as a function of V_{dc} in the range 0 to 1 V in steps of 0.25 V. Clearly in Fig. 8.2, the leakage current increases with increasing CVS. Furthermore, J_{dc} varies linearly with V_{dc}^2/d^3, irrespective of V_{stress}. This observation suggests that electrical conduction in the MIM structures at room temperature is space-charge limited, and that it is significantly influenced by ionized defects in the Parylene-C columnar μFTFs [155, 156].

Parylene-C columnar μFTFs are semi-crystalline and porous [128]. Interface and bulk defects that are accompanied by localized states in the bandgap must occur in

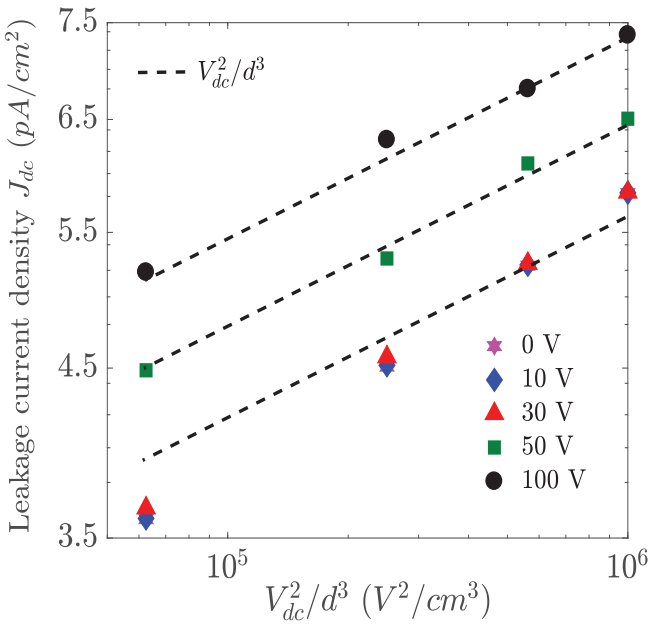

Figure 8.2. J_{dc} measured at room temperature in relation to V_{dc}^2/d^3 after CVS application for $t = 600$ s of $V_{\mathrm{stress}} \in \{10, 30, 50, 100\}$ V.

this material. Such a disordered structure will have large concentrations of electronic defect states. When the injection level of charge carriers at an electrode is high, these defect states will be filled and, hence, modulate the space charge inside the insulating layer [154]. Since $J_{dc} \propto V_{\mathrm{dc}}^2$ holds regardless of the value of V_{stress}, the same defects are contributing to the space-charge-limiting process. These defects are presumably introduced during the deposition of the Parylene-C columnar μFTF, no additional defects being induced by the CVS application.

8.4 Transient leakage current characterization under CVS

The transient leakage current $I_{\mathrm{m}}(t)$ was measured as a function of duration t while a CVS was being applied to four different MIM structures, the voltage stress V_{stress} being 10, 30, 50 or 100 V. Figure 8.3 shows the measured data for $1 \leq t \leq 600$ s. The leakage

current in the MIM structures increases as V_{stress} increases. The transient leakage current $I_{\text{m}}(t)$ comprises a decaying component I_{d} that dominates for $1 < t < 100$ s and a steady-state component I_{L} that dominates for $t > 100$ s, regardless of V_{stress}, if the capacitor-charging current is neglected because it is small and exists for only a short duration [157].

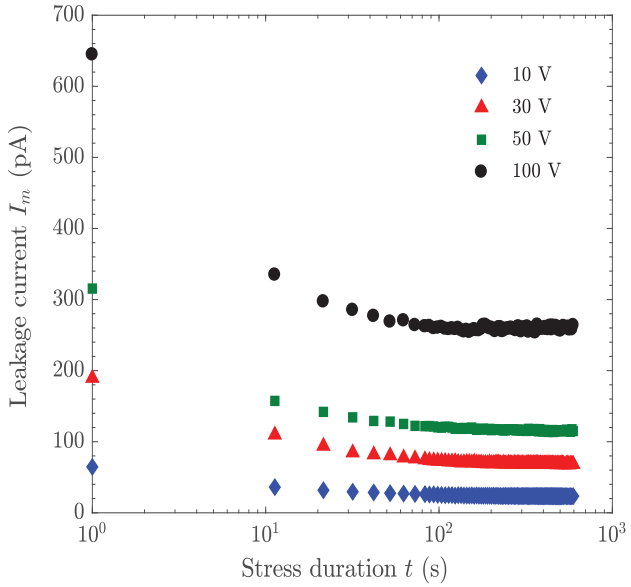

Figure 8.3. $I_{\text{m}}(t)$ measured at room temperature as a function of duration t during the application of $V_{\text{stress}} \in \{10, 30, 50, 100\}$ V

In Parylene-C columnar μFTFs, just as in other disordered materials, $I_{\text{d}}(t)$ arises from the time-dependent orientation of the dielectric polarization and the trapping/emission of charge at defects [157, 158]. The former process is presumably more effective than the latter process in determining the relaxation time, as dielectric polarization is the slower of the two processes [157, 158]. The decay current in disordered materials may be modeled by a stretched exponentially decaying function. The function most commonly used is the Kohlrausch–William–Watt (KWW) relaxation

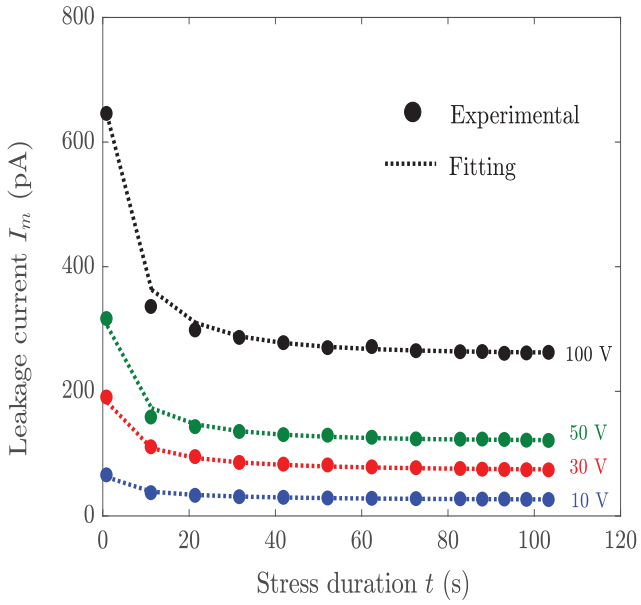

Figure 8.4. Measured and fitted values of the leakage current $I_m(t)$ in relation to the duration t of $V_{\text{stress}} \in \{10, 30, 50, 100\}$ V

function [157, 158]; accordingly [157],

$$I_{\text{d}}(t) = I_o \exp\left[-\left(\frac{t}{\tau}\right)^{\beta}\right], \quad 0 < \beta < 1, \tag{8.3}$$

where $I_o = I_{\text{d}}(0)$, τ is the relaxation time, and β is the stretch factor. Thus,

$$I_{\text{m}}(t) = I_o \exp\left[-\left(\frac{t}{\tau}\right)^{\beta}\right] + I_{\text{L}}, \quad 0 < \beta < 1. \tag{8.4}$$

The measured data in Fig. 8.3 were fitted to Eq. (8.4) for $1 \leq t \leq 100$ s, as shown in Fig. 8.4. The parameters β, τ, I_o, and I_{L} are provided in Table 8.1 for $V_{\text{stress}} \in \{10, 30, 50, 100\}$ V. Both I_o and I_{L} increase as V_{stress} increases from 10 to 100 V. Concurrently, β increases from 0.42 to 0.52 whereas τ decreases from 3.9 to

Table 8.1. Parameters β, τ, I_o, and I_{L} of $I_{\mathrm{m}}(t)$ for $V_{\mathrm{stress}} \in \{10, 30, 50, 100\}$ V.

$\mathbf{V_{stress}}$ **(V)**	**10**	**30**	**50**	**100**
β	0.42	0.46	0.50	0.52
τ (s)	3.90	3.72	3.53	3.51
I_o (pA)	65	189	315	645
I_{L} (pA)	25	37	120	260

3.51 s. But the changes in β and τ with V_{stress} are weak and it is not possible to unambiguously conclude that the observed correlations are authentic or are only within experimental and fitting errors.

The KWW parameters β, τ, and I_o are generally used to describe the observed characteristics but without indicating the physical mechanisms involved. However, it has been suggested that the stretch factor β may offer indications about the material's intrinsic features that could affect the relaxation processes [159]. Thus, $\beta \sim 0.6$ is characteristic of materials with short-range coulomb forces, whereas $\beta \sim 0.43$ characterizes amorphous materials with long-range forces during non-Debye dipolar relaxation [159]. For the Parylene-C columnar μFTFs investigated here, the obtained values of a β range from 0.42 to 0.52 and are therefore indicative of the relaxation of dielectric polarization arising from long-range forces.

When an external electric field E_{ext} is applied to the MIM structure, the defects in the Parylene-C columnar μFTF close to the Au/Parylene-C interface, which are presumably present in high density and have large capture cross-sections, become charged and reorient. The resulting time-dependent dielectric polarization P leads to a reduction in the local electric field [160]

$$E_{\mathrm{local}} = E + \frac{1}{3\varepsilon_o} P, \tag{8.5}$$

where E is the actual electric field in the Parylene-C columnar μFTF. That reduction is observed as a current decay with time evident in Fig. 8.3 [161, 162].

In disordered materials (such as Parylene-C columnar μFTFs), E saturates and never reaches the value of the externally applied electric field $E_{\rm ext} = V_{\rm dc}/d$ [163]. Since Parylene-C columnar μFTFs are semi-crystalline and should be regarded as composite materials [6], the macroscopic polarization has contributions from (i) dipoles in the amorphous phase, (ii) dipoles in the crystalline phase, and (iii) interfacial polarization [163].

8.5 Capacitance-frequency characterization After CVS

Let $C_o(f)$ denote the capacitance of a MIM structure before the application of a CVS and $C_{\rm s}(f,t)$ the capacitance of the same MIM structure after the application of a CVS for duration t, when the frequency is f; thus, $C_0(f) = C_{\rm s}(f,0)$. Figure 8.5 shows $C_{\rm s}(f,t)$ measured for $f \in \{1, 10, 100, 1000\}$ kHz with $V_{\rm stress} = 100$ V applied for $t \in \{0, 1800, 3000, \ \ 7200, 9000\}$ s at room temperature. The fact that capacitance decreases with the duration t suggests that κ also decreases with t. It is been shown in Chapter 6 that κ of Parylene-C columnar μFTFs decreases as the frequency increases, and that the spectral variation of κ at low frequencies is dominated by molecular-dipole polarization.

The relative difference $\delta C(f,t) = 1 - C_{\rm s}(f,t)/C_0(f)$ increases from 0.3% at $t = 1800$ s to 1.94% at $t = 9000$ s when $f = 1$ kHz; likewise, $\delta C(f,t)$ increases from 0.83% at $t = 1800$ s to 3.36% at $t = 9000$ s when $f = 1000$ kHz. Thus, the change in capacitance at a fixed frequency depends on the duration of the CVS application, as has previously been reported for other disordered materials as well [164].

The variations in $C_{\rm s}$ with d for the columnar μFTFs are within 0.3-pF range. To ensure that these variations are significant, the capacitance of an 10-pF HP 16382A

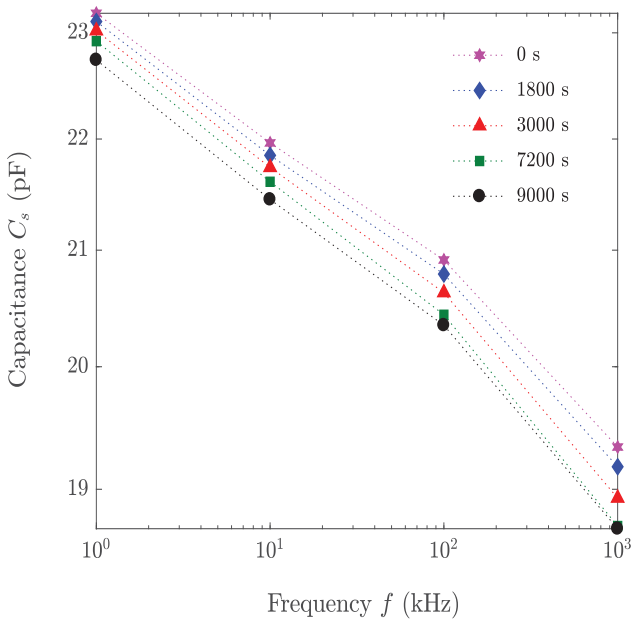

Figure 8.5. Cs (f, t) measured for $f \in \{1, 10, 100, 1000\}$ kHz with $V_{\text{stress}} = 100$ V applied for $t \in \{0, 1800, 3000, \ \ 7200, 9000\}$ s at room temperature.

standard structure was measured and the error was found to be less than 0.2% in the 1 kHz to 1000 kHz frequency range. Since the measured capacitances of the MIM structures are on the order of 1 pF, the capacitance of a standard surface-mounted AVX Multilayer Ceramic MLCC-SMD/SMT structure (1 ± 0.02 pF) was measured and found to be 1 ± 0.08 pF and 1 ± 0.024 pF at 1 kHz and 1000 kHz, respectively. As the resolution of the LCR meter was on the order of 10^{-6} pF, the capacitance variations reported in Fig. 8.6 and Table 8.2 are reliable.

Afterv using the data presented in Table 8.2, it is found that $\Delta C(f,t) = C_0(f) - C_{\text{s}}(f,t)$ varies linearly with the duration t of CVS application. As shown in Fig. 8.6, for example, when $V_{\text{stress}} = 100$ and $f = 1000$ kHz, $\Delta C(f,t) = 0.3\ln(t) - 2.04$, where ΔC is measured in pF and t in s. An extrapolation with $t = 10$ years $= 3.16 \times 108$ s, $\Delta C(f,t) = 3.77$ pF. This value indicates that the MIM structure containing the 100-µm-thick Parylene-C columnar µFTF will undergo approximately 20% degradation

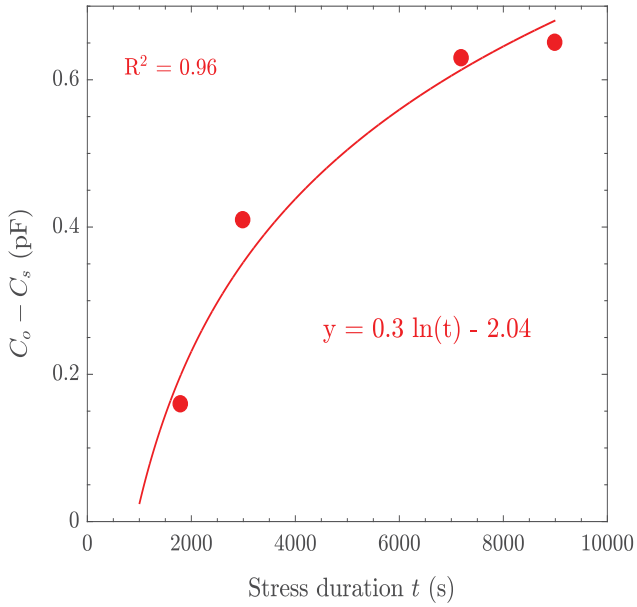

Figure 8.6. The values of $\Delta C(f,t) = C_0(f) - C_s(f,t)$ for different stress-times under operating conditions 100-V and 1000-kHz.

in 10 years when compared with $C_o(f) = 19.34$ pF for $f = 1000$ kHz.

Table 8.2. Values of C_0, C_s, and δC for $f \in \{1, 10, 100, 1000\}$ kHz with $V_{stress} = 100$ V applied for $t \in \{0, 1800, 3000, 7200, 9000\}$ s at room temperature.

f (kHz)	C_0 (pF)	C_s (pF)				δC (%)			
	0 s	1800 s	3000 s	7200 s	9000 s	1800 s	3000 s	7200 s	9000 s
1	23.2	23.1	23.0	22.9	22.7	0.30	0.70	1.20	1.90
10	22.0	21.9	21.7	21.6	21.5	0.50	1.00	1.60	2.30
100	20.9	20.8	20.6	20.4	20.3	0.60	1.40	2.30	2.70
1000	19.4	19.2	18.9	18.7	18.6	0.80	2.10	3.30	3.40

8.6 Concluding remarks

In this chapter, the effects of constant-voltage stress on the stability of Parylene-C columnar μFTFs for applications in flexible electronics are reported. 100-μm-thick

columnar μFTFs were fabricated as the insulating layers of MIM structures. A stress voltage $V_{\text{stress}} \in [10, 100]$ V was applied to each MIM structure at room temperature for a duration as large as 10^4 s. Before and after the CVS application, I-V and C-f measurements were made at frequencies ranging 1 kHz and 1000 kHz.

The leakage current density J_{dc} was found to depend on the bias voltage V_{dc} as $J_{dc} \propto V_{\text{dc}}^m$, where the exponent $m \sim 2.0$, both before and after the application of the CVS and without any dependence on V_{stress}. The linear variation of J_{dc} with V_{dc}^2/d^3 suggests that the electric conduction in any Parylene-C columnar μFTF is space-charge limited. The space charge is suggested to arise from carrier trapping at defects as electrons are injected into the μFTF.

Initial current transients observed over the first 100 s are attributed to the polarization orientation with relaxation time τ. The transient current was fitted to the Kohlrausch–William–Watt relaxation function with $3.5 \leq \tau \leq 3.9$ s. The CVS impact on the Parylene-C columnar μFTFs was also assessed using capacitance measurements. Capacitance values before and after CVS application were found to effectively track charge buildup and predicted that MIM structure containing 100-μm-thick Parylene-C columnar μFTFs would undergo approximately 20 % degradation in 10 years.

Chapter 9
Charge Buildup and Leakage Current in Bulk Parylene-C Thin Films

9.1 Introduction

Parylene-C films have been extensively studied [4, 6–9, 57–61] as gate dielectrics in OFETs. However, very little is known about the electrical stability and reliability of Parylene C and its interfaces with the active layers in these devices. Current-voltage measurements are commonly made to study the electrical degradation of OFETs under constant-voltage stress (CVS) [9]. However, capacitance-voltage measurements are more sensitive than current-voltage measurements for investigating interface characteristics [165]. In order to address this shortfall, the electrical stability and reliability of Parylene C as a gate dielectric were investigated using capacitance-voltage measurements.

A systematic analysis of gold/Parylene-C/Pentacene metal–insulator–semiconductor (MIS) structures was performed. The effects of CVS, the capacitance-voltage curve-shift, and time-dependent dielectric-breakdown (TDDB) were experimentally analyzed. Needless to add, the gold/Parylene-C/Pentacene system is the heart of the OFET.

9.2 Experimental procedure

Capacitance-voltage (C-V) measurements were carried out using a Precision LCR Meter (HP 4284, Hewlett-Packard, Palo Alto, CA, USA), while the parallel mode of 'C-D' option was selected. These measurements were made at 1,10,100, and 1000 kHz frequency and room temperature with an applied gate voltage $V_g \in [-2, 2]$ V and an oscillating voltage signal $V_{\text{ac}} = 24$ mV. Using a Semiconductor Parameter Analyzer (HP 4155C, Hewlett-Packard, Palo Alto, CA, USA), the time-dependent leakage current I_{stress} as a function of time t was measured while a stress voltage $V_{\text{stress}} \in \{\pm 10, \pm 15, \pm 20\}$ V was being applied at room temperature. A fresh Au/Parylene-C/Pentacene/Au/Cr/SiO2/p-Si structure was used for every value of V_{stress}.

9.3 Dielectric properties of bulk Parylene-C

C-V measurements at room temperature and at frequencies ranging from 1 to 1000 kHz were used to determine κ of bulk Parylene-C. MIM structures contain three bulk films of thicknesses 1, 2, and 3 μm , as measured by a profilometer (P-16+, KLA Tencor, Milpitas, CA, USA), were fabricated using the amounts of Parylene-C dimer 0.5, 1, and 1.5 g, respectively. Figure. 9.1(a) shows that C decreases with increasing film thickness d for the bulk films. This inverse dependence of C on d is expected because the capacitance of a MIM struture is given by $C = \kappa\varepsilon_o A/d$. Knowing C, A, and d, we can determine κ for the data presented in Fig. 9.1(a).

The obtained results shown in Fig. 9.1(b) indicate that κ decreases as the frequency increases from 1 to 1000 kHz. This dispersion of κ at fairly low frequencies [12, p. 708, Fig. 7.15] suggests that orientational polarization associated with molecular dipoles is the dominant polarization mechanism for the bulk Parylene-C films [51]. The values of κ reported in Fig. 9.1(b) for the bulk films are about 11% higher at 1 kHz and

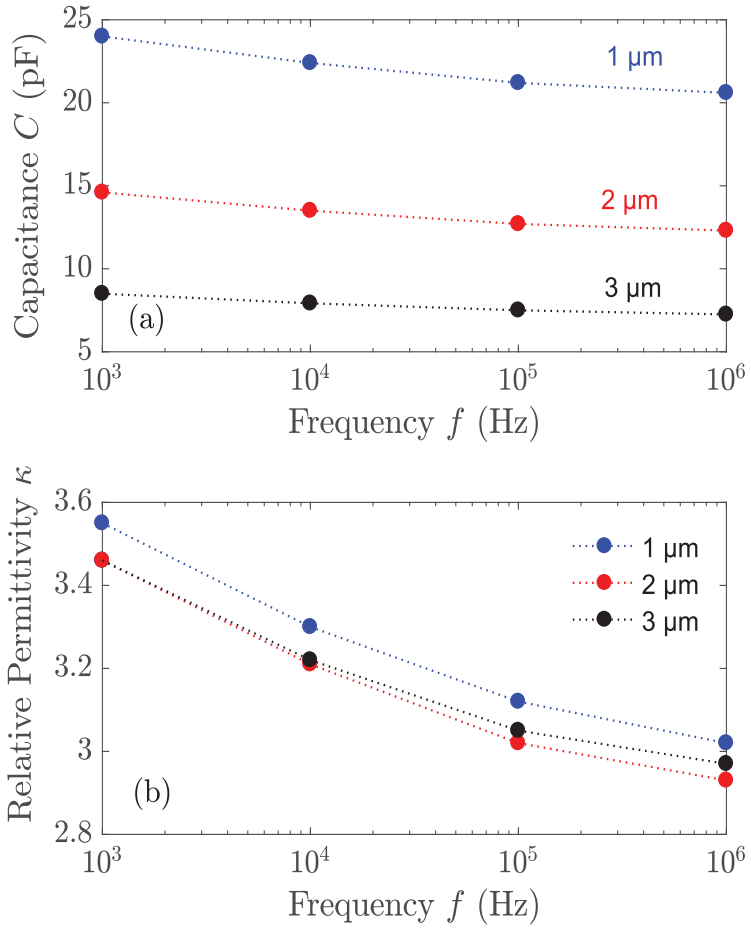

Figure 9.1. Measured C-V characteristics of MIM structures with different bulk Parylene C film thicknesses 1, 2, and 3 μm. (a) Capacitance of three MIM structures measured as a function of frequency at room temperature, and (b) Calculated relative permittivity κ determined as a function of frequency.

about 2% lower at 1000 kHz than those reported by Kumar [37]. As 93.2%-pure dimer was used, these differences in κ can be attributed to the presence of impurities. Indeed, the average κ for three bulk films in Fig. 9.1(b) reduces from 3.49 to 2.97 as the frequency increases from 1 to 1000 kHz.

9.4 Capacitance-voltage characterizations of the MIS structure before CVS

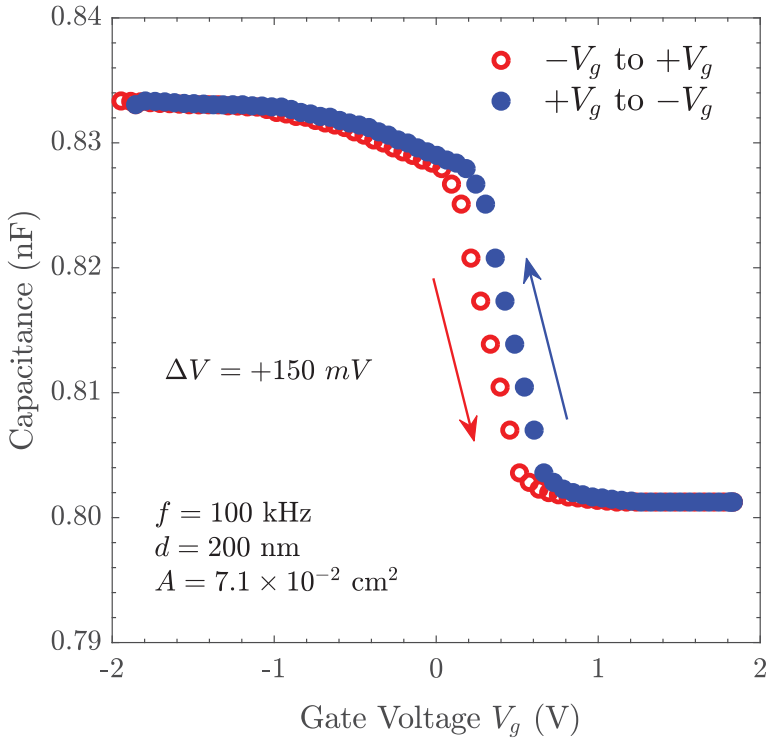

Figure 9.2. Measured C-V characteristics of a Au/Parylene-C/Pentacene structure, functioning as a control sample (i.e., $V_{\text{stress}} = 0$) at 100 kHz and room temperature. The Parylene-C layer is of thickness $d = 200$ nm and the top-electrode area $A = 7.1 \times 10^{-2}$ cm^2.

The measured C-V characteristics of an Au/Parylene-C/Pentacene structure at 100 kHz are shown in Fig. 9.2. As this sample was not subjected to CVS, it served as the control sample. Its C-V characteristics were measured in small voltage sweeps from ± 2 V to ∓ 2 V. The capacitance shows an apparent transition from accumulation to depletion. A small hysteresis is evident, the C-V curve-shift ΔV of 150 mV being very small [166, 167].

An MIS structure is generally modeled as two structures in series: the insulator capacitance $C_{\rm i}$ and the semiconductor-depletion-layer capacitance $C_{\rm sim}$ [165, 166, 168]; hence, the capacitance of the MIS structure is

$$C_{\rm m} = \frac{C_{\rm i} C_{\rm sim}}{C_{\rm i} + C_{\rm sim}} \,. \tag{9.1}$$

For $V_g > 0$, the measured capacitance reaches a constant value equivalent to $C_{\rm m}$ given by Eq. (9.1). In contrast, for $V_g < 0$, the capacitance saturates to a value close to

$$C_{\rm i} = \epsilon_o \kappa \frac{A}{d}. \tag{9.2}$$

The bulk Parylene-C layer is of thickness $d = 200$ nm and the top-electrode area $A = 7.1 \times 10^{-2}$ cm^2.

9.5 Characterization of MIS structures under CVS

9.5.1 Capacitance-voltage characterizations after CVS

Figure 9.3 shows the C-V curves measured at 100 kHz in the Au/Parylene-C/Pentacene MIS structures after the room-temperature application of (a) $V_{\rm stress} \in \{-10, -15, -20\}$ V and (b) $V_{\rm stress} \in \{10, 15, 20\}$ V for duration $t = 10$ s. After the 10-s application of $V_{\rm stress} \gtrless 0$, a C-V curve-shift $\Delta V \gtrless 0$ is observed for all three values of $|V_{\rm stress}|$, which suggests a positive (resp. negative) charge buildup in the insulator of the MIS structure during the application of positive (resp. negative) CVS. For the same $|V_{\rm stress}|$ and t, $|\Delta V|$ is higher for $V_{\rm stress} > 0$ than for $V_{\rm stress} < 0$.

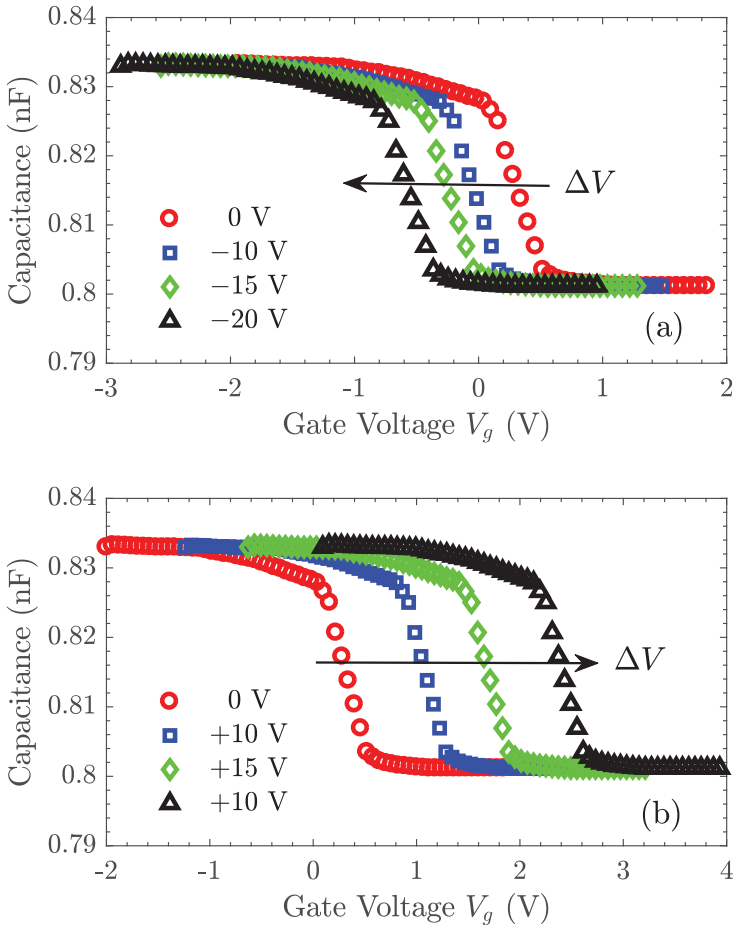

Figure 9.3. Measured C-V characteristics of a Au/Parylene-C/Pentacene structures at 100 kHz and room temperature, after the application of (a) $V_{\text{stress}} \in \{-10, -15, -20\}$ V and (b) $V_{\text{stress}} \in \{10, 15, 20\}$ V for $t = 10$ s.

9.5.2 Time-dependent leakage current under CVS

The time-dependent leakage current I_{stress} was measured as a function of $t \in [1, 11]$ s during the application of CVS on MIS structures for $V_{\text{stress}} \in \{\pm 10, \pm 15, \pm 20\}$ V. The data presented in Fig. 9.4 show that I_{stress} is larger for larger $|V_{\text{stress}}|$. For the same $|V_{\text{stress}}|$, I_{stress} is lower by three orders of magnitude for $V_{\text{stress}} > 0$ than for $V_{\text{stress}} < 0$.

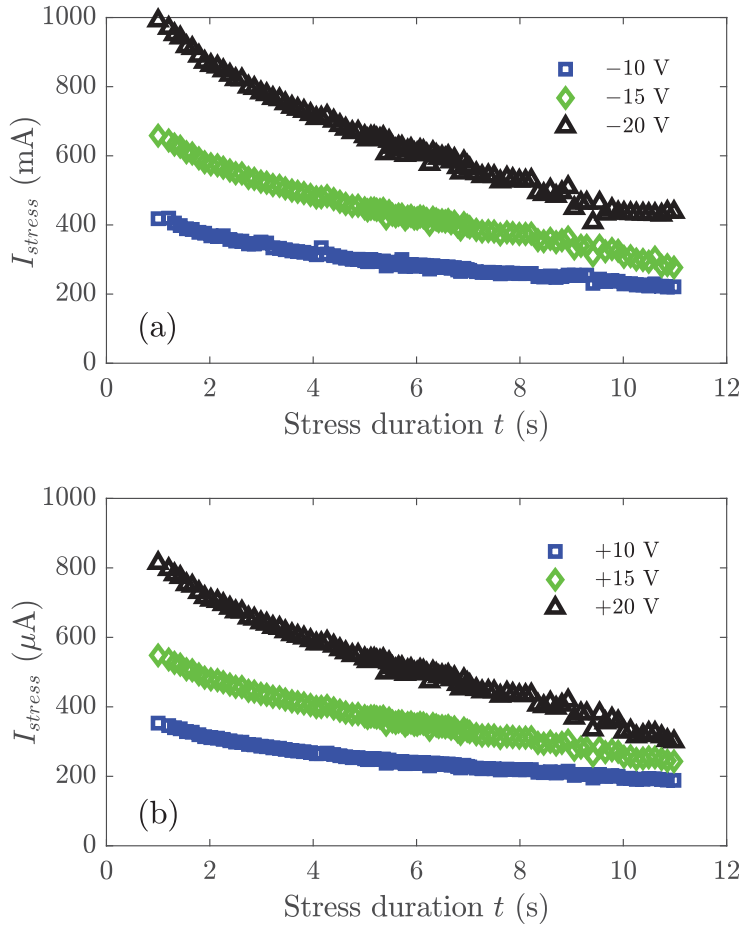

Figure 9.4. Measured time-dependent leakage current I_{stress} in a Au/Parylene-C/Pentacene structures at room temperature as a function of duration $t \in [1, 11]$ s during CVS application. (a) $V_{\text{stress}} \in \{-10, -15, -20\}$ V and (b) $V_{\text{stress}} \in \{10, 15, 20\}$ V.

Irrespective of the polarity of V_{stress}, I_{stress} decays as t increases.

9.5.3 TDDB characterization after CVS

The TDDB characteristics of the Au/Parylene-C/Pentacene structures were obtained by recording the current-voltage (I-V) response before and after the 10-s application

of $V_{\text{stress}} > 0$. Before CVS, the I-V curve in Fig. 9.5(a) shows a dielectric breakdown occurs at an electric field of 1.62 MV cm^{-1}. This value is comparable to the values of the breakdown electric field E_{bd} in the range 1.9 to 2.2 MV cm^{-1} reported for 200-nm-thick Parylene-C layers in MIM structures [39, 169], but for a much smaller gate electrode area of about $3{\times}10^{-4}$ cm^2.

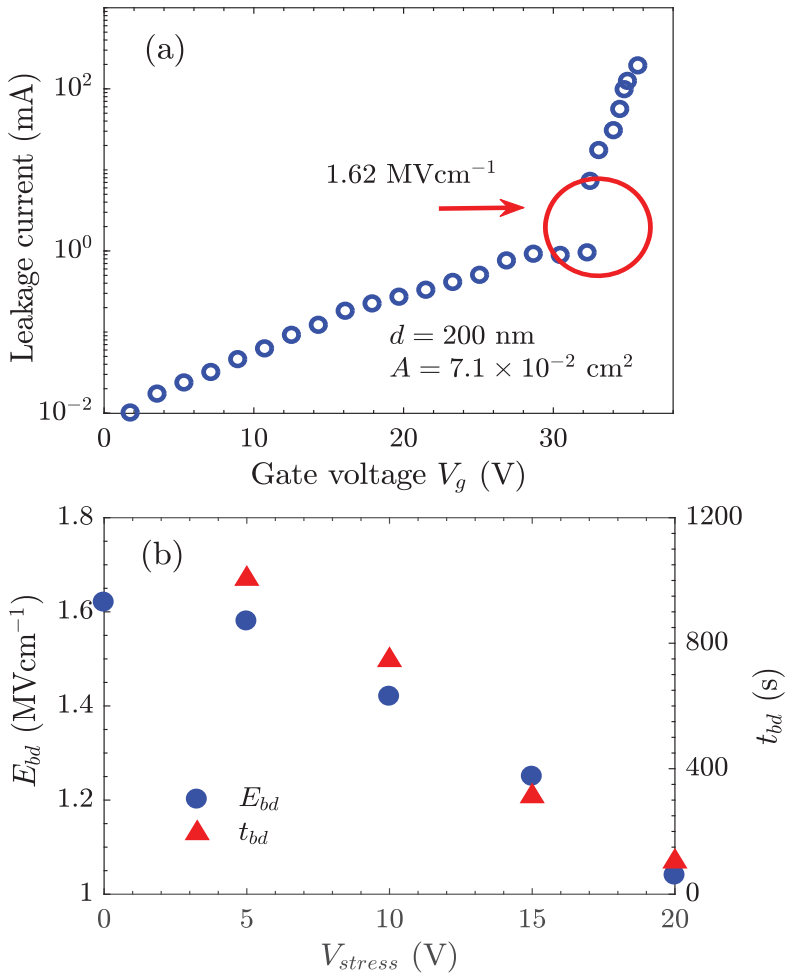

Figure 9.5. Room-temperature TDDB characteristics of Au/Parylene-C/Pentacene structures: (a) Leakage current measured as a function of gate voltage V_{g} before CVS application (control sample). (b) Breakdown electric field E_{bd} and time t_{bd} after application of $V_{\text{stress}} \in \{5, 10, 15, 20\}$ V.

In Fig. 9.5(b), measured values of the breakdown field $E_{\rm bd}$ and the time-to-breakdown $t_{\rm bd}$ are plotted as functions of $V_{\rm stress} \in \{5, 10, 15, 20\}$ V. Time-to-breakdown $t_{\rm bd}$ is the time it takes for the Parylene C to breakdown under the application of each $V_{\rm stress}$.

As expected, both $E_{\rm bd}$ and $t_{\rm bd}$ decrease as $V_{\rm stress} > 0$ increases. The value of $E_{\rm bd}$ decreases from 1.62 MV cm^{-1} for the control sample (i.e., $V_{\rm stress} = 0$) to 1.04 MV cm^{-1} for the sample stressed with $V_{\rm stress} = 20$ V. Furthermore, $t_{\rm bd}$ decreases from 1005 s for the control sample to 104 s for the sample stressed with $V_{\rm stress} = 20$ V.

9.6 Analysis of the CVS effects on the MIS structure

The C-V characteristics of organic-based MIS structures are limited by contact injection [165,170–173]. The C-V curve obtained in Fig. 9.2 can be explained in terms of charge accumulation arising from injection and contained within the semiconductor layer.

For $V_g > 0$, a thin accumulated layer of injected holes occurs at the Au/Pentacene interface, while the Parylene-C/Pentacene interface is depleted and devoid of any significant free charge carriers. As a result, a depletion layer is created inside the Pentacene. Hence, the capacitance is given by $C_{\rm m}$ in Eq. (9.1). For $V_g < 0$, an accumulation of holes occurs near the interface of Pentacene/Parylene-C. As V_g further increases to more negative values, $C_{\rm sim}$ increases and $C_{\rm m}$ approaches $C_{\rm i}$ given by Eq. (9.2).

The C-V curve shifts observed in Fig. 9.3 are attributed to charge buildup $\Delta Q_{\rm t}$ in Parylene C [174, 175]. Charges of three different provenances are associated with $\Delta Q_{\rm t}$ [174, 175]; i.e.,

$$\Delta Q_{\rm t} = Q_{\rm m} + Q_{\rm b} + Q_{\rm i}\,. \tag{9.3}$$

Here, $Q_{\rm m}$ is the charge density of mobile positive charges located in the bulk of the

insulator and arising from ionic impurities such as Na^+. The effect of these charges can be seen as a hysteresis in the C-V curve when sweeping V_g in a negative-positive-negative loop. Also, Q_b is the charge density of charges trapped in the bulk insulator. It can be either negative or positive, depending on whether holes or electrons are trapped. Q_i is the charge density of charges trapped in the semiconductor/insulator interface. It can also be either negative or positive. Because these charges are trapped at the interface, Q_i has the largest effect on ΔV.

As can be deduced from Fig. 9.2, Q_m is negligibly small because a very small hysteresis ($\Delta V = 150$ mV) is detected as the gate voltage is swept from -2 V to $+2$ V to -2 V. Hence, Q_m plays no role in the charge buildup observed in Parylene C after the application of CVS so that

$$\Delta Q_t = Q_b + Q_i \,. \tag{9.4}$$

A quantitative analysis of ΔQ_t and its dependence on V_{stress} and t is now in order. Accordingly [176],

$$\Delta Q_t = -\frac{\Delta V\, C_i}{A} \,. \tag{9.5}$$

Table 9.1 and Table 9.2 provide the values of ΔQ_t for $V_{stress} \in \{\pm 10, \pm 15, \pm 20\}$ V. Clearly, the charge buildup are positive for $V_{stress} < 0$ but negative for $V_{stress} > 0$. Furthermore, for fixed $|V_{stress}|$, the charge buildup is more than twice in magnitude for $V_{stress} > 0$ than for $V_{stress} < 0$.

During the time that $V_{stress} < 0$, electrons are injected from the gate and holes are injected from the layer of accumulated holes near the Parylene-C/Pentacene interface. Electrons and holes transiting the Parylene-C layer can be trapped at defect sites

Table 9.1. C-V curve-shift ΔV of and the charge buildup $\Delta Q_{\rm t}$ in a Au/Parylene-C/Pentacene MIS structure subjected to $V_{\rm stress} \in \{-10, -15, -20\}$ V for $t = 10$ s.

	$V_{\rm stress}$ (V)		
	-10	-15	-20
ΔV (V)	-0.35	-0.56	-0.89
$\Delta Q_{\rm t}$ (C cm^{-2})	$+4.10\times10^{-9}$	$+6.50\times10^{-9}$	$+1.04\times10^{-8}$

Table 9.2. C-V curve-shift ΔV of and the charge buildup $\Delta Q_{\rm t}$ in a Au/Parylene-C/Pentacene MIS structure subjected to $V_{\rm stress} \in \{+10, +15, +20\}$ V for $t = 10$ s.

	$V_{\rm stress}$ (V)		
	$+10$	$+15$	$+20$
ΔV (V)	$+0.76$	$+1.37$	$+2.10$
$\Delta Q_{\rm t}$ (C cm^{-2})	-8.90×10^{-9}	-1.60×10^{-8}	-2.45×10^{-8}

and give rise to charge buildup. It is apparent from Table. 9.1 that hole trapping dominates and the net charge buildup is positive for $V_{\rm stress} < 0$.

In contrast, holes are only injected from the gate into Parylene-C. The resulting hole-leakage current is observed to be much smaller than $I_{\rm stress}$ shown in Fig. 9.4(a) during the time that $V_{\rm stress} > 0$. This is because a significant portion of the applied $V_{\rm stress}$ is dropped across the depleted (i.e., devoid of charge carriers) layer near the Pentacene/Parylene-C interface; much less hole transport takes place across Pentacene for $V_{\rm stress} > 0$. However, the charge-buildup sign is negative, which may indicate that the observed charge buildup is not entirely due to the trapping of charge carriers (electrons and holes) but could also be caused by defect generation. Presumably, these generated defects are electrons traps that are populated during the application

of V_{stress}.

The I-V curve in Fig. 9.5(a) shows a dielectric breakdown occurs at an electric field of 1.62 MV cm^{-1}. This breakdown may indicate the formation of a defect-related conduction path [177, 178]. In other words, a higher applied voltage could induce defects that eventually form different conducting paths from the gate to the semiconductor in the Au/Parylene-C/Pentacene structure.

As shown in Fig. 9.5(b), the decrease in E_{bd} suggests that more/longer conductive paths are formed with increasing $V_{\text{stress}} > 0$. Conductive paths result from defect-generation processes and, hence, more defects are presumably generated as V_{stress} further increases to higher values. This deduction is in agreement with earlier inference from Table 9.2 that defect generation dominates over charge trapping during $V_{\text{stress}} > 0$.

9.7 Concluding remarks

A systematic analysis of the reliability of Au/Parylene-C/Pentacene MIS structures under constant-voltage stress was performed, with focus on the effects of CVS on the stability of Parylene C as a gate dielectric. 200-nm-thick Parylene-C thin films were utilized as gate-dielectric layers in Au/Parylene-C/Pentacene MIS structures. Measurements and analysis of the C-V curve-shift, the time-dependent leakage current, and the time-dependent dielectric breakdown were performed before and after application of CVS. Positive and negative stress voltages of the same magnitude were applied for 10-s duration.

A summary of the obtained results is as follows:

- The MIS capacitance shows an apparent transition from accumulation to depletion.

- The C-V curve-shift is higher for positive stress voltage than for negative stress voltage of the same magnitude.
- The time-dependent leakage current for positive stress voltage is three orders of magnitude lower than for negative stress voltage.
- The charge density of trapped charges increases with the stress voltage, the polarity of the trapped charges being opposite to the polarity of the stress voltage.
- As the application of CVS increases, the breakdown voltage decreases as does the time to breakdown.

Therefore, the main conclusions of this study are as follows:

- The C-V characteristic can be explained in term of accumulation charges within the semiconductor layer.
- This accumulation charge is due to contact injection.
- Inside the insulating layer, the charge buildup resulting from the accumulation of trapped charges affects the stability of the the MIS structure by shifting its C-V curve.
- The shift of the C-V curve is attributed to the trapping and recombination of electrons and holes inside Parylene C and its interface with Pentacene.
- The dielectric-breakdown mechanism is defect dominated.

Overall, the buildup of trapped charges in the Parylene-C layer and near the Parylene-C/Pentacene interface plays a major role in the degradation of Au/Parylene-C/Pentacene structures. The analysis presented in this chapter provides a first-level

understanding of the charge buildup in Au/Parylene-C/Pentacene structures and, perhaps, will serve as the basis of future studies on the defect-generation process and the trapping of charge carriers within the insulator layer in OFETs.

Chapter 10
Conclusions and Future Work

The use of Parylene C as a multifunctional insulator (i.e., substrate, gate dielectric, and passivation layer) in the same device will result in effective cost reduction and improved sustainability of flexible electronics. This goal motivated the work presented in this dissertation which focuses on engineering Parylene-C films and studying their electrical and mechanical properties for flexible electronics. Also, the possibility of lowering κ of Parylene C using a physicochemical deposition technique provided the impetus for examining its use as an ultralow-κ ILD in flexible ICs.

As discussed in Chapter 1, the objectives of the research conducted for this dissertation were executed in the following sequence:

1. Study the Parylene-C columnar μFTFs' morphology, porosity, flexibility, and dielectric properties in relation to the deposition angle in oblique-angle physiochemical deposition technique.

2. Identify charge transport and conduction mechanisms in Parylene-C columnar μFTFs.

3. Investigate stability and electrical-stress resistance of Parylene-C columnar μFTFs.

4. Understand the different physical phenomena of charge buildup and electrical

degradation in bulk Parylene-C films.

10.1 Summary and conclusions

Parylene-C columnar μFTFs were grown using an oblique-angle physicochemical vapor deposition technique. The static Young's moduli, yield strengths, and the relative permittivity were correlated to the porosity, crystallinity, and the direction of the vapor flux during deposition. Moreover, electrical characterization using capacitance-voltage-temperature and current-voltage-temperature experiments at different temperatures were performed to study the dielectric properties of and charge transport in Parylene-C columnar μFTFs. Consequently, the d.c. and a.c. conduction mechanisms were identified. Also, a systematic study of the degradation caused by CVS in Parylene-C columnar μFTFs was carried out to explore their suitability for applications in flexible electronics. Moreover, the effects of constant-voltage stress, the capacitance-voltage curve-shift, and time-dependent dielectric breakdown were experimentally analyzed in gold/bulk Parylene C/Pentacene MIS structures.

The main conclusions for this dissertation are as follows:

- Cross-sectional FESEM images and porosity measurements show that the porosity decreases from 0.56 to 0.38 as the deposition angle χ_v increases from 30° to 90°. The static Young's moduli and the yield strengths depend on the deposition angle χ_v, and they are lower than their counterparts for bulk Parylene C by about two orders of magnitude. The relative permittivity was successfully lowered to be about 70% of that of the bulk Parylene C. DC charge transport in the Parylene-C columnar μFTFs arises from the Poole-Frenkel conduction mechanism while a.c. conduction is due to the small-polaron tunneling mechanism. The leakage current after the application of a constant-voltage stress for a given duration follows the Kohlrausch-Williams-Watts

relaxation model, and the capacitance is found to degrade by about 20% in 10 years. It is concluded that Parylene-C columnar μFTFs have a potential for use as ultralow-κ ILDs in flexible electronics.

- The capacitance-voltage curve-shift is higher for positive stress voltage than for negative stress voltage of the same magnitude. However, the time-dependent leakage current for positive stress voltage is three orders of magnitude lower than for negative stress voltage. Dielectric breakdown is defect dominated, as defects form a conduction path or multiple conduction paths inside the insulator layer. Also, the charge buildup resulting from the accumulation of trapped charges affects the stability of the MIS structure by shifting its C-V curve. This shift is attributed to the trapping and recombination of electrons and holes inside Parylene C and its interface with Pentacene. Overall, the buildup of trapped charges in the bulk Parylene-C used as a gate dielectric and near the Parylene-C/Pentacene interface plays a major role in the degradation of Au/bulk Parylene-C/Pentacene structures.

The overall conclusion is that both mechanical and dielectric properties of the Parylene-C columnar μFTFs can be controlled by selecting χ_v appropriately. As a result, Parylene-C columnar μFTFs can be fabricated to deliver $\kappa = 2.02$, which is lower than $\kappa = 3.0$ of bulk Parylene C by 30%. Therefore, Parylene-C columnar μFTFs are promising candidates for deployment as ultralow-κ ILDs beside their electrical stability and reliability.

10.2 Suggestions for future work

10.2.1 Parylene-C columnar μFTFs: thickness optimization

Parylene-C columnar μFTFs have been prepared at different deposition angles using an oblique-angle physicochemical vapor deposition technique. For this dissertation, the minimum thickness achieved is about 80 μm. However, this thickness needs to be scaled down in order to use Parylene-C columnar μFTFs in different flexible devices.

The deposition conditions such as the temperature of the substrate and the pressure of the deposition chamber play significant roles during the growth and the fabrication of columnar μFTFs, as discussed in Chapter 5. Hence, to define the parameters space of the deposition process of the Parylene-C columnar μFTFs, a systematic study of the deposition conditions such as the temperature of the substrate, the pressure in the chamber, and the rate and time of the deposition is needed in order to obtain a better understanding of the growth and the fabrication of Parylene-C columnar μFTFs.

10.2.2 Parylene-C columnar μFTFs as a substrate for flexible electronics

Mechanical flexibility is an essential feature for any flexible device. An important design parameter for flexible devices is the radius of curvature r_{crit} at which the flexible device fails electrically due to irreversible mechanical degradation [1]. The parameter r_{crit} is a function of the critical strain $\varepsilon_{\text{crit}}$ that can be sustained by the flexible device; thus [1]

$$r_{\text{crit}} = \frac{d_s}{2\varepsilon_{\text{crit}}}, \tag{10.1}$$

where d_s is the thickness of the substrate.

The mechanical properties of Parylene-C columnar μFTFs were found in Chapter 6 to depend on the deposition angle χ_v. They are lower than of their counterparts for bulk Parylene C by about two orders of magnitude. Parylene-C columnar μFTFs are softer than bulk Parylene C. Therefore, the use of Parylene-C columnar μFTFs as a substrates could improve device flexibility.

To validate this hypothesis, MIS structures, introduced in Chapter 9, containing either a Parylene-C columnar μFTF or bulk Parylene C as the substrate can be bent to different values of the radius of curvature while being electrically tested. The MIS structure can be bent to different degrees, while applying the same systematic analysis provided in Chapter 9, before and after an appropriate combination of electrical and mechanical stresses.

10.2.3 Parylene-C columnar μFTFs as a composite dielectric

In contrast to the pinhole-free films of bulk Parylene C, every columnar μFTF is a group of parallel microfibers inclined at an angle $\chi \in (0°, 90°]$ with respect to the substrate plane. Also, air occupies the inter-microfiber regions. Therefore, a columnar μFTF is a composite material comprising Parylene C and air as its constituent materials.

In disordered materials (such as Parylene-C columnar μFTFs), the electric field saturates and never reaches the value of the externally applied electric field [163], as discussed in Sec. 8.4. Parylene-C columnar μFTFs could be considered as electrostrictive polymer composites [179] that have the capability of realizing conversion between electrical and mechanical energy to be utilized as micro-actuators in different applications.

To validate this assumption, an empirical model proposed by Capsal et al. [163]

can be used. Beginning with Eq. (7) of Capsal et al. [163], I get

$$P = 3\varepsilon_o \kappa E_{sat} \tanh\left(\frac{E_{ext}}{3E_{sat}}\right), \tag{10.2}$$

which can be simplified to

$$P = \varepsilon_o \kappa E_{sat} \tanh\left(\frac{E_{ext}}{E_{sat}}\right). \tag{10.3}$$

Because $E_{ext} \ll E_{sat}$ from the definition of the local field and its Lorentzian prescription [160], one gets

$$\frac{\kappa + 2}{3} = E_{local} = E + \frac{P}{3\varepsilon_o}, \tag{10.4}$$

which gives

$$E = \frac{\kappa}{\kappa - 1} E_{sat} \tanh\left(\frac{E_{ext}}{E_{sat}}\right). \tag{10.5}$$

For $\kappa = 2.74$ then,

$$E = 1.6 E_{sat} \tanh\left(\frac{E_{ext}}{E_{sat}}\right). \tag{10.6}$$

To incorporate this empirical model [163], Eq. (10.6) should be modified to

$$E = E_{sat} \tanh\left(\frac{E_{ext}}{E_{sat}}\right). \tag{10.7}$$

Equation (10.6) will yield Eq. (10.7) if only κ is significantly larger than 10. Therefore, Parylene-C columnar μFTFs could be considered as an electrostrictive polymer composites.

A Parylene-C columnar μFTF has the potential to be used also as an electrostric-

tive polymer composite by adding small amounts of organic/inorganic micro/nanoparticles to enhance κ ($\kappa > 10$). This approach [163] is used to engineer nanostructures by introducing nanofillers with κ similar to that of the matrix for energy-harvesting applications.

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Vita

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