THE DEVELOPMENT AND USE OF A TRADE SPACE VISUALIZATION MODEL
FOR SOFTWARE-DEFINED RADIO RECEIVER DESIGN

A Thesis in
Electrical Engineering

by

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ABSTRACT

Software-defined radio (SDR) systems are flexible communications systems in which key operational radio characteristics are reconfigurable and defined in software. Free from many of the rigid constraints associated with traditional hardware radio (HR) systems, SDR systems are driving modern communications technology development and innovation. However, the ability to develop highly reconfigurable radio systems gives rise to a large number of difficult and complex multivariable design decisions involving tradeoffs between many design criteria. Essential system features such as cost, radio flexibility, size, weight, and power result not only from typical component selection choices but also from complex decisions such as those surrounding the determination of what will be defined in software versus hardware. The massive quantity of design alternatives and the complexity of the selection provide a challenge to the designer that can be overwhelming, motivating the need for new design tools. One tool that could serve to benefit SDR developers is a trade space visualization tool that supports multi-dimensional data visualization of design alternatives, tradeoffs, and goals. Such a tool would allow SDR developers to simulate design alternatives and visualize them while determining and analyzing design preferences for selection. This work describes the considerations, development, and use of a proof-of-concept model for trade space visualization of simple, single-RF-chain SDR receiver design to show the merits and feasibility of trade space visualization for SDR system design. For this work, system components were cataloged into SDR receiver component databases (SR-CDs), an SDR receiver model (SDR-RM) was developed, and an existing trade space visualization tool was leveraged that was developed at the Applied Research Laboratory (ARL) at The Pennsylvania State University called the ARL Trade Space Visualizer (ATSV).
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Chapter 1

Introduction

Software-defined radio (SDR) systems are flexible communications systems in which key operational radio characteristics are reconfigurable and defined in software [Buracchini, 2000; Mitola, 1995]. Free from many of the rigid constraints associated with traditional hardware radio (HR) systems, SDR systems are driving modern communications technology development and innovation. Enabled by rapid and dramatic improvements in semiconductor technology, SDR systems are offering levels of radio flexibility never before seen [Brannon, 2008].

The reconfigurable and flexible nature of SDR systems give rise to numerous benefits over traditional hardware radios. One such benefit is enabling radios to achieve sweeping interoperability. By facilitating significant changes to the frequency band and type of waveform transmitted and received by the radio, SDR systems are able to offer true interoperability to the military, to the numerous domestic and international agencies that respond to disasters and emergencies, and to consumers accessing cellular communications infrastructure. Another benefit of SDR systems over traditional HR systems, beyond interoperability, is the simplification of radio manufacturing since single hardware platforms can support a multitude of radio applications. Their reconfigurable nature is bringing about dramatic and rapid changes in radio technology [Brannon, 2008].

The ability to develop highly reconfigurable radio systems also poses a significant challenge to designers. SDR designers are faced with many complex decisions based on given design criteria associated with determining to what extent a radio can be reconfigurable and how to enable this flexibility. As with other design fields, design tools can serve to greatly benefit designers facing the complex decisions associated with cutting-edge system design.
1.1. **Motivation**

Enabling the highly reconfigurable nature of SDR systems is associated with a large number of difficult and complex multivariable design decisions involving tradeoffs between many criteria. Essential system features such as cost, radio flexibility, size, weight, and power result, not only from typical component selection choices, but also from complex decisions such as those surrounding the determination of what will be defined in software versus in hardware. The large number of design alternatives and the complexity of the selection provide a challenge to the designer that can be overwhelming without the aid of various tools.

As shown in Chapter 2, some early work has been done in the area of developing design tools for SDR design. This early work, done by a NASA team, serves to emphasize the need for design tools to aid SDR designers in making key design decisions. Continued work in the space was needed, and it is clear that SDR designers could benefit greatly from multiple effective design tools.

A robust and comprehensive trade space visualization tool is under continuous development at the Applied Research Laboratory (ARL) at The Pennsylvania State University called ATSV [Simpson et al., 2008]. The ARL Trade Space Visualizer (ATSV) is a Java-based tool that facilitates trade space visualization of existing databases of design alternatives or databases of designs generated on-the-fly by an external model. ATSV offers a multitude of visualization options that help users evaluate complex, multivariable design decisions including decisions directly linked to preferences specified by the user to alter a trade space in real time.

Given the need for SDR design tools to aid in complex decision making, and given the access to the ATSV tool at Penn State, this work was developed to pursue the creation of a proof-of-concept SDR receiver design model to be linked to ASTV for the implementation of SDR receiver design trade space visualization. Such a combined tool would allow SDR designers to...
visualize and explore feasible SDR receiver design alternatives in the context of multivariable receiver output specifications and the related relationships, trends, and tradeoffs associated with decisions. ATSV, which facilitates the identification of most preferred designs and optimal Pareto frontiers based on user-generated design goals, would allow SDR designers to view their existing or conceptualized SDR receiver designs against other alternatives in the trade space to help facilitate multivariable understandings and to foster innovation.

1.2. Contributions

The primary purpose of this work is to demonstrate the feasibility of visualizing the SDR receiver design trade space through the use of a trade space analysis model and a trade space visualization tool. The primary contribution presented within this work is the development of an SDR receiver model (SDR-RM) used to model single RF chain superheterodyne SDR receiver architecture in a manner suitable for the visualization of critical output specifications of simulated, feasible designs using an existing trade space visualization tool: ATSV. This primary contribution is supported by SDR receiver trade space visualization examples conducted using the developed SDR-RM and the leveraged ATSV tool. Also contributed by this work is the necessary background information to support the developed SDR-RM and the use of ATSV.

1.3. Overview of the Thesis

This thesis is organized into six chapters. The first of these chapters is the introductory material.

Chapter 2 provides necessary background material with respect to SDR, early work in the SDR design tool space, and trade space visualization. The SDR background places an emphasis
on SDR receiver architecture and associated considerations essential to modeling an SDR receiver system for trade space analysis. Background material on SDR design tool work is focused on a particular SDR design tool developed by a NASA group. Background material concerning trade space visualization is focused on the ARL Trade Space Visualizer (ATSV) used in this work.

Chapter 3 provides detailed background regarding critical SDR receiver specifications and considerations essential to the development of an SDR receiver trade space analysis model. The specification definitions, calculations, and assumptions contained within Chapter 3 provide the basis for the model developed and used in Chapter 4 and Chapter 5.

Chapter 4 describes the primary contribution of this work: the development of an SDR receiver model (SDR-RM) and the linking of the model to the ARL Trade Space Visualizer (ATSV) for trade space analysis. The chapter explains the overall approach taken for the visualization of the SDR receiver design trade space, which consists of using ATSV to sample inputs to and visualize outputs from the SDR-RM. The chapter further explains the development and use of the three fundamental components of the SDR-RM: SDR receiver component databases (SR-CDs), the SDR receiver trade space analysis model (SR-TSAM), and the configured link between ATSV and the SDR-RM in the form of configuration files.

Chapter 5 describes the use of the SDR-RM and ATSV by providing example, hypothetical use-cases of the tools. The chapter describes the use of ATSV for the visualization of SDR receiver design at the individual component level using the SR-CDs as well as its use for the visualization of SDR receiver design at the broader, system level using the SDR-RM. At the system level, three hypothetical systems are described and visualized.

Chapter 6 summarizes major conclusions drawn from the work regarding the feasibility of trade space visualization of SDR receiver design using the approach contained herein. The chapter further provides recommendations for future work in the field.
Finally, end-matter is comprised of two appendices. Appendix A contains a list of acronyms and abbreviations used in the work, and Appendix B contains an image appropriate to the work too large to fit within the pages of the work.
Chapter 2

Background Information

This chapter provides a background on software-defined radio (SDR), early SDR design tool work, and trade space visualization. Section 2.1 provides SDR background with an emphasis on receiver architecture and associated considerations of importance to the development and implementation of an SDR receiver model suitable for trade space visualization. Section 2.2 provides background regarding early SDR design tool development by a NASA group. Section 2.3 provides background of trade space visualization, provides an introduction to the ARL Trade Space Visualizer (ATSV) used in this work, and provides the context for the trade space exploration methods of this work.

2.1. Software-Defined Radio Background

Critical operational radio characteristics and attributes are reconfigurable and defined in software for SDR systems [Buracchini, 2000; Mitola, 1995]. Unlike traditional hardware radio (HR) systems, SDR systems generally consist of only minimal analog RF processing, while the bulk of signal processing is handled digitally on a software platform [Hosking, 2006]. Analog processing in SDR systems is generally limited to only that which is necessary to receive and transmit RF signals and to prepare these signals for Analog-to-Digital (A/D) conversion (in the receive path) as well as for Digital-to-Analog (D/A) conversion (in the transmit path). Digital software processing defines such critical radio characteristics and attributes as frequency band and radio channel bandwidth, modulation and coding scheme, radio resource and mobility management protocols, and user applications.
2.1.1. Software Radio Classification

Software-Defined Radio systems are categorized as Tier 2 radio systems in a 5 tier (0–4) classification system used in the field and described in Bilén [2009]. Table 2-1 displays the tier system classification of software radio systems:

Table 2-1: Software radio classification tiers [Bilén, 2009]

<table>
<thead>
<tr>
<th>Tier</th>
<th>Classification</th>
<th>Software Capability Details</th>
</tr>
</thead>
<tbody>
<tr>
<td>Tier 0</td>
<td>Hardware Radio (HR)</td>
<td>No radio characteristics can be controlled or configured in software.</td>
</tr>
<tr>
<td>Tier 1</td>
<td>Software-Controlled Radio (SCR)</td>
<td>Radio functionality can be controlled in software but the radio attributes (i.e., modulation scheme, frequency band) cannot be configured in software.</td>
</tr>
<tr>
<td>Tier 2</td>
<td>Software-Defined Radio (SDR)</td>
<td>Certain key radio attributes are reconfigurable in software (i.e., modulation scheme, frequency band, etc.), but with certain analog hardware/processing requirements including antenna(s), amplification, filtering, and certain heterodyne mixing.</td>
</tr>
<tr>
<td>Tier 3</td>
<td>Ideal Software Radio (ISR)</td>
<td>Essentially, an SDR system without need of analog amplification and heterodyne mixing prior to A/D conversion or after D/A conversion.</td>
</tr>
<tr>
<td>Tier 4</td>
<td>Ultimate Software Radio (USR)</td>
<td>Radio system entirely controlled and configured in software on a single chip requiring no external antenna without any restrictions on operating frequency.</td>
</tr>
</tbody>
</table>

Tier 4: Ultimate Software Radio (USR) represents a currently infeasible system for actual implementation, but is defined to establish a case for comparison of lower tier software radio capabilities. Tier 3: Ideal Software Radio (ISR) represents a perhaps more attainable standard in which the only analog components of a radio communications system required prior to or after data conversion would involve the antenna(s) necessary for reception and transmission of signals. Modern technology generally facilitates Tier 2: Software-Defined Radio (SDR), which has an architecture that includes required analog components beyond antennas including band-pass
filters (BPFs), low noise amplifiers (LNAs), and, likely, RF mixers [Bilén, 2009, Buracchini, 2000].

2.1.2. Software-Defined Radio Receiver Architecture

SDR receivers leverage multiband antennas, traditional RF/IF front-end processing, wideband A/D conversion, and, most defining and importantly, the implementation of baseband (and possibly further IF) and bit stream processing functions in general-purpose programmable processors [Mitola, 1995]. The critical aspect of SDR architecture that enables increased flexibility over traditional hardware radios is the conversion of analog signals to digital signals directly after a receiver RF front-end for further baseband processing. While large multiband SDR receivers might require multiple RF chains, this work will consider single RF chain receivers to pursue the development of an early SDR receiver model for use with a trade space visualization tool. The basic, single-RF-chain receiver architecture considered and used within this work is a digital radio receiver architecture based on a traditional, single RF chain, superheterodyne receiver, which therefore first be considered.

As shown in Figure 2-1, the architecture of a traditional superheterodyne receiver proceeded by digital baseband processing can be broken down into three fundamental stages: the Radio Frequency (RF) stage, the Intermediate Frequency (IF) stage, and the Baseband (BB) stage [Buracchini, 2000].
In a basic single-RF-chain, superheterodyne receiver like that shown in Figure 2-1, the RF stage generally consists of RF signal reception at an antenna, RF signal filtering through a band-pass filter (BPF), and RF signal amplification through a low-noise amplifier (LNA); or some similar variation of this basic structure. The IF stage of a traditional superheterodyne receiver generally consists of analog downconversion of the amplified RF signal via mixing with the signal from an local oscillator (LO), filtering of the resulting IF signal through a low-pass filter (LPF), and amplification of the filtered IF signal possibly controlled by an automatic gain control (AGC) mechanism. The BB stage includes separation of the In-phase and Quadrature (I/Q) signal components during analog mixing with a baseband signal from a voltage-controlled oscillator (VCO) controlled by signals from the baseband processor via a digital-to-analog converter (DAC), filtering of the I and Q BB components through LPFs, amplification of the BB components through RF amplifiers, analog-to-digital (A/D) conversion of the BB components via analog-to-digital converter(s) (ADCs), and, finally, digital baseband processing by a processor such as an ASIC (application-specific integrated circuit) [Buracchini, 2000; Rhode and Whitaker, 2001].

The RF and IF stages of the traditional super-heterodyne receiver are implemented entirely with analog hardware, and the BB stage is also implemented with analog hardware with the exception of digital signal processing on the recovered BB signal for further information.

**Figure 2-1:** Traditional superheterodyne receiver architecture [Buracchini, 2000]
recovery and use. SDR systems are designed for increased radio flexibility through the use of
digital, software-based processing, and therefore it is desirable to condense as much of the RF, IF,
and BB stages into the digital domain as possible. Furthermore, modern advances in DSP
technology have enabled the digital back-end capabilities that allow for this analog-to-digital
push. Converting analog signals into the digital domain as soon as possible in the receive path
comes with many advantages best summarized by the simple fact that the earlier this occurs, the
larger the number of receiver functions that can be implemented in the digital domain. The
advantages of digital domain implementation of receiver functions are numerous. For example,
filters can be fully reconfigured in the digital domain to alter how and what signals are passed;
possibilities for complex modulation/demodulation schemes are limitless and come with no
quadrature errors in the digital domain, unlike in the heavily limited analog domain; digital
mixing of signals is highly precise and limited only by the bit precision of the digital math used as
opposed to analog mixing, which often comes with numerous inaccuracies and unwanted mixer
products; and digital receiver functions are consistent when reproduced as opposed to analog
hardware components that often have certain inconsistencies even between the same devices.
Figure 2-2 shows a radio architecture representing ideal software radio receiver architecture with
A/D conversion implemented early in the receive path [Brannon, 2008; Buracchini, 2000;
Papantonopoulos, 2007].

![Ideal software radio receiver architecture](image)

**Figure 2-2:** Ideal software radio receiver architecture [Buracchini, 2000]
In the single-RF-chain ideal software radio receiver shown in Figure 2-2, only three analog components are used prior to A/D conversion: an antenna, a BPF, and an LNA. The Ideal Software Radio (ISR) classified as Tier 3 would include only an antenna prior to A/D conversion, but the ideal radio architecture of Figure 2-2 illustrates a more attainable ideal SDR receiver (Tier 2). In the ideal SDR configuration of Figure 2-2, RF signals only need to be received, filtered from noise and irrelevant frequency bands, amplified, and converted to digital samples by an ADC for signal recovery at baseband and further digital signal processing (DSP) at baseband [Bilén, 2009].

While the ideal software radio receiver architecture of Figure 2-2 represents a more attainable ideal architecture than theoretical Tier 3 radio and, in fact, is revisited to some extent in Chapter 4, there are still certain technical limitations that prevent it from being fully realizable for most modern SDR receiver designs [Buracchini, 2000]. First of all, SDR systems intended for significant multiband use cannot yet be realized with such architecture due to the nonexistence of antennas and LNAs capable of bandwidth ranging the full spectrum of potential interest. However, this limitation holds true for any single RF chain SDR system, which is the focus of this work. True, broad multiband systems can be realized with the addition of further RF chains and stages. Therefore, some more noteworthy technical limitations preventing the use of the Figure 2-2 architecture involving the ADC are considered.

A/D conversion involves the sampling of an analog signal and the conversion of the sampled signal to discrete digital values according to one of numerous conversion methods. Therefore, a critical specification for an ADC is its sampling rate, or sampling frequency, which determines the analog signal frequency and bandwidth that can be sampled effectively by the ADC. According to the Nyquist–Shannon sampling theorem, in order to sample a signal without aliasing, the ADC must have a sampling rate of at least twice that of the signal bandwidth and/or twice that of the signal frequency. This would suggest that a 2.4-GHz signal would require an
ADC sampling rate of at least 4.8 Gsps (gigasamples per second), which is not generally practical with modern ADC technology. A more practical implementation would be to downconvert the 2.4-GHz signal to an IF frequency level such as 70 MHz with an analog IF stage, which would then require a more attainable ADC sampling rate of at least 140 Msps (megasamples per second). This limitation can be avoided within reason in some cases through the use of sub-sampling, which allows for the careful selection of ADC sampling rates for high frequency signals to exploit aliasing and retain the ability to recover the signal. In this case, the sampling rate of the ADC limits only the bandwidth of the signal and is addressed further later in this work. However, sub-sampling is only possible with ADCs that have full analog bandwidths that exceed the sampling rate of the ADC. In other words, the ADC must accept signals at higher frequencies and not attenuate signals that exceed the sampling rate. Nevertheless, even if sub-sampling is assumed possible in all design cases, thereby allowing the ideal software radio receiver architecture of Figure 2-2, other critical ADC characteristics provide yet other limitations resulting in a typical need for at least one analog IF stage [Altera Corporation, 2007; Buracchini, 2000; Mitola, 1995; Rives, 2006].

Another critical ADC specification that limits the feasibility of the ideal software radio architecture of Figure 2-2 is the spurious-free dynamic range (SFDR) of the ADC. The extent to which a receiver can successfully process low-level signals and reject larger interference is closely related to the signal-to-noise ratio (SNR) and SFDR of the ADC. While these characteristics also have far reaching effects on the receiver that are explored further in this work, the SFDR can contribute to the need for a radio to have an IF stage. SFDR is the ratio, measured in dBc (a measurement of the ratio of signal noise in reference to a carrier), of the desired carrier signal to the next highest spurious component, harmonic or not, in the output of the ADC. While many modern high-end ADCs offer high levels of linearity, SFDR still tends to be non-linearly related to analog input frequency. The higher the analog input frequency, the worse the SFDR
performance and, therefore, at high RF frequencies an IF stage would be more practical than a lack of one in order to maximize necessary SFDR performance. SNR can also exhibit similar non-linear behavior and impose similar limitations as SFDR on the overall system. Furthermore, even when performing linearly, the raw values of the SNR and SFDR specifications can limit the actual input signals the ADC can accept and effectively convert to such a great extent that filtering, amplification, and mixing prior to conversion may be required [Papantonopoulos, 2007; Schratz, 2007].

A further ADC limitation preventing widespread practical use of the Figure 2-2 receiver architecture involves timing jitter. Internal ADC jitter adds to the sampling clock and, as with SFDR, overall performance decreases as frequency is increased. Jitter not only makes A/D conversion directly at RF highly difficult, but it further places limits on how high an IF stage frequency can be prior to conversion [Buracchini, 2000; Papantonopoulos, 2007]. The sampling rate, SFDR, SNR, and jitter characteristics of an ADC within an SDR system can all contribute to a need for at least one analog IF stage in the receiver architecture, despite the push to provide as many radio functions digitally as possible. Hence, the following digital radio receiver architecture in Figure 2-3 represents a more practical SDR architecture and that which is used throughout the majority of this work.

![Digital radio receiver architecture](image-url)

**Figure 2-3:** Digital radio receiver architecture [Buracchini, 2000; Hosking, 2006]
The digital radio receiver architecture shown in Figure 2-3 is similar to the traditional superheterodyne receiver of Figure 2-1 in that it begins with an analog RF stage followed by an analog IF stage. However, unlike the Figure 2-1 architecture, the receiver converts the analog signal to digital form directly at IF for further digital signal processing such as digital mixing to baseband, digital filtering, and digital demodulation. In this receiver architecture, functions typically performed in analog RF circuitry in a traditional superheterodyne receiver are performed in a digital receiver chip. The digital receiver chip is also referred to either as a digital downconverter (DDC), a digital drop receiver (DDR), or a programmable downconverter (PDC) [Buracchini, 2000; Hosking, 2006]. This receiver architecture is more carefully explored in the following section.

2.1.3. The Single-RF-Chain Superheterodyne SDR Receiver Architecture

For the purposes of this work, the digital radio receiver architecture of Figure 2-3 is referred to as a single-RF-chain superheterodyne SDR receiver. The analog RF and IF stages of the receiver architecture are essentially the same as those of the traditional superheterodyne receiver: analog RF signals are received at an antenna, filtered, amplified, mixed to IF, further filtered at IF, and then amplified at IF (the IF amplification stage may include AGC). Beyond the analog IF stage is where the superheterodyne SDR receiver of Figure 2-3 differs from the traditional superheterodyne receiver of Figure 2-1. The IF signal is still separated into I and Q components, downconverted to baseband, and filtered; however, rather than taking place in analog RF circuitry, these processes take place in the digital domain on the digital receiver chip. The block diagram shown in Figure 2-4 shows the general breakdown of these functions in the digital receiver chip.
Figure 2-4 shows a likely configuration of the digital receiver chip, or digital downconverter (DDC), within the single-RF-chain superheterodyne SDR receiver architecture. The primary input to the DDC is the digital form of the IF signal generated by the ADC, which is a stream of digital samples with a sample frequency equivalent to the sampling frequency of the ADC, $f_s$. This stream of bits is first mixed with samples from a digital local oscillator [Hosking, 2006].

The local oscillator (LO) of the DDC is a direct digital frequency synthesizer (DDS), otherwise referred to as a numerically controlled oscillator (NCO) that outputs digital samples of two signals: a sine wave and a cosine wave (offset by 90°). Given an ADC clock input, these signals are sampled at precisely the same sampling frequency as the ADC sample clock frequency; hence, the DDC output is at $f_s$. The actual signal frequency of the sampled sine and cosine waves is determined by the programmable and directly proportional phase advance per sample. This phase advance is programmable from DC to $f_s/2$ (according to the Nyquist criterion) [Hosking, 2006].
The samples from the DDS are next mixed with the digital samples from the ADC via mathematical multiplication through two digital multipliers: the ADC samples are mixed with the DDS sine wave samples through one multiplier and are mixed with the DDS cosine wave samples through the other. The two multipliers output the complex I and Q components of the signal respectively. Each component consists of digital samples at $f_s$, whose signal information has been downconverted from IF. Digital downconversion at this stage is likely from IF to baseband, but, in some cases where further IF stages are required, a second IF stage may be digitally implemented prior to further digital downconversion to baseband. As briefly discussed with respect to the ideal software radio receiver architecture of Figure 2-1, wherever possible IF stages should be implemented digitally as opposed to in analog circuitry, which applies to single-IF-stage and multi-IF-stage designs alike [Hosking, 2006; Mitola, 1995]. The primary advantages to implementing necessary IF stages digitally when possible include: the enablement of digital signal processing prior to signal detection and demodulation; the reduction of the cost of mixed channel access modes; and the focusing of numerous “component tradeoffs to a single central issue: providing the computational resources (I/O bandwidth, memory, and processing capability) critical to each architecture segment, subject to the size, weight, power, and cost constraints of the application” [Mitola, 1995]. This mixing is highly efficient: unlike analog mixers, the digital mixer is nearly ideal and does not generate unwanted mixer products [Hosking, 2006].

The resulting I and Q digital sample streams at $f_s$, with signal information now at BB are next passed through a decimating low-pass filter. Through digital signal processing methods, the LPF implements a finite impulse response (FIR) filter transfer function. Through the process of signal decimation, the filter passes signals from 0 Hz to a programmable cutoff frequency or bandwidth. As a complex filter, it is capable of outputting complex I and Q components as well as real values. The bandwidth of the filter is programmable through the adjustment of the filter’s decimation factor, $N$. The value of $N$ also further dictates the output sampling rate of the complex
and real outputs of the filter [Hosking, 2006]. The effects of $N$ on all three of these values are found according to,

$$\text{Output Filter Bandwidth} = \frac{f_s}{N},$$  \hspace{1cm} (Eq. 2-1)

$$\text{Complex Output Sampling Rate} = \frac{f_s}{N}, \text{ and}$$  \hspace{1cm} (Eq. 2-2)

$$\text{Real Output Sampling Rate} = \frac{2 \cdot f_s}{N}.$$  \hspace{1cm} (Eq. 2-3)

The DDC has served fundamentally the same function in the single-RF-chain superheterodyne SDR receiver as the analog component of the BB stage in the traditional single-RF-chain superheterodyne receiver. The DDC receives digital sample inputs representing the IF signal, then, via a programmable local oscillator and digital multipliers, the signal is translated down to DC centered on 0 Hz, and, finally, the baseband signal is passed through a programmable filter to pass only the band of interest through as a digital stream of samples for further digital signal processing. What is fundamentally different about these DDC functions as those found in analog RF circuitry in the traditional, hardware radio is that they are highly reconfigurable without changes to hardware. The mixing stage and filter stage are easily reprogrammable, allowing for changes to acceptable input IF signal frequency and bandwidth as well as for changes to output bandwidth [Hosking, 2006]. Just as with the traditional superheterodyne receiver’s analog BB stage, the output signal from the DDC can then be passed to a DSP for further processing if desired and necessary prior to being passed to its end-use hardware or software. However, with modern technology, DDC functionality often can be combined with some and, in cases of minimal needs, all DSP functionality.

Increasingly, FPGAs (field-programmable gate arrays) are being used to perform the functions of the DDC [Hosking, 2006]. FPGAs are “organized as an array of logic elements and programmable routing resources used to provide the connectivity between the logic elements, I/O
pins and other resources such as on-chip memory, digital clock managers, embedded hardware multipliers, embedded microprocessors and multi-gigabit transceivers” [Benson and Lall, 2004]. With built-in hardware multipliers and large amounts of RAM (random access memory), FPGAs are not only sufficiently capable of handling DDC tasks, but also offer further radio flexibility over ASIC DDCs given their readily re-programmable nature. Furthermore, FPGAs are equipped to handle digital signal processing tasks traditionally only handled by DSPs for low sample rate applications and ASICs for high sample rates. FPGAs can add DSP performance to a system typically only possible with custom ASICs, but are more reconfigurable and are without the large costs associated with custom ASIC production [Benson and Lall, 2004; Hosking, 2006].

While not all systems require further DSP processing, many systems do require additional processing beyond the DDC whether handled on an FPGA or a DSP processor. For example, demodulation tasks can be implemented on an FPGA or DSP processor by loading the appropriate algorithm(s), energy scanning algorithms can be implemented with an FFT (fast Fourier transform), cryptography analysis can be implemented, etc. With this signal analysis in the digital domain, any changes that need to be made in the future, such as new modulation schemes, can be made to existing hardware with new software, particularly when implemented on FPGAs [Hosking, 2006].

The single-RF-chain superheterodyne SDR receiver is used throughout the remainder of this work and is the architecture implemented in the trade space visualization model and tool presented in Chapter 4.
2.2. **SDR Design Tool Background—An Early Tool: Space Transceiver Analysis Tool**

Design tools are paramount to the design process in emerging and developing technologies, and particularly those that involve numerous and complex decisions and tradeoffs. Design tools stand to benefit greatly the development of software-defined radio technology.

Moore et al. [2005] presented “a tool chain, methodology, and initial results of a study to provide a thorough, objective, and quantitative analysis of the design alternatives for space Software Defined Radio (SDR) transceivers” [Moore et al., 2005]. The paper describes the development and use of the Space Transceiver Analysis Tool (STAT), which was developed as part of NASA GRC’s Space Telecommunications Radio Systems (STRS) project conducted by NASA GRC, General Dynamics, and Southwest Research Institute. The STRS project’s purpose is to evaluate the applicability and tradeoffs of using SDR in space missions. Focused on space missions, the STRS team set out to quantitatively assess all the major costs associated with employing SDR technologies such as size, weight, power, latency, and development costs. The team also set out to understand the costs of adopting an open standard architecture for space-based SDR transceivers considering two primary approaches: either leveraging the existing and robust Joint Tactical Radio System (JTRS) Software Communication Architecture (SCA) or developing a tailored, space-specific NASA architecture. While the STAT therefore was tailored by the STRS team specifically to SDR systems and software-based reconfigurable transceivers (RTs) for space flight applications, it also presents a useful approach to design for the entire SDR design space [Moore et al., 2005].

More et al. [2005] describes, the STAT “was developed to help users identify and select representative designs, calculate the analysis data, and perform a comparative analysis of the representative designs,” and to allow “for the design space to be searched quickly while permitting incremental refinement in regions of higher payoff” [Moore et al., 2005]. Prior to
using the STAT for system analysis, designers first build models of four aspects of the SDR transceiver system: “(1) the communications requirements for space missions, (2) the wireless communications waveforms that are used for space applications, (3) the computer hardware available for space flight, and (4) the properties of the various software architectures that could be used to implement the transceivers” [Moore et al., 2005]. Mission models are used to provide important mission communication requirements such as channel, frequency, waveform, data rate, etc. and specifications for all stages of the mission such as launch, orbit, etc. Waveform models provide specified “algorithms used to implement a communications channel endpoint” and all associated specifications and implications. Hardware models stored in a pre-defined database are used to provide the available computational resources of a particular hardware platform such as MIPS, gates, and memory as well as other attributes including clock speed, size, weight, and power consumption. Infrastructure models, comprised of infrastructure components (such as real-time operating systems and middleware layers), provide details regarding resource requirements such as processing and communication overheads, dynamic memory size, static memory size, and configuration time [Moore et al., 2005].

The user-generated models are mapped to a specific hardware platform in order to form the basis for a test case as a point design, referred to as “as-built transceivers.” The STAT then specifies and analyzes properties of each as-built transceiver test case. These as-built transceivers represent choices of “hardware platform, software infrastructure, waveform algorithms, channel parameters, and mapping of waveforms components onto hardware components” [Moore et al., 2005]. Software components are allocated to hardware components as part of an implementation platform involving hardware and software infrastructure selection based on mission requirements. The STAT determines the validity of an as-built transceiver design based on whether utilized resources are within available resources and whether or not modem latency is within mission specifications. A valid, as-built transceiver design is analyzed by the STAT for the quantification
of resource utilization, SWaP (size, weight, and power), and modem latency. Resource utilization analysis includes the evaluation of generic operations per second (MOPS – million generic ops/sec), FPGA/ASIC logic gates (kLEs – kilo logic equivalents), throughput (MBps – megabytes/sec), clock rate (MHz), clock count (number of clocks), and memory (MB – megabytes). SWaP analysis includes the evaluation of footprint (cm$^2$), volume (cm$^3$), mass (grams), power (mW), non-recurring engineering (NRE) costs (USD), system cost (USD), and availability (year) [Moore et al., 2005].

The STAT particularly focused on the software platform component of SDR design. Even the hardware analysis in the STAT had a software emphasis by focusing on evaluating a hardware configuration’s ability to facilitate particular software platforms as well as evaluating the impact of hardware design decisions on software platform selection. This is due to the STRS project’s focus on evaluating the options for developing an SDR open standard architecture for space flight missions to enable SDR use in space flight design. However, the tool captures well the SWaP characteristics critical to SDR designers [Moore et al., 2005].

The STAT was successfully tested using the Landsat 7 satellite launched on April 15, 1999 as a test mission. More et al. [2005] concludes based on the analysis of the tool and its Landsat 7 test case that “the STAT supports a thorough, objective, and quantitative analysis of the design alternatives for space transceivers.” The paper further concludes that as the STAT continues to be used and developed, the model database will grow further enabling the tool to become more accurate and, hence, a part of the transceiver design process. It highlights some suggested future work such as including in the STAT “an ability to conduct parametric analysis by automatically varying channel requirements or design choices such as waveform algorithm selections, hardware component properties, software to hardware allocation, and infrastructure properties [Moore et al., 2005].” It suggests the realization of these goals by “leveraging contemporary work in design space exploration and extending the tool with the ability to
automatically identify valid designs (those which meet requirements and have acceptable resource utilization margins) [Moore et al., 2005].”

The Space Transceiver Analysis Tool represents a start of a highly powerful design tool to be included as one of hopefully numerous tools available to software-defined radio designers.

2.3. Trade Space Visualization Background—The ARL Trade Space Visualizer

Given their growing capacity and complexity, many modern technologies are best viewed as extensive systems comprised of numerous components, each with their own inputs, outputs, interfaces, purposes, constraints, etc. In fact, these components can be, and are often, best viewed as sub-systems further broken down into their own individual components. As technology systems grow increasingly sophisticated, design engineers are faced with an increasing number of design tradeoffs, information, and possibilities. Trade studies are highly useful tools for the decision process when faced with such complex and diverse challenges. Fortunately, as modern computing capabilities increase, it is possible for technology system designers to more easily pursue such studies by automatically simulating thousands and even millions of design alternatives relatively cheaply and quickly, thereby enabling extensive analysis of the design space. However, without proper trade space exploration tools that support extensive multi-dimensional data visualization, the resulting data from such simulations has the potential to become overwhelming to the point of uselessness [Simpson et al., 2008].

2.3.1. Trade Space Studies and Trade Space Exploration Tools

Trade studies can be a useful tool in the design process of particularly complex systems. In fact, for the development of space systems, the NASA Systems Engineering Handbook
[NASA, 2007] cites trade studies as a critical part of the systems engineering and decision analysis process. According to the handbook, a trade study begins with the definition and identification of system goals/objectives and constraints. The basic outline for a trade study according to the process explained in the NASA Systems Engineering Handbook can be seen in Figure 2-5 [NASA, 2007].

As seen in Figure 2-5, the general outline of a NASA-defined trade study consists basically of first defining and identifying all design goals and constraints, performing functional analysis of these parameters against design alternatives, analytically measuring and computing resulting design specifications and trade study metrics for each design alternative, making design selections, checking selection acceptability, and, finally, feeding trade study outputs to further analysis processes. Without a trade study like that defined by NASA, the design and decision-making approach to a complex system will often not address the broad space of possible designs,
thereby limiting a designer or design team only to what knowledge and/or design practices already exist. Unfortunately, trade studies can be highly resource intensive, which is why exploiting modern computing power to pursue automation of such studies with trade space exploration tools is of significant interest [NASA, 2007; Richards, 2009].

With the proper computer-based system models and supporting computer software, trade space exploration tools can produce results similar to those achieved from trade studies but more simply and automatically. A common trade space exploration process with such tools involves three steps/components as visualized in Figure 2-6 [Simpson et al., 2008].

![Figure 2-6: Typical Approach to Trade Space Exploration](image)

In the process displayed in Figure 2-6, a simulation model is first developed for system analysis that captures the relationships between design inputs and design outputs. Since these relationships may or may not be known, a “black box” model may be employed. Experiments are then run iteratively using many—hundreds, thousands, or even millions—design alternatives by varying the model inputs and capturing corresponding outputs for each sample. Finally, captured
results can be interactively visualized and explored by trade space exploration software. Results can be checked for design feasibility and checked against custom design preferences. Often, this analysis includes the identification of most preferred point designs or Pareto frontiers displaying Pareto-efficient designs. Because tools of this kind facilitate the simulation and processing of massive amounts of design alternatives based on many variables and inputs, the resulting output data can easily overwhelm designers to the point of rendering results useless. Advanced and comprehensive visualization capabilities can help prevent the overwhelming nature of these results by presenting visual representations and control of trends found in the results [Simpson et al., 2008].

2.3.2. Trade Space Visualization and ATSV

Graphical visualization of a trade space provides designers with the ability to quickly identify trends and tradeoffs in a design space of interest based on model inputs and constraints. Visualization can also be used interactively to further drive trade space exploration. Interactive, real-time visualization can be used to provide designers with the ability to modify, delete, and even add objectives and constraints on-the-fly while exploring a trade space. Furthermore, with the proper software in place, interactive visualization can be used to steer design by allowing designers to drive the optimization process with visual input and output for improved solutions. However, while many trade space exploration tools include visualization capabilities, they often lack the full suite of visualization features necessary to facilitate comprehensive visual analysis of the entire modeled design space. For example, even some tools that include visual steering of design optimization limit visualization to only two-dimensional and three-dimensional representations of the constraints and objectives. A useful listing of many trade space exploration
tools and their visualization capabilities can be found in the appendix of the work by Simpson et al. [2008].

**Introduction to ARL Trade Space Visualizer (ATSV)**

To present designers with a full suite of trade space visualization capabilities, the Applied Research Laboratory’s Trade Space Visualizer (ATSV) was developed. ATSV is “a Java-based application that displays multi-dimensional trade spaces using any combination of glyph, 1-D and 2-D histograms, 2-D scatter, scatter matrix, and parallel coordinate plots, linked views, and brushing” [Simpson et al., 2008]. While many of the visualization capabilities of ATSV are available in other trade space exploration tools, ATSV includes a full suite of capabilities not typically seen in other packages and also includes some unique functionality that other packages do not support. An example of a capability unique to ATSV is the highly multi-dimensional nature of its three-dimensional glyph plot, which can display “up to seven dimensions by assigning different variables to the x-, y-, and z-axes and the size, color, orientation, and transparency of the individual glyph icons” [Simpson et al., 2008] and can facilitate an eight dimension with the addition of text and still a ninth dynamically varied dimension with preference brushing. The display in Figure 2-7 shows examples of the visualization capabilities of ATSV [Simpson et al., 2008].
Visual Data Representation Capabilities of ATSV

As seen in Figure 2-7, ATSV displays trade space exploration data several ways that together provide a comprehensive solution for trade space visualization. ATSV presents data in 3-D glyph plots, 2-D scatter plots, scatter matrix plots, parallel coordinates plots, 1-D histogram plots, and 2-D histogram plots. When coupled with the preference-defining capabilities of ATSV via its Brush/Preference Controls feature as well as the model sampling techniques of ATSV in its Exploration Engine to be addressed later in this section, these displays offer a real-time useful view of trade space exploration results [Schratz, 2007]. These visualizations are briefly introduced and explained within this section but are best viewed in use in Chapter 5.

**Graphical Displays**

The 3-D glyph plot provides an interactive, three-dimensional display of the samples (each graphical dot representing a point design sample). As previously mentioned, the glyph plot
offers the ability to easily visualize seven dimensions and the further possibility of nine dimensions with display adjustments. Any point design can be selected for a full listing of point details. Pareto frontier visualization can also be enabled on the glyph plot allowing designers to quickly identify Pareto-efficient designs and the trends of preferred configurations. Furthermore, infeasible designs (according to user preferences) can be shown or hidden as desired [Schratz, 2007; Simpson et al., 2008].

The scatter plot provides a two-dimensional visualization of any two variables/attributes for all samples (again, each graphical dot representing a point design sample). As with the glyph plot, additional dimensions can be visualized by leveraging plot point attributes, which, in the case of the scatter plot, include color and text labels. Also, like the glyph plot, the scatter plot can display Pareto frontiers and can show or hide infeasible designs. An additional feature of the scatter plot of particular benefit is a Find Mappings feature that can generate data between variable pairs on correlation, second-order goodness fit, multivariate normality, outliers, uniformity, and number of clusters between variable pairs in the dataset. Furthermore, the scatter plot offers basic curve fitting for orders 1–5 [Schratz, 2007].

Scatter matrix plots are simply the arrangement of the 2-D scatter plots into a matrix such that the relationships between all variables in the model can be viewed quickly in tabular form in the format of an $N^2$ matrix. The designer has the ability to sort variables based on positive or negative correlation as well as to select variables based on kurtosis, outlier estimation, and uniformity/non-uniformity criteria. As with the glyph and 2-D scatter plot, the scatter matrix plots can display Pareto frontiers and show/hide infeasible designs [Schratz, 2007].

The parallel coordinates plot highlights correlations between different variables of the model: variables with strong positive correlations have parallel interconnections between them while those with strong negative correlations have intersecting lines between them. Designers are given the ability to rearrange the variables to view any variable next to any other variable.
Designers are also given the ability to sort variables based on positive or negative correlations as well as to select variables based on skewness, kurtosis, univariate outlier estimation, and uniformity. Again, like the previously described ATSV plots, users can display Pareto frontiers and show/hide infeasible designs [Schratz, 2007].

The histogram plot provides a histogram for each variable, which provides the designer a view of the spread of all variables involved in the model. Designers can use histogram plots to identify design drivers and non-drivers based on the variability of specific design variables and attributes. The histogram plot allows for the designer to find mappings based on skewness, kurtosis, outliers, and uniformity [Schratz, 2007].

The 2-D histogram plot joins the histograms of two variables and thereby affords designers the ability to identify non-intuitive relationships related to the spread of variables that may not come out with the 1-D histogram plots. Designers are able find mappings based on multivariate normality, outliers, uniformity, and number of clusters [Schratz, 2007].

Preference Definition

Of particular importance to the designer in exploring a trade space is the ability to define preferences for design outputs. For example, a designer may want to minimize the cost of a system, minimize the power consumption of the same system, but yet maximize the speed at which the system operates. These multivariable preferences dictate where Pareto frontiers are in the trade space and determine what designs and trends are of interest to the designer. The ability to visualize this during the decision-making process is critical [Simpson et al., 2008].

ATS V includes a “Brush/Preference Controls” system that allows designers to limit displayed point designs by adjusting the allowable ranges of continuous variables or by excluding particular discrete or categorical variable values, and allows designers to establish maximization and minimization goals with assigned weightings. From here, designers can chose to have the most preferred design highlighted in ATSV’s visualization plots. Brush/preference controls are a
critical piece in giving designers the ability to dynamically investigate the tradeoffs they are faced with in design selection. Furthermore, these preferences can be leveraged in the actual generation of data for trade space visualization analysis [Schratz, 2007; Simpson et al., 2008].

**Generation of Data Using ATSV**

To perform trade space visualization, ATSV leverages one of two methods for generating design variables (inputs) and design performance metrics (outputs): (1) generation of inputs and outputs offline as a static dataset to be read into ATSV for visualization and manipulation; or (2) generation of inputs and outputs dynamically and “on-the-fly” by using an “Exploration Engine” to link a simulation model to ATSV for visualization and manipulation in real-time [Simpson et al., 2008].

**Leveraging Existing Databases**

ATSV can be used to visualize results from external static databases that may have been generated a number of ways whether from existing known values for a particular system or from an external system model. ATSV recognizes standard data files such as TXT (often created using a standard text editor) or CSV files (often created using either a text editor or a spreadsheet program such as Microsoft Excel®). ATSV simply recognizes input variable categories by columns and input entries by rows and presents the data in visual form for trade space exploration according to its available capabilities [Schratz, 2007].

**Leveraging the ATSV Exploration Engine and Visual Steering Commands**

A powerful capability of the ARL Trade Space Visualizer is the ability to interface to an external model and drive the model in a similar manner as that displayed for trade space exploration in Figure 2-6. This is done using the Exploration Engine of ATSV that, when properly linked and configured, can vary model inputs across discrete, continuous, or categorical ranges to capture model outputs, which can also be discrete, continuous, or categorical values. By capturing outputs from an external model, such as an Excel-based model, ATSV is able to
generate a database of desired outputs. Furthermore, by using different sampling models, the Exploration Engine offers designers to ability to visually steer the trade space exploration process [Schratz, 2007; Simpson et al., 2008].

“The novelty in [the ATSV] approach to trade space exploration lies in providing designers with a set of visual steering commands to simultaneously explore the trade space and exploit new information and insights as they are gained” [Simpson et al., 2008]. This is done by changing the manner in which the Exploration Engine samples inputs to a linked model used to generate and capture model outputs. Designers have the ability to explore either the entire design space of interest or only along its Pareto frontier via manual or random sampling using a Basic Sampler, Point Sampler, and/or Pareto Sampler. Additionally, designers can exploit information gained from the exploration process and search particular points of interest or regions of high preference using an Attractor Sampler or Preference Sampler [Simpson et al., 2008].

The ATSV Basic Sampler and Point Sampler allow the designer to either randomly or manually generate sample inputs for trade space exploration of resulting model outputs. These samplers are used to explore the design space and, by generating a database of initial outputs, represent the first step to trade space exploration with the ATSV Exploration Engine. Parameterized by user-defined variables for the number of samples and multi-dimensional sampling bounds, the ATSV Basic Sampler uses Monte Carlo random sampling to generate model input values from either a normal or a uniform distribution. The bounds of the input design variables can be reduced at any time during trade space visualization to focus on smaller regions of interest. The Point Sampler simply allows the designer to manually define model input values. This can be done to record specific test cases of interest for inclusion in the overall database of outputs [Simpson et al., 2008].

Once an output database has been generated either from the Basic Sampler or the Point Sampler, ATSV offers further sampling functions that allow for the refinement of the model and
the concentration of sampling to point designs alternatives around particular points or preferences. There are three samplers that facilitate this type of functionality: the Pareto Sampler, Preference Sampler, and the Attractor Sampler [Schratz, 2007; Simpson et al., 2008].

The ATSV Pareto Sampler facilitates the sampling of new points along the Pareto frontier according to the design preferences for all objectives of interest to the designer. The Pareto Sampler leverages an algorithm developed by Madavan [2002] called the Pareto Differential Evolution algorithm to focus sampling to points along a Pareto frontier by using minimization and maximization preferences set by the designer on particular objectives [Simpson et al., 2008].

The ATSV Attractor Sampler allows designers to specify a point of interest in the trade space (by graphically indicating a position on one of the ATSV plots) in order to focus sampling to this position of interest. By leveraging Differential Evolution (DE) and minimizing the DE fitness function, which is defined as the Euclidean distance between sample points and a selected attractor point, the Attractor Sampler generates points close to the attractor [Simpson et al., 2008].

Like the Attractor Sampler, the ATSV Preference Sampler also leverages DE to focus point sampling to user-defined regions of interest in the design space. However, the DE fitness function is defined as the linear weighted sum of the designer’s preference structure laid out in the brush/preference controls. This allows designers to focus exploration on regions of high preference within the design space [Simpson et al., 2008].

By leveraging the visual steering capabilities offered by the different samplers of ATSV, designers are able to effectively explore a design space in a focused and calculated fashion. Coupled with the comprehensive visualization options and capabilities of ATSV, this steering ability gives rise to a tool that cuts down on the overwhelming nature of trade space exploration data.
2.4. Chapter Summary

The primary SDR architecture used throughout this work is the single-RF-chain superheterodyne SDR receiver architecture. This architecture represents a simple, but practical, implementation of an SDR receiver that is sufficient for proof-of-concept modeling. Even simple SDR systems, such as this receiver architecture, require complex, multivariable decision making to enable radio flexibility and to best select from a large number of design alternatives.

Various design tools can aid designers in making complex, multivariable designs. Some early work has been done to pursue the development of such tools for SDR systems. The STAT, a design tool developed for NASA SDR applications, is of particular interest given its promising results and quantitative analysis and exploration of design alternatives.

An effective way to explore design alternatives is through trade space visualization, which consists of interactively visualizing all design alternatives resulting from a trade space exploration process. A particular tool developed by ARL at Penn State, ATSV, offers thorough and robust trade space visualization. Leveraging ATSV for the SDR receiver design trade space would serve to further benefit the field of SDR design tool development.
Chapter 3

SDR Receiver Design Considerations for Trade Space Visualization

In order to properly model a single RF chain superheterodyne SDR receiver for trade space visualization, it is necessary to identify critical radio receiver design specifications, specific design tradeoffs and limitations, and other design selection and implementation considerations. While not all design specifications, tradeoffs, and implementation considerations are modeled by the tool developed in this work and described in Chapter 4, an understanding of many of these is necessary for early as well as continued model development.

3.1. Critical Receiver Design Specifications

SDR receivers can be described according to a large number of specifications. Sections 3.1.1–3.1.6 highlight some the critical specifications from which certain model output specifications were derived for the trade space visualization model to be discussed in Chapter 4. Section 3.1.7 discusses briefly and highlights some other critical specifications. The development of SDR receivers involves both analog and digital components. It is notable that in the determination of overall receiver specifications, the trade space analysis model developed for this work and described in Chapter 4 places a large emphasis on the RF front-end analog circuitry of SDR receiver architecture. This is because the model used for visualization is hardware specification-focused and, as further discussed later, leaves the digital resource availability analysis to the designer via access to individual component specification trade space visualization. Therefore, Sections 3.1.1–3.1.7 have a particular focus, although not an exclusive
one, on overall specifications pertaining to the RF front-end analog circuitry of SDR receiver design within the specific context of SDR systems.

3.1.1. **Size, Weight, and Power (SWaP) Specifications**

Three of the most important specifications for any radio receiver, whether based on an analog or digital architecture, are its size, weight, and power (SWaP) specifications. For most systems, SWaP requirements are well-defined and have limited, if any, flexibility. Consider, for example, a handheld radio intended for mobile use such as the AN/PRC-152 JTRS SCA-compliant handheld radio by the Harris Corporation. The AN/PRC-152 is a tactical military radio intended for mobile field use, which means that its size, weight, and battery life are of critical importance to an end-user such as a deployed warfighter. The Harris Corporation datasheet for the AN/PRC-152 radio provides the physical dimensions of the complete radio with its rechargeable lithium-ion battery in a $2.9 \times 9.6 \times 2.5$ in package with a weight of 2.6 lbs. These end specifications coupled with numerous mechanical design attributes of the radio, such as those that enable in-field durability, suggest that the SWaP requirements placed on transceiver design were very strict [Harris Corporation, 2009; Koski, 2010; Moore et al., 2005].

The power dissipation (consumption) specification is often arguably the most important of the SWaP specifications since it is commonly a leading driver of the other two: size and weight. Furthermore, power dissipation can also have a lot to do with other radio specifications such as available resources for digital capabilities. Overall receiver power dissipation, usually given in mW, is simply the summation of the power dissipation of all receiver components, and may vary depending on the functionality required at any given time. In the single-RF-chain superheterodyne SDR receiver, two major drivers of the final power dissipation specification are the ADC and the FPGA. ADC power consumption can be variable but high-end, high-sample
rate ADCs tend to dissipate a large amount of power relative to the other components in the receiver. FPGA power consumption is also highly variable and is dependent on resource needs as illustrated by the existence of extensive power consumption estimation tools provided by FPGA manufacturers such as those provided by Altera [Altera Corporation, 2010; Koski, 2010; Moore et al., 2005].

Size and weight specifications are determined from the summation of respective individual specifications of the individual receiver components along with final implementation considerations (i.e., layout, mechanical design, support hardware, etc.).

### 3.1.2. Frequency and Bandwidth Specifications

Obvious specifications significant to receiver performance are those directly concerning the frequency band(s) the receiver can operate on. This is of particular interest in the domain of SDR, where increased frequency band capabilities translate to increased receiver flexibility. As with SWaP specifications, the end frequency and bandwidth characteristics of a receiver are likely to follow strict requirements. Again, take the AN/PRC-152 transceiver as an example. The AN/PRC-152 has a total bandwidth of 482 MHz covering a frequency range of 30–512 MHz with a tuning resolution of 10 Hz. This end specification was undoubtedly driven by the need to interoperate on numerous military channels using one of many reconfigurable waveforms (such as MIL-STD-188-181B, SINCGARS, HAVE QUICK II, etc.) [Buracchini, 2000; Harris Corporation, 2009].

Frequency specifications are driven by the RF front-end components (amplifiers, filters, mixers, etc.) in the analog RF and IF stages of the receiver as well as the ADC. RF analog components have individual frequency and bandwidth specifications that directly drive the frequency and bandwidth specifications for the RF front-end of a single-RF-chain
superheterodyne SDR receiver. If the ADC and digital BB processing components could handle any frequency bands, these front-end specifications would drive overall receiver frequency/bandwidth specifications. However, as briefly highlighted earlier in Chapter 2, a leading determinate of these specifications is in fact the ADC [Buracchini, 2000; Mitola, 1995; Rives, 2006].

Since the RF signal center frequency will likely be downconverted to an IF center, and since the sub-sampling technique highlighted in the ADC sampling rate discussion in Section 2.1.2 may be employed, the ADC will most likely directly affect the overall bandwidth capability of the receiver. According to the Nyquist criterion, the sampling rate of the ADC, \( f_s \), will determine the maximum bandwidth that can be digitized and processed without aliasing to be \( f_s/2 \). However, it should be noted that many practical systems in fact require modest oversampling; for example, maximum bandwidth may be determined to be \( f_s/2.5 \) [Mitola, 1995]. Notably, if sub-sampling is not employed, the ADC sampling rate may similarly limit the actual RF stage center frequency in the case of direct conversion or the actual IF stage center frequency in the case of analog downconversion prior to the ADC.

The frequency and bandwidth ranges of a receiver can easily be determined from considering all the ranges of all analog components and the sampling rate capacities of the digital portion of the architecture (primarily, the ADC).

### 3.1.3. Intermodulation Distortion and Intermodulation Intercept Points

Intermodulation distortion (IMD) causes several major issues for SDR receivers and, therefore, has several related specifications to consider including those pertaining to specific components and processes as well as those pertaining to overall receiver performance.
Intermodulation products (IPs), the source of IMD, are the result of unintentional mixing in analog amplifiers and mixers typically occurring when multiple signals close in frequency are processed simultaneously (whether via actual reception or via internal device reflection) and when at least one of these signals is high enough in magnitude to cause the analog hardware to not behave as intended [Bowick, 2008; Whites, 2006].

**Intermodulation and Analog Mixers**

Consider first, the case of intermodulation products in analog mixers. During analog downconversion in the IF stage of a superheterodyne receiver, IF signals are generated as result of the sum and difference of the local oscillator (LO) signals and the RF signals according to [Bowick, 2008]

\[ f_{\text{IF}} = f_{\text{LO}} \pm f_{\text{RF}}. \]  \hspace{1cm} (Eq. 3-1)

While both the sum and difference signals are of equal amplitude, generally it is the difference signal that is passed and used for further processing. The sum signal, which is referred to more formally as the image signal, is then removed by the subsequent IF filter (a BPF in the single-RF-chain superheterodyne SDR receiver introduced in Figure 2-3). However, a secondary IF signal, \( f_{\text{IF}}^{*} \), is generated from the sum of the reflection of the image signal back into the mixer and the second harmonic of the LO signal according to [Bowick, 2008]

\[ f_{\text{IF}}^{*} = \pm 2f_{\text{LO}} - (f_{\text{LO}} - f_{\text{RF}}). \]  \hspace{1cm} (Eq. 3-2)

While the secondary signal of (Eq. 3-2) is at the same frequency as the primary IF signal, phase differences between the signals often results in uneven mixer conversion-loss response resulting in IMD. This disruptive interference can be minimized by maintaining constant impedance matching between an analog filter and the subsequent filter and by absorption of image signals by filters (built into some discrete filters). An important specification here is the return loss of the
filter, which ultimately determines the level of the image signal that is reflected back into the analog mixer [Bowick, 2008].

Of considerable concern for a receiver is the IMD resulting from two-tone intermodulation products generated by the mixing of spurious and harmonic responses from the LO and input RF signals. When two signals of different frequencies \( f_1 \) and \( f_2 \) are mixed, they result in intermodulation products. To best illustrate this, resulting signal voltage can be thought of as the expansion of a Taylor series according to [Bowick, 2008; Whites, 2006]

\[
V = G_v V_i + G_2 V_i^2 + G_3 V_i^3 + G_4 V_i^4 + G_5 V_i^5 + \ldots \quad \text{(Eq. 3-3)}
\]

Since two signals of frequencies \( f_1 \) and \( f_2 \) are mixed, \( V_i \) from (Eq. 3-3) can be broken down as follows [Whites, 2006]:

\[
V_i = V_1 \cos(2\pi \cdot f_1 \cdot t) + V_2 \cos(2\pi \cdot f_2 \cdot t). \quad \text{(Eq. 3-4)}
\]

The desired output is \( G_v V_i \) in (Eq. 3-3), but when both signals in the sum in (Eq. 3-4) are sufficiently high (high \( V_1 \) and \( V_2 \)) dependent on the values of \( G_2 \), \( G_3 \), etc. relative to \( G_v \), intermodulation product frequency spurs can be introduced to the output signal, \( V \). These intermodulation products can be determined from the expansion of the expression for each order of the Taylor series. A summary of the intermodulation product spurs can be seen in the Table 3-1. Also in Table 3-1 are the resulting intermodulation products for a specific example given two signals with \( f_1 = 100 \) kHz and \( f_2 = 101 \) kHz [Bowick, 2008; Whites, 2006].
The example in Table 3-1 reveals that, in the case of odd-order intermodulation products, resulting frequency spurs can be close to the two fundamental frequencies, $f_1$ and $f_2$. If both signals are sufficiently large and the associated magnitude of the intermodulation products is large enough for some of the orders, intermodulation distortion can occur. While intermodulation products generated at frequencies vastly different from the fundamental frequencies can be easily filtered out, odd-order intermodulation products at frequencies close to the fundamentals cannot.

The analog RF-to-IF mixing stage in superheterodyne receiver architecture such as the single-RF-chain superheterodyne SDR receiver of Figure 2-3 can be a large source of intermodulation distortion, which can dramatically degrade overall receiver performance. Therefore, specifications are provided to quantify the intermodulation effects. These specifications are expressed as intercept points. Because analog devices such as mixers do not behave strictly linearly, IMD gets increasingly worse outside the linear operating zone of a device. Essentially, intermodulation products increase relative to the desired output outside of linear operation. The intercept point specifications are summarized in Table 3-2 [Bowick, 2008]:

<table>
<thead>
<tr>
<th>Order</th>
<th>Intermodulation Products</th>
<th>Example: $f_1 = 100$ kHz, $f_2 = 101$ kHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>1st Order</td>
<td>$f_1$</td>
<td>$f_2$</td>
</tr>
<tr>
<td>2nd Order</td>
<td>$f_1 + f_2$</td>
<td>$f_2 - f_1$</td>
</tr>
<tr>
<td>3rd Order</td>
<td>$2f_1 - f_2$</td>
<td>$2f_2 - f_1$</td>
</tr>
<tr>
<td></td>
<td>$2f_1 + f_2$</td>
<td>$2f_2 + f_1$</td>
</tr>
<tr>
<td>4th Order</td>
<td>$2f_1 + 2f_2$</td>
<td>$2f_2 - 2f_1$</td>
</tr>
<tr>
<td>5th Order</td>
<td>$3f_1 - 2f_2$</td>
<td>$3f_2 - 2f_1$</td>
</tr>
<tr>
<td></td>
<td>$3f_1 + 2f_2$</td>
<td>$3f_2 + 2f_1$</td>
</tr>
<tr>
<td>etc.</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Intermodulation and Other Analog Devices

While other analog devices do not necessarily have the IMD concerns directly associated with LO interference and harmonics, they do suffer from IMD outside of their linear operation in much the same way as summarized for mixers in Table 3-2. IMD plays a particular role in the selection of analog RF amplifiers used in a receiver. Similar to mixer behavior, given a large enough RF signal input in terms of power (generally provided in dBm), an amplifier ceases to exhibit the linear behavior it exhibits at lower signal levels. That is, given a large enough signal input, the output signal will not increase proportionally to the specified gain of the amplifier. This means that, if a signal is large enough, it is possible for the intermodulation products to overtake the input RF signal [“Cascaded 1 dB Compression Point (P1dB),” 2010].

The governing specifications for amplifier and other analog component IMD characteristics are the same intermodulation intercept points (generally given in dBm).

Table 3-2: Intermodulation Intercept Points [Bowick, 2008]

<table>
<thead>
<tr>
<th>Intercept Points</th>
<th>Intercept Point Explanation</th>
</tr>
</thead>
<tbody>
<tr>
<td>P1dB: 1-dB Compression Point</td>
<td>Compression is the measurement of the linearity of an analog device. As the RF input signal level increases to an analog mixer, the IF output should directly follow. However, at a certain signal level, the IF output cannot linearly follow the RF input. The point at which this deviation occurs by 1 dB on an RF input vs. IF output curve is referred to as the 1-dB compression point.</td>
</tr>
<tr>
<td>IP2: Second-Order Intercept Point</td>
<td>The point at which the second-order intermodulation products become equal in amplitude to the RF input signal is referred to as the second-order intercept point.</td>
</tr>
<tr>
<td>IP3: Third-Order Intercept Point</td>
<td>The point at which the third-order intermodulation products become equal in amplitude to the RF input signal is referred to as the third-order intercept point. Because this is involves the first odd intermodulation product, it is typically a significant specification and closely related to IMD. Terminology note: IIP3 is the input-referred IP3 and OIP3 is the output-referred IP3. IIP3 is OIP3 divided by small-signal gain.</td>
</tr>
</tbody>
</table>
summarized in Table 3-2. However, the 1-dB compression point is related to a curve other than RF input vs. IF output; for example, the P1dB specification of an analog amplifier refers to the point of 1-dB compression (non-linearity) on an RF input vs. RF amplified output curve [“Cascaded 1 dB Compression Point (P1dB),” 2010].

**Capturing Intermodulation Characteristics and Introduction to MAS**

Intermodulation effects play a critical role in determining the maximum signal level a receiver can detect, the maximum allowable signal (MAS), which is discussed in Section 3.1.4. It is largely because of IMD that there is a limit to how strong an input RF signal can be to a receiver and still be processed effectively. If the RF signal input is high enough to exceed a critical intermodulation intercept point of the overall receiver, particularly overall IP3, then IMD will likely overwhelm the system and make signal detection impractical. Therefore, to aid in the determination of MAS, which is an essential overall receiver specification, it is necessary to get an overall picture of the intermodulation characteristics of the receiver’s entire analog RF front-end and not just its individual analog components [Bowick, 2008; Miranda, 2007].

Since the design of SDR receivers involves the recovery of information in the digital domain, Bit Error Rate (BER) is ultimately one of the best metrics for receiver performance analysis. BER is a frequent metric called upon for radio performance and specification analysis in the TIA (Telecommunications Industry Association) standard TIA-102.CAAB-B Land Mobile Radio Transceiver Recommendations, Project 25 – Digital Radio Technology, C4FM/CQPSK Modulation. The TIA-102.CAAB-B standard includes intermodulation rejection guidelines and test methods. It indicates that a receiver’s ability to reject intermodulation is to be measured by introducing an interfering signal to a reference signal input to the receiver and detecting the BER for further calculations [TIA-102.CAAB-B, 2004]. However, while measuring intermodulation rejection of an SDR receiver according to BER determines a critical receiver specification, it is also useful to understand the theoretical intermodulation characteristics of the RF front-end.
Getting an overall theoretical picture of the intermodulation characteristics of the analog RF front-end of a superheterodyne SDR receiver is useful but not necessarily straightforward. The simplest way is to provide theoretical overall RF-front-end intermodulation intercept points. This can be done by cascading the critical OIP3 specifications for each stage of the RF front-end to obtain an overall OIP3 value. This can be done using linear, mW, values for OIP3 and linear gain (not logarithmic dB) values according to

\[
\text{OIP3} = \frac{1}{\text{OIP3}_{N-1} \cdot G_N} + \frac{1}{\text{OIP3}_N} \quad \text{(mW)},
\]

(Eq. 3-5)

where \( N \) is the index if the current stage, \( N-1 \) is the index of the previous stage, and \( G \) is gain given in linear form of the current stage [“Cascaded 1 dB Compression Point (P1dB),” 2010].

Understanding where linear behavior compresses in a receiver is also useful and, therefore, obtaining an overall P1dB intermodulation intercept point for the RF front-end is also of value. Unfortunately, this determination can be more complex given the need for polynomial analysis of the linearity curves at each stage. However, an overall OP1dB value can be estimated using the same cascade equation for OIP3 found in (Eq. 3-5). This is due to the existence of a rule-of-thumb relationship that exists between P1dB and IP3. This relationship states that the IP3 is generally 10–12 dB higher than the P1dB. In fact, one study seeking to test this rule-of-thumb found a mean difference of 11.7 dB with a standard deviation of 2.9 dB [“Cascaded 1 dB Compression Point (P1dB),” 2010]. Therefore, the overall OP1dB of a multi-stage system can be estimated according to

\[
\text{OP1dB} = \frac{1}{\text{OP1dB}_{N-1} \cdot G_N} + \frac{1}{\text{OP1dB}_N} \quad \text{(mW)}.
\]

(Eq. 3-6)

OP1dB, or P1dB\text{OUTPUT}, is the output P1dB intercept point. It is related to input P1dB, P1dB\text{INPUT}, according to [“Cascaded 1 dB Compression Point (P1dB),” 2010]
\[ P_{1\text{dB}_{\text{OUTPUT}}} = P_{1\text{dB}_{\text{INPUT}}} + (\text{gain} - 1) \text{ (dBm).} \quad \text{(Eq. 3-7)} \]

3.1.4. Receiver Dynamic Range (DR)

The dynamic range (DR) of the receiver is the difference between the maximum allowable signal (MAS) and the minimum detectible signal (MDS). Essentially, dynamic range represents the range of signal powers that the receiver can detect and process effectively. With MAS and MDS expressed in dBm values (as opposed to mW) dynamic range is defined as [Miranda, 2007]

\[ \text{DR} = \text{MAS} - \text{MDS} \text{ (dBm).} \quad \text{(Eq. 3-8)} \]

Caution must be observed in the determination and interpretation of the DR specification because several definitions are often used, and different tests are conducted to determine a value. While the definition of (Eq. 3-8) holds true, the determination of MAS can be highly varied and different relationships may arise. For example, the definition of DR given by (Eq. 3-8) can be re-expressed as the single-tone dynamic range according to [Rhode and Whitaker, 2001]

\[ \text{DR} = 1\text{dBGC} - \text{MDS} \text{ (dBm).} \quad \text{(Eq. 3-9)} \]

In (Eq. 3-9), 1dBGC refers to the 1-dB gain compression point, which is the measured point at which gain compresses by 1-dB up to the first mixer. This value is a measured value found during desensitization measurements, which consists of two signal generators being used to test signal levels through a receiver [Rhode and Whitaker, 2001]. This value can be closely related to the previously discussed P1dB intermodulation intercept point and can be viewed for this definition as the MAS of the receiver, but, again, caution must be taken in interchanging empirical and theoretical values as well as definitions such as those concerning at which point in the RF chain specifications are defined [Rhode and Whitaker, 2001; Miranda, 2007].
Another definition of DR more directly relates intermodulation product intercept points with DR according to the following general relationship [Rhode and Whitaker, 2001]

\[ n \text{DR} = (n-1) \left[ \text{IP}_{n \text{INPUT}} - \text{MDS} \right] \text{ (dBm)}, \quad \text{(Eq. 3-10)} \]

where \( n \) is the order of the intercept point and \( \text{IP} \) is the intermodulation intercept point in dBm.

Therefore, for the commonly used third order intermodulation intercept point analysis of DR it would follow that [Rhode and Whitaker, 2001]

\[ \text{DR} = \frac{2 \left[ \text{IP}^{3 \text{INPUT}} - \text{MDS} \right]}{3} \text{ (dBm)}. \quad \text{(Eq. 3-11)} \]

**Maximum Allowable Signal (MAS)**

As introduced in Section 3.1.3, the maximum allowable signal (MAS) level is the highest input power that a receiver can effectively process. MAS is often tied to intermodulation specifications, but the determination of this relationship is varied. The overall P1dB or 1dB GC may be chosen as unacceptable input signal levels thereby dictating MAS, or IP3 may be used to dictate a MAS relationship [Rhode and Whitaker, 2001; Miranda, 2007]. Furthermore, in an SDR receiver, the ADC may also be the driver of the MAS specification [Brannon, 2008].

MAS is limited to the maximum ADC input voltage and corresponding analog input terminating resistance. Should a signal power level exceed that of the specified ADC input, signal clipping will occur, thereby preventing effective A/D conversion. Each ADC has a specified peak-to-peak voltage input \( (V_{p-p}) \) and terminating resistance \( (R_{IN}) \). Using the peak voltage, \( V_p \), derived from \( V_{p-p} \) and \( R_{IN} \), the maximum signal power for the ADC input (the possible MAS driver) can be determined according to Maxim Integrated Products, 2002

\[ V_{rms} = \frac{V_p}{\sqrt{2}} \quad \text{(V_{rms}),} \quad \text{(Eq. 3-12)} \]
Signal Power = \frac{V_{\text{rms}}^2}{R_{\text{IN}}} \quad \text{(W)}, \quad \text{(Eq. 3-13)}

Signal Power = 10 \times \log \left( \frac{V_{\text{rms}}^2}{R_{\text{IN}}} \times \frac{1000 mW}{W} \right) \quad \text{(dBm)}, \quad \text{(Eq. 3-14)}

In the case of a traditional analog superheterodyne receiver, MAS would be driven primarily by IMD and intermodulation product intercept points; however, in a superheterodyne SDR receiver, the ADC maximum input before clipping also drives MAS determination [Brannon, 2008; Maxim Integrated Products, 2002; Miranda, 2007].

The determination of the MAS component of DR is varied and must be clearly defined when both the MAS and DR specifications are defined.

**Minimum Detectible Signal (MDS)**

A critical specification in radio design is receiver sensitivity, which dictates the lowest level effectively detectable by a radio. While the term ‘sensitivity’ can apply to a number of specifications, arguably the most critical related specification that, with MDS, determines receiver DR is the minimum detectable signal (MDS) [Brannon, 2008; Koski, 2010; TIA-102.CAAB-B, 2004].

MDS can be determined from the total noise figure \((NF_{\text{total}})\) of the system (to be discussed in Section 3.1.6), the bandwidth \((BW)\) of the signal, the minimum signal-to-noise ratio required \((\text{SNR}_{\text{min}})\) at the ADC input, receiver noise temperature \((T)\), and the Boltzmann constant \((k_B)\). The calculation for MDS is [Brannon, 2008; Miranda, 2007]

\[
MDS_{\text{linear}} = k_B \cdot T \cdot BW \cdot NF_{\text{total}}(linear) \cdot \text{SNR}_{\text{min}}(linear) \quad \text{(W)} \quad \text{and} \quad \text{(Eq. 3-15)}
\]

\[
MDS = 10 \log \left( \frac{k_B \cdot T \cdot BW}{0.001} \right) - NF_{\text{total}} - \text{SNR}_{\text{min}} \quad \text{(dBm)}. \quad \text{(Eq. 3-16)}
\]
While the signal bandwidth (BW) is a receiver parameter likely to be set as a system requirement, the noise figure (NF_{total}) and minimum required SNR (SNR_{min}) are specifications dependent on specific design selection. The total noise figure is simply a cascaded total of the noise figures of all RF front-end analog components that is explained in Section 3.1.6 [Brannon, 2008]. The minimum SNR is a more complex specification. There are several methods to determine SNR_{min} based on individual ADC component specifications such as ADC SNR and SFDR [Seo et al., 2003]. Because the methods for determining this value are complex and varied, the model described in Chapter 4 determines this through a user-defined assumption. Therefore, for the purposes of this work, the determination of this value is not considered in depth.

3.1.5. RF Front-End Gain

The RF front-end gain is another important receiver specification. It is critical for determining the signal level at the end of the RF front-end stage at the input of the ADC. As long as the signal level remains within the bounds of linear analog device behavior, the gain of the RF front-end is a simple summation of the gain (in logarithmic form, dB) through all analog components on the front-end. For components with specified insertion loss, such as filters, loss is simply treated as negative gain the summation. An example of an RF front-end gain calculation using the single-RF-chain superheterodyne SDR receiver architecture from Figure 2-3 is given as

\[
G_{total} = G_{antenna} - L_{BPF(RF)} + G_{LNA} + G_{mixer} - L_{BPF(IF)} + G_{Amp} \quad (\text{dB}), \quad \text{(Eq. 3-17)}
\]

where \( G \) is logarithmic gain in dB and \( L \) is logarithmic insertion loss in dB [Rhode and Whitaker, 2001].
3.1.6. RF Front-End Noise Figure (NF)

An important consideration in the performance of a receiver is the noise introduced from components in the receiver chain that add to the receiver noise floor. The noise performance of the receiver is a major driver of the MDS specification discussed in Section 3.1.4. Noise characteristics and considerations are specified in a number of ways, such as power spectral density (PSD) and overall receiver signal in noise and distortion (SINAD), but one of the most critical and basic specifications is the noise figure (NF) of the RF front-end [Bowick, 2008].

The analog components of the RF front-end of a receiver each have a noise figure associated with them. It should be noted that for passive analog components such as filters, noise figure is simply the insertion loss. Noise figure is the logarithmic (dB) form of noise factor (\(F\)), which is the ratio of the SNR at the output of a component compared to the SNR at the input of the same component. Therefore, \(NF\) and \(F\) are defined as [Bowick, 2008]

\[
F = \frac{\text{SNR}_{\text{out}}}{\text{SNR}_{\text{in}}}, \text{ and} \tag{Eq. 3-18}
\]

\[
NF = 10 \log \left( \frac{\text{SNR}_{\text{out}}}{\text{SNR}_{\text{in}}} \right) \text{ (dB).} \tag{Eq. 3-19}
\]

The total noise figure for the RF front-end of a receiver (\(NF_{\text{total}}\)) is the logarithmic expression of the ratio between the output SNR of the entire RF front-end and the input SNR to the entire RF front-end. This total can be arrived at through a cascaded summation of expressions relating component NF and gain (\(G\)) for each component, i.e.,

\[
F = 10^{\frac{NF}{10}}, \tag{Eq. 3-20}
\]

\[
F_{\text{total}} = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1G_2} + \frac{F_n - 1}{G_1G_2\ldots G_{n-1}}, \text{ and} \tag{Eq. 3-21}
\]

\[
NF_{\text{total}} = 10 \log (F_{\text{total}}) \text{ (dB),} \tag{Eq. 3-22}
\]
where \( F_1 \) is the noise factor (linear) of the stage 1 component, \( G_1 \) is the linear gain of the stage 1 component, and \( n \) is the index of the final stage [Bowick, 2008].

The total noise figure of the RF front-end provides a good summary of the noise contribution of the analog components and further contributes to the determination of MDS. However, as addressed in Section 3.1.3 within the introduction to MDS and its relationship to intermodulation products, bit error rate (BER) is a common metric used to analyze overall SDR receiver performance, and BER is often used to analyze final noise performance. Noise characteristics and MDS performance of an SDR receiver may ultimately be specified by BER tests, but as with intermodulation intercept points and MAS, noise figure provides an excellent theoretical benchmark for MDS [Bowick, 2008; TIA-102.CAAB-B, 2004].

### 3.1.7. Other Important Specifications

Sections 3.1.1–3.1.6 provide some of the most critical receiver specifications and discuss those that are most directly used in the trade space visualization model to be discussed in Chapter 4. However, they do not represent all critical receiver specifications. This section serves to briefly introduce or simply mention other receiver specifications of importance.

Of particular importance are two specifications not listed in Sections 3.1.1–3.1.6: channel selectivity and spurious suppression. Adjacent channel selectivity (ACS) is the ratio of the receive filter attenuation on an assigned channel to that on the adjacent channel. Spurious suppression is a measurement of the suppression of LO leakage that causes IMD [Bowick, 2008; Koski, 2010].

Two highly relevant radio design standards referenced in the development of this work include the previously mentioned TIA-102.CAAB-B standard for public safety land mobile radio transceivers and the MIL-STD-188-141B (United States Military Standard 188-141B) for the
interoperability and performance of medium and high frequency military radios. These standards provide specifications that define best-practice, interoperability, and acceptance criteria. Therefore, these can be referenced for further receiver specifications or characteristics and associated considerations of importance. A summary of all the listed receiver specifications or characteristics, by title only, in these two standards can be found in Table 3-3. Some of the listed specifications overlap with or are the specifications described in Sections 3.1.1–3.1.6 [MIL-STD-188-141B, 1999; TIA-102.CAAB-B, 2004].


<table>
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3.2. Some SDR Receiver Design Considerations

Recent SDR technology developments have been largely fueled by major advances in digital signal processing (DSP) and semiconductor technologies. Given this enabling digital development, as SDR systems are being realized and implemented, they are also pushing the capabilities and limits of other technologies such as traditional analog receiver components. As a result, there are a large number of design considerations including limitations and tradeoffs associated with the development and design of SDR systems directly related to the balancing of analog and digital components and functions [Brannon, 2008]. The existence of these limitations, tradeoffs, and other considerations are a large motivator for the trade space visualization of SDR receiver design. Chapters 4 and 5 demonstrate how effective trade space visualization can highlight considerations that influence design decisions. However, Section Error! Reference source not found. and Section 3.2.2 first addresses some major known considerations as examples. Section Error! Reference source not found. discusses some of the known design considerations associated with A/D conversion technology, which is an enabling component of SDR design that represents a current bottleneck in the evolution and growth of SDR technology. Section 3.2.2 explores some other miscellaneous design considerations associated with SDR receivers.

3.2.1. Analog-to-Digital Conversion Considerations

Advances in DSP and FPGA technology have made a robust digital backend available to SDR designers. This digital backend is capable of handling many of the radio functions required of truly flexible SDR systems. However, this powerful digital backend relies on the input of digital signals that reliably represent the analog signals initially received from the air at an
antenna. Without the ability to reliably convert sensitive analog signals into digital form, the powerful digital backend available to SDR receivers is meaningless [Benson and Lall, 2004; Papantonopoulos, 2007].

Many of the most critical design limitations and tradeoffs associated with SDR receiver design revolve around the goal to convert received analog signals into digital form as soon as possible. With a powerful digital backend available, the motivation for this goal is simple: the earlier the conversion of analog signals to digital signals takes place along the receive path, the more receiver functions can be implemented in the digital domain as opposed to the analog; and the more receiver functions that are implemented digitally, the increasingly reconfigurable and flexible the SDR receiver becomes [Brannon, 2008; Buracchini, 2000]. Unfortunately, in current practice, analog signals cannot and generally are not converted directly from RF signal reception at an antenna to the digital domain, and some radio functions in the receiver front-end therefore will remain in the analog domain. This is largely due to A/D converter (ADC) technology limitations, but can also be attributed to practical design parameters such as tolerable cost and risk considerations often associated with high-end ADC selection. Therefore, one of the most critical design questions facing the modern SDR receiver designer is: how early can received signals be converted to the digital domain, and what receiver functions must remain implemented in the analog domain based on technology and design parameter limitations?

Two critical receiver specifications highlighted in Section 3.1 that have a close relationship with A/D conversion in the SDR design space include receiver sensitivity and receiver bandwidth. ADCs are critical to these overall specifications because the sensitivity of the actual ADC can drive overall receiver sensitivity and can demand increased analog front-end circuitry for amplification and, because the sampling rate of the ADC, can dictate the maximum usable bandwidth of an SDR receiver. Therefore, ADCs are the largest current bottleneck in SDR receivers since ADC technology is not yet advanced enough to directly sample RF signals and
feed them to the advanced digital backend DSP technology that, in fact, is prepared to handle directly sampled signals. Three ADC specifications often place limitations on overall SDR receiver design: ADC signal-to-noise ratio (SNR), ADC spurious-free dynamic range (SFDR), and ADC sampling rate ($f_s$). SNR and SFDR drive the sensitivity of an ADC and determine its ability to receive small signals, and the sampling rate drives the ADC’s ability to effectively sample a signal. These three parameters often dictate what analog RF hardware must precede the ADC and play a critical role in answering the question posed to the modern SDR receiver designer in the latter paragraph [Papantonopoulos, 2007].

**ADC Sensitivity**

As seen in (Eq. 3-15) and (Eq. 3-16), the sensitivity of the ADC drives overall sensitivity since the minimum signal SNR required at the input of the ADC ($\text{SDR}_{\text{min}}$) is a major driver in the calculation of the receiver minimum detectable signal (MDS). The individual SNR and SFDR specifications of the ADC are major determinates of this minimum input SNR [Papantonopoulos, 2007; Seo et al., 2003].

When the input power of a received signal is especially low, the SNR often becomes the limiting factor in overall receiver sensitivity. While the precise relationship between ADC SNR and its input sensitivity, and hence overall receiver MDS, is complex (Seo et al. [2003] can be referenced for example considerations), generally speaking an increased ADC SNR translates to improved ADC sensitivity [Papantonopoulos, 2007; Seo et al., 2003].

Greater ADC SNR results from greater ADC bit resolution. Until relatively recent advancements in ADC technology, greater ADC bit resolution meant decreased ADC sampling rate. This means that lower-end and older ADCs maintain this tradeoff: higher ADC SNR and increased radio sensitivity translates to lower ADC sampling rate and smaller usable bandwidths. Fortunately, this tradeoff is evaporating with the development of new, high-speed, high-resolution
ADCs. Nevertheless, designers still must remain aware of this tradeoff when not using cutting-edge ADCs [Papantonopoulos, 2007].

ADC SFDR also plays a critical role in determining the sensitivity of an ADC. The SFDR of the ADC is a critical specification that is a measurement of the ratio of the RMS signal amplitude to the RMS value of the peak spurious spectral content. SFDR determines how well signals are measured through distortion at differing input power levels and is comparable in some ways to intermodulation intercept points for mixers and amplifiers [Kester and Bryant, 2007]. As explained in Section 2.1.2, SFDR is not always linear in nature when compared to analog frequency input to the ADC. As input frequency increases, ADC SFDR has a tendency to decrease with other conditions and parameters held constant. This non-linearity as well as the raw SFDR specification of an ADC itself, like the ADC SNR, can drive the specific needs of the analog circuitry required to precede A/D conversion [Papantonopoulos, 2007].

Another consideration that plays into the sensitivity of the ADC is also the signal power level required at the input. Not only do ADCs require a certain minimum SNR at their input, they require an input power level within the range of the ADC. While the ADC itself can add gain to the signal through processing gain (PG) or conversion gain, this can require over-specifying the required bit resolution and may not add all the required gain necessary to prepare a raw signal of low received signal strength (RSS) for conversion. Again, input power requirements may drive a need for analog circuitry before the ADC [Brannon, 2008; Papantonopoulos, 2007].

Together, with other ADC specifications the ADC specifications mentioned herein help determine the sensitivity of the ADC, which ultimately dictates the SNR and power level a signal must achieve before being input to the ADC. For most SDR receiver applications, modern ADCs require analog filtering, amplification, and signal downconversion processes to occur prior to their input to achieve the signal parameters required for successful A/D conversion. Another contributor to this need beyond the simple technical limitations of ADCs is the fact that specific
signal parameters (such as minimum input power level and minimum input SNR) must likely be maintained for wide frequency bands. Wideband reception is an enabler of receiver flexibility, but brings higher risks of receiving undesired noise and signals. [Brannon, 2008; Papantonopoulos, 2007; Seo et al., 2003]

The work of Brannon [Brannon, 2008] can be referenced for further SNR and SFDR considerations for receiver sensitivity and performance.

**ADC and Available Bandwidth**

As highlighted in Section 2.1.2, the sampling rate of the ADC has a significant influence on the overall bandwidth the receiver is capable of processing. As previously discussed, the maximum bandwidth an ADC can convert to the digital domain without aliasing is, at most, half of its sampling rate. Furthermore, if sub-sampling techniques are not employed or are not possible for a particular ADC, the ADC also has the potential to determine the maximum signal frequency a receiver is capable of processing without an existing analog IF stage due to the very same relationship. Therefore, the sampling rate of the ADC limits the available bandwidth of the receiver and has the potential to require an analog IF. [Papantonopoulos, 2007]

### 3.2.2. Miscellaneous Considerations

Two further considerations are presented within this section. Additional SDR design considerations can be referenced in works such as that of Brannon [Brannon, 2008].

**IF Selection Considerations**

Largely due to ADC limitations, at least one analog IF stage is often required in SDR receiver architecture. Many factors related as well as unrelated to the ADC contribute to the selection of the intermediate frequency. The ultimate goal is to leverage a single IF stage to limit analog hardware with as high an intermediate frequency as possible to facilitate as high a
bandwidth as possible. However, there are a number of factors that can play into decreasing the IF. For example, as already discussed, both ADC SNR and ADC SFDR are not always linear given certain input frequencies. As input frequencies to an ADC increase, both specifications have the potential to decrease except to a lesser extent for some of the more modern, cutting-edge ADCs. If this degradation is not tolerable for sensitivity reasons, then too large an IF may not be possible. In fact, SNR and SFDR parameters are often given in ADC datasheets at specified IF levels. As another example, aliasing harmonics within an ADC are also a consideration when selecting the IF. The IF must be precisely chosen such that potential aliased harmonics resulting from wideband A/D conversion fall away from the fundamental, desired input. [Altera Corporation, 2007; Brannon, 2008; Papantonopoulos, 2007]

**Gain and Intermodulation Distortion Considerations**

In traditional HR superheterodyne receiver architecture (like that of Figure 2-1), conversion gain is distributed throughout the entire receive chain and the gain at various stages is chosen to balance noise figure (NF) with intermodulation distortion (IMD): gain must be kept high enough to maintain a low NF but low enough to avoid overloading the receiver with IMD. Furthermore, gain is primarily reserved for after-channel filtering to further avoid excessive IMD. However, in SDR superheterodyne receiver architecture (like that of Figure 2-3), this balance is no longer the same. Because many analog stages are removed from the architecture and A/D conversion happens before the BB stage of the radio, conversion gain must occur earlier in the receive path and may be done at high bandwidths in the presence of many spurious signals. Therefore, IMD characteristics of gain elements are of more importance in SDR receiver design [Brannon, 2008].
3.3. Non-Technical Design Considerations—Risks, Uncertainties, and Human-Factors

Strictly technical considerations based on component-level and overall receiver performance specifications as well as their associated tradeoffs and limitations are not the only factors in SDR design decision making. Nontechnical considerations may also factor into the design process. The detailed analysis of these considerations goes beyond the scope of this work; however, an introduction to these considerations is made within this section to provide some limited background for the “Manufacturer Preference” and “Component Preference” considerations built into the trade-space analysis model developed and elaborated upon in Chapter 4. There are often risk, uncertainty, and human-factor considerations made in the design process [Koski, 2010].

One particular example of a consideration an SDR receiver designer must address when faced with design decisions is the manufacturability of the design. Factoring into this manufacturability consideration are several assessments made by the designer. One of the major assessments made for this consideration is an assessment of the sourcing risk associated with the components in a given design option. The sourcing risk of a component is tied to several factors such as where a particular component is in its lifecycle (i.e., does the component exist only as samples, is it in full-scale production, or is it nearing the end of its lifecycle?); the size and stability of the manufacturer producing the component (i.e., is the manufacturer a small supplier with small production runs or is it a large producer, does the manufacturer have a stable business or an instable one?); the track record of the manufacturer producing the component (i.e., does the manufacturer have a clean or blemished record of conformance issues, delivery issues, etc.?); and how replaceable the component is (i.e., if the exact component can no longer be sourced, can a replacement be easily found and implemented?). The designer considers the latter factors along with others to gain an assessment of the sourcing risk associated with selecting components. By
assessing the sourcing risk and combining it with other considerations, the designer can evaluate the manufacturability of a particular design [Koski, 2010].

The manufacturability consideration given in the previous paragraph provides a good example for what other considerations are like but only just begins to scratch the surface of non-technical, non-specification related considerations that factor into the design decision-making process. The sub-sections on “Manufacturer Preference” and “Component Preference” in Section 4.2.2 elaborate further on some of the non-technical considerations used for this particular work.

3.4. Chapter Summary

There are many specifications that describe SDR receivers. In order to properly model an SDR receiver and its output specifications that result from design inputs and criteria, at least the most critical of these specifications must be understood. The primary specifications considered in detail by this work and used for modeling SDR receiver design include: (1) size, weight, and power (SWaP); (2) frequency and bandwidth; (3) intermodulation distortion and intermodulation intercept points; (4) receiver dynamic range and associated specifications such as maximum allowable signal and minimum detectable signal; (5) RF front-end gain; and (6) RF front-end noise figure.

SDR receiver design is driven by many design considerations that include both technical and non-technical considerations. This work examines some of these considerations. Particularly examined are some design considerations concerning ADC selection and technology. Other considerations examined are technical ones such as the selection of IF frequency and various gain considerations as well as non-technical ones such as risks, uncertainties, and human-factors.
Chapter 4

Trade Space Visualization of SDR Receiver System Design

This chapter provides the details of this work’s major contribution: the development of a Microsoft Excel–based model of single-RF-chain superheterodyne SDR receiver architecture and the linking of the model to the ARL Trade Space Visualizer (ATSV) for trade space exploration studies. Section 4.1 introduces the overall approach taken for trade space visualization of single-RF-chain superheterodyne SDR receiver design. Section 4.2 describes the development and results of hardware component databases for use in a model. Section 4.3 describes the developed Microsoft Excel–based model used to establish feasible receiver designs and to determine receiver characteristics based on input sampled components and user-defined receiver design parameters. Finally, Section 4.4 explains the linking of the model to ATSV and the considerations associated with establishing trade space visualization of the model. This chapter describes the development component of the contribution of this work while Chapter 5 provides some example results from the use of the model with ATSV.

4.1. SDR Trade Space Visualization Approach

The standard approach to trade space exploration provided in Section 2.3.1 involve a three stage process: the development of a model, the running of experiments, and the exploration of the trade space based on experiment results. ATSV and this work generally adopt this method. Therefore, in the development of a trade space visualization method using ATSV for single-RF-chain superheterodyne SDR receiver design, three high-level stages were used: a single-RF-chain
superheterodyne SDR receiver model was developed; experiments were run by sampling the model with the ATSV Exploration Engine described in Section 2.3.2; and ATSV was used to explore and refine experiment results using its comprehensive suite of visualization tools. The contribution made by this work is the use and not the development of ATSV and, hence, the focus of this chapter is the work’s primary contribution: the development of the actual model in the first stage of standard trade space exploration as well as the linking of the model to ATSV for sufficient experimentation.

The selected approach to simulating SDR receiver design in a manner suitable for useful trade space visualization was the implementation of a basic architecture model that simply places receiver components with their corresponding specifications into the model according to the prescribed single-RF-chain superheterodyne SDR receiver architecture described in Chapter 2. Component specifications, read in from databases, are checked against designer-specified receiver system input specifications and assumptions as well as against other components for basic system compatibility in order to select feasible designs for analysis. Component specifications and designer inputs are also used to calculate output SDR receiver specifications to be logged and visualized. This model is linked to the ATSV Exploration Engine for sampling and detailed visualization and exploration of the SDR receiver design space. The component databases for model reference as well as the actual SDR receiver model are implemented in Microsoft Excel, which was selected for its proof-of-concept simplicity and its seamless link with the ASTV tool via .ECF configuration files. The selected approach for the model is summarized in Figure 4-1, which can be viewed as a detailed, lower level look at the “Simulation Model” block in the block diagram outlining the trade space exploration process in Figure 2-6.
As represented in Figure 4-1, the SDR Receiver Model (which is abbreviated to SDR-RM) is comprised of three primary elements: the SDR Receiver Component Databases (herein abbreviated to SR-CDs), the SDR Receiver Trade Space Analysis Model (herein abbreviated to SR-TSAM), and the link to ATSV (the input and output link are handled by the same component). SR-CDs are implemented in Microsoft Excel with each component having its own XLS file and its own equivalent .CSV file. The SR-TSAM is also implemented in Microsoft Excel with a single XLS file. The link to ATSV, which inputs sample component index values and outputs receiver output specifications, is handled by a special configuration file in .ECF form defined by the ATSV Exploration Engine. Within the SDR-RM, the basic flow is as follows: the ATSV exploration engine inputs index sample values to the SDR-RM via the configuration file-based link; these samples are inserted into the SR-TSAM as component indices used to reference SR-CDs; the indices in the SR-TSAM are used to index the SR-CDs, which return specification values and details of the indexed component for each component in the single-RF-chain.
superheterodyne SDR receiver architecture; the SR-TSAM calculates overall receiver specifications and characteristics (including basic compatibility/feasibility); then calculated output values are output to ATSV from the SDR-RM via the .ECF link; and ATSV then displays the data in visual form and iterates according to user interaction. The three components of the SDR-RM (SR-CD, SR-TSAM, and ATSV link) are described in detail in Sections 4.2–4.4.

4.2. SDR Receiver Component Database (SR-CD) Development & Implementation

Following the single-RF-chain superheterodyne SDR receiver architecture of Figure 2-3, databases for each respective component had to be developed for access by the SR-TSAM. If every component were modeled in the SR-TSAM, then the SDR Receiver Component Databases (SR-CDs) that would be required would include:

- Antenna SR-CD
- Band-Pass Filter (BPF) SR-CD
- Low-Nosie Amplifier (LNA) SR-CD
- RF Mixer SR-CD
- Local Oscillator (LO) SR-CD
- RF Amplifier SR-CD
- Components associated with Automatic Gain Control (AGC) SR-CD
- Analog-to-Digital Converter (ADC) SR-CD
- Field-Programmable Gate Array (FPGA) SR-CD for digital receiver chip
- Digital Signal Processor (DSP) SR-CD

However, the actual implemented SR-TSAM of this work, which is intended to be a first step and proof-of-concept model to be expanded upon, does not model all of these components, thereby diminishing the required number of SR-CDs. Model assumptions are explained in Section 4.3,
but given the assumptions and simplifications of the SR-TSAM, the components actually modeled and, hence, those with database needs include BPF, LNA, RF mixer, RF amplifier, ADC, and FPGA.

SR-CDs were generated using COTS components and available corresponding specifications. COTS components were logged into Microsoft Excel XLS and equivalent .CSV files. The remainder of this section explains the databasing methods explored and those implemented as well as highlights specific database attributes and assumptions.

4.2.1. SR-CD Development – Sources and Methodology

The SR-CD development process is presented herein. The findings of the development process are presented in addition to the investigated and leveraged development methods.

Data Sources for SR-CD Development

The Internet was used as the source for COTS components and their respective specifications compiled into SR-CDs. The objective of the databasing process was to find an efficient method to collect COTS component data from publicly available sources on the Internet in a manner accessible and achievable to a wide range of designers from amateur to professional. Ultimately, two types of Internet sources were used for the collection of data: manufacturer-provided component data and component distributor-provided component data.

Manufacturer-Provided Component Data

The initial approach used to collect data for the SR-CDs was to make use of manufacturer-available component data on manufacturer websites. It was found that the manufacturers of receiver components generally have product listings that take one or several of three typical forms: online tables (such as HTML tables) that are often parametrically searchable; downloadable catalog listings often in PDF format; and/or downloadable databases often in XLS
format. The latter format is ideal given that components are already presented in a form close to that which is required for access by the SR-TSAM. Unfortunately, however, downloadable databases were not always available, and, often, manufacturers presented component data in online tables or catalog listings. The methodology for collecting this data is explored later within this section.

Collecting component data directly from manufacturers had clear benefits as well as clear drawbacks. The greatest benefit was the ability to collect data already in database form when made available by manufacturers. Among the benefits was also the focused, non-repetitive nature of the data, which is best explained by highlighting a drawback to be reiterated later regarding the use of online distributor catalogs as a data source: often, distributor catalogs contain a great deal of component repetition since they list all the different slight variations of the same component, which are difficult to filter out. Manufacturer sources also sometimes include customizable tables enabling online visitors to select from a large number of available specifications to sort by.

Using manufacturer sources also had some significant drawbacks. One significant drawback was the infrequent but possible non-availability of database or online tabular component/specification listings and instead the availability of downloadable catalogs in inconvenient formats such as PDF. Many other drawbacks had to do with the inconsistencies found between one manufacturer’s listings and another’s. For example, some manufacturer’s might highlight a component’s typical power consumption from the data sheet in a table summarizing component specifications while another’s might highlight the component’s maximum power consumption. Furthermore, some manufacturers might choose to present different specifications in a table than those presented by others. Often, these inconsistencies result from manufacturers choosing to highlight the features that present their products in the best possible light. Because datasheets were not manually accessed for every component, these inconsistencies presented immense challenges in producing valuable SR-CDs suitable for model
use. A summary of the major pros and cons associated with leveraging manufacturing data sources is presented in Table 4-1.

**Table 4-1: Pros and Cons of the Use of Manufacturer Sources for SR-CD Development**

<table>
<thead>
<tr>
<th>Pros</th>
<th>Cons</th>
</tr>
</thead>
<tbody>
<tr>
<td>▪ Possible access to existing databases</td>
<td>▪ Possible non-availability of convenient data formats</td>
</tr>
<tr>
<td>▪ Focused, non-repetitive data</td>
<td>▪ Inconsistencies in specifications</td>
</tr>
<tr>
<td>▪ Possible access to customizable tables with a lot of specification categories</td>
<td>▪ Inconsistencies in featured categories</td>
</tr>
</tbody>
</table>

**Distributor-Provided Component Data**

A later approach taken in the databasing of receiver components and their specifications and the one used for the majority of the final SR-CDs was to use distributor-provided component data from online catalogs. In the case of the SR-CDs developed for SR-TSAM in this work, the online catalog of electronic component distributor the Digi-Key Corporation® was used. While the Digi-Key Corporation’s catalog was used, other similar online distributor catalogs were also examined such as those by Mouser Electronics and IC Master: both offer fewer parametric search options and present fewer specifications in easily-accessible tabular form than Digi-Key. Other online catalogs could be leveraged in the future, but Digi-Key’s catalog offered the best source for a first version of the SR-CDs.

All available components could be easily called up on the Digi-Key online catalog by simply leveraging the websites search features, and component searches could be parametrically refined to limit the display of component results if desired. As with the use of the manufacturer-provided data sources, leveraging the Digi-Key online catalog as a component source offered benefits as well as drawbacks.

The benefits of leveraging an online catalog were clear including: consistency of specifications, readily available critical specifications, strong parametric search capabilities, and
the “one-stop-shop” nature of such the source. However, there were drawbacks as well including
the previously mentioned repetition of components, the lack of some non-participating
manufacturers, and the lack of some specification categories of interest. These benefits and
drawbacks are best viewed in a table of pros and cons displayed in Table 4-2.

**Table 4-2: Pros and Cons of the Use of Distributor Sources for SR-CD Development**

<table>
<thead>
<tr>
<th>Pros</th>
<th>Cons</th>
</tr>
</thead>
<tbody>
<tr>
<td>Consistency of specifications</td>
<td>Vulnerable to repetitious data: numerous re-listings of the same component with only slight variations</td>
</tr>
<tr>
<td>Readily available critical specifications for all manufacturers</td>
<td>Does not necessarily include all manufacturers</td>
</tr>
<tr>
<td>Strong parametric search capabilities</td>
<td>Does not always include all specifications of interest</td>
</tr>
<tr>
<td>“One-stop-shop” nature</td>
<td></td>
</tr>
</tbody>
</table>

**Methodology for the SR-CD Development**

In developing a method for extracting information from component data sources for SR-
CD databasing, an important objective was to use a minimalistic approach. There are two
different directions that the further development of the SDR-RM for visualization may go, and
both drive the objective for a minimalistic approach to component databasing in the current SDR-
RM version. In one case, future evolutions of the proof-of-concept SDR-RM presented within
this work may eventually be aggressively refined for use in professional industrial settings or in
research-intensive academic settings with a focus not on the development of the model but on
using the model for actual receiver design. Such a circumstance would likely require a major
overhaul of the database process to implement a customized experience that better captures all
required specifications of interest to a particular group with a high level or reliability as well as to
better capture practical, end-use-specific factors such as business-to-business sourcing
arrangements. In a second case, future evolutions of the proof-of-concept SDR-RM presented in
this work, especially those versions in the developmental interim between its current state and more aggressive professional use, may remain in a research and development setting focused on the advancement of the actual model itself or on the use of the model for receiver design in a way that tolerates and may even require simple SR-CDs. In this second case, SR-CDs should be simple to develop and update from readily available sources without significant complexity or customization.

As previously discussed, existing XLS component databases were often not available, and, instead, component manufacturers and distributors made component product information available on the Internet in HTML-based tables that were often parametrically searchable. Because these common HTML tables were easy to find and navigate, a clear minimum-complexity approach to SR-CD development was to copy these HTML tables in XLS Excel-based databases. Initially, an attempt was made to do this very simply, by using standard Microsoft Windows® copy-and-paste functionality. Generally, the result of copying an HTML table in one of any number of commercially available Internet browsers such as Microsoft Internet Explorer®, Mozilla Firefox, and Google Chrome™ is the storage in the Windows clipboard of a grouping of text with some type of delimiter between row and column entries. When this delimiter is well defined, simple paste functionality in Excel generally does a good job separating rows from columns with a high level of overall accuracy. However, this method has several major drawbacks including but not limited to: the inconsistency of copy performance and delimiter use by different browsers and browser versions, the occasional need to edit delimiters in a text editor prior to an import to Excel, the existence of invisible formatting characters such as the common ALT+0160 invisible space character, highly inconsistent formatting frequently requiring cumbersome manual reformatting, the negative impact of pictures within tables on overall format integrity, and the need to precisely highlight each table prior to copying and pasting. While Visual Basic-based macros written by the author were used for the removal of
invisible characters and to aid the re-formatting process, the high level of customization needed for each specific copied table in addition to the other drawbacks rendered the simple Windows clipboard copy and paste technique impractical for implementation. Ultimately a tool was required to aid the copy process.

A publicly available freeware tool called TableTools was selected and used to facilitate the copying of HTML tables into Excel files. The tool is provided as an add-on extension to the commonly used, open-source Internet browser, Mozilla Firefox. TableTools offers users of Firefox a feature set that increases their ability to interact with HTML tables. The feature of interest to the development of the SR-CDs is the ability to copy HTML tables one of several ways: as tab-delimited text, as justified tab-delimited, or as HTML. When installed to the Firefox browser, TableTools allows users to right-click anywhere within an HTML table and select a copy option, which places the table on the clipboard in a consistent fashion. When using the “Copy As Tab-Delimited Text” feature, users are able to copy a table in a form with consistent tabs. The tab-delimited version of the table can be simply pasted from the clipboard directly into Excel. The pasted table will exclude images, exclude invisible characters in many cases, exclude special formatting, and will consist only of unformatted text in a simple table exactly as it should be with the rows and columns properly aligned and not merged. The TableTools copy menu can be seen used on a Digi-Key FPGA listing in Figure 4-2.
TableTools was used to capture data from the Digi-Key online catalog as well as from manufacturer online table-based databases where existing XLS databases were not available for download. Collecting data from the Digi-Key online catalog simply consisted of searching for a component, viewing all appropriate component hits, and then copying each table on each page of listings using TableTools to then be pasted into Excel. Most SR-CDs were constructed from the Digi-Key online catalog, but for reasons to be discussed, several components were databased using manufacturer sources. The following section next highlights the sources for and highlight some considerations regarding each SR-CD.

4.2.2. The SR-CDs for SR-TSAM and ATSV

As discussed in Section 4.2.1, SR-CDs were developed either from manufacturer sources or from the Digi-Key Corporation’s online catalog. This section briefly highlights the sources for each SR-CD as well as address major adjustments made to and considerations regarding the data.
**Bandpass Filter (BPF) SR-CD**

The BPF SR-CD is actually indexed and referenced twice by the SR-TSAM: once for the BPF in the RF stage and once for the BPF in the IF stage. The component specifications and characteristics captured for the BPFs in the final SR-CD include: manufacturer, manufacturer part number, series, description, center frequency, bandwidth, filter type, ripple, insertion loss, package/case, mounting type, and unit price. Characteristics manually added to the data include: component number (the index used in the SR-TSAM to call return specifications), component preference (to be explained in a sub-section to follow SR-CD explanations), and manufacturer preference (to be explained with component preference).

Two sources were used to compile the BPF SR-CD: the Digi-Key Corporation (distributor) online catalog and the Mini-Circuits (manufacturer) online catalog. While the Digi-Key Corporation catalog tends to be preferable for the development of most SR-CDs, the catalog did not contain information from several critical RF filter manufacturers including Mini-Circuits and Hittite. Furthermore, the Digi-Key catalog did not include BPFs for a wide enough range of center frequencies for early proof-of-concept SR-TSAM use and testing. Therefore, given its straightforward HTML table-based catalog, the Mini-Circuits website was used to collect information on BPFs by Mini-Circuits.

A drawback to using multiple sources (as highlighted in the previous section) is the inconsistency of specification listings. Inconsistencies can range to the listing or non-listing of specific specifications/characteristics in a summary table to presenting the same specifications/characteristics in different way. Unfortunately, the Mini-Circuits summary table did not include the following categories: series, description, ripple, and insertion loss. Furthermore, pricing was hidden on the table and each component had to be individually accessed for price listings at different quantities. The series and description categories were simply filled with NaN entries and ignored. Ripple and insertion loss categories were also generally filled with
NaN entries. However, as seen in the description on the SR-TSAM, the insertion loss for a BPF is used in calculations. Therefore, the datasheets of several filters were manually accessed to identify specific insertion loss values for filters to be used in example tests of the SR-TSAM. Because price is also a critical value used in the SR-TSAM, some manual work was put into accessing the prices of filters. A typical value was found for filters in the same general product family and applied over the entire family. Precise pricing must be checked by a designer, but the supplied estimates are sufficient for modeling and trend visualization. Specifications provided in the Mini-Circuits online catalog but not in the Digi-Key online catalog were simply removed.

As was the case for all SR-CDs some amount of simple column reformatting was required. For example, the “Frequency” category of the Digi-Key Corporation listing did not simply include numbers within the column, but instead each entry specified the value followed by the units of the value and text designating it as center frequency. For example, as seen in Figure 4-3, an entry would read “2.45GHz Center” under a category listed as “Frequency” as opposed to “2.45” under a category listed as “Center Frequency (2.45GHz).”

<table>
<thead>
<tr>
<th>Image</th>
<th>Digi-Key Part Number</th>
<th>Manufacturer Part Number</th>
<th>Description</th>
<th>Series</th>
<th>Manufacturer</th>
<th>Frequency</th>
<th>Bandwidth</th>
<th>Filter Type</th>
<th>Ripple</th>
<th>Insertion Loss</th>
</tr>
</thead>
<tbody>
<tr>
<td><img src="image1.png" alt="Image" /></td>
<td>49X-4745-2ND</td>
<td>1FB143401S09B740</td>
<td>FILTER BANDPASS 2.45GHz 09B740</td>
<td>-</td>
<td>Murata Electronics North America</td>
<td>2.45GHz Center</td>
<td>50MHz</td>
<td>Bandpass</td>
<td>0.7dB</td>
<td>1.8dB</td>
</tr>
<tr>
<td><img src="image2.png" alt="Image" /></td>
<td>49X-4745-1ND</td>
<td>1FB143401S09B740</td>
<td>FILTER BANDPASS 2.45GHz 09B740</td>
<td>-</td>
<td>Murata Electronics North America</td>
<td>2.45GHz Center</td>
<td>50MHz</td>
<td>Bandpass</td>
<td>0.7dB</td>
<td>1.8dB</td>
</tr>
<tr>
<td><img src="image3.png" alt="Image" /></td>
<td>49X-4745-6ND</td>
<td>1FB143401S09B740</td>
<td>FILTER BANDPASS 2.45GHz 09B740</td>
<td>-</td>
<td>Murata Electronics North America</td>
<td>2.45GHz Center</td>
<td>50MHz</td>
<td>Bandpass</td>
<td>0.7dB</td>
<td>1.8dB</td>
</tr>
<tr>
<td><img src="image4.png" alt="Image" /></td>
<td>445-4951-2ND</td>
<td>D2A1015010D105S09B740</td>
<td>DELAY LINE DCL-PCS SMD</td>
<td>-</td>
<td>TDK Corporation</td>
<td>1.8GHz Center</td>
<td>100MHz</td>
<td>Bandpass</td>
<td>-</td>
<td>0.4dB</td>
</tr>
</tbody>
</table>

**Figure 4-3:** Digi-Key Online catalog Listings of BPFs
The latter occurrence was common in Digi-Key listings; for example, as seen in Figure 4-3, similar issues hold for bandwidth ripple and insertion loss listings. In these cases, columns were divided (often using custom specified delimiters in Microsoft Excel’s “Text to Columns…” capability) to separate values from units. Where necessary, values could be made consistent with simple formulas carried down through columns to multiply or divide units where necessary. For example, MHz is the chosen unit for frequency in the BPF SR-CD; therefore, values from the Digi-Key table with associated “GHz” columns were multiplied by 1,000 whereas those with associated “MHz” columns were kept as provided. This approach was used to establish consistent values for all SR-CDs when needed. Once units were made consistent, text tags such as units or unit details such as “Center” were simply removed. A partial view of the compiled, completed BPF SR-CD result can be seen in Figure 4-4.

![Partial View of BPF SR-CD (“Zoomed Out” Showing All Columns)](image)

**Low Noise Amplifier (LNA) SR-CD**

The LNA SR-CD is indexed and referenced by the LNA entry in the RF stage of the single-RF-chain superheterodyne SDR receiver architecture in the SR-TSAM. The component specifications and characteristics captured for the LNA in the final SR-CD include manufacturer, manufacturer part number, description, lower bound frequency, upper bound frequency, RF type, gain, noise figure, P1dB, current supply minimum, current supply maximum, voltage supply

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minimum, voltage supply maximum, test frequency, package/case, and unit price. As with the BPF SR-CD and all other SR-CDs, characteristics manually added to the data include: component number, component preference, and manufacturer preference. The Digi-Key online catalog was used as the only source for this SR-CD.

As with the BPF SR-CD certain specifications, columns required reformatting such as those with units. Furthermore, in the reformatting process an especially notable adjustment and an assumption were made. The frequency range for LNAs in the Digi-Key catalog varied in their presentation. Sometimes, a range with a lower bound and upper bound frequency were clearly given. Other times, simply a list of frequencies (often, two frequencies) were given with commas separating the values. Still other times, only one frequency was specified. Given ranges were separated into two values: lower bound and upper bound values. Those with only one frequency specified were then categorized as the lower bound frequency to be detected and treated as center frequencies with an assumed bandwidth in the SR-TSAM (this is further explained in Section 4.3). Finally, when frequencies were given in a list, the lower frequency was used as a lower bound value and the higher of the frequencies was used as an upper bound value. This last assumption does not actually reflect the reality of many of these amplifiers since some amplifiers, in fact, may be simply multi-band amplifiers with two regions of linearity. Also, it is notable that the range assumptions were also made for multiple ranges of voltage supply values. As with price assumptions for the Mini-Circuits BPFs in the BPF SR-CD, the designer should be cautioned that the actual datasheet for specific LNAs should be referenced since the SR-TSAM and SR-CD values are intended to estimate receiver performance and compatibility for trend visualization purposes. A partial view of the final LNA SR-CD is shown in Figure 4-5.
RF Mixer (or Downconverter) SR-CD

The RF Mixer, or Downconverter, SR-CD is indexed and referenced by the RF Mixer entry in the IF stage of the single-RF-chain superheterodyne SDR receiver architecture in the SR-TSAM. The component specifications and characteristics captured for the RF Mixer in the final SR-CD include: manufacturer, manufacturer part number, series, description, lower bound frequency, upper bound frequency, RF type, number of mixers, gain, noise figure, current supply minimum, current supply maximum, voltage supply minimum, voltage supply maximum, package/case, and unit price. As with the other SR-CDs, characteristics manually added to the data include component number, component preference, and manufacturer preference. The Digi-Key online catalog was used as the only source for this SR-CD and the component of interest searched for were downconverter-specific RF mixers. Similar formatting adjustments to those made for the BPF and LNA SR-CDs were made including certain range adjustments made for the LNA SR-CDs. Another important note on the RF Mixer SR-CD is that it includes ICs that have system-on-a-chip (SoC) style RF front-ends within the chip including filters and amplifiers. These RF mixer ICs are not highlighted and are simply treated as RF mixers only. Again, specific datasheets should be accessed for component details. A partial view of the final RF Mixer SR-CD is shown in Figure 4-6.
The RF Mixer is part of what is defined in Section 4.3 as the “IF Conversion Block” in the SDR receiver architecture used by the SR-TSAM. As discussed in the description of the SR-TSAM, there are essentially two architecture options within the SR-TSAM: one that includes the IF Conversion Block and one that does not. To accommodate a situation in which an IF Conversion Block does not exist, a component entry is added to the RF Mixer with a Component Number value of zero. Its component is “[EMPTY]” and all specification values are set to zeros or blanks. The BPF SR-CD actually has such an entry as well for the IF stage BPF, which is also [EMPTY] in the absence of the IF Conversion Block.

**RF Amplifier (RF Amp) SR-CD**

The RF Amplifier SR-CD is indexed and referenced by the RF Amp entry in the IF stage of the single-RF-chain superheterodyne SDR receiver architecture in the SR-TSAM. The component specifications and characteristics captured for the RF Amplifier in the final SR-CD include manufacturer, manufacturer part number, description, lower bound frequency, upper bound frequency, RF type, lower bound gain, upper bound gain, noise figure, P1dB, current supply minimum, current supply maximum, voltage supply minimum, voltage supply maximum, test frequency, package/case, and unit price. As with all other SR-CDs, characteristics manually added to the data include: component number, component preference, and manufacturer preference. The Digi-Key online catalog was used as the only source for this SR-CD. It is notable that this SR-CD is essentially the same as the LNA SR-CD and all the same assumptions.

<table>
<thead>
<tr>
<th>Component #</th>
<th>Manufacturer</th>
<th>Manufacturer Part Number</th>
<th>Series</th>
<th>Description</th>
<th>Frequency Lower Bound (MHz)</th>
<th>Frequency Upper Bound (MHz)</th>
<th>RF Type</th>
<th>Number of Mixers</th>
<th>Gain</th>
<th>Noise Figure</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 [EMPTY]</td>
<td>[EMPTY]</td>
<td>[EMPTY]</td>
<td>[EMPTY]</td>
<td>[EMPTY]</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1 Analog Devices Inc AD608AR AD608 IC MIXER/LIMIT 500 NaN FM GSM PM PhS</td>
<td>1 24 16</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2 Analog Devices Inc AD608AR-REEL AD608 IC MIXER/LIMIT 500 NaN FM GSM PM PhS</td>
<td>1 24 16</td>
<td></td>
<td></td>
<td></td>
<td></td>
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<td></td>
</tr>
<tr>
<td>3 Analog Devices Inc AD608ARZ AD608 IC MIXER/LIMIT 500 NaN FM GSM PM PhS</td>
<td>1 24 16</td>
<td></td>
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<td></td>
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<tr>
<td>4 Analog Devices Inc AD608ARZ-RL AD608 IC MIXER/LIMIT 500 NaN FM GSM PM PhS</td>
<td>1 24 16</td>
<td></td>
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<td></td>
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<td></td>
</tr>
<tr>
<td>5 Analog Devices Inc AD6636BBCC AD6636 IC RSP 6CHAN NaN NaN Cellular CDMA200</td>
<td>1 NaN NaN</td>
<td></td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>6 Analog Devices Inc AD6636BBCCZ AD6636 IC DIGITAL DW NaN NaN Cellular CDMA200</td>
<td>1 NaN NaN</td>
<td></td>
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<tr>
<td>7 Analog Devices Inc AD6636BCZ AD6636 IC DIGITAL DW NaN NaN Cellular CDMA200</td>
<td>1 NaN NaN</td>
<td></td>
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</tr>
<tr>
<td>8 Analog Devices Inc AD831AP AD831 IC MIXER DWN 500 NaN HF VHF</td>
<td>1 0 14</td>
<td></td>
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</tr>
<tr>
<td>9 Analog Devices Inc AD831AP-REEL AD831 IC MIXER LOW 500 NaN HF VHF</td>
<td>1 0 14</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
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<td></td>
<td></td>
</tr>
</tbody>
</table>
and reformatting applied. The only addition to the RF Amplifier SR-CD above the LNA SR-CD is the division of the gain specification into a lower bound and upper bound since ranges were sometimes specified. Specified ranges sometimes indicate variable gain amplifiers (VGAs), which are often used as part of an AGC setup. To maintain this information for future use, the gain column is divided accordingly and amplifiers with only a single specified gain are listed with the lower bound gain. As addressed in Section 4.3, AGC processes are not considered in the current SR-TSAM, but keeping gain ranges specified in the SR-CD allows for some degree of flexibility in new revisions of the SR-TSAM to come. A partial view of the final RF Amplifier SR-CD is shown in Figure 4-7.

<table>
<thead>
<tr>
<th>Component #</th>
<th>Manufacturer</th>
<th>Manufacturer Part Number</th>
<th>Description</th>
<th>Frequency Lower Bound (MHz)</th>
<th>Frequency Upper Bound (MHz)</th>
<th>Current Minimum (mA)</th>
<th>Current Maximum (mA)</th>
<th>Voltage Minimum (V)</th>
<th>Voltage Maximum (V)</th>
<th>Gain Lower Bound (dB)</th>
<th>Gain Upper Bound (dB)</th>
</tr>
</thead>
<tbody>
<tr>
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<td>[EMPTY]</td>
<td>[EMPTY]</td>
<td>[EMPTY]</td>
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<td>0</td>
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<td>6000</td>
<td>93</td>
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<td>5.5</td>
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<td>50</td>
<td>6000</td>
<td>93</td>
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<td>IC GAIN BLOCK</td>
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<td>50</td>
<td>6000</td>
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<td>2700</td>
<td>104</td>
<td>124</td>
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<td>5.5</td>
<td>11.5</td>
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<td>400</td>
<td>2700</td>
<td>104</td>
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<td>4.5</td>
<td>5.5</td>
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<td>2700</td>
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<td>124</td>
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<td>5.5</td>
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<td>124</td>
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<td>5.5</td>
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<td>104</td>
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<tr>
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<td>IC AMP RF DRIVER</td>
<td>2.7GHz SOT89</td>
<td>400</td>
<td>2700</td>
<td>104</td>
<td>124</td>
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<td>2700</td>
<td>104</td>
<td>124</td>
<td>4.5</td>
<td>5.5</td>
<td>11.5</td>
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<tr>
<td>13</td>
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<td>ADL5542ACPZ-R7</td>
<td>IC AMP RF DRIVER</td>
<td>2.7GHz SOT89</td>
<td>400</td>
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<td>104</td>
<td>124</td>
<td>4.5</td>
<td>5.5</td>
<td>11.5</td>
</tr>
</tbody>
</table>

**Figure 4-7**: Partial View of RF Amplifier SR-CD (“Zoomed In” Not Showing All Columns)

While the RF Amplifier is not a part of the IF Conversion Block as defined by the architecture in the SR-TSAM to be highlighted further later, an [EMPTY] entry does exist as does for the components of the IF Conversion Block. This is to allow for designs without this amplification stage.

**Analog-to-Digital Converter (ADC) SR-CD**

The ADC SR-CD is indexed and referenced by the ADC entry at the end of the RF front-end of the single-RF-chain superheterodyne SDR receiver architecture in the SR-TSAM. The component specifications and characteristics captured for the ADC in the final SR-CD include manufacturer, manufacturer part number, bit resolution, sampling rate, number of channels,
power dissipation (typ.), signal-to-noise ratio (SNR), effective number of bits (ENOB), input voltage range, integral nonlinearity (INL), differential nonlinearity (DNL), signal-to-noise distortion (SINAD), total harmonic distortion (THD), spurious free dynamic range (SFDR), architecture, input/output (I/O), package, supply voltage range, comments, and unit price. As with all other SR-CDs, characteristics manually added to the data include component number, component preference, and manufacturer preference. The final ADC SR-CD implemented and accessed by the SR-TSAM is comprised of multiple sources from ADC manufacturers. While an ADC SR-CD was developed using the especially thorough ADC section of the Digi-Key online catalog, this SR-CD was not that implemented for the final SR-TSAM due to two major drawbacks.

The Digi-Key online catalog includes 11,801 ADCs by 12 different manufacturers. While this listing is extremely thorough, it has two major drawbacks that render its use and implementation not useful for the SR-TSAM. The first of these drawbacks is the overwhelming and repetitious nature of the listings. As highlighted in Section 4.2.1 in the discussion on component data sources, the catalog includes many entries of the same component with only minor differences. These differences often do not affect the critical specifications used by the SR-TSAM, which results in the SR-TSAM having access to 11,000+ ADCs that are not truly unique. The excessive sampling needs of the ATSV Exploration Engine indexing this type of database are wasteful if not all ADCs are unique. More practical would be to present only unique ADCs with different specifications and leave it to the designer to select the exact “flavor” of an ADC of interest. Unfortunately, filtering out repetition from the Digi-Key database is cumbersome. Considering the second major drawback in the following paragraph, this filtering exercise is not worth the effort.

The second drawback to the Digi-Key catalog listings of ADCs is the catalog’s lack of certain important specifications in the table. Because the ADC is such a critical component of an
SDR receiver, it was concluded that individual ADC specifications should be visualized and be made available for preference adjustment and visualization in ATSV. Therefore, even though the specifications actually used by the current version of the SR-TSAM for output specification calculations and compatibility checks are included in the Digi-Key ADC listings, other specifications critical to ADCs that should be available for visualization are not. Specifications like SNR, SFDR, and SINAD are absent from the Digi-Key online catalog. Not only should these and other specifications be available for individual visualization and preference control, future versions of the SR-TSAM are likely to actually leverage these specifications. Therefore, individual manufacturer sources were used to compile the ADC SR-CD. Many of the individual manufacturers listed some of the critical ADC specifications for high-speed ADCs. It should be noted that lower speed ADCs generally do not include some of these specifications in the captured SR-CD.

The manufacturer sources used for the ADC SR-CD include Analog Devices, Linear Technology, Maxim Integrated Products, National Semiconductor, and Texas Instruments. Analog Devices, Linear Technology, Maxim Integrated Products, and Texas Instruments all featured export functions that facilitated catalog access in XLS database form. While these databases often required reformatting, this resulted in an ideal SR-CD development scenario. National Semiconductor required the use of TableTools.

Because the tables presented by manufacturers were different, not all specifications could be compiled for all manufacturers, and the compiling and reformatting process for the ADC SR-CD was more aggressive and demanding than that for other SR-CDs. Furthermore, Linear Technology did not supply pricing within their table. Like the Mini-Circuits BPFs, pricing could only be found by individually accessing each component. Because this is a critical specification and because estimating prices for a range of products was more difficult than for the Mini-Circuit BPFs, each price was input to the database manually. Because multiple prices were given for
each component, the unit price for 1,000 unit quantities was given. This was selected since most other databases for ADCs and other components listed unit price per 1,000. However, as is the case with some other specifications, this should be individually checked when an ADC is selected. Many other specifications must also be checked for consistency when actually selected such as SFDR, which can be expressed as either dBC or dBS. A partial view of the final ADC SR-CD is shown in Figure 4-8.

<table>
<thead>
<tr>
<th>Component #</th>
<th>Manufacturer</th>
<th>Manufacturer Part #</th>
<th>Bit Resolution</th>
<th>Sampling Rate (MSPS)</th>
<th>Number of Channels</th>
<th>Power Dissipation (typ) (mW)</th>
<th>SNR (dB)</th>
<th>ENOB</th>
</tr>
</thead>
<tbody>
<tr>
<td>1632</td>
<td>Texas Instruments</td>
<td>TLV5535-Q1</td>
<td>8</td>
<td>35</td>
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<td>106</td>
<td>46.5</td>
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<tr>
<td>1633</td>
<td>Texas Instruments</td>
<td>TLC5540</td>
<td>8</td>
<td>40</td>
<td>1</td>
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<td>Texas Instruments</td>
<td>THS0842</td>
<td>8</td>
<td>40</td>
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<td>Texas Instruments</td>
<td>THS1040</td>
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</table>

**Figure 4-8:** Partial View of ADC SR-CD (“Zoomed In” Not Showing All Columns)

**Field Programmable Gate Array (FPGA) SR-CD**

The Field Programmable Gate Array (FPGA) SR-CD is indexed and referenced by the FPGA entry in the digital stage of the single-RF-chain superheterodyne SDR receiver architecture in the SR-TSAM. The component specifications and characteristics captured for the FPGA in the final SR-CD include manufacturer, manufacturer part number, series, description, delay time, number of I/O, number of logic blocks/elements, number of registers, minimum voltage supply, maximum voltage supply, operating temperature minimum, operating temperature maximum, package/case, and unit price. As with the other SR-CDs, characteristics manually added to the data include component number, component preference, and manufacturer preference. The Digi-Key online catalog was used as the only source for this SR-CD. The FPGAN SR-CD was developed from the Digi-Key online catalog and hence suffers from the same drawback of repetitious entries as discussed with regards to the ADC listings in the Digi-Key online catalog.
There are many FPGAs that represent only slight variations of others and repeat specifications. As a result, there are 3,967 entries in the FPGA SR-CD. In the case of the FPGA, this drawback was tolerated for two reasons: (1) the major manufacturers of FPGAs listed data in difficult-to-copy PDF catalogs as opposed to easily accessible and searchable HTML tables; and (2) the FPGA specifications are used for very little in the current version of the SR-TSAM and for this to change in future versions, a major digital resource analysis component will need to be added to the model, which may require certain database adjustments (this is further discussed in a later section). A partial view of the final FPGA SR-CD is shown in Figure 4-9.

<table>
<thead>
<tr>
<th>Component #</th>
<th>Manufacturer</th>
<th>Series</th>
<th>Manufacturer Part Number</th>
<th>Description</th>
<th>Delay Time (ns)</th>
<th>Number of I/O</th>
<th>Number of Logic Blocks/Elements</th>
<th>Number of Registers</th>
<th>Voltage Supply Min (V)</th>
<th>Voltage Supply Max (V)</th>
</tr>
</thead>
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<tr>
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<td>3.6</td>
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</tr>
</tbody>
</table>

**Figure 4-9:** Partial View of FPGA SR-CD (“Zoomed In” Not Showing All Columns)

**Manufacturer and Component Preference**

Each SR-CD includes the manually-input characteristics “Component Preference” and “Manufacturer Preference.” These two values represent a first step in the direction of what should become a major component of trade space visualization of SDR receiver design. The two characteristics are intended to address some of the design considerations and tradeoffs addressed in Section 3.3 of this work.

A designer is highly unlikely to select a component only based on its compatibility with a system and on its technical specifications. In reality, a designer is likely to have preferences associated with less tangible, less technical qualities. There are numerous factors involving such
things as risk, uncertainty, and logistics that a designer will consider in the selection of individual components for a system as well as in the overall design of the system. Because there are numerous tradeoffs associated with these factors, objectifying these as much as possible serves to benefit the visualization of the SDR receiver design space. For this work, two values are defined to capture a summary of some of these factors and preferences at both the manufacturer and the component level.

Manufacturer Preference

While many factors exist that will drive designers’ preferences concerning manufacturers, three likely factors include risk, uncertainty, and logistical considerations.

When designers are selecting components for a system, they must consider the level of risk associated with using a particular manufacturer. The risk factor, as with other factors, can be even further broken down into individual considerations. One risk consideration is the sourcing risk of a particular manufacturer: an assessment of the ability for the manufacturer to successfully source components in the required quantities for the required period of time. Another example of a risk consideration is technical risk: an assessment of the technological capabilities of a manufacturer as well as its technical track record.

Designers may also assess the level of uncertainty associated with a manufacturer. An example of an uncertainty consideration involves simple familiarity: an assessment of how familiar a designer and the designer’s available knowledge base (at a company or within an academic institution) is with the use of components from a particular manufacturer.

Designers may also consider logistical factors in the selection of components. For example, designers at companies or even academic research environments may have specific, strategic business arrangements, or possibly even business conflicts, with certain manufacturers but not others.
Capturing all of these factors and their considerations that influence manufacturer preference is difficult and complex. It is an issue that should undoubtedly be further investigated in the development of new SDR-RM versions. Capturing these preferences in sufficient detail is likely to involve a certain level of customization depending on the end-user of the SDR-RM in order to accommodate differing approaches and considerations. However, to establish the feasibility of the inclusion of such considerations in the SDR-RM for trade space visualization as well as to illustrate a possible approach, a simple preference index system is implemented in the current SDR-RM. The SR-CD entry “Manufacturer Preference” is intended to be a summary of all factors involved in the determination of a designer’s preference towards a particular manufacturer. The value is a measurement of how “preferred” a manufacturer is by the designer on a scale from 0 to 5, with 0 being the least preferred and 5 being the most. This value, which defaults to zero in the current SR-CDs (although is adjusted for examples such as that in Section 5.2.3), is meant to be manually set by the users of the SDR-RM according to their own measurements. The Manufacturer Preference of one selected component in the SR-TSAM can be combined with the values of others to determine the overall Manufacturer Preference value of the receiver system. In future versions of the SDR-RM, this value may divided up among multiple more specifically defined preference values to capture all factors of importance to the end-user designer. Even in the simple examples of factors and considerations listed above, the need for separation can be seen: perhaps a designer would like to minimize the sourcing risk and technical risk from a manufacturer but does not require high familiarity with this manufacturer or the leveraging of any existing business relationships; in this case, an objective set simply to minimize or maximize manufacturer preference will not yield the desired results.

Component Preference

The “Component Preference” SR-CD entry is very similar to the Manufacturer Preference entry. As with the use of particular manufacturers, designers are likely to have
preferences related to the use of specific, individual components based on factors such as risk, uncertainty, and logistical considerations. In the case of selecting individual components, these factors may actually be dependent on some similar considerations as those associated with selecting a manufacturer but at a lower, component level. For example, sourcing risk is likely to be a risk consideration at the component level, but instead of assessing a manufacturer’s ability to source components in general, this may assess the likelihood that a manufacturer can adequately source a specific component, which may be influenced by its age (very old, very new, or recently announced components may have a high source risk, for example) or by any sub-contractors involved in a specific component. Technical risk is another risk consideration likely to be considered at the component level as well; however, this may be a more significant consideration at the component level than at the manufacturer level in which a designer must analyze how proven the underlying technology of a particular component is (again, this may be heavily driven by the age of the component). Familiarity and logistical arrangements may also play a role in a similar way as at the manufacturer level. How familiar a designer is with a particular component will factor into preference, and specific component deals and arrangements between manufacturers and designers may also factor in.

A particularly notable hypothesis regarding Component Preference is that many factors and considerations are likely to be highly dependent on the novelty of a particular component. For example, as mentioned, a new, or even an announced but yet-to-be released, component may bring with it a high sourcing risk (i.e., will it be ready in time and in the right quantities and will it last?), high technical risk (i.e., is it going to work as expected or could there be unforeseen problems?), high unfamiliarity, possible unavailability through existing channels, etc. In the realm of SDR, this is important to quantify when developing the SR-CDs. The true flexibility and functionality of SDR systems is heavily dependent on the availability of many emerging and cutting-edge components. For example, as discussed in Section 0, a large number of design
tradeoffs and capabilities are tied directly to available ADC technology. In many cases, cost aside, the absolute best ADC available might seem to be the obvious choice for receiver design. However, a designer may be averse to the high risks associated with selecting the latest ADCs and particularly those that have not been released yet but should be available by design completion and production. In future investigation and development, a way to quantify the novelty of devices and its impact on component preference must be investigated.

As was the case with Manufacturer Preference, Component Preference is complex and difficult to quantify. Furthermore, it should be divided into many sub-factors and sub-considerations that influence preferences according to the end-user application. However, the same system is employed for Component Preferences as Manufacturer Preference to prove the feasibility of including preference considerations and to investigate examples: a value is assigned measuring how “preferred” a component is by the designer on a scale from 0 to 5, 0 being the least preferred and 5 being the most.

**A Note on Blank Values**

As has been alluded to, not all specifications could be collected for all components in the SR-CDs. This is a product of different sources being used as well as simply the limited availability of certain specifications even within a single source. Because this is an inevitability of SR-CD development, it is important to ensure that blank values are treated properly.

For the purposes of being referenced by the SR-TSAM, the text “NaN” (specifying “not a number”) was automatically inserted into all blank entries using the Find & Replace feature in Excel. Many blank entries actually started with some text (typically a single hyphen) when collected from sources, so in such cases, this text was first removed also using the Find & Replace feature.

The entry of “NaN” into the SR-CDs ensures that if the SR-TSAM encounters a blank value where it requires a numerical value for a calculation, it will return an error. If the entry is
simply left blank, Excel will complete a calculation simply treating the blank value as a zero. For example if a component is missing a price listing, the total cost of the SDR receiver would return an error in the SR-TSAM if “NaN” has been inserted in this blank entry, whereas if the entry was left blank the total cost of the receiver would have assumed it was a free component. While errors help prevent problems like free components, passing these into ATSV can result in data integrity problems. Therefore, for SR-TSAM output specification calculations likely to encounter such problems, NaN value entries can instead be used to set outlying output values to be easily filtered out by ATSV. For example, instead of returning errors, the component price output specification is actually set to return $0.00 for total system cost if one component has a “NaN” price entry. This enables easy filtering in ATSV of obviously poor data (see the “Component Price” sub-section of Section 4.3.6 for more details on this process).

4.2.3. Refining SR-CDs for Better Exploration Engine Interface

The SR-CDs described in Section 4.2.2 are in XLS form and, given all necessary formatting adjustments for unity, are ready for access by the SR-TSAM. However, two adjustments were made to the SR-CDs to improve their interaction with ATSV and its Exploration Engine.

Frequency Sorted SR-CD Versions

The SR-CDs are sampled by the SR-TSAM using discrete “Component Number” values that index respective SR-CDs in order to return specific component specification values corresponding with a Component Number sample. The ATSV Exploration Engine can sample ranges of discrete values with relative ease and with little user input requiring only the range input. A user specifies the range of discrete values to be sampled for each SR-CD when linking the ATSV Exploration Engine and the SR-TSAM. While the entire range of Component
Numbers for a particular SR-CD can be sampled, it also may be convenient to streamline the sampling process by indicating a smaller range of discrete values that are more likely to sample feasible components.

As elaborated upon in Sections 4.3.8 and 4.3.9, many of the compatibility checks that dictate design feasibility have to do with frequency values. Therefore, a useful way to streamline the sampling process between the ATSV Exploration Engine and the SR-TSAM would be to specify a range of discrete Component Number values that represent components within the correct frequency range of the design of interest. Because the SR-CDs described in Section 4.2.2 were sorted first by manufacturer and next by manufacturer part number to make component searching easy, Component Numbers are specified accordingly. Therefore, in order to specify a range of discrete values to sample that represent a certain frequency range regardless of manufacturer, the SR-CDs had to be re-sorted in Excel. A special set of SR-CDs was developed called “Frequency Arranged SR-CDs” that first arranged components by frequencies (or sampling rates) and next by bandwidths where relevant. These versions include Component Number values arranged according to this new sorting, and old Component Number values were retained under the column “Legacy Component Number.”

**Comma Separated Value Versions**

In addition to being used for SR-TSAM access, the SR-CDs can be effectively used for visualization of independent component trends within ATSV. This alone serves to benefit greatly SDR designers seeking to understand trends and tradeoffs associated with individual components. However, in order to accommodate use with ATSV, CSV versions had to be created. To accomplish this, all commas were removed using the Find and Replace feature of Microsoft Excel, and the XLS was simply resaved to a CSV. Furthermore, all previously blank values set with NaN values were reset to blank values to allow ATSV to automatically assign NaN and Null values during the loading of a database.
4.3. SDR Receiver Trade Space Analysis Model (SR-TSAM) Development & Implementation

The SDR Receiver Trade Space Analysis Model (SR-TSAM) is an Excel-based model of a single-RF-chain superheterodyne SDR receiver that leverages SR-CD inputs and designer-generated system design inputs to determine “feasible” designs based on simple compatibility checks and to calculate basic receiver specifications. The purpose of the SR-TSAM is to be linked to ATSV for sampling and trade space visualization of the single-RF-chain superheterodyne SDR receiver design space. The SR-TSAM consists of five primary sections: Component Inputs, Key Signal Inputs, Key System Design Inputs, Key System Specification Outputs, and Component Compatibility Determination. Figure 4-10 shows an image of the XLS SR-TSAM with example input values in the model. The image displays all sections except the Component Inputs section, which is only featured as a partial view since each individual component input along the bottom of the SR-TSAM extends beyond the cells featured in the image. Due to the small size of Figure 4-10, Figure B-1 in Appendix B can be referenced instead for a clearer image of the all SR-TSAM sections except for the Input Components section.
Sections 4.3.1 and 4.3.2 introduce the architecture possibilities and assumptions that govern the component inputs to the SR-TSAM. Section 4.3.3 addresses the Component Inputs section of the SR-TSAM. Sections 4.3.4 and 4.3.5 explains the user inputs sections including the Key Signal Inputs and the Key System Design Inputs sections respectively. Section 4.3.6 discusses the Key System Specification Outputs section of the SR-TSAM. Section 4.3.7
introduces Component Compatibility Determination and Sections 4.3.8–4.3.11 breaks down the Component Compatibility Determination section in detail.

4.3.1. Single-RF-Chain Superheterodyne SDR Receiver Architecture Possibilities

The receiver architecture used by the SR-TSAM is the single-RF-chain superheterodyne SDR receiver defined in Section 2.1.3 with an FPGA serving as the digital receiver chip. However, the SR-TSAM features the ability to simulate an alternate architecture that excludes an analog IF stage and consists of an RF stage directly converted to digital form. The two architecture possibilities used by the SR-TSAM to identify feasible designs are illustrated in Figure 4-11 as they appear in the SR-TSAM XLS file.

**Figure 4-11**: The Architecture Possibilities of the SR-TSAM
The top figure in Figure 4-11 is the single-RF-chain superheterodyne SDR receiver architecture as it has been defined and described in previous chapters. It features an intermediate frequency (IF) stage in which the originally received radio-frequency (RF) signal is downconverted via heterodyning (or, signal mixing) to a lower frequency. The IF stage of the top figure in Figure 4-11 consists of the components represented in gold: the RF mixer (or, analog mixer), the local oscillator, the IF band-pass filter, the RF amplifier, and then the transition into the digital domain via the ADC and FPGA in which digital downconversion to baseband will occur. For the purposes of this work, three of the IF components are defined as part of the “IF Conversion Block”: the RF mixer, the LO, and the IF BPF.

The bottom figure in Figure 4-11 is the single-RF-chain superheterodyne SDR receiver architecture without the IF Conversion Block. In this architecture, an analog IF stage is not present. Instead, the RF stage, represented in orange, extends into the digital domain. There are two additional possibilities within this architecture: one regarding the final RF amplifier and the other regarding the presence of an IF stage. The SR-TSAM has the ability to recognize designs with and without a final amplification stage. This is actually true of the architecture with the analog IF stage (top figure in Figure 4-11) as well as the architecture without the IF Conversion Block (bottom figure in Figure 4-11). While the absence of this component is unlikely, the flexibility is left there to accommodate minimalistic designs given a powerful enough ADC and high enough gain in the RF front. Furthermore, it is possible that even a digital IF stage does not exist and instead the RF signal is directly digitally downconverted to baseband within the DDC (implemented via FPGA). This possibility does not concern this particular work or the current SR-TSAM since the software platform of the FPGA or DSP chip is not considered. It should be noted, however, that in the absence of an IF stage, the term “superheterodyne” is actually a misnomer.
For most receiver designs, the absence of any analog IF stage (the IF Conversion Block) is unlikely. However, given the increasing speeds and resolution of ADCs, an architecture that excludes the IF Conversion Block is allowed by the SR-TSAM so long as it satisfies the compatibility requirements to be described in Sections 4.3.7–4.3.11. This is intended to be a first step in investigating tradeoffs associated with removing an IF stage if the possibility arises. For example, at the current time, the removal of the IF Conversion Block is likely to require an especially high-end ADC, which will increase the cost and, most likely, the power consumption of the ADC above the levels with an IF Conversion Block present. By allowing the SR-TSAM to recognize designs with and without the IF Conversion Block that meet basic feasibility requirements, the designer is enabled to explore these tradeoffs visually using ATSV.

4.3.2. Architecture Simplification Assumptions

Several assumptions and simplifications are applied to the current version of the SR-TSAM that must be noted. Many of these assumptions and simplifications should be adjusted in future versions of the SR-TSAM.

Compatibility Determination Scope

As described in Sections 4.3.7–4.3.11, each modeled component is checked for its compatibility with the overall system according to four primary criteria: (1) frequency range, (2) bandwidth, (3) voltage supply, and (4) the use of the IF Conversion Block. While some of those criteria mean different things for different components, they represent the full scope of compatibility determination. Therefore, no compatibility considerations are included beyond those outlined in Sections 4.3.7–4.3.11. As future models of the SR-TSAM are developed, the existing compatibility determination fields should be refined and improved, and new compatibility determination fields should be added.
No Available Digital Resource Analysis

A critical consideration in the design of SDR systems is the availability of digital computing resources for the digital functionality of the system. This was a large focus in the Space Transceiver Analysis Tool (STAT) described in Section 2.2, which included resource utilization analysis. The SR-TSAM currently does not include an analysis of available digital resources but instead facilitates goal-driven visualization of individual ADC and FPGA specifications (further elaborated upon in Section 4.4). Modeling is focused on hardware compatibility and analog RF front-end specifications as opposed to detailed digital resource analysis.

Missing Components

The current SR-TSAM does not model the following components featured in the receiver architecture shown in Figure 4-11: antenna, LO, and DSP.

Antenna

The antenna is not modeled in the current SR-TSAM version, and an antenna SR-CD has not been developed. In designing a true SDR receiver, the antenna selection decision may range from one of little significance to one of great significance depending on the needs and requirements of the system. SDR systems requiring especially large bandwidths to cover a number of frequencies and waveforms demand special antenna considerations and the use of special antenna systems such as multiband antennas and smart antennas. These special antennas, in addition to antenna systems involving multiple RF chain receiver architectures, are outside the scope of this work and the SR-TSAM version presented herein. Because the antenna is not modeled, yet the impedance and gain specifications are used in an output calculation, assumptions are made that are explained in Section 4.3.5.
**Local Oscillator**

The local oscillator (LO) is not modeled in the current SR-TSAM version, and an LO SR-CD has not been developed. Selecting a proper LO is outside the current scope of the initial, proof-of-concept SDR-RM developed for this work. As a result, a critical assumption is made in the SR-TSAM: any standard intermediate frequency can be selected without regard to LO selection. This must be revisited in the future with the addition of an LO SR-CD.

**Digital Signal Processing Chip**

The DSP component beyond the FPGA is not modeled in the current SR-TSAM version, and a DSP SR-CD has not been developed. The use of a DSP is heavily dependent on the software platform and application-specific needs of the radio, which is outside the scope of this initial proof-of-concept SR-TSAM.

**No Automatic Gain Control**

It is likely that an SDR receiver would include automatic gain control (AGC). AGC can be accomplished one of several ways in hardware and/or in software. In this model, AGC is not considered directly. AGC algorithms therefore are assumed to exist only in the digital domain, and all RF amplifiers are considered for the final amplifier in the analog hardware chain as opposed to only those with variable gain controlled by AGC algorithms in hardware or software. Variable gain amplifiers (VGAs) are in the RF Amplifier SR-CD along with other single-gain amplifiers, but future versions of the SR-TSAM should explore these separately as well as explore hardware AGC implementations in order to facilitate visualization of various AGC implementations.

**Single-RF-Chain Architecture**

As previously discussed, multiband SDR systems with significantly large bandwidth needs may likely require multiple-RF-chain architectures. However, this proof-of-concept version of the SR-TSAM presented within this work considers only single-RF-chain design. A
well-refined single-RF-chain architecture-based SR-TSAM will lend itself to simple translation to versions based on other architectures.

4.3.3. Component Inputs – Sampling the SR-TSAM

The SR-TSAM contains three types of model inputs and outputs that are critical to the visualization process in ATSV. As shown in Figure 4-10 and Figure B-1, the SR-TSAM contains a Model I/O Color Key that defines the colors used to designate these critical inputs and outputs. The color key can be seen in Figure 4-12.

The ATSV inputs highlighted in the light blue color seen in Figure 4-12 are those that actually define each individual receiver design being investigated at each ATSV sample point for visualization. A particular receiver design is defined in the SR-TSAM by the components selected from the SR-CDs. Each modeled component in the single-RF-chain superheterodyne SDR receiver architecture is sampled using an ATSV input field “Database Component Number.” According to its sampling routine to be discussed in Section 4.4, the ATSV Exploration Engine provides discrete values to each of these Database Component Number input fields for each modeled component. These discrete values are used to index the corresponding SR-CD for each component. The values in the Database Component Number fields correspond to the “Component #” fields in their respective SR-CDs. Using the Microsoft Excel VLOOKUP command, component specification values that match up with the indexed Component # are returned from each SR-CD to corresponding fields in the SR-TSAM. For example, as can be seen in the partial view of the Component Inputs section of the SR-TSAM in Figure 4-13, if the
ATSV Exploration Engine inputs the sample discrete value of 1675 to the Database Component Number filed of the Analog to Digital Converter Input, then the number 1675 is used to index the ADC SR-CD using the “Component #” field in the SR-CD. In the frequency-sorted SR-CDs described in Section 4.2.3, component number 1675 corresponds to the Analog Devices AD9054A-200 ADC. Therefore, this ADC is returned to the SR-TSAM, and all of its associated specifications are returned to corresponding fields in the SR-TSAM in the Component Inputs section. Several other partial views of component examples are shown from the Component Inputs section in Figure 4-13.

The specifications for these indexed components then are referenced by the rest of the SR-TSAM and are used in the system specification output calculations as well as the compatibility determination algorithms yet to be described.

As highlighted in Sections 4.2.2 and 4.3.1, components in the IF Conversion Block can be left out of the design to allow for the exploration of designs without an analog IF component. Furthermore, the final RF Amplifier can also be left out of the design. These components are left out of the design when the ATSV Exploration Engine uses the discrete value 0 to sample the

---

**Figure 4-13:** Partial View of the Component Inputs in the SR-TSAM With Example Samples

<table>
<thead>
<tr>
<th>Band-Pass Filter (IF) Input</th>
<th>Database Component Number: 25</th>
</tr>
</thead>
<tbody>
<tr>
<td>BPF(IF) Manufacturer</td>
<td></td>
</tr>
<tr>
<td>BPF(IF) Part Number</td>
<td></td>
</tr>
<tr>
<td>BPF(IF) Series</td>
<td></td>
</tr>
<tr>
<td>BPF(IF) Description</td>
<td></td>
</tr>
<tr>
<td>BPF(IF) Center Frequency (MHz)</td>
<td></td>
</tr>
<tr>
<td>BPF(IF) Bandwidth (MHz)</td>
<td></td>
</tr>
<tr>
<td>Max-Circuits</td>
<td></td>
</tr>
<tr>
<td>BPF-70 (+)</td>
<td>NaN</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>RF Amplifier Input</th>
<th>Database Component Number: 10</th>
</tr>
</thead>
<tbody>
<tr>
<td>RF Amp Manufacturer</td>
<td></td>
</tr>
<tr>
<td>RF Amp Part Number</td>
<td></td>
</tr>
<tr>
<td>RF Amp Description</td>
<td></td>
</tr>
<tr>
<td>RF Amp Frequency Lower Bound (MHz)</td>
<td></td>
</tr>
<tr>
<td>RF Amp Frequency Upper Bound (MHz)</td>
<td></td>
</tr>
<tr>
<td>RF Amp Current Minimum (mA)</td>
<td></td>
</tr>
<tr>
<td>Avago Technologies US Inc.</td>
<td></td>
</tr>
<tr>
<td>BMA-3T14-BLKG</td>
<td>AMP MMC SI BIPOLAR</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Analog to Digital Converter Input</th>
<th>Database Component Number: 1675</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADC Manufacturer</td>
<td></td>
</tr>
<tr>
<td>ADC Part Number</td>
<td></td>
</tr>
<tr>
<td>ADC Bit Resolution</td>
<td></td>
</tr>
<tr>
<td>ADC Sampling Rate (NSPS)</td>
<td></td>
</tr>
<tr>
<td>ADC Number of Channels</td>
<td></td>
</tr>
<tr>
<td>ADC Power Dissipation (mW)</td>
<td></td>
</tr>
<tr>
<td>Analog Devices</td>
<td></td>
</tr>
<tr>
<td>AD9054A-200</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Field Programmable Gate Array Input</th>
<th>Database Component Number: 10</th>
</tr>
</thead>
<tbody>
<tr>
<td>FPGA Manufacturer</td>
<td></td>
</tr>
<tr>
<td>FPGA Part Number</td>
<td></td>
</tr>
<tr>
<td>FPGA Series</td>
<td></td>
</tr>
<tr>
<td>FPGA Description</td>
<td></td>
</tr>
<tr>
<td>FPGA Delay Time (ns)</td>
<td></td>
</tr>
<tr>
<td>FPGA Number of I/O</td>
<td></td>
</tr>
<tr>
<td>Altera</td>
<td></td>
</tr>
<tr>
<td>ACEX-1K6</td>
<td></td>
</tr>
<tr>
<td>EPH10YC144-2N</td>
<td>IC ACEX 1K FPGA 10K 1</td>
</tr>
</tbody>
</table>

---

1 Figures such as Figure 4-13 are images of tables from the SR-TSAM
components. In the RF Mixer, BPF, and RF Amplifier SR-CDs, the component number 0 corresponds to an [EMPTY] component. An example of such a scenario can be seen in Figure 4-14.

<table>
<thead>
<tr>
<th>Database Component Number:</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>BPF(IF) Manufacturer</td>
<td>[EMPTY]</td>
</tr>
<tr>
<td>BPF(IF) Manufacturer Part Number</td>
<td>[EMPTY]</td>
</tr>
<tr>
<td>BPF(IF) Series</td>
<td>[EMPTY]</td>
</tr>
<tr>
<td>BPF(IF) Description</td>
<td>[EMPTY]</td>
</tr>
<tr>
<td>BPF(IF) Center Frequency (MHz)</td>
<td>0</td>
</tr>
<tr>
<td>BPF(IF) Bandwidth (MHz)</td>
<td>0</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Database Component Number:</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>RF Amp Manufacturer</td>
<td>[EMPTY]</td>
</tr>
<tr>
<td>RF Amp Manufacturer Part Number</td>
<td>[EMPTY]</td>
</tr>
<tr>
<td>RF Amp Description</td>
<td>[EMPTY]</td>
</tr>
<tr>
<td>RF Amp Lower Bound (MHz)</td>
<td>0</td>
</tr>
<tr>
<td>RF Amp Upper Bound (MHz)</td>
<td>0</td>
</tr>
<tr>
<td>RF Amp Current Minimum (mA)</td>
<td>0</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Database Component Number:</th>
<th>1675</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADC Manufacturer</td>
<td>Analog Devices</td>
</tr>
<tr>
<td>ADC Manufacturer Part Number</td>
<td>AD9064A-200</td>
</tr>
<tr>
<td>ADC Bit Resolution</td>
<td>8</td>
</tr>
<tr>
<td>ADC Sampling Rate (MSPS)</td>
<td>200</td>
</tr>
<tr>
<td>ADC Number of Channels</td>
<td>1</td>
</tr>
<tr>
<td>ADC Power Dissipation (typ) (mW)</td>
<td>791</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Database Component Number:</th>
<th>10</th>
</tr>
</thead>
<tbody>
<tr>
<td>FPGA Manufacturer</td>
<td>Altera</td>
</tr>
<tr>
<td>FPGA Manufacturer Part Number</td>
<td>ACEX-1K8</td>
</tr>
<tr>
<td>FPGA Description</td>
<td>EP1K10TC144-2N</td>
</tr>
<tr>
<td>FPGA Delay Time (ns)</td>
<td>43</td>
</tr>
<tr>
<td>FPGA Number of I/O</td>
<td>95</td>
</tr>
</tbody>
</table>

Figure 4-14: Partial View of the Component Inputs in the SR-TSAM With Empty Components

4.3.4. Key Signal Inputs—Basic SR-TSAM Objectives

The first set of user inputs (light green according to the Model I/O Color Key) in the SR-TSAM are the Key Signal Inputs. These represent the basic objectives the designer has for the receiver before attempting the visualization process. Two signal inputs are specified: signal frequency and signal bandwidth. One signal assumption is specified: the minimum SNR required at ADC. These fields can be seen in Figure 4-15. These input fields are described within this section.

<table>
<thead>
<tr>
<th>Key Signal Inputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>Frequency (MHz)</td>
</tr>
<tr>
<td>Bandwidth (kHz)</td>
</tr>
<tr>
<td>Minimum SNR Required at ADC (dB)</td>
</tr>
</tbody>
</table>

Figure 4-15: Key Signal Inputs Section of the SR-TSAM
**Frequency**

The “Frequency” field, which is given in MHz, is where the designer specifies the center frequency of the signal that the receiver must capture. To illustrate the use of the SR-TSAM, consider the following simple example: a designer intends to develop a single-RF-chain superheterodyne SDR receiver to encompass the full 162–174 MHz range, which is a band used by the FAA (Federal Aviation Administration) for land communications [“Aviation Frequencies,” 2010]. The frequency in the center of the band of interest to the designer is 168 MHz; hence, the designer inputs the value 168 into the Frequency field.

**Bandwidth**

The “Bandwidth” field, which is given in kHz, is where the designer specifies the full bandwidth of the signal that the receiver must capture. The bandwidth is defined in the SR-TSAM as being centered on the center frequency specified by the latter field. Referring to the land communications FAA example, the bandwidth of interest is 12 MHz (6 MHz on either side of the center frequency, 168 MHz). Therefore, the designer inserts the value 12,000 into the Bandwidth field.

**Minimum SNR Required at ADC**

The “Minimum SNR Required at ADC” field actually defines a key assumption for the receiver system. While this assumption is not necessarily a signal parameter, it does play a significant role in the determination of receiver sensitivity, which is a specification that a designer may start with in mind.

The value specified in dB within the “Minimum SNR Required at ADC” field is used directly in the calculation of Minimum Detectable Signal (MDS) as described in Section 4.3.6. This value represents the minimum signal-to-noise ratio (SNR) required at the input of the ADC for successful A/D conversion for further processing down the receiver chain. This value appeared as $\text{SNR}_{\text{min}}$ in (Eq. 3-16) in Section 3.1.4. As discussed in Section 3.1.4, the minimum
input SNR to the ADC (or, the output SNR from analog RF/IF stages) in a digital superheterodyne receiver architecture can actually be calculated from numerous ADC specifications, especially SNR and SFDR. However, given the differing methods for this determination, the complexity of the determination, and the limitations of the existing ADC SR-CD, the value is assumed to be defined in this field. This is much the same way as minimum SNR values for traditional hardware radios may be assumed according to end use application [Miranda, 2007]. The assumption made in the “Minimum Required at ADC” field allows for an MDS calculation to prove the feasibility of conducting sensitivity calculations in the SR-TSAM. The assumption of this value provides further justification for modifications made to the SR-TSAM-to-ATSV configuration link described in Section 4.4.2. In the case of the given example, 15 dB is used.

4.3.5. Key System Design Inputs—Dynamic SR-TSAM Rules

The second set of user inputs (light green according to the Model I/O Color Key) in the SR-TSAM are the Key System Design Inputs. These represent various assumptions and design rules the designer must define prior to design space visualization. Ten fields are defined in this section of the SR-TSAM: (1) Sub-Sampling Allowed, (2) Sampling Rate Factor, (3) IF Frequency, (4) Constant Voltage Level, (5) Voltage Supply, (6) Assumed Filter Insertion Loss if Missing, (7) Amplifier Default Half Bandwidth %, (8) Mixer Default Half Bandwidth %, (9) Antenna Impedance, and (10) Antenna Gain. These fields can be seen in Figure 4-16. These input fields are described within this section.
The “Sub-Sampling Allowed” field is the input field in which the designer can specify whether or not sub-sampling techniques can be employed at the ADC. As discussed in Section 2.1.2, using sub-sampling techniques a designer can carefully select an ADC sampling rate such that critical signal information is not lost despite aliasing. This means that the ADC sampling frequency does not necessary have to be at least twice the input center frequency as required by the Nyquist criterion. Therefore, if the designer enables sub-sampling in this field, the sampling rate of the ADC does not have to be at least twice the signal frequency, which is a compatibility determination field discussed in Section 4.3.8. It is notable that a significant assumption has been made in this current SR-TSAM version that should be revisited in future versions. It is assumed that, with sub-sampling enabled, any signal center frequency whether from the RF or an IF stage is compatible with any ADC sampling rate. In reality, not all ADCs are even capable of sub-sampling; in order to facilitate frequency folding techniques, ADCs must have full analog bandwidths that exceed their sampling rates. Furthermore, even these ADCs are not necessarily capable of any frequency. Therefore, future SR-TSAM and ADC SR-CD development should correct and adjust this assumption.
A designer enables, or allows, sub-sampling techniques to be employed by setting this field input to a discrete value of 1. The discrete value 0 disables, or does not allow, sub-sampling. Figure 4-16 shows the continuation of the FAA land communications example introduced in Section 4.3.4. In this example, sub-sampling is disabled.

**Sampling Rate Factor**

The “Sampling Rate Factor” field allows the user to tweak the multiplier used to determine the required ADC sampling rate for sufficient sampling of the input signal from the input signal’s frequency and/or bandwidth. According to the Nyquist criterion, the sampling rate must be at least twice that of the input frequency and bandwidth (or simply, the bandwidth for this SR-TSAM version if sub-sampling is enabled) to avoid signal aliasing. However, many actual systems require oversampling to ensure the absence of aliasing in practical use [Mitola, 1995]. For example, a designer may specify that the required sampling frequency must be 2.5 times that of signal frequency and/or bandwidth as is given in the example displayed in Figure 4-16. In this case the sampling rate factor (SRF) is 2.5.

**IF Frequency**

The “IF Frequency” field is where the user specifies the intermediate frequency that will be used with the IF Conversion Block is present. This field actually represents a significant assumption required by RF Mixer SR-CD limitations: the current SR-TSAM version assumes that any selected intermediate frequency can be output by any of the selected RF mixers and that any local oscillator required is available and also compatible with selected RF mixers. This is a significant assumption that should be revisited in future versions of the SR-TSAM and future versions of the RF Mixer SR-CD.

It is reasonable to expect that a designer may indeed have an IF preference. The designer is likely to input a standard intermediate frequency into this field dictated by crystal oscillator and related technology as well as possibly by regulation. Some common, standard IFs include 455
kHz, 10.7 MHz, 21.4 MHz, 60.0 MHz, 70.0 MHz, and 140.0 MHz [Dixon, 1998]. In the example provided, 70 MHz is selected.

**Constant Voltage Level**

The “Constant Voltage Level” field allows the designer to specify if a receiver design should hold one constant voltage supply level. This allows the designer to minimize the power supply hardware and specify that one voltage level must be accepted by all devices within a design. As further described in Section 4.3.10, if the designer specifies that the voltage level for the power supply of the receiver is to be at a constant level accepted by all devices, than the selected level specified in the “Voltage Supply” input field must fall within the minimum and maximum voltage supply level of all components in order for a design to be deemed compatible with the available voltage supply. If a constant voltage level is not required, then the Voltage Supply level simply must exceed the minimum voltage supply requirements for all components to be deemed a compatible design under the assumption that the designer may step down voltage where necessary within the architecture. A discrete value of 1 specifies that a constant voltage must be maintained while a value of 0 releases this requirement. In the given example, 0 is selected, thereby releasing the receiver from the requirement that all components accept the unaltered voltage specified in the Voltage Supply field.

**Voltage Supply**

The “Voltage Supply” field is where the designer specifies the available voltage supply level for the receiver. This field represents the maximum voltage supply level available to the components of the receiver. Depending on the value within the “Constant Voltage Level” field, this value may represent the voltage level that must simply exceed the minimum voltage supply requirement of all components or may represent the precise voltage level that must be used by all components (between the minimum and maximum voltage supply requirement for each component). In the given example, this value is set to 5 V.
Assumed Filter Insertion Loss if Missing

The “Assumed Filter Insertion Loss if Missing” field is where the designer may specify an insertion loss in dB to apply to a BPF (in the RF or IF stage) that does not have a specified insertion loss in the BPF SR-CD. Unfortunately, as highlighted in Section 4.2.2, many of the filters in the BPF SR-CD do not include insertion loss information. Specifically, the Mini-Circuits filters do not have listed insertion loss values. Therefore, an insertion loss should be assumed for these filters for calculations in the Key System Specification Outputs section such as for receiver noise figure. If the designer prefers to not use an assumed value, the designer may enter a NaN value to this field, which results in errors in calculations using this value such as noise figure. Future versions should address this in a similar way pricing errors are handled (see the “Component Price” sub-section of Section 4.3.6).

A value of 2 dB is given in the current example and actually serves as a good default value given that it is on the higher end of typical insertion loss parameters for many of the Mini-Circuits BPFs in the BPF SR-CD that are missing values. This was determined by checking a number of the Mini-Circuits BPF datasheets and filling in some of the values manually in the SR-CD.

Amplifier Default Half Bandwidth Percentage

The “Amplifier Default Half Bandwidth %” field gives the designer the ability to specify a bandwidth for amplifiers without specified bandwidths. As described in Section 4.2.2, when LNAs and RF Amplifiers did not specify a lower and upper bound frequency in component specification tables but instead specified only one frequency, this frequency was recorded into the respective SR-CDs as the lower bound frequency. However, in the absence of an upper bound frequency, this recorded lower bound frequency is actually assumed to be a center frequency for an amplifier. The Amplifier Default Half Bandwidth (ADHB) specified by the designer in the “Amplifier Default Half Bandwidth %” field is a value given as a percentage that is used to
calculate a lower and upper bound frequency centered on the given center frequency \( f_c \)
according to

\[
f_l = f_c - \text{ADHB} \cdot f_c \quad \text{(MHz)},
\]

(Eq. 4-1)

\[
f_u = f_c + \text{ADHB} \cdot f_c \quad \text{(MHz)},
\]

(Eq. 4-2)

\[
BW = f_u - f_l \quad \text{(MHz)},
\]

(Eq. 4-3)

where \( f_l \) is lower bound frequency, \( f_u \) is upper bound frequency, and \( BW \) is bandwidth.

The lower and upper bound frequencies for each amplifier must be individually checked in their respective datasheets when values are not explicitly specified, but the ADHB parameter allows for a rough estimation in the model to prevent an excess of amplifiers from being filtered out for simply not having their bandwidths adequately captured in the SR-CDs. The value used for the ADHB in the given example is 10%.

**Mixer Default Half Bandwidth Percentage**

The “Mixer Default Half Bandwidth %” field gives the designer the ability to specify a bandwidth for RF mixers without specified bandwidths. This field is essentially the same as the “Amplifier Default Half Bandwidth %” field but for RF Mixers as opposed to LNAs and RF Amplifiers. As described in Section 4.2.2, when RF Mixers did not specify a lower and upper bound frequency in component specification tables but instead specified only one frequency, this frequency was recorded into the SR-CD as the lower bound frequency. This lower bound frequency is assumed to be a center frequency \( f_c \) for the mixer. The designer sets a Mixer Default Half Bandwidth (MDHB) just as the ADHB. The MDHB is used to determine the upper and lower bound frequencies mixers without specified values as well as the bandwidth according to

\[
f_l = f_c - \text{MDHB} \cdot f_c \quad \text{(MHz)},
\]

(Eq. 4-4)
\[ f_u = f_c + \text{MDHB} \cdot f_c \] \hspace{1cm} \text{(MHz), and} \hspace{1cm} \text{(Eq. 4-5)}

\[ BW = f_u - f_l \] \hspace{1cm} \text{(MHz).} \hspace{1cm} \text{(Eq. 4-6)}

As with amplifiers, the lower and upper bound frequencies for each mixer must be individually checked in their respective datasheets when values are not explicitly specified, but the MDHB parameter allows for a rough estimation in the model to prevent an excess of mixers from being filtered out for simply not having their bandwidths adequately captured in the SR-CD. The value used for the MDHB in the given example is 10%.

**Antenna Impedance**

The “Antenna Impedance” field is where the user specifies the input impedance of the antenna and entire receiver (assuming no matching circuits). While the antenna is not modeled, this impedance value, given in ohms, is used in the calculation of “RMS Voltage Level at ADC” in the Key System Specification Outputs. The value used for the given example is 50 Ω.

**Antenna Gain**

The “Antenna Gain” field is where the user specifies the assumed gain of the antenna. This value, given in dB, is used only for the calculation of “RMS Voltage Level at ADC.” It is notable that this assumed gain value is not included in the determination of overall receiver gain. The value for the given example is that of a half-wave dipole: 2.15 dB.

**4.3.6. Output System Specifications—SR-TSAM SDR Receiver Specification Results**

Component specification values (only modeled components except where otherwise noted) and the designer inputs described in Sections 4.3.4 and 4.3.5 are used to generate receiver specification outputs. These outputs (designated by yellow cells according to the Model I/O Color Key) in the SR-TSAM are the Key System Specification Outputs. Three categories of outputs exist: (1) Power Characteristics, (2) RF Chain Gain Profile, and (3) Other Notable
Characteristics. Within these three categories are a total of 16 output specifications that are to be described within this section. All output specifications can be seen in Figure 4-17.

<table>
<thead>
<tr>
<th>Key System Specification Outputs</th>
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<tbody>
<tr>
<td>Power Characteristics</td>
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<tr>
<td>Minimum Voltage Level (V)</td>
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<tr>
<td>Maximum Constant Voltage Level (V)</td>
</tr>
<tr>
<td>Power Dissipation (mW) [Excluding FPGA]</td>
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<tr>
<td>RF Chain Gain Profile (From BPF (RF) through RF Amplifier)</td>
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<tr>
<td>Noise Figure (dB)</td>
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<td>Gain (dB)</td>
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<td>Maximum Allowable Signal [MAS] (dBm) [Amp. P1dB]</td>
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<tr>
<td>Minimum Detectable Signal [MDS] (dBm)</td>
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<tr>
<td>Dynamic Range [DR] (dBm) [Single-Tone Dynamic Range]</td>
</tr>
<tr>
<td>RMS Voltage Level at ADC [w/ Antenna] (V)</td>
</tr>
<tr>
<td>Other Notable Characteristics</td>
</tr>
<tr>
<td>Maximum Bandwidth (MHz)</td>
</tr>
<tr>
<td>Minimum Frequency (MHz)</td>
</tr>
<tr>
<td>Maximum Frequency (MHz)</td>
</tr>
<tr>
<td>Component Preference Index</td>
</tr>
<tr>
<td>Manufacturer Preference Index</td>
</tr>
<tr>
<td>Component Price (USD)</td>
</tr>
<tr>
<td>Component Price w/o FPGA (USD)</td>
</tr>
</tbody>
</table>

**Figure 4-17:** Key System Specification Outputs Section of the SR-TSAM

**Minimum Voltage Level**

The first of the three categories within Key System Specification Outputs is Power Characteristics, which includes three overall receiver specification outputs. The first of these output specifications is the “Minimum Voltage Level,” which is the minimum supply voltage, given in volts, required to power the receiver. The Minimum Voltage Level excludes the ADC due to ADC SR-CD limitations, but includes all other powered modeled components. The filters in the receiver are assumed to be passive components. The Minimum Voltage Level is determined by finding the collective maximum voltage supply requirement among the minimum voltage supply levels required by the components according to

\[
V_{S,\text{min}} = \max \{ V_{LNA S,\text{min}}, V_{\text{mixer } S,\text{min}}, V_{\text{Amp } S,\text{min}}, V_{\text{FPGA } S,\text{min}} \} \quad \text{(V)}, \quad \text{(Eq. 4-7)}
\]
where $V_{S_{\text{min}}}$ is the minimum receiver supply voltage and $V_{\text{LNA } S_{\text{min}}}$ is the minimum LNA supply voltage, etc.

In the example provided, the Minimum Voltage Level is 4.5 V, meaning that the supply voltage to the receiver in the FAA land communications example must be at least 4.5 V.

**Maximum Constant Voltage Level**

The second of the three Power Characteristics output specifications is the “Maximum Constant Voltage Level.” The Maximum Constant Voltage Level is the largest constant voltage the receiver could tolerate based on the maximum voltage ratings of the components considered, which includes the same components as those considered for the Minimum Voltage Level. Again, it should be noted that, in the current SR-TSAM version, ADC voltage requirements have not been captured in this field due to SR-CD limitations. The Maximum Constant Voltage Level is determined by finding the collective minimum voltage supply rating among the maximum voltage supply level ratings listed for each considered component according to

$$V_{cS_{\text{min}}} = \max(V_{\text{LNA}_{cS_{\text{max}}}}, V_{\text{mixer}_{cS_{\text{min}}}}, V_{\text{Amp}_{cS_{\text{min}}}}, V_{\text{FPGA}_{cS_{\text{min}}}}) \quad \text{(V)}, \quad \text{(Eq. 4-8)}$$

where $V_{cS_{\text{max}}}$ is the maximum receiver constant supply voltage and $V_{\text{LNA}_{cS_{\text{max}}}}$ is the maximum LNA constant supply voltage, etc.

It is important to note that the SR-TSAM first checks for the presence of the IF Conversion Block as well as the presence of the final RF Amplifier. If either or both of these are missing, they are excluded from (Eq. 4-8) to prevent a return value of 0 V.

It is possible for the Maximum Constant Voltage Level to be less than the Minimum Voltage Level. In such a case, regardless of the designer’s preference regarding a constant voltage level, a constant voltage supply level is not possible since the voltage supply level must be at least that dictated by the Minimum Voltage Level but must not exceed that of the Maximum Constant Voltage Level. Aside from supply voltage compatibility to be described in Section
4.3.10, comparing the Minimum Voltage Level and the Maximum Constant Voltage Level is an indicator to the designer whether a constant voltage level is possible and can be seen as a summary of the voltage supply needs of a particular receiver. The Maximum Constant Voltage Level found in the given example is 3.6 V, which is in fact less than the Minimum Voltage Level of 4.5 V. Therefore, it can be said that the receiver requires at least a 4.5-V supply, and some components will require that this voltage be stepped down.

**Power Dissipation [Excluding FPGA]**

The final output specification of the Power Characteristics is the “Power Dissipation [Excluding FPGA].” This output specification is the total power dissipation, given in mW, of the receiver excluding the FPGA, assuming passive filters and excluding all components not modeled. It is found from the summation of the power dissipation through the LNA, the RF Mixer, the RF Amplifier, and the ADC. To find the power dissipation through the amplifiers and the mixer, which are not directly specified as it is for the ADC, the voltage supply level is multiplied by the maximum current supply specification for each component. The voltage supply level used in the calculation of each component is either done using the minimum voltage supply level specified for each component or using the constant voltage supply level specified in the Key System Design Inputs section if Constant Voltage Level is enabled. The equation for the receiver power dissipation using individual voltage specifications and the equation using one constant voltage level are given by

\[ P = I_{\text{LNA\_max}} V_{\text{LNA\_min}} + I_{\text{Mixer\_min}} V_{\text{Mixer\_min}} + I_{\text{Amp\_max}} V_{\text{Amp\_min}} + P_{\text{ADC\_typ}} \] (mW) and \hspace{1cm} (Eq. 4.9)

\[ P = I_{\text{LNA\_max}} V_{cS} + I_{\text{Mixer\_max}} V_{cS} + I_{\text{Amp\_max}} V_{cS} + P_{\text{ADC\_typ}} \] (mW), \hspace{1cm} (Eq. 4.10)

where \( P \) is the receiver power dissipation in mW, \( I_{\text{LNA\_max}} \) is the maximum LNA current in mA, \( V_{\text{LNA\_max}} \) is the maximum LNA voltage supply level in V, \( P_{\text{ADC\_typ}} \) is the typical ADC power
dissipation in mW, and \( V_{cs} \) is the constant voltage supply level specified in Key System Design Inputs.

In (Eq. 4-9), minimum voltage levels are used under the assumption that when opting not to use a constant voltage supply, the designer will power the components with the minimal voltage level possible. However, in both (Eq. 4-9) and (Eq. 4-10), the maximum specified current level is used. Using the maximum current level ensures a worst-case-scenario calculation. However, it should be noted that sometimes the SR-CDs do not include a maximum current level and only specify one current level, which is placed into the minimum current level column by default. In these cases, the SR-TSAM detects the missing specification and instead uses the minimum current level.

It should be further noted that, in the absence of the IF Conversion Block and/or in the absence of the final RF Amplifier, the power dissipation through the missing components is 0 W and, as such, preserves the integrity of the power dissipation calculation.

In a true SDR system, the FPGA makes up of a major portion of receiver power dissipation. In fact, for many radio systems it may double power dissipation. However, FPGA power dissipation varies greatly based on the quantity and complexity of the activities it is programmed to handle. In fact, some manufacturer-provided tools exist to estimate the power consumption of various FPGA product families based on detailed user inputs regarding software resource needs [Altera Corporation, 2010]. Given that this is a highly variable value yet such a large percentage of total power dissipation, excessive assumptions and estimation threatens to destroy the usefulness of the number calculated according to either (Eq. 4-9) or (Eq. 4-10). The calculated power dissipation in the “Power Dissipation [Excluding FPGA]” field is not necessarily to reflect true power consumption of the receiver but is instead intended to enable relative, trade-space decisions and analysis. Including an unknown estimated power dissipation value for the FPGA that could potentially double the total power dissipation value could prevent
the relative relationships between other components from being usefully visualized. Therefore, in future SR-TSAM versions, a separate FPGA analysis should be built in. This future FPGA model should include an analysis of what will be required of the FPGA general enough to allow decision flexibility, but restrictive enough to further determine FPGA compatibility and enable power analysis. As mentioned, several tools (Excel-based) exist from FPGA vendors for various product families that allow for detailed FPGA power dissipation analysis [Altera Corporation, 2010].

In the example provided the power dissipation is found to be about 1.3 W.

**Noise Figure**

The second of the three categories within Key System Specification Outputs is RF Chain Gain Profile (from BPF (RF) through RF Amplifier), which includes six overall receiver specification outputs related to the gain, noise, and sensitivity characteristics of the receiver. The first of these output specifications is the “Noise Figure”. The “Noise Figure” output field reports the noise figure of the RF front-end including the BPF (RF), LNA, RF Mixer, BPF (IF), and RF Amplifier. The total noise figure is determined from a cascaded calculation of the individual component noise figures for each component according to the equations introduced in Section 3.1.6 according to (Eq. 3-20), (Eq. 3-21), and (Eq. 3-22). The resulting implemented calculation is

\[ F_{BPF(RF)} = 10^{NF_{BPF(RF)} / 10} , \quad F_{LNA} = 10^{NF_{LNA} / 10} , \quad \text{etc.} , \quad (\text{Eq. 4-11}) \]

\[ F_{\text{total}} = F_{BPF(RF)} + \frac{F_{LNA} - 1}{G_{BPF(RF)} G_{LNA}} + \frac{F_{\text{Mixer}} - 1}{G_{BPF(RF)} G_{LNA} G_{\text{Mixer}}} + \frac{F_{\text{BPF(IF)}} - 1}{G_{BPF(RF)} G_{LNA} G_{\text{Mixer}} G_{\text{BPF(IF)}}} , \quad \text{and} \quad (\text{Eq. 4-12}) \]

\[ NF_{\text{total}} = 10 \log(F_{\text{total}}) \quad (\text{dB}) , \quad (\text{Eq. 4-13}) \]

where \( F_{BPF(RF)} \) is the noise factor of the BPF (RF) component and \( G_{BPF(RF)} \) is the linear gain of the BPF (RF) component, etc.
It is $NF_{total}$ that is reported in the “Noise Figure” output field. An important note is that, for passive components without a specified noise figure or gain (the two BPFs), the insertion loss is used for the specified noise figure. In the case of filters missing insertion loss values (a NaN value is in the SR-CD insertion loss field), the value from the “Assumed Filter Insertion Loss if Missing” input field is taken as the insertion loss. Furthermore, in the absence of the IF Conversion Block and/or the final RF Amplifier, the calculations in (Eq. 4-11), (Eq. 4-12), and (Eq. 4-13) still hold since the field for an empty component in the SR-CDs contain the necessary 0s to prevent empty components from impacting the overall calculation (the linear equivalent of 0-dB values listed for component noise figures and gains is 1).

In the example provided, the overall noise figure is found to be 2.27 dB.

**Gain**

The second RF Chain Gain Profile output specification is the “Gain” output field, which specifies the overall gain, in dB, of the RF front-end of the receiver. This value is simply the summation of the gain of each modeled component in the RF front-end of the receiver. The insertion loss of passive components is simply treated as negative gain. Since the SR-CDs specify gain and insertion loss values in dB, a simple summation captures the overall gain as given by

$$G_{total} = -L_{BPF(RF)} + G_{LNA} + G_{Mixer} - L_{BPF(IF)} + G_{Amp} \text{ (dB)},$$

(Eq. 4-14)

where $G$ is logarithmic gain in dB and $L$ is logarithmic insertion loss in dB.

If insertion loss values are not specified in the BPF SR-CD for a selected filter, again the “Assumed Filter Insertion Loss if Missing” input field value is used. Any components left empty as a result of the IF Conversion Block and/or final RF Amplifier being left out of a design will have 0-dB insertion loss values or 0-dB gain values, thereby not affecting the use of (Eq. 4-14) for the determination of overall RF front-end gain. It should be noted that, while the user has the ability to specify an assumed antenna gain in the Key System Design Inputs section, this gain is
not used in determining the overall RF front-end gain. This is to focus ATSV-visualization on known values.

In the example provided, the overall gain is found to be 54.86 dB.

**Maximum Allowable Signal [MAS] [Amp. P1dB]**

The third RF Chain Gain Profile output specification field is the “Maximum Allowable Signal [MAS] [Amp. P1dB].” This field gives an estimate of the maximum allowable signal (MAS) in dBm for the RF front-end of the SDR receiver. This is the upper bound frequency used in the determination of the receiver’s dynamic range (DR). As discussed in Section 3.1.4, there are numerous ways in which MAS can be defined and determined. MAS can be driven by intermodulation distortion (IMD) considerations as well as ADC clipping.

The selected definition of MAS for this version of the SR-TSAM is that which follows the single-tone dynamic range definition that essentially defines MAS as the overall P1dB (first-order intermodulation intercept point) of the RF front-end of the receiver. According to this definition, MAS is the maximum signal level that the RF chain can receive while maintaining linear operation. For this particular field, only the LNA and RF Amplifier (should one exist in a given design) are considered. Therefore, the total MAS is the maximum signal level the receiver can receive and maintain linear gain in the amplifiers. This value is determined by cascading the OP1dB (output P1dB points, which are assumed to be the specified P1dB values in the SR-CDs for the amplifiers) using the cascading method for a system total OIP3 (output third-order intermodulation intercept point), according to the assumptions and equations elaborated upon in Section 3.1.3. The equation used for this calculation is

\[
\text{MAS} = \text{OP1dB}_{\text{total}} = \left( \frac{1}{\text{OP1dB}_{\text{LNA(linear)}} + \text{OP1dB}_{\text{Amp(linear)}}} \right) \text{ (dBm), (Eq. 4-15)}
\]
where \( \text{OP1dB}_{\text{LNA}} \) is the OP1dB of the LNA in linear form and \( g_{\text{Amp}} \) is the gain for the RF Amplifier in linear form. If a final RF Amplifier is not included in a design, then MAS is simply set to the value of \( \text{OP1dB}_{\text{LNA}} \) and (Eq. 4-15) is not used.

A major assumption used in the calculation of MAS using (Eq. 4-15) is that only the amplifiers affect MAS, which is not necessarily the case. Essentially, all other components (particularly the RF Mixer) have been assumed to have an infinite OP1dB value, thereby removing their influence on the overall calculation. Therefore, (Eq. 4-15) could be expressed with all OP1dB values, but the fractions within the denominator containing OP1dB values set at infinity will simply tend to 0, thereby not influencing the overall calculation.

Another major assumption used in the calculation of MAS using (Eq. 4-15) is that cascading OP1dB values works the same as cascading OIP3 values, which is an assumption explained previously in Section 3.1.3.

The MAS found in the example provided is 8.99 dBm.

**Minimum Detectable Signal [MDS]**

The fourth RF Chain Gain Profile output specification field is the “Minimum Detectable Signal [MDS].” This field gives the minimum detectable signal (MDS), given in dBm, which is the minimum signal that can be effectively captured by the receiver system. The MDS depends on the noise figure of the system, the bandwidth of the signal, the minimum SNR required at the ADC input, the system noise temperature, and the Boltzmann constant. The MDS is determined from these things according to the equations described by (Eq. 3-15) and (Eq. 3-16) in Section 3.1.4. Therefore, the MDS output field is found according to

\[
\text{MDS} = 10 \log \left( \frac{k_B \cdot T \cdot BW}{0.001} \right) - NF_{\text{total}} - \text{SNR}_{\text{min}} \quad \text{(dBm)}. \quad (\text{Eq. 4-16})
\]

A critical value and assumption in determination of overall MDS from (Eq. 4-16) is that the minimum SNR at the input of ADC (\( \text{SNR}_{\text{min}} \)) required for successful A/D conversion is that
specified in the Key Signal Inputs section in the input field “Minimum SNR Required at ADC” as described in Section 4.3.4.

The bandwidth ($BW$) used for (Eq. 4-16) is the result of the “Maximum Bandwidth” field under the Other Notable Characteristics subsection of the Key System Specification Outputs section to be discussed in more detail within this section.

For this SR-TSAM, the noise temperature ($T$) is assumed to be at room temperature ($T = T_0$), which thereby sets the temperature to 290 K. Furthermore, for reference, the Boltzmann constant is $k_B = 1.38 \times 10^{-23}$ J/K.

In the example provided, the MDS was found to be −107.17 dBm.

**Dynamic Range [DR] [Single-Tone Dynamic Range]**

The fifth RF Chain Gain Profile output specification field is the “Dynamic Range [DR] [Single-Tone Dynamic Range].” This field gives the range of signals, in dBm, that the RF front-end is capable of detecting and passing to the ADC. Like MAS, DR can be defined numerous ways, but as already highlighted, the single-tone dynamic range has been selected. Therefore, the MAS calculated in the “Maximum Allowable Signal [MAS] [Amp. P1dB]” field is taken as the absolute MAS. DR is then calculated using MDS according to

$$\text{DR} = \text{MAS} - \text{MDS} \quad (\text{dBm}).$$  \hspace{1cm} (Eq. 4-17)

The DR found in the example provided is 116.16 dBm.

**RMS Voltage Level at ADC [w/ Antenna]**

The sixth and final RF Chain Gain Profile output specification field is the “RMS Voltage Level at ADC [w/ Antenna].” This field gives an approximate value for the RMS voltage level of the signal at the input of the ADC from the RF front-end if a signal at the MDS level were to be received at the antenna. Unlike the other fields in the RF Chain Gain Profile, this calculation includes the use of the assumed antenna characteristics (gain and impedance) specified by the designer in the Key System Design Inputs section of the SR-TSAM.
This calculation uses an important equation that relates received dBm values to actual signal voltages within a receiver system,

\[ P = 10 \log \left( \frac{V^2}{R \cdot p_0} \right) \text{ (dBm)}, \]  

(Eq. 4-18)

where \( P \) is the power level in dBm, \( V \) is the RMS voltage in V, \( R \) is the load impedance in \( \Omega \), and \( p_0 \) is the reference power (1 mW for dBm) [“Reference Designer Calculators,” 2009]. The RMS Voltage Level at ADC is determined using the smallest detectable signal (MDS) as an assumed receiver input and calculates the voltage this signal would translate to after passing through the entire RF front-end. The signal will be boosted by the gain of the system (including the antenna), and hence is determined as such. The equation used for the determination of this field is derived from (Eq. 4-18) and the receiver gain considerations and is

\[ V = \sqrt{10^{\left( MDS + G_{\text{total}} + G_{\text{antenna}} \right)/10}} \cdot R \cdot 1\text{mW} \text{ (V)}, \]  

(Eq. 4-19)

where MDS is the minimum detectable signal in dBm, \( G_{\text{total}} \) is the total receiver gain in dB calculated earlier, \( G_{\text{antenna}} \) is the assumed antenna gain in dB, \( R \) is the load impedance in \( \Omega \), and \( V \) is the RMS voltage in V. The load impedance \( (R) \) is specified in the “Antenna Impedance [for Voltage Level @ ADC]” field in the Key System Design Inputs and the antenna gain \( (G_{\text{antenna}}) \) is specified in the same section in the “Antenna Gain [for Voltage Level @ ADC]” field.

The resulting RMS voltage can be compared to the ADC input voltage range to determine true compatibility with the ADC in a given design; however, this is not automatically checked in the current SR-TSAM version due to SR-CD limitations and prohibitive assumptions.

**Maximum Bandwidth**

The third and final of the three categories within Key System Specification Outputs is Other Notable Characteristics, which includes seven overall receiver specification outputs. The first of these output specifications is the “Maximum Bandwidth” field. This field specifies the
bandwidth of the signal allowed to pass from the RF front-end analog RF/IF stages and through the ADC into the digital realm. Therefore, this field represents the maximum bandwidth that the receiver can draw signals from within the digital domain. In a feasible design that satisfies the compatibility criteria laid out in Sections 4.3.8 and 4.3.9, this bandwidth should be at least as much as the designer-specified bandwidth requirement provided in the Key Signal Inputs section. The Maximum Bandwidth, given in MHz, is calculated from the values given in “Maximum Frequency” and “Minimum Frequency” output fields to be further addressed within this section along with the ADC sampling rate according to

\[
BW_{\text{max}} = \min \left( \left[ f_{\text{max}} - f_{\text{min}} \right] \left[ \frac{f_s}{\text{SRF}} \right] \right) \text{ (MHz)},
\]

(Eq. 4-20)

where \(f_s\) is the sampling rate of the ADC (Msps) and SRF is the sampling rate factor (at least 2 for the Nyquist criterion). Either the input frequency range \(\left[ f_{\text{max}} - f_{\text{min}} \right]\) or the ADC sampling rate and sampling rate factor \(\left[ f_s/\text{SRF} \right] \) may be the limiting factor in determining maximum bandwidth. In certain configurations (such as in the absence of the IF Conversion Block with sub-sampling disallowed), these values may match based on the manner in which the “Maximum Frequency” field is calculated, which is further addressed later within this section.

It should be noted that, if a design is found to be infeasible as per compatibility determination fields, the maximum bandwidth is not calculated and instead “N/A” is returned. The maximum bandwidth found in the given example is 80 MHz, which indeed exceeds the required minimum of 12 MHz.

**Minimum Frequency**

The second output specification of the Other Notable Characteristics category is the “Minimum Frequency” field. Given in MHz, this field represents the lowest frequency that is passed through the RF front-end and through the ADC. The number is calculated from the lower bound frequencies of relevant modeled components. When lower bound frequencies are not
specified, bandwidths are used where given and when bandwidths are not explicitly given, bandwidths calculated from the specified ADHB/MDHB values are used. In such a case, half of the total bandwidth is subtracted from the specified center frequency to obtain the component’s lower bound frequency. The lower bound frequency (the minimum frequency) for each individual component is identified and then the overall maximum of the lower bound frequencies is taken as the output of the “Minimum Frequency” field. The relevant components used in this calculation differ based the existence or non-existence of the IF Conversion Block. If the IF Conversion Block is used, the RF Mixer must be included in the analysis, but the BPF (IF) and final RF Amplifier are not considered since they are at IF and have no relevance to the incoming RF signal. However, if the IF Conversion Block is excluded, the RF Mixer and BPF (IF) do not even exist, but the RF Amplifier is considered since it is now at RF. When an IF Conversion Block is used, the minimum frequency is found according to
\[
 f_{\text{min}} = \max\left(f_{\text{BPF(RF)min}}, f_{\text{LNA min}}, f_{\text{Mixer min}}\right) \text{ (MHz).} \quad (\text{Eq. 4-21})
\]
When an IF Conversion Block is not used, the minimum frequency is found according to
\[
 f_{\text{min}} = \max\left(f_{\text{BPF(RF)min}}, f_{\text{LNA min}}, f_{\text{Amp min}}\right) \text{ (MHz).} \quad (\text{Eq. 4-22})
\]
It should be noted that in both (Eq. 4-21) and (Eq. 4-22), \( f_{\text{Amp min}} \) is excluded if the RF Amplifier is left empty. It should also be noted that, if a design is found to be infeasible as per compatibility determination fields, the minimum frequency is not calculated and instead “N/A” is returned. Therefore, it should also be noted that the ADC sampling rate is not considered since the design must be compatible for this calculation to occur. If a design is compatible, the sampling rate of the ADC must satisfy requirements. The ADC sampling rate will be considered for the “Maximum Frequency” field.

The minimum frequency found for the example provided is 120 MHz.
**Maximum Frequency**

The third output specification of the Other Notable Characteristics category is the “Maximum Frequency” field. Given in MHz, this field represents the highest frequency that is passed through the RF front-end and through ADC. The number is calculated from the upper bound frequencies of relevant modeled components. When upper bound frequencies are not specified (sometimes the case with amplifiers and always the case with the RF Mixer) bandwidths are used where given and when bandwidths are not explicitly given, bandwidths calculated from the specified ADHB/MDHB values are used. In such a case, half of the total bandwidth is added to the specified center frequency to obtain the component’s upper bound frequency. The upper bound frequency (the maximum frequency) for each individual component is identified, and then the overall minimum of the upper bound frequencies is taken as the output of the “Maximum Frequency” field. The relevant components used in this calculation differ based the existence of non-existence of the IF Conversion Block. If the IF Conversion Block is used, the RF Mixer must be included in the analysis, but the BPF (IF), final RF Amplifier, and ADC are not considered since they are at IF and have no relevance to the incoming RF signal. However, if the IF Conversion Block is excluded, then the RF Mixer and BPF (IF) do not even exist, but the RF Amplifier is considered since it is now at RF and so is the ADC. However, the ADC is only considered as a possible frequency limiter when sub-sampling is not allowed. When an IF Conversion Block is used, the maximum frequency is found according to

\[
f_{\text{max}} = \min (f_{\text{BPF(RF) max}}, f_{\text{LNA max}}, f_{\text{Mixer max}}) \quad (\text{MHz}). \tag{Eq. 4-23}
\]

When an IF Conversion Block is not used and ADC sub-sampling is not allowed, the maximum frequency is found according to

\[
f_{\text{max}} = \min \left( f_{\text{BPF(RF) max}}, f_{\text{LNA max}}, f_{\text{Amp max}}, \left[ \frac{f_s}{\text{SRF}} \right] \right) \quad (\text{MHz}), \tag{Eq. 4-24}
\]
where \( f_s \) is the sampling rate of the ADC (Msps) and SRF is the sampling rate factor. It should be noted that, in (Eq. 4-22), \( f_{\text{Amp,\text{max}}} \) is excluded if the RF Amplifier is left empty and \([f_s/SRF]\) is excluded if ADC sub-sampling is enabled. It should also be noted that if a design is found to be infeasible as per compatibility determination fields, the maximum frequency is not calculated and instead “N/A” is returned.

The maximum frequency found for the given example is 210 MHz. For the FAA land communications example provided, the designer specified that a center frequency of 168 MHz needed to be detected with a bandwidth of 12 MHz; therefore, the lower and upper bound frequencies needed to be at most 162 MHz and at least 174 MHz, respectively. As highlighted in Section 4.3.8, it can be easily seen that the example design, which facilitates signal detection between 120 MHz and 210 MHz, successfully meets the design objectives.

**Component Preference Index**

The fourth output specification of the Other Notable Characteristics category is the “Component Preference Index” field. This field gives an overall component preference index value for the whole receiver based on the individual component values for component preference. For the meaning of Component Preference, the “Manufacturer and Component Preference” subsection of Section 4.2.2 should be referenced. The overall component preference index is simply an average of the component preference values of each individual component. Therefore, the overall component preference index value will be a value from 0–5 indicating some degree of preference. If the IF Conversion Block and/or the final RF Amplifier are omitted from the design, they are omitted from the average. The component preference index for the example provided is 0.

**Manufacturer Preference Index**

The fifth output specification of the Other Notable Characteristics category is the “Manufacturer Preference Index” field. This field gives an overall manufacturer preference index
value for the whole receiver based on the individual component values for manufacturer preference. For the meaning of Manufacturer Preference, the “Manufacturer and Component Preference” subsection of Section 4.2.2 should be referenced. The overall manufacturer preference index is simply an average of the manufacturer preference values of each individual component. Therefore, the overall manufacturer preference index value will be a value from 0–5 indicating some degree of preference. If the IF Conversion Block and/or the final RF Amplifier are omitted from the design, they are omitted from the average. The manufacturer preference index for the example provided is 0.

**Component Price**

The sixth output specification of the Other Notable Characteristics category is the “Component Price” field. This field gives the total price in USD (United States Dollars) for all of the selected components. It is determined simply for the summation of all component costs specified in the SR-CDs. When costs are not listed in the SR-CDs and NaN values exist, the price for the design is set to $0.00 (to be filtered out of the trade space with bounds set in ATSV). This is to avoid any errors in reporting price and is further commented on in Section 5.2.2 as well as in Section 6.2. When components are left empty (when the IF Conversion Block and/or final RF Amplifier are omitted), the corresponding prices in the SR-CDs is 0, thereby maintaining the integrity of a simple summation. The prices in the “Component Price” field may not necessarily reflect the pricing available to the designer. Exact pricing may differ based on sourcing channels and quantities. The prices in the SR-CDs are taken from consumer-available price listings and generally using quantities at 1,000 components. Therefore, like many output fields, the “Component Price” field is useful for highlighting trends for visualization as opposed to precise values. The “Component Price” field can highlight low and high cost trends and tradeoffs associated with various design decisions such as the use of high performance, high speed ADCs
to facilitate the elimination of IF Conversion Block components. The cost of the receiver in the example provided is $150.75.

**Component Price without FPGA**

The seventh and final output specification of the Other Notable Characteristics category, and the final output of the Key System Specification Outputs section of the SR-TSAM is the “Component Price w/o FPGA” field. This field gives the total price in USD (United States Dollars) for all of the selected components without the price of the FPGA included. Given the dynamic cost of FPGAs and the fact that FPGAs are handled somewhat individually in the SR-TSAM (they are not heavily considered in compatibility determination or in output specification calculations, but are instead given visualization links to ATSV), it is useful to consider the receiver price without the FPGA cost included. This allows the designer to focus on the cost trends associated with the decisions made on the components that are more interdependent in the SR-TSAM. The cost of the receiver in the example provided without the FPGA is $132.50.

### 4.3.7. Component Compatibility Determination—SR-TSAM Feasibility Filter

A critical function of the SR-TSAM is to determine feasible receiver designs based on basic compatibility criteria applied to sampled input components. While a very large number of SDR receiver designs can be generated randomly by sampling the “Database Component Number” for each component in the receiver architecture, only a fraction of randomly generated designs are actually feasible. Visualizing the trade space of SDR receiver design is only of value if the trade space is comprised of mostly feasible designs. While the current proof-of-concept version of the SR-TSAM does not guarantee truly feasible designs 100% of the time due to a relatively limited feasibility determination scope, some of the most fundamental compatibility checks are implemented to significantly reduce the number of infeasible designs. The
fundamental compatibility determination fields include frequency compatibility, bandwidth compatibility, and voltage supply compatibility. The current version of the SR-TSAM ensures that components are compatible with the designer’s inputs in terms of the frequency of the input signal, the bandwidth of the input signal, and the available power supply. Figure 4-18 displays the Component Compatibility Determination section of the SR-TSAM shown in two figures that in reality stretch across the same rows as shown in Appendix B in Figure B-1 (in other words, the bottom image in Figure 4-18 is simply the continuation of the top image).

<table>
<thead>
<tr>
<th>System Component</th>
<th>Antenna</th>
<th>BPF (RF)</th>
<th>LNA</th>
<th>RF Mixer</th>
</tr>
</thead>
<tbody>
<tr>
<td>Database Component Number</td>
<td>NOT MODELED</td>
<td>51</td>
<td>10</td>
<td>16</td>
</tr>
<tr>
<td>Manufacturer</td>
<td></td>
<td>Mini-Circuits</td>
<td>Avago Technologies</td>
<td>Texas Instruments</td>
</tr>
<tr>
<td>Part Number</td>
<td></td>
<td>RBP-160+</td>
<td>MGA-68563-1LKG</td>
<td>SN76188PIWRG4</td>
</tr>
<tr>
<td>Frequency Compatibility</td>
<td>NOT MODELED</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>Bandwidth Compatibility</td>
<td>NOT MODELED</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>Voltage Supply Compatibility</td>
<td>NOT MODELED</td>
<td>N/A</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>Basic Compatibility</td>
<td>NOT MODELED</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>Analog IF Conversion Basic Presence</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>Component Compatibility</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Figure 4-18: The Component Compatibility Determination Section of the SR-TSAM

The Component Compatibility Determination section has ten rows as seen in Figure 4-18 with example inputs based on the FAA land communications example. The first row defines the columns for the section: each component has a column. The RF stage components (antenna, BPF (RF), LNA, and sometimes RF amplifier and ADC) are represented with orange coloring, the IF stage components (RF mixer, LO, BPF (IF), and sometimes RF amplifier, ADC, and FPGA) are
represented with gold coloring, and the BB stage components (FPGA and DSP) are represented with green coloring.

The second, third, and fourth rows of the Component Compatibility Determination section simply summarize some of the fields from the Component Inputs section of the SR-TSAM to give an easily-accessible view of the current sampled design. The component fields summarized include Database Component Number, Manufacturer, and Part Number.

The fifth, sixth, and seventh rows of the Component Compatibility Determination section consist of the fundamental basic compatibility checks for each component: Frequency Compatibility, Bandwidth Compatibility, and Voltage Supply Compatibility. Each cell in these rows contains formulas for determining the compatibility of each component against the Key Signal Inputs and Key System Design Inputs specified by the user. The results of the compatibility checks are given as either a value of 1, 0, or 99 according to the compatibility key shown in the following figure:

<table>
<thead>
<tr>
<th>Compatibility Key</th>
<th>1 - Compatible</th>
<th>0 - Not Compatible</th>
<th>99 - N/A (Excluded)</th>
</tr>
</thead>
</table>

**Figure 4-19:** Compatibility Key for the SR-TSAM

As shown in Figure 4-19, a value of 1 indicates that the component of interest is compatible in the given field (either frequency, bandwidth, or voltage supply), a value of 0 indicates incompatibility, and a value of 99 indicates that the component has simply been excluded (i.e., the IF Conversion Block components set to [EMPTY] using Database Component Number 0). Only modeled and sampled components with SR-CDs are checked and, therefore, the antenna, the LO, and the DSP are not checked for compatibility.

The eighth row of the Component Compatibility Determination Section is used for the field “Basic Compatibility”, which summarizes the compatibility fields in the latter three rows. For each component, the results of the three compatibility checks (frequency, bandwidth, and
voltage supply) are checked. If all three compatibility checks result in a 1 (compatible), then the
“Basic Compatibility” field reports a 1 (compatibility) for the component, which represents
overall compatibility. If a component is excluded from the design, its basic overall compatibility
is simply reported as a 1 (compatible). If, however, a component is included and at least one of
its compatibility checks reports a 0 (incompatibility), then the “Basic Compatibility” field reports
a 0 (incompatibility) for the component, thereby representing overall incompatibility. It should
be noted that some compatibility checks are not implemented for certain components (for
example, the Voltage Supply compatibility check is not applied to either of the BPF components
because it does not apply). In these cases the “Basic Compatibility” field simply ignores these
compatibility checks (for example, the basic overall compatibility for BPF components depends
only upon the results of the frequency and bandwidth compatibility checks).

The ninth row of the Component Compatibility Determination section, the “Analog IF
Conversion Block Presence” field, captures the existence or non-existence of the IF Conversion
Block in one entry thereby capturing whether or not a design leverages an analog IF stage. This
field, which is explained in Section 4.3.11, can either be a value of 1 (indicating the existence of
the IF Conversion Block), 0 (indicating some incompatibility resulting from only a portion of the
IF Conversion Block existing), or 99 (indicating the non-existence of the IF Conversion Block).

Finally, the tenth row of the Component Compatibility Determination section is the
“Component Compatibility” field, which, like the previous field, contains only one value. This
field summarizes the overall component-based compatibility of the entire SDR receiver design. If
all modeled components have their “Basic Compatibility” fields set to 1 and the “Analog IF
Conversion Block Presence” field is either a value of 1 or 99, then the “Component
Compatibility” field is set to 1, thereby indicating complete overall design compatibility. For any
other case, the field is set to 0, thereby indicating complete overall design incompatibility. It is
using this final field, that, using ATSV, the designer will be able to filter out all incompatible designs from the trade space of interest.

Sections 4.3.8–4.3.10 elaborate upon the compatibility checks for each component. Section 4.3.11 explains the “Analog IF Conversion Block Presence” field in more detail that this section has.

4.3.8. Frequency Compatibility Determination

The first of the compatibility checks applied to each component of a sampled SDR receiver design is frequency. Each modeled component is checked for compatibility with the Key Signal Inputs and Key System Design Inputs specified by the designer. The specifications called from the SR-CDs and listed in the Component Inputs section are referenced for these checks. This section serves to briefly explain the checks conducted for each component.

BPF (RF) Frequency Compatibility Determination

Within this field, the input signal frequency specified by the designer in the “Frequency” field of the Key Signal Inputs section is checked against the frequency range of the RF stage band-pass filter. The frequency range for the BPF (RF) is determined by adding and subtracting half of the specified BPF bandwidth to the specified BPF center frequency. If the input signal frequency falls within the frequency range of the BPF, this compatibility field is set to a value of 1 (compatible). Otherwise, the field is set to a value of 0 (incompatible).

LNA Frequency Compatibility Determination

Within this field, the input signal frequency specified by the designer is checked against the frequency range of the LNA. For some LNAs, a lower bound and upper bound frequency are specified while for others only a center frequency is specified in the lower bound frequency specification field from the SR-CD. When only a center frequency is given, the lower and upper
bound frequencies for the LNA are determined using the ADHB value specified in the Key System Design Inputs section according to Reference source not found.—Error!

Reference source not found. If the input signal frequency falls within the frequency range of the LNA, this compatibility field is set to a value of 1 (compatible). Otherwise, the field is set to a value of 0 (incompatible).

RF Mixer Frequency Compatibility Determination

Within this field, the input signal frequency specified by the designer is checked against the frequency range of the RF Mixer. For some RF Mixers, a lower bound and upper bound frequency are specified while for others only a center frequency is specified in the lower bound frequency specification field from the SR-CD. When only a center frequency is given, the lower and upper bound frequencies for the RF Mixer are determined using the MDHB value specified in the Key System Design Inputs section according to (Eq. 4-4)–(Eq. 4-6). If the input signal frequency falls within the frequency range of the RF Mixer, this compatibility field is set to a value of 1 (compatible). Otherwise, the field is set to a value of 0 (incompatible). If the RF Mixer is excluded from the design and its Database Component Number is set to 0, this compatibility field will be set to 99 to indicate its exclusion.

It is notable that the current SR-TSAM version does not include a compatibility check regarding the ability for an RF mixer to be capable of outputting the specified intermediate frequency in the Key System Design Inputs section. All RF mixers are currently assumed compatible with any output IF.

BPF (IF) Frequency Compatibility Determination

Within this field, the intermediate frequency specified by the designer in the “IF Frequency” field of the Key System Design Inputs section is checked against the frequency range of the IF stage band-pass filter. The frequency range for the BPF (IF) is determined by adding and subtracting half of the specified BPF bandwidth to the specified BPF center frequency. If the
specified IF falls within the frequency range of the BPF, this compatibility field is set to a value of 1 (compatible). Otherwise, the field is set to a value of 0 (incompatible). If the BPF (IF) is excluded from the design and its Database Component Number is set to 0, this compatibility field will be set to 99 to indicate its exclusion.

**RF Amplifier Frequency Compatibility Determination**

Within this field it is first determined if the RF Amplifier is part of the RF stage or the IF stage. If there is no RF Mixer in the design, then it can be assumed that no analog IF section will exist in the design. Under this circumstance, within this compatibility field the input signal frequency specified by the designer in the “Frequency” field of the Key Signal Inputs section is checked against the frequency range of the RF Amplifier. If, however, an RF Mixer is present in the design and an analog IF section therefore exists, it is the intermediate frequency specified by the designer in the “IF Frequency” field of the Key System Design Inputs section that is checked against the frequency range of the RF Amplifier.

Depending on the presence of an RF Mixer, either the RF input signal frequency or the intermediate frequency specified by the designer is checked against the frequency range of the RF Amplifier. For some RF Amplifiers, a lower bound and upper bound frequency are specified while for others only a center frequency is specified in the lower bound frequency specification field from the SR-CD. When only a center frequency is given, the lower and upper bound frequencies for the LNA are determined using the ADHB value specified in the Key System Design Inputs section according to \[ \text{Error! Reference source not found.-Error! Reference source not found.} \]. If the signal frequency of interest (either RF or IF) falls within the frequency range of the RF Amplifier, this compatibility field is set to a value of 1 (compatible). Otherwise, the field is set to a value of 0 (incompatible). If the RF Amplifier is excluded from the design and its Database Component Number is set to 0, this compatibility field will be set to 99 to indicate its exclusion.
ADC Frequency Compatibility Determination

Within this field the ADC sampling rate is checked against either the RF input signal frequency or the intermediate frequency if sub-sampling is not allowed. In the current SR-TSAM version, if sub-sampling is enabled by the designer in the Key System Design Inputs, then it is assumed that any ADC with any sampling rate is compatible with any RF input signal frequency or any intermediate frequency. Therefore, if sub-sampling is enabled this compatibility field is simply set to 1 indicating frequency compatibility of the ADC. This assumption must be revisited and refined in future versions of the SR-TSAM. If sub-sampling is not enabled, then the sampling rate must be checked against the frequency of the signal input to the ADC.

If there is no RF Mixer in the design, then it can be assumed that no analog IF section exists in the design. Under this circumstance, within this compatibility field the input signal frequency specified by the designer in the “Frequency” field of the Key Signal Inputs section is checked against the sampling rate of the ADC. If, however, an RF Mixer is present in the design and an analog IF section therefore exists, then it is the intermediate frequency specified by the designer in the “IF Frequency” field of the Key System Design Inputs section that is checked against the sampling rate of the ADC.

Depending on the presence of an RF Mixer, either the RF input signal frequency or the intermediate frequency specified by the designer is checked against the sampling rate of the ADC. In order for the ADC to be deemed compatible within this frequency compatibility field, the ADC sampling rate must be at least the value of either the RF input signal frequency or the intermediate frequency (depending upon the existence of the IF Conversion Block) multiplied by the sampling rate factor specified in the “Sampling Rate Factor” field in the Key System Design Inputs section. For example, in the given FAA land communications example, for the ADC to be deemed compatible when sub-sampling is disabled, the sampling rate must be at least 70 MHz (the specified intermediate frequency) multiplied by 2.5 (the specified sampling rate factor);
therefore, the required sampling rate of the ADC is at least 175 Msps. If the ADC sampling rate is found to meet this compatibility requirement, then this compatibility field is set to a value of 1 (compatible). Otherwise, the compatibility field is set to a value of 0 (incompatible).

**FPGA Frequency Compatibility Determination**

No frequency compatibility analysis is conducted for the FPGA in the current version of the SR-TSAM.

### 4.3.9. Bandwidth Compatibility Determination

The second of the compatibility checks applied to each component of a sampled SDR receiver design is regarding bandwidth. This section serves to briefly explain the checks conducted for each component.

**BPF (RF) Bandwidth Compatibility Determination**

This compatibility field functions similarly to the “BPF (RF) Frequency Compatibility Determination” field described in the Section 4.3.8. However, rather than checking that the RF input signal center frequency is contained within the frequency range of the BPF (RF), the entire input signal is checked to ensure it is fully within the BPF (RF) frequency range. To make this determination, a lower bound and upper bound frequency for the RF input signal are determined according to

\[
\begin{align*}
  f_u &= f_c + \frac{BW}{2} \quad \text{(MHz)} \quad \text{(Eq. 4-25)} \\
  f_l &= f_c - \frac{BW}{2} \quad \text{(MHz)}, \quad \text{(Eq. 4-26)}
\end{align*}
\]

where \(f_u\) is the upper bound RF input frequency, \(f_c\) is the specified RF input center frequency, \(BW\) is the specified RF input signal bandwidth, and \(f_l\) is the lower bound RF input frequency.
If the entire RF input signal, as bounded by (Eq. 4-25) and (Eq. 4-26), is within the frequency range of the BPF (RF), this compatibility field is set to a value of 1 (compatible). Otherwise, the field is set to a value of 0 (incompatible). It should be noted that if this bandwidth compatibility field is found to be compatible, the frequency compatibility field will also be compatible; however, given that the opposite is not true it is still useful to have separate fields so that a designer may recognize when a center frequency falls within the frequency bounds of the component, but the bandwidth exceeds the range. This is also true for the LNA, RF Mixer, BPF (IF) and RF Amplifier.

**LNA Frequency Bandwidth Determination**

This compatibility field functions similarly to the “LNA Frequency Compatibility Determination” field described in the Section 4.3.8. However, rather than checking that the RF input signal center frequency is contained within the frequency range of the LNA, the entire input signal is checked to ensure it is fully within the LNA frequency range. This is checked using the upper and lower bound frequencies of the RF input signal found using (Eq. 4-25) and (Eq. 4-26). If the entire input signal frequency falls within the frequency range of the LNA, this compatibility field is set to a value of 1 (compatible). Otherwise, the field is set to a value of 0 (incompatible).

**RF Mixer Frequency Bandwidth Determination**

Again, as with the previous three fields, this compatibility field functions similarly to its counterpart in Section 4.3.8, the “RF Mixer Frequency Compatibility Determination” field. However, rather than checking that the RF input signal center frequency is contained within the frequency range of the RF Mixer, the entire input signal is checked to ensure it is fully within the RF Mixer frequency range. As with the latter two compatibility fields, this is checked using the upper and lower bound frequencies of the RF input signal found using (Eq. 4-25) and (Eq. 4-26). If the entire input signal frequency falls within the frequency range of the RF Mixer, this compatibility field is set to a value of 1 (compatible). Otherwise, the field is set to a value of 0
(incompatible). If the RF Mixer is excluded from the design and its Database Component Number is set to 0, this compatibility field will be set to 99 to indicate its exclusion.

It is notable that the current SR-TSAM version does not include a compatibility check regarding the output of the RF Mixer. The RF Mixer is assumed to be capable of outputting any intermediate frequency specified by the designer. However, in practice, not only is this not the case, but if the intermediate frequency is too low, it may not be able to sufficiently support the bandwidth specified in the Key Signal Inputs section. The ability for the intermediate frequency to support the required bandwidth is not checked until the next compatibility field for the BPF (IF).

**BPF (IF) Bandwidth Compatibility Determination**

This field functions similarly to the “BPF (RF) Bandwidth Compatibility Determination” field described within this section. This field checks whether the entire signal of interest is contained within the frequency range of the BPF (IF). However, unlike the bandwidth check for the BPF (RF), the signal input to the filter is not centered on the RF frequency specified in the Key Signal Inputs section, but is instead centered on the intermediate frequency specified in the Key System Design Inputs section. Therefore, the “entire signal” now refers to the entire IF signal which is bounded by upper and lower bound frequencies according to

\[
\begin{align*}
    f_{u_{IF}} &= f_{c_{IF}} + \frac{BW}{2} \quad \text{(MHz)} \\
    f_{l_{IF}} &= f_{c_{IF}} - \frac{BW}{2} \quad \text{(MHz)}
\end{align*}
\]

(Eq. 4-27)

(Eq. 4-28)

where \(f_{u_{IF}}\) is the upper bound IF input frequency, \(f_{c_{IF}}\) is the specified IF input center frequency, \(BW\) is the specified input signal bandwidth, and \(f_{l_{IF}}\) is the lower bound IF input frequency.

If the entire IF signal falls within the frequency range of the BPF (IF), this compatibility field is set to a value of 1 (compatible); otherwise, the field is set to a value of 0 (incompatible).
If the BPF (IF) is excluded from the design and its Database Component Number is set to 0, this compatibility field will be set to 99 to indicate its exclusion.

**RF Amplifier Bandwidth Compatibility Determination**

This field functions similarly to the “LNA Bandwidth Compatibility Determination” field described within this section. However, the field first must determine if the incoming signal is at RF or IF depending on the existence of the IF Conversion Block. If the IF Conversion Block is present, this compatibility field checks whether or not the entire IF signal, as bounded by (Eq. 4-27) and (Eq. 4-28), is contained within the RF Amplifier frequency range. If the IF Conversion Block is not present, then this compatibility field checks whether or not the entire RF signal, as bounded by (Eq. 4-25) and (Eq. 4-26), is contained within the RF Amplifier frequency range. If entire signal of interest (either RF or IF) falls within the frequency range of the RF Amplifier, this compatibility field is set to a value of 1 (compatible). Otherwise, the field is set to a value of 0 (incompatible). If the RF Amplifier is excluded from the design and its Database Component Number is set to 0, this compatibility field will be set to 99 to indicate its exclusion.

**ADC Bandwidth Compatibility Determination**

This field checks the ADC sampling rate against the bandwidth of the input signal. In order to avoid signal aliasing, the ADC sampling rate must be at least the product of the required bandwidth and the sampling rate factor (SRF) in order for compatibility. This holds true regardless of whether the signal is at RF or IF when fed to the ADC. Therefore, this field determines compatibility based on

\[
f_s \geq BW \cdot SRF \quad \text{(MHz)}
\]

(Eq. 4-29)

where \( f_s \) is the sampling rate of the ADC (Mps), \( BW \) is the specified input signal bandwidth, and \( SRF \) is the sampling rate factor. If the relationship of (Eq. 4-29) holds true, then this compatibility field is set to a value of 1 (compatible). Otherwise, the field is set to a value of 0 (incompatible).
It is notable that the user can see ADC compatibility in the “Maximum Bandwidth” output specification field within the Key System Specification Outputs section. If the maximum bandwidth in this field exceeds the required bandwidth, it holds true that the “ADC Bandwidth Compatibility Determination” compatibility field will display compatibility.

**FPGA Bandwidth Compatibility Determination**

No bandwidth compatibility analysis is conducted for the FPGA in the current version of the SR-TSAM.

### 4.3.10. Voltage Supply Compatibility Determination

The third of the compatibility checks applied to each component of a sampled SDR receiver design is regarding voltage supply. This compatibility determination is highly straightforward for each component checked. Therefore, a simple explanation is provided within to encompass all components.

The BPF (RF) and BPF (IF) components are assumed to be passive and the SR-CDs do not capture power supply information. Therefore, these components are not considered for voltage supply compatibility analysis and their respective voltage supply compatibility fields simply display “N/A.” The ADC SR-CD does capture voltage supply information. However, the information is presented in a highly inconsistent manner from manufacturer to manufacturer that has not been reformatted and adjusted for this current SDR-RM version. Therefore, the ADC voltage supply compatibility field displays “Insufficient Data” and is ignored in compatibility analysis. As with frequency and bandwidth compatibility analysis, components that are not modeled in the current SR-TSAM version (antenna, LO, and DSP) are not analyzed for compatibility and their respective voltage supply compatibility fields display “Not Modeled.”
For the components that are modeled and considered for voltage supply compatibility analysis (LNA, RF Mixer, RF Amplifier, and FPGA), a very simple compatibility check is put into place. Each of the modeled components considered has their Minimum Voltage Supply and Maximum Voltage Supply specifications read into the SR-TSAM from their respective SR-CDs. For each component, the analysis described in the following paragraph is used to determine compatibility.

The “Constant Voltage Level” field from the Key System Design Inputs section of the SR-TSAM is referenced. If a constant voltage level is specified as required, then the specified “Voltage Supply” from the Key System Design Inputs must fall within the minimum and maximum voltage supply specifications of the component of interest in order for its respective “Voltage Supply Compatibility” field to yield compatibility (return a value of 1). However, if a constant voltage level is not specified as required by the “Constant Voltage Level” field, then the specified “Voltage Supply” level must simply exceed the minimum voltage supply specification of the component of interest in order for its respective “Voltage Supply Compatibility” field to yield compatibility (i.e., return a value of 1).

When a particular component is found to be compatible with the voltage supply requirements from the Key System Design Inputs section of the SR-TSAM according to the criteria laid out in the latter paragraph, a value of 1 is returned in this compatibility field for this particular component. Otherwise, this field reports a 0 (incompatibility) for the component of interest.

4.3.11. Analog IF Conversion Block Presence

The “Analog IF Conversion Block Presence” field captures whether or not a feasible architecture is being implemented by the SR-TSAM within the context of the existence of the IF
Conversion Block. Two architecture options are possible in the SR-TSAM: one with the IF Conversion Block and one without it. While the RF Amplifier can be used in either, its existence, or non-existence, does not constitute alternate architectures for the sake of simplicity. However, since the IF Conversion Block consists of three components (RF Mixer, LO, and BPF (IF)) and two of these are modeled (RF Mixer and BPF (IF)), the SR-TSAM must ensure that either both of these components are used or neither of the components are used. Since designs are developed through random sampling of the Database Component Number fields for each component in the architecture, one of the modeled IF Conversion Block components may be set to empty (Database Component Number = 0) while the other may contain a component (Database Component Number ≠ 0). This is not a compatible architecture.

The “Analog IF Conversion Block Presence” returns one of three values: 1, 0, or 99. A value of 1 indicates that the IF Conversion Block exists, which holds when an actual component exists for both the RF Mixer and the BPF (IF) component blocks in the receiver architecture. A value of 99 indicates that the IF Conversion Block does not exist, which holds when both the RF Mixer and the BPF (IF) component blocks are left empty. A 0 indicates an infeasible architecture caused by one of the IF Conversion Block component blocks being empty and the other being filled. Either a 1 or a 99 must be returned for the final, overall “Component Compatibility” field in order for the Component Compatibility Determination section to return a 1 (compatibility) assuming the “Basic Compatibility” field contains all values of 1 (compatibility) for each respective component.

4.4. ATSV Control of the SDR Receiver Model

The purpose of the SR-TSAM is to construct a trade space of single-RF-chain superheterodyne SDR receiver design alternatives for exploration by the ARL Trade Space
Visualizer (ATSV). The Key Output Specifications and Component Compatibility Determination in the SR-TSAM are intended for trade space exploration via visualization. As summarized in Section 4.1 and illustrated in Figure 4-1, ATSV builds a trade space using the SR-TSAM by sampling the components in the architecture of the modeled SDR receiver and then by collecting the resulting outputs (specification and compatibility) of each sampled design. In order for ATSV to sample the component inputs of the SR-TSAM and collect the outputs of the SR-TSAM, a link must be established between the SR-TSAM and ATSV. This section explains the development of this link as well provide the details of its use to control the SDR-RM.

4.4.1. Development of the ECF SR-TSAM-to-ATSV Link

This section explains the development of the SR-TSAM-to-ATSV link developed for ATSV to access and control the SR-TSAM.

Configuration File (ECF) Development in the ATSV Exploration Engine

The link between the SR-TSAM and ATSV is done through the ATSV Exploration Engine and takes the form of an ATSV-proprietary configuration file in ECF form. Specific ECF files were created to interact with the SR-TSAM. The Exploration Engine is configured directly from the ATSV program. Figure 4-20 shows the main ATSV console window.
The Exploration Engine and its configuration are accessed from the File menu from the ATSV main window. As shown in Figure 4-21, the option “Link to Exploration Engine” is selected to configure the Exploration Engine and develop the ECF link.

Figure 4-21: ATSV Main Window Exploration Engine Selection

Figure 4-22 shows the option window for the Exploration Engine. To develop a configuration file linked to an Excel-based model such as the SR-TSAM, the option “Create/modify configuration for Excel analysis” must be selected as shown. This option can also be selected to modify an existing configuration file.
Upon selection of the option shown in Figure 4-22, the Exploration Engine Configuration File Wizard is started as shown in the left-most image in Figure 4-23.

The ATSV Exploration Engine Configuration File Wizard is the window in which the designer is able to specify model input and outputs to be directly linked to the Excel-based model to be used for trade space visualization. In the case of the SDR-RM, the ATSV Exploration Engine Configuration File Wizard is linked to the SR-TSAM file:
“SDRReceiver_TradeSpaceAnalysisModel_PoC.xls.” This specific link is shown in the right-most image in Figure 4-23.

**SR-TSAM Input and Output Variable Definitions**

Within the Exploration Engine Configuration File Wizard the input and output variables for the SR-TSAM are defined.

**SR-TSAM Input Variables**

The SR-TSAM inputs intended for control from the ATSV Exploration Engine are the Database Component Numbers for each component in the SDR receiver architecture. These inputs consist of discrete values that correspond to values in component SR-CDs and are used to index the SR-CDs in order to retrieve component specification values for a randomly sampled component. The adding of a variable in the Exploration Engine Configuration File Wizard is initiated by clicking the “Add Variable” button in the wizard, which brings up the “Add Excel Variable” window shown in Figure 4-24.

![Add Excel Variable](image)

**Figure 4-24:** ATSV Exploration Engine Input Variable Addition—BPF (RF) Shown

As seen in Figure 4-24, for each variable four fields must be defined: the variable name, the location of the cell for the variable of interest within the SR-TSAM, the type of variable (either continuous values, discrete values, or categorical values), and whether the variable is an input or an output. The example displayed in Figure 4-24 is the configuration of the first SR-TSAM input variable: the BPF (RF) Database Component Number. The name and cell location of this BPF variable were defined, and, as with the all of the inputs specified, the variable was
defined as a discrete input. The “Add Excel Variable” window was prompted and used to define each of the inputs to the SR-TSAM, which were the Database Component Numbers for the BPF (RF), the LNA, the RF Mixer, the BPF (IF), the RF Amplifier, the ADC, and the FPGA. Figure 4-25 displays the Configuration File Wizard with all SR-TSAM input variables defined.

![Configuration File Wizard for Command Line Problems](image)

**Figure 4-25:** ATSV Exploration Engine Configuration File Wizard With Configured Inputs

After defining the input variables, the input sample values were then defined for each variable. Each input variable must have a range or set of discrete values to use during the sampling process in order to properly index the SR-CDs from the SR-TSAM. The range for each component is dictated by the range of Component Numbers that exist in each component’s SR-CD. To establish a range of values for an input in the Exploration Engine Configuration File Wizard, the “Capture” option corresponding to the input of interest is selected, which prompts the “Input Distribution” window shown in Figure 4-26.
Figure 4-26: ATSV Exploration Engine Input Variable Range Configuration—BPF (RF) Shown

Figure 4-26 displays the Input Distribution window for the BPF (RF) component. The range of values defined for this particular input is from 1–421. The BPF SR-CD contains component entries for Component Number values from 0–421. Component Number 0 corresponds to an empty component. Because a BPF must exist at the RF stage in the receiver architecture, 0 is excluded; however, all other components can be included in the architecture, and, hence, the 1–421 range is used. A range of discrete values was defined for every component input according to Table 4-3.

Table 4-3: Discrete Value Ranges for the SR-TSAM Component Inputs

<table>
<thead>
<tr>
<th>Component Input Variable</th>
<th>Discrete Range of Component Numbers</th>
</tr>
</thead>
<tbody>
<tr>
<td>BPF (RF) Database Number</td>
<td>1 – 421</td>
</tr>
<tr>
<td>LNA Database Number</td>
<td>1 – 117</td>
</tr>
<tr>
<td>RF Mixer Database Number</td>
<td>0 – 113</td>
</tr>
<tr>
<td>BPF (IF) Database Number</td>
<td>0 – 421</td>
</tr>
<tr>
<td>RF Amplifier Database Number</td>
<td>0 – 1524</td>
</tr>
<tr>
<td>ADC Database Number</td>
<td>1 – 1754</td>
</tr>
<tr>
<td>FPGA Database Number</td>
<td>1 – 3967</td>
</tr>
</tbody>
</table>
SR-TSAM Output Variables

After the component inputs were defined and assigned input ranges, the output variables were then defined. Output variables are also defined in the “Add Excel Variable” window from the Exploration Engine Configuration File Wizard. The SR-TSAM outputs were each defined. Figure 4-27 displays example output definitions.

The left image in Figure 4-27 displays the definition of the “Component Compatibility” output variable, which references the final field of the Component Compatibility Determination section of the SR-TSAM. Because this field only displays either a 1 or a 0 to indicate a feasible or infeasible design respectively, the output variable was defined as a discrete output variable. The right image in Figure 4-27 displays the definition of the “Minimum Voltage Level (V)” output variable, which references the first field of the Key System Specification Outputs section of the SR-TSAM. This field can be a discrete value given in terms of volts and, hence, it was defined as a continuous output variable. The full list of output variables defined for the configuration file is given in Table 4-4.

Figure 4-27: ATSV Exploration Engine Output Variable Addition
Table 4-4: Output Variables Defined for the Configuration File

<table>
<thead>
<tr>
<th>Output Variable</th>
<th>Variable Type</th>
<th>SR-TSAM Section</th>
</tr>
</thead>
<tbody>
<tr>
<td>Component Compatibility</td>
<td>Discrete</td>
<td>Component Compatibility Determination</td>
</tr>
<tr>
<td>IF Conversion Block Preference</td>
<td>Discrete</td>
<td>Component Compatibility Determination</td>
</tr>
<tr>
<td>Minimum Voltage Level (V)</td>
<td>Continuous</td>
<td>Key System Specification Outputs</td>
</tr>
<tr>
<td>Maximum Constant Voltage Level (V)</td>
<td>Continuous</td>
<td>Key System Specification Outputs</td>
</tr>
<tr>
<td>Noise Figure (dB)</td>
<td>Continuous</td>
<td>Key System Specification Outputs</td>
</tr>
<tr>
<td>Gain (dB)</td>
<td>Continuous</td>
<td>Key System Specification Outputs</td>
</tr>
<tr>
<td>Maximum Allowable Signal (dBm)</td>
<td>Continuous</td>
<td>Key System Specification Outputs</td>
</tr>
<tr>
<td>Minimum Detectable Signal (dBm)</td>
<td>Continuous</td>
<td>Key System Specification Outputs</td>
</tr>
<tr>
<td>Dynamic Range (dBm)</td>
<td>Continuous</td>
<td>Key System Specification Outputs</td>
</tr>
<tr>
<td>RMS Voltage Level at ADC (V)</td>
<td>Continuous</td>
<td>Key System Specification Outputs</td>
</tr>
<tr>
<td>Maximum Bandwidth (MHz)</td>
<td>Continuous</td>
<td>Key System Specification Outputs</td>
</tr>
<tr>
<td>Minimum Frequency (MHz)</td>
<td>Continuous</td>
<td>Key System Specification Outputs</td>
</tr>
<tr>
<td>Maximum Frequency (MHz)</td>
<td>Continuous</td>
<td>Key System Specification Outputs</td>
</tr>
<tr>
<td>Component Preference Index</td>
<td>Continuous</td>
<td>Key System Specification Outputs</td>
</tr>
<tr>
<td>Manufacturer Preference Index</td>
<td>Continuous</td>
<td>Key System Specification Outputs</td>
</tr>
<tr>
<td>Component Price (USD)</td>
<td>Continuous</td>
<td>Key System Specification Outputs</td>
</tr>
<tr>
<td>Component Price w/o FPGA (USD)</td>
<td>Continuous</td>
<td>Key System Specification Outputs</td>
</tr>
</tbody>
</table>

Upon definition of all SR-TSAM output variables in the Exploration Engine Configuration File Wizard, the configuration file was ready for finalization. The final configuration is shown in Figure 4-28. Upon selection of the “OK” option of the bottom of the ATSV Exploration Engine Configuration File Wizard, the option to save the configuration file is given. The settings captured in Figure 4-28 were saved as “SRTSAM-to-ATSV_Link.ecf.” This ECF file can be used and/or modified by SDR receiver designers for trade space visualization of the existing SDR-RM.
4.4.2. Modification of the ECF SR-TSAM-to-ATSV Link

The “SRTSAM-to-ATSV_Link.ecf” file described in Section 4.4.1 can be modified prior to its use for specific design goals. Modifications of the configuration file can help streamline visualization by decreasing the number of input or output variables or by decreasing the range of input variables. For example, input variable ranges could be focused on smaller ranges or output variables irrelevant to the designer’s goals could be eliminated. Modifications could also help the designer gain more information by increasing the number of input or output variables. For example, inputs currently made directly in the SR-TSAM could be adjusted to be ATSV input variables or individual component specifications could be added as output variables. The configuration file can also simply be adjusted as SR-CDs are updated or as the SR-TSAM is
refined and added to. For the current SDR-RM, two modifications are particularly useful: the addition of output variables and the focusing of input variable value ranges.

**Addition of Output Variables**

Because the current version of the SR-TSAM does not calculate many overall system specifications related to the digital resources provided by the ADC and FPGA, it is useful to allow the designer to visualize and set goals based on the individual specifications of these two components. Because this is an especially useful modification of the configuration file described in Section 4.4.1, a separate configuration file was developed to include individual ADC and FPGA specifications called from their respective SR-CDs into the SR-TSAM. The additions were made by simply loading the “SRTSAM-to-ATSV_Link.ecf” file in the ATSV Exploration Engine Configuration File Wizard as seen in Figure 4-28 and defining new variables such as those shown in Figure 4-29. A full list of the added variables can be seen in Table 4-5.

![Figure 4-29: ATSV Exploration Engine Output Variable Addition of Component Variables](image-url)
Table 4-5: Added ADC and FPGA Output Variables Defined for the Configuration File

<table>
<thead>
<tr>
<th>Added Output Variable</th>
<th>Variable Type</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADC Manufacturer</td>
<td>Categorical</td>
</tr>
<tr>
<td>ADC Manufacturer Part Number</td>
<td>Categorical</td>
</tr>
<tr>
<td>ADC Bit Resolution</td>
<td>Continuous</td>
</tr>
<tr>
<td>ADC Sampling Rate (MSPS)</td>
<td>Continuous</td>
</tr>
<tr>
<td>ADC Number of Channels</td>
<td>Continuous</td>
</tr>
<tr>
<td>ADC Power Dissipation (typ. mW)</td>
<td>Continuous</td>
</tr>
<tr>
<td>ADC SNR (dB)</td>
<td>Continuous</td>
</tr>
<tr>
<td>ADC ENOB</td>
<td>Continuous</td>
</tr>
<tr>
<td>ADC Input Voltage Range</td>
<td>Categorical</td>
</tr>
<tr>
<td>ADC INL (± LSB)</td>
<td>Continuous</td>
</tr>
<tr>
<td>ADC DNL (± LSB)</td>
<td>Continuous</td>
</tr>
<tr>
<td>ADC SINAD (dB)</td>
<td>Continuous</td>
</tr>
<tr>
<td>ADC THD (dB)</td>
<td>Continuous</td>
</tr>
<tr>
<td>ADC Architecture</td>
<td>Categorical</td>
</tr>
<tr>
<td>ADC I/O</td>
<td>Categorical</td>
</tr>
<tr>
<td>ADC Package</td>
<td>Categorical</td>
</tr>
<tr>
<td>ADC Supply Voltage Range</td>
<td>Categorical</td>
</tr>
<tr>
<td>ADC Price (USD)</td>
<td>Continuous</td>
</tr>
<tr>
<td>ADC Component Preference</td>
<td>Continuous</td>
</tr>
<tr>
<td>ADC Manufacturer Preference</td>
<td>Continuous</td>
</tr>
<tr>
<td>FPGA Manufacturer</td>
<td>Categorical</td>
</tr>
<tr>
<td>FPGA Series</td>
<td>Categorical</td>
</tr>
<tr>
<td>FPGA Manufacturer Part Number</td>
<td>Categorical</td>
</tr>
<tr>
<td>FPGA Delay Time (ns)</td>
<td>Continuous</td>
</tr>
<tr>
<td>FPGA Number of I/O</td>
<td>Continuous</td>
</tr>
<tr>
<td>FPGA Number of Logic Blocks/Elements</td>
<td>Continuous</td>
</tr>
<tr>
<td>FPGA Number of Registers</td>
<td>Continuous</td>
</tr>
<tr>
<td>FPGA Voltage Supply Minimum (V)</td>
<td>Continuous</td>
</tr>
<tr>
<td>FPGA Voltage Supply Maximum (V)</td>
<td>Continuous</td>
</tr>
<tr>
<td>FPGA Operating Temperature Minimum (°C)</td>
<td>Continuous</td>
</tr>
<tr>
<td>FPGA Operating Temperature Maximum (°C)</td>
<td>Continuous</td>
</tr>
<tr>
<td>FPGA Package/Case</td>
<td>Categorical</td>
</tr>
<tr>
<td>FPGA Price (USD)</td>
<td>Continuous</td>
</tr>
<tr>
<td>FPGA Component Preference</td>
<td>Continuous</td>
</tr>
<tr>
<td>FPGA Manufacture Preference</td>
<td>Continuous</td>
</tr>
</tbody>
</table>

The new configuration with the added ADC and FPGA specification output variables was saved to a new configuration file called “SRTSAM-to-ATSV_Link_ADC&FPGAexpansion.ecf.”
Focusing of Input Variable Ranges

As shown in Chapter 5, it is often useful to streamline the use the ATSV Exploration Engine through modifying the value ranges of the input components. Because using the current SR-TSAM in conjunction with either the “SRTSAM-to-ATSV_Link.ecf” or the “SRTSAM-to-ATSV_Link_ADC&FPGAexpansion.ecf” configuration files involves the designer specifying Key Design Inputs and Key System Design Inputs within the XLS SR-TSAM file, certain system parameters are pre-defined. The most useful of these pre-defined parameters are the frequency and the bandwidth of the RF input signal as well as the frequency of the IF signal.

By using the SR-CDs sorted by frequency and bandwidth specifications developed in Section 4.2.3, a designer can easily limit the discrete value ranges of the input component variables in the Exploration Engine Configuration File Wizard to sample only components in the correct range for the frequency and bandwidth parameters specified in the SR-TSAM. Doing so dramatically cuts down on the number of infeasible designs that inevitably would be generated through random sampling of input components. In fact, making such modifications to the configuration file can change the sampling process from yielding primarily infeasible designs in a sample run to yielding primarily feasible designs.

When the frequency- and bandwidth-sorted SR-CDs are used, the modifications to the value ranges of the component input variables simply consist of selecting a new input ranges. For example, take the FAA land communications example used throughout this chapter. The RF input frequency is 168 MHz, the input bandwidth is 12 MHz, and the IF (used if a design uses an IF Conversion Block) is selected to be 70 MHz. This means that the designer knows the BPF (RF), LNA, and RF Mixer must have frequency ranges that capture the 168 MHz signal. It also means that the BPF (IF) must have a center frequency near 70 MHz. Furthermore, the RF Amplifier needs to have a frequency range that either captures 70 MHz or 168 MHz. It also is known that the ADC must at least have a sampling rate of twice (potentially more depending on
SRF) that of the bandwidth: at least 24 Msps. Using this information, the discrete value ranges of the input variables can be adjusted to the values displayed in Table 4-6 assuming the frequency and bandwidth-sorted SR-CDs are used.

Table 4-6: Discrete Value Ranges for SR-TSAM Component Inputs Adjusted for FAA Example

<table>
<thead>
<tr>
<th>Component Input Variable</th>
<th>Discrete Range of Component Numbers</th>
<th>% Decrease in Search</th>
</tr>
</thead>
<tbody>
<tr>
<td>BPF (RF) Database Number</td>
<td>46 – 59</td>
<td>~ 95%</td>
</tr>
<tr>
<td>LNA Database Number</td>
<td>1 – 26</td>
<td>~ 78%</td>
</tr>
<tr>
<td>RF Mixer Database Number</td>
<td>0 – 22</td>
<td>~ 78%</td>
</tr>
<tr>
<td>BPF (IF) Database Number</td>
<td>0*, 21 – 37</td>
<td>~ 95%</td>
</tr>
<tr>
<td>RF Amplifier Database Number</td>
<td>0 – 652</td>
<td>~ 51%</td>
</tr>
<tr>
<td>ADC Database Number</td>
<td>1673 – 1754</td>
<td>~ 69%</td>
</tr>
<tr>
<td>FPGA Database Number</td>
<td>1 – 3967</td>
<td>0%</td>
</tr>
</tbody>
</table>

*Individual values can be easily added to a range. 0 must be maintained for components that can be left empty in the architecture

Of the input variable ranges adjusted (all except the FPGA), the designer decreased the search area by around 78%. Therefore, this adjustment is highly useful for focusing design searches and increasing the overall efficiency of sampling. Using the frequency- and bandwidth-sorted SR-CDs, the adjustment is done with relative ease. Given the simplicity but usefulness of the adjustment, this modification is recommended to designers using the current SDR-RM.

4.4.3. Using the ECF SR-TSAM-to-ATSV Link – Sampling

Once an ECF configuration file is configured and selected for use with the SR-TSAM, the ATSV Exploration Engine main window opens as shown in Figure 4-30.
The ATSV Exploration Engine is used to sample the SR-TSAM and generate input designs by supplying the “Database Component Number” fields with randomly generated discrete values. Figure 4-30 displays the ATSV Exploration Engine window with a modified set of SR-CD component input values tailored to the FAA land communications example. These input values are similar to those presented in Table 4-6 but are further refined based on the specified SRF of 2.5.

In the version of ATSV used for this work (version 3.2.4), five samplers are available within the Exploration Engine. These are the five samplers described in Section 2.3.2: Basic Sampler, Preference Sampler, Attractor Sampler, Pareto Sampler, and Point Sampler. It was found that because all sampled input values are discrete and SR-TSAM output results are highly
random, the most useful sampler was the simplest and most random, the Basic Sampler. However, to test specific designs of interest and include them in the trade space, the Point Sampler was also used. The Basic Sampler can be run multiple times with the desired number of runs per cycle as shown in Figure 4-30. Each cycle of sampling generates results that are appended to existing results from previous runs in the current Exploration Engine session. The results collected for each run are all of the specified outputs.

Before moving to visualization, it is also useful to focus some basic sampling even further. For example, since it is desirable to visualize designs that do not include the IF Conversion Block, and since these designs are difficult to come by at random (since this involves two separate components having a Database Component Number value of 0 simultaneously), it is useful to force sampling of these designs. Figure 4-31 shows an example of such a focusing.

![Figure 4-31: ATSV Exploration Engine Main Window – Focused Sampling](image)

In Figure 4-31 it can be seen that to focus designs on those with no IF Conversion Block, the RF Mixer and BPF (IF) have been permanently set to a value of 0 and ADC components are
further refined to include those closer to compatibility with the RF frequency (since sub-sampling is disallowed in the example). Once at least one sampling cycle is completed (done by selecting “Start” within the Exploration Engine window), the visualization options within the main ATSV window illuminate and become active as seen in Figure 4-32.

The activation of visualization options means that, at any time, visualization of the trade space generated from sampling in the Exploration Engine can be accomplished. The Exploration Engine window is left open and visualization can happen in real time as a designer switches between sampling and visualization if desired.

4.4.4. Trade Space Visualization of Exploration Engine Results

As the designer continues to sample from the Exploration Engine or after a designer is satisfied with the amount of sampling conducted, the designer can focus on the actual visualization of the trade space data. Chapter 5 further investigates the trade space visualization of SDR receiver design examples, but this current section serves to introduce the basic trade space visualization of Exploration Engine sampling results for the SDR receiver design space. Three visualization features are examined and are highlighted in Figure 4-33:
The first visualization option of ATSV is the 3-D glyph plot, which, as explained in Section 2.3.2, offers up to nine dimensions of visualization. After Exploration Engine sampling of the SDR receiver design space associated with the persisting FAA land communications example, the 3-D glyph plot will look something like that featured in Figure 4-34.

Axes, scales, and other visualization options are easily adjusted within the “Glyph Plot” window. The example display in Figure 4-34 shows the trade space presented in three dimensions according to three overall receiver output specifications calculated from the SR-TSAM using actual SR-CD component inputs: Noise Figure, Gain, and Power Dissipation.
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(Excluding FPGA). However, this trade space has not yet been filtered according to feasible designs. In fact, no design goals are specified at all by default. Therefore, the designer must access the Brush/Preference Controls from the ATSV main window. This prompts the “Brush/Preference Controls” window shown in Figure 4-35.

Design goals and preferences can be specified within the Brush/Preference Controls of ATSV. These goals and preferences can be specified for each input and output from the Exploration Engine link to the SR-TSAM. However, before considering any trade space exploration with these preferences and goals, a user of the SR-TSAM and ATSV must first limit the design space to only feasible designs. As explained in Section 4.3.7, feasible designs are determined from the Component Compatibility Determination section of the SR-TSAM. Therefore, the “Component Compatibility” discrete output specified in the Exploration Engine and controlling ECF configuration file must be selected within the “Brush/Preference Controls” window. Upon selection of this output, the discrete output value of 1 (indicating compatible designs) can be selected for inclusion in the trade space, while the discrete output value of 0 (indicating incompatible designs) can be deselected for exclusion in the trade space. This is shown in Figure 4-36.
Also selected for preference control in Figure 4-36 is the “IF Conversion Block Presence” output variable. The value 0 can be deselected to eliminate infeasible architectures, although no such architectures will appear in the trade space if the “Component Compatibility” output is configured to only allow compatible designs. However, the “IF Conversion Block Presence” can be used to limit the trade space to designs that include or exclude the IF Conversion Block by selecting only the discrete value of 1 or 99 respectively.

Upon limitation of the trade space according to feasibility based on the Component Compatibility output from the Component Compatibility Determination section of the SR-TSAM, the trade space is reduced to the “feasible trade space.” The feasible trade space for the FAA land communications example can be seen in the glyph plot of Figure 4-37. A reduction from the trade space visualized in Figure 4-34 can be readily observed.
Once a feasible trade space is established from Exploration Engine sampling, the designer is free to explore the trade space through visualization as is demonstrated by example in Chapter 5. For the sake of further introduction to this process, additional example preferences are displayed in Figure 4-38. In Figure 4-38, it is shown that the designer is interested in visualizing designs that either include or exclude the IF Conversion Block; designs with a dynamic range (DR) of at least 80 dBm and up to the maximum DR value found in the trade space, 138.32 dBm; designs with a maximum bandwidth of at least 25 MHz and up to the maximum bandwidth value found in the trade space, 90 MHz; and designs that cost anywhere from around $50 to around $1630 without the FPGA. All other designs are excluded from the trade space altogether like those that were deemed infeasible. It can be further seen that the top preference of the designer is to minimize the price of the receiver, while the next preference weighted about 40% of the cost preference is to maximize the DR, while the final preference weighted about 10% of the cost preference is to maximize the maximum bandwidth.

**Figure 4-37:** ATSV 3-D Glyph Plot of FAA Example Feasible Trade Space
Once brush/preference controls are set as in the previous paragraph and Figure 4-38, preferences can be observed in the trade space visuals such as the glyph plot. An especially convenient way to visualize preference is to select preference shading as a feature to establish a heat map of preferences. The glyph plot from Figure 4-37 can be seen redefined according to the brush/preference controls of Figure 4-38 and with preference shading enabled in Figure 4-39.

Figure 4-38: Example Brush/Preference Controls for FAA Land Communications Example

Figure 4-39: ATSV 3-D Glyph Plot of FAA Example With Preferences of Figure 4-38
The designer can then select a more useful view of the trade space with more appropriate axes based on the configured brush/preference controls. An alternate view of the trade space can be seen in Figure 4-40 that features axes more directly related to the specified brush/preference control settings: “Dynamic Range,” “Maximum Bandwidth,” and “Component Price w/o FPGA.” Another feature is highlighted within the glyph plot view in Figure 4-40, the highlighting of the Pareto frontier. In the case of the given example, two design points are along a Pareto frontier (representing Pareto efficient designs that most efficiently meet the criteria set forth in the brush/preference controls specified in Figure 4-38). These points are highlighted in white.

Figure 4-40: Alternate View and Axes of the Trade Space from Figure 4-39

Again, as shown in Chapter 5, the designer can explore the trade space specified by brush/preference controls in many different ways using ATSV. For example, the designer can view any two variables and their relationship to each other in the 2-D Scatter Plot. For example, visualizing a relationship (or lack thereof) shown in Figure 4-40 between “Component Price w/o
FPGA” and “Dynamic Range” in a 2-D Scatter Plot with preference shading enabled can be seen for the given FAA land communications example in Figure 4-41.

**Figure 4-41:** ATSV 2-D Scatter Plot Example for FAA Land Communications Example

Given sampling results from the Exploration Engine’s input/output interaction with the SR-TSAM, an SDR designer is free to explore the trade space of single-RF-chain superheterodyne SDR receiver design using the full suite of visualization options in the ARL Trade Space Visualizer. By leveraging this connection and capabilities, designers can identify trends, tradeoffs, and other relationships in the trade space of SDR receiver design.

4.5. **Chapter Summary**

Trade space visualization of SDR receiver system design has been implemented by developing a unique SDR receiver model (SDR-RM) and linking it to an existing trade space
visualization tool, ATSV. The SDR-RM consists of three primary components: (1) SDR component databases (SR-CDs); (2) an SDR receiver trade space analysis model (SR-TSAM); and (3) an input/output link to the ATSV Exploration Engine.

An SR-CD was developed for each of the six SDR components: (1) BPFs, (2) LNAs, (3) RF mixers, (4) RF amplifiers, (5) ADCs, and (6) FPGAs. The Excel-based SR-CDs were compiled from online sources including both manufacturer-provided and distributor-provided component product listings. The SR-CDs were formatted and refined to be consistent and easily accessible to the SR-TSAM.

The SR-TSAM is an Excel-based model of a single-RF-chain SDR receiver. The model has two architecture options: (1) one that includes an analog IF stage (the “IF Conversion Block”) and (2) one that does not include an analog IF stage. The SR-TSAM consists of five main sections: (1) Component Inputs, which is a section made up of ATSV inputs that query the SR-CDs as well as of the return component specifications from the SR-CDs; (2) Key Signal Inputs, which is a section of user-defined inputs concerning the received signal; (3) Key System Design Inputs, which is a section of user-defined inputs concerning the receiver; (4) Key System Specification Outputs, which is a section of SR-TSAM-calculated output receiver specifications; and (5) Component Compatibility Determination, which is a section of SR-TSAM outputs that report on the compatibility of the receiver.

The ATSV-to-SR-TSAM link is a configuration file that defines input values to be issued to the SR-TSAM from the ATSV Exploration Engine as well as output values to be provided from the SR-TSAM to ATSV for visualization. Inputs are discrete values that sample components in the modeled SDR receiver architecture within the SR-TSAM, and outputs are discrete, continuous, and categorical values provided from the SR-TSAM for systems corresponding to particular input configurations. Configuration files can be modified to improve the sampling and visualization process.
The ATSV Exploration Engine is used to sample the SDR-RM and collect outputs for visualization. ATSV can be leveraged for trade space visualization of the SDR receiver design trade space.
Chapter 5

SDR Receiver Trade Space Visualization Example Results

The ARL Trade Space Visualizer (ATSV) can be used to visualize a trade space contained in an existing database or to visualize a trade space developed in real time by a model such as the SDR-RM. Therefore, in the pursuit of visualization of the SDR receiver design trade space, ATSV can be used two ways: to visualize individual SDR Receiver Component Databases (SR-CDs) or to visualize the outputs of the SDR Receiver Model (SDR-RM) as described in Section 4.4. The purpose of this chapter is to illustrate how ATSV can be used for SDR receiver trade space visualization as well as to highlight some example results found visualizing both the SR-CDs and the SDR-RM. Section 5.1 describes visualization of the SR-CDs using one example SR-CD. Section 5.2 describes visualization of the SDR-RM using three different examples with different SR-TSAM inputs.

5.1. Trade Space Visualization of SR-CDs—High-Speed ADC Example

As discussed in previous chapters, the analog-to-digital converter (ADC) is one of the most critical components within an SDR receiver. The sensitivity and sampling rate of the ADC often determine what kind of analog RF circuitry must precede A/D conversion. Therefore, the ADC is the component selected for example visualization using ATSV for the purposes of this work.

Introduction to ADC Visualization and 3-D Glyph Plot Visualization

The ADC SR-CD described in Section 4.2.2 contains a large number of ADCs. With 1,754 total ADCs, the ADC SR-CD developed for this work contains all ADCs found from the
selected manufacturer’s Internet-based product listings including ADCs from sampling rates as low as around 1 sps to as high as 3 Gsps. However, as seen throughout Section 5.2, the ADCs most relevant to SDR receiver design are those at higher sampling rates. As discussed in previous chapters, the sampling rate of an ADC must be at least twice the bandwidth of the signal the receiver is intended to receive. Because SDR receivers are intended to offer radio flexibility beyond the capabilities of traditional hardware receiver, signal bandwidth is more likely to be relatively high as opposed to low. For this reason, for this section, a new SR-CD was generated that contains only ADCs with sampling rates of 10 Msp or greater.

A CSV version of the higher-speed ADC SR-CD was loaded into ATSV using the “Open Data File” from the File menu of the main ATSV window, which can be seen in Figure 4-21 in Chapter 4. Upon loading the SR-CD, ATSV automatically suggests the insertion of NaN and Null values in all blanks within the CSV file. After loading, the data is ready for visualization and Figure 5-1 shows the first plot obtained from the visualization process.

![3D Glyph Plot](image)

**Figure 5-1:** ADC (10MSPS+) 3-D Glyph Plot—Bit Resolution, Sampling Rate, SNR
Figure 5-1 shows the high-speed ADC data loaded into ATSV from the SR-CD within a 3-D glyph plot. The 3-D glyph plot displayed shows a three-dimensional view of the data leveraging the axes of the plot to display three variables: bit resolution (bits), sampling rate (Msps), and signal-to-noise ratio (dB). Using the glyph plot of Figure 5-1, a designer can easily see where relationships might exist. Each of the three variables seems possibly to relate to the others in some way. The glyph plot, which can be freely rotated in any direction, provides an opportunity to the designer to quickly visualize several dimensions at once to search for trends and relationships. The glyph plot can be easily viewed in more two-dimensional ways as well to further look at how two variables relate. For example, Figure 5-2 shows the glyph plot of Figure 5-1 rotated such only the relationship between and bit resolution is easily visible.

![Figure 5-2: ADC (10+ Msps) 3-D Glyph—Bit Resolution, Sampling Rate, SNR (2-D View 1)](image)

Figure 5-2 essentially shows a 2-D plot and relationship within the 3-D glyph plot viewing window. The particular relationship shown is that between SNR and bit resolution. A direct relationship is clearly seen between the two variables in the figure, which confirms what one might expect as per the discussion on ADC sensitivity in Section Error! Reference source not found. It is known that higher SNR is generally achieved with higher bit resolution.
Therefore, the results found in Figure 5-2 serve three purposes: to confirm the validity of the SR-CD data, to confirm the functionality of ATSV with regards to visualizing the data, and to use a known relationship to illustrate how a designer can begin to search for trends and relationships within the 3-D glyph plot.

Figure 5-3 shows a view of ADC sampling rate versus ADC SNR. While Section Error! Reference source not found. described a known direct relationship between SNR and bit resolution, it also discussed a possible indirect relationship between sampling rate and SNR. As mentioned in Section Error! Reference source not found., higher SNR traditionally comes with the tradeoff of lower sampling rate. However, as highlighted by Section Error! Reference source not found., modern high-performance ADC technology has begun to diminish the tradeoff. Visualizing the two variables and the relationship between them is one way for a designer to qualify and analyze the tradeoff as it stands in the overall trades pace of available ADCs. Figure 5-3 shows that some kind of relationship may exist. However, the relationship is less readily apparent than that seen in Figure 5-2; therefore, Figure 5-3 provides an example for a possible relationship identified in the convenient 3-D glyph plot view that a designer is likely to revisit in other plots to further analyze and search for relationships and trends. Different regions of the plot seem to follow different relationships. Before moving on to the further analysis a designer might pursue in studying a potential relationship, the final 2-D view of the glyph plot is examined in Figure 5-4.
The glyph plot view of Figure 5-4 shows sampling rate versus bit resolution. This view shows a possible relationship between sampling rate and bit resolution, but, similar to the results of Figure 5-3, represent a relationship less readily apparent than that of Figure 5-2. Given the close direct relationship between SNR and bit resolution, the similarities between Figure 5-3 and Figure 5-4 are unsurprising. Both plots require further analysis.

Figure 5-3: ADC (10+ Msps) 3-D Glyph—Bit Resolution, Sampling Rate, SNR (2-D View 2)

Figure 5-4: ADC (10+ Msps) 3-D Glyph—Bit Resolution, Sampling Rate, SNR (2-D View 3)
2-D Scatter Plot Analysis—Bit Resolution, Sampling Rate, and SNR

There are many ways to analyze relationship and trends within ATSV, and there are numerous plots available for use. Some of these are explored throughout this chapter, but the next to be leveraged is particularly useful for examining relationships and trends between two variables, the 2-D scatter plot.

The 2-D scatter plot essentially offers the same view of the trade space as pictured in Figure 5-2–Figure 5-4. However, the plot is more geared for 2-D analysis and facilitates curve fitting to give a user a sense of the relationships that may or may not exist. Figure 5-5 shows a 2-D scatter plot of SNR vs. bit resolution comparable to the glyph plot view of Figure 5-2 but more clearly shows the direct relationship between SNR and bit resolution. It is readily apparent that SNR generally increases as bit resolution is increased. This can be further clarified with the curve fitting feature in the ATSV scatter plot.

Figure 5-5: ADC (10+ Msps) Scatter Plot—SNR vs. Bit Resolution

Figure 5-6 shows the same scatter plot as Figure 5-5, but with a first-order and second-order curve automatically fit to the points. The curve(s) added to a scatter plot in ATSV can be examined to give the user a rough idea of the relationships that exist between variables as well as...
given the user a visual sense for how existent such relationships are based on how closely the sample points fit the selected curve.

Figure 5-6: ADC (10+ Msps) Scatter Plot—SNR vs. Bit Resolution w/ Curve Fitting

As mentioned in Section 2.3.2, an additional feature of ATSV in the scatter plot window is to find mappings between variables. In particular, correlation, second-order goodness fit, multivariate normality, outliers, uniformity, and number of clusters data can be automatically found between variable pairs in the trade space. Unfortunately, however, the version of ATSV used for this work (version 3.2.4) has a limitation that prevents the use of this feature in this work: unlike curve fitting on the actual scatter plot, brush/preference controls cannot be referenced in the generation of the mapping data. Particularly useful would be the ability to access second-order goodness fit mappings between variable pairs, which would allow a user to determine the coefficient of determination, $R^2$, for the second-order curve between variables. For example, a user could access the $R^2$ value for the second-order curve in Figure 5-6, thereby facilitating a quantification of how close the predicted values of the curve are to the actual values found in the trade space. This would allow the designer to better determine the existence of a relationship or trend between SNR and bit resolution as well as understand quantitatively the
actual reality of the relationship. Unfortunately, since brush/preference controls are not referenced in the generation of data, all infeasible designs remain a part of the analysis. This causes three major problems: faulty data cannot be filtered out, only overall trends for the trade space can be evaluated and not trends in trade space segments, and designs deemed infeasible by the designer cannot be filtered.

For the ADCs as well as other components from the SR-CDs, the failure of the automatic mapping feature to reference brush/preference controls means that components will be included in the mappings that should actually be filtered that do not reflect actual values (i.e., ADCs from the SR-CD that contain mistaken values, such as 0 for variables that should instead have NaN values). This can be fixed through manual SR-CD editing and filtering. Furthermore, this can be fixed by exporting only filtered data from ATSV to a data file and then by reloading the data without the filtered values into ATSV. In fact, a smaller database of high-speed ADCs from Analog Devices was used to prove the functionality of this feature. In a plot similar to Figure 5-6, an $R^2$ value of around 0.91 for the second-order fit showing a fairly high direct correlation between SNR and bit resolution. However, while this problem can be fixed from manual SR-CD adjustment or reloading data into ATSV, the other two problems are not so easily addressed.

Another problem resulting from limitation of the feature used to find mappings is that sometimes different relationships and trends exist for different value ranges of the variables in the trade space. While these sections of the trade space, individually determined according to certain variable ranges, could simply be reloaded into ATSV individually, this would limit the data visualization of other variables in the same trade space. This problem is seen in the discussion to follow concerning the results of Figure 5-7–Figure 5-10.

Finally, the automatic mapping feature’s failure to reference brush/preference controls creates another problem: entirely infeasible designs/components or those not of interest to the designer cannot be filtered out for the identification of mappings. This last problem is of
especially great concern in using the full SDR-RM with the SR-TSAM for trade space visualization and is further addressed in Section 5.2. Again, the trade space can be reloaded after first being filtered and exported, but this again limits the real-time advantages of brush controls.

Because the automatic mappings feature cannot currently be leveraged within the scope of the SDR-RM, the remainder of this chapter and work qualitatively examines relationships visually.

Another scatter plot from the high-speed ADC SR-CD is shown in Figure 5-7 for further qualitative analysis of the ADC trade space. Comparable to Figure 5-3, Figure 5-7 shows ADC SNR vs. ADC sampling rate. Given the view in the two figures (the glyph plot view of the two variables in as well as the scatter plot view), this is an example of a view of the trade space that requires further analysis in order to understand the relationships and trends. One useful way to conduct such analysis is to examine the trade space in segments as done by sampling rate in Figure 5-8–Figure 5-10.

![Figure 5-7: ADC (10+ Mps) Scatter Plot—SNR vs. Sampling Rate w/ Curve Fitting](image)

Figure 5-7: ADC (10+ Mps) Scatter Plot—SNR vs. Sampling Rate w/ Curve Fitting

Figure 5-8 shows only sampling ADCs with sampling rates between 10 Mps and 100 Mps. By changing the axis settings and brush/preference controls, only this portion of the trade
space is visualized in the scatter plot, and only this portion is used to generate curve fittings. In Figure 5-8, it can be qualitatively observed that almost no relationship exists between SNR and sampling rate for ADCs of sampling rates 10–100 Msps. Again, this would be more accurately examined quantitatively by obtaining values such as the coefficient of determination. However, given the second listed problem caused by ATSV’s failure to reference brush/preference controls when finding mappings between variable pairs, no single section like that shown in Figure 5-8 can be quantitatively analyzed without reloading the data with only the data shown, which then limits the remainder of variable visualization in the trade space in a single visualization session.

Figure 5-9 shows the ADC trade space with respect to SNR versus sampling rate for ADCs with sampling rates between 100 Msps and 500 Msps. Unlike, the portion of the trade space including ADCs between 10 Msps and 100 Msps shown in Figure 5-8, this portion of the trade space shows a very slight inverse trend between the two variables as suggested by the possible tradeoff between SNR and sampling rate highlighted in Section Error! Reference source not found. However, it easily and qualitatively can be observed that this relationship is relatively weak when compared to the relationship between SNR and bit resolution. The

Figure 5-8: ADC (10–100 Msps) Scatter Plot—SNR vs. Sampling Rate w/ Curve Fitting
deviation of many actual data points from the predicted curve values can be relatively large, and some values for SNR at 100 Msps are nearly identical to values found at 500 Msps. Nevertheless, a slight trend is observed.

Figure 5-9: ADC (100–500 Msps) Scatter Plot—SNR vs. Sampling Rate w/ Curve Fitting

Figure 5-10 shows the ADC trade space with respect to SNR versus sampling rate for ADCs with sampling rates between 500 Msps and 3000 Msps (or 3 Gsps). Again, a slight inverse trend is observed, but, again, the relationship is somewhat weak.
Parallel Coordinates Plot Analysis—Bit Resolution, Sampling Rate, SNR, ENOB, & SFDR

Another useful visualization plot feature in ATSV is the parallel coordinates plot. This can be particularly useful when qualitatively determining the existence or non-existence of a relationship between variables. For example, as seen from Figure 5-7–Figure 5-10, a possible negative correlation exists between SNR and sampling rate, but the relationship is difficult to precisely determine and is likely weak. The positive correlation between SNR and bit resolution seen in Figure 5-5 and Figure 5-6, however, is strong and well-defined. The parallel coordinates plot can be used as another visualization option for analyzing these relationships. As stated in Section 2.3.2, variables with strong positive correlations will have parallel connections between variables, while those with negative correlations will have intersecting connections. Using a parallel coordinates plot, Figure 5-11 shows the relationships between sampling rate and SNR and between SNR and bit resolution of all 10+ Msps ADCs in the selected trade space. As expected and already shown, there is a strong positive correlation between SNR and bit resolution. This is observed from the parallel nature of the interconnections. The relationship between sampling rate and SNR is, again, more ill-defined. While intersections do seem to occur (indicating a negative relationship), the parallel nature suggests a weak or nonexistent correlation.
correlation), there are indeed some parallel interconnections. As with the scatter plot, it is useful to observe only segments of the trade space at a time. Consider, therefore, the portion of the trade space containing only ADCs of sampling rates 500+ Msps given that this portion seemed to yield the most promising results for a relationship in the scatter plot analysis. Figure 5-12 provides the parallel coordinates plot for this part of the trade space.

Figure 5-11: ADC (10+ Msps) Parallel Coordinates—Sampling Rate, SNR, Bit Resolution

Figure 5-12 again shows parallel interconnections between SNR and bit resolution further confirming the strong positive correlation. The interconnections between sampling rate and SNR do seem to typically intersect, indicating a negative correlation. However, as concluded from the scatter plot analysis, the negative relationship is somewhat weaker than the positive one between SNR and bit resolution. The parallel coordinates plot can be used to search for relationships.
Figure 5-13 shows a parallel coordinates plot of the entire selected trade space (all ADCs of sampling rate 10 Msps). This plot shows an example of how parallel coordinates plots can be used to search for trends within an SR-CD or within the outputs of the SDR-RM. Variables can be arranged in any order and any number of existing variables can be added to a single plot. The plot in Figure 5-13 shows SNR, bit resolution, ENOB (effective number of bits), and SFDR (spurious free dynamic range). SNR and bit resolution are placed side by side to provide a point of comparison for a variable pair with a strong positive correlation. Except for some relatively low, outlying ENOB values, a strong positive correlation is observed between bit resolution and ENOB. Additionally, except for the same relatively low, outlying ENOB values, a positive correlation is observed between ENOB and SFDR. Parallel coordinates plots prove useful for quickly identifying trends. By deductive reasoning, given the positive correlations between variable pairs shown in Figure 5-13, one can quickly identify trends not explicitly shown such as a likely positive correlation between SFDR and SNR (the starting and end variables of Figure 5-13). Figure 5-14 shows the exploration of this conclusion through the use of another scatter plot comparing two variables.
Figure 5-13: ADC (10+ Msps) Parallel Coordinates—SNR, Bit Resolution, ENOB, SFDR

Figure 5-14 shows a scatter plot in ATSV of SFDR vs. SNR with best-fit curves of the first and second order. As deduced from the parallel coordinates plot, a relatively strong positive correlation can be qualitatively observed between the two variables.

Figure 5-14: ADC (10+ Msps) Scatter Plot—SFDR vs. SNR w/ Curve Fitting

Exploring Critical Specifications and Possible Tradeoffs—Cost and Power

Two specifications of extreme importance to a designer with regards to most components and whole systems are likely to be cost and power dissipation. A designer is likely bounded by a
budget for each of these critical specifications. Furthermore, power dissipation is listed as one of the critical SWaP specifications, and, as discussed in Section 3.1.1, is arguably the most important of these.

An important specification for ADCs in particular is the sampling rate of the ADC. When employed in an SDR receiver, the ADC is a major deciding factor in the determination of the maximum bandwidth of the receiver and may also drive the IF stage needs of the design. Because cost and power are critical overall specifications of likely importance to the designer, and because the sampling rate of the ADC is also of critical importance with respect to the individual component, it is useful to compare sampling rate against cost and power.

Figure 5-15 shows a scatter plot of ADC sampling rate versus ADC unit price. Initially, a positive correlation seems apparent. However, much like plotting SNR versus sampling rate, a breakdown of the trade space would prove useful. Of particular importance to the SDR designer, is examining the higher speed ADCs that are likely to be used for wide bandwidth applications.

**Figure 5-15:** ADC (10+ Msps) Scatter Plot—Sampling Rate vs. Price w/ Curve Fitting

Figure 5-16 shows only ADCs with a sampling rate of 250 Msps or higher. The plot qualitatively suggests a strong positive correlation between the unit cost of ADCs and the
sampling rate as seen by the best-fit curves of the first and second order. While unsurprising, this is the type of observation that will prove significant to the designer in SDR design since it suggests that selecting a higher ADC sampling rate results in a higher cost. This means that increasing the bandwidth of the receiver results in higher costs. It also suggests that in the absence of sub-sampling facilitating, higher intermediate frequencies or avoiding the IF stage altogether are likely to result in higher costs at the ADC level than leveraging IF stages with lower frequencies. If a designer has an opportunity to eliminate an IF stage, then the cost of doing so with regards to the ADC will need to be measured against the cost savings of eliminating the stage, making the plot of Figure 5-16 of great importance to the designer.

Figure 5-16: ADC (250+ Msps) Scatter Plot—Sampling Rate vs. Price w/ Curve

Also important in overall SDR receiver design is the power dissipation of components. As with cost, if a designer has the ability to eliminate an IF stage or simplify the IF stage by leveraging an ADC with a large enough sampling rate to handle RF level frequencies or lower intermediate frequencies, then the power dissipation must also be a consideration. Questions must be answered such as does an ADC with increased sampling rate have increased power
dissipation, and, if so, will the increased power dissipation outweigh power savings from simplifying the RF front-end?

Figure 5-17 is a scatter plot showing ADC power dissipation versus ADC sampling rate for ADCs of 10–100 Msps. For the plot of Figure 5-17, like the sampling rate versus price and the SNR versus sampling rate scatter plots, it proves useful to divide up the trade space for better viewing. Figure 5-17 shows a general, positive trend, but is highly variable and appears to be a weak relationship. While the extreme power dissipation values tend to increase with sampling rate, other values do not necessarily follow the trend.

Figure 5-17: ADC (10–100 Msps) Scatter Plot—Power vs. Sampling Rate w/ Curve

Figure 5-18 is a scatter plot showing ADC power dissipation versus ADC sampling rate for ADCs of 100–250 Msps. The same type of general behavior is observed in Figure 5-18 as in Figure 5-17.
Figure 5-19 is a scatter plot showing ADC power dissipation versus ADC sampling rate for ADCs of 250–1000 Msps. Again, a general positive trend is observed. Furthermore, it is notable that at each segment of the trade space from Figure 5-17 to Figure 5-18 to Figure 5-19, the minimum power dissipation value has increased indicating a somewhat positive overall correlation. However, the correlation is qualitatively weaker than that observed when considering SNR versus bit resolution. In fact, in the same, smaller Analog Devices-only database of ADCs used to obtain the \( R^2 \) value of 0.91 for SNR versus bit resolution, an \( R^2 \) value of 0.316 was found for a trade space including sampling rates from around 10 Msps to 300 Msps. This suggests to the designer that, while dramatic increases in sampling rates at the ADC level may increase the power dissipation at the ADC level, there is some flexibility in the trade space and, depending on other goals and preference, the tradeoff may not be as significant as that found with price and sampling rate.
Leveraging Brush/Preference Controls

When evaluating any trade space, the use of the ATSV brush/preference controls are likely to be of great benefit to a designer trying to evaluate overall design and component-level alternatives. Figure 5-20 provides a hypothetical example of bush/preference controls a designer could indicate when evaluating ADC component alternatives within the ADC trade space including sampling rates of 10 Msps or higher. In Figure 5-20, the designer has specified the ranges of values that will be allowed for several variables using the brush controls. Any components that do not have output variables within these ranges will no longer be plotted as feasible designs. In Figure 5-20, the designer has also leveraged the preference controls to set maximization and minimization preferences. In particular the designer has specified a preference to maximize ADC sampling rate while minimizing the ADC unit price. The designer has indicated that the price minimization goal is of more importance than the sampling rate maximization goal.

Figure 5-19: ADC (250–1000 Msps) Scatter Plot—Power vs. Sampling Rate w/ Curve
Once the brush/preference controls are adjusted, all visualization plots are updated in real time within ATSV. All plots have the ability to show or hide the infeasible designs as designated by the brushing controls and preferences can be viewed in a variety of ways as designated by the preference controls. Figure 5-21 shows a 3-D glyph plot of the 10+ Msps trade space with the brush/preference controls of Figure 5-20.

Figure 5-21 shows a 3-D glyph plot including SNR, sampling rate, and power dissipation of the ADCs plotted on the axes. However, in Figure 5-21 a fourth variable is also plotted: preference. The preferences specified by the preference controls in the Brush/Preference Controls window in Figure 5-20 are plotted using the Color feature within the Glyph Plot window. The preference coloring is done as a heat map, with red indicating the best preference fit and blue indicating the weakest fit. Notably, only one of the two variables with specified preferences is explicitly shown: sampling rate. Price is not shown on this particular glyph plot, which allows the designer to visualize other important specifications (SNR and power dissipation) and their relationship to sampling rate and preference. A large variety of variable options are available to the designer.
Also provided within the glyph plot of Figure 5-21 is a highlighted most preferred design, representing the most Pareto-efficient design according to the given preferences. The highlighting of this point, given in purple highlighting on the plot, can be enabled or disabled from the Brush/Preference Controls window. Each individual design, including this most preferred point can be selected from the 3-D glyph plot and from other plots as well. Figure 5-22 shows the selection of the most Pareto-efficient highlighted point from Figure 5-21. The device that best fits the preferences given by the designer and remains bounded by the brush controls given by the designer is a National Semiconductor ADC with a sampling rate of 500 Msps and unit price (at a quantity of 1,000) of $36.
Besides selecting the most efficient alternative, it is also useful to visualize the entire Pareto frontier showing designs that fit the preferences specified by the ATSV user. The Pareto frontier can be highlighted as shown in Figure 5-23.
The Pareto frontier highlighted in Figure 5-23 can also be exclusively viewed without other components from the trade space as shown in Figure 5-24.

**Figure 5-23:** ADC (10+ Msps) 3-D Glyph Plot—SNR, Sampling Rate, Power—Pareto Highlight

**Figure 5-24:** ADC (10+ Msps) 3-D Glyph Plot—SNR, Sampling Rate, Power—Pareto Frontier

**Summary**

ATSV can be used to visualize various relationships and trends within the trade space of particular SDR receiver components using the SR-CDs developed for the SDR-RM. This allows designers to conducted individual trade space analysis of components if the rest of the SDR
receiver system design is in place or even if the system design is not in place and component-level analysis is useful. Whether done proactively or retroactively, identifying critical tradeoffs at the component level through visualization of the SR-CDs can help the designer to pinpoint and understand tradeoffs at the system level during visualization of the SDR-RM. For example, the tradeoff between ADC sampling rate and ADC price is likely to factor into decisions made at the system level.

5.2. Trade Space Visualization of the SDR-RM

While the SR-CDs are useful resources and leverage ATSV to explore the relationships and trends within them, the largest and most useful contribution of this work is the development of the entire SDR-RM, which includes the SR-TSAM. The SR-TSAM allows for system-level analysis that facilitates the visualization of the SDR receiver design trade space at the system level. This allows for users to evaluate broader, system-level relationships, trends, and tradeoffs beyond the component level and between components. For example, rather than considering simply how ADC price changes when ADC sampling rate is increased to accommodate the simplification of the RF front-end through the possible elimination of an analog IF stage, a designer can consider how the entire cost of the system changes with the simplification. The designer can weigh cost savings of analog components against the cost increase realized at the ADC level. Simple changes to IF frequency can be evaluated similarly. Countless multivariable scenarios can be evaluated in a visual manner.

The following section provides example visualization exercises leveraged and results found using ATSV and the SDR-RM. Three separate SDR receiver system trade spaces are evaluated throughout the section. Each of these trade spaces is based on a set of SR-TSAM inputs for a hypothetical system for a particular application. For each example the SR-CDs with
components arranged by frequency were used to allow for the focusing on input sampling according to the methods described in Section 4.4.2.

5.2.1. FAA Land Communications Example

The first of the example SDR receiver designs is for a hypothetical receiver system intended for FAA (Federal Aviation Administration) land-based communications. The FAA uses two bands for land communications: 162–174 MHz and 406.1–420.0 MHz [“Aviation Frequencies,” 2010]. For this particular example, the first of these two bands was used to define the hypothetical system. The system was defined according to the SR-TSAM inputs found in Figure 5-25, which shows the Key Signal Inputs and Key System Design Inputs used in the SR-TSAM for the FAA land communications receiver example used throughout this section.

<table>
<thead>
<tr>
<th>Key Signal Inputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>Frequency (MHz)</td>
</tr>
<tr>
<td>Bandwidth (kHz)</td>
</tr>
<tr>
<td>Minimum SNR Required at ADC (dB)</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Key System Design Inputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sub-Sampling Allowed</td>
</tr>
<tr>
<td>Sampling Rate Factor</td>
</tr>
<tr>
<td>IF Frequency (MHz)</td>
</tr>
<tr>
<td>Constant Voltage Level?</td>
</tr>
<tr>
<td>Voltage Supply (V)</td>
</tr>
<tr>
<td>Assumed Filter Insertion Loss if Missing (dB)</td>
</tr>
<tr>
<td>Amplifier Default Half Bandwidth %</td>
</tr>
<tr>
<td>Mixer Default Half Bandwidth %</td>
</tr>
<tr>
<td>Antenna Impedance (ohms) (for Voltage Level @ ADC)</td>
</tr>
<tr>
<td>Antenna Gain (dB) (for Voltage Level @ ADC)</td>
</tr>
</tbody>
</table>

Figure 5-25: FAA Land Communications Example (162–174 MHz) SR-TSAM Inputs

The center frequency was chosen in the center of the 162–174 MHz band (168 MHz), the bandwidth was selected to cover the full band (12 MHz), and the minimum SNR required at the ADC was assumed to be 15 dB. Sub-sampling techniques were not allowed for consideration, the sampling rate factor was set to 2.5, an IF of 70 MHz was selected, the voltage level was allowed to not be one constant level, the available voltage supply was set to 5 V, the assumed insertion
loss of BPFs was set to 2 dB if BPFs do not include the specification, the ADHB and MDHB were set to 10%, the antenna and system impedance was assumed to be at 50 Ω, and the gain of the antenna was assumed to be that of a half-wave dipole (2.15 dB).

**Configuring the Exploration Engine**

The ECF files developed in Sections 4.4.1 and 4.4.2 were leveraged as the basis for sampling the SR-TSAM and collecting the SR-TSAM outputs with the Exploration Engine. However, modifications were made to existing ECF files to focus the sampling on designs more likely to be feasible for the FAA land communications example according to the focusing modifications described in Section 4.4.2. From the Exploration Engine configuration window shown in Figure 4-28, the discrete input ranges for the input variables to the SR-TSAM were changed to reflect those in Table 5-1.

**Table 5-1:** Input Value Ranges for “SRTSAM-to-ATSV_Link_168MHzRF&70MHzIF.ecf”

<table>
<thead>
<tr>
<th>Component Input Variable</th>
<th>Discrete Range of Component Numbers</th>
</tr>
</thead>
<tbody>
<tr>
<td>BPF (RF) Database Number</td>
<td>46 – 59</td>
</tr>
<tr>
<td>LNA Database Number</td>
<td>1 – 26</td>
</tr>
<tr>
<td>RF Mixer Database Number</td>
<td>0 – 22</td>
</tr>
<tr>
<td>BPF (IF) Database Number</td>
<td>0, 21 – 37</td>
</tr>
<tr>
<td>RF Amplifier Database Number</td>
<td>0 – 652</td>
</tr>
<tr>
<td>ADC Database Number</td>
<td>1673 – 1754</td>
</tr>
<tr>
<td>FPGA Database Number</td>
<td>1 – 3967</td>
</tr>
</tbody>
</table>

**Running the Exploration Engine and First 3-D Glyph Visualization**

Using the input values shown in Table 5-1 as the ranges of sample inputs, the Exploration Engine was then used to sample the SR-TSAM using the Basic Sampler. The Basic Sampler was run numerous times to generate a trade space of SR-TSAM outputs based on random, Monte Carlo sampling of the components. In addition to fully random sampling runs with all input
values selected (seen for the FAA example in Figure 4-30), focused sampling was also conducted to ensure a mix of designs with IF Conversion Blocks and without IF Conversion Blocks (focused sampling for designs without an IF stage can be seen for the FAA example in Figure 4-31).

As described in Section 4.4.4 with respect to Figure 4-36, the ATSV brush/preference controls were leveraged throughout the Exploration Engine sampling process to limit plotted designs to only those that pass the compatibility checks of the SR-TSAM. The brush-preference controls were set for this feasibility filtering according to the Brush/Preference Controls window settings as shown in Figure 5-26.

By leveraging the controls shown in Figure 5-26, only feasible designs were included in the visualized trade space. Once sampling was completed and the feasibility brush/preference controls were implemented, the designs were visualized by ATSV. As with the ADC trade space visualization, the first plot to be considered will be a 3-D glyph plot, the axes of which can be scaled if necessary as shown in Figure 5-27.
Figure 5-27: FAA 3-D Glyph Plot Axis Adjustment

Figure 5-27 shows the axes settings of the Glyph Plot Settings window, which can be used to adjust the axis ranges of the 3-D glyph plot. In the visualization of SDR-RM outputs of SDR receiver design at the system level, this was found to be a commonly required adjustment to avoid allowing extreme outliers to skew visualization and prevent effective qualitative analysis. The 3-D glyph plot of the trade space that resulted from the sampling process and the axes settings shown in Figure 5-27 can be seen in Figure 5-28, which shows the 3-D glyph plot view of the SDR receiver design trade space for the FAA land communications example. The plot displays dynamic range (DR), component price (w/o FPGA), and power dissipation (excluding FPGA).
While the SR-TSAM’s (and, hence, the SDR-RM’s) ability to output feasible designs that do not include an analog IF stage (referred to in the SDR-RM as the IF Conversion Block) is predicated on assumptions and simplifications, it does represent a first step towards identifying opportunities to pursue simpler SDR receiver architecture with A/D conversion conducted closer to the antenna. Therefore, finding ways to visualize designs with and without the IF Conversion Block is of importance to analyzing the various relationships, trends, and tradeoffs associated with the inclusion or exclusion of the analog IF stage.

The most basic way in which the different designs (with and without the IF Conversion Block) can be viewed is by simply adjusting the brush/preference controls to include only one design and exclude the other. Figure 5-29 shows the adjustments made to the trade space in the FAA land communications example and shows two instances of the Brush/Preference Controls window: the top leverages brush controls to include only designs without an IF Conversion Block and the bottom leverages brush controls to include only designs with an IF Conversion Block.

**Figure 5-28:** FAA 3-D Glyph Plot—DR, Price, Power

**Designs With and Without the IF Conversion Block**

While the SR-TSAM’s (and, hence, the SDR-RM’s) ability to output feasible designs that do not include an analog IF stage (referred to in the SDR-RM as the IF Conversion Block) is predicated on assumptions and simplifications, it does represent a first step towards identifying opportunities to pursue simpler SDR receiver architecture with A/D conversion conducted closer to the antenna. Therefore, finding ways to visualize designs with and without the IF Conversion Block is of importance to analyzing the various relationships, trends, and tradeoffs associated with the inclusion or exclusion of the analog IF stage.

The most basic way in which the different designs (with and without the IF Conversion Block) can be viewed is by simply adjusting the brush/preference controls to include only one design and exclude the other. Figure 5-29 shows the adjustments made to the trade space in the FAA land communications example and shows two instances of the Brush/Preference Controls window: the top leverages brush controls to include only designs without an IF Conversion Block and the bottom leverages brush controls to include only designs with an IF Conversion Block.
Figure 5-30 displays the results found upon implementation of the controls in Figure 5-29. The 3-D glyph plot on the left shows the trade space from Figure 5-28 with only designs that do not have an analog IF stage, while the plot on the right shows only designs with an analog IF stage.

While it may be useful to visualize the two IF design alternatives separately as shown in Figure 5-30, it was found of especially great benefit to visualize the two together in a manner that facilitates direct comparison. Therefore, the second way the different IF stage design alternatives can be visualized and the manner found to be most useful in making direct comparisons within
this work is to leverage the color feature within the plots of ATSV. As was done to visualize preference in Figure 5.21, shading can be used to show designs including the IF Conversion Block separate from those excluding it on the same plot as seen in Figure 5.31.

Figure 5.31 shows a heat mapping of designs in the FAA land communications example trade space based on the existence or lack of the IF Conversion Block in designs. Blue represents designs with an output value of 1 for the “IF Conversion Block Presence” variable, indicating designs that include the block. Red represents designs with an output value of 99 for the “IF Conversion Block Presence” variable indicating designs that do not include the block.

![Figure 5.31: FAA 3-D Glyph—DR, Price, Power—IF Design Shading (2-D View 1)](image)

The particular view shown in Figure 5.31 is a 2-D view within the 3-D glyph plot of power dissipation (excluding FPGA) versus DR. The view does not qualitatively reveal a direct or indirect relationship between the two variables; however, the plot does seem to reveal a possible relationship between IF Conversion Block presence and power dissipation. The plot Figure 5.31 suggests that designs with the IF Conversion Block have lower minimum power dissipation values than those without the IF Conversion Block and that the designs without the analog IF stage tend to have higher power dissipation values than those with the stage. While this
appears true, it does not necessarily mean that designs with IF Conversion Blocks are always lower in power dissipation. This observation is a critical one that is suggestive of a tradeoff: within this FAA example, the decision to exclude an analog IF stage will likely result in higher power dissipation values than those achievable in designs with an analog IF stage.

Figure 5-32 shows the same glyph plot as Figure 5-31 but with a different 2-D view showing component price (w/o FPGA) versus power dissipation (excluding FPGA). As has been observed and will be observed for other variable pairs in the visualization process, this variable pair seems to have relationships in at least some parts of the trade space, but it requires further analysis to identify. However, as with the results in Figure 5-31, those in Figure 5-32 do suggest relationships pertaining to the IF Conversion Block preference. This view again shows that designs without the IF Conversion Block tend to have higher power dissipation values than those with IF Conversion Blocks; and while designs with the analog IF stage can be as high in power dissipation in as those without, those without the analog IF stage cannot be as low in power dissipation as those with. Furthermore, the more expensive design alternatives seem to be those that do not include the IF Conversion Block.

Figure 5-32: FAA 3-D Glyph—DR, Price, Power—IF Design Shading (2-D View 2)
Figure 5-33 shows the glyph plot of Figure 5-32 and Figure 5-31 but with a view of component price (w/o FPGA) versus DR. Aside from the price observation with respect IF Conversion Block presence, no trends are readily apparent from this view. However, like other variable pairs, the axes can be scaled to gain a closer view of part of the trade space. Eliminating the outlying high price designs shown in Figure 5-33 through scaling resulted in Figure 5-34.

Figure 5-33: FAA 3-D Glyph—DR, Price, Power—IF Design Shading (2-D View 3)

While Figure 5-34 provides a view of the plot from Figure 5-33 without outlying values that skew viewing, thereby hampering qualitative analysis, it reveals no further conclusions. As was the case for the analysis of variable pairs for SR-CD visualization in Section 5.1, it was useful to further analyze variable pairs in 2-D scatter plots.
2-D Scatter Plot Analysis of Select FAA Example Variable Pairs

The first variable pair visualized in 2-D scatter plot form from the 3-D glyph plots of Figure 5-31—Figure 5-34 is component price (w/o FPGA) versus DR as shown in Figure 5-35.

As with the 3-D glyph plot, color can be used to distinguish between designs with an IF Conversion Block and without. In Figure 5-35, the image on the left shows the scatter plot comparing price to DR without shading, which is the default view showing all design alternatives. The image on the right shows the same scatter plot, but with shading based on the presence of the
IF Conversion Block using the same color scheme as that found in the 3-D glyph plots. Figure 5-36 shows a larger view of the right plot of Figure 5-35 with best-fit curves.

Figure 5-36 further confirms the conclusions made regarding Figure 5-33 and Figure 5-34: no direct or indirect trend between component price and DR is readily apparent. However, Figure 5-36 allows for easier visualization of the IF Conversion Block price trend. Again, it is seen that higher-priced design alternatives are generally those that do not include the IF Conversion Block. However, it is possible for designs without the IF Conversion Block to be as low as those with the analog IF stage and those with the analog IF stage can also get to higher price levels.

Figure 5-37 shows component price (w/o FPGA) versus power dissipation (excluding FPGA). This is the same variable pair shown in the 3-D glyph plot of Figure 5-32. A very weak direction relationship seems to exist between the variables, but only for the overall data and not necessarily between like designs with the same IF stage configuration. A closer look at a portion of the trade space with best-fit curves shown in Figure 5-38 illustrates this.
Figure 5-37: FAA 2-D Scatter—Price vs. Power—IF Design Shading w/ Curve Fitting

Figure 5-38 shows that an overall weak direct relationship appears to exist. However, this relationship seems to arise from the fact that many of the higher-priced designs are those without an analog IF stage, and more of the higher power dissipating designs are also those without an analog IF stage. The relationship is weak and suggests dependency on more closely correlated values.

Figure 5-38: FAA 2-D Scatter—Price vs. Power – IF Design Shading w/ Curve Fitting (Scaled)
**Example Brush/Preference Controls Analysis**

As with visualization at the component level, a designer can leverage brush/preference controls in ATSV to search the trade space for preferred designs and Pareto frontiers according to specific design goals and interests.

Figure 5-39 provides a set of example brush preference controls used in the FAA land communications example herein. Using brush controls in Figure 5-39, the designer has specified that designs with and without an IF Conversion Block are of interest, that only systems under $1000 are to be considered, that only systems with a dynamic range of at least 95 dBm are to be considered, and that systems must dissipate less than 2500 mW (2.5 W) to be considered. These brush controls represent the possible design constraints and budgets facing the designer. The designer has leveraged the preference controls in Figure 5-39 to specify that the number one design goal is to minimize the power dissipation (excluding FPGA) of the system while two equally important secondary goals are to minimize the component price (w/o FPGA) and maximize the DR. The resulting trade space is shown with a most preferred Pareto efficient design highlighted (in purple) in Figure 5-40.

![FAA Example Brush/Preference Controls Example](Image)

**Figure 5-39:** FAA Example Brush/Preference Controls Example
Figure 5-40 features a 3-D glyph plot displaying the three output variables that have preferences associated with them: DR, component price (w/o FPGA), and power dissipation (excluding FPGA). Furthermore, IF Conversion Block shading is implemented to highlight designs with and without an analog IF stage. The highlighted design in the plot is one with a relatively high DR, relatively low power dissipation, and most importantly a low component price. This reflects the preferences given in Figure 5-39. Furthermore, only designs are included that fit the criteria given in the brush controls of Figure 5-39.

**Figure 5-40:** FAA 3-D Glyph—DR, Price, Power—IF Design Shading—Preferred Design Shown

Figure 5-41 shows the 3-D glyph plot of Figure 5-40 with only the Pareto frontier displayed. The frontier contains only design alternatives on the low end of the component price (w/o FPGA) range and also reflects the secondary preferences of minimizing power dissipation
and maximizing DR where possible. Pareto frontiers can also be shown in plots other than the 3-D glyph plot such as 2-D scatter plots as shown in Figure 5-42.

Figure 5-41: FAA 3-D Glyph—DR, Price, Power—IF Design Shading—Pareto Frontier Shown

Figure 5-42 shows the 2-D scatter plot of Figure 5-38, but with the brush/preference controls of Figure 5-39 enabled and the resulting Pareto frontier highlighted (with black cross-hairs). In this view of the trade space it can be clearly seen that the Pareto frontier includes designs of low cost and relatively low power dissipation (except where influenced by other design preferences).
As was the case with visualizing the component level trade space in Section 5.1, the most preferred point according to the brush/preference controls can be selected from any of the plots. Figure 5-43 shows the most preferred point according to the example brush/preference controls given in Figure 5-39. Some specifications appropriate to the given preferences include: a component price (w/o FPGA) of $67.68, a DR of 128.03 dBm, and power dissipation (excluding FPGA) of 631.46 mW. The components selected for design can be easily determined by simply imputing the “Database Component #” values for each component into the SR-TSAM to call up the specific design.

**Figure 5-42:** FAA 2-D Scatter—Price vs. Power—IF Design Shade w/ Highlighted Pareto Front
Also notable regarding the most preferred point given in Figure 5.43 is that it includes an IF Conversion Block. After visualizing the Pareto frontier resulting from initial brush/preference controls, a designer may be further compelled to adjust the controls to investigate designs without the IF Conversion Block. This can be done using either brush or preference controls. It was accomplished for this example using brush controls shown in Figure 5.44.

**Figure 5-43:** FAA Most Preferred Design from Figure 5-39 Brush/Preference Controls
Figure 5-44 shows the removal of the value of 1 from the “IF Conversion Block Presence” variable. This means that all designs with an IF Conversion Block will now be hidden as infeasible designs in the trade space, thereby changing the Pareto frontier. A similar exercise is conducted in the examples in Section 5.2.2 and Section 5.2.3, but within this current example simple the new resulting most preferred point is shown in Figure 5-45.

Figure 5-45 displays the new most preferred point for the FAA land communications example using the updated brush/preference controls given in Figure 5-44. The new design does not include an IF Conversion Block. The component price (w/o FPGA) is actually down from the previous most preferred point to $53.69, the DR is slightly up from the previous most preferred point at 128.53 dBm, but the power dissipation has considerably increased to 1.10 W. This result is of great significance to the designer. Despite the noted trend that some of the more expensive designs in the trade space were those that did not include an analog IF stage, for this particular case, a lower cost was obtained from excluding the IF stage. This is the result of the weakness of the price relationship noted earlier that some cheaper designs existed without analog IF conversion blocks. However, a consequence of the general trend for designs without the IF...
Conversion Block to consume more power, the power dissipation of the new most preferred
design point has increased power dissipation by about 74% over the previous most preferred
point. This observation is exactly the type of observations that aids a designer in evaluating
design tradeoffs. In this case and in simplified terms, with all preferences held constant as
specified in Figure 5-39 and Figure 5-44 with the exception of the IF Conversion Block, the
designer can choose to pursue a design with an analog IF stage that meets preferences or can
choose to pursue a design without an analog IF stage that still allows for relatively low cost and
high DR but at the expense of an increase in power dissipation by around 74%.

**Figure 5-45**: FAA Most Pareto-Efficient Design from Figure 5-44 Brush/Preference Controls

**Analysis of Gain and Noise Figure**

In order to support the effectiveness in the SDR-RM and ATSV in yielding true
relationships and trends, a known relationship will be examined throughout the example systems
modeled in this chapter: the generally inverse relationship between gain and noise figure. Firstly,
the noise figure of components is generally inversely related to the gain. Secondly, passive components with no gain have a noise figure simply equivalent to component insertion loss (negative gain). Finally, as can be easily observed from the cascading noise factor equation given in (Eq. 3-21), at the system level, the larger the gain values of devices, the lower the overall noise figure is likely to be. Therefore, the FAA land communications example herein is used to search for this relationship.

Figure 5-46 provides a 3-D glyph plot of the FAA land communications trade space with shading used to differentiate designs with an analog IF stage from those without. The glyph plot shows noise figure, gain, and component price (w/o FPGA).

**Figure 5-46:** FAA 3-D Glyph—Noise Figure, Gain, Price—IF Design Shading

Figure 5-47 shows the glyph plot with only a view of gain versus noise figure. Figure 5-48 provides a closer view of the trade space for systems with a gain less than 50 dB.
Figure 5-47: FAA 3-D Glyph—Noise Figure, Gain, Price—IF Design Shading (2-D View 1)

Figure 5-47 and Figure 5-48 suggest an overall inverse relationship between the noise figure and gain variables. The overall relationship is present but qualitatively appears relatively weak. However, another interesting trend is observed: the inverse curve for gain versus noise figure for designs with an IF Conversion Block is farther out than the curve for designs without an analog IF stage. In other words, at given noise figures, gain is typically higher for designs with IF Conversion Blocks than for those without. Furthermore, at low noise figure values, gain values are achieved by designs with IF Conversion Blocks higher than those ever achieved at any noise figure by designs without IF Conversion Blocks, and for designs of low gain, higher noise figure values are observed for designs with IF Conversion Blocks than values ever observed for designs without IF Conversion blocks.
To further visualize the relationship between gain and noise figure in the FAA land communications example, scatter plots were used. Figure 5-49 shows a plot of receiver gain versus receiver noise figure for systems with a gain less than 50 dB and a noise figure less than 4.5 dB. Both designs with an analog IF stage and without an analog IF stage are shown using preference shading in the figure. Again, a weak inverse relationship is observed and further illustrated with the curve-fitting shown in the figure. However, to better understand the relationship it was found to be useful to visualize designs with an IF Conversion Block separately from those without one.

Figure 5-48: FAA 3-D Glyph—Noise Figure, Gain, Price—IF Design Shading (Scaled)
Figure 5-49: FAA 2-D Scatter—Gain vs. Noise Figure—IF Design Shading (Scaled) w/ Curve

Figure 5-50 shows the scatter plot of Figure 5-49 with only designs shown that have an IF Conversion Block. An inverse relationship observed and qualitatively appears stronger than that observed for Figure 5-49.

Figure 5-50: FAA 2-D Scatter—Gain vs. Noise Figure—IF Stage (Scaled) w/ Curve
Figure 5-51 shows the scatter plot of Figure 5-49 with only designs shown that do not have an IF Conversion Block. Again, an inverse relationship is observed that qualitatively appears stronger than that observed in Figure 5-49.

An inverse relationship between gain and noise figure is clearly observed in the FAA land communications example as expected. Notable results include that relationship is strongest when observed separately between designs with analog IF stages and designs without analog IF stages and that the curve for those with analog IF stages is farther out that for those without.

5.2.2. GSM-850 Downlink Example

The second of the example SDR receiver designs is for a hypothetical receiver system intended for GSM-850 communication. The receiver downlink for GSM-850 is on the 869–894 MHz band [Agilent Technologies, 2008]. The system was defined according to the SR-TSAM inputs found in Figure 5-52, which shows the Key Signal Inputs and Key System Design Inputs used in the SR-TSAM for the GSM-850 receiver example used throughout this section.
The center frequency was chosen in the center of the 869–894 MHz band (881.5 MHz), the bandwidth was selected to cover the full band (25 MHz), and the minimum SNR required at the ADC was assumed to be 15 dB. Sub-sampling techniques were not allowed for consideration by default but are adjusted in the example, the sampling rate factor was set to 2.0 (the minimum value according to the Nyquist criterion), an IF of 140 MHz was selected, the voltage level was allowed to not be one constant level, the available voltage supply was set to 5 V, the assumed insertion loss of BPFs was set to 2 dB if BPFs do not include the specification, the ADHB and MDHB were set to 10%, the antenna and system impedance was assumed to be at 50 Ω, and the gain of the antenna was assumed to be that of a half-wave dipole (2.15 dB).

### Configuring the Exploration Engine

The ECF files developed in Sections 4.4.1 and 4.4.2 were leveraged as the basis for sampling the SR-TSAM and collecting the SR-TSAM outputs with the Exploration Engine. However, modifications were made to existing ECF files to focus the sampling on designs more likely to be feasible for the GSM-850 receiver example according to the focusing modifications described in Section 4.4.2. From the Exploration Engine configuration window shown in Figure 4-28, the discrete input ranges for the input variables to the SR-TSAM were changed to reflect those in Table 5-2. Furthermore, an additional discrete input variable was added to the

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**Table 5-2:** GSM-850 Downlink Example (869–894 MHz) SR-TSAM Inputs

<table>
<thead>
<tr>
<th><strong>Key Signal Inputs</strong></th>
</tr>
</thead>
<tbody>
<tr>
<td>Frequency (MHz)</td>
</tr>
<tr>
<td>Bandwidth (kHz)</td>
</tr>
<tr>
<td>Minimum SNR Required at ADC (dB)</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th><strong>Key System Design Inputs</strong></th>
</tr>
</thead>
<tbody>
<tr>
<td>Sub-Sampling Allowed</td>
</tr>
<tr>
<td>Sampling Rate Factor</td>
</tr>
<tr>
<td>IF Frequency (MHz)</td>
</tr>
<tr>
<td>Constant Voltage Level?</td>
</tr>
<tr>
<td>Voltage Supply (V)</td>
</tr>
<tr>
<td>Assumed Filter Insertion Loss if Missing (dB)</td>
</tr>
<tr>
<td>Amplifier Default Half Bandwidth %</td>
</tr>
<tr>
<td>Mixer Default Half Bandwidth %</td>
</tr>
<tr>
<td>Antenna Impedance (ohms) (for Voltage Level @ ADC)</td>
</tr>
<tr>
<td>Antenna Gain (dB) (for Voltage Level @ ADC)</td>
</tr>
</tbody>
</table>

**Figure 5-52:** GSM-850 Downlink Example (869–894 MHz) SR-TSAM Inputs
configuration file: “Sub-Sampling Allowed.” In the GSM-850 example to follow, the impact of the allowance of sub-sampling was observed on a number of receiver outputs. To facilitate this observation, the sub-sampling variable was changed from a user input to the SR-TSAM to an ATSV Exploration Engine input to the SR-TSAM for sampling purposes. A sampled value of 0 disallows sub-sampling techniques from a design while a sampled value of 1 allows sub-sampling techniques. The input values for this added variable are also seen in Table 5-2.

Table 5-2: Input Value Ranges for “SRTSAM-to-ATSV_Link_881.5MHzRF&140MHzIF.ecf”

<table>
<thead>
<tr>
<th>Component Input Variable</th>
<th>Discrete Range of Component Numbers</th>
</tr>
</thead>
<tbody>
<tr>
<td>BPF (RF) Database Number</td>
<td>92, 102</td>
</tr>
<tr>
<td>LNA Database Number</td>
<td>1 – 71</td>
</tr>
<tr>
<td>RF Mixer Database Number</td>
<td>0 – 78</td>
</tr>
<tr>
<td>BPF (IF) Database Number</td>
<td>0, 46, 51</td>
</tr>
<tr>
<td>RF Amplifier Database Number</td>
<td>0 – 986</td>
</tr>
<tr>
<td>ADC Database Number</td>
<td>1728 – 1754</td>
</tr>
<tr>
<td>FPGA Database Number</td>
<td>1 – 3967</td>
</tr>
<tr>
<td>Sub-Sampling Allowed</td>
<td>0, 1</td>
</tr>
</tbody>
</table>

Running the Exploration Engine and First 3-D Glyph Visualization

The Exploration Engine was run using the ECF file generated according to Table 5-2 for the GSM-850 example just as it was run for the FAA land communications example. Sampling was done in a completely random manner as well as a focused manner sampling designs without analog IF Conversion Blocks as shown in Figure 5-53.
Figure 5-53 shows the Exploration Engine settings used during the sampling process of the GSM-850 receiver example for focused sampling of designs without an IF Conversion Block. The notable difference between these settings and those used for the FAA land communications example and shown in Figure 4-31 is the inclusion of the “Sub-Sampling Allowed” input variable. This value was set to only sample a value of 0 (no ADC sub-sampling allowed) during random sampling. However, the value was changed during focused sampling used to find designs without IF Conversion Blocks. During this focused sampling, sampling runs using a value of 0 were used and runs using a value of 1 were used for the sub-sampling input variable.

Furthermore, the range of available ADCs was set to include all ADCs when the value was set to 1 (ADC Database values from 1728 to 1754) and was set to include only ADCs with a large enough sampling rate to accommodate no sub-sampling when the value was changed to 0 (ADC Database values form 1752 to 1754). It is assumed that all ADCs in the sample set (ADC Database values from 1728 to 1754) can accommodate sub-sampling as needed if the “Sub-Sampling Allowed” variable is set to 1. This assumption was highlighted in Section 4.3.5.
As with the FAA land communications receiver example, the trade space was limited to only feasible designs according to the “Component Compatibility” field using the brush/preference controls of ATSV, which can be seen in Figure 5-54.

![Figure 5-54: GSM-850 Example Feasibility Filtering Using Brush/Preference Controls](image)

After sampling the SDR-RM, collecting model outputs, and filtering the results to feasible designs, ATSV was then used to visualize the trade space of the GSM-850 receiver example with a 3-D glyph plot shown in Figure 5-55. Figure 5-55 shows a 3-D glyph plot similar to those generated in the FAA land communications example. The glyph plot visualizes four variables one of which is the presence of the IF Conversion Block through the use of color and the other three on the plot axes: noise figure, gain, and power dissipation (excluding FPGA).
Analysis of Gain and Noise Figure and Introduction to Sub-Sampling Effect Analysis

As was done for the FAA land communications example, the relationship between gain and noise figure was examined for reference against the other example systems as well as to confirm the existence of a known relative relationship. Figure 5-56 shows the 3-D glyph plot of Figure 5-55 but with a 2-D view showing gain versus noise figure.

Figure 5-55: GSM 3-D Glyph—Noise Figure, Gain, Power—IF Design Shading

Figure 5-56: GSM 3-D Glyph—Noise Figure, Gain, Power—IF Design Shading (2-D View)
With the exception of some outlying data with noise figure values of over 4.5 (greater than that seen in the majority of points observed in the FAA example), Figure 5-56 exhibits behavior similar to the behavior observed in the FAA land communications example seen in Figure 5-47: a generally indirect relationship between gain and noise figure with the inverse curve for designs with IF Conversion Blocks appearing to be farther out from the curve for designs without IF Conversion Blocks. However, as with the FAA land communications example, it was found useful to examine the relationship separately for designs with and without analog IF stages.

Figure 5-57 shows two versions of the 3-D glyph plot from Figure 5-56: one with only those designs with an analog IF stage (left image) and one with only designs without an analog IF stage (right image). While these are examined best in 2-D scatter plot form, one more 3-D glyph plot view was generated to also then be examined in a 2-D scatter plot: a view of only the designs without analog IF stages (the right-most image in Figure 5-57) shaded according to the “Sub-Sampling Allowed” variable. As can be seen with analysis of variable pairs to follow this gain versus noise figure analysis (i.e., ADC price versus system component price (w/o FPGA)), it was found that separating the designs with no analog IF stage into those that were allowed to leverage sub-sampling and those that were not sometimes highlighted additional relationships. The separation of these values can be seen in Figure 5-58.
Figure 5-58 shows only designs for the GSM-850 receiver example system that do not include analog IF stages. It displays such designs that did not leverage sub-sampling in blue and those that did leverage sub-sampling in red. However, no new relationships were readily identified through qualitative analysis of Figure 5-58.

As with the FAA land communication example, scatter plots were used to better evaluate the relationship between variable pairs for the GSM-850 example. Figure 5-59 shows the 2-D scatter plot of gain versus noise figure including best-fit curves of the first-order and second-order for all designs (those that include analog IF sections and those that do not).
As expected from the observations made on Figure 5-56, Figure 5-59 shows a general indirect correlation between gain and noise figure. This is best observed divided in Figure 5-60 and Figure 5-61.

Figure 5-60 shows only the portion of the trade space with designs that do not include the IF Conversion Block. This plot is further divided by color like Figure 5-58 into designs that leveraged sub-sampling and those that did not. Again, with the exception of some outlying data, a general inverse trend is observed between gain and noise figure; however, no trend is readily and visually apparent between the use and nonuse of sub-sampling with respect to gain and/or noise figure.
Figure 5-60: GSM 2-D Scatter—Gain vs. Noise Figure—No IF Stage—Sub-Sample Shading

Figure 5-61 shows only the portion of the trade space with designs that do include the IF Conversion Block. Again, a general inverse trend is observed between gain and noise figure. Due to the focused sampling process leveraged by the Exploration Engine, all designs in the portion of the trade space did not leverage sub-sampling.

Figure 5-61: GSM 2-D Scatter—Gain vs. Noise Figure—IF Stage—Sub-Sample Shading
ADC Selection Impact on System Component Price (w/o FPGA)

As discussed throughout this work, the effect of ADC sampling rate on the overall performance and characteristics of the SDR receiver is large. The ADC sampling rate is a main driver in the maximum achievable bandwidth and, depending on sub-sampling capabilities, can drive what frequencies can be received thereby driving the need for an analog IF stage and dictating the frequency level for the IF stage. For instance, in the current GSM-850 receiver system example, to accommodate the 25-MHz bandwidth of the GSM-850 downlink signal, using a sampling rate factor of 2 (the minimum Nyquist value), an ADC must have a bandwidth of at least 50 Msps. If it is assumed that any selected ADC can leverage sub-sampling, then this 50 Msps is the minimum required sampling rate for the ADC. However, if it is assumed that sub-sampling cannot necessarily be leveraged or is not leveraged, then the ADC sampling rate must accommodate the highest signal frequency at its input. If expected to receive the full RF signal without aliasing, the ADC must then have a sampling rate of at least 1.788 Gsps (using 894 MHz as the upper bound input frequency and a sampling rate factor of 2). If an analog IF section is used and, according to the current example, the IF is set to 140 MHz, then the ADC must have a sampling rate of at least 305 Msps (using 152.5 MHz as the upper bound input frequency). Clearly, from these given these values, for a relatively high-frequency, high-bandwidth application (such as the current GSM-850 example), determinations such as those regarding the use of an analog IF section and/or the possible use of ADC sub-sampling techniques have a massive impact on the type of ADC required. Given that this is the case, it stands to reason that such determinations are likely to have a large impact on many critical overall system specifications. One of these critical specifications investigated herein is overall system cost.

The plot in Figure 5-16 in Section 5.1 revealed that for ADCs with sampling rates over 250 Msps, the ADC unit cost generally increases as sampling rate is increased. This general relationship was also observed for ADCs in general with sampling rates of 10 Msps and greater.
but with more outliers. Furthermore, many very high-speed ADCs (1+ Gsps) were observed to be considerably more expensive than those below the Gsps range. Given that these tendencies have been observed, it follows that increasing ADC sampling rate in a system to accommodate higher intermediate frequencies or to accommodate sampling at RF without sub-sampling will result in a direct overall system cost increase. Therefore, ATSV was used to explore this trend to confirm its existence and analyze its effect. The first plot in this analysis is seen in Figure 5-62, which shows a 2-D scatter plot of the GSM-850 receiver design example trade space and plots ADC unit price versus system component price (w/o FPGA).

![GSM 2-D Scatter—ADC Price vs. System Price—IF Design Shading w/ Curve](image)

**Figure 5-62:** GSM 2-D Scatter—ADC Price vs. System Price—IF Design Shading w/ Curve

A very clear and very strong direct relationship was observed between ADC unit cost and overall system cost in Figure 5-62. Furthermore, at each ADC price level, the cost between design alternatives varied relatively little when compared to the larger price scale, which is especially true at higher ADC price levels. This result suggests that within this particular trade space, according to the SR-CD component inputs specified by Table 5-2, ADC selection has a large impact on overall price. As the price of the selected ADC increases, so does the overall system cost; furthermore, if an ADC is held constant, then pricing tends to vary less than it can
from ADC changes, particularly at higher ADC price levels. It should be noted that this is observed when viewing the full range of resulting component prices and ADC prices. A view of a much smaller segment of the trade space is shown in Figure 5-70 and displays a different relationship; however, examining the entire trade space is of most interest in order to examine different IF Conversion Block configurations, which may require ADCs with very high sampling rates.

This relationship in Figure 5-62 is critical for analysis since it demonstrates to what extent ADC selection and ADC price drives overall system cost. Furthermore, the relationship can be examined for trends relating to the existence or nonexistence of an analog IF stage in design alternatives. The scatter plot in Figure 5-62 includes shading to designate designs with analog IF stages from those without; however, because sub-sampling was allowed for some designs in the sampling process, designs without analog IF stages do not necessarily require higher sampling rates than those with analog IF stages (if sub-sampling is allowed) to be deemed compatible and be included in the trade space. For such designs with sub-sampling techniques employed, the ADC sample set is no different than for designs that include analog IF stages. Therefore, to best examine the relationship in Figure 5-62, it was found to be more useful to break the trade space into designs with analog IF stages and those without and then further breakdown the trade space of designs without analog IF stages into designs assuming the use of sub-sampling and those assumed to not use sub-sampling.

Figure 5-63 shows two scatter plots of the same nature of Figure 5-62 but with a divided trade space: designs with analog IF stages are plotted on the left and those without analog IF stages are plotted on the right. The same strong, direct relationship between ADC price and system price was observed when dividing the trade space accordingly. Furthermore, little difference is observed between the two plots including such traits as curve slope, minimum and maximum values, and point deviation. As discussed in the previous paragraph, this is primarily
due to the fact that designs without IF Conversion Blocks include designs that both leverage and do not leverage sub-sampling. Therefore, the right-most plot of Figure 5-63 was further divided according to Figure 5-64.

Figure 5-64 shows only designs that do not include analog IF stages. Shading is used to differentiate the sampled input value for the “Sub-Sampling Allowed” input variable. Blue points indicate design alternatives with a value of 0, indicating that sub-sampling cannot be used. Red points indicate design alternatives with a value of 1, indicating that sub-sampling can be used. It is observed that designs that do not leverage sub-sampling are all high in price (well above $500) and are at the higher range of ADC prices with the exception of one outlying point. This result closely reflects an easily deduced expectation: a receiver design with no analog IF stage and no sub-sampling employed needing to sample up to 894 MHz will be considerably more expensive than possible design alternatives with an IF stage needing only to sample 152.5 MHz or than designs allowing sub-sampling needing only to sample 25 MHz due to considerably more expensive ADCs.
One outlying point was observed in Figure 5-64 and, for reference, the details of the outlier are provided in Figure 5-65. The outlying ADC is a National Semiconductor ADC (part number: ADC10D1000CIUT) with a sampling rate of 1 Gsps that is priced at $1500, which is far above the price points of other ADCs (including the National Semiconductor ADC08B3000CIYB, which has a sampling rate of 3 Gsps, which is nearly half the price).
For reference, the system design alternatives in the GSM-850 receiver design example trade space plotted with their respective ADC prices versus ADC sampling rates in Figure 5-66 to confirm the outlying point as well as the previously observed general direct relationship between ADC price and ADC sampling rate.

The direct relationship between ADC price and ADC sampling rate is shown in Figure 5-66, and the outlying point at $1500 is the same as that highlighted in Figure 5-64. Using this relationship and expanding upon findings from Figure 5-62–Figure 5-64, Figure 5-67 shows the relationship between ADC sampling rate and component price (w/o FPGA).
Figure 5-66: GSM Scatter Plot—ADC Price vs. ADC Sample Rate (300MSPS+)

Figure 5-67 shows all designs in the GSM-850 receiver design example trade space. As expected, a direct relationship is observed: as ADC sampling rate is increased substantially across the trade space so is the end system price. Again, outlying data is seen for the National Semiconductor ADC10D1000CIUT, which is priced at $1500 for a sampling rate of 1 Gsps. A view of the plot from Figure 5-67 without the outlying data is shown in Figure 5-68.

Figure 5-67: GSM 2-D Scatter—ADC Sampling Rate (300+ Msps) vs. System Price
The relationships between ADC sampling rate, ADC price, and system price can also be visualized together in a parallel coordinates plot in Figure 5-69. Figure 5-69 is also scaled and is governed by brush controls used to eliminate the outlying National Semiconductor ADC for visual clarity. Parallel interconnections can be seen between ADC sampling rate and component price (w/o FPGA) as well as between component price and ADC price. The plot of Figure 5-69, therefore, confirms the direct relationships identified between these variable pairs and represents another way to visualize them using ATSV. It can be concluded from Figure 5-64, Figure 5-68, and Figure 5-69 that ADC price directly affects overall system price when examining the entire trade space of interest and that dramatically increasing the sampling rate of the ADC, which generally directly affects ADC price, increases overall system cost. Furthermore, designs without the IF Conversion Block cannot be as cheap as those with the IF Conversion Block if sub-sampling is not employed (Figure 5-64). From these conclusions it therefore follows that designs that require dramatically higher ADC sampling rates such as those without IF Conversion Blocks...
and without sub-sampling or those with higher IF levels and without sub-sampling will generally cost more than designs requiring much lower ADC sampling rates.

**Figure 5-69: GSM Parallel Coordinates—ADC Sampling Rate, System Price, ADC Price**

It must be noted before ending the discussion of ADC sampling rate and ADC price’s effect on overall system component cost that the trend observed was that between ADCs of dramatically different sampling rates on the higher end of the spectrum to illustrate the tradeoffs facing a designer when determining whether or not to include an IF Conversion Block section in the design and to visualize what happens when the designer assumes sub-sampling is possible versus when the assumption is not made. For ADCs at the lower end of the sampling rate spectrum, the price of ADCs is much cheaper and less directly tied to sampling rate (as seen by increased “outliers” in Figure 5-15); therefore, in this region of the trade space ADC price does not as dramatically impact system price. This is seen in Figure 5-70, which shows that the increase of ADC price does not necessarily directly affect overall system cost at lower ADC price levels. This is important for the designer to notice for drawing conclusions in the GSM-850 SDR receiver example trade space. Different sections of the trade space have different trends and behavior. When considering designs requiring very high ADC sampling rates (i.e., designs without the IF Conversion Block and without sub-sampling), the cost of the system dramatically
increases and become closely and directly tied to the cost of the ADC. When considering designs that do not require such high ADC sampling rates (i.e., designs with the IF Conversion Block or those without the analog IF section but with sub-sampling), systems costs can be kept much lower with proper ADC selection.

**Example Brush/Preference Controls Analysis**

For the sake of example, a brush/preference control scenario is given for the hypothetical GSM-850 SDR receiver. Brush/preference controls were specified for the example in ATSV as given by Figure 5-71 in which six variables have specified brush and preference controls. The “IF Conversion Block” variable was set to allow designs with and without the IF Conversion Block and was set as the top preference for maximization (meaning that the designer preferred to pursue designs within the brushed trade space that do not include an analog IF stage). The “Component Compatibility” variable was simply set to accept only feasible designs. The “Component Price (w/o FPGA)” variable was set to accept only values from the lowest actual price ($43.31) up to $1,000 and was set for preferred minimization. Notably, the price was set to

**Figure 5-70:** GSM 2-D Scatter—ADC Price (< $40) vs. System Price (< $200)—IF Shading
a value above the minimum found in the trade space, which was to filter out $0.00 values resulting from errors resulting from NaN values listed for any single component prices (see Section 4.3.6). The “Sub-Sampling Allowed” variable was set to accept designs with and without assumed sub-sampling; however, a preference was specified to most prefer designs that do not make the sweeping assumption. The “Minimum Detectable Signal” variable was set to accept values no higher than −100 dBm and was set to be minimized. Finally, the “Maximum Allowable Signal” variable was set to accept no values less than 10 dBm and was set to be maximized.

Figure 5-71: GSM Example Brush/Preference Controls Example

The newly-defined trade space with included preferences specified by the settings in Figure 5-71 is seen in a 3-D glyph plot shown in Figure 5-72. Figure 5-72 shows the trade space with heat mapped preference shading and with the most preferred design (according to Figure 5-71 brush/preference controls) highlighted. The more preferred designs (red and orange points), cover a wide range of values (the easiest to see given the viewing angle provided in Figure 5-72 is component price, which is set to be minimized) given the conflicting criteria given in the brush/preference controls. Therefore, even though the three variables with major preferences
were selected for axes, most preferred designs and the Pareto frontier is difficult to see without the aid of ATSV (unlike the fairly obvious set of preferred points found in Figure 5-40 for the FAA land communications example). This points to one of ATSV’s major strengths: allowing for multi-variable visualization and analysis of conflicting design preferences and goals.

![Figure 5-72: GSM 3-D Glyph—Price, MDS, MAS—Preference Shading—Preferred Shown](image)

Because color was used for preference heat mapping in Figure 5-72, the difference between designs with analog IF stages and without analog IF stages could no longer be visualized with color. Instead, size was leveraged as seen in Figure 5-73 where designs without analog IF stages appear larger (from values of 99 for the “IF Conversion Block Presence” variable) than those with analog IF stages (from values of 1).
The resulting most preferred point from the example exercise is given in Figure 5-74.
5.2.3. FM Radio Example

The third and final of the example SDR receiver designs given in this work is for a hypothetical receiver system intended for common, commercial FM radio communication. The well-known band for FM radio communication is 88–108 MHz. The system was defined according to the SR-TSAM inputs found in Figure 5-75, which shows the Key Signal Inputs and Key System Design Inputs used in the SR-TSAM for the FM receiver example used throughout this section.

**Figure 5-74:** GSM Example Most Preferred Design from Figure 5-73
The center frequency was chosen in the center of the 88–108 MHz band (98 MHz), the bandwidth was selected to cover the full band (20 MHz), and the minimum SNR required at the ADC was assumed to be 15 dB. Sub-sampling techniques were not allowed for consideration and were not subject to Exploration Engine input, the sampling rate factor was set to 2.5, an intermediate frequency of 60 MHz was selected, the voltage level was allowed to not be one constant level, the available voltage supply was set to 5 V, the assumed insertion loss of BPFs was set to 2 dB if BPFs do not include the specification, the ADHB and MDHB were set to 10%, the antenna and system impedance was assumed to be at 50 Ω, and the gain of the antenna was assumed to be that of a half-wave dipole (2.15 dB).

### Configuring the Exploration Engine

From the Exploration Engine configuration window shown in Figure 4-28, the discrete input ranges for the input variables to the SR-TSAM were changed to reflect those in Table 5-3.

<table>
<thead>
<tr>
<th>Key Signal Inputs</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Frequency (MHz)</td>
<td>98</td>
</tr>
<tr>
<td>Bandwidth (kHz)</td>
<td>20</td>
</tr>
<tr>
<td>Minimum SNR Required at ADC (dB)</td>
<td>15</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Key System Design Inputs</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Sub-Sampling Allowed</td>
<td>0</td>
</tr>
<tr>
<td>Sampling Rate Factor</td>
<td>2.5</td>
</tr>
<tr>
<td>IF Frequency (MHz)</td>
<td>60.0</td>
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<tr>
<td>Constant Voltage Level?</td>
<td>0</td>
</tr>
<tr>
<td>Voltage Supply (V)</td>
<td>5.0</td>
</tr>
<tr>
<td>Assumed Filter Insertion Loss if Missing (dB)</td>
<td>2.0</td>
</tr>
<tr>
<td>Amplifier Default Half Bandwidth %</td>
<td>10.0%</td>
</tr>
<tr>
<td>Mixer Default Half Bandwidth %</td>
<td>10.0%</td>
</tr>
<tr>
<td>Antenna Impedance (ohms) [for Voltage Level @ ADC]</td>
<td>50</td>
</tr>
<tr>
<td>Antenna Gain (dB) [for Voltage Level @ ADC]</td>
<td>2.15</td>
</tr>
</tbody>
</table>

**Figure 5-75:** FM Radio Example (88–108 MHz) SR-TSAM Inputs
Special Note on Component Preference and Manufacturer Preference

Two important specifications given for components in the SR-CDs and for overall systems in the SR-TSAM Key System Outputs are the “Component Preference” and “Manufacturer Preference” specifications. These two specifications currently represent early proof-of-concept fields that should be fully explored, refined, and likely divided into more specifications in future versions of the SDR-RM. Currently, the 0–5 values assigned to these specifications are intended to capture designer-defined preferences according to designer-defined criteria to roughly summarize some of the risks and other considerations concerning the selection of particular components and particular manufacturers for an SDR receiver design. In the FAA land communications SDR receiver example as well as the GSM-850 SDR receiver example, neither one of these two specifications was investigated. The FM radio example contained herein includes an analysis of these specifications.

To demonstrate the use of the preference specifications in the SDR-RM and ATSV, a set of preference values were arbitrarily assigned to components in each SR-CD. Values of 5 indicated highest preference, while values of 0 indicated lowest preference.

Table 5-3: Input Value Ranges for “SRTSAM-to-ATSV_Link_98MHzRF&60MHzIF.ecf”

<table>
<thead>
<tr>
<th>Component Input Variable</th>
<th>Discrete Range of Component Numbers</th>
</tr>
</thead>
<tbody>
<tr>
<td>BPF (RF) Database Number</td>
<td>34, 35, 39</td>
</tr>
<tr>
<td>LNA Database Number</td>
<td>1 – 4</td>
</tr>
<tr>
<td>RF Mixer Database Number</td>
<td>0 – 16</td>
</tr>
<tr>
<td>BPF (IF) Database Number</td>
<td>0, 19 – 21</td>
</tr>
<tr>
<td>RF Amplifier Database Number</td>
<td>0 – 651</td>
</tr>
<tr>
<td>ADC Database Number</td>
<td>1636 – 1754</td>
</tr>
<tr>
<td>FPGA Database Number</td>
<td>1 – 3967</td>
</tr>
</tbody>
</table>

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For the BPF SR-CD, all Mini-Circuits BPFs were given a manufacturer preference value of 5. All other manufacturers were given a manufacturer preference value of 0. All of the BPFs (including all manufacturers) were given a component preference value of 5.

For the LNA SR-CD and the RF Amplifier SR-CD, the manufacturer preference values included a value of 5 for all Analog Devices amplifiers, a value of 0 for all Atmel amplifiers, a value of 3 for all Avago Technologies amplifiers, a value of 3 for all Maxim Integrated Products amplifiers, and a value of 4 for all Texas Instruments amplifiers. All amplifiers were assigned a component preference value of 5.

For the RF Mixer (or Downconverter) SR-CD, the manufacturer preference values included a value of 5 for all Analog Devices mixers, a value of 3 for all Avago Technologies mixers, a value of 0 for all Linear Technology mixers, a value of 3 for all Maxim Integrated Products, a value of 0 for NEC mixers, a value of 0 for Skyworks mixers, and a value of 4 for Texas Instruments mixers. Again, all mixers were assigned a component preference value of 5.

For the ADC SR-CD, the manufacturer preference values included a value of 5 for Analog Devices ADCs, a value of 0 for Linear Technology ADCs, a value of 3 for Maxim Integrated Products ADCs, a value of 3 for National Semiconductor ADCs, and a value of 4 for Texas Instruments ADCs. All ADCs with a sampling rate of less than 250 Msps were assigned component preference values of 5. At a randomly selected “Component Number” value in the frequency-arranged SR-CD, within the sampling rate range of 250 Msps component preference values were changed to 3 and 4 (random selection). Upon increase to 1000 Msps sampling rates, component preference values were changed to 0, 1, and 2.

For the FPGA SR-CD, the manufacturer preference values included a value of 5 for Altera FPGAs, a value of 0 for Xilinx FPGAs, and a value of 0 for Atmel FPGAs. All FPGAs were given a component preference value of 3 except for the Stratix III and Stratix IV series FPGAs by Altera, which were given values of 4 and 5, respectively.
The given preference values were selected arbitrarily but with some consistency between manufacturers and were selected in some cases to simulate possible considerations. Examples of simulated considerations include increased risk considered for ADCs with especially high sampling rates and designer experience and familiarity with a particular series of FPGAs.

**Analysis of Gain and Noise Figure**

As with the FAA land communications example and the GSM-850 example, the relationship between noise figure and gain was examined to check for consistency and a known relationship. As with the prior two examples, the feasible trade space was developed through Exploration Engine sampling of the SDR-RM and through the use of brush/preference controls to eliminate infeasible designs. A 3-D glyph plot of the trade space featuring gain and noise figure is provided in Figure 5-76, which has system noise figure, gain, and dynamic range on its axes and displays IF Conversion Block presence with shading.

![FM 3-D Glyph—Noise Figure, Gain, DR—IF Design Shading](image)

**Figure 5-76:** FM 3-D Glyph—Noise Figure, Gain, DR—IF Design Shading

Figure 5-77 provides the 2-D scatter plot analysis of the noise figure versus gain relationship. As has been observed for the FAA land communications and the GSM-850 examples, Figure 5-77 shows a generally indirect relationship between noise figure and gain for
the FM radio example. While the top figure shows all designs and does not readily show the
relationship, stronger relationships are seen for the bottom two figures showing separate parts of
the trade space according to IF stage configuration (the bottom left image showing designs
without IF Conversion Blocks and the bottom right image showing those with IF Conversion
Blocks). Again, the inverse curve for designs with IF Conversion Blocks appears farther out
from that of those without analog IF stages.

![Figure 5-77: FM 2-D Scatter—Noise Figure vs. Gain—IF Design Shading](image)

To further demonstrate the general, qualitatively-observed inverse relationship between
noise figure and gain, the parallel coordinates plot of Figure 5-78 was generated. Figure 5-78
shows a parallel coordinates plot for the noise figure and gain variable pair. Color is again used
to differentiate between designs of the two possible IF stage configurations. A large number of intersecting lines are observed indicating an inverse relationship.

**Figure 5-78:** FM Parallel Coordinates—Noise Figure & Gain

**Examining Preference**

While the values input to the SR-CDs governing manufacturer and component preferences were substantially arbitrary, the following sub-section highlights some exercises used to factor preference variables into the visualization process. Because it is known that ADC sampling rate was used in the determination of component preference values within the ADC SR-CD and that most other components in other SR-CDs have component preference values of 5, ADC sampling rate and its effect on overall system “Component Preference Index” is used throughout this example to demonstrate a type of relationship that may be found linked to preference.

This first plot generated in the preference exploration exercise is the 3-D glyph plot given in Figure 5-79, which shows Component Preference Index, Manufacturer Preference Index, and ADC sampling rate on its three axes and leverages shading to show IF configuration.
Figure 5-79: FM 3-D Glyph—Component Preference, Manufacturer Pref., ADC Sampling Rate

Figure 5-80 provides an alternate view of the glyph plot in Figure 5-79 showing a 2-D view of ADC sampling rate versus overall “Component Preference Index.” An inverse relationship is expected and does appear as can be further explored and discussed with regards to Figure 5-81 and Figure 5-82.

Figure 5-80: FM 2-D Scatter—ADC Sampling Rate vs. Component Pref. — IF Design Shading
Figure 5-81 is a parallel coordinates plot showing overall system component preference and ADC sampling rate to confirm the dependency of high sampling rate on overall system component preference. Figure 5-81 shows that the interconnections attached to high sampling rates intersect with the interconnections attached to lower rates indicating, thereby an indirect relationship. This simply confirms expectation for this particular example since it is known that the ADC SR-CD uses lower and lower component preference values for ADCs with sampling rates at and above 250 Msp (and, the trade space of interest considers ADCs at 150 Msp and substantially higher) and that other component preference values from other SR-CDs are fairly constant besides only a minority of FPGAs. However, had a designer observed the behavior of Figure 5-81 without such explicit previous knowledge, a critical observation would be made that designs in the trade space using higher ADC sampling rates (such many without the IF Conversion Block as indicated by red interconnections in the plot) are generally lower in overall component preference index value. This would represent a large tradeoff in the field of preference. To further visualize this inverse relationship a scatter plot with curve fitting for the same variable pair is given in Figure 5-82.

Figure 5-81: FM Parallel Coordinates—Component Preference & ADC Sampling Rate
Figure 5-82 confirms the inverse relationship observed in Figure 5-81. To further explore the trade space with respect to preferences, ADC sampling rate is replaced by dynamic range (DR) in the 3-D glyph plot view of the trade space seen in Figure 5-83.

Figure 5-82: FM 2-D Scatter—ADC Sampling Rate vs. Component Pref.—IF Design Shading

Figure 5-83 provides a view of the trade space that displays IF stage configuration with shading and DR, Component Preference Index, and Manufacturer Preference Index on axes.

Figure 5-83: FM 3-D Glyph—DR, Component Pref., Manufacturer Pref.—IF Design Shading
Rather than extensively search the trade space for trends relating preference to DR which was unlikely to yield conclusive results, a brush/preference controls use case was executed.

Figure 5-84 provides the brush/preference controls for a hypothetical scenario of interest to a designer: one in which all feasible designs in the trade space are considered, the preference for DR is maximization, the preference for overall manufacturer preference is maximization, and, to a lesser extent, the preference for overall component preference is minimization. These controls offer a designer an opportunity to search through the trade space for designs using components from preferred manufacturers and components with relatively high preference values as well while pursuing other design goals (such as maximizing DR). Because manufacturer preference and component preference values may be random across numerous data sets (with the exception of times when certain specifications are directly tied to preference such as high ADC sampling rate yielding lower component preference values), these preferences can alter Pareto fronts in difficult-to-predict ways; therefore, the ability to visualize Pareto frontiers and the effects of these preferences across a multitude of variables is tremendously beneficial.

Figure 5-84: FM Example Brush/Preference Controls Example Scenario
To very simply examine the results of the brush/preference controls of Figure 5-84 directly with respect to preference values and DR, Figure 5-85 is given. Figure 5-85 shows the glyph plot of Figure 5-83 with a highlighted Pareto frontier (designs highlighted in white) resulting from the brush/preference controls of Figure 5-84.

**Figure 5-85:** FM 3-D Glyph—Figure 5-83 w/ Figure 5-84 Brush/Preference Controls—Pareto

Figure 5-86 provides a view of the plot from Figure 5-85 with preference shading enabled and with a viewing angle that enables the observation of the Pareto frontier along the maximum range of all variables listed for maximization in the brush/preference controls of Figure 5-84. The most efficient design is highlighted in purple within the Pareto frontier.
Figure 5-86: FM 3-D Glyph—Figure 5-85—Preference Shading—Pareto Frontier

Figure 5-87 provides the glyph plot of Figure 5-86 with only the Pareto frontier shown without any other designs. The image on the left shows the plot with preference shading enabled, while shading is leveraged in the right-most image for differentiating designs with analog IF stages from those without analog IF stages. The most preferred design is given in Figure 5-88.

Figure 5-87: FM 3-D Glyph—Figure 5-85/Figure 5-86—Only Pareto Frontiers

Figure 5-88 shows a most preferred design that has a DR of 135.12 dBm, a component preference index value of 4.4, and a manufacturer preference index value of 4.2. As clearly seen in the Pareto frontier shown in Figure 5-87, this design is not the point with the highest component and manufacturer preference index values, but it does represent the preferences of the
designer best within the Pareto front. For an example, a random design point was selected with a higher component preference index and is shown in Figure 5-89.

**Figure 5-88**: FM Most Preferred Design Point From Figure 5-85–Figure 5-87

Figure 5-89 shows that while the selected point has a component preference index value that, at 4.8, is higher than the most preferred design, it is at the expense of a lower manufacturer preference index value now at 3.8 and a substantially lower DR now at 108.88 dBm.
Continued Search for Trends, Relationships, and Tradeoffs

The SDR receiver design trade space has countless trends, relationships, and tradeoffs that sometimes differ and sometimes remain generally the same between specific examples. Besides the trends, relationships, and tradeoffs called out in this work for the three example systems provided (the FAA land communications SDR receiver, the GSM-850 SDR receiver, and the FM radio SDR receiver) there are many others. These can be identified a number of ways. Thus far in this chapter, relationships have been largely highlighted first by manipulating 3-D glyph plots and viewing/manipulating 2-D scatter plots of variable pairs of interest followed by further support from plots such as parallel coordinates plots. These relationships were also studied within the context of specified brush/preference controls. However, this approach was often predicated on either pre-existing knowledge or pre-existing suspicions of certain relationships or based on an interest in specific variable pairs. In the development of this work, two other methods were found useful for quickly identifying relationships not necessarily initially
sought after: (1) the use of parallel coordinates plots to search for relationships and (2) the use of the scatter matrix to search for relationships.

*Leveraging Parallel Coordinates Plots to Search for Relationships*

Just as they can be used to substantiate the findings of a particular relationship, parallel coordinates plots can be used to identify relationships. Consider, for example, Figure 5-90, which shows a parallel coordinates plot pairing maximum allowable signal (MAS) with dynamic range (DR) and DR with minimum detectable signal (MDS). Given that DR is simply the difference between MAS and MDS it follows that DR is likely to have a close relationship with both of these variables making these good variables to demonstrate the effectiveness of parallel coordinates plots at highlighting relationships. While some exceptions do exist, a large number of parallel interconnections exist between MAS and DR, suggesting a direct relationship. Again, while some exceptions do exist, a large number of intersecting interconnections exist between DR and MDS suggesting an indirect relationship. The high density of parallel interconnections for MAS to DR and the high density of intersecting interconnections for DR to MDS suggest strong relationships. Again, this result is expected given the equation for DR, which suggests that a higher MAS yields a higher DR, and a smaller MDS yields a higher DR in a very linear way. However, it is easy to see how if a relationship was not known, the parallel coordinates plot would easily identify such a strong relationship. The conclusions drawn from the parallel coordinates plot can be verified with scatter plots.
Figure 5-90: FM Parallel Coordinates—MAS, DR, & MDS Sampling Rate

Figure 5-91 shows a 2-D scatter plot comparing MAS to DR. A very strong direct relationship can be seen in the figure, confirming the findings of the parallel coordinates plot.

Figure 5-91: FM 2-D Scatter—MAS vs. DR—IF Design Shading

Figure 5-92 shows a 2-D scatter plot comparing MDS to DR. A very strong indirect relationship can be seen in the figure, confirming the findings of the parallel coordinates plot.
Parallel coordinates plots can highlight disconnected variables as seen in Figure 5-93, which shows a parallel coordinates plot linking ADC sampling rate and overall system power dissipation (excluding FPGA).

Figure 5-92: FM 2-D Scatter—MDS vs. DR—IF Design Shading

Figure 5-93: Parallel Coordinates—ADC Sampling Rate & Power—IF Preference Shading

Figure 5-17–Figure 5-19 from Section 5.1 demonstrated a slight direct relationship between ADC sampling rate and ADC power dissipation. However, the relationship was weak for and shallow for lower sampling rates. Furthermore, even for higher sampling rates, the
somewhat weak nature of the relationship does not guarantee that increases in ADC sampling rate would increase overall SDR receiver power dissipation. In the FM radio example, when qualitatively viewing the entire trade space (all ADC sampling rates and all power dissipation levels) in Figure 5-93, no strong relationships exist. Some interconnections intersect while others are parallel. In a manner similar to confirming a relationship, the lack of a relationship can be further confirmed with a scatter plot.

Figure 5-94 supports the lack of a strong relationship between sampling rate and system power dissipation (excluding FPGA) when the entire trade space is viewed (smaller portions of the space are not considered herein).

![Figure 5-94: FM 2-D Scatter—Power vs. ADC Sampling Rate—IF Preference Shading](image)

### Leveraging Scatter Matrices to Search for Relationships

Another particularly useful tool in ATSV is the scatter matrix, which consists of a matrix of 2-D scatter plots. The matrix, which can be viewed in several ways, allows designers to view a single variable on one axis against any number of other variables along a changing axis. The designer is able to select and deselect variables for view just as with the parallel coordinates plot. A scatter matrix for the FM radio example can be seen in Figure 5-95, which shows a large
number of system variables for the FM radio SDR receiver design trade space example. Each variable can be quickly referenced against another variable within the view of a single window as shown. Given the large number of variables and limiting size of the image shown Figure 5-95, a partial view of the same scatter matrix is provided in Figure 5-96.

Figure 5-95: FM Scatter Matrix—Select Variables—with IF Preference Shading

Scatter matrices like those shown in Figure 5-95 and Figure 5-96 can be quickly referenced to identify relationships between variable pairs. For example, a pair that stands out as having a possible relationship in Figure 5-96 is that of noise figure and minimum detectable signal.
Figure 5.96 shows a closer look at the 2-D scatter plot of noise figure vs. MDS. As easily noticed in the scatter matrix, a clear direct relationship exists between the two variables as shown. This is an unsurprising result given the dependence of MDS on noise figure (which appears directly in the MDS calculation).
Another, more intriguing, relationship that was noticed from the scatter matrix was that between the maximum bandwidth of the receiver and MDS. Figure 5-98 shows the 2-D scatter plot comparing maximum bandwidth to MDS. A general, direct relationship is observed with some outliers. Furthermore, a clear tradeoff can be identified in Figure 5-98 that was also apparent from the scatter matrix: designs with IF Conversion Blocks have lower MDS value minimums than those without IF Conversion Blocks, which suggests that the additional hardware is likely to increase the MDS (decreasing sensitivity).

Figure 5-97: FM 2-D Scatter—Noise Figure vs. MDS—IF Design Shading w/ Curve Fitting
Again, parallel coordinates plots can be used to confirm observed relationships. Relationships found in the scatter matrix can be checked against parallel coordinates plots like that shown in Figure 5-99. Figure 5-99 shows a parallel coordinates plot linking maximum frequency to maximum bandwidth (a primarily direct relationship), maximum bandwidth to MDS (found to be somewhat of a direct relationship with some outliers), MDS to noise figure (a direct, but not necessarily linear relationship), and noise figure to gain (a primarily indirect relationship).
The scatter matrix can also highlight familiar variable pair patterns. Figure 5-100 shows a 2-D scatter plot of the FM radio SDR receiver design example trade space comparing DR to component price (w/o FPGA). This plot has an extremely similar pattern as the same plot for the FAA land communications SDR receiver design example trade space seen in Figure 5-36.

Figure 5-99: FM Parallel Coordinates—Max. Freq., Max. BW, MDS, Noise Figure, Gain

Figure 5-100: FM 2-D Scatter—DR vs. Price—IF Preference Shading w/ Curve Fitting
Figure 5-101 shows a plot of the system component price versus the system power dissipation for the FM radio receiver example. The image on the left shows the entire trade space, while the image on the right shows a smaller, more magnified view of the trade space. Like the direct comparability of Figure 5-100 to Figure 5-36, the patterns observed in Figure 5-101 are directly comparable to those observed for the FAA land communications receiver example in Figure 5-37 and Figure 5-38. These similar patterns and trends are also of significance to a designer seeking to understand the SDR receiver design trade space in general.

![Figure 5-101: FM 2-D Scatter—Price vs. Power—IF Preference Shading w/ Curve Fitting](image)

5.3. **Chapter Summary**

ATSV is used for visual exploration of the SDR receiver system design trade space resulting from sampling the SDR-RM. ATSV is also used to visualize the trade spaces within individual SR-CDs for simple, component-level trade space exploration.

Presented within this chapter is the visualization of a modified ADC SR-CD that included ADCs above 10 Msps. ATSV is used to explore the relationships, trends, and tradeoffs between different variables. Known relationships such as the direct relationship between SNR and bit resolution are confirmed, while other, less-known relationships are tested and explored. Brush
and preference controls are leveraged to demonstrate interactive exploration of the trade space with respect to design criteria specified by the user.

Also presented within this chapter is the visualization of SDR-RM output trade spaces for three hypothetical SDR receiver systems: (1) an FAA land communications receiver; (2) a GSM-850 receiver; and (3) an FM receiver. ATSV is used in each example to explore the SDR receiver design trade space. Known relationships, trends, and tradeoffs are investigated to demonstrate the functionality of the SDR-RM and ATSV. Some less-known relationships, trends, and tradeoffs are also investigated to demonstrate the usefulness of the model and tool. Additionally, in order to confirm the consistency of results, one variable pair with a known inverse relationship is examined for all three examples: RF front-end gain and RF front-end noise figure. Each example also has unique variable pair investigations to show different uses and findings of the SDR-RM and ATSV.

The FAA land communications example introduces several investigation methods. The GSM-850 example shows how individual component specifications from the SR-CDs can be included with system-level specifications for further relationship analysis. In particular, the GSM-850 example highlights several relationships and tradeoffs at the system-level due to ADC component-level selection. The FM example introduces the visualization of non-technical preference considerations (i.e., component preference and manufacturer preference).

The example results within this chapter demonstrate how ATSV and the SDR-RM can be used to visualize the SDR receiver design trade space, and show the usefulness of the results. Furthermore, these example results help to validate this work’s approach to SDR receiver design trade space visualization.
Chapter 6

Conclusions and Future Work

This work developed a Software-Defined Radio Receiver Model (SDR-RM) and demonstrated its use for trade space visualization of the SDR receiver design space using the existing ARL Trade Space Visualizer (ATSV) tool. Chapter 2 provided necessary background information. Chapter 3 discussed background on specific specifications and characteristics used for the modeling of SDR receiver design. Chapter 4 presented the primary contribution of the work, namely, the development of the SDR-RM and its linkage to ATSV for trade space exploration. Chapter 5 discussed results obtained through trade space visualization of the SDR receiver design trade space using the SDR-RM and ATSV. The purpose of this chapter is to conclude the work and provide suggestions for future work.

6.1. Conclusions

A primary goal in this work was to develop a method for and demonstrate the feasibility and usefulness of visualizing the SDR receiver design trade space for the purpose of trade space exploration involving the analysis of relationships, trends, and tradeoffs within the design space. The approach selected for trade space visualization using the existing ATSV tool presented in Chapter 4 is again presented in Figure 6-1.
SDR Receiver Component Databases (SR-CDs) were developed to provide a library of components available to a model of an SDR receiver. The SDR Receiver Trade Space Analysis Model (SR-TSAM) was developed to model single-RF-chain superheterodyne SDR receiver architecture design whereby components are sampled from the SR-CDs and placed into the blocks of the receiver block diagram for overall receiver output specification calculations and feasibility determinations based on basic user-defined inputs. Linking configuration files were created to link the SR-TSAM to the ATSV trade space visualization tool in a manner in which ATSV controls the SR-CD component samples and collects output data for visualization.

Many tests were run on the SDR-RM (comprising of the SR-CDs, SR-TSAM, and link to ATSV) to confirm the functionality of the model and to facilitate visualization with ATSV. Some of the results from three examples were presented in Chapter 5. Many of the results presented in Chapter 5 are visualization results that reflect various relationships, trends, and tradeoffs between SDR receiver specifications and characteristics that were easily predicted or known. These
results were pursued and presented to provide support for the validity and feasibility of the SDR-RM as well as to the overall approach taken to SDR receiver trade space visualization. In pursuing and explaining these results within Chapter 5, examples are also presented demonstrating the usefulness of ATSV-based trade space visualization of the SDR receiver design trade space as well as ways in which visualization can be effectively used.

The conclusion of this work is that the SDR-RM provides a solid foundation for future work in the field of trade space visualization of SDR receiver design. The model is in the early stages and represents a proof-of-concept version; however, the validity of the model and its use for visualization has been shown in Chapter 5, and, as explained in Chapter 4, is firmly based on realistic specification and compatibility determinations for SDR receivers presented in Chapter 3.

Trade space visualization of SDR receiver design alternatives can help designers understand and prioritize the numerous and complex multivariable design decisions they face in designing SDR receivers.

6.2. Future Work

The SDR-RM and the exercises and results pursued to demonstrate its functionality with ATSV are to be taken as proof-of-concept efforts. The efforts have laid the groundwork for and demonstrated the value of continuing development efforts in the area of trade space visualization of the SDR receiver design space with ATSV. It is an intent of this work to stimulate future work in this field. In particular several recommendations for future work are provided herein including work on the SR-CDs, work on the SR-TSAM, work on ATSV, and work on testing efforts.

SR-CD development must be a continual effort. It is recommended that SR-CDs be created for digital signal processing chips, antennas, and local oscillators so that they may be included in the SR-TSAM. It is also recommended that the SR-CDs be improved by eliminating
NaN and Null values within the databases and replacing them with actual values. SR-CDs should also be further improved by ensuring only like components are cataloged together. For example, LNA and RF Amplifier SR-CDs should be separated into amplifiers and variable gain amplifiers. SR-CDs should also include a more detailed breakdown of component and manufacturer preference criteria into such categories as sourcing risk, technical risk, etc. Any hardware associated with automatic gain control (AGC) besides variable gain amplifiers should also be cataloged into SR-CDs for inclusion in the SR-TSAM.

The SR-TSAM should also be continued to be improved. Antenna, local oscillator, AGC, and DSP chips should be built into the model including associated output specification calculations and compatibility determinations. Additional software versus hardware flexibility analysis beyond the simple existence or nonexistence the IF Conversion Block should be investigated and implemented (such as different AGC implementations). New compatibility checks should be added beyond the simple frequency, bandwidth, and voltage supply checks currently in place. New output specifications should be generated. Assumptions should be checked and improved upon. Certain calculations should be improved: in particular those that result in outliers. While, the component price values in the SR-TSAM are configured in a way that any NaN price values result in a price of $0.00 to be filtered out in ATSV, several others do not perform this check causing limited but nevertheless existent faulty outliers in the resulting trade space. Some type of digital resource analysis component involving the needs of the FPGA and possibly DSP should be implemented. Digital resource analysis as well as the modeling of compatibility and specifications might also be outsourced to external, more complex models (e.g., RF modeling, etc.) that report back to the SR-TSAM. The SR-TSAM should also be developed into different versions with different architectures or to have differing architecture options within single versions.
Several improvements to ATSV would improve the visualization process with the SDR-RM. While the SDR-RM was built to fit with ATSV, certain limitations were unavoidable. One limitation that should be addressed is ATSV’s limitation on quantitative analysis of mappings between variable pairs. Currently, mappings cannot be found between variables in just segments (i.e., variable ranges) of the trade space without reloading exported databases, which prevents real-time analysis during Exploration Engine sampling and may limit analysis of other variables in the same trade space. The process for focusing sampling on particular discrete value ranges could be improved within the Exploration Engine. Given that the SDR-RM leverages discrete input values, it would be useful to adjust the ranges of these values on-the-fly during sampling without the need to individually check or uncheck values (this is to enable focused sampling of designs without IF Conversion Blocks).

It is also hoped that continued work will be made on the testing of the SDR-RM with ATSV. It is hoped that as the architecture options improve for the SR-TSAM, many existing, actual SDR designs will be simulated with the SDR-RM so that existing designs can be viewed within a trade space to determine how close an existing design is to Pareto frontiers and most preferred values. This will further provide insight into the functionality of the model and ATSV as well as provide a basis for future use during the actual design of SDR receiver systems whereby designers can compare design concepts to segments of the trade space and can evaluate trends and tradeoffs easily.
## Appendix A

### List of Acronyms and Abbreviations

<table>
<thead>
<tr>
<th>Acronym</th>
<th>Description</th>
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<tbody>
<tr>
<td>2-D</td>
<td>Two-Dimensional</td>
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<tr>
<td>3-D</td>
<td>Three-Dimensional</td>
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<tr>
<td>ACS</td>
<td>Adjacent Channel Selectivity</td>
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<tr>
<td>A/D</td>
<td>Analog-to-Digital</td>
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<tr>
<td>ADC</td>
<td>Analog to Digital Converter</td>
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<tr>
<td>ADHB</td>
<td>Amplifier Default Half BW % *</td>
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<tr>
<td>AGC</td>
<td>Automatic Gain Control</td>
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<tr>
<td>ARL</td>
<td>Applied Research Laboratory</td>
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<tr>
<td>ASIC</td>
<td>Application Specific IC</td>
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<tr>
<td>ATSV</td>
<td>ARL Trade Space Visualizer</td>
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<tr>
<td>BB</td>
<td>Baseband</td>
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<tr>
<td>BER</td>
<td>Bit Error Rate</td>
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<tr>
<td>BPF</td>
<td>Band-Pass Filter</td>
</tr>
<tr>
<td>BW</td>
<td>Bandwidth</td>
</tr>
<tr>
<td>COTS</td>
<td>Commercial Off-The-Shelf</td>
</tr>
<tr>
<td>CSV</td>
<td>Comma Separated Values</td>
</tr>
<tr>
<td>D/A</td>
<td>Digital-to-Analog</td>
</tr>
<tr>
<td>DAC</td>
<td>Digital to Analog Converter</td>
</tr>
<tr>
<td>DDC</td>
<td>Digital Downconverter</td>
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<tr>
<td>DDR</td>
<td>Digital Drop Receiver</td>
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<tr>
<td>DDS</td>
<td>Direct Digital Synthesizer</td>
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<tr>
<td>DE</td>
<td>Differential Evolution</td>
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<tr>
<td>DNL</td>
<td>Differential Nonlinearity</td>
</tr>
<tr>
<td>DR</td>
<td>Dynamic Range</td>
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<tr>
<td>DSP</td>
<td>Digital Signal Processing</td>
</tr>
<tr>
<td>ENOB</td>
<td>Effective Number of Bits</td>
</tr>
<tr>
<td>F</td>
<td>Noise Factor</td>
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<tr>
<td>FAA</td>
<td>Federal Aviation Administration</td>
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<tr>
<td>FFT</td>
<td>Fast Fourier Transform</td>
</tr>
<tr>
<td>FIR</td>
<td>Finite Impulse Response</td>
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<tr>
<td>FM</td>
<td>Frequency Modulation</td>
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<tr>
<td>FPGA</td>
<td>Field-Programmable Gate Array</td>
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<tr>
<td>GC</td>
<td>Gain Compression</td>
</tr>
<tr>
<td>GRC</td>
<td>Glenn Research Center (NASA)</td>
</tr>
<tr>
<td>GSM</td>
<td>Global System for Mobile Communications</td>
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<tr>
<td>HR</td>
<td>Hardware Radio</td>
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<tr>
<td>HTML</td>
<td>HyperText Markup Language</td>
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<tr>
<td>I/Q</td>
<td>In-phase &amp; Quadrature</td>
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<tr>
<td>IC</td>
<td>Integrated Circuit</td>
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<tr>
<td>IF</td>
<td>Intermediate Frequency</td>
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<tr>
<td>IMD</td>
<td>Intermodulation Distortion</td>
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<tr>
<td>INL</td>
<td>Integral Nonlinearity</td>
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<tr>
<td>Abbreviation</td>
<td>Description</td>
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<tr>
<td>IP</td>
<td>Intermodulation Product</td>
</tr>
<tr>
<td>ISR</td>
<td>Ideal Software Radio</td>
</tr>
<tr>
<td>JTRS</td>
<td>Joint Tactical Radio System</td>
</tr>
<tr>
<td>LNA</td>
<td>Low Noise Amplifier</td>
</tr>
<tr>
<td>LO</td>
<td>Local Oscillator</td>
</tr>
<tr>
<td>LPF</td>
<td>Low-Pass Filter</td>
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<td>MAS</td>
<td>Maximum Allowable Signal</td>
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<td>MDS</td>
<td>Minimum Detectable Signal</td>
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<td>MDHB</td>
<td>Mixer Default Half BW % *</td>
</tr>
<tr>
<td>MIL-STD</td>
<td>United States Military Standard</td>
</tr>
<tr>
<td>MIPS</td>
<td>Millions of Instructions / Second</td>
</tr>
<tr>
<td>NCO</td>
<td>Numerically Controlled Oscillator</td>
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<td>NF</td>
<td>Noise Figure</td>
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<td>NRE</td>
<td>Non-Recurring Engineering</td>
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<tr>
<td>PDC</td>
<td>Programmable Downconverter</td>
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<tr>
<td>PG</td>
<td>Processing Gain</td>
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<tr>
<td>PoC</td>
<td>Proof of Concept</td>
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<tr>
<td>PSD</td>
<td>Power Spectral Density</td>
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<tr>
<td>RAM</td>
<td>Random Access Memory</td>
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<tr>
<td>RF</td>
<td>Radio Frequency</td>
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<tr>
<td>RMS</td>
<td>Root Mean Squared</td>
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<tr>
<td>RSS</td>
<td>Received Signal Strength</td>
</tr>
<tr>
<td>RT</td>
<td>Reconfigurable Transceiver</td>
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</table>
Appendix B

SR-TSAM Image

[Large image of SR-TSAM on following page for reference]
Figure B.1: The SR-TSAM Without Component Inputs Section With Example Values

Single RF Chain Superheterodyne SDR Receiver Without Analog IF Conversion (Possible Digital IF Conversion)

Manufacturer Preference Index 2.00

Component Preference Index 0.00

Maximum Frequency (MHz) 210

Maximum Bandwidth (MHz) 80

Antenna Gain (dB) 54.86

Antenna Impedance (ohms) 116.67

BB Stage

RF Stage

Gain (dB) 2.15

Voltage Supply (V) 5.0

Sampling Rate Factor 2.5

Sub-Sampling Allowed 0

Assumed Filter Insertion Loss if Missing (dB) 2.0

Voltage Supply Compatibility NOT MODELED

Bandwidth Compatibility NOT MODELED 1 1 1 NOT MODELED 1 1 1

Part Number

Database Component Number

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Key Signal Inputs

Proof-of-Concept SDR Receiver Trade Space Analysis Model

Compatibility Key

1 - Compatible 0 - Not Compatible 99 - N/A (Excluded)

Model I/O Color

Component Compatibility Determination

Antenna BPF (RF) LNA RF Mixer LO BPF (IF) RF Amp ADC FPGA DSP

Trade Space Analysis Model

Proof-of-Concept SDR Receiver

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References


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