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2D ELECTROSTRICTIVE FET BASED CIRCUITS: COMPACT MODELING AND DEVICE-CIRCUIT CO-DESIGN

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ABSTRACT

2D Electrostrictive FET (EFET) is an emerging steep switching device with immense potential to replace conventional MOSFETs. EFET has 4-terminals: gate (G), source (S), drain (D) and back contact (B). An electrostrictive material (EM) is sandwiched between gate and back contact of the EFET. EM exhibits longitudinal expansion on application of voltage (V_{GB}) across it inducing pressure on 2D channel material. This results in bandgap modulation and its steep switching (sub 60mV/dec) characteristics.

In this work, we present a Verilog A based compact model of EFET that solves the governing equations of electrostrictive effect and 2D electrostatics/channel transport self-consistently. With this model we perform simulations of EFET device characteristics and EFET based circuits (using HSPICE). We observe 163% increase in ON current and 9% decrease in sub threshold swing (SS) in EFET compared to 2D FET. By virtue of its unique operating mechanism and structure, EFET presents several opportunities for optimization. We show that band-bending (hence EFET device characteristics) can be effectively optimized through: (i) Strain Transduction Coefficient (STC which is related to electrostrictive and 2D material) and (ii) back voltage (V_B). We show 42% decrease in SS and 7.5X increase in I_{ON} by increasing STC=2856 eV-pm/V (70% transduction efficiency). In addition, by modulating V_B=-0.6V, I_{ON} increases by 2.8X.

The steep switching and greater drive strength of EFETs is accompanied by capacitance overheads due to - (i) electrostrictive dielectric (C_{GB}) and (ii) parasitic capacitance ($C_{GD,}$ C_{GS}). A potential outcome of this is higher delay in EFET circuits. Our study shows the possibility of enhancement in performance/stability/energy efficiency of EFET circuits by co-optimization of STC and V_B of EFETs. Precisely, this work focuses on thorough analysis and device-circuit co-optimization of the following EFET based circuits: (i) ring oscillator (RO) and (ii) SRAM.

Through transient analysis of 7-stage EFET based ring oscillator (RO) we investigate the influence of capacitance driven delay in EFET circuits compared to 2D FET circuits. Firstly, we study energy-delay in RO with ideal 2D/EFET (ignoring parasitic capacitances: C_{GB}/$C_{GD/S}$). We observe 1.15X lower delay than the 2D FET RO at iso-energy. Parasitic capacitances (C_{GB}/$C_{GD/S}$) considered, EFET RO performs 1.2X slower than 2D FET RO at iso-energy. Increased delay is

result of large $C_{GD/S}$ overlap capacitances (higher than $C_{GD/S}$ in 2D FET) in preliminary EFET structure (EFET 1). To improve energy-delay performance, we propose EFET 2 with $C_{GD/S}$ comparable to 2D FET. However, EFET 2 RO shows 2.26X larger delay compared to 2D FET RO due to inherent C_{GB}. STC optimization of EFET 2 RO helps achieve 1.7X lower energy at iso-delay (at 70% transduction efficiency). We also note that the EFET 2 RO shows energy-delay benefits over 2D FET RO in wire capacitance dominated (Cw>2fF) circuits.

Finally, we study EFET based SRAMs with (i) EFET as drop-in replacement (EFET SRAM-I) and (ii) EFET with separate V_B for access transistor (EFET SRAM-II). Based on our initial device analysis with STC and V_B, we propose EFET SRAM-II since this design permits their co-optimization. Analysis of SRAM-I and SRAM-II are carried out individually for EFET 1 and EFET 2. First, we compare EFET 1 SRAM-I with EFET 2 SRAM-I. We conclude better performance characteristics of the latter which we summarize as: 15% lower read time at comparable read stability and 3% decrease in write time (compared to 2D FET SRAM). STC optimization of EFET 2 SRAM-I leads to 50% decrease in read time, 33% increase in noise margin and 6% decrease in write time (compared to 2D FET SRAM) at 70% transduction efficiency.

Applying V_B and STC co-optimization in EFET SRAM-II, both EFET 1 and EFET 2 based configurations display drastic improvements. 20% and 70% increase in read noise margin is observed at STC=2856 eV-pm/V (70% efficiency) with V_B=0V for EFET 1 SRAM-II and EFET 2 SRAM-II respectively. With V_B=0.6V and STC=2856 eV-pm/V, 30% and 50% reduction in write is seen in EFET 1 SRAM-I and EFET 2 SRAM-II respectively.

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Chapter 1

INTRODUCTION

1.1 Motivation for Steep Switching Devices

Ever since the inception of metal oxide semiconductor field effect transistor (MOSFET), the electronics industry is driven by scaling of devices. In today's industry, the demand for low power, high performance circuits is immense for personal computing, wireless communication and biomedical applications. Moore's law has been the binding rule for scaling witnessed by the industry [1]. The two aspects of scaling are: dimension scaling and voltage scaling [2-3]. In the initial era of Dennard scaling, dimension scaling allowed the number of transistor per chip to increase by 1000000x and consequently their speed to increase by 1000x. Voltage scaling kept the power density practically constant throughout this scaling regime [4]. However, post Dennard scaling, voltage scaling has stopped due to non- scalability of the subthreshold swing (SS) to below 60mV/decade arising out of Boltzmann statistics. Dimension scaling, however, continued beyond this era leading to increase in power density. The power dissipation of a CMOS based circuit can be expressed as [4]

$$P=f_{clk}.\alpha.C_{tot}.V_{DD}^{2}+V_{DD}.I_{sc}+V_{DD}.I_{leakage} \quad (1)$$

Where, f_{clk} is the clock frequency, α is the average switching activity, C_{tot} is the total capacitance, I_{sc} is the short circuit current between rail to rail supply and $I_{leakage}$ is the leakage current. The dynamic power is directly proportional to the square of the supply voltage, and short circuit power is proportional to the supply voltage. Further, the leakage current depends exponentially on the supply voltage. Hence, supply voltage (V_{DD}) scaling is extremely important for low-power circuit design. However, lowering V_{DD} affects the circuit speed drastically. By lowering the threshold voltage (V_{TH}), the performance of the circuits at low V_{DD} can be improved. However, this comes at

the cost of higher leakage. To mitigate the performance-leakage trade-offs, lowering SS<60mV/dec has been the research focus in the recent past. Devices that exhibit such characteristics are called steep switching devices. Steep switching devices exhibit higher I_{ON}/I_{OFF}, hence perform better than CMOS devices [5-10].

Several steep slope devices, e.g., tunneling FETs, piezoelectric strain modulated Si FinFETs, negative capacitance ferroelectric FETs, excitonic FETs and spin-based FETs [11-17] have emerged in the recent past. TFETs are a mature concept in steep switching devices. However, the greatest challenge for tunneling FETs is that their low ON state current densities are limited by large tunneling barriers. TFETs show huge potential for scaling supply voltages and for bringing down the power consumption [18-21]. However, since TFETs are unidirectional devices and have asymmetric current conduction, therefore, design of TFET based SRAM cells and other circuits is still challenging [19-21]. Piezoelectric strain modulated Si FinFETs are also promising but suffers from the limitation of bulk nature of Si at the scaling limits. Another promising candidate for steep switching devices is the Ferroelectric FETs (FEFET). FEFET employs negative capacitance in FE layer in the gate stack to achieve <60 mV/dec subthreshold swing (SS). Due to the presence of this layer, the gate capacitance increases which could adversely affect the delay [14, 22-25]. Hence, there are avenues for new steep switching device concepts and their thorough study.

The other aspect of scaling is the channel length scaling. Scaling in Si devices are limited due to the bulk nature of the material. Aggressive scaling in such devices are associated with loss of electrostatic control and short channel effects, e.g., drain induced barrier lowering, etc. Hence for length scaling, low dimensional systems like nanotubes, nanowires, nanosheets [26-31] are being considered as alternative materials to Si. Such materials permit enhanced scaling while maintaining good electrostatic control.

The objective for devices post CMOS are as following: SS slope should be as low as possible to meet the low power requirement whereas the ON current should be sufficiently high to

meet the targeted performance. In this context, 2D layered semiconductors have received significant attention as possible candidates for post-Si electronics owing to their ultra-thin body nature that allows aggressive channel length scaling and hence, high performance [27-31]. Moreover, recent experimental and theoretical studies show that the bandgap of multilayer transition metal dichalcogenides (TMDs) like MoS_2, WSe_2 etc. can be dynamically reduced to zero by applying out-of-plane stress [32,33]. Aggressive scalability of 2D materials combined with bandgap modulation has been combined to propose the disruptive device called the 2D Electrostrictive FET (2D EFET) [34].

1.2 2D Electrostrictive FET (EFET) With Bandgap Modulation

The device structure of a 2D EFET resembles a conventional 2D FET with the exception that the gate is coupled with an electrostrictive material through a back contact. The operating principle, however, differs significantly since an EFET operates on the principle of dynamic bandgap (E_G) modulation of 2D channel enabled by voltage induced strain transduction. The electrostrictive material undergoes longitudinal expansion when an electric field is applied and transduces an out-of-plane stress on the 2D channel material, e.g., MoS2, WSe2, etc. Since these are layered materials with strong in-plane covalent bonds and out-of-plane weak Vander Waal's forces, applying pressure along the Vander Waal's forces can monotonically reduce bandgap in them. Thus, in the OFF state, the 2D EFET operates with a large bandgap and prevents current conduction whereas in the ON state, it operates with a smaller or zero bandgap and increases conductivity [32-34]. The fascinating aspect of 2D EFET is that it offers steep SS below 60mV/decade owing to an internal feedback mechanism giving rise to voltage amplification and at the same time provides significantly higher ON state current density.

1.3 This Work

The recently proposed 2D EFET [34] is currently evolving. While experimentalists are exploring the fabrication methods and techniques for optimizing the device performance, it is vital to study the device characteristics and circuit performance of the device to identify the design space for its optimization. The design time optimizations identified during simulations could lead to improved fabricated devices in later versions. To enable such study of the EFET, we develop a circuit compatible a model of the 2D EFET in Verilog-A for SPICE simulations of 2D EFET based circuits. Using this model, we study the phenomenon of band-gap change in 2D materials and its effect on current-voltage characteristics of 2D EFETs. We evaluate the various parameters that lead to optimization of the device. We categorize this study into design time optimization through enhancing the material related parameters of the electrostrictive and 2D material and run time optimization by modulating the voltage of the back contact. This part of the study is presented in Chapter 2.

The structure of the EFET and the presence of the electrostrictive material leads to overheads e.g., increased capacitance in the EFET which affects delay. We perform delay analysis using a 7 stage ring oscillator. Here, we also consider the other sources of delay – (i) parasitic capacitance, (ii) transduction delay in the electrostrictive material and (iii) circuit delay. We study energy delay trends of ring oscillator with the above factors and suggest methods to optimize the same at design and run-time. This work is presented in Chapter 3.

In Chapter 4, we present the EFET based SRAMs. We begin this analysis by comparing whether EFET devices can replace CMOS devices in SRAM design. Our study reveals that a drop-in replacement does not yield an optimal solution. We propose an alternative SRAM design and study its operations – read time and stability; write time. Finally, we propose methods to improve trade-off in the operation metrics by means of *STC*-V_B co-optimization.

Finally, we revisit the contributions, results and improvements in this work in Chapter 5 and discuss the possibilities of future study.

Chapter 2

Circuit Compatible Model of 2D EFET and Device Analysis

2.1 Introduction

The 2D EFET (Fig. 2-1(a)) is a novel, aggressively scalable, steep switching transistor [34] that consists of 4 terminals, viz. - source (S), drain (D), gate (G) and back contact (B). The channel is realized with mono/multilayer transition metal di-chalcogenides (TMD), e.g., MoS_2/WSe_2. Several works [32-33] have demonstrated the possibility of bandgap change in 2D materials by applying an out-of-plane pressure. This is possible due to weak inter layer forces in 2D materials. The applied pressure reduces the inter-layer distance between the consecutive layers of the semiconducting 2D material [32], thereby dynamically reducing its bandgap. The 2D EFET utilizes dynamic bandgap (E_G) modulation in its 2D channel to achieve sub 60mV/dec subthreshold swing (SS). An electrostrictive material (EM) between the gate (G) and back terminal (B) in 2D-EFET makes bandgap reduction (ΔE_G) achievable. When voltage V_{GB} is applied across EM, it leads to expansion of EM that transduces out-of-plane stress (or pressure) on the 2D channel materials, e.g., MoS2, WSe2, etc. diminishing its bandgap [34] similar to Fig. (2-2(b)). Consequently, 2D-EFET shows

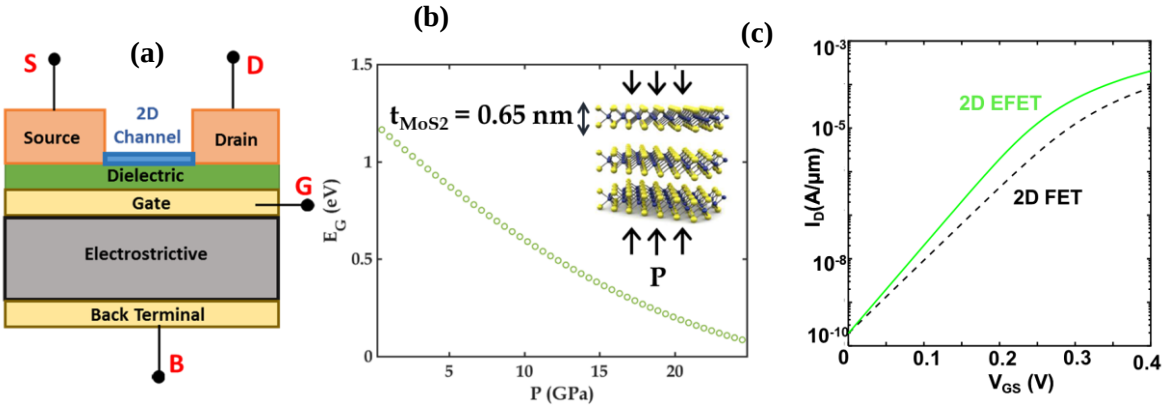

Figure 2-1 (a) Device structure of 2D EFET (b) Bandgap variation with applied pressure in MoS_2 [32] (c) Steep switching in 2D EFET

sub 60mV/dec sub-threshold swing (SS) and higher ON current (I_{ON}) (Fig. 2-3(c)). The steep switching behavior enables aggressive voltage scaling, which, with proper device-circuit co-design, leads to ultra-low power and robust circuit operation.

2.2 Electrostrictive Transduction in 2D Channel

The core of the EFET is the phenomenon of development of strain in the electrostrictive material and its translation to the 2D channel. In this section, we study the mechanism of strain in piezoelectric/electrostrictive material. Piezoelectric/electrostrictive materials are uniquely known to expand along the direction of applied potential. This is attributed to positive strain in the material as given by (2.1). Strain experienced by such a material is directly proportional to the electric field across it which is given by (2.2(a-b)), the proportionality constant being a material dependent parameter. For piezoelectric/electrostrictive material this is given by piezoelectric/electrostrictive constant (d_{33}/e_{33}) respectively. It is important to note that while piezoelectric materials demonstrate linear strain (2.2(a)) response with applied potential, electrostrictive materials display quadratic behavior [34]. Equation (2.2(b)) and Fig. 2-2(b)) illustrates this strain response.

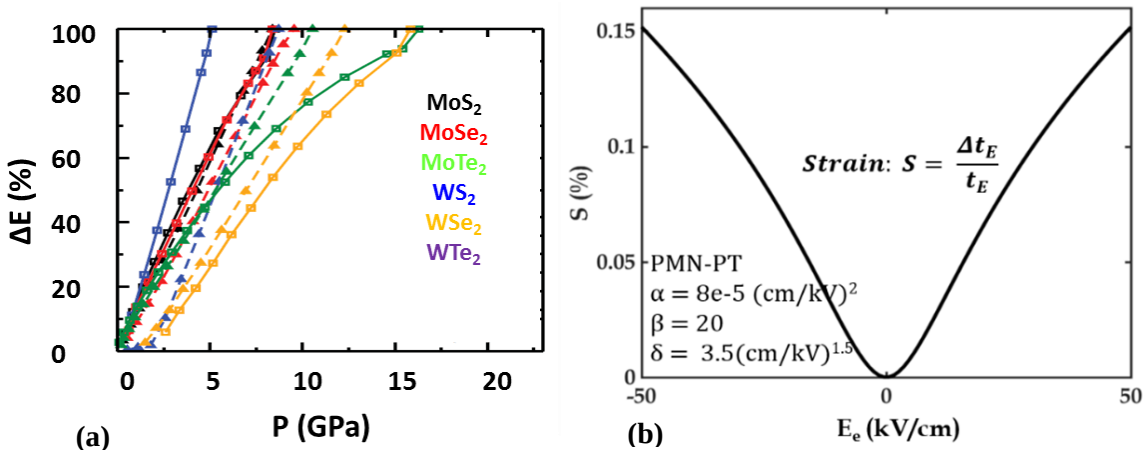

Figure 2-2 (a) Change in bandgap with applied pressure in 2D materials [32] (b) Strain (S) versus electric field (E_e) characteristics of an electrostrictive material (PMN-PT) [34]

$$\boldsymbol{Strain(S) = \frac{\Delta t_e}{t_e}} \quad (2.1)$$

$$\boldsymbol{Strain\ in\ Piezoeletric\ Material\ (S_P) = d_{33}E} \quad (2.2(a))$$

$$\boldsymbol{Strain\ in\ Electrostrictive\ Material\ (S_E) = e_{33}E^2} \quad (2.2(b))$$

Stress in electrostrictive material is ultimately felt as pressure (P) in 2D material. The strain from the electrostrictive material is transduced to the 2D material through the gate metal and dielectric resulting in some loss. This is accounted by the strain transfer coefficient η such that $\eta = \frac{\Delta t_{2D}}{\Delta te}$ and $0 < \eta < 1$. This results in the out-of-plane pressure in the 2D material which is expressed by (2.3). C_{33} is the 2D out-of-plane compliance parameter that captures the conversion of strain to pressure. t_e and t_{2D} is the thickness of electrostrictive material and 2D material respectively, S is the strain in the electrostrictive material and η is the % of strain transfer from electrostrictive to 2D material [34].

$$\boldsymbol{P = (\eta)\left(C_{33}\frac{te}{t_{2D}}\right)S} \quad (2.3)$$

The weak out-of-plane Vander Waals' forces binding the layers 2D materials [32] experience pressure, P which leads to reduction of the distance between the layers. This leads to reduction of band-gap in the 2D material. The change in bandgap with pressure is given by (2.4) where α and χ are material parameters [34].

$$\boldsymbol{\Delta E_G = \alpha P - \chi P^2} \quad (2.4)$$

The above described mechanism is depicted as a flow chart in Fig. (2-3)

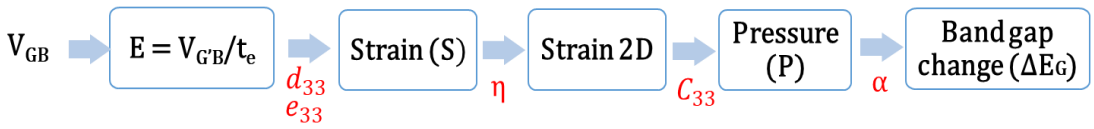

Figure 2-3 Flow chart of transduction of electrostrictive action and band gap change in 2D channel.

2.2 Modeling of 2D EFET

The EFET has been conceptualized with its future application in low-power/energy and efficient logic and memory systems. It is pertinent to first study the performance of the EFET through modeling and simulation before it can be used a as fundamental block in digital systems. We develop a circuit compatible model for n- and p-type 2D EFETs in Verilog-A. The model can be used for circuit simulation using HSPICE. The following effects are modeled to constitute the 2D EFET model:

1. Actuation of electrostriction in the electrostrictive material
2. Transduction of electrostriction to the 2D material and band gap change
3. Current transport in EFET
4. Parasitic capacitance in EFET

2.2.1 Modeling of actuation of electrostriction in the electrostrictive material

We model the actuation of electrostriction in terms of strain as described by (2.2 (a, b)). Although the EFET is conceived with Electrostrictive material PMN-PT for optimal strain, experiments till now have been carried out on piezoelectric material PZT due to the relative ease in preparing PZT sol-gel solutions and the film growth [42]. We generalize the strain equation in our model to be applicable to both sets of materials as in (2.5). $d_{33}/e_3=0$ if the material is electrostrictive /piezoelectric respectively.

$$\boldsymbol{S = S_P + S_E = d_{33}E + e_{33}E^2} \tag{2.5}$$

2.2.2 Modeling of transduction of electrostriction to 2D material and band gap change

In section 2.1, we explain in detail the mechanism of development of strain in electrostrictive material and its translation to 2D channel. We also describe that the bandgap in the 2D material changes as a result of the pressure. Equation (2.4) represents this phenomenon mathematically. The final expression of ΔE_G can be obtained by substituting the expression of Pin (2.3) in (2.4). The impact of $\boldsymbol{\chi}$ is minimal and hence is assumed =0 in this analysis. Further, (2.5) is used for strain, S. Hence, ΔE_G can be written as,

$$\Delta \boldsymbol{E_G} = \boldsymbol{\alpha C_{33}\, \eta \frac{t_e}{t_{2D}}\, d_{33}\, E} + \boldsymbol{\alpha C_{33}\, \eta \frac{t_e}{t_{2D}}\, e_{33} E^2} \tag{2.6}$$

We model the bandgap change (ΔE_G) in Verilog A as a voltage controlled voltage source by expressing the electric field (E) in (2.7) in terms of the applied potential across the electrostrictive material (V_{GB} in Fig. (2-2(a)) as $\left(E = \frac{V_{GB}}{t_e}\right)$. Hence, the final expression of ΔE_G in our model is as shown below

$$\Delta \boldsymbol{E_G} = \boldsymbol{\frac{1}{t_{2d}}\left(\alpha C_{33}\, \eta d_{33}\, V_{GB} + \alpha C_{33}\, \eta e_{33} \left(\frac{{V_{GB}}^2}{t_e}\right)\right)} \tag{2.7}$$

In our further analysis, we focus on improving ΔE_G for better EFET characteristics by virtue of two broad aspects of circuit optimization - (A) Design time and (B) Run time**.** In (2.7) parameters $\boldsymbol{\alpha, C_{33}, \eta, d_{33}}$ all relate to properties of either the electrostrictive/2D materials. Hence, optimization of these are taken care of at design time. We group $\boldsymbol{\alpha C_{33}\, \eta d_{33}}$ into a parameter called the Strain Transduction Coefficient (STC) and $\boldsymbol{\alpha C_{33}\, \eta e_{33}}$ is referred to as Strain Transduction Electrostrictive Coefficient (STEC) to study the material properties of the 2D EFET. Run time optimization is realized by tuning $V_{GB.}$

$$\Delta \boldsymbol{E_G} = \boldsymbol{\frac{1}{t_{2d}}\left(STCV_{GB} + STEC\left(\frac{{V_{GB}}^2}{t_e}\right)\right)} \tag{2.8}$$

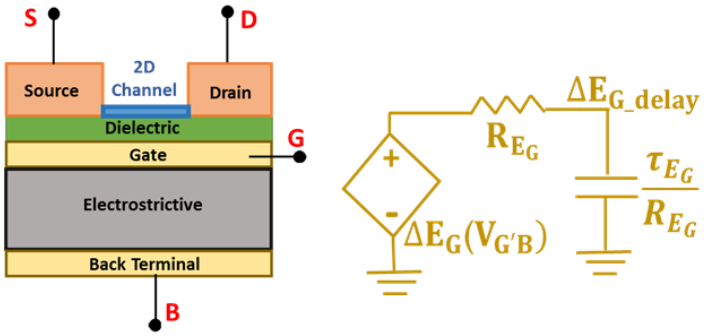

Figure 2-4 Schematic of EFET and modeling of electrostrictive action and band gap change in 2D channel.

For the incorporation of (2.8) in the model, we consider generic asymmetric movements of the conduction and valence bands. In other words, if the bandgap reduces by $\Delta \boldsymbol{E_G}$, the conduction band moves down by $\eta_C \Delta \boldsymbol{E_G}$ (where $0 < \eta_C < 1$) and the valence band moves up by $(1-\eta_C)\Delta \boldsymbol{E_G}$. For η_C equal to ½, the band movements are symmetric, which is considered in this work.

It is important to note here that there is a delay ($\boldsymbol{\tau_E}$) associated with appearance of ΔE_G when V_{GB} is applied. This delay occurs in the electrostrictive material due to finite time required for strain (or change in electrostrictive material thickness, Δt_e) to develop. The time taken depends on the speed of the acoustic wave propagation (v_e) in the electrostrictive material [34] and the thickness of the material. The network diagram for the delay in band gap change is shown in Fig. (2-4). The delayed bandgap change ($\Delta \boldsymbol{E_{G\_Delay}}$) can thus be expressed as in (2.9). In the model, $\boldsymbol{\tau_E}$ is modeled using resistor (R_{EG})-capacitor ($C_{EG}=\frac{\tau_{EG}}{R_{EG}}$) delay network R_{EG} and C_{EG}.

$$\Delta \boldsymbol{E_{G\_Delay}} = \Delta \boldsymbol{E_G}\left(\mathbf{1} - \boldsymbol{e}^{\frac{-\boldsymbol{t}}{\boldsymbol{\tau_{E_G}}}}\right) \tag{2.9}$$

2.2.3 Current transport model in EFET

Our aim is to develop a circuit compatible compact model of the 2D EFET. We base our current transport on the capacitance network based model (Fig. (2.5)) similar to what has been

demonstrated in [43]. It is important to note that the transport mechanism in EFET is similar to that of a conventional 2D FET, with the effect of change in bandgap incorporated seamlessly into it. This effect reflects as an increase in channel charge Q_{CH} which impacts the drain current I_{DS}. The transport in EFET is a self-consistent solution of two independent models – 1. Transport in 2D FET and 2. Bandgap change in electrostrictive material

a) Transport in 2D FET

The 2D FET is modeled using a capacitance network and voltage controlled voltage source, as highlighted in Fig. (2-5). Here, C_{OX}, C_{CH}, C_{IT} refer to gate-oxide capacitance, channel capacitance (arising due to the channel charge and voltage across the channel) and capacitance due to trap charges. V_{FB} is the flat band voltage required for gate work function engineering. Channel capacitance (C_{CH}) can be thought as $C_{CH}=\frac{dQ_{CH}}{dV_{CH}}$, where V_{CH} is the channel potential. Q_{CH} at

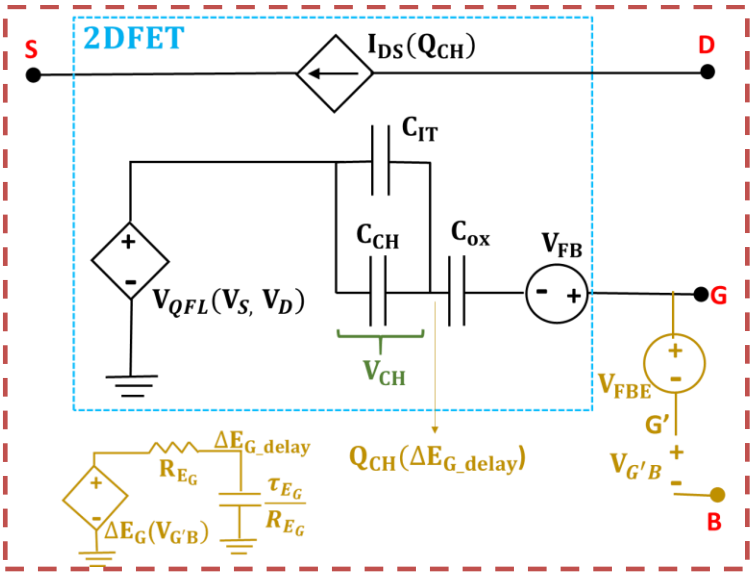

Figure 2-5 Capacitance network of EFET.

source/drain is obtained using 2D density of states (DOS_{2D}) and fermi statistics (f(E)) at source and drain, taking into account the K and Q valleys as shown in (2.11). [44] reports carrier occupancy in different valleys in 2D materials, e.g., MoS_2 and WSe_2.

$$\mathbf{Q_{CH(S,D)}(E) = q.\, n_{2D} = q.\int_{E_0}^{\infty} DOS_{2D}(E).\, f_{(S,D)}(E)\, dE} \tag{2.10}$$

$$\mathbf{DOS_{2D} = DOS_K + DOS_Q e^{\frac{-\Delta E_{KQ}}{kT}}} \tag{2.11}$$

$$\mathbf{f_{(S,D)}(E) = \frac{1}{1 + exp(qV_{QFL(S,D)} - E_O)}} \tag{2.12}$$

The analytical expression of Q_{CH} obtained after solving (9) and (10) is –

$$\mathbf{Q_{CH(S,D)}(E) = -qN_{2D} \ln(1 + \exp \frac{qV_{QFL(S,D)} - E_O}{kT})} \tag{2.13}$$

Where the subscripts S/D stand for source/drain, $\boldsymbol{E_O}$ is the conduction band and $\boldsymbol{V_{QFL(S,D)}}$ (Fig. (2-5)) is the quasi fermi level at the source/drain [43]. V_{QFL} is a voltage controlled voltage source and it is function of the applied bias at the terminal. The expression for V_{QFL} is provided in (2.14(a-b)) [43].

$$\mathbf{V_{QFL(S)} = \frac{Q_{CH,S}(E)}{C_{OX}} + V_{GS} - V_{FB}} \tag{2.14(a))}$$

$$\mathbf{V_{QFL(D)} = \frac{Q_{CH,D}(E)}{C_{OX}} + V_{GS} - V_{FB} - V_{DS}} \tag{2.14(b))}$$

An interesting observation from (2.13), (2.14(a-b)) is that Q_{CH} and V_{QFL} are dependent on each other. Hence, a self-consistent solution is required to obtain Q_{CH} and V_{QFL}. Once Q_{CH} and V_{QFL} are calculated, they can be used to determine the current. Current is calculated by means of continuity equations that are based on drift-diffusion transport (2.15). They are solved self-consistently with electrostatics and carrier densities in the channel. The channel charge in the 2D material (Q_{CH}) is obtained using 2D density of states (DOS_{2D}) and fermi statistics (f(E)), taking into account the K and Q valleys.

$$\mathbf{I_{DS\_2DFET} = WQv = \frac{\mu W}{L}\int_{V_D}^{V_S} Q_{CH}(E)\frac{dV_{QFL}}{dV_{CH}} dV_{CH}} \tag{2.15}$$

Here, q is the electronic charge, n_{2D} is the electron concentration, N_{2D} is the effective density of states, kT is the thermal energy, $DOS_{K/Q}$ are the density of states for K and Q valleys and ΔE_{KQ} is the energy difference between K and Q valleys. This approach for modeling of 2D FETs is similar

to S2DS model from Stanford [44], albeit with requisite modifications for the EFET structure. To account for non-idealities, channel charge in our model is considered to consist of fixed trap charge apart from the conduction charges via capacitance $C_{IT.}$

b) Integration of bandgap change in Electrostrictive material with current transport

For 2D EFETs, the electrostatics and transport equations are solved in conjunction with the models for electrostrictive effect. The electrostrictive effect is incorporated into the current equation by virtue of the channel charge, $\mathbf{Q_{CH}}$. Hence, in the 2D EFET the channel charge is a function of the diminished band gap (E_G-ΔE_G).

$$\mathbf{Q_{CH}}(\mathbf{E},\ \boldsymbol{\Delta \mathbf{E}_{G\_Delay}}) = \mathbf{q}.\mathbf{n_{2D}} = \boldsymbol{q}.\int_{\mathbf{E_0}}^{\infty} \mathbf{DOS_{2D}}(\mathbf{E}).\mathbf{f}\left(\mathbf{E},\ \boldsymbol{\Delta \mathbf{E}_{G\_Delay}}\right)\mathbf{dE} \tag{2.16}$$

$$\mathbf{I_{DS\_EFET}} = \mathbf{WQv} = \frac{\mu \boldsymbol{W}}{\boldsymbol{L}} \int_{V_D}^{V_S} \boldsymbol{Q_{Ch}}(\mathbf{E},\ \boldsymbol{\Delta \mathbf{E}_{G\_Delay}}) \frac{\boldsymbol{dV_{QFL}}}{\boldsymbol{dV_{CH}}} \boldsymbol{dV_{CH}} \tag{2.17}$$

All the constituent equations are self-consistently solved in Verilog-A to obtain the current-voltage and capacitance-voltage characteristics.

2.2.4 Parasitic Capacitance

The model also accounts for parasitic capacitances such as the fringe capacitance and gate-source/drain overlap capacitances. The parasitic capacitance for the structure in Fig. (2-1) arises from gate-drain and gate-source overlap shown as $C_{GS,OV}$ and $C_{GD,OV}$ and gate-back contact capacitance due to the electrostrictive material, C_{GB} as shown in Fig. (2-6). From our calculations, $C_{GB}=\frac{\epsilon_E WL}{t_e}$=0.71fF, $C_{OX}=\frac{\epsilon_{ox} WL_G}{t_{ox}}$=0.74fF and $C_{GD/S,OV}=\frac{\epsilon_{ox} WL_{D/S}}{t_{ox}}$=1.5fF for W=1μm, L=100nm, L_G=20nm, $L_{D/S}$=40nm and t_{ox}=1μm. It is clear that the parasitic capacitance in the proposed EFET

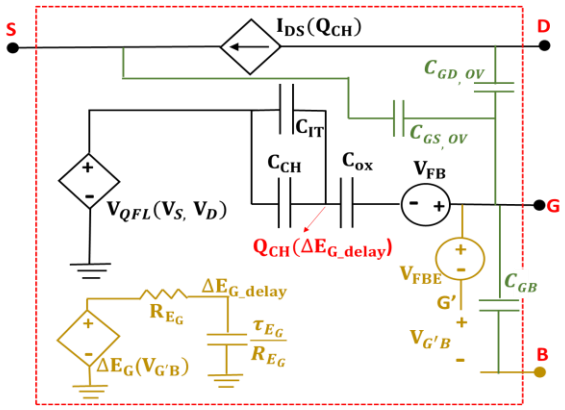

Figure 2-6 Capacitance network of EFET 1 including parasitic capacitances

structure is significant due to large overlap areas. Hence, it is imperative to reduce the overlap to achieve lower parasitic capacitance.

2.2.5 EFET Structure with Reduced Parasitic Capacitance (EFET 2)

Recall that in the previous structure, the gate extends across the length of the device resulting in high overlap $C_{GS/D}$, which can potentially lead to higher delays. A direct motivation is to diminish $C_{GS/D}$ to be comparable to parasitic capacitance in 2D FET. Hence, propose an alternative structure of the EFET (EFET 2) (Fig. 2-7) with gate along channel length as in a 2D FET, avoiding overlap. Note that in EFET 2, $C_{GS/D}$ is comparable to 2D FET. Reducing the gate length will result in fringing

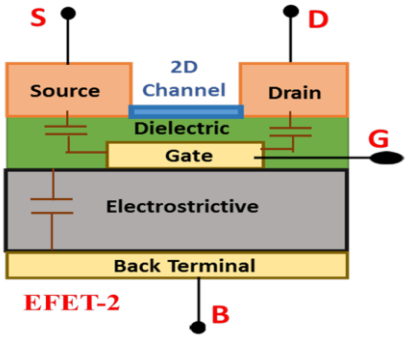

Figure 2-7 Device Structure of EFET 2

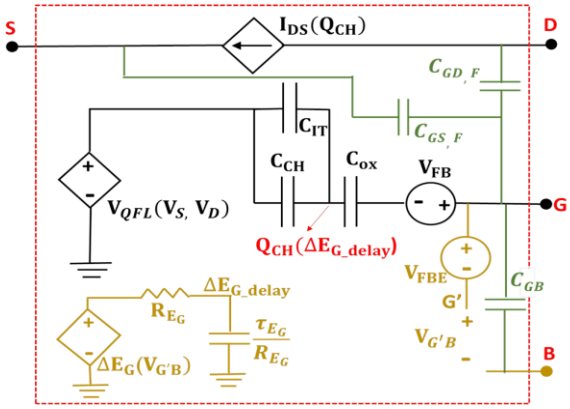

Figure 2-8 Capacitance network of EFET 2 including parasitic capacitance

of electric field from gate to drain and source contacts, giving rise to fringing capacitance ($C_{GS,F,}$ $C_{GD,F}$) as shown in Fig.(2-8).

2.3 Summary

Through this chapter, we have made the following contributions:

1. We present a circuit compatible Verilog A model of the 2D EFET that solves the governing equations of electrostrictive effect and 2D electrostatics self-consistently, while also considering the parasitic capacitances of the device.
2. We evaluate the parasitic capacitances in the proposed EFET device structure (EFET 1) and conclude that high overlap gate-source/drain capacitance ($C_{GS/GD}$) may lead to delay overhead in EFET 1 based circuits compared to 2D FET circuits.
3. We propose an alternative EFET structure (EFET 2) with reduced gate-source/drain capacitance ($C_{GS/GD}$) which is comparable to baseline 2D-FET $C_{GS/GD}$.

Chapter 3

2D EFET Device Analysis

In this chapter we analyze the transfer (I_D-V_{GS}) and output characteristics (I_D-V_{DS}) of the 2D EFET using DC analysis. We discuss the characteristics for different Strain Transfer Coefficient (STC) and back voltage (V_B). We provide insights on the effect of STC and V_B on ON-current (I_{ON}), OFF-current (I_{OFF}) and sub-threshold swing. Here, the results and trends have been discussed elaborately with respect to n-EFET, with brief understanding of the p-EFET trends. The concepts of n/p-EFETs discussed in this chapter will be used in subsequent chapters on circuit design. Note that p-EFET operation is detailed wherever necessary to develop comprehensive understanding of the circuit operation. The results presented in this and subsequent chapters are based on the EFET model presented in Chapter 2.

3.1 I_D-V_{DS} and I_D-V_{GS}

Fig. (3-1) shows I_D-V_{DS} for different V_{GS} for the EFET/2DFET. The EFET displays higher I_{ON} than 2D FET due to reduction of bandgap (ΔE_G>0). It is to be recalled from (2.7) that ΔE_G is directly proportional to V_{GB} and STC. Here, V_B=0V for the n-EFET and STC=408eV-pm/V with the parameter values provided in Table 1. As V_G is increased, V_{GB} increases and consequently ΔE_G increases monotonically. However, this effect gives rise to exponential increase in channel charge Q_{CH} (2.16). Hence, the increase in I_{ON} at higher V_{GS} for EFET is much higher compared to 2D FET. A 163% increase in I_{ON} is observed for V_{GS}=0.4V for 10% transduction efficiency.

The I_D-V_{GS} characteristics for different V_{DS} are shown in Fig. (3-2). At V_B=0V and STC=408eV-pm/V, increasing V_G leads to additional lowering of conduction bands in EFET (due to ΔE_G>0) than in 2D FET. This leads to steep switching behavior in EFET compared to 2D FET and 9% decrease

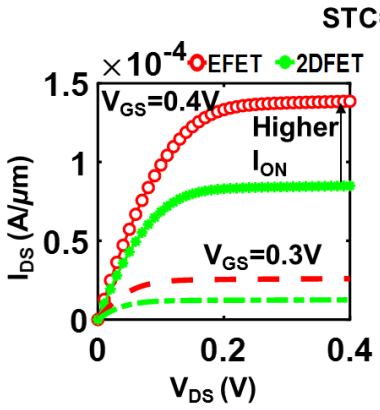

Figure 3-1 I_D-V_{DS} of EFET and 2D FET. EFET shows higher ON current compared to 2D FET.

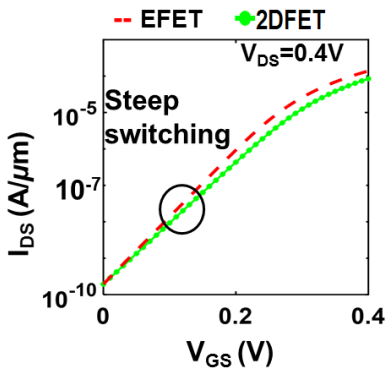

Figure 3-2 I_D-V_{GS} of EFET and 2D FET. EFET shows steeper switching behavior than 2D FET.

in sub threshold swing (SS). It is important to note that these simulations are carried out at 10% strain transduction efficiency and further decrease in sub-threshold swing is observed with higher efficiency.

3.2 Optimization of Device Characteristics

The underlying principle of reduction in bandgap (ΔE_G>0) that leads to lower SS and higher I_{ON} in EFET depends on STC (=$\boldsymbol{\alpha C_{33}\,\eta d_{33}}$) and back voltage V_B, as explained by (2.7). In this section, we aim to establish the impact of STC and V_B on various EFET characteristics.

a) Impact of STC

We operate the EFET at V_{GS}=0.4/V_{DS}=0.4V, V_B=0 while varying the STC. First, we discuss the I_D-V_{GS} characteristics and analyze the trend in SS (Fig. 3-3, 3-4), followed by I_D-V_{DS} characteristics and increase in I_{ON} (Fig. 3-5,3-6). By increasing STC (through optimizing one or more constituent parameters), ΔE_G>0 is enhanced which leads to increased band bending in the sub-threshold regime and lowered conduction band in the ON state of the device compared to 2D FET. The former leads to 42% decrease in SS when STC to 2856 eV-pm/V (=70% efficiency) while ON current due to the

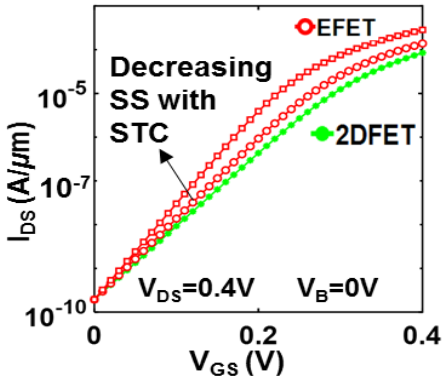

Figure 3-3 I_D-V_{GS} of EFET with increasing STC. EFET shows decreasing SS with increasing STC.

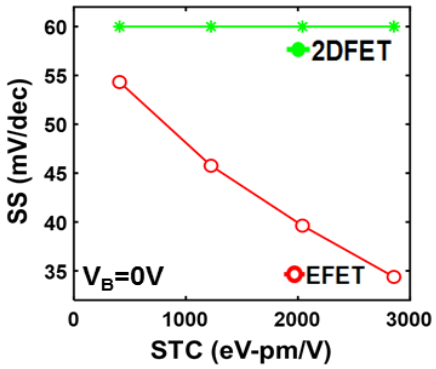

Figure 3-4 SS vs. STC. SS decreases with increase in STC.

latter increases to as large as 7.5X for the same increase in STC. The OFF current is unaffected as in Fig. (3-5) since at V_{GS}=0V, ΔE_G=0 and cannot be unaffected by STC.

b) Impact of V_B

While material optimization is possible to tune the device-circuit characteristics, an effective knob offered in the EFETs is the back contact (B), which directly controls the electrostriction and the bandgap change (ΔE_G) through V_{GB} (2.7). Larger potential difference across the electrostrictive material (V_{GB}) results in increased strain of the material and greater band bending (ΔE_G>0) in the channel material. By decreasing V_B<0V, V_{GB} in an n-EFET is increased, ΔE_G is enhanced and I_{ON} increases. Consequently, I_{OFF} increases; since the electrostrictive material experiences positive V_{GB}

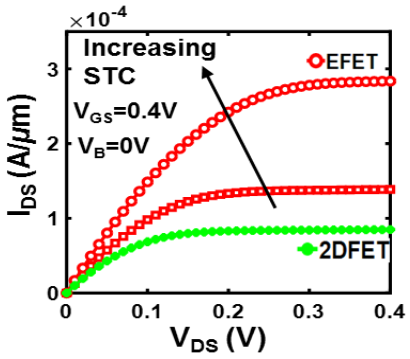

Figure 3-5 I_D-V_{DS} characteristics of EFET for STC. With increase in STC EFET shows increase in ON current.

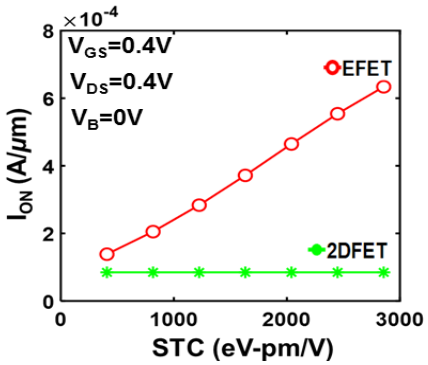

Figure 3-6 I_{ON} vs. STC. I_{ON} increases with STC.

in the OFF state (V_G=0), resulting in lowered bands (ΔE_G>0) compared to 2D FET. The reverse is true for V_B>0V. Fig. (3-7,9) shows how the device characteristics (ON and OFF currents) can be dynamically tuned to give up to 10X decrease in OFF current for V_B=0.6V (Fig. 3-8) and 2.8X increase in ON-current for V_B=-0.6V (Fig. 3-10). However, note that unlike STC, back voltage does not change sub-threshold swing but causes a shift in threshold voltage (V_{TH}). Decreasing V_B decreases V_{TH} and vice-versa for increase in V_B. Note that these trends of V_{TH} with V_B are opposite compared to that of V_{TH} vs. body voltage in a conventional CMOS device [46]. Change in EFET characteristics and unique V_{TH} tunability with V_B leads to the possibility of dynamically adapting

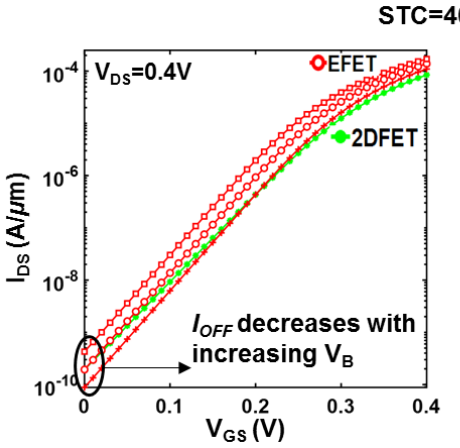

Figure 3-7 I_D-V_{GS} characteristics of EFET with varying V_B showing effect on OFF current

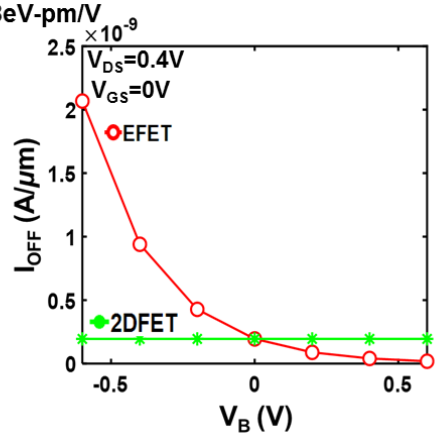

Figure 3-8 I_{OFF} with varying V_B. I_{OFF} decreases with increase in V_B

circuit characteristics and prospects of new circuit designs [47]. E.g., logic threshold voltage of an inverter can be dynamically tuned using back voltage. Also, better energy-delay characteristics can be obtained by optimizing the back voltage which is discussed in detail in Chapter 4.

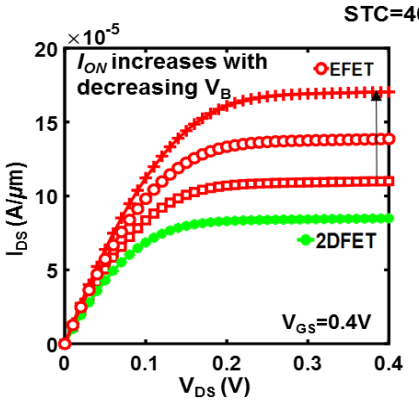

Figure 3-9 I_D-V_{DS} characteristics of EFET for different V_B. I_{ON} increases with decrease in V_B.

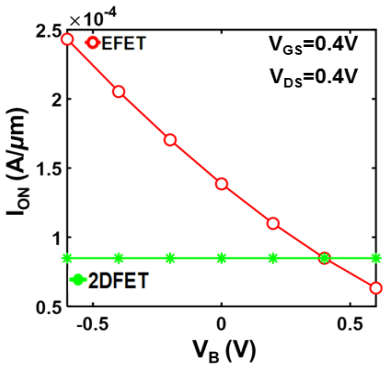

Figure 3-10 I_{ON} with varying V_B. I_{ON} of EFET shows higher values than 2D FET for V_B<V_{GS}.

3.3 Summary

To summarize the contributions of this chapter,

1. EFET shows lower SS and higher I_{ON} compared to 2D FET.
2. The conjunctive impact of STC and V_B on electrostriction/ΔE_G modulation leads to interesting trends in device characteristics, viz., SS, I_{ON} and I_{OFF}.
3. Increasing STC to 2856 eV-pm/V leads to 42% decrease in SS and 7.5X increase in I_{ON}.
4. When V_B is -0.6V, I_{ON} increases by 2.8X at the cost of higher I_{OFF}. Increasing V_B to 0.6V, decreases I_{OFF} by 10X and I_{ON} by 1.3X respectively.
5. V_B allows V_{TH} tuning in EFET that is opposite to V_{TH} tuning obtained with back contact in CMOS, leading to unique opportunities for EFET circuit design.

TABLE 1 SIMULATION PARAMETERS

Parameter Type	**Parameters**	**Values**
Electrostrictive (PMN-PT)	d_{33}	850 pm/V (n-type) -850 pm/V (p-type)
	e_{33}	0
	C_{33}	60 GPa
	α	80 meV/GPa
	η	0.1
2D (MoS_2)	ϵ_e	800 F/m
	ϵ_{2D}	3.3 F/m
	t_{2d}	2nm
	m (K valley)	$0.45m_0$ (n-type) $0.64m_0$ (p-type)
	m (Q valley)	$0.63m_0$ (n-type) $0m_0$ (p-type)

	E_g	1.2 eV (n/p-type)
	E_{KQ}	0.13 eV
	μ	90 cm^2/Vs(n-type) 250 cm^2/Vs (p-type)
Device Parameters	L	0.1 μm
	L_g	20 nm
	t_{ox}	3nm
	t_e	1μm
	ϵ_{ox}	12.5 F/m
	τ_e	1ns
	V_{FB}	-0.2V

Chapter 4

Circuit Analysis of 2D EFET

4.1 Introduction

In the previous chapter, we presented the transfer characteristics of the 2D EFET obtained through DC analysis. We have thoroughly investigated the factors for design and run time optimization of I_{ON}. The DC analysis is not adequate means for analysis of time-dependent effects. Hence, in order to study those effects, viz., impact of capacitance, energy-delay of EFET and their impact on circuits, we have adopted transient simulation. In this chapter, we discuss the energy-delay characteristics of EFET based 7 stage ring-oscillator (RO) shown in Fig. 4.1.

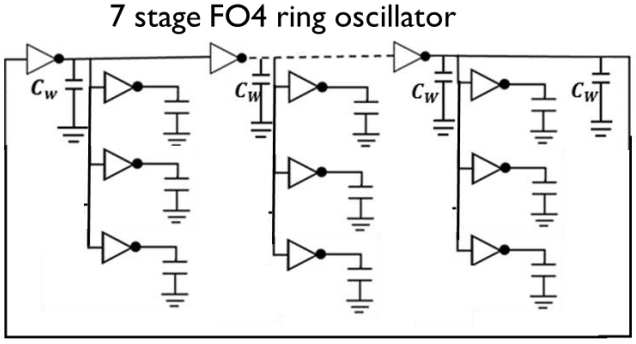

Figure 4-1 Schematic of Ring Oscillator

4.2 Delay in 2D EFET

The delay associated with an EFET can arise due to two factors –

1. Delay in the transduction mechanism ($\boldsymbol{\tau_{EG}}$)

2. Gate Delay ($\boldsymbol{\tau_{gate}} = \frac{C_G V_{DD}}{I_{OFF}}$ [48]), where C_G is the total gate capacitance. C_G in EFET comprises of (a) gate oxide capacitance (C_{ox}), (b) parasitic capacitance, viz., gate drain capacitance ($C_{GD,F/OV}$) and gate source capacitance ($C_{GS,F/OV}$) and (c) electrostrictive capacitance (C_{GB}). Parasitic capacitance in EFET 1 is a result of overlap capacitance ($C_{GD/S,OV}$) while in EFET 2 it is fringe capacitance ($C_{GD/S,F}$) as discussed in Chapter 2.

C_{GB} adds an additional capacitance to the EFET compared to 2D FET. Further, while $C_{GD/S}$ of EFET 2 is comparable to 2D FET, the same is higher in EFET 1 as discussed in Chapter 2. Due to higher capacitance in EFET, higher delay may be expected than 2D FET. However, the greater drive strength (I_{ON}) of EFET compared to 2D FET may help mitigate the increase in delay due to capacitance. The counteracting effects of capacitance and I_{ON} on delay motivates us to thoroughly investigate their impact on EFET based circuits. We perform this study by analyzing energy-delay characteristics of EFET based ring oscillators (RO) and comparing them with 2D FET RO.

4.2 Ring Oscillator

A ring oscillator (RO) is a device composed of odd number of inverters in a chain. The output of the last inverter is fed back into the first forming a loop (Fig. (3-1)). The output oscillates between V_{DD} and 0. The delay of the ring oscillator (τ_{RO}) depends on the number of stages, n and the delay time of each inverters τ_{inv} as $\tau_{RO} = 2n\tau_{inv}$ and frequency, $f = \frac{1}{\tau_{RO}}$.

4.3 2D EFET 7 Stage Ring Oscillator Analysis

In this section, we provide a systematic analysis of the different delay components in EFET that contribute to energy-delay performance of EFET based RO. We begin our analysis with an ideal EFET showing electrostriction without any parasitic capacitance or transduction delay. Subsequently, we study the EFET performance by considering transduction delay and parasitic capacitances.

4.3.1 Analysis Without Parasitic Capacitance

To study the effect of different delay components, we first analyze RO circuit for EFET 1 with $\boldsymbol{\tau_{EG}} = 0$ and neglecting parasitic capacitances $C_{GD,OV}$, $C_{GS.OV}$ and $C_{GB.}$ Hence, C_G=C_{ox} and we obtain

the performance of the fastest possible EFET. In other words, the said EFETs (operating with $|V_{GB}|$=0.4V) have 163% higher I_{ON} than 2DFET (Fig. 3-1) without any additional performance over-heads. In comparison to the 2DFET RO, the EFET RO shows 1.5X delay reduction at iso-energy. The lower delay is attributed to higher I_{ON}.

Now, we consider the case with transduction delay ($\boldsymbol{\tau_{EG}}$) while neglecting parasitic capacitances ($C_{GD/GS}$ and C_{GB}) . We consider an electrostrictive material with t_e=1µm (such that C_{GB} is comparable to parasitic capacitance, to be discussed later). The time an acoustic wave takes to travel through 1µm of t_{ox} ~1ns, considering speed of acoustic wave=880m/s. Hence, we perform our analysis around at $\boldsymbol{\tau_{EG}}$=1ns. With a delay of $\boldsymbol{\tau_{EG}}$=1ns, the electrostrictive material may not expand to its full potential before current conduction has taken place. However, certain amount of expansion does take place before conduction which will lead to band gap change, $\Delta E_{G,delay.}$ Thus, the drive strength of the EFET for $\Delta E_{G,delay}$ ($I_{ON,delay}$) is less than the steady state I_{ON} which is the result of maximum ΔE_G for a given $V_{GB.}$ As a result, EFET with $\boldsymbol{\tau_{EG}}$=1ns shows 1.15X higher delay (Fig. 4.2) than EFET with $\boldsymbol{\tau_{EG}}$=0 at iso-energy. It should be noted that $I_{ON,delay}$>$I_{ON,2DFET}$ since

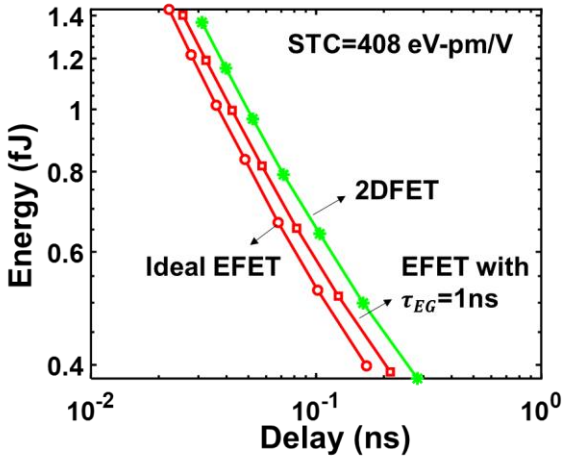

Figure 4-2 Energy delay of EFET RO without parasitic capacitance vs. 2D FET RO

$\Delta E_{G,delay}$>0. Hence EFET RO shows 1.2X lower delay (Fig. 4-2) than 2DFET pushing the energy delay plot for EFET with $\boldsymbol{\tau_{EG}}$=1ns closer to 2D FET.

4.3.2 Analysis with Parasitic Capacitance

(a) EFET 1

Now we combine the effect of transduction delay ($\boldsymbol{\tau_{EG}}$=1ns) and parasitic capacitance of the EFET while studying the trends of the EFET RO. The gate capacitance C_G=C_{OX}+$C_{GD,OV}$+$C_{GS,OV}$+$C_{GB.}$ Electrostrictive/piezoelectric materials are well known for their high dielectric constant. For this work, PMN-PT is considered as the electrostrictive material with ϵ_E=800$\epsilon_o F/m$. In order to keep its capacitance comparable to parasitic capacitance, the thickness of material is considered as t_e=1μm. Our calculations reveal that C_{GB}=$\frac{\epsilon_E WL}{t_e}$=0.71fF, C_{OX}=$\frac{\epsilon_{ox} WL_G}{t_{ox}}$=0.74fF and $C_{GD/S,OV}$=$\frac{\epsilon_{ox} WL_{D/s}}{t_{ox}}$=1.5fF. Here, $L_{D/S}$=2L_G. It is important to note here that the overlap capacitance cannot be decreased further since the source and the drain contact cannot conventionally be scaled lower than $2L_G$. With these considerations, the overlap capacitance are the largest contributors to delay. Fig. 4-3 shows the energy-delay plot for EFET 1 RO with transduction delay and gate delay (parasitic capacitance inclusive). Considering that the RO circuit is ideal with no delays due to

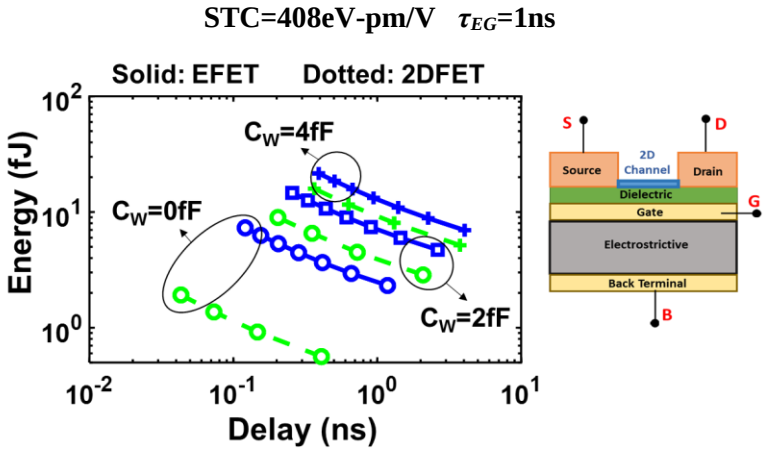

Figure 4-3 Energy delay of EFET 1 RO with parasitic capacitance and transduction delay

parasitic wire capacitance (C_W=0fF), EFET shows 6.4X higher energy than the 2DFET at Iso-delay as a result of high parasitic capacitance ($C_{GD/S,OV}$ and C_{GB}). Also, due to transduction delay ($\boldsymbol{\tau_{EG}}$=1ns) in the electrostrictive material I_{ON} of the EFET is lower than steady state I_{ON}. The combined effect of higher capacitance and sub-optimal increase in drive strength is the cause of higher degradation of delay in EFET compared to 2D FET. A realistic condition is the presence of combined effect of higher capacitance and sub-optimal increase in drive strength is the cause of higher degradation of delay in EFET compared to 2D FET. A realistic condition is the presence of circuit delay due to wire capacitance. In C_W dominated circuits (=2fF/4fF), we observe that the relative worsening of delay of EFET to 2DFET is lower case, as the delay due to C_W counteracts with $\boldsymbol{\tau_{EG}}$. For C_W=4fF, EFET shows 1.3X higher energy at iso-delay.

(b) EFET 2

In section 2.2.5, we propose an alternative EFET structure whose gate to source/drain parasitic capacitance ($C_{GD/S,F}$) are due to fringing fields [45] and are comparable to 2DFET. The overhead in the EFET 2 capacitance (or delay) is due to C_{GB}. With ϵ_E=800$\epsilon_o F/m$ and t_e=1μm, C_{GB}=$\frac{\epsilon_E WL}{t_e}$=0.71fF, C_{OX}=$\frac{\epsilon_{ox} WL_G}{t_{ox}}$=0.74fF and $C_{GD/S,F}$. In this case, delay of the EFET 2 is 2.26X greater than 2D FET at iso-energy (=1.3fJ) for C_W=0 (Fig. 4-4). Comparing this with the result

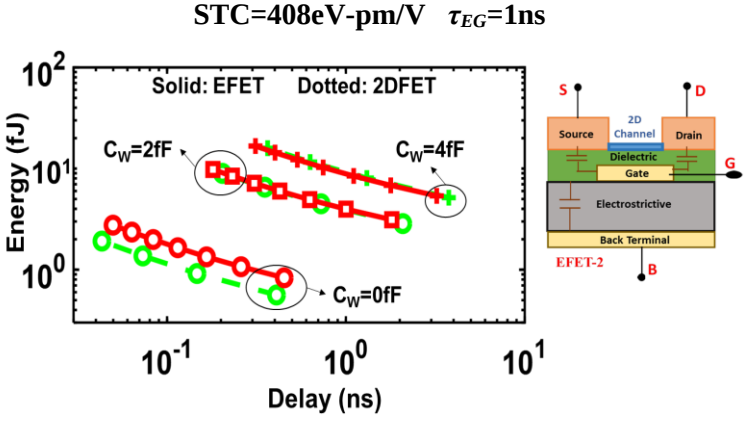

Figure 4-4 Energy delay of EFET 2 RO with parasitic capacitance and transduction delay

obtained for EFET 1 we observe that the delay in EFET 2 is drastically lower than EFET 1. Similar to our observation of EFET 1 for increased C_W, relative degradation of EFET to 2DFET RO is lower. It is interesting to note here that for high C_W (=4fF), the performance of both EFET and 2DFET are comparable.

4.4 Impact of STC on 2D EFET 7 Stage RO

In Chapter 3, we presented design time optimization of EFET through Strain Transfer Co-efficient ($\boldsymbol{STC = \alpha C_{33}\, \eta d_{33}}$). Higher STC leads to increase in I_{ON} by reducing the bandgap ($\Delta E_G = STC.V_{GB}$) more and more. Higher I_{ON} of the EFET can overcome the detrimental effects of delay, resulting in better energy-delay performance of the EFET. We analyze both RO based on EFET 1 and EFET 2 by varying STC for C_W=2fF. STC=408 eV-pm/V corresponds to 10% efficiency of transfer of transduction from the electrostrictive material to the 2D channel. In order for EFET 1 RO to match 2DFET RO performance (Fig. 4-5), efficiency is increased to 70% (STC=2856 eV-pm/V). On the contrary, EFET 2 displays similar performance trends at 10% efficiency. Hence, optimization of EFET 2 is achieved at lower I_{ON}/STC. EFET 2 shows ~1.7X reduced energy at iso-delay (delay=0.18ns) compared to 2D FET for 70% transfer of transduction.

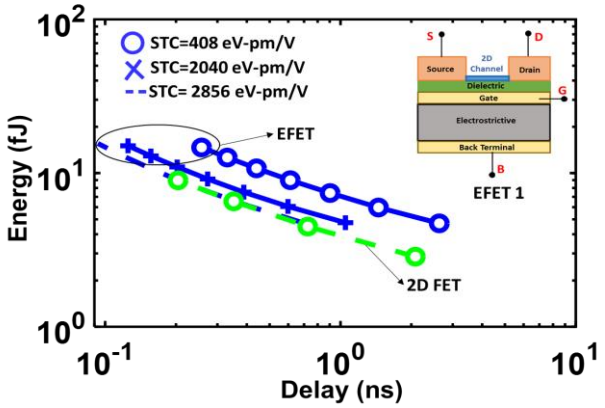

Figure 4-5 Energy delay optimization of EFET 1 RO for different STC

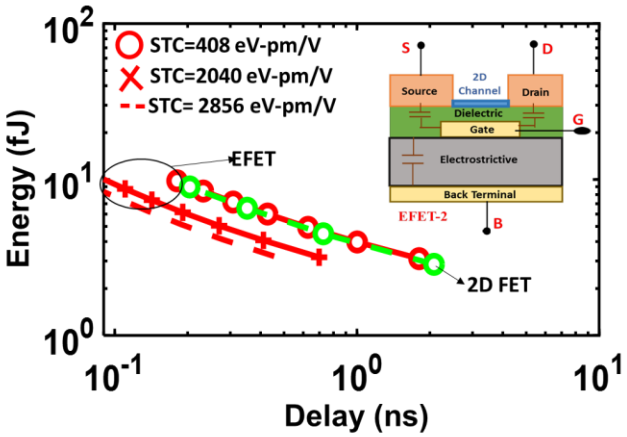

Figure 4-6 Energy delay optimization of EFET 2 RO for different STC

4.5 Summary

From this chapter, we conclude the following:

(1) Ideal EFET RO without transduction delay and parasitic capacitance ($C_{GS,GD}$ and C_{GB}) shows 1.5X lower delay than 2D FET RO at iso-energy.

(2) With transduction delay (τ_{EG}=1ns) and no parasitic capacitance ($C_{GS,GD}$ and C_{GB}), EFET RO shows 1.15X higher delay than ideal RO and 1.2X lower delay than 2D FET RO.

(3) In ideal circuits with wire capacitance C_W=0fF, EFET 1 RO (with transduction delay and parasitic capacitance) shows 6.4X higher energy than the 2DFET RO at iso-delay because of $C_{GD/GS}$ and C_{GB}. EFET 2 shows 2.26X higher delay at iso-energy due to C_{GB}.

(4) In capacitance dominated circuits (C_W=4fF), EFET 1 RO shows 1.3X energy at iso-delay while the performance of EFET 2 RO is comparable to 2D FET RO.

(5) Through STC optimization (70% efficiency), performance of EFET 1 RO is matched to that of 2D FET RO. EFET 2 RO which shows similar performance at 10% efficiency, shows ~1.7X reduced energy at iso-delay (delay=0.18ns) compared to 2D FET for 70% transfer of transduction.

Chapter 5

2D EFET in SRAM Design

Memory elements are critical components in most digital systems. Among the various types of memories, Static Random-Access Memories (SRAMs) are widely used in electronics industry as a cache memory in state of the art systems [46]. A considerable attention has been paid to the design of low-power, high-performance SRAMs [48] since they are a critical component in both hand-held devices and high-performance processors. The flexibility of design time optimization of EFET by means of STC (through appropriate material selection) and run time optimization by independently biasing the fourth terminal V_B in EFET makes it a promising candidate for SRAM design. It is intriguing to investigate whether the EFET can mitigate the read-write-hold conflicts. In this chapter we analyze and compare the 6T 2D EFET SRAM with the 2DFET SRAM.

5.1 Fundamentals of SRAM

A conventional 6T SRAM consists of two inverters connected in a cross-coupled manner forming a bi stable latching circuit (Fig. (5-1)). The schematic of a 6T SRAM cell is shown in Fig. (5-2). Data in the memory cell is stored at complimentary storage nodes Q and QB which correspond to the two stable points of the circuit. Based on the state of Q/QB, the data in the memory cell is interpreted either as logic 0 or as a logic 1. In order to read the data stored in the memory cell or to

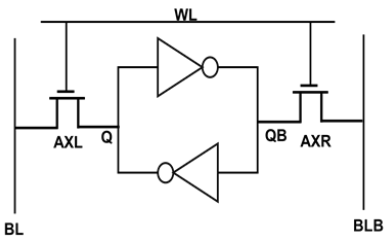

Figure 5-1 Gate level view of 6T SRAM

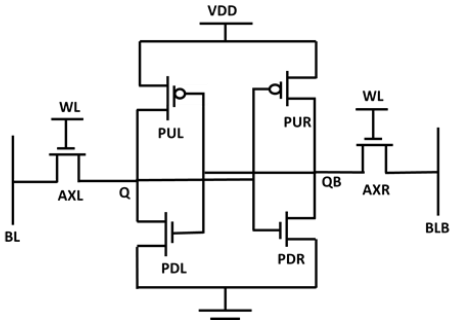

Figure 5-2 Schematic of 6T SRAM

write into the memory cell, we use two separate lines - BL and BLB (Fig. (5-1, 2)). Access transistors (AXL, AXR) connect/disconnect the bit lines to the bi-stable circuit by turning ON/OFF the word line (WL).

The read and write operations of the SRAM are explained below:

Read: Let us assume that the initial voltage at QB, V_{QB}=0 and at Q, V_Q=V_{DD}. For the read operation, BL and BLB are first pre-charged to V_{DD} and then WL is set to V_{DD}. The SRAM schematic after these conditions are set is shown in Fig. (5-3). The access transistors AXL, AXR, pull up transistor PUL and pull down transistor PDR are turned on. Due to the read current I_R, flowing through AXR and PDR, V_{QB} starts to rise and the BLB starts to discharge as shown in Fig. (5-3). The differences in the voltages of BL and BLB are then sensed after amplification through a sense amplifier to obtain the value stored in the SRAM cell. The rise in voltage value at the node QB, V_{READ}, depends on the relative driving strengths of AXR and PDR. In order to ensure that a read is stable, V_{READ} should not become greater than the V_M (logic threshold voltage) of the inverter formed by PUL and PDL. Therefore, to increase the read stability of the SRAM cell, the driving strength of the pull-down transistors should be greater than the access transistors.

Write: Let us assume that we want to write data=0, i.e., V_Q=V_{DD}→0 and V_{QB}=*0*→V_{DD}. In the write operation, BLB is driven to V_{DD}, BL to 0 and the WL is thereafter asserted. As shown in Fig. (5-4), during this operation, I_{WRITE} flows from PUL and AXL to BL discharging node Q to V_{WRITE}. If V_{WRITE}

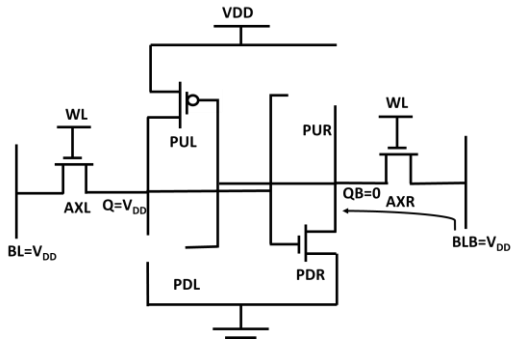

Figure 5-3 6T SRAM during read operation showing initial voltage conditions

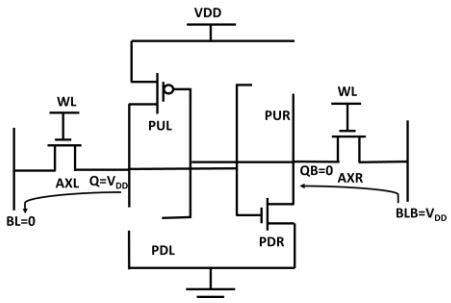

Figure 5-4 6T SRAM during write operation showing initial voltage conditions

is smaller than the V_M of the inverter formed by PUR and PDR, then 0 will get stored in the SRAM cell. To increase the write ability of the SRAM cell the driving strength of the access transistor should be more than the driving strength of the pull up transistor.

From the above description of read and write operations, it is important to note that SRAM has conflicting design requirements to achieve high read performance, read stability and write ability simultaneously. In order to have higher read stability, driving strength of the access transistor should be less whereas for higher write ability, the corresponding driving strength should be high [48]. In order to fulfill this design requirement, one design option is to have W_{PU}:WAC:W_{PD}= 1:1.5:2 so as to achieve balanced read stability and write ability at once [48]. Furthermore, there are following 4 metrics which are used to characterize a 6T SRAM [46]:

- **Read/Access Time**: Access time or read time is defined as the amount of time it takes for the bit line to discharge to certain voltage level that can be sensed by a sense amplifier once the word lines are asserted.
- **Read Noise Margin:** The read noise margin measures how much external DC noise can be applied to the inputs of the two cross - coupled inverters before a stable state is lost during the read operation [46]. To capture the effect of parasitic capacitance on SRAM read performance, we perform dynamic read noise margin analysis. The bias conditions to perform this analysis are same as that during read. We introduce disturbance (noise) to storage nodes Q and QB by means of noise voltages (-V_n and V_n). By increasing V_n, we

note its magnitude when Q and QB flips to their complementary logic. This value of V_n corresponds to the read noise margin.

- **Write Time**: Write time is the amount of time it takes to write the SRAM cell or the time taken to flip the values of Q and QB after the word lines are asserted.

In this work, we compare the above discussed metrics - the access time (read time), read noise margin and write time of the EFET based SRAM with the 2DFET based SRAM. The results presented here correspond to an SRAM array size of 2048 rows and 2048 columns. At the BL, we consider metal capacitance=80fF. 1 each SRAM cell, we calculate metal capacitance equivalent to 2 times poly pitch and multiply it with 2048 to obtain the BL metal capacitance for the array. WL capacitance used is 3 times BL capacitance (=240fF). Note that, the parasitic capacitance of the 2047 un-accessed cells also contributes to the final BL capacitance. We also analyze the impact of STC and V_B on the read and write operations of SRAM.

5.2 2D EFET 6T SRAM Design

The fourth terminal (V_B) in EFET provides additional configurability to the EFET strength, which can help to mitigate the trade-offs associated with read-write operation in run time. We propose two variations of the SRAM design based on static/dynamic biasing of the access transistor back voltage ($V_{B,AX}$):

(i) SRAM-I: Fixed bias ($V_{B,AX}=V_{DD}$) representing EFETs as drop-in replacement (Fig. (5-5))

(ii) SRAM-II: Dynamic control of V_B based on the operation (Fig. (5-6)).

In both the configurations, the back contact of the pull up and pull down EFET of the cross-coupled inverters are connected to V_{DD} and ground respectively, such that $|V_{GB}|=V_{DD}$ in the on state of the

device. For subsequent discussions of SRAM, we refer to design (i) and (ii) as SRAM-I and SRAM-II respectively.

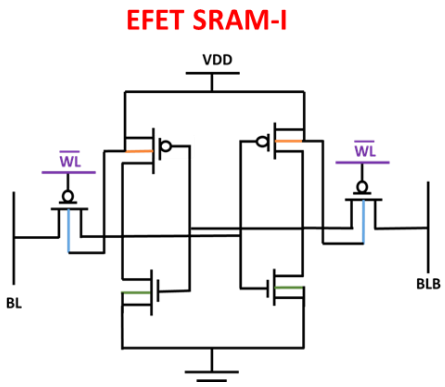

Figure 5-5 6T EFET SRAM-I with fixed back contact for access transistor

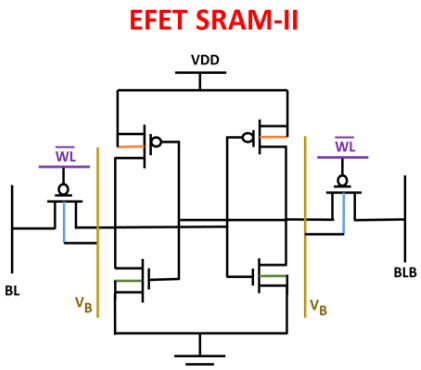

Figure 5-6 6T EFET SRAM-II with controllable back contact for access transistor

Now we describe the other design aspects of the 6T 2D EFET SRAM (I/II). The design of the 6T 2D FET/EFET SRAM is similar to the CMOS/FINFET SRAM design. However, we employ p-type access transistors in EFET SRAM instead of n-type in CMOS/FINFET SRAM. It is well known that the mobility of electrons is higher than holes in Si. n-type transistors are hence preferred, since they are faster devices and aid in write. However, in 2D materials, e.g., MoS_2, WSe_2, etc. the mobility of holes is greater than electrons. Hence, we adopt p-EFET access transistors. BL and BLB will now be pre-charged to 0, since p-FET passes a weak '0' which helps in read stability. For the read operation, increase in BL voltage will be sensed. If V_Q=V_{DD} and V_{QB}=0, read current I_R

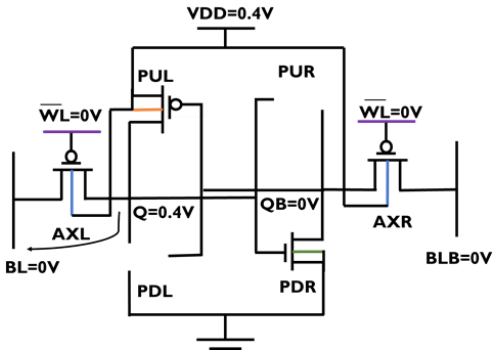

Figure 5-7 Read operation of 6T EFET SRAM-I

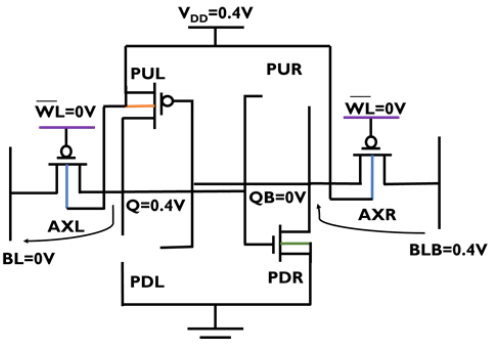

Figure 5-8 Write operation of 6T EFET SRAM-I

flows from through the PUL and AXL transistors to the BL and V_Q decreases to V_{READ}. In order for V_{READ} to not decrease below V_M, PUL should be stronger than AXL. Again, in order to write a '1', if BL=0V, BLB=V_{DD}, V_Q =V_{DD} and V_{QB}=0V, AXL should be stronger than PDL. Hence, the sizing trend in EFET SRAM is based on the above requirements. In this work, we consider W_{PU}:W_{AC}:W_{PD}=1:1.5:2 and W_{PU} =3λ, where λ=L_G/2=10nm. The supply voltage is V_{DD}=0.4V, pull up transistor back voltage is $V_{B,PU}$=0.4V and pull down transistor back voltage is $V_{B,PD}$=0V. The nominal STC is 408 eV-pm/V and $\tau_{EG} = 1ns$ for all simulations except otherwise mentioned. These results correspond to BL capacitance pertaining to an array size of 2048*2048 SRAM cells. The WL signal is fed through two inverters (word-line drivers). The EFET (EFET 1 or EFET 2) used to design the word-line drivers is consistent with the EFETs in SRAM design.

5.3 6T EFET SRAM-I (with fixed V_B)

(A) Read

For the read operation, BL and BLB are pre-discharged to 0V. Q and QB are initialized to V_{DD} and

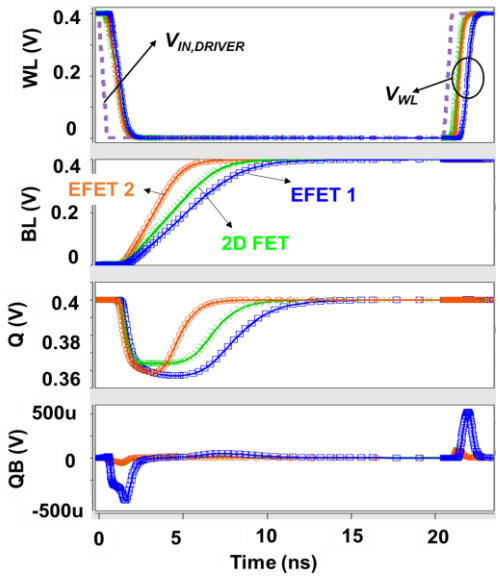

Figure 5-9 EFET SRAM-I and 2D FET SRAM read waveform

0V respectively. The WL is then asserted by driving it to 0V. The schematic of the EFET SRAM for the read operation is shown in Fig. (5-7). The transient waveforms of the read operation are provided in Fig. (5-9). When the word line is asserted, the voltage at node Q (V_Q) discharges to V_{READ} following the mechanism in Section 5.2 and charges BL up. The access time of the cell is defined as the time taken for ΔV_{BL}=50mV which is sensed by the sense amplifier.

To analyze the read time in detail, we show the effect of EFET capacitances on the WL signal in Fig. (5-9). Let us consider the same WL signal applied at the input of the WL driver (labeled as $V_{IN,DRIVER}$) in Fig. (5-9)). The output of the WL driver which controls the gate of the access transistor has been labeled as V_{WL}). Since EFET 1 has the highest capacitance ($C_{GS/D,OV}$ and C_{GB}) compared to EFET 2 and 2D FET, the WL signal experiences greater delay than the other two. Moreover, higher capacitance of the EFET 1 also leads to increase in BL capacitance in this case, contributed by the un-accessed cells. Both these effects result in 20% higher time required to charge BL for read in EFET 1 SRAM-I (Fig. 5-9, 10) compared to 2D FET SRAM. Whereas, EFET 2 has $C_{GS/D,F}$ comparable with 2D FET. Delay due to higher C_{GB} of EFET 2 compared to 2D FET is mitigated by the boosted I_{ON} achieved by electrostriction. Hence, read time of EFET 2 SRAM-I is 15% lower than 2D FET.

To be able to correctly analyze the impact of delay/ parasitic capacitance of EFET 1/EFET 2 on read stability in EFET 1 SRAM-I/EFET 2 SRAM-I and compare them, we performed transient analysis. We calculate dynamic noise margin of the EFET SRAM using the method described in

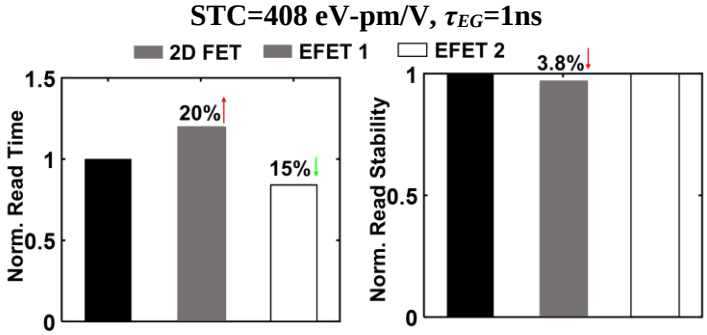

Figure 5-10 Read performance of EFET SRAM-I and 2D FET SRAM. EFET 2 shows lower read time and higher read stability compared to EFET 1 SRAM-I/2D FET SRAM.

Section 5.1. The read stability of EFET 1 SRAM-I is 3.8% lower than 2D FET while EFET 2 shows comparable read stability. To explain this trend we investigate the currents involved in charging and discharging node Q. Initially during read, V_Q decreases and BL charges up. If the WL is ON for a sufficient time, $V_{BL}>V_Q$ at which point the BL will start to charge Q again with current $I_{reverse}$ (say) and Q approaches initial state ~V_{DD}. Thus, $I_{reverse}$, helps in enhancing the read stability. Recall, the BL capacitance in case of EFET 2 SRAM-I is lower than EFET 1 SRAM-I since C_{GD} of the former is lower. Hence, $I_{reverse}$ in the former is released with lower delay and node Q is charged faster (and before it can be disturbed). In other words, it would require a larger noise to disturb Q in EFET 2 SRAM-I. As a result, EFET 2 SRAM-I has higher dynamic read noise margin than EFET 1 SRAM-I.

(B) Effect of Transduction Delay on Read Stability and Read Time

Another source of delay in EFET apart from parasitic capacitance is transduction delay (τ_{EG} described in Section 2.2.2). Due to this effect, bandgap modulation (ΔE_G) appears as a transient effect which affects transient ON current. In order to achieve maximum benefits of ΔE_G, the effect of band-gap should be propagated to the channel before the drain-source current charges/discharges the capacitor.

By decreasing τ_{EG}, the access transistor experiences more effective band bending due to lower delay in the electrostrictive action. That is, the access transistor pumps more current and charges BL faster as τ_{EG} decreases. This manifests into lower read time in EFET SRAM. Recall that for τ_{EG}=1ns, EFET 1 SRAM-I shows 20% higher read time compared to 2D FET (discussed in Section 5.3(A) and Fig. 5-10). When τ_{EG} is decreased to 1ps, read time of EFET 1 SRAM-I becomes comparable to 2D FET SRAM. Again, at τ_{EG}=1ps, EFET 2 SRAM shows 33% lower read time compared to 2D FET SRAM. EFET 2 SRAM-I (τ_{EG}=1ps) shows 17% improvement (Fig. (5-11))

in read time when compared to its own performance at τ_{EG}=1ns (Fig. 5-10). Conversely, when τ_{EG} increases to 10ns, EFET 1 SRAM-I shows higher 42% higher read time than 2D FET SRAM. EFET 2 SRAM-I read time is comparable with 2D FET SRAM at τ_{EG}=10ns.

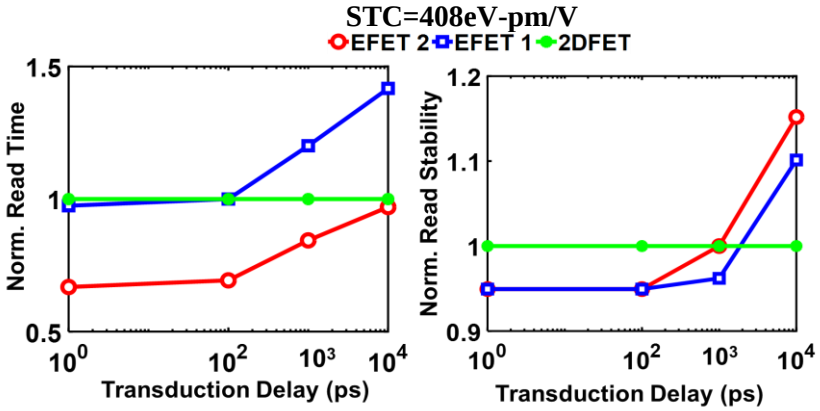

Figure 5-11 Read performance of EFET SRAM-I and 2D FET SRAM. Increasing transduction delay increases read time and read stability

To analyze the effect of τ_{EG} on read stability, it is noteworthy that the pull-up transistor (with drain at V_{DD}, gate at 0 and back terminal at V_{DD}) is under stead state conditions with regard to the electrostrictive effect. In other words, irrespective of τ_{EG}, the pull-up transistor has a low bandgap. However, as WL (gate of the access transistor) is asserted during read, the access transistor undergoes transient bandgap modulation. Hence, increasing the access transistor strength by lowering τ_{EG} (pull-up transistor is in steady state) causes a relative increase of access to pull up transistor strength which leads to larger likelihood of the node voltage Q being disturbed. As a result, read noise margin diminishes compared to 2D FET SRAM as τ_{EG} decreases. When τ_{EG} is decreased to1ps, read noise margin of EFET 1 SRAM-I and EFET 2 SRAM-I is 5% lower. Contrast this with noise margin at τ_{EG}=1ns: EFET 1 SRAM-I shows 3.8% lesser while EFET 2 SRAM-I showed comparable read stability with 2D FET SRAM. When τ_{EG} increases (=10ns), read stability increases by 10% and 15% for EFET 1 SRAM-I and EFET 2 SRAM-I respectively.

(C) Read Optimization Considering Strain Transduction Coefficient (STC)

Increasing STC leads to higher I_{ON} due to reduction in bandgap (increasing ΔE_G) as reported in Section 3.3.2. STC is a process related parameter that globally affects all transistors. Therefore, with increase in STC, both pull-up and access transistor involved in the read operation become stronger (higher I_{ON}). As a result, higher I_{READ} flows during the read operation with increase in STC. The read time of EFET 2 SRAM-I improves by 33% at STC=408 eV-pm/V (10% efficiency) and 50% at STC~2856 eV-pm/V (70% efficiency) compared to 2D FET SRAM for EFET 2 SRAM-I (Fig. (5-12)). Although EFET 1 SRAM-I shows higher read time at 10% efficiency, 30% reduction in the same is observed at 70% efficiency (Fig. (5-12)). At 20% efficiency, iso read time condition is achieved.

Interestingly, read margin also increases as STC increases. We explain this trend by carefully studying the currents involved in charging and discharging node Q. Initially during read, V_Q decreases and BL charges up. If the WL is ON for a sufficient time, $V_{BL}>V_Q$ at which point the BL will start to charge Q again with current $I_{reverse}$ (say) and Q approaches initial state ~V_{DD}. In a way, this implies an undisturbed state of V_Q. As STC increases, BL charges faster, $V_{BL}>V_Q$ condition dominates and Q is rather held at ~V_{DD}. This leads to increase in noise margin as STC

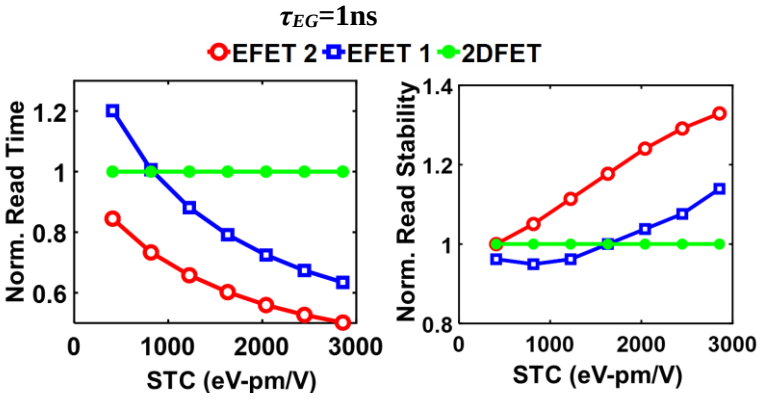

Figure 5-12 Read optimization of EFET SRAM-I with STC. Read time decreases with increase in STC. Improvement in read noise margin is observed with increasing STC.

increases. EFET 2 SRAM-I shows iso read stability at STC=408 eV-pm/V (10% efficiency) and 33% increase in noise margin when STC=2856 eV-pm/V (70% efficiency) while EFET 1SRAM-I shows slightly lower stability at 10% efficiency which increases to 14% improvement at 70% efficiency.

(D) Write

In order to write, BLB and BL are driven to V_{DD} (=0.4V) and 0V respectively. QB and Q are initialized to 0V and V_{DD} respectively (Fig. 5-8). The WL is then asserted by driving it to 0V. Fig. 5-13 shows the transient waveform of the write operation. Write ability is determined by the relative strength of the access transistor (AXR) and pull down (PDR). For lower write time, AXR should be stronger than PDR such that V_{QB} is charged to logic threshold voltage (V_M) of left inverter faster

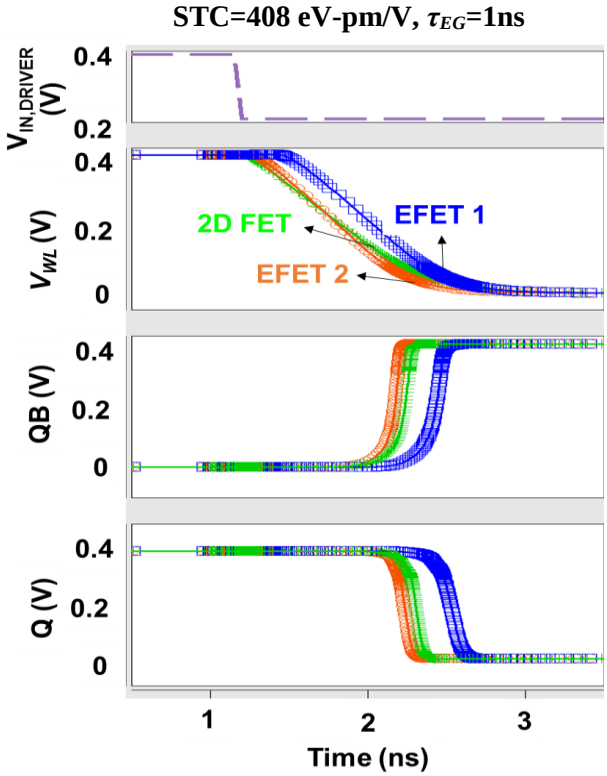

Figure 5-13 Waveforms of write operation for EFET SRAM-I and 2D FET SRAM. EFET 1 SRAM-I shows higher write time than EFET 2 SRAM-I/2D FET SRAM due to higher parasitic capacitance. Electrostrictive effect mitigates higher C_{GB} in EFET 2 SRAM-I, resulting in lower write time.

(detailed description in Section 5.1). Note that, EFET AXR/PDR in steady state are biased with $|V_{GB}|=V_{DD}$ and should be stronger than 2DFET. However, during transient analysis, such as write, AXR and PDR will be affected by τ_{EG} (similar to the explanation provided in the previous section). To establish the effect of τ_{EG} on EFET AXR and PDR strength during write and conclude about the dominating EFET, let us analyze their bias conditions. Initially, for AXR: $V_{BLB}=V_{S,AXR}=V_{DD}$ and $V_{QB}=V_{D,AXR}=0$V. Hence $|V_{DS,AXR}|=V_{DD,}$ $V_{GB,AXR}=0$V ($V_{G,AXR}=V_{WL}=V_{DD}$ before WL is turned on and $V_{B,AXR}=V_{DD}$ for p-EFET). In contrast, for PDR: $V_{QB}=V_{D,PDR}=0$ and $V_{S,PDR}=0$. Hence $V_{DS,PDR}=0$, $V_{GB,PDR}=V_{DD}$ ($V_{G,PDR}=V_Q=V_{DD}$ and $V_B=0$ for n-EFET). Note that at the onset of write, $|V_{DS,AXR}|=V_{DD}$ and $V_{DS,PDR}=0$, i.e., AXR has higher drive strength than PDR. This is despite the fact that PDR has already experienced optimal band bending (due to initial $V_{GB,PDR}=V_{DD}$). While the WL is asserted (V_{WL} changes from V_{DD} to 0), V_{GB} in AXR begins to increases and AXR strength increases. Hence, initially V_{QB} begins to increase, dominated by AXR action. This implies that drain voltage of PDR $V_{D,PDR}$ increases. At the same time, V_Q (at the left inverter discharges), hence gate voltage of PDR $V_{G,PDR}$ ($=V_Q$) becomes smaller. Thus $V_{GB,PDR}$ decreases and PDR strength falls. The concatenated effect of initial low strength in PDR and progressive decrease in its V_{GB} (which affects electrostriction) leads to the conclusion that PDR is weaker than AXR. As a result, the influence of τ_{EG} on AXR will dominate, rather than that on PDR.

When τ_{EG} is small (<1ns), the access transistor drives more current (more effective ΔE_G) and write time decreases compared to 2D FET SRAM. Note that this happens although the capacitance at node Q for EFET 1 SRAM-I (due to $C_{GS,D,OV}$ and C_{GB}) is greater than EFET 2 SRAM-I and 2DFET SRAM. In this case, the enhanced I_{ON} of EFET mitigates the overhead of capacitance. As τ_{EG} increases, slower ΔE_G lowers results in sub-optimal I_{ON} and higher capacitance effect dominates resulting in higher write time.

At τ_{EG}=1ps, EFET 1 and EFET 2 SRAM shows 16% and 35% lower write time and at τ_{EG}=10ns, write time of EFET 1 and EFET 2 SRAM is 40% and 9% higher as shown in Fig. (5-14). At τ_{EG}=*1ns*

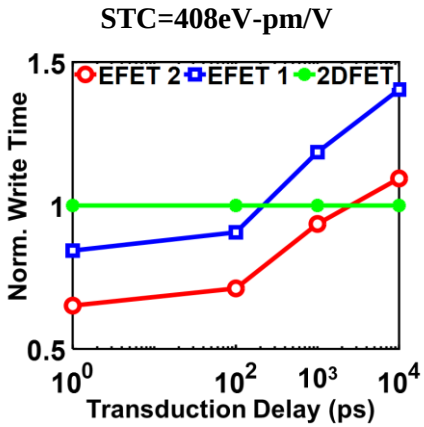

Figure 5-14 Write time of EFET SRAM-I for different transduction delay. Write time increases as transduction delay increases.

(value for this work), write time of EFET 1 SRAM is 20% higher while EFET 2 SRAM shows 3% lower write time compared to 2D FET SRAM.

(E) STC Optimization for EFET SRAM Write

In the previous section, we concluded that at τ_{EG}=1ns, EFET 1 shows higher write time than 2D FET. A possible way to circumvent this is by choosing a higher STC for the EFET. As STC increases, ΔE_G and consequently I_{ON} of the access transistor increases, while τ_{EG} is constant. This in turn, leads to I_{ON} playing a dominant role over the overhead of parasitic capacitance at node Q. Note that since PDR is weaker than AXR (discussed in the previous section), effect of STC on

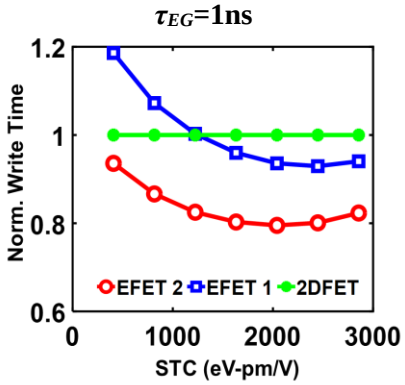

Figure 5-15 Write time optimization of EFET SRAM-I with STC. Write time decreases as STC increases. At STC>1224 eV-pm/V, effects of parasitic capacitance in EFET 1 SRAM-I are mitigated and it shows lower write time compared to 2D FET SRAM.

AXR dominates over that on PDR. As a result write time decreases. iso write time is observed for EFET 1 SRAM-I at STC=1224 eV-pm/V, EFET 1 SRAM-I and EFET 2 SRAM-I shows 6% and 18% decrease in write time respectively at 70% efficiency achieved with STC=2856 eV-pm/V (Fig. (5-15)).

5.4 EFET SRAM with dynamic $V_{B,AX}$ modulation (EFET SRAM-II)

The possibility of device-circuit co-optimization through back contact and STC in EFET based circuits provides impetus for circuit modifications to the 6T EFET SRAM-I cell design. Recall that

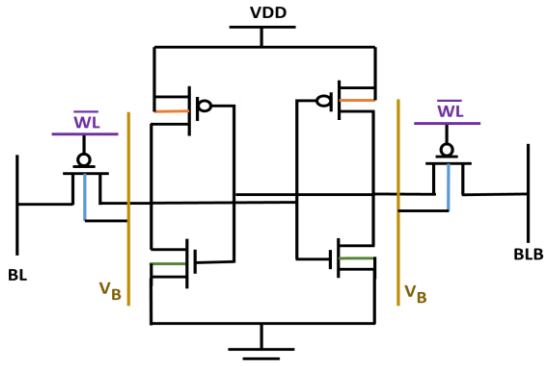

Figure 5-16 Proposed EFET SRAM-II with controllable back voltage of access transistor

EFET SRAM-I utilizes EFET as drop-in replacement in 6T 2D FET SRAM. It is known that in order to improve stability, the EFET access transistor should be made weaker compared to the 2D FET. Hence, there is a need for a local modification to the circuit. Since, design time modifications mostly affect transistors globally, we look into run time circuit modification for enhancing the read stability. The fourth terminal V_B can provide interesting ways for run time improvement of read stability. It has been discussed in Chapter 2 that positive bandgap change (ΔE_G) which results in higher I_{ON} in EFET is directly proportional to V_{GB}. By appropriate tuning of V_B, the access transistor strength can be modulated. In this regard, we propose EFET SRAM-II with separate bias control for V_B of the access transistor (Fig. (5-16)).

(A) V_B optimization for Read

In an ON state p-EFET (V_G=0V) and V_B=V_{DD}, | V_{GB} |=V_{DD} (or V_{GB}=-V_{DD}). Note that for the p-EFET bias conditions, piezoelectric constant is negative (d_{33}=-850pm/V) and overall ΔE_G (2.7) is positive. By decreasing V_B, |V_{GB} | decreases from V_{DD} and ΔE_G diminishes. This implies that increasing V_B lowers I_{ON} in a p-EFET, which is observed in the access transistor drive current of the SRAM. Consequently, time taken to charge BL increases. At V_B=0.2V, read time in EFET 1 is ~30% higher than 2D FET. At the same time, V_B has opposing effect on read stability. The weakening of the access transistor by decreasing its V_B results in pull up EFET (V_{GB}=|V_{DD}|) holding V_Q more strongly to ~V_{DD}. Consequently, noise margin increases.

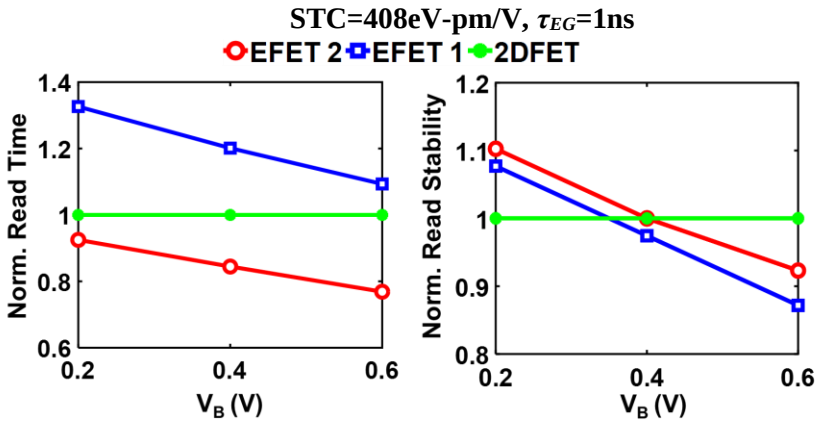

Figure 5-17 Read performance of EFET SRAM-II different V_B showing decrease in read time and stability with increase in V_B due to increase in access transistor strength.

At V_B=0.2V, ~10% improvement in noise margin is achieved for EFET 1 and EFET 2 respectively. Increasing V_B (=0.6V) results in better read time at the cost of lowering read margin. At V_B=0.6V, EFET 2 SRAM shows ~20% decrease in read time. These trends are observed in Fig. (5-17).

(B) Read Optimization Considering STC and V_B

The relation of change in bandgap, $\Delta E_G = STC.V_{GB}$ (2.7) and separate V_B control in EFET SRAM-II allows us for STC and V_B co-optimization. Fig. 5-18 shows the effect of STC-V_B co-optimization on read stability. By driving V_B of the access transistor to 0V, $|V_{GB}|$=0V (V_G=V_{WL}=0) and ΔE_G=0. Hence, the electrostrictive effect of the access transistor is nullified. Note that the pull up transistor ($|V_{GB}|$=V_{DD}) is stronger than the access transistor. Further, increasing STC enhances the pull up transistor strength but without impacting the access transistor (which is in ΔE_G=0 condition). In consequence, V_Q is pulled up more closely to V_{DD} resulting in higher read margin. The read margin for EFET SRAM-II at STC=408eV-pm/V (10% efficiency) is ~20% higher than 2D FET SRAM and can be further enhanced to ~70% at 70% efficiency (Fig. (5-18)).

The unique feature of read optimization in EFET SRAM-II through V_B can be applied to counter the effect of global process variations. Process corners with fast p-EFET result in lower read time and lower stability in SRAMs. V_B optimization with V_B=0V can be implemented to improve the read margin in the fast p-EFET corner as shown in Fig. 5-19. Conversely, SRAMs designed around slow p-EFET corners can be optimized with V_B=0.4V to achieve lower read time.

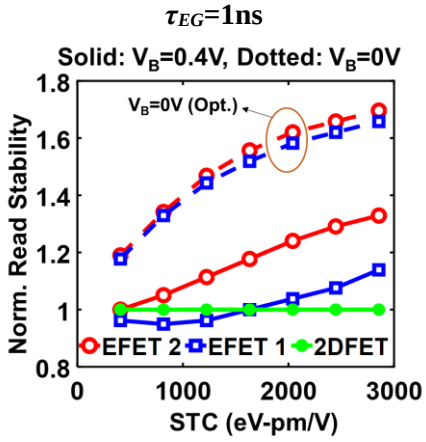

Figure 5-18 Read stability optimization of EFET SRAM-II with STC and V_B. V_B=0V shows drastic improvement is read noise margin due to weak access transistor.

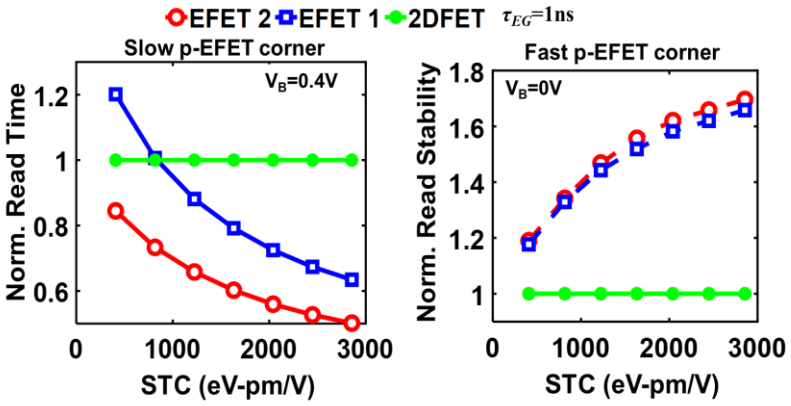

Figure 5-19 Read optimization of EFET SRAM-II with STC and V_B for slow and fast corner.

(C) Write Optimization with STC and V_B

In section 5.3(D) (EFET SRAM-I), we observed that increasing STC lowers write time when V_B is tied to V_{DD}=0.4V. However, the write time of EFET 1 was 1.2X higher than 2D FET SRAM and iso write time condition was achieved at 30% efficiency (Fig. (5-15)). In EFET SRAM-II, by leveraging the run time bias control of V_B (=0.6V), the write time can be further decreased and iso write time can be achieved at 20% efficiency. Note that increasing V_B enhances electrostriction in p-EFET ($|V_{GB}|$ and ΔE_G increases). At 70% efficiency, 30% and 50% reduction in write time can be

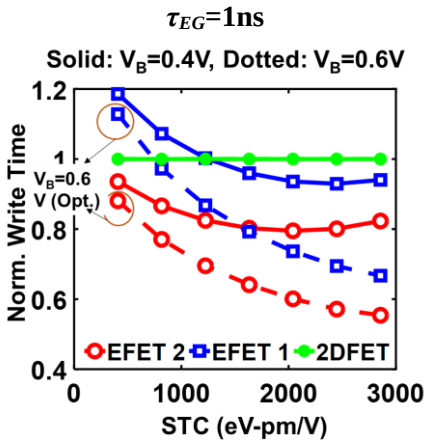

Figure 5-20 Write operation optimization of EFET SRAM-II with STC and V_B. By increasing V_B=0.6V write time decreases and iso write time of EFET 1 SRAM-II is achieved at lower STC.

obtained in EFET-1 SRAM-II and EFET-2 SRAM-II when V_B is optimized at 0.6V. These trends are observed in Fig. (5-20)

5.5 Summary

Following are the contributions of this chapter:

1. We perform a comparative analysis of 6T SRAM with EFET as drop-in replacement (EFET SRAM-I) and 6T SRAM with 2D FET. Both EFET 1 (with overlap parasitic capacitance) and EFET 2 (with fringe parasitic capacitance) are used for the analysis of SRAM-I.
2. We propose a 6T EFET SRAM (EFET SRAM-II) with separate V_B control for the access transistor. Similar to the above analysis, both EFET 1 and EFET 2 are used for its analysis.
3. At τ_{EG}=1ns considered in this work (derived from material parameters) and STC=408eV-pm/V (10% efficiency), the performance of EFET 2 SRAM-I is better than EFET 1 SRAM-I. In the former we achieve 15% lower read time at comparable read stability and 3% decrease in write time compared to 2D FET SRAM.
4. τ_{EG} impacts read and write performance. Decreasing τ_{EG} lowers read time at the cost of lower read stability. At τ_{EG}=1ps, EFET 2 SRAM-I shows 33% lower read time at the cost of 5% degraded read margin and 35% lower write time. At τ_{EG}=10ns, EFET 2 SRAM-I shows read time comparable to 2D FET with 15% improved read margin but write time increases by 9%.
5. STC allows unique optimization of the EFET SRAM read performance. EFET 1 SRAM-I and EFET 2 SRAM-I shows 14% and 33% increase in noise margin when STC=2856 eV-pm/V (70% efficiency). At the same STC, read time for the respective SRAMs decreases by 30% and 50%. Write time decreases by 6% and 18% respectively at 70% efficiency.

6. V_B and STC co-optimization enables aggressive improvement of read stability in EFET SRAM-II. 20% and 70% increase in read noise margin is observed at 70% efficiency with V_B=0V for EFET 1 SRAM-II and EFET 2 SRAM-II.
7. Using V_B modulation (=0.6V) and STC=2856 eV-pm/V (70% efficiency), 30% and 50% reduction in write time can be obtained in EFET 1 SRAM-II and EFET 2 SRAM-II.

Chapter 6

Conclusion and Future Work

6.1 Conclusion

In this work we present a Verilog A based circuit compatible compact model of the novel steep switching device known as the Electrostrictive Field Effect Transistor (EFET) and present its characteristics through HSPICE simulations. The model solves the governing equations of the electrostrictive effect and 2D electrostatics self-consistently, while also considering the parasitic capacitances of the device. We explore the various opportunities provided by EFET for device circuit co-optimization. Finally, we study the performance of EFET based circuits and utilize device-circuit co-optimization analysis to enhance their performance. Specifically, we study EFET based ring oscillator and SRAM. In this work, we propose an SRAM design for optimizing read and write performance of the SRAM. We summarize the outcome of this work as following:

(I) **Analysis of EFET characteristics and design space for optimizing electrostriction**

The material properties of the electrostrictive and 2D material (STC) play an important role in determining bandgap modulation; hence device performance. In addition, the impact of back contact (V_B) is coupled to bandgap modulation. Our results show that increasing STC to 2856 eV-pm/V (70% efficiency) leads to 42% decrease in SS and 7.5X increase in $I_{ON.}$ At 10% efficiency, 163% increase of ON current and 9% decrease in SS can be obtained. In addition, by modulating V_B=-0.6V, I_{ON} increases by 2.8X at the cost of higher I_{OFF}. Increasing V_B to 0.6V, decreases I_{OFF} by 10X and I_{ON} by 1.3X respectively.

(II) **Optimization of parasitic capacitance**

We evaluate the parasitic capacitances in the proposed EFET device structure (EFET 1) and conclude that high overlap gate-source/drain capacitance may lead to delay overhead in EFET 1 based circuits compared to 2D FET circuits. We propose an alternative EFET structure (EFET

2) with reduced gate-source/drain capacitance which is comparable to baseline 2D-FET. Our study shows that EFET 2 requires lower energy at iso-delay compared to EFET 1.

(III) **EFET based circuits and device-circuit co-optimization**

- **Ring Oscillator:** The ring oscillator analysis reveals that high parasitic capacitance in EFET (C_{GB}, $C_{GD/GS,OV}$) may lead to sub-optimal EFET performance (high energy-delay). Ideal EFET RO without transduction delay and parasitic capacitance ($C_{GS,GD}$ and C_{GB}) shows 1.5X lower delay than 2D FET RO at iso-energy. EFET 1 RO (with transduction delay and parasitic capacitance) shows 6.4X higher energy than 2DFET RO at iso-delay, while EFET 2 shows 2.26X higher delay at iso-energy. In wire capacitance (C_W>2fF) dominated circuits, EFET 2 based RO performs similar to 2D FET. STC optimization (70% efficiency) allows performance of EFET 1 RO to be matched to that of 2D FET RO while EFET 2 RO shows ~1.7X reduced energy at iso-delay (=0.18ns) compared to 2D FET RO.
- **SRAM Design:** We perform a comparative analysis of 6T SRAM with EFET as drop-in replacement (EFET SRAM-I) and 6T SRAM with 2D FET. In addition, we leverage the back contact of EFET to propose EFET SRAM-II with separate V_B control for the access transistor. Our study provides a comprehensive analysis of SRAM I and II with EFET 1 and EFET 2 (mentioned in II) with respect to the following design space: (a) transduction delay (b) STC and (c) V_B. We show that co-optimization of STC and V_B leads to significant enhancement of EFET SRAM performance.

  Transduction delay in the electrostrictive material affects SRAM read time, read stability and write time. For $\tau_{EG} = 1ns$ considered in this work (derived from material parameters) and STC=408eV-pm/V (10% efficiency), the performance of SRAM-I with EFET 2 is better with 15% lower read time at comparable read stability and 3% decrease in write time compared to 2D FET SRAM. Decreasing τ_{EG} lowers read time at the cost of lower read stability. At $\tau_{EG} = 1ps$, EFET 2 SRAM-I shows 33% lower read time at the cost of 5%

degraded read margin. At $\tau_{EG} = 10ns$, EFET 2 SRAM-I gives read time comparable to 2D FET with 15% improved read margin. At τ_{EG}=1ps, EFET 2 SRAM-I displays 35% lower write time while at τ_{EG}=*10ns*, write time increases by 9%.

STC allows unique optimization of the EFET SRAM-I read performance. EFET 1 SRAM-I and EFET 2 SRAM-I 14% and 33% increase in noise margin when STC=2856 eV-pm/V (70% efficiency). At the same STC, read time for the respective SRAMs decreases by 30% and 50%. Write time decreases by 6% and 18% respectively at 70% efficiency.

The EFET SRAM-II design allows us to perform back contact (of access transistor) and STC co-optimization, which leads to aggressive improvement of read stability and write time. 20% and 70% increase in read noise margin is observed at 70% efficiency with V_B=0V for EFET 1 SRAM-II and EFET 2 SRAM-II. Using V_B modulation (=0.6V) and STC=2856 eV-pm/V (70% efficiency), 30% and 50% reduction in write time can be obtained in EFET 1 SRAM-II and EFET 2 SRAM-II.

Based on this work we conclude that EFETs have huge potential to replace conventional transistors in design of circuits for low power domain. Nevertheless, as discussed, optimization of STC and V_B is crucial for the design of circuits based on EFET. In summary, with a combination of STC and V_B co-design, overheads of EFETs can be mitigated making them a suitable candidate for low power design.

6.2 Future Work

A future line of research could be the employment of write-assist techniques such as negative bit line and boosted word line to remove the write time penalty exhibited by EFET SRAMs. Moreover, analysis of other logic gates based on EFETs should be explored. The model for EFET can be extended to include the Schottky contact effects and field dependent mobility.

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