PLASMA-ENHANCED ATOMIC LAYER DEPOSITION ZINC OXIDE FLEXIBLE THIN FILM ELECTRONICS

A Dissertation in

Electrical Engineering

by

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ABSTRACT

This thesis demonstrates high performance flexible thin film electronics fabricated by low temperature process. A novel process for forming high quality stable oxide films using weak oxidant plasma-enhanced atomic layer deposition (PEALD) has been used to achieve fastest flexible oxide integrated circuits reported to date. In addition, a unique approach based on plasma-enhanced chemical vapor deposition (PECVD) silicon nitride for organic light emitting diodes (OLEDs) encapsulation at low temperature (<70 °C) is also reported.

Among several low temperature deposition approaches PEALD process provides highly crystalline and dense ZnO thin films which are uniform and conformal at 200 °C. Crossover measurement results also demonstrate the advantage of PEALD process in thin film deposition on flexible substrates. PEALD ZnO flexible TFTs have high field-effect mobility (~ 20 cm²/V·s) and excellent bias stress stability with ALD Al₂O₃ passivation. 15-stage ring oscillators with propagation delay of <20 nsec/stage have been successfully fabricated on flexible substrates. To the best of our knowledge, these are the fastest oxide-semiconductor circuits on flexible substrates reported to date, and they are about 20 times faster than the best previous report.

This thesis also presents the investigation of ZnO device physics by modeling. Non-ideal ZnO device characteristics, including passivation, contacts, and output conductance, have been well modeled and verified with experimental results.
Two different approaches were also proposed to extract device parameters for compact models and form the foundation for later circuit design and simulations. A TCAD ZnO model is established and can well describe the operation physics from single transistor to simple circuits. This model is verified by reasonable agreement with experimental data.

Building on the results of ZnO TFTs and circuits, several ZnO based applications have been demonstrated. Microsensors with ZnO pyroFETs have been fabricated on flexible substrates for implantable application, and temperature sensitivity of 7 mV/°C has been obtained. Moreover, PEALD ZnO also exhibits excellent low noise characteristics. A Hooge parameter of less than $10^{-4}$ was extracted from low frequency noise measurements. Based on the radiation hardness of PEALD ZnO, TFTs with Gadolinium as the floating gate have been also demonstrated in neutron detection.
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Chapter 1

Introduction

1.1 Overview

Thin films technology has established an important role in the electronics industry for many years, and significant interest has emerged from its applications such as photovoltaic, batteries, sensors, information storage, lighting, and large area electronics. In the meantime displays based on a variety of technologies act as human-machine interfaces in tremendous applications, such as cellular phones, digital cameras, and laptops. It is expected that display applications using thin-film electronics will become a $7.3 billion industry by 2011. The high demand for portable devices requires that thin films in flat panel displays are large and lightweight, use low power, and have high resolution.

Compared to most commercially available liquid crystal displays (LCDs) and plasma screens, organic light emitting diodes (OLEDs) have a variety of desired technology features, including wider viewing angles, higher brightness, and richer colors due to its inherently emissive properties. Nevertheless, OLED lifetime is still a primary obstacle for practical use in displays. Exposure to moisture and humidity quickly degrades the performance of OLEDs, and it is necessary to have an encapsulation layer. Several approaches have been made to improve OLED lifetimes. Rigid encapsulation methods such as glass-on-glass encapsulation are effective, but negate many of the advantages of
using flexible substrates. Thin film encapsulation seems to be the most natural solution for protecting OLEDs while also maintaining the advantages of flexible substrates.

In addition to encapsulation of OLEDs, backplane in flat-panel display has also made rapid developments in the last two decades, and thin film transistors (TFTs) with hydrogenated amorphous silicon (a-Si:H) or polysilicon (poly-Si) based semiconductors have been widely used. However, it is practically difficult to apply a-Si:H TFTs for high resolution display due to their low mobility of less than 1 cm²/V·s and poor electrical stress stability. On the other hand, some limitations occur for poly-Si TFTs in scaling up for large-area display, such as more complicated processes, higher cost, and non-uniform electrical properties. Oxide semiconductor based TFTs emerging in recent years may overcome these issues. Among various oxide semiconductors, zinc oxide (ZnO) has a strong potential to be used as the next-generation backplane technology. ZnO is wide bandgap material, and insensitive to visible light. ZnO based TFTs have not only higher performance but also improved stability compared to a-Si:H. Its lower processing temperatures may also permit the use of polymeric substrates, which are very attractive for portable electronics.

Although glass is used as the starting substrate material in the fabrication process of most flat panel displays, it has the undesirable characteristics of being extremely fragile and needing additional efforts to avoid damages. Therefore, mechanically flexible electronics have the potential to realize novel applications, and they have attracted expanding studies over the past several years. Transistors with high mobilities, low leakage currents, and
appropriate threshold voltages are desirable for high-performance active-matrix display applications, particularly for the integration of driver circuitry, but low temperatures process (<300 °C) must be maintained for compatibility with low-cost plastic substrate materials.

1.2 Research Objectives and Thesis Organization

This work will demonstrate high performance flexible thin film electronics fabricated by low temperature process. Several low temperature deposition approaches will be discussed. Among them is a novel process for forming high quality stable oxide films at low temperature using weak oxidant plasma-enhanced atomic layer deposition (PEALD), which is more suitable for flexible thin film electronics. Transistor modeling will be also addressed in detail for further understanding of device physics and laying the foundation for several practical oxide thin film based applications.

Chapter 2 will describe a unique approach for OLEDs thin film encapsulation: low temperature plasma enhanced chemical vapor deposition (PECVD) silicon nitride. A brief description of the deposition process will provide necessary information for thin film optimization, and two different methods will be discussed on OLEDs encapsulation. The results will be compared to mature glass-to-glass encapsulation, which is currently widely used in the display industry. The chapter will conclude with a discussion of encapsulation on flexible OLEDs.
Chapter 3 will discuss several approaches for depositing a high performance oxide semiconductor at a low temperature. A short review of PECVD ZnO will address the importance of weak reactants and plasma in the process. Then an improved process, pulsed-PECVD deposition, will be described in detail, from material property to devices both on glass and silicon substrates. The device performance will demonstrate that pulsed-PECVD plasma deposition is a promising approach and may have potential for other metal oxide thin film synthesis. The chapter will conclude with a brief description of PEALD process and its advantages in flexible electronic applications.

Chapter 4 will mainly describe high performance oxide semiconductor devices and circuits on flexible substrates. Many of the potential challenges associated with fabrication on flexible substrates will be fully discussed, including the surface roughness of the substrate, chemical and thermal stability, and dielectric integrity. In addition to that device stability and bending stress, results will hopefully provide some insights for practical flexible application. The chapter will conclude with the demonstration of the fastest oxide circuits on flexible substrates.

Chapter 5 will focus on the ZnO thin film transistor modeling. A TCAD Sentaurus Device simulator will be mainly used to understand non-ideal device characteristics, including chemical doping on the back interface from passivation, gated diode devices with Schottky contacts, and output conductance caused by self-heating. On the other hand, two different approaches (surface potential model and TCAD) will be discussed for better understanding electron transport in ZnO TFTs. Corresponding device parameters
will be extracted for a compact model, and the chapter will conclude with simple circuit modeling including inverters and ring oscillators.

Chapter 6 will present the applications of ZnO thin film electronics. Starting from low frequency noise measurement, PEALD ZnO will show the lowest Hooge parameter of all the thin film semiconductors. Together with its pyroelectric property, PEALD ZnO will be demonstrated as an ideal candidate for temperature sensors and thermal imaging. Finally, the radiation hardness of ZnO will be described and the corresponding method to detect neutrons will be discussed.

Chapter 7 will conclude the thesis by summarizing the work in flexible thin film electronics and proposing several ideas for future work. Negative bias stress stability of PEALD ZnO is one of the most important issues that need to be considered before practical application. Additionally, fully transparent ZnO devices on flexible Polyethylene naphthalene (PEN) or Polyethylene terephthalate (PET) substrates will also be interesting because of the combination with a self-gate aligned process, and corresponding circuit speed will be expected to further increase. The third will be a CMOS circuit, in which stable and high performance p-type semiconductor is required.
Chapter 2

Low Temperature Thin Film Encapsulation

2.1 Background

Organic light emitting diodes (OLEDs) have been widely considered the next generation display technology because of their wider viewing angles, higher brightness, and richer colors due to their inherently emissive properties when compared to most commercially available liquid crystal displays (LCDs) and plasma screens. Nevertheless, OLED lifetime is still a primary obstacle for practical use in displays. Exposure to moisture and humidity quickly degrades the device performance, and it is necessary to have an encapsulation layer.

Most OLEDs to date have been used for glass-based displays, and the most effective solution for encapsulation has been sealing the device with a glass lid or metal in an inert atmosphere by UV-cured epoxy resin. Getter materials (Calcium oxide or barium oxide) are often stored within the package, eliminating any moisture and oxygen from residues and diffusion through the seal as shown in Figure 2.1 (a) [1]. However, the conventional encapsulation techniques are not compatible with flexible displays due to their rigidity; thus, thin film direct encapsulation is of interest because of its great flexibility and decreased concern for abrasion damage from the lid. Figure 2.1 (b) and (c) show two typical thin film encapsulations: monolithic thin film, and laminated barrier-coated lid. Generally, thin film encapsulation materials can be categorized into two classes: organic polymer-based barrier encapsulates, and inorganic thin films. The typical requirement of
water vapor transmission rate (WVTR) and oxygen transmission rate (OTR) for sufficient encapsulation is less than $10^{-6}$ (g/m$^2$/day) and $10^{-3}$ (cm$^3$/m$^2$/day) respectively. Table 2.1 compared permeation rates for several common materials used as encapsulates [2]. It is clear that polymer materials could provide better ruggedness than glass and good surface coverage, but they do not provide sufficient protection from water and oxygen permeation. Inorganic materials have much lower permeation rates, but may suffer from film defects and uniformity depending on the deposition techniques.
In the case of thin film direct encapsulation, the thin film itself must be robust enough for handling by the users, and its deposition process must be compatible with OLEDs as well. It is critical to have low temperature thin film deposition and process to avoid device degradation, and any contacts (plasma or solvents) to the device’s active region must be minimized to prevent damages. Several groups have demonstrated that longer OLED lifetime could be achieved by thin film encapsulation [3-5], and combinations of inorganic and polymer films have shown promising results [6].

### 2.2 Low Temperature PECVD Silicon Nitride Process

Silicon nitride is commonly used as a dielectric, and also as a scratch and ion barrier for completed circuitry. For applications requiring deposition at low temperatures, silicon nitride thin films are typically deposited by plasma enhanced chemical vapor deposition (PECVD) from silane and ammonia. For depositions at substrate temperatures from 250 ~ 400 °C this approach can provide films with acceptable dielectric and etching characteristics. However, as the deposition temperature is reduced to 200 °C and lower,

<table>
<thead>
<tr>
<th>Film</th>
<th>WVTR (g/m²/day)</th>
<th>OTR (cm³(STP)/m²/day)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Polyethylene</td>
<td>1.2 ~ 5.9</td>
<td>70 ~ 550</td>
</tr>
<tr>
<td>Polypropylene</td>
<td>1.5 ~ 5.9</td>
<td>93 ~ 300</td>
</tr>
<tr>
<td>Polystyrene</td>
<td>7.9 ~ 40</td>
<td>200 ~ 540</td>
</tr>
<tr>
<td>PET</td>
<td>3.9 ~ 17</td>
<td></td>
</tr>
<tr>
<td>PEN</td>
<td></td>
<td>3.0</td>
</tr>
<tr>
<td>Polyimide</td>
<td>0.4 ~ 21</td>
<td>0.04 ~ 17</td>
</tr>
<tr>
<td>SiOx/PET</td>
<td></td>
<td>0.007 ~ 0.03</td>
</tr>
<tr>
<td>OLED requirement</td>
<td></td>
<td>10⁻⁶</td>
</tr>
<tr>
<td></td>
<td></td>
<td>10⁻⁵ ~ 10⁻³</td>
</tr>
</tbody>
</table>

*Table 2.1 - Permeation rates for common encapsulants materials.*
film quality degrades due to increased incorporation of hydrogen [7]. For OLED encapsulation, a deposition temperature well below the glass transition temperature of the OLED organic materials (typically 100 ~ 150 °C) is desirable, and conventional PECVD SiNx films deposited at such low temperatures typically have poor quality.

A new approach for depositing PECVD SiNx film at a low temperature was investigated here for the feasibility of encapsulating OLEDs. The deposition system was commercialized Ionic Systems [8]. The cutaway view of the process chamber is shown in Figure 2.2. In this drawing, the substrates are fixed between two housings. Each housing is covered with stainless steel mesh, which is either ground or insulated. The first housing acts as the vehicle for the introduction of the reactant gases into the process chamber. Within this housing are a plurality of chambers which alternate the delivery of silane and nitrogen. The silane chambers have a baffle inside to distribute the gas uniformly throughout the chamber. The nitrogen cavities have a baffle as well, but it is isolated from the ground and attached to an atomizer RF generator, which produces plasma in the nitrogen channels to dissociate or ‘atomize’ nitrogen and provide it in an atomic state to the plasma in the main chamber, where the deposition occurs. The second housing is covered by the insulated main chamber, where hot electrode screen is attached to the main RF generator producing plasma surrounding the substrates. This second housing contains a pumpout baffle to further promote the laminar flow conditions in the deposition area.
This approach to plasma deposition eliminates the need for ammonia as a nitrogen donor, using instead ultra-high purity diatomic nitrogen. This produces improved film stoichiometry and greatly reduces the amount of hydrogen available to incorporate into the film. It also allows films of very high quality to be deposited uniformly over large areas (~0.5 m²), with no heat used in the reaction. The system is load-locked and allows film stress to be controlled by varying film stoichiometry.

Table 2.2 provides a summary of the deposition parameters used in this study. Four deposition substrates were mounted on a vertical substrate holder (104 cm × 94 cm) and lowered into the load chamber. After load chamber evacuation, the substrate holder was transferred to the deposition chamber for film deposition. Substrate temperature does rise during film deposition, and sample mounted temperature change indicators and paints
were used to verify a maximum process temperature of less than 70 °C for long film deposition time.

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>Substrate temperature</td>
<td>Room temperature</td>
</tr>
<tr>
<td>Nitrogen flow rate</td>
<td>100 sccm to 180 sccm</td>
</tr>
<tr>
<td>Silane flow rate</td>
<td>15 sccm</td>
</tr>
<tr>
<td>Pressure</td>
<td>300 mtorr</td>
</tr>
<tr>
<td>Main chamber power density</td>
<td>8.79 mW/cc</td>
</tr>
<tr>
<td>Atomizer chamber power density</td>
<td>136 mW/cc to 227 mW/cc</td>
</tr>
</tbody>
</table>

*Table 2.2 – Deposition conditions and parameter range of SiNx thin films.*

### 2.3 Thin Film Characterization and Optimization

The stoichiometry of silicon nitride films is strongly related to the chemical composition of silicon, nitrogen, and hydrogen, and it also plays a major role in determining physical and chemical properties such as refractive index and intrinsic film stress. Changing the deposition parameters can alter the film stoichiometry and film properties significantly. Since we use bottom emission OLEDs here, it is important for the encapsulation layer to be transparent in OLED emitting spectrum [9]. As Figure 2.3 (a) shows, 500 nm thick SiNx exhibits more than 80% transmission over a wide spectrum range.

![Figure 2.3](image)

*Figure 2.3 – (a) Transmission spectrum for SiNx with different nitrogen contents. (b) Operational encapsulated OLEDs on 6” glass substrate.*
On the other hand, the deposited thin films are ultimately intended to encapsulate large area displays, as shown in Figure 2.3 (b); it is desirable to have low stress films, allowing a small minimum bending radius without delamination from the underlying structure. The parameters for modifying film stress include power, flow rate, reaction power, and plasma stoichiometry. The stress of low temperature PECVD SiN$_x$ films was measured on [100] silicon wafers by using a Tencor FLX 2320. This instrument measure changes in the radius of curvature in a sample with film deposition, which can then be correlated to the stress of the deposited film. Figure 2.4 (a) shows film stress results as a function of the nitrogen to silane flow ratio for two different atomizer RF powers. Increasing silicon incorporation tends to make film stress more compressive, and reducing silicon incorporation tends to make film stress more tensile. A minimum compressive film stress of 2.9x10$^8$ dynes/cm$^2$ was obtained for a N$_2$/SiH$_4$ flow ratio of 9 (135 sccm / 15 sccm).

![Film stress vs N$_2$/SiH$_4$ ratio](image1)

**Figure 2.4** – (a) SiNx film stress as a function of silane and nitrogen ratio. (b) BOE etching rate and optical refractive index of SiNx film.

The optical refractive index of SiNx thin films was also measured by ellipsometry, and it can be used as an unsophisticated, approximate indicator of film density. Figure 2.4 (b) shows that the film’s refractive index (measured at 628.7 nm) increases as the nitrogen-to-silane ratio decreases. The refractive index of stoichiometric silicon nitride with low
hydrogen content is expected to be about 2.05. Wet etch tests performed on high index films show a residue, likely silicon, indicating a silicon-rich film with silicon clusters. The RMS of surface roughness, measured by atomic force microscopy, is about 1~2 nm for 500 nm thick films on both silicon and flexible substrates, as Figure 2.5 shows.

![Figure 2.5](image)

**Figure 2.5** – (a) 500 nm SiNx on silicon substrate. (b) 500 nm SiNx on flexible substrate (PEN).

### 2.4 Single Layer Encapsulation

OLED test pixels of different types were received from Universal Display Cooperation, and both top and bottom emission devices were encapsulated by low temperature PECVD SiNx thin films. (A typical bottom emission OLED structure is described in Figure 2.6 (a).) OLEDs were then encapsulated on a 6”x6” glass plates with a 3x3 array of test structures and four individual OLED pixels in each test structure. Among these samples, spin-cast polyimide was patterned as the OLED isolation material. After encapsulation, the OLEDs were put into a humidity chamber with a fixed temperature of 65 ºC and a relative humidity of 85% for lifetime evaluation. These tests provide information about the causes and evolution of device failure in a relatively short time (compared to room
temperature tests). By monitoring the accelerated degradation, a better understanding of the mechanism of device failure can be reached.

A single layer, 1 μm thick, of SiNₓ film was used to encapsulate OLEDs. The optimized deposition conditions were SiH₄/N₂:14/98 sccm, atomizer power 150 W, and deposition power 500 W. Figure 2.6 (b) shows the single layer encapsulation results. There is no observable delamination, and OLED has excellent room temperature drive lifetime.

![Figure 2.6](image)

**Figure 2.6** – (a) Typical OLED structure for thin film passivation. (b) Single layer 1 μm SiNx encapsulation results.

Although the encapsulated device life was comparable with the ones with glass-to-glass encapsulation, the OLEDs still suffered from dark spots generation in a room temperature life test. A typical dark spot microscope picture is shown in Figure 2.7 (a), and possible formation mechanisms of dark spots have been already well studied [10, 11]. Besides the oxidation of the cathode due to the moisture, the pin holes in the encapsulation film can easily allow the oxygen and water to contact organic materials, generating non-emissive areas in OLEDs. As Figure 2.7 (b) shows, the byproducts from dark spots, typically H₂, are trapped and gradually accumulated inside the encapsulation layer, and finally cause
the delamination at the interface between adjacent layers of a device. Therefore, in order to achieve adequate OLED lifetime, the defect density in the encapsulation layer must be low enough to prevent the ingress of water and oxygen from the device layers, oxidization of the cathode, and formation of dark spots [12].

\[ \text{(a) Microscope picture of dark spots. (b) Dark spots generation in encapsulated OLEDs.} \]

Despite the fact that the optimized deposition conditions outlined in section 2.3 can provide dense and low stress thin film, the OLEDs show fast dark spot growth under accelerated testing (65 °C, 85 % RH), as shown in Figure 2.8 (a), indicating high defect density in the SiNₓ film. These defects can come from either film stoichiometry or particulate contaminations (such as pin holes) during the OLED manufacturing. The latter case is unlikely, not only because of high standard clean room environment, but also because of vertical loading in a low temperature PECVD system, which can prevent the adhesion of particles onto the OLED surface. As it is discussed previously, silicon clusters can form during the thin film deposition, especially with silicon rich condition. Therefore, Fourier transform infrared (FTIR) analysis was performed on optimized SiNx films for encapsulation, and it showed a relatively small, yet significant amount of silicon-silicon bonding, suggesting that flaws in the silicon nitride may stem in part from silicon clusters in the film. Hydrogen dilution has been reported as a method to improve the uniformity and encapsulation quality of silicon nitride films [13, 14], since it can etch
weak silicon-silicon bonding. Thus, a small amount of H\textsubscript{2} (SiH\textsubscript{4}/N\textsubscript{2}/H\textsubscript{2} = 15/100/15) was added into the PECVD process. A comparison of FTIR results is shown in Figure 2.8 (b) for films deposited with and without hydrogen dilution. Obviously, silicon-silicon bonding was significantly reduced with hydrogen dilution while silicon-hydrogen and nitrogen-hydrogen bonding were only slightly affected.

![Accelerated Shelf Test Results](image)

**Figure 2.8** – (a) Fast dark spots growth in accelerated life test. (b) Comparison of FTIR analysis on SiNx films with and without hydrogen dilution.

With hydrogen dilution in the SiNx process, thin film defect density from silicon clusters is expected to be greatly lowered, and encapsulated OLEDs should have a better chance to prevent water and oxygen permeation. An extreme life test environment, a tank filled with hot water (60 °C), was set up to verify this improvement. Encapsulated OLEDs were fully immersed and still functioned very well. No new dark spots were generated during the whole process, which demonstrates that hydrogen dilution is an effective way to lower defect density in the SiNx thin film.
It is noticeable that almost all the OLEDs have dark spots right after encapsulation. To find out how the dark spots were introduced in the process, two experiments were performed. The first experiment is shown in Figure 2.9 (a). Dark spots were intentionally introduced before encapsulation by simply exposing the OLEDs to water vapor for some time. Next, the encapsulation devices were immersed in hot water for 4 hours. The microscope pixel pictures show that no new dark spots were generated, and the original ones became bigger and bigger. This can be explained by the thermal growth of non-emissive areas. The second experiment results are shown in Figure 2.9 (b). Two groups of OLEDs were used for direct comparison. Group A was exposed to the air for 30 minutes before encapsulation, and group B was encapsulated instantly. Though both groups showed the same results after encapsulation, group A has dark spots generated after 30 minutes of immersion in hot water, while group B still has no new dark spots. It can be concluded that the dark spots in our encapsulated OLEDs actually come from the sample transportation, since encapsulation and OLED fabrication were done at different places. The defect density in low temperature PECVD SiNx is low enough for encapsulation in OLEDs’ real application such as commercial products.
In addition to silicon clustering, particles are a likely source of defects in our single layer SiNₓ films. One way to decouple the defects in the film is to use multiple layer encapsulations [15]. Vitex Systems has succeeded in depositing such coatings using an organic/inorganic, thin film multilayer structure termed Barix™ encapsulation, and 2500 hours lifetime (half initial luminance as criteria) was achieved on a DC tested 5mm2 FOLED pixel [6, 16]. However, there are several disadvantages of this organic/inorganic approach. The whole encapsulation layer is very thick, typically several microns for 4 ~ 5 layer pairs. The sample has been moved back and forth between organic and inorganic material deposition, which dramatically increases the possibility of particulate contamination. Last but not least, the edge seal problem still exists.

In single layer encapsulation, we have demonstrated that optimized low temperature PECVD SiNx can have quite low defect density, and also possibly cover the edges very well because most of the dark spots were located inside the pixel instead of on the edge.
Thus, it makes sense for us to directly use multilayer SiNx for encapsulation. The first layer (500 nm SiNx) has tensile but extremely low stress, accommodating the OLED stack beneath that. It also planarizes the topography on the substrate, providing a smooth surface for the second layer deposition. After first layer passivation, high-pressure water jet cleaning was used to remove trapped surface particles. By decoupling the successive 500 nm SiNx layer, the propagation of defects from layer to layer is effectively stopped, and the final defect density is further reduced, compared to single layer encapsulation (1 μm thick SiNx). This bilayer approach increased the total path length for moisture or oxygen diffusion through pinholes or defects in the layers. In addition to that, it also decreases the probability of catastrophic failure due to some enormous defects.

Figure 2.10 (a) shows normalized lifetime results for bilayer encapsulated OLEDs under an accelerated test environment. Compared to traditional glass-to-glass encapsulation, the bilayer thin film approach has about three times longer lifetime. Devices were also submerged in a hot water bath, and any defects in the encapsulation film, including the effect on the edges, can be easily found by this severe environment testing. After 14 hours operation in the hot water, the bilayer encapsulated OLEDs were still functional, and their intensity was nearly unchanged, as Figure 2.10 (b) shows. There were only a few growing dark spots that appear to be related to residual defects in the deposited film. These results are quite encouraging especially for flexible display.
Electrical characteristics and electroluminescent spectra were also compared in Figure 2.1 for OLEDs before and after thin film encapsulation. The J-V (current density versus voltage) curve was measured with a Keithley 236 source measurement unit, and thin film encapsulated OLEDs showed the same characteristics as the ones encapsulated by glass in Figure 2.1 (a), demonstrating that the plasma and chemical reaction in the deposition were safe for OLEDs. The electroluminescent spectra (EL) of the bottom and top emission OLEDs were also compared in Figure 2.1 (b) for both glass and thin film encapsulation. It is clear that thin film encapsulation dramatically changed the OLEDs spectra, and their electroluminescent all exhibited red shift despite of device structure difference. In thin film encapsulation SiNx has become an integral part of the optical microcavity, and OLED output spectra is determined not only by the encapsulation film thickness but also the material’s refractive index. This actually increases the freedom for OLED design, where the thin film encapsulation layer can be adjusted to obtain or further tune the output spectra. It is worth pointing out that the EL intensity difference for top
emission OLEDs are from device variation, not real intensity decrease for thin film encapsulation.

![Figure 2.11](image)

**Figure 2.11** – (a) Comparison of OLED $J-V$ characteristics with low temperature SiNx and glass-to-glass encapsulation, respectively. (b) Comparison of OLED output spectrum between SiNx thin film and glass encapsulation.

### 2.5 Flexible OLEDs Encapsulation

Substrate selection is extremely important for flexible OLEDs application, and its water vapor transmission rate (WVTR) and oxygen transmission rate (OTR) should be as low as possible. On the other hand, the dimension stability for flexible substrates should also be considered in OLED manufacturing. Polyimide was used here as a substrate due to its relative high glass transition temperature and low WVTR and OTR. Before OLED stack deposition, the substrate was carefully cleaned and coated with 500 nm low temperature SiNx on both sides, preventing moisture and oxygen diffusion in the latter process. 100 nm ITO was sputtered as the anode and patterned by lithography, and then the OLED stack was deposited through a shadow mask as the one on the glass substrate. Finally, flexible OLEDs were encapsulated with the same SiNx as before. Figure 2.12 shows the pictures of encapsulated flexible OLEDs. Devices were still functional when wrapped
around the beaker with a bending radius 2”, but edge delamination was observed after banding several times. This problem can finally lead to device failure, because the inorganic material of SiNx is brittle and cracks easily, especially when the substrates are encapsulated with a whole layer of thin film instead of only pixel areas.

![Image](image_url)

**Figure 2.12** – Flexible OLEDs encapsulation by low temperature PECVD SiNx.

In order to make thin film encapsulation compatible with flexible display, it is necessary to have pixel level encapsulation. Since the encapsulation layers are isolated from each other and form an island on the substrate, the internal stress caused by banding cannot accumulate and is easily released when the sample is back to flat status. In addition to that, pixel level encapsulation can effectively prevent catastrophic damages. If dark spots were generated and kept growing in one pixel, it would not transport or affect adjacent pixels, because the encapsulation layers are isolated from each other in this method. In
Figure 2.13 the details of pixel level encapsulation process are given. Thin film SiNₓ is first deposited onto ITO anodes, and is later isolated by lithography, providing anode edges protection. Following that, polyimide as the isolation layer is spin coated everywhere and forms an undercut profile by double lithography. Then, organic materials in the OLED stack are evaporated onto the whole sample. In the next Aluminum evaporation, samples are placed on the holder--not horizontally, but with a certain angle--leading to full Aluminum coverage on the edges of organic materials. Finally, another SiNₓ encapsulation layer is deposited on top and self-isolated by the patterned polyimide beneath layer.

In conclusion, with the advancement in flexible display technology, more pixels are now integrated and higher standards are required for defects control in encapsulations. Whereas the complexity of the OLED process is slightly increased, pixel level encapsulation can be a viable choice, one that is especially suitable for active-matrix OLEDs displays.
Chapter 3

ZnO Thin Film Transistor Technology

3.1 Background

Thin film electronics for large area applications have greatly improved the quality of human life since their introduction, decades ago. One of the most important technologies is the thin film transistor (TFT), which serves as a pixel control element (switch) in display backplanes and sensor arrays, and as an active circuit element in applications requiring computation. To increase electronic functionality for broader applications, new thin film semiconductor materials, manufacturing methods, and computer aided electronic design tools are required.

In general the structures of TFTs can be categorized into two main kinds according to the

![Figure 3.1 – Typical structures of common TFTs.](image)
position of their active layer: staggered, and coplanar as Figure 3.1 shows. Depending on the position of the gate electrode, they can be further divided into normal and inverted structure. From the material point of view, the semiconductors used as active channels in TFTs commonly include low temperature polycrystalline silicon (LTPS), hydrogenated amorphous silicon (a-Si:H), and organic based material. Among them, LTPS has the highest carrier mobility, a stable threshold voltage, and can be directly integrated with the drivers since it can provide both n-channel and p-channel devices. Staggered structure (top gate) is typically used because of the high temperature in a-Si:H recrystallization by laser annealing. However, it is difficult to achieve good yield and reasonable uniformity for LTPS due to the challenges associated with recrystallization. The higher process temperature (>300 °C) also needs special glass materials (quartz) and increases the manufacturing cost [17]. Therefore, LTPS applications are limited to small screen display, such as the mobile market.

Amorphous silicon provides greater spatial uniformity and a low temperature process. More importantly, it is relatively mature due to applications in photovoltaic. Inverted staggered structure (bottom gate and top contact) is widely used for a-Si:H TFTs in the manufacturing of display panels due to the performance consideration. In staggered structure, special care has to be taken to control the plasma power during the nitride deposition to avoid damaging the a-Si and dielectric interface. Though low mobility (~1cm²/V•s) of a-Si:H TFTs can be compensated by device design, there has not been a good way to solve the threshold voltage stability issue [18]. Organic materials also seem to be promising due to their low cost and comparable mobility with a-Si:H. Their device
structure is also made flexible by taking advantage of a solution process. However, organic materials are easily oxidized in air and need to be passivated, which is possible only in the case where inorganic thin film technology is used [19, 20].

Considering the TFTs discussed above, what is needed is a new, low temperature-deposited semiconductor material that can combine together the advantages of a-Si TFTs and LTPS so that large area electronics with high performance can be produced at reduced manufacturing costs. Oxide semiconductors thin film has been in the spotlight in recent years, and, especially for Zinc oxide (ZnO), its promising property has attracted tremendous interest in a variety of fields, such as transparent electronics, UV detectors, and sensor applications [21]. Its exciton binding energy is ~ 60 meV, which can enhance the luminescence of light emission for blue and UV optical devices. Also its wurtzite structure results in polar symmetry along the hexagonal axis, and can contribute to piezoelectricity and spontaneous polarization. Therefore ZnO epitaxial layer and single crystals are important for the development of surface acoustic wave (SAW) resonators and spintronics. In addition, ZnO in single crystal has electron Hall mobility of ~ 200 cm²/V·s and high electron saturation velocity at room temperature. It has superiority in high temperature endurance in air as a nature of oxides as well. These interesting electronic properties are expected to be advantageous to the high performance transistors. For the past decade, many publications have emerged discussing ZnO as an ideal candidate for TFT channel material. In table 3.1 ZnO is compared with other TFT technologies in several important aspects, such as manufacturability, device mobility, stability, uniformity over a large area, and process temperature. In addition to the aspects
outlined in that table, ZnO TFTs offer several other merits: (1) High mobility can be found both in crystalline and amorphous phases, because electron transport in ZnO is associated with the conduction band formed by s orbitals of metal cations, whose spherical and symmetric nature renders the orbital overlap and electron transport less sensitive to material disorders [22]. (2) Good transparency in visible light could be used to improve the aperture ratio of flat panel display, since ZnO is a direct wide bandgap material with bandgap energy of 3.37 eV [23]. (3) Devices can potentially be fabricated at low temperatures but while maintaining high performance [24].

<table>
<thead>
<tr>
<th>Materials</th>
<th>a-Si</th>
<th>Poly-Si</th>
<th>Organic</th>
<th>Zinc oxide</th>
</tr>
</thead>
<tbody>
<tr>
<td>Manufacturability</td>
<td>Good</td>
<td>Poor</td>
<td>Potentially good</td>
<td>Very good</td>
</tr>
<tr>
<td>Reproducibility</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Device mobility (cm²/V·s)</td>
<td>Low ~ 1</td>
<td>High ~ 80</td>
<td>Low ~ 1</td>
<td>~ 20 to 40</td>
</tr>
<tr>
<td>Uniformity over a large area</td>
<td>Good</td>
<td>Poor</td>
<td>Poor</td>
<td>Good</td>
</tr>
<tr>
<td>Device stability</td>
<td>Poor</td>
<td>Good</td>
<td>Poor</td>
<td>Good</td>
</tr>
<tr>
<td>Temperature (ºC)</td>
<td>~ 300</td>
<td>High</td>
<td>RT</td>
<td>RT ~ 200</td>
</tr>
</tbody>
</table>

*Table 3.1 – Comparison of materials used as active layer in thin film transistor technology.*

In addition to active layer semiconductor dielectric materials also play an important role in determining TFT performance. Due to the large bandgap and electron affinity (~ 4.5 eV) of ZnO, an insulator with a large bandgap (> 6 eV) is needed to provide barriers to both the valence and conduction bands. These requirements largely rule out most organic dielectrics and many inorganic dielectrics. PECVD silicon nitride is interesting due to its widespread integration into amorphous silicon TFTs for LCD displays. However, the band gap for silicon nitride is undesirably small (~ 5.1 eV), and charge trapping is known
to be a significant problem particularly for low temperature (< 200 °C) deposited
dielectrics. Al₂O₃ was chosen in this work due its large bandgap (~8.7 eV) and low
temperature deposition. However, it is a very difficult material to gas phase etch, and
chamber back etching processes are actually essential in maintaining system cleanliness
to ensure yield in large-area displays.

A variety of techniques have been used to deposit ZnO thin films, including metal
organic chemical vapor deposition (MOCVD) [25, 26], sputtering [27], pulsed laser
deposition (PLD) [28], ion beam assisted reactive deposition, and atomic layer deposition
(ALD) [29, 30]. Since the first ZnO thin film transistors were reported in 2000 [31],
great strides have been made to improve the device performance. Among all the reported
ZnO devices and circuits, TFTs fabricated by pulsed laser deposition (PLD) at 400 °C
(600 °C post annealing) on Si substrates had mobility over 100 cm²/V·s [32], and five-
stage ring oscillators based on 0.5 μm gate length indium-gallium-zinc-oxide (IGZO)
TFTs fabricated on silicon substrates had a propagation delay below 1 ns/stage for
bootstrapped ring oscillators and below 10 ns/stage for more conventional saturated load
ring oscillators [33]. Earlier, we also reported that ring oscillators fabricated on glass
substrates using ZnO thin films deposited by spatial atomic layer deposition (ALD) had a
propagation delay of 31 ns/stage [34].

Although devices and circuits built on silicon wafers allow understanding of material
peak performance, flexible electronics using semiconductor materials deposited at low
temperature are of interest for new applications on low cost substrates such as active-matrix displays and sensors.

3.2 Plasma-enhanced Chemical Vapor Deposition (PECVD)

There are few reports of ZnO by plasma enhanced chemical vapor deposition (PECVD) [35], which is the current technique used to deposit silicon nitride and amorphous silicon for large-area displays. For PECVD, the plasma used to aid in the decomposition of reactants may allow low-temperature thin film deposition without the need for post-deposition annealing [36].

We previously reported undoped thin film transistors (TFTs) with ZnO films deposited by PECVD with field-effect mobility of 10 cm²/V·s for gate dielectrics with relatively large leakage current, as shown in Figure 3.2 [37]. However, PECVD ZnO TFTs fabricated with low leakage dielectrics have reduced field-effect mobility (typically <1 cm²/V·s). As shown in Figure 3.3, ZnO TFTs turn on very slowly and have relatively
long reconversion region. Besides this, the circuits fabricated with these devices on glass substrates have poor performance, suggesting enormous interface states or bulk traps exist in these devices.

3.3 Pulsed-PECVD Deposition

Pulsed-PECVD has been reported on many materials depositions, with improvement in film quality for some [38, 39]. Based on the PECVD results, pulsed-PECVD was used here to improve ZnO material quality and the interface between the ZnO and dielectric. A pulsed-PECVD system with a 56 cm diameter electrode, circumferential gas input, and electrode-center pumping, as shown in Figure 3.4, was used for this approach. The substrates were loaded onto the lower, electrically grounded electrode. The powered upper electrode was connected to a 13.56 MHz RF power generator through an impedance-matching network, and an external pulse generator was used to turn the RF power, and plasma, on and off. The electrode spacing was 5 cm. The reactants were introduced from a gas ring, entering the plasma region (the region between the electrodes) at its outer edge, and flowing inward toward a pumping port at the center of

![Figure 3.3 – PECVD ZnO TFT with low leakage dielectrics (W/L = 100 μm/20 μm, tox = 150 nm). (a) ZnO TFT transfer characteristics for V_{DS} = 40 V, and (b) Output characteristics for several V_{GS}.](image)
the lower electrode. The substrate temperature was 200 °C and argon was used as the carrier gas for the diethylzinc (DEZ) bubbler, which was held at 18 °C to maintain a stable vapor pressure. In this approach the reactants were supplied continuously and the RF plasma was periodically pulsed to deposit thin films. The reaction byproducts generated by the plasma were effectively purged before the next plasma step. The weak reactants N₂O or CO₂ were used here to minimize reactions with the plasma off step that could result in non-uniform deposition. This is necessarily imperfect because reaction precursors are absorbed on the reactor interior during the plasma off step and can be desorbed back into the plasma and detrimentally impact film quality. For this reason, short plasma pulse times were used to favor film reactions from gas components near the substrates.

**Figure 3.4** – Schematic of pulsed PECVD ZnO deposition system.

In other words, pulsed-PECVD process is a simple modification to existing mature PECVD technology, and does not have any manufacturing barrier. It also exhibits PECVD advantages: low temperature, and good uniformity.
3.3.1 Deposition Process

For pulsed PECVD ZnO using CO₂ as the oxidant, the deposition rate as a function of CO₂ to DEZ ratio is shown in Figure 3.5 (a). The chamber process pressure was maintained at 440 mtorr, and CO₂ flow was fixed at 200 sccm. The deposition rate decreases as the CO₂ to DEZ ratio increases, suggesting that the process is metal organic limited. In the meantime, denser ZnO film is also grown according to the higher optical refractive index, as shown in Figure 3.5 (b), when DEZ to CO₂ ratio is decreased. In Figure 3.6 (a), with a fixed pulse and purge time, the deposition rate is almost constant for a wide range of plasma power. Figure 3.6 (b) shows that the deposition rate decreases somewhat with increasing purge time. This suggests that there are parasitic CVD processes associated with plasma generated byproducts, which compete with the pulsed PECVD.

![Figure 3.5](image-url) – CO₂ as oxidant: (a) Deposition rate as a function of CO₂ to DEZ ratio.
When \( \text{N}_2\text{O} \) is used as the oxidant, high RF power results in high reaction rates near the gas input ring and little film growth farther in on the electrode. This happens at a much lower power than for \( \text{CO}_2 \), likely because oxygen is more easily liberated from \( \text{N}_2\text{O} \). Figure 3.7 shows that for \( \text{N}_2\text{O} \) the deposition rate in the middle of the electrode ring decreases dramatically with increasing RF. For low RF power, the growth rate of \( \text{ZnO} \) with \( \text{N}_2\text{O} \) as the oxidant is about 50% larger than with \( \text{CO}_2 \).

**Figure 3.6** – \( \text{CO}_2 \) as oxidant. (a) Deposition rate versus plasma power. (b) Deposition rate as a function of purge time.

**Figure 3.7** – \( \text{N}_2\text{O} \) as oxidant: (a) deposition rate versus plasma power, (b) deposition rate as a function of purge time.
3.3.2 Film Characterization

The thickness and refractive index of the pulsed PECVD, undoped ZnO thin films were characterized by spectroscopic ellipsometry with a wavelength range of 350 ~ 1000 nm. In general, higher refractive index is correlated with denser films. Figure 3.8 (a) shows refractive index as a function of wavelength for 20 nm thick ZnO films deposited from CO$_2$ by pulsed PECVD, conventional PECVD, and PEALD at 200 °C. PECVD ZnO films were deposited in the same system as the pulsed-PECVD used, and the ratio of CO$_2$ to DEZ was about 10 with a RF power density of 0.05 W/cm$^2$. For PEALD ZnO, the process uses a weak oxidant both to purge the metal organic precursor and to react with the precursor during the plasma step, and it will be described in detail in the next section [40]. For pulsed PECVD, the cycle time was 10 seconds with a plasma on time of 2 seconds. The refractive index for the pulsed-PECVD ZnO was comparable to PEALD, and much higher than for ZnO deposited by PECVD. Figure 3.8 (b) shows results from room temperature photoluminescence, with a photon transition energy at 3.28 eV and a full-width at half–maximum (FWHM) of 300 meV. This transition energy is smaller than single crystal ZnO (3.4 eV), and it indicates there are defects levels in the bandgap for the pulsed PECVD ZnO. The inset picture in Figure 3.8 (b) is the AFM image for a 40 nm thick pulsed PECVD ZnO thin film. The RMS surface roughness was 1.5 nm, and the apparent grain size was about 35 nm.
3.3.3 Pulsed-PECVD ZnO TFTs

A bottom-gate TFT structure as shown in Figure 3.9 was used in this work. 100 nm thick Cr was deposited by ion beam sputtering on glass as a blanket gate layer with 35 nm of plasma-enhanced atomic layer deposition (PEALD) Al₂O₃ as the gate dielectric. As an alternative, a heavily doped silicon wafer with 50 nm thermal SiO₂ was used as the gate and gate dielectric. For either substrate and gate dielectric combination, 10 nm of undoped ZnO was deposited by pulsed PECVD at 200 °C. Finally, the ZnO was patterned by wet etching in diluted HCl, and titanium source and drain electrodes were deposited by sputtering and patterned by lift-off.

![Figure 3.8](image)

**Figure 3.8** – (a) Refractive index of ZnO thin films deposited by PECVD, PEALD, and pulsed-PECVD. (b) Room temperature photoluminescence spectra. Inset picture is 1 μm scan AFM image.

![Figure 3.9](image)

**Figure 3.9** – Bottom-gate ZnO TFT structure. (a) 35 nm PEALD Al₂O₃ as dielectric. (b) 50 nm thermal oxide as dielectric.
For comparison we fabricated ZnO TFTs from N₂O and DEZ on 50 nm thermal oxide and 35 nm PEALD Al₂O₃. Devices were measured with a HP semiconductor parameter analyzer 4156B with medium integration time, and measurement conditions had no effects on device performance. For devices with a channel width and length of 200 µm and 20 µm on PEALD Al₂O₃, a saturation mobility of 15 cm²/V·s, threshold voltage of 6.6 V, subthreshold slope of 370 mV/dev, and current on/off ratio of 10⁸ were extracted from √I_DS and Log(I_DS) versus V_GS curves, as shown in Figure 3.10 (a). Figure 3.10 (b) shows the I_DS versus V_DS characteristics for several values of gate voltage.

**Figure 3.10** – Pulsed PECVD ZnO TFT with 35 nm PEALD Al₂O₃ as dielectric. (a) Log(I_DS) and √I_DS versus V_GS, μₑ = 15 cm²/V·s, V_T = 6.6 V, V_subthreshold = 0.37 V/dec, and current on/off ratio = 10⁸. (b) I_DS versus V_DS for several values of V_GS.

TFTs with the same dimensions fabricated on thermal oxide have 50% lower saturation field-effect mobility, ~ 7.5 cm²/V·s, a threshold voltage of 14 V, subthreshold slope of 450 mV/dec, and a current on/off ratio of 10⁷ at V_DS = 25 V, as shown in Figure 3.11. The differences in performance between TFTs fabricated using pulsed-PECVD ZnO thin films deposited on SiO₂ and Al₂O₃ may be due to a relatively poorer interface with the thermal oxide. The active layers in these devices are very thin (~ 10 nm), and devices on SiO₂ and Al₂O₃ were also not passivated. Therefore, any charges on the channel back
interface can dramatically affect the band bending in the accumulation region, and further lead to hysteresis in the devices, although the value is small (~ 500 mV). It is also worth it to point out that non-saturation characteristics of these devices may be related with non-ideal contacts. Intrinsice ZnO was used in these devices as channel material, and there were no contact doping regions in TFTs. It is likely to form a Schottky barrier at the source/drain contact, and the barrier height would be influenced by the carrier accumulation from the gate. In this situation, it is unlikely to produce strong low voltage current saturation because most of the drain voltage will be dropped across the source barrier and the current will increase strongly with drain voltage [41]. The physics of contact effects in ZnO TFTs will be addressed in the chapter IV.

![Figure 3.11](image)

**Figure 3.11** – Pulsed PECVD ZnO TFT with 50 nm thermal oxide as dielectric. (a) Log(\( I_{DS} \)) and \( \sqrt{I_{DS}} \) versus \( V_{GS} \); \( \mu_e = 7.5 \) cm\(^2\)/V-s, \( V_T = 14 \) V, \( V_{subthreshold} = 0.45 \) V/dec, and current on/off ratio = \( 10^7 \). (b) \( I_{DS} \) versus \( V_{DS} \) for several values of \( V_{GS} \).

TFTs fabricated with pulsed PECVD ZnO thin films deposited using CO\(_2\) and N\(_2\)O were also compared. As shown in Figure 3.12 (a), TFTs using pulsed PECVD thin films from N\(_2\)O had larger field effect mobility and better subthreshold slope, possibly indicating higher quality ZnO thin films. On the other hand, deposition plasma power also impacts device performance. Increasing plasma power tends to cause a negative threshold
voltage shift and a stretched subthreshold slope, possibly due to defects generation in ZnO thin film such as oxygen vacancy and Zinc interstitial, which cause increased conductivity in ZnO. As Figure 3.12 (b) shows, TFTs fabricated with optimized pulsed PECVD ZnO thin films are significantly improved compared to TFTs fabricated with ZnO thin films deposited by conventional PECVD. Pulsed PECVD plasma deposition is a promising approach for depositing high quality ZnO thin films at low temperature, and may have potential for other metal oxide thin film synthesis.

3.4 Plasma-enhanced Atomic Layer Deposition (PEALD)

Plasma-enhanced atomic layer deposition (PEALD) provides many of the advantages of an atomic layer deposition (ALD) process, such as uniformity and conformity, but it has the additional ability to add substantial energy from the plasma, which may be important in defect control, low-temperature deposition, and doping. PEALD of ZnO as well as Al₂O₃, HfO₂, and ZrO₂ have been previously demonstrated using a metal-organic source and high-reactivity oxidants such as O₂ or H₂O [42, 43]. In these previous reports, the
use of a plasma significantly reduced the incorporation of -OH groups, which are related to conduction in ZnO and defects in Al₂O₃, ZrO₂, and HfO₂ [42].

3.4.1 Deposition Process

In contrast to conventional atomic layer deposition (ALD), PEALD is a novel process that uses a weak oxidant both to purge the metal organic precursor and to react with the precursor during the plasma step [44]. An explanation of the PEALD process follows. First, a metal organic precursor, typically diethylzinc (DEZ), is pulsed into the chamber, and soaked for some time as shown Figure 3.13 (a). The excess precursor is later fully purged by a weak oxidant, and a monolayer is formed on the sample surface, as shown in Figure 3.13 (b). Then the RF plasma is turned on as a pulse to oxidize the absorbed zinc precursor. Finally, the precursor gas phase reaction products are purged using the weak oxidant, as shown in Figure 3.13 (c). This constitutes one cycle, and undoped ZnO thin films are deposited layer-by-layer by repeating the cycles as Figure 3.13 (d) shows.

Figure 3.13 – Schematics of PEALD deposition process.
In this process, plasma not only provides an oxidant but also enhances surface reactions. PEALD also shares the same merits of ALD, and it is possible to control significant thin film deposition. In conventional ALD, where at least three kinds of gases (metal organic precursor, inert purge, and reactants) alternatively flow into the system, inert gas is required to fully purge the system after each gas flow, whereas in PEALD, a typical process cycle is shown in Figure 3.14 (a). Only one gas is switched during the whole process, and weak reactants can constantly flow into the system because there is no free reaction. Plasma is turned on more and often to drive the process. Compared with conventional ALD, the PEALD process greatly simplifies system complexity and lowers the total deposition time. On the other hand, plasma in the process can further lower the process temperature, which is critical for flexible thin film electronics.

![Figure 3.14](image)

Figure 3.14 – (a) Typical PEALD deposition cycle. (b) Schematics of PEALD deposition system. (c) Computer controlling interface for PEALD system (Labview®).

Due to the novelty of this process, there is no commercially available PEALD deposition system. The PEALD system used here is customer designed and set up. As shown in Figure 3.14 (b), it has a stainless steel chamber with a 4.5" diameter heated area (~200 °C) and a 4.5" aluminum RF electrode isolated using an adjustable polycarbonate spacer. The electrode spacing was ~1" for the films grown here. The RF (13.56 MHz) plasma was typically run at (~0.1 W/cm²). All the gas sources are temperature controlled as well for stable pressure. The whole system is fully automatic and based on computer control.
through a Labview™ interface. Typical PEALD cycle times in this system ranged from 4-20 s/cycle. An example cycle for ZnO deposition used was 1 s DEZ pulse, 2 s DEZ soak, 4 s purge with N₂O, 2 s plasma, 4 s purge with N₂O.

In addition to the system mentioned above, another system was set up for large area PEALD deposition. The system volume was much smaller and gas flow was close to laminar. It was also fully automatic computer control. Since most of the work here was done from the small system, the detailed information about large system design and operation process can refer to [45].

Although the above two systems are straightforward and easy to use, it is preferred to have a load lock system. Since the deposition is similar ALD process, it is critical to control the film growth and interface. For both small and large systems described above, moisture and particles can be easily trapped on the chamber walls when the systems are vented. These contaminations can deposited back into the film when plasma is turned on, and dramatically affect thin film properties, resulting poor device performance. Therefore, a PEALD load lock system is setup as Figure 3.15 shows.
The process chamber is based on Applied Materials P5000 showerhead PECVD system, and load lock chamber and transport arm are from other separate systems. An adapter was also designed to connect these two chambers. RF matching box was located directly on top of the showerhead to minimize RF reflection, and custom designed heater was used here to replace the original one in P5000 system. The process chamber is always maintained in high vacuum and temperature for better film quality control. It is worth pointing out that the gas flow in the load lock system is totally different with the above two systems. The gas is flowed from shower head and pumped out from the side. Unlike the laminar flow in large system, a relatively high pressure is formed on top of the sample holder, forcing all the gas flow outwards to the holder edge. For PEALD process the byproducts from plasma reaction and contaminations from chamber walls have no chance to access the sample due to higher pressure in the center. Therefore, it is believed that purge time in the process can be further minimized in this system design. Additionally, shower head is favored in PECVD system due to its uniform deposition control. Although the deposition in this work is ALD process, the thin film uniformity is also possible to be improved.

Figure 3.15 – (a) Computer controlling interface for PEALD system (Labview®). (b) Load lock PEALD thin film deposition system.
3.4.2 Typical Film Characteristics

The crystal structure of PEALD ZnO thin film was characterized by X-ray diffraction (XRD) as Figure 3.16 (a) shows. Though the film thickness is as small as 30 nm, PEALD ZnO exhibits strong (002) diffraction without any other direction peaks. This strong ordered material property results in polar symmetry along a hexagonal axis, and may contribute to piezoelectricity and pyroelectricity. An AFM picture in Figure 3.16 (a) also shows PEALD ZnO has very smooth surface, and RMS of surface roughness is around 1.5 nm. The detailed information about material can also be seen from the TEM picture in Figure 3.16 (b). ZnO has columnar grains with crystalline continuity from the Al₂O₃ interface to the top of ZnO, and the estimated grain size is about 10 ~ 20 nm, which can be also calculated from full width at half maximum (FWHM) in XRD results. A TEM picture also shows that the interface between Al₂O₃ and ZnO is smooth. As it is discussed in section 3.2, interface defects can dramatically affect device performance, and fewer interface traps are preferred. On the other hand, the back interface for ZnO is much rougher compared to the front dielectric interface, and easily traps charges, resulting in the instability of devices. Several passivation methods have been adopted,

Figure 3.16 – (a) XRD results for 30 nm PEALD ZnO thin film, and 1 μm AFM scan picture shown in the inset. (b) TEM picture of ZnO on Al₂O₃ dielectric and Si as substrate.
and corresponding modeling work will be addressed in chapter 4 [46, 47]. It is worth pointing out that deposited PEALD ZnO is quite resistive, and thus different from conducting ZnO deposited by traditional ALD. High resistivity is important for enhancement mode device (normally off), and more useful for display and other electronic applications.

### 3.4.3 PEALD ZnO TFTs

Bottom gate top contact thin films transistors were fabricated on glass substrates with 32 nm Al₂O₃ and 10 nm ZnO. For these simple test devices (shown in Figure 3.17), a blanket chrome gate layer rather than a patterned gate was used. Transistor characteristics for a passivated PEALD ZnO TFT with W = 200 µm, L = 20 µm were extracted from log (I_D) versus V_{GS} and √I_D versus V_{GS} curves as shown in Figure 3.17 (a). Typical TFT has a field effect mobility of 20 ~ 30 cm²/V·s, a threshold voltage of 4.5 V, a sub-threshold slope of ~ 200 mV/dec, and a current on/off ratio of ~10⁹. As deposited, the PEALD ZnO films are highly resistive and form enhancement mode TFTs, but the passivation process slightly shifts the threshold voltage of the devices (~ -2 V), and slightly increases the subthreshold slope (to 150 mV/dec – 200 mV/dec). However, the device hysteresis is reduced from ~500 mV to <40 mV after passivation, and the device stability is significantly improved [44].
N$_2$O was chosen as oxidants in ZnO deposition due to the higher device performance. The N$_2$O based devices showed mobility of 20 ~ 30 cm$^2$/V·s while the CO$_2$ devices were typically 7-15 cm$^2$/V·s. The cause of this factor of two is still not entirely clear, but may be related to a more highly ordered columnar structure observed in N$_2$O films compared to CO$_2$ (determined by cross sectional TEM). However, this somewhat oversimplifies the difference and other devices properties, which may be expected to change with a large reduction in mobility, such as the subthreshold slope, are nearly identical for both devices. Another possible reason is the carbon incorporation. Since the process temperature is as low as 200 °C, ZnO deposited from CO$_2$ may have more carbon than the films from N$_2$O, and carbon is widely considered as defect centers, which dramatically affect electron transport in the films.

Additionally, CO$_2$ was chosen in Al$_2$O$_3$ deposition due to similar consideration. It was found that devices fabricated using N$_2$O to form Al$_2$O$_3$ and N$_2$O to form the ZnO...
exhibited extremely low mobility and tremendous hysteresis related to incredibly poor stability. The reason for this is also not entirely clear but can be assumed to be related to a large interface state density at the dielectric semiconductor interface or enhanced charge injection into the Al₂O₃ layer. The difference in Al₂O₃ is not surprising as the addition of N₂ gas to O₂ in PEALD of Al₂O₃ has been shown to yield a considerably higher breakdown fields than with O₂ alone. As a result of the better performance, CO₂ based Al₂O₃ is used as the dielectric throughout this work.
Chapter 4

Flexible ZnO Thin Film Transistor and Circuits

4.1 Background

Electronic devices fabricated on flexible plastic substrates have been the object of dynamically expanding studies over the past several years [48]. The reasons for this are, first, the possibility of fabricating radically new devices (flexible displays or solar cells integrated into clothes, hemisphere “eyes” type) based on this technology and expanding the market for electronics [49]. Second, a substantial reduction of the production cost for the flexible devices in comparison with the integrated-circuit production on rigid silicon or glass wafer, and this can be attained by using the “roll-to-roll” technology, in which case the devices are formed on a roll of a moving plastic tape similar to newspaper printing.

There are several potential flexible substrates that could be used for thin film devices including stainless steel foil, polymeric films, woven fabric, and ultra-thin glass. Besides being flexible, the ideal substrate should be lightweight, rugged, electrically insulating, transparent to the visible spectrum, impermeable to moisture, chemically and thermally stable, and have a smooth surface. Though there is no single ideal flexible substrate that has all the advantages, a lower process temperature can provide more choices. In general the maximum operation temperatures of the majority of flexible plastics are low, and the glass transition temperatures for them are in the range from 80 to 250 °C. This will preclude the many technologies that are traditionally used in the fabrication of devices.
based on silicon, including thermal oxidation, diffusion, or epitaxy. Correspondingly, the choice of semiconductor materials for the flexible devices is also limited.

The use of flexible substrates also raises concerns about the integrity of thin films during both the fabrication process and under the stress of flexing. To be useful, it is important that thin films have good adhesion to the substrate on which they are deposited. Both van der Waal forces (physiosorption) and chemical interactions (chemisorption) contribute to adhesion. In addition, adhesion also depends on substrate morphology, nucleation processes, and interdiffusion at the film-substrate interface. It is also important to note that virtually all thin films have internal stress (tensile or compressive) that develops during growth, which can lead to film failure even without external stress if there is poor adhesion. Stress can develop during thermal cycles, especially if there is a large mismatch in thermal expansion coefficients between the films and substrate.

Most of the difficulty arises in trying to deposit a high quality semiconductor and gate dielectric at low temperatures. In fact, as discussed in the previous chapter, PEALD can be an ideal process candidate to solve these problems. Its thin film deposition is not only uniform but also conformal, and thus suitable for use as a flexible substrate. As part of this study, significant effort was put into improving both the material and fabrication processes.

So far, many results of flexible devices and circuits have been reported. Organic TFT ring oscillators fabricated on a polyester substrate have achieved a propagation delay of
680 ns/stage [50]. Source-drain implant self-aligned CMOS ring oscillators on a polyimide substrate using sequential laterally solidified (SLS) silicon had a propagation delay near 1 nS/stage [51]. There have also been several reports of oxide TFTs and circuits on flexible substrates using either stainless steel foils or plastic substrates [52-55]. Recently, Hsieh, et al, reported five-stage ring oscillators using amorphous indium-gallium-zinc-oxide (IGZO) TFTs on a polyimide substrate with a propagation delay of 350 ns/stage at a supply voltage of 20 V [56].

4.2 Substrate Selection and Fabrication Process

The flexible polyimide substrates used here had a high glass transition temperature (T_g ~354 °C) and relatively small coefficient of thermal expansion (CTE ~16 ppm/°C). The substrate’s surface was characterized by an atomic force microscope (AFM), and the RMS surface roughness was found to be ~30 nm for 10 μm scan (shown in Figure 4.1.) There are many surface features such as white dots on the AFM picture, representing significant local defects or damages in the substrate. In general, a planarization layer and a thick dielectric (≥ 300 nm) are required to make the surface smooth enough for

Figure 4.1 – Optical (left) and AFM (right) image of a 125 μm thick polyimide substrate.
First, the 125 µm thick polyimide substrates were prebaked at 200 °C in a vacuum oven for 24 hours, and then laminated onto glass carriers with a silicone gel for ease of handling during device fabrication. Next, a 100 nm thick chromium gate layer was deposited by ion-beam sputtering directly onto the polyimide substrate and patterned by wet etching. After gate patterning, PEALD was used to deposit a 50 nm thick Al₂O₃ film from trimethylaluminum (TMA) and CO₂, and a 30 nm ZnO film from diethylzinc and N₂O, both at 200 °C. After the PEALD step the ZnO was patterned by wet etching in diluted HCl, and the Al₂O₃ was patterned by wet etching in hot (80 °C) phosphoric acid. Next, titanium source and drain electrodes were deposited by sputtering and patterned by lift-off. Finally, devices were passivated using 30 nm of Al₂O₃ deposited by ALD from TMA and water at 200 °C, and the passivation layer was patterned by wet etching. After processing, the flexible substrate is easily delaminated from the glass substrate. Figure 5.3 shows a single device structure (bottom gate and top contact) and a completed polyimide substrate with ZnO TFTs and circuits after removal from the carrier substrate.
4.3 The Integrity of PEALD Dielectric Materials

For multilayer devices on polymeric substrates, it is necessary to have a conformal, uniform, and low defect density dielectric that is able to cover the often rough surface of the flexible substrate. The dielectric thickness in the device is only 50 nm, slightly higher than the substrate surface roughness. It might be questionable for dielectric material integrity and device yield, especially in traditional thin film deposition processes such as PECVD and sputtering, but the following experimental results demonstrate the uniqueness of PEALD in controlling the quality of significantly thin film.

An array of test structures, each containing 8000 crossovers with top and bottom metal layers separated by 50 nm of PEALD Al₂O₃, were fabricated on the polyimide substrate material to test the dielectric effectiveness (Figure 4.3 (a)). The leakage current for the test structure was typically less than 10⁻⁷ A/cm² at an electric field of 6 MV/cm as shown in Figure 4.3 (b), accounting for dielectric tunneling current. Using 10⁻⁷ A/cm² as a test criteria, an array of 28 of the 8000 crossovers test structures had a yield of >80% when tested at 3 MV/cm. Most of the test structures with test currents >10⁻⁷ A/cm² had
identifiable defects such as scratches or large particles. None of the processing for this test was done in a clean room, and the surprisingly good yield for a thin dielectric layer (50 nm) demonstrates that the PEALD Al₂O₃ is conformal and has low defect density.

Comparing to the common dielectric SiNx thickness (≥ 300 nm) of a-Si TFTs used in display technology, PEALD deposited Al₂O₃ (50 nm) is much thinner and still maintains the same integrity, even on the rough flexible substrates. On the other hand, Al₂O₃ has a dielectric constant similar to SiNx. The thinner dielectric thickness results in higher gate capacitance, and can further lower gate/drain voltage in the circuit application with no performance penalty. The current drive voltage for display is around 20 ~ 30 V. With the advantages of PEALD deposited dielectric materials, the power consumption can be expected to dramatically decrease and become more attractive for the mobile market.

4.4 Flexible TFTs and Stability

Bottom gate devices with top contacts were fabricated by the process previously described. Figure 4.4 shows typical characteristics for a passivated polyimide substrate ZnO TFT with a channel width and length of 50 μm and 10 μm, respectively. A linear
region field effect mobility of 20 cm$^2$/V·s, threshold voltage of 2 V, sub-threshold slope of 350 mV/decade, and current on/off ratio $>10^8$ were extracted from log(I_D) versus $V_{GS}$ in the linear region. Passivated devices also have a small hysteresis of ~200 mV. These results are similar to those obtained on glass substrates, but with about 30% lower mobility and somewhat higher subthreshold slope due to the rough surface of the substrates.

![Graph](image)

**Figure 4.4** – (a) ZnO TFT with 30 nm ALD Al$_2$O$_3$ passivation log(I_D) versus $V_{GS}$ and differential mobility versus $V_{GS}$ characteristics for $V_{DS} = 0.5$ V ($W/L = 50 \mu$m/20 $\mu$m, $t_{ox} = 50$ nm). (b) ZnO TFT I_D versus $V_{DS}$ characteristics for several values of $V_{GS}$ ($W/L = 50 \mu$m/20 $\mu$m, $t_{ox} = 50$ nm).

Flexible substrate ZnO TFTs statistics were measured on 1.5” sample as Figure 4.5 shows. The yield for 108 TFTs was 99% (only one bad device) with an average mobility of 20.4 cm$^2$/V·s and mobility standard deviation of 1.9 cm$^2$/V·s, and average turn-on voltage of -2.9 V with standard deviation of 1.5 V. Due to the non-square law characteristics of the ZnO TFTs, the gate voltage for a $10^{-9}$ A drain current was used as the turn-on voltage for simple extraction in device uniformity measurements. These statistics also match the dielectric crossover experimental results. Most of the non-working devices came from the defects or damages in the dielectric. The conformal
deposition of PEALD provides excellent support for semiconductor material growth and device performance.

In addition to electrical characteristics, device stability is also an important parameter in real application. For example, current a-Si suffers from threshold voltage instability, and additional compensation circuits have to be used in electronic applications to maintain the current level of each device [57]. As a result, the instability not only increases the complexity of the whole electronics, but also further limits the technology application range. Initial bias stress measurements were performed on the passivated PEALD ZnO TFTs on flexible substrates at room temperature, and the device was biased with 3 V on both drain and gate electrodes, as Figure 4.6 shows. The drain current density is about 1mA/mm, high enough to drive single typical OLED pixel. After 40000 seconds operation the device current was nearly unchanged, and there was only small threshold

Figure 4.5 – Statistics of 108 ZnO TFTs on flexible substrate.
voltage shift, less than 50 mV. Passivated ZnO flexible TFTs show excellent stability at the room temperature.

![Graph showing voltage shift](image)

**Figure 4.6** – Bias stress measurement for passivated PEALD ZnO TFTs.

### 4.5 Bending Stress

For flexible electronics, material and device durability are extremely important for real application. SONY has developed a flexible AMOLED display with a bending radius of less than 4mm, and the display was driven by organic TFTs [58]. However, inorganic materials, such as SiNₓ, Al₂O₃, and ZnO, are brittle and easily damaged. One possible solution is to pattern all the layers, forming islands of TFTs on the substrate to release internal stress during the bending. To investigate the bending effects on ZnO TFTs on a flexible substrate, devices were measured with a 1.5 inch bending radius after the passivation layer was patterned. The measurements were taken on devices in the following five different steps: flat, compressed, flat, tensile, and flat. As shown in Figure 4.7 (a), the transfer characteristics of these flexible TFTs were nearly unchanged after each measurement step, suggesting no change in field effect mobility as well. Device threshold voltage shifts were extracted and plotted in Figure 4.7 (b), and a relatively small negative shift of 0.5 V was observed after bending for several times. The reason
for the threshold voltage shift can be explained by piezoelectric charges in the ZnO materials. Since ZnO thin film deposited by PEALD has polycrystalline structure with (002) orientation, it is expected that piezoelectric and pyroelectric charges should exist in this situation. The initial experimental results (in Figure 4.7) have shown this piezoelectric effect is small and may be further reduced by proper device design. On the other hand, as Figure 4.7 (b) also shows, the bending results did not repeat well. Device threshold voltage should completely shift back to the starting point because of zero piezoelectric charges, instead of maintaining a negative shift. There appeared to be some residual stress memory in the substrate, and the mechanism behind that needs to be further explored.

Figure 4.7 – Bending stress measurement in PEALD ZnO TFTs.

4.6 Flexible Circuits

A PEALD ZnO TFT inverter with a conventional saturated load was also fabricated on a flexible polymeric substrate (shown in Figure 4.8). The inverter has a beta ratio of 5 with $L_{\text{drive}} = 5 \, \mu\text{m}$, $W_{\text{drive}} = 25 \, \mu\text{m}$, $L_{\text{load}} = 5 \, \mu\text{m}$ and $W_{\text{load}} = 5 \, \mu\text{m}$. With a supply voltage of 9 V, the voltage gain is $\sim 1.5$. Ideally, the gain should be the square root of beta ratio (width ratio, same channel length), around 2.7, since the drive and load TFTs must have
the same current during the operation. However, this theory is based on the constant mobility model, in which devices have the same mobility under different bias conditions. As shown in previous sections, the field effect mobility of ZnO TFTs typically increases when the gate field is increased. Therefore, device width ratio is not the only parameter which can affect the gain anymore. This difference is a critical problem, and an accurate compact model is necessary for corresponding circuit design. 15-stage ZnO TFTs ring oscillators were also fabricated using passivated ZnO TFTs (shown in Figure 4.9.) The circuits had a beta ratio of 5 with drive transistor $L_{\text{drive}} = 1 \ \mu m$, $W_{\text{drive}} = 25 \ \mu m$, $W_{\text{load}} = 5 \ \mu m$, beta ratio = 5). Contacts had a source/gate and drain/gate overlap of 2.5 $\mu m$. Figure 4.9 (a) shows the oscillation frequency and propagation delay as a function of supply voltage. The circuit operates for $V_{\text{DD}}$ as small as 2 V and oscillates at slightly more than 2 MHz for a supply voltage of $V_{\text{DD}} = 18 \ V$, corresponding to a propagation delay of <20 nsec/stage. The peak-to-peak amplitude of oscillation is 2.7 V. To the best of our knowledge, these are the fastest oxide-semiconductor circuits on flexible substrates reported to date, and they are about 20 times faster than the best.
previous report [56]. Scaling channel length and mobility can result in faster circuit speed, but larger supply currents and thermal effects dominate maximum speed on glass and flexible substrates. The thermal runaway will be addressed in Chapter 5.

Figure 4.9 – (a) Oscillation frequency and propagation delay as a function of $V_{DD}$ for a 15-stage ring oscillator ($L_{\text{drive}} = 2$ μm, $W_{\text{drive}} = 100$ μm, $L_{\text{load}} = 2$ μm, $W_{\text{load}} = 20$ μm, beta ratio = 5, 2 μm source/gate and drain/gate overlap); minimum propagation delay is 58 ns/stage at supply voltage 18V. (b) Circuit diagram of 15-stage ring oscillator (left), and its microscope picture (right).

Parasitic capacitance is another dominant factor in propagation delay. As Figure 4.10 (a) shows, there are gate-to-source and gate-to-drain overlaps in the device structure, which is normally characterized as $C_{gs}$ and $C_{gd}$ in circuits. They can dramatically affect circuit speed, especially for $C_{gd}$, which becomes the Miller capacitance, as the inset picture of Figure 4.10 (b) shows. $C_{gd}$ is the capacitance between drain and gate in drive TFT, where the voltages keep changing during the whole operation, resulting in positive feedback in the circuit. One way to minimize this capacitance is by simply lowering the overlap distance. Figure 4.10 (b) shows compact modeling results for different overlap distances. Circuit speed can increase almost one order higher when the overlap distance is decreased from 5 μm to 0.5 μm. However, the situation for flexible devices becomes more complicated due to the dimensional instability of substrates. For instance, any high
temperature process can easily cause the substrate to expand or compress, resulting in more challenges later on in the device fabrication.

![Diagram of ZnO TFT structure with parasitic capacitance and propagation delay](image)

**Figure 4.10** – (a) Parasitic capacitance in a typical ZnO TFT structure. (b) Propagation delay of ring oscillators versus gate to source/drain overlap distance by compact modeling.

The designs for these circuits in Figure 4.9 used relaxed layout rules (larger alignment tolerance) for the gate-to-source and gate-to-drain overlaps to compensate for dimensional stability limitations of the polyimide substrates. This results in increased parasitic capacitance and increases propagation delay compared to circuits designed with tighter alignment tolerance. The circuit speed varies with parasitic capacitance and operation current. The operation current can be varied by adjusting the TFT dimensions. In Figure 4.9, ring oscillators using drive and load TFTs with 3.5 μm channel length and 2.5 or 3 μm gate-to-source and gate-to-drain overlaps had propagation delays for \( V_{DD} = 16 \) V of 45 and 53 nsec/stage, respectively (faster for smaller overlap and reduced parasitic capacitance). Ring oscillators using TFTs with 3 μm gate-to-source and gate-to-drain overlap and 1 or 3.5 μm channel length had propagation delays for \( V_{DD} = 16 \) V of 19 and 45 nsec/stage, respectively (faster for shorter TFT channel length and thus increased drive current).
Although the dimension instability problem of flexible substrates can be temporarily avoided by using relaxed design rules, the circuit speed is seriously limited by introducing large parasitic capacitance. Several kinds of new flexible substrates have been reported with improved dimension instability, including liquid crystal polymer [59]. However, they are still far worse when compared with rigid substrates such as glass and silicon. Therefore, a self-aligned process is a requirement, and should work on most flexible substrates.

One possible solution is a self-gate aligned process, which has been demonstrated with PEALD ZnO devices and circuits on a glass substrate [60]. In this approach, backside exposure was used to create self-aligned contacts with the gate as the lithography mask. The overlap distance can be easily and precisely controlled in the lithography step. This process is robust and takes advantage of the transparency of the dielectric and ZnO layers. Figure 4.11 shows the results of a self-gate-aligned process on a glass substrate. The overlap distance was controlled to 0.25 μm, and the propagation delay of ring oscillators has been successfully lowered to less than 10 ns/stage. However, the overlap distance cannot be further decreased, since it is already comparable to contact transfer length for these devices. Therefore, doped contacts become the key issue in further pushing device speed limitations.
Figure 4.11 – Self-aligned-gate circuits. (a) Microscope picture of overlap distance and channel length in load and drive TFTs. (b) Propagation delay versus supply voltage for 7-stage ring oscillators.
Chapter 5

ZnO Thin Film Transistor Modeling

5.1 Background

ZnO-based TFTs have potential as higher performance and improved stability replacements for a-Si TFTs, and they are also considered the primary device backplane technology in the next generation of display with OLEDs. High performance PEALD ZnO TFTs and circuits have been successfully demonstrated not only on glass but also on flexible substrates in previous chapters. However, further study on device physics is needed in order to understand non-ideal characteristics of ZnO devices, such as non-square law saturation characteristics and strong dependence of mobility on gate voltage, and device modelling is the fundamental tool for analysing these problems and explaining the physics behind them.

Additionally, there are only a few reports on ZnO device modeling [61-63], although the fundamental transport properties and electron structure in ZnO materials are well understood now [22]. Most of the modeling work focused on one particular aspect (like traps) instead of considering device problems as a whole [64-67]. In this chapter, both device and circuit model are presented, in addition to detailed explanations on several important non-ideal characteristics in ZnO TFTs. Compared to all the standard models developed for silicon technology, the general approaches in TFT physics are always the same: Poisson’s equation relates variations in electrostatic potential to local charge densities. The continuity and the transport equations (drift-diffusion model) describe the way that the electron and hole densities evolve as a result of the transport, generation, and
recombination processes. The main model tool used here is Synopsys TCAD, a two-dimensional drift-diffusion device simulator [68].

5.2 Passivation Modeling

5.2.1 Passivation of ZnO TFTs

In all oxide semiconductors, defect chemistry and hydrogen play a critical role in controlling the free carrier concentration, and therefore it is unsurprising that these materials can have strong interactions with changes in atmosphere [69, 70]. Any technology built on oxide semiconductors will require high-quality passivation. This passivation layer is required to improve device stability by minimizing the charge on the back surface as well as acting as a diffusion barrier.

The selection of potential inorganic passivation materials is broad, and dielectric materials such as SiO₂ and Si₃N₄ are obvious choices due to their wide applicability in various semiconductor applications. However, the deposition of these materials at low temperature typically requires the use of PECVD processes where the samples are exposed to both plasma bombardment as well as hydrogen from the silane precursor. Figure 5.1 shows the experimental results on two kinds of ZnO TFTs for different passivation methods. It is worth pointing out that similar passivation results were observed on other oxide devices as well, not just on spatial atomic layer deposited (SALD) and PEALD ZnO TFTs [29]. In Figure 5.1 (a) SALD ZnO TFTs were passivated by 50 nm standard PECVD SiNx at 250 °C (0.06 W/cm² from silane and NH₃), and large threshold voltage \( V_T \) of more than 40 V was observed. As a result the devices
could not be turned off before dielectric breakdown. On the same thin ZnO layers, a smaller shift resulted from SiO$_2$ passivation (0.04 W/cm$^2$ from silane and N$_2$O), although it was still greater than 7 V. It has previously been demonstrated that even very short (<1 min) argon plasma treatments can dramatically increase the free carrier concentration in ZnO and IGZO films (>10$^{20}$/cm$^3$), and have been used to form heavily doped regions for ohmic contacts [71-73]. Considering ion bombardment in the plasma during PECVD passivation process, it is no doubt that the whole ZnO channel becomes highly conductive and devices cannot be turned off. Similarly, hydrogen has been regarded as a shallow donor in ZnO and it has been shown that hydrogen plasma treatments can dramatically increase the free carrier concentration in various oxide thin films [73-75]. There were large amounts of hydrogen generated from the precursors for both SiO$_2$ and Si$_3$N$_4$ passivation. It is therefore unsurprising that hydrogen and plasma based passivation

**Figure 5.1** – (a) SALD ZnO devices (17 nm ZnO thickness) before passivation and after 50 nm of PECVD Si3N4. (b) PEALD ZnO devices (11.5 nm ZnO thickness) as fabricated and after ALD and PEALD passivation.
on oxide transistors with materials such as SiO\textsubscript{2} or Si\textsubscript{3}N\textsubscript{4} typically results in negative V\textsubscript{T} shifts indicative of significant increases in surface or bulk free carrier concentration.

It makes sense that minimizing hydrogen introduction or avoiding plasma bombardment might dramatically change the passivation results shown in Figure 5.1 (a). In addition to SiO\textsubscript{2} and Si\textsubscript{3}N\textsubscript{4}, another passivation material choice is alumina, deposited by PEALD from TMA and CO\textsubscript{2}. Although a plasma based process still exists in this passivation, the introduced hydrogen by precursors is now dramatically decreased. After the devices were passivated with 30 nm of PEALD Al\textsubscript{2}O\textsubscript{3} (from trimethylaluminum (TMA) and CO\textsubscript{2}, plasma power 0.16 W/cm\textsuperscript{2}), negative V\textsubscript{T} shifts (>6 V) were still observed, as shown in Figure 5.1 (b). However, the shift was much smaller than the ones passivated by PECVD SiO\textsubscript{2} and Si\textsubscript{3}N\textsubscript{4}. The device hysteresis was also completely removed and the field-effect mobility was improved (~30 cm\textsuperscript{2}/V·s). Furthermore, standard chamber-based ALD (grown with TMA and H\textsubscript{2}O at 200 °C) passivation was also used (see Figure 5.1 (b)), which lacks both the plasma bombardment and hydrogen byproducts in the process. A significantly smaller negative V\textsubscript{T} shift (~2 V) was observed, while maintaining the improvement in device hysteresis and mobility. The current difference for PEALD and ALD passivation was from the V\textsubscript{T} shift, but the shape of the device transfer curve was nearly unchanged, suggesting no change in field effect mobility. In many potential applications, including AMOLED displays, enhancement mode devices are preferred. There have been many reports of unpassivated enhancement mode oxide TFTs, but very few reports of stable passivated enhancement mode oxide TFTs [34, 76]. Therefore, ALD passivation results are quite encouraging.
Despite the fact that a significantly smaller $V_T$ shift was obtained with ALD passivation, devices still exhibit some non-ideal characteristics, especially for the ones with a thick ZnO channel as shown in Figure 5.2. Devices before passivation were fairly similar. The thinnest channel layers show lower mobility and significant hysteresis (> 500 mV), and the thickest films had higher mobility and less hysteresis (< 300 mV), but also a small hump in the subthreshold regime. ZnO films greater than 15 nm had nearly identical field-effect mobility, and all devices had similar $V_T$. Figure 5.2 (b) shows the results after 30 nm of ALD Al$_2$O$_3$ passivation. The first notable characteristic is that all devices showed negligible hysteresis after the passivation. The threshold voltages after passivation for all ZnO thicknesses were also very similar. However, significant degradation of the subthreshold characteristics were observed in the thicker films (>20 nm).
nm). This change in subthreshold characteristics can be quantified by using not the device $V_T$, but rather the turn on voltage ($V_{ON}$) which is defined here as the $V_{GS}$ where $I_{DS} = 10^{-11}$ A. It is obvious that ZnO TFTs with thicker channels have more negative turn on voltage.

Apparently these non-ideal characteristics are only related to passivation, and there are three possible physical models that might explain these results. The first is back interface charges. As it is discussed earlier, an oxide semiconductor is sensitive to its defect chemistry on the back interface, which is exposed to the environment constantly before passivation. It is possible that some charges are generated or introduced on the back interface during the passivation. The second is the fixed charges in the passivation layer, which behave as a second gate on the back channel. It is expected that device characteristics can be dramatically changed under such double gate structures. The third possible model is the chemical doping introduced by passivation. Detailed studies on the effects of exposure of ZnO to TMA have shown that TMA preferentially etches Zn from the surface of the film, so stoichiometry defects are expected [77]. This would have the effect of appearing as a “doping” layer on the passivated device. However, it is critical to differentiate this doping from surface and bulk effects. Therefore, modeling work is necessary to find out which above model could more accurately represent the physics in these passivated devices.

In a TCAD Sentaurus device simulator, the semiconductor parameters are defaulted for silicon and there is no ZnO material in its database. It is also possible for ZnO deposited
by different methods to have different values. Here the material file was set up based on silicon and further modified according to the values listed in Table 5.1.

<table>
<thead>
<tr>
<th>Material parameters (ZnO)</th>
<th>Value (unit)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dielectric constant, $\varepsilon$</td>
<td>8.5</td>
</tr>
<tr>
<td>Electron affinity, $\chi$</td>
<td>4.29 (eV)</td>
</tr>
<tr>
<td>Bandgap, $E_g$ (300K)</td>
<td>3.437 (eV)</td>
</tr>
<tr>
<td>Electron density of states, $N_e$ (300K)</td>
<td>$3.66 \times 10^{18}$ (/cm$^3$)</td>
</tr>
<tr>
<td>Hole density of states, $N_v$ (300K)</td>
<td>$1.18 \times 10^{19}$ (/cm$^3$)</td>
</tr>
<tr>
<td>Maximum electron mobility, $\mu_0$</td>
<td>200 (cm$^2$/V·s)</td>
</tr>
</tbody>
</table>

Table 5.1 – ZnO material parameters for device modeling.

5.2.2 Back Interface Charges

In Chapter 2 the TEM picture of PEALD ZnO thin film showed that its back interface is much rougher than the front dielectric interface, although AFM showed relatively smooth surface termination. These back surface states can easily trap charges and change ZnO Fermi level position. It is also expected that a top gate device will have much lower field effect mobility due to charges scattering in the interface. In the model the same device structure (bottom gate and top contacts) was simulated with 50 nm thick Al$_2$O$_3$ dielectric and 30 nm thick Al$_2$O$_3$ passivation. All the devices were compared under the same 2 \( \mu \)m channel length. A series of ZnO channels with different thicknesses was simulated with different amounts of back interface charges. The assumption was also made here that devices have Ohmic contact and interface charges are fixed, which do not change with Fermi level position moving.

Figure 5.3 shows the simulation results for 5 nm thick ZnO with various amounts of back interface charges. The transfer curves in Figure 5.3 (a) exhibit similar characteristics, with passivation results shown in Figure 5.2 (b). Device operation can be clearly
described by plotting electron concentration versus channel location, as shown in Figure 5.3 (b). As the gate voltage increases, electrons gradually accumulate in the ZnO close to dielectric interface, forming the conductive channel. When the device is turned off with a gate voltage of -10 V, all the electrons in the ZnO are fully depleted. However, ZnO here is only 5 nm thick, and it is difficult to decouple the electrons between the channel and back interface. More information can be obtained from Figure 5.4, where simulation results for 50 nm thick ZnO are shown. Likewise, non-negligible humps in the subthreshold region were observed, indicating additional conductive paths exist in the channel. In Figure 5.4 (b) it is obvious that these fixed charges induced significant electron accumulation on the back interface, which was clearly separated from the channel region due to the thick ZnO. The electron concentration on the back interface was high compared to the one in the channel even if the device was biased far into accumulation region. On the other hand, this additional channel has to be fully depleted in order to turn the device off, leading to the humps in Figure 5.4 (a).

Figure 5.3 – 5 nm thick ZnO TFTs with different back interface charges. (a) Simulated transfer characteristics for different amount of back interface charges. (b) Electron density distribution in ZnO for different gate voltages (1-D cut perpendicular to ZnO/Al2O3 interface).
Although simulated devices show similar behavior such as humps in the subthreshold region, this model cannot fit well with experimental results, especially after $V_T$ and $V_{ON}$ versus ZnO thickness were plotted in Figure 5.5. Apparently devices have a negative $V_{ON}$ shift due to additional channels on the back interface, but $V_T$ also shifted negatively, which was actually not observed in the real devices.
2.3 Fixed Charges in Passivation

As a high-$k$ dielectric material, ALD Al$_2$O$_3$ is typically deposited at a high temperature (~900 °C), and post annealing is required [78-80]. Although PEALD can dramatically lower the process temperature and has comparable dielectric quality [44], ALD Al$_2$O$_3$ deposited at 200 °C was used as the passivation material to avoid plasma bombardment. As a result, it is possible that there are fixed charges in the low temperature Al$_2$O$_3$.

Figure 5.6 shows the model used to simulate these passivation charges. 50 nm thick ZnO and 50 nm thick Al$_2$O$_3$ were shown in Figure 5.6 (a), and fixed charges in the passivation layer were varied from $2 \times 10^{17}$ /cm$^3$ to $2 \times 10^{18}$ /cm$^3$. Compared with the back interface charges model, devices show much smaller humps and a relatively smaller negative shift of $V_{ON}$ as shown in Figure 5.6 (b). It is unsurprising since these fixed charges behave as a floating gate in the passivation layer. According to charge neutrality the energy band of
ZnO on the back interface was forced to change to accommodate these charges. In this situation, devices are biased not only by the bottom electrical gate but also by the top floating gate. As a result, besides $V_{ON}$ the $V_T$ has to be negatively shifted as well, and it is observed in Figure 5.6 (b) by fitting an $I_D-V_{GS}$ curve in the linear region.

![Figure 5.6](image-url)

**Figure 5.6** – Modeled Sentaurus data for passivated devices. (a) Device structure in the simulation. (b) Modeled transfer characteristics for 50 nm ZnO TFTs.

As discussed early in this chapter, passivation is a universal challenge and happens not only on PEALD TFTs but also on SALD TFTs. Considering the difference in Al$_2$O$_3$ deposition technology for these two kinds of devices, SALD TFTs were also simulated in this model, as shown in Figure 5.7. Although simulation shows a slightly higher $V_{ON}$ shift for different passivation thicknesses, there is still a good agreement between our experiment and the simulation. It is expected that this difference will be much smaller if the fixed charge concentration is lower than $10^{18}$ /cm$^3$. Another difference in the experimental data lies in the $V_{ON}$ dispersion for devices with different channel lengths, which was not observed in the simulation. This can be explained by contact effects. It is
likely that some contact barrier exists at the source/drain contacts, while Ohmic contact is assumed in the simulation.

\[ V_{on, pass} = V_{on} - \frac{Q_{charges}}{C_{ox}} - \frac{Q_{charges}}{C_{ZnO}} \]

\[ V_{on} = \text{SALD experimental results (left)} \]

\[ V_{on} = \text{modeled data (right)} \]

Figure 5.7 – The \( V_{on} \) comparison between SALD experimental results (left) and modeled data (right).

### 5.2.4 Back Channel Doping

It is known that TMA is a strong reactant and may replace Zinc on the surface. A simple experiment was conducted to testify this theory by using the following combination PEALD cycle: DEZ, TMA, and N\(_2\)O plasma. It was found that there was no ZnO deposition, just Al\(_2\)O\(_3\). Since the precursors used as the passivation material were TMA, it is quite possible for TMA to chemically dope ZnO, and the doping depth and concentration are important in determining device characteristics.

From the discussions of the previous two models, it is known that humps in the passivated device result from some charges in ZnO, which has to be fully depleted in order to turn the device off. The physics can be simply described by the following equation.
Since the dielectric constants for Al₂O₃ and ZnO are similar, as the ZnO thickness becomes comparable to, or larger than, the Al₂O₃ thickness, the ZnO depletion capacitance must be added in series with the oxide layer capacitance. Using this simple model, a linear relationship between the ZnO thickness and the $V_{ON}$ from the experimental data is expected, as shown in Figure 5.8 (a). From the experimental data, we can therefore estimate a back channel charge of $\sim 4 \times 10^{12} \text{ /cm}^2$ induced during the passivation processes. To simulate the chemical doping from the passivation process, the ZnO film in the model is assumed to have a background doping of $10^{17} \text{ /cm}^3$ with a constant mobility of $30 \text{ cm}^2/\text{V·s}$. In the case of no chemical doping, $V_T$ and $V_{ON}$ are weak functions of the ZnO thickness without the back channel doping (curves with open and solid squares in Figure 5.8 (b)), which are very similar to the as-deposited experimental data. In the case of back channel doping, a 2 nm-thick layer on the surface

![Graph](image_url)

**Figure 5.8** – (a) Experimental data from PEALD-deposited samples. (b) Modeled Sentaurus data for devices both as-deposited and after passivation. Devices were modeled with a background doping of $10^{17}$ in the ZnO films, and to simulate the effect of passivation, an additional 2 nm channel on the back surface (back channel doping) was doped to $2 \times 10^{19} \text{ /cm}^3$. The effect of bulk doping was also examined, and background doping was increased from $10^{17}$ (black) to $10^{18}$ (blue).
of the ZnO film is modified to have a doping concentration of $2 \times 10^{19}$ /cm$^3$. Figure 5.8 (b) also shows the result of the simulation before and after the back-doping was added. In comparison, with the back channel doping, $V_{ON}$ shows a strong dependence on the ZnO thickness while $V_T$ almost remains the same (curves with open and solid circles). This simulation result matches the experimental data for passivated samples very well. In the case of significant ZnO bulk-doping, both $V_T$ and $V_{ON}$ are strong functions of the ZnO thickness (curves with open and solid triangles), which does not match the experimental data. This trend with ZnO thickness is observed even if a large number of states are placed at the back surface to effectively pin the Fermi level. Thus the passivation results can be reasonably explained by the back channel doping model, in which the passivation layer induced electrical charges in these ZnO devices.

Despite the chemical doping on the back channel in the ALD Al$_2$O$_3$ passivation process, the use of relatively thin ZnO channels (~ 10 nm) can be a promising method of fabricating high-performance passivated oxide transistors with threshold voltages of ~0 V. What’s more, film thickness can be precisely controlled by a PEALD process, and threshold voltage variation from the materials deposition can be effectively avoided. Another promising method is surface treatment before passivation. It is reported that hydrogen peroxide treatments effectively prevent back surface from being doped, and devices have minimal hysteresis. Its physics mechanism is explained by an –OH surface concentration decrease or ZnO$_2$ wider bandgap material formation [81, 82].
5.3 Contacts in Thin Film Transistors

5.3.1 Review of Contacts to ZnO TFTs

Two kinds of contacts form at a metal-semiconductor interface: Schottky contact and Ohmic contact. Schottky contact behaves like a p-n junction diode with nonlinear conductivity, and has the advantages of low power and high speed. Therefore, it is typically used in high frequency and power rectifier diode. Ohmic contact can be treated as a small resistor, whose resistance is much smaller than the channel in thin film transistors.

It is well known that contact resistance, part of parasitic resistance, can substantially reduce the overall performance of many electronic devices, including TFTs. In the simplest model, contact resistance is added in series with the channel resistance. This contact resistance makes it difficult to access the intrinsic device performance. For example, in a common source TFT circuit the source resistance acts as a negative feedback element and parasitically degrades the available device transconductance. More generally, both the contact and channel resistance are a function of gate electric field (that is, the contact resistance does not have a fixed value); however, the channel resistance is proportional to the channel length, while the contact resistance is independent of channel length. Therefore, devices with very low channel resistances (high mobility or short channel length) require low absolute contact resistance to ensure minimal contact impact.
Figure 5.9  – (a) Typical transfer characteristics for PEALD ZnO TFTs. (b) Field effect mobility comparison for devices with Ohmic and Schottky contact.

Figure 5.9 shows the comparison for PEALD ZnO TFTs with different contacts. It is obvious that devices with Schottky contact show strong channel dependence for field effect mobility, because contact resistance is much higher than channel resistance. While for devices with Ohmic contact, the mobility remains the same and can actually reflect material property. Thus, it is critical to have Ohmic contact in high performance devices. Under the assumption that essentially all semiconductor-metal junctions have some barrier, there are limited approaches to form acceptable contacts. For conventional semiconductors, including single crystal and amorphous silicon, as well as GaAs, GaN, and SiC, Ohmic contacts are formed using heavily doped semiconductor regions at metal-semiconductor interfaces [83, 84]. Heavy doping reduces the Schottky barrier depletion layer thickness sufficiently so that carrier tunneling provides low-resistance ohmic contacts, even for significant contact barrier height.

Tremendous effects have been made in order to form good Ohmic contacts to ZnO related material, including heavily doped regions and surface treatment. Many reports point out that post annealing in N₂ at high temperatures (300 – 700 °C) can dramatically
lower the specific contact resistivity from $10^{-4}$ to $10^{-6} \, \Omega \cdot \text{cm}^2$ [85, 86]. The lowest value ($\sim 10^{-7}$) is achieved with Ti/Al/Pt/Au metals annealed at 200 °C [87]. Other reports on doped ZnO have shown the specific contact resistivity is about $10^{-5}$ with Al/Pt metals, but thermal stability is an issue [88].

### 5.3.2 Doped Contacts

To accurately describe contact effects of ZnO materials, several physical models were included in the simulations. A Schottky contact model with nonlocal tunneling was used for source and drain electrodes, and the Shockley-Read-Hall (SRH) recombination mechanism was introduced to model the exchange of carriers between contacts and the semiconductor channel. Since the carrier concentration in the doping region is high, Fermi-Dirac distribution statistics were also used for more accurate representation.

Figure 5.10 (a) shows the typical device structure with doped contacts used in simulation. Channel length is 4 μm and width is 200 μm. 50 nm ZnO is deposited on 22 nm Al₂O₃ with a source/gate and drain/gate overlap of 1 μm. It well describes the operation of a typical TFT, where electrons were injected into the channel from the source and later collected at the drain electrode. Figure 5.10 (b) compares the transfer curves for devices with and without doped contacts. The device without contact doping turned on very slow, and exhibited non-square characteristics. The extracted field effect mobility was almost 50% lower than the values in the material parameter file due to the Schottky contact effects. However, devices with doped contacts behaved ideally, just as the Ohmic contact theory predicted.
One way to form doped ZnO regions as contacts is by contact etching. The principle is described in Figure 5.11 (a). After double lithography was performed on the ZnO, forming the contact regions, a relatively high energy Ar ions beam was used to physically etch ZnO materials to some depth. This physical etching step created surface defects and generated a high concentration of electrons, forming the doped ZnO regions for later metallic contacts [72]. Figure 5.11 (b) compared the devices between as deposited and etched contacts. Apparently, contact etching increased the mobility from 8 cm$^2$/V·s to 15 cm$^2$/V·s with no change in threshold voltage, and also improved the square-law characteristics. It is also worth pointing out that doped regions generated by contact etching were thermally stable and reliable, different with other impurities doping methods.
In addition to contact etching, Al doped ZnO deposited by SALD was also used to form doped contacts. Due to the difficulty in selective etching between Al doped ZnO (AZO) and ZnO, top gate and bottom contact structure was used, as Figure 5.12 (a) shows. 100 nm SALD deposited AZO on a glass substrate was first patterned by lithography, and 30 nm PEALD ZnO and 5.5 nm PEALD Al₂O₃ were deposited in situ on top of AZO. Then wet etching was used to pattern dielectric and active layer, followed by 27 nm Al₂O₃ for complete edge coverage. Finally, 150 nm titanium was sputtered to form contacts. Figure 5.12 (a) also shows the microscope picture of a finished top gate TFT with doped contacts. To investigate the effects of AZO as a doped contact, the transfer length method (TLM) under different gate electrical field was used to extract contact resistance, as Figure 5.12 (b) shows. However, negative contact resistance was extracted when the gate bias was under 4 V and 6 V. Under this low gate field, total resistance was actually dominated by channel resistance, so it is difficult to accurately extract contact resistance, which might be very low for AZO doped contacts. As the gate field further increased the extraction accuracy improved, since channel resistance was much lower or even comparable to contact resistance. Therefore, contact resistance of 145 Ω was extracted at...
$V_{GS} = 8$ V, and specific contact resistivity is around $1.74 \times 10^{-5} \Omega \cdot \text{cm}^2$. This value is comparable to the reported literature [88], and good enough for practical applications.

**Figure 5.12** – (a) Device structure and microscope picture for top gate ZnO TFTs with doped contacts. (b) Gated TLM measurement results for several $V_{GS}$.

Figure 5.13 shows typical electrical characteristics of top gate TFTs with doped contacts. A linear differential mobility of $6 \text{ cm}^2/\text{V} \cdot \text{s}$ was extracted at $V_{GS}$ of $8$ V from the device transfer curve in Figure 5.13 (a). Compared with the bottom gate structure, the top gate device has much lower field effect mobility at the same $V_{GS}$-$V_T$, but almost no hysteresis.

In the bottom gate structure, the device channel is close to the front surface of the ZnO material, which has an extremely smooth interface, as the TEM picture showed in chapter 3. However, the device channel is switched to the back surface of the ZnO materials in the top gate structure, where significant surface features were observed. These back surface states behave as electron traps and scattering centers, resulting in low field effect mobility. On the other hand, the top gate structure has the unique advantage of passivation since ZnO was completely isolated from the external environment by a substrate at the bottom and by an Al$_2$O$_3$ dielectric on top. Therefore, a hysteresis free
device could be expected in this structure. Despite the low mobility, top gate TFTs with doped contacts still show good output characteristics, as shown in Figure 5.13 (b).

![Graph](image)

**Figure 5.13** – Electrical characteristics of top gate ZnO TFTs with doped contact. (a) Transfer characteristics in linear region and extracted mobility. (b) $I_{DS}$ versus $V_{DS}$ for several values of $V_{GS}$.

Simple circuits including inverters and ring oscillators were also fabricated on glass substrates with top gate devices with doped contacts. Figure 5.14 (a) shows the results of an inverter with a beta ratio of 5 and a 3 μm channel length. The gain was still limited by the gate field dependent mobility, as discussed in Chapter 4. With the same channel length and saturated load design, 7-stage ring oscillators were successfully operated under supply voltages ranging from 10 V to 17 V, as Figure 5.14 (b) shows. The overlap distance of source-to-gate and drain-to-gate was 2 μm, and the minimal propagation delay was ~ 60 ns/stage. Compared to the results with bottom gate devices, this speed is about three times slower, and low mobility is the main reason. Similar device structure has been reported on ALD ZnO but with even lower mobility and no circuit results [89].
83

5.3.3 Ohmic Contact and TFTs in Large Accumulation Region

While previous results have shown it is very easy to form doped ZnO with carrier concentrations \( >10^{19} \text{ /cm}^3 \), challenges with doping stability and integration have resulted in limited demonstrations [90, 91]. In addition, simple processes have been developed to improve undoped metal-ZnO contacts to the point where additional doped layers are not necessary for many applications. The primary approach employs a plasma treatment (oxygen, hydrogen, or argon) to dope or generate defects in the oxide semiconductor (and thus increase the free carrier concentration) beneath the source and drain regions of the device [92, 93]. Energetic ion bombardment during plasma treatment can induce nonstoichiometric sputtering due to the physical momentum transfer between ions in the plasma and atoms on the surface. This nonstoichiometric surface and bombardment induced damage can increase the surface carrier concentration and decrease contact resistivity [94, 95].

![Figure 5.14](image_url) - Circuit results for top gate ZnO TFTs with doped contact. (a) Output characteristics for inverter with beta ratio of 5. (b) Propagation delay versus \( V_{\text{DD}} \) for 7-stage ring oscillator with channel length of 3 \( \mu \text{m} \).
Short oxygen plasma was used here to treat source/drain regions immediately before metallization during device fabrication. To further investigate oxygen plasma effects on contacts, gated TLM was used, as Figure 5.15 (a) shows. It is worth pointing out that small drain voltage ($V_{DS}=0.1$ V) was used to avoid space-charge-limited current during the measurement. Channel resistance $R_{ch}$ and contact resistance $R_{SD}$ were obtained from the slope and intercept on the total resistance axis, respectively. Since there are no heavily doped n$^+$ ZnO regions at metal-semiconductor interfaces and moderate resistance exists on the contacts, contact resistance quickly decreased as gate voltage increased, as Figure 5.15 (b) shows. When the device was operated in the large accumulation region with a $V_{GS}$ of 12 V, the extracted contact resistance was 66 $\Omega$, much smaller than the channel resistance of 71 k$\Omega$. The extracted specific contact resistivity was $2.5 \times 10^{-5}$ $\Omega\cdot$cm$^2$, and contact impact was minimal in this situation. However, when the device was operated in the weak accumulation region, the contact resistance was comparable to the channel resistance and could not be treated as ohmic contact anymore. As a result, the accuracy of extracted field effect mobility, subthreshold slope, and threshold voltage can be dramatically affected.
Another important parameter in contacts is the transfer length $L_T$, a physical distance over which most of the current transfers between the semiconductor and contacts. In this case, the extracted transfer length from TLM was 0.2 $\mu$m and weakly dependent on gate voltage. More realistically, $L_T$ is also the limitation of overlap between gate and source/drain contacts. In high speed applications, self-align technology is commonly used to minimize this overlap distance, lowering the parasitic capacitance. However, device characteristics and circuit speed may suffer from current loss when the overlap distance is approaching $L_T$ [60]. Despite these limitations, plasma treatment of oxide contacts does provide one approach to significantly reduce the impact of barriers in oxide TFTs.

5.3.4 Gated-Schottky Diode

Despite the requirements and difficulty in making Ohmic contacts, TFTs are still widely used to probe novel material properties. However, device physics may become different
in this situation. In conventional MOSFET, channel potential is modulated by gate field to limit the current flow, as shown in Figure 5.16 (a), but for devices with Schottky contacts, the barriers could be high enough to constrict current as well. The gate electric field is not only modulating the channel conductance, but also will change the effective barrier width and magnitude of current in the end, as Figure 5.16 (b) and (c) show. Furthermore, it is nearly impossible for this type of device to pinch off at the saturation region, because most of the drain voltage will be dropped across the contact barriers instead of channels, and current keeps increasing as drain voltage increases. Therefore, device behaviors are more like “Schottky-gated diodes” or “Schottky Barrier FETs” (SBFETs), which are used in MOSFET to minimize short channel effects. However, extracted device parameters such as field effect mobility and threshold voltage from traditional MOSFET are not meaningful anymore due to the change in device operation principle.

![Figure 5.16](image-url)  
**Figure 5.16** – (a) Schematics of operation principle for typical MOSFET. (b) Schematics of operation principle for SBFET. (c) Barrier width decreases and tunneling current increases when gate field modulates the barriers on the contacts.

It is also interesting to note that many of the publications on high mobility ZnO TFTs make no mention of contact resistivity and show similar characteristics with SBFET devices. The following experimental and modeling results will demonstrate that
extremely high field-effect mobility could be easily extracted but is not likely connected to real transport in these materials.

Figure 5.17 shows the electrical characteristics of PEALD ZnO TFTs with N₂O based Al₂O₃ passivation. The device structure and process are almost the same as the ZnO TFTs discussed in the previous section except for the passivation layer. The device shown has exceptionally high mobility at a very low voltage, and a very different shape to the differential mobility curve than the observed ohmic contact TFTs. A sharp peak in differential mobility (> 70 cm²/V·s) is observed as the device turns on, and then the mobility slowly tapers off but still remains > 40 cm²/V·s even at large accumulation. In some cases, extremely high mobility (>200 cm²/V·s), even higher than single crystal ZnO material, was also observed. Figure 5.17 (b) shows the less ideal output characteristics as the devices do not fully saturate as expected; however, large current densities are observed.

![Figure 5.17](image)

**Figure 5.17** – Passivated ZnO TFT with PEALD Al₂O₃ from N₂O and TMA. (a) Device transfer characteristics, and mobility of > 100 cm²/V·s in linear region is extracted. (b) I_DS versus V_DS for several values of V_GS.
As a result, the impact of contact barriers has been modeled by including non-local tunneling in TCAD for this passivated staggered inverted structure. Figure 5.18 (a) shows a schematic of the model used to simulate these staggered inverted ZnO TFTs. In the model a thin channel region (10 nm) of the device was lightly doped ($5 \times 10^{14}$ cm$^{-3}$). Here the impact of doping at the back interface (from N$_2$O based Al$_2$O$_3$ passivation) was modeled using a 2.5 nm thick layer doped $10^{20}$ cm$^{-3}$ at the back interface, as discussed in the previous passivation model. The model used a 0.6 eV barrier at both the source and drain contacts. In addition, the critical material mobility parameter for the ZnO layer was defined to be constant (30 cm$^2$/V·s). Figure 5.18 (b) shows device transfer characteristics from the simulation. The first and most notable characteristic observed was a peak in differential mobility to 130 cm$^2$/V·s (more than 4x the defined constant material mobility). This overshoot in mobility continues well into strong accumulation, and at $V_G-V_T = 10$ V, the mobility was still 50 cm$^2$/V·s. The turn on and threshold voltage were also unexpectedly positive for the high level of back channel doping. To understand this, consider the voltage required to deplete the back channel charge with the series capacitance of the oxide and ZnO layer. For 50 nm Al$_2$O$_3$ with $\varepsilon_r = 8$, in series with 7.5 nm ZnO with $\varepsilon_r = 9.5$ and sheet charge of $2.5 \times 10^{13}$/cm$^2$, a relative shift of -32 V was expected. However, only -5 to -10 V of shift was observed. This difference can be attributed to the large contact barrier, which allows the device to be turned off at the contact without fully depleting the channel. Thus, poor contacts in oxide TFTs can lead to an incorrect extraction of device threshold voltage and field effect mobility. Figure 5.18 (c) shows that the output characteristics for the device are also non-ideal, with considerable curvature a low $V_{DS}$ and poor saturation at high $V_{DS}$. This demonstrates that
it is possible to extract non-meaningful mobility, threshold voltage and subthreshold slope values from devices with non-ohmic contacts.

The ZnO layer is 10 nm thick and lightly doped \(5 \times 10^{14} \text{ /cm}^3\) while the back interface is heavily doped \(10^{20} \text{ /cm}^3\) to simulate the passivation process. (b) \(\log(I_D)\) and differential mobility from the simulation for linear and saturation regime. The differential mobility is extracted for \(V_{DS} = 0.5\) V. (c) Linear \(I_D\) versus \(V_{DS}\) for several gate voltages showing considerable non-ideality.

It is worth pointing out that the key parameters in materials such as electron tunneling mass can also affect the mobility overshoot peak and width, as Figure 5.19 shows. Compared to the experimental data modeling, results show similar characteristics for extracted mobility in both linear and saturation regions. The linear region mobility was much higher than the saturation region mobility and also peaks early. In the meantime devices with shorter channel length have smaller extracted mobility in Figure 5.19 (a). Another view to explain these Schottky contact effects is that devices can be treated with extremely short channel length when biased in large accumulation region. The channel is so conductive that most the potential is dropped at the contacts. Therefore, depletion width at the contacts should be used to extract real mobility instead of physical channel length, and mobility overestimation can be qualitatively evaluated by the ratio of physical channel length to depletion width. Since the depletion width is only determined by the contact barrier in this case, long channel devices have much higher overestimation in
mobility, as shown in Figure 5.19 (a). On the other hand, tunneling mass of ZnO materials is also sensitive for the magnitude of mobility overestimation. Figure 5.19 (b) shows that a smaller tunneling mass leads to higher extracted mobility for devices with the same channel length.

In summary, contact non-idealities can alter or even dominate device measurements and can result in large errors in apparent mobility, threshold voltage, and subthreshold slope for typical parameter extraction approaches. It is important to note that this SBFFET also exists in many organic devices and careful attention should be made when exploring the new material properties.

5.4 Thermal Modeling

5.4.1 Output Conductance in Oxide TFTs

There are a variety of key transistor parameters which determine performance in practical digital and analog applications. Parameters such as field-effect mobility garner attention
in new materials, but often more important is the related parameter, transconductance, 
\( g_m = \frac{dI_{DS}}{dV_{GS}} \). An often overlooked parameter is the output conductance \( g_d = \frac{dI_{DS}}{dV_{DS}} \) in the saturation regime where \( V_{DS} > V_G - V_T \). Ideally, this output conductance should be effectively zero for long channel MOSFET. Both the transconductance and output conductance set limits for important applications such as amplifiers. For example, the intrinsic TFT low frequency voltage gain is the ratio of the transconductance to the output conductance \( A_{V0} = \frac{g_m}{g_d} \).

However, PEALD TFTs show significant output conductance in the saturation region, as Figure 5.20 (a) shows. This device behavior is similar with “gated diode” or SBFET, except that there is no mobility overshoot, but further TLM measurements showed Ohmic contacts for these devices. Another possibility is the short channel effect, especially drain induced barrier lowering (DIBL). In MOSFET, with the device continually scaling down, the lateral field in the device becomes comparable to the gate electrical field. The gate begins to lose control on channel potential modulation due to the two-dimensional effect. Figure 5.20 (b) shows the result of TCAD modeling results of ZnO thin film transistors (TFTs) with varying channel lengths. The channel lengths are normalized to one square by multiplying by \( L/W \). The modeled device has a 32 nm thick \( \text{Al}_2\text{O}_3 \) dielectric with a dielectric constant of 8. As shown, the device output conductance related to short channel effects is negligible until the device dimensions are significantly less than 1 micron. Therefore, the output conductance observed in long channel oxide TFTs (> 1 \( \mu \text{m} \) in Figure 5.20 (a)) is related to neither short channel effects nor Schottky contacts.
From another point of view, output conductance was extracted from devices with various channel lengths and plotted versus input power density, as shown in Figure 5.21 (a). A linear trend was clearly observed, suggesting the output conductance was actually originated from thermal effects or self-heating. It is worth pointing out that the ZnO thermal effect is quite different with conventional FETs, which has been investigated in detail. In conventional FETs, the thermal effect is found to greatly reduce the output conductance of transistor characteristics [96]. It can be explained that the device lattice temperature quickly increases under large drain bias, resulting in the increase of the carrier phonon scattering rate as well, which leads to the drop in the carrier mobility. Although self-heating effects have been reported in ZnO TFTs [97], the devices among those reports were not passivated and have poor stability under a moderate gate electrical field, which can also cause the negative output conductance and lead to an inaccurate conclusion. On the other hand, the positive output conductance was observed not only in PEALD ZnO TFTs but also in other reported oxide devices, as shown in Figure 5.21 (b).
Therefore, it is a universal challenge for oxide semiconductor devices. The physics behind this positive output conductance can be explained by donor states and pyroelectric charges. Reports have shown there are some donor states extremely close (~ 10 meV) to the conduction band in the oxide semiconductor, although the origin of these states is not yet understood well [98]. When the device is operated in saturation regions, a self-heating effect can thermally generate electrons from these states, and device current is increased, leading to the positive output conductance. In addition to that, PEALD ZnO has a polycrystalline structure, and piezoelectric and pyroelectric charges are expected. Temperature measurements have shown the pyroelectric charge coefficients range from 1.5 ~ 2.7 nC/cm²K. When the temperature is increased by self-heating, threshold voltage of devices shift negatively due to pyroelectric effects and more currents are therefore generated. Obviously, this step can lead to more power flowing into devices, forming positive feedback on self-heating effects [45].

![Graphs](image.png)

**Figure 5.21** – (a) PEALD device input power versus output conductance. (b) Oxide TFTs input power versus output conductance.
5.4.2 Self-heating for Flexible Electronics

Due to the low thermal conductivity of flexible plastic substrates, higher positive conductance in the saturation is expected due to the self-heating effect. Figure 5.22 (a) shows the typical output characteristics for a PEALD ZnO TFT fabricated on a flexible substrate. The solid blue lines of the DC $I_{DS}$ versus $V_{DS}$ curves fail to saturate for higher gate voltage. Using pulsed measurements, the effects of self-heating can be reduced; the black curves with open symbols show pulsed measurements. It is found that the Joule-heating effects in the devices can be largely neglected when gate pulse widths <100 $\mu$s with few percent duty cycle, and steady state occurs for pulse widths >1 ms shown in Figure 5.22 (b). Figure 5.22 (a) compares a DC sweep with a 10 $\mu$s width and 1.5% duty cycle pulsed measurement. Where the device power is low, the DC and pulsed measurements are identical. However, the device power increases linearly with $V_{DS}$ and $I_{DS}$, and at larger gate voltages in the saturation regime, there are significant differences between the pulsed and DC data.

![Figure 5.22](image_url) (a) Output characteristic comparison between DC sweep and pulse measurement for PEALD ZnO TFT. (b) Drain current versus pulse width.
Considering device parameter extraction, significant consequences of Joule heating can happen, depending on how these oxide thin film transistors are measured. In general most reported oxide semiconductor TFTs typically do not follow the standard “square-law” behavior expected for long channel MOSFETs [99]. One component of this appears to be gate field dependent carrier mobility, which can be explained by the grain boundary effects [100, 101]. However, as the majority of oxide transistors are reported in the saturation regime and with considerable drain current and voltage, the effects of Joule heating should also be considered as a cause of non-ideality. Figure 5.23 shows DC (solid curve) and gate pulsed (open symbols) transfer characteristics in both the linear ($V_{DS} = 0.5 \, \text{V}$) and saturation regime for a ZnO TFT on glass and flexible plastic substrates. In Figure 5.23 (a), for devices on the glass in the linear regime, the pulsed and DC sweeps both have nearly identical characteristics and extracted field-effect mobility ($18 \, \text{cm}^2/\text{V} \cdot \text{s}$). In saturation, while the two curves have a similar threshold voltage (~1.5 V), the extracted mobility of the DC sweep is 25.5 cm$^2$/V·s versus 16.5 cm$^2$/V·s for the pulsed measurement. Based on the change in transconductance between the pulsed and the DC sweep in Figure 5.23, this overestimation of field-effect mobility (>50%) will continue to grow as the drain voltage is further increased, and this non-ideality becomes worse. The shape of the device transfer curve can be roughly evaluated by the $m$ factor in the equation $I_{DS} = K \times (V_{GS} - V_T)^m$, and ideally $m$ should be 2. For devices on flexible substrates, in the saturation region $m$ is extracted to be 4.2 in the DC sweep, and 3.8 in the pulse measurement. As previously discussed, self-heating results increased current generation, further distorted device transfer characteristics, and resulted in mobility overestimation. Therefore, it is critical to include self-heating effects when mobility is
evaluated in the saturation region. On the other hand, device temperature is estimated to be >200 °C on the glass substrate by using temperature dependent experimental data, and details can be referred to [45].

Figure 5.23 – (a) DC sweep and pulse measurement for device on glass substrate. (b) DC sweep and pulse measurement for device on flexible substrate.

5.4.3 Thermodynamic and COMSOL Model

To accurately simulate self-heating effects in the devices, a thermodynamic model has to be included. The reason for this requirement is that high currents produce Joule heat in the device regions, which may raise the lattice temperature significantly. Since many models used in the simulation, including electron traps in the bandgap and the SRH generation-recombination models, are functions of the lattice temperature, solving the lattice temperature is necessary to improve the accuracy of the simulation under such conditions.

The thermodynamic model extends the drift-diffusion approach by assuming that carriers are in thermal equilibrium with semiconductor lattice, and is typically used in high power density long channel device simulation.
The device structure used here was the same as the one previously described except that a glass substrate was added, and channel length was 2 µm. To keep consistency with the experimental setup, devices were also swept in the saturation region ($V_{GS} = V_{DS} = 8$ V), and the power density was $10^{-3}$ W/µm. Figure 5.24 (a) shows the two-dimension simulation results for the ZnO TFT on a glass substrate. Even though the model here ignored the heat sink effects from all the contacts, the whole device was still heated up more than 700 ºC and the temperature near the drain region can reach close to 800 ºC. Compared to the estimated value of 200 ºC from the experimental data, the simulation obviously has a much higher temperature, mainly due to the following two assumptions. The thickness of the glass substrate was only 10 µm instead of 0.5 mm due to mesh penalty in the simulation, and heat dissipation in the substrate was underestimated. The current model is more like a SOI (silicon on insulator) structure, and self-heating is also a significant issue for SOI devices [102, 103]. Another assumption is that device width was not considered in the 2-D simulation, which was accurate for the drift-diffusion model since electrical characteristics were only considered. In reality the third dimension (device width) can dramatically change the heat dissipation. The three-dimensional model shown in Figure 5.22 should be used to solve this problem. However, a 3-D structure will increase simulation complexity exponentially, so 2-D is good tradeoff for a rough picture at this point.
Another approach to simulate self-heating is based on a heat transfer model, where ZnO TFT is simply treated as a heat source. Although it is impossible to get detailed temperature information inside the devices, heat spreading over the substrate can be well simulated in macro scale. An example of this modeling for a device on glass can be seen in Figure 5.25. The finite element modeling software used here is COMSOL Multiphysics [104]. Figure 5.25 (a) shows a 3-dimentional structure of the device on 0.5 mm glass substrate with the bottom boundary at 27 °C and all other boundaries thermally isolated. The modeled TFT channel area (W/L = 200/5 µm) is $10^{-5}$ cm$^2$. Two different input powers (40 mW and 10 mW) were evaluated on self-heating effects in Figure 5.25 (b). It is clear that the temperature peaks in the middle of the device channel and drops down fast on both sides due to heat sinking from the source/drain electrodes. Therefore, self-heating effects can be somewhat alleviated by changing the contacts with higher thermal conductivity metals. It is also worth pointing out here that the change in temperature for an input power of 10 mW (P2 in Figure 5.25 (b)) is within 10% of the experimental value, demonstrating that finite element modeling can accurately describe self-heating effects.

**Figure 5.24** – (a) Thermodynamic modeling for self-heating in ZnO TFT (2-D). (b) 3-Dimentional structure for more accurate modeling in self-heating.
The models have shown that the thermal effects are dependent on many device parameters including the thermal conductivity and thickness of the substrate, and device electrodes and dimensions. However, metal materials are typically chosen only for Ohmic contact consideration, and device dimensions are mainly designed to meet application requirements. How to manage self-heating of oxide semiconductors on low cost substrates without sacrificing the performance is quite a challenge.

One possible solution is using a substrate with high thermal conductivity. Unfortunately, most low cost substrates are plastic and have very low thermal conductivity. To obtain high thermal conductivity some coating layers have to be introduced and cannot destroy the substrate flexibility. To further investigate thermal effects, PEALD ZnO TFTs were fabricated on Cu-coated polyimide substrate. The polyimide is intentionally made extremely rough by the vendor to obtain good adhesion with the copper layer. After the
substrate was laminated onto the glass carrier, 500 nm PECVD SiNx was deposited at 200 °C as a buffer layer to electrically insulate it from the copper. Then 30 nm PEALD ZnO and 52 nm PEALD Al₂O₃ was deposited in-situ. The whole device structure is shown in Figure 5.26 (a). It is noticeable from the microscope picture of the finished device in Figure 5.26 (b) that Cu-coated polyimide has an incredibly rough surface. Amazingly, the devices were still operational because of the conformal deposition PEALD has brought. Figure 5.26 (c) shows device I_D versus V_DS characteristics for several values of V_GS, and highest current density of 35 mA/mm were achieved for oxide semiconductors on flexible substrates. Table 5.2 also summarizes the power to thermal breakdown for devices on different substrates. Although copper coating dramatically helps the heat dissipation, its maximum power density is still one order lower than the one on silicon substrate.
In summary, self-heating effects on low-cost, low-thermal conductivity substrates such as glass and plastic have important consequences such as significant output conductance and overestimation of field-effect mobility in the saturation regime. Although some thermal engineering methods have been proposed, their practical applications are still limited. Since most TFTs are used as switches, CMOS like circuits can effectively solve this thermal problem on low cost substrates [105].

### 5.5 Device Modeling

#### 5.5.1 Overview

Since the first ZnO TFT was reported in 2000, tremendous efforts have been made to improve device field-effect mobility. When comparing with the electron mobility of 200 cm$^2$/V·s in a single crystal structure, the relatively low field effect mobility (10 ~ 100 cm$^2$/V·s) is typically explained by grain boundary and interface states. Hossain et al successfully built a ZnO device model and explained the grain boundary effects on device characteristics [61, 62]. However, in reality it is hard to decouple interface states and grain boundary effects, and both of them are typically treated as trap states in the

<table>
<thead>
<tr>
<th>Substrate</th>
<th>Thermal conductivity (W/m·K)</th>
<th>Power to thermal breakdown (mW/mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Si/100 nm SiO$_2$</td>
<td>90</td>
<td>8500</td>
</tr>
<tr>
<td>GaAs</td>
<td>35</td>
<td>3000</td>
</tr>
<tr>
<td>5 µm Cu coated polyimide</td>
<td>-</td>
<td>1000</td>
</tr>
<tr>
<td>Glass</td>
<td>1.3</td>
<td>225</td>
</tr>
<tr>
<td>Polyimide</td>
<td>0.12</td>
<td>85</td>
</tr>
</tbody>
</table>

Table 5.2 – Device power to rapid thermal runaway breakdown on various substrates with different thermal conductivity.
material bandgap. Most of the reported modeling work is actually focused on extracting these states by fitting device characteristics [64, 65]. In these models Ohmic contact is always assumed, which is not always true as discussed previously. In addition to that, the theoretical approach of using physical parameters (not fitting parameters) to determine the bias dependencies of carrier density, channel mobility, and on-current has been rarely reported, although it is essential to the device model.

In this section two different approaches are discussed to extract trap states in ZnO TFTs, and a corresponding compact model is built for further circuit simulations.

5.5.2 Surface Potential Approach

Surface potential model has become the tendency in developing modern devices, because it does not rely on the smooth functions in joining different regions and it brings more accuracy. The analytical model has been successfully developed on a-Si:H TFT, which considers the effect of free carriers and localized trapped charges simultaneously [106]. A similar approach was also reported in amorphous IGZO TFT [67], but channel mobility was used instead of band mobility, which has no physical meaning in material transport. It is necessary to have an accurate and fast DC model for ZnO transistors.
Figure 5.27 – Diagram for surface potential modeling.

Figure 5.27 shows the algorithm of surface potential model used here. The device has the same inverted staggered (bottom gate and top contacts) structure as before, and Ohmic contact was assumed for the initial simulation. The total trap states in the bandgap can be described by adding two exponential distributions, tail states $g_t(E)$ and deep states $g_d(E)$. 

$$g(E) = g_d \cdot \exp \left( \frac{E - E_c}{kT_d} \right) + g_t \cdot \exp \left( \frac{E - E_c}{kT_t} \right)$$  \hspace{1cm} (1)
$T_d$ and $T_t$ are deep and tail states characteristic temperature, respectively. $E_c$ is the bottom of the ZnO conduction band. When the ZnO TFT is biased in accumulation region, Poisson’s equation is solved to obtain the potential along the $x$-direction from the dielectric interface to the back channel interface:

$$\frac{\partial^2 \phi}{\partial x^2} = -\frac{dE_f}{dx} = \frac{q}{\epsilon} \left[ n_{\text{loc}}(x) + n_{\text{free}}(x) \right]$$

(2)

Where $n_{\text{loc}}$ represents all the trapped charges and $n_{\text{free}}$ is the concentration of free electrons in the channel. Among them trapped charges have been investigated well and can be calculated from (1), and the free electron is simply determined by

$$n_{\text{free}} = N_c \exp \frac{q\phi - qV_{\text{ch}(y)} - E_F}{kT}$$

(3)

By using Gauss’s law and electrical field $E_f$ from integrating (2) surface potential $\phi$ and gate voltage $V_{GS}$ can be connected together through the following equation.

$$Q_t = qn_t = -\varepsilon E_f = -C_{ox}(V_{GS} - V_{FB} - \phi_s)$$

(4)

Clearly it is necessary to have the expression of the density of charges $Q_t$ in the channel before solving the relationship between $\phi$ and $V_{GS}$. In this situation the operation region of the ZnO TFT can be separated into two parts, below and above threshold regions. In the below threshold region, most of the carriers are assumed to be trapped in the deep states, and charges in the channel are determined by $Q_t = f(gd(E)) = f(\phi_s, V_{\text{ch}(y)})$. In the above threshold region, most of the carriers are trapped in the tail states, and correspondingly the charges in the channel are expressed by $Q_t = Q(gt(E)) = f(\phi_s, V_{\text{ch}(y)})$. Therefore equation (4) now becomes

$$f(\phi_s, V_{\text{ch}(y)}) = -C_{ox}(V_{GS} - V_{FB} - \phi_s)$$

(5)

Considering gradual channel approximation, the current density can be calculated from
\[ I_{ds}(y) = -\mu_n W Q_f \frac{dV_{ch}(y)}{d\phi} \frac{d\phi}{dy} \]  

(6)

Where \( dV_{ch}(y)/d\phi \) can be calculated from (5) by taking the derivative respective to \( dV_{ch}(y) \) on both sides, and total sheet concentration of free electrons \( Q_f \) is obtained by integrating (2) from dielectric surface \( \phi_s \) to 0. \( \mu_n \) is electron mobility in the conduction band, a defined constant in the material file. Then the current in (6) becomes

\[ I_{ds}(y)dy = -\mu_n W Q_f \left( \frac{2kT/q}{Q_f(y)} c_{ox} + 1 \right) d\phi \]  

(7)

As it is discussed earlier, the charges in the channel can be expressed as trapped charges in the tail states or in the deep states depending on how the ZnO TFT is operated. Finally, the total current in the device is achieved by integrating (7) on both sides along the channel from source \( \phi_s = \phi_{ss} \) to drain \( \phi_s = \phi_{ds} \), and the boundary condition can be solved from (4).

In addition to the drain current, several other issues need to be considered as well. Since device operation is divided into two separate regions, it is necessary to combine them together, as the last step in Figure 5.27 shows. In order to take the contact effects into account, source/drain contact resistance \( R_c(V_{GS}) \) have to be included. Their values can be experimentally calculated from TLM measurement, and \( V_{DS} \) also has to be corrected to the internal voltage \( V_{DS}' \), \( V_{DS}' = V_{DS} - I_{DS} \times R_c(V_{GS}) \). However, self-heating can dramatically affect device characteristics in the saturation regions, and it is difficult for the DC model derived above to fit well with the experimental data. One possible solution is the phenomenological introduction of modulation factor \( \lambda \) with drain current rewritten as \( I_{DS} = I_{DS}' \cdot (1 + \lambda V_{DS}) \). It is worth pointing out that the modulation factor here is only for curve fitting and does not represent any real physics.
As shown in Figure 5.28, the experimental data, including transfer and output curves, agree well with those calculated with surface potential approach. The material parameters were the same as before (μ_n = 30 cm^2/V·s), and additional values were initial Fermi level position E_F0 of 0.1 eV and flat band voltage V_FB of -2.2 V. The extracted traps states are g_d = 2.3×10^{20}/cm^3, g_t = 6.25×10^{20}/cm^3, T_d = 1050 K, and T_t = 545K.

The difference in the subthreshold region in Figure 5.28 (a) can be explained by contact effects. Since there are no doped contact regions in these devices, TFT is actually turned off by depleting the ZnO beneath the source/drain contacts instead of depleting the channel. It has been verified by the experiments with an intentionally doped contact region formed by a gated contact in [45], and the device subthreshold region was actually stretched as modeling shows in Figure 5.28 (a). Another limitation for the surface potential approach is the traps spacial distribution. In the model, traps were assumed to be uniformly distributed in the channel, while in reality this is not always true, especially

Figure 5.28 – (a) Device transfer characteristic for modeling and experimental. (b) Output characteristic for modeling and experimental.
for the ZnO beneath the contacts. To accurately address these problems, a two-
dimension based drift-diffusion model is necessary.

### 5.5.3 Drift-diffusion Approach

A TCAD Sentaurus device simulator was used here to model TFT characteristics
including PEALD ZnO and SALD ZnO, and trap states were extracted correspondingly.
In a TCAD model, traps can be treated with various forms such as exponential, Gaussian,
and discrete distribution. Similarly, acceptor-like traps are mainly considered here.

Figure 5.29 shows the TCAD simulation setup for SALD ZnO TFTs. Due to the
difference in deposition technology, the material parameter was slightly modified in
Figure 5.29 (a). The device has 30 nm thick ZnO and 50 nm thick Al₂O₃, and channel
length is 20 μm. Figure 5.29 (b) clearly shows that electrons were injected into the
channel from the source contact and collected by the drain, and the electron peak
concentration in the channel shows close to the interface due to the quantum effects. For
SALD ZnO TFTs, Ohmic contact was assumed in the simulation and trap states were
extracted in the linear region to avoid self-heating effects.

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Values</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dielectric constant, ε</td>
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</tr>
<tr>
<td>Electron affinity, X</td>
<td>4.29 (eV)</td>
</tr>
<tr>
<td>Band gap, E₉ (300K)</td>
<td>3.437 (eV)</td>
</tr>
<tr>
<td>Electron density of states, Nₑ (300K)</td>
<td>3.66x10¹⁸ (cm⁻³)</td>
</tr>
<tr>
<td>Hole density of states, Nₓ (300K)</td>
<td>1.18x10¹⁹ (cm⁻³)</td>
</tr>
<tr>
<td>Maximum electron mobility, μₑ</td>
<td>200 (cm³/V·s)</td>
</tr>
<tr>
<td>Temperature, T</td>
<td>300 K</td>
</tr>
</tbody>
</table>

**Figure 5.29** – (a) Material parameters of ZnO used in TCAD modeling for SALD ZnO TFTs. (b) Device structure in 2D drift-diffusion modeling.
Single exponential distribution of acceptor traps was used, as shown in Figure 5.30 (a), and this model can well reproduce the device transfer characteristics in Figure 5.30 (b), especially for the subthreshold region. The extracted concentration of traps states is $7 \times 10^{19}$ /cm$^3$ and width is 80 meV. However, the Fermi level of ZnO is only about 87 meV below the conduction band $E_c$. All the states below Fermi level have already been filled with electrons, which do not contribute to the device current. When the device is biased, more electrons are trapped as the Fermi level moves closer to $E_c$. This gradual trapping process leads to the slow turn-on as observed in experimental. It is also worth pointing out that the concentration of trap states in ZnO is at least one order lower than a-Si:H, suggesting possible higher mobility in oxide semiconductor materials.

![Figure 5.30 - SALD ZnO device modeling. (a) Single exponential trap distribution and Fermi level position in ZnO bandgap. (b) Transfer characteristic for modeling and experimental.](image)

To further investigate the influence of traps on the device, trap concentration and width were used as variables to simulate device transfer curves. It is observed in Figure 5.31 (a) that trap width $E_s$ has strong effects on subthreshold slope. With larger $E_s$, more traps are located near the Fermi level, resulting in slower turn-on and large subthreshold slope. However, these additional traps do not affect device’s current as much as trap
concentration does, as shown in Figure 5.31 (b). When the concentration is increased to $2 \times 10^{20} / \text{cm}^3$, the on current is extremely low and mobility begins to be comparable with a-Si:H. In conclusion traps with single exponential distribution can well model SALD ZnO TFTs.

![Figure 5.31](image1)  ![Figure 5.31](image2)

**Figure 5.31** – Influence of trap parameters on TFT characteristics. (a) The width of trap distribution. (b) The peak density states of traps.

Using the same approach, a TCAD model was also used to simulate PEALD ZnO TFTs. Based on the results from the surface potential approach, two similar exponential traps (tail states and deep states) were assumed in the model, and non-local tunneling was included to deal with Schottky barrier on the contacts. Figure 5.32 shows the simulation results for device transfer and output characteristics. The extracted contact barrier is 0.35 eV. The extracted trail states have a peak concentration of $7 \times 10^{20} / \text{cm}^3$ with a width of 30 meV, and deep states have a peak concentration of $1 \times 10^{19} / \text{cm}^3$ with a width of 90 meV. Compared to the surface potential approach, the extracted tail states were similar, but the TCAD model has much lower extracted deep states, leading to the deeper subthreshold region shown in Figure 5.32 (a). The difference comes from the back channel doping effects in experimental devices, which was not included in the TCAD.
As discussed in the passivation model, ALD Al$_2$O$_3$ can chemically dope the ZnO back interface, leading to a stretched subthreshold region. However, this does not affect the conclusion that a TCAD model can well represent PEALD ZnO TFTs, and extracted parameters can be used in a compact model for further circuit simulation.

![Graph](image)

**Figure 5.32** – TCAD modeling for PEALD devices. (a) Device transfer characteristic for modeling and experimental. (b) Output characteristic for modeling and experimental.

### 5.6 Circuit Modeling

Advances in thin film transistors have resulted in high demand for circuit modeling. Traditional research mainly targets the extraction of parameters from device DC I-V characteristics and then performs SPICE-like simulation with compact models. However, a seamless simulation flow from a single transistor to complex circuits is more attractive. This is particularly more important for oxide semiconductors, since material deposition, fabrication process, and other variables can result in different device properties.
5.6.1 Inverters

Based on the previously built model in TCAD, simple inverters with different beta ratios were directly simulated without any compact model. The results are shown in Figure 5.33 (a). Device width is 20 µm, with channel length 4 µm in the drive transistor. For direct comparison inverters with the same designs were fabricated on glass substrates. Figure 5.33 (b) shows the experimental results for an inverter with beta ratio of 10. Good agreement between experimental data and simulation results is observed and can help to predict that the noise margin for these inverters decreases as beta ratio increases.

An inverted connected to load capacitor of 20 fF was also simulated to evaluate its switching behavior, and the results are shown in Figure 5.34. The output curve shows distinct asymmetry, where rising time is much longer than falling time. It is also observed experimentally and can be explained by the depletion load impedance. Considering the situation where the input voltage is low, the capacitor is fully charged. When the input is switched to high, the drive transistor instantly becomes conductive and
charges on the capacitor are discharged quickly. However, when the input is switched back to low, capacitance has to be charged by $V_{DD}$ through the load transistor, which has much higher impedance. Thus the rising time becomes longer.

![Figure 5.34 – TCAD modeling of AC response for ZnO inverter with beta ratio of 5.](image)

**5.6.2 Ring Oscillators**

A ring oscillator is an important part in circuit design, and often used to evaluate transistor speed and uniformity. Three-stage ring oscillators with different beta ratios were simulated here, as shown in Figure 5.35 (a). In order to start oscillation, the supply voltage and one stage gate voltage were ramped to 15 V and 9 V in 10 ns, respectively. It is observed that the oscillators reach the steady state after 400 ns, and that a smaller beta ratio can provide faster oscillator speed. For direct comparison with the compact model in the SPICE-like approach, a ring oscillator with the same design was simulated by AIMSpice after parameter extraction from a single ZnO TFT. Figure 5.35 (b) shows AIMSpice results for a ring oscillator with a beta ratio of 20. Both approaches, which have the exact same circuit design, show similar propagation delays of 40 ns/stage with supply voltage of 15 V.
In conclusion, a TCAD ZnO model can well describe the operation physics from single transistor to simple circuits, and is verified by reasonable agreement with experimental data. It is suited to give some insight in design and optimization of ZnO circuit applications.

**Figure 5.35** – Modeling results for 3-stage ring oscillator with beta ratio of 20. (a) TCAD modeling. (b) AIMSSpice compact modeling.
Chapter 6

ZnO Thin Film Electronic Application

6.1 Low Frequency Noise for ZnO Thin Film

Although numerous reports have been published on ZnO transistors in the past decade, there have been few reports on the noise characteristics of oxide semiconductor TFTs [107, 108]. Low frequency noise has been used as an indication of device quality and reliability in Si technology [109]. 1/f noise is often related to an empirical noise power spectral density fitting parameter, the Hooge parameter. Typical crystalline silicon MOSFETs have Hooge parameters in the $10^{-4}$ and $10^{-5}$ range [110]. Field effect transistors fabricated from single-crystal ZnO nanowires have been reported to have a Hooge parameter of $5 \times 10^{-3}$ at room temperature [111]. Extremely high Hooge parameters (>10) were also reported for Al-doped ZnO films [112]. Recently, Cho, et al, reported a low frequency noise for amorphous indium-gallium-zinc-oxide (a-IGZO) TFTs. To achieve low noise in these a-IGZO TFTs, the devices were annealed in an oxygen ambient at 300 °C for one hour, and Hooge parameters of 1.4 and $6 \times 10^{-3}$ were obtained on ALD Al$_2$O$_3$ and PECVD SiN$_x$ gate dielectrics, respectively [108]. Therefore, it is necessary to understand the noise characteristics of PEALD ZnO TFTs.

PEALD ZnO TFTs were fabricated on glass substrates by the same process discussed previously. After fabrication, TFTs were wire bonded in 16-pin DIP packages. Low frequency noise was measured at room temperature with two different approaches, as Figure 6.1 (a) shows. Both of them used a low noise DC gate biasing source and a Stanford Research SRS570 low-noise preamplifier. The only difference was how to
Traditionally, an Agilent 35670A dynamic signal analyzer (DSA) was connected for automatic signal processing. However, this method was limited by the resolution of DSA, so wide frequency range had to be processed independently. An alternative approach was proposed here by using a dual channel filter and a digital process card. The dual channel filter provided band-pass function to remove the aliasing effect after the amplifier, and the digital process card can capture all the noise and process its frequency spectrum by fast Fourier transform (FFT) in a computer. In theory the resolution is only limited by the card in this approach, and the frequency spectrum can be processed as a whole. Figure 6.1 (b) compares these two approaches, and they are equivalent for the application used here. It is also worth pointing out that devices were mounted in a shielded box for noise testing, and device measurements were done in the linear region of operation to minimize self-heating.

![Diagram](image)

**Figure 6.1** – (a) Two different approaches for low frequency noise measurements. (b) The comparison of noise result for two different approaches.

Figure 6.2 (a) shows the noise power spectra, obtained from drain current fluctuations for a PEALD ZnO TFT measured with $V_{GS} = 3$ V and several values of drain voltage. For $1/f$ noise we expect [113]

$$S_f = \frac{A_t^2}{f^\beta}$$

(6.1)
where $S_I$ is the noise power spectra of the drain current, $A$ is the noise amplitude, $\beta$ is the frequency exponent, and increasing drain bias leads to larger current noise. Figure 6.2 also shows that these PEALD TFTs have $1/f$ noise behavior with $\beta$ close to 1. Figure 6.2 (b) shows the normalized noise power spectra for TFTs with channel lengths of 2 $\mu$m and 5 $\mu$m. The magnitude of the normalized noise is independent of drain bias and scales well with device volume.

![Noise power spectra](image)

**Figure 6.2** – (a) Noise power spectra of drain current for several drain biases at $V_{GS} = 4$ V. (b) Normalized noise spectra of drain current for TFTs with channel lengths of 2 $\mu$m and 5 $\mu$m at two drain biases of 0.5 V and 1.5 V.

To understand the physical mechanism of the $1/f$ noise, the normalized power spectrum of the drain current fluctuations in the linear operation region was measured as a function of gate bias (Figure 6.3 (a)). By extracting the noise power at 30 Hz and plotting normalized noise power versus drain current on a log-log scale (Figure 6.3 (b)), a straight line results. This dependence has been related to mobility fluctuations [113-116] and suggests that this is the dominant noise mechanism in these PEALD ZnO TFTs.
The low frequency $1/f$ noise behavior can be described by

$$A = \frac{\alpha_H}{N}$$  \hspace{1cm} (6.2)

where $\alpha_H$ is the Hooge parameter and $N$ is the total number of carriers in the channel [111, 114]. As a figure of merit, the Hooge parameter can be used to compare $1/f$ noise across different devices, material systems, and device geometries. For PEALD ZnO TFTs with a width of 200 $\mu$m and length of 2 $\mu$m on a 32 nm PEALD Al$_2$O$_3$ dielectric, a Hooge parameter of less than $10^{-4}$ is extracted, which is more than one order of magnitude lower than reported for IGZO TFTs [108]. Figure 6.4 shows that the extracted Hooge parameter is nearly independent of gate bias, indicating the noise mainly originates from the channel and not from the contacts.

**Figure 6.3** – (a) Normalized noise spectra of drain current for several gate biases at $V_{DS} = 0.1$ V. (b) Normalized noise spectra as a function of drain current. The dotted line shows a slope of -1.
The low Hooge parameter of these PEALD ZnO TFTs may be related to the quality of the semiconductor-dielectric interface. For the top gate IGZO TFTs of reference 101, Al₂O₃ and SiNx/Al₂O₃ dielectrics were deposited by ALD or plasma enhanced chemical vapor deposition (PEALD) followed by ALD, onto IGZO deposited by RF magnetron sputtering. The Al₂O₃ and ZnO layers used for the bottom gate TFTs in this work were deposited sequentially in a single pumpdown by PEALD. The relatively high mobility of the TFTs used for this work may indicate reduced interface related trapping and scattering, resulting in lower noise. Compared to TFTs using other semiconductors including organic materials ($\alpha_H > 1$) [115, 116], amorphous silicon ($\alpha_H \sim 10^{-3}$) [117], and polycrystalline silicon ($\alpha_H \sim 10^{-2}$) [118], PEALD ZnO TFTs may offer some advantages for low noise. In contrast to elemental semiconductors such as silicon, the electron transport in oxide semiconductors such as ZnO is not strongly affected by structural disorder. In covalent semiconductors like silicon, the chemical bonds are $p$ or $sp^3$ orbitals with strong directivity. In amorphous versions of these semiconductors, strained bonds and other defects lead to trap states, and the mobility of the amorphous

![Figure 6.4](image)

Figure 6.4 – Normalized noise power at 10 Hz and extracted Hooge parameter versus gate bias for devices with 32 nm PEALD Al₂O₃ dielectric.
semiconductors is much less than their crystalline counterparts. However, the cations in ZnO form states at the conduction band minimum from spherically extended s orbitals of the metals. This greatly reduces the role of disorder for conduction band transport because the orbital overlap with adjacent spherical orbitals is largely unaffected by the disorder. This has been observed in practice, and the conduction band transport mobility in amorphous oxide semiconductors is similar to that in polycrystalline and even single crystal materials [22]. ZnO deposited at 200 °C by PEALD is polycrystalline and the impact of grain boundaries is expected to be relatively small compared to, for example, polycrystalline silicon, resulting in low noise 1/f characteristics.

In conclusion, the low frequency noise characteristics of PEALD ZnO TFTs were investigated. The noise power spectra of bottom gate, top contact, passivated TFTs exhibited a 1/f frequency dependence. The noise spectra scaled with drain bias, channel length, and gate bias, suggesting that the noise is dominated by mobility fluctuation in the TFT channel. A Hooge parameter of less than $10^{-4}$ was extracted, more than one order of magnitude smaller than previously reported oxide semiconductor 1/f noise. To the best of our knowledge, PEALD ZnO TFTs have the lowest Hooge parameter reported for any thin film transistor.

### 6.2 Temperature Sensor and Image Array

Infrared imaging has been being developed for many years, primarily in military applications. The imaging system is originally based on quantum devices that typically need liquid nitrogen for cooling. With the advancement of technology more systems tend
to be used in civil applications such as road obstacle sensors in the car and people rescue for firefighters. However, the operation temperature becomes the main challenge. Recently the emergence of a new generation of sensors – the microbolometer technology – based on an infrared thermal detection mechanism which is particularly suited to operate at ambient temperature has opened the opportunity for achieving low cost infrared imaging systems for both military and commercial applications [119, 120].

Figure 6.5 (a) shows a typical image pixel in the microbolometers [121]. The membranes are made thin enough and become very sensitive to infrared incoming radiations heating. Current microbolometers use materials such as a-Si:H, or vanadium oxide (VOₓ) and rely on the negative temperature coefficient of resistance (TCR) of these materials on the membranes for thermal imaging. The sensitivity of these materials is dictated in part by the TCR of the material (typically 1 - 4%) [121, 122]. In addition to that, the voltage or charge signal developed by pyroelectric materials can also be used for thermal imaging, but pyroelectric imagers typically require a mechanical chopper because they do not measure absolute charge. Here another method based on pyroelectric field effect transistors (pyroFETs) without the use of a mechanical chopper was proposed. As shown in Figure 6.5 (b), field effect transistors are sensitive to charges developed in the semiconductor or dielectric. When a pyroFET is biased in the subthreshold region, any small temperature change can result in its threshold voltage shift, leading to dramatic change in the device current. If these changes in threshold voltage or current can be precisely measured, corresponding temperature change is then easily extracted. Similar technology has been successfully demonstrated by organic transistors, but poor stability
and high low frequency noise (~ 1) make it impossible for organic materials to be used in practical applications.

From the application point of view, large area infrared is another challenge for microbolometers. Although they have taken benefits from the latest silicon technology advances, complicated Germanium lenses are designed to increase the image range due to rigid substrate choice. Curved microbolometer arrays are one of the solutions, and have potential to greatly reduce the size, weight, and cost of uncooled microbolometers [123]. However, the fabrication of a structure like the one in Figure 6.5 (a) on flexible and deformable substrates is not easy to solve.

As discussed in Chapter 4, high performance PEALD devices and circuits have been successfully demonstrated on flexible substrates with excellent bias stress stability. Besides that the ZnO deposited from a PEALD process has polycrystalline structure with the native property of pyroelectric material. Therefore, it is necessary to explore the use of arrays of these ZnO pyroFETs as flexible, thin film temperature micro sensors.
Flexible temperature sensors have previously been reported based on platinum resistors with small dimensions < $100 \times 100 \mu\text{m}$ and with good temperature resolution of $\sim 2 ^\circ\text{C}$ [2]. The flexible temperature sensors described here have comparable size, but provide improved sensitivity and lower current operation, as well as simple integration with additional TFTs for sensor selection and isolation.

Figure 6.6 (a) shows the temperature dependence of flexible ZnO pyroFETs. The devices were measured from 20 to 70 $^\circ\text{C}$, and the extracted turn on voltage was plotted in Figure 6.6 (b). A linear and reversible shift is observed. Assuming that the threshold voltage shift arises from the pyroelectric charge, a pyroelectric charge coefficient of 1.5 nC/cm$^2$K can be extracted. Compared with the devices on rigid substrates such as glass, this value is about 50% lower due to the rough surface of the flexible substrate. The threshold voltage shift is also found to recover rapidly (seconds or less), which is distinctly different from other oxide semiconductor TFTs, where defect generation is believed to be responsible for threshold voltage shifts which require hours for recovery [1]. The field-effect mobility of PEALD ZnO TFTs is found to be only very weakly activated with an activation energy $< 10$ meV down to 77 K, which is more than an order of magnitude lower than for materials such as a-Si:H where the transport is dominated by tail states [2]. The low temperature activation is also evidence of a limited number of deep traps in PEALD ZnO TFTs.
According to the operation principle of pyroFETs, when measured in the subthreshold region at constant gate bias, a small change in threshold voltage results in a large change in conductance, and provides good temperature sensitivity. Figure 6.7 shows the thermal response of single pyroFETs. Devices were calibrated between 20 ~ 35 °C using a surface mounted thermocouple and a gate voltage of -3 V and constant drain current of 4 nA. Sensitivity depends on the bias conditions, and in the subthreshold a maximum of > 350 mV/°C is observed. This change is equivalent to an effective temperature coefficient of resistance of more than 10%. Using a more complex biasing approach, it is possible to adjust the sensor sensitivity and dynamic range to suit various applications. These results demonstrate that high performance ZnO pyroelectric TFTs can be used for temperature sensing on flexible substrates and may provide opportunities in novel non-planar and integrated temperature arrays.

Figure 6.6 – (a) log (I_{DS}) - V_{GS} for V_{DS} = 0.5 V as a function of temperature (W/L = 200 μm/5 μm). (b) Change in threshold voltage as a function of temperature for device (left) showing a pyroelectric charge coefficient of 1.5 nC/cm²K.
ZnO pyroFET temperature sensors were fabricated on 25 µm thick polyimide substrates using PEALD at 200 °C and a previously described TFT fabrication process [3]. Several designs of nine individual 100 × 5 µm ZnO pyroelectric TFTs were fabricated on 2 cm long and 500 µm wide flexible probes, and in some designs, line select TFTs were also integrated, as shown in Figure 6.8. The sensors were designed as pillars due to practical application consideration. They were so small that it is possible to be implanted into a rat’s brain. It is reported seizures in the rats can be predicted by the temperature change in the local brain, which is hoped to be measured by these sensor pillars. Devices on these polyimide substrates typically had field-effect mobility of 10 - 15 cm²/V·s and excellent stability.

**Figure 6.7** – (a) Drain voltage response ($I_{DS} = 4$ nA, $V_{GS} = -3$V) as a function of time as the temperature is changed. (b) Temperature sensor calibration curve. The sensitivity decreases as the shift in threshold voltage moves the device out of the subthreshold region.
Several methods can be used to evaluate ZnO pyroFET temperature sensors. By calculating the change in channel conductance with temperature at a constant gate voltage of -2.5 V in the subthreshold region, an equivalent TCR of 3-5% was extracted from ZnO pyroFETs as shown in Figure 6.9 (a), which is comparable with current microbolometers. Another approach is shown in Figure 6.9 (b). By connecting ZnO pyroFETs as diodes and driving with a supply voltage of 5V, temperature sensitivity of 7 mV/°C was extracted. It is worth pointing out that the limitation of sensitivity comes from the operation region of ZnO pyroFET. Since it is connected as a diode ($V_{GS} = 0$), the gate voltage cannot be flexibly changed to bias the device in the steep subthreshold region. This problem becomes even more complicated for temperature sensor imaging arrays, because the diode connection requires each device to be measured independently, which is time consuming and increases the possibility of failure.

**Figure 6.8** – Flexible temperature sensor for implantable measurements. (a) Sensor diagram with 9 spatially distributed pyroFETs at the end of the pillar. (b) Single pyroFET structure.
One approach to solving this problem is described in Figure 6.10. In addition to being used as pyroFETs, ZnO transistors were designed as current mirror circuits. The working principle of the thermal imaging array in Figure 6.10 (a) can be explained as follows. By independently selecting the rows of pyroFET sensors, the devices in the selected row were biased into the appropriate subthreshold region with proper designed gate voltage. Then external current or voltage was supplied through current mirror circuits, driving the pyroFETs in the selected rows. Since all the rows and columns in the array were connected in parallel, the voltage of each pyroFET in the selected row can be read as a whole. From another point of view this design is similar to active matrix design in LCD/OLED display, and the only difference is the signal direction (input or output). Figure 6.10 (b) shows the mask layout of a 32 × 32 thermal imaging array.
A compact model was extracted, as discussed in Chapter 5, to simulate the above circuit design for the thermal image array. By choosing a bias current of 10 nA and gate voltage of 3 V for row selection, the pyroFETs with a channel length of 5 μm and width of 50 μm were forced to work in the subthreshold region. The simulation results are shown in Figure 6.11 (a), and the temperature sensitivity of 20 mV/°C was extracted. Compared with the diode connection design, the sensitivity is increased almost three times. It is also necessary to consider the uniformity of pyroFETs in large scale applications. Especially when the flexible substrate is deformed, the threshold voltage of pyroFETs can shift due to piezoelectric charges, which have been demonstrated by bending measurement in Chapter 4. A differential pair in Figure 6.11 (b) was designed to avoid threshold voltage variations. Two different currents were supplied into two pyroFETs with the same dimensions, and two different output voltages ($V_1$ and $V_2$) were input into a post differential amplifier. The temperature signal was determined by multiplying $V_1 - V_2$ with the gain of the post amplifier. Therefore, any noise introduced from threshold voltage

Figure 6.10 – (a) Circuit diagram for thermal image array. (b) Corresponding mask layout (32 × 32).
can be removed by $V_1$-$V_2$ because of the same dimension design in these two pyroFETs. However, the sensitivity is decreased to around 10 mV/°C.

Figure 6.12 (a) shows the finished thermal imaging arrays on a flexible substrate. The 2 inch $\times$ 2 inch sample includes $32 \times 32$, $16 \times 16$, $8 \times 8$ arrays, electrical and process test devices. The measurement system was controlled by Labview, and Figure 6.12 (b) shows the interface of measurement. Before thermal imaging the circuits are controlled by computer to automatically scan the whole sensor array obtaining device uniformity information, which is displayed on the left of the computer screen. After imaging the voltages from the readout are converted into temperature according to the calibration data and displayed on the right. The control program is also designed into auto and manual two modes.
Figure 6.13 shows the operational diagram of the thermal imaging array. The sample is ACF bonded and signals are brought to the test board, which quickly (1 ~ 3 frames/s) reads up to 32 device data lines to provide an image of the array. The difficulty does not lie in the measurement but in the bonding. Mechanical and electrical noise from bonding can dramatically lower the sensitivity of arrays. The future work will be focused on robust bonding and sensitivity improvement.

Figure 6.12 – (a) Thermal image array sample (left), and microscope picture of ZnO pyroFETs (right). (b) Automatic measurement interface by Labview.

Figure 6.13 – Thermal image array measurement diagram.
6.3 Irradiation for ZnO and Neutron Detectors

Thin film transistors are of considerable interest in sensors and other large-area electronic applications, and have the potential of being integrated on arbitrary substrates. They also have the potential application in space and some other harsh environments filled with radiation. Radiation damages have been investigated on various electronic devices such as Si and SiC MOSFET, and it is well known that radiation induces leakage in the channel and positive charge accumulation in the oxide, leading to permanent device failure in the end. This damage can be dramatically alleviated by using enclosed geometry and guardrings in properly designed deep submicron gate length Si MOSFETs. Devices can have small threshold voltage shifts and leakage increase for doses of 100 kGy (10 Mrad) or even larger [1]. However, polysilicon and organic TFTs show significant performance degradation even with low dose radiation exposure (<1 kGy) due to back channel turn-on and intermolecular cross-linking, respectively. For amorphous silicon (a-Si:H) TFTs, this radiation damage is quite shallow, but the low mobility and instability are still main drawbacks for a-Si TFTs. Although radiation hardness of ZnO materials has been investigated, no studies were performed on ZnO devices. In this work the effects of gamma-ray radiation on ZnO TFTs and circuits were explored.

The ZnO TFTs used in this work have the same structure as before and were fabricated on both borosilicate glass and polyimide substrates. 100 nm thick Cr deposited by ion-beam sputtering and patterned by wet etching was used as the gate layer. Next, 54 nm thick Al₂O₃ from trimethylaluminum (TMA) and CO₂, and 10 nm undoped ZnO from diethylzinc and N₂O were deposited at 200 °C by PEALD. The ZnO and Al₂O₃ were
then patterned by wet etching in diluted HCl and hot phosphoric acid, respectively. Ti source and drain electrodes were then deposited by sputtering and patterned by lift-off. Finally, devices were passivated by 30 nm ALD Al₂O₃ from TMA and water at 200 °C. After fabrication, unbiased devices and circuits in the sample boxes were exposed to ⁶⁰Co gamma rays with doses from 10 kGy to 1 MGy, as shown in Figure 6.14 (a). Figure 6.14 (b) shows images of the samples and sample boxes after various exposure periods. Even after the shortest exposures (10 kGy), the samples and boxes both began to yellow, which is expected as color centers form [124].

![Diagram](image)

**Figure 6.14** – PEALD ZnO sample exposed with gamma-ray irradiation. (a) Diagram for irradiation. (b) Color centers formed in glass and plastic substrate samples after various doses of irradiation.

PEALD ZnO TFTs used for irradiation have typical electrical characteristics with the threshold voltage of ~ -1 V and the linear region field effect mobility of ~ 18 cm²/V·s on glass substrates. Figure 6.15 (a) shows the linear region log(I_D) versus V_G characteristics for devices with ⁶⁰Co gamma ray doses from 0 to 1 MGy, and Figure 6.15 (b) shows extracted threshold voltage and mobility changes. Irradiated devices have a negative threshold voltage of ~ 1 V for a 10 kGy dose, increasing to ~1.5 V for 50 kGy, and increasing more slowly for larger doses. The saturation of threshold voltage shift with larger doses likely indicates self-annealing at the irradiation temperature (35 ~ 40 °C).
In Figure 6.15 irradiated device mobility is nearly unchanged, but subthreshold slope increases somewhat with each dose so that the low current turn-on voltage shifts negatively with increasing each radiation dose (Figure 6.16(a)). Both the threshold voltage and turn-on shifts are nearly completely removed by annealing at 200 °C for 1 minute, and some recovery is also seen even at room temperature. The effect of $^{60}$Co gamma ray irradiation on 7-stage ZnO TFTs ring oscillators was also studied. Figure 6.16 (b) shows the operation characteristics for oscillators as fabricated and after 10 kGy and 200 kGy gamma ray doses. The circuits operate well after irradiation, with an increase in starting voltage and increased oscillation frequency. These changes are expected from the negative threshold voltage shift found for irradiated TFTs. Irradiation results for both devices and circuits on polyimide substrates are similar to those found on glass substrates.
Compared to conventional covalent silicon materials, ZnO TFTs have the potential for excellent radiation resistance. In conventional covalent semiconductors (like silicon in Figure 6.17 (a)), the chemical bonds are $p$ or $sp^3$ orbitals with strong directivity, and radiation damage can lead to strained bonds and deep trap states. In ZnO the cations form states at the conduction band minimum from spherically extended $s$ orbitals of the metals, greatly reducing the role of damage and disorder for conduction band transport because of the large overlap between adjacent spherical orbitals. (See Figure 6.17 (b).)

Figure 6.16 – (a) Extracted turn-on voltage shift versus irradiation doses. (b) 7-stage ring oscillators after different irradiation doses.

Figure 6.17 – (a) Energy band comparisons among several common semiconductors. (b) Top of valence band of ZnO (left), and bottom of conduction band of ZnO (right).
Due to its excellent radiation resistance, ZnO has the potential to be used in radiation environments, especially for neutron detection. Conventional neutron detectors generally include a sealed vessel containing a neutron sensitive gas, such as $^3$He or BF$_3$, and an electrically charged wire having leads that extend outside of the vessel [125, 126]. The whole system is bulky and has low sensitivity. Several attempts have been made on portable neutron detectors including PN diodes and Schottky junctions [127, 128]. The operation principles are identical: electron-hole pairs are generated from neutron absorption and later collected by semiconductor devices. However, conventional semiconductor material has the possibility of being affected by neutron irradiation as well, resulting in detection errors. In this work a new method of neutron detection was proposed by using floating gate ZnO TFTs.

Figure 6.18 shows the device structure for neutron detection. A ZnO TFT with the same inverted staggered structure was fabricated on a glass substrate first, followed by 30 nm ALD deposited Al$_2$O$_3$ for device passivation. 500 nm Gadolinium was then evaporated as the floating gate and patterned by a liftoff process. Finally, devices were encapsulated with 55 nm Al$_2$O$_3$ by PEALD. Gadolinium, a conversion material, was used as the floating gate because it has an exceptionally large capture cross-section for neutrons. The whole capture process can be described by the following equation, $^{157}\text{Gd} + n = ^{158}\text{Gd}^* \rightarrow ^{158}\text{Gd} + \gamma + X + e^-$. After neutrons were captured by Gadolinium, thermal electrons were generated and quickly escaped from devices because of their high energy, leaving positive charges in the floating gate. It is possible for thermal electrons to
generate 2\textsuperscript{nd} electrons if their energies are high enough, which can increase the detection sensitivity.

The positive charges raised the floating gate potential, resulting in a threshold voltage shift in the ZnO TFTs. Figure 6.19 shows the results of the floating gate neutron detection. Although the device transfer characteristics in Figure 6.19 (a) exhibited large negative threshold voltage for as deposited devices due to the process issue, they did not affect the detection. Devices were exposed to a homemade neutron source for 24 and 48 hours, respectively, and positive threshold voltage shifts were observed. The results were consistent with the operation principle of these devices, in which the floating gate has positive potential as well.

\textbf{Figure 6.18} – (a) Device structure of floating gate ZnO TFTs. (b) Microscope picture of single devices surrounded with big area of gadolinium for radiation detection.
Turn on voltage of devices with two different exposure areas were extracted and plotted in Figure 6.20. After being exposed to a low activity neutron source for 48 hours, a positive shift of 0.5 V was observed, corresponding to $5.5 \times 10^{11}$ /cm$^2$ charges in the floating gate. Devices with a larger exposure area also have a larger shift in turn on voltage. On the other hand, exposed devices were stored in an ambient environment for 12 hours and no shift was observed. It demonstrates that a 55 nm PEALD Al$_2$O$_3$ top layer is effective enough to retain a turn on voltage shift.

**Figure 6.19** – (a) Transfer characteristics for single TFT after being exposed to neutron source for some time. (b) Details of device curve show positive shift after exposure to neutron source.
In conclusion ZnO shows excellent radiation hardness, and preliminary results of neutron detection are encouraging for harsh environment applications.

**Figure 6.20** – Extracted turn-on voltage shift versus different exposure time for devices with two different exposure areas.

\[ V_{on} \text{ at } I_{DS} = 10^{-8} \text{ A} \]
Chapter 7

Conclusions and Future Work

7.1 Conclusions

In this thesis several achievements on flexible thin film electronics have been described. Great efforts have been made to obtain high performance thin film devices and circuits by low temperature processes. A unique approach of low temperature PECVD SiNx was proposed to encapsulate OLEDs. No delamination was observed for accelerated testing at high temperature and humidity, and the lifetime of encapsulated OLEDs with a bilayer process is longer than glass-to-glass encapsulation for room temperature aging. For an oxide semiconductor, pulsed-PECVD was proposed to fabricate ZnO films at a low temperature (200 °C) from diethylzinc (DEZ) and weak oxidants N₂O or CO₂. Pulsed-PECVD significantly increases the film’s refractive index and likely film density. Compared to the devices deposited by PECVD process, ZnO TFTs from pulsed-PECVD have much higher electronic performance with a saturation mobility 15 cm²/V·s, threshold voltage of 6.6 V, and current on/off ratio of 10⁸. Based on this work, a novel, low temperature deposition process (PEALD) was developed, and a high performance device with the fastest oxide circuits on flexible substrates were achieved. In order to better understand electron transport in oxide devices, tremendous work was done on device modeling. Non-ideal device characteristics such as passivation, contacts and output conductance were well modeled and verified with experimental results. Two different approaches were also proposed to extract device parameters for compact models and form the foundation for later circuit design and simulations. With the help of this novel deposition process and a better understanding of device physics in oxide
semiconductors, several application demos were successfully demonstrated. The lowest Hooge parameters of PEALD ZnO TFTs form a solid base for thermal application. Equivalent TCR of 5% in PEALD ZnO pyroFETs was extracted and comparable to current microbolometer technology. Microsensors with ZnO pyroFETs were also fabricated on flexible substrates for implantable application, and temperature sensitivity of 7 mV/°C was obtained. Finally, the irradiation hardness of PEALD ZnO was demonstrated, and ZnO TFTs with Gadolinium as the floating gate were successfully used to detect neutrons. In summary, the work in this thesis has ranged from a material deposition process to practical demo applications, and hopefully these achievements can explore new areas and opportunities in flexible thin film electronics.

### 7.2 Future Work

Since the first ZnO thin film transistor was reported in 2000, a decade has passed with numerous reported published. In 2010 SID oxide TFTs and OLEDs have been widely considered the two most important next generation display technologies. The oxide semiconductor for the display industry has stepped out of the research stage and into product production. However, research space for oxide semiconductors is still wide open, and new processes and materials may be the directions to follow.

Although ALD Al₂O₃ passivated devices on both glass and flexible substrates show excellent bias stress stability, negative bias stress stability has not been investigated for PEALD ZnO TFTs, especially under illumination conditions. In active matrix display switching TFTs are turned off most of the time and biased by negative stress. Devices
usually maintain stability under this condition. However, the stability becomes worse when the devices are exposed to ambient light. This situation is inevitable since display panels and oxide materials are transparent. One solution is using metals to block light, like a-Si:H technology. It is effective but will increase the cost and sacrifice the transparency. Initial investigations on amorphous IGZO have shown that oxygen vacancy ($V_O$) acts as a hole trap and plays an important role in the instability [129, 130]. Therefore, it is critical to understand the behavior of PEALD ZnO TFTs under negative bias illumination stress (NBIS). So far, almost all the amorphous oxide semiconductors deposited from sputtering have relatively worse NBIS, which becomes the main obstacle for further industry application. The PEALD process is novel and may have different results due to the different material properties. In addition to that, dielectric materials also play an important role in NBIS. Although Al$_2$O$_3$ is used in this work as dielectric mainly due to the well-controlled interface with ZnO, its charge injection and oxygen vacancy induced traps are the main source of device instability. It is also a very difficult material for gas phase etching. One possible solution is SiO$_2$, which has enough bandgap and nearly perfect dielectric characteristics. Since the load lock system described in chapter 3 is a showerhead system, compatible with main stream PECVD SiO$_2$ process, it is possible to deposit SiO$_2$ and ZnO in situ. Another improvement may lie in the passivation methods. ALD Al$_2$O$_3$ passivation has shown excellent stability for PEALD ZnO TFTs, but device threshold has to be controlled by using very thin ZnO active layer. To avoid chemical doping on the back channel from TMA, weaker reactants such as dimethylaluminum isopropoxide (DMAI) for ALD Al$_2$O$_3$ or metal organic silane for ALD SiO$_2$ should be considered.
Another interesting direction is the use of transparent ZnO devices on flexible PEN/PET substrates. In Chapter 4 polyimide was used as a substrate for flexible ZnO circuits; however, polyimide is more expensive and has a brown color compared to transparent plastic substrates such as PEN and PET, which are already commercially available. The difficulty of using these two substrates is their low glass transition temperature, ~ 175 °C. Though polyimide has a much higher glass transition temperature, unavoidable dimension instability was observed, and large relaxation design rules have to be applied by sacrificing the circuit speed due to large overlap parasitic capacitance. In addition to that, device performance degrades dramatically when the deposition temperature is lowered. Figure 7.1 shows the transfer characteristics of ZnO TFTs deposited by PEALD at 150 °C. Significant hysteresis and much lower current (mobility less than 1 cm²/V·s) were observed. How to improve device performance under lower deposition temperature

![Figure 7.1](image)

**Figure 7.1** – (a) Passivated ZnO TFTs deposited at 150 °C. (b) Diagram of self-aligned gate process. will become the main challenge. The hysteresis in these low temperature deposited device may come from the dielectric interface. It is believed that the deposition of initial several layers is critical for device performance and stability. Since the bombardment
from the plasma may damage the interface, low energy process for the initial ZnO layer deposition is preferred. One possible solution is to use ALD ZnO deposition for these layers. However, ALD deposited ZnO has mixture of different crystalline orientation, resulting negative threshold voltage shift. It is quite challenging to minimize this shift. To further take advantage of the transparency of the dielectric (Al₂O₃) and ZnO layers, a self-aligned process can be used to fabricate circuits on transparent substrates [60]. With transparent plastic substrates like PEN or PET, a self-aligned process has the natural ability of handling the dimension instability problem. This advantage can also bring the easiness of controlling the overlaps between source/drain and gate, further dramatically lowering parasitic capacitance. It is expected that the speed of ZnO circuits on transparent plastic substrates will be further increased.

The third major area lies in the p-type material. With a relatively high performance p-type TFT, it is possible to fabricate CMOS circuits. Compared with unipolar circuits, CMOS has several advantages including logic level conservation, simple circuit design, and high gain analog circuits. As discussed in Chapter 5, self-heating severely limits the application of oxide semiconductors on flexible substrates, but CMOS can effectively solve this problem by providing the advantage of low power consumption. Although organic TFTs have been used with oxide semiconductors to form hybrid CMOS circuits [105], the mismatch in their mobility is so large that the size of organic TFTs is significantly larger, resulting in low aperture ratio in display. Due to the large traps near the valence band in ZnO, it is impossible for it to become p-type material [22]. Several other oxide semiconductors were proposed, and p-type TFTs with relatively high
performance have been achieved [131]. However, the device stability for p-type TFTs and process compatibility with n-type ZnO are the main drawbacks. Therefore, it is important to explore some new p-type materials.

In conclusion, low temperature high performance thin film devices enabled new opportunities on large area electronic applications, and new materials and novel processes have become the main motivation for research in flexible thin film electronics.
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Vita

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