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HIGH PRESSURE CONFINED CHEMICAL VAPOR DEPOSITION OF ELECTRONIC METALATTICES AND SEMICONDUCTORS IN EXTREME GEOMETRIES

A Dissertation in

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ABSTRACT

New materials design with tunable physical properties has been the dream of many. Well-ordered nanometer-scale materials with 3-dimensional structural order could interact with electronic, magnetic and vibrational degrees of freedom of materials to engineer new properties into well developed semiconductor platforms such as silicon and germanium. The synthetic realization of such structures, which we define as metalattices with periodicity from 1 – 60 nm highlights the possibility of continuous tuning of properties. Ordered, electrically continuous 3D structural modulations of quantum confinement and interfacial physics could lead to new physical phenomena with new electrical, thermal, magnetic and acoustic responses.

This dissertation focus on the synthesis of electronic metalattice structures and other functional materials using high pressure confined chemical vapor deposition (HPcCVD). The synthetic route presented here allows for control over metalattices' periodicity, size, symmetry, chemical composition, topology and surface chemistries. The strategy used to fabricate metalattices is to deposit semiconductors such as silicon, germanium and zinc selenide into the pores of nano-templates using HPcCVD. High pressure (up to 70 MPa), allows for void free infiltration of high quality electronic grade materials into nano-pores. A series of templates, including silica colloidal crystals of different sizes, zeolites, mesoporous silica and metal-organic frameworks were examined for tuning periodicities, symmetries and sizes of metalattices. The first silicon and germanium metalattices with 14 nm, 30 nm and 60 nm were made possible with HPcCVD infiltration. A variety of characterization techniques, including Raman spectroscopy, scanning electron microscopy, transmission electron microscopy and x-ray diffraction were used to assess the as deposited materials quality. Post processing methods were developed to remove the nano-template and prepared the sample for advanced characterization and to increase the crystallinity of the synthesized metalattices.

Chapter 1 will provide a brief introduction to designable materials with tunable physical properties by altering the macro- and nano- scale structures of a material. The current synthetic limitation of structures similar to metalattices will be discussed and the HPcCVD infiltration of semiconductor in nano-templates will be introduced. Experimental designs and kinetics of HPcCVD will be discussed in *Chapter 2*. *Chapter 3* focuses on the synthesis of the first elemental semiconductor metalattices made with silicon and germanium. Void free filling of nano-templates is confirmed using positronium annihilation lifetime spectroscopy. As deposited amorphous Si and Ge metalattice were crystallized via thermal processing. A method combining with Cl_2 reaction ion etching (RIE) and hydrofluoric (HF) acid was developed to remove unwanted HPcCVD semiconductor coatings and template removal for surface chemistry tuning. Compound semiconductor metalattice is demonstrated in *Chapter 4* by HPcCVD infiltration of ZnSe into pores of silica colloidal crystals. *Chapter 5* will present metalattice structures made with templates other than silica colloidal crystals, including zeolite Y, mesoporous silica and metal-organic frameworks. Other functional materials, silicon glue between substrates and hydrogenated amorphous silicon solar fabrics are addressed in *Chapter 6*, with demonstration of a proof-of-concept Schottky junction on the HPcCVD infiltration solar fabric.

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Chapter 1

Introduction: From Materials Discovered in Nature to Materials by Design

For many years, materials discovery has been about finding existing structures allowed by nature. Materials discovery to real life application is a long road as scientists spend a good portion of their time to understand physical properties of the newly found materials. They then transition to being creative to find an everyday application. For example, one of the most technologically relevant and important semiconductor, silicon, was first discovered in 1824 by a Swedish chemist named Jöns Jacob Berzelius[1]. But it was not widely known as a useful material until more than a century later when the first silicon transistor was made in 1954.

William Shockley and coworkers from Bell Labs made the first semiconductor transistor using germanium in 1947[2,3]. By early 1950s, many researchers were learning to make transistors out of one of the most earth abundant elements, silicon, but most thought it was not possible for mass production. The realization of silicon transistors was a dramatic event and shock the semiconductor community. On May 10, 1954 at the National Conference on Airborne Electronics held in Dayton, Ohio by the Institute of Radio Engineers, Gordon Teal of Texas Instruments Inc. announced the following[3],

> "Contrary to what my colleagues have told you about the bleak prospects for silicon transistors, I happen to have a few of them here in my pocket. …… Yes, we have three types of silicon transistors in production"
>
> - Gordon Teal[3], May 10, 1954

Teal, a physical chemist, spent years perfecting the growth and processing of silicon before he was able to make the first silicon transistor one month before the conference[3]. The demonstration of silicon transistor manufacturing revolutionized the semiconductor industry and brought attention to the field that silicon can be used to replace germanium. The rise of Si transistors and computer components eventually lead to the creation of many current technology leaders including Intel, AMD, Nvidia and Kleiner Perkins[4]. Silicon has since become the building block of electronic devices, from calculators, smart phones and computers to semiconductor detectors and solar cells. One reason silicon became the most important semiconductor is its degree of freedom in tuning electrical properties in synthesis by introducing a small concentration of impurities as dopants. The electrical conductivity can be engineered systematically by controlling amounts of positive or negative carriers (defects) introduced to the silicon crystal. For example, the resistivity of polycrystalline silicon drops from about $5 \times 10^{2}\ ohm\ cm$ to $1 \times 10^{-1}\ ohm\ cm$ when the boron dopant concentration increases from $1 \times 10^{18}\ atoms\ /cm^{3}$ to $1 \times 10^{19}\ atoms\ /cm^{3}$, respectively[5,6]. The relationship between dopant concentrations and electrical properties of bulk silicon can be measured experimentally and calculated theoretically[7]. This degree of freedom allows for tuning of properties to suit different applications.

The transition from discovery of elemental silicon to using silicon as the basics of transistors took 130 years which is seemingly long for technological demands and needs in modern days. If it were possible to design materials so the researcher can control what properties and functionality the product has, we might then be able to satisfy today's technology needs quicker. That is the idea of functional materials by design, where a need for particular functionality in a material is first identified for an application. Those criterion are input to discover and synthesize the new material from the bottom up at the atomic and molecular scale[8]. Designable materials would allow us to build artificial materials and structures beyond what is

allowed by nature, creating ever complex structures with improved properties. The key to success in the materials by design idea is that we must build a strong foundation in understanding the structure-property relationship, then apply our knowledge to construct new materials. Synthetic control over such materials would be essential in creating a functional material.

One of the fields that has taken the "materials by design" idea is photonic metamaterials. Instead of searching for materials existing in nature with the proper optical properties, scientists have learned to synthesize artificial structures which manipulate transport of electromagnetic waves from near-ultraviolet (UV) to near-IR wavelengths[9–13]. Photonic metamaterials can be made with refractive index values never observed in nature. For example, negative refractive index metamaterials[11], high and low refractive indexes (less than 1 and higher than 3.5 real part of refractive index compared to most solid materials)[11] and invisible cloaks[14,15].

1.1. Macro-scale 3D Ordered Semiconductors

In one class of photonic metamaterials, photonic bandgap crystals[10,13,16], a three-dimensional metamaterial can be created to control and prohibit certain wavelengths of light traveling through the material. These materials are called photonic bandgap as they forbid electromagnetic waves of certain frequencies to pass through a medium[10,16], similar to an electronic bandgap where no electronic states in those energies exist in a semiconductor. Photonic bandgap crystals haves periodic structures in 3D and repeating units in hundreds of nanometers and up to micrometers to confine and manipulate how photons of the corresponding wavelengths guide through the material. Photonic crystals are typically made by filling various materials into the pores of synthetic opal. Synthetic opal are silica or polystyrene nanoparticles in hundreds of nanometers up to a few microns in diameter self-assembled to form a closed packed FCC structure. The interstitial sites are then infiltrated by liquid or gas phase synthesis with

various materials, including silicon[10,13,17], germanium[17], carbon[18], titania[19], silica[20], indium oxide[21] and nickel/nickel oxide core/shell[22]. These structures are excellent in controlling the optical properties of a solid material, as the structural order interacts with certain frequencies of light. The modulation of light could allow for all optical integrated devices instead of relying on electron transport for information.

1.2. Nano-scale 3D Ordered Semiconductors

In addition to photonic metamaterials, the synthesis and study of metamaterials in the nanoscale has been a rising field in recent years yielding materials with tunable electrical, thermal and vibrational properties. For example, researchers are interested in building semiconductor nanocrystal arrays by self-assembling nanoparticles or quantum dots[23,24]. Heat transport in semiconductor is different from metal in that the heat is carried by phonons, quantized vibration of atomic lattices, instead of by electrons[25]. Heat and electrical transport can then be tuned independently. Semiconductors in nano-sizes are prone to quantum confinement effects[26] with tunable electronic properties, but when assembled together, the nanoparticles can only be kept stable with ligands or surfactants, complicating the electrical transport processes through multiple mediums and interfaces. The electrical conductivity of nanocrystal arrays are usually lower than that of bulk semiconductor because it is more difficult to inject charge into a nanoparticle; then transfer that charge from one nanoparticle to the other one through the ligands[25]. Most ligands are made of organic materials with long chains of insulating hydrocarbons and can lower conduction because of poor electron tunneling through the surfactants[24,27,28]. One option to reduce charge transfer limited by ligands or surfactants is to sinter the assembled nanocrystal array to a continuous film. The injected charge can then be directly transferred between particles. Nanocrystal arrays can be fused into a continuous film at a lower temperature compared to the

melting point of its equivalent bulk material by the effect of surface tension. This approach has been used to make both metallic (gold[29] and silver[30]) and semiconducting (CdS [24], CdSe [31,32] and HgTe [33]) fused film. However, the challenge with sintering quantum confined nanocrystals is again the ligands which are needed to maintain its stability, shapes and sizes[24]. Most ligands are made of organic materials that can only withstand low temperature; these ligands decompose during the sintering process and thus contaminate the semiconductor nanoparticles. On-going research by various groups have been focusing efforts to replace the ligands with all inorganic materials such as $In_2Se_4^{2-}$ to increase the conductivity between particles[25].

1.3. Electronic Metalattices in the Nano-Scale

Materials discovery has long been about searching for materials existing in nature then understanding their physical properties, which derive from atomic alignments or atomic lattices then applying such materials for specific applications. However, materials found in nature do not necessarily contain the properties that could suit the needs. Many have tried to discover materials in a proactive way where we combine both theory and synthesis to predict structure-property relationships. With the help of computational studies, we can quickly screen hundreds to thousands of materials for feasibility experimentally. For example, 56 graphene like 2D structures were found to have interesting properties and possible to reproduce experimentally from a list of 108,423 structures[34]. Over the years, chemists have found creative methods to substitute elements[35] in a known structure to yield a new crystal, which could have very different properties than its original structure[36,37]. The discovery of graphene led to great interest in graphene like 2D materials made with other elements such as MoS_2 and hexagonal BN. The chemical composition of a material can be altered to change its electronic, optical magnetic and vibration properties. Photonic metamaterials in IR or optical length-scale (hundreds of

nanometers to a few micro-meters) are known and scientist are successful in manipulating their optical properties[9–13]. However, 3-dimensional artificial electronic metalattices in the intermediate length-scale, from 1- 60 nm, cannot be designed with high purity semiconductors. The repeating units, or periodicity (similar to lattice spacing in atomic lattices), are appropriate in coupling with many physical phenomena, including magnetic coherence lengths, electrons, excitons and phonons as it matches with the mean free paths of these processes (**Figure 1-1**).

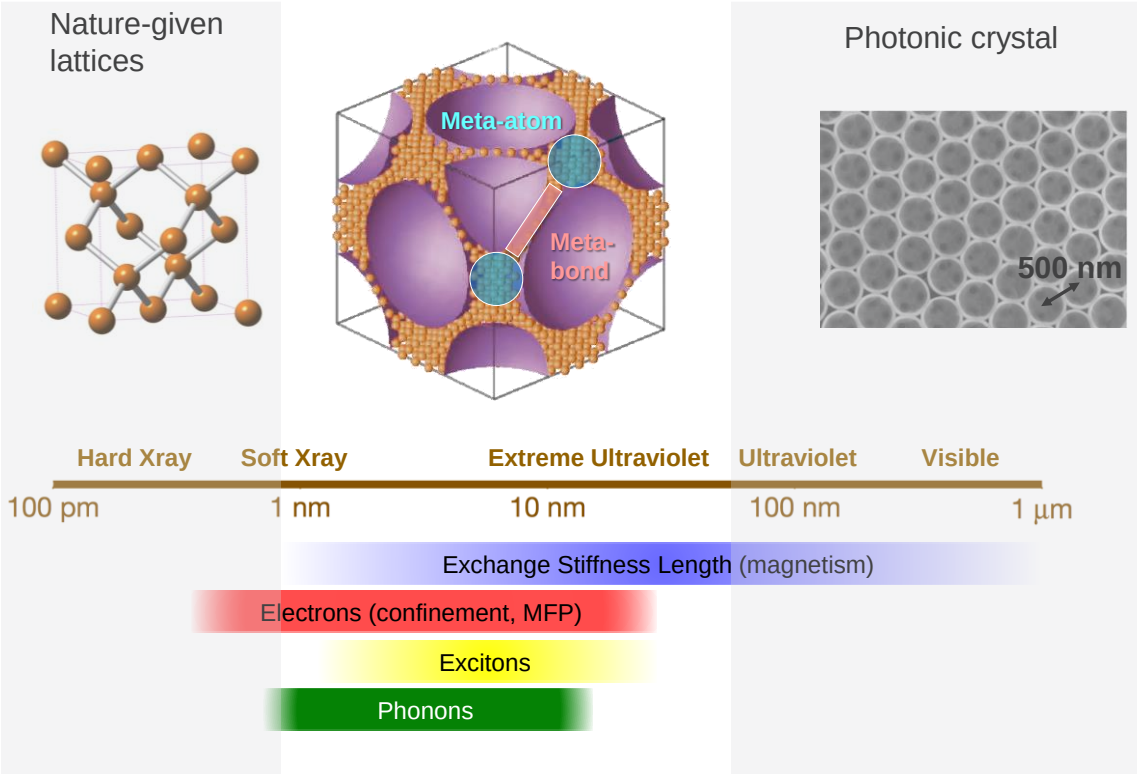

Figure 1-1. 3D electronic metalattices. Artificial metalattice structures have the same periodicity as many physical processes, such as electron, exciton and phonon mean free path, and magnetic coherence lengths. Metalattices have length-scale between atomic lattices and photonic crystal, which is appropriate to interact with many physical phenomena to give rise to new physics and chemistry. The length-scale of interest in metalattice is from 1 – 60 nm in the white window shown above.

We call these artificial periodic structures with intermediate lengthscale metalattices. Metalattices consists of two major components, meta-atoms and metabonds, which are macro

equivalent of an atom and a chemical bond composed of clusters of atoms (**Figure 1-1**). Meta-atoms are similar to its quantum dots counterparts but are interconnected by thin meta-bonds made of the same chemical composition. Freedom in tuning metalattices' sizes, periodicity and chemical composition could allow for tuning of physical properties and allows application in areas such as solar cells, near-IR photonics, light emitting devices and thermoelectrics. For example, semiconductors with sizes smaller than its exciton Bohr radius can exhibit quantum confinement effects for tunable bandgap (**Figure 1-2**). The exciton Bohr radius is around 4.5 nm in Si and 24 nm in Ge[38,39]. Quantum confinement happens when one or more dimensions of a structure is confined to below the exciton Bohr radius of the material limiting charge carrier's degree of freedom in a semiconductor[40]. Quantum dots are when all three dimensions of a structure are confined, where there is zero degree of freedom for carrier particles. When two dimensions are confined, it is known as a quantum wire (1D wire), and a quantum wall (2D thin film) is defined when only 1 dimension is confined[39] (**Figure 1-3**). Since meta-atoms are similar to quantum dots in shape, we could alter its bandgap by changing its sizes to confine the individual meta-atom in all 3 dimensions; but meta-atoms are different from quantum dots in that they are interconnected by meta-bonds that could facilitate pervasive 3D transport of electron and phonons while preserving quantum confinement.

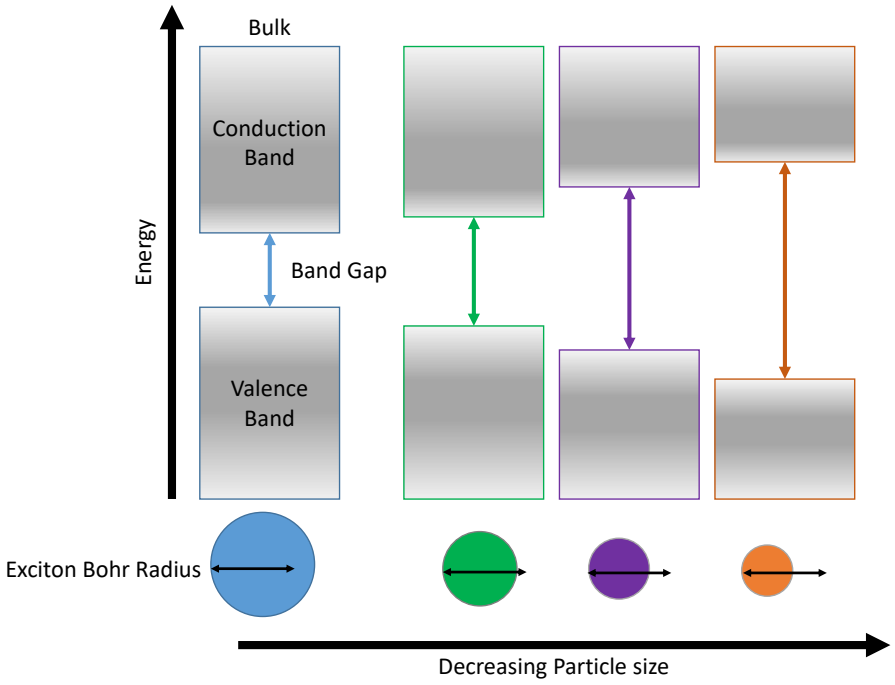

Figure 1-2. Quantum confinement effect in nano-structures. When the particle size in quantum dots, or semiconductor nanoparticles, are smaller than of its exciton Bohr radius, the band gap of the semiconductor is larger than of the bulk material.

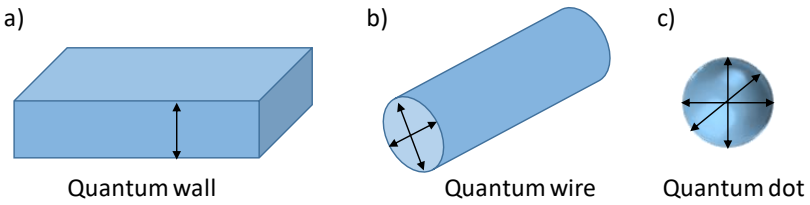

Figure 1-3. Quantum confinement in various dimension. Quantum confinement can be implied in 1D (a), 2D (b) and 3D (c) for quantum wall, quantum wire and quantum dot, respectively.

Highly ordered, interconnected materials also interweave the structure; the lattice can interact with different physical processes in semiconductors, metals and co-lattices of two materials. Structural modulations of quantum confinement and interfacial physics may define a new physical regime for electronic, optical, magnetic, and thermal response. The synthetic

realization of metalattices made with well-developed semiconductor platforms such as Si could lead to new physical phenomena and practical application, such as high mobility semiconductors with properties tunable by quantum confinement and strain, high Tc ferromagnetic semiconductors and improved thermoelectric materials. Independent control over metalattices' periodicity, sizes, chemical composition, surface chemistry and symmetry will be essential in increasing the degree of freedom for tuning of physical properties.

1.4. Existing Synthetic Routes and Limitations

Previous studies on structures similar to metalattices show limitations in creating highly ordered structures made with electronic grade semiconductors (99.999% purity). Some methods such as magnesiothermic reduction[41] (high temperature reduction of silica to silicon using magnesium), solution phase synthesis[42,43] and decomposition of diphenylsilane[44,45] attempted to produce mesoporous (2 – 50 nm) structures, comparable to metalattices, but fails to achieve high quality semiconductors with precise doping. These methods also suffers from precursor/ reactant/ parent structure (such as silica in magnesiothermic reduction) shrinkage during reaction, making it difficult to control the porosity and periodicity of the final products.

Other methods, such as chemical vapor deposition (CVD) and atomic layer deposition (ALD) have been used to create inverse opal structures but at a larger length-scale from 160 nm – 1.1 μm[46–48], exceeding the characteristic length-scale of interest. CVD and ALD can afford high purity materials and dopant precursors can be added to the gas mixture for precise doping concentration. ALD uses surface chemistry to deposit materials layer by layer which has a limit on what materials can be deposited, has a slow reaction rate[49], and cannot fully fill the pores because the meta-atom are larger than meta-bond regions. Conventional CVD cannot be used to deposit in nanopores and deep trenches because the molecular mean free paths of precursors limit

gas transport. CVD or ALD deposition in other templates, such as in zeolites and mesoporous silica using disilane and digermane pyrolysis, failed to make interconnected structures and instead made isolated nanoparticles in the pores of the templates[50]. At the metalattice's scale regime of 1 – 60 nm, infiltration of materials into nanopores using conventional CVD and ALD is difficult due to low density of infiltrated precursors into the 3D template, shrinkage of precursor upon reaction, lack of pressure driven flow and blockage of pores from homogeneous nucleation.

1.5. Novel Approach using Nano-templates and High Pressure Technique

Although reasonable micro-scale ordered structures similar to the proposed structure of metalattices have been synthesized, smaller length-scale at 10s of nanometers with electrically connected 3-dimensional semiconductor networks has yet to be discovered. Existing synthetic methods lacks the ability to create electronic grade semiconductor in confined, yet ordered and interconnected structures. Most of the existing structures either shorts on the quality of semiconductor or the overall order of the structure. This dissertation will focus on an unique approach by combining high pressure confined chemical vapor deposition (HPcCVD)[51–55] and nano-templates to create highly ordered electronic metalattices made with ultra high purity semiconductors, including a-Si:H, a-Si, c-Si, n^+-Si, a-Ge:H, a-Ge, n^+-Ge and ZnSe. The semiconductors of interest here are all well-developed and studied platforms, which will allow us to easily compare the newly created structural materials with bulk structures. In addition, study of silicon (currently most widely used semiconductor) and germanium means that metalattices could easily be intergraded to the current technologies and semiconductor industries.

The possibility of creating an artificial structural order that could interact with physical processes is intriguing in that the metalattice may allow us to finely engineer specific physical properties into a material that cannot exist in nature. The thought of shaping elemental silicon,

one of the most earth abundant element, to other properties can lead to higher performance in silicon-based devices, such as detectors, electronics, photonics and optoelectronics. High pressure techniques allows molecular precursors in gas phase to infiltrate into complex 3-dimensional topologies to yield the proposed metalattice structure. In addition, opportunities from using HPcCVD to infiltrate various 1-dimensional, 2-dimensional and 3-dimensional templates with features in the nano-scale to micro-scale to fabricate atom-precise electronic metalattices, optical fibers, thin film structures and solar fabrics will be discussed. This approach provides a pathway to high quality semiconductor structures that is challenging in traditional synthetic routes. Structural materials in the nano-scale can be synthetically realized using HPcCVD, paving a way to study structure-property relationship with coupling to electron, phonon, exciton and photon mean free path.

1.6. References

1. Physik, M. B. ART . XI . --On the Mode of obtaining Silicium , and on the Characters and Properties of that Substance. *Bost. J. Philos. Arts* **3,** 115 (1826).
2. Shampo, M. A., Kyle, R. A. & Steensma, D. P. William Shockley and the Transistor. in *Mayo Foundation for Medical Education and Research* **87,** e43 (Elsevier Inc., 2012).
3. Riordan, M. & Hoddeson, L. *Crystal Fire: The Birth of the Information Age*. (W. W. Norton & Company, 1997).
4. Thackray, A., Brock, D. C. & Jones, R. *Moore's Law: the life of Godon Moore, Silicon Valley's quiet revolutionary*. (Basic Books - The Perseus Books Group, 2015).
5. Pearson, G. L. & Bardeen, J. Electrical properties of pure silicon and silicon alloys containing boron and phosphorus. *Phys. Rev.* **75,** 865–883 (1949).
6. Seto, J. Y. W. The electrical properties of polycrystalline silicon films. *J. Appl. Phys.* **46,**

5247–5254 (1975).

7. Thurber, W. R., Mattis, R. L., Liu, Y. M. & Filliben, J. J. *Semiconductor Measurement Technology: The Relationship Between Resistivity and Dopant Density for Phosphorus- and Boron- Doped Silicon*. (U. S. Department of Commerce, 1981).
8. Shuguang Zhang. Building from the bottom up. *Mater. Today* **6,** 20–27 (2003).
9. Liu, N. *et al.* Three-dimensional photonic metamaterials at optical frequencies. *Nat. Mater.* **7,** 31–37 (2008).
10. Blanco, A. *et al.* Large-scale synthesis of a silicon photonic crystal with a complete three-dimensional bandgap 1.5 micrometres. *Nature* **405,** 437–440 (2000).
11. Smith, D. R., Pendry, J. B. & Wiltshire, M. C. K. Metamaterials and negative refractive index. *Science (80-.).* **305,** 788–792 (2004).
12. Iwanaga, M. Photonic metamaterials: A new class of materials for manipulating light waves. *Sci. Technol. Adv. Mater.* **13,** 53002 (2012).
13. Joannopoulos, J. D., Villeneuve, P. R. & Fan, S. Photonic crystals:putting a new twist on light. *Nature* **386,** 143–149 (1997).
14. Gandji, N. P. & Semouchkina, E. Employing self-collimation phenomena in photonic crystals for the invisibility cloak development. in *2016 IEEE Antennas and Propagation Society International Symposium, APSURSI 2016 - Proceedings* 1967–1968 (2016). doi:10.1109/APS.2016.7696690
15. Semouchkina, E. *et al.* Superluminal media formed by photonic crystals for transformation optics-based invisibility cloaks. *J. Opt.* **18,** 44007 (2016).
16. Vlasov, Y. A., Bo, X. Z., Sturm, J. C. & Norris, D. J. On-chip natural assembly of silicon photonic bandgap crystals. *Nature* **414,** 289–293 (2001).
17. Meseguer, F. *et al.* Synthesis of inverse opals. *Colloids Surfaces A Physicochem. Eng. Asp.* **202,** 281–290 (2002).

18. Zakhidov, A. A. *et al.* Carbon structures with three-dimensional periodicity at optical wavelengths. *Science (80-.).* **282,** 897–899 (1998).

19. Waterhouse, G. I. N. & Waterland, M. R. Opal and inverse opal photonic crystals: Fabrication and characterization. *Polyhedron* **26,** 356–368 (2007).

20. Hatton, B., Mishchenko, L., Davis, S., Sandhage, K. H. & Aizenberg, J. Assembly of large-area, highly ordered, crack-free inverse opal films. *Proc. Natl. Acad. Sci.* **107,** 10354–10359 (2010).

21. Amrehn, S. *et al.* Indium oxide inverse opal films synthesized by structure replication method. *Photonics Nanostructures - Fundam. Appl.* **19,** 55–63 (2016).

22. Kim, J.-H. *et al.* Ni–NiO core–shell inverse opal electrodes for supercapacitors. *Chem. Commun.* **47,** 5214–5216 (2011).

23. Talapin, D. V & Murray, C. B. PbSe Nanocrystal Solids for n-and p-Channel Thin Film Field-Effect Transistors. *Science (80-.).* **310,** 86–90 (2005).

24. Talapin, D. V., Lee, J.-S., Kovalenko, M. V. & Shevchenko, E. V. Prospects of Colloidal Nanocrystals for Electronic and Optoelectronic Applications. *Chem. Rev.* **110,** 389–458 (2010).

25. Lee, J. S., Kovalenko, M. V., Huang, J., Chung, D. S. & Talapin, D. V. Band-like transport, high electron mobility and high photoconductivity in all-inorganic nanocrystal arrays. *Nat. Nanotechnol.* **6,** 348–352 (2011).

26. Takagahara, T. & Takeda, K. Theory of the quantum confinement effect on excitons in quantum dots of indirect-gap materials. *Phys. Rev. B* **46,** 15578–15581 (1992).

27. Yu, D., Wang, C. & Guyot-Sionnest, P. n-Type Conducting CdSe Nanocrystal Solids. *Science (80-.).* **300,** 1277–1280 (2003).

28. Vanmaekelbergh, D. & Liljeroth, P. Electron-conducting quantum dot solids: novel materials based on colloidal semiconductor nanocrystals. *Chem. Soc. Rev.* **34,** 299–312

(2005).

29. Wu, Y. *et al.* High-performance organic thin-film transistors with solution-printed gold contacts. *Adv. Mater.* **17,** 184–187 (2005).

30. Wu, Y., Li, Y. & Ong, B. S. Printed silver ohmic contacts for high-mobility organic thin-film transistors. *J. Am. Chem. Soc.* **128,** 4202–4203 (2006).

31. Ridley, B. A., Nivi, B. & Jacobson, J. M. All-Inorganic Field Effect Transistors Fabricated by Printing. *Science (80-.).* **286,** 746–750 (1999).

32. Colvin, V. L., Schlamp, M. C. & Alivisatos, A. P. Light-emitting diodes made from cadmium selenide nanocrystals and a semiconducting polymer. *Nature* **370,** 354–357 (1994).

33. Kim, H., Cho, K., Kim, D. W., Lee, H. R. & Kim, S. Bottom- and top-gate field-effect thin-film transistors with p channels of sintered HgTe nanocrystals. *Appl. Phys. Lett.* **89,** 173107 (2006).

34. Mounet, N. *et al.* Two-dimensional materials from high-throughput computational exfoliation of experimentally known compounds. *Nat. Nanotechnol.* **13,** 246–252 (2018).

35. Anno, H., Hokazono, M., Kawamura, M. & Matsubara, K. Effect of Transition Element Substitution on Thermoelectric Properties of Semiconductor Clathrate Compounds. in *22nd International Conference on Thermoelectrics* 121–126 (2003).

36. Abate, A. Perovskite Solar Cells Go Lead Free. *Joule* **1,** 659–664 (2017).

37. Ong, W. L., Rupich, S. M., Talapin, D. V., McGaughey, A. J. H. & Malen, J. A. Surface chemistry mediates thermal transport in three-dimensional nanocrystal arrays. *Nat. Mater.* **12,** 410–415 (2013).

38. Barbagiovanni, E. G., Lockwood, D. J., Simpson, P. J. & Goncharova, L. V. Quantum confinement in Si and Ge nanostructures: Theory and experiment. *Appl. Phys. Rev. 1* **1,** 11302 (2014).

39. Park, N. M., Choi, C. J., Seong, T. Y. & Park, S. J. Quantum confinement in amorphous silicon quantum dots embedded in silicon nitride. *Phys. Rev. Lett.* **86,** 1355–1357 (2001).

40. Koole, R., Groeneveld, E., Vanmaekelbergh, D., Meijerink, A. & de Mello Donega, C. in *Nanoparticles* 13–51 (Springer, 2014). doi:10.1007/978-3-662-44823-6

41. Richman, E. K., Kang, C. B., Brezesinski, T. & Tolbert, S. H. Ordered mesoporous silicon through magnesium reduction of polymer templated silica thin films. *Nano Lett.* **8,** 3075–3079 (2008).

42. Sun, D. *et al.* Hexagonal nanoporous germanium through surfactant-driven self-assembly of Zintl clusters. *Nature* **441,** 1126–1130 (2006).

43. Armatas, G. S. & Kanatzidis, M. G. Hexagonal Mesoporous Germanium. *Science (80-.).* **313,** 817–820 (2006).

44. Nicholas R. B. Coleman, Morris, M. A., Spalding, T. R. & Holmes, J. D. The Formation of Dimensionally Ordered Silicon Nanowires within Mesoporous Silica. *J. Am. Chem. Soc.* **123,** 187–188 (2001).

45. Coleman, N. R. B. *et al.* Synthesis and Characterization of Dimensionally Ordered Semiconductor Nanowires within Mesoporous Silica. *J. Am. Chem. Soc.* **123,** 7010–7016 (2001).

46. Lee, Y., Park, S., Han, S. W., Lim, T. G. & Koh, W. G. Preparation of photolithographically patterned inverse opal hydrogel microstructures and its application to protein patterning. *Biosens. Bioelectron.* **35,** 243–250 (2012).

47. Stein, A., Li, F. & Denny, N. R. Morphological control in colloidal crystal templating of inverse opals, hierarchical structures and shaped particles. *Chem. Mater.* **20,** 649–666 (2008).

48. Retsch, M. & Jonas, U. Hierarchically structured, double-periodic inverse composite opals. *Adv. Funct. Mater.* **23,** 5381–5389 (2013).

49. George, S. M. Atomic Layer Deposition: An Overview. *Chem. Rev.* **110,** 111–131 (2010).

50. Besson, S., Gacoin, T., Ricolleau, C., Jacquiod, C. & Boilot, J. P. 3D Quantum Dot Lattice Inside Mesoporous Silica Films. *Nano Lett.* **2,** 409–414 (2002).

51. Sazio, P. J. A. *et al.* Microstructured Optical Fibers as High-Pressure Microfluidic Reactors. *Science (80-.).* **311,** 1583–1586 (2006).

52. Baril, N. F. *et al.* Confined high-pressure chemical deposition of hydrogenated amorphous silicon. *J. Am. Chem. Soc.* **134,** 19–22 (2012).

53. He, R., Day, T. D., Sparks, J. R., Sullivan, N. F. & Badding, J. V. High Pressure Chemical Vapor Deposition of Hydrogenated Amorphous Silicon Films and Solar Cells. *Adv. Mater.* **28,** 5939–5942 (2016).

54. Sparks, J. R., Sazio, P. J. A., Gopalan, V. & Badding, J. V. Templated Chemically Deposited Semiconductor Optical Fiber Materials. *Annu. Rev. Mater. Res.* **43,** 9.1-9.31 (2013).

55. Baril, N. F. *et al.* High-Pressure Chemical Deposition for Void-Free Filling of Extreme Aspect Ratio Templates. *Adv. Mater.* **22,** 4605–4611 (2010).

Chapter 2

High Pressure Confined Chemical Vapor Deposition (HPcCVD)

High pressure can be used to overcome some limitations of low pressure chemical vapor deposition techniques, such as slow mass transport of gas precursors and high kinetic barrier, to produce electronic grade semiconductors in high surface area to volume ratio geometries[1–12]. Operating pressure in most chemical vapor deposition (CVD, low pressure or atmospheric pressure) are in the range of 1 Pa to 0.1 MPa[13–18], whereas the operating pressure in high pressure CVD systems are in the range of 35 – 70 MPa[1,2,5,7,19]. Most of the gas phase chemistry in the low pressure system can be adapted to high pressure CVD systems and serve as a guideline for materials fabrication. However, modification to gas mixture ratios, reaction conditions and reactor designs are needed for high pressure systems as compared to LPCVD or APCVD because the increased pressure also alters kinetics of various reaction mechanisms. This chapter will focus on fundamentals of High Pressure confined Chemical Vapor Deposition (HPcCVD) and how the technique can be used to fabricate 1-dimensional[1–4,6–8,19,20], 2-dimensional[5] and 3-dimensional[11] structural materials in the micro- and nano- scales.

2.1. Limitation of Low Pressure and Conventional Chemical Vapor Deposition

Chemical Vapor Deposition (CVD) is a powerful technique for conformal deposition of high purity semiconductor with precise control of dopant concentration over a large area[21]. In the case of low pressure CVD, precursor gas molecules and carrier gas (inert gas such as helium or argon) are driven toward the targeted deposition substrate through a small pressure gradient. Reactant gas molecules are decomposed near the surface of the substrate and materials can be

deposited onto the substrate[21]. By-products and excess reactants can then be exhausted through the outlet (**Figure 2-1**). Intentional impurities are introduced into the gas mixture to allow controlled doping in semiconductors. For example, a small amount of phosphine (PH_3) or diborane (B_2H_6) can be added to a mixture of silane (SiH_4) and carrier gas to afford n-Si and p-Si, respectively. However, there are limitations in low pressure and conventional CVD preventing its use in complex geometries in the micro- and nano-scale[22].

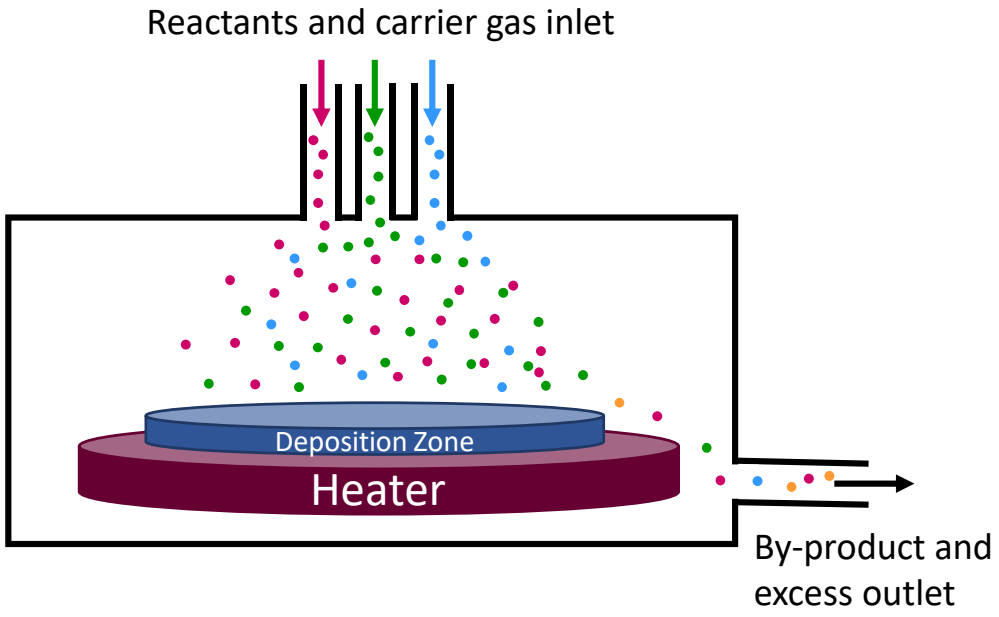

Figure 2-1. Schematic of a low pressure or conventional CVD chamber. Multiple reactants are sent into the reaction chamber individually to deposit various materials. The mean free path of precursor gas molecules is in the range of hundreds of nanometers in the low pressure regime, limiting mass transport of precursor gas molecules into pores smaller than the MFP of the molecules.

The mean free path of the gas molecules which is the average distance a molecule would travel before colliding with another molecule, can describe mass transport of precursors into small pores. In conventional CVD, the most common operating pressure ranges from vacuum to

1 atm, where gas molecules have a large mean free path of hundreds of nanometers, given by the kinetic theory of gases[23],

$$l = \frac{k_B T}{\sqrt{2}\pi d^2 P} \qquad \textbf{(Equation 2.1)}$$

where k_B is the Boltzman's constant, T is the temperature of gas molecule, P is the pressure of the gas and d is the kinetic diameter of the gas molecule. Conformal coating inside geometries with a diameter close to or less than the MFP of gas molecules becomes a challenge because mass transport of reactants into pores relies on effusion (**Figure 2-2**), a slower process as compared to diffusion. This results in slow materials growth inside micro- and nano-pores. When the deposition zone in conventional CVD reaction is replaced with a porous structure, insufficient amount of gas molecules are transported into the pores before the outer surface is coated with deposited materials, quenching further transfer of gas molecules into the pores and stopping materials growth inside the pores altogether.

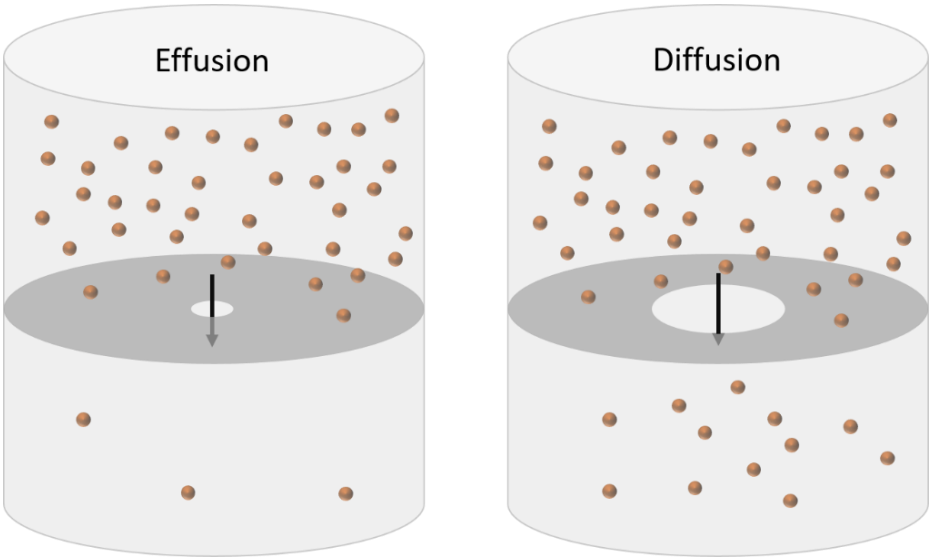

Figure 2-2. Difference between effusion and diffusion. In effusion, the mean free path (MPF) of the gas molecule is significantly larger than the pore diameter, limiting the number of gas molecules traveling into a new volume because only molecules traveling a certain path can enter through the pore. When diffusion is the dominating mechanism, gas molecules can travel to the new volume through hydrodynamic flow.

High pressure can be used in CVD systems to increase the transport rate of gas molecules in micro- and nano-pores[7]. As suggested by **equation 2.1**, MFP of gases are inversely proportional to pressure of the gas. When the MPF of gas molecules in a system is smaller than the diameter of the pore it has to travel through, the kinetic barrier is smaller and gases can pass by the pore by diffusion (**Figure 2-2**), allowing hydrodynamic flow.

2.2. Void Free Infiltration of Semiconductors using High Pressure Chemical Vapor Deposition in 1D Geometries

High pressure plays an important role in allowing materials production in extreme aspect ratio geometries, such as in silica capillaries for optical fiber fabrication with various semiconductors including silicon[2,3,5,19], germanium[20] and zinc selenide[6,7,10]. The traditional method of optical fiber fabrication is by a drawing technique[24,25], where a preform is heated to its glass transition temperature and quickly pulled to form a thin strand of glass. However, not all materials can be drawn into an optical fiber, especially high purity semiconductors. Optical fiber drawing requires the cladding (silica tube) and core to have similar melting temperatures, but melting the core and cladding materials together could introduce defects into the final product. For example, when silicon optical fibers are fabricated using fiber drawing technique, oxygen is often incorporated in the interface of Si/SiO_2 affecting Si material quality[26,27]. High pressure CVD was developed in 2006 to address such issue by depositing high quality, electronic grade semiconductors in silica capillaries for optical fiber fabrication[1]. During HPCVD optical fiber fabrication, precursor and carrier gas enters into the pore of silica capillary and materials are gradually deposited onto the wall of the inner pore. Carrier gas and by products are exhausted through the outlet.

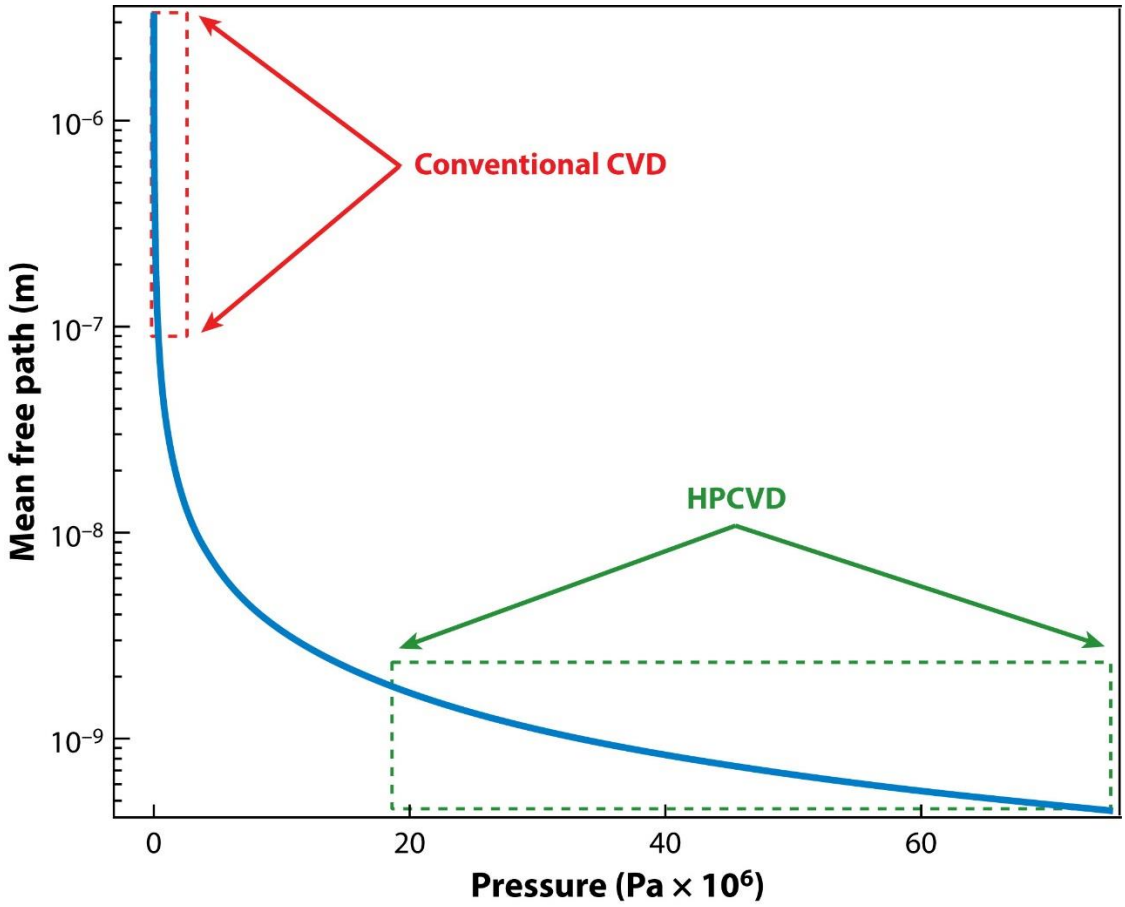

Figure 2-3. Effect of pressure on MFP of gas molecules in CVD systems. In the high pressure region, the MFP of H_2 gas molecules at 400 °C is reduced to less than 1 nm as shown with this plot. Reprinted with permission from Reference 7. Copyright 2018 Annual Reviews.

As discussed in the previous section, high pressure enables gas molecules to travel into small pores via diffusion because of its reduced MFP. **Figure 2-3** shows how pressure affects the mean free path of hydrogen molecules at 400 °C. In low pressure and atmospheric pressure CVD, MFP of gas molecules are from μm to hundreds of nm. Most optical fiber fabrication uses silica capillary with μms ranges inner pore diameter. However, the inner diameter shrinks over time as materials are deposited in the core of a silica capillary; precursor gas must travel through a smaller pore to completely fill the pore and as the filling progresses, it becomes more difficult for more reactants to enter into the pore in low pressure systems. High pressure allows gases to

diffuse into tiny pores quickly to completely fill the remaining spaces. When the total pressure of hydrogen is in the high pressure CVD regime (**Figure 2-3**), from 30 – 70 MPa, MFP of H_2 gases drop to less than 1 nm to eliminate the mass transport issue observed in low pressure and atmospheric pressure CVDs. For the case of silicon and germanium optical fiber fabrication, the gas chemistry (**Reaction 2.1** and **Reaction 2.2**) allows void free filling through a long length from a back filling method[19].

$$SiH_{4\,(g)} \rightarrow Si_{(s)} + 2\ H_{2\,(g)} \qquad \textbf{(Reaction 2.1)}$$

$$GeH_{4\,(g)} \rightarrow Ge_{(s)} + 2\ H_{2\,(g)} \qquad \textbf{(Reaction 2.2)}$$

The only by-product from silane and germane pyrolysis for silicon and germanium HPCVD deposition is hydrogen gas, which has a small kinetic diameter of 2.89 Å[28]. During deposition temperature, from 300 °C to 500 °C, H_2 and He (carrier gases) are permeable through the amorphous silica capillary, while silane or germane remains inside the capillary. When the pore is closed, H_2 and He diffuse out of the silica capillary to increase the concentration of reactants (SiH_4 and GeH_4) to allow additional materials deposited upstream to the plug. Using HPCVD, silicon and germanium optical fibers can be made into centimeters to meters long[3,19]. The deposition method will be discussed in details in *Section 2.2.2*.

2.2.1. Kinetics of HPcCVD Si in 1D Confined Geometries

Another advantage of high pressure is its effect on the kinetics of reaction in CVD systems. Hereafter we will discuss the fabrication of hydrogenated amorphous silicon (a-Si:H) as an illustration of effect of pressure on kinetics and rate of reaction. a-Si:H is a technologically relevant material[29] for applications such as next generation solar cells[30–32] and thin film transistors[33,34]. However, there are limited methods to deposit a-Si:H with a sufficient amount of hydrogen incorporated in amorphous silicon (a-Si)[35]. To deposit silicon using CVD, silane (SiH_4)

is one of the most common reactants. A high enough temperature or energy is needed to decompose silane molecules for deposition at reasonable rates, but low temperature (< 500 °C) is required for hydrogen to passivate the dangling bonds in a-Si. Hot wire CVD[36–38] and plasma enhanced CVD[39,40] are often used. High pressure CVD can also be used to increase the rate of precursor decomposition at low temperatures[1,2,19]. It was determined from previous studies that the rate of silicon deposition using silane pyrolysis increase by 30-fold when using high pressure CVD as compared to conventional CVD at the same reaction condition. The growth rate increased from 0.01 Å/s to 0.3 Å/s in high pressure CVD at 450 °C with silane partial pressure of 13 Pa[1,19].

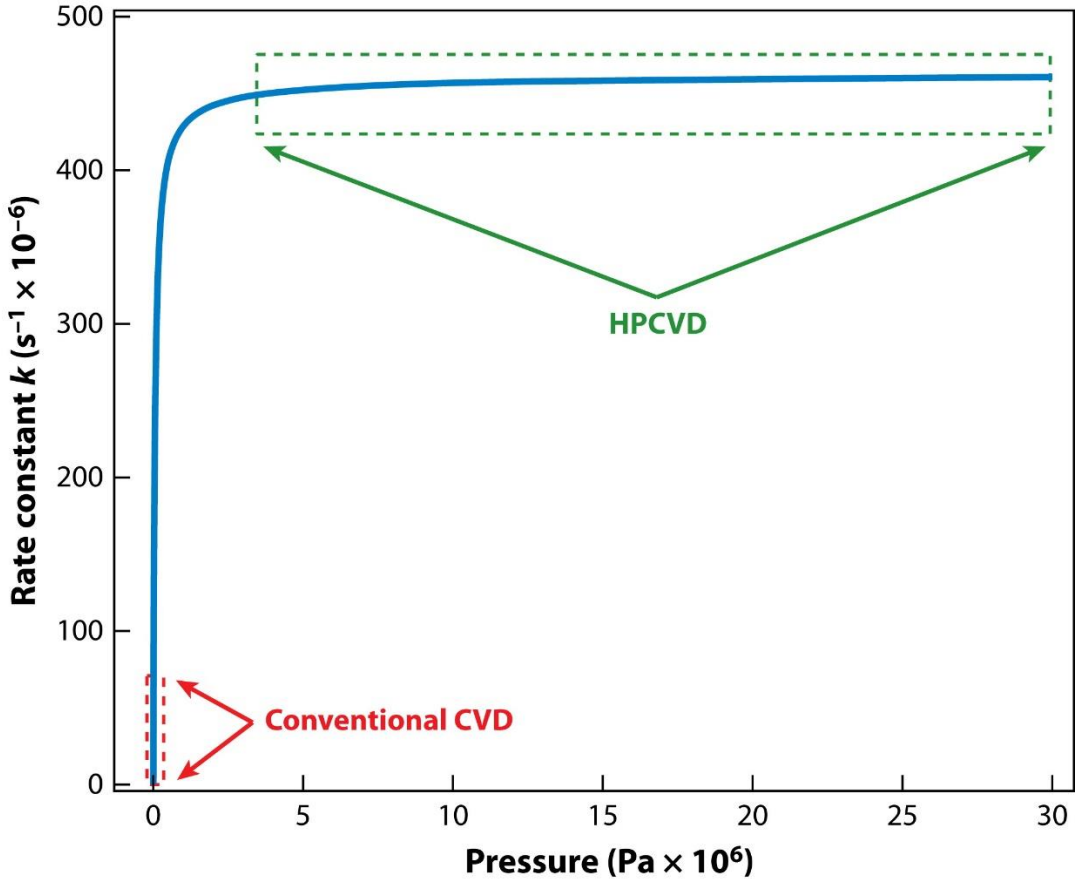

Figure 2-4. Effect of pressure on rate constant during silane pyrolysis. This plot shows the rate constant for the decomposition of silane to silylene as a function of pressure at 400 °C with He carrier gas. Reprinted with permission from Reference 7. Copyright 2018 Annual Reviews.

Silane pyrolysis is a unimolecular reaction, but it is activated by molecular collision; therefore, a high total pressure in the reactor including carrier gas can also affect the rate of reaction. Even the pressure fraction of silane does not increase significantly in high pressure CVD as compared to conventional CVD, molecular collision promoted from carrier gas (He or H_2) can also increase the rate of reaction. One of the very first step that is widely accepted for silane pyrolysis is the decomposition of silane molecules to silylene (SiH_2)[2,41,42].

$$SiH_{4\,(g)} \rightarrow SiH_{2\,(g)} + H_{2\,(g)} \qquad \textbf{(Reaction 2.3)}$$

And the rate constant can be simplified as the following,

$$-\frac{d[SiH_4]}{dt} = k\,[SiH_4] \qquad \textbf{(Equation 2.2)}$$

The decomposition rate of silane to silyene can be calculated using Quantum Rice-Ramsperger Kassel (QRRK) theory modeling (**Figure 2-4**), where the rate constant increases from $1.6 \times 10^{-7}\ s^{-1}$ at 13 Pa to $4.6 \times 10^{-4}\ s^{-1}$ at 10 MPa [2]. The rate constant increase plateaus at about 10 MPa where increase in pressure no long increase the rate constant significantly. A series of reactions then follow to create the final product of silicon (**Table 2-1** and **Table 2-2**). However, most experimental and theoretical studies are performed under low pressure and there is little known in high pressure regime. To further understand the effect of pressure on silane pyrolysis, the rate limiting step and film growth in micro-capillaries, we studied the growth of a-Si:H in 5.9 μm inner diameter silica capillaries[43].

Table 2-1. Homogeneous gas phase reaction proposed by Ho et al[44]. Reprinted with permission from Reference 43. Copyright 2017 American Chemical Society.

$$SiH_4 \leftrightarrow SiH_2 + H_2 \quad (1)$$
$$Si_2H_6 \leftrightarrow SiH4 + SiH_2 \quad (2)$$
$$Si_2H_6 \leftrightarrow H_3SiSiH + H_2 \quad (3)$$
$$Si_3H8 \leftrightarrow SiH_2 + Si_2H_6 \quad (4)$$
$$Si_3H8 \leftrightarrow SiH4 + H_3SiSiH \quad (5)$$
$$H_3SiSiH \leftrightarrow H_2SiSiH_2 \quad (6)$$
$$H_3SiSiH + H_2 \leftrightarrow SiH4 + SiH_2 \quad (7)$$
$$H_3SiSiH + SiH4 \leftrightarrow Si_2H_6 + SiH_2 \quad (8)$$
$$H_3SiSiH \leftrightarrow Si + SiH4 \quad (9)$$
$$Si + Si_2H_6 \leftrightarrow SiH_2 + H_3SiSiH \quad (10)$$

Table 2-2. Heterogeneous thermal decomposition of silane on amorphous silicon surface proposed by Gates et al[45, 46]. Reprinted with permission from Reference 43. Copyright 2017 American Chemical Society.

$$SiH_4 + 2* \xrightarrow{k_1} SiH_3^* + H^* \quad (1)$$
$$SiH_3^* + * \xrightarrow{k_2} H^* + SiH_2^* \quad (2)$$
$$2SiH_2^* \xrightarrow{k_3} H_2 + 2SiH^* \quad (3)$$
$$2SiH^* \xrightarrow{k_4} H_2 + 2Si^* \quad (4)$$
$$2H^* \xrightarrow{k_5} H_2 + 2* \quad (5)$$
$$Si^* \xrightarrow{k_6} Film + * \quad (6)$$

Silicon deposition on a surface could result from either homogeneous or heterogeneous mechanism. In homogeneous mechanisms[41,42,44,47–49], silane molecules decompose in gas phase to form higher order silanes (such as disilane, Si_2H_6 or trisilane, Si_3H_8) or silyenes. These intermediates are then absorbed onto the surface to further decompose to Si semiconductor. In contrast, silane molecules are first absorbed onto the surface to decompose on or near the surface in heterogeneous reactions[50,51] (**Table 2-1**). The dominating mechanism in silicon film growth using silane pyrolysis varies depending on reaction conditions, including temperature, pressure, silane concentration and surface to volume ratio of the deposition zone[52,53].

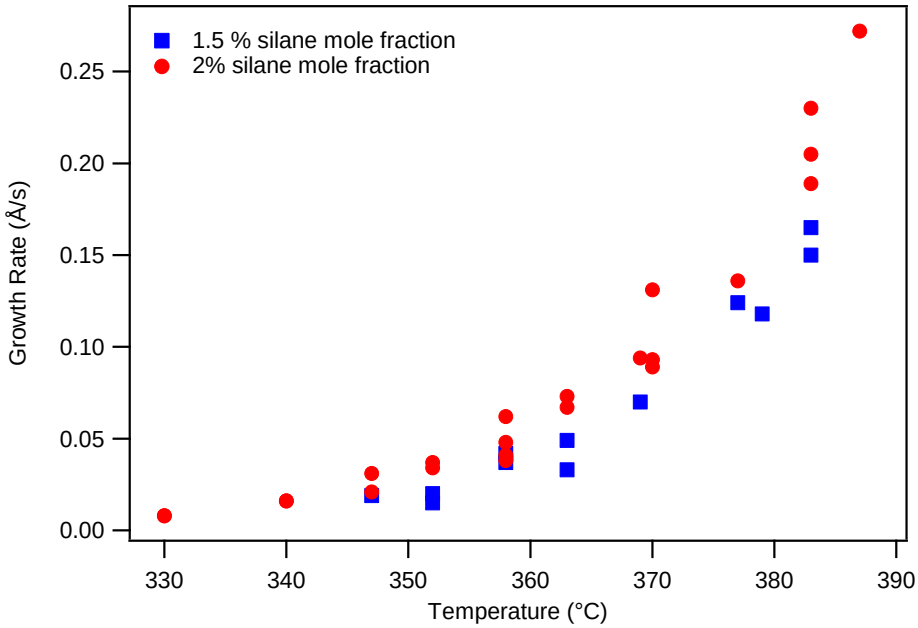

Figure 2-5. Silicon growth rate in 5.9 μm silica capillary with varying temperature and silane mole fraction. Reprinted with permission from Reference 43. Copyright 2018 American Chemical Society.

The growth rate of a-Si:H in silica capillary (**Figure 2-5**), a high surface to volume ratio template, can be related to the film thickness (δ), silane mole fraction (α), precursor pressure (P), reaction time (t), reaction rate constant (k), temperature of deposition (T), molecular weight (M_w) and density (ρ) of a-Si:H as the following,

$$\frac{d\delta}{dt} = k\alpha\left(\frac{M_w P}{\rho RT}\right) \qquad \textbf{(Equation 2.3)}$$

assuming the gas mixture to be ideal gas like and silane decomposition reaction to be first order with respect to silane concentration. The activation energy can then be determined using an Arrhenius plot (**Figure 2-6**). The activation energy was found to be E_0 = 53.7 $\pm$2.9 kcal/mol and pre-exponential factor was 1.5 x 10^{10} m/s. The predicted activation energy agrees with hydrogen desorption reactions in heterogeneous silane pyrolysis[54,55] (k_3, k_4 and k_5 in **Table 2-1**), suggesting that the rate limiting step in HPCVD of a-Si:H is the desorption of hydrogen from the surface, where parting of hydrogen allows more sites for silane molecules to stick onto the

surface. In conjunction with reactive molecular dynamics simulations using ReaFF at 7 MPa and 400 °C of silane molecules on silicon, it was determined that heterogeneous thermal decomposition of silane at the amorphous silicon surface is the dominant mechanism for deposition of a-Si:H in HPCVD of silicon micro-wires. This is because the silica capillary has high surface area relative to its volume. The capillary, or micro-reactor, creates a confinement effect limiting homogeneous gas phase reaction for particle nucleation. Kinetics studies of 2D thin film using HPcCVD will be discussed later in this chapter.

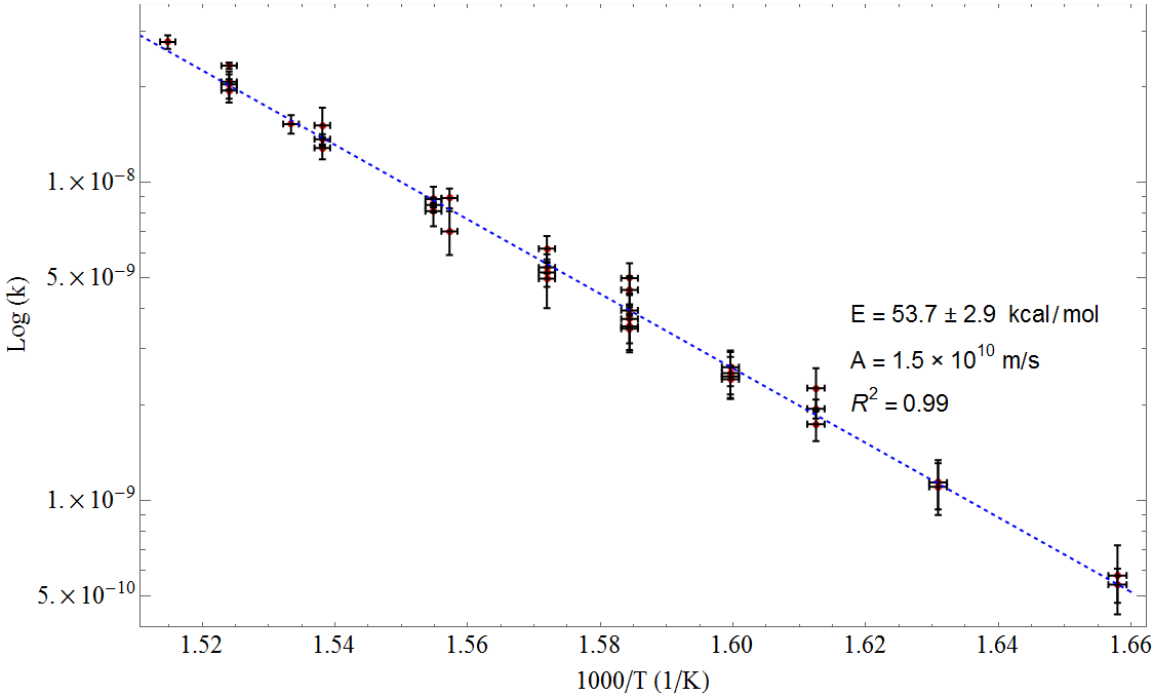

Figure 2-6. Arrhenius plot for the surface reaction rate constant in relation to furnace temperature. Reprinted with permission from Reference 43. Copyright 2018 American Chemical Society.

2.2.2. HPCVD and Reactor Confinement in 1D Geometries

The major difference between conventional CVD (1 - 130 Pa in low pressure CVD and 0.1 MPa in atmospheric pressure CVD) and high pressure CVD (35 – 70 MPa) is the total pressure used inside of a reaction chamber. Reactor geometries must also be considered in high

pressure CVD because the increase in pressure also promote gas molecular collision, thus activating reactions at lower temperature than expected. In addition, high pressure encourages gas phase nucleation (homogeneous reaction) if the open volume inside of reactor is too large[2]. As discussed in a previous section, HPCVD of a-Si:H in 5.9 μm silica capillaries was found to be heterogeneous surface film growth. Previous studies on varying the inner diameter silica capillary in high pressure CVD show that particle growth occurs when the inner diameter is larger than 300 μm (**Figure 2-7**).

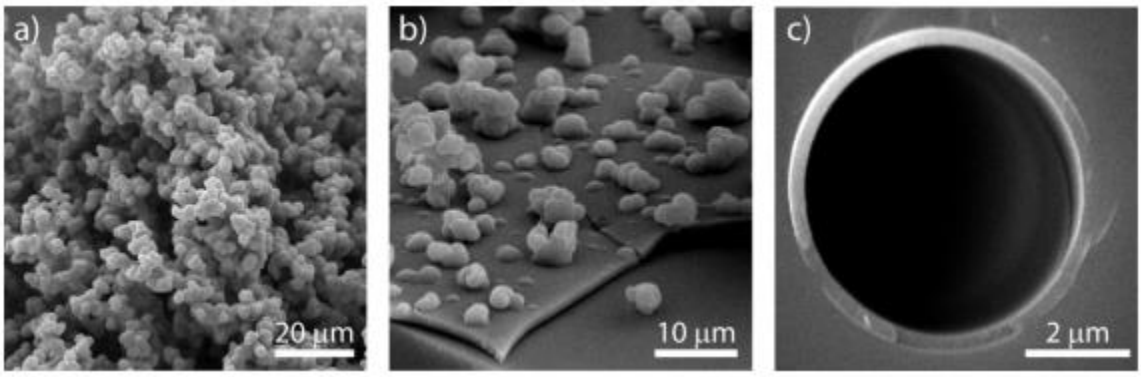

Figure 2-7. HPCVD of Si in silica capillaries of decreasing inner diameter. a) Homogeneous gas phase particle formation is the dominating process when the silica capillary has an inner diameter of 2.5 mm. b) At 1 mm inner diameter capillary, a thin film starts to form at the surface, but particle formation can still be observed. c) When the inner diameter of capillary is kept below 300 μm, heterogeneous film growth is the dominating process, where only uniform film can be observed on the inner surface of the capillary after HPCVD. Reprinted with permission from Reference 2 and 7. Copyright 2018 American Chemical Society and Annual Reviews.

In 1D geometries, the advantage of using silica capillary as a template is that the silica capillary can serve as a micro-reactor, where precursor gas molecules are directly transferred from a larger gas mixture volume into the inner pore of silica capillary. **Figure 2-8** shows a schematic of a typical experimental set-up for HPCVD of 1D micro-wires using silica capillaries. The silica capillary is connected to 316 stainless steel high pressure rated parts for easy transfer of precursor gas into the open pore. 316 stainless steel is used to prevent hydrogen embrittlement

during experiments at high pressure and high temperature. Hydrogen is sometimes used as a carrier gas and is also a by-product in many CVD reactions, especially when hydrides are used. The experimental set-up is connected to a precursor gas reservoir, an ultra-high purity helium gas line for purging and a vacuum line for air and inert gas evacuation. Before deposition, a dry scroll pump is used to remove any air, gas or moisture contaminants from the experimental set-up. A silica capillary with an inner diameter from nm to μm is then placed inside of a home built electric resistance tube furnace. Multiple capillaries can be placed inside of an experimental set-up for mass production. Resistive wires are used as the heating element; the wire provides resistance to the passage of the electrical current and heats up as a response to the applied current. A heating profile can be created along the length of the furnace depending on the build of the furnace and the goal of the experiment.

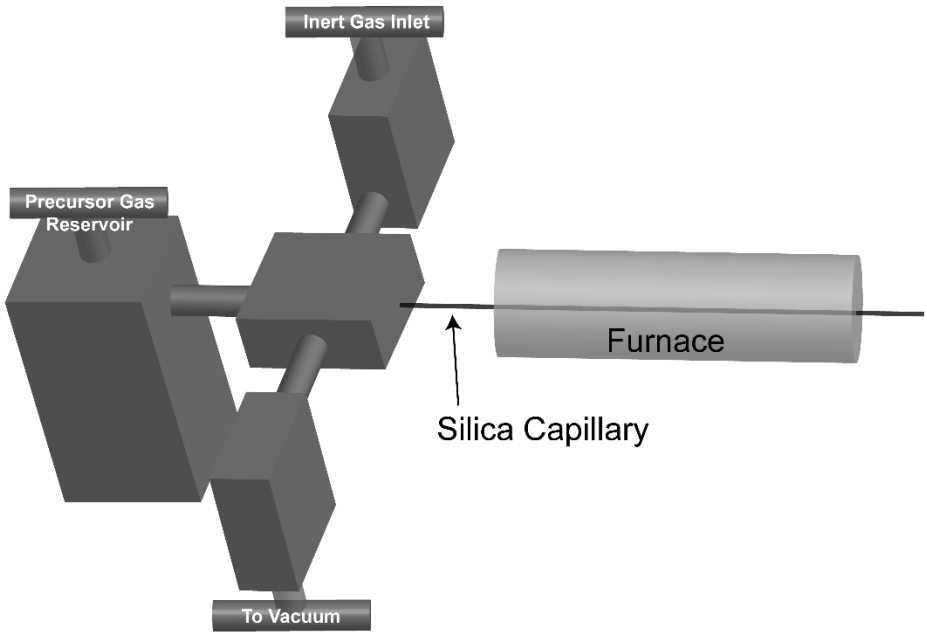

Figure 2-8. Schematic of HPCVD experimental set-up. The silica capillary is connected to a high pressure rated stainless steel set-up for transfer of precursor gas into the inner pore. The experimental set-up is connected to an ultra-high purity inert gas line and vacuum line for gas purging before start of reaction to evacuate air.

The temperature inside of the furnace is measured using a k-type thermocouple (chromel-alumel) and the amount of voltage sent to the resistive wires is controlled by a proportional-integral-derivative (PID) controller. The PID controller records the temperature is measured by the thermocouple and adjust the voltage as it tries to match the measured temperature to the set temperature. The thermocouple measures temperature using the thermoelectric effect of two different conductors, translating temperature dependent voltage to temperature. The temperature of the heated furnace is kept within $\pm$ 0.01 °C of the set temperature using a PID controller. The deposition temperature varies and is determined by the materials quality of the final product. For example, amorphous silicon is deposited below 520 °C and crystalline silicon is deposited above that temperature with silane pyrolysis. In addition, a lower temperature, 200 °C to 450 °C is needed for hydrogenated amorphous silicon and deposition temperature varies depending on carrier gas and amount of hydrogen incorporation needed in the final product.

After evacuation and pre-heating of the silica capillary, precursor (for example, silane, SiH_4 for Si) and carrier gas (helium or hydrogen) are introduced into the experimental set-up and the silica capillary. Deposited materials' quality depend greatly on precursor gas purity. We will discuss transfer of gases from stock electronic grade gas tanks to smaller volume reservoirs in *Section 2.4*. When the gas mixture passes through the heating zone, materials can deposit onto the surface (**Figure 2-9**). By products such as hydrogen for the case of silane and germane pyrolysis, and excess reactants are release through the outlet. As time progresses during the deposition, a thicker layer of material is deposited onto the surface; eventually, the entire heated length of silica capillary can be deposited with materials void free.

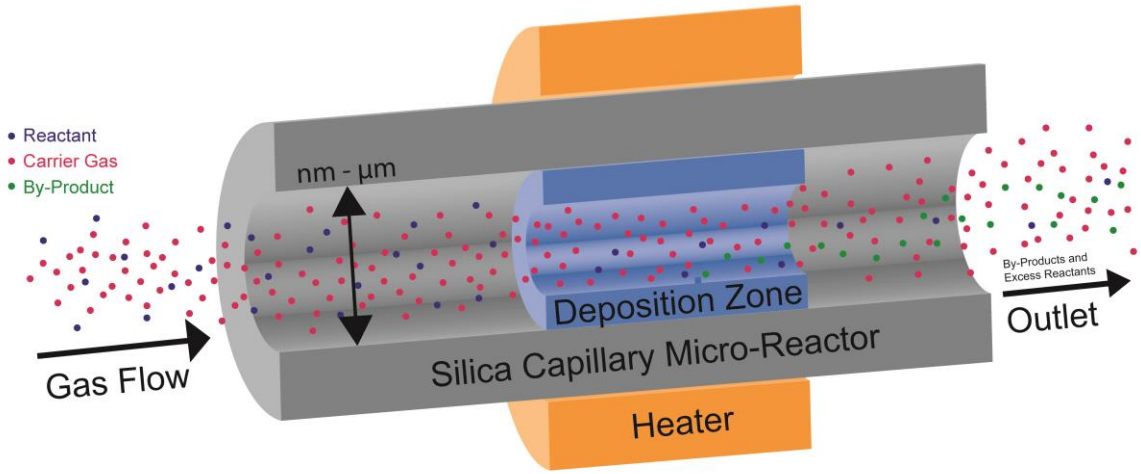

Figure 2-9. Schematic of 1D HPcCVD micro-reactor using silica capillaries. Precursor gas and carrier gas (helium or hydrogen) are sent into the silica capillary micro-reactor for deposition of semiconductors in 1D geometries.

2.3. High Pressure Chemical Vapor Deposition in 2D and 3D Geometries

High pressure alters gas dynamics, diffusion, reaction kinetics and thermodynamics in CVD chemistry, providing a way to deposit materials in small pores and lowering the temperature needed to decompose gas precursors. HPCVD with confinement can also be used to fabricate large area silicon, amorphous silicon and hydrogenated amorphous silicon for thin film solar cell purposes[5]. a-Si:H thin film is one of the candidates for next generation high performance solar cell materials. However, synthesis and fabrication of such materials in large area could be challenging. As discussed in *Section 2.2.1*, a-Si:H can be prepared with methods such as plasma-enhanced CVD (PECVD)[39,40] or hot wire CVD (HWCVD)[36–38]. PECVD requires a complex electronic system and large reactor to generate uniform plasma across a large region to decompose silane for uniform deposition over a large area. HWCVD requires precise control over the heating filament, alloying complexes and contaminants elimination. On the contrary, high pressure CVD provides a method to decompose silane at low temperature for hydrogen

incorporation with reasonable rate of deposition, and does not require a complex system like PECVD and HWCVD.

The previous section discussed the use of high pressure in 1D geometries where semiconductors such as silicon and germanium are deposited inside the pore of a silica capillary. Silica capillary is a high surface area to volume ratio (SVA) template, which has a SVA of 4/*d*, where *d* is the diameter of the silica capillary (**Figure 2-10**). When the diameter of the capillary is maintained below 300 µm while the length can be centimeters to meters long, heterogeneous gas phase reaction is the dominating process, where reactant gas molecules must land onto a surface before it can further decompose to silicon. The reactor geometry in 1D tubes prevent particle nucleation in gas phase (homogeneous reaction mechansium). This technique used to promote film growth and suppress particle growth can be applied to planar (2D) and three-dimensional (3D) materials fabrication.

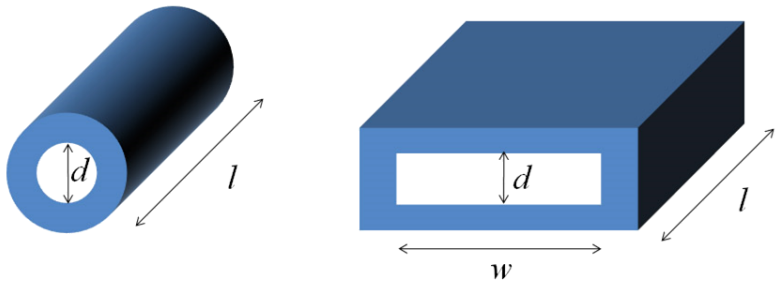

Figure 2-10. Confinement of planar substrate compared to confinement in 1D templates. The surface area to volume ratio is defined as 4/*d* in silica capillary (left). The surface area to volume ratio in a planar substrate is 2/*d* (right). If same confinement effect in silica capillary applies to planar, uniform thin film is possible on planar substrate if *d*, the distance between two substrates is constrained.

Surface area to volume ratio (SAV) inside of a planar substrate can be determined by its deposition area and the empty distance between two substrates (**Figure 2-10**). If the SVA of a planar reactor is comparable to that of silica capillary, heterogeneous film growth should be favored. For example, the SAV of a 300 µm silica capillary for a length of 10 cm is

$1.3 \times 10^4\ m^{-1}$, the equivalent spacing between deposition zone in a planar reactor would be 150 µm. Since the length and width does not affect the surface area to volume ratio of a planar reactor, theoretically, we can deposit a uniform thin film onto a planar substrate as large a planar reactor would allow, as long as all open dimensions inside of the reactor is limited.

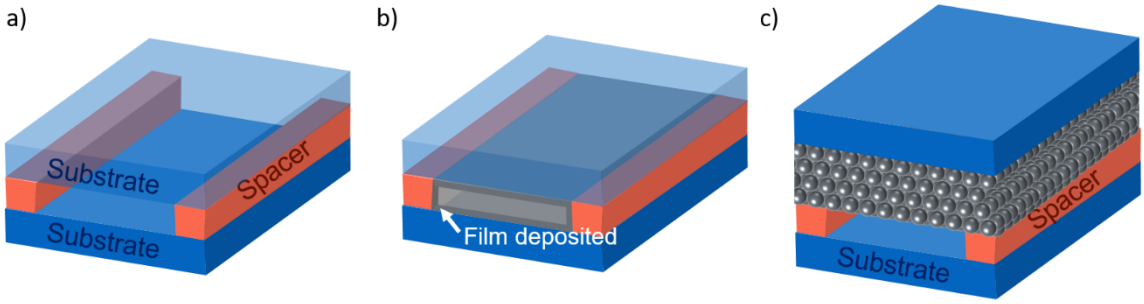

Figure 2-11. Schematic of 2D and 3D deposition zone geometry. (a) The spacing (*d*) between two substrate is controlled by using stainless steel spacers of a fixed thickness, films are then deposited onto the surface in (b). A templated substrate such as in (c) can be used for 3D materials fabrication. Discussion on templates such as in (c) to fabricate metalattices will be in *Chapter 3*.

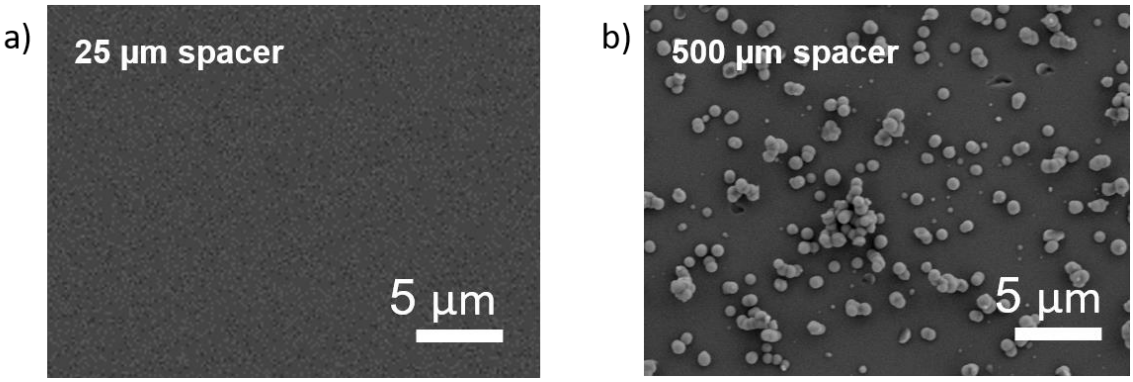

Figure 2-12. SEM images showing effect of reactor confinement in 2D/ 3D geometries. (a) When the spacing between two polished silicon wafers is confined using a 25 µm thickness spacer, a uniform thin film is deposited onto the surface, whereas when the spacing is kept at 500 µm, heterogeneous film growth is no longer the only deposition mechanism and particle growth can be observed.

The spaces in between two substrate determines if heterogeneous film formation is the main process. To control the spaces between two substrates, or deposition zones, a spacer made of stainless steel with a fixed thickness is used to separate the two surfaces (**Figure 2-11**). After

introduction of precursor gases, a thin film can then be deposited onto the surface. The thickness of the spacer is crucial in determining if homogeneous particle formation can be suppressed. For example, in **Figure 2-12**, when the spacer is at 500 μm with a SAV of only $4 \times 10^3\ m^{-1}$ in a silicon deposition using silane pyrolysis on a polished silicon wafer surface, particle growth can be observed because the reactant gas and reaction intermediates have time to nucleate and grow to form particles in gas phase before being absorbed onto the surface, similar to previous high pressure studies[48]. When a 25 μm spacer is used, with a SAV of $8 \times 10^4\ m^{-1}$, only film growth can be observed.

2.3.1. Reactor Confinement in 2D and 3D Geometries

In addition to confinement between substrates, confinement inside of a reactor is also important in reducing particle growth. In conventional CVD, there are two methods of heating a CVD reactor, one is to heat only the deposition substrate (cold wall reactor) and the other is to heat the entire reactor (hot wall reactor). A cold wall reactor can prevent pre-mature gas molecule decomposition before the precursors reach the deposition zone, which ideally would be preferred for high pressure CVD systems. However, for safety reasons, high pressure rated parts generally have a very small volume to prevent rupture and explosion at elevated temperatures. Therefore, an internal heater engineered into the inside of a reactor is more challenging. In addition, it is more difficult to prevent film growth on an internal heating element itself because high pressure gases, including reactants and carrier gas, can penetrate into small pores to deposit materials in the electronics and thus affect the heater performance overtime. Most high pressure reactors are made of stainless steel which adds additional complexity in designing a heater internally because it is both thermally and electrically conductive. For all of the above reasons, all high pressure CVD reactors in the discussion of this dissertation, including 1D, 2D and 3D

materials fabrication, are made with a hot wall reactor using an external electric resistance furnaces. A cold wall reactor would assist in fabrication of certain materials (such as epitaxy growth of single crystalline silicon) and could allow materials that are currently limited in HPcCVD. Future efforts should investigate this feasibility.

Figure 2-13 shows an illustration of a 2D/ 3D non-flowing high pressure confined chemical vapor deposition (HPcCVD) reactor. The reactor is machined and designed using high quality 316 stainless steel to minimize hydrogen embrittlement at elevated temperature. The sample holder fits tightly inside the high pressure reactor to prevent homogeneous particle growth. A groove is engraved on the bottom of the sample holder for mass transport of gas mixtures toward the deposition zone. For silane and germane pyrolysis, or most other hydride precursor decompositions, a closed non-flowing reactor such as in **Figure 2-13** can be used because the only by-product is hydrogen gases. Hydrogen has a small kinetic diameter of 2.89 Å[28], which can diffuse through most substrates and templates such as amorphous silica (pores as from 3 – 5 Å).

Experimental set-up (**Figure 2-14**) and deposition procedures for 2D and 3D materials using HPcCVD is very similar to 1D systems, except a stainless steel reactor is used instead of a silica capillary micro-reactor. First, the samples are assembled in the sample holder such as in **Figure 2-13**. The stainless steel spacer is configured in a U-shape or as two parallel strips (**Figure 2-11**) in between the substrate or deposition zone to maximize empty surfaces for materials deposition. The sample holder can be replaced by a rolled up flexible substrate and the furnace length can be extended if large area deposition is needed. After placing the sample holder with deposition substrate into the reactor, the reactor is connected to the experimental set-up as shown in **Figure 2-14**. The same procedure of ultra-high purity inert gas purging reported in *Section 2.2.2*. then follows to remove air, moisture and contaminants in the reactor. The

reactor is pre-heated to 150 °C to 200 °C in vacuum before precursor gases are let into the reactor.

After deposition, residual gas and by-products are vented out of the system.

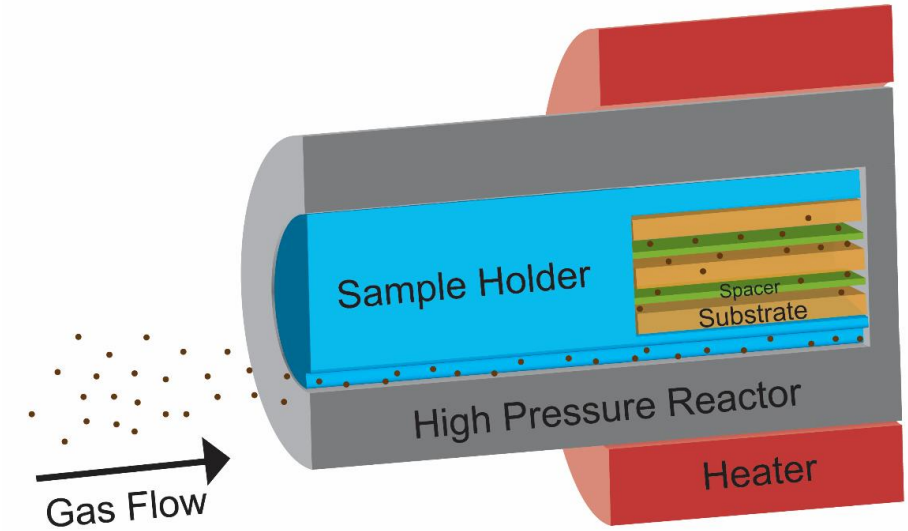

Figure 2-13. Schematic of 2D/ 3D high pressure confined chemical vapor deposition reactor. The reactor is made of high pressure rated 316 stainless steel. Inside of the reactor, samples are contained in the sample holder (blue). A small grove is machined on the bottle of the sample holder to allow precursor gas transport near the heated region. All of the open spaces inside of the reactor is confined to minimize homogeneous particle growth. The largest opening in a high pressure reactor is the groove for precursor gas transfer.

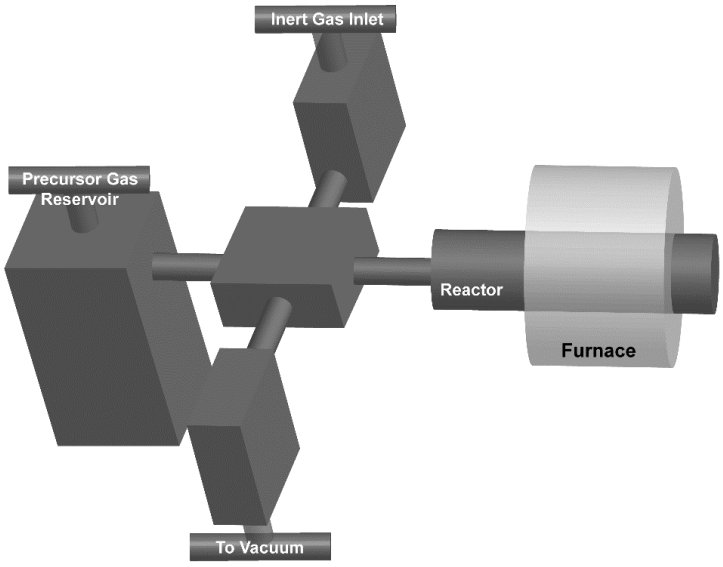

Figure 2-14. Schematic of 2D/ 3D high pressure confined chemical vapor deposition experimental set-up.

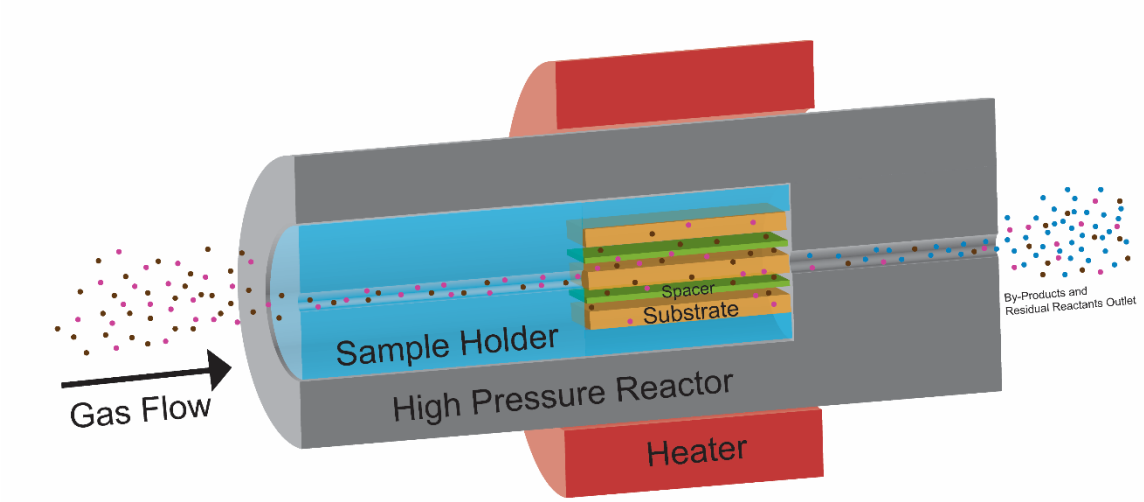

Figure 2-15. Schematic of a 2D/ 3D high pressure confined chemical vapor deposition flowing reactor. The pore for gas transport is located in the middle of the sample holder for direct flow of precursor gas toward the substrate. A small opening after the substrate is added to allow for by-products and residual reactants exhaust. In addition, a silica capillary can be attached to the outlet, where different inner diameters and lengths of capillaries can be used to control flow rate of exhaust.

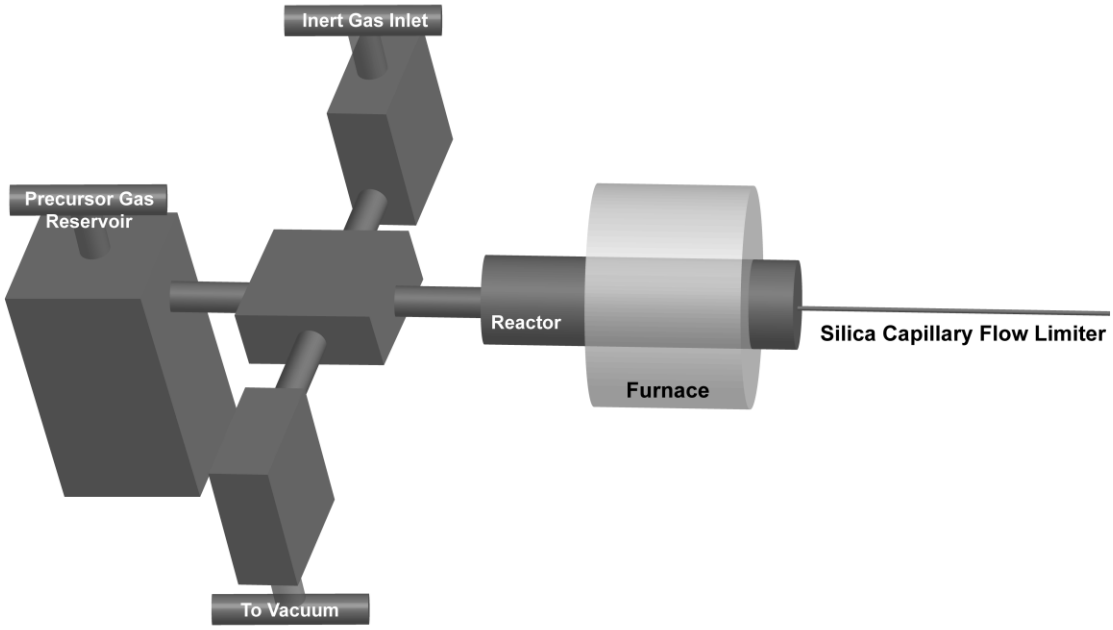

Figure 2-16. Schematic of a 2D/ 3D high pressure confined chemical vapor deposition experimental set-up with a flowing reactor, where exhaust of by-product is required for continuous deposition.

When the by-product is too large to permeate through deposited materials and the substrate and removal of by-products is needed for additional reactants to flow toward the deposition zone, a flowing reactor (**Figure 2-15**) is needed to promote continuous film growth. A flowing reactor ensures by-products can leave the reactor as they build up during precursor decomposition and are carried out of the deposition zone at a reasonable rate by high pressure carrier gas; more reactants can then enter into the reactor and decompose near the deposition zone. In addition, the sample holder geometry inside of a flowing reactor is different from the non-flowing reactor, so the gas mixture can flow directly onto the surface of the deposition substrate. We will discuss the effect of sample holder and spacer geometry in *Chapter 4* for materials deposited using organometallics compounds as the reactants. A silica capillary is connected at the exhaust of a flowing reactor to control the flow rate of by-products and residual gas mixture. For example, assuming gas flow through a silica capillary by hydraulic flow and laminar flow condition exists, we can describe the total flow rate (Q_h) by the Poiseuille equation[56],

$$Q_h = \frac{\pi \Delta p R^4}{8 \eta L} \qquad \textbf{(Equation 2.4)}$$

Where Δp is the pressure, R is radius of the capillary, η is viscosity of the material flowing through the capillary and L is the length of the capillary. For a 5 μm inner diameter capillary with a length of 15 cm at 70 mPa, the flow rate of hydrogen gas at 400 °C (furnace set temperature) is 37.86 cm^3/s. When the silica capillary exhaust tube is replaced by a 10 μm inner diameter pore, flow rate is increased to 605.7 cm^3/s under the same condition. Size selection of the exhaust tube also depends on the initial and targeted final pressure, reaction rate and reaction duration. A larger inner diameter silica capillary has a higher flow rate, hence faster release of reactant gas mixture and can drain the high pressure reservoir earlier and exhaust more residual gas if there is not enough time for reactants to decompose at or near the heating zone. The experimental set-up

using a flowing reactor (**Figure 2-16**) is very similar to non-flowing reactor, with the difference of having a flow limiting silica capillary attached to the end.

2.3.2. Kinetics of HPcCVD Si in 2D Geometries

To further understand the role of pressure in high pressure confined chemical vapor deposition (HPcCVD), we studied the kinetics of silane pyrolysis using a 2D flowing reactor. A flowing reactor was used instead of a non-flowing reactor to eliminate mass transport limitations to maintain a constant silane concentration inside the reactor. Since a 2D flowing stainless steel reactor is used, we can assume that the deposition zone has a uniform temperature controlled by a PID controller. In collaboration with Dr. Seyed Pouria Motevalian, Penn State Chemical Engineering, and Dr. Stephen Aro, it was determined numerically that gas flow inside of a silica capillary (1D) and 2D confined thin film are both laminar and subsonic. To determine the reaction rate of 2D confined geometries using HPcCVD silane pyrolysis, we studied the film thickness at various temperatures, pressures and reaction times (**Table 2-3**) with 9.4 % silane in helium carrier gas.

Table 2-3. Experimental conditions for 2D thin film kinetic studies.

Temperature (°C)	Time (Minutes)	Initial Pressure (psi)	Final Pressure (psi)	Film Thickness Measured by Profilometry (nm)
390	120	3833	3353	43
390	120	3269	2868	44
380	300	2843	2495	89
400	110	2433	2172	84
410	80	2157	1926	65
420	70	1918	1724	89

The spacer geometry is made into two linear strip along the direction of flow to prevent blockage of gas traveling toward the exhaust. The reaction was quenched immediately by release

of residual precursors from the experimental set-up after the set reaction time. A micro-scaled pattern was put onto the surface of the deposited substrate to create a height difference for film thickness measurements (**Figure 2-17**). Hard contact lithography was done using Karl Suss MABA6 and Megaposit™ SPR™ 955-CM (photoresist). After developing the photoresist, the samples were placed inside of a reactive ion etcher to remove the un-patterned HPcCVD a-Si:H using chlorine radicals in Plasma-Therm Versalock. Before film thickness characterization, the developed photoresist was removed using NANO™ REMOVER PG.

The film thickness was determined by optical profilometry using the Zygo Nexview™ 3D Optical Surface Profiler. The detection limit of the profiler is $\pm$ 5 nm. The film thickness is measured by determining the wavelength difference between the incident light projected toward a reference mirror and the light projected toward the sample. When the two beams recombine before the detector, the degree of interference between the two beams give rise to information of surface contours of the measured film. Optical profilometry was found to be the most effective and accurate way of measuring the thin film thickness, as other techniques, such as scanning electron microscope and ellipsometry require careful polishing of the sample to view the side and knowledge of refractive index of the film, respectively. All film thickness measurements were done using the pattern near the center line of the film to eliminate edge effects.

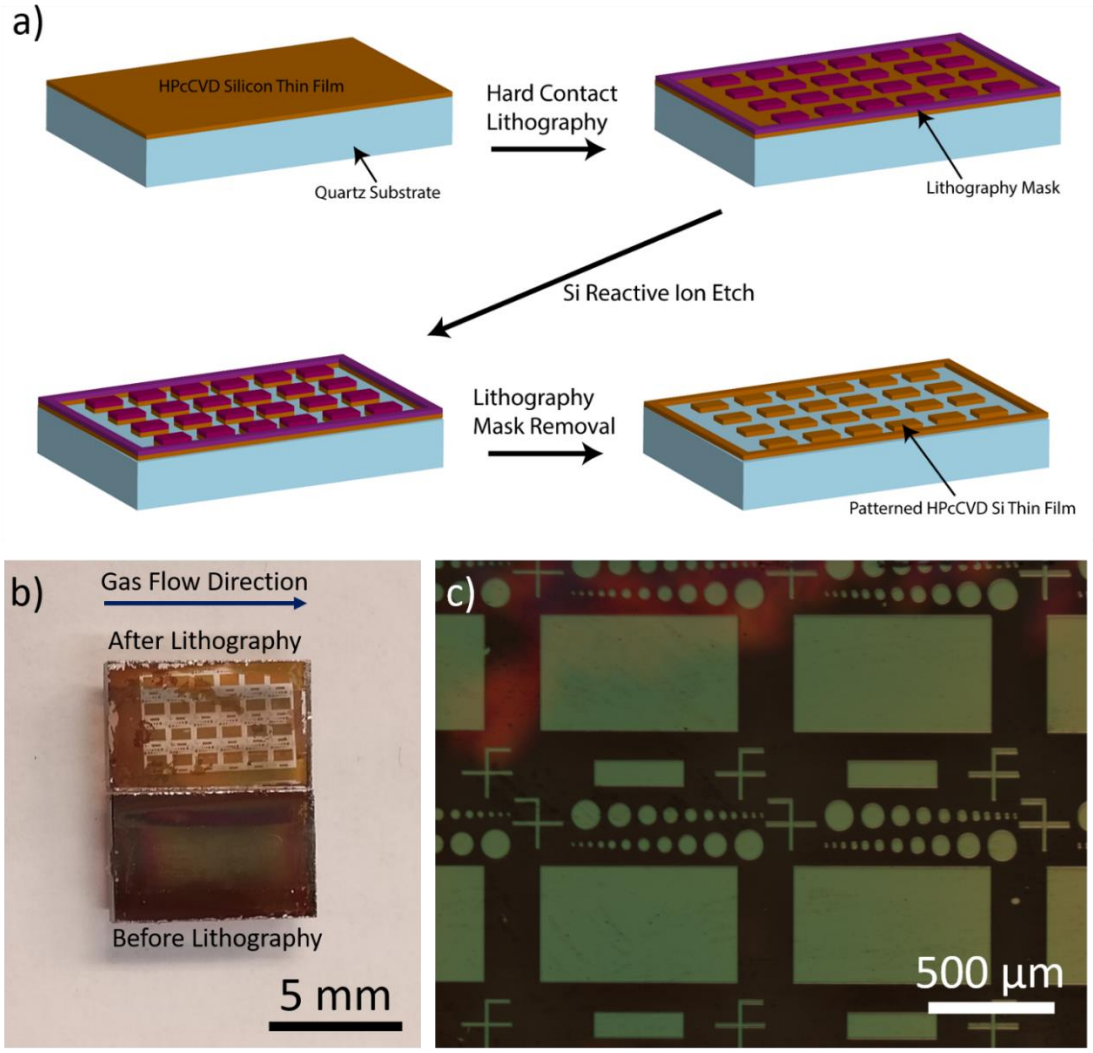

Figure 2-17. Lithography process for HPcCVD silicon thin film thickness measurements. (a) Schematic of lithography processes. Hard Contact lithography using Megaposit™ SPR™ 955-CM photoresist. After developing the photoresist, reactive ion etch using chlorine gas is used to remove the silicon layer that was not protected by the mask. The mask is then removed using NANO™ REMOVER PG prior to film thickness measurement using optical profilometry. (b) Optical image of as deposited film before and after lithography, film thickness is measured relative from 0.5 – 0.7 of the flow direction (start of the flow is 0 and end of flow is 1). (c) Zoomed in microscope image of pattern.

Under HPcCVD 2D reactor conditions, the film thickness axial variation (**Figure 2-18**) along the path of gas flow was found to be within the detection limit of the profiler, $\pm$ 5 nm.

Film thickness for each set of experimental conditions was determined by an average of 3

profilometry measurements. The activation energy extracted from the Arrhenius plot (**Figure 2-19**) was found to be $48.8 \pm 23.3\ kcal/mol$ and pre-exponential factor was found to be $2 \times 10^7 m/s$, which again agrees with the range of reported values for heterogeneous silane pyrolysis[54,55] as stated in *Section 2.2.2.* Hydrogen desorption from the surface to produce new dangling-bonds for additional precursor gas absorption is believed to be the rate limiting step in a-Si:H using high pressure 2D confined chemical vapor deposition reactors.

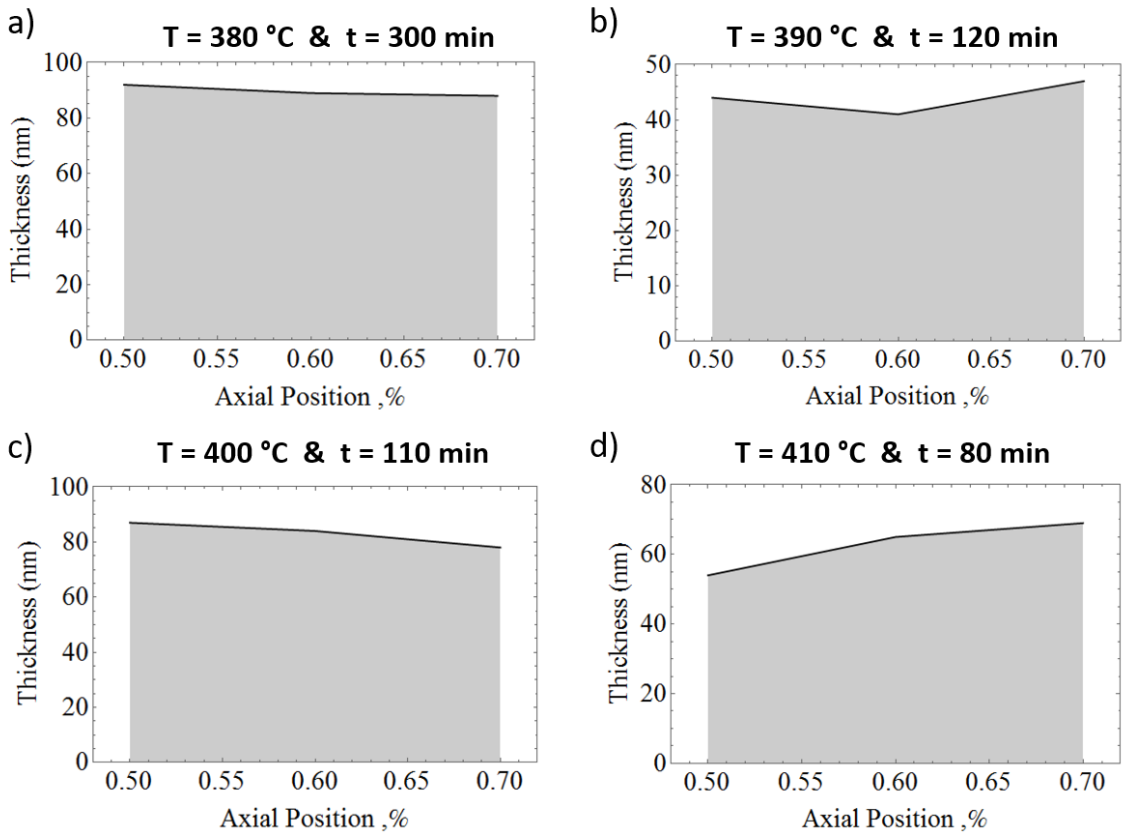

Figure 2-18. Axial variation of film thickness in 2D flowing reactor at various deposition temperature and reaction time. Axial position is relative to flow direction, where 0 is beginning of the flow and 1 is at the end of the sample. Credit: Seyed Pouria Motevalian

The standard deviation of activation energy found in the 2D systems is much higher than of silica capillary systems. In addition, the R^2 value is lower, at 0.9 (Figure 2-19). Additional experiments at other temperatures, pressures and times are needed to improve the data set where

incoming graduate students will continue the efforts in understanding silane pyrolysis at high pressure. Moreover, silane pyrolysis at high pressure in 3D geometries, such as metalattices should be investigated to understand the HPcCVD infiltration mechanism.

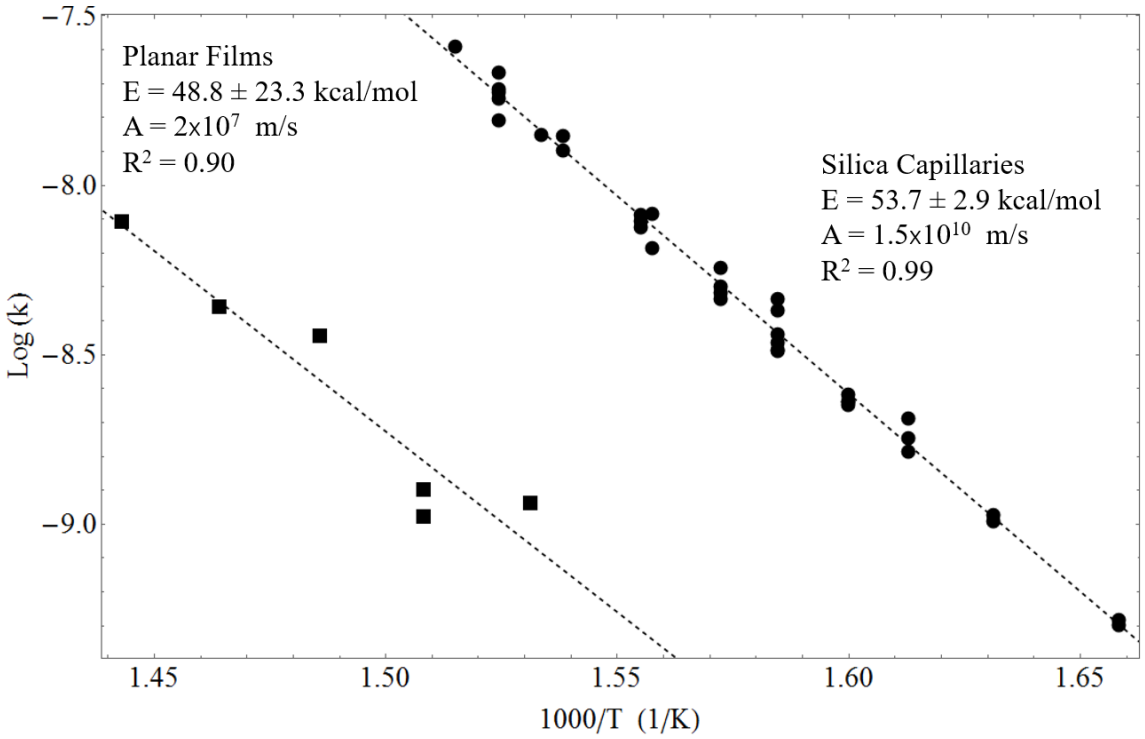

Figure 2-19. Arrhenius plot of surface reaction rate versus deposition temperature of HPcCVD 1D wires and 2D thin films. Credit: Seyed Pouria Motevalian.

2.4. High Purity Materials using HPcCVD

The quality of materials deposited using chemical vapor deposition systems depends greatly on the purity of precursor gas mixtures. Most electronic grade purity precursor gas comes with 99.999% purity, but any transfer of gas from one tank to another container could introduce gas, liquid or solid impurities into the gas mixture leading to decreased purity of the final product. In high pressure CVD systems, a smaller gas container is used to generate high pressure and to

lower risk of catastrophic explosion at high pressure. A gas transfer or loading system consists of both an ultra-high vacuum for contaminates removal and a high pressure pump for high pressure gas generation. Since there are no commercially available products with ultra-high vacuum and high pressure co-existing in a single system, a home built gas loading system (**Figure 2-20**) was designed and built by two previous member of the Badding research group, Dr. Derek Keefer and Dr. Stephen Aro.

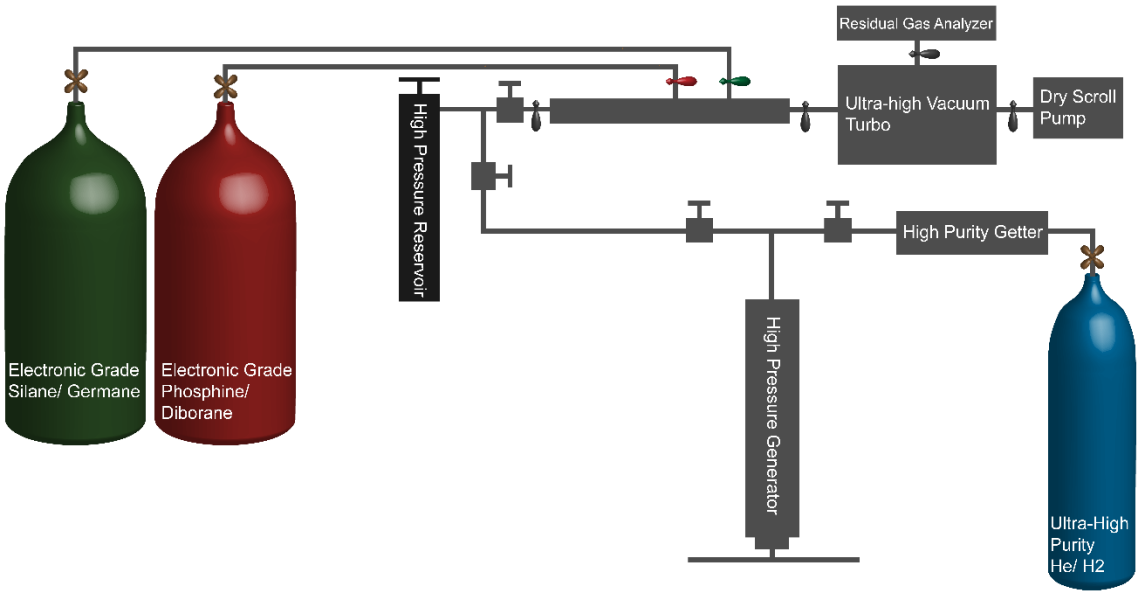

Figure 2-20. Schematic of high purity gas loading line used to prepare high pressure gas mixture. Electronic grade precursors and ultra-high purity carrier gas (H_2 or He) are transported into a high pressure reservoir in a home built gas loading system to ensure purity of gas mixture. The system contains both an ultra-high vacuum turbo to evacuate any impurities and high pressure generator to increase the total pressure of the gas mixture.

The gas loading line has access to both an ultra-high vacuum and a high pressure generator. Transfer of precursor gas begins with attachment of all gas containers, including a high pressure reservoir and electronic grade gases. For example, for silicon deposition using silane pyrolysis, a silane tank is attached to the loading line. The system, except electronic grade

gas tanks, is then open to the ultra-high vacuum pump and the entire loading line is heated for a minimum of 1 hour or until it reach a baked pressure of low 10^{-8} torr, measured by a hot filament ionization gauge. After baking, the loading line is cooled to room temperature in ultra-high vacuum to prevent precursor gas decomposition during transfer. Electronic grade precursor gases are transferred into a high pressure reservoir using cryogenic condensation. Precursor gas is first loaded into the intermediate zone with a fixed volume (unlabeled grey box in the center of **Figure 2-20**). The high pressure reservoir is then cooled using liquid nitrogen to condense precursor gas into the reservoir. Multiple cycles are needed for higher concentrations of precursor to carrier gas ratio. The high pressure reservoir will be warmed up to room temperature before adding high pressure inert carrier gas. A manual high pressure generator is used to pump carrier gas, hydrogen or helium, to suitable pressure of 35 – 70 MPa for deposition. A manual pump is used instead of an electric hydraulic pump to prevent contact between carrier gas and oiled machine parts. Finally, carrier gas is transferred into the high pressure reservoir for deposition.

The purity of as-deposited materials, such as a-Ge optical fiber in silica capillary, using the home built high pressure gas loading system has been analyzed using electron probe micro-analyzer (EPMA)[20]. When an electron beam is projected onto a material, the electron is absorbed by the material and it can emit characteristic x-ray that corresponds to different element. The as deposited materials contains only germanium, and no other impurities, such as nitrogen and chorine can be detected at the detection limit of the instrument (~100 pm).

2.5. References

1. Sazio, P. J. A. *et al.* Microstructured Optical Fibers as High-Pressure Microfluidic Reactors. *Science (80-.).* **311,** 1583–1586 (2006).
2. Baril, N. F. *et al.* Confined high-pressure chemical deposition of hydrogenated amorphous silicon. *J. Am. Chem. Soc.* **134,** 19–22 (2012).
3. He, R. *et al.* Silicon p-i-n junction fibers. *Adv. Mater.* **25,** 1461–1467 (2013).
4. Sparks, J. R. *et al.* Selective Semiconductor Filling of Microstructured Optical Fibers. *J. Light. Technol.* **29,** 2005–2008 (2011).
5. He, R., Day, T. D., Sparks, J. R., Sullivan, N. F. & Badding, J. V. High Pressure Chemical Vapor Deposition of Hydrogenated Amorphous Silicon Films and Solar Cells. *Adv. Mater.* **28,** 5939–5942 (2016).
6. Sparks, J. R. *et al.* Conformal Coating by High Pressure Chemical Deposition for Patterned Microwires of II-VI Semiconductors. *Adv. Funct. Mater.* **23,** 1647–1654 (2013).
7. Sparks, J. R., Sazio, P. J. A., Gopalan, V. & Badding, J. V. Templated Chemically Deposited Semiconductor Optical Fiber Materials. *Annu. Rev. Mater. Res.* **43,** 9.1-9.31 (2013).
8. Chaudhuri, S., Sparks, J. R., Ji, X., Krishnamurthi, M. & Shen, L. Crystalline Silicon Optical Fibers with Low Optical Loss. *ACS Photonics* **3,** 378–384 (2016).
9. Ji, X. *et al.* Single-Crystal Silicon Optical Fiber by Direct Laser Crystallization. *ACS Photonics* **4,** 85–92 (2017).
10. Sparks, J. R. *et al.* Zinc selenide optical fibers. *Adv. Mater.* **23,** 1647–1651 (2011).
11. Liu, Y. *et al.* Confined Chemical Fluid Deposition of Ferromagnetic Metalattices. *Nano Lett.* **18,** 546–552 (2018).
12. Healy, N. *et al.* Extreme Electronic Band-Gap Modification in Laser Crystallized Silicon

Optical Fibres. *Nat. Photonics* **Submitted,** (2014).

13. Manfredotti, C. amorphous silicon prepared by low pressure chemical vapour deposition. *Thin Solid Films* **1411,** 171–178 (1986).
14. Harbeke, G., Krausbauer, L., Steigmeier, E. F. & Widmer, A. E. Growth and Physical Properties of LPCVD Polycrystalline Silicon Films. *J. Electrochem. Soc.* **131,** 675–682 (1984).
15. Foster, D. W., Learn, A. J. & Kamins, T. I. Deposition properties of silicon films formed from silane in a vertical-flow reactor Deposition properties of silicon films formed from silane in a vertical-flow reactor. *J. Vac. Sci. Technol. B Microelectron. Process. Phenom.* **4,** 1182–1186 (1986).
16. Kuiper, A. E. T., Groot, J. De & Veltkamp, G. W. Modeling of Low-Pressure CVD Processes. *J. Electrochem. Soc.* **129,** 2288–2291 (1982).
17. Kurokawo, H. P-Doped Polysilicon Film Growth Technology. *J. Electrochem. Soc.* **129,** 2620–2624 (1982).
18. Meyerson, B. S. & Olbricht, W. Phosphorus-Doped Polycrystalline Silicon via LPCVD. *J. Electrochem. Soc.* **131,** 2361–2365 (1984).
19. Baril, N. F. *et al.* High-Pressure Chemical Deposition for Void-Free Filling of Extreme Aspect Ratio Templates. *Adv. Mater.* **22,** 4605–4611 (2010).
20. Ji, X. *et al.* Single-Crystal Germanium Core Optoelectronic Fibers. *Adv. Opt. Mater.* **5,** 1600592 (2017).
21. Jones, A. C. & Hitchman, M. L. in *Chemical Vapour Deposition: Precursors, Processes and Applications* 1–36 (Royal Society of Chemistry, 2009).
22. Calkins, J. A., Peacock, A. C., Sazio, P. J. A., Allara, D. L. & Badding, J. V. Spontaneous Waveguide Raman Spectroscopy of Self-Assembled Monolayers in Silica Micropores. *Langmuir* **27,** 630–636 (2011).

23. Sears, F. W. & Salinger, G. L. *Thermodynamics, Kinetic Theory, and Statistical Thermodynamics*. (Addison-Wesley Publishing Company, Inc., 1975).

24. Roberts, P. J. *et al.* Ultimate low loss of hollow-core photonic crystal fibres. *Opt. Express* **13,** 236–244 (2005).

25. Orf, N. D. *et al.* Fiber draw synthesis. *Proc. Natl. Acad. Sci. U. S. A.* **108,** 4743–4747 (2011).

26. Ballato, J. *et al.* Silicon optical fiber. *Opt. Express* **16,** 18675–18683 (2008).

27. Scott, B., Wang, K., Caluori, V. & Hall, H. Fabrication of silicon optical fiber. *Opt. Enginnering* **48,** 100501 (2009).

28. Mehio, N., Dai, S. & Jiang, D. Quantum Mechanical Basis for Kinetic Diameters of Small Gaseous Molecules. *J. Phys. Chem. A* **118,** 1150–1154 (2014).

29. Street, R. A. *Hydrogenated Amorphous Silicon*. (Cambridge University Press, 1991).

30. Stuckelberger, M., Biron, R., Wyrsch, N., Haug, F. & Ballif, C. Review : Progress in solar cells from hydrogenated amorphous silicon. *Renew. Sustain. Energy Rev.* **76,** 1497–1523 (2017).

31. Misra, S., Yu, L., Foldyna, M. & Roca, P. High efficiency and stable hydrogenated amorphous silicon radial junction solar cells built on VLS-grown silicon nanowires. *Sol. Energy Mater. Sol. Cells* **118,** 90–95 (2013).

32. Abeles, B., Cody, G. D., Goldstein, Y., Tiedje, T. & Wronski, C. R. Hydrogenated Amorphous Silicon Solar Cells. *Thin Solid Films* **90,** 441–449 (1982).

33. Lim, B. C., Choi, Y. J., Choi, J. H. & Jang, J. Transistor Fabricated on Plasma Treated Silicon. *IEEE Trans. Electron Devices* **47,** 367–371 (2000).

34. Kanicki, J., Libsch, F. R., Griffith, J. & Polastre, R. Performance of thin hydrogenated amorphous silicon thin-film transistors Performance of thin hydrogenated amorphous silicon thin-film transistors. *J. Appl. Phys.* **69,** 2339–2345 (1991).

35. Jasinski, J. M. & Gates, S. M. Silicon Chemical Vapor Deposition One Step at a Time : Fundamental Studies of Silicon Hydride Chemistry. *Acc. Chem. Res.* **24,** 9–15 (1991).

36. Wiesmann, H., Ghosh, A. K., Mcmahon, T. & Strongin, M. a-Si:H produced by high-temperature thermal decomposition of silane. *J. Appl. Phys.* **50,** 3752–3754 (1979).

37. Jadkar, S. R. *et al.* Deposition of hydrogenated amorphous silicon (a-Si:H) films by hot-wire chemical vapor deposition (HW-CVD) method : Role of substrate temperature. *Sol. Energy Mater. Sol. Cells* **91,** 714–720 (2007).

38. Soni, S. K., Phatak, A. & Dusane, R. O. Solar Energy Materials & Solar Cells High deposition rate device quality a-Si : H films at low substrate temperature by HWCVD technique. *Sol. Energy Mater. Sol. Cells* **94,** 1512–1515 (2010).

39. Cocorullo, G., Corte, F. G. Della & Rendina, I. Amorphous silicon waveguides and light modulators for integrated photonics realized by low-temperature plasma-enhanced chemical-vapor deposition. *Opt. Lett.* **21,** 2002–2004 (1996).

40. Scott, B. A., Reimer, J. A. & Longeway, P. A. Growth and defect chemistry of amorphous hydrogenated silicon. *J. Appl. Phys.* **54,** 6853–6863 (1983).

41. Purnell, J. H. & Walsh, R. The Pyrolysis of Monosilane. in *Proceedings of the Royal Society of London* **293,** 543–561 (1966).

42. Giunta, C. J., Mccurdy, R. J., Chapple-sokol, J. D. & Gordon, R. G. Gas-phase kinetics in the atmospheric pressure chemical vapor deposition of silicon from silane and disilane. *J. Appl. Phys.* **67,** 1062–1075 (1990).

43. Motevalian, S. P. *et al.* Kinetics of Silane Decomposition in High-Pressure Confined Chemical Vapor Deposition of Hydrogenated Amorphous Silicon. *Ind. Eng. Chem. Res.* **56,** 14995–15000 (2017).

44. Ho, P., Coltrin, M. E. & Breiland, W. G. Laser-Induced Fluorescence Measurements and Kinetic Analysis of Si Atom Formation in a Rotating Disk Chemical Vapor Deposition

Reactor. *J. Phys. Chem.* **98,** 10138–10147 (1994).

45. Gates, S. M., Greenlief, C. M., Kulkarni, S. K. & Sawin, H. H. Surface reactions in Si chemical vapor deposition from silane. *J. Vac. Sci. Technol. A Vacuum, Surfaces, Film.* **8,** 2965–2969 (1991).

46. Gates, S. M. & Kulkarni, S. K. Kinetics of surface reactions in very low-pressure chemical vapor deposition of Si from SiH4 Kinetics of surface reactions deposition of Si from SiH4 in very low-pressure chemical vapor. *Appl. Phys. Lett.* **58,** 2963–2965 (1991).

47. Coltrin, M. E., Kee, R. J. & Evans, G. H. A Mathematical Model of the Fluid Mechanics and Gas-Phase Chemistry in a Rotating Disk Chemical Vapor Deposition Reactor. *J. Electrochem. Soc.* **136,** 819–829 (1989).

48. Odden, J. O., Egeberg, P. K. & Kjekshus, A. From Monosilane to Crystalline Silicon , Part II : Kinetic Considerations on Thermal Decomposition of Pressurized Monosilane. *Int. J. Chem. Kinet.* **38,** 309–321 (2006).

49. Hsin, W. & Tsai, D. Surface Reaction Probabilities of Silicon Hydride Radicals in SiH 4 / H 2 Thermal Chemical Vapor Deposition. *Ind. Eng. Chem. Res.* **41,** 2129–2135 (2002).

50. Robertson, R. & Gallagher, A. Reaction mechanism and kinetics of silane pyrolysis on a hydrogenated amorphous silicon surface. *J. Chem. Phys.* **85,** 3623–3630 (1996).

51. Claassen, W. A. P., Bloem, J., Valkenburg, W. G. J. N. & Van der Brekel, C. H. J. The depositionof silicon from silane in a low-pressure hot-wall system. *J. Cryst. Growth* **57,** 259–266 (1982).

52. Buss, R. J., Ho, P., Breiland, W. G. & Coltrin, M. E. Reactive sticking coefficients for silane and disilane on polycrystalline silicon Reactive sticking coefficients for silane and dlsilane on polycrysialline silicon. *J. Appl. Phys.* **63,** 2808–2819 (1988).

53. Weerts, W. L. M., de Croon, M. H. J. M. & Marin, G. B. The adsorption of silane , disilane and trisilane on polycrystalline silicon : a transient kinetic study. *Surf. Sci.* **367,**

321–339 (1996).

54. Greenlief, C. M., Gates, S. M. & Holbert, P. A. Reaction kinetics of surface silicon hydrides. *J. Vac. Sci. Technol. A Vacuum, Surfaces, Film.* **7,** 1845–1849 (1989).

55. Sinniah, K. *et al.* New Mechanism for Hydrogen Desorption from Covalent Surfaces: The Monohydride Phase on Si(100). *Phys. Rev. Lett.* **62,** 567–570 (1989).

56. Li, H. & Gale, R. J. Hydraulic and Electroosmotic Flow through Silica Capillaries. *Langmuir* **9,** 1150–1155 (1993).

Chapter 3

Silicon and Germanium Metalattices using HPcCVD

The continuous search for new materials has always been the key to advanced technologies. The fastest way to discover materials for a specific use is to design physical properties into a material. We have seen successes in photonic meta-materials where an artificial lattice, similar to atomic lattices, in IR or visible optical scale is used to create an invisible effect when the corresponding wavelengths of light is projected onto the material[1]. However, most of the important physical processes including electron and phonon mean free path, exciton radius, and quantum confinement, have a much shorter characteristic length-scale. Three-dimensional (3D) lattices with periodic units in 10's of nms or less could interact with electronic, vibrational, and optical processes to open up new opportunities in designable materials, such as affordable thermoelectric materials for heat and energy conversion using silicon with up to 100-fold increase in performance[2,3].

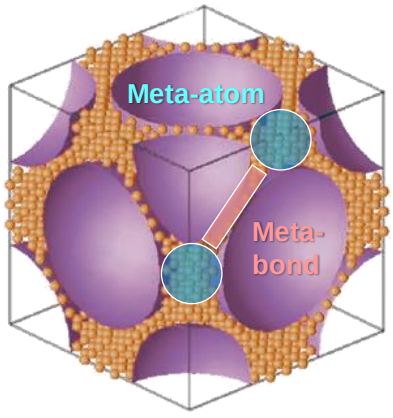

Figure 3-1. Schematic of an example metalattice made by infiltrating materials (orange spheres as Si atoms) into the pores of a silica colloidal crystal template (purple as silica nanoparticles), which consist of meta-atoms (similar to nanoparticles with tetrahedral or octahedral shapes) interconnected by meta-bonds. Periodicity is measured by distance between center of two silica spheres.

The goal here is to design a new class of structural materials with designable physical properties by developing a general strategy to synthesize highly ordered 3D artificial solids, called meta-lattices[4,5] (**Figure 3-1**) with periodic units of 1-60 nm. Independent control over the meta-lattices' size, periodicity, symmetry, chemical composition and interfaces to is also important to increase the degree of freedom in designing advanced materials with specific properties.

Synthesis of elemental semiconductor meta-lattices remains a challenge as existing synthetic routes, such as magnesiothermic reduction of mesoporous silica[6] and solution phase synthesis[7,8], fail to produce high purity precisely doped materials with interconnecting periodic structures. To resolve this issue, a synthetic route using high pressure confined chemical vapor deposition (HPcCVD) to infiltrate high purity (>99.999%) semiconductors into pores of templates such as silica nanoparticle colloidal crystal (this chapter), zeolite Y, mesoporous silica and metal-organic frameworks (*Chapter 5*) have been developed. The use of nano-templates provides flexibility in choosing periodicity and symmetry, but suffers from incomplete filling when using commercially available CVD systems (operates at < 1atm) as only a low density of precursors can travel into the template before clogging all openings. HPcCVD[9–13] takes advantage of pressure driven flow for void free filling by high pressure (up to 350 atm) and uses CVD as it is the industry standard for electronic grade semiconductor production. However, drastic increases in pressure also increase the kinetics of precursor decomposition, promoting gas phase nucleation which leads to particle growth outside of templates and blocking gas molecules from entering. Reactor dimensions must be confined to avoid gas phase particle growth. In this chapter, fabrication and characterization of elemental semiconductor, silicon and germanium metalattice will be discussed. This chapter will focus on elemental semiconductor metalattices

made using silica colloidal crystal template, and *Chapter 4* will focus on compound semiconductor metalattices.

3.1. HPcCVD of Amorphous Silicon and Germanium Metalattices

By combining HPcCVD and nano-templates, the ability to independently control metalattices' size, periodicity, morphology, symmetry, chemical composition and surface chemistry will be demonstrated in this section. Metalattices can be defined as a three-dimensional artificial crystal which has a periodic length-scale, or repeating units similar to atomic lattices, in 10s of nm to up to about 60 nm. As shown in **Figure 3-1**, a typical metalattice consists of two major parts, meta-atoms and meta-bonds. Meta-atoms are similar semiconductor nanoparticles that they are in the nano-scale, but meta-atoms also have interconnectivity between them through the thin meta-bonds. The periodicity of a metalattice is defined by the distance between its repeating units, which is the length between two similar meta-atoms. Metalattices' length-scale of interest varies depending on what materials or semiconductors it is made out of. In the case of silicon, metalattice with periodicity less than 10 nm would give rise to tetrahedral and octahedral features less than its exciton bohr radius, which could take advantage of band-gap tuning from quantum confinement, while still maintaining electrical conductivity through the interconnected structure. A series of templates can be selected to expand the variety of metalattices with different periodicity and symmetry. **Figure 3-2** shows examples of some the templates used in this dissertation for HPcCVD fabrication of electronic metalattices. This chapter will focus on using silica colloidal crystal templates, where *chapter 5* will discuss metalattice made using zeolite Y, mesoporous silica and metal-organic frameworks.

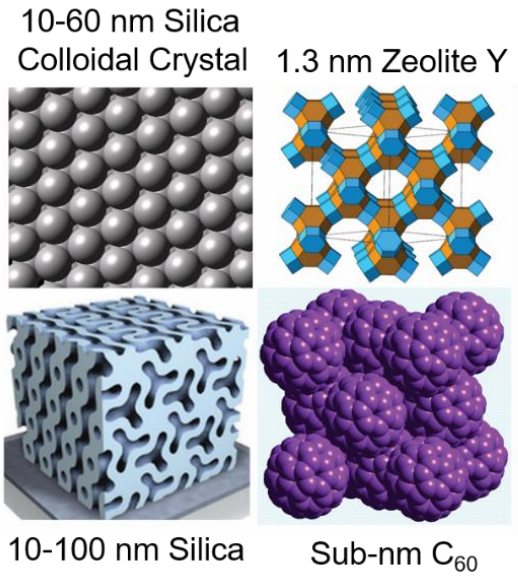

Figure 3-2. Silicon and germanium metalattices nano-templates. Various templates can be used to tune the morphology, symmetry and periodicity of metalattices. Such as silica colloidal crystal made with silica nanoparticles with diameters ranging from 10 – 60 nm, zeolite Y, mesoporous silica and C_{60} crystals.

Silica colloidal crystal is an excellent candidate as metalattice template because of its flexibility in sizes, periodicity and symmetry, where the sizes and periodicity is controlled by the diameter of silica nanoparticles used to make the silica colloidal crystal and the symmetry can be tuned by using colloidal crystal made with two different diameters of silica nanoparticles. Metalattices made using single sized silica colloidal crystal templates have two different sizes and shapes of meta-atoms. For example, if the colloidal crystal is assembled using 30 nm silica nanoparticles in face centered cubic (FCC) structure, the metalattice made from HPcCVD infiltration of such template will have a periodicity of 30 nm and it would have two sizes and shapes of interstitial sites (**Figure 3-3**), a 6.75 nm tetrahedral site (0.225 of the diameter) and a 12.42 nm octahedral site (0.414 of the diameter). The meta-bond will be a tube with 2 nm in diameter interconnecting these two sites together. Except for the case of silica colloidal crystal made using two different diameters of silica nanoparticles, all of the colloidal crystal templates in the dissertation are in FCC crystal packing.

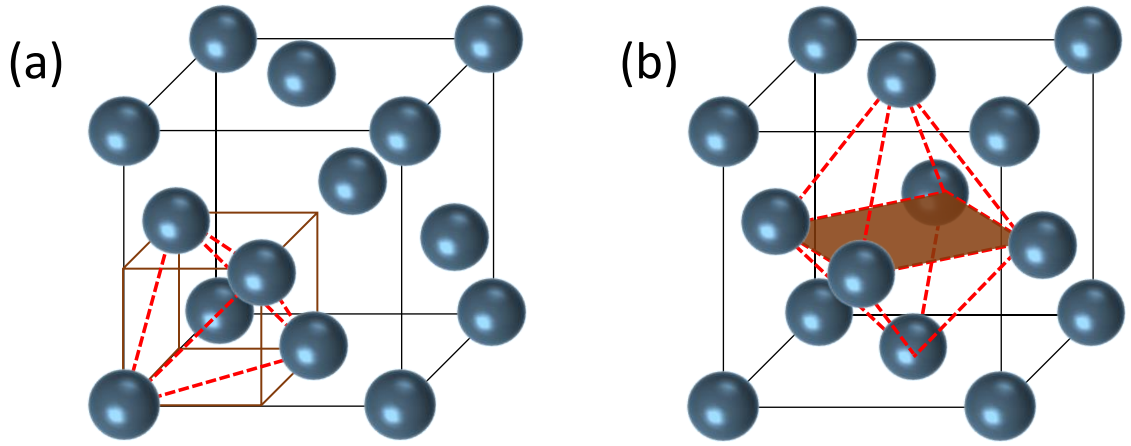

Figure 3-3. Interstitial site in a FCC lattice. There are eight tetrahedral (a) sites and four octahedral sites (b) in each unit cell. The sizes of each site is a fraction of the silica nanoparticles diameter, 0.225 and 0.414 for the tetrahedral and octahedral site, respectively.

High Pressure confined Chemical Vapor Deposition (HPcCVD) of elemental semiconductors, including silicon and germanium, uses high pressure gases and reactor open space confinement to ensure materials can be deposited in the interstitial sites of silica colloidal crystal templates. Silane (SiH_4) and germane (GeH_4) are the reactants mixed with helium carrier gas and reactor configuration can be found in *Chapter 2*. **Figure 3-4** shows the relationship between reactor open dimension, mean free path of gas molecules and pressure to demonstration the infiltration ability of HPcCVD. When the pressure is increased to HPcCVD regime, from 35 – 70 MPa, the mean free path of gas molecules reduces down to less than 1 nm for effective mass transport through diffusion. However, infiltration is only possible if the reactor is confined. If the reactor has large open dimensions, film and large particles will grow quickly on the outer surface of the template to clog the openings of the pores.

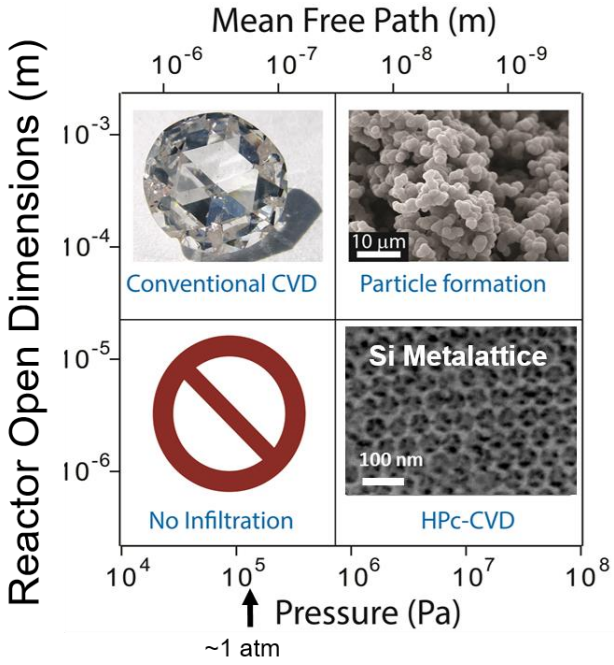

Figure 3-4. Pressure, MFP and reactor open dimension in nano-templates infiltration. Conventional CVD uses low pressure and vacuum (top left), MFP of gas molecules is large and cannot infiltrate into small pores (bottom left). When pressure is raised in high pressure CVD without reactor modification, homogeneous reaction dominates to yield particle formation (top right). When high pressure (35-70 MPa) is combined with reactor open dimension confinement, infiltration into small pores is possible (bottom right).

The reactor confinement effect can be seen in **Figure 3-5**. To demonstrate the effect of reaction open space confinement, two different sizes of spacers were used in HPcCVD infiltration of silica colloidal crystal. .When a 500 µm thickness spacer (not confined) was used instead of 25 µm in confined reactor, insufficient amounts of precursor gas can enter into the pores quickly before the outer surface is coated with a thick layer silicon and large particles formed on top of the template. Many voids remained in the template as shown is **Figure 3-5 (c)**. Under the same reaction conditions including pressure, temperature and deposition time, the nano-template can be infiltrated with silicon void free (**Figure 3-5, (d) – (f)**).

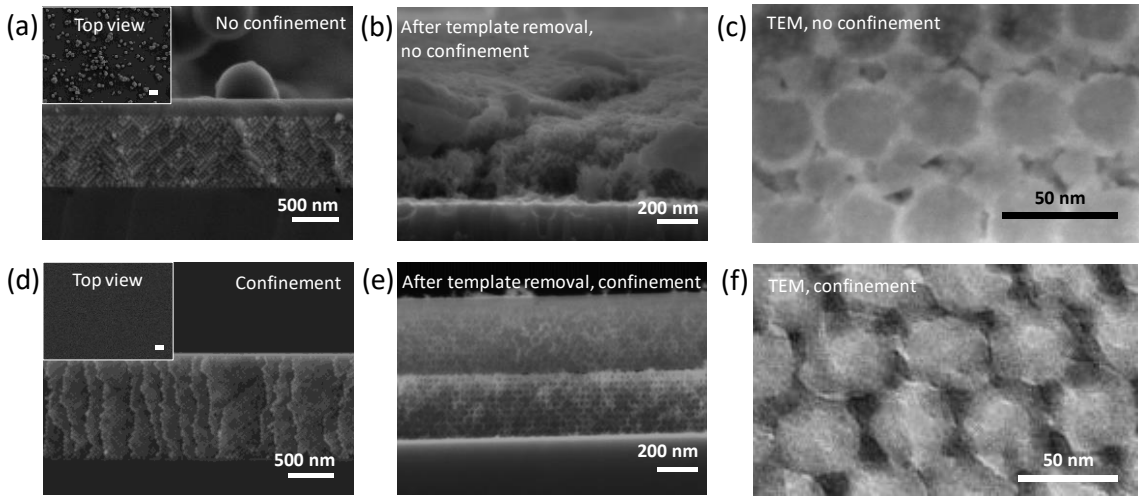

Figure 3-5. Rector confinement effect in HPcCVD of 30 nm Si metalattice. Under the same reaction condition, when the reactor is not confined (a) - (c) on top, large particles grow on top of the surface and forms a film quickly to clog the openings (a). (b) During template removal, the structure cannot stay intact because the semiconductor was not interconnected. Bright field TEM images (c) also suggests that the structure was not completely filled. Darker spots in the image are the empty voids after infiltration. When the reactor is confined (d) – (f), only a thin film is deposited on top (d) and template can be removed without destruction due to silicon interconnectivity (e). Bright field TEM image of Si metalattice.

3.1.1. Silica Colloidal Crystal Template Synthesis

Silica colloidal crystal templates were prepared by Dr. Jennifer Russel from Dr. Thomas Mallouk at Penn State following a vertical deposition method. Silica nanoparticles with diameters ranging from 20 to 200 nm were prepared using a water based synthesis developed by Hartlen et. al. and the sizes of the nanoparticles were controlled by using a regrow method[14]. Nanoparticles with smaller diameter, 14 nm, were synthesized following the method described by Watanabe and coworkers[15]. In short, a biphasic mixture containing nano-pure water (aqueous phase), cyclohexane (organic phase), l-arginine (surfactants) and tetraethyl orthosilicate (TEOS, silica nanoparticles reagent) was used to grow the initial nanoparticle seed. Additional reaction time and TEOS is added to the solution to regrow the nanoparticles to a larger size. The nanoparticles are dispensed in nano-pure water and are used immediately after synthesis to avoid

nanoparticle shape shifting and size changing over time. To prepare for vertical deposition, the prepared nanoparticle solution is further diluted to 7.5 to 10 times lower concentration. The dilution factor changes the quality of the final product and is tested for each size of nanoparticles[16,17].

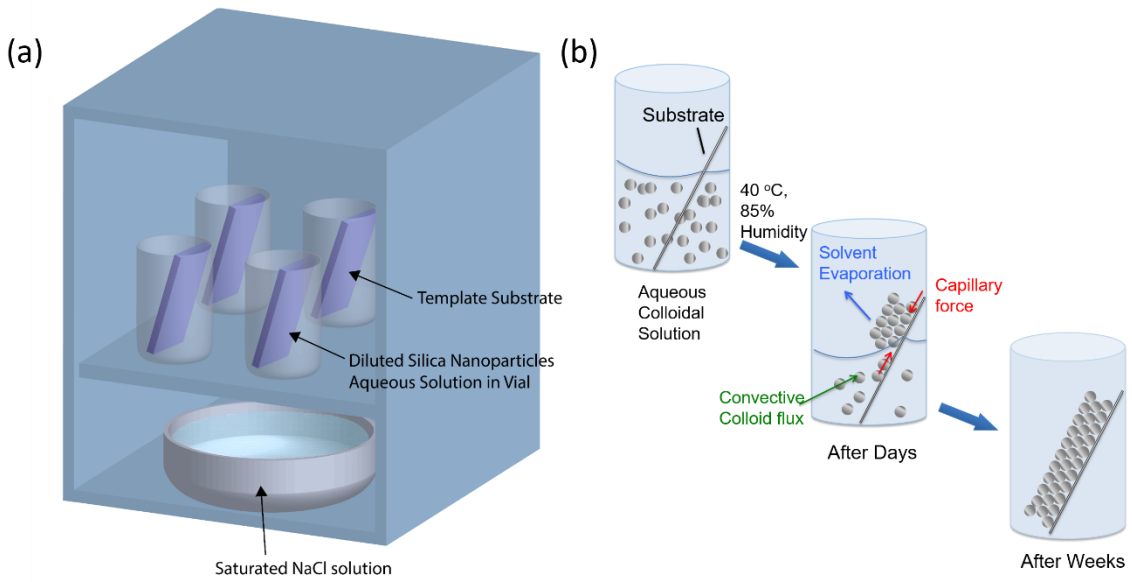

Figure 3-6. Schematic of silica nanoparticles vertical deposition process. (a) Internal arrangement of colloidal solution, substrate and salt solution. The substrate is slanted at 30 ° to normal for smooth thin film deposition. The saturated NaCl solution is used to keep oven relative humidity at roughly 80%. (b) Progression of colloidal crystal fabrication over time. Capillary force and colloid convective flux draws nanoparticles toward the liquid air interface to assemble. Uniform deposition over cm in length is possible. Minimum disruption, including vibration and door opening to the vacuum oven is needed to ensure steady temperature and humidity during growth for a slow, uniform growth rate.

The nanoparticles are deposited and assembled onto a substrate using static vertical evaporation[16–18]. Single crystal silicon wafer or quartz slides are used as a template substrate. The substrates were cleaned using piranha solution (3:1 by volume of 18.4M sulfuric acid and 30% hydrogen peroxide) and rinsed with nano-pure water prior deposition. The substrates are slated into a container approximately 30 degree from normal (**Figure 3-6**) with monodispersed

silica nanoparticle solution filled to the top of the deposition substrate. The humidity and temperature were found to be crucial for good film deposition with controlled growth rate. Therefore, a vacuum oven was modified for precise temperature control (**Figure 3-7**). Temperature and relative humidity inside of the oven is monitored using a Measurement Computing™ USB-520-PLUS RH/Temperature Data Logger. Relative humidity inside of the oven is set at 85% controlled by adding saturated sodium chloride (NaCl) solution. The deposition temperature is set at 40 °C with ±0.01 °C variation controlled by a temperature/ process controller (Athena series 16C) and K-type thermocouple. A thermocouple is placed next to the heating element to control the temperature range and the front glass door is heated using heating tape at 40 °C to minimize heat lose through the glass door.

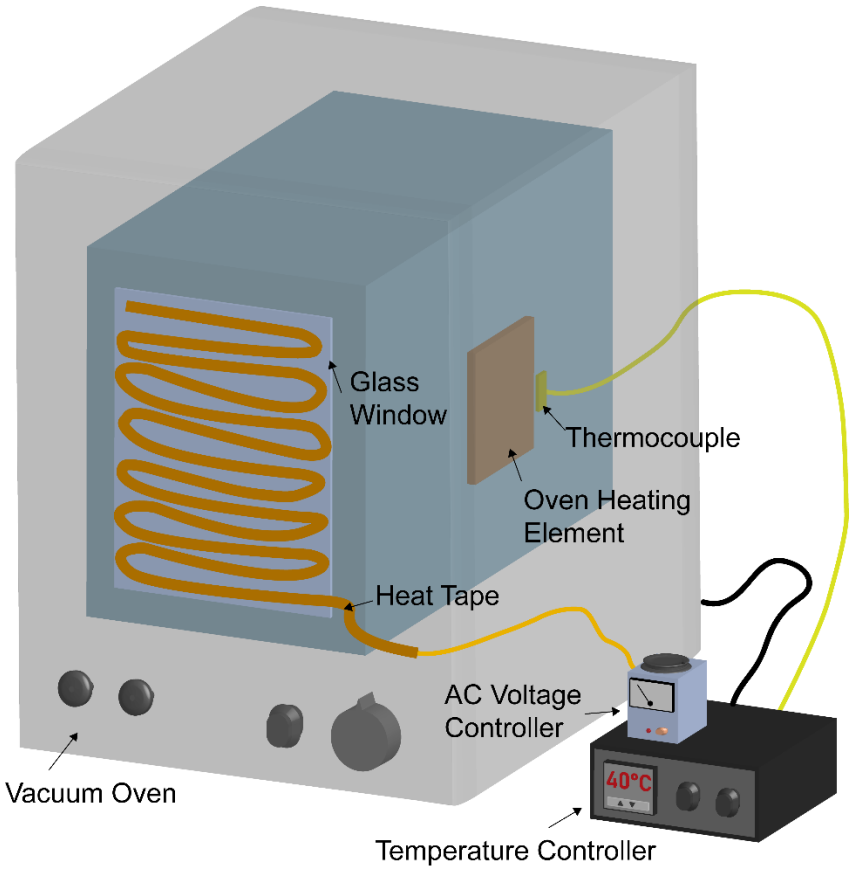

Figure 3-7. Schematic of silica nanoparticles vertical deposition vacuum oven.

3.1.2. HPcCVD of a-Si and a-Ge Experimental Methods

The high pressure confined chemical vapor deposition methods of amorphous Si (a-Si) and amorphous Ge (a-Ge) are similar in terms of experimental set-up and sample preparation. The difference between two materials is the reactant gases and experimental conditions, including temperature, partial pressure and deposition time. Both infiltration of a-Si and a-Ge can be achieved by using a 2D/ 3D closed reactor as shown in **Figure 2-13** and experimental set up in **Figure 2-14**. The overall process is as follows,

1. Prepare templated substrates and place into the sample holder by stacking 25μm thick 304 stainless steel U shaped spacers between each surfaced. Sacrificial glass slides will be placed on both ends to occupy all empty spaced in the reactor for reactor confinement. The samples are secured in the sample holder by set screws.
2. Insert sample holder into the reactor and place the furnace near the deposition zone.
3. Connect the reactor and furnace to the experimental set-up as shown in **Figure 2-14**.
4. Purge experimental set-up with ultra-high purity helium line that is attached to the experimental set-up for 3 cycles.
5. Connect the experimental set-up with a dry scroll pump to vent ultra high purity helium and vacuum the set-up.
6. Repeat steps 4 - 5 for 3 – 5 cycles and preheat the furnace to 200 °C for silicon deposition and 150 °C for germanium deposotion.
7. At the last purge and vacuum cycle, leave the system in vacuum and release high pressure precursor and carrier gas mixture to the system. Typical gas mixtures are SiH_4/ He and GeH_4/ He.
8. Heat the system to deposition temperature, 325 °C for a-Ge and 400 °C for a-Si. The temperature is maintained within +/- 0.01°C by a Stanford Research Systems PTC10

Programmable Temperature Controller. The reaction time varies depending on concentration and total pressure of the gas reservoir.

9. At the end of the experiment, residual precursor gases are vented out of the system through a small pore silica capillary (<100 μm) into the hood to form silica and germania.

3.2. Structure and Morphology of Silicon and Germanium Metalattices

Amorphous silicon metalattice can be synthesized by HPcCVD infiltration using 1 – 10% silane in helium (by partial pressure) at 400 °C reactor internal temperature with total pressure of 20 – 35 MPa. The reaction time ranges from 30 minutes to 3 hours depending on the silane partial pressure and periodicity sizes. For example, the reaction time for 10% silane infiltration of a 30 nm template is 30 minutes and of a 60 nm template is 1 hour because of larger void volume. When the silane partial pressure and total pressure are lower, reaction time increase. All silicon and germanium metalattices are deposited in amorphous form and further annealed thermally at 800 – 850 °C and 550 – 650 °C to c-Si and c-Ge, respectively. The as synthesized silicon were analyzed using scanning electron microscope (SEM) and transmission electron microscope (TEM). Silicon are deposited inside the interstitial sites of silica colloidal crystal via HPcCVD by silane pyrolysis. **Figure 3-8** shows some representative SEM and TEM images of silicon metalattices made with different periodicity and symmetry. By tuning the diameters of silica nanoparticles for silica colloidal crystal assembly, periodicity can be turned freely from 14 nm to hundreds of nms. Shown in **Figure 3-8** are silicon metalattice with periodicity of 14 nm, 30 nm and 60 nm. The respective sizes of tetrahedral and octahedral sites in a metalattice are 3.15 nm and 5.80 nm for 14 nm periodicity, 6.75 nm and 12.42 nm for 30 nm periodicity, and 13.5 nm and 24.8 nm for 60 nm periodicity. In addition, a silica colloidal crystal template with

AB_2 symmetry, assembled using nanoparticles diameters of 30 nm and 20 nm can be infiltrated with silicon to yield metalattice of different symmetry. Metalattice exhibits crystal like features such as metalattice steps, equivalent of atomic steps in single crystalline materials as shown in **Figure 3-8 (b)**.

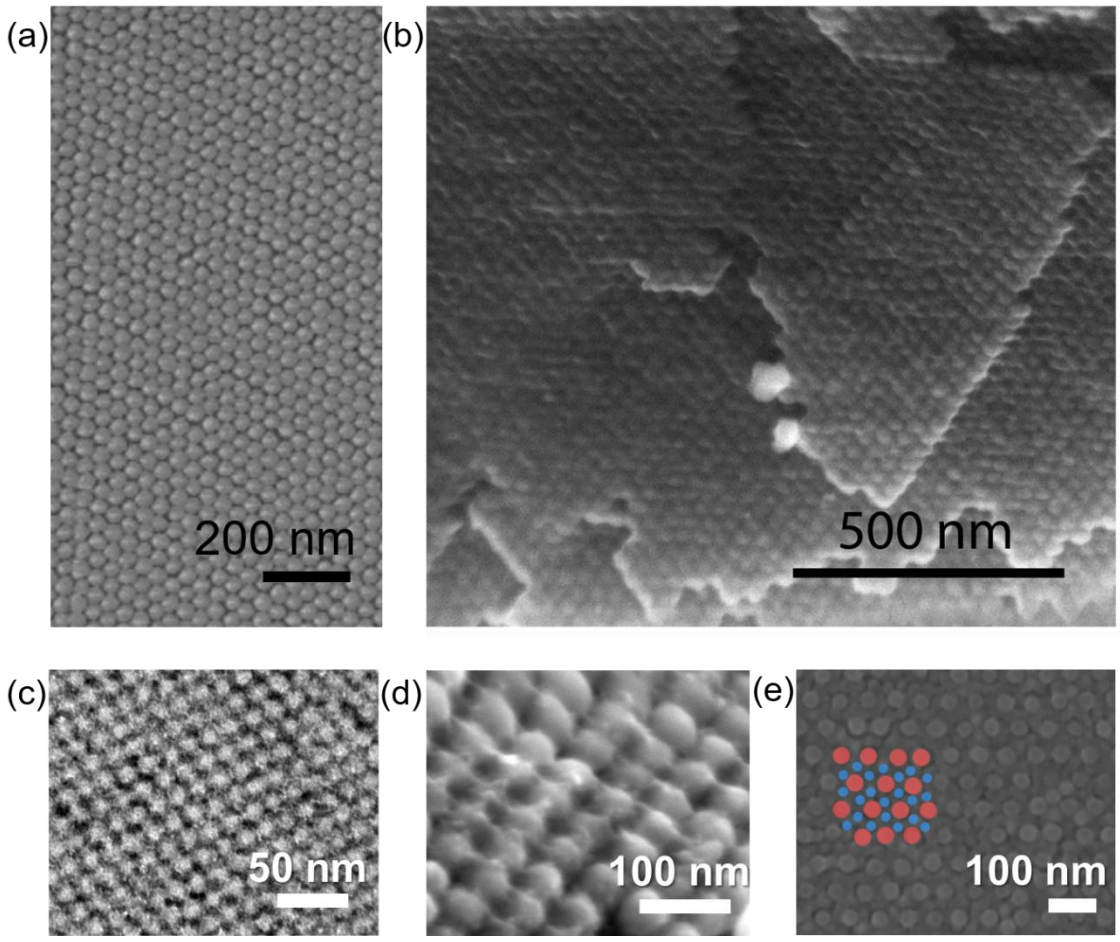

Figure 3-8. FESEM and HRTEM images of HPcCVD silicon metalattices. (a) FESEM top view of 30 nm empty silica colloidal crystal template. (b) FESEM cross sectional view of HPcCVD infiltrated 30 nm silicon metalattice. (c) High Resolution Transmission Electron Microscope (HRTEM) image of 14 nm intrinsic silicon metalattice. (d) FESEM of 60 nm silicon metalattice. (e) HPcCVD silicon metalattice with AB_2 symmetry. Red and blue circles indicate two different sizes of nanoparticle responsible for the AB_2 symmetry.

To further understand and study the shapes and structure of metalattice features including the two different interstitial sites (meta-atoms) and meta-bonds, we looked into high resolution TEM and TEM tomography of 30 nm silicon metalattice. A small section of the HPcCVD infiltrated i-Si 30 nm silicon metalattice was dissected using focused ion beam (FIB). The sample was then thinned using the FIB to about 100 nm, roughly three layers of metalattices. Silica colloidal template was removed using hydrofluoric acid to increase contrast, because silicon and silica has very poor Z-contrast due to similar elemental components. After three-dimensional reconstruction, TEM tomography of Si metalattice (**Figure 3-9**) shows that the overall structure is as predicted (**Figure 3-1**). In particular, the meta-atoms sizes and shapes agree well with prediction where the longest length of the tetrahedral site is 12.4 nm and 6.5 nm (**Figure 3-9, (b) and (c)**).

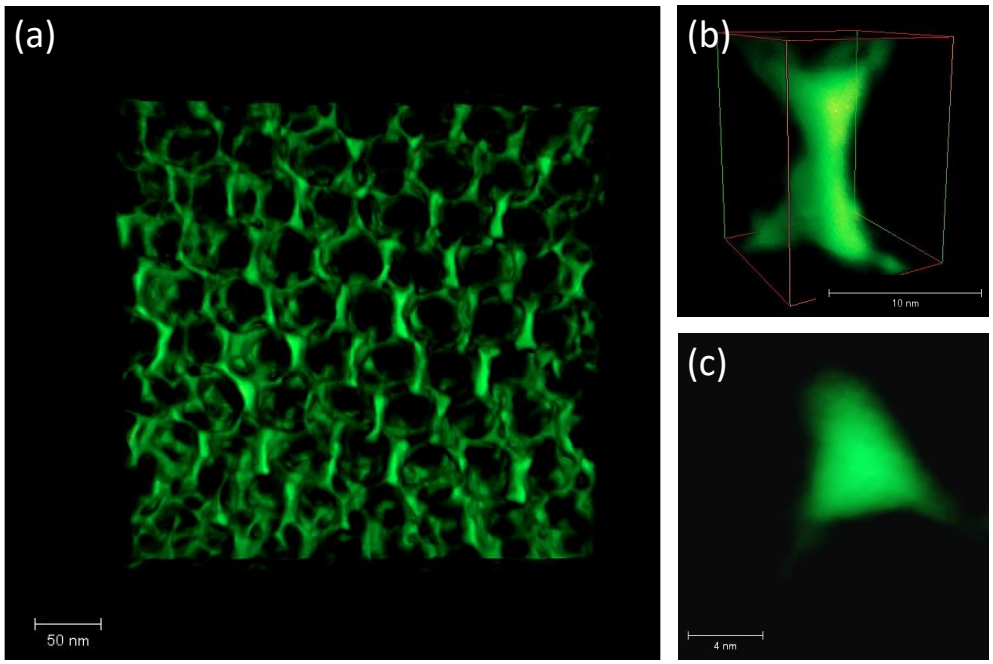

Figure 3-9. TEM Tomography of 30 nm Si metalattice. (a) Overall view of the metalattice. (b) octahedral site and (c) tetrahedral site. TEM credit: Shih-Ying Yu.

Germanium metalattice can be fabricated by changing the gas chemistry in HPcCVD from silane pyrolysis to germane pyrolysis. The reactor configuration is the same for Ge metalattice fabrication, but reaction time, reactant concentration and temperature are different because germane decomposes at a lower temperature. The concentrations of germane used are from 2.5 % to 8 % by partial pressure in helium with a total pressure of 25 – 35 MPa. Reactor internal temperature is 325 °C for amorphous germanium silica colloidal crystal infiltration. The reaction time ranges from 1 hour to 5 hours depending on germane partial pressure. When the germane partial pressure is less than 2.5 %, the deposition rate is too slow for a reasonable growth rate. **Figure 3-10** shows the cross-section of a 30 nm germanium metalattice after the HPcCVD process. The metalattices step that was found to be easiest to cleave was the <111> plane, likely because it is the lowest energy cleavage plane, similar to preferred cleavage planes in single crystalline materials[19,20].

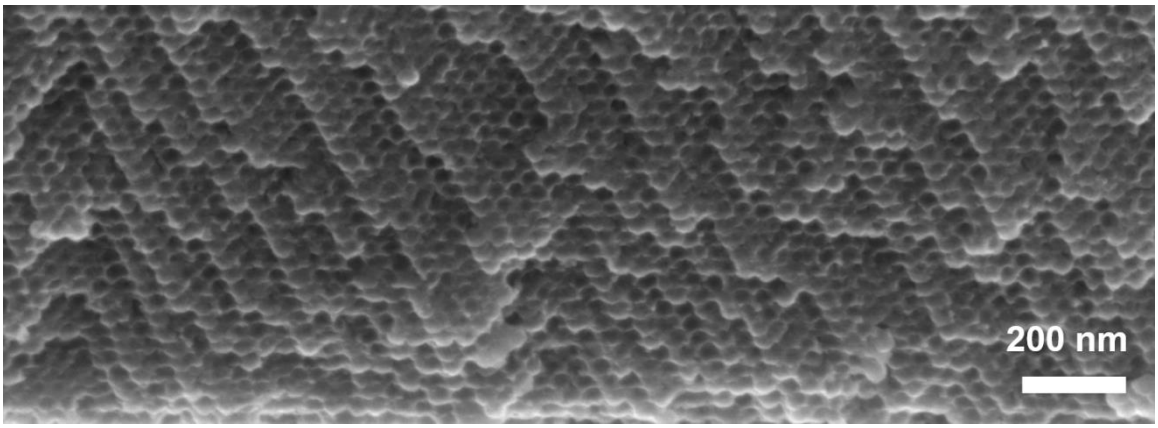

Figure 3-10. FESEM cross section of HPcCVD intrinsic germanium metalattices. Similar to the intrinsic silicon metalattice, the metalattice steps (equivalent of atom steps in single crystalline materials but at a larger scale) can be seen in the cross section view. The metalattice step appears to be on <111> plane.

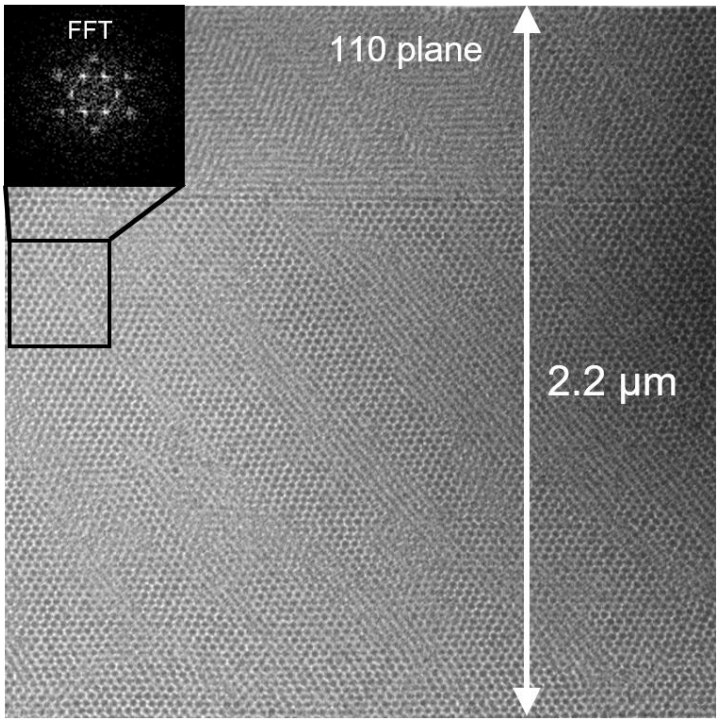

Figure 3-11. Low resolution TEM image of 30 nm Ge metalattice. FFT of TEM image (insert) shows that the structure is well ordered in FCC. The sample was cut along the 110 plane and it is uniform and filled through the thickness, 2.2 μm. Lattice variation and plane changes can be contributed from the angle cut into the sample during TEM preparation, a slight angle off to the <110> plane could make the structure look distorted over a large area. TEM credit: Shih-Ying Yu.

Bright field TEM was used to visualize the metalattice structure at a smaller scale. **Figure 3-11** shows that the structure is uniform and ordered over a large area (2.2 μm) and the HPcCVD process does not disrupt the order of the template. The crystal packing of the metalattice was found to be FCC as shown by the Fast Fourier Transform (FFT) of the TEM image. There were a few stacking faults and lattice variation, which most likely is due the colloid crystal assembly method used. When the sample was cut using the focused ion beam, a small variation to the <110> plane causes the image to show distortion in 2D TEM images. In addition, High-Angle Annular Dark Field TEM (HAADF-TEM) and Energy Dispersive X-ray Spectroscopy (EDS) were used to look at a 30 nm germanium metalattice (**Figure 3-12**) and the elemental components of the metalattice. Only TEM EDS studies were done on germanium

metalattice because it gives a better contrast between Ge and SiO_2 (template) compared to Si and SiO_2. The Ge was found to be well infiltrated into the interstitial sites of the template within the detection limit of the TEM EDS spectrometer.

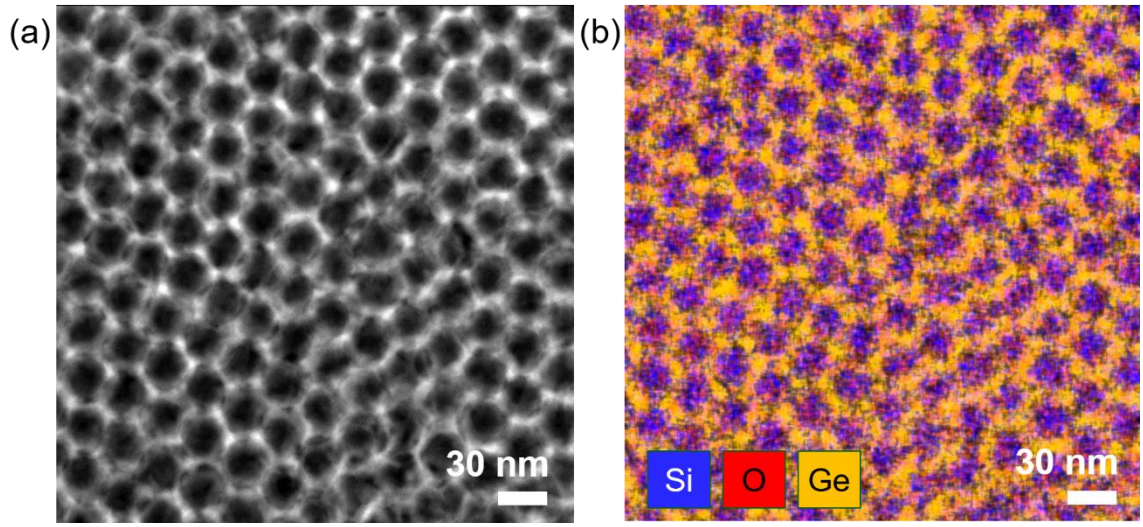

Figure 3-12. High Resolution TEM and EDS mapping of 30 nm Ge metalattice. TEM credit: Shih-Ying Yu

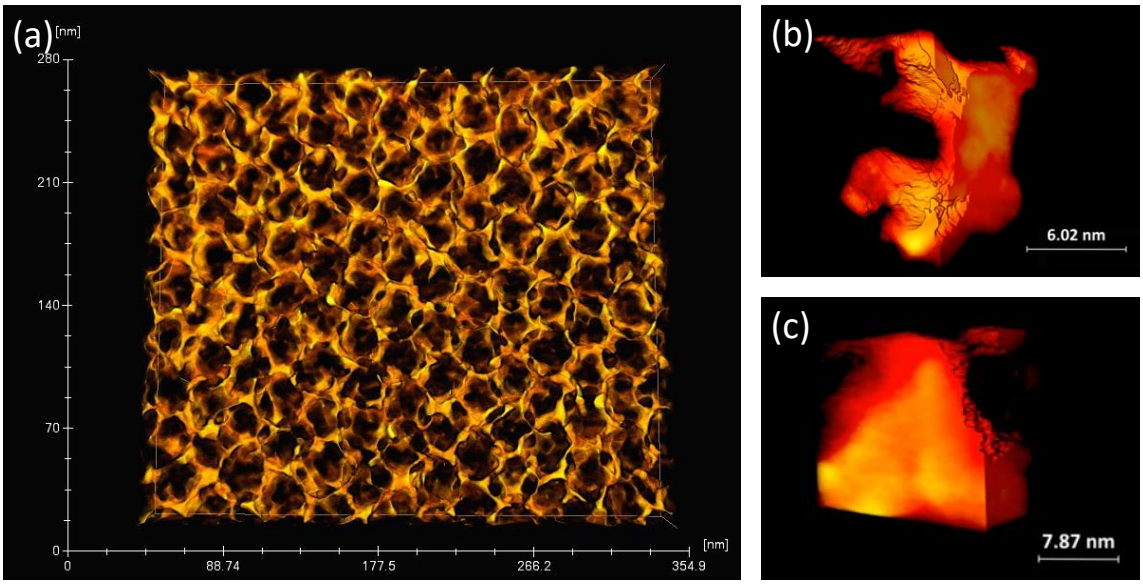

Figure 3-13. TEM Tomography of 30 nm Ge metalattice. TEM credit: Shih-Ying Yu

TEM tomography was also used to visualize the germanium metalattice (**Figure 3-13**). The tetrahedral and octahedral sites were cut open in the center using the TEM reconstruction tool and the selected interstitial sites were found to be fully filled void free with germanium.

3.3. HPcCVD Void-Free Filling and Pores Analysis of Metalattices

Although SEM/ TEM imaging and tomography were able to determine that the selected area (about 350 nm x 300 nm by 60 nm) used for analysis were infiltrated with silicon or germanium void free, a bulk analysis is needed to confirm the filling for the entire dimension of the sample (5 mm x 8 mm x 0.5 – 2 μm). Most porosity characterization methods of solid materials, such and pycnometry, gas absorption and mercury porosiometry, can only measure pores within an open-network[21]. The liquid or gas used in these methods must have a path to enter into the pores for the porosity to be measurement. However, the metalattice structure could have semiconductors coated on the outer surface, blocking all of the entrances and yet not completely filling the interstitial sites. In addition, these porosity characterization techniques do not work well on thin films and requires a large quantity of sample (> 100 mg). A technique that can measure closed pores and thin films is needed to confirm the filling fraction of HPcCVD electronic metalattices.

Positronium annihilation lifetime spectroscopy (PALS) can be used to analyze porous thin films with closed pores[22–25]. PALS does not require special treatment to the sample and can be used to scan films up to μm in thickness over the positron beam diameter[22,23]. Positrons can be generated through a radioactive-decay technique using radio-isotopes such as ^{22}Na, with a half-life of 2.6 years and positron branching ratio of 0.89 (number of positron emission/ total decay emission). Positron implantation energies can be tuned to control the implant depth of the thin film. When positrons are implanted into the film, it locates electrons within the structure to form

positroniums. Positronium (Ps) then travels through the structure to low density regions such as voids and vacancies, where it can minimize its zero point quantum energy. Depending on the sizes of the pores and hence its local electronic environment, positroniums annihilate to emits gamma (γ) rays for Ps lifetime detection. If the structure has a fully interconnected open network, some positrons can be implanted into the solid then form a Ps to travel out of the structure to its surrounding environment (vacuum) without significant attenuation.

PALS studies of metalattice film was completed in collaboration with Prof. David Gidley from the University of Michigan using the monoenergetic electrostatically-focused positron beam[22]. A beam energy of 3.2 keV and 4.2 keV was used to obtain mean implantation depths of 180 nm and 280 nm respectively. This beam energy can optimize positronium (Ps) formation throughout the film while preventing positron implantation to the silicon substrate. Both 30 nm templates and infiltrated samples were studied using PALS, including post thermal processing effects on the films.

PALS studies of the 30 nm silica colloidal crystal template (pre-annealed) was effective in providing information about the interconnectivity of the voids, 23 % of all positrons implanted into the film formed positronium (Ps). Four lifetime signals were fitted at 137 ns, 22 ns, 5.2 ns and 1.83 ns (**Figure 3-14**). There interconnected pore were represented by 30 % of all decays are 137 ns, which escaped to the vacuum. A negligible amount of decays had a 22 ns of lifetime corresponding to a 2 nm in diameter tube shape, representing the meta-bond regions. Another 30 % of the Ps decays at 5.2 ns, representing a 1 nm in diameter cylindrical pore, which could be assigned to the spacing and defects between silica nanoparticles in the as-assembled stage. This was confirmed by thermal annealing the template at 800 °C to remove defects of the colloidal crystal[26]. The remaining 40 % Ps decays had a 1.83 ns lifetime of 0.53 nm in diameter spherical shape, which can be assigned to the amorphous silica network. This 0.53 nm void in the silica network shrank to 0.44 nm of 1.4 ns when the template was heated to 800 °C. The octahedral and

tetrahedral sites were not observed in PALS due to the interconnectivity of the template, where Ps at those sites can easily escape the pores to enter into the vacuum. In attempts to resolve those two sites, a capping layer can be placed on top to try to trap Ps in the interstitial sites. Aluminum with thickness of 40 nm and 80 nm were used to cap the top surface as it is a low density metal for better positron implantation. Both 14 nm and 30 nm templates were capped using Al for interstitial sites PALS studies. Unfortunately, the two studies shown that the 40 nm and 80 nm Al were not able to completely cap the surface, which could be due to defects, imperfections and cracks in the Al sputtered layer. The fitted decays in 14 nm colloidal crystal template, which represent a large void, is 107 ns and 118 ns for 30 nm template, corresponds to spherical shapes of 10 nm and 15 nm respectively. Assuming these decays originated from the tetrahedral sites, which are not as interconnected to the surface compared to the octahedral sites (direct channel from top or bottom surface), these pore diameters are 3x and 2x larger for 14 nm and 30 nm respectively. Since Ps has a tendency to find larger voids and reside there until it decays, it is possible that Ps are decaying in silica colloidal crystal defects such as missing spheres and the spaces between the template and the substrate.

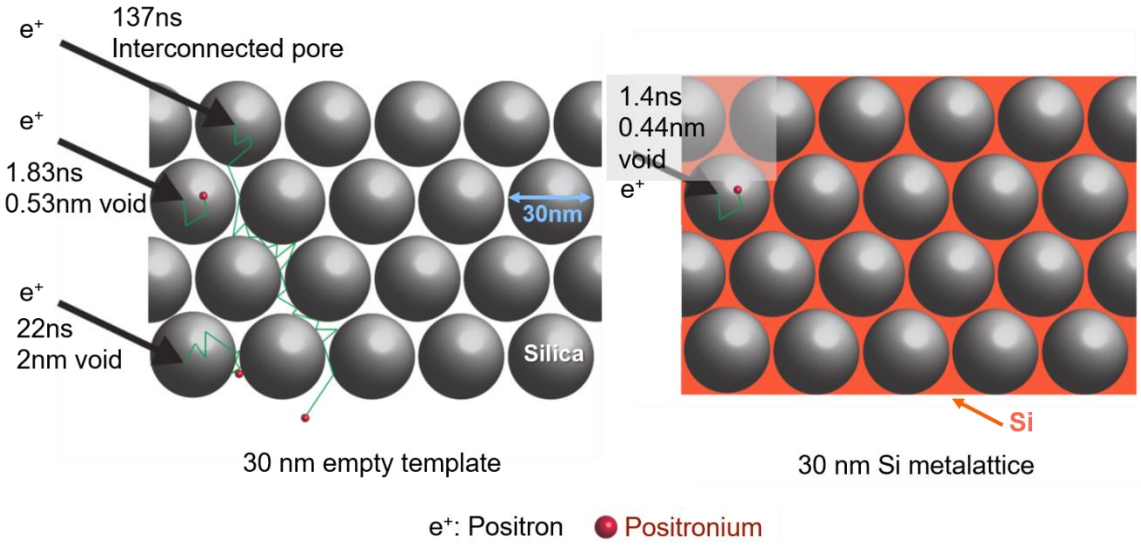

Figure 3-14. Positronium Annihilation Lifetime Spectroscopy (PALS) diagram of 30 nm silica colloidal crystal template (left) and c-Si metalattice (right).

Table 3-1. PALS positronium lifetime, intensity and corresponding spherical diameter of 30 nm empty silica colloidal crystal template and a fully filled 30 nm Si metalattice. Credit: David Gidley.

30 nm empty silica colloidal crystal template		
Ps lifetime	**Intensity**	**Spherical Diameter**
1.83 ± 0.05 ns	9.3 ± 0.2%	0.5 ± 0.01 nm
5.2 ± 0.2 ns*	7.0 ± 0.2%*	0.96 ± 0.02 nm
22 ± 4 ns	0.4 ± 0.1%	2.0 ± 0.2 nm
137 ± 1 ns	6.5 ± 0.5%**	vacuum
30 nm empty silica colloidal crystal template after 800°C treatment		
1.4 ns	-	0.44 nm
132 ns	-	Vacuum
i-Si infiltrated 30 nm Si metalattice		
1.40 ± 0.02 ns	19.1 ± 0.2%	0.44 ± 0.01 nm

The HPcCVD 30 nm crystalline silicon metalattice was annealed at 800 °C prior to PALS analysis and only a 1.4 ns corresponding to 0.44 nm spherical pore was found in the structure. This suggest that there is no open voids within the structure larger than a diameter of 0.44 nm (**Figure 3-14, Table 3-1**). In addition to silicon metalattice, PALS was also used to study the porosity of HPcCVD c-Ge metalattice to show the versatility of HPcCVD in void-free filling different materials in nano-templates. The crystallization temperature of a-Ge metalattice is lower than of silicon at 650 °C and c-Ge metalattices crystalized at 650 °C were found to contain two Ps decays signals, 1.4 ns corresponding to a 0.44 nm in diameter spherical pore and 5 ns corresponding to a 1 nm pore as found in the parent silica colloidal crystal template. When the c-Ge metalattice was further heat treated to 800 °C, only the 1.4 ns was found, again suggesting there were no open pores larger than 0.44 nm, and this corresponding signal is most likely due to the amorphous silica nanoparticles.

Open reactor confinement effects can also be shown using PALS. When the reactor spacer was increased to a 500 μm spacing as shown in **Figure 3-5**, more decays were found even

after 800 °C thermal annealing. Pores in the range of 1 nm and 3-5 nm with decay times of 7 ns and 60 ns respectively were seen in the un-confined samples. This is another indication that open reactor confinement is necessary for void free HPcCVD filling of silica colloidal crystal to fabricate electronic metalattices.

3.4. Reactive-ion Etching of Bulk Semiconductor Layer Grown on Metalattices

During HPcCVD fabrication of electronic metalattices, a layer of semiconductor is deposited coating the entire metalattice surface immediately after complete interstitial sites fillings. It is difficult to adjust the reaction condition to prevent the growth of this layer because the growth rate of Si and Ge in HPcCVD condition is very fast and thin film deposition happens during or right after pore infiltration. This metalattice outer coating becomes problematic for device fabrication and most characterization such as electrical, thermal and optical measurements because the coating acts as a bulk thin film material. The bulk film could prevent access to and probing of the metalattice structure.

Various etching methods can be used to remove the coating layer to gain access to the metalattices. Semiconductor removal can be done in two major categories, wet etching and dry etching. Wet etching uses chemicals in solution as an etchant and can be grouped into isotropic (such as buffered hydrofluoric acid solution for Si) and anisotropic (such as hot potassium hydroxide (KOH), tetramethylammonium hydroxide (TMAH), ethylenediamine pyrocatechol (EDP) for Si [27]. Isotropic meaning it has no etching preference based on direction of the crystal and anisotropic etching means the etchant is more effective in removing materials at a certain direction (based on crystalline planes). However, Si and Ge metalattices are deposited as amorphous and can only be annealed to polycrystalline metalattices in the current system. Wet anisotropic chemical etching would have yielded similar results to isotropic etching where the

etchant can remove the materials at equal rate in all direction of the film as depicted in **Figure 3-15**. Therefore, all wet etching methods are considered to be isotropic for the Si and Ge metalattice structure.

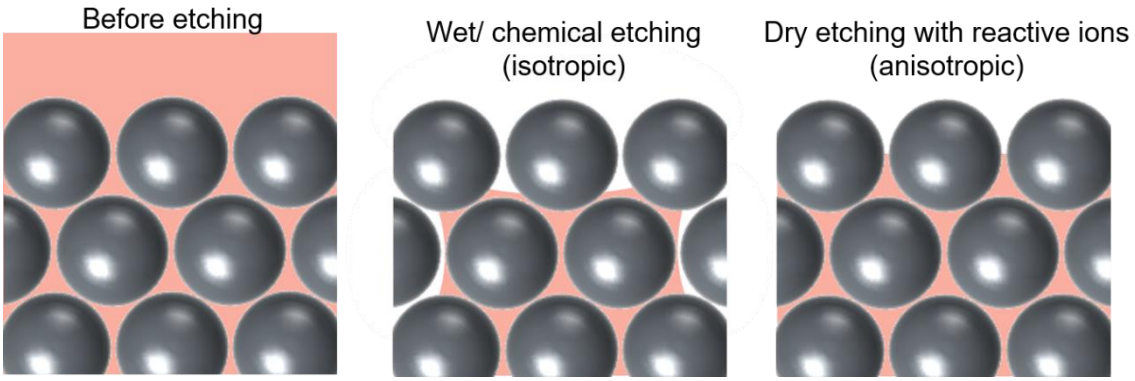

Figure 3-15. Different etching methods to remove semiconductor over-layer in electronic metalattices.

Dry etching using plasmas reactive ions can be used to remove the semiconductor layer on top of the metalattice thin film. Plasma etching can also be grouped into isotropic (such as SF_6 for Si) and anisotropic (such as Cl_2 for Si)[28,29], which differs from the same term used in wet etching. In plasma etching, isotropic etching means materials removal rate has a small variation on the samples' horizontal and vertical direction in correlation to the incident plasma and the etchant can undercut the resist or stop etch materials[29]. In anisotropic plasmas etching, the rate of lateral materials removal is much lower than of downward etching, which can provide a clean and sharp etch[29]. To minimize over-etching of the metalattice structure and empty template exposure after etching, an isotropic plasma reactive ion etching using chlorine radicals was used for both silicon[30] and germanium[31] over-layer removal.

The etching chemistry for silicon is as follows, where chlorine radicals are produced by the plasma to form $SiCl_n$ volatile species to be removed by vacuum. Ge etching uses the same gas but instead will form $GeCl_n$ gaseous species.

$$Cl_{2\,(g)} \rightarrow \bullet Cl + \bullet Cl \text{ (radicals)} \qquad \textbf{(Reaction 3-1)}$$

$$n \bullet Cl + Si \rightarrow SiCl_{n\,(g)} \qquad \textbf{(Reaction 3-2)}$$

Chlorine radical were chosen instead of other silicon and germanium anisotropic plasma etch methods because chlorine etch can result in high silicon to silica selectivity, with over 20 : 1 silicon to silica ratio[30]. Germanium is expected to etch faster than Si in chlorine dry etch[31] and the selectivity should be greater than that of silicon to silica. Since the nano-template is made of silica, the most top layer of silica colloidal crystal can act as a stop etch/ resist material and no silicon or germanium can be removed beyond the top layer of template. Moreover, chlorine was used over other gases such as CF_4 because it does not have possible carbon contamination on the surface[31,32]. **Figure 3-16** depicts the results of Cl_2 reactive ion etched silicon metalattices. After etching, the thin film on the top surface is removed while the top surface remained smooth to the template. The semiconductor infiltrated interstitial sites were protected by the top layer of silica nanoparticles.

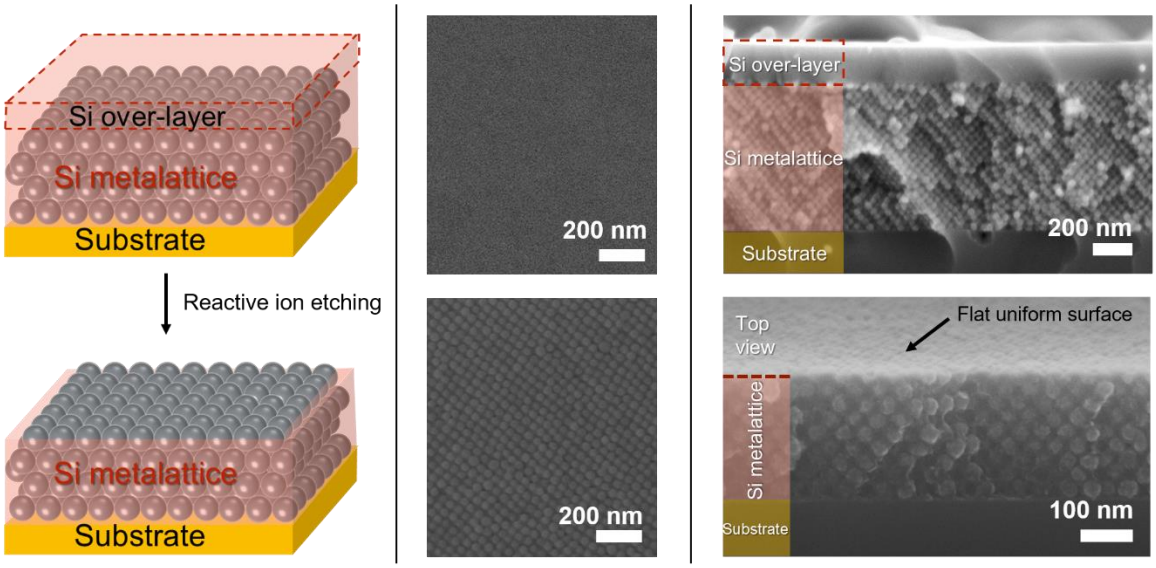

Figure 3-16. Chlorine reactive ion etching of silicon over layer. (left) Schematic of targeted etching results, where only the top layer is removed and the metalattices is not disrupted. (middle) FESEM top view of Si metalattice (top) before and (bottom) after chlorine reactive ion etching. The top layer of silica nanoparticle is acting as a stop-etch material because chlorine radicals have a Si:SiO_2 selectivity of 20:1. (right) Cross section FESEM view of 30 nm Si metalattice (top) before and (bottom) after RIE. A uniform surface with colloidal crystal morphology is obtained after RIE.

3.5. Thermal Processing of Silicon and Germanium Metalattices

The as deposited silicon and germanium metalattices were made of amorphous form. Most semiconductor device uses crystalline materials because they exhibits better electronic and thermal properties than their amorphous counter-parts. Although polycrystalline Si or Ge can be deposited using HPcCVD with higher deposition temperature, the growth mechanism is different than amorphous materials fabrication and could prevent void free filling. Unless single crystalline materials can be deposited by HPcCVD, it is more desirable to deposit as amorphous then use post annealing methods to produce a higher semiconductor quality with largest possible grain sizes[33–35]. Thermal annealing is one of the possible routes in crystallizing amorphous materials. Other methods such as laser annealing[36–38] might also be possible to yield single crystalline semiconductor metalattices.

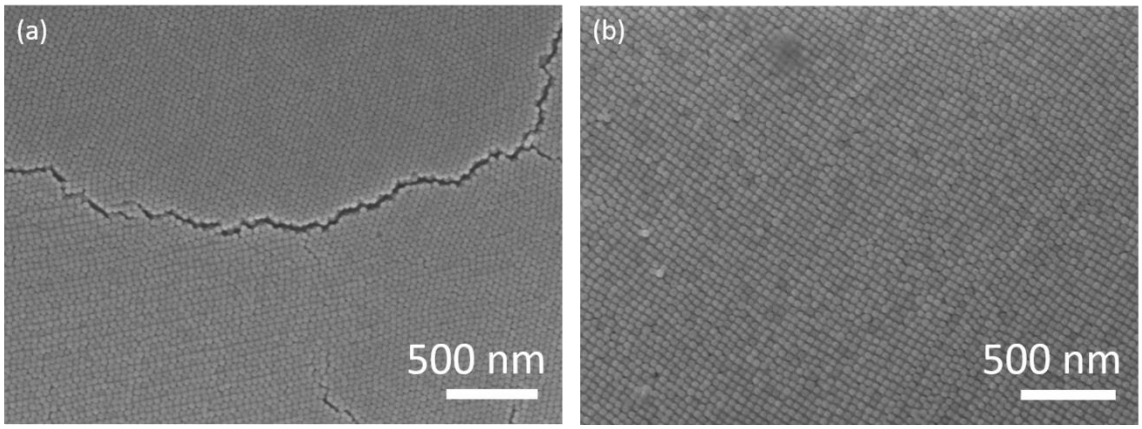

Figure 3-17. Difference between fast and slow ramp rate on 30 nm Si metalattices structure. (a) When the thermal annealing furnace was set to ramp as fast as possible, cracks develops during heating/cooling cycle. (b) No cracks were seen on the metalattice structure after thermal processing when the ramp rate was set to 1 °C/ second for both heating and cooling.

Thermal annealing can be performed using a tube furnace with flowing inert gas, Ar or N_2 at 60 cubic feet per meter. The ramp rate for both heating and cooling was found to be important to metalattice final product. **Figure 3-17** shows when a fast ramp and cooling rate was

used. Cracks start to develop in the structure, disturbing the continuity of the metalattice. This could be due to the thermal expansion difference between the semiconductor (2.6 ppm/°C for Si and 5.8 ppm/°C for Ge at 20 °C) and template (0.55 ppm/°C at 20 °C for silica)[39]. When the ramp rate is lowered to 1 °C/ second, cracking of the metalattice can be eliminated. All of the metalattices, both silicon and germanium were heated with 1 °C/ second ramp up and cool rate and stays at the peak temperature for 30 minutes before cool down.

Previous studies in crystallization of low-pressure chemical vapor deposited amorphous Si nucleates between 550 – 600 °C [40], but HPCVD amorphous silicon optical fiber crystallize at as low as 519 °C. The crystallization mechanism varies depends on experimental conditions including thickness, deposition condition, interfaces, and geometry of the materials. In most crystallization process, small crystallites forms at some critical temperature. These small crystals serves as nuclei to grow larger grains, and eventually the grains merge to form a crystal. This process could be more complicated in the metalattice structure because of its highly interfaced and ordered structure. Crystallites tends to nucleate at the Si/ SiO_2 interface, providing many nucleation sites in the metalattice structure to limit large grain size growth and increase induced-stress to the structure from volume contraction. Low temperature annealing could promote large grain size growth, but higher temperature is needed to eliminate stress induced crystal defects. Si metalattices were heated in 25 °C increments to determine the crystallization temperature. The crystallinity of the metalattices were checked using Raman spectroscopy using 364 nm excitation (**Figure 3-18**). 364 nm excitation was used instead of 633 nm excitation because c-Si metalattices exhibits high photoluminescence backgrounds beyond 200 cm^{-1} Raman shift covering the crystalline Si peaks.

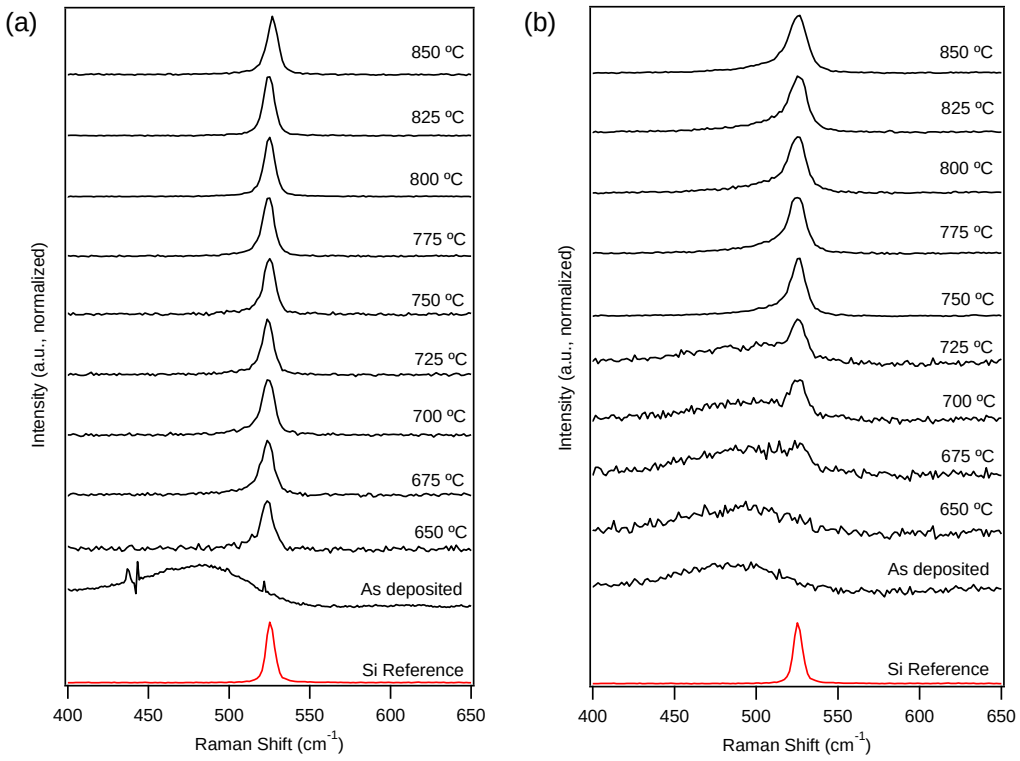

Figure 3-18. Raman spectra of HPcCVD Si thin film on quartz (a) and 30 nm Si metalattice (b) at increasing annealing temperatures. Crystalline Si Raman mode is at near 520 cm^{-1} and amorphous Si Raman mode centers around 480 cm^{-1}. Thin film HPcCVD Si on quartz substrate are deposited as amorphous and crystallized at 650 °C, where 30 nm Si metalattice crystallize at around 700 °C.

The crystallization temperature of HPcCVD Si metalattice is at 700 °C and full crystallization is above 750 °C, which is much higher as compared to 650 °C for HPcCVD Si thin films on a quartz substrate (both were deposited as amorphous at 400°C). This increase in annealing temperature could be due to many factors, including smaller total volume (26% Si in 74% template), stress induced by Si/SiO_2 interfaces, mechanical strain energy, surface chemistry and nucleation sites restricted by the template. This results agrees with previous reports on a-Si/ SiO_2 superlattice thermal annealing, where thinner a-Si layers requires a higher annealing temperature. Using an empirical model[41], the annealing temperature of a 6.75 nm thickness thin film would crystallize at 756 °C. The crystallinity was probed using the first order A_{1g} c-Si peak at 520 cm^{-1}, fitted with Voigt peak to determine the Lorentizian Raman and Gaussian instrument

components. The c-Si full width at half maximum (FWHM) of the single crystalline silicon wafer reference was 5.57, while the FWHM of HPcCVD Si thin film ranges from 7.18 to 9.19 with 825 °C peak temperature having the lowest value of 7.18. The Si metalattices c-Si FWHM ranges from 13.39 to 14.32 with 750 °C peak temperature having the lowest value.

To further investigate the crystallite growth inside of metalattices, high resolution transmission electron microscopy (HR-TEM, in collaboration with Dr. Shih-Ying Yu) was used to look at grain structure and sizes in the meta-atom site. A metalattice sample was prepared using the Helios NanoLab 660 focused ion beam (FIB) and imaged using the FEI Titan^3 G2*. **Figure 3-19** shows a representative image of a 30 nm Si metalattice, where crystallites (5x4 nm) smaller than the size of the meta-atom site (7 nm and 13 nm) can be grown at an annealing temperature of 850 °C. Smaller crystallites from 1 – 3 nm in length can also be seen surrounding the larger crystals. Nano-crystallites with different crystal orientations were observed.

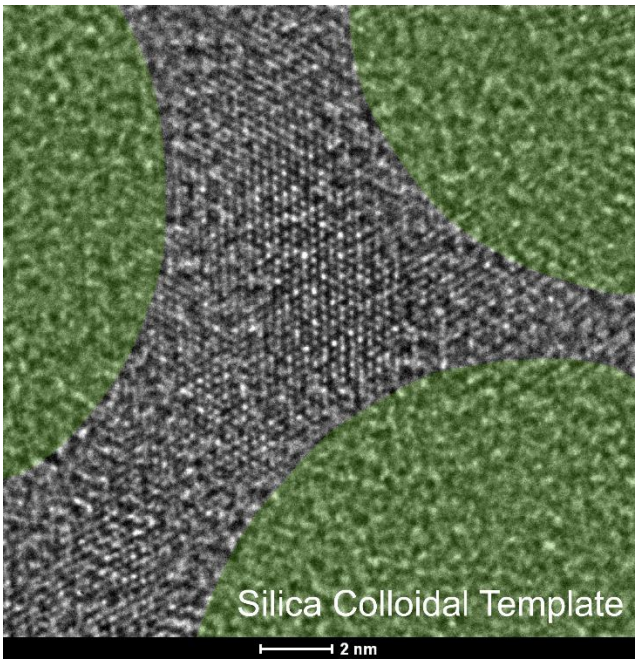

Figure 3-19. HRTEM of 30 nm silicon metalattice after crystallization. TEM credit: Shih-Ying Yu.

Another possible thermal annealing process is by rapid thermal annealing (RTA), where previous studies have shown crystallinity of silicon embedded in a matrix can be improved[42]. However, as discussed earlier, fast cooling can introduce cracks to the sample and can be detrimental to device fabrication. Cracking could be reduced if a slow cool rate was chosen and if the templates were removed prior annealing to eliminate thermal expansion mismatch. To test if RTA does provide higher quality crystallites, HPcCVD Si on a quartz substrate was tested and Raman spectroscopy was used to analyze its crystallinity. **Figure 3-20** shows the Raman spectra of the comparison between thermal annealing, RTA and single crystal Si reference. The RTA Lorentizian component does have a lower FWHM (7.56) as compared to thermal annealing sample (8.5), suggesting that RTA crystallization methods might produce better crystals. The asymmetric broadening as seen in **Figure 3-20** is indicative of nano-crystalline structures. However, peak position results from the Raman spectra suggested RTA resulted in smaller crystal grains as compared to thermal annealing. Due to phonon confinement in smaller crystals, the Raman band shape changes and this change can be used to correlate crystal sizes using various correlation length models[43]. We assume that there are negligible local temperature effect due to the incident laser beam. Generally, high power laser irradiation of sample can cause disturbance to the interatomic potential to downshift the peak position and increase the bandwidth[43]. The power density used was low at about 22 kW/cm^2 to as best eliminate thermal effects. Plasma-enhanced chemical vapor deposited (PECVD) silicon nano-crystallites[43] have been studied using both a correlation length model[44] and Zi's probability model[45] based on Raman peak shifts, and it was found that Zi's probability model is preferred with nano-crystal silicon. Using Zi's model[45], RTA processing of HPcCVD Si on quartz has average crystal sizes of 5.3 nm and thermal annealing results in average crystal sizes of 6.9 nm. Raman analysis based on peak position differs from the FWHM, where the peak broadening could also come from total difference sizes of crystals in the matrix. It is possible that thermal annealing of HPcCVD Si on quartz produces

larger crystals, but also a wider crystal size distribution, while RTA results in smaller crystals with a smaller crystal size distribution.

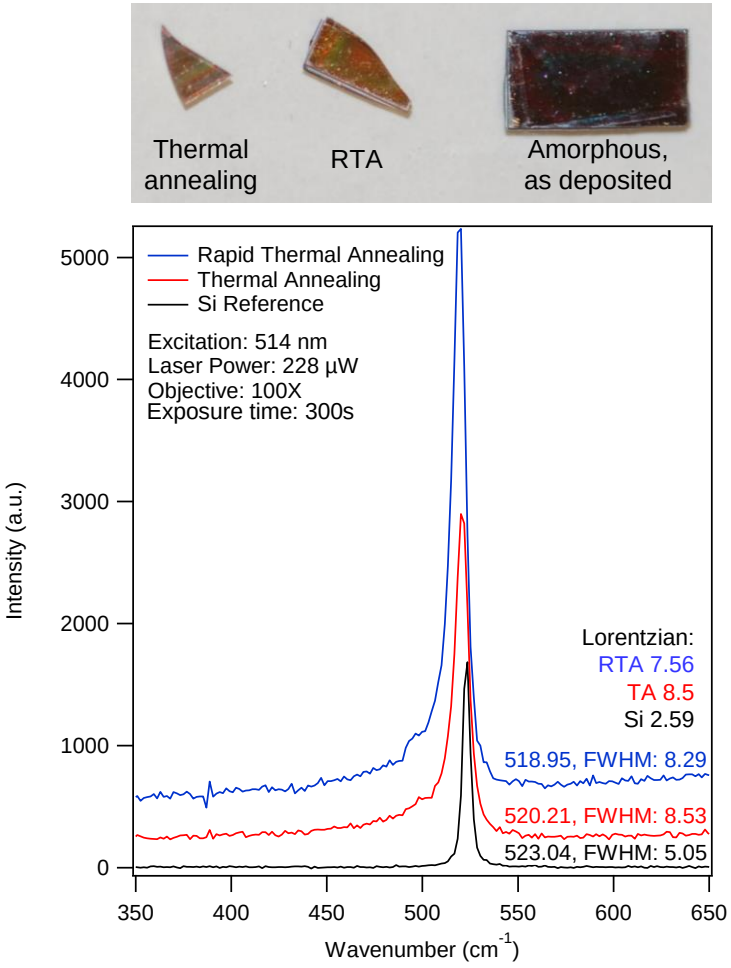

Figure 3-20. Rapid thermal annealing (RTA) vs thermal annealing of HPcCVD thin film on quartz shown by Raman spectroscopy.

The crystallization of germanium metalattice was also examined using thermal annealing processes. Amorphous Ge (a-Ge) can be crystallize from 400 – 420 °C from previous studies[46,47], while lower temperatures can be achieved depending on deposition condition, film thickness and annealing environment. Similar to silicon metalattices, Ge metalattices crystalize at a higher

temperature compared to Ge thin film deposited on quartz substrate, both deposited as amorphous at 325 °C and thermally annealed from 350 °C to 600 °C. A higher temperature was avoided to prevent Ge nanocrystal evaporation and diffusion into the silica matrix[48]. Although higher temperature could result in larger overall crystals, the crystals are not single crystalline and crystal defects along the grain boundaries can increase[49].

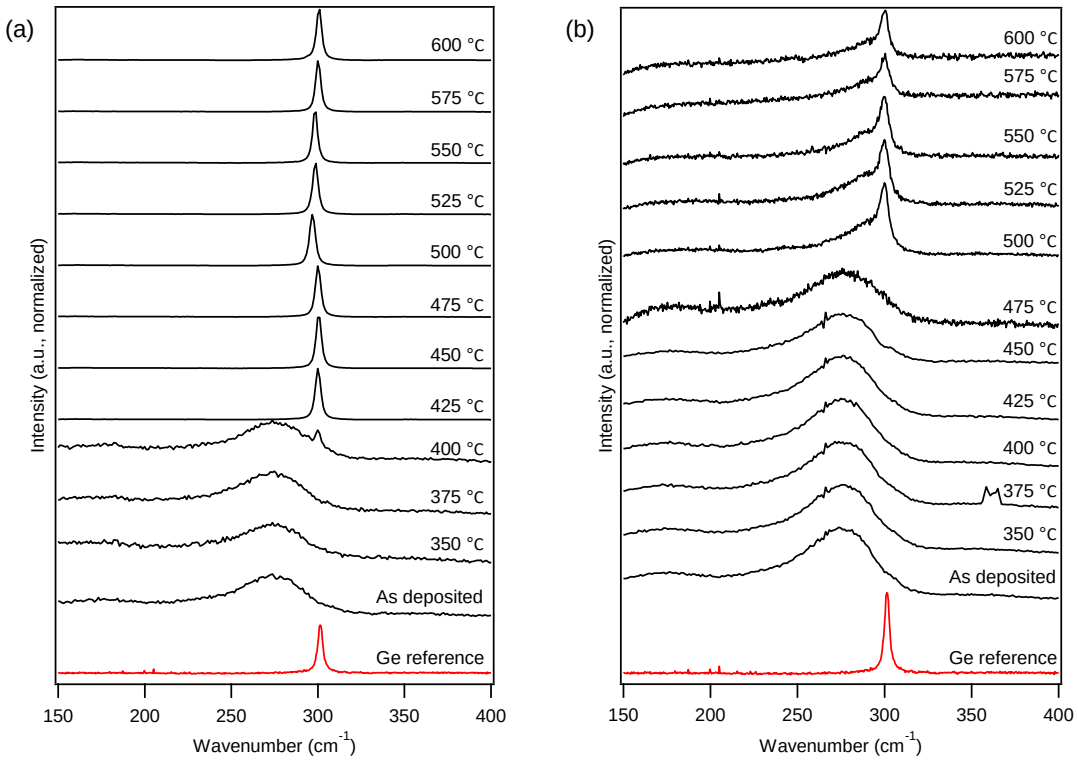

Figure 3-21. Raman spectra Ge thin film on quartz (a) and 30 nm Ge metalattice (b) at increasing annealing temperatures. Crystalline Ge Raman TO mode centers around 305 cm^{-1} and its amorphous peak is around 275 cm^{-1}. HPcCVD thin film Ge deposited on quartz substrate crystallize at 425 °C, where 30 nm Ge metalattice crystallize at around 500 °C.

Ge metalattices crystalize at 500 °C while Ge thin film crystallizes at a lower temperature of 425 °C. The crystallinity of Ge was examine by Raman spectroscopy with 364 nm excitation wavelength where the metalattice shows a strong peak broadening indicating presence of nano-crystallites at various sizes (**Figure 3-21**). The Ge single crystal wafer reference peaks at 300.82

cm^{-1} with a Lorentizian FWHM of 3.14. The FWHM of HPcCVD Ge annealed at various temperature ranges from 2.78 to 3.82, with 550 °C and 575 °C having the lowest value of 3.14 and 2.78 respectively. The FWHM of 30 nm crystalline Ge metalattice is much larger due to large volume of nano-crystals, ranging from 14.281 to 73.561 with 600 °C having the lowest value. For the metalattices, there was a slight red shift of 2 – 3 wavenumbers, which could be due to compressive stress on the Ge metalattice exerted by the silica colloidal crystal template.

3.6. Template Removal for Surface Modification

Another tunable parameter of interest for synthesizing metalattices is the possibility of altering surface chemistry and interfaces. Thus far in the dissertation, chemical composition of the metalattices can be changed by using different gas chemistry in HPcCVD. The periodicity and symmetry can be tuned by using various sizes and packing of silica colloidal crystals. The as synthesized Si or Ge metalattice have a Si/ SiO_2 or Ge/ SiO_2 interface. There are several ways to change the surface, such as using colloidal crystals made of other materials, surface passivating the template prior to HPcCVD or removing the template followed by surface treatment. Colloidal crystals made of other materials could change the semiconductor mechanism. For example, one commonly assembled nanoparticle is gold, but gold can form a eutectic phase with silicon to grow single crystalline silicon with gold incorporation, thus contaminating the silicon. Surface passivation prior to HPcCVD can also alter the Si/ Ge growth mechanism since the first steps of silane or germane pyrolysis is to have reactive SiH_n and GeH_n molecules adhere to the surface. Template removal is the most versatile method and could open up countless possibilities of interfacial design.

Silica templatse can be removed by wet chemistry or plasma dry etch. Most dry etches operates in ultra-high or low vacuum to maintain a steady plasma[29], which is not ideal in

removing the nano-template in a metalattice because the mean free path of reactive ions in vacuum is low and they might not be able to travel through the network to completely remove all of the templates. Moreover, most dry etching gas chemistry often removes both silica and silicon. For example, even though CHF_3 is considered to be a high selectivity SiO_2/ Si etching gas, it still removes silicon in the process. Wet chemical etchant can penetrate into the strenuous pathway in the metalattices. To allow for further surface modification and interfacial design, hydrofluoric acid (HF) was used to remove the silica colloidal crystal template. However, upon template removal and drying, the metalattice structure would collapse to disordered silicon as shown in **Figure 3-22**.

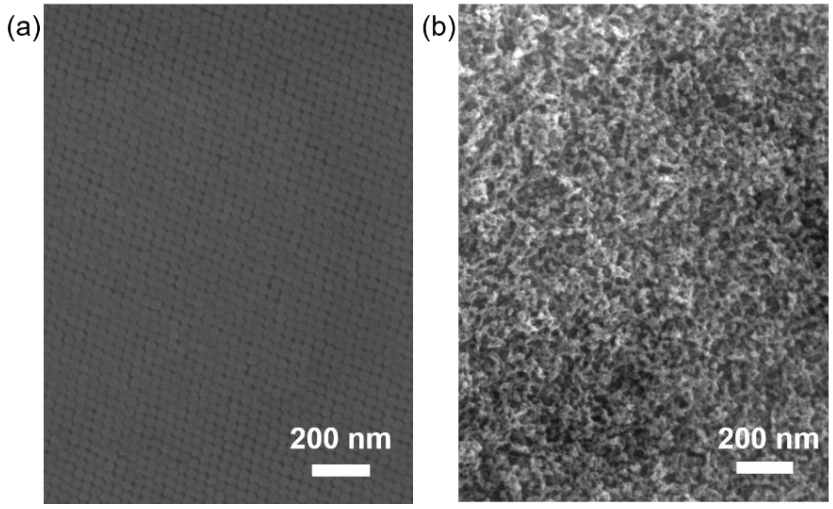

Figure 3-22. Si metalattice structure collapse after template removal using HF wet-etch. (a) Top surface of 30 nm silicon metalattice after reactive ion etching and before template removal. (b) Metalattice structure collapsed after template removal using hydrofluoric acid etching and drying in water.

Previous studies on porous silicon, which has comparable pore diameters to silicon metalattice but has disordered pores, has shown that the drying process after HF etching is what determines if the structure would collapse[50,51] . The internal pressure experienced by a pore is determined by the pore diameters (**Table 3-2**) and surface tension of the drying solvent; this

internal pressure can be reduced if solvent of a lower surface tension is used. Pressure experienced by the pore can be expressed by the Young-Laplace equation,

$$\Delta p = \gamma \frac{2\cos\theta}{r} \quad \textbf{(Equation 3-1)}$$

Where Δp is the pressure difference between within the pore and its surroundings, γ is the liquid surface tension, θ is the contact angle, and r is the pore radius. Since the drying solvent will be surrounded by the metalattice, we can assume the contact angle to be zero and the only term that can be alter is the surface tension.

Table 3-2. Internal and external pressure difference with different spherical pore sizes.

Pore Radius	ΔP (atm)
1 mm	0.0014
1 μm	1.45
10 nm	145
1 nm	1450

Disordered porous Si uses either supercritical carbon dioxide (CO_2) drying (zero surface tension) or pentane[52] as the drying solvent (15.5 mN m^{-1} at 20 °C [53]). Both of these two processes would add complications to HF etching of Si or Ge metalattices. Supercritical CO_2 drying requires a complex experimental apparatus. Pentane is highly flammable and is not miscible with water. Since a water rinse is required after HF etching to remove excess HF and by-products, an additional solvent exchange step will be needed if pentane was used. To test if lowering the surface tension of drying solvent as compared to water can help prevent structure collapse, a series of solvents (**Table 3-3**) were selected based on the requirements of low surface tension, miscibility with water, interaction with metalattices, low toxicity and low flammability.

Table 3-3. Surface Tension of different drying solvents[54].

Drying Solvent	Surface Tension (mN m^{-1} at 20 °C)
Water	72.8
11% Ethanol in Water (by mass)	46.03
Acetone	23.7
Methanol	22.6
Ethanol	22.27
n-Hexane	18.4

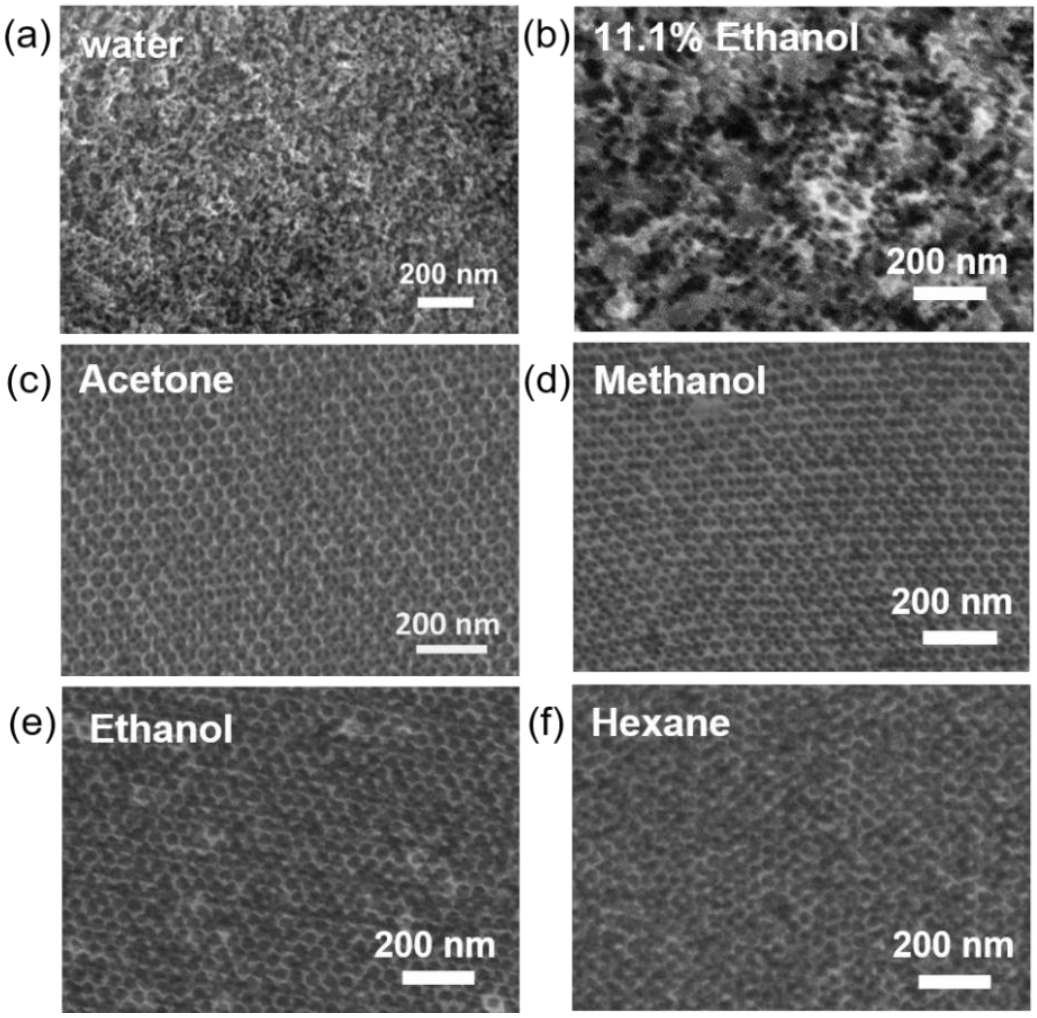

Figure 3-23. Solvent effect on the drying process during silica colloidal crystal template removal. When water (a), surface tension of 72.8 mN m^{-1} at 20 ℃, was used as the drying solvent, the metalattice structure collapsed due to internal pressure build up in the pores. When surface tension is reduced to 46.03 mN m^{-1} at 20 °C (b), metalattice structure starts to develop. All the templates can be removed without disrupting the order and 3D morphology when surface tension reaches below 23.7 mN m^{-1} at 20 ℃, (c) – (f).

The results shown is **Figure 3-23** suggest that drying solvent with surface tension lower than that of acetone, 23.7 mN m^{-1} at 20 °C, is enough to minimize internal pressure in the pores to lead to a fully ordered, undisturbed metalattice structure. Solvents with lower surface tension were also tested but there were not significant improvement to the overall resultant structure. Furthermore, methanol and ethanol have been shown in previous studies of disordered studies that the alcohol groups could absorbed onto the surface, altering photoluminescence properties of the native structure. n-Hexane has the lowest surface tension out of the selected solvents, but it is not miscible with water and would require an additional solvent exchange step. Acetone was chosen as the drying solvent for both Si and Ge metalattices.

3.7. Photoluminescence Studies on Si and Ge Metalattices

Quantum confinement effect and optical properties of metalattices were examined by looking at the photoluminescence properties of as deposited and crystalized Si and Ge metalattices were characterized using a Renishaw Raman spectrometer with a 633 nm excitation He-Ne laser. Ground state electrons in the metalattice are excited by photons from the incident beam then relax and recombine to emit light. The disordered silicon atomic lattices in a-Si metalaticce exhibits no PL; PL arises after thermal processing to crystalize the Si metalattice (**Figure 3-24**). In agreement with Raman studies of thermal annealed sample at 800 °C, nanocrystallites form in the metalattice network exhibits quantum confinement effect to yield emission peaking at the 650 nm (1.9 eV) region at room temperature.

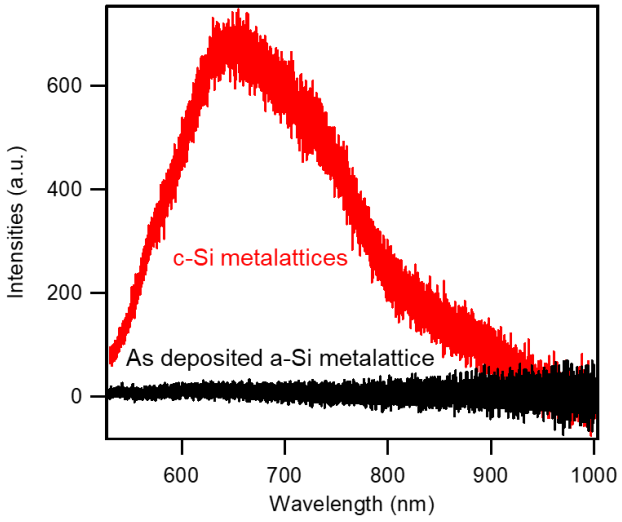

Figure 3-24. Photoluminescence spectra of 30 nm as deposited a-Si metalattice (black) and c-Si metalattice (red).

Two of the most plausible origins of recombination mechanism from nanocrystal silicon and germanium are quantum confinement and surface states[52,55]. Although the initial PL study in **Figure 3-24** suggests possibility of quantum confinement, it was difficult to determine which of the recombination mechanisms is dominant. To further understand the photoluminescence mechanism and the recombination process, PL behavior after template removal was also examined. **Figure 3-25** shows the comparison of PL before and shortly after template removal (within 30 minutes to minimize native oxide formation on silicon). The PL emission dissipates immediately after template removal, suggesting that a silicon/ silica interface is needed and therefore surface states should have been the dominating factor instead of quantum confinement. In addition, when the Si metalattice sample was left at atmosphere for a long periodic of time after template removal, PL reappears (**Figure 3-26**). Si metalattice is prone to surface oxidation in air after template removal if stored in air[56,57]. It is reasonable to believe that a thicker layer of native oxide is formed over time. The PL studies in **Figure 3-26** are in agreement with the

hypothesis that surface states is the dominant mechanism because PL intensity increases in correlation to the time the metalattice is left in air to form native oxide.

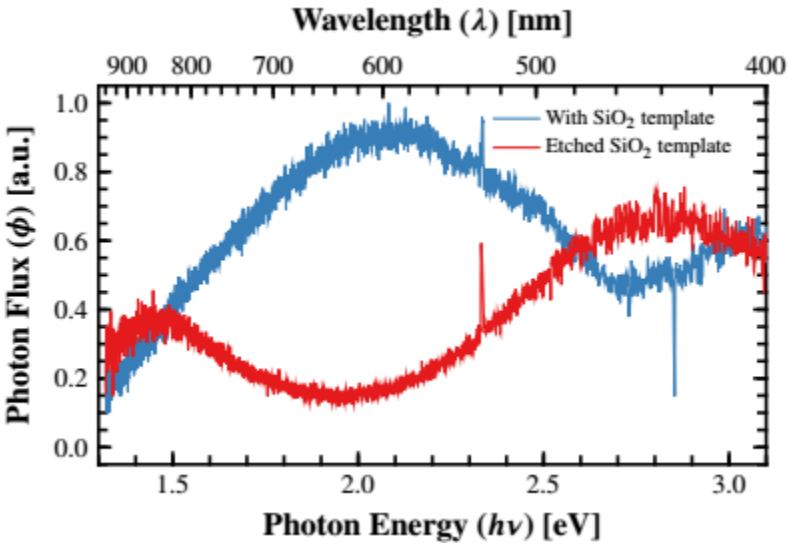

Figure 3-25. Photoluminescence spectra of 30 nm as deposited c-Si metalattice before (blue) and after (red) template removal. Credit: Alex Grede.

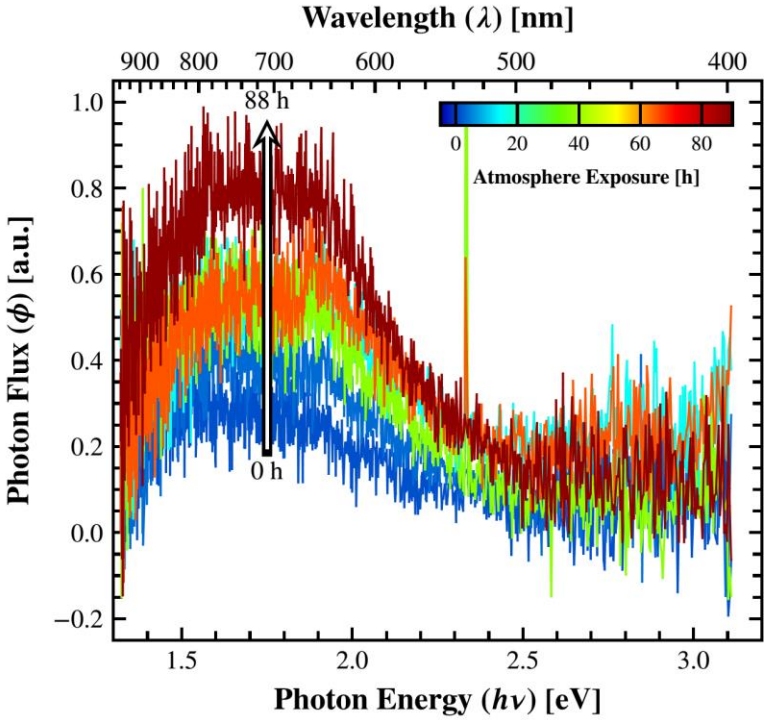

Figure 3-26. Photoluminescence spectra of 30 nm c-Si metalattice after template removal with varying atmosphere exposure time. Credit: Alex Grede.

We also examined the PL properties of 30 nm Ge metalattice, which has similar behavior compared to 30 nm Si metalattice (**Figure 3-27**). In collaboration with Alex Grede and Prof. Noel Giebink from Electrical Engineering of Pennsylvania State University, we proposed the recombination mechanism as the following, semiconductor metalattice (Si or Ge) are excited by photons from the incident beam. During the relaxation process, the excited electron travels toward the surface and thermalizes in the silica template instead of in the semiconductor to emit light (**Figure 3-28**). This proposed mechanism explain why both Si and Ge metalattices, two very different semiconductors with bandgap at 1.1 eV and 0.66 eV respectively, have very similar PL behavior. In this proposed mechanism, the light emission process is controlled by the silica medium, therefore the two metalattices have nearly identical PL. Since surface states is the dominating PL mechanism, it would be beneficial to surface passivate the metalattices after template removal.

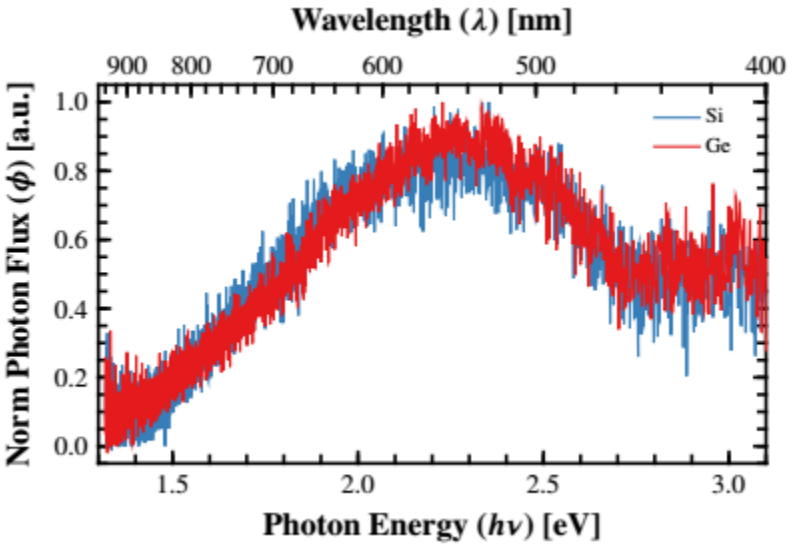

Figure 3-27. Photoluminescence spectra of 30 nm c-Si metalattice (blue) and c-Ge metalattice (red) before template removal. Credit: Alex Grede.

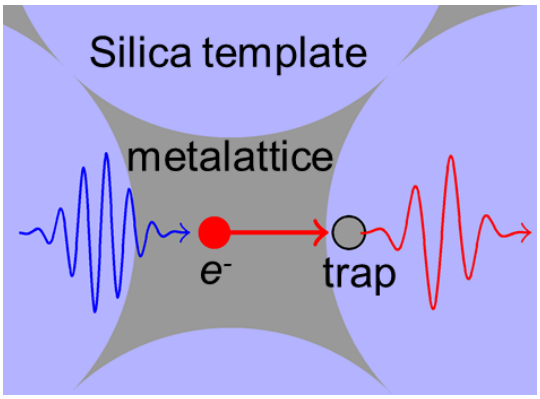

Figure 3-28. Proposed photoluminescence recombination mechanism of Si and Ge metalattices. Credit: Alex Grede.

3.8. Surface and Structure Modification using HPcCVD

The advance in template removal after HPcCVD synthesis of electronic metalattice provides a platform for tuning surface chemistry for interfacial design. Before template removal was successful, the Si and Ge metalattice structure always had a Si/SiO_2 or Ge/SiO_2 interface. Metalattices are a highly surfaced material. Surface passivation is very important in controlling properties such as enhanced light emitting performance by reducing recombination losses in the interface[58,59]. Many methods can be used to passivate the surface, for example silicon dangling bonds can be passivated using hydrogen[60] or surface doped by introducing a negative fixed charge using alumina (Al_2O_3)[61]. Crystalline silicon can also be passivated by other materials available by high pressure confined chemical vapor deposition (HPcCVD), such as amorphous silicon[58]. In addition to surface passivation, a compound metalattice made of an interlayer of two semiconductor can also be created by infiltrating a template removed parent metalattice with different materials. As a proof of concept, a silicon/germanium core shell structure was prepared by infiltrating a silicon metalattice immediately after template removal. The template was remove as described in the previous section then inserted into an HPcCVD reactor for the second

material deposition. Hydrofluoric acid (HF) etching of the silica template should provide a reliable hydrogen terminated silicon surface on the metalattice. Since the template removed Si metalattice was quickly put into the reactor and stored in inert gas (ultra high purity helium) or in vacuum, minimal oxidation should occur[56,57].

Raman spectroscopy was used to characterization the core/shell structure with an excitation wavelength of 633 nm (**Figure 3-29**). The penetration depth of Ge at 633 nm excitation is 32 nm [62] and was not able to probe the parent silicon metalattice because the top was covered by germanium (**Figure 3-30**). **Figure 3-30** shows a scanning electron microscopy image of the core-shell structure. A layer of germanium was deposited on top of the core-shell structure and the periodic structure remained ordered after template removal and the second infiltration.

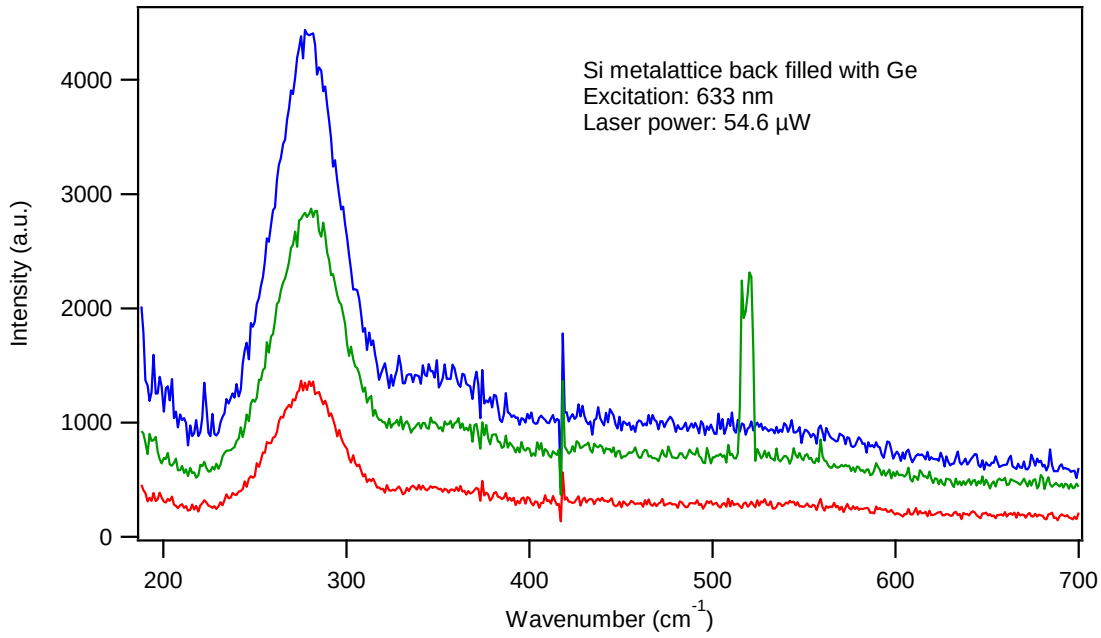

Figure 3-29. Raman spectra of as deposited Si/Ge core shell structure. Silicon signals cannot be seen in the spectra because the penetration depth Ge at 633 nm is only of 32 nm and the overlayer on top is too thick to allow the incident beam to probe the silicon layer.

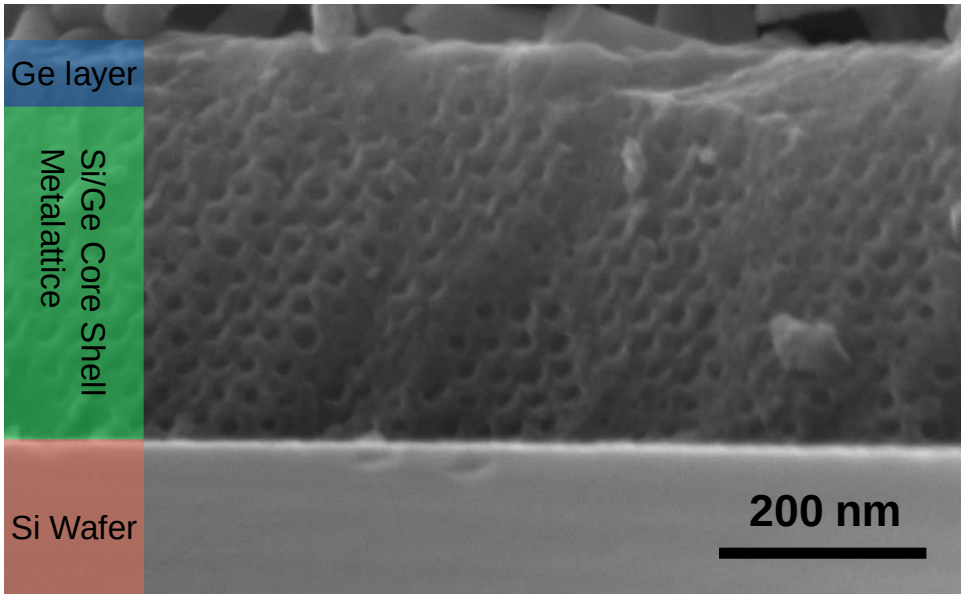

Figure 3-30. SEM image of the as synthesized Si/ Ge core shell metalattice structure. The structure remained ordered after the second infiltration.

Transmission electron microscope (TEM) was also used to characterize the Si/ Ge core shell structure. The sample was prepared by using a focused ion beam by slicing a thin film of the metalattice and transferring it to a TEM grid. **Figure 3-31** shows the ordered core shell structure and energy dispersive spectroscopy (EDS) elemental mapping of the as synthesized Si/Ge metalattice. The parent Si metalattice (shown in red in **Figure 3-31**, right) is evenly coated by Ge during the second HPcCVD infiltration. The reversed structure, where silicon is used to coat a Ge metalattice structure can also be made by switching the order of gas chemistry. A Ge/Si core shell structure can be used to surface passivate the germanium layer with SiGe alloy, which forms during thermal annealing of the Ge layer. The optical characterization of effectiveness in Ge passivation in such structure will be carried out by Pratibha Mahale (under the supervision of Prof. Thomas Mallouk) and Alex Grede (under the supervision of Prof. Noel Giebink) and they will continue to investigate in that area.

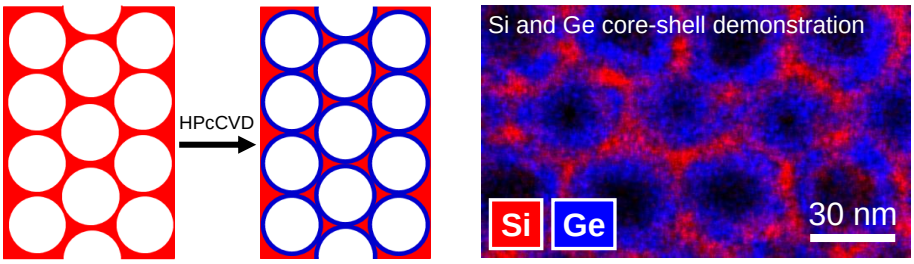

Figure 3-31. Si/ Ge core shell metalattice structure. (Left) Illustration of core shell metalattice preparation. A second layer of material is deposited after template removal using HPcCVD. (Right) TEM EDS mapping of Si/ Ge core shell metalattice. TEM credit: Shih-Ying Yu.

3.9. Quantum Confinement through Electron Energy Loss Spectroscopy

Although the PL studies in previous section suggest the dominating recombination mechanism arises from surface state between the metalattice and the silica colloidal crystal template, it is important to know if quantum confinement effects exist in metalattices for further properties tuning. For example, we can learn to passivate the surface to eliminate surface effects if quantum confinement effects exhibit in metalattices. Electron energy loss spectroscopy (EELS) was used to study local electronic structure information[63–66]. The work on electron energy loss spectroscopy (EELS) is in collaboration with Dr. Shih-Ying Yu from the group of Prof. Suzanne Mohney from Pennsylvania State University. Scanning transmission electron microscopy (STEM) with high spatial and energy resolution was used to probe the different meta-atom and meta-bond sites. **Figure 3-32** shows the core-loss EELS spectra of Si $L_{2,3}$ edge of 30 nm Si metalattice probing meta-bond, tetrahedral and octahedral sites compared to bulk single crystalline Si substrate. The Si $L_{2,3}$ edge represents the energy differcet between the bottom of the conduction band relative to the Si 2p core level. Si $L_{2,3}$ energy varies depending on the quantum confinement level[64–66]; Si $L_{2,3}$ core energy loss increases as the bandgap expands due to quantum confinement. The Si substrate underneath of the metalattice structure was used as a reference with a Si $L_{2,3}$ energy loss of 99.34 eV. When the electron beam was probing directly on

the octahedral, tetrahedral and meta-bond sites (**Figure 3-33**), blue shifts of Si $L_{2,3}$ energy loss at 99.67, 99.72 and 100 eV, respectively were observed. The shape of the Si $L_{2,3}$ edge at the metalattices sites are comparable to those observed in Si nanocrystals with a diameter less than 5 nm[63]. The blue shift can be explained by effective mass theory that predicts increase in conduction band energy with decreasing crystal size in smaller metalattices features (**Table 3-4**). The EELS studies showed that 3D interconnected Si metalattices does exhibit quantum confinement effects.

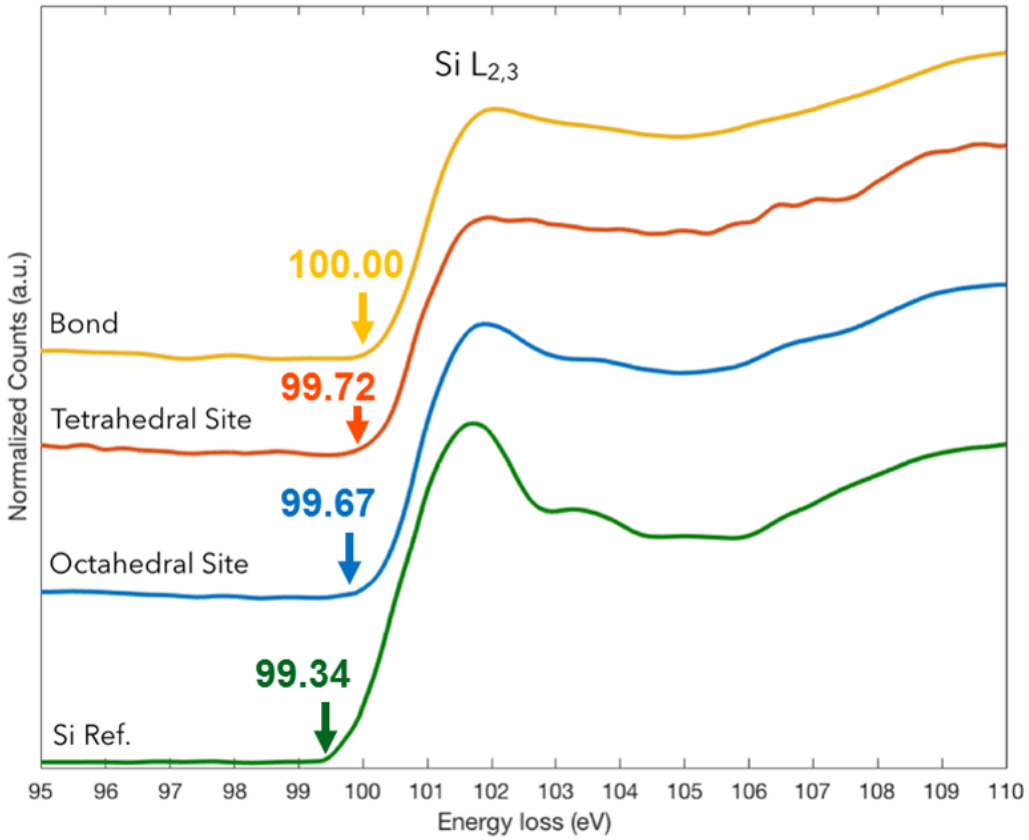

Figure 3-32. Electron Energy Loss Spectroscopy (EELS) Si $L_{2,3}$ edge core loss study of 30 nm silicon metalattice. EELS Credit: Shih-Ying Yu.

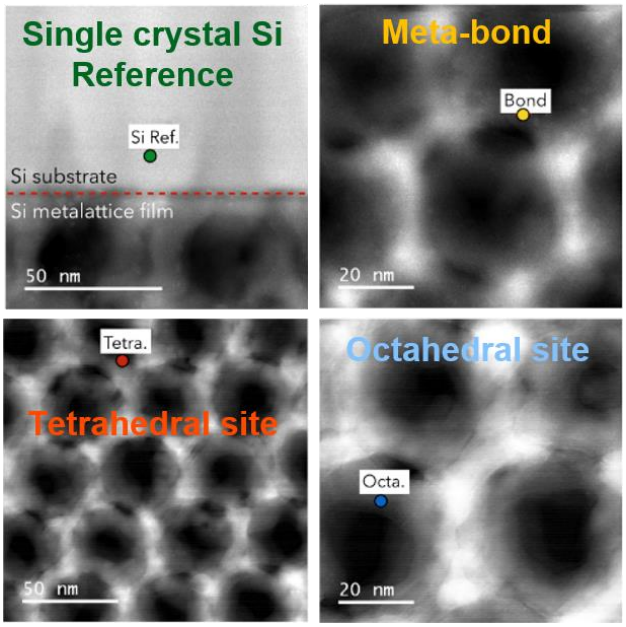

Figure 3-33. Representative HRTEM images of regions scanned for Si $L_{2,3}$ EELS. Silicon reference was taken on the single crystalline silicon substrate underneath the 30 nm metalattice sample. Multiple scans were taken at each meta-bond and meta-atom (tetrahedral and octahedral) sites. TEM credit: Shih-Ying Yu.

Table 3-4. 30 nm Si metalattice energy shifts in EELS Si $L_{2,3}$ edge under TEM.

Features	Energy shift from bulk Si	Size of shape
Meta-bond	0.66 eV	2 nm tube
Tetrahedral site	0.38 eV	7 nm
Octahedral site	0.33 eV	13 nm

3.10. Electrical and Thermal Properties

The 3-omega method was used to determine the thermal conductivity of 30 nm silicon metalattice (theoretical studies was in collaboration with Weinan Chen in Professor Isamila Dabo's research group at Pennsylvania University and characterization was in collaboration with Disha Talreja in Professor Venkatraman Gopalan's research group at Pennsylvania State University). Using Molecular dynamic simulation, it was predicted that the thermal conductivity

will decrease as the void volume increases inside of a metalattice (**Figure 3-34 (b)**) due to enhanced phonon scattering from the ordered porous nano-structure. The void volume in a perfect ordered template removed metalattice is 74 %. The thermal conductivity of c-Si 30 nm metalattice was found to be at 3.28 W/mK compared to bulk c-Si of 148 W/mK. The experimental results agrees very well with the calculated measurements.

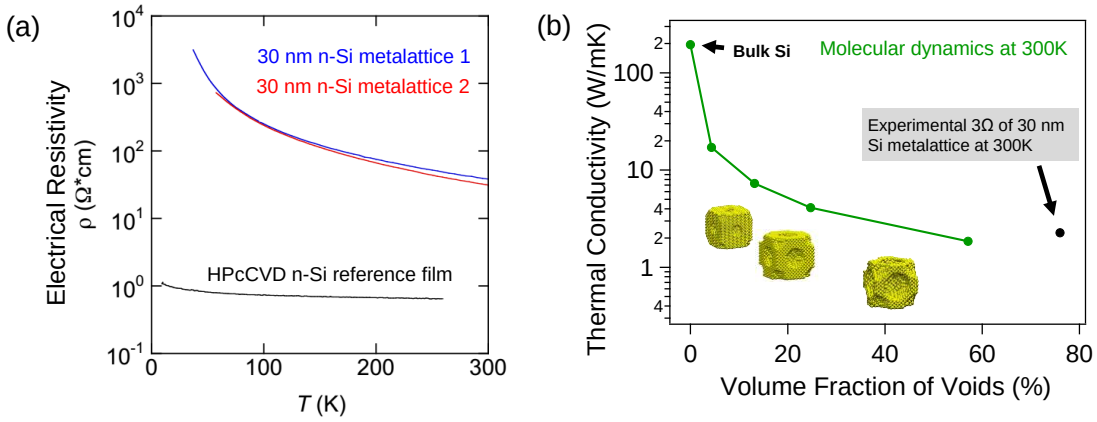

Figure 3-34. Electrical and thermal conductivity measurements of 30 nm n-Si and i-Si metalattice, respectively. Credit: Shaun Mills (electrical resistivity), Weinan Chen and Disha Talreja (thermal conductivity)

The Van der Pauw method, 4 probe current voltage measurements technique was used to determine the resistivity of metalattice from 4K to ~ 300K (In collaboration with Dr. Shaun Mills and Yixuan Chen from Professor Ying Liu's research group at Pennsylvania State University). The electrical conductivity of HPcCVD Si films and metalattices were increased by introducing dopants in the gas mixture. Phosphine (PH_3) was added to the gas mixture to deposit n-Si materials. Various amount of PH_3 can be added using the gas loading system shown in **Chapter 2** to tune the dopant concentration. Temperature dependent electrical resistivity was measured with n-Si metalattices doped with phosphorous by introducing PH_3 in the precursor gas mixture.

The dopant concentration of the n-Si metalattice was found to have an average dopant concentration of $1.23 \times 10^{21} atoms/cm^3$. The resistivity of a HPcCVD thin film was also measured to compare to the metalattice structure. Although the metalattice was found to be electrically conductive, metalattices' resistivity was much higher than of the HPcCVD thin film made of same doping level.

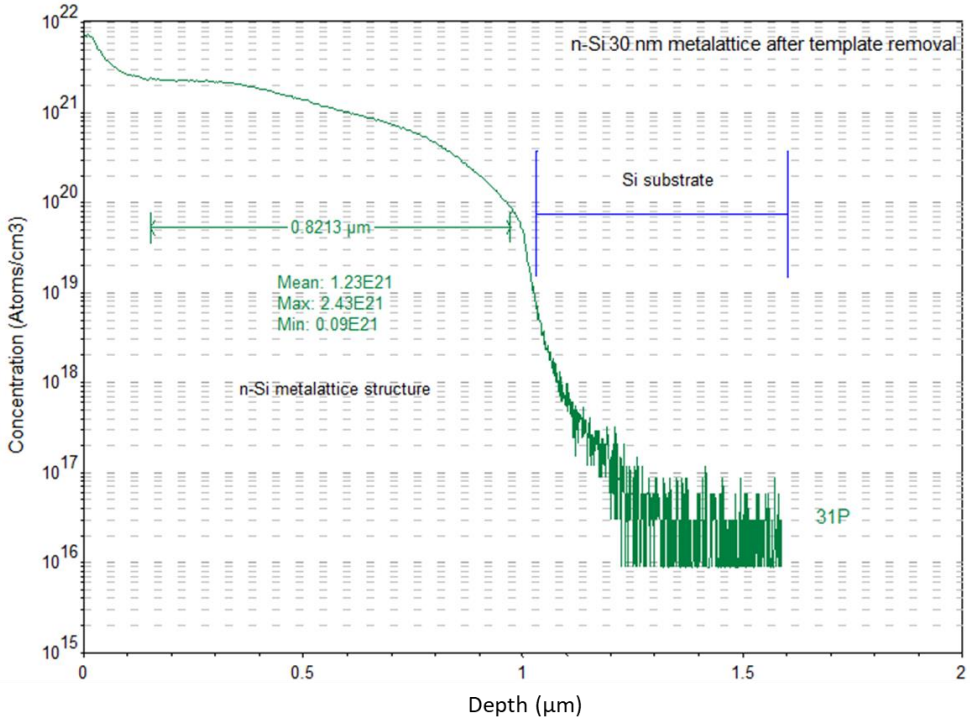

Figure 3-35. Secondary ion mass spectrometry of n-Si metalattice after template removal.

Although the silicon metalattice was heavily doped (from SIMS analysis, **Figure 3-35**), the electrical conductivity of 30 nm n-Si metalattice was significantly lower than that of HPcCVD n-Si thin film. The meta-bond thickness in a 30 nm metalattice is 2 nm in diameter and might not be large enough for a sufficient amount of charge carrier to transport through the meta-atoms. It is also possible that a smaller amount of charge carrier is deposited in the meta-bond regions due

to different gas transport rates of PH_3 compared to SiH_4. The meta-bond thickness can be increased in the HPcCVD synthesis process in an attempts to increase the electrical conductivity of the metalattice. **Figure 3-36** shows the SEM images of a metalattice after meta-bond thickness increase. A second HPcCVD infiltration process of the same materials can be used to deposit a layer of Si in the original metalattice structure, thus increasing the meta-bond thickness and decreasing the void volume. In addition to increasing electrical conductivity, tuning of void volume via second infiltration can also be used to tune thermal properties as suggested by the theoretical prediction of Si metalattice thermal conductivity in **Figure 3-34 (b)**. Further electrical and thermal characterization of the improved structure will be needed to confirm the properties of the improved structure, which will be carried out by Disha Talreja and Yixuan Chen.

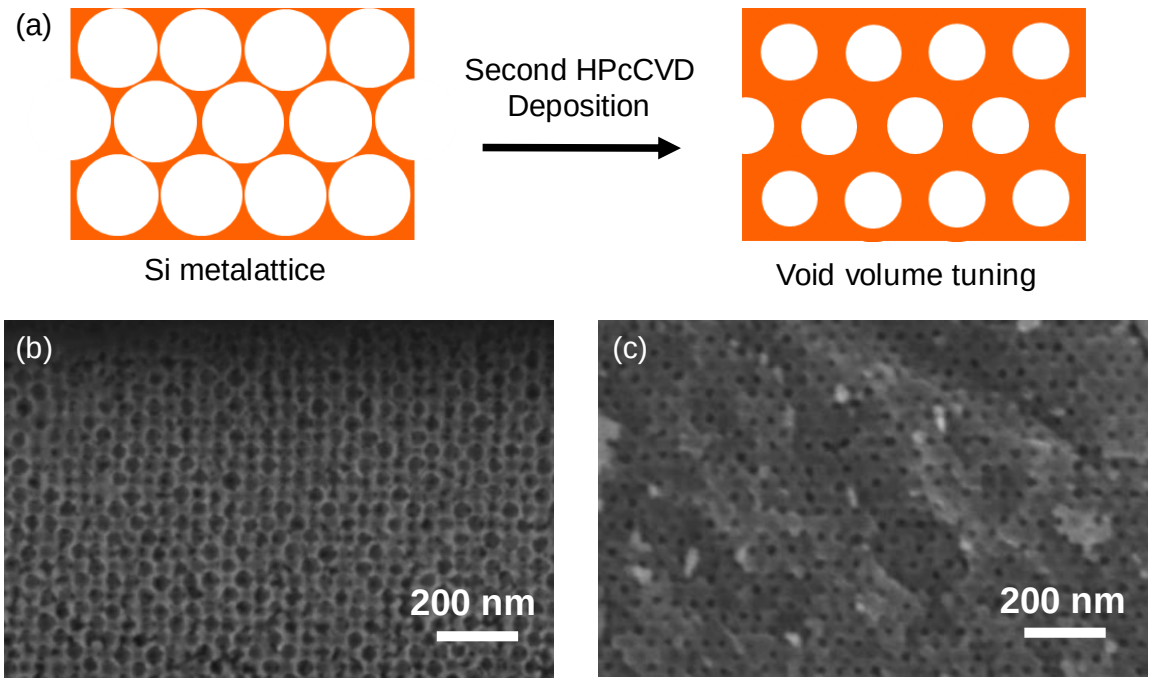

Figure 3-36. Meta-bond thickness tuning by re-growing the metalattice structures with HPcCVD after template removal.

3.11. Conclusion and Future Prospects

The use of silica colloidal crystal and HPcCVD infiltration of elemental semiconductor is a versatile synthetic route to fabricate an electronic metalattices structure. HPcCVD allows for independent tuning of chemical composition, surface chemistry, interfacial designs and void volume of metalattices, and colloidal crystal allows of control over sizes, periodicity and symmetry. Chemical composition is tuned by gas phase chemistry in HPcCVD, surface chemistry and interfacial design is varied by surface treatment followed by template removal, void volume is altered by HPcCVD regrowth after template removal and the sizes, periodicity and symmetry is controlled by selecting different nano-templates for infiltration. This chapter has shown the possibility of synthesizing metalattices that matches the length-scale of many physical processes, including electron, phonon and exciton mean free paths. The synthetic realization of electronic metalattices permits for study of physical properties and structural relationship. Further studies on detailed characterization, such as thermal and electrical transport, optical responses, and quantum confinement effects on metalattices of varying periodicity, chemical composition, surface chemistry and porosity will help to develop such structural order/ properties relationship, which could one day lead us one step closer to designable materials by controlling physical properties during synthesis.

The synthetic route shown here is flexible and preserves many degrees of freedom in designing the final structure of metalattices; in terms of the metalattice structures shown in Chapter 3, several steps could be taken to improve the materials quality. First, control over dopant types and concentration. The n-doped silicon and germanium metalattices shown here are created by introducing phosphine (PH_3) to the gas mixture to intentionally add impurities to the metalattices structure. However, the HPcCVD gas phase method had difficulties in introducing p-type dopants, such as boron by using diborane (B_2H_6), into the metalattice structure. Even

when a high concentration of diborane (30:1 of SiH_4 and B_2H_6) was used, the electrical properties of the final product did not improve compared to HPcCVD intrinsic silicon. We hypothesize that this is due to boron diffusion into silica glass at high temperature[67,68]. During HPcCVD of n-Si or high temperature annealing processes to yield crystalline Si metalattices, B travels to silica nanoparticles or the quartz substrate to form borosilicate glass. Phosphorus is less of an issue because its diffusion rate is expected to be much slower compared to boron[67] and most studies show P-diffusion occurs at elevated temperatures above those used in the HPcCVD or annealing processes[69,70]. To overcome the diffusion problem during post processing high temperature annealing, other doping techniques should be examined. For example, surface doping via molecular layer[71] could be used to introduce dopants, both n- and p- types to the metalattice after template removal and thermal annealing. Dopant introduction after template removal can prevent dopant diffusion to the silica nanoparticles.

The elemental semiconductor metalattices made in this dissertation are either amorphous or polycrystalline. It would be advantageous to achieve single crystalline materials as that could increase materials quality and improve electrical transport through larger grain sizes. To achieve single crystalline silicon or germanium metalattices, two different areas can be examined, thermal processing from a-Si or a-Ge to single crystal materials and direct growth of single crystalline Si and Ge by HPcCVD. First is by laser annealing of the as deposited amorphous materials, where we have already shown success in fabricating long single crystalline Si [37] and Ge [36] micro-wires. A single crystalline wafer of Si or Ge could be used as the seed to promote single crystal growth through the metalattice (**Figure 3-37**).

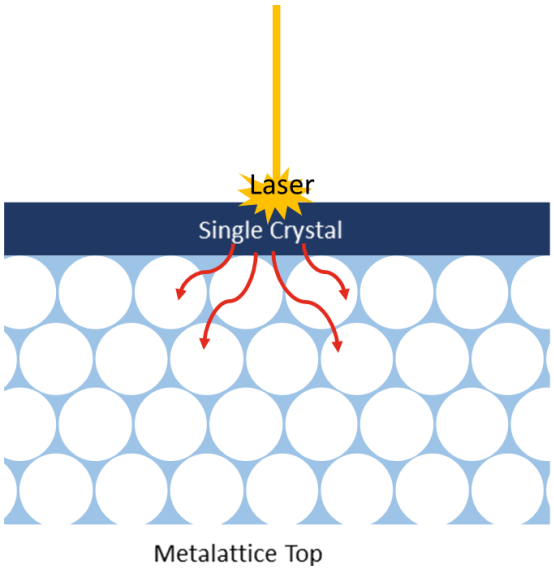

Figure 3-37. Laser annealing of Si or Ge metalattices. The laser incident beam will be introduced from the back of the substrate made with either single crystal Si or Ge to propagate the crystal growth from wafer to the metalattice.

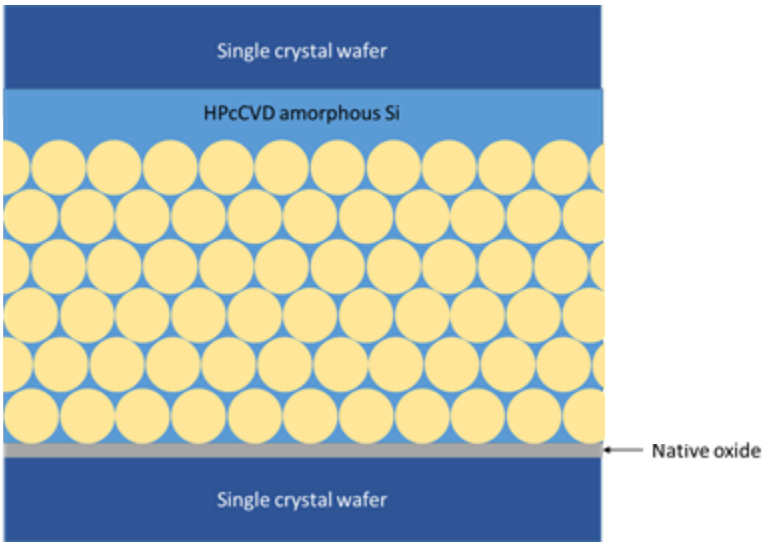

Figure 3-38. Epitaxial regrowth of a-Si metalattice to single crystal Si metalattice.

Another possible post processing method is by solid phase epitaxial regrowth of a-Si or polycrystalline Si to single crystalline Si [72]. The metalattice structure can be fabricated between two single crystalline Si wafer (**Figure 3-38**). The top Si wafer can be passivated by HF acid prior to infiltration, then placed on top of the templated Si substrate to sandwich the metalattice.

The top wafer is needed because native oxide cannot be present in this method, and the native oxide under the template cannot be removed prior to infiltration as HF acid also chemically removes the silica nanoparticle template. When the native oxide on the top surface is minimized, epitaxial regrowth could be encouraged for single crystal metalattice growth.

To address direct single crystal growth using HPcCVD, epitaxial gas phase deposition of Si and Ge should be examined. The kinetics studies shown in chapter 2 can serve as a guide to determine the best reaction conditions for Si epitaxial CVD using silane pyrolysis. Generally, slow growth of Si from a single crystalline Si wafer is needed for proper atomic arrangement as the precursors decompose near the surface.

3.12. References

1. Chomski, B. E. & Ozin, G. A. Panoscopic Silicon-A Material for 'All' Length Scales. *Adv. Mater.* **12,** 1071–1078 (2000).
2. Hochbaum, A. I. *et al.* Enhanced thermoelectric performance of rough silicon nanowires. *Nature* **451,** 163–168 (2008).
3. Boukai, A. I. *et al.* Silicon nanowires as efficient thermoelectric materials. *Nature* **451,** 168–171 (2008).
4. Han, J. & Crespi, V. Tuning Fermi-Surface Properties through Quantum Confinement in Metallic Metalattices: New Metals from Old Atoms. *Phys. Rev. Lett.* **86,** 696–699 (2001).
5. Han, J. & Crespi, V. Abrupt Topological Transitions in the Hysteresis Curves of Ferromagnetic Metalattices. *Phys. Rev. Lett.* **89,** 197203 (2002).
6. Richman, E. K., Kang, C. B., Brezesinski, T. & Tolbert, S. H. Ordered mesoporous silicon through magnesium reduction of polymer templated silica thin films. *Nano Lett.* **8,** 3075–3079 (2008).
7. Sun, D. *et al.* Hexagonal nanoporous germanium through surfactant-driven self-assembly of Zintl clusters. *Nature* **441,** 1126–1130 (2006).
8. Armatas, G. S. & Kanatzidis, M. G. Hexagonal Mesoporous Germanium. *Science (80-.).* **313,** 817–820 (2006).
9. Sazio, P. J. A. *et al.* Microstructured Optical Fibers as High-Pressure Microfluidic Reactors. *Science (80-.).* **311,** 1583–1586 (2006).
10. He, R., Day, T. D., Sparks, J. R., Sullivan, N. F. & Badding, J. V. High Pressure Chemical Vapor Deposition of Hydrogenated Amorphous Silicon Films and Solar Cells. *Adv. Mater.* **28,** 5939–5942 (2016).
11. Baril, N. F. *et al.* Confined high-pressure chemical deposition of hydrogenated amorphous

silicon. *J. Am. Chem. Soc.* **134,** 19–22 (2012).

12. Baril, N. F. *et al.* High-Pressure Chemical Deposition for Void-Free Filling of Extreme Aspect Ratio Templates. *Adv. Mater.* **22,** 4605–4611 (2010).
13. Sparks, J. R., Sazio, P. J. A., Gopalan, V. & Badding, J. V. Templated Chemically Deposited Semiconductor Optical Fiber Materials. *Annu. Rev. Mater. Res.* **43,** 9.1-9.31 (2013).
14. Hartlen, K. D., Athanasopoulos, A. P. T. & Kitaev, V. Facile Preparation of Highly Monodisperse Small Silica Spheres (15 to >200 nm) Suitable for Colloidal Templating and Formation of Ordered Arrays. *Langmuir* **24,** 1714–1720 (2008).
15. Watanabe, R. *et al.* Journal of Colloid and Interface Science Extension of size of monodisperse silica nanospheres and their well-ordered assembly. *J. Colloid Interface Sci.* **360,** 1–7 (2011).
16. Russell, J. L., Noel, G. H., Warren, J. M., Tran, N. L. & Mallouk, T. E. Binary Colloidal Crystal Films Grown by Vertical Evaporation of Silica Nanoparticle Suspensions. *Langmuir* **33,** 10366–10373 (2017).
17. Russell, J. L. & Mallouk, T. E. Double Replication of Silica Colloidal Crystal Films. *ACS Appl. Mater. Interfaces* **9,** 42075–42083 (2017).
18. Ye, Y., Leblanc, F., Haché, A. & Truong, V. Self-assembling three-dimensional colloidal photonic crystal structure with high crystalline quality. *Appl. Phys. Lett.* **78,** 52–54 (2001).
19. Perez, R. & Gumbsch, P. An AB initio study of the cleavage anisotropy in silicon. *Acta Mater.* **48,** 4517–4530 (2000).
20. Pérez, R. & Gumbsch, P. Directional Anisotropy in the Cleavage Fracture of Silicon. *Phys. Rev. Lett.* **84,** 5347–5350 (2000).
21. Lowell, S., Shields, J. E., Thomas, M. A. & Thommes, M. *Characterization of Porous Solids and Powers: Surface Area, Pore Size and Density*. (Kluwer Academic Publishers,

2004).

22. Gidley, D. W., Peng, H. & Vallery, R. S. Positron Annihilation as a method to characteriza porous materials. *Annu. Rev. Mater. Res.* **36,** 49–79 (2006).

23. Gidley, D. W. *et al.* Positronium annihilation in mesoporous thin films. *Phys. Rev. B* **60,** R5159 (1999).

24. Li, S. *et al.* Evaluation of Pore Structure in Pure Silica Zeolite MFI Low- k Thin Films Using Positronium Annihilation Lifetime Spectroscopy. *J. Phys. Chem. B* **108,** 11689–11692 (2004).

25. Sun, J., Gidley, D. W., Hu, Y., Frieze, W. E. & Ryan, E. T. Depth-profiling plasma-induced densification of porous low-k thin films using positronium annihilation lifetime spectroscopy. *Appl. Phys. Lett.* **81,** 1447–1449 (2002).

26. Ruckdeschel, P., Kemnitzer, T. W., Nutz, F. A., Senker, J. & Retsch, M. Hollow silica sphere colloidal crystals: insights intocalcination dependent thermal transport. *Nanoscale* **7,** 10059–10070 (2015).

27. Yoo, C. S. *Semiconductor manufacturing technology*. (World Scientific Publishing Company, 2008).

28. Jansen, H., Gardeniers, H., de Boer, M., Elwenspoek, M. & Fluitman, J. Related content microtechnology A survey on the reactive ion etching of silicon in microtechnology. *J. Micromechanics Microengineering* **6,** 14–28 (1996).

29. Shul, R. J. & Pearton, S. J. *Handbook of Advanced Plasma Processing Techniques*. (Springer-Verlag Berlin Heidelberg, 2000).

30. Rangelow, I. W. & Fichelscher, A. reactive ion etching Si-trench etching. in *SPIE 1392, Advanced Techniques for Integrated Circuit Processing* 240–245 (1990). doi:10.1117/12.48918

31. Oehrlein, G. S., Bestwick, T. D., Jones, P. L., Jaso, M. A. & Lindstrom, J. K. Selective

Dry Etching of Germanium with Respect to Silicon and Vice Versa. *J. Electrochem. Soc.* **138,** 1443–1452 (1991).

32. Rueger, N. R. *et al.* Selective etching of SiO 2 over polycrystalline silicon using CHF 3 in an inductively coupled plasma reactor. *J. Vac. Sci. Technol. A* **17,** 2492–2502 (1999).
33. Bo, X., Yao, N., Shieh, S. R., Duffy, T. S. & Sturm, J. C. Large-grain polycrystalline silicon films with low intragranular defect density by low- temperature solid-phase crystallization without underlying oxide. *J. Appl. Phys.* **91,** 2910–2915 (2002).
34. Kamins, T. I. & Greenwald, A. C. Pulsed-electron-beam annealing of polycrystalline-silicon films. *Appl. Phys. Lett.* **35,** 282–285 (1979).
35. Mandurah, M. M., Saraswat, K. C. & Kamins, T. I. Phosphorus Doping of Low Pressure Chemically Vapor-Deposited Silicon Films. *J. Electrochem. Soc.* **126,** 1019–1023 (1977).
36. Ji, X. *et al.* Single-Crystal Germanium Core Optoelectronic Fibers. *Adv. Opt. Mater.* **5,** 1600592 (2017).
37. Healy, N. *et al.* Extreme electronic bandgap modification in laser-crystallized silicon optical fibre. *Nat. Mater.* **13,** 1122–1127 (2014).
38. Ji, X. *et al.* Single-Crystal Silicon Optical Fiber by Direct Laser Crystallization. *ACS Photonics* **4,** 85–92 (2017).
39. Coefficient, T. H. E., Linear, O. F., Series, C. D. & Properties, M. in (ASM International).
40. Hatalis, M. K. & Greve, D. W. Large grain polycrystalline silicon by low-temperature annealing of low-pressure chemical vapor deposited amorphous silicon films. *J. Appl. Phys.* **63,** 2260–2266 (1991).
41. Zacharias, M. *et al.* Thermal crystallization of amorphous Si/SiO2 superlattices. *Appl. Phys. Lett.* **74,** 2614–2616 (1999).
42. Wan, Z., Huang, S., Green, M. A. & Conibeer, G. Rapid thermal annealing and crystallization mechanisms study of silicon nanocrystal in silicon carbide matrix.

Nanoscale Res. Lett. **6,** 129 (2011).

43. Huet, S., Viera, G. & Boufendi, L. Effect of small crystal size and surface temperature on the Raman spectra of amorphous and nanostructured Si thin films deposited by radiofrequency plasmas. *Thin Solid Films* **403–404,** 193–196 (2002).

44. Fauchet, P. M. & Campbell, I. H. Raman spectroscopy of low-dimensional semiconductors. *Raman Spectrosc. low-dimensional Semicond.* **14,** s79–s101 (1988).

45. Zi, J. *et al.* Raman shifts in Si nanocrystals. *Appl. Phys. Lett.* **69,** 200–202 (1996).

46. Germain, P., Zellama, K., Squelard, S., Bourgoin, J. C. & Gheorghiu, A. Crystallization in amorphous germanium. *J. Appl. Phys.* **50,** 6986–6994 (1979).

47. Chen, H. S. & Turnbull, D. Specific Heat and Heat of Crystallization of Amorphous Germanium Thermal conductivity of sputtered amorphous Ge films. *J. Appl. Phys.* **40,** 4214–4215 (1969).

48. Rahim, A. F. A. *et al.* Applied Surface Science Self-assembled Ge islands and nanocrystals by RF magnetron sputtering and rapid thermal processing : The role of annealing temperature. *Appl. Surf. Sci.* **275,** 193–200 (2013).

49. Choi, W. K., Ho, Y. W. & Ng, V. Effect of size of Ge nanocrystals embedded in SiO2 on Raman spectra. *Mater. Phys. Mech.* **4,** 46–50 (2001).

50. Griining, U. & Yelon, A. Capillary and Van der Waals forces and mechanical stability of porous silicon. *Thin Solid Films* **255,** 135–138 (1995).

51. Bisi, O., Ossicini, S. & Pavesi, L. Porous silicon : a quantum sponge structure for silicon based optoelectronics. *Surf. Sci. Rep.* **38,** 1–126 (2000).

52. Cullis, A. G., Canham, L. T. & Calcott, P. D. J. The structural and luminescence properties of porous silicon. *J. Appl. Phys.* **82,** 909–965 (1997).

53. Grigoryev, B. A., N, B. V, Kurumov, D. S. & Sengers, J. V. Surface Tension of Normal Pentane , Hexane , Heptane , and Octane. *Int. J. Thermophys.* **13,** 453–464 (1992).

54. Zhamu, A. & Jang, B. Z. Mass production of pristine nano graphene materials. (2012).

55. Dutta, A. K. Visible photoluminescence from Ge nanocrystal embedded into a SiO2 matrix fabricated by atmospheric pressure chemical vapor deposition. *Appl. Phys. Lett.* **68,** 1189–1191 (1996).

56. Hirashita, N., Kinoshita, M., Aikawa, I. & Ajioka, T. (100) surfaces Effects of surface hydrogen on the air oxidation at room temperature of HF, treated SI (100) surfaces. *Appl. Phys. Lett.* **56,** 451–453 (1990).

57. Niwano, M. *et al.* Infrared spectroscopy study of initial stages of oxidation of hydrogen terminated Si surfaces stored in air. *J. Appl. Phys.* **76,** 2157–2163 (1994).

58. Dan, Y. *et al.* Dramatic Reduction of Surface Recombination by in Situ Surface Passivation of Silicon Nanowires. *Nano Lett.* **11,** 2527–2532 (2011).

59. Aberle, A. G. Crystalline Silicon Solar Cells: A Review. *Prog. Photovolt Res. Appl.* **8,** 473–487 (2000).

60. Fenner, D. B., Biegelsen, D. K. & Bringans, R. D. Silicon surface passivation by hydrogen termination : A comparative study of preparation methods. *J. Appl. Phys.* **66,** 419–424 (1989).

61. Hoex, B., Schmidt, J., Pohl, P., van de Sanden, M. C. M. & Kessels, W. M. M. Silicon surface passivation by atomic layer deposited Al2O3. *J. Appl. Phys.* **104,** 44903 (2008).

62. Horiba Scientific. *Strain measurements of a Si cap layer deposited on a SiGe substrate determination of Ge content*.

63. Batson, P. E. & Heath, J. R. Electron Energy Loss Spectroscopy of Single Silicon Nanocrystals: The Conduction Band. *Phys. Rev. Lett.* **71,** 911–914 (1993).

64. Mitome, M., Yamazaki, Y., Takagi, H. & Nakagiri, T. Size dependence of plasmon energy in Si clusters. *J. Appl. Phys.* **72,** 812–814 (1992).

65. Hanrath, T. & Korgel, B. A. A Comprehensive Study of Electron Energy Losses in Ge

Nanowires. *Nano Lett.* **4,** 1455–1461 (2004).

66. Nguyen, P. D., Kepaptsoglou, D. M., Ramasse, Q. M. & Olsen, A. Direct observation of quantum confinement of Si nanocrystals in Si-rich nitrides. *Phys. Rev. B* **85,** 85315 (2012).

67. Shimakura, K., Suzuki, T. & Yadoiwa, Y. Boron and phosphorus diffusion through an SiO2layer from a doped polycrystalline Si source under various drive-in ambients. *Solid State Electron.* **18,** 991–996 (1975).

68. Aoyama, T. *et al.* Effect of fluorine on boron diffusion in thin silicon dioxides and oxynitride. *J. Appl. Phys.* **77,** 417–419 (1995).

69. Ghoshtagore, R. N. Silicon dioxide masking of phosphorus diffusion in silicon. *Solid State Electron.* **18,** 399–406 (1975).

70. Ghoshtagore, R. N. Phosphorus diffusion processes in SiO2 films. *Thin Solid Films* **25,** 501–513 (1975).

71. Ho, J. C. *et al.* Controlled nanoscale doping of semiconductors via molecular monolayers. *Nat. Mater.* **7,** 62–67 (2008).

72. Ghannam, M. Y. & Dutton, R. W. Solid phase epitaxial regrowth of boron-doped polycrystalline silicon deposited by low-pressure chemical vapor deposition. *Appl. Phys. Lett.* **51,** 611–613 (1987).

Chapter 4

Compound Semiconductor Metalattices

The combination of high pressure confined chemical vapor deposition (HPcCVD) and nano-templates opens a platform in creating metalattice structures that previously could not be made with electrical interconnectivity, while preserving quantum confinement. The results in the first sets of elemental semiconductor silicon and germanium metalattices provided us the opportunity to study well-ordered 3D structural materials. However, there is only a short list of elemental semiconductors, which limits what materials a metalattice could be made of. HPcCVD of compound semiconductors infiltrated in nano-templates to fabrication electronic metalattices could lead to endless tuning of structural materials and physical properties. However, compound semiconductors deposited using high pressure CVD presents its own challenge. Gas phase chemistry is more complex than of unary semiconductors and requires the addition of multiple precursors to yield a compound semiconductor[1–3].

Conventional CVD, including low pressure and atmospheric pressure, and atomic layer deposition (ALD) have the advantage of storing each precursor independently and each gas is sent into the reaction chamber by its own gas line. Due to the low pressure used in conventional CVD, reactants do not react until they meet near the heating zone to decompose and further deposit materials. High pressure is needed in metalattice fabrication for hydrodynamic mass transport of precursor gases into small trenches of pores. In high pressure CVD, reactivity between different precursors must be considered. The rise in pressure increases molecular collision and thus gas precursors could react with each other more rapidly, even at room temperature. All precursors and carrier gas are stored in one gas reservoir before being

introduced to the deposition zone for ease of experimental apparatus design. Therefore, precursors in well-developed conventional CVD chemistry might not be transferable to HPCVD; precursors must be chosen carefully in high pressure systems to prevent pre-reaction in gas reservoirs. In addition, materials growth mechanism could be very different in high pressure systems because pressure alters chemical thermodynamics and reactor geometry must be carefully considered as shown in *Chapter 2***.**

We have seen many successes in high pressure chemical vapor deposition of II-VI semiconductors, such as ZnSe[1,3], ZnS[1] and ZnO in silica capillaries to fabricate optical fibers. The gas phase chemistry could be adopted to HPcCVD for conformal coatings in thin film and nano-porous templates. As a first step to realizing compound semiconductor metalattices, ZnSe was used as a test materials to infiltrate silica colloidal crystal templates for its wide band gap and excellent optical transmission at 500 – 22000 nm.

4.1. Zinc Selenide

Zinc selenide (ZnSe) has been studied widely for many potential applications, such as light emitting diodes[4], blue light/ laser source[5,6] and solar cells[7]. In addition, ZnSe nanoparticles have drawn attention from optoelectronic applications to photocatalysis[8,9] and biomedial labels[9–11]. ZnSe is a wide bandgap compound semiconductor with a direct bandgap of 2.67 eV[9,12] and an exciton binding energy of 21 meV[9,12] at room temperature. ZnSe has a exciton Bohr radius of 3.8 nm[7], where recent studies have shown promising results in utilizing quantum confinement effects in ZnSe quantum dots in silica/ epoxy composites for use as a solid state white light emitting diodes device[4,13]. ZnSe inside of a metalattice of appropriate sizes, such as in 14 nm silica colloidal crystal, could provide a way of synthesizing uniform sizes of quantum confined ZnSe

nano-crystallites with tunable bandgap, yet electrically interconnected structure for application such as optoelectronics, LEDs and catalysis.

4.2. HPCVD of Zinc Selenide

High pressure chemical vapor deposition of zinc selenide (ZnSe) in silica capillaries was previously reported by Sparks and coworkers, where centimeters long ZnSe optical fibers was made by deposition inside of silica capillaries[1,3]. In conventional CVD, dimethyl zinc ($(CH_3)_2Zn$) and hydrogen selenide (H_2Se) are used with low concentration of reactants[14]. It is well known that the two precursors does react at home temperature and could cause homogeneous gas phase reaction[15] (particle formation in gas phase). These two precursors were not suitable for HPCVD. An organometallic precursors encapsulation method was developed by Sparks et al[1] using the following chain reactions,

$$(CH_3)_2Zn + H_2 \rightarrow Zn + 2\ CH_4 \qquad \textbf{(Reaction 4-1)}$$

$$(CH_3)_2Se + 2\ H_2 \rightarrow H_2Se + 2\ CH_4 \qquad \textbf{(Reaction 4-2)}$$

$$Zn + H_2Se \rightarrow ZnSe + H_2 \qquad \textbf{(Reaction 4-3)}$$

The precursor gas ratio needs to be carefully controlled to yield ZnSe of the proper stiochiometry. High pressure CVD of ZnSe uses precursors that has fairly large by-products as compared to silicon or germanium deposition. In Si and Ge HPCVD, hydrides are used and the only by product is hydrogen gas, which can diffuse through most templates including the fused silica walls. However, methane is too large to diffuse through silica; if methane is not removed from the system, deposition slows down and eventually cease as it builds up near the deposition zone[1,2]. A mean of gas flow is needed in HPCVD of ZnSe to ensure new precursor gases are being carry into the deposition zone and by products are being exhaust out of the system downstream.

The total pressure used in HPCVD of ZnSe is at 35 – 70 MPa for a deposition zone temperature of 350 – 500 °C. The temperature used varies depending on reactant ratios and pressures used. In the case of optical fibers, the flow stops and terminates the reaction when the central pore is clogged or narrowed to less than 500 nm. ZnSe deposits as crystalline materials as opposed to Si and Ge where amorphous materials can be deposited. To translate HPCVD of ZnSe from 1D geometries (optical fiber) to 2D and 3D geometries (thin films and metalattices), the HPcCVD reactor geometry must be altered to adopt to the needs of an exhaust to remove by products. A flowing reactor was designed and machined as shown in **Figure 2-15** and the experimental set-up (**Figure 2-16**) is altered to allow for gas flow and flow rate is controlled by using different diameters silica capillaries.

4.3. Reactor Modification for 2D and 3D Zinc Selenide Materials

We hypothesize that a flowing reactor would allow byproducts to leave the deposition zone and bring in more precursors into the system. The HPcCVD reactor was designed as that there will be a constant flow from the gas reservoir to the outlet, where the outlet is connected to a silica capillary for flow rate control. The experimental details are similar to *Section 3.1.2.* for a-Si and a-Ge infiltration, but with slight modification to the spacer thickness, shapes, reactor geometries and experimental set-ups. Samples are prepared as described in *Section 3.1.2.*, but with 25 μm or 50 μm thickness of 304 stainless steel spacers. A flowing reactor was used and the outflow is connect to a 6 μm inner diameter silica capillary for flow rate control. The end silica capillary was sealed during the purging and vacuum process to ensure no air can return back into the HPcCVD experimental set-up. The silica capillary is cleaved after introduction of precursor gas and when the reactor reached deposition temperature. The reactor was held at 200 °C during purging and prior to raising to deposition temperature of 350 °C to 450 °C. Once flow is

established, the reaction will continue until flow stops or until total pressure of the experimental set-up drops below 20 MPa, whichever happens first. Electronic grade organometallic precursors are transferred into the gas reservoir using the high purity gas transfer line shown in *Section 2.4*. The stoichiometric ratio of dimethyl zinc and dimethyl selenium used varies ranging from VI/II of 2:1 to 4:1. The partial pressure of reactants is 0.1% in H_2 carrier gas with a total starting pressure of 40 – 45 MPa.

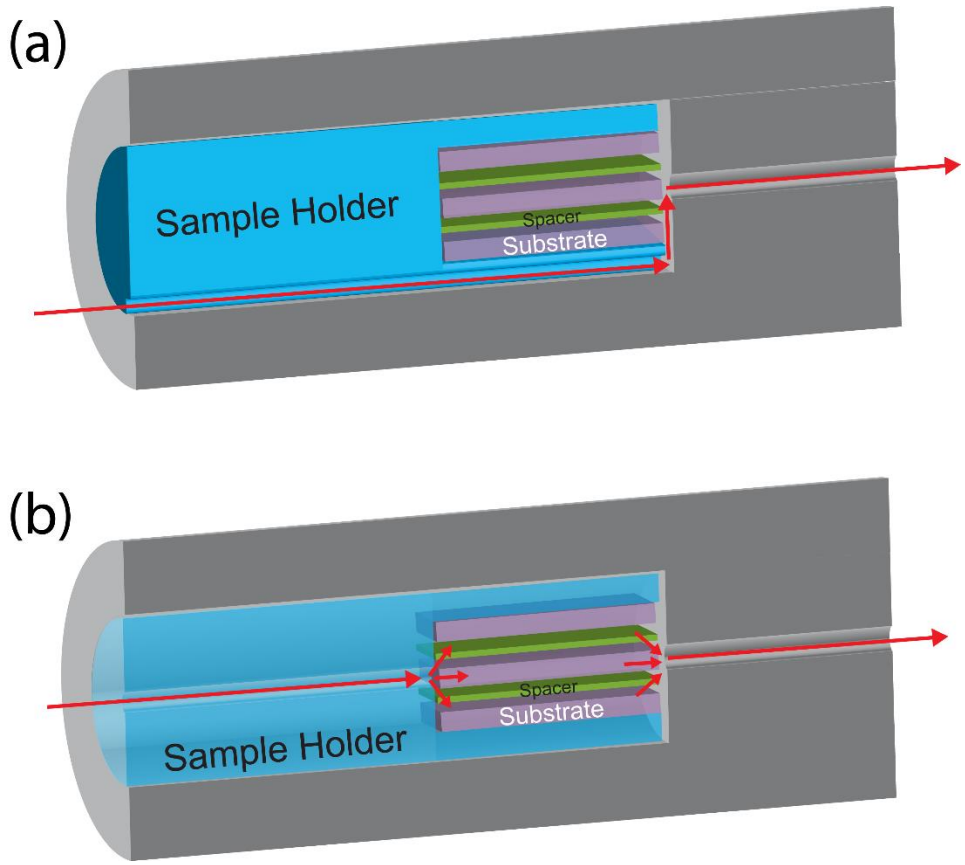

Figure 4-1. Schematic of sample holder and gas flow paths difference toward the samples. Red arrows depicts expected gas flow through the reactor. (a) The most plausible gas pathway is through the inlet from the bottom of the sample holder, bypassing the samples and only a limited amount of precursors can travel to the sample during the initial gas introduction before vent fiber was cut. This reactor set-up prevent additional precursor and carrier gas flow through the sample. (b) The gas must flow through the samples and spacers at all time during experiment if the gas inlet is placed in the center of the sample holder.

The sample holder geometry was found to be important in HPcCVD of ZnSe thin films and metalattices. A direct flow of precursor gases is need to encourage continuous by-products removal. **Figure 4-1** shows how different sample holders can affect gas flow directions. The red arrow indicates expected gas flow from the gas reservoir to the silica capillary exhaust. If the gas inlet is placed on the bottom of the sample holder, precursor gas would travel to the exhaust through the easiest path, by-passing the samples and failing to remove by-products. When sample holder as shown in **Figure 4-1 (a)** was used, little to no deposition was seen on the film. To increase direct gas flow through the sample during deposition, the sample holder was modified where gas inlet travels from the center of the rod to the templated substrates and leaves through the exhaust.

Table 4-1. HPcCVD of ZnSe based on spacer sizes and shapes

Thickness of spacer (μm)	Shape of spacer (**Figure 4-2**)	HPcCVD Deposition
25	U ⊥ to flow	No
25	U ∥ to flow	No
25	Strips ∥ to flow	Little to no deposition
50	U ⊥ to flow	No
50	U ∥ to flow	Little to no deposition
50	Strips ∥ to flow	Yes

In addition to sample holder geometry, the thickness, shape and positioning of the spacers was crucial in ZnSe HPcCVD thin film and metalattice deposition. The conditions tested for HPcCVD of ZnSe is summarized in **Table 4-1**. The most effective condition was when using 50 μm thick spacers with a parallel strips shape (**Figure 4-2 (c)**). Spacers with parallel strips was overall most effect with both 25 μm and 50 μm thickness, but less confinement (50 μm) showed more materials deposited on the surface of planar substrates and in the interstitial sites of metalattices. U shapes spacers were not as sufficient in removing gas on the top surface because

part of the pathways are block by the spacer and thicker spacer provides a higher flux of carrier gas through the substrate to remove byproducts.

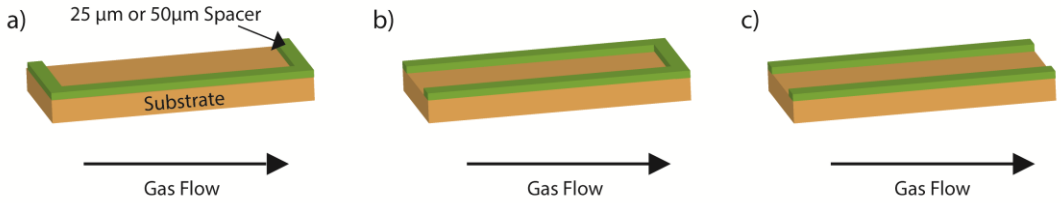

Figure 4-2. Schematic of spacer geometry inside of a flowing reactor. (a) U shape ⊥ to gas flow, (b) U shape ‖ to flow and (c) strips ‖ to flow.

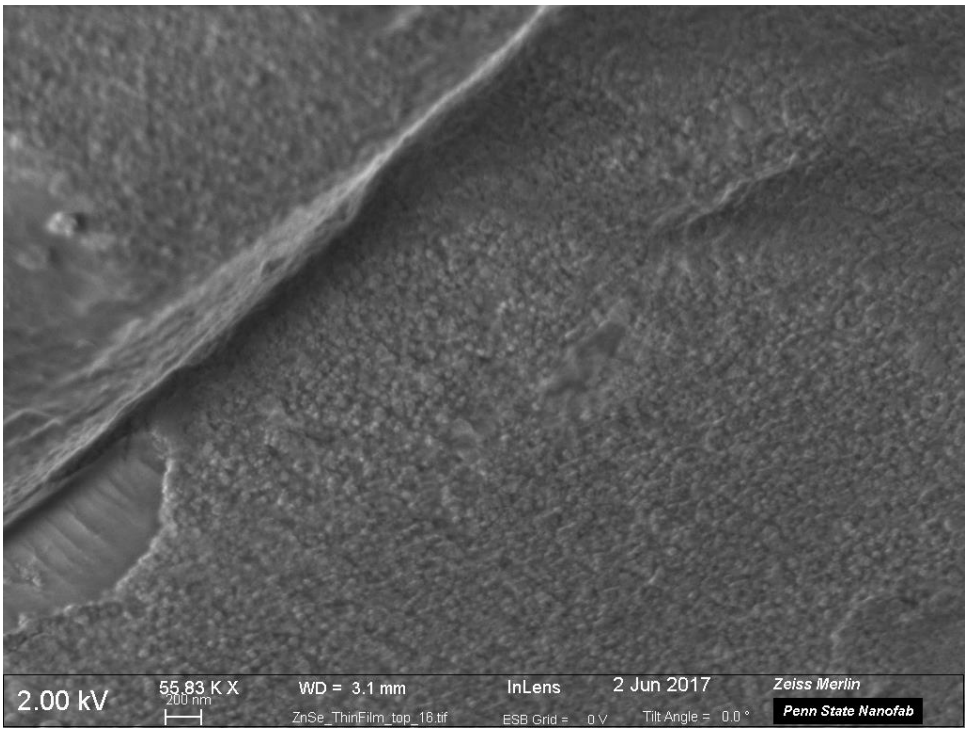

Figure 4-3. SEM image of HPCVD deposited ZnSe thin film on quartz substrate. Particle formation can be seen on the SEM image.

Figure 4-3 shows scanning electron microscope image of HPcCVD deposited ZnSe thin film on quartz substrate. The film was deposited using a flowing reactor as described above with VI/II precursor ratio of 2:1, reactor internal temperature of 400 °C at the deposition zone and total

starting pressure of 41 MPa for 30 minutes with final total pressure of 35 MPa. The same stoichiometric ratio of precursors in silica capillary deposition gives rise to conformal film coatings. However, ZnSe particle growth can be observed in the SEM image (**Figure 4-3**) of thin film deposition inside the 2D/ 3D reactor, indicating gas phase chemistry in the reactor is different than that of silica capillary.

Various conditions were tested for silica colloidal crystal template infiltration of ZnSe using HPcCVD. The experimental conditions used for infiltration is summarized in **Table 4-2**. All results shown in **Table 4-2** uses the parallel strip shape spacers. For VI:II precursor ratio of 2.0, no sign of deposition was found at 375 °C reactor internal temperature. **Figure 4-4** shows that no materials were deposited on top or in the interstitial sites for the 60 nm silica colloidal crystal template. When reactor temperatures of 400 °C and 425 °C were used, ZnSe can be deposited (**Figure 4-5**) in various templates, including 30 nm, 60 nm, 70 nm and 250 nm.

Table 4-2. HPcCVD infiltration conditions of ZnSe in silica colloidal crystal.

Diameter of silica colloidal crystal (nm)	Temperature (°C)	VI:II precursor ratio (by partial pressure)	Infiltration?
30 nm	375	2.0	No
	425	2.0	Yes
	400	4.0	No
60 nm	400	2.0	Yes
70 nm	375	2.0	No
	425	2.0	Yes
	400	4.0	No
100 nm	375	2.0	No
250 nm	375	2.0	No
	450	2.0	Yes
	400	4.0	No

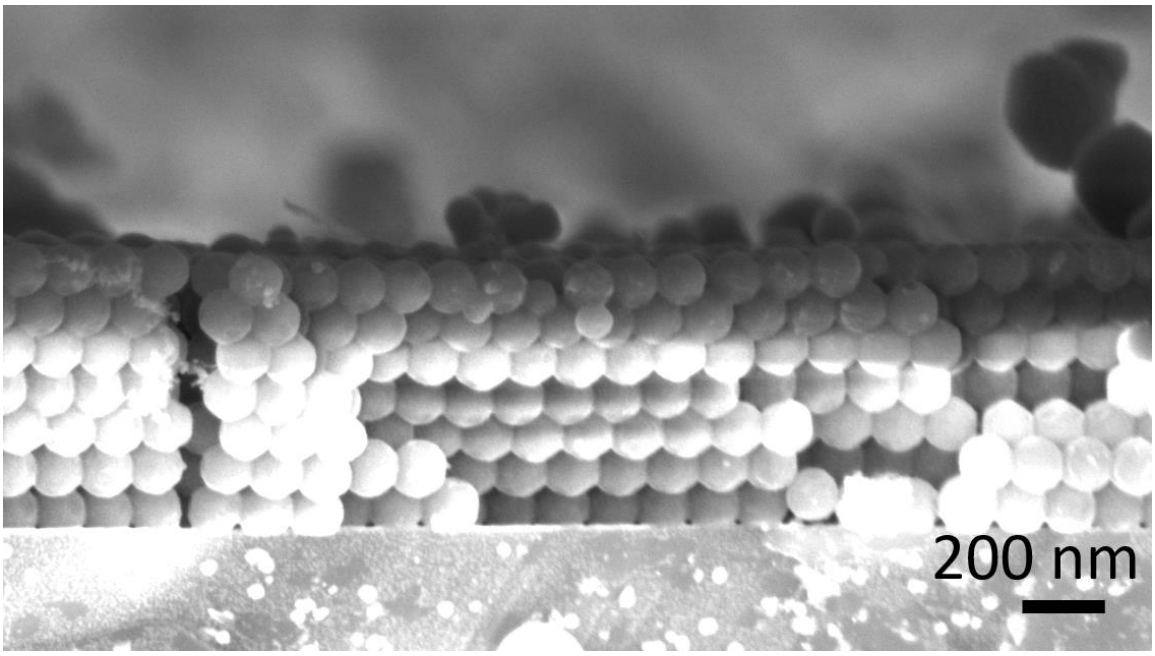

Figure 4-4. Cross-sectional view of HPcCVD infiltration of ZnSe (1:2 precursor ratio) at 375 °C in 100 nm. No infiltration or thin film deposited on top can be observed using a scanning electron microscope.

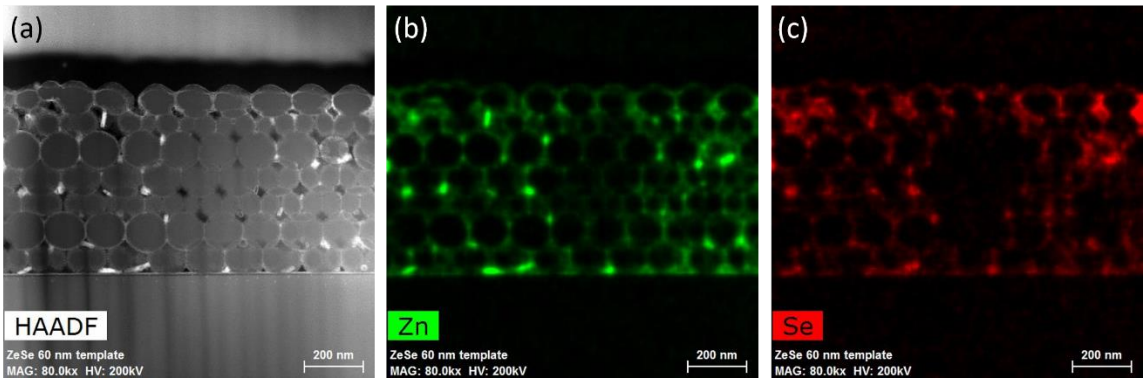

Figure 4-5. TEM Images and EDS mapping of 60 nm ZnSe metalattices deposited using VI;II of 2.0 at 400 °C. The template was not fully filled and clusters can be seen in some of the larger interstitial sites.

In ZnSe optical fiber fabrication using HPCVD, previously developed by Sparks et al[1–3], the silica micro capillary reactor was heated to deposition temperature prior to introducing precursors to the inner pore, and the end of silica capillary is sealed initially and cleaved open simultaneously when gas starts flowing to the deposition zone. This step ensure ZnSe deposition

is not terminated prematurely due to byproducts (methane) build up from fast dimethyl zinc and dimethyl selenium decomposition. However, if the same exhaust method was used, no materials can be seen deposited in the interstitial sites. This is due to the small pathways the precursors must diffuse through to access the pores of silica colloidal crystal template. Amount of time it takes the precursors to get into the pores must be taken into account in 3D infiltration. In the silica capillary studies, when the central pore is less than 500 nm, flow becomes limited and it significantly slows the reaction[3]. To increase the amount of precursor gases in the interstitial before decomposition starts, the reactants and carrier gas mixture is first introduced into the pre-heated reaction chamber. The reactor was pre-heated to 150 ℃ to remove moisture and air, and at this temperature it is not hot enough to decompose the two gas precursors. The samples sit in the precursors bath for 1 – 2 hours before raising the reactor temperature to a deposition temperature of 400 ℃ or 425 ℃. As soon as the reactor reaches deposition temperature, the silica capillary that is attached to the end of the reactor for gas flow management is cleaved open to allow for continuous flow as methane forms during the forward reaction.

4.4. Transmission Electron Microscopy (TEM) of Zinc Selenide in Colloidal Crystal Templates

HPcCVD infiltrated ZnSe metalattices are then characterized using transmission electron microscope. The TEM work shown here is a collaborative effort with Dr. Shih-Ying Yu from Penn State University. All samples were prepared using the Helios NanoLab 660 Focus Ion Bean and characterize using the Talos F200X TEM. TEM energy dispersive spectroscopy (EDS) was used to analyze the Zn and Se ratio of the synthesized products. A ZnSe optical window was used as a standard, with atomic % (at. %) of 50.4 % zinc and 49.6 % selenium (**Figure 4-6, (a)**). As ZnSe optical fiber synthesized using HPCVD was also characterization for comparison; using

reaction conditions of 400 ℃ deposition temperature and VI:II of 2.0, the ratio of Zn and Se in the optical fiber were 51.7 at% and 48.3 at %, respectively, which is very close to 1:1 ratio. The EDS mapping of the HPCVD optical fiber also shows uniform distribution of Zn and Se. HPcCVD ZnSe inside of a 60 nm silica colloidal crystal template does not exhibit similar atomic concentration as compared to the optical fiber synthesized under the same deposition conditions (**Figure 4-6, (c)**). The atomic % was 79.9 Zn : 20.1 Se, where the EDS mapping shows that most of the selenium is on top and most of the Zn are in the interstitial sites. Some of the region does have ZnSe clusters as shown in **Figure 4-6 (c)** with yellow in color. This result indicates the transport of two different precursor in nano-pores is very different compared to the single pore 1D silica capillary geometry and tuning of precursor ratios and temperature is required.

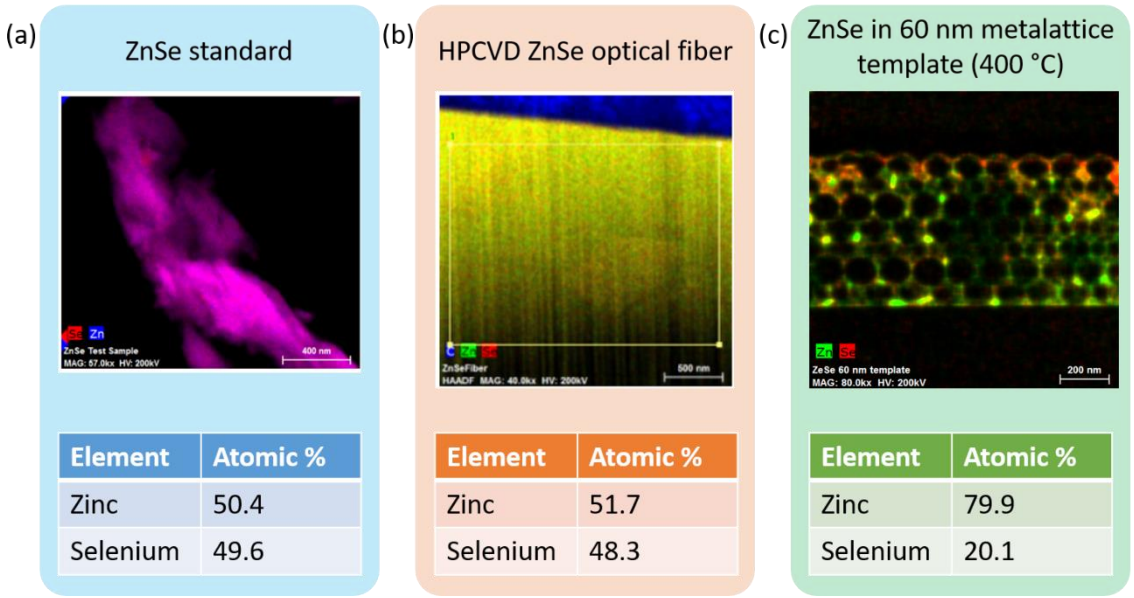

Figure 4-6. TEM EDS analysis of Zn and Se atomic percentage in HPcCVD optical fibers and 60 nm metalattices deposited at 400 °C. (a) EDS mapping and atomic % of Zn and Se of a ZnSe optical window used as a standard. (b) HPCVD ZnSe optical fiber showing close to 1:1 atomic % of Zn and Se. (c) EDS mapping of 60 nm metalattice made from HPcCVD infiltration of ZnSe. Most selenium are deposited near the top surface (shown in red) and zinc are in the interstitial sies (green). ZnSe regions are shown in yellow. TEM credit: Shih-Ying Yu.

Since the concentration of selenium is much lower than of zinc, we needed to find a method to increase the amount of selenium inside the template. This could be achieved by either increasing the concentration of selenium precursor or by increasing the deposition temperature because a high temperature is needed to decompose H_2Se in H_2. From a previous HPCVD of ZnSe study[1,3], elemental Se formation was not observed even when the concentration of VI:II was increased to above 5, but columnar growth was observed and conformal film cannot be grown. When a 4.0 VI:II stoichiometric ratio of precursors was used for infiltration into silica colloidal crystal templates, no deposition in the pores was observed at deposition temperature of 400 °C (**Table 4-2**). When the precursor ratio was kept at 2.0 VI:II, but with a higher deposition temperature of 425 °C, ZnSe was deposited in the interstitial sites, and Zn and Se atomic ratio improves compared to 400 °C. It is expected that more Se precursor can be decomposed at high temperatures[16]. **Figure 4-7** shows TEM HAADF and EDS mapping of 250 nm ZnSe metalattice at 425 °C. The structure is not filled void-free, but the atomic ratio of Zn : Se improves to 60% : 40%. The atomic percent of selenium doubles compared to infiltration using a lower deposition temperature of 400 °C.

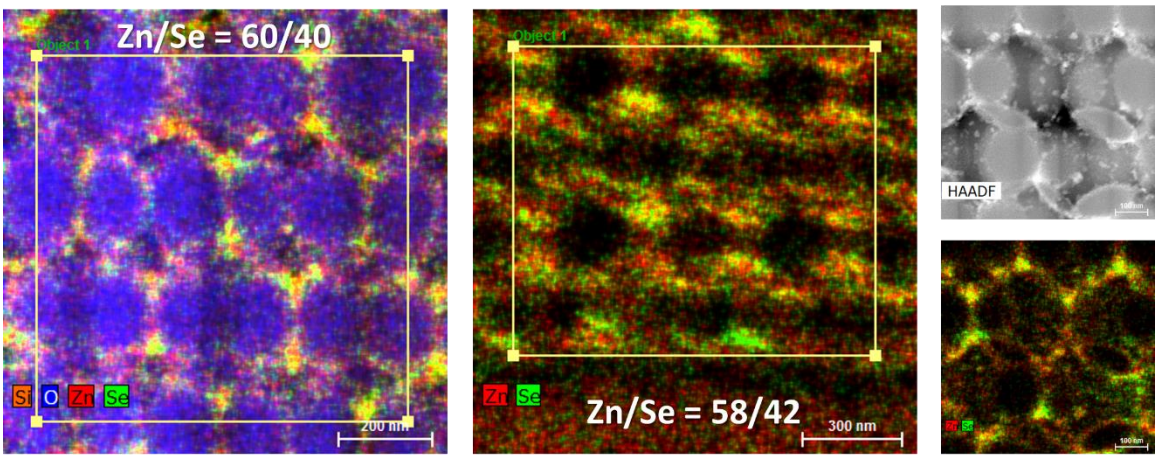

Figure 4-7. TEM EDS analysis of Zn and Se atomic ratio in HPcCVD 250 nm metalattices deposited at 425 °C when precursor ratio VI:II = 2.0. TEM credit: Shih-Ying Yu.

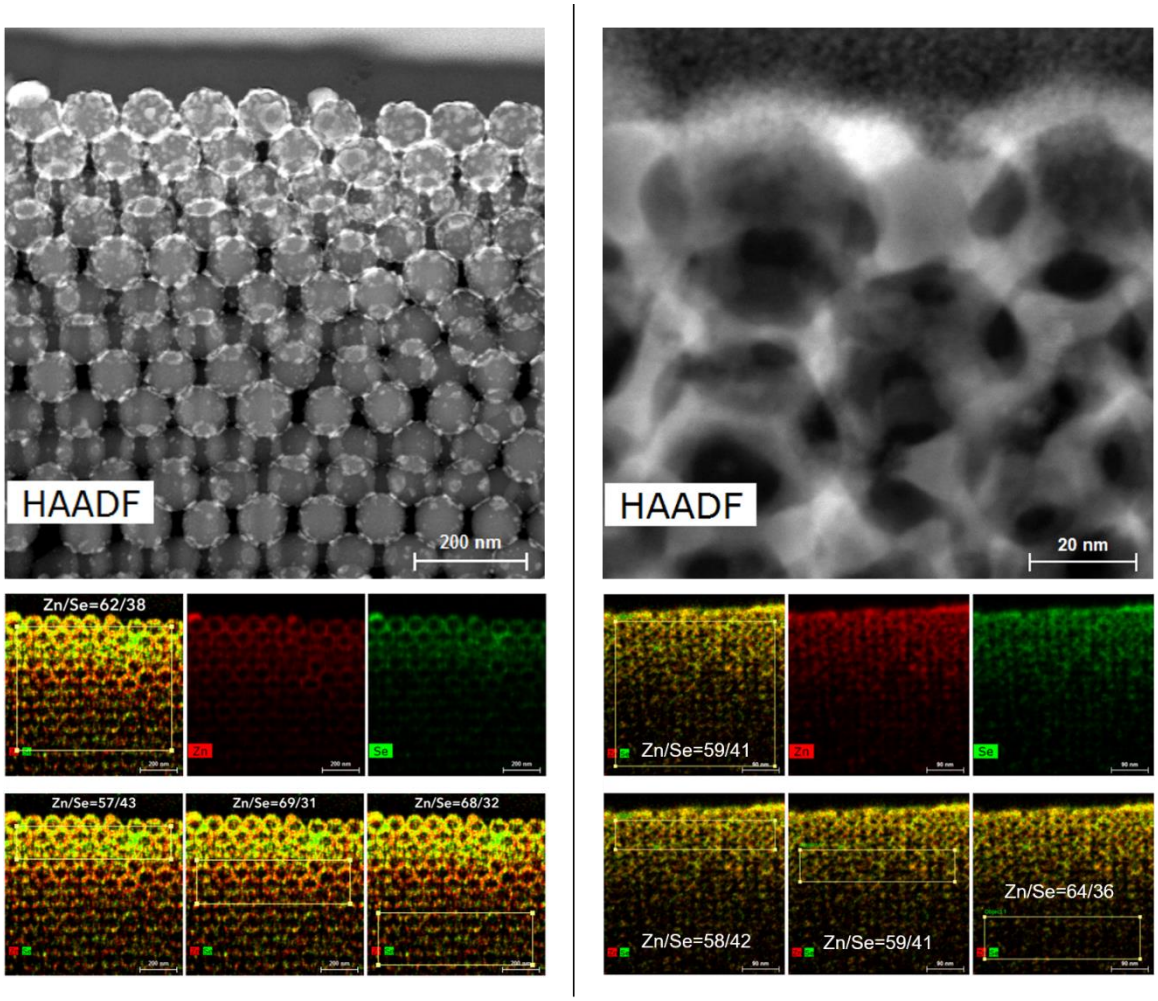

Figure 4-8. TEM HAADF images and EDS analysis of Zn and Se stoichiometry in HPcCVD 30 nm (right) and 70 nm (right) metalattices deposited at 425 °C. More materials are deposited near the top surface as shown in both the 30 nm (right) and 70 nm (left) templates. The atom ratio of Zn and Se changes depending on its relative position to the top surface of the template. For example, for the 70 nm template, Zn:Se changes from 57:43 (top 200 nm) to 69:31 (200 nm from the top surface, and to 68:32 (500 nm from the top surface). This suggests a longer diffusion time is needed for precursor gas molecules to enter deeper into the template. TEM credit: Shih-Ying Yu.

In addition to the 250 nm periodicity templates, silica colloidal crystal templates with smaller repeating units of 30 nm and 70 nm were also investigated. A filter effect can be seen for selenium concentration in the smaller templates at VI:II ratio of 2.0 and deposition temperature of 425 °C. A high concentration of selenium is found on the top layers of the template. The overall

Zn/Se atomic ratio of a 70 nm ZnSe metalattice (**Figure 4-8, left**) was 62:38, but the concentration of Zn and Se varies depending on its relative position to the substrate. More materials for both Zn and Se are deposited near the top (furthest away from the substrate), but the ratio of Zn:Se in the 70 nm template drops from 57:43 (top 3 layers) to 69:31 (200 nm from the top surface), and down to 68:32 (500 nm from the top surface), suggesting that the selenium precursor diffuse into the nano-pores poorly. This is likely due to larger sizes of dimethyl selenium compared to dimethyl zinc. In addition, precursors can enter into the template more effectively through the top surface than the edges because there are more pathways on the top than the sides (**Figure 4-9**). The high annular angle dark field (HAADF) image of the 70 nm ZnSe metalattice appears to be disconnected (**Figure 4-8, top left**). ZnSe particles can be seen throughout the interstitial sites and most particles growth begins on the template surface.

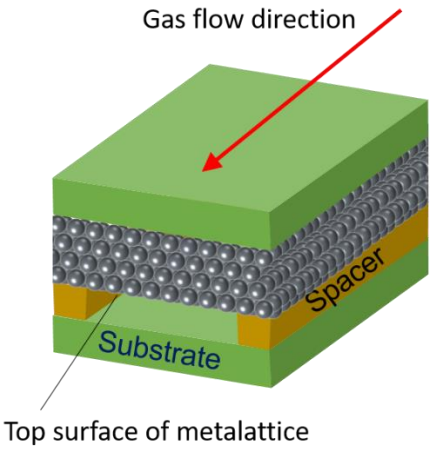

Figure 4-9. Schematic of silica colloidal crystal template and metalattice inside of the reaction show the top surface and gas flow direction. As shown in the TEM EDS images in Figure 4-7 and Figure 4-8. Most materials are deposited on the top surface, where there is the largest opening for precursor gas entrance.

The concentration of Zn and Se in the 30 nm template shows similar results to the 70 nm HPcCVD ZnSe infiltration. The top 200 nm has an atomic ratio of 58:42 for Zn:Se while the

ratio drops to 64:36 from 300 nm from the top surface. The 30 nm ZnSe metalattice has a better connectivity as shown in the HAADF images in **Figure 4-8**. High resolution TEM images of the ZnSe filled areas of 30 nm metalattice shows crystalline materials in the interstitial sites (**Figure 4-10**). When a Fast Fourier Transform is applied to the crystalline regions, it was found that the FFT matches well with ZnSe [5 0 9] zone axis, suggesting the materials deposited is ZnSe. The concentration of Zn/ Se and fillings of materials in the interstitial sites needs to be improved to further yield a well ordered, interconnected metalattice. Further improvements of the infiltration process will be discussed in the future work section at the end of this chapter.

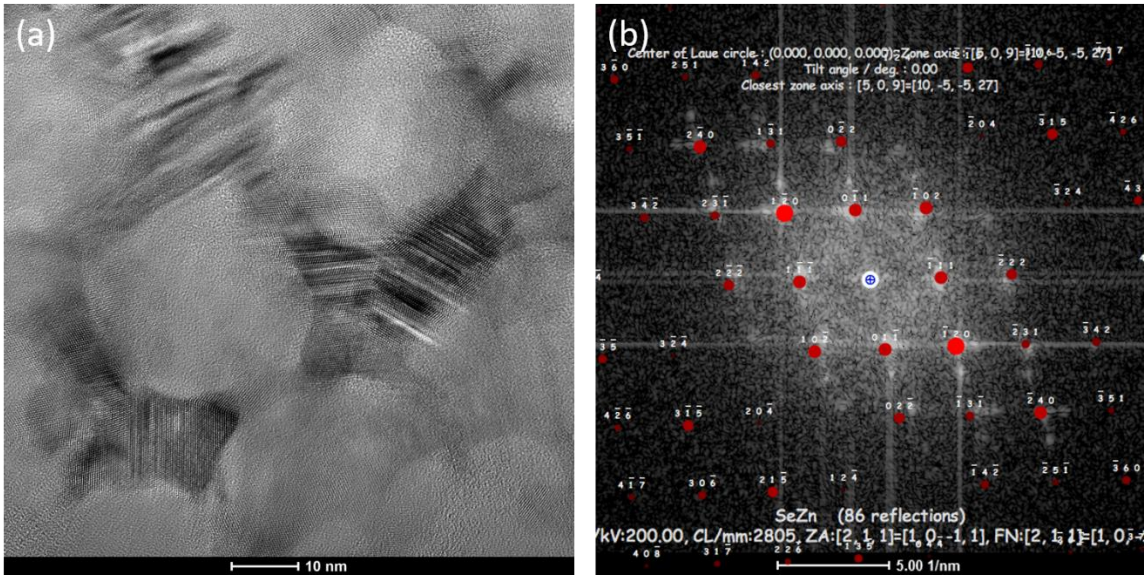

Figure 4-10. (a) High resolution TEM image of 30 nm ZnSe metalattice. Crystalline ZnSe is deposited in the interstitial sites. (b) A Fast Fourier Transform of the crystalline area shows that it matches with the lattice spacing of ZnSe. TEM Credit: Shih-Ying Yu.

4.5. Other Characterizations

Other characterizations were used to study the ZnSe metalattice with the best chemical composition according to TEM EDS studies (250 nm template made of 58:42 Zn:Se ratio). SEM imaging was done using Zeiss MERLIN Field Emission Scanning Electron Microscopy

(FESEM). Raman spectroscopy was done using Renishaw inVia Raman microscopy system with 514 nm excitation wavelength. The XRD spectra were collected using two different systems, both with Cu K∝ source, PANalytical Empyrean for conventional XRD and PANalytical XPert Pro MPD for Grazing Incidence XRD (GIXRD).

4.5.1. Scanning Electron Microscope Imaging of ZnSe Metalattice

A scanning electron microscope was used to image the top surface of the template to understand materials deposited along the precursor gas flowing pathway. Most materials deposited on the larger template (**Figure 4-11**) of 250 nm diameter silica colloidal crystal template suggest particle growth take place in the gap between silica nanoparticles. Most of the smaller pores are filled with ZnSe during a 1 hour deposition, but larger pores appear to be partially filled. A longer deposition time may be needed to increase the filling fraction. Unlike the silicon deposition process, where a film is deposited on top of the template coating the outer surface, HPcCVD infiltration of ZnSe does not produce a film immediately. Only a few small particles of ZnSe can be seen on top as shown in **Figure 4-11**.

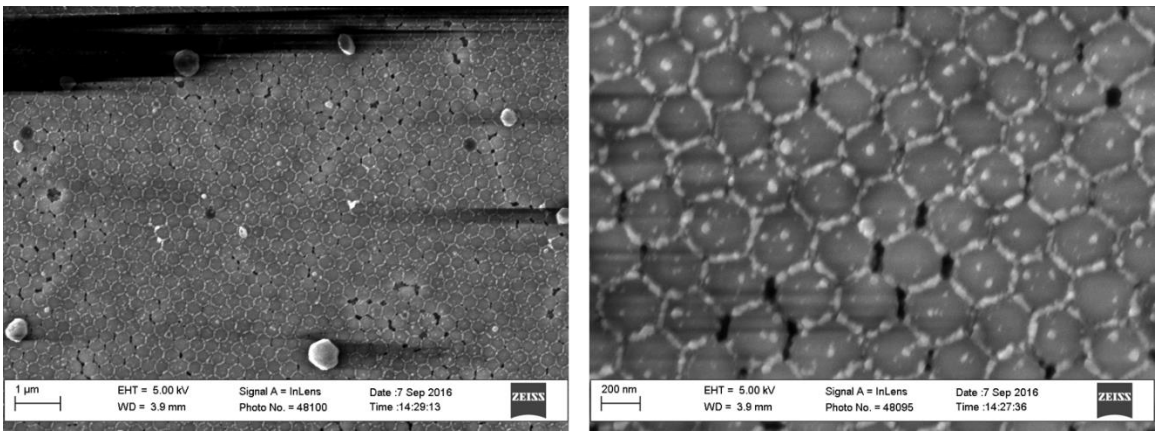

Figure 4-11. SEM top view of HPcCVD ZnSe 250 nm metalattice. Infiltration for 1 hour shows that materials are deposited in the interstitial sites. Longer deposition time may be needed for higher fraction of fillings.

4.5.2. Raman Spectroscopy of 250 nm ZnSe Metalattice

Raman spectroscopy is a non-destructive characterization method often used to analyze material's quality. Optical phonons inside of a materials can be probed to extract information such as bonding environment and crystallinity. A light source, usually a laser of a particular wavelength is used to interact with the electron cloud of a material. When the material is excited to the virtual energy state, it relaxes to lower levels then emits photons. Two types of scattering can happen at this stage, inelastic and elastic scattering. Elastic scattering is Rayleigh scattering, which has the same frequency as the incident beam. Inelastic scattering is what contributes to the Raman effect where emitted photon either shifted to lower or higher energy states than the incident light. This happens when the molecules oscillating polarization is couple to other polarization of the molecules, such as vibration, which shifts the molecules to a new rotational or vibrational state. When the new state has a higher energy than the initial state, the scattered photon will have a lower energy than the incident beam to compensate the energy difference, which is known as stoke shift. If the opposite happens, with lower energy in the new state, the excited photon will have a higher energy than the incident beam, known as anti-stoke shift.

An excitation wavelength of 514 nm was used for the ZnSe Raman analysis. The presence of characteristic transverse optical (TO_{ZnSe}) and longitudinal optical (LO_{ZnSe}) phonon modes[17] were probed in the 250 nm ZnSe metalattice (**Figure 4-12**). The sharp peak at 522.45 cm^{-1} can be contributed to the TO Raman mode of single crystalline Si substrate. The ZnSe infiltrated sample is crystalline, but both TO (211.28 cm^{-1}) and LO (253.94 cm^{-1}) modes of ZnSe are broaden. The TO and LO modes have a Lorentzian FWHM fit of 11.66 and 31.16, respectively. For crystalline materials in bulk, the $q = 0$ momentum selection rule is satisfied in first order Raman spectrum because the phonon eigenstates are plane waves. The broadening of the TO and LO modes are due to ZnSe materials in the nanoscale, where momentum conversation

rules are relaxed and phonons at $q \neq 0$ can be contributed to the spectra[18–22]. The homogeneous broadening of TO_{ZnSe} and LO_{ZnSe} can be contributed to the nano-sized crystals[18,22], which correlates with the TEM studies.

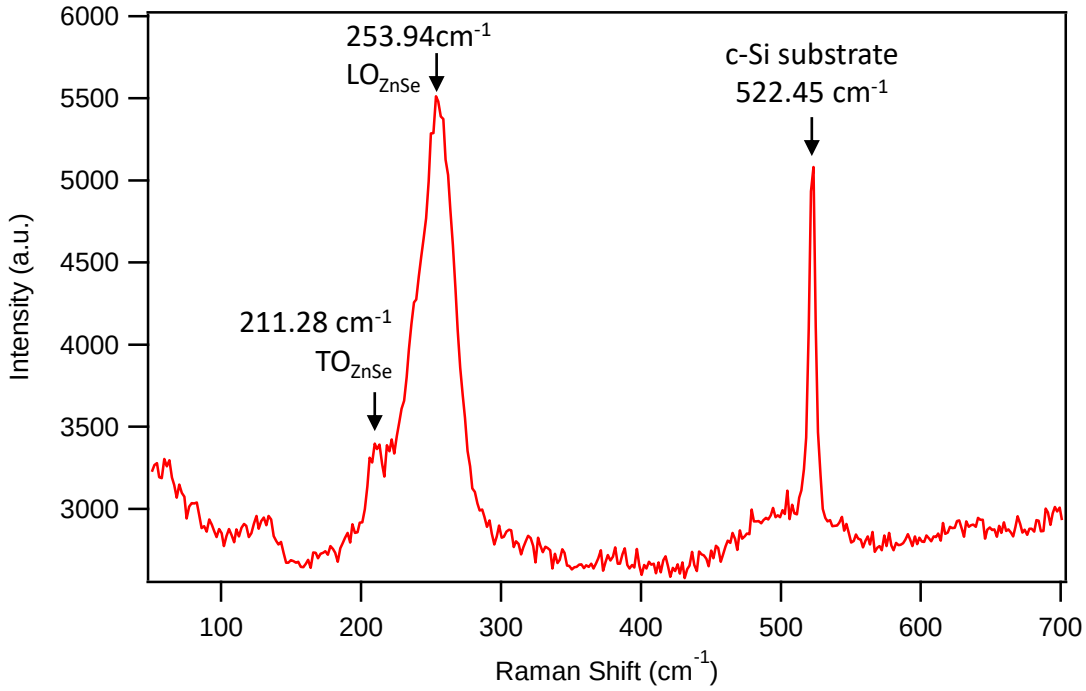

Figure 4-12. Raman spectra of 250 nm HPcCVD infiltrated ZnSe metalattice.

4.5.3. X-Ray Diffraction of 250 nm ZnSe Metalattice

250 nm ZnSe metalattice was also analyzed using thin film x-ray diffraction (XRD). XRD of the thin film ZnSe metalattice demonstrate existence of ZnSe nanocrystals from the broaden peaks[23,24]. **Figure 4-13** shows the XRD pattern of the as synthesized film. A polycrystalline ZnSe optical window was used as a ZnSe standard. Diffraction peaks of (111) and (220) at $2\theta = 27.2$ and $2\theta = 45.2$, respectively, were observed for both the standard and 250 nm ZnSe metalattice. Due to the strong (400) peak arising from the substrate, <100> Si

wafer, other peaks at $2\theta = 53.6, 65.8, 72.5$, corresponding to (311), (400) and (331) were not observed.

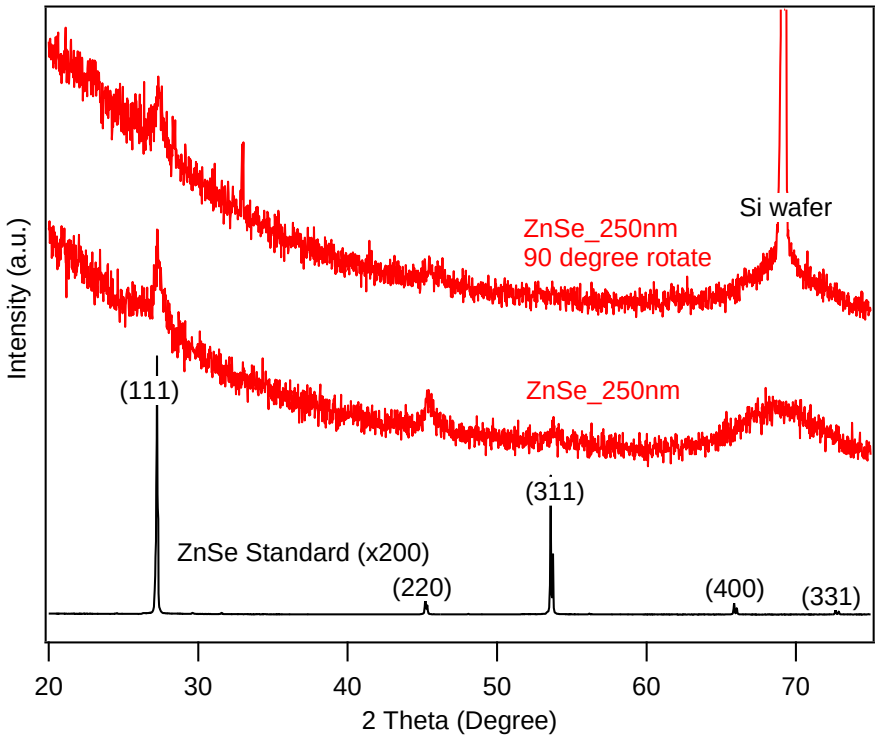

Figure 4-13. XRD of 250 nm HPcCVD infiltrated ZnSe metalattice.

To better resolve the other diffraction peaks of ZnSe. Grazing incident XRD (GIXRD) was used to study the thin film. GIXRD can be used to analyze thin films of 1-1000 nm to minimize the substrate contribution. The incidence angle used here was 1°. The substrate was <100> Si wafers, where some of the diffraction peaks does appear but with a lower intensity compared to XRD at certain direction of the film in relation to the incident beam. To better eliminate diffraction patterns from the substrate, the sample was rotated 90 ° in relation to the incident beam. In GIXRD, the incident beam is set a fixed angle as opposed to rotating angle in conventional XRD. The diffraction angles are varied to measure 2θ. The ZnSe crystalline peaks of (111), (220) and (311) were observed in the 250 nm sample at $2\theta = 27.3°, 45.3°, 53.8°$,

respectively (**Figure 4-14**). No evidence of elemental Zn can be observed from the XRD results even though the atomic ratio of Zn was found to be higher than Se in the TEM studies. The resulting ZnSe metalattice likely has selenium vacancies in its crystal structure.

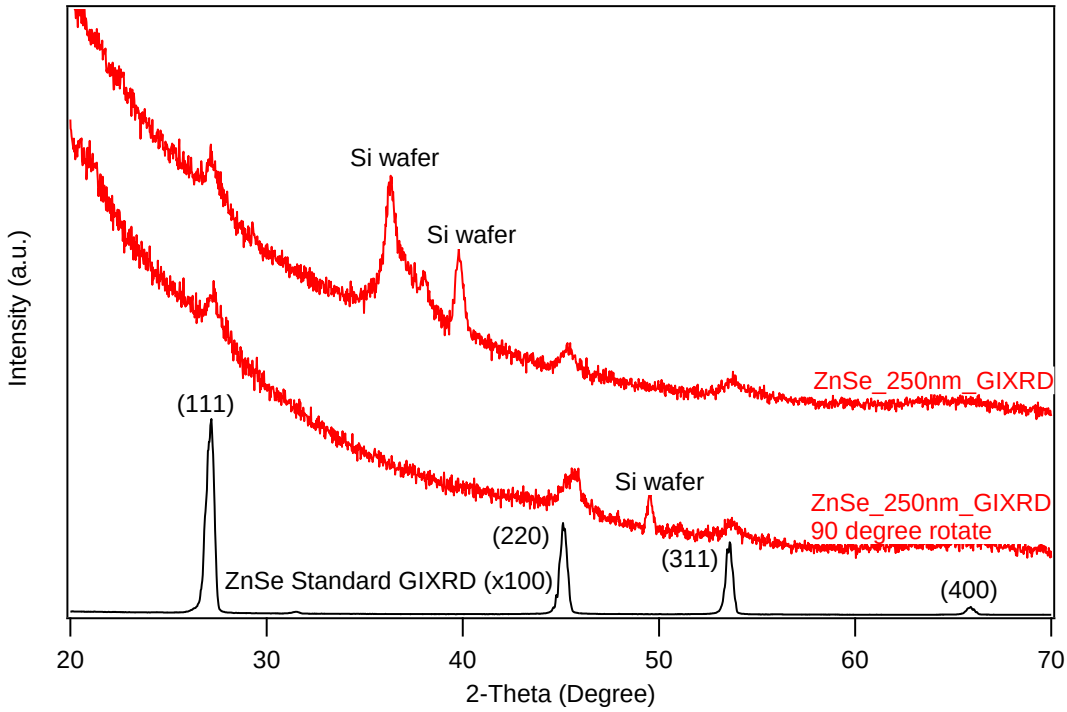

Figure 4-14. GIXRD of 250 nm HPcCVD infiltrated ZnSe metalattice.

4.6. Conclusion and Future Directions

The use of HPcCVD is a powerful technique in infiltrating materials with small pores. In addition to unary semiconductor, compound semiconductor can be deposited. Compound semiconductors often have a more complex gas chemistry and require a careful tuning of precursor gas ratio. The effect of reactor design, sample placement, pressure, temperature and precursor gas ratios are all important in determining if the infiltration was successful. The results shown in this chapter suggest that a void free infiltrated ZnSe metalattice is possible with

additional tuning of reaction conditions. In addition, other semiconductors such as GaN, ZnS and ZnO could be deposited in the silica colloidal crystal template.

A new design to the reactor geometry could help improve gas transport into the interstitial sites in the silica colloidal crystal template. Since the top surface has many more gas molecules entrances, a reactor designed in such that the precursor gases must go through the silica colloidal template before traveling to the exhaust would force all reactants to enter into the interstitial sites. The template can then be thought of as a membrane filtering the reactants, while the carrier gas can move the by-product methane out of the system. One possible solution is to assemble silica colloidal crystals directly in a silica capillary with inner diameter in 10s of micrometers. The silica capillary can be used as a micro-reaction, similar to ZnSe optical fiber fabrication, but the colloidal crystal template will be in the inner pore to yield ZnSe metalattice.

The partial pressure of precursors used is much lower in HPcCVD of ZnSe compared to HPcCVD Si and Ge. The partial pressure of precursor to carrier gas is 0.083% in ZnSe deposition compared to 2-10% in Si and Ge deposition. The concentration of dimethyl zinc and dimethyl selenium in a gas reservoir is limited by the vapor pressure of the two precursors in the gas transfer process. When a higher concentration of both precursors are put in the reservoir, dimethyl zinc and dimethyl selenium returns to liquid phase. Growth rate of ZnSe is much higher than of silicon or germanium in the silica optical fiber geometry, but is different in the silica colloidal crystal template due to the confined structure and strenuous path the gas needs to travel to enter the interstitial sites. An increase in precursor gas partial pressure might be needed to allow more precursor gas to penetrate into the pores. This could be achieved by doing multiple condensations of each precursor gas using the gas loading system shown in *chapter 2*. The gas reservoir itself can be heated to elevated temperature during deposition to increase the vapor pressure of the precursor gases, such as 100 °C to keep the precursors in vapor phase while preventing them from decomposing at higher temperatures. In addition, a longer precursor gas

bath soak time for the templates could increase the concentration of precursors in the interstitial sites prior to raising the reactor to deposition temperature.

4.7. References

1. Sparks, J. R. *et al.* Conformal Coating by High Pressure Chemical Deposition for Patterned Microwires of II-VI Semiconductors. *Adv. Funct. Mater.* **23,** 1647–1654 (2013).
2. Sparks, J. R., Sazio, P. J. A., Gopalan, V. & Badding, J. V. Templated Chemically Deposited Semiconductor Optical Fiber Materials. *Annu. Rev. Mater. Res.* **43,** 9.1-9.31 (2013).
3. Sparks, J. R. *et al.* Zinc selenide optical fibers. *Adv. Mater.* **23,** 1647–1651 (2011).
4. Bingxia, Z. *et al.* Doped quantum dot@silica nanocomposites for white light-emitting diodes. *Nanoscale* **7,** 17231–17236 (2015).
5. Revaprasadu, N., Malik, M. A., O'Brien, P., Zulu, M. M. & Wakefield, G. Single-source molecular precursors for the deposition of zinc selenide quantum dots. *J. Mater. Chem.* **8,** 1885–1888 (1998).
6. Zhang, H., Mo, J. & Lu, X. Synthesis and photoluminescence properties of wash-board belt-like ZnSe nanostructures. *Optoelectron. Lett.* **9,** 401–404 (2013).
7. Pejova, B. & Grozdanov, I. Three-dimensional confinement effects in semiconducting zinc selenide quantum dots deposited in thin-film form. *Mater. Chem. Phys.* **90,** 35–46 (2005).
8. Mohanan, J. L., Arachchige, I. U. & Brock, S. L. Porous Semiconductor Chalcogenide Aerogels. *Science (80-.).* **307,** 397–401 (2005).
9. Feng, B., Cao, J., Yang, J., Yang, S. & Han, D. Characterization and photocatalytic activity of ZnSe nanoparticles synthesized by a facile solvothermal method , and the

effects of different solvents on these properties. *Mater. Res. Bull.* **60,** 794–801 (2014).

10. Senthilkumar, K., Kalaivani, T., Kanagesan, S., Balasubramanian, V. & Balakrishnan, J. Wurtzite ZnSe quantum dots : synthesis , characterization and PL properties. *J Mater Sci Mater Electron* **24,** 692–696 (2013).
11. Li, L., Zhang, F., Ding, Y., Wang, Y. & Zhang, L. Synthesis of Functionalized ZnSe Nanoparticles and Their Applications in the Determination of Bovine Serum Albumin. *J. Fluoresc.* **19,** 437–441 (2009).
12. Feng, B., Cao, J., Han, D., Yang, S. & Yang, J. Study on growth mechanism and optical properties of ZnSe nanoparticles. *J. Mater. Sci. Mater. Electron.* **26,** 3206–3214 (2015).
13. Hutagalung, S. D. & Loo, S. C. Zinc Selenide (ZnSe) Nanoparticles Prepared by Sol-Gel Method. in *7th IEEE International Conference on Nanotechnology* 930–933 (2007).
14. Wright, P. J. & Cockayne, B. The Organometallic Chemical Vapour Deposition of ZnS and ZnSe at Atmospheric Pressure. *J. Cryst. Growth* **59,** 148–154 (1982).
15. Stringfellow, G. B. *Organometallic vapor phase epitaxy : theory and practice*. (Academic Press, 1989).
16. Maung, N., Fan, G. H., Ng, T. L., Williams, J. O. & Wright, A. C. Mass-spectrometric study of the pyrolysis reactions in the MOVPE of Ga2Se 3 by in-situ gas sampling. *J. Cryst. Growth* **158,** 68–78 (1996).
17. Mitra, S. S. Phonon Assignments in ZnSe and GaSb and Some Regularities in the Phonon Frequencies of Zincblende-Type Semiconductors. *Phys. Rev.* **132,** 986–991 (1963).
18. Nesheva, D. *et al.* Raman Scattering from ZnSe Nanolayers. *Acta Physcia Pol. A* **116,** 75–77 (2009).
19. Carroll, P. J. & Lannin, J. S. Raman Scattering of Amorphous Selenium Films. *Solid State Commun.* **40,** 81–84 (1981).
20. Poborchii, V. V. Raman Spectra of Sulfur, Selenium or Tellurium Clusters Confined in

Nano-Cavities of Zeolite A. *Solid State Commun.* **107,** 513–518 (1998).

21. Shi, L., Wang, C., Wang, J., Fang, Z. & Xing, H. Temperature-Dependent Raman Scattering of ZnSe Nanowires. *Adv. Mater. Phys. Chem.* **6,** 305–317 (2016).

22. An, H.-Z., Zhao, Q. & Du, W.-M. Raman spectra of ZnSe nanoparticles synthesized by thermal evaporation method. *Chinese Phys.* **13,** 1753–1757 (2004).

23. Wang, M., Wang, Y., Yao, X., Kong, F. & Zhang, L. In-situ growth and spectrum characterization of ZnSe nanocrystals in silica gel-glasses. *Chinese Sci. Bull.* **49,** 747–750 (2004).

24. Wang, M. *et al.* Preparation and characterization of ZnSe nanocrystals in silica gel-glasses. *J. Electroceram.* **21,** 815–818 (2008).

Chapter 5

HPcCVD of Electronic Metalattices from Other Templates

Nano-templates used for metalattices are not limited to silica colloidal crystals. Although the ability to tune the sizes, symmetry and periodicity of colloidal crystal templates provides a robust platform in designing metalattices, other templates should also be explored, especially if metalattices of smaller periodicity are of interest. Colloidal crystals made of silica nanoparticles have a size limit related to how small a silica nanoparticle can be made, usually less than 10 nm, but other templates such as zeolites, mesoporous silica and metal-organic frameworks can provide access to smaller pores in the range of 2-8 nm. In addition, the ordering of the nanoparticles during colloidal crystal assembly relies heavily on the sizes and shapes of the nanoparticles. Even a small deviation in nanoparticle sizes can increase disorder of the overall metalattice structure which may increase electron and phonon scattering. Atom precise templates such as zeolite and metal-organic frameworks can be used to address such issues to yield highly ordered metalattice. In this chapter, we will discuss the HPcCVD effort in fabricating electronic metalattices of smaller periodicity and with atomic precision using nano-templates other than silica colloidal crystals.

5.1. Zeolite Y

Zeolites are porous solids made up of silicon, oxygen and aluminum with cations such as Na^+, Ca^+ and K^+ loosely attached to the framework[1]. Zeolites have a variety of uses including adsorbents[2], catalysts[3] and filtration membranes[4]. The pore dimension can range from 1-dimensional tube shapes to 3-dimensional interconnected pores[1]. The thermal stability of zeolites can be tuned by adjusting the Si/Al ratio and cations in the framework[5], making them suitable for

high pressure confined chemical vapor deposition to infiltrate semiconductors in the pores. Zeolite Y (Faujasite, **Figure 5-1**) is a true three-dimensional aluminosilicate porous solid with two available cages for semiconductor infiltration[6]. The void spaces inside of a Faujasite can be filled with semiconductor to yield an interconnected, yet ordered metalattice with precision down to the atomic scale. The cages' sizes are 1.3 nm ∝ supercages and 0.8 nm in diameter sodalite β cages[7]. The supercages are interconnected with each other by the sodalite cages of 24 ring windows of 0.75 nm in diameter[7]. The supercages are arranged in a diamond cubic crystal structure. Zeolite Y can be used a host materials for synthesizing quantum confined semiconductor nanoparticles and clusters such as CdS[8,9], GaP[10] and Ga_2S_3 [11].

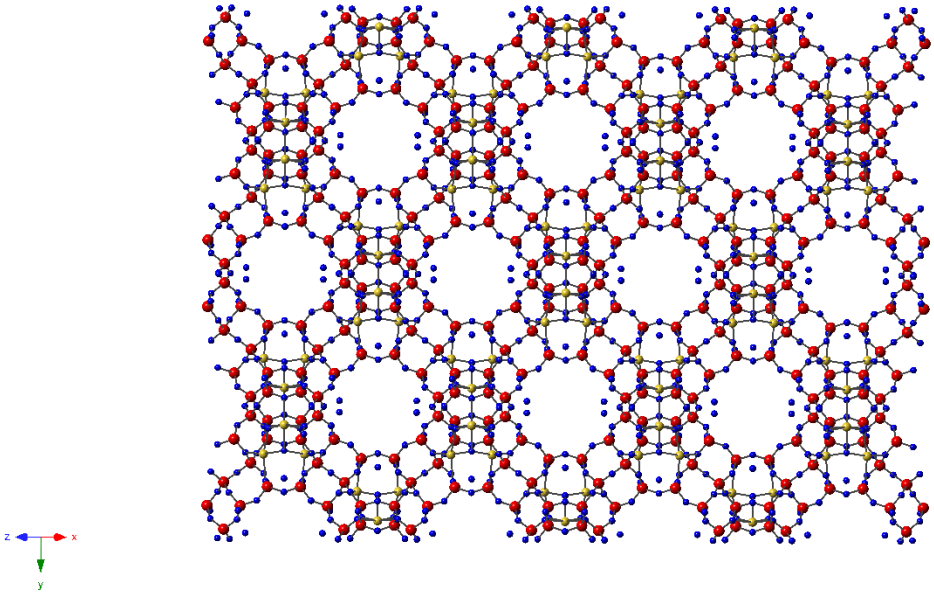

Figure 5-1. Schematic illustration of Faujastic (FAU, zeolite Y) frameworks from the <110> projection showing the 1.3 nm in diameter spherical ∝ supercage. The supercages are interconnected in 3D by 0.75 nm in diameter necks. Red, blue and gold spheres depicts silicon, oxygen and aluminum atoms, respectively. The cation, sodium, can be exchanged to other ions if needed.

Previous studies in incorporating silicon or germanium in the zeolite Y frameworks use various methods, such as topotactic chemical vapor deposition (CVD) of disilane[12,13] and

digermane[14], reduction of germanium after germania[15] encapsulation in the cages and Ge cluster formation in the cages from germane CVD[16]. The incorporation of semiconductors in these studies requires that the precursor gas molecules naturally adsorb in the ∝ supercage, then thermally decompose at a higher temperature. For example, disilane was heated to 100 °C to decompose. However, precursor molecules have been shown to anchor onto the framework to block the entrance (β cage) of incoming precursors, limiting the amounts of materials that can be deposited in the template[12]. In addition, gas molecules could be chemisorbed at the cation sites, reducing their chances to decompose at the two cages[12]. Only clusters formation have been found from previous studies due to the limited amount of precursors allowed in the framework prior thermal decomposition[9,12–18]. In addition, none of these studies have shown the possibility of chemical doping for the semiconductors, which is very useful in tuning the electrical properties. As shown in previous studies, high pressure confined chemical vapor deposition (HPcCVD) can be used to infiltration nano-pore void free. Zeolite Y can be infiltrated with Si and Ge with the HPcCVD infiltration method discussed in *Chapter 2*.

Zeolite Y with crystal sizes ranging from 500 nm to 1 μm in diameter were used for infiltration. Zeolite Y with proton (H) was used as the host template for its high stability up to 500 °C [6]. Zeolite Y-H can be achieved by cation exchange and deammoniation[16]. The zeolite Y powder was packed inside of 1 mm outer diameter, 0.8 mm inner diameter and 8 mm long borosilicate glass tubes as shown in **Figure 5-2**. The tubes were then position inside of the HPcCVD infiltration reactor sample holder for high pressure infiltration. Prior to infiltration, 12 hours of heat treatment at 400 °C in vacuum was employed to remove moisture and air from the pores of zeolite Y-H. The reactor was cooled to 100 °C before the introduction of precursor gas molecules so the template could remain moisture free and silane or germane molecules would not decompose before entering into the cages of the zeolite Y template. Si and Ge were deposited at

400 °C and 350 °C, respectively. Total reactor pressure for the infiltration ranges from 25 – 35 MPa with a partial pressure of 1-5% of silane for Si or 2 % of germane for Ge.

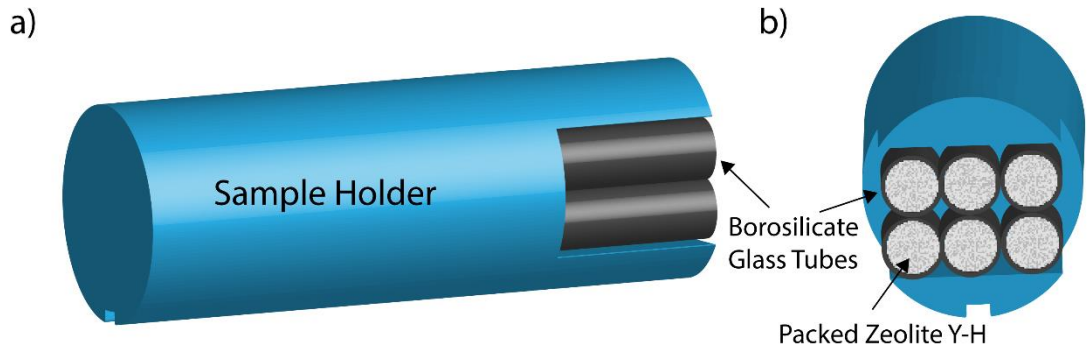

Figure 5-2. Illustration of sample holder showing the arrangement of zeolite Y-H packing inside of the HPcCVD reactor.

5.1.1. X-Ray Diffraction of Si and Ge HPcCVD infiltrated zeolite Y-H

Powder x-ray diffraction (XRD) was used to study the Si and Ge HPcCVD infiltration of zeolite Y-H. Zeolite Y-H has a framework topography of a Faujasite, which has been extensively studied in experiments and theory[19]. **Figure 5-3** shows the powder x-ray diffractionof Si infiltrated zeolite Y-H using Cu kα source. The diffraction peaks suggest the crystal structure has remained intact after infiltration. In addition, zeolite Y-H was heated in reducing conditions (10 % partial pressure of H_2 in He to mimic high pressure high temperature without silane or germane precursors) to understand the thermal stability of zeolite Y-H under HPcCVD conditions. No changes to the diffraction pattern can be seen for the 400 °C heated zeolite Y-H, suggesting the high pressure condition does not alter its crystal structure. Significant peak shifts can be seen for the Si infiltrated zeolite Y-H. The Si HPcCVD zeolite Y-H has larger 2θ values compared to the bare zeolite Y-H XRD pattern (**Table 5-1**). The lattice parameters of the first 10 crystalline planes shrink between 0.72% to 2.84% with an average of 1.08% as shown in **Table 5-1**. No

crystalline silicon peak was found for the infiltrated or the annealed sample, as the crystallites in the supercages or β cages would be too small to be observed (peak broadening due to nano-sized particles). The unit cell shrinkage can possibly be contributed to the contraction of semiconductors inside of the supercages and β cages of the framework, causing the zeolite Y-H framework to shrink as the infiltrated Si cools.

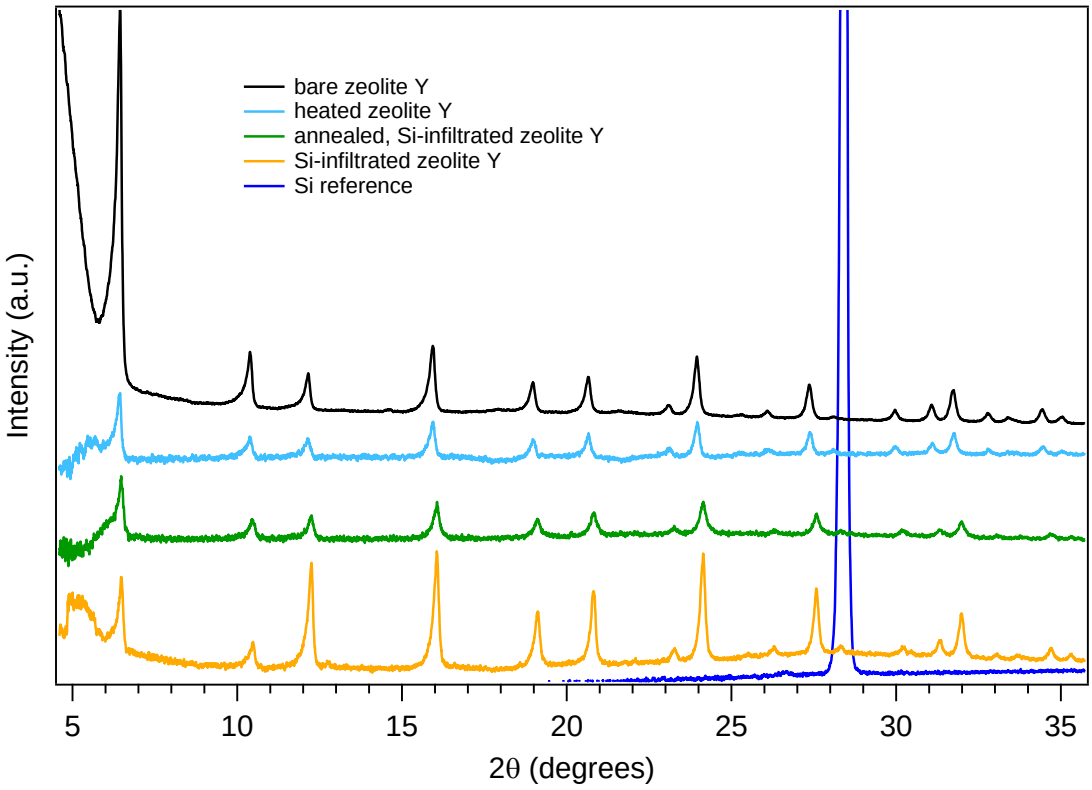

Figure 5-3. Powder x-ray diffraction of Si infiltrated zeolite Y-H compared to bare zeolite Y-H, heated annealing Si infiltrated zeolite Y-H with Si reference.

Table 5-1. Lattice parameters of Si infiltrated zeolite Y-H compared to zeolite Y-H standards.

2θ (degree)		d-spacings		Miller Indices			Lattice parameter		Difference %
Filled	Empty	Filled	Empty	h	k	l	Filled	Empty	
6.485	6.3	13.61864	14.01814	1	1	1	23.58818	24.28012	2.84982
10.48	10.348	8.434441	8.541733	2	2	0	23.8562	24.15967	1.256094
12.25	12.12	7.219438	7.296581	3	1	1	23.94417	24.20002	1.057243
16.055	15.909	5.51599	5.566281	3	3	1	24.04364	24.26286	0.903497
19.105	18.95	4.641718	4.679334	4	2	2	22.73968	22.92396	0.803866
20.805	20.636	4.266118	4.300672	4	4	0	24.13281	24.32828	0.803468
23.275	23.105	3.818674	3.846384	6	2	0	24.15141	24.32667	0.720435
24.145	23.945	3.683012	3.713319	5	3	3	24.15112	24.34986	0.816186
26.29	26.08	3.387178	3.413973	5	5	1	24.18929	24.38065	0.784886
27.58	27.359	3.231609	3.257209	6	4	2	24.18315	24.37472	0.785958
Average (%), first 10									1.078145

Table 5-2. Lattice parameters of Ge infiltrated zeolite Y-H compared to zeolite Y-H standards.

2θ (degree)		Miller Indices			Lattice parameter		Difference (%)	Average (%) First 10 values
Filled	Empty	h	k	l	Filled	Empty		
6.2	6.2	1	1	1	24.67135	24.67135	0	0.224817376
10.165	10.14	2	2	0	24.59344	24.65392	0.245298906	
11.935	11.905	3	1	1	24.57375	24.63545	0.250455406	
15.715	15.7	3	3	1	24.56046	24.58378	0.094851929	
18.79	18.735	4	2	2	23.11739	23.18464	0.29009229	
20.445	20.41	4	4	0	24.5531	24.59476	0.169375324	
22.91	22.85	6	2	0	24.53093	24.59448	0.258409339	
23.76	23.7	5	3	3	24.5367	24.59792	0.248909679	
25.935	25.855	5	5	1	24.5146	24.58916	0.303202902	
27.185	27.12	6	4	2	24.52777	24.58545	0.234616046	

XRD (**Figure 5-4**) was also used to characterize the HPcCVD Ge infiltrated zeolite Y-H by germane pyrolysis. **Table 5-2** shows the changing lattice parameters of Ge infiltrated Zoelite Y-H compared to the standard. Similar to the Si infiltrated zeolite Y-H, amorphous or crystalline Ge diffraction peaks were not seen in the XRD pattern because the small crystallites would

drastically broaden the peaks. The lattice shrinkage after Ge infiltration is less than that of Si infiltrated zeolite Y-H, ranging from 0.09% to 0.30% in the first 10 diffraction peaks, with an average of 0.23%. **Figure 5-4 (b)** shows the difference between Si and Ge infiltrated, heated, and empty zeolite Y-H at $2\theta = 27.12°$ (zeolite Y-H standard), corresponding to the (642) crystalline plane. Smaller changes to lattice parameters in Ge infiltrated zeolite Y-H compared to Si infiltrated zeolite Y-H could be because Si has a better adhesion to silica (majority of zeolite framworks) as compared to Ge[20]. Uniaxial shrinkage can be seen in the infiltrated samples as certain planes have a larger shrinkage percentages than others.

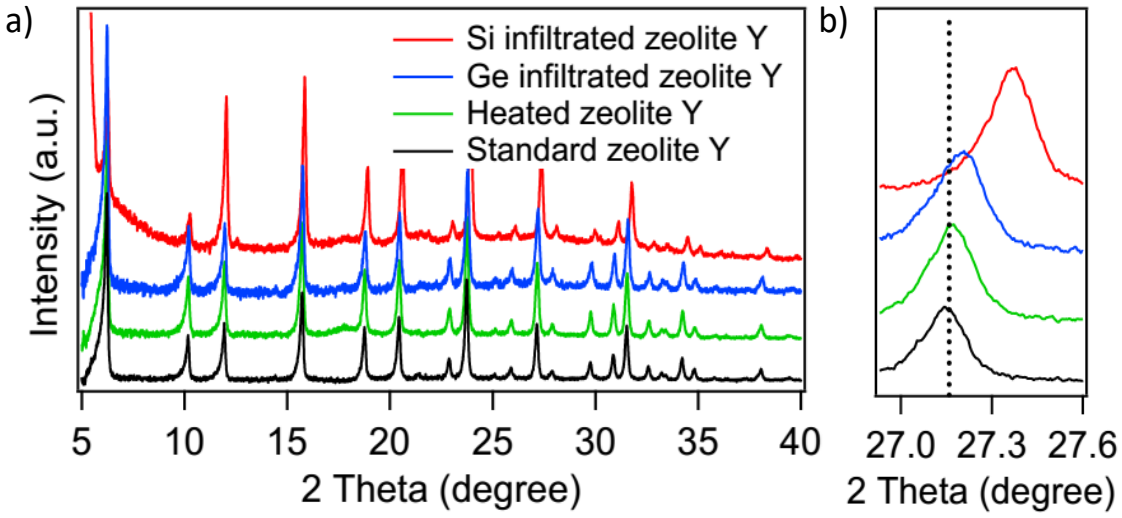

Figure 5-4. Powder x-ray diffraction of Si and Ge infiltrated zeolite Y compared to heated and standard zeolite Y. Zeolite Y diffraction peaks were resolved in all samples, but Si or Ge diffraction peaks were not resolved. However, there are significant shifts for the infiltrated zeolite Y, suggesting shrinking of the lattice parameter as compared to the infiltrated semiconductor. The diffraction pattern of zeolite Y in green shows that treating the material in reducing environment (H_2) does not affect its crystallinity or lattice parameters.

5.1.2. Raman Spectroscopy of HPcCVD Si and Ge Infiltrated Zeolite Y-H

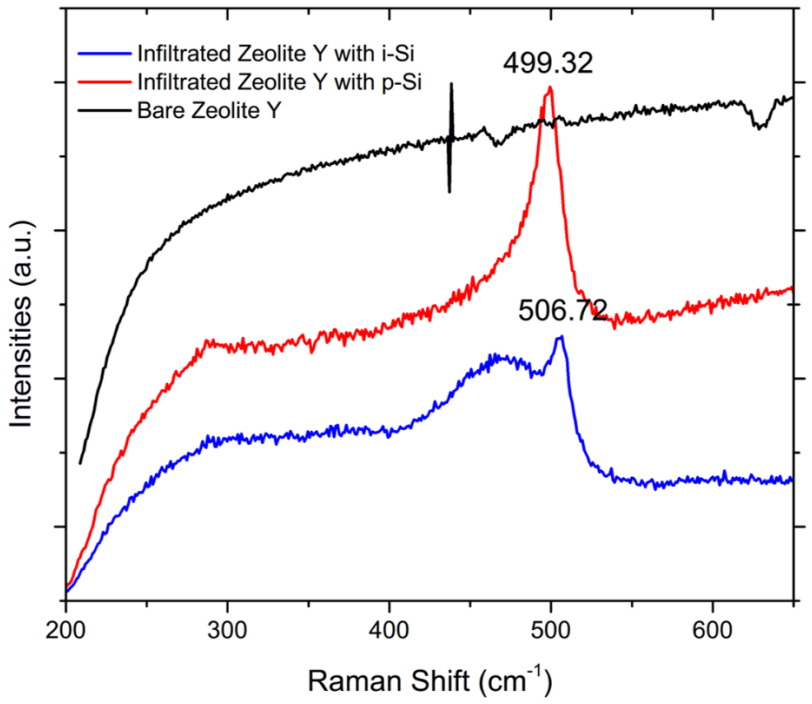

Figure 5-5. Raman spectroscopy of HPcCVD intrinsic and p-doped Si infiltrated zeolite Y-H. The zeolite peaks at 499.32 cm^{-1} and 506.72 cm^{-1} can be seen in the infiltrated samples, while the zeolite features are cover by the photoluminescence background. An amorphous Si peak is also observed (shoulder in red curve and bump in blue curve).

The chemical composition of the infiltrants were characterize using Raman spectroscopy using 633 nm excitation light. No Raman modes were seen in the template prior to infiltration due to the photoluminescence background[21]. The zeolite Y-H bending vibration of the Si-O-Al 4 membered ring[22] (499.32 cm^{-1} and 506.72 cm^{-1} in p-Si and i-Si infiltrated zeolite Y-H, respectively) can be observed in the HPcCVD Si infiltrated zeolite Y-H (**Figure 5-5**), suggesting changes to the photoluminescence mechanism in the infiltrated samples. The amorphous silicon centered at 480 cm^{-1} (**Figure 5-5**) and crystalline Ge at 293.54 cm^{-1} and 295.73 cm^{-1} (**Figure 5-6**) were observed in the infiltrated samples. Ge was deposited at temperature of 350 °C by germane decomposition, which resulted in crystalline material. However, no zeolite Y-H 4 membered ring

bending mode was observed in the c-Ge infiltrated sample, which could be hidden by the stronger PL background compare to a-Si infiltrated zeolite Y-H. Although both XRD and Raman spectroscopy characterization suggest materials have been deposited in the supercages and β-cages, other characterization methods such as microscopy are needed to further confirm that the materials was deposited inside of the pores instead of coating the outer surface of the zeolite crystals.

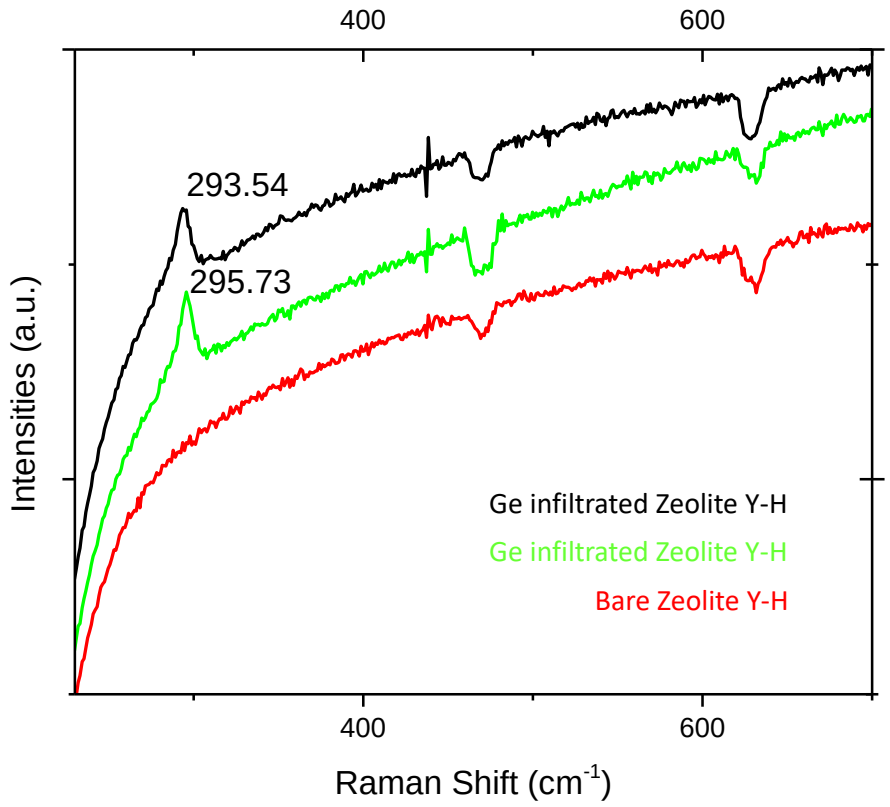

Figure 5-6. Raman spectroscopy of HPcCVD infiltrated Ge zeolite Y-H. Ge was deposited by germane pyrolysis at 350 °C. Photoluminescence background is seen in the bare zeolite Y-H (red curve). Crystalline Ge modes can be observed after infiltration.

5.1.3. Electron Microscopy of HPcCVD Si and Ge Infiltrated Zeolite Y-H

Scanning electron microscope (SEM) and transmission electron microscope (TEM) were used to characterize the silicon and Ge infiltrated zeolite Y-H. **Figure 5-7** shows SEM images of intrinsic Si infiltrated samples compared to the empty zeolite Y-H. The samples were prepared by spreading the powder zeolites onto conductive carbon tape. The SEM images shows that the overall sizes and shapes have not changed significantly due to Si over coating. To further look into the pores and possible infiltration by HPcCVD, TEM was used. The samples were prepared by first sonicating in n-hexane for 60 minutes then drop casted onto a lacey-carbon coated copper TEM grid, and imaged using JEOL 2010 F TEM at 200 kV.

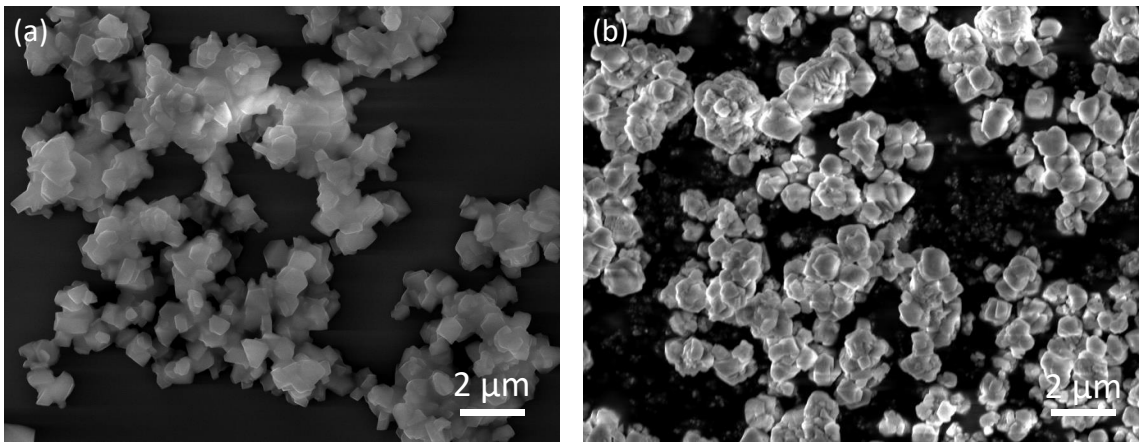

Figure 5-7. SEM images of empty (a) and i-Si infiltrated (b) zeolite Y power.

Electron microscope imaging of zeolite has been a challenge due to radiolysis. When the electron beam (e-beam) shines onto the sample, Al-O bond are being broken and cations (such as Na^+ and Ca^+) are thus moved to the dangling O bonds to permanently change the structure[23]. Empty zeolite Y suffers from radiolysis and is damaged within seconds after exposure to the electron beam, going from crystalline to amorphous. **Figure 5-8 (a)** shows a TEM image of

empty zeolite Y, imaged by focusing at another crystal before moving to the crystal of interest and taking an image. After infiltration, the Si infiltrated zeolite Y can stay undamaged for the duration of the TEM experiment under the same TEM conditions at 200 eV e-beam power (**Figure 5-8 (b)**). Crystalline fringes can be seen in both Si infiltrated and empty zeolites, corresponding to the zeolite Y-H (111) spacing of 1.4 nm (∝ supercages).

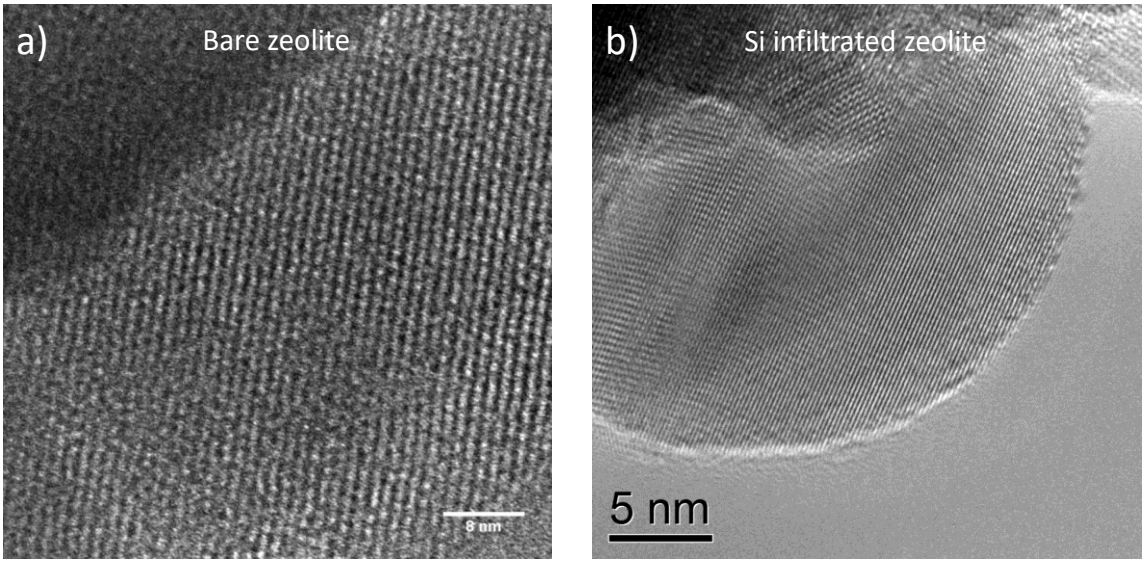

Figure 5-8. TEM images of bare and Si infiltrated zeolite Y. The bare zeolite decomposed quickly under the electron beam (within a minute), while the silicon infiltrated zeolite is stable under the electron beam throughout the duration of imaging.

To increase the z-contrast and distinguishable energy dispersive spectroscopy (EDS) chemical analysis, a HPcCVD Ge infiltrated zeolite Y-H was used instead of Si infiltrated sample. **Figure 5-9 (a)** shows a high resolution image of the Ge infiltrated zeolite Y-H, where zeolite crystalline spacing of 1.38 nm can be seen by measuring the distances of the fringes in the FFT inset, corresponding to the (111) crystalline plane of zeolite Y-H. In addition, an EDS spot scan of the Ge infiltrated zeolite Y-H shows that Ge is encapsulated in the framework (**Figure 5-9 (b)**), suggesting successful HPcCVD infiltration. However, these TEM studies cannot confirm whether Ge has been infiltrated into the framework void-free to create an interconnected

metalattice structure with 1.4 nm periodicity. A higher resolution TEM study is needed to confirm the connectivity of the Ge infiltrant and a direct view from the (110) zone axis is needed to view the pores (**Figure 5-1**).

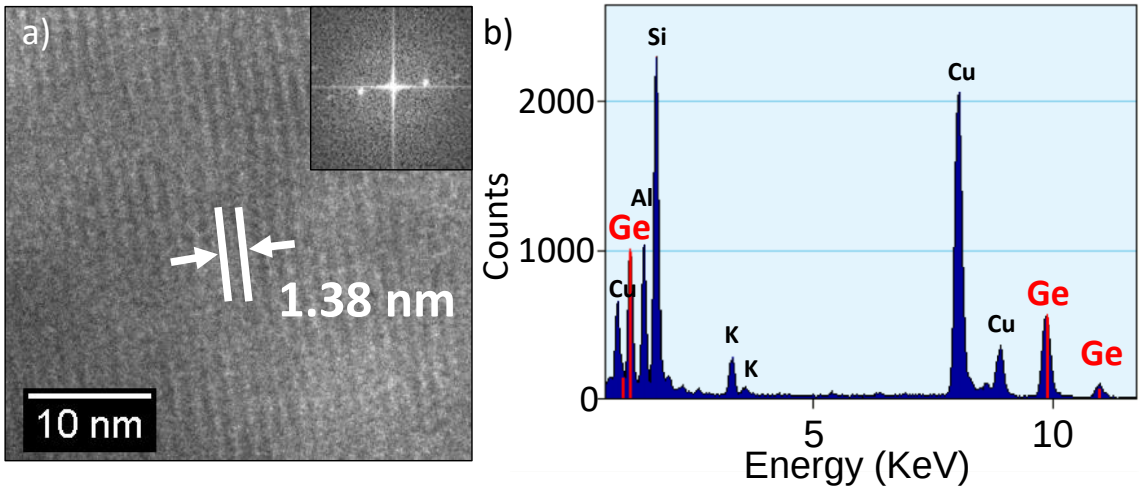

Figure 5-9. TEM image and EDS spot characterization of Ge infiltrated zeolite Y. Lattice spacing of 1.38 nm, corresponding to the (111) plane of crystalline zeolite Y can be determined from the fast Fourier transform of the TEM image (inset). EDS spot scan reveals Ge is found in the TEM sample.

5.1.4. HPcCVD Infiltration of Single Crystal Zeolite Y

In attempts to directly view the zeolite Y through the (110) plane to reveal the interconnected pores after infiltration, large zeolite Y single crystals were infiltrated with Ge. After infiltration, the crystal was placed vertically on a SEM post and a TEM sample was prepared by using focused ion beam (FIB) to cut perpendicular to the (110) plane. Zeolite Y with diameter of up to 150 μm (provided by Dr. David Evan W. Vaughan from Pennsylvania State University) was used (**Figure 5-10**). The crystals were calcined at 400 °C with slow ramp rate of 1 °C/s for 24 hours in vacuum prior to infiltration. Then the crystals were sit in the precursor gas

bath for 12 hours at 150 °C before heating to deposition temperature of 325 °C for amorphous Ge infiltration. The crystals turns dark after infiltration (**Figure 5-10 (b)**) from the Ge coating on the outer surface. The TEM sample was prepared as shown in **Figure 5-10 (c)-(d)**, cut perpendicular to the (110) plane for viewing on that plane in TEM.

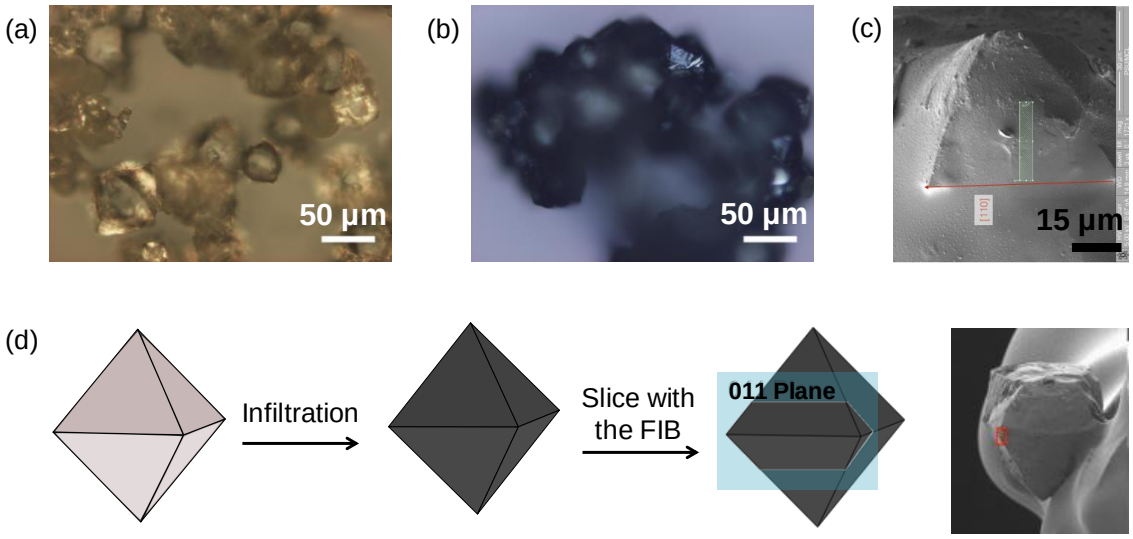

Figure 5-10. Single crystal zeolite Y with diameters up to 150 µm was used for Ge infiltration. (a) single crystal zeolite Y prior to and (b) after Ge infiltration. The octahedral morphology of the crystals are observed. (c) SEM image of the FIB cut for TEM sample preparation. The red line indicates the (110) plane. (d) Illustration of the infiltration and cut with the FIB.

TEM images (**Figure 5-11**) show that the single crystal zeolite have been sliced into layers and the in-between layers were filled with Ge after HPcCVD infiltration. EDS mapping of Ge showed that Ge was deposited throughout the structure while the Si and O showed that the framework was sliced by the HPcCVD process. However, single crystal x-ray crystallography confirms that the zeolite crystal structure was unchanged after infiltration with a R-factor of 0.8. Further investigation into HPcCVD infiltration experimental conditions and high resolution imaging of direct viewing into the pores will help in understanding the filling in the future.

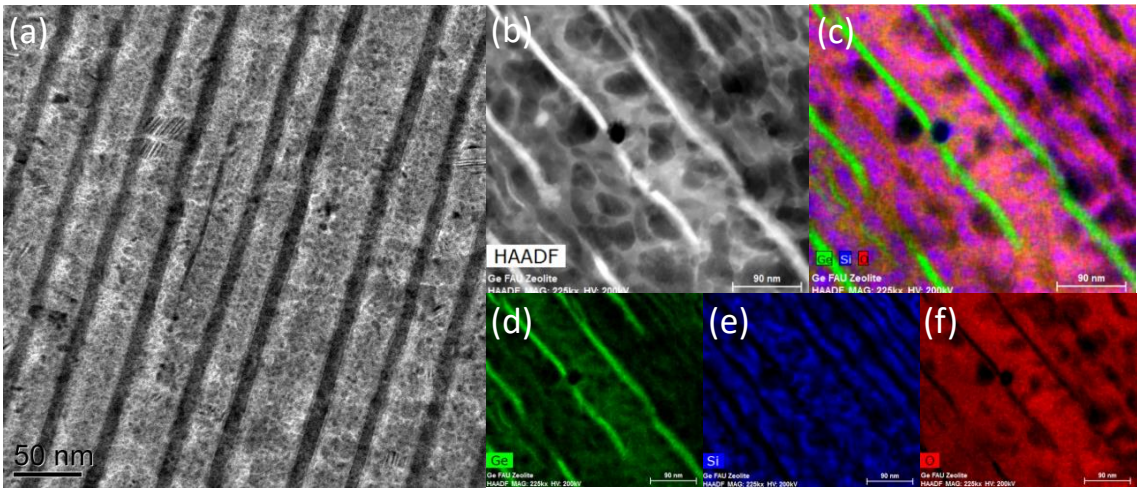

Figure 5-11. High resolution TEM (a), HAADF (b) and EDS (c-f) mapping of HPcCVD infiltrated Ge zeolite Y. TEM credit: Shih-Ying Yu.

5.2. Mesoporous Silica

Another nano-template candidate for HPcCVD infiltration to fabricate metalattice is mesoporous silica. The pore sizes, connectivity, and dimension of the pores can be tuned by varying the reaction condition, such as surfactants used and reaction temperatures. Pore diameter can range from 2 nm up to 30 nm with 1D channels or 3D interconnected pores[24,25]. Infiltration of semiconductors into mesoporous silica provides a route to ordered, self organized quantum dot lattices at a large scale for applications such as nonlinear optics, optoelectronics and catalysis[26]. Solution methods can be used to soak the template to produce semiconductors in the pores[26], but high purity, electronic grade semiconductor lattices are difficult to achieve with these methods. Other CVD[27,28] methods fails to completely fill the pores and form only clusters of semiconductor in the pores due to insufficient mass transport of precursor gas molecules before the pore entrance are clogged by surface coatings. High pressure confined CVD, on the other hand, has shown promising results in the infiltration of nano-pores as shown in this dissertation. The infiltration of 3D mesoporous silica reported here uses HPcCVD to incorporate semiconductor such as silicon

and germanium into the pores. The mesoporous silica template was provided by Dr. Shoji Hall (under Dr. Thomas Mallouk, Pennsylvania State University). The template has 6 nm diameter spherical pores which are 3-dimensionally interconnected. The template was calcined at 600 °C for 2 hours in air prior to infiltration and heated in vacuum for 1 hour at 400 °C before introducing the precursor gas into the reaction chamber. The infiltration follows the procedure described in *Section 2.3.1*. with a germane decomposition temperature of 325 °C for 60 minutes.

5.2.1. Raman Spectroscopy of HPcCVD Ge Infiltrated 3D Mesoporous Silica

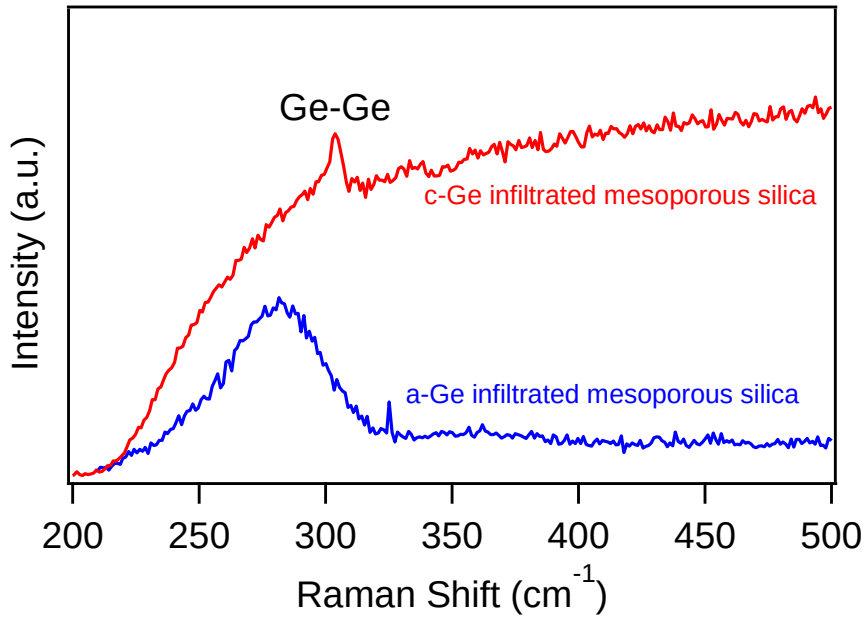

Figure 5-12. Raman spectroscopy of Si Ge infiltrated 3D mesoporous silica. The Ge-Ge vibrational mode is observed for the as synthesized amorphous Ge mesoporous silica (blue curve). After thermal annealing at 500 °C, Ge can be crystallize (red curve).

Raman spectroscopy was used to analyze the as synthesized and thermal annealed HPcCVD Ge infiltrated 3D mesoporous silica using method described in *Section 5.1.2*. using 633 nm excitation wavelength. The as synthesized sample was deposited as amorphous Ge (**Figure**

5-12, blue) and can be crystallize to yield c-Ge (**Figure 5-12, red**). Upon crystallization, a strong photo luminescent background is seen in the Raman spectra, suggesting changes to its electronic structure, which could be coming from quantum confined Ge nano-crystallites in the pores of mesoporous silica.

5.2.2. X-ray Diffraction of HPcCVD Ge Infiltrated 3D Mesoporous Silica

Thin film x-ray diffraction was used to further characterize both the chemical composition and pores of the Ge infiltrated 3D mesoporous silica. Characterization method described in *Section 5.1* was used here to characterize the film. In the wide angle XRD shown in **Figure 5-13**, the amorphous Ge peak at $2\theta = 26.22°$ with d-spacing of 3.36 Å was observed. The strong signal could be due to the over-coating on the top surface.

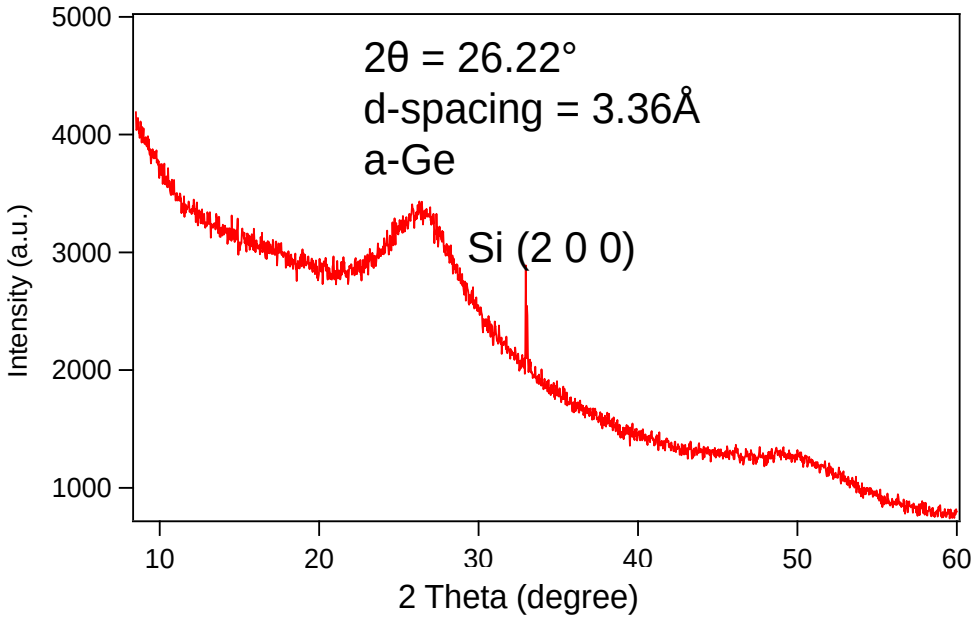

Figure 5-13. Thin film XRD of 6 nm Ge infiltrated silica mesoporous silica.

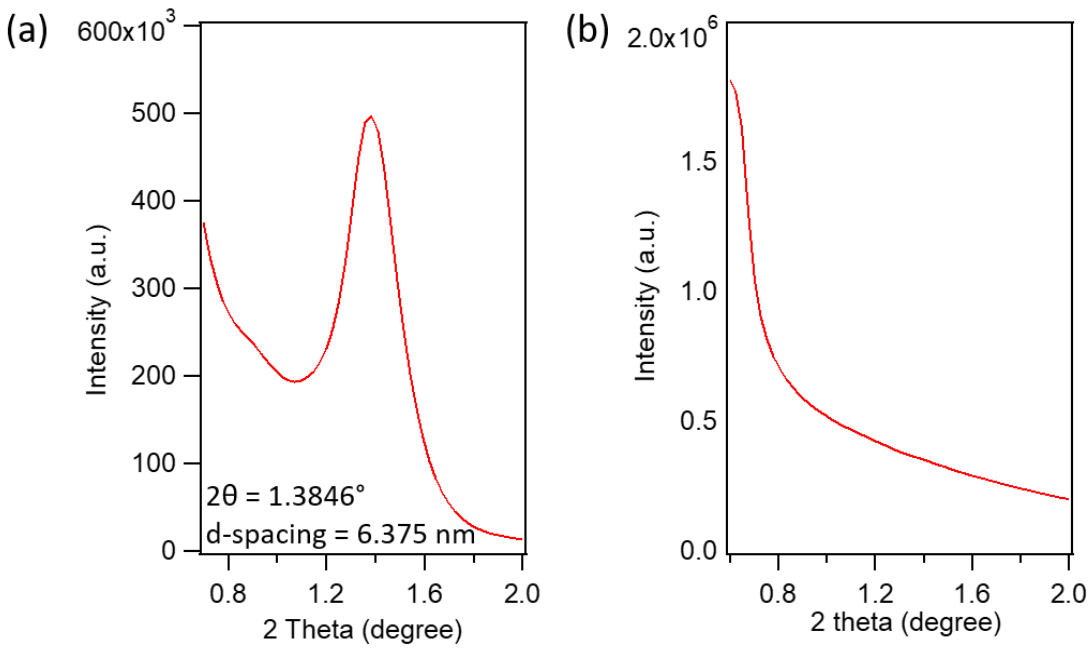

Figure 5-14. Small angle x-ray scattering (SAXS) of bare (a) and Ge infiltrated (b) mesoporous silica. (a) The 6 nm pore can be seen in the SAXS before infiltration, with a 2θ of 1.3846° and d-spacing of 6.375 nm. (b) After infiltration, no small angle signal can be detected, suggesting filling of the empty pores.

In addition to wide angle XRD, small angle x-ray scattering (SAXS) was used to characterize the mesoporous silica. Prior to infiltration, the 6 nm spherical pore is observed in the SAXS spectra, with at $2\theta = 1.3846°$, which corresponds to a d-spacing or pore diameter of 6.375 nm (**Figure 5-14 (a)**). After infiltration, the diffraction peak representing the pores in the template disappears, further confirming the pores in the mesoporous silica has been infiltrated with Ge using HPcCVD (**Figure 5-14 (b)**).

5.2.3. Transmission Electron Microscopy of HPcCVD Ge Infiltrated 3D Mesoporous Silica

In order to confirm the filling of the mesoporous silica visually, transmission electron microscope was used to characterize Ge infiltrated mesoporous silica. TEM samples were

prepared as described in *Section 3.5*. **Figure 5-15** shows the bright field TEM image of the Ge infiltrated sample, where the darker spots represents Ge as it has a higher Z-contrast (larger atomic number). In addition to the infiltration, a-Ge film was deposited on the top surface (left in **Figure 5-15**). The porous network is observed in the TEM image.

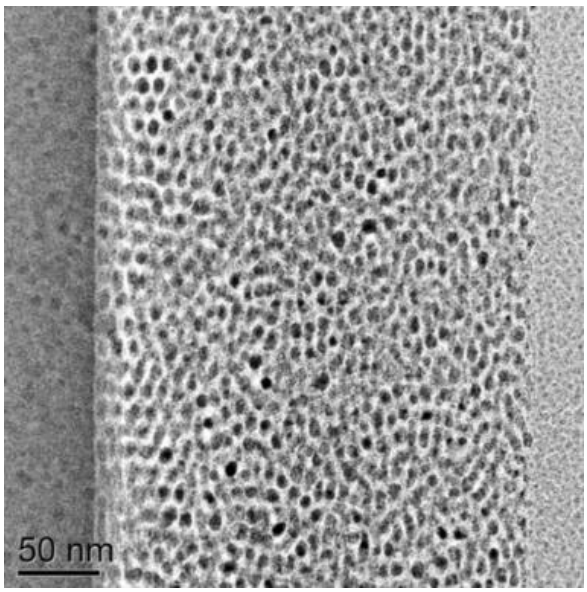

Figure 5-15. Bright field TEM images of 6 nm Ge infiltrated silica mesoprous silica. Shown on the left is the Ge layer deposited on the top surface and on the right is the Si substrate. TEM credit: Shih-Ying Yu.

Both small angle x-ray scattering and TEM characterization suggests that Ge can be deposited in the pores of 3D mesoporous silica template using HPcCVD. High pressure is a versatile technique in delivering various semiconductor materials in nano-pores of various templates. Further characterization is needed to confirm the interconnectivity (chemically and electrically) of these smaller metalattices. Promising results are shown here which could further advance the choice of periodicity and symmetry synthesized by combining nano-templates and HPcCVD.

5.3. Metal-Organic Frameworks

In addition to zeolite Y, another group of materials for atom precise metalattice fabrication is metal-organic frameworks (MOFs). MOFs are 3D solids with metals ions interconnected by organic species, while some have an open framework network for infiltration, some have only closed pores. MOFs contain molecular bridges to organize metal ions with a fixed distance to create pores of less than 2 nm in diameter. MOFs can be synthesized in large quantities and made with tunable 3D interconnected pores (as well as 1 D channels) by using molecular building blocks[29]. The pores in MOFs can be used for materials storage such as hydrogen storage or as a host site for nano-clusters synthesis. Since the pores are created by organizing molecular bridges and metal ion species, the precision of pore organization is down to atomic scales. Unfortunately, most metal-organic frameworks are not stable at high temperatures[30–32], which makes chemical vapor deposition in the pores of MOFs difficult as elevated temperatures are needed to decompose precursor gas molecules. Most often, MOFs decompose at high temperature when the node (metal sites) linker (organic molecular bridges) bonds breaks. The linkers then decompose to break down the framework. Other possibilities of thermal degradation could be due to MOF amorphization, melting, metal cluster dehydration and molecular bridges graphitization[30]. Most conventional CVD methods require a high temperature for precursor decomposition, making it unsuitable for materials infiltration in MOFs. High pressure can be used to reduce the deposition temperature to down to 150 °C for boron doped Si[33] (p-Si). A small amount of diborane (B_2H_6) can be added to the gas mixture to dope Si for p-Si.

HKUST-1 (CuBTC, copper 1, 3, 5-benezenetricarboxylate (BTC)) has an open framework network, and a relatively high thermal stability up to about 300 °C with the organic linkers decomposing at about 360 °C [32]. HKUST-1 is a face-centered-cubic crystal with interconnected 3D square shaped pores of 9 Å x 9 Å [34]. The large pore sizes and open network

would allow silane and germane gas molecules to enter the pores to deposit Si and Ge. p-Si HPcCVD was used to infiltration materials into the pores for its low deposition temperature. The infiltration was carried out in the 2D/3D HPcCVD closed reactor using 2% SiH_4 by partial pressure in He and a B_2H_6/ SiH_4 ratio of 0.013. However, HKUST-1 decomposes after infiltration as shown by the powder XRD (**Figure 5-16**). HKUST-1 was heated at the same temperature under high pressure conditions in helium gas, which had no effect on the structure (**Figure 5-16**, red curve), which suggest the framework is stable at deposition temperatures. We theorize that the metal ions, Cu, are being reduced by hydrogen, a by-product of silane pyrolysis during HPcCVD infiltration. To further understand the decomposition of the framework during HPcCVD infiltration and to determine a better strategy in selecting MOFs for infiltration, HKUST-1 was heated in 10 % H_2 in He to mimic deposition conditions. After heat treatment at 175 °C in hydrogen environment, HKUST-1 decomposed showing no XRD pattern similar to **Figure 5-16, green curve**. After this studies, only MOFs with metal ions that can sustain high temperature in reducing environment were considered.

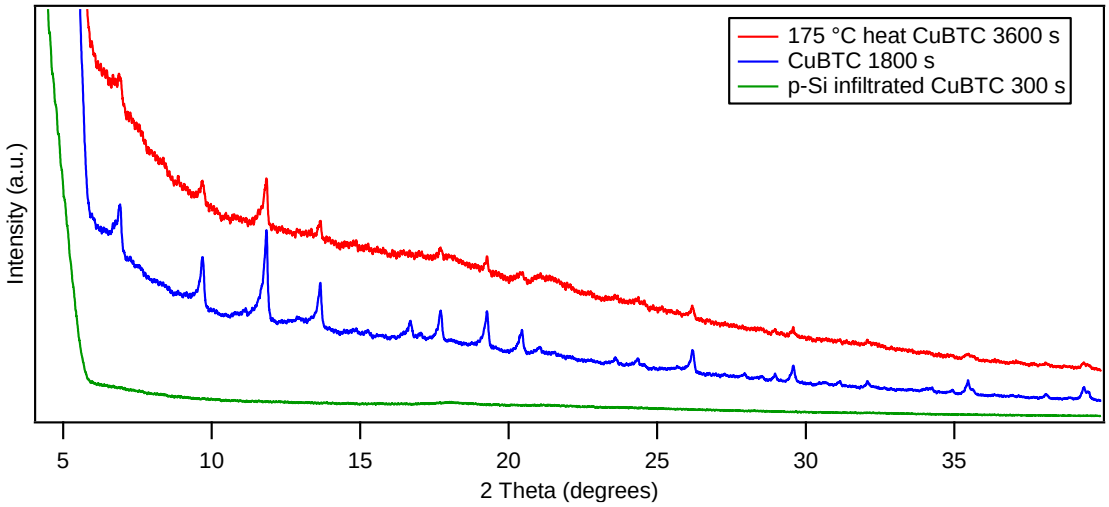

Figure 5-16. Powder XRD of HKUST-1 after heat treatment and silicon infiltration attempts. The crystalline diffraction pattern of HKUST-1 can be seen before infiltration and after heat treatment at high pressure at the deposition temperature of 175 °C. However, after p-Si infiltration at the same temperature, the solid had decomposed as shown by the power XRD pattern.

Some of the metal ions that are stable, or have a higher metal activity as compared to hydrogen, include Al and Zn. MIL-53 (Al), $[Al(OH)1, 4\text{-terephthalate})]_n$ has a 3D framework structure and 1D channels along the a-axis[35]. The material has been reported to be stable at up to 500 °C and contains Al as the metal ion instead of Cu, Ag or Au metals that have a tendency of being reduced by hydrogen. MIL-53 (Al) has 6.4 Å x 6.4 Å pores[29], and the pores are stretchable at high temperature. The initial heat test in reducing environment (10 % H_2 in He by partial pressure) suggests that the structure is stable at HPcCVD conditions (**Figure 5-17**). Further investigation will be carried out by other members of the Badding group to determine HPcCVD infiltration of MOFs to yield metalattices. Other templates, such as zirconium-based MOF UiO-66 with high thermal stability to maintain crystallinity and porosity at >500 °C [30] would be considered in future infiltration efforts.

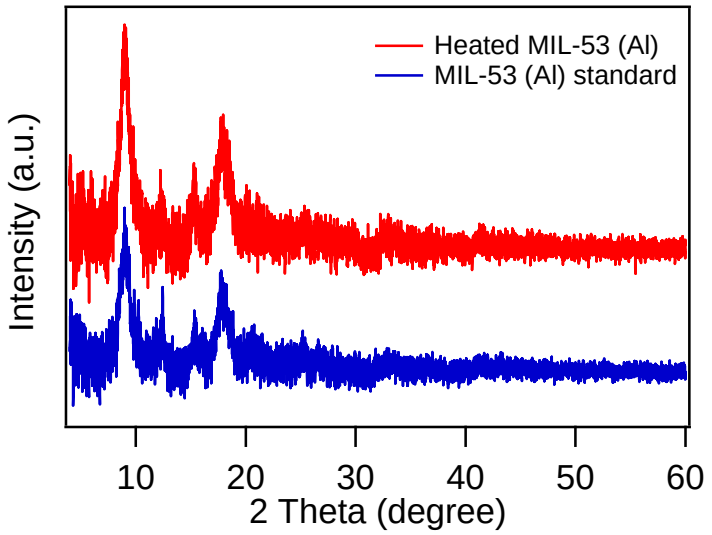

Figure 5-17. Powder XRD of MIL-53 (Al) and after heat treatment in reducing environment at deposition temperature.

5.4. Conclusion and Future Efforts

High pressure confined CVD has the ability to infiltrate pores down to a few nanometers in diameter to fabricate electronic grade semiconducting metalattices. The use of other templates, such as zeolite Y, 3D mesoporous silica and metal-organic frameworks, as shown in this chapter, expands the tenability of periodicity, symmetry and morphology of metalattices made by HPcCVD, including the possibility of metalattices with atom-precise control of where the meta-atoms and meta-bonds are located. Future studies are needed to further select appropriate templates for infiltration, but this work suggest that infiltration into smaller pores is possible using the unique high pressure confined chemical vapor deposition technique. Other characterization techniques should be used to confirm the inter-connectivity of the semiconductors infiltrated into this set of atom-precise templates shown in this chapter. For example, additional high resolution TEM imaging and tomography could be used to image the Si and Ge infiltrated zeolite Y. The zeolite template could be removed by HF acid washing[36] to obtain a zeolite templated silicon or germanium; if the structure stays connected after template removal, that could further suggest and provide evidence that a metalattice structure has been successfully created using HPcCVD and zeolites. Once it is confirmed that the semiconductors are interconnected in the pores of zeolite and other templates shown here, electrical and thermal transport will be of interest as they complete the studies of structural order and physical properties with smaller periodicity.

Other templates, such as those discussed in the previous section (MIL-53(Al) and UiO-66 (Zn)) could be used for HPcCVD infiltration for metalattices of other periodicity, sizes and symmetry. In addition, the development of large area fabrication of highly ordered 3D mesoporous silica[37],metalattice, up to cm in sizes, could be possible with small periodicity for device fabrication.

5.5. References

1. Moshoeshoe, M., Nadiye-tabbiruka, M. S. & Obuseng, V. A Review of the Chemistry , Structure , Properties and Applications of Zeolites. *Am. J. Mater. Sci.* **7,** 196–221 (2017).
2. Wang, S. & Peng, Y. Natural zeolites as effective adsorbents in water and wastewater treatment. *Chem. Eng. J.* **156,** 11–24 (2010).
3. Yilmaz, B. & Muller, U. Catalytic Applications of Zeolites in Chemical Industry. *Top. Catal.* **52,** 888–895 (2009).
4. McLeary, E. E., Jansen, J. C. & Kapteijn, F. Zeolite based films , membranes and membrane reactors : Progress and prospects. *Microporous Mesoporous Mater.* **90,** 198–220 (2006).
5. Cruciani, G. Zeolites upon heating : Factors governing their thermal stability and structural changes. *J. Phys. Chem. Solids* **67,** 1973–1994 (2006).
6. Jacobs, P. A., Flanigen, E. M., Jansen, J. C. & van Bekkum, H. *Introduction to Zeolite Science and Practice*. (Elsevier Science, 2001).
7. Lutz, W. Zeolite Y : Synthesis , Modification , and Properties — A Case Revisited. *Adv. Mater. Sci. Eng.* **2014,** 724248 (2014).
8. Jeong, N. C., Kim, H. S. & Yoon, K. B. New Insights into CdS Quantum Dots in Zeolite - Y. *J. Phys. Chem. C* **111,** 10298–10312 (2007).
9. White, J. C. & Dutta, P. K. Assembly of Nanoparticles in Zeolite Y for the Photocatalytic Generation of Hydrogen from Water. *J. Phys. Chem. C* **115,** 2938–2947 (2011).
10. Dougall, J. E. Mac *et al.* Synthesis and Characterization of III-V Semiconductor Clusters: GaP in Zeolite Y. *J. Am. Chem. Soc.* **111,** 8006–8007 (1989).
11. Marquez, F. & Fornes, V. Synthesis and characterisation of Ga2S3 semiconductor included in zeolite Y. *Solid State Commun.* **112,** 17–20 (1999).

12. He, J. *et al.* Encapsulation of Silicon Nanoclusters in Zeolite Y. *J. Am. Chem. Soc.* **120,** 10697–10705 (1998).

13. Dag, O., Kuperman, A., Macdonald, P. M. & Ozin, G. A. in *Zeolites and Related Microporous Materials: State of the Art* **84,** 1107–1114 (1994).

14. Dag, O., Kuperman, A. & Ozin, G. A. Germanium Nanoclusters: Chemical Vapor Deposition of Digermane in Zeolite Y and Mordenite. *Adv. Mater.* **6,** 147–150 (1994).

15. Miguez, H., Fornés, V., Meseguer, F., Marquez, F. & Lopez, C. Low-temperature synthesis of Ge nanocrystals in zeolite Y. *Appl. Phys. Lett.* **69,** 2347–2349 (1996).

16. Tomiya, S. *et al.* Germanium Loaded Zeolite Y: preparation and characterization. *Mat. Res. Sco. Symp. Proc.* **286,** 353–358 (1993).

17. He, J. *et al.* The nature of encapsulated silicon nanoclusters in zeolite Y. *Appl. Phys. Lett.* **74,** 830–832 (1999).

18. Seidel, A., Loos, J. & Boddenberg, B. Copper nanoparticles in zeolite Y. *J. Mater. Chem.* **9,** 2495–2498 (1999).

19. Treacy, M. M. J. *Collection of Simulated XRD Powder Patterns for Zeolites*. (Elsevier, 2001).

20. Sazio, P. J. A. *et al.* Microstructured Optical Fibers as High-Pressure Microfluidic Reactors. *Science (80-.).* **311,** 1583–1586 (2006).

21. Knops-Gerrits, P.-P., Vos, D. E. De, Feijen, E. J. P. & Jacobs, P. A. Raman spectroscopy on zeolites. *Microporous Mater.* **8,** 3–17 (1997).

22. Yu, Y., Xiong, G., Li, C. & Xiao, F. Characterization of aluminosilicate zeolites by UV Raman spectroscopy. *Microporous Mesoporous Mater.* **46,** 23–34 (2001).

23. Csencsits, R. & Gronsky, R. Damage of zelite Y in the TEM and its effects on TEM images. *Ultramicroscopy* **23,** 421–431 (1987).

24. Huo, Q., Margolese, D. I. & Stucky, G. D. Surfactant Control of Phases in the Synthesis of

Mesoporous Silica-Based Materials. *Chem. Mater.* **8,** 1147–1160 (1996).

25. Zhao, D., Huo, Q., Feng, J., Chmelka, B. F. & Stucky, G. D. Nonionic Triblock and Star Diblock Copolymer and Oligomeric Surfactant Syntheses of Highly Ordered , Hydrothermally Stable , Mesoporous Silica Structures. *J. Am. Chem. Soc.* **120,** 6024–6036 (1998).
26. Besson, S., Gacoin, T., Ricolleau, C., Jacquiod, C. & Boilot, J. P. 3D Quantum Dot Lattice Inside Mesoporous Silica Films. *Nano Lett.* **2,** 409–414 (2002).
27. Coleman, N. R. B. *et al.* Synthesis and Characterization of Dimensionally Ordered Semiconductor Nanowires within Mesoporous Silica. *J. Am. Chem. Soc.* **123,** 7010–7016 (2001).
28. Gao, F., Lu, Q., Liu, X., Yan, Y. & Zhao, D. Controlled Synthesis of Semiconductor PbS Nanocrystals and Nanowires Inside Mesoporous Silica SBA-15 Phase. *Nano Lett.* **1,** 743–748 (2001).
29. Rowsell, J. L. C. & Yaghi, O. M. Minireviews Strategies for Hydrogen Storage in Metal – Organic Frameworks. *Angew. Chem. Int. Ed.* **44,** 4670–4679 (2005).
30. Howarth, A. J. *et al.* Chemical, thermal and mechanical stabilities of metal–organic frameworks. *Nat. Rev. - Mater.* **1,** 15018 (2016).
31. Mu, B. & Walton, K. S. Thermal Analysis and Heat Capacity Study of Metal À Organic Frameworks. *J. Phys. Chem. C* **115,** 22748–22754 (2011).
32. Yuan, B., Yin, X., Liu, X., Li, X. & Sun, L. Enhanced Hydrothermal Stability and Catalytic Performance of HKUST - 1 by Incorporating Carboxyl-Functionalized Attapulgite. *ACS Appl. Mater. Interfaces* **8,** 16457–16464 (2016).
33. He, R. *et al.* Silicon p-i-n junction fibers. *Adv. Mater.* **25,** 1461–1467 (2013).
34. Prestipino, C. *et al.* Local Structure of Framework Cu(II) in HKUST-1 Metallorganic Framework: Spectroscopic Characterization upon Activation and Interaction with

Adsorbates. *Chem. Mater.* **18,** 1337–1346 (2006).

35. Meilikhov, M., Yusenko, K. & Fischer, R. A. Incorporation of metallocenes into the channel structured Metal – Organic Frameworks MIL-53(Al) and MIL-47(V). *Dalt. Trans.* **53,** 10990–10999 (2010).

36. Nueangnoraj, K. *et al.* Formation of crosslinked-fullerene-like framework as negative replica of zeolite y. *Carbon N. Y.* **62,** 455–464 (2013).

37. Kobayashi, M. *et al.* Thickness control of 3-dimensional mesoporous silica ultrathin films by wet-etching. *Nanoscale* **9,** 8321–8329 (2017).

Chapter 6

High Pressure Confined Chemical Vapor Deposition of Silicon Based Functional Materials

Silicon, as one the most abundant element in the earth's crust with oxygen and aluminum, is the most industrially relevant semiconductor. Over the years, scientists have found ways to incorporate silicon into new electronic devices, such as transistors, diodes, photodetectors and solar cells. High quality materials grade silicon is needed for advanced functionality, and can be obtained easily through chemical vapor deposition. However, CVD faces challenge when the features sizes drops to the micrometer and nanometer scales. Functional materials in 1D and 2D geometrics, such as optical fibers[1–9] and 2D thin films[10] can be fabricated by HPcCVD. This chapter explores the use of high pressure confined chemical vapor deposition to fabricate functional materials other than electronic metalattices shown is *Chapter 1-5*.

6.1. Conductive Silicon Glue

Wafer to wafer bonding plays an important part of modern day technological developments, including new stacked structures, Complementary-Metal-Oxide-Semiconductor (CMOS) technologies, Micro-Electro-Mechanical (MEM) systems, microelectronics, transistors, and integrated circuits[11–14]. Various methods in connecting substrate to substrate such as anodic bonding[15], adhesion bonding[12], eutectic bonding[16], glass frit soldering[17], thermo-compression bonding[18] and direct wafer bonding[11,13,14,19] have been developed. Anodic bonding requires alkaline glass as one of the substrates, limiting the combination of binding materials. Adhesion bonding, eutectic bonding and glass fritting all uses an additional material to essentially glue two

substrates together, which allows for different materials bonding. However, most adhesion bonding is done using polymers and therefore cannot achieve hermetic seals, meaning that it has limited stability against temperature, moisture and chemicals[12]. Eutectic bonding faces similar challenges as the bonded substrates cannot be heated above the eutectic point of the materials used[16]. Glass fritting can create hermetic seals. Glass frit is a dielectric material used to bond between two substrates by thermo-compression, which is suitable when an insulating material is needed between layers. However, electrical transport through the stacked structures is difficult. Direct wafer bonding has the advantage of directly creating chemical bond between two substrates made of the same material or dissimilar materials through careful physical and chemical surface preparation. Many materials, including Si, SiO_2, Ge, III-V compound semiconductors, glass, metals, and perovskites can use direct wafer bonding to create stacking structures[14]. Direct wafer bonding has issues in that it requires extensive wafer preparation processes to ensure particle free and metallic contamination free substrates prior to bonding. The interaction between two substrates and the mechanical strength of the bonding depends on the substrate preparation. A method for both homogeneous and heterogeneous substrates bonding without the need to extensively prepare the surface to yield a highly stable stack structure would be advantageous. One possible method is to use high pressure chemical vapor deposition, where we have already seen success in filling small pores void free, to bond together substrates made of the same or different materials. In addition, multiple materials can be deposited using HPcCVD, which could allow for interfacial physics design to maintain electronic and thermal (phonon) transport between layers.

6.1.1. HPcCVD Bonding of Two Substrates

High pressure confined chemical vapor deposition (HPcCVD) can be used to deposit conductive materials, such as hydrogenated amorphous silicon and crystalline silicon for wafer bonding purposes. Precursor gas molecules in HPcCVD can penetrate into the gap between two substrates to then deposit materials on the inside and create a chemically bonded, yet electrically connected layer between two substrates. Previous studies have shown that HPcCVD can be used to fully fill silica capillaries and deposit uniformly over large area. The increase in pressure lowers the mean free path of gas molecules to increase gas collusion for fast transport of precursors into small confined spaces. In the case of wafer bonding, Si can be deposited between two flat substrates that are in contact, with minimal spaces in between. Prior to deposition, the wafers are cleaned with acetone and HPLC grade isopropyl alcohol to remove dust and debris. The substrates are placed inside of a HPcCVD reactor as shown in *Section 2.3.1* without any spacer between the bonding surfaces. The spaces between two substrates are kept to minimum by using two set screws clapping the substrates together. HPcCVD reaction conditions similar to those described in *Chapter 2* were used with ~35 MPa total pressure of 5-10 % partial pressure of SiH_4 in He carrier gas and deposition temperature of 400 °C. **Figure 6-1** shows the SEM image of HPcCVD a-Si bonded single crystalline Si wafers. The SEM sample was prepared by cutting a HPcCVD bonded single crystal Si wafers using a dicing saw with a diamond blade, which was then polished with increasing grit polishing paper. The final polished surface was achieved using 50 nm colloidal silica polishing suspension. The distance between the two silicon wafers was 255 nm, and was filled with Si as shown by the SEM image (**Figure 6-1**). In addition to bonding Si wafers, the HPcCVD technique can also be used to bond other substrates, such as fused silica, quartz, borosilicate glass, germanium and sapphire. The two substrates being bonded do not have

to be made of the same materials. For example, Si wafers can be bonded to sapphire, allowing both homogeneous and heterogeneous wafer bonding.

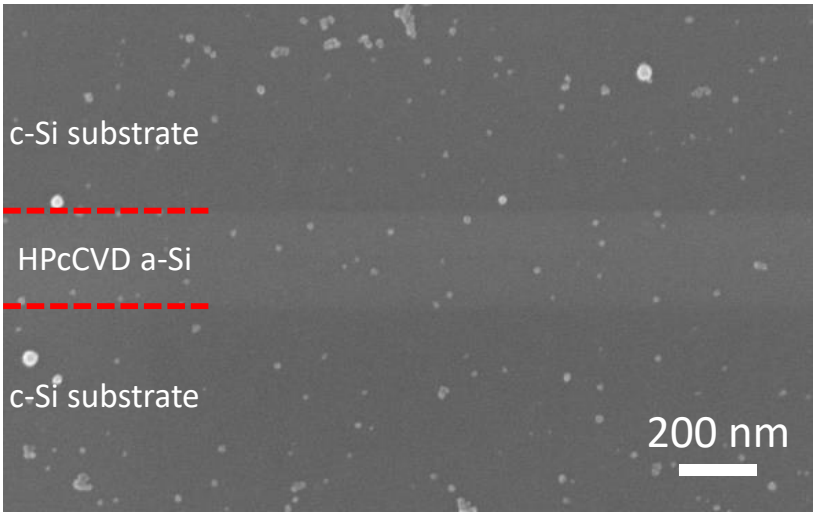

Figure 6-1. SEM Image of polished single crystalline Si wafers bonded using HPcCVD a-Si layer. The HPcCVD a-Si layer has a thickness of 255 nm.

6.1.2. Raman Analysis

HPcCVD wafer bonding of optically transparent substrates was characterized using Raman spectroscopy depth profiling with excitation wavelength of 633 nm. The step size was controlled by a motorized stage with increments of 100 nm. The penetration depth of crystalline Si at 633 nm is 3 μm[20], therefore depth profile scan with HPcCVD a-Si bonded c-Si wafers would not be possible because the wafers are too thick (280 μm) for the incident light to penetrate through. HPcCVD bonded sapphire-sapphire and sapphire-crystalline Si were studied. Typical depth profile mapping is shown in **Figure 6-2**. Position 0 is on the top of the surface and the stage moves up to move the focused plane toward the HPcCVD layer. Characteristic features from the substrates and HPcCVD layers are monitored, for example sapphire feature at 417 cm^{-1} [21] and HPcCVD amorphous Si feature at 480 cm^{-1} in the HPcCVD bonded sapphires (**Figure 6-**

3). As the focus plane reaches toward the HPcCVD a-Si layer, amorphous Si-Si stretching at 480 cm^{-1} emerges and the signature stretching from sapphire[21] at 417 cm^{-1} ceases.

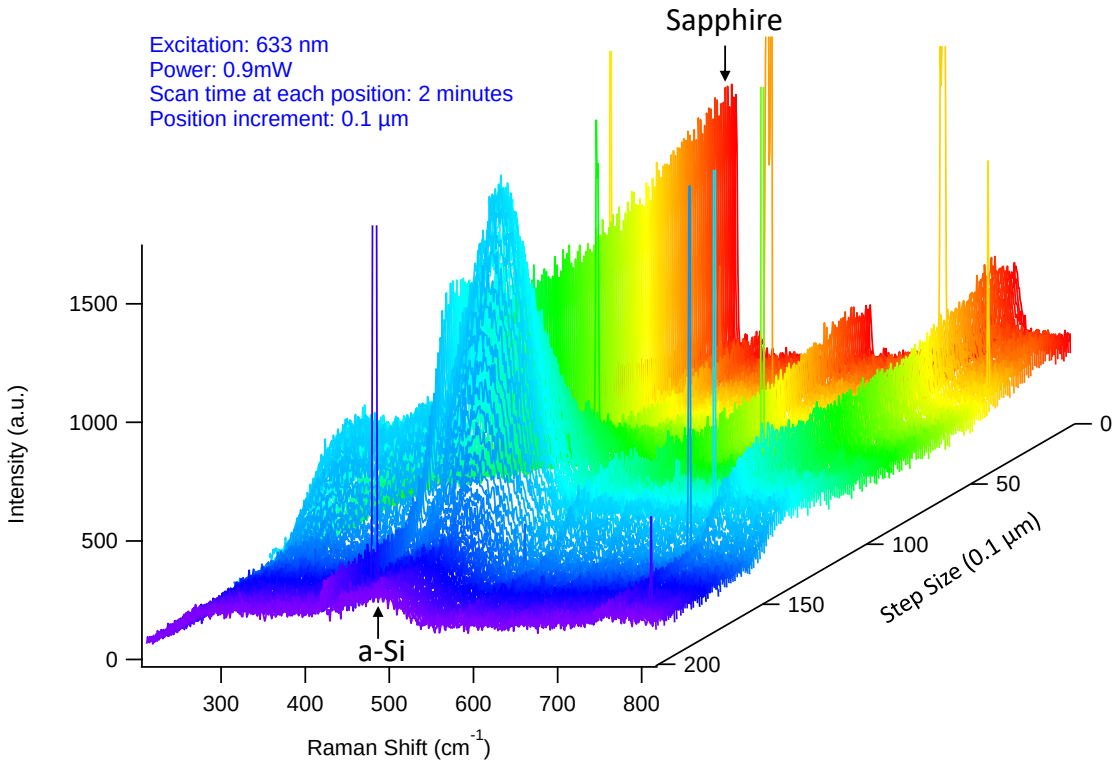

Figure 6-2. Raman mapping of HPcCVD a-Si bonding of sapphire substrates. The a-Si stretching at around 480 cm^{-1} and one of the stretching in sapphire at 417 cm^{-1} Raman shift can be used to probe the two materials.

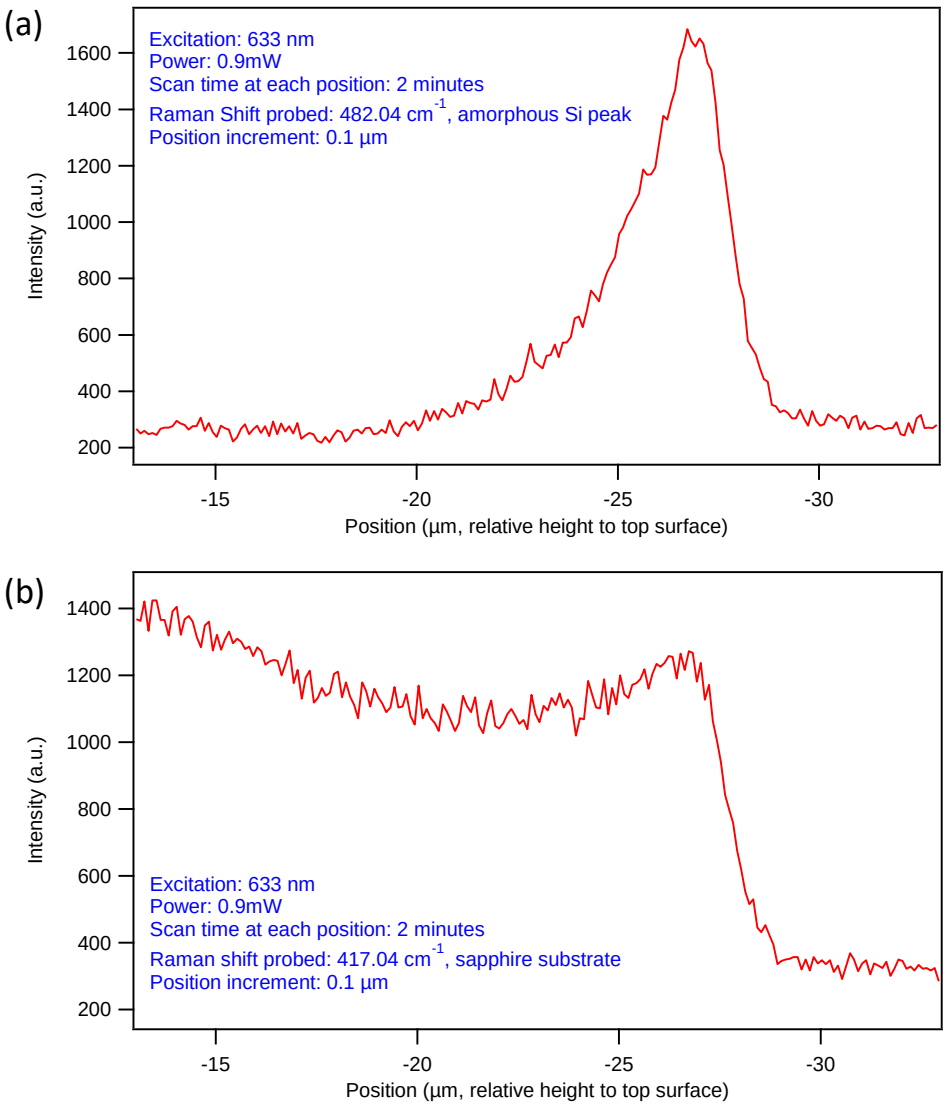

Figure 6-3. Raman depth profile of HPcCVD a-Si bonded sapphire substrates probing the (a) a-Si stretching at 480 cm^{-1} and (b) sapphire stretching at 417 cm^{-1} Raman shift. Position as shown is the arbitrary position relative to the top surface.

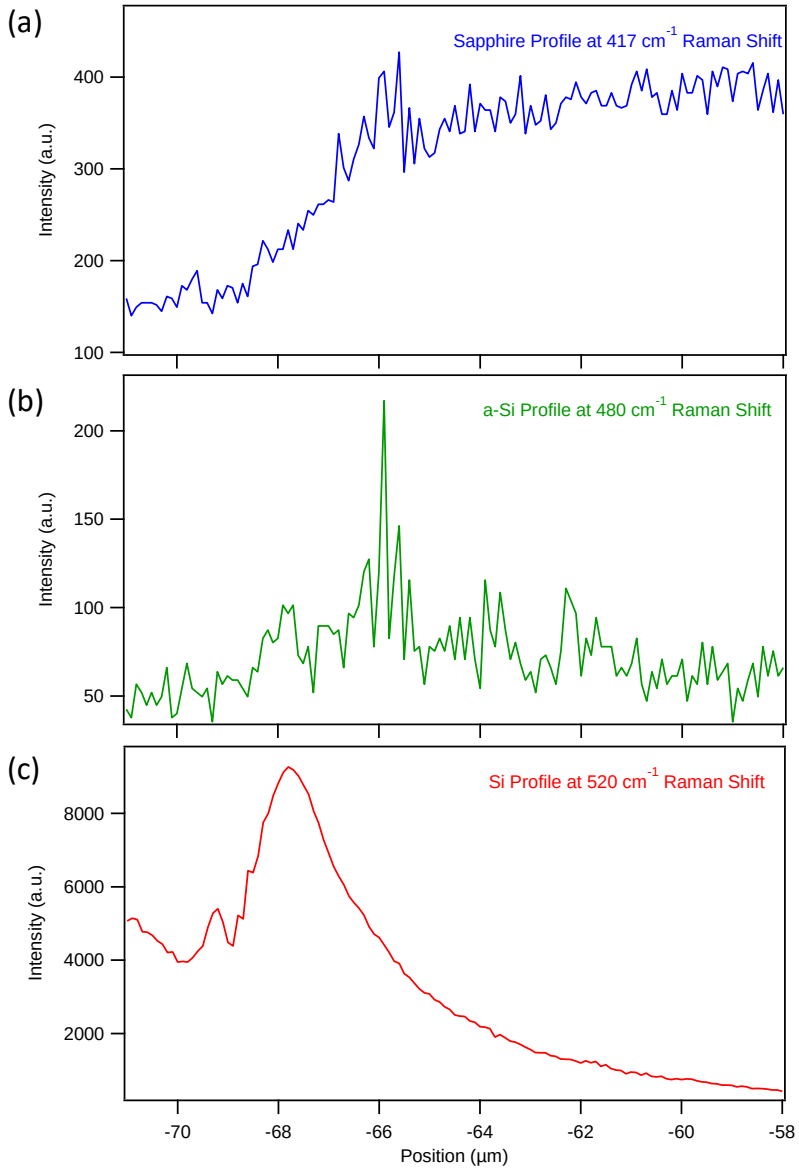

Figure 6-4. Raman mapping of the HPcCVD a-Si bonded single crystalline Si wafer to sapphire. The signature stretching of sapphire (a), a-Si (b) and c-Si (c) at 417 cm^{-1}, 480 cm^{-1} and 520 cm^{-1}, respectively, are probed. As the sapphire stretching decreases at -65 μm (arbitrary position from the top surface), the a-Si from HPcCVD arises, suggesting that a layer of a-Si is deposited between the substrates (at ~66 μm). Eventually, c-Si stretching has an increase in its intensity (from -66 μm to -68 μm) when the incident beam is focused closer to the Si substrate, away from the sapphire and HPcCVD a-Si layer.

Bonding of heterogeneous substrates is useful in building stacked structures. HPcCVD can be used to build stacked structures made of different substrates such as sapphire to c-Si wafer. The bonding layer is deposited at a-Si between two very different substrates with little to no requirement for substrate treatment. Most wafer bonding methods require extensive substrate cleaning and surface preparation, but HPcCVD allows for easy adaptation to different substrates. The bonding of sapphire and c-Si is monitor by Raman depth profiles. **Figure 6-4** shows the evolution of the materials from sapphire to the HPcCVD a-Si layer, then eventually the c-Si substrate.

6.1.3. Future Direction

SEM analysis and Raman depth profile mapping show that high pressure confined chemical deposition has the ability to chemically bond two substrates (homogeneous or heterogeneous) by depositing a thin layer of semiconductor, such as a-Si shown here, in the small gap between the two substrates. Further investigation on mechanical, electrical and thermal properties of the bonded substrates will allow better understanding of the performance of the materials. For example, the changes to electrical conductivity through two substrates should be studied as compared to other wafer bonding methods to determine if HPcCVD bonding can obtained electron transport for the bonded structure. In addition, other materials such as elemental semiconductors, compound semiconductors, doped semiconductors, metals and insulators could be used as the bonding layer to design interfacial chemistry and physics when fabricating electronic devices. To further improve the bonding method and reduce the distance between two substrates, it is possible to utilize intermolecular interactions, such as van der Waals forces and hydrogen bonds, between two substrates prior to HPcCVD infiltration.

6.2. Flexible Semiconductor Fabrics

Flexible electronics and wearable electronic consumer products have sparked great interest in the 21st century since the developments of light emitting diodes, thin film transistors in plastic substrates[22] and conductive flexible polymers[23]. Flexible electronic materials[24] are the basis in designing the next generation functional and designable products. In the current technology, we have already seen success in flexible screen displays[25], photovoltaics[26,27], medical devices[28], wearable electronics[29] and early stage research in electronic textiles[30–32]. This section will focus on the use of high pressure confined chemical vapor deposition (HPcCVD) for next generation fabrication of high performance flexible electronic devices. Flexible electronic devices can be fabricated either by the transfer of thin film conductive materials onto a substrate such as flexible polymers, or by direct conductive materials incorporation into the flexible parent material. The work described hereafter uses the second methods, where HPcCVD is used to deposit various semiconductors onto the surface of flexible substrates such as fiber glass fabrics, high temperature carbon based fabrics, cotton t-shirts and stainless steel fabrics.

6.2.1. Conformal Coatings Using High Pressure confined Chemical Vapor Deposition

Technological impacts has long been the driving force for developing new methods to synthesis high quality, uniform thin film semiconducting materials. Applications such as thin film solar cells[30,31], thin film transistors for liquid crystal displays[22,25] (LCD), sensing devices[33,34] and even electronic skin and paper[29] are some of the most attractive areas. Methods to synthesize thin films can be categorized to two major groups, by physical vapor deposition[35] (PVD) or chemical vapor deposition (CVD). In PVD, methods such as evaporation and sputtering are used, where the materials of interest is directly transferred to the substrate in gas phase by using heat,

electron beam or plasma to knock off atoms from the source to move them toward the deposition zone. The challenge with these techniques is the uniformity of the resultant film and limits to materials that can be deposited. While most materials, including germanium and silicon can be deposited using PVD[35], some other compound materials cannot be achieved because each components in the materials might have very different vapor pressure; the resultant material will end up with the incorrect stoichiometry. In addition, PVD methods have difficulties in depositing materials in small pores and deep trenches because PVDs operates at ultra-high vacuum to ensure high purity of deposited materials. The long molecular mean free path in PVDs prevents materials from entering and depositing onto complex substrate.

On the other hand, chemical vapor deposition (CVD) can be performed at various experimental condition, such as low pressure, atmospheric pressure and high pressure. In addition, atomic layer deposition (ALD) [36] which uses pulses of varying gas precursors for layer-by-layer materials deposition is excellent in uniformly coating smalls pores and complicated structures. However, ALD has its own limitations; ALD relies on proper surface chemistry management for self quench reactions to ensure that only one layer of materials can be deposited for each incoming pulse of precursors. The substrates allowed in ALD are limited and must be properly treated for the desire surface reaction. Moreover, ALD has a slow growth rate because only one layer of materials is deposited at each pulse of precursor gas. For example, the growth rate of c-Si is 0.004 – 0.09 Å/s while the growth rate of hydrogenated amorphous silicon (a-Si:H) is 2 Å/s in plasma enhanced CVD (PECVD) [37] and 3.7 Å/s in high pressure CVD [2]. HPcCVD has the advantages of high precursor gas mobility and increase rate of reaction because the small molecular mean free path promotes gas molecules collision. Previous thin film studies have shown HPcCVD's ability to conformally coat large area with a-Si:H, a task which has

traditionally been performed by PECVD or hot wire CVD, methods that require complex deposition system and high cost equipment.

a-Si:H is a technologically relevant semiconductor for many applications, including those discussed earlier in this section. Hydrogen incorporation in the material is used to passivate the amorphous silicon for improved electrical and optical properties. A low enough temperature is require to prevent hydrogen leakage from the deposited materials. At temperatures above 500 °C [37], hydrogen can obtain enough energy to diffuse out of the amorphous silicon. HPcCVD has the ability to decrease the deposition temperature and increase the amount of hydrogen incorporation in a-Si:H. In addition to a-Si:H, HPcCVD can also conformally coat complex substrates and structures with other materials such as a-Si, c-Si, n^+ type a-Si:H, a-Ge, a-Ge:H, c-Ge and n^+type a-Ge:H to fabricate functional textiles.

6.2.2. HPcCVD of Si and Ge Fabrics

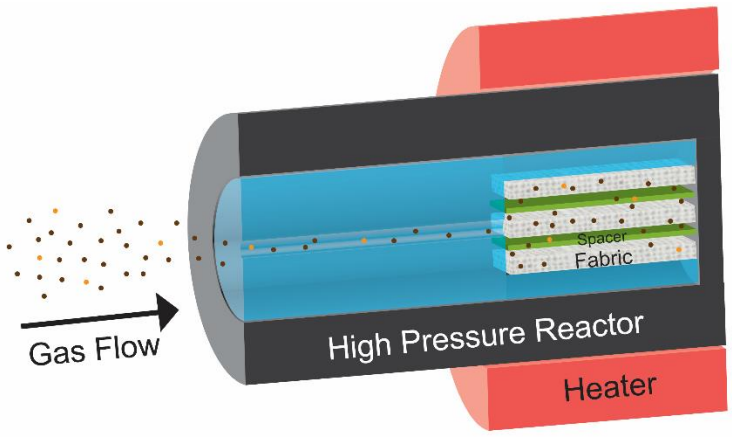

Figure 6-5. Schematic of reactor geometry for electronic fabrics fabrication using HPcCVD. Reaction conditions are similar to those described in *Section 2.3.1*, but with longer bake time and reaction time to allow for complete removal of air and moisture.

HPcCVD can be used to synthesize flexible electronic fabrics by infiltrating semiconductors into and on common textiles such as woven cotton (the substrate) without damaging the parent substrate. The process is similar to HPcCVD infiltration as discussed in *Section 2.3.1*, except the substrate is replaced by fabrics (**Figure 6-5**). The reaction temperature of a-Si:H and n^+-type a-Si:H were done at 400 °C, except when lower temperature is needed to prevent template degradation, for example n^+-type a-Si:H was deposited at 300 - 350 °C when using cotton cloths. a-Ge:H was deposited at 300 °C and n^+-type a-Ge:H was deposited at 250 °C. A longer bake of 6 hours in vacuum was used prior to introduction of precursor gas into the reaction chamber to effectively remove absorbed air and moisture in the cloths. The deposition time ranged from 3-6 hours depending on the thickness of materials in order to ensure deposition into and on top of the substrate. A series of substrates was tested to demonstrate HPcCVD's unique ability to fabricate electronic fabrics with different parent materials. The decomposition temperature of the parent substrate was considered greatly in accessing their feasibility, as HPcCVD does requires an elevated temperature, even it is much lower than of other types of CVD. In addition to high temperature resistivity, the geometry of the fabric was important to satisfy reactor confinement in HPcCVD. For example, for the stainless steel fabric, if the fibers were too thick, > 500μm, the spacing between the fabrics is no longer confined. Homogeneous gas phase reaction dominates in un-confined reactors to promote particle formation in gas phase and reduce the possibility of thin film coating on the substrate. Fabrics with small and fine fibers were selected to ensure the reaction is confined for thin film coatings. All of the parents materials selected here shows reasonable amount of semiconductor deposited with HPcCVD, including woven cotton shirt (made of cellulose) with a degradation temperature of 300 – 355 °C [38].

Figure 6-6 shows successful infiltration of n^+-type a-Ge:H using HPcCVD, the SEM and EDS mapping of the infiltrated and coated sample shows (cross-sectional images **Figure 6-6 (d)–(f)**) that the semiconductor has infiltrated and coated the parent cotton fabric. In addition to the coatings on the outer surface of the cotton fibers, the fibers are inter-connected by HPcCVD Ge after deposition, providing an electrically connected, yet flexible electronic fabric. The low deposition temperature (250 °C for n^+ type Ge) allowed in HPcCVD prevents breakdown of the cotton fabric during deposition. The demonstration of Ge infused cotton cloth is the first step toward functional fabrics.

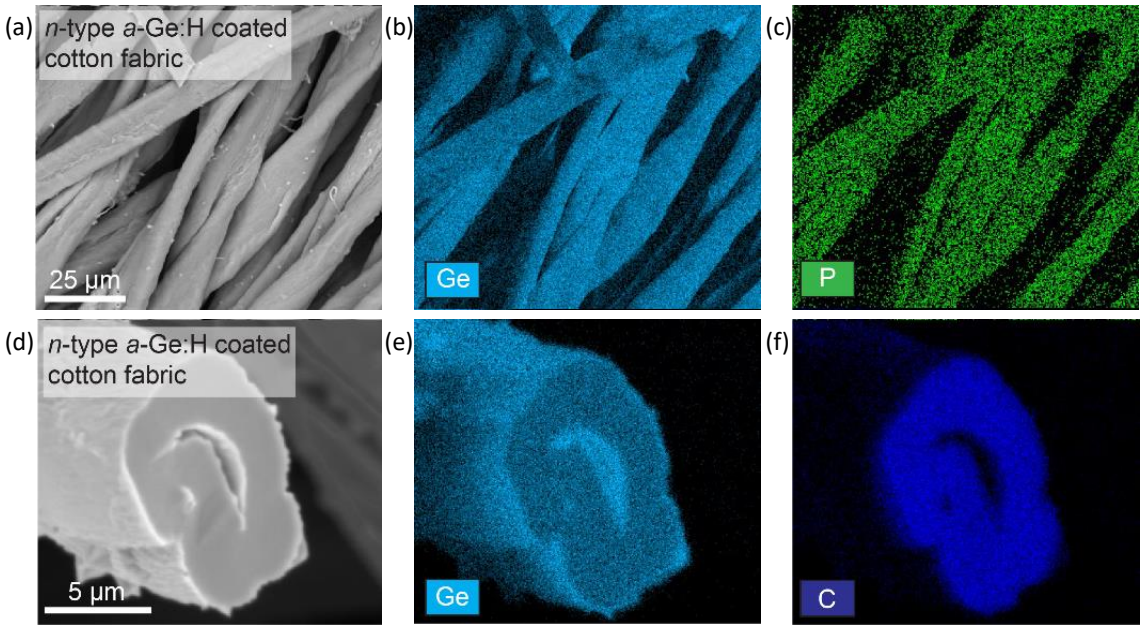

Figure 6-6. SEM and EDS Mapping for n^+-type a-Ge:H infiltrated and coated cotton fabric. (a) – (c) show the top surface of the HPcCVD cotton with Ge and P mapping. The semiconductor was doped by using a mixture of GeH_4 and PH_3. (d) – (f) shows the cross-sectional image after infiltration. The sample was cross-sectioned after infiltration, suggesting that the Ge has been infiltrated in-between the cotton fibers and coated the other surface. The outer surface has a lower concentration of carbon as shown in (f) because it has been coated by a thicker layer of Ge. SEM credit: Xiaoyu Ji.

In addition to cotton cloth, high temperature resistant carbon cloth (**Figure 6-7**) was used for fabrication of silicon electronic fabrics, which has a higher HPcCVD deposition temperature than that of Ge. For a deposition time of 6 hours, n^+-type a-Si:H was deposited using SiH_4 and PH_3 precursor gas mixture. SEM and energy dispersive X-ray spectroscopy (EDX) mapping of the fabrics shows that both Si and P have been incorporated into the structure (**Figure 6-8**). A Si and Ge dopant concentration of $10^{18} – 10^{20}$ atoms/ cm^3 can be observed in SEM EDX mapping[39]. The dopant concentration is expected to be in the range of $10^{19} – 10^{20}$ atoms/ cm^3 from previous studies[4,40]. Due to the high characterization x-ray excitation volume of 1 μm, the parent carbon fiber chemical analysis can be seen under EDS mapping (**Figure 6-8 (d), (h)**). The conformal semiconductor coating on the parent material can be shown by the cross-sectional EDS mapping in **Figure 6-9**. Since most of the semiconductors have coated the outer surface of the fabric fibers, a lower concentration C can be seen on the surface. Some of the Si was also infiltrated within a single fabric fiber, as suggested by the EDS mapping of the cross-section in **Figure 6-9 (c)**; the cross section was made after infiltration to reveal the internal chemical composition of the fabric fibers.

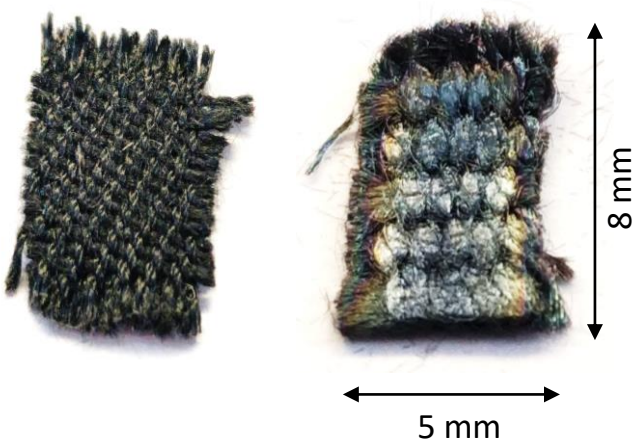

Figure 6-7. Pictures of carbon fabric before (left) and after (right) HPcCVD infiltration. The sample was 8 mm and 5 mm across in length and width. The color change after infiltration is due to the thin film interference effect of the Si thin film that was deposited onto the substrate. The flexibility of the fabrics remains after infiltration.

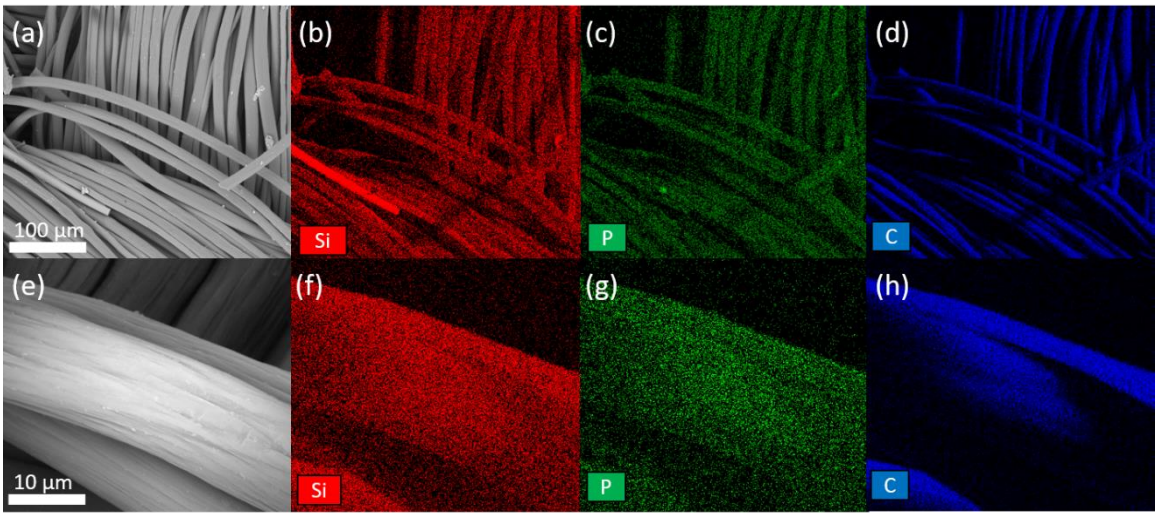

Figure 6-8. SEM Images and EDS mapping of n^+-type a-Si:H carbon fabric after HPcCVD. The fabric fibers were not damaged as shown by the SEM image. Uniform coating on the surface is observed. The concentrate of carbon in EDS mapping was low because most a layer of Si was deposited on top of the fiber to cover up the C signals. SEM credit: Xiaoyu Ji.

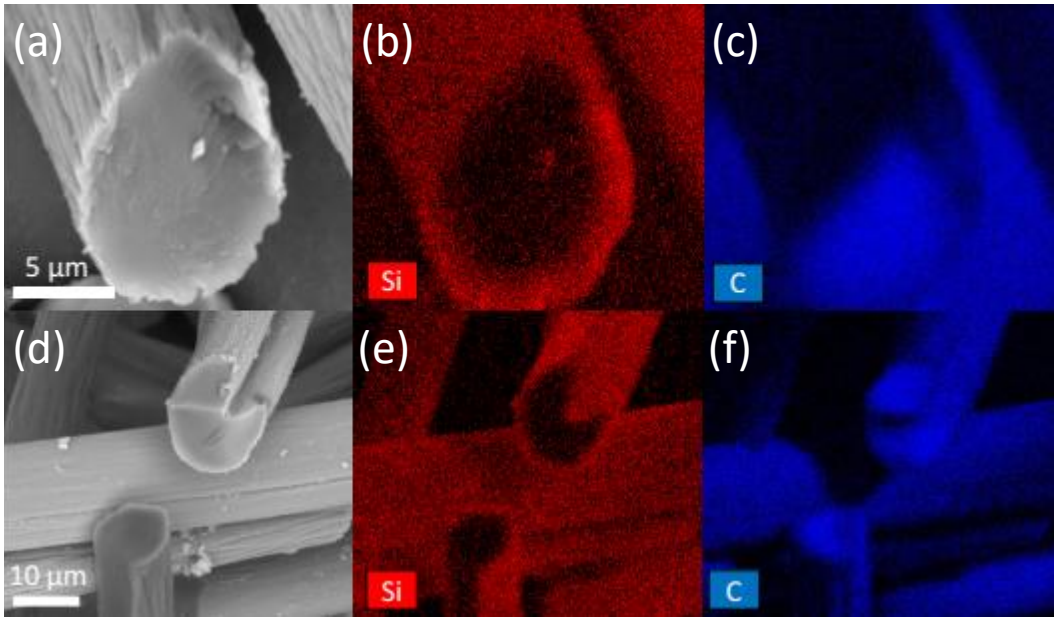

Figure 6-9. SEM Images and EDS mapping of cross-section of n^+-type a-Si:H carbon fabric after HPcCVD. The concentration of carbon is less on the outer surface than in the core, suggesting Si has uniformly coated the fabric fibers. Si can also be seen in the core of the fabric fibers because precursor gas can travel into the core to deposit at those location. SEM credit: Xiaoyu Ji

Another fabrics candidate for HPcCVD electronic fabrics is high temperature silica fiber cloths, which is often used as welding curtains or protective gears for high temperature processing. Such templates can withstand temperatures > 500 °C, which is suitable for a-Si:H coatings at 450 °C (**Figure 6-10**).

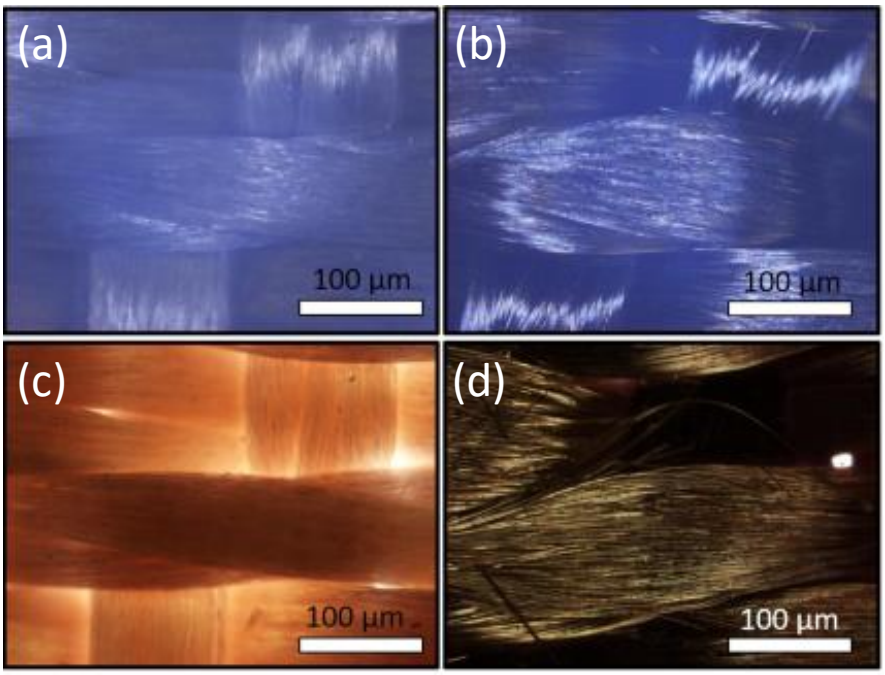

Figure 6-10. Microscope images of silica fiber fabrics before (left) and after (right) HPcCVD. (a) and (b) are imaged under reflected light and (c) and (d) are imaged under transmitted light. After infiltration, the fabrics appears to be darker with coating of silicon on the outer surface. The deposition was done at 450 °C.

6.2.3. Proof-of-Concept Schottky Junction Fabric

The success in conformal coatings on various templates shown in the previous section provides encouraging results that HPcCVD can be used to deposit semiconductor to fabricate photovoltaic cells directly onto flexible substrates. The work shown in this section is in collaboration if Dr. Xiaoyu Ji from Dr. Venkatraman Gopalan's research group at Penn State University. The ability of HPcCVD to conformally coat each string of the fibers provides a way to integrate electronic and optoelectronic inorganic materials. Most of the current technology and research relies on the transfer of inorganic materials to a flexible substrate, rather than direct integration of solar cells onto fabrics[41]. Solution phase[23] and vapor phase[42–44] approaches have been used in some of the direct integration examples, but solution phase techniques suffer from irregular wetting, surface chemistry issues and flow induced crystallization to yield poor conformal coating at the microscale[42]. Vapor deposition processes were also used to uniformly coat fabrics, such as studies by Andrew et. al. using vapor phase organic chemistries[42,43], but no photovoltaic characterizations was reported for the prepared solar fabric. a-Si:H *p-i-n* junctions on fiber glass fabric[45] was made using plasma enhance CVD by Plentz et. al., but PECVD itself uses a high cost complex deposition system and it was not clear if the individual fibers were conformally coated with materials like was shown with HPcCVD fabrics. Other attempts in fabricating photovoltaic cells using individual fibers and wires have been made[4,26,46,47]; however, additional weaving is needed to yield an electronic fabric, which can cause damage to the electronic materials and the active layer[32]. A technique like HPcCVD which can directly deposited various semiconductors on a flexible substrate is advantageous.

Here we explore the use of HPcCVD to fabricate flexible photovoltaic cells by integrating a conductive flexible fabric and silicon. The fabric choice was a stainless steel mesh purchased from Direct Metal with fabric fiber diameter of 25 μm and opening pores of 38 μm x

38 μm squares. Stainless steel has good conductivity and high strength at small diameters with smooth surfaces, making it a good candidate as an electrode for organic photovoltaic fibers[27]. We have fabricated a Schottky junction structure on the stainless steel fabrics by depositing a 300 nm thick layer of n^+-*type* a-Si:H and a 1 μm thick intrinsic a-Si:H coating each strings of the parent fabric using HPcCVD. The n-Si coating on the surface of the fabric is uniform as confirmed by the SEM and EDS mappings (**Figure 6-11**). In addition, **Figure 6-11 (a)** shows the chemical composition of the stainless steel fabric before and after deposition. Both Si-H and Si-H_2 stretching can be found in the Raman spectroscopy study shown in **Figure 6-12**, providing evidence that amorphous silicon dangling bonds are passivated by hydrogen in the structure to reduce Staebler-Wronski degradation[37,48].

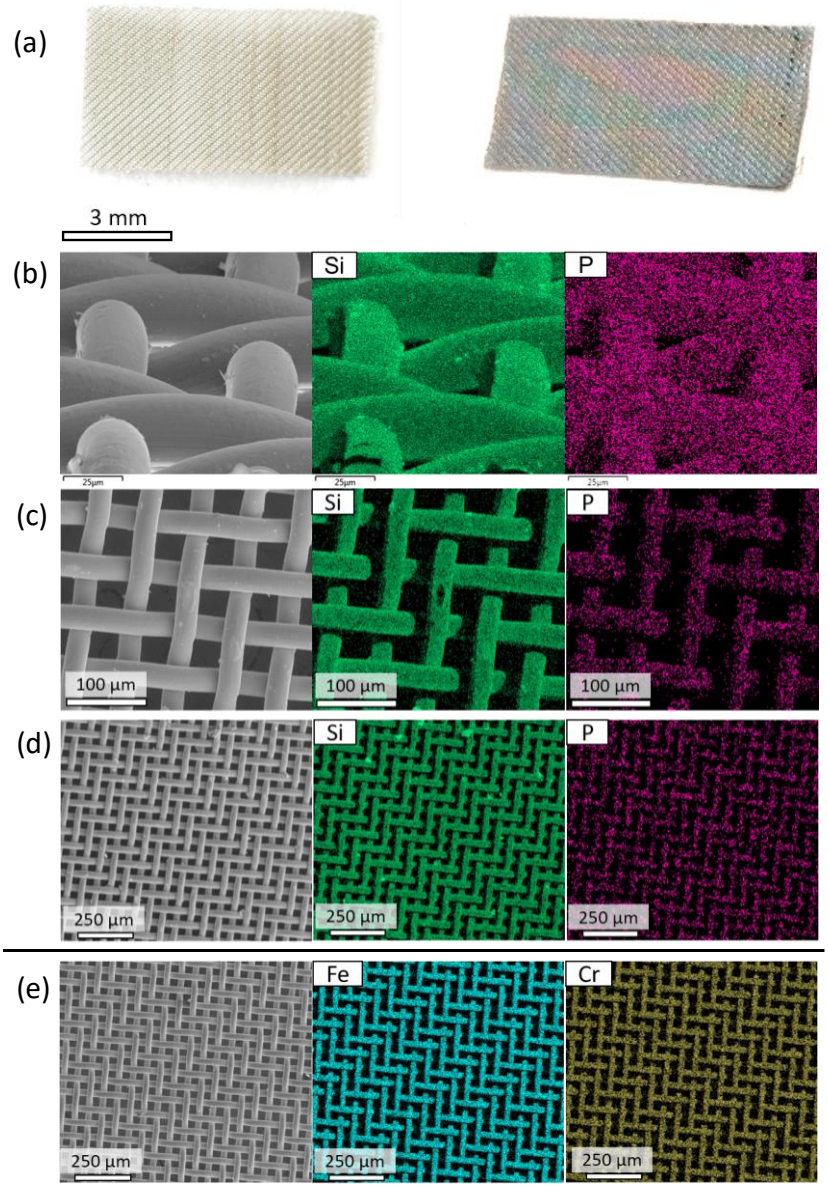

Figure 6-11. Picture and SEM image of n-Si coated stainless steel fabric. (a) Picture of stainless steel fabric before (left) and after (right) HPcCVD infiltration. The color variation is derived from silicon thin film interference. (b)-(d) SEM image and EDS mapping for the n-Si HPcCVD coated fabric shows the even distribution of Si and P on the wires' surfaces. (e) SEM and EDS mapping of the stainless steel mesh template. SEM credit: Xiaoyu Ji.

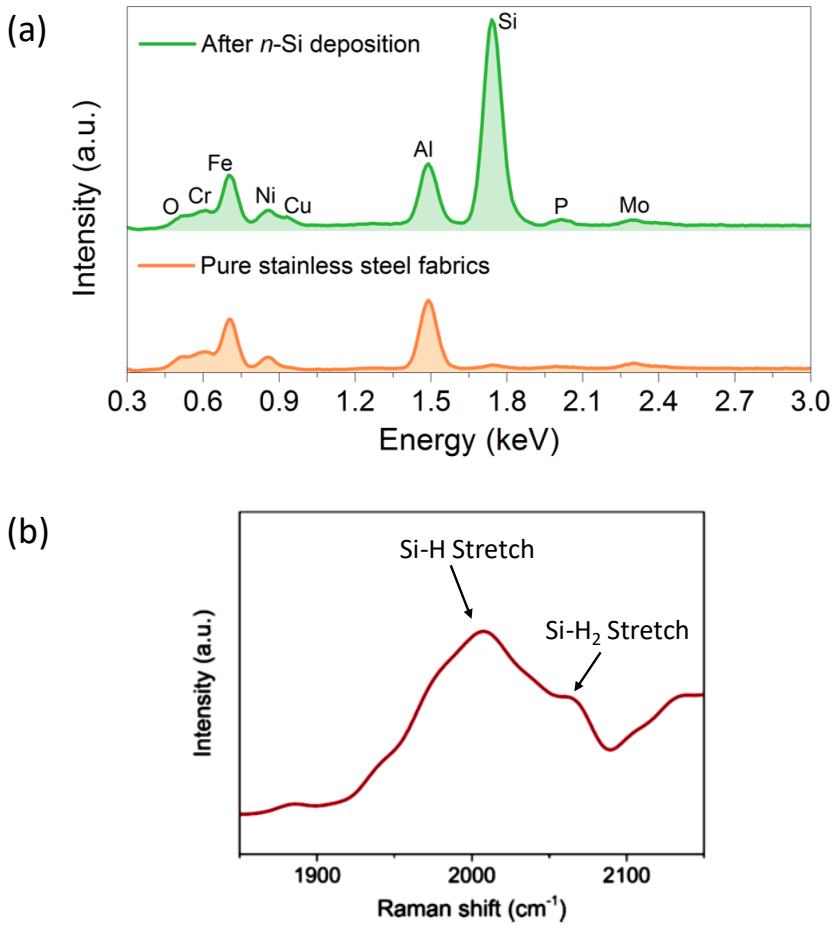

Figure 6-12. (a) Energy dispersive spectra showing elemental composition of the fabric before and after HPcCVD deposition. (b) Raman spectroscopy of the HPcCVD stainless steel fabric showing incorporation of hydrogen in the silicon. SEM EDS credit: Xiaoyu Ji.

The electrical and photovoltaic properties were examined. The dopant energy level was determined by measuring the dark electrical conductivity of a n^+-type a:Si:H film deposited on quartz substrate under the same HPcCVD reaction conditions. The n^+-type Si, doped with phosphorous deposited using HPcCVD, has a thermal activation energy E_a of 0.19 eV (**Figure 6-13**). To fabricate a photovoltaic cells using the HPcCVD fabric, Pt was sputtered onto the Si coated fabric as an electrode using a shadow mask with 0.5 mm diameter circles. Contact was made between the Pt dots on top of the n^+-type a-Si:H/ intrinsic a-Si:H and the parent stainless

steel fabric. The stainless steel fabric was recovered after HPcCVD by using chlorine reactive ion etching to remove the deposited Si. **Figure 6-13 (a)** shows the configuration of I-V measurements under illumination to assess the photovoltaic performance of the Schottky junction. Fill factor is often used to determine the efficiency of a solar cell by comparing the measured power and theoretical power in an open circuit and short circuit current. The solar fabric was found to have a fill factor (FF) of 0.395, a power conversion efficiency of 0.03 % and a specific power of 1.5 W kg^{-1}, with typical photodiode behavior measured using an open circuit voltage of 0.41 V and short circuit current density of 0.18 mA cm^{-2}.

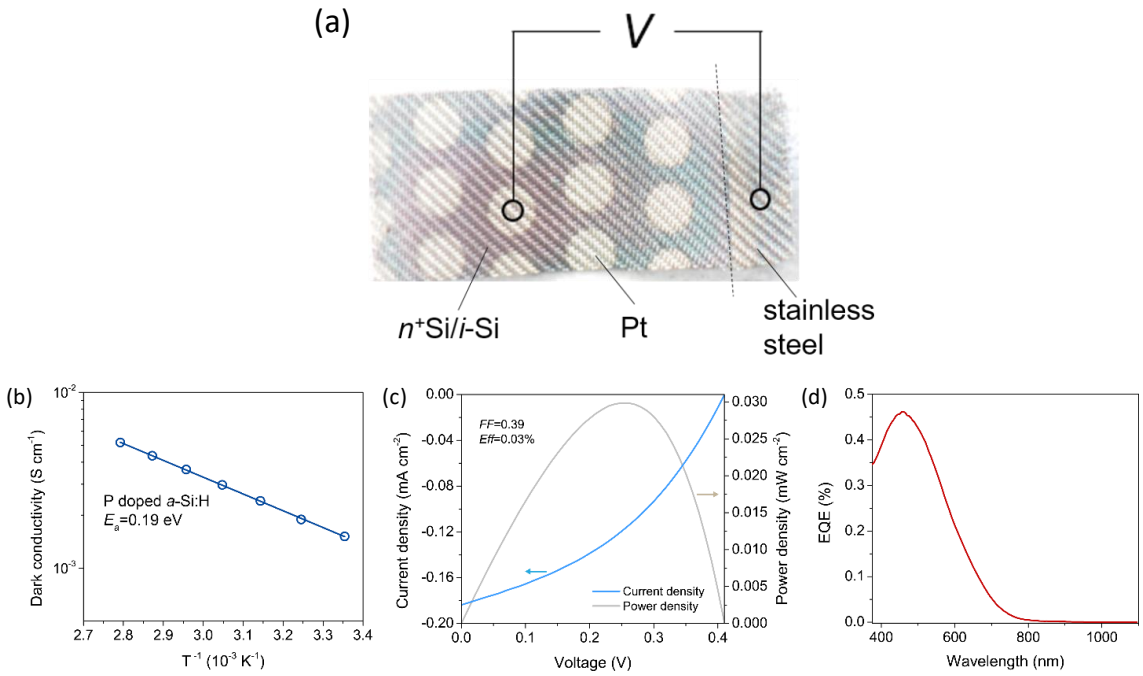

Figure 6-13. (a) Configuration of electrodes for the HPcCVD electronic fabric. (b) Arrhenius plot of van der Pauw measurement of the electronic fabric, with and activation energy of 0.19 eV extracted from slope. (c) Photodiode behavior of the a-Si:H thin film solar fabrics with Pt/i-Si/n^+-type Si junctions. (d) External quantum efficiency (EQE) measurement of the fabric showing spectral response of the fabric solar cell to lights.

The low fill factor could be due to low carrier diffusion length in a-Si:H (~0.1 μm) and the Pt contacts on the fabric. Since the contacts were sputtered onto the surface, it is possible that the Pt cannot conformally coat all of the surfaces on the wire, causing loss of current between probes. Series resistance could also arise from poor contact between n^+-type Si to the stainless steel fabric, which could be improved by increasing the dopant concentration and surface chemistry treatment prior to HPcCVD.

External quantum efficiency (EQE) was used to determine spectral response of the fabric solar cell to light (**Figure 6-13 (c)**). At around 730 nm, the EQE reaches its limit, which matches the intrinsic hydrogenated amorphous silicon mobility gap energy of 1.7 eV [49]. This correspondence suggest that electron-hole pairs are generated from light absorption in the intrinsic a-Si:H.

6.3. References

1. Sazio, P. J. A. *et al.* Microstructured Optical Fibers as High-Pressure Microfluidic Reactors. *Science (80-.).* **311,** 1583–1586 (2006).
2. Baril, N. F. *et al.* Confined high-pressure chemical deposition of hydrogenated amorphous silicon. *J. Am. Chem. Soc.* **134,** 19–22 (2012).
3. Baril, N. F. *et al.* High-Pressure Chemical Deposition for Void-Free Filling of Extreme Aspect Ratio Templates. *Adv. Mater.* **22,** 4605–4611 (2010).
4. He, R. *et al.* Silicon p-i-n junction fibers. *Adv. Mater.* **25,** 1461–1467 (2013).
5. Sparks, J. R. *et al.* Conformal Coating by High Pressure Chemical Deposition for Patterned Microwires of II-VI Semiconductors. *Adv. Funct. Mater.* **23,** 1647–1654 (2013).
6. Sparks, J. R., Sazio, P. J. A., Gopalan, V. & Badding, J. V. Templated Chemically

Deposited Semiconductor Optical Fiber Materials. *Annu. Rev. Mater. Res.* **43,** 9.1-9.31 (2013).

7. Chaudhuri, S., Sparks, J. R., Ji, X., Krishnamurthi, M. & Shen, L. Crystalline Silicon Optical Fibers with Low Optical Loss. *ACS Photonics* **3,** 378–384 (2016).
8. Ji, X. *et al.* Single-Crystal Germanium Core Optoelectronic Fibers. *Adv. Opt. Mater.* **5,** 1600592 (2017).
9. Sparks, J. R. *et al.* Zinc selenide optical fibers. *Adv. Mater.* **23,** 1647–1651 (2011).
10. He, R., Day, T. D., Sparks, J. R., Sullivan, N. F. & Badding, J. V. High Pressure Chemical Vapor Deposition of Hydrogenated Amorphous Silicon Films and Solar Cells. *Adv. Mater.* **28,** 5939–5942 (2016).
11. Reiche, M. & Gösele, U. in *Handbook of Wafer Bonding* 81–100 (John Wiley & Sons, Incorporated, 2011).
12. Niklaus, F., Enoksson, P., Kalvesten, E. & Stemme, G. Low-temperature full wafer adhesive bonding. *J. Micromechanics Microengineering* **11,** 100–107 (2001).
13. Wang, C. *et al.* Low-temperature wafer direct bonding of silicon and quartz glass by a two-step wet chemical surface cleaning. *Jpn. J. Appl. Phys.* **57,** 02BD02 (2018).
14. Moriceau, H. *et al.* Overview of recent direct wafer bonding advances and applications. *Adv. Nat. Sci. Nanosci. Nanotechnol.* **1,** 43004 (2010).
15. Hanneborg, A., Nese, M., Jakobsen, H. & Holm, R. Silicon-to-thin film anodic bonding. *J. Micromech. Microeng.* **2,** 117–121 (1992).
16. Wolffenbuttel, R. F. & Wise, K. D. Low-temperature silicon wafer-to-wafer bonding using gold at eutectic temperature. *Sensors Actuautors A* **43,** 223–229 (1994).
17. Knechtel, R. Glass frit bonding : an universal technology for wafer level encapsulation and packaging. *Microsyst. Technol.* **12,** 63–68 (2005).

18. Panousis, N. T. & Hall, P. M. Applications of Grain Boundary Diffsion Studies to Soldering and thermocompression bonding. *Thin Solid Films* **53,** 183–191 (1978).

19. Kibria, M. G., Zhang, F., Lee, T. H., Kim, M. J. & Howlader, M. M. R. Comprehensive investigation of sequential plasma activated Si / Si bonded interfaces for nano-integration on the wafer scale. *Nanotechnology* **21,** 134011 (2010).

20. Horiba Scientific. *Strain measurements of a Si cap layer deposited on a SiGe substrate determination of Ge content*.

21. Kadleikova, M., Breza, J. & Vesely, M. Raman spectra of synthetic sapphire. *Microelectron. J.* **32,** 955–958 (2001).

22. Street, B. R. A. Thin-Film Transistors. *Adv. Mater.* **21,** 2007–2022 (2009).

23. Wu, C., Whan, T., Guo, T. & Li, F. Nano Energy Wearable ultra-lightweight solar textiles based on transparent electronic fabrics. *Nano Energy* **32,** 367–373 (2017).

24. *Flexible Electronics : Materials and Applications*. (Springer Science+Business Media, LLC, 2009).

25. Sheraw, C. D. *et al.* Organic thin-film transistor-driven polymer-dispersed liquid crystal displays on flexible polymeric substrates Organic thin-film transistor-driven polymer-dispersed liquid crystal displays on flexible polymeric substrates. *Appl. Phys. Lett.* **80,** 1088–1090 (2002).

26. Jost, K., Dion, G. & Gogotsi, Y. Textile energy storage in perspective. *J. Mater. Chem. A* **2,** 10776–10787 (2014).

27. Lee, M. R. *et al.* Solar Power Wire Based on Organic Photovoltaic Materials. *Science (80-.).* **324,** 232–235 (2009).

28. Kim, J. *et al.* Noninvasive Alcohol Monitoring Using a Wearable Tattoo-Based Iontophoretic-Biosensing System. *ACS Sensors* **1,** 1011–1019 (2016).

29. Santiago, G. *et al.* Magnetosensitive e-skins with directional perception for augmented reality. *Sci. Adv.* **4,** 1–10 (2018).

30. Stuckelberger, M., Biron, R., Wyrsch, N., Haug, F. & Ballif, C. Review : Progress in solar cells from hydrogenated amorphous silicon. *Renew. Sustain. Energy Rev.* **76,** 1497–1523 (2017).

31. Lee, T. D. & Ebong, A. U. A review of thin fi lm solar cell technologies and challenges. *Renew. Sustain. Energy Rev.* **70,** 1286–1297 (2017).

32. Yun, M. J., Cha, S. I., Seo, S. H. & Lee, D. Y. Highly Flexible Dye-sensitized Solar Cells Produced by Sewing Textile Electrodes on Cloth. *Sci. Rep.* **4,** 1–6 (2014).

33. Maiolo, L. *et al.* Flexible pH sensors based on polysilicon thin film transistors and ZnO nanowalls. *Appl. Phys. Lett.* **105,** 93501 (2014).

34. Mannsfeld, S. C. B. *et al.* Highly sensitive flexible pressure sensors with microstructured rubber dielectric layers. *Nat. Mater.* **9,** 859–864 (2010).

35. Shulga, V. I. Comparative study of silicon and germanium sputtering by 1–20 keV Ar ions. *Nucl. Instruments Methods Phys. Res. B* **254,** 200–204 (2007).

36. George, S. M. Atomic Layer Deposition: An Overview. *Chem. Rev.* **110,** 111–131 (2010).

37. Street, R. A. *Hydrogenated Amorphous Silicon*. (Cambridge University Press, 1991).

38. Dahiya, J. B. & Rana, S. Thermal degradation and morphological studies on cotton cellulose modified with various arylphosphorodichloridites. *Polym. Int.* **53,** 995–1002 (2004).

39. Robin, E. *et al.* Quantification of dopants in nanomaterial by SEM/EDS. in *Euorpean Microscopy Congress* 380–381 (EMC 2016 Proceedings, 2016).

40. He, R. *et al.* Integration of gigahertz-bandwidth semiconductor devices inside microstructured optical fibres. *Nat. Photonics* **6,** 174–179 (2012).

41. Schubert, M. B. & Werner, J. H. Flexible solar cells into clothing. *Mater. Today* **9,** 42–50 (2006).

42. Cheng, N., Zhang, L., Kim, J. & Andrew, T. L. Vapor phase organic chemistry to deposit conjugated polymer films on arbitrary substrates †. *J. Mater. Chem. C* **5,** 5787–5796 (2017).

43. Allison, L., Hoxie, S. & Andrew, T. L. Towards seamlessly-integrated textile electronics : methods to coat fabrics and fibers with conducting polymers for electronic applications. *Chem. Commun.* **53,** 7182–7193 (2017).

44. Kovacik, P., Hierro, G., Livernois, W. & Gleason, K. K. Materials Horizons thin fi lms for next-generation electronics. *Mater. Horizons* **2,** 221–227 (2015).

45. Plentz, J. *et al.* Amorphous silicon thin-film solar cells on glass fiber textiles. *Mater. Sci. Eng. B* **204,** 34–37 (2016).

46. Chen, T., Qiu, L., Yang, Z. & Peng, H. Novel solar cells in a wire format Tao. *Chem. Soc. Rev.* **42,** 5031–5041 (2013).

47. Peng, M. & Zou, D. Flexible fiber/wire-shaped solar cells in progress: properties, materials, and designs. *J. Mater. Chem. A* **3,** 20435–20458 (2015).

48. Smets, A. H. M., Kessels, W. M. M. & van de Sanden, M. C. M. Vacancies and voids in hydrogenated amorphous silicon. *Appl. Phys. Lett.* **82,** 1547–1549 (2003).

49. Guha, S. *et al.* Band-gap profiling for improving the efficiency of amorphous silicon alloy solar cells. *Appl. Phys. Lett.* **54,** 2330–2332 (1989).

Chapter 7

Conclusion and Future Prospects

High pressure confined chemical vapor deposition (HPcCVD) is a versatile technique for creating unique and functional electronic materials such as three dimensional metalattices (*Chapter 3*, *4* and *5*), silicon glue (*Chapter 6*) and flexible solar cells (*Chapter 6*). The gas transfer apparatus used in HPcCVD systems provides a method to transfer electronic grade (99.999%) precursor gases without adding any impurities. The experimental set up and reactor design shown in this dissertation allows for infiltration and conformal coatings of many substrates and templates, including silica colloidal crystals, zeolite Y, mesoporous silica, metal-organic frameworks, planar substrates and flexibles cloths. In addition to the future works described at the end of each chapter, several other studies are of interest which could further advance the work shown in this dissertation.

The kinetics study of silane pyrolysis in HPcCVD was completed for both 1D and 2D geometries. Additional data points are needed to further confirm the 2D study (discussed in *Chapter 2*). We can further understand and validate the silane pyrolysis reaction mechanism at high pressure by probing unreacted precursors, intermediates and by-products in situ using the high pressure gas loading apparatus. A residual gas analyzer (RGA) is attached directly to the gas loading apparatus. HPcCVD of Si can be performed directly using the apparatus. Other reaction mechanisms, such as germane pyrolysis and ZnSe deposition using dimethyl zinc and dimethyl selenium could also be studied using the RGA.

The high pressure reaction mechanism and the infiltration process in 3D systems such as in silica colloidal crystals are not understood. Our preliminary studies suggests that HPcCVD fully filled metalattices are allowed by non-uniform deposition rate of Si or Ge in the interstitial

sites (**Figure 7-1**). High pressure gases enters into different features of silica colloidal crystal templates at varying velocity. Gas passes through meta-bond region faster than that of meta-atom regions due to the Venturi effect. This change in velocity along the path of gas transport can affect concentration of precursors at those regions, and thus affect deposition rate at those regions. Studies on silane pyrolysis in 3D nano-templates provide a guideline in developing HPcCVD infiltration of other materials, especially compound semiconductors which have complex reaction mechanisms and need careful precursor ratio control.

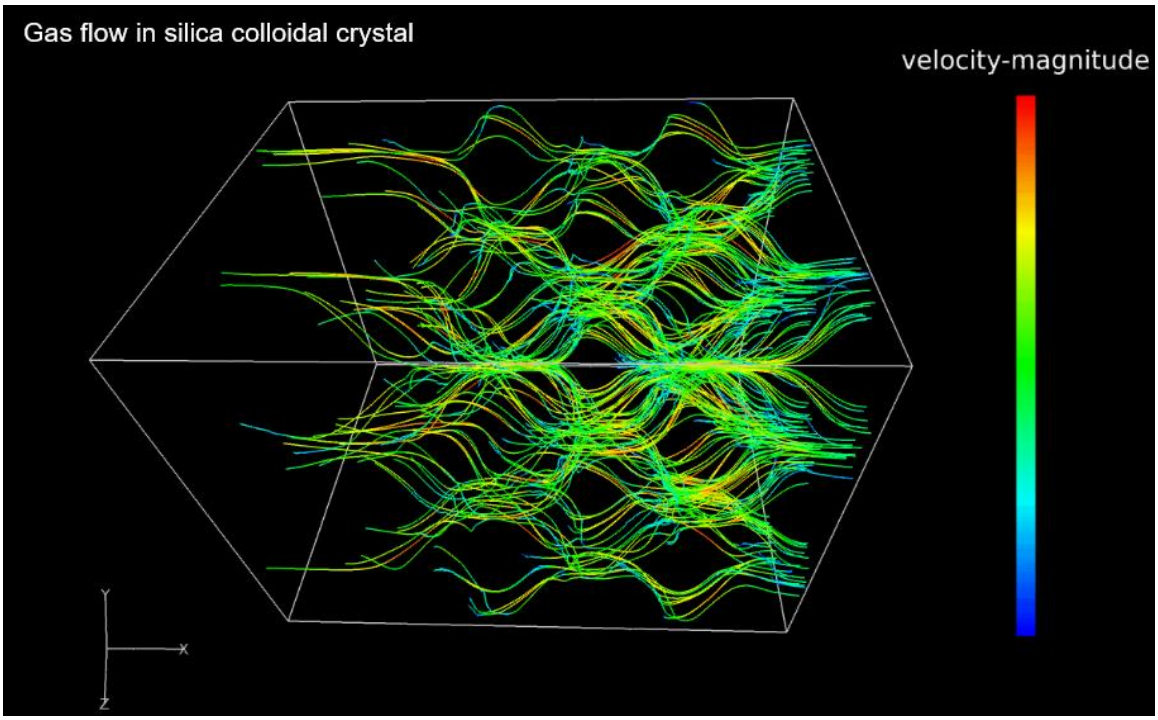

Figure 7-1. Gas flow in 30 nm silica colloidal crystal showing variation in velocity along the path of gas transport from right to left. Precursor gases travels slower at meta-bond regions as compared to meta-atom regions. Credit: Seyed Pouria Motevalian.

This dissertation has shown the powerful strategy by combining nano-templates and high pressure confined chemical vapor deposition to fabricate electronic metalattices. The tuning of metalattices' periodicity, sizes, symmetry, chemical composition, surface chemistry and interfacial design are shown in *Chapter 3, Chapter 4* and *Chapter 5*. The synthetic realization of

metalattices open up opportunities to study the relationship between nano-structural ordered and properties. As discussed in *Chapter 3*, the developed synthetic route can also create ordered porous silicon structure with varying porosity (**Figure 7-2**). A complete porosity characterization is needed to confirm the void volume. Porosity studies such as mercury porosimetry might be possible since these structures have an open network of pores. The increase of porosity is possible by other methods using silica colloidal crystal. For example, a higher temperature treatment of the template prior to infiltration can fuse together the silica nanoparticles to reduce the volume of the interstitial sites for semiconductor HPcCVD infiltration.

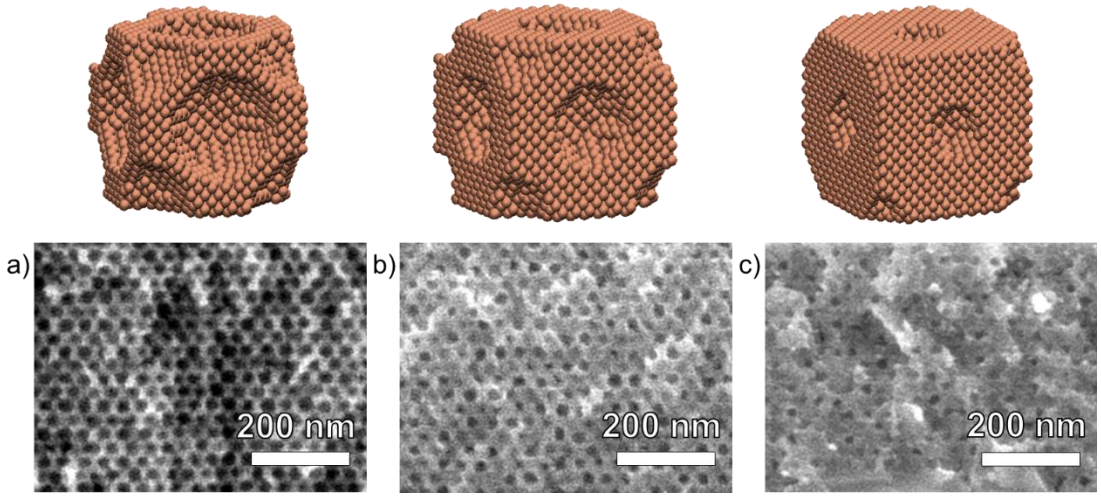

Figure 7-2. SEM of 30 nm Si metalattices with varying void volume (a)-(c). All of the above metalattices structure have a smaller void volume compared to their parent metalattices of 74% voids. From left to right are decreasing in void volume by increasing deposition time of the coatings after template removal.

For the high pressure CVD process, large area deposition on flexible substrate is possible but it is difficult on non-flexible substrates. Development of large HPCVD reaction chambers would allow for increased deposition rate and lowered energy cost for industrial use. Such development in industrial scale could also replace current methods for fabricating hydrogenated amorphous silicon.

In summary, this dissertation presents the usefulness of high pressure chemical vapor deposition in fabricating high quality semiconducting materials. 1D, 2D and 3D structures can be created using HPcCVD including optical fibers, thin films and metalattices. HPcCVD can deposit materials in nano-pores void free to make pervasive 3D interconnected structures. Intentional impurities can be added to the HPcCVD system easily for dopant inclusion to increase electrical conductivity of deposited materials. Electronic grade materials can be deposited in different templates and onto substrates using HPcCVD, with potential applications in solar cells, electronics, thermalelectrics, photonics and optoelectronics.

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SELECTED PUBLICATIONS

1. Ji, X., **Cheng, H. Y.**, Grede, A., Talreja, D., Molina, A., Mohney, S. Giebink, N., Badding, J., Gopalan, V., Conformal Coating of Amorphous Silicon and Germanium by High Pressure Chemical Vapor Deposition for Photovoltaic Fabrics, APL Mater., in review
2. Motvalian, S. P., Aro, S. C., **Cheng, H. Y.**, Day, T. D., van Duin, A. C. T., Badding, J. V., Borhan, A., Kinetics of Silane Decomposition in High-Pressure Confined Chemical Vapor Deposition of Hydrogenated Amorphous Silicon, ACS Ind. Eng. Chem. Res., 56, 14995-1500, 2017
3. Ji, X., Yu, S.-Y., Lei, S., **Cheng, H. Y.**, Chaudhuri, S., Liu, W., Mohney, S., Badding, J. V., Gopalan, V., Single Crystal Small Core Semiconductor Optical Fibers for All-Fiber Optoelectronics, OSA Tech. Dig. SM2K.5, 2017
4. Ji, X., Poilvert, N., Liu, W., Xiong, Y., **Cheng, H. Y.**, Badding, J. V., Dabo, I., Gopalan, V., A silicon microwire under a three-dimensional anisotropic tensile stress, Appl. Phys. Lett., 110, 091911, 2017
5. Ji, X., Lei, S. Yu, S.-Y., **Cheng, H. Y.**, Liu, W. Poilvert, N., Xiong, Y., Dabo, I., Mohney, S., Badding, J. V., Gopalan, V., Single-crystal silicon optical fiber by direct laser crystallization, ACS Photonics, 4 (1), 85-92, 2017
6. Healy, N., Mailis, S., Bulgakova, N. M., Sazio, P. J. A., Day, T. D., Sparks, J. R., **Cheng, H. Y.**, Badding, J. V., Peacock, A. C., Extreme electronic bandgap modification in laser-crystallized silicon optical fibres, Nature Materials, 13, 1122-1127, 2014
7. Shen, L., Healy, N., Xu, L., **Cheng, H. Y.**, Day, T. D., Price, J. H. V., Badding, J. V., Peacock, A. C., Four-wave mixing and octave-spanning supercontinuum generation in a small core hydrogenated amorphous silicon fiber pumped in the mid-infrared, Optics Lett., 39 (19), 5721-5724, 2014