PLASMA-ENHANCED ATOMIC LAYER DEPOSITION ZINC OXIDE FOR MULTIFUNCTIONAL THIN FILM ELECTRONICS

A Dissertation in
Materials Science and Engineering

by

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Submitted in Partial Fulfillment of the Requirements for the Degree of

Doctor of Philosophy

August 2010
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Abstract

A novel, weak oxidant, plasma-enhanced atomic layer deposition (PEALD) process has been used to fabricate stable, high mobility ZnO thin film transistors (TFTs) and fast circuits on glass and polyimide substrates at 200 °C. Weak oxidant PEALD provides a simple, fast deposition process which results in uniform, conformal coatings and highly crystalline, dense ZnO thin films. These films and resulting devices have been compared with those prepared by spatial atomic layer deposition (SALD) throughout the work.

Both PEALD and SALD ZnO TFTs have high field-effect mobility (>20 cm²/V·s) and devices with ALD Al₂O₃ passivation can have excellent bias stress stability. Temperature dependent measurements of PEALD ZnO TFTs revealed a mobility activation energy < 5 meV and can be described using a simple percolation model with a Gaussian distribution of near-conduction band barriers. Interestingly, both PEALD and SALD devices operate with mobility > 1 cm²/V·s even at temperatures < 10 K. The effects of high energy irradiation have also been investigated. Devices exposed to 1 MGy of gamma irradiation showed small threshold voltage shifts (<2 V) which were fully recoverable with short (1 min) low-temperature (200 °C) anneals.

ZnO TFTs exhibit a range of non-ideal behavior which has direct implications on how important parameters such as mobility and threshold voltage are quantified. For example, the accumulation-dependent mobility and contact effects can lead to
significant overestimations in mobility. It is also found that self-heating plays an important role in the non-ideal behavior of oxide TFTs on low thermal conductivity substrates. In particular, the output conductance and a high current device runaway breakdown effect can be directly ascribed to self-heating.

Additionally, a variety of simple ZnO circuits on glass and flexible substrates were demonstrated. A backside exposure process was used to form gate-self-aligned structures with reduced parasitic capacitance and circuits with propagation delay < 10 ns/stage. Finally, to combat some of the self-heating and design challenges associated with unipolar circuits, a simple 4-mask organic-inorganic hybrid CMOS process was demonstrated.
Table of Contents

LIST OF FIGURES .................................................................................................................................. vi
ACKNOWLEDGEMENTS ................................................................................................................ xvi
CHAPTER 1 ........................................................................................................................................... 1

CHAPTER 2 ......................................................................................................................................... 8
   2.1 PLASMA-ENHANCED CHEMICAL VAPOR DEPOSITION (PECVD) .................................................... 8
   2.2 SPATIAL ATOMIC LAYER DEPOSITION (SALD) .............................................................................. 10
   2.3 PLASMA-ENHANCED ATOMIC LAYER DEPOSITION (PEALD) ..................................................... 15
   2.4 PEALD SYSTEM DEVELOPMENT ................................................................................................. 21
   2.5 ZNO MATERIALS CHARACTERIZATION ...................................................................................... 29
   2.5.1 ZNO CRYSTALLINITY .............................................................................................................. 29
   2.5.2 ZNO OPTICAL PROPERTIES .................................................................................................. 35

CHAPTER 3 ........................................................................................................................................... 37
   3.1 BACKGROUND .............................................................................................................................. 37
   3.2 DIELECTRICS FOR TFTs .............................................................................................................. 41
   3.2.1 ALUMINA .................................................................................................................................. 42
   3.2.2 SILICON DIOXIDE ..................................................................................................................... 46
   3.3 SALD ZNO TFTs ........................................................................................................................... 47
   3.4 PEALD ZNO TFTs .......................................................................................................................... 54
   3.5 PASSIVATION OF ZNO TFTs .......................................................................................................... 62
   3.6 BIAS STRESS STABILITY OF ZNO TFTs ....................................................................................... 77
   3.7 TEMPERATURE DEPENDENCE OF ZNO TFTs ............................................................................... 82

CHAPTER 4 ......................................................................................................................................... 96
   4.1 NON-IDEAL CHARACTERISTICS ................................................................................................. 96
   4.2 OUTPUT CONDUCTANCE AND JOULE HEATING .......................................................................... 103
   4.3 CONTACTS .................................................................................................................................... 122
   4.3.1 CONTACT DOPING ...................................................................................................................... 123
   4.3.2 GATED CONTACT TFTs ............................................................................................................ 128
   4.3.3 INDEPENDENT CONTACT GATE TFTs .................................................................................... 135

CHAPTER 5 ......................................................................................................................................... 139
   5.1 BACKGROUND ............................................................................................................................. 139
   5.2 CIRCUIT DESIGN, LAYOUT, AND FABRICATION ........................................................................ 140
   5.3 PECVD ZNO TFT CIRCUITS ........................................................................................................ 145
   5.4 SALD ZNO TFT CIRCUITS .......................................................................................................... 147
   5.5 PEALD ZNO TFT CIRCUITS .......................................................................................................... 148
   5.6 GATE-Self-ALIGNED PEALD ZNO TFT CIRCUITS ...................................................................... 155
   5.7 FLEXIBLE PEALD ZNO TFTs AND CIRCUITS ........................................................................... 160
   5.8 RADIATION HARD ZNO DEVICES AND CIRCUITS ................................................................... 167
   5.9 HYBRID ORGANIC/ZNO CMOS CIRCUITS ................................................................................ 172

CHAPTER 6 ......................................................................................................................................... 180
   6.1 CONCLUSIONS ............................................................................................................................ 180
   6.2 FUTURE WORK ............................................................................................................................ 181

REFERENCES ...................................................................................................................................... 185

VITA
List of Figures

Figure 1 – ISI Web of Science publications results for “ZnO” over the last 40 years. .... 3

Figure 2 - SEM images of (left) 350 nm conducting B-doped ZnO films deposited by PECVD at 200 °C, (right) 100 nm undoped high resistivity ZnO by PECVD at 200 °C. The different microstructures are likely related to crystallinity differences and impurity incorporation arising from the very different deposition conditions. ........................................ 10

Figure 3 –(a) SALD lateral flow head design with alternating channels of metal organic, inert gas, and oxidant. (b) Typical film deposited using SALD. The center region receives 4 full ALD cycles every time the head moves from left-to-right and back. In comparison the edge only receives 1 ALD cycles during this motion. ...................... 13

Figure 4 – Schematics of different ALD processes as published by Levy et al.[39] (left) conventional ALD chamber and precursor pulse sequence. The pulse sequence below shows the overall sequence experienced by the substrate. (right) Spatial-ALD coating head with spatially defined gas regions in contact with the substrate. The pulse sequence below shows the series of gas exposures experienced by a point Q on the moving substrate, yielding a typical ALD sequence.[39] .................................................. 14

Figure 5 – Schematics of spatial ALD processes as published by Levy et al.[39] (left) A perspective view of a spatial ALD coating head showing the gas inlet and exhaust slots as well as a substrate floating on the head. The inset shows the desired gas isolation regions for two inert channels adjacent to a central reactive gas channel. (right) Side view of the spatial ALD coating head showing gas inlet slots (upward arrows) and gas exhaust slots (downward arrows) with a relatively large separation leading to low pressure fields and significant gas mixing and smaller separation leading to larger pressure fields and little gas mixing.[39] ............................................................................................... 15

Figure 6 - Diagram showing three cycles of chamber/sample exposure (left) conventional ALD with two reactants and inert purge between each, (right) weak oxidant PEALD process where metal-organic and weak reactant do not free react, allowing the weak reactant to act as both purge when the plasma is off and oxidant source when the plasma is on. ................................................................. 17

Figure 7 – (a) Growth of PEALD ZnO films with a short plasma time (0.2 s) as a function of number cycles for 6 different samples. The process is layer-by-layer and therefore the linearity with cycles is expected. (b) Comparison of saturation characteristics for the oxygen source. The growth rate is significantly higher for PEALD compared to conventional ALD, but saturates at somewhat longer times. The growth rate and saturation characteristics are also a strong function of the oxidant source and likely other parameters which influence the plasma (pressure, power, etc). ........................................................................ 21

Figure 8 – (Left) simple side-view schematic for the small PEALD system showing the gas flow pattern and location of vacuum sealing o-rings as well as RF electrode and
heater. (Middle) side view of small PEALD system with arrows showing the aluminum RF electrode and polycarbonate spacer. (Right) top down view of small PEALD system with the top off showing the input and output gas areas of the system as well as the heated pedestal.

Figure 9 – (Top) simple side-view schematic for the aluminum large PEALD system showing the location of all key elements (heaters, copper cooling loop, o-rings, polycarbonate spacer, stainless steel flanges, and alumina filled epoxy support) (Bottom left) LabView front panel for program designed to manual and automatically control both the large and small PEALD systems. (Bottom center) Photograph of large PEALD system mounted on its rack. (Bottom right) Photograph of large PEALD open with dotted line highlighting the outer edge of the heated area. Gas inlet (near) and outlet slots (far) are also labeled.

Figure 10 – Very simple single metal-organic PEALD system for new materials investigation. The plasma pressure is set manually by the needle valve and regulated by the weak reactant pressure. The diluted metal organic in the bubbler has a single pneumatic value downstream which is connected to the opposite switch valve and the soak valve for the system. By rapidly switching between the two positions on the switch valve the fixed diluted volume (hatched region) and turning on a plasma, the PEALD cycle is completed.

Figure 11 – X-Ray diffraction patterns for films grown from PECVD (boron-doped), spatial ALD, and PEALD on (100) silicon substrates [except for the 30 nm spatial ALD which came from grazing incidence XRD on glass/Mo/Al₂O₃]. Also included are thinner and thicker films from both spatial and PEALD showing the evolution of the different crystal structure where PEALD has strong (002) texture even in thin films (< 50 nm) while spatial ALD has (100) texture in thick films and is weakly ordered in thin films. A reduction in FWHM for the PEALD films as the film thickness is correlated to an increase in grain size which can be seen in SEM (Figure 14).

Figure 12 – Grazing incidence x-ray-diffraction (1°) measurement used to examine transistor stacks from SALD (ZnO/100nm Al₂O₃/100nm Mo/glass) on glass substrates and minimizing the influence of the amorphous glass substrate. As the film thickness becomes > 30 nm, the random oriented crystals become (100) textured. No clear diffraction is observed for the very thin films < 20 nm.

Figure 13 – Transmission electron microscope images taken by David Saint-John in Materials Science and Engineering: (left) bright-field image of typical Al₂O₃/ZnO (Al₂O₃ grown using CO₂, ZnO grown using N₂O) stack to be used in thin film transistors. Notably the Al₂O₃/ZnO interface appears to be very smooth and the ZnO has columnar grains which extend continuously from the interface to the top surface. (Right) dark-field image of the stack showing grain boundaries perpendicular to the interface. Also, diffraction is observed for single crystalline grains of ~ 10-15 nm.

Figure 14 – Scanning electron microscope images of typical PEALD ZnO films 70 nm thick (left) and 40 nm thick (right) deposited on Si at 200 °C. The average grain size for
the 70 nm layer (left) is ~ 30 nm and for the 40 nm layer (right) is ~15-20 nm. These grain sizes are consistent with the Scherrer formula calculation from the XRD. 

Figure 15 – Spectroscopic ellipsometry (left) for thick ZnO films deposited by PECVD, ALD, and PEALD. The high resistivity ZnO by PECVD is highly porous with low index of refraction. The spatial ALD and PEALD are both high. (Right) Plot of index of refraction for spatial ALD and PEALD films. PEALD films have high values even in very thin films, and nearly as high as epitaxial ZnO films grown on C-sapphire [55]....

Figure 16 – Schematics for passivated (a) bottom gate staggered-inverted structure for ZnO TFTs (b) top gate staggered structure.

Figure 17 – (a) Thickness as function of number of cycles for PEALD Al2O3 at 200 °C. (b) Capacitance voltage measurements for 22 nm PEALD Al2O3 (Si/Al2O3/Al, device area 100 x 220 μm). Two different MOS structures were stressed at 5V and -5 V (inset) for 12 hrs and then the shift in flat band voltage was measured.

Figure 18 – Leakagew current density as a function of applied field for typical PEALD (22 nm) and SALD (110 nm) Al2O3 in metal-insulator-metal structures. Both show very low leakage current densities below 6 MV/cm and typical breakdown values are between 6-8 MV/cm.

Figure 19 – (a) Arrhenius plot of temperature dependent leakage for 32 nm PEALD Al2O3 layer at 3.125 MV/cm (Glass/Cr/Al2O3/Ti), showing an exponential increase from 100 °C to 180 °C. (b) Current density at 3.125 MV/cm as a function of time for a temperature ramp from room temperature to 200 °C showing breakdown after short times at high temperature.

Figure 20 – Characteristics of typical transverse head SALD ZnO TFTs with device width (W) and length (L) W/L = 500/50 μm (ITO/100 nm Al2O3/25 nm ZnO:N/Al). (a) Square-root of I_D and log(I_D) versus V_GS for V_DS = 20V. The gate current I_G is also shown. (b) Linear I_D versus V_DS for various gate voltages.

Figure 21 – Characteristics of typical floating head SALD ZnO TFTs with W/L = 200/20 μm (Cr/50 nm Al2O3/25 nm ZnO/Ti). (a) log(I_D) and differential mobility versus V_GS for V_DS = 0.5V. (b) Linear I_D versus V_DS for various gate voltages.

Figure 22 – Typical device characteristics for unpassivated PEALD ZnO TFTs from the large ring-fed PECVD system (CO2 for ZnO) using (a) PECVD SiO2 (on silicon substrates) and (b) PEALD Al2O3 (on glass and patterned chrome gate) as the gate dielectric.

Figure 23 – Differential mobility as a function of channel charge (Q=COX(V_G-V_T)) for devices fabricated on PECVD SiO2 and PEALD Al2O3.

Figure 24 – Typical device characteristics for unpassivated ZnO TFTs (W/L = 200/20 μm, t_ox = 37 nm, e_r = 8) using N2O and CO2 as the oxidant source for the ZnO film deposition.
(a) log(I_D) versus VGS in the linear regime (V_DS = 0.5V) and extracted differential mobility.  (b) linear I_D versus V_DS for several values of VGS........................................... 59

Figure 25 – Forward and reverse sweeps for log(I_D) versus VGS in the linear regime (V_DS = 0.5V) and extracted differential mobility for a device with both Al2O3 and ZnO grown using N2O as the oxidant................................................................................................... 60

Figure 26 – Forward and reverse sweeps for log(I_D) versus VGS in the linear regime (V_DS = 0.5V) and extracted differential mobility for a device with both Al2O3 and ZnO grown using N2O as the oxidant................................................................................................... 61

Figure 27 – SALD ZnO TFTs with (a) shadow mask evaporated Al contacts and (b) Photolithographically and lift-off patterned evaporated Al contacts.  The influence of process chemicals results in volts of device hysteresis.................................................... 63

Figure 28 –(a) SALD ZnO devices (17 nm ZnO thickness) before passivation, after 50 nm of PECVD SiO2, and after 50 nm of PECVD Si3N4.  (b) PEALD ZnO devices (11.5 nm ZnO thickness) as fabricated and after ALD and PEALD passivation...................... 68

Figure 29 – Experimental data for devices with various PEALD-deposited ZnO thicknesses before passivation (a) and after passivation (b).  A weak thickness dependence on threshold voltage before and after passivation is observed but large changes in the subthreshold regime are seen after passivation as the ZnO thickness increases........................................................................................................................... 69

Figure 30 – (a) Experimental data compared from PEALD-deposited samples. SALD samples showed the same trend.  (b) Modeled Sentaurus data for devices both as-deposited and after passivation.  Devices were modeled with a background doping of 10^{17} /cm^3 in the ZnO films, and to simulate the effect of passivation an additional 2 nm channel on the back surface (“back channel doping”) was doped to 2x10^{19} /cm^3.  The effect of bulk doping was also examined and background doping was increased from 10^{17} /cm^3 (squares) to 10^{18} /cm^3 (triangles)............................................................................. 70

Figure 31 – Characteristics of undoped SALD ZnO TFTs as fabricated compared to devices which have been soaked in peroxide and then passivated with ALD Al2O3.  Devices with ZnO thicknesses < 30 nm show more positive threshold voltages and significant hysteresis, however, devices > 30 nm still have V_{ON} > 0 V and negligible hysteresis................................................................. 74

Figure 32 – Characteristics of SALD ZnO TFTs with NH3 bulk doping as a function ZnO thickness before and after ALD passivation.  The threshold voltage (V_T) and turn on voltage (V_{ON}) are only slightly changed after passivation and the hysteresis for the devices (right axis) becomes negligible.................................................. 75

Figure 33 – (a) log(I_D) - V_{GS} for V_{DS} = 0.5 (W/L = 200 μm/10 μm, t_{ox} = 32 nm, εr = 8) including forward and backward sweeps before and after 20,000 s, V_{GS} = 2 V, V_{DS} = 4 V, stress at 80 °C.  (insert) Zoom in to boxed region of (a) to show threshold voltage shift,
which is < 50 mV, (b) Normalized current as a function of time during the constant current stress at 80 °C showing 90% of $I_o$ after 50,000 s...

Figure 34 – Bias stress for SALD devices after passivation. (a) log($I_D$) - $V_{GS}$ for $V_D = 0.25$ (W/L = 400 μm/50 μm, $t_{ox} = 50$ nm, $\varepsilon_r = 8$) including forward and backward sweeps for NH$_3$ doped (33 nm) and undoped H$_2$O$_2$ treated (50 nm) devices after 30 nm ALD Al$_2$O$_3$ passivation. (b) Normalized drain current during the stress at room temperature (200 s with $V_G = 10$ V and $V_D$=0 V then sweep $V_G$ 10 to −5V with $V_D = 0.25$V and repeated). (c) Calculated $\Delta Q$ from change in current assuming only a lateral shift in $V_T$.

Figure 35 – Bias stress measurements on ZnO TFTs. (a) Change in channel charge ($\Delta Q$=$C_{ox}\Delta V_T$) during a 300s stress for PEALD TFTs as a function of gate electric field at three temperatures. (b) Comparison of the activation of bias stress for PEALD TFTs compared to SALD TFTs. The SALD devices have activation energy of ~ 880 meV compared to ~ 550 meV for PEALD.

Figure 36 – Bias stress for PMMA passivated PEALD devices on thermal SiO$_2$ (large PECVD system, CO$_2$ for ZnO). (a) log($I_D$) - $V_{GS}$ for $V_D = 20$ V (W/L = 220 μm/10 μm, $t_{ox} = 45$ nm, $\varepsilon_r = 3.9$) including forward and backward sweeps before and after the stress. (b) Normalized drain current during the stress at room temperature (24 hr with $V_G$ = $V_D$= 15 V).

Figure 37 – (a) log($I_D$) and $I_D$ versus $V_G$ for PEALD devices on 45 nm thermal SiO$_2$ at temperatures from 80 to 360 K (40K steps). (b) log($I_D$) and differential mobility versus $V_G$ over the same temperature range corrected for the shift in threshold voltage.

Figure 38 – (a) Arrhenius plot for two different channel length PEALD ZnO devices on thermally oxidized silicon (CO$_2$ for ZnO) at temperatures greater than ~100K the activation energy is ~ 15 meV. (b) Threshold voltage as a function of temperature which is nearly linear down to 77K with a charge coefficient of ~0.75 nC/cm$^2$K.

Figure 39 – (a) log($I_D$) and $I_D$ versus $V_G$ for PEALD ZnO devices (Al$_2$O$_3$ dielectric, N$_2$O for ZnO) at various temperatures from room temperature to 10K. (b) $I_D$ and differential mobility as a function of gate voltage corrected for the threshold voltage shift over this temperature range.

Figure 40 – (a) log($I_D$) and $I_D$ versus $V_G$ for floating head SALD devices at various temperatures from room temperature to 10K. (b) Differential mobility as a function of gate voltage over this temperature range.

Figure 41 – (a) Subthreshold slope and (b) charge ($\Delta Q$=$C_{ox}\Delta V_T$) as a function of temperature for SALD and PEALD ZnO TFTs down to 10K. The change in threshold voltage is calculated two ways from a straight line fit to $g_m$ and where $I_D = 10^{-9}$ A.

Figure 42 – Temperature dependent transmission line measurements to extract sheet resistance ($\rho_s$) and contact resistance ($R_C$) as a function of temperature.
Figure 43 – (a) Mobility temperature activation comparison of several different thin film transistor materials (*Chen et al. [83]). (b) Table summarizing the room temperature mobility, mobility activation energy, and change in charge with temperature for various materials discussed in this section. 90

Figure 44 – Differential mobility at a variety of constant $V_G - V_T$ for (a) PEALD device shown in Figure 39 and (b) SALD device shown in Figure 40. The dotted lines in the high temperature range are the modeled fit. The activation energy for both PEALD and SALD approaches ~ 0 eV as the temperature decreases below 50 K 92

Figure 45 – (a) Barrier height extraction from PEALD and SALD devices. The error bars represent standard deviations in the Gaussian distribution. The calculated Fermi level as a function of doping assuming a 5 nm uniformly doped channel is also marked. The 5 nm channel accumulation is an approximation to roughly estimate the carrier concentration in the channel to compare to IGZO Hall measurements. (b) Comparison between the temperature independent mobility parameter from the barrier extraction and differential mobility. 95

Figure 46 – (a) Extracted differential mobility and sheet concentration for a typical SALD TFT. The mobility is a strong function of gate voltage. (b) Gated Hall-effect measurements for SALD ZnO TFTs. The measured sheet concentration increases linearly with gate voltage as expected. The Hall-effect mobility is nearly linearly dependent on gate voltage. 97

Figure 47 – Typical passivated PEALD device measured in the linear regime. The straight-line fit is used to calculate field-effect mobility and threshold voltage for the device. 99

Figure 48 – (a) Comparison of experimental data with calculated currents assuming constant -3V threshold voltage and either constant mobility of 22 cm$^2$/Vs (long dash) or calculated differential mobility (short dash). Both overestimate the current by nearly a factor of two. (b) Differential mobility typically extracted (in Chp 3 and literature) compared to constant mobility from straightline fit (22 cm$^2$/Vs, long dash), and calculated mobility from measured drain voltage assuming constant threshold voltage of -3 V (short dash). 100

Figure 49 – (a) Typical PEALD ZnO TFT with vertical line indicating the extracted threshold voltage from the $H(V_G)$ function. (b) $H(V_G)$ as calculated from the integral of the drain current over the drain current. A straightline fit determines the threshold voltage and power, “m” which is > 3 instead of the ideal 2. 103

Figure 50 – Sentarus simulated short channel effects. The model used a dielectric thickness of 32 nm and a dielectric constant of 8. Doped contact regions were used to ensure contact effects did not contribute to the model. DIBL is observed for channel lengths much less than 1 micron. 104

Figure 51 – (a) Typical output characteristics for devices used in this work with 5 and 10 micron channel length (200 micron wide). (b) output conductance ($dI_D/dV_D$) plotted as a
function of current density for a variety of channel lengths. The output conductance is correlated with input power and is very weakly a function of channel length, indicating that thermal and not short channel effects are dominant. ............................................... 106

Figure 52 - Drain current for devices running in saturation as a function of gate voltage pulse width. It is found that the thermal time constant for heating is > 100 μs. In addition, for the devices measured, steady state Joule heating occurs >50 ms. ............. 108

Figure 53 - (a) linear $I_D$ vs $V_{DS}$ output characteristics for several values of $V_{GS}$ for a typical PEALD ZnO TFT on glass [W/L = 200/5 μm, $t_{ox}$ = 32 nm, $\varepsilon_r$ = 8] compared using a DC sweep versus a pulsed gate measurement (10 μs pulse 1.5% duty cycle). (b) log ($I_D$) vs $V_{GS}$ for both linear ($V_{DS} = 0.5$ V) and saturation regimes ($V_{DS} = 8$V) comparing DC sweep and pulsed measurements for the same device. Also the square root of ID is shown for saturation sweep showing similar threshold voltage but a difference in mobility..................................................................................................... 108

Figure 54 - (a) Arrhenius plot of mobility for mobility versus temperature. Over the range of 30 to 130 °C the devices show a small activation energy of ~ 5 meV. (b) Threshold voltage as a function of temperature from 30 to 130 °C. A linear shift is observed with coefficient of ~1.7 nC/cm²K. ..................................................................................................... 110

Figure 55 - Calculated change in temperature as based on the current difference between the pulsed and DC sweep shown in Figure 2. The change in temperature is found to be linear with output power as expected with Joule-heating with thermal resistance of ~7000 W/K........................................................................................................................... 111

Figure 56 - (a) Table 1 of output power where thermal runaway results in breakdown (device gate and either source or drain is shorted together and dark bubbles observed on device) on various substrates (device width = 200 μm) [*the thermal conductivities were evaluated using COMSOL multiphysics to roughly account for insulating layers and changes in thermal conductivity over the temperature range from 20-300 °C] (b) Graph of power to breakdown as a function of substrate thermal conductivity. A linear relationship implies that the temperature at breakdown is similar on the different substrates........................................................................................................................ 115

Figure 57 - (a) Experimentally measured output conductance for PEALD TFTs (W=200 μm) comparing standard chrome gate and 150 nm Ti contacts with thick 250 nm thermally conducting Al contacts and chrome gold gates. Improved thermal conductivity of the gate and source drain each show ~30-40% improvement in output conductance for a given power. (b) Experimentally measured output conductance as a function of device width. Narrow devices show 2-3 times lower output conductance for comparable powers. ......................................................................................................................................... 117

Figure 58 - Output conductance ($dI_D/dV_D$) for a variety of oxide TFTs (*[16,38], **[67,90], ***[95]) on glass and silicon substrates (Si/100 nm SiO₂) as a function of device power. The data is fit using a second order polynomial which is roughly expected for self-heating in the saturation regime. ........................................................................ 119
Figure 59 – Comparison of Al-SALD ZnO contacts and ZnO:B (PECVD)-SALD ZnO. (a) Al source drain contacts with oxygen plasma have specific contact resistivity $10^{-5}$ $\Omega cm^2$. (b) Doped ZnO contacts have specific contact resistivity $>10^{-4}$ $W/cm^2$ and lower field effect mobility. ................................................................. 124

Figure 60 - Process flow for argon ion beam etched contacts. A double layer resist pattern is used to etch only the contact regions of the device. Then metal is evaporated/sputtered and lifted off. Finally the devices are electrically isolated by patterning the ZnO layer. ...................................................................................................................................... 126

Figure 61 - SALD device results for contact etching with Ar-ion beam. (a) log $(I_D)$ and sqrt $(I_D)$ versus $V_G$ for transverse head SALD device with $W/L = 200/5 \mu m$. The contact resistance is decreased by 2 orders of magnitude and the mobility is increased from 8 to 15 cm$^2$/V·s. (b) Specific contact resistivity as a function of time in air and on a hot plate at 160 and 200 °C. The difference between etched and non-etched contacts is relatively well maintained over time and annealing. ........................................................................................................ 128

Figure 62 - log $(I_D)$ and differential mobility versus gate voltage for H$_2$ plasma treated ZnO TFTs on 45 nm thermal oxide. .............................................................................................................. 131

Figure 63 - Sentaurus simulation of high mobility ZnO gated diode TFT. A constant carrier mobility of 30 cm$^2$/V·s was set in the ZnO layer for the simulation and a Schottky barrier height of 0.6 eV was used. (a) The ZnO layer is 10 nm thick and lightly doped (5x$10^{14}$/cm$^3$) while the back interface is heavily doped (10$^{20}$/cm$^3$) to simulate the passivation process. (b) log $(I_D)$ and differential mobility from the simulation for linear and saturation regime. The differential mobility is extracted for $V_{DS} = 0.5V$. (c) Linear $I_D$ versus $V_{DS}$ for several gate voltages showing considerable non-ideality. ..................................................................................................................... 133

Figure 64 - (a) log $(I_D)$ and differential mobility versus gate voltage in the linear and saturation regime for 10 nm ZnO layer passivated with N$_2$O based Al$_2$O$_3$ resulting in gated-diode ZnO TFTs. (b) linear $I_D$ versus $V_{DS}$ for the same TFT in (a). The significant output conductance in these devices is not from self-heating but rather from the gated contact........................................................................................................................................ 135

Figure 65 - (a) Schematic of double gated structure. (b) Cross-section of fabricated double gated structure. Glass and a blanket layer of chrome act as the channel gate. Pd is used as the contact gate. ........................................................................................................................................ 136

Figure 66 - (a) Results for double-gated structure with ($t_{ox\ channel} = 64$ nm, $t_{ox\ contact} = 32$ nm). The contact electric field is varied from 0 MV/cm to 3.75 MV/cm and changes in the measured device field-effect mobility are observed as expected. (b) Comparison of contact gated and contact electric field the same as the channel electric field. The subthreshold region of the device is markedly different for contact and channel at the same electric field. ..................................................................................................................................... 137

Figure 67 – AIMSpice fit to typical passivated ZnO TFTs. ......................................................................................... 142
Figure 68 – AIMSpice simulations for various parameters in 7-stage ring oscillator design. All simulations are based on extraction for SALD ZnO TFT with 100 nm Al₂O₃ dielectric. A 3 pF output capacitance and 10¹⁵ Ω output resistor in series model the effect of probing the actual device. (upper left) Frequency for various beta ratios with mobility 10 cm²/V·s, 5 micron channel length, and 2 μm overlap. (upper right) Frequency for various channel lengths with mobility 10, 2 μm overlap and beta ratio 5. (lower left) Frequency for varied device mobility with channel length 5 μm, beta ratio 5, and overlap 2 micron. (lower right) Frequency for various device overlaps with channel length 5 μm, beta ratio 5, and mobility 10 cm²/V·s. ............................ 144

Figure 69 – Mask layout for ZnO ring oscillators. (a) Original design with box and zoom in to a unit inverter. (b) Compact design to minimize thermal effects with box and zoom to unit inverter................................................................. 145

Figure 70 – PECVD ZnO TFT with low-leakage Al₂O₃ dielectric (left) log (I_D) versus V_GS and √I_D versus V_GS characteristics for V_DS = 40 V, and (right) ZnO TFT I_D versus V_DS characteristics for several values of V_GS (W/L = 100 μm/10 μm, t_oX = 150 nm). ............ 146

Figure 71 – PECVD ZnO ring oscillator with low-leakage Al₂O₃ dielectric (left) optical micrograph of 7-stage ring oscillator (right) Frequency and propagation delay for PECVD circuits which appear to be dominated by slow interface states............. 147

Figure 72 – (left) Output waveform of seven-stage ring oscillator (L_drive = 4 μm, W_drive = 100 μm, L_load = 4 μm, W_load = 20 μm, beta ratio = 5, 1.5 μm source/gate and drain/gate overlap), operating at 2.3 MHz, and (right) oscillation frequency and propagation delay as a function of V_DD (t_oX = 110 nm) for both experiment and AIMSPICE simulation. .. 148

Figure 73 – (a) Schematic and optical micrograph of unit saturated load inverter from PEALD ZnO TFTs. (b) Output characteristics for inverter with beta ratio of 5 for various supply voltages (2, 4, 6, 8V). .......................................................... 150

Figure 74 – (a) Schematic of unit depletion load inverter. (b) Output characteristics for depletion mode inverter formed with PEALD ZnO TFTs for various supply voltages (1 to 8V, 1 V/step). .................................................................................. 152

Figure 75 – (a) AIMSpice model with threshold voltage adjusted by changing V_TO and V_FB. The supply current for the depletion lead given a W/L = 10 is shown and corresponding ring oscillator propagation delay. The propagation delay is a weak function of V_DD for depletion load inverters but a strong function of load supply current. ................................................................. 152

Figure 76 – (left) optical micrograph of 15-stage PEALD ZnO TFT ring oscillator, (middle) schematic of inverter chain plus output stage, (right) frequency and propagation delay as a function of supply voltage (t_oX = 32 nm) for ring oscillator with 2.5 μm channel length and 1.5 μm gate to source/drain overlaps. .......................................................... 153
Figure 77 – (left) Frequency, propagation delay, and supply power for 7-stage ring oscillator with beta ratio = 5, channel length = 3 μm, and 1 μm source/gate and drain/gate overlap. (right) Run to run uniformity for passivated PEALD circuits on three different samples. RO1 had beta ratio = 5, channel length = 5 μm, and 4 μm source/gate and drain/gate overlap. RO2 had beta ratio = 5, channel length = 3 μm, and 2 μm source/gate and drain/gate overlap.

Figure 78 – (left) Schematic of staggered bottom-gate ZnO TFTs with parasitic capacitances indicated as well as overlap distance (ΔL). AIMSpice simulated propagation delay for a 7-stage ZnO ring oscillator based on typical PEALD ZnO TFTs. The overlap capacitance between the gate and source-drain regions is varied in the model to represent a varying overlap distance in real devices. The propagation delay drops below 10 ns/stage as the overlap distance is reduced to < 0.5 μm.

Figure 79 – (a)-(d) Backside exposure process used to fabricate gate-self-aligned TFTs. (a) Patterned films of Cr, Al2O3, and ZnO have a double layer resist (PMMA/1811) spin coated and then exposed from the backside, (b) Both resist layers patterned exposing ZnO for self-aligned contacts, (c) Ti layer patterned by lift-off and single layer resist coated for source-drain isolation, (d) Ti isolated by dry etching in CF4/O2 plasma. (e) Optical micrograph of self-aligned-gate ZnO TFT with dotted box indicating zoom region (f). The S/D to gate overlap shown in this example TFT is < 0.5 μm.

Figure 80 – (left) log(ID) versus VGS for VDS = 0.5 V and VDS = 12 V (W/L = 205 μm/12 μm, tOX = 32 nm), (right) ID versus VDS characteristics for several values of VGS for the same device.

Figure 81 – Gated transmission line measurement for gate-self-aligned PEALD ZnO TFTs.

Figure 82 – (a) Optical micrograph of 7-stage, 2.8 μm channel length ring oscillator and load and drive TFTs with source-drain to gate overlap ~0.3 μm. (b) Frequency and propagation delay as a function of supply voltage reaching minimum propagation delay < 10 ns/stage.

Figure 83 – Dielectric integrity test for 50 nm PEALD Al2O3 on polyimide substrates. (a) AFM image for polyimide Kapton TabE used in this work. (b) Optical micrograph of 8,000 crossover test structure and zoomed region to show gate lines (horizontal) and top metal (vertical line). (c) Current density as a function of electric field for two good 8,000 crossovers. The current density is < 10^-7 A/cm^2 at 6 MV/cm. (d) Current density map at 3 MV/cm for an array of 28, 8000 crossover tests. The yield criteria was < 10^-7 A/cm^2 at 3 MV/cm.

Figure 84 – Typical characteristics for passivated PEALD ZnO TFTs on flexible polyimide substrates. (a) log(ID) versus VGS and differential mobility versus VGS characteristics for VDS = 0.5 V (b) ID versus VDS characteristics for several values of VGS for the same device (W/L = 50 μm/20 μm, tox = 50 nm).
Figure 85 – (a) Optical micrograph and schematic of 15 stage ZnO ring oscillator plus output buffer stage. (b) Frequency and propagation delay for PEALD ZnO TFT ring oscillator on polyimide ($W_{\text{drive}} = 100 \, \mu m$, $W_{\text{load}} = 20 \, \mu m$, beta ratio = 5, $CL = 1 \, \mu m$, overlap = 2.5 $\mu m$). ................................................................. 167

Figure 86 – Images of fluoroware containers and PEALD devices on glass ranging from no exposure (left) to 1 MGy exposure (right). The samples and boxes turn yellow as color centers form from the radiation. .................................................................................. 169

Figure 87 – (a) $\log I_D$ vs $V_G$ for as fabricated and irradiation doses of 10, 200, and 1000 kGy. A negative threshold voltage is observed during irradiation and indicated by arrow. The 200 kGy device was also annealed in air at 200 °C for 1 min and the curve is marked but overlays nearly exactly with as fabricated. (b) Plot of the threshold voltage and mobility as a function of irradiation dose and best fit line to 0, 10, 200, and 1000 kGy points with standard deviations. (c) Turn on voltage $V_{ON}$ as a function of irradiation dose. The increases in $V_{ON}$ are larger than $V_T$ which indicates the subthreshold slope is slightly increasing during irradiation .............................................................................. 171

Figure 88 – Ring oscillator performance after exposure to gamma radiation of 10 kGy and 200 kGy. The speed for the two different samples is similar (RO1 and RO2) and a significant increase in speed and the minimum operation voltage is observed with radiation. This is expected given the negative threshold voltage shift observed. ......... 172

Figure 89 – (top) Schematic cross-section of organic/ZnO CMOS inverter (top). Optical micrograph of CMOS inverter (bottom left) and enlarged image of diF TES-ADT microstructure on the untreated oxide area (top right) and PFBT-treated gold electrode (bottom right). ........................................................................................................ 176

Figure 90 – Drain current as a function of drain voltage for several gate voltages for discrete p-channel (left) and n-channel (right) devices. The p-channel device has a field-effect mobility of ~0.1 cm$^2$/V·s and the n-channel device has a field effect mobility of ~12 cm$^2$/V·s .......................................................................................................................... 177

Figure 91 – Output voltage and supply current for a unit CMOS inverter with a beta ratio of 10 (left). Experimentally measured propagation delay as a function of channel length for 7-stage CMOS ring oscillators with AIMSpice simulated propagation delay in the dotted line (right). ........................................................................................................... 179

Figure 92 – (a) Layout for 8x8 array for temperature sensing ZnO TFTs on flexible substrates. (b) Initial results for ZnO TFTs on PZT:PNN (500 nm, $\varepsilon_r > 1000$) and Al2O3 buffer layer (5 nm, $\varepsilon_r = 8$). The subthreshold slope is ~100 mV/dec and mobility of 10-20 cm$^2$/V·s is achieved at low voltage. ........................................................................ 183
**Acknowledgements**

I would like to express my deepest gratitude for the guidance and support of my thesis advisor, Dr. Thomas Jackson. I would also like to thank my thesis committee members: Dr. Susan Trolier-McKinstry, Dr. Joan Redwing, and Dr. Jerzy Ruzzylo for the care and time to review and guide this doctoral thesis.

This work has been made possible by a large group of collaborators, colleagues, and friends. First, I would like to thank all of the members of the research group at Penn State (JERG), particularly Dr. Jie Sun, Dalong Zhao, and Dr. Sungkyu Park for mentoring and helping me throughout the process. Second, I would like to thank the ZnO team from Eastman Kodak Company including Dr. David Levy, Dr. Mitchell Burberry, Dr. Lee Tutt, and particularly Dr. Shelby Nelson for an exciting and fruitful collaboration. Third, I would like to thank all individuals from Penn State, National Institute for Standards and Technology, Konica Minolta, Air Products, and the University of Kentucky, for help and support of this work.

Finally, I would like to thank my parents Deborah Mourey and Thomas Mourey as well as my significant other Zoe Downing for love, support, and understanding throughout.
Chapter 1

Introduction and Background

The field of large-area thin film electronics requires materials which are low-cost and widely available. Some technologies, such as single crystalline Si, can afford to use expensive processes and high-cost materials, because they have very high value per unit area. However, in large-area electronics it is often more cost efficient to use low temperature processes which may provide a path to lightweight, inexpensive, flexible substrates. There are a variety of new materials being developed, all with different advantages and disadvantages, to provide a pathway to new large-area technologies. One major class of these materials is organic semiconductors, which focus on low-cost materials and processing. While there have been considerable developments in organic semiconducting materials and devices, the relatively low performance and poor stability combined with a sensitive fabrication process makes these materials less appealing for many potential applications.

A second class of materials technology which has emerged with tremendous interest from the large-area display field is oxide-based electronics. The current technology infrastructure in large-area display backplanes is plasma enhanced chemical vapor deposition (PECVD) of silicon nitride and amorphous silicon. While amorphous silicon is a mature technology and is widely used in a variety of thin film applications, the material is limited by low field-effect mobility (~1 cm²/Vs). The low field-effect mobility is the result of a large exponential tail state density near the conduction band. Beside poor carrier mobility, other materials limitations of a-Si:H have been well
documented and include poor photo and electrical stability.[1, 2] In a-Si:H TFTs, the stability can be improved by depositing the gate insulator and semiconducting layer at higher temperatures (>300 °C). However, these high temperatures make the process incompatible with many low cost substrates.[3] Oxide electronics could potentially be a low-temperature, high-performance, and high stability alternative to amorphous silicon in many novel thin film electronic applications.

Zinc oxide is one of the most widely studied oxide semiconductor materials. It is a low cost material which has garnered interest for a range of applications largely due to its large direct band gap (3.4 eV) and single crystals have high room temperature electron mobility (205 cm²/Vs).[4, 5] Zinc oxide has a hexagonal wurtzite structure with lattice parameters \( a = 0.3296 \text{ nm} \) and \( c = 0.52065 \text{ nm} \).[6, 7] The structure of ZnO can be simply described as a number of alternating planes composed of tetrahedrally coordinated \( \text{O}^{2-} \) and \( \text{Zn}^{2+} \) ions, stacked alternately along the \( c \)-axis.[6] The crystal structure in ZnO results in non centrosymmetric and consequently the materials is piezoelectric and pyroelectric. [6] The defect chemistry is a critical component in ZnO films and crystals and persistent intrinsic defects such as oxygen vacancies, zinc interstitials, and hydrogen act as donors and cause n-type conductivity (although it somewhat disputed which defect causes room temperature conduction).[8]

In addition, ZnO is a highly ionic semiconductor and the conduction band is made up nearly entirely of states from the \( \text{Zn}^{2+} \) cation, and the valence band nearly entirely of the \( \text{O}^{2-} \) anions.[9] This has tremendous implications on the role of disorder in oxide
semiconductors. Because the electron transport is governed only by the position of the cations, and these atoms have large spherical 4s orbitals, the transport is highly insensitive to order.[9, 10] This allows imperfect, low-temperature, deposited films to still maintain excellent transport. The combination of these properties has prompted broad interest from a variety of applications including transparent conductors, varistors, piezoelectric transducers, UV LEDs, and UV detectors.[4, 8, 11-13] As a result of the broad application interest, it is unsurprising that a simple ISI Web of Science search for ZnO resulted in more than 4,500 papers in 2009 (see Figure 1). In addition, there has been sustained growth since the early nineties with an exponential growth over the last ten years.

**Figure 1** – ISI Web of Science publications results for “ZnO” over the last 40 years.

Recently, ZnO has attracted considerable attention for possible application in thin film transistors (TFTs) due to the high electron mobility of ZnO as well as its insensitivity to
disorder. The high mobility results in high drive currents and faster device operating speeds, which may extend the range of accessible applications. However, most reports of field-effect devices from epitaxial thin films show field-effect mobility that is considerably lower (<50 cm²/V·s) than the single crystal Hall-effect mobility.[14, 15] Despite this, there have been reports of polycrystalline films deposited by pulsed laser deposition (PLD) at high temperature (400-700°C) which have shown field-effect mobility > 100 cm²/Vs.[16] This indicates that it is possible to form thin films and metal-dielectric interfaces that enable carrier transport orders of magnitude higher than other large-area thin film electronic materials (ie. a-Si:H and organics) and comparable with polycrystalline silicon. The primary goal of this work is to develop deposition methods which enable high performance devices at considerably lower deposition temperatures (≤ 250 °C). By reducing the deposition temperature, a range of novel applications on flexible plastic substrates would be enabled.

In addition to crystalline oxides like ZnO, there are large research efforts on amorphous ternary and quarternary materials such as indium-zinc-oxide (IZO) and indium-gallium-zinc-oxide (IGZO) with high field-effect mobility (>30 cm²/Vs).[17, 18] While the defect concentration is often difficult to control in IZO, resulting in small current on/off ratios, the addition of gallium makes this less of a problem and results in a robust process.[19, 20] In addition, the polycrystalline nature of ZnO results in grain boundaries and faceted surfaces which have been identified as possible points of instability.[21, 22] Amorphous oxides do not contain these grain boundaries and faceted surfaces, which may make them more uniform and stable.
This work will describe a novel process for forming high quality stable oxide films at low-temperature using weak oxidant plasma-enhanced atomic layer deposition (PEALD). The PEALD process will be examined in the context of current challenges in oxide based electronics primarily by studying simple thin film transistors (TFTs) and circuits. An improved understanding of the growth and materials properties of films deposited using PEALD will hopefully demonstrate a flexible and robust process capable of forming thin films suitable for a variety of applications.

Chapter 2 will provide an overview of several deposition processes used to form ZnO and Al$_2$O$_3$ thin films at low temperature. A brief description of PECVD will provide the basis for the development of PEALD. In addition, throughout this work, films deposited by a process developed by Eastman Kodak and referred to as spatial atomic layer deposition (SALD) will be compared to PEALD. As a result, a brief description of this technique will be included. The PEALD development effort involved system building and optimization which will be discussed. Chapter 2 will conclude by describing some of the basic materials characteristics of films deposited using these different techniques, highlighting important similarities and differences.

Chapter 3 will describe the basics of thin film transistors and how they are evaluated. The fabrication of thin film transistors (TFTs) requires both a high quality semiconductor but also a dielectric. Several thin film dielectric materials will be discussed and the advantages and disadvantages of these will be compared. Basic TFTs from SALD and
PEALD will be compared. In particular, passivation and electrical stability will be described. The chapter will conclude by describing the temperature dependence of these devices and how this relates to fundamental transport in these thin films.

Chapter 4 will build on the discussion in Chapter 3 with a focus on some of the non-idealities which exist in ZnO TFTs. The chapter will begin by discussing the “non-square-law” behavior and implications on extracting mobility and threshold voltage. This will be followed by a detailed section on the implications of self-heating for electronics on low-cost substrates such as glass and plastic. In particular, we find that output conductance and a runaway breakdown effect can be directly ascribed to self-heating. The chapter will conclude with a discussion of contact non-ideality in oxide TFTs related to barriers at the source and drain. Contact phenomena, which cause both underestimation and overestimation in mobility, will be described and approaches to improve and more accurately evaluate performance will be discussed.

Chapter 5 will describe the application of ZnO TFTs from PECVD, SALD, and PEALD in simple circuits. These circuits provide both an application demonstration and also verify the fast dynamic performance of the devices. This chapter will also contain a description of several ways to improve the circuits (section 5.6), as well as extend the functionality to new substrates and environments (sections 5.7 and 5.8). Finally, fully complementary circuits are achieved by combining these ZnO TFTs with p-channel organic TFTs, demonstrating a pathway to complex low power thin film electronics.
Chapter 6 will conclude the discussion and provide suggestions for future work. In particular, emphasis on integration of current oxide TFTs with other fields will be described. Additionally, suggestions to improve the current device performance will be described with focus on stability and processability.
Chapter 2

Thin Film Deposition Processes and ZnO Characterization

2.1 Plasma-Enhanced Chemical Vapor Deposition (PECVD)

The development of a robust deposition process for ZnO thin films has involved experimenting with a series of deposition techniques. In particular, while sputtering of semiconducting oxide thin films such as indium oxide, tin oxide, zinc oxide, indium zinc oxide (IZO), and indium gallium zinc oxide (IGZO) has been widely studied, in this work different approaches were intentionally pursued.[17, 23-29] PECVD is very similar to chemical vapor deposition (CVD) using metal-organic precursors, but rather than having only thermal energy to drive surface reactions, the plasma can also drive these reactions. This can lead to substantially lower deposition temperatures than in conventional thermal CVD processes. Lowering the growth temperature may allow the use of low-cost flexible substrates and expand the range of potential applications. In addition, as described in the introduction, the largest thin film electronics market is large-area displays. In this technology, the primary dielectric and semiconducting layers, SiNₓ and a-Si:H, are deposited by PECVD. Therefore, using PECVD to deposit ZnO may present a lower potential barrier to implementation in large area industrial applications.

The initial investigations of thin film ZnO at Penn State used PECVD to deposit both doped and undoped ZnO thin films. This investigation was led by Jie Sun and supported by myself. In particular, low-reactivity oxidants such as carbon dioxide and nitrous oxide (as opposed to high-reactivity oxidants such as O₂, O₃, or H₂O) were used to prevent
premature gas phase reactions with the metal-organic precursor and simplify system design. While it was possible to deposit textured thin films with a resistivity near that of indium tin oxide (ITO) through boron doping (in a showerhead PECVD system)[30], the process window for depositing these films was relatively narrow, making the results difficult to reproduce. It was also possible to deposit high resistivity ZnO films (in a ring-fed PECVD system), but the films appeared porous in nature from scanning electron microscopy (SEM) (see Figure 2 (right)) with very low index of refraction from spectroscopic ellipsometry (see Figure 15). Using an effective medium approximation (with bulk ZnO and void), these films contained more than 25% voids. Despite the low density, these films formed thin films transistors with field-effect mobility \( \sim 10-15 \text{ cm}^2/\text{V} \cdot \text{s} \). However, this high mobility was only observed on dielectrics with large gate leakage current (\( > 5 \times 10^{-6} \text{ A/cm}^2 \)). This, combined with very poor electrical stability, suggested the presence of a large numbers of charge states within the ZnO layer or at the dielectric semiconductor interface.[31] In these devices, the gate leakage allowed these states to be charged at a slow rate. However, because the DC sweep was slower, the states were filled and the devices appeared to have high mobility. As a result, the dynamic device performance was very poor and only a fraction of the charge responded at high frequencies. This phenomenon is not new and has been intentionally used to form high performance III-V devices where the interface state densities are known to be large.[32] In addition, in the field of oxide transistors many of the early reports of high mobility devices were also associated with large leakage current densities, prompting similar dynamic response concerns.[23, 33, 34] While most have not reported dynamic response, Hoffman et al. showed capacitance measurements for sputtered ZnO films with
very large dispersion at high frequency (>100 kHz), further suggesting the presence of slow charging interface states.[24] In our PECVD devices, by reducing the gate leakage (to <10^{-7} A/cm²) necessary to charge these states in short times, the field-effect mobility was reduced to ~10^{-2} cm²/Vs.[31] In addition to the low-mobility, simple ring oscillator circuits formed using this material were very slow (~60 μs/stage).[31] The PECVD process also suffered from reproducibility issues in both doped and undoped films and was unacceptable in both performance and stability for most applications.

![Figure 2 - SEM images of (left) 350 nm conducting B-doped ZnO films deposited by PECVD at 200 °C, (right) 100 nm undoped high resistivity ZnO by PECVD at 200 °C. The different microstructures are likely related to crystallinity differences and impurity incorporation arising from the very different deposition conditions.](image)

2.2 Spatial Atomic Layer Deposition (SALD)

While films deposited using PECVD proved unacceptable, in collaboration with Eastman Kodak Company, the use of atomic layer deposition (ALD) was examined to form high quality thin films of zinc oxide. In particular, the process and initial devices were developed at Eastman Kodak by David Levy, Shelby Nelson as well as many others. As the collaboration continued films were sent to Penn State for analysis and device fabrication. ALD involves exposing a reactive surface to a metal-organic precursor which forms a single layer by a self-limiting absorption process. This metal-organic
monolayer is then exposed to a second precursor which reacts with the absorbed metal-organic to form a complete layer. This cycle is repeated to form thin films. While very simple in principle, most practical ALD forms an incomplete monolayer (due to steric effects, desorption kinetics, etc) and often rely heavily on surface reaction kinetics, which are highly dependent on temperature.[35] As a result, most ALD growth processes have a temperature “window” over which the growth is self-limiting with a reasonably constant growth rate. Atomic layer deposition has several key advantages over other deposition processes such as PECVD and sputtering. The first is that it is a very conformal process and can uniformly coat structures with large aspect ratios.[35] Using ALD dielectrics may provide higher yield in thinner films because the process is less sensitive to defects such as pinholes and particles. The reduction of dielectric thickness is important to reduce the device power and is likely to be important in low-cost flexible electronics, as will be discussed in detail later (section 4.2). In addition, because the process forms self-limiting layers, it is possible to accurately deliver extremely uniform films over large areas. The major disadvantage of ALD is that, in general, it is substantially slower than PECVD or CVD processes. In some materials systems, the absorption and reaction kinetics can limit the overall growth rate; however, this is not the case for the materials which will be discussed in this work. The primary cause of slow growth is lengthy purge times required between exposures to each of the reactive species. In typical ALD systems, this long purge reduces the deposition rate to < 1 nm/min. There are several approaches to improve upon this low deposition rate. The first is to make the chamber volume very small and use large amounts of inert gas to rapidly purge
the system. This approach is implemented in commercial systems, such as the Sundew and Beneq ALD tools, which have cycle times <1s.[36, 37]

An alternative to this approach was developed by Eastman Kodak Company and is referred to an atmospheric pressure spatial atomic layer deposition.[38, 39] In this process, channels of the metal-organic precursor and the oxidant are spatially isolated on the substrate as seen in Figure 4 (right). By moving these across the substrate, a given point on the substrate is rapidly exposed to metal-organic, inert gas, and oxidant (see Figure 3 (a)). The earliest head design and an image of a typical film are shown in Figure 3. The film has an interesting stepped thickness which is related to the number of exposures each region receives as the head moves back and forth. This head contains 2 metal organic channels. In the center region, the sweep from left-to-right produces 2 ALD layers, and the sweep back from right-to-left produces 2 more (in total 4 metal layers = 4 xM). In comparison, the far right or left of the sample are only exposed to a single ALD layer per motion (1 xM). Therefore, those layers near the edge of the sample are 4 times thinner than the center region. In between, there are two other steps related to 2 and 3 ALD layers per sweep (back and forth). All of the devices for this work will be described from the uniform center region of the films which had an area of ~30 x 50 mm.
The details of the process have significant implications on how the system runs. First, as shown in Figure 5 (right), to maintain acceptable gas isolation between the two reactive precursors, the separation between the gas flow channels and the substrate needs to be very small (< 100 μm). This requirement means that the isolated gas volume is very small, particularly compared to any chamber based design. This reduction in volume means faster purge times. Second, the most recent spatial ALD system uses gas inlet channels surrounded by two exhaust channels, as shown in Figure 5. By tuning the flows and exhaust channels, the same pressure fields required for isolation will “float” the substrate a fixed distance above the head similar to a gas bearing.[39] This significantly improves the system operation, as high tolerance mechanical structures are not required to hold the sample parallel to the gas channels in extremely close proximity. Small volumes lead to fast rates (> 10-20 nm/min) and good utilization, which is a significant

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**Figure 3** --(a) SALD lateral flow head design with alternating channels of metal organic, inert gas, and oxidant. (b) Typical film deposited using SALD. The center region receives 4 full ALD cycles every time the head moves from left-to-right and back. In comparison the edge only receives 1 ALD cycles during this motion.
advantage of this process, with the chamber volume being replaced in a few tens of milliseconds compared to a few tens of seconds in most chamber based systems. Finally, the nature of the spatial ALD process means that the substrate is run at atmospheric pressure and the gases are constantly flowing. By using constant gas flows, the spatial ALD design can avoid the degradation of pneumatic valve seats after a large number of cycles that are significant issues in chamber based systems. Because the process runs at atmospheric pressure with the substrate suspended by the pressure fields, the spatial ALD process may be potentially interesting for low-cost, roll-to-roll processing. While the spatial ALD process has not yet achieved commercial development, very recently, spatially isolated gases designs have been applied to commercially available research grade roll-to-roll ALD systems by Beneq.[37]

**Figure 4** – Schematics of different ALD processes as published by Levy et al.[39] (left) conventional ALD chamber and precursor pulse sequence. The pulse sequence below shows the overall sequence experienced by the substrate. (right) Spatial-ALD coating head with spatially defined gas regions in contact with the substrate. The pulse sequence below shows the series of gas exposures experienced by a point Q on the moving substrate, yielding a typical ALD sequence.[39]
Due to the difficulties forming highly crystalline, dense, high resistivity ZnO films with good semiconductor-dielectric interfaces by PECVD, different approaches were of interest. By combining the low deposition temperature advantages of PECVD and the knowledge of the ALD process from Kodak a new process was developed referred to as plasma-enhanced atomic layer deposition (PEALD). PEALD of ZnO, as well as Al$_2$O$_3$, HfO$_2$, and ZrO$_2$, has been previously demonstrated using a metal-organic zinc source and high-reactivity oxidants such as O$_2$ and H$_2$O.[40-42] The use of plasma significantly reduced the incorporation of –OH groups, which are related to conduction in ZnO and defects in Al$_2$O$_3$, ZrO$_2$, and HfO$_2$.}[40-42]
In a similar manner to previous PECVD work the use of low-reactivity oxidants, either CO₂ or N₂O, was used in PEALD and a plasma generated the reactive oxidizing species. This allows a simple and fast PEALD process where the low-reactivity oxidant can continuously flow and act as the purge gas when the plasma is not active, and the oxidant with the plasma is started as seen in Figure 6. This may be faster than a conventional ALD cycle where a separate inert gas is required to fully purge each precursor before the next can be introduced. In addition, the plasma chemistry is expected to be somewhat different with different gases (CO₂ and N₂O), powers, and pressures providing additional controllable parameters to optimize low-temperature growth. PEALD, like ALD, is a conformal process with the ability to add substantial energy from the plasma, which may be important in defect control, low-temperature deposition, and doping. For instance, using ALD Al₂O₃ with trimethylaluminum (TMA) and water has been reported at growth temperatures as low as 100°C but the density and etch rate rapidly increases below 150°C.[43] However, Yun et al. also reported Al₂O₃ with low etch rates in dilute HF at temperatures < 90°C using a PEALD process with mixtures of O₂ and N₂.[43] Using PEALD of Al₂O₃ from TMA and either CO₂ or N₂O plasma, films can be formed at room temperature and very low power densities (<0.1 W/cm²). This may be important in a variety of applications, such as encapsulation and diffusion barriers, where high temperature processes are often not acceptable.
The PEALD process with low-reactivity oxidants can be very simple.[44] Undoped ZnO films are deposited layer-by-layer by first providing a pulse of a metal-organic precursor, diethylzinc (DEZ), purging the excess precursor using the weak oxidant, pulsing the RF plasma (13.56 MHz) to oxidize the absorbed zinc precursor, and once again purging the precursor using the weak oxidant. This constitutes one cycle and is repeated to deposit thin films. Figure 6 shows a schematic of system flow for three cycles from both PEALD and conventional ALD.[44] Depending on the plasma conditions, undoped PEALD thin films from CO₂ and N₂O can form high resistivity layers and enhancement mode TFTs, or low resistivity layers and depletion mode thin film transistors.[44] This is substantially different from most reports of conventional ALD ZnO where undoped films are typically limited to only low resistivity and depletion mode devices, and require the use of doping compensation to form high resistivity films and enhancement mode transistors (however, some thin SALD films can be high resistivity).[45-46] While it is possible to perform this PEALD process in conventional PECVD systems, the development of a smaller PEALD system allowed a more rapid and controllable study the growth of ZnO thin films and devices.

Figure 6 - Diagram showing three cycles of chamber/sample exposure (left) conventional ALD with two reactants and inert purge between each, (right) weak oxidant PEALD process where metal-organic and weak reactant do not free react, allowing the weak reactant to act as both purge when the plasma is off and oxidant source when the plasma is on.
The next section will describe the development of two different PEALD systems and a variety of design considerations for future improvements. In both of these systems, a variety of cycle configurations and times were explored. Table 1 shows both the range over which values were explored, as well as values typically used for the high performance devices, which will described in the next chapter. As shown in Table 1 the unoptimized but typical cycles times were 10 – 15 s. Given the typical growth rates for these films (0.1 – 0.3 nm/cycle), the resulting growth rate is 0.4 - 1.8 nm/min. While this process and system is not optimized for speed, this slow growth clearly demonstrates the primary shortcoming of ALD.

Table 1 – Typical cycles times used in three typical processes used throughout this work, but different combinations and configurations were also examined. Here R1 refers to the first reactant typically a metal organic such as TMA or DEZ, and R2 is the second reactant. All values in the table are times in seconds for each segment of the cycle (left column). The format is first the range over which the parameter space was explored, and then typical values used in the parentheses.

<table>
<thead>
<tr>
<th></th>
<th>ALD Al₂O₃</th>
<th>PEALD Al₂O₃</th>
<th>PEALD ZnO</th>
</tr>
</thead>
<tbody>
<tr>
<td>Reactants (R1, R2)</td>
<td>TMA, H₂O</td>
<td>TMA, CO₂ Plasma</td>
<td>DEZ, N₂O Plasma</td>
</tr>
<tr>
<td>R1 Dose (s)</td>
<td>0.5 – 4.0 (0.5)</td>
<td>0.5 – 2.0 (0.5)</td>
<td>0.5 – 2.0 (0.5)</td>
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<td>1 Soak (s)</td>
<td>0.5 – 4.0 (2.0)</td>
<td>0.5 – 4.0 (1.0)</td>
<td>0.5 – 4.0 (1.0)</td>
</tr>
<tr>
<td>R1 Purge (s)</td>
<td>1.0 – 8.0 (4.0)</td>
<td>1.0 – 8.0 (6.0)</td>
<td>1.0 – 8.0 (8.0)</td>
</tr>
<tr>
<td>R2 Dose (s)</td>
<td>0.5 – 4.0 (0.5)</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>R2 Soak/Plasma Time (s)</td>
<td>0.5 – 4.0 (2.0)</td>
<td>0.5 – 4.0 (2.0)</td>
<td>0.5 – 4.0 (2.0)</td>
</tr>
<tr>
<td>R2 Purge (s)</td>
<td>1.0 – 8.0 (4.0)</td>
<td>1.0 – 8.0 (4.0)</td>
<td>1.0 – 8.0 (4.0)</td>
</tr>
<tr>
<td>Total Cycle Time</td>
<td>4.0 – 32.0 (13.0)</td>
<td>4.0 – 26.0 (13.5)</td>
<td>4.0 – 26.0 (15.5)</td>
</tr>
</tbody>
</table>

Spectroscopic ellipsometry has been used to measure film thicknesses and optical properties as a function of exposure times for both Al₂O₃ and ZnO to study the self-limiting nature of the ALD process. ALD Al₂O₃ from TMA and water is considered a nearly ideal system as the kinetics are very fast (<< 1 s) and the surface layer absorbed is very close to the theoretical value for a single monolayer of TMA.[35] The reaction that proceeds is an acid-base reaction with two water molecules donating H⁺ to the radical (–
CH$_3$)$_2$ groups resulting in methane. In that system, the growth rate (less than one Al$_2$O$_3$ monolayer) is largely determined by steric hindrance in the relatively low density TMA monolayer.[35] As a result, a typical saturated growth rates for ALD Al$_2$O$_3$ from TMA and H$_2$O at 200 °C is ~1.0 Å/cycle. In PEALD, a combustion reaction between oxygen radicals and the methyl groups is observed and not the acid-base reaction observed in ALD.[47] However, steric effects still dominate the number of utilized surface states during TMA absorption. As a result, the growth rate for PEALD Al$_2$O$_3$ is nearly identical to that of ALD based Al$_2$O$_3$ at 1.0 - 1.1 Å/cycle.

In comparison, reports of the saturated growth rate for ALD ZnO range from 1.4 – 2.2 Å/cycle at 200 °C.[46, 48-50] In addition, the growth rate is often observed to be a strong function of temperature. This variability may be the result of any number of effects, including multiple monolayer absorption, various levels of impurities, and surface roughness effects. In particular, the crystallinity of the films typically undergoes a transition from (h00) [(100) peak] textured to (00l) [(002) peak] textured at temperatures > 220 °C which has been associated with the loss of residual hydrocarbon.[51] The crystalline order also often results in faceted surfaces which evolve with ZnO thickness, and it is likely that the monolayer absorption is impacted by the spatial changes in surface energy. Despite this wide variability, ALD ZnO has fast reaction kinetics (<< 1 s) as proven by the spatial ALD work described in the previous section with growth rates > 20 nm/min. PEALD ZnO thin films have been deposited from various oxidants including CO$_2$, N$_2$O, H$_2$:N$_2$O, and ozone and have noticed significant differences in growth rate and device performance, depending on the oxygen
source and plasma conditions. All growths were layer by layer and the growth was linear with number of cycles as expected, as seen in Figure 7 (a). However, the saturation characteristics for PEALD ZnO reveal several interesting trends. First, Figure 7 (b) shows distinct differences in growth rate per cycle are observed comparing PEALD ZnO from CO₂ and N₂O. One explanation for this may be that the more ready dissociation of N₂O allows for more complete oxidation reaction to proceed under low power density conditions (0.16 W/cm²). In addition, the growth rates observed for N₂O based ZnO is nearly 2x higher than ALD based ZnO reports from DEZ and H₂O. This high growth rate has also been observed for PEALD ZnO films from dimethylzinc (DMZ) and oxygen, but was ascribed to the smaller metal organic molecule and less steric hindrance.[52] However, it seems more likely that this difference comes from changes in surface reactant mobility induced by the direct plasma bombardment, or secondary reactions from the plasma byproducts and weakly bound metal organic species typically unreacted or desorbed in ALD. In addition to the high growth rate, the plasma time to saturated growth is quite long (> 2 s). This is not likely a fundamental limit and may be significantly modified by changing and optimizing the plasma conditions in future work. The PEALD ZnO used in most of the devices that will be described was formed using N₂O in a near saturated plasma time of 2 s and rate of 2.0-2.7 Å/cycle. It is worth noting that this high deposition rate evolved somewhat as the system functionality changed. As the gas delivery system improved and moved towards high pressure diluted flows (as will be described in the next section), the grow rate dropped to ~2.2 Å/cycle with a smaller dependence on plasma time than observed in this data. This likely indicates that the purge process was more complete with the diluted metal organics minimizing the
parasitic PECVD growth that occurred in this example. However, despite this significant change in growth rate little to no impact on index of refraction, grain size, and device mobility was observed.

![Graph](image)

**Figure 7** – (a) Growth of PEALD ZnO films with a short plasma time (0.2 s) as a function of number cycles for 6 different samples. The process is layer-by-layer and therefore the linearity with cycles is expected. (b) Comparison of saturation characteristics for the oxygen source. The growth rate is significantly higher for PEALD compared to conventional ALD, but saturates at somewhat longer times. The growth rate and saturation characteristics are also a strong function of the oxidant source and likely other parameters which influence the plasma (pressure, power, etc).

### 2.4 PEALD System Development

The earliest depositions by PEALD were done in a slightly modified large Plasma-Therm PECVD system (chamber volume >50 L), however, the large volume and non-ideal gas delivery resulted in very long cycle times (~ 90 s). This long cycle time was particularly a problem with the dielectric growth which, typically is more than 300 cycles (> 7 hrs) meaning that it was impractical to grow every Al2O3/ZnO stack in-situ. Because these films were generally deposited ex-situ, the integrity of the dielectric-semiconductor
interface was often uncontrolled, leading to inconsistent results. Additionally, the condition of the system and even the room humidity for this non-load locked system all impacted the reproducibility of the results.

As a result, a small volume PEALD was built to provide significantly shorter cycles and better system operation and control. As described earlier, in a conventional atomic layer deposition system, the cycle time is often limited by the purging of the excess reactive species. This first system provides not only a smaller volume, which is easier to purge compared to the large PECVD system used in initial trials, but also is computer controlled to provide a highly flexible deposition process. A simple schematic of the small PEALD system, as well as labeled side and top view photographs of the system, are shown in Figure 8. The system is a stainless steel chamber based on an ISO 160 size flanges with a pedestal heater bolted to the base of the system and sealed by an o-ring. This works particularly well, as the heater is surrounded almost entirely by vacuum and the low thermal conductivity gives excellent thermal isolation from the heated area to the walls of the system where o-rings seal the top and bottom. There are several other features to the system which are not as apparent in the pictures. The first is a set of computer controlled pneumatic values required to provide various gases to the chamber over time. Depending on the dosing configuration, which will be discussed in some detail later, there are three or more temperature controlled baths for each liquid source to ensure accurate and reproducible vapor pressure, as well as a series of low-pressure drop MKS 330 mass flow controllers. A machined block of aluminum and a series of spacers acted as an adjustable height powered RF electrode, which stuck through a piece of
polycarbonate, which provided electrical isolation from the rest of the chamber. The heater and chamber walls all act as the RF ground. To enable plasma-enhanced atomic layer deposition, a 13.56 MHz RF network needed to be developed. Several matching systems were used (a manual matching box based on a variable capacitor and rolling inductor, and later an auto matching box based on a logically controlled combinatory switching of various capacitors and inductors) to ensure the impedance presented to the RF generator was close to 50 ohms. Another important feature of these systems is a high voltage supply (> 2 kV) attached to a simple vacuum feed through with a threaded screw on either end. The sharp edges of the screw create a spark when the high voltage is applied and provide a source of electrons to the plasma when it is first started. It was determined that over time, this high voltage feedthrough provided the only consistent way to ensure that the plasma started instantly every time even at low RF power densities. Because this system was an initial design, a capacitance monometer was attached to the right hand side to monitor chamber pressure during the runs. The residual unreacted metal organic in the system goes through a filter flooded with moist air to fully react the metal organic precursors and keep the pump oil relatively clean. Finally, because by its nature ALD require many repetitive valve switches, so LabView software was developed to control all of the system valves. The pneumatic values are controlled using a series of solenoids. These solenoids can be controlled manually using a series of toggle switches or by a LabView controlled board.

This system provided the basis for the vast majority of the results, which will be discussed from this point on, and has a variety of significant advantages, as well as several notable
shortcomings. This system successfully provided a significantly reduced chamber volume (~ 1 L) and subsequently reduced cycle time (typically < 20 s). As a result of the shorter cycle times, nearly all the device results from PEALD were deposited in-situ leading to a highly reproducible semiconductor dielectric interface. In addition, the system had a pedestal heater which was thermally isolated by vacuum and therefore allowed the system to rapidly heat to > 300 °C, although the vast majority of this work was done at 200 °C. The primary drawback to this system design is that the gas flow is non-laminar and not highly uniform. To alleviate this problem, the system often used a soak valve which isolated the pump from the system and diffusion allowed the gases to reach all areas of the chamber uniformly. In addition, the non uniform gas flow required significantly longer constant purges (or fill and purge cycles) to fully evacuate the metal organic gas before the plasma was started.

![Diagram of PEALD system](image)

**Figure 8**  – (Left) simple side-view schematic for the small PEALD system showing the gas flow pattern and location of vacuum sealing o-rings as well as RF electrode and heater. (Middle) side view of small PEALD system with arrows showing the aluminum RF electrode and polycarbonate spacer. (Right) top down view of small PEALD system with the top off showing the input and output gas areas of the system as well as the heated pedestal.

Due to some of the non-uniform flow issues associated with the small system, as well as the desire to deposit on larger substrates. a second PEALD system was designed and built
and can be seen in Figure 9. In order to improve the flow characteristics, the goal was to design a system where the top and bottom electrodes were parallel as well as use uniform slots at the input and output. This means that the use of a pedestal heater (small system) is not possible. However, one of the key advantages to the small system heater is that it is thermally isolated using the minimal thermal conductivity of the vacuum. This thermal isolation is necessary to provide a heated area for the sample which may be > 200 °C but also provide surfaces for o-ring seals which need to be at considerably lower temperatures (< 120 °C). In the large PEALD system, the approach to provide thermal isolation between the heated area and the outer o-rings was to use a thinned aluminum region to limit the thermal heat flow between the central heated area and an outer region which is cooled by a cooling loop. This has been modeled using a finite element model (COMSOL)[53]. It was found that a relatively thin region (1 mm) could provide good thermal isolation and still a large highly uniform ($\Delta T < 5 \%$) heated area (> 5 x 5”). A full design was drawn and the system was fabricated from a single block of Fortal aluminum. Aluminum was chosen for its machinability and Fortal aluminum had a relatively low thermal conductivity (~130 W/mK) compared to other aluminums (> 200 W/mK), providing better thermal isolation. However, after fabrication, it was found that the built in stress from the worked Fortal aluminum resulted in a reversible warping upon heating. To partially fix this problem, an alumina filled epoxy (very low thermal conductivity) from Arremo was used to backfill the thinned region and add mechanical rigidity to the system to minimize warping. While the process development is still a work in progress in this large PEALD system, initial results were very encouraging. This system also provided significant learning about dosing the metal organic precursors for
maximum uniformity in the shortest times. It also revealed a potential non-uniformity in PEALD deposition for two reasons. First, a pressure gradient exists from gas inlet to outlet which interacts with the plasma, and second, the byproducts from the reactions near the gas inlet are incorporated into the plasma towards the outlet, further changing the plasma chemistry. Therefore, appropriate pressures and flow ranges are necessary to minimize the effects of these non-uniformities on the resulting film properties.

The final piece of system development which was extensively worked on to improve uniformity was the gas delivery. Three different methods were employed to deliver the liquid metal-organic materials to the system. The first and most common approach for many ALD systems is to simply pump directly on the vapor pressure of a bottle of metal organic. By doing this, large quantities of metal organic can be delivered to the system.
very rapidly. In our initial designs, this concept was slightly modified to use a MKS 330 low-pressure drop mass flow controller to deliver metal organic vapor at modest flow rates (<10 sccm). The problem with this approach is that with or without the MKS 330 (slightly better with the 330), the dose is entirely dictated by the valve timing. In many ALD cycles, the valve times can be quite short <<1s therefore requiring the valves to open and close in a very reproducible rate. This works, but not ideally. An improved design uses two valves and a fixed volume which fills to a known vapor pressure of metal organic and every cycle doses a fixed pressure and volume regardless of valve time. However, regardless of one or two valves, using a pure metal-organic vapor has another considerable drawback: the tradeoff between dose time and utilization. In many of the metal-organic materials used in this work, the vapor pressure is quite low (<10 torr) but the required dose is also very small (only one monolayer). Because the system had relatively high background pressures (> 500 mT) due to a constantly flowing weak reactant, the pressure volume product for the chamber was significant (0.5 T * 1L = 0.5 Torr·L). In order to significantly impact this pressure-volume product large volumes of metal-organic would be necessary (> 0.1 L), and the utilization for the system would be very poor, as still only one monolayer would be used. It would still be possible to dose a small quantity (1 cm³, 0.01 Torr·L), but then very long dose times would be required so that diffusion of the metal-organic could uniformly coat the chamber. In a better and current design, bubblers are pressurized with a gas that does not free react with the metal organic to create dilute mixtures (~0.5-1%) of metal-organic vapor. This dilute gas is subsequently dosed in fixed volumes. Using this method, small volumes of gas are dosed
(~1-5 cm$^3$, > 2 Torr·L), providing good metal organic utilization but with large pressure volume products primarily made up of inert gas.

Figure 10 shows a schematic for a simple PEALD system design for a single material deposition using the combined advantages of weak reactant and diluted flow. This is a simplified system which switches between only two configurations (via a single switch valve): weak reactant flowing and metal organic soak. The advantage is the process requires only one gas bottle and one metal organic bubbler. Additionally, only a single solenoid needs to be controlled to run the system. The dotted lines represent the compressed air lines, that when activated by the solenoid, open and close the valves. In the first step, the switch valve is as shown in Figure 10 and a constant flow of a weak reactant is metered manually by the needle valve (soak valve is also open). At the same time, the single pneumatic valve between the bubbler and switch valve is open, filling the hatched area to a constant pressure (diluted metal organic in weak reactant). When the switch valve position is switched, the soak valve and the pneumatic valve are simultaneously closed, and a constant volume of diluted metal-organic (hatched area between pneumatic valve and switch valve) is introduced to the system. To then purge the system, the switch valve is moved to its first position. A large pressure pulse (regulated pressure times the volume between the needle valve and switch valve) rapidly purges the chamber and as the pressure stabilizes the RF plasma can be started to complete the PEALD cycle. This example demonstrates how simple the system design and plumbing can be using weak reactant PEALD, making it highly appealing for setting
up and testing new materials; however, where multiple gas sources are used in the same system, the design can quickly become more complicated.

2.5 ZnO Materials Characterization

Throughout the development of these deposition technologies various materials characteristics were examined to identify key similarities and differences. The thin films deposited using PECVD, ALD, and PEALD all have unique physical properties which can be related to the growth conditions and the resulting electrical properties. In particular, assessing the potential differences and advantages that PEALD has over ALD is a goal of this work.

2.5.1 ZnO Crystallinity

The first notable difference between PECVD, ALD, and PEALD is the degree and orientation of the crystallinity in the ZnO thin films deposited at 200 °C. Figure 11 shows X-ray diffraction for films from all three techniques (PECVD from CO₂ and DEZ
on Si/SiO₂, PEALD from CO₂ and DEZ large ring-fed system on Si/SiO₂, SALD from GIXRD shown in Figure 12). The comparison is not perfect, as the films are substantially different in thickness, but shows the orientation as the films evolve. Films less than 300 nm by PECVD have substantially smaller grains than the 300 nm thick film shown, but retain the (002) texture which is typical for most high temperature thin film ZnO.[51] While the PECVD films can have large faceted grains (see SEM image in Figure 2 (left)), these films typically have stoichiometric defects, which result in deposited resistivities <10⁻¹ ohm·cm. In addition, as will be briefly discussed later, the film shown in this XRD has been heavily doped by boron reducing its resistivity < 10⁻³ ohm·cm and may also be responsible for the shifted peak position associated with larger d-spacing. It is possible to form highly resistive ZnO layers by PECVD, but these tend to have very small clusters (< 20 nm) (see SEM image in Figure 2 (right)) and little diffraction in thin films (<100 nm).
Thick ZnO films deposited at 200 °C using spatial ALD (SALD) ZnO show a dominant (100) orientation. The prevalent (002) peak for high temperature and sputtered ZnO films has been reported to be suppressed in ZnO films deposited by ALD from water and DEZ between 155 - 220 °C.[51] Adhesion of anions from the metal-organic source to the polar Zn surface was proposed as a possible explanation for this suppression, and above 220 °C the (002) arises.[51] Another possible explanation is that due to the low resistivity of the ALD films (< 10^{-1} ohm·cm), compensation was added (N-doping through NH₄OH as demonstrated [45]) to form high resistivity layers for thin film transistors. The addition of high levels of nitrogen in the films may also be responsible.

**Figure 11** – X-Ray diffraction patterns for films grown from PECVD (boron-doped), spatial ALD, and PEALD on (100) silicon substrates [except for the 30 nm spatial ALD which came from grazing incidence XRD on glass/Mo/Al₂O₃]. Also included are thinner and thicker films from both spatial and PEALD showing the evolution of the different crystal structure where PEALD has strong (002) texture even in thin films (< 50 nm) while spatial ALD has (100) texture in thick films and is weakly ordered in thin films. A reduction in FWHM for the PEALD films as the film thickness is correlated to an increase in grain size which can be seen in SEM (Figure 14).
for the difference in crystalline orientation. Because high performance TFTs are a primary goal of this work the first \(~2 - 5\) nm of growth is very important. As will be shown in the structures typically used the current is transported through an accumulation channel which is confined to this first few nanometers of ZnO. Therefore the degree and orientation of crystallinity that existed in very thin ALD ZnO layers is of particular interest. For consistency with devices, the same structures used to make thin film transistors (a stack of glass/molybdenum/aluminum oxide/ZnO) were used for grazing incidence x-ray diffraction with an incident angle of one degree to minimize the contributions from the amorphous glass substrate which would cover the ZnO peaks. The results can be seen in Figure 12. As the ZnO thickness increases, the peak intensity increases and in thick films the (100) texture emerges. In particular in films \(< 20\) nm it is not clear that any distinct crystallinity can be seen from x-ray diffraction. In addition, as will be discussed later in this section, very thin films from ALD not only have a random orientation and poor crystallinity, but from spectroscopic ellipsometry, a reduced index of refraction, possibly related to disorder or porosity.
In comparison, PEALD films show (002) texture at 200°C in thin films < 40 nm (see Figure 11), which is consistent with transmission electron microscope (TEM) images (see Figure 13, taken by David Saint-John from Materials Science and Engineering), which show highly ordered columnar grains extending from the interface up to film surface. In addition, the full-width-half-maximum (FWHM) decreased from 0.41° to 0.29° as the film thickness increased from 40 nm to 70 nm. There are a variety of reasons for this, but the most likely is a change in crystalline domain size which has been described in using an analytical model referred to as the Scherrer formula.[54] This formula states that in the absence of strain and other effects, the domain size will be inversely proportional to the crystalline domain size. Therefore approximately a 40% increase in grain size is expected between these films. Figure 14 shows SEM images for both thickness films and represents a typical surface morphology observed in most PEALD ZnO films. Assuming
the domains observed in the SEM are correlated with underlying crystalline domains, a grain size of ~ 30 nm is estimated for the 70 nm thick film and 15-20 nm for the 40 nm thick film representing the expected 40% increase. This suggests that the faceted surfaces observed in SEM are indeed crystalline domains.

Figure 13 – Transmission electron microscope images taken by David Saint-John in Materials Science and Engineering: (left) bright-field image of typical Al$_2$O$_3$/ZnO (Al$_2$O$_3$ grown using CO$_2$, ZnO grown using N$_2$O) stack to be used in thin film transistors. Notably the Al$_2$O$_3$/ZnO interface appears to be very smooth and the ZnO has columnar grains which extend continuously from the interface to the top surface. (Right) dark-field image of the stack showing grain boundaries perpendicular to the interface. Also, diffraction is observed for single crystalline grains of ~ 10-15 nm.
2.5.2 ZnO Optical Properties

The optical properties of a wide variety of Al₂O₃ and ZnO films were studied by spectroscopic ellipsometry and some were analyzed with the help of Nicolas Podraza from Electrical Engineering. Figure 15 shows the difference in index of refraction for high resistivity ZnO films deposited by PECVD, spatial ALD, and PEALD. As mentioned in the PECVD section, it was challenging to deposit dense, high-resistivity films by PECVD. Using an effective medium approximation with voids > 30% void fractions were routinely extracted for these PECVD films. In comparison, thick spatial ALD films often showed considerably higher indices of refraction as well as improved device performance and crystallinity. This high index of refraction (high film density) was used as a marker for improved quality. Even unoptimized initial runs deposited by PEALD showed considerably higher index of refraction than PECVD. In addition, as described in the XRD section, the first few layers represent the region where the carrier accumulation will occur and likely important for transport so ZnO films from PEALD and spatial ALD have been analyzed as a function of thickness. Figure 15 shows that
index of refraction for the spatial ALD films rapidly decreases below about 80 nm and is < 1.9 for films < 20 nm in thickness. In comparison, PEALD films < 20 nm show high index of refraction > 1.94 and are very close to epitaxial films grown on c-plane sapphire. In addition, the spatial ALD films were fit using a more complex model which included surface roughness. In this model an effective medium approximation of ZnO with 50% void was used to model the top surface. However, this was not included in the PEALD results. It is expected that surface roughness contributions would result in a significant improvement in the index of refraction for the thinnest PEALD ZnO films, further flattening the curve. These results are consistent with the highly crystalline dense thin films observed from XRD and TEM and suggest that high quality thin films of ZnO can be grown by PEALD even at low temperature (200 °C). This may be important for a wide range of applications, including thin film devices, but also as potential seed layers for thick ZnO films where the crystalline quality and texture are important.

**Figure 15** – Spectroscopic ellipsometry (left) for thick ZnO films deposited by PECVD, ALD, and PEALD. The high resistivity ZnO by PECVD is highly porous with low index of refraction. The spatial ALD and PEALD are both high. (Right) Plot of index of refraction for spatial ALD and PEALD films. PEALD films have high values even in very thin films, and nearly as high as epitaxial ZnO films grown on C-sapphire [55].
Chapter 3

ZnO Thin Film Transistors

3.1 Background

As described in the introduction, thin film transistors (TFTs) have significant technological importance in large-area displays. The range of applications accessible to these transistors has been somewhat limited by their overall poor performance on low-cost substrates compared to conventional silicon MOSFETs. This poor performance can be characterized using several measures, including field-effect mobility, subthreshold slope, device hysteresis, and bias stress stability. All of these parameters have implications towards the implementation of TFTs in real applications. Additionally, at a more fundamental level, all of these parameters reveal important electrical characteristics of the semiconductor, dielectric, and interface layers. Therefore, fabricating TFTs has two primary goals: providing a useful measure of the electrical properties of new materials, and allowing for the development of real application demonstrations. As an example of the first goal, new organic semiconducting materials are synthesized continuously for use in photovoltaic, as well as TFT applications. These materials often have very low mobility (<1 cm²/Vs) and low carrier concentrations making more direct measurements of the mobility (Hall-effect measurements, capacitance-voltage measurements) nearly impossible in most cases. Other measures of the mobility such as time-of-flight measurements are often very time consuming and therefore, fabricating TFTs provides a rapid method to evaluate the transport. As will be described in this
chapter and the next chapter, the role of interfaces and device non-idealities can have dramatic implications on the values of mobility extracted from TFTs.

The simple model used to evaluate thin film transistors was developed to understand silicon MOSFETs. MOSFETs are typically considered majority carrier devices where most of the current in n-channel devices is from electron and in p-channel devices, holes. The general principle is that a gate is electrically isolated from the semiconductor by a dielectric material and through capacitive coupling induces changes in the semiconducting layer. These changes result in the formation of thin channel of charge, which can be modulated by the gate and is connected to two terminals, the source and drain. The current of a long channel MOSFET (length between source and drain is much larger than the oxide thickness) can be modeled based on the gradual channel approximation, which is valid for the long channel MOSFET operation. Using this model, simple expressions for the current in the linear ($V_{DS} << V_G - V_T$) and saturation regimes ($V_{DS} >> V_G - V_T$) of device operation can be found [detailed derivation and description can be found in [56]]. These expressions are shown below in Equation 1.

$$I_{D,\text{sat}} = \frac{W}{2L} C_\text{ox} \mu_e (V_a - V_F)^2$$

$$I_{D,\text{lin}} = \frac{W}{L} C_\text{ox} \mu_e (V_a - V_T) V_{DS}$$

Equation 1

In these equations, the channel length (L) is defined as the distance between the source and drain which is uniform over a certain width (W). The capacitance of the gate dielectric is assumed to be constant over a range of gate voltages and is given as $C_\text{ox}$. One critical simplification made in these expressions is that the field-effect mobility is
assumed to be independent of the gate voltage. This simplification allows an algebraic solution for the drain current, but it is important to note that in real thin devices this condition is rarely satisfied, and the mobility has some dependence on the gate voltage. Despite the assumption of constant mobility, these simple expressions are widely used to evaluate the performance of long channel MOSFETs as well as thin film transistors.

Short channel MOSFETs are analyzed using different formulas because as the lateral field approaches the vertical gate field, the model breaks down. In this regime the drain field has significant control over the device current and drain induced barrier lowering (DIBL) results in well known short channel effects. In the vast majority of thin film transistors, the channel lengths are typically long (>5 μm) because the devices need to be fabricated over very large areas at low cost. While the oxide thicknesses often need to be somewhat thick (>200 nm) to allow for acceptable yield, the ratio of these two (L/tox) is typically >25 and short channel effect are negligible. This will be reexamined in Chapter 4, along with a variety of other device non-idealities, which make such simple models difficult to usefully apply.

An important difference for many TFTs, including amorphous silicon and ZnO, compared to conventional silicon MOSFETS, is that a staggered structure is typically used. In staggered structures, the contacts are not on the same plane as the accumulation channel, but rather, on the opposite interface of the active layer. This is very different than conventional coplanar MOSFETs where buried wells form the contacts directly in contact with the inversion channel. The staggered structure has the potential for
significant contact effects (since the current must travel through the entire active layer to reach the metallic contacts), particularly as a function of the active layer thickness. Typical structures for staggered and staggered-inverted PEALD ZnO TFTs are shown in Figure 16. Coplanar TFTs can also be formed in both the top and bottom gate forms, and for instance, bottom gate coplanar TFTs are widely used for organic TFTs due to the process sensitivity of the organic materials.

Compared to widely used TFT technologies such as polysilicon and amorphous silicon, the main difference in the ZnO TFTs is the lack of a heavily doped region between the contacts and the active layer. This heavily doped region is the most common way to form Ohmic contacts to semiconductors by sufficiently thinning the contact barrier so that carriers can freely tunnel. In ZnO TFTs, metal contacts rather than doped contacts are commonly used primarily due to process simplification. Most importantly, metals such as Ti and Al form relatively good contacts as deposited with a relatively low specific contact resistivity of $\sim 10^{-4} \ \Omega \cdot \text{cm}^2$. This can be further reduced by using plasma treatments before contact metallization to create a high carrier concentration interface.[57, 58] As a result, for a variety of applications, such as AMOLED, these contacts appear

![Figure 16 – Schematics for passivated (a) bottom gate staggered-inverted structure for ZnO TFTs (b) top gate staggered structure.](image-url)
sufficient and are very simple to form. However, Chapter 4 will describe in detail the impact of non-Ohmic contacts on thin film transistors, which may arise from the staggered structure or a lack of doped contacts.

This chapter will detail simple bottom gate staggered-inverted structure TFTs from SALD and PEALD. A short discussion of PECVD devices and circuits can also be found in Chapter 5. The primary focus of this work was to fabricate high mobility devices with controlled threshold voltage and excellent stability. This work will demonstrate that there are many similarities between the devices fabricated with SALD and PEALD, but there are also some unique and important differences as well.

3.2 Dielectrics for TFTs
The fabrication of oxide TFTs required the development of dielectric materials to act as the gate insulator. In particular, for many large-area TFT applications such as displays, there are a variety of critical parameters for the gate dielectric including: gate leakage current, breakdown voltage, mobile and fixed charge, and charge trapping characteristics. In addition, in ZnO TFTs, due to the large bandgap (~ 3.3 eV) [8] and large electronegativity (~ 4.5 eV) [11], an insulator with a large bandgap (> 6 eV) is needed to provide barriers to both the valence and conduction bands. These requirements largely rule out most organic dielectrics and many inorganic dielectrics. The primary choices for using oxide electronics are silicon dioxide, aluminum oxide, hafnium oxide, and silicon nitride. PECVD silicon nitride is interesting due to its widespread integration into amorphous silicon TFTs for LCD displays. However, the band gap for silicon nitride is
undesiably small (5.1 eV) [59], and charge trapping is known to be a significant problem particularly for low temperature (< 200 °C) deposited dielectrics.[60] Hafnium oxide has a slightly larger bandgap (5.7 eV) [61] than silicon nitride but is still borderline for oxide TFTs. However, the high dielectric constant (~25) [61] means that it is highly suitable for low power applications. In this work, hafnium oxide has not been explored, but it is potentially a promising material for future development. This section will describe the two gate dielectrics used in this work: alumina (Al₂O₃) and silicon dioxide (SiO₂).

3.2.1 Alumina
The majority of TFTs that will be described in this work used an alumina gate dielectric. This was primarily due to the ability to reproducibility form reasonable quality layers at low deposition temperature by atomic layer deposition and the large bandgap of Al₂O₃ (~8.7 eV).[59] Figure 17 (a) shows typical growth characteristics for PEALD Al₂O₃ at 200 °C. As described in chapter 2, PEALD Al₂O₃ is a nearly ideal system and the growth rate observed (1.05 Å/cycle) is similar to conventional ALD. Simple MIS and MIM capacitors are formed by depositing Al₂O₃ on lightly doped silicon and chrome respectively and then depositing a photolithographically patterned aluminum top contact by evaporation and lift-off. From capacitance voltage (CV) measurements on these MIS and MIM structures, the dielectric constant of PEALD Al₂O₃ is found to be ~8, similar to ALD Al₂O₃ at 200 °C, which is slightly lower than often reported for high temperature processes (~9) [59] but still more than twice that of silicon dioxide. From CV on the MIS structures, shifts in the flat band voltage are observed after modest field (2.2 MV/cm) stresses for 12 hrs. Figure 17 (b) shows that these shifts (associated charge of
Q=C_0DV_{FB} \sim 10^{11} \text{ /cm}^2\) in the CV characteristics for both stress conditions (± 2.2 MV/cm) are observed after this stress. These results suggest that large amounts of mobile or trapped bulk or interface charge are not present in this PEALD Al_2O_3.

These Al_2O_3 films also satisfy several of the key application requirements, including low leakage current density and high breakdown field. Figure 18 shows typical current density versus field for SALD Al_2O_3 and PEALD Al_2O_3 deposited at 200 °C. The leakage current density for both materials is very low and less than or equal to 10^{-8} A/cm\(^2\) up to 5 MV/cm. The breakdown voltage for both is similar, between 6-8 MV/cm (breakdown is defined in this case as the voltage where the dielectric catastrophically breaks and the structure becomes shorted, however there is a time dependence to this breakdown which is not represented here (i.e. long times at lower field would also lead to breakdown)). These properties demonstrate low deposition temperature Al_2O_3 films meet many of the requirements described previously for large area oxide electronics.

**Figure 17** – (a) Thickness as function of number of cycles for PEALD Al_2O_3 at 200 °C. (b) Capacitance voltage measurements for 22 nm PEALD Al_2O_3 (Si/Al_2O_3/Al, device area 100 x 220 \(\mu\)m). Two different MOS structures were stressed at 5V and -5 V (inset) for 12 hrs and then the shift in flat band voltage was measured.
However, there are some significant challenges with Al<sub>2</sub>O<sub>3</sub> which are important to consider. First, Figure 22 (a) shows that these Al<sub>2</sub>O<sub>3</sub> layers have strongly temperature dependent leakage current. An Arrhenius plot shows a thermally activated current density at temperatures $>100$ °C with activation energy $E_A = 830 \pm 44$ mV. Similar activation has been observed in other thick film dielectrics, such as silicon nitride, and can be understood as the Poole-Frenkel effect where field-assisted thermal excitation moves carriers between trap states or to the conduction band.[62] The second consequence of this leakage is that it reveals a breakdown mechanism. Figure 22 (b) shows the current for the capacitor structure at 3.125 MV/cm during the temperature ramp. After the temperature reached 190 °C, the device broke down. Additionally, time dependent measurements at high temperatures $>150$ °C showed that large leakage currents were associated with shorter time to breakdown. This result suggests that a finite amount of charge can be supported before breakdown occurs in these layers. As a
result a charge to breakdown phenomena is the likely failure mechanism in these dielectric stacks. In later discussion of self-heating and thermal effects, the temperatures in the devices reach > 200 °C before breakdown, and it seems likely that this activated leakage combined with charge-to-breakdown is the likely failure mechanism. Additionally, later in this chapter, the devices stability will be shown to have a strong field-dependence suggesting charge injection into the dielectric. As a result, most of our device measurements have a rough upper working field of 3-4 MV/cm.

A final challenge associated with Al₂O₃ and particularly ALD Al₂O₃ is the manufacturability of the process. In general, ALD processes suffer from very low throughput particularly where thicker coatings are required. However, it is possible to process in a batch system to minimize some of the throughput issues. In addition to throughput, Al₂O₃ is a very difficult material to gas phase etch. Chamber back etching

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**Figure 19** – (a) Arrhenius plot of temperature dependent leakage for 32 nm PEALD Al₂O₃ layer at 3.125 MV/cm (Glass/Cr/Al₂O₃/Ti), showing an exponential increase from 100 °C to 180 °C. (b) Current density at 3.125 MV/cm as a function of time for a temperature ramp from room temperature to 200 °C showing breakdown after short times at high temperature.
processes are essential in maintaining system cleanliness to ensure yield in large-area displays. Fluorine based chemistries are widely used to dry etch in the semiconductor industry; however, AlF₃ has a very low volatility meaning that the etching process is very inefficient.\[63\] In comparison, AlCl₃ is considerably more volatile and although Cl₂ gas rapidly etches Al metal, it is insufficient to etch Al₂O₃. As a result, ion bombardment in combination with chemistry is required and the dry etching of Al₂O₃ has been demonstrating using BCl₃ based plasma chemistries.\[63\] However, issues related to etch selectivity \[63\] and increased system cost due to the highly corrosive nature of chlorine based gases make this approach somewhat undesirable.

Despite the aforementioned concerns, Al₂O₃ meets most of the initial requirements to form high performance oxide TFTs and is used in most of the devices in this work. In addition to its properties as a dielectric alone, as will described later in this chapter, Al₂O₃ appears to form a relatively high quality interface to ZnO, resulting in improved device characteristics.

3.2.2 Silicon dioxide

The second dielectric used in this work is silicon dioxide. Silicon dioxide has many favorable dielectric qualities including a very high breakdown strength (>10 MV/cm), large band gap (~ 9 eV), low leakage, and it can be fabricated with very low mobile and trapped charges. Additionally, unlike Al₂O₃, dry etching SiO₂ is straightforward and well understood using fluorine based plasma chemistries. However, there are several
drawbacks to SiO₂, particularly, a relatively low dielectric constant (3.9), and the difficulty forming very high quality layers at low deposition temperature (< 500 °C).

The approach examined to deposit SiO₂ was a highly helium diluted PECVD based process originally developed by Batey et al.[64, 65] Batey et al. reported deposited oxide films with properties similar to thermal oxide (large breakdown field, low Dᵥ) at relatively low temperature (350 °C). The parameters used for deposition were similar to those reported; however, a lower growth temperature (280 °C, to make flexible samples possible) and somewhat lower RF power density (to drive uniformity). We achieved similar results as Batey with large breakdown fields (~10 MV/cm) and very low leakage current density. The only drawback to this approach is that the highly diluted He plasma resulted in low growth rates (2 – 6 nm/min) which are not appreciably faster than many ALD processes. The low growth rate makes it less likely that this process is suitable for high throughput manufacturing particularly given the fact that the lower conformality (compared to ALD) means that thicker films will be required to ensure yield. As a result, PECVD SiO₂ films from silane and N₂O without dilution have garnered interest in many oxide TFTs, and despite the somewhat lower quality, may be good enough for many large-area applications.[16, 18]

3.3 SALD ZnO TFTs

As is the case with PEALD, the SALD process developed at Eastman Kodak is continually developing and improving. Designs for the head, as well as the growth conditions, varied widely over the duration of the interaction between Penn State and
Eastman Kodak. Many of these devices fall into two categories: transverse head or floating head (as described in Chapter 2). The devices from the two systems were anecdotally similar, but the majority of ZnO device films from the transverse head used nitrogen doping to compensate intrinsic defects and reduce the free carrier-concentration.[38, 66] As reported by Levy et al. the resistivity for 150 nm ZnO layers was increased by more than 4 orders of magnitude from 1 \( \Omega \cdot \text{cm} \) to \( > 5 \times 10^4 \ \Omega \cdot \text{cm} \) with nitrogen doping.[67] This increase in bulk resistivity was instrumental in forming enhancement mode transistors with good subthreshold slopes.[38] In comparison, many of the devices which were grown with the floating head were formed without any nitrogen compensation, and as a result, higher mobility was observed, but often with implications on the threshold voltage and subthreshold slope. In the discussion of passivation of floating head devices the use of nitrogen doping will also be shown to have particular advantages despite the reduced mobility.

In the collaboration with Eastman Kodak some devices were fully fabricated at Eastman Kodak and sent to Penn State for testing. However, in many cases unpatterned stacks of metal, Al\(_2\)O\(_3\), and ZnO were sent for fabrication and testing at Penn State. The typical fabrication process for SALD TFTs was first cleaning a borosilicate glass substrate using acetone and isopropyl alcohol (glass cleaning at PSU included H\(_2\)SO\(_4\)::H\(_2\)O\(_2\), and high pressure water jet cleaning as well). Then typically a 70 - 100 nm sputtered or evaporated chromium gate (or ITO) was deposited (and in some cases patterned by wet etching). Then these metal coated glass samples were loaded to the SALD system where a 20 -110 nm Al\(_2\)O\(_3\) gate dielectric (from TMA and H\(_2\)O) and 10 – 100 nm thick ZnO
semiconducting layer (from DEZ and H₂O) were deposited. Finally, aluminum source and drain contacts were deposited by evaporation and patterned by either shadow mask or photolithography and lift-off. Because the SALD process is an atmospheric pressure process, the Al₂O₃ and ZnO layers are typically grown ex situ and therefore the critical dielectric semiconductor interface is exposed to an uncontrolled environment. Surprisingly, the ALD process is robust enough to yield fairly reproducible results despite the lack of control of this critical interface. The SALD-grown devices typically have evaporated Al contacts and typically show specific contact resistivity of 10⁻⁴ to 10⁻⁵ Ω·cm² which will be described in more detail in the contact section of Chapter 3. The majority of devices used the blanket Cr layer as a common gate for all devices and devices were isolated from one another by patterning the ZnO layer around the contacts using dilute HCl (1 to 4000 in H₂O, ~30 nm/min). Many devices processed at Kodak had a somewhat different process and used shadow mask to deposit the source and drain metal rather than lift off. The ZnO isolation at Kodak was typically done using a patterned PMMA layer rather than 1811 photoresist used at Penn State. These differences can have important consequences due to the process sensitivity of ZnO. During photolithography, plasma treatments are often incorporated in the contact holes to provide lower specific contact resistivity; however, this process is not implemented with a shadow mask. Additionally, the ZnO layer is very susceptible to etching in any weak acid and some bases, including photoresist developer. This means that the use of PMMA (which is dissolved in organic solvent such as toluene) may provide a less damaging process. As will be described in the passivation section, the process-induced changes make a stable process extremely important for oxide TFTs.
TFT devices were measured in the linear and saturation regime and the threshold voltage was calculated from a linear fit of the $I_D$ vs. $V_{GS}$ curve. Due to the non-ideality of the devices, which will be described in detail in Chapter 4, the conventional extraction of threshold voltage has a dependence on the gate voltage. We have also extracted a turn-on voltage. The turn-on voltage ($V_{ON}$), is defined as the gate voltage where the drain current is in the range of $10^{-11}$ to $10^{-9}$ A depending on the device dimensions (this current level is arbitrarily chosen to a level where the device has a small current). Hysteresis was derived from the difference in $V_{ON}$ in the forward minus the reverse directions.

Figure 20 (a) shows an example of a relatively high mobility unpassivated SALD device from the transverse head with nitrogen compensation. The device is swept in the saturation regime and had an extracted field-effect mobility ($\mu_n$) of ~15 cm$^2$/V·s, turn on voltage ($V_{ON}$) of ~0 V, threshold voltage ($V_T$) of ~5 V, subthreshold slope ($V_{SUB}$) of ~0.6 V/dec, and on/off current ratio ($I_{ON/OFF}$) of >$10^7$. It is interesting to note that for unpassivated devices, these devices show relatively small hysteresis <200 mV. The on/off current ratio is primarily determined by the off-current in the device. The off-current is limited by leakage through the gate dielectric. The relatively high values for gate current (~0.1 nA) are primarily the result of large overlaps between the common gate and the large source and drain pads (500 x 300 $\mu$m). The leakage current density in these devices is very low (<$10^{-7}$ A/cm$^2$) for all gate voltages swept. As a result, by using patterned gates, it is possible to form devices with similar on currents but much lower off currents (< 0.1 pA) and therefore on/off current ratios which are >$10^9$. It is also
noteworthy that compared to PECVD devices which required large gate leakage to have high mobility, these SALD devices exhibited high mobility with this low-leakage dielectric. This finding, combined with the circuit results, which will be described in Chapter 5 suggested that a high quality interface between the ALD Al₂O₃ and ALD ZnO:N was formed.

Figure 20 (b) shows the linear $I_D$ versus $V_{DS}$ characteristics for various gate voltages. The devices are linear at low $V_{DS}$, suggesting reasonable contacts. In addition, the devices saturate relatively well. As will be described thoroughly in chapter 4, the output conductance ($dI_D/dV_D$ in saturation ($V_D>V_G-V_T$)) that does occur is primarily related to self-heating and in this example, the increases in current from self-heating are partially offset by a strongly temperature dependent bias stress, actively reducing the current. In the least stable devices, a negative output conductance is observed as the magnitude and time constants of the positive bias stress dominate. SALD TFTs from the transverse head typically showed field-effect mobility of 5-15 cm²/V·s. These were amongst the earliest demonstrations of high performance ZnO TFTs fabricated using ALD [38, 45, 66] primarily made possible by controlling the free carrier concentration using nitrogen doping. It also suggested that an ALD approach was an easy way to form a high quality interface with Al₂O₃ dielectrics.
The second major class of SALD devices was formed with the floating head. As the process evolved, the use of nitrogen compensation was found to be less important in the floating head. The reason for this is not entirely clear, but the floating head does a much better job of purging the surface and the design led to a significantly more uniform deposition.[39] Additionally, due to its unique design, the pressure range and deposition rates achieved using the floating head are dramatically different than those used in conventional ALD systems where thick films are found to have very low resistivity ($10^{-2}$ Ω·cm) at 200 °C. It is found that in thick films (>100 nm) the floating head SALD films begin to show a rapidly decreasing resistivity which may imply changes in the structure with thickness. This change to highly conducting ZnO films appears to be dependent on a variety of factors including the substrate, recently deposited materials in the SALD system, and possibly even the interaction with the contacts (as will be described in Chapter 4). However, the films used for TFTs are typically < 50 nm and in this regime, it is possible to form enhancement mode devices using uncompensated SALD films.

![Figure 20](image-url)  
Figure 20 – Characteristics of typical transverse head SALD ZnO TFTs with device width (W) and length (L) W/L = 500/50 μm (ITO/100 nm Al$_2$O$_3$/25 nm ZnO:N/Al). (a) Square-root of $I_D$ and log($I_D$) versus $V_{GS}$ for $V_{DS} = 20$V. The gate current $I_G$ is also shown. (b) Linear $I_D$ versus $V_{DS}$ for various gate voltages.
However, the use of nitrogen may have significant implications on TFT performance as nitrogen incorporation in ALD ZnO films has been shown to significantly reduce the Hall-effect mobility.[45]

As a result of the improved growth process which allowed the removal of nitrogen compensation, higher mobility TFTs were fabricated. The typical transverse head TFTs had mobility of $\sim 10 \text{ cm}^2/\text{V} \cdot \text{s}$ while the floating head devices were typically $>15 \text{ cm}^2/\text{V} \cdot \text{s}$. The mobility for some floating head devices reached $\sim 30 \text{ cm}^2/\text{V} \cdot \text{s}$ for uncompensated ZnO films, however, a negative threshold voltage was the primary reason for the higher performance (due to the accumulation dependent mobility). Figure 21 shows a typical floating head device. As will be described in Chapter 4, devices have been measured in the linear regime to prevent self-heating and overestimation of the filed-effect mobility. This device shares many of the same characteristics of the transverse head devices including small hysteresis ($<200 \text{ mV}$) and good subthreshold slope ($\sim 250 \text{ mV/dec}$). Figure 21 (b) shows that as in the transverse head, the devices are highly linear at low $V_{\text{DS}}$, suggesting reasonable contacts, and the devices saturate fairly well at high $V_{\text{DS}}$. The subthreshold slope for the nitrogen doped films both from the transverse head and later from the floating head was typically somewhat lower ($\sim 170 \text{ mV/dec}$) than the uncompensated films ($\sim 250 \text{ mV/dec}$). This is not completely unexpected, as it has been identified that fully depleted active layers are necessary to form the lowest subthreshold slope oxide TFTs.[68] Throughout the rest of this work, SALD devices will be used as a comparison point for PEALD devices.
3.4 PEALD ZnO TFTs

Initial TFTs fabricated using SALD demonstrated that it was possible to form a low defect density interface between ALD Al₂O₃ and ALD ZnO layers. This was notably different than the PECVD devices fabricated previously. In an effort to borrow advantages from both processes, PEALD was developed. Notably, the first runs fabricated by PEALD had higher mobility on low-leakage dielectrics than any that had been fabricated in several years of PECVD. In the initial development of PEALD TFTs, there was a rapid period of optimization.

The first major device difference was found by comparing different gate dielectric materials. Figure 22 shows devices on PECVD SiO₂ and PEALD Al₂O₃. The PECVD SiO₂ device is comparable to most devices fabricated on thermal oxide but with somewhat improved subthreshold slope (≈200 mV/dec on PECVD oxide, ≈400 mV/dec...
on thermal oxide). The SiO$_2$ devices had moderate mobility ~6-10 cm$^2$/V·s at relatively large fields 5-10 MV/cm. These devices also had large on-off current ratios >10$^8$. The primary factor limiting the on-off current ratio is the device off-current. The current where the device is off (large negative $V_G$) is primarily the gate leakage current ($I_G$ in Figure 22 (a)). These test PECVD SiO$_2$ devices were fabricated using heavily doped silicon wafers as a common gate and therefore the source/drain overlap areas were relatively large (2.2x10$^{-4}$ cm$^2$), which resulted in off currents in the pA range despite a very low leakage current density (< 10$^{-8}$ A/cm$^2$). However, in real applications, patterned gates result in much smaller overlaps (<10$^{-5}$ cm$^2$) and therefore on-off current ratios of >10$^{10}$ should be achievable.

In comparison to devices with SiO$_2$ gate dielectrics, devices fabricated on PEALD Al$_2$O$_3$ typically had higher mobility and lower subthreshold slopes. Figure 22 (b) shows an initial PEALD device on glass with patterned gates. As mentioned above, the patterned gate results in lower off currents < 100 fA and therefore higher on-off current ratios >10$^{10}$. These devices showed larger field-effect mobility (>15 cm$^2$/V·s) and remarkably low subthreshold slopes (< 100 mV/dec). The subthreshold slopes achieved approached the theoretical limit (60 mV/dec) for the diffusion current over the contact barrier expected from conventional MOSFET theory.[56] However, as will be described in more detail in Chapter 4, other effects such as contacts may play a large role in these low subthreshold slope values. Figure 22 (b) also shows some device hysteresis (~200 mV), which is primarily related to instability in the devices and will be described in the next two sections.
Both devices fabricated on SiO$_2$ and Al$_2$O$_3$ had turn-on voltages of ~0 V, and threshold voltages of +2 V and +1.25 V respectively. Using these threshold voltages it is possible to compare devices with various gate oxide thicknesses and dielectric constants by plotting the channel charge ($Q_{\text{channel}} = COX(V_G-V_T)$) as a function of gate voltage. This is shown in Figure 23, and a factor of approximately two in mobility between Al$_2$O$_3$ and SiO$_2$ is easily observed. The reason for this difference is not understood, but may be the result of differences in the charged interface states at the dielectric semiconductor interface or the ZnO film growth. There is some error in this calculation, as the exact threshold voltage is difficult to define due to the device non-ideality. Chapter 4 will discuss techniques to extract threshold voltage in non-ideal devices, which make this comparison possible. Additionally, both of these devices were measured in the saturation regime, and therefore, as will be explained in detail in section 4.2, self-heating effects may result in a mobility overestimation. Because the SiO$_2$ devices were formed on
silicon substrates, the self-heating at these power densities is expected to be small; however, the Al$_2$O$_3$ devices on glass are likely to have approximately a 30-50% overestimation in mobility due to self-heating. This would reduce the mobility in the Al$_2$O$_3$ devices to 12-15 cm$^2$/V·s. This plot also identifies several important characteristics of these ZnO TFTs. First, the mobility is a strong function of channel accumulation which will be described in more detail in Chapter 4.1. Second, the devices only show high field-effect mobility at extremely large channel accumulations (>10$^{13}$ /cm$^2$). However, in many applications, to ensure stability, the maximum gate dielectric field may restrict the devices to significantly lower concentrations (< 2x10$^{12}$ /cm$^2$) and therefore much lower mobility (~ 2 cm$^2$/V·s). An understanding of the underlying mechanism behind the carrier dependent mobility is essential in future work.

Another significant increase in field-effect mobility was achieved by using N$_2$O as the oxidant source compared to CO$_2$. The fact that the two devices behaved differently may not be a huge surprise given nearly a factor of 2 in growth rate (see Figure 7). Figure 24
shows the characteristics of PEALD TFTs grown with both CO$_2$ and N$_2$O (both 2s plasma). The N$_2$O based devices showed mobility of 20-30 cm$^2$/V·s [44] while the CO$_2$ devices were typically 7-15 cm$^2$/V·s. The cause of this factor of two is still not entirely clear, but may be related to a more highly ordered columnar structure observed in N$_2$O films compared to CO$_2$ (determined by cross sectional TEM). However, this somewhat oversimplifies the difference and other devices properties, which may be expected to change with a large reduction in mobility, such as the subthreshold slope, are nearly identical for both devices. Particularly in the early development of PEALD devices, the ZnO layers were formed on SiO$_2$ and Al$_2$O$_3$ exsitu. In that case, it was routinely observed that the devices fabricated with N$_2$O had similar or lower mobility and significantly larger hysteresis than devices fabricated with CO$_2$.

As a result, most of the early PEALD ZnO devices were fabricated with CO$_2$ and had mobility of 7-15 cm$^2$/V·s. It was only after the small PEALD system was built that most runs of Al$_2$O$_3$ and ZnO was done insitu and the factor of two in mobility with N$_2$O was routinely observed. Additionally, the growth details were found to be critical in the formation of high mobility TFTs from N$_2$O.[44] In the best PEALD devices, CO$_2$ was used to form the Al$_2$O$_3$ and N$_2$O was used to form the ZnO. However, it was found that devices fabricated using N$_2$O to form Al$_2$O$_3$ and N$_2$O to form the ZnO exhibited extremely low mobility and tremendous hysteresis related to incredibly poor stability [Figure 25]. The reason for this is also not entirely clear but can be assumed to be related to a large interface state density at the dielectric semiconductor interface or enhanced charge injection into the Al$_2$O$_3$ layer. The difference in Al$_2$O$_3$ is not surprising as the
addition of N₂ gas to O₂ in PEALD of Al₂O₃ has been shown to yield a considerably higher breakdown fields than with O₂ alone. As a result of the better performance, CO₂ based Al₂O₃ is used as the dielectric throughout this work.

**Figure 24** – Typical device characteristics for unpassivated ZnO TFTs (W/L = 200/20 μm, tₘ = 37 nm, εᵣ = 8) using N₂O and CO₂ as the oxidant source for the ZnO film deposition. (a) log(I_D) versus V GS in the linear regime (V DS = 0.5V) and extracted differential mobility. (b) linear I_D versus V DS for several values of V GS.
There were a variety of other important growth details which enabled improved devices. Interestingly, it was found that effectively any type of plasma treatment (H\textsubscript{2}, N\textsubscript{2}O) had detrimental effects on the interface properties of the dielectric, leading to reduced mobility and increased hysteresis. In fact, it was found to be essential that the first cycle of the ZnO cycle begin with a metal organic pulse rather than a plasma step, as even short N\textsubscript{2}O plasmas (2 s) created a large number of interface states. In an effort to completely remove the impact of plasma bombardment on the interface, the use of very thin (1.6 nm) ALD ZnO layers (from DEZ and H\textsubscript{2}O) was examined before deposition of the normal 10 nm of PEALD ZnO. The result for the passivated TFTs (the passivation process will be described in the next section) can be seen in Figure 26. The ALD based interface resulted in higher field-effect mobility and improved subthreshold slope, suggesting a reduced interface state density due to the lack of plasma bombardment. Future work on processes which continue to reduce this impact of the plasma, such as a remote plasmas.

Figure 25 – Forward and reverse sweeps for log(I\textsub{DS}) versus V\textsub{GS} in the linear regime (V\textsub{DS} = 0.5V) and extracted differential mobility for a device with both Al\textsub{2}O\textsub{3} and ZnO grown using N\textsub{2}O as the oxidant.
and helium dilution, may be important to continuing to improve the performance of these devices. Table 2 summarizes many of the devices described to this point. The passivated undoped floating head SALD devices and the ALD interface PEALD ZnO devices have the highest mobility and lowest hysteresis.

**Table 2** - Table summarizing the TFT results from various techniques at 200 °C shown in this Chapter. Unless explicitly stated all Al₂O₃ by PEALD is from CO₂ and all Al₂O₃ done in same system as dielectric.

<table>
<thead>
<tr>
<th>Substrate</th>
<th>Dielectric</th>
<th>S/D</th>
<th>Metal</th>
<th>Passivation</th>
<th>Mobility (cm²/Vs)</th>
<th>Hysteresis (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>p+ silicon</td>
<td>45 nm SiO₂</td>
<td>30 nm (CO₂ ring fed PEALD system)</td>
<td>100 nm evap Al</td>
<td>PMMA</td>
<td>6</td>
<td>&lt;0.1 V (best)</td>
</tr>
<tr>
<td>p+ silicon</td>
<td>40 nm PECVD SiO₂</td>
<td>30 nm (CO₂ ring fed PEALD system)</td>
<td>100 nm evap Al</td>
<td>None</td>
<td>6</td>
<td>0.5 V</td>
</tr>
<tr>
<td>Glass/Cr</td>
<td>22 nm PEALD Al₂O₃</td>
<td>30 nm (CO₂ ring fed PEALD system)</td>
<td>100 nm evap Al</td>
<td>None</td>
<td>15</td>
<td>0.3 V</td>
</tr>
<tr>
<td>Glass/Cr</td>
<td>32 nm</td>
<td>30 nm (CO₂)</td>
<td>150 nm</td>
<td>None</td>
<td>12</td>
<td>0.5-1 V</td>
</tr>
</tbody>
</table>

**Figure 26** – Forward and reverse sweeps for log(I_D) versus V_G in the linear regime (V_DS = 0.5V) and extracted differential mobility for a device with both Al₂O₃ and ZnO grown using N₂O as the oxidant.
3.5 Passivation of ZnO TFTs

In all oxide semiconductors, defect chemistry and hydrogen play a critical role in controlling the free carrier concentration and therefore, it is unsurprising that these materials can have strong interactions with processing steps and changes in atmosphere.[7, 8] Any technology built on oxide semiconductors will require a high quality passivation. This passivation layer is required to improve device stability by minimizing charge on the back surface as well as acting as a diffusion barrier.
Figure 27 shows the impact of photolithographic processing on an unpassivated SALD ZnO TFT. In particular, Figure 27 (a) shows that if a shadow mask is used, the device hysteresis can be very small (< 200 meV). However, Figure 27 (b) shows that when photolithography (which involves aqueous basic, and organic solvents) is used, the device hysteresis is very large (>2 V). The cause of this hysteresis is not entirely clear, but may be the result of changes in the charged states on the back interface (eg. Eastman Kodak determined that for SALD devices, PMMA dissolved in methyl isobutyl ketone (MIBK) cause less hysteresis than 1811 in propylene glycol methyl ether acetate (PGMEA)). In many cases, this hysteresis was improved by short anneals at moderate temperatures (30 s at 180 °C is typical); however, it never became as low as the devices which have not seen any processing. Therefore, as this section goes on, one notable characteristic of the passivation is that the hysteresis in many cases is completely removed, despite interactions with photolithography chemicals.

![Figure 27 - SALD ZnO TFTs with (a) shadow mask evaporated Al contacts and (b) Photolithographically and lift-off patterned evaporated Al contacts. The influence of process chemicals results in volts of device hysteresis.](image)

In addition to process related changes, in many potential applications (including active matrix organic light emitting diode (AMOLED) displays) enhancement mode devices are
preferred. There have been many reports of unpassivated enhancement mode oxide TFTs, [25, 58, 66] but very few reports of stable, passivated enhancement mode oxide TFTs. There is a good reason for this. The selection of potential inorganic passivation materials is broad and dielectric materials such as SiO₂ and Si₃N₄ are obvious choices due to their wide applicability in various semiconductor applications. However, the deposition of these materials at low temperature typically requires the use of PECVD processes where the samples are exposed to both plasma bombardment, as well as hydrogen from the siliane precursor. It has previously been demonstrated that very short (< 1 min) argon plasma treatments can dramatically increase the free carrier concentration in ZnO and IGZO films (>10²⁰/cm³).[57, 58, 69] This increase in carrier concentration has been used to form heavily doped regions for ohmic contacts.[57, 58, 69] Similarly, hydrogen has been regarded as a shallow donor in ZnO [70], and it has been shown that hydrogen plasma treatments can dramatically increase the free carrier concentration in various oxide thin films.[69, 71] Hydrogen plasma treated regions and hydrogenated oxide films have also been used to create heavily doped contact regions and ohmic contacts.[69, 72] It is therefore unsurprising that the hydrogen and plasma based processes to passivate oxide transistors with materials such as SiO₂ or Si₃N₄ typically result in negative threshold voltage shifts, indicative of significant increases in free carrier concentration.[18] Figure 28 (a) shows a device before and after PECVD Si₃N₄ deposition. The threshold voltage shift after passivation is estimated to be > 40 V. Despite this general effect the oxide surface properties and deposition details are likely important, and smaller threshold voltage shifts have been observed with PECVD SiO₂ (from silane and N₂O) than from PECVD Si₃N₄ (from silane and NH₃). Additionally, it
has been shown that the use of a \( \text{N}_2\text{O} \) plasma treatment on a-IGZO layers before PECVD SiO\(_2\) deposition can result in small shifts in threshold voltage (compared to > 40 V shift without plasma pretreatment) and near enhancement mode transistors.[18]

In addition to process-induced doping in oxide semiconductors, another important consideration during the passivation process is the role of absorbed surface species. There have been reports of metal oxide thin film transistors, which are very sensitive to changes in the oxygen partial pressure.[73, 74] In both amorphous indium-zinc-oxide and a-IGZO, it has been shown that simply placing the devices in high vacuum (<10\(^{-5}\) T) results in significant negative shifts in the threshold voltage of the devices. These results suggest that the physisorbed oxygen compensates or pins the Fermi level on the exposed surface of these oxide films. The removal of this absorbed layer uncovers a channel layer concentration of \( >10^{20} \) cm\(^{-3}\) in the case of a-IGZO. Therefore, the removal of a layer of absorbed oxygen may also be a component that changes the threshold voltage observed during passivation of some oxide TFTs. However, we have not observed similar phenomenon in either our ZnO TFTs before or after passivation.

The effects of passivation on ZnO TFTs grown by PEALD and SALD were compared. Additionally, these results were compared to the above mentioned literature results on passivation of amorphous metal oxides. Because of the general sensitivity to processing, atomic-layer-deposited-Al\(_2\)O\(_3\) was identified for passivation, due to its lack of plasma bombardment and minimal hydrogen incorporation. This effect of this ALD Al\(_2\)O\(_3\) passivation technique on the behavior of bulk NH\(_3\)-doped SALD ZnO layers, and of H\(_2\)O\(_2\)
surface treatments prior to passivation is also described. 2D drift diffusion modeling using Synopsis Sentaurus [75] was used to understand the dominant electrical effects of passivation, and to distinguish between bulk doping and back channel effects.

As an aside, a variety of polymeric layers (parylene, polyimide, PMMA, etc) were investigated for patterning purposes and also encapsulation, and find that while these films do not generate shifts in the threshold voltage, they do not entirely remove device hysteresis and do not significantly improve the bias stress stability. These polymeric layers are known to be relatively poor barrier layers [76] and are not likely sufficient for many applications such as AMOLED. Thus only inorganic passivation layers are discussed below.

PECVD Si₃N₄ and SiO₂ would be convenient choices for passivation materials, as they are known to work well on Si-based devices and equipment is readily available. Standard PECVD SiO₂ (0.04 W/cm²) and Si₃N₄ (0.06 W/cm²) depositions at 250 °C were used for passivation and it was found that the devices exhibited large threshold voltage shifts (>7 V). In the case of Si₃N₄, the shifts were > 40V negative and as a result the devices could not be turned off before dielectric breakdown [Figure 28 (a)]. Considering the significant amount of hydrogen in the plasma from silane, and previous work on amorphous InGaZnO without pretreatments [18], this doping-like effect was not surprising. Unlike previous work on InGaZnO devices [18], however, N₂O plasma pre-passivation treatment of either SALD or PEALD ZnO films was not effective at surpressing this large threshold voltage shift.
Another straightforward material choice is alumina, which is already present in the devices as the gate dielectric. An interesting difference is evident between PEALD- and ALD-deposited Al₂O₃. Figure 28 (b) shows the device characteristics before and after passivation. For very thin ZnO layers (<12 nm), the devices typically have significant hysteresis (>500 mV) and somewhat reduced field-effect mobility (~10 cm²/V·s). This is not a huge surprise given the close proximity of the back channel to the accumulation channel and charged species (from absorption or fabrication materials) are expected to interact strongly with the device characteristics. After passivating the devices with 30 nm of PEALD Al₂O₃ (trimethylaluminum (TMA) and CO₂ plasma, 0.16 W/cm²), large negative threshold voltage shifts (> 6V) are observed. However, the device hysteresis was completely removed and the field-effect mobility was improved (~30 cm²/V·s). In comparison, by using ALD (grown with TMA and H₂O), which lacks the plasma bombardment present in the PEALD deposition, a significantly smaller negative threshold voltage shift (~2 V) is observed, while maintaining the improvement in device hysteresis and mobility (> 20 cm²/V·s).
Despite the significantly smaller threshold voltage shift observed for ALD-passivated devices, a considerable negative shift in threshold voltage is still observed (~ 2 V) and results in devices with non-negligible current (>100 nA) at $V_{GS} = 0$ V. The device shifts are not completely unexpected as $\text{Al}_2\text{O}_3$/ZnO hybrid films (AZO), deposited by ALD have been demonstrated as low resistivity transparent conducting oxides.[49] Detailed studies on the effects of exposure of ZnO to TMA have shown that TMA preferentially etches Zn from the surface of the film, so stoichiometric defects are expected.[49] This would have the effect of appearing as a “back channel doping” layer on the passivated device. To examine whether this back channel doping was responsible for the threshold voltage shift observed, devices were fabricated with a variety of active layer thicknesses.

Figure 28 –(a) SALD ZnO devices (17 nm ZnO thickness) before passivation, after 50 nm of PECVD SiO$_2$, and after 50 nm of PECVD Si$_3$N$_4$. (b) PEALD ZnO devices (11.5 nm ZnO thickness) as fabricated and after ALD and PEALD passivation.
This will allow discrimination between surface (back channel doping) and bulk effects. The ZnO thicknesses were chosen to vary from 12 nm to 100 nm.

Figure 29 – Experimental data for devices with various PEALD-deposited ZnO thicknesses before passivation (a) and after passivation (b). A weak thickness dependence on threshold voltage before and after passivation is observed but large changes in the subthreshold regime are seen after passivation as the ZnO thickness increases.

Figure 29 (a) shows the devices before passivation were fairly similar with the thinnest channel layers showing lower mobility and significant hysteresis (> 500 mV). In comparison, the thickest films were slightly different showing higher mobility and less hysteresis (< 300 mV), but also a small hump in the subthreshold regime. ZnO films greater than 15 nm had nearly identical field-effect mobility and all devices had similar threshold voltages. Figure 29 (b) shows the results after 30 nm of ALD Al₂O₃ passivation. The first notable characteristic is that all devices showed negligible hysteresis after the passivation. The threshold voltages after passivation for all ZnO
thicknesses were also very similar. However, significant degradation of the subthreshold characteristics were observed in the thicker films (>20 nm). This change in subthreshold can be quantified by using not the device threshold voltage ($V_T$), but rather the turn on voltage ($V_{ON}$), which is defined here as the $V_{GS}$ where $I_{DS} = 10^{-11} \text{A}$.

![Figure 30](image_url)  
(a) Experimental data compared from PEALD-deposited samples. SALD samples showed the same trend. (b) Modeled Sentaurus data for devices both as-deposited and after passivation. Devices were modeled with a background doping of $10^{17} / \text{cm}^3$ in the ZnO films, and to simulate the effect of passivation an additional 2 nm channel on the back surface (“back channel doping”) was doped to $2 \times 10^{19} / \text{cm}^3$. The effect of bulk doping was also examined and background doping was increased from $10^{17} / \text{cm}^3$ (squares) to $10^{18} / \text{cm}^3$ (triangles).
As shown in Figure 30 (a), for PEALD-deposited samples, there is a nearly constant ~ -2 V shift in $V_T$ nearly independent of the ZnO thickness. In comparison, $V_{ON}$ is a strong function of the ZnO thickness. The physics behind this difference can be described in a simple model considering the capacitance of the semiconductor layer as well as that of the gate dielectric. Assuming a charge sheet on the back surface of the ZnO ($Q_b$) the turn on voltage after passivation ($V_{ON, PASS}$) can be related to the turn on voltage before passivation ($V_{ON}$), and the layer capacitances ($C_{OX}$ and $C_{ZnO}$) using:

$$V_{ON, PASS} = V_{ON} - \frac{Q_b}{C_{OX}} - \frac{Q_b}{C_{ZnO}} = V_{ON} - \frac{Q_b t_{ZnO}/\varepsilon_{ZnO} \varepsilon_0}{t_{Ox} / \varepsilon_{Ox} \varepsilon_0} \quad \text{(Eq. 1)}$$

In the case where the ZnO layer is very thin, the depletion layer capacitance is negligible (third term in Eq. 1) the $V_{ON}$ shift is the same as the $V_T$ shift and is just $Q_{BACK}/C_{OX}$ (the second term in Eq. 1). Since the dielectric constant for Al$_2$O$_3$ and ZnO are similar, as the ZnO thickness becomes comparable to, or larger than, the Al$_2$O$_3$ thickness, the ZnO depletion capacitance must be added in series with the oxide layer capacitance. Using this simple model, a linear relationship between the ZnO thickness and the turn on voltage is observed as in the experimental and simulation data. From the experimental data, an induced back channel charge of ~ 4 x $10^{12}$ /cm$^2$ can be estimated during the passivation processes, for the PEALD-deposited samples, and a slightly lower charge for the SALD-deposited samples ~2.5 x $10^{12}$ /cm$^2$. To confirm this simple model and add in a realistic 2D contact geometry, Synopsis Sentaurus [75], a 2D drift-diffusion simulation tool, was used to model the devices. The dimensions used in the model are matched to the PEALD TFTs ($t_{OX} = 32$ nm). To simulate the effect of doping from the passivation
process, the ZnO film is assumed to have a background doping of $10^{17}$/cm$^3$ with a constant mobility of 30 cm$^2$/V·s, and a 2 nm-thick layer (arbitrarily thin thickness chosen but results nearly identical to a charge sheet) on the surface of the ZnO film was doped $2\times10^{19}$/cm$^3$. Figure 30 (b) shows the result of the simulation before and after the back-doping was added. $V_T$ and $V_{ON}$ are weak functions of the ZnO thickness without the back channel doping, which is very similar to the as-deposited experimental data. The absolute values of $V_T$ are somewhat different between the experiment and model; however, this is largely due to non-linear device characteristics and a threshold voltage which is a function of gate bias. In comparison, with back channel doping, $V_{ON}$ shows a strong dependence on the ZnO thickness, and matches the experimental data for passivated samples very well. In strong contrast, if a model is run with high ZnO bulk-doping, $V_T$ and $V_{ON}$ are both strong functions of the ZnO thickness (Figure 30 (b)), which does not match the data. This trend with ZnO thickness is observed even if a large number of states are placed at the back surface to effectively pin the Fermi level. Thus, the model support a back-channel doping (an explanation of passivation induced device shifts) in these ZnO devices and not bulk doping.(Figure 30 (b))

Despite the estimated $>10^{12}$/cm$^2$ back channel charge, the use of thin ZnO channels (<20 nm) and a gentle ALD process is a method of fabricating high performance passivated oxide transistors with threshold voltages of ~0V. It is clear, however, that variations in film thickness will introduce variability in threshold and turn on voltage, so the active-layer thickness control offered by ALD-like processes offer a clear advantage for
inherently good uniformity, reproducibility, and conformality, even in extremely thin films.

A preferred device passivation scheme would not change characteristics with ZnO thickness, and since the accumulated charge is at the ZnO surface, surface treatments were investigated. In the literature, H\textsubscript{2}O\textsubscript{2}-based treatments have been used in single crystals of ZnO to reduce the free carrier concentration.[77] A proposed mechanism, in line with literature XPS reports, is that a lower –OH surface concentration may reduce conductivity after peroxide treatments.[78] Another possible explanation consistent with the observed behavior is that the hydrogen peroxide is converting a thin layer to zinc peroxide. The bandgap of the peroxide is wider than ZnO and is stable to about 200 °C. [79] ZnO\textsubscript{2} can be formed by the interaction of ZnO and hydrogen peroxide.[80] The XPS oxygen peak at 532 eV is consistent with either a peroxide or an O\textsuperscript{2-}.[81] However, it is worth noting that is phenomena is still poorly understood and further work is continuing to distinguish the species present and its impact on the interaction with the passivation films.

SALD-grown TFT devices with a variety of ZnO thicknesses were soaked for 15 minutes in neutralized peroxide, rinsed in DI water for 20 s, dried with N\textsubscript{2} and heated to 180 °C on a hotplate in air for 1 minute immediately preceding the usual 30 nm Al\textsubscript{2}O\textsubscript{3} passivation by SALD. (The 30% solution of hydrogen peroxide in water was neutralized with a 45 weight-percent solution of potassium hydroxide in water to a pH of 7. In the single crystal literature[77], this step is apparently not included, but the mildly acidic H\textsubscript{2}O\textsubscript{2} as received will rapidly and completely etch thin ZnO films.)
The results are shown in Figure 4. After peroxide treatment and passivation, threshold voltages on the thinner samples, 8 nm and 17 nm ZnO, actually move positive, but did not shift at all for 33nm and 50nm-thick ZnO. In even greater contrast to Figure 3, the large dependence on $V_{ON}$ observed without peroxide treatment was completely removed by peroxide pre-passivation treatment. A similar stabilizing effect of $V_T$ and $V_{ON}$ was also observed for H$_2$O$_2$ treated PEALD ZnO TFTs.

Interestingly, the hysteresis story is more mixed. Before passivation, hysteresis was small for all but the thinnest ZnO devices and was completely removed after passivation without pre-treatment, as seen in Figure 4. In the devices treated with peroxide and then passivated, the hysteresis was more negative for thin ZnO layers but approached zero for ZnO devices thicker than 20 nm.

Figure 31 – Characteristics of undoped SALD ZnO TFTs as fabricated compared to devices which have been soaked in peroxide and then passivated with ALD Al$_2$O$_3$. Devices with ZnO thicknesses < 30 nm show more positive threshold voltages and significant hysteresis, however, devices > 30 nm still have $V_{ON}$ > 0 V and negligible hysteresis.
Another approach to eliminate the back-channel doping after passivation is to eliminate carriers not just at the surface, as with the peroxide treatment, but by compensatory doping in the bulk. Ammonia doping in ZnO devices has been shown to compensate intrinsic defects (oxygen vacancies) in ZnO.[8] Ammonia-doped devices grown by SALD show similar mobility to undoped, and had steeper subthreshold slopes [0.31 (V/decade) compared with 0.41 (V/decade) for undoped peroxide pretreated devices]. As seen in Figure 5, ammonia doping had little effect on $V_T$ and $V_{ON}$ before passivation, where a shift of only +0.3 V relative to undoped devices was observed. Similar to undoped ZnO devices, little hysteresis was present in thick unpassivated devices, but it increased as the thickness decreased. After passivation, $V_T$ and $V_{ON}$ shifted negative by ~1.2 V, rather than that observed without ammonia (~ 3 V), and after passivation, negligible hysteresis was observed for all ZnO thicknesses.

![Figure 32](image_url)  

**Figure 32** – Characteristics of SALD ZnO TFTs with NH$_3$ bulk doping as a function ZnO thickness before and after ALD passivation. The threshold voltage ($V_T$) and turn on voltage ($V_{ON}$) are only slightly changed after passivation and the hysteresis for the devices (right axis) becomes negligible.
It might seem that the combination of NH$_3$ doping and H$_2$O$_2$ treatments would provide steep subthreshold slopes, negligible hysteresis, and zero negative threshold voltage shift. In fact, the $V_T$ with and without ammonia doping, after peroxide treatment and passivation, was the same within experiment error. However, as with undoped samples, peroxide treatment before passivation gave rise to large negative hysteresis that decreased as the semiconductor layer thickness increased, but never became as low as untreated passivated devices. A summary of the different passivation processes with uncompensated layers can be found in Table 1.

Table 2. Shift in threshold voltage and assessment for passivation processes which result in enhancement mode TFTs. Several comparable points for sputtered a-IGZO are also included.

<table>
<thead>
<tr>
<th>Passivation Material</th>
<th>Deposition Method</th>
<th>Hysteresis</th>
<th>Threshold Voltage Change</th>
<th>Comparable InGaZnO literature</th>
</tr>
</thead>
<tbody>
<tr>
<td>Polymeric layers (i.e., PMMA, spin on polyimide, parylene)</td>
<td>Spin-on</td>
<td>&lt;200 mV</td>
<td>Negligible</td>
<td>Reduced hysteresis and somewhat improved stability [35]</td>
</tr>
<tr>
<td>SiO$_2$</td>
<td>PECVD</td>
<td>&lt;20 mV</td>
<td>&gt;7 V</td>
<td>&gt;40 V without N$_2$O treatment, &lt;2 V with N$_2$O treatment [19]</td>
</tr>
<tr>
<td>Si$_3$N$_4$</td>
<td>PECVD</td>
<td>&lt;50 mV</td>
<td>&gt;40 V</td>
<td>&gt;60 V [36]</td>
</tr>
<tr>
<td>Al$_2$O$_3$</td>
<td>PEALD</td>
<td>&lt;50 mV</td>
<td>&gt;5 V</td>
<td>N/A</td>
</tr>
<tr>
<td>Al$_2$O$_3$</td>
<td>ALD</td>
<td>&lt;20 mV</td>
<td>&lt;3 V (undoped) 1 V (NH$_3$ doped)</td>
<td>&gt;15 V [35]</td>
</tr>
<tr>
<td>Peroxide plus Al$_2$O$_3$</td>
<td>Soak, then ALD</td>
<td>~100 mV</td>
<td>~0 V</td>
<td>N/A</td>
</tr>
</tbody>
</table>

Thus far, several passivation processes that give good device characteristics have been demonstrated. In addition to protecting the semiconductor from changes in ambient and
providing electrical isolation from upper layers, passivated devices must also show good bias stress stability.

3.6 Bias Stress Stability of ZnO TFTs
The bias stress stability of a device refers to its ability to maintain constant performance under periods of continuous operation for a given application. In amorphous silicon TFTs, a threshold voltage shift is observed upon operation. It is well established that the mechanism responsible for the shift at low gate electric fields is defect generation in the bulk semiconductor layer or at the dielectric-semiconductor interface.[2, 60] At high electric fields, charge injection and trapping in the silicon nitride gate dielectric is the primary mechanism.[2, 60] The charge injection into the silicon nitride is a strong function of the deposition conditions, particularly the deposition temperature. As a result of both of these mechanisms, high temperatures are typically used (>300 °C) and still volts of shift in the threshold voltage are observed for short stresses. For a wide range of applications, including AMOLED, the bias stress stability typically makes implementation impossible.

One potential advantage of oxide TFTs over a-Si:H is improved bias stress stability for films deposited at low temperature (<200 °C). Figure 6 shows an example of the bias stress stability for ALD-passivated PEALD ZnO TFTs. The devices have negligible hysteresis as can be seen in the before and after stress curves. The bias stress conditions used for these PEALD devices were $V_{GS} = 2 \text{ V} \ (6.25 \times 10^5 \text{ V/cm})$ and $V_{DS} = 4 \text{ V}$ held continuously for 20,000 s accelerated by testing at 80 °C. The normalized current
dropped 10% after 20,000 s of stress and the device threshold voltage shift observed was less than 50 mV or \(~7 \times 10^{10} /\text{cm}^2\). These results demonstrate that passivated PEALD ZnO TFTs using thin ZnO layers and ALD passivation can have excellent bias stress stability.

The stability of PEALD ZnO TFTs has been directly compared to the SALD TFTs with NH$_3$ doping and with H$_2$O$_2$ treatment. Figure 34 (a) shows typical TFT characteristics for both SALD devices. The NH$_3$-doped device had near 0 V $V_{ON}$ (-0.6 V), a field-effect mobility of \(~12.5 \text{ cm}^2/\text{V} \cdot \text{s}\), and negligible hysteresis. The H$_2$O$_2$ treated device showed a slightly positive $V_{ON}$ (+0.4 V), field-effect mobility of 15 cm$^2$/V·s, and slight negative hysteresis as described above. For SALD devices, a slightly different bias stress measurement was applied. The bias stress measurement was performed by applying a gate voltage stress of 10 V (2x10$^6$ V/cm) while the drain and source were both grounded, for a given time, with sweeps from +10 V to -5 V, punctuating the measurement at 200 s.

Figure 33 – (a) log($I_D$) - $V_{GS}$ for $V_{DS} = 0.5$ (W/L = 200 $\mu$m/10 $\mu$m, $t_{ox} = 32$ nm, $\varepsilon_r = 8$) including forward and backward sweeps before and after 20,000 s, $V_{GS} = 2$ V, $V_{DS} = 4$ V, stress at 80 °C. (insert) Zoom in to boxed region of (a) to show threshold voltage shift, which is < 50 mV; (b) Normalized current as a function of time during the constant current stress at 80 °C showing 90% of I$_0$ after 50,000 s.
intervals. Figure 7(b) shows that the NH₃ doped device showed only 10% reduction in current after 44,000 s for this relatively high gate-field stress. Assuming that a lateral shift in the threshold voltage is the only change, the change in the electric charge at the interface was calculated ($\Delta Q = C_{ox} \times \Delta V_T$) to be $4 \times 10^{11}$ /cm² after ~25,000 s of stress. The stability of the H₂O₂ treated device was slightly better with a $\Delta Q$ of $4 \times 10^{11}$ /cm² after ~80,000 s of stress. Both of these results demonstrate excellent stability comparable to PEALD ZnO (within the range of differences in test conditions). In particular, both materials show considerably better bias stress stability than a-Si:H with higher field-effect mobility.[3, 60]

While both PEALD and SALD devices have good bias stress stability, there are still non-negligible shifts that occur during long stresses and high-gate electric fields. Figure 35 (a) shows the change in channel charge ($\Delta Q = C_{ox} \Delta V_T$) for passivated PEALD ZnO TFTs after a 300 s stress at various gate field and several temperatures. Figure 35 (a) also clearly shows a very strong gate field dependence on the bias stress. Near the dielectric
breakdown voltage (6 MV/cm) at 80 °C, the change in threshold voltage is between 4 and 5 volts in 300 s. This strong activation is similar to the charge injection observed in the amorphous silicon - silicon nitride system. In addition, the bias stress measurements were performed at 40, 80, and 120 °C, and can be seen in the inset of Figure 35 (a). Temperature does have a small impact on the stress, representing approximately a factor of 2 in charge for comparable fields. However, the impact of temperature is significantly smaller than the electric field for PEALD ZnO TFTs. This combined with short low temperature anneals (30 – 60 s at 150 – 200 °C) recovering process and radiation-induced defects in the PEALD ZnO, suggest that defect generation is not a dominant mechanism in the bias stress of these oxide TFTs. This distinction is somewhat less clear when comparing SALD devices. Figure 35 (b) compares the temperature dependence of $\tau_{90}$ (time for the normalized current to reach 0.9) at low electric field (0.8 MV/cm) for SALD and PEALD ZnO TFTs. The SALD devices are significantly more temperature activated ($E_A \sim 880 \pm 12$ meV) than PEALD devices ($E_A \sim 558 \pm 103$ meV) and may suggest that defect generation mechanisms may be somewhat more important in these devices. In fact, the room temperature stability for SALD devices is often somewhat better than PEALD ZnO TFTs and $\tau_{90}$ can be extracted to $> 10^7$ for low fields ($< 0.5$ MV/cm). Clearly, at low fields the charge injection for both PEALD and SALD devices can be small; however, the mobility at low fields is also low ($< 5$ cm$^2$/V·s), so moving to a dielectric with considerably less charge injection at moderate fields where the mobility is higher ($> 20$ cm$^2$/V·s) is needed to maximize the performance advantage of oxide TFTs.
As a result, the use of other dielectric materials has been of interest. As mentioned in sections 3.2.2 and 3.4, SiO$_2$ may be a much more manufacturable dielectric compared to Al$_2$O$_3$. In addition, thermally oxide silicon is known to be a high quality dielectric. In addition while section 3.5 suggested that back channel charge was a critical part of high stability, the charge injection suggests that the semiconductor-dielectric interface as well as the dielectric material is more important. To exemplify this, Figure 36 shows the bias stress for an early PEALD ZnO TFT ($t_{ZnO} = 80$ nm, CO$_2$) on thermally oxidized silicon with only PMMA as a passivation layer. While the device performance is significantly lower than the devices on Al$_2$O$_3$ (mobility ~ 4 - 6 cm$^2$/V·s), the stability has several very interesting characteristics. The first is for relatively high field stress (3 MV/cm); the total change in charge after 24 hrs is $< 2 \times 10^{11}$/cm$^2$. Most interestingly, Figure 36 (b) shows the normalized drain current during the stress and the shift in threshold voltage saturates after the first 12 hrs of stress and becomes completely stable. This further suggests that

\[ \text{Figure 35} \quad \text{Bias stress measurements on ZnO TFTs. (a) Change in channel charge} \quad (\Delta Q=C_{ox} \Delta V_d) \text{during a 300s stress for PEALD TFTs as a function of gate electric field at three temperatures. (b) Comparison of the activation of bias stress for PEALD TFTs compared to SALD TFTs. The SALD devices have activation energy of ~ 880 meV compared to ~ 550 meV for PEALD.} \]
defect generation is not a primary mechanism in the stress and that if a high quality low temperature SiO$_2$ is developed, highly stable ZnO devices are possible. Further work to develop the low temperature SiO$_2$ and understand the reduced mobility will be essential steps towards a manufacturable process.

3.7 Temperature Dependence of ZnO TFTs

To this point, basic thin film devices were fabricated and the performance could be more than an order of magnitude higher than other thin film technologies. However, nearly an order of magnitude still exists between the single crystal mobility (~200 cm$^2$/V·s) and the measured field-effect mobility. Therefore, an understanding of the carrier transport in ZnO is important in further improving device performance. One approach to studying carrier transport is to examine the temperature dependence.

The first temperature measurements done were on early PEALD devices on thermally oxidized silicon gate dielectrics and can be seen in Figure 37. These devices had the
advantage of a highly temperature stable dielectric (compared to some of the temperature dependent effects for Al2O3 shown in section 3.2.1). Immediately, several important observations can be made. First, the devices are still operating quite well at low temperatures with mobility > 1 cm²/V·s at 77 K. Second, the threshold voltage for the device is steadily moving positive as the temperature decreases. Finally, the shape of the curve, particularly the subthreshold slope, is increasing as temperature decreases. This is unexpected as the subthreshold current for a MOSFET is expected to be primarily diffusion current. The first two of these points will be elaborated on throughout this section, and the subthreshold slope will be discussed somewhat during the discussion of contacts in section 4.3.

Figure 37 – (a) log(I_D) and I_D versus V_G for PEALD devices on 45 nm thermal SiO₂ at temperatures from 80 to 360 K (40K steps). (b) log(I_D) and differential mobility versus V_G over the same temperature range corrected for the shift in threshold voltage.
There are several important temperature dependent characteristics in these PEALD ZnO TFTs. Figure 38 (a) shows a plot of $\ln(\mu_e)$ versus $1/T$ shows that the field-effect mobility is very weakly activated between 400 K and 100 K with activation energy of $\sim 15$ meV for these devices on SiO$_2$ (DEZ and CO$_2$ plasma used to deposit ZnO TFTs at 200 °C). This temperature dependence is nearly independent of channel length (even though the mobility is lower for the short channel device due to contact resistance). This result suggests that the temperature dependent transport in these oxide materials may also be quite different from semiconductors such as amorphous silicon. Figure 43 shows that in amorphous silicon the temperature dependence can be modeled as a simple activated process with activation energy often an order of magnitude higher ($> 150$ meV) due to the large density of localized tail states.[82, 83]
The second large change is a nearly linear positive shift in threshold voltage as the temperature decreases. This threshold voltage shift ($\Delta V_T \sim 0.01 \text{ V/K}$) can be converted to a charge ($Q = C_{ox} \Delta V_T$), and is $\sim 0.75 \text{ nC/cm}^2\text{K}$. The nature of this threshold voltage shift is not well understood but may be related to pyroelectric charge in the ZnO layer and will be touched upon in this section and has significant implications for self-heating in devices as will be described in section 4.2. It is notable that this shift in threshold voltage is fully reversible and has a relatively short time constant (less than ms shifting measured, less than seconds recovery measured and likely faster).

Figure 39 shows the temperature dependent behavior of a passivated PEALD ZnO TFT on Al$_2$O$_3$ (N$_2$O for ZnO) from 300 K down to 10 K. The activation energy from 300 K to 100 K at equivalent $V_G-V_T$ can be seen in Figure 43 and with activation energy of $\sim 5 \text{ meV}$ is somewhat lower than the device on SiO$_2$. As the temperature decreases below 100 K, the activation energy continuously decreases and as a result PEALD ZnO TFTs still operate with mobility $> 1 \text{ cm}^2/\text{V} \cdot \text{s}$ even at temperatures $< 10 \text{ K}$. Figure 41 (b) shows a more significant positive shift in threshold voltage with decreasing temperature is observed than for the thermal oxide devices described above. The shift in threshold voltage with decreasing temperature from 300 K to 100 K is again fully reversible with a charge coefficient of about -2.9 to -4.9 nC/cm$^2$K. This is approximately 5 times larger than SiO$_2$, and the discrepancy in the values comes from challenges extracting an accurate threshold voltage (which will be described in section 4.1). The temperature dependent characteristics of these TFTs also demonstrate that PEALD ZnO does not appear to contain a large concentration of deep subgap traps which reduces the field-
effect mobility with decreasing temperature as found in other low-deposition-temperature thin film systems. However, a large threshold voltage shift and increase in subthreshold slope is observed at low temperatures leading to large reductions in device current and demonstrating that simple MOSFET theory cannot fully explain the device behavior.

Similarly, Figure 40 shows the temperature dependence of SALD floating head ZnO TFTs on Al₂O₃. Many similar trends are observed between PEALD and SALD devices. The field-effect mobility for the SALD devices is very weakly activated with nearly identical activation energy (~ 5 meV) as PEALD from 300 to 100 K (see Figure 43). The threshold voltage shift over that temperature range is also linear (1.3-2.2 nC/cm²K) and about half that of the PEALD devices. In addition, due to the smaller threshold voltage shift, it is possible to observe the peak differential mobility even at 10 K. Interestingly, the mobility is still ~ 8.5 cm²/V·s only approximately a 50% reduction from room

Figure 39 – (a) log(I_D) and I_D versus V_G for PEALD ZnO devices (Al₂O₃ dielectric, N₂O for ZnO) at various temperatures from room temperature to 10K. (b) I_D and differential mobility as a function of gate voltage corrected for the threshold voltage shift over this temperature range.
temperature. The same device non-idealities that were present in the PEALD devices are observed in SALD devices. The changes in threshold voltage shift and the subthreshold slope both accelerate at temperatures below 100 K. The changes in threshold voltage and subthreshold slope are not understood but may be related to contact effects. In section 4.3, a discussion of contact gating may provide a partial explanation for both of these low-temperature non-idealities.

Figure 40 – (a) log(I_D) and I_D versus V_G for floating head SALD devices at various temperatures from room temperature to 10K. (b) Differential mobility as a function of gate voltage over this temperature range.
Despite this claim and contact non-idealities, which will be discussed in section 4.3, contacts alone do not seem to provide a complete explanation for the device characteristics. Transmission line measurements have been performed as a function of temperature to examine this effect. Transmission line measurements simplify a transistor as a set of resistors in series (contact resistance + channel resistance + contact resistance). By measuring transistors with various channel lengths, a plot of resistance versus channel resistance allows the extraction of the channel resistance (varies with L) and contact resistance (invariant with L). The same devices on SiO₂ shown in Figure 37 and Figure 38 were used and 3 channel lengths (5, 10, 35 micron) were fit to extract the contact resistance and the sheet resistance. The result is shown in Figure 42. Interestingly, the contact resistance is a strong function of temperature from room temperature to 150 K with activation energy ~86 meV. However, below 150 K the contact resistance becomes nearly temperature independent with activation energy ~6 meV. While these
measurements do not extend down to 10K where large changes were observed, they do suggest that contact resistance is not dominant. Particularly given that at high temperatures where the mobility and threshold voltage are changing slowly, the contact resistance is changing rapidly. Accordingly, the extracted sheet resistance follows the shape of the extracted mobility data much better over this temperature range. From these results, it is clear that still unknown phenomena are changing the threshold voltage and subthreshold slope at temperatures below 100 K.

![Temperature dependent transmission line measurements to extract sheet resistance (ρ_s) and contact resistance (R_C) as a function of temperature.](image)

**Figure 42** – Temperature dependent transmission line measurements to extract sheet resistance (ρ_s) and contact resistance (R_C) as a function of temperature.

While there are some phenomena to understand, there are some conclusions which can be reached. Figure 43 (b) shows a table comparing these materials and interestingly the change in channel charge from the threshold voltage shift seems to be inversely proportional to the peak mobility and mobility activation energy. In addition, all of the devices fabricated on Al₂O₃ had larger charge coefficients than SiO₂. This may suggest that the dielectric itself plays a role. Figure 43 (a) shows an Arrhenius plot for mobility
for various materials described in this section. As described, all the oxide TFTs have considerably smaller activation energies than materials such as amorphous silicon.

A potential explanation and model for the small activation energy, which decreases as the temperatures decreases below 100K, is also important to consider. Kamiya et al. have thoroughly described the electronic structures of many amorphous and crystalline oxide semiconductors.[9, 84, 85] In general, the unique component of oxide semiconductors is that due to the highly ionic nature, the conduction band is comprised nearly entirely from the heavy metal cations, and the valence band nearly entirely from the oxygen anions. This has significant consequences as the large spherical 4s orbitals that make up the conduction band are fairly insensitive to order. As a result, amorphous and crystalline manifestations of the same material often have very similar mobility. Temperature dependent Hall-effect measurements in doped amorphous and crystalline indium-gallium-zinc oxide films showed that for heavily doped films (>10^{20} /cm^3) the activation energy

Figure 43 – (a) Mobility temperature activation comparison of several different thin film transistor materials (*Chen et al. [83]). (b) Table summarizing the room temperature mobility, mobility activation energy, and change in charge with temperature for various materials discussed in this section.

<table>
<thead>
<tr>
<th>Dielectric</th>
<th>Active</th>
<th>( \mu ) (cm^2/Vs)</th>
<th>( E_A ) (meV)</th>
<th>( \Delta Q ) (nC/cm²K)</th>
</tr>
</thead>
<tbody>
<tr>
<td>SiN_x</td>
<td>a-Si*</td>
<td>1</td>
<td>&gt;150</td>
<td>-</td>
</tr>
<tr>
<td>thermal SiO_2</td>
<td>PEALD ZnO</td>
<td>6</td>
<td>15</td>
<td>0.75</td>
</tr>
<tr>
<td>thermal SiO_2</td>
<td>PEALD ZnO</td>
<td>12</td>
<td>9</td>
<td>1.7</td>
</tr>
<tr>
<td>thermal SiO_2</td>
<td>PEALD ZnO</td>
<td>20</td>
<td>5</td>
<td>2 – 5</td>
</tr>
<tr>
<td>thermal SiO_2</td>
<td>PEALD ZnO</td>
<td>20</td>
<td>5</td>
<td>1 – 3</td>
</tr>
<tr>
<td>SALD Al_2O_3</td>
<td>SALD ZnO</td>
<td>20</td>
<td>5</td>
<td>1 – 3</td>
</tr>
</tbody>
</table>
was approximately zero. However, lightly doped films (<10^{18} /cm^3) were highly activated. The temperature behavior was well described using a percolation model assuming a Gaussian distribution of barriers above the conduction band edge. The mobility can be described using Equation 2 where \( \mu_0 \) is a temperature independent mobility parameter, \( e \) is the unit charge of an electron, \( k \) is Boltzmann’s constant, \( T \) is temperature, and \( \phi_0 \) and \( \sigma_\phi \) represent the barrier height and standard deviation for the Gaussian distribution, respectively.

\[
\mu_s(T) = \mu_0 \exp\left(-e \frac{\phi_0 - e\sigma_\phi^2 / 2kT}{kT}\right)
\]

Equation 2

Using this model, the barrier heights of the highest quality crystalline and amorphous indium-gallium-zinc oxide films was found to be effectively zero for films with doping densities greater than 10^{19} /cm^3. This explains the observation that negligible changes in mobility with temperature were observed for degenerate films. The following discussion will apply a similar model to extracted temperature dependent field-effect mobility data in PEALD and SALD devices and finally compare the performance to these reported amorphous oxide films.

Figure 44 shows an Arrhenius plot for the differential mobility as a function of temperature at a variety of constant gate voltage past threshold for the data shown in Figure 39 and Figure 40. By fitting temperature dependent behavior at constant \( V_G - V_T \) it is possible to examine how the model barrier height changes with channel carrier accumulation. Figure 44 shows an example of several fits to both PEALD and SALD
TFTs on Al₂O₃. The model works well when the barrier height is less than 10 times the thermal energy (kT).

Figure 45 (a) shows that in PEALD ZnO TFTs on Al₂O₃ (peak differential mobility ~ 20-30 cm²/V·s), the barrier height and standard deviation steadily decrease from ~ 50 ± 20 meV at 5 x 10¹²/cm² to ~ 7 ± 6 meV at 1.4 x 10¹³/cm² and the temperature independent mobility prefactor increases from 12 to 22 cm²/V·s. This reduction of barrier height and distribution width provides a mechanism for the carrier concentration dependent mobility observed in nearly all oxide thin films and devices. In addition, at the highest accumulations (>10¹³/cm²), the barrier height becomes very small (<10 meV) which is consistent with the good performance of these devices even at very low temperature. Interestingly, a similar trend is observed for PEALD ZnO TFTs on SiO₂ (peak differential mobility ~5-10 cm²/V·s). The barrier height and standard deviation steadily

Figure 44 – Differential mobility at a variety of constant V₉-V₇ for (a) PEALD device shown in Figure 39 and (b) SALD device shown in Figure 40. The dotted lines in the high temperature range are the modeled fit. The activation energy for both PEALD and SALD approaches ~ 0 eV as the temperature decreases below 50 K.
decrease from \(~ 108 \pm 30\) meV at \(6 \times 10^{11}/cm^2\) to \(~ 23 \pm 11\) meV at \(7 \times 10^{12}/cm^2\) and the temperature independent mobility prefactor increases from 2.2 to 15 cm²/V·s. This is noteworthy because the devices on SiO₂ are typically more than a factor of 2 lower in field-effect mobility, and if this was related to structure, the temperature dependence is expected to be different. However, at comparable accumulations, the temperature independent mobility parameter is nearly identical for both the Al₂O₃ devices and SiO₂. The temperature data does not extend to very high fields on SiO₂, and Figure 45 (b) shows that the extracted differential mobility is just starting to separate between Al₂O₃ at accumulations \(> 5 \times 10^{12}/cm^2\). It is therefore expected that the barrier height for SiO₂ will likely not reduce to values as low as Al₂O₃ at large channel accumulations, and this results in the difference in extracted mobility.

A similar picture is formed for the SALD based devices. The barrier height and standard deviation steadily decrease from \(~ 50 \pm 19\) meV at \(1.8 \times 10^{12}/cm^2\) to \(~ 8 \pm 7\) meV at \(1.1 \times 10^{13}/cm^2\) and the temperature independent mobility prefactor increases from 6.8 to 21 cm²/V·s. These devices have notably smaller barriers at lower carrier accumulations compared to PEALD devices; however, the barrier height appears to reach a slightly higher minimum at \(~ 8\) meV at carrier accumulations \(> 10^{13}\) /cm². This is a very important difference for real device performance because in many applications, low dielectric fields are imposed to ensure stability and therefore, the maximum carrier accumulations reached for enhancement mode devices is typically \(< 5 \times 10^{12}/cm^2\). As a result, it is desirable to have a high mobility at low carrier accumulations to differentiate from materials such as amorphous silicon. In this regard, the SALD TFTs have an
advantage over PEALD TFTs. This is not likely fundamental and comparing a range of SALD and the best PEALD devices would likely yield less marked differences.

Figure 45 (a) also shows that the thermal energy at room temperature (~26 meV) is significantly larger than the barrier height and multiple standard deviations at the highest carrier accumulations for the devices on Al2O3. This suggests that thermionic emission over barriers (e.g. grain boundaries) does not reduce the field effect mobility from its single crystal value (~200 cm²/V·s) to the measured values (~20 cm²/V·s). These values were also consistent with the reported high quality amorphous and crystalline IGZO.[86] However, further work to understand the mechanism driving a reduction in mobility is necessary. In addition, the assumption that the threshold voltage should be removed from this calculation (comparing at constant Q = Cox (V_G - V_T)) makes the accurate calculation of this value very important. Figure 45 (b) also shows that the calculated temperature independent mobility prefactor from the barrier model follows a similar trend to the extracted differential mobility at room temperature. This confirms that comparing the slopes and peaks of the differential mobility as a function of carrier accumulation at room temperature is a meaningful method to understand the device transport.
Figure 45 – (a) Barrier height extraction from PEALD and SALD devices. The error bars represent standard deviations in the Gaussian distribution. The calculated Fermi level as a function of doping assuming a 5 nm uniformly doped channel is also marked. The 5 nm channel accumulation is an approximation to roughly estimate the carrier concentration in the channel to compare to IGZO Hall measurements. (b) Comparison between the temperature independent mobility parameter from the barrier extraction and differential mobility.
Chapter 4  
Device Non-idealities and Physical Mechanisms

4.1 Non-ideal Characteristics

Chapter 3 outlined typical characteristics of PEALD and SALD ZnO TFTs. However, there are some important non-idealities in the device characteristics that have significant implications on the interpretation of these characteristics, as well as how the devices are implemented in real applications. The first and most prominent non-ideality present in nearly all oxide TFTs is an accumulation dependent mobility. This results in numerous negative effects which will be discussed over the next several chapters, including miscalculation of mobility and threshold voltage (this section) and reduced saturated load inverter gain (section 5.5). The mechanism behind this non-ideality is still not well understood and has been described as grain boundary barrier modulation [87] and may be related to above conduction band potential barriers as modeled in section 3.7.

Figure 46 shows this effect clearly by comparing TFT extractions to a gated Hall-Effect measurement. The extracted mobility as shown throughout Chapter 3 is a strong function of gate voltage (and therefore $N_s$). The interpretation of threshold voltage and the impact of many other device parameters such as contacts can create differences in the extracted TFT mobility. However, Figure 46 (b) shows the results of a gated Hall-effect measurement on the same sample. A Van der Pauw structure was formed on a gate and oxide which allowed the semiconductor accumulation to be changed as a function of the applied gate voltage. Then, the Hall-effect (0.5 T magnetic field) can be used to provide another measure of mobility in these materials. It is notable that the mobility is also a
function of sheet concentration (even up to large values of $N_s \sim 10^{13}/\text{cm}^2$). However, the slope of the mobility versus gate voltage is much lower. The following discussion will describe this phenomena and its impact on the extraction of key parameters, such as threshold voltage and mobility.

This accumulation dependent mobility has significant implications on the evaluation of TFT performance. From the gradual channel approximation, Chapter 3.1 discussed the simple evaluation of current in the linear and saturation regime and relationships were derived for both (see below).

$$I_{DS,lin} = \frac{W}{L} \mu c \sigma (V_g - V_T) V_{DS}, \quad V_{DS} << V_g - V_T$$

$$I_{DS,sat} = \frac{W}{2L} \mu c \sigma (V_g - V_T)^2, \quad V_{DS} > V_g - V_T$$

Equation 3

Therefore, a common approach to determining the threshold voltage and field effect mobility, assuming both are constant, is to fit a plot of $I_D$ versus $V_{GS}$ in the linear regime.
or $\sqrt{I_{DS}}$ versus $V_{GS}$ in the saturation regime. Therefore, in the further discussion, a “square-law” device will refer to a device which satisfies both the above relationships and has approximately a constant mobility and threshold voltage.

However, in these oxide TFTs, the mobility and threshold voltage is not typically constant and therefore the simple interpretations that are used throughout the literature, as well as in Chapter 3 here do not represent the device current accurately. Figure 47 shows this non-ideality for the typical PEALD devices shown in Figure 26. A straight-line fit to this linear regime $I_{DS}$ versus $V_{GS}$ yields a mobility of $\sim 22 \text{ cm}^2/\text{V}\cdot\text{s}$ and a threshold voltage of $\sim 2 \text{ V}$. However, it is notable that this fit is only valid for a small range of gate voltages (4 – 8 V), and the device appears to be far out of subthreshold at the extracted threshold voltage ($\sim 2 \text{ V}$). In fact, the differential mobility (which is solved by taking the $dI_D/dV_G$ of Equation 3, solving for mobility, and plotting versus $V_G$), which is shown in Figure 26 is somewhat higher than this straight-line fit and gives peak mobility values of $\sim 24 \text{ cm}^2/\text{V}\cdot\text{s}$. This arises because the mobility continues to change between 4 and 8 V where the straight-line is fit. Therefore, it is clear that neither of these approximations is effective at evaluating the current over a wide range of accumulation.
The first primary problem is that it is clear that the threshold voltage extraction is not sensible. A more reasonable threshold voltage can be determined by a variety of methods which will be described later in this section. These different methods yield values of the threshold voltage for this device of between -2 and -3 V. However, if this more reasonable threshold voltage is used, both the constant mobility extracted from a straightline fit and the differential mobility significantly overestimate the device current. This can be seen in Figure 48 (a) where a comparison of the measured device current and calculated currents based on constant threshold and different definitions of mobility are considered. In both cases, the actual device current is approximately half of what is expected given the threshold voltage and mobility. This is reemphasized in Figure 48 (b) where the differential mobility commonly used in the literature and in Chapter 3 is compared to the mobility back calculated from the measured current assuming a constant

**Figure 47** - Typical passivated PEALD device measured in the linear regime. The straight-line fit is used to calculate field-effect mobility and threshold voltage for the device.
threshold voltage of -3 V. Once again, reductions of nearly a factor of two in field effect mobility were observed when this difference is accounted for.

It is also noteworthy that after assuming a constant threshold voltage and calculating the mobility from the drain current, there is still a strong dependence on the carrier accumulation. It is also evident that the peak mobility is extended out to slightly higher accumulations than determined from the differential mobility. Therefore, as mentioned above, determining reproducible ways to identify a threshold voltage to calculate mobility are highly relevant. In addition, the identification of a single threshold voltage is important in the development of compact models.

There are several potential methods for calculating the threshold voltage for a non-square law device. The first common approach used often in amorphous silicon, as well as this
work, is to use the gate voltage where a set current in the subthreshold regime is observed. This voltage, $V_{ON}$, was described in Chapter 3.5. The disadvantage to this method is that changes in the subthreshold slope directly interact with this voltage. Particularly where humps and large subthreshold stretching is observed, it is possible for $V_{ON}$ to vary by many volts.

The second approach is a straightline fit to the differential mobility plot. Because the extracted mobility for these oxide TFTs is often approximately linearly dependent on accumulation, this is a straightforward way to determine where the device turns on. As an example, for a typical device such as Figure 24 this would yield a threshold voltage of $\sim 2.5$ V.

Finally, in other thin film transistors, such as amorphous silicon, non-square law behavior is observed and a method of modeling this behavior has been developed and included in compact models.[88, 89] This method uses a modified model to fit the drain current. This modification is shown below.

$$I_{DS,lin} = \frac{W}{L} \mu_e C_{ox} (V_G - V_T)^m V_{DS} \quad , \quad V_{DS} \ll V_G - V_T$$

$$I_{DS,sat} = \frac{W}{2L} \mu_e C_{ox} (V_G - V_T)^m \quad , \quad V_{DS} > V_G - V_T$$

Equation 4

The $(V_G - V_T)$ term is modified to have a variable power and fit the carrier dependent mobility. In this case, the variable “$m$” typically ranges from 1 to 2.5 in the linear regime and 2-3.5 in the saturation regime for the oxide TFTs in this work. The method for determining this power is a straightforward and is shown below.
\[
H(V_G) = \frac{\int_{V_G}^{V_T} I_{D,\text{sat}}(V_G)dV_G}{I_{D,\text{sat}}} \quad \Rightarrow \quad H(V_G) \approx \frac{\int_{V_G}^{V_T} I_{D,\text{sat}}(V_G)dV_G}{I_{D,\text{sat}}} \quad \Rightarrow \quad H(V_G) = \frac{(V_G - V_T)}{m+1}
\]

Equation 5

The integral of the drain current between threshold and a given gate voltage is divided by the drain current over the same range in the saturation regime. This function, \(H(V_G)\), then can be fit by a straight-line to determine the power “\(m\)” and a threshold voltage \(V_T\). Figure 49 (a) shows a PEALD ZnO TFT and Figure 49 (b) shows \(H(V_G)\) and the extracted “\(m\)” as a function of gate voltage. From this it can clearly be seen that the devices which are expected to follow \( (V_G-V_T)^2 \) are fit much closer to \( (V_G-V_T)^3 \). Using this method, a threshold voltage of 0.55 V can be extracted as indicated on Figure 49 (a). In comparison to the conventional method, which would have yielded threshold voltages of 3 V, this method reproducibly determines where the device exits the subthreshold regime. This method has been used to calculate threshold voltages, although it is somewhat more tedious than conventional extraction methods. It does have significance, as it has been integrated into the AIMSpice level 15 model (amorphous silicon), which will be used in Chapter 5 to evaluate TFT circuit performance.
4.2 Output Conductance and Joule Heating

In thin film transistors of all sorts there are a variety of key parameters which dictate the performance in real digital and analog applications. Some parameters, such as field-effect mobility, garner large attention in new materials, but often more important is the related parameter, transconductance, \((g_m = dI_{DS}/dV_{GS})\). An often overlooked parameter in transistors made with new materials is the output conductance, \((g_d = dI_{DS}/dV_{DS})\). Both the transconductance and output conductance often set upper limits for many important applications such as amplifiers and microwave devices.

PEALD ZnO TFTs can have high transconductance; however, significant output conductance is observed particularly for short channel devices (<10 µm) with high output power \(P_{OUT} = I_{DS} \times V_{DS}\). In an ideal long channel MOSFET, the output conductance is effectively zero; however, as device dimensions are reduced, effects such as drain induced barrier (DIBL) lowering become important and result in short channel effects.

Figure 49 - (a) Typical PEALD ZnO TFT with vertical line indicating the extracted threshold voltage from the \(H(V_G)\) function. (b) \(H(V_G)\) as calculated from the integral of the drain current over the drain current. A straightline fit determines the threshold voltage and power, “m” which is > 3 instead of the ideal 2.
and significant output conductance.[56] As a result, for high performance ZnO TFTs, based on the fact that the output conductance was more significant in short channel devices, it was proposed that DIBL may be responsible.[90] However, for these and the vast-majority of published oxide TFTs, the channel length is more than 30 times longer than the gate oxide thickness, and short channel effect are expected to be small. Sentaurus [75], a two dimensional drift-diffusion based simulation tool, was used to model ZnO TFTs ($t_{ox} = 32$ nm, $\varepsilon_r = 8$) with varying channel length shows only small output conductance for channel lengths in the range typically reported (>1 $\mu$m) (see Figure 50). As a result, short channel effects cannot account for this abnormality in the reported oxide transistors.

![Simulated Short Channel Effects](image)

**Figure 50** - Sentaurus simulated short channel effects. The model used a dielectric thickness of 32 nm and a dielectric constant of 8. Doped contact regions were used to ensure contact effects did not contribute to the model. DIBL is observed for channel lengths much less than 1 micron.

Other thin film technologies, such as poly silicon, show significant output conductance even in long channel devices; however, the mechanism is not related to DIBL. Hot carrier-effects such as impact ionization at the drain side of the device result the “kink-
effect” which has significant implications on the range over which these devices can be used.[91, 92] However, the output conductance observed in oxide TFTs typically does not have the same shape and drain field dependence observed for poly-silicon TFTs.

Due to a large density of tail states amorphous silicon TFTs can show output conductance associated with self-heating which has been studied and included in some compact models.[93] However, due to various instabilities in all current applications amorphous silicon TFTs do not operate in a regime where the device power is high enough to lead to significant self-heating, so the effects have had minimal impact on real applications. To further disprove short channel effects and support self-heating, a plot of the output conductance as a function of output power for a variety of channel lengths for our PEALD ZnO devices is shown in Figure 51. It is obvious that the output conductance correlates well with device power and is nearly independent of channel length.
Self-heating in semiconductor devices is well known and has a critical impact on many technologies, including silicon-on-insulator (SOI) MOSFETs [94], gallium arsenide devices, and GaN LEDs. However, in the development of new low-cost electronics, the effects of self-heating have not been emphasized. This may be because the output powers required to significantly increase the temperature were not easily reached in stable devices, due to the low carrier mobility of most low-cost thin film materials. As a result, the applications which developed typically have very low output powers. However, the high performance of oxide thin film devices now presents possibilities for new high performance applications, but also considerably larger self-heating. These effects will be particularly important on low-cost substrates such as glass and plastic.

Figure 51 - \(\text{(a) Typical output characteristics for devices used in this work with 5 and 10 micron channel length (200 micron wide). (b) output conductance (dI_D/dV_D) plotted as a function of current density for a variety of channel lengths. The output conductance is correlated with input power and is very weakly a function of channel length, indicating that thermal and not short channel effects are dominant.}\)
where the thermal conductivity is orders of magnitude below the single crystal examples described above.

Figure 53 shows the typical output characteristics for a PEALD ZnO TFTs. Using pulsed gate measurements at modest duty cycles, it is possible to probe the effects of self-heating in the devices. The devices are measured by sourcing a constant drain voltage and measuring current as a function of time. The gate is then driven by a pulse generator and the drain currents are recorded. This technique requires that the drain sampling time be somewhat smaller than the gate pulse width restricting the minimum pulse width to > 5 μs. Luckily, Figure 52 shows that Joule-heating effects in the devices can be largely neglected for gate pulse widths < 100 μs, and steady state occurs for > 50 ms. In addition, it is found that there are minimal differences in Figure 52 as the duty cycle is increased from 1 to 20%. As a result for the measurement shown in Figure 53, a sweep is compared with a 10 μs pulse width and a duty cycle of 1.5%. It can be seen that where the output power is low for low gate voltages and/or low drain voltages, the DC and pulsed sweeps are identical. However, at larger gate voltages in the saturation regime, the output power increases linearly with \( V_{DS} \) and \( I_{DS} \) and differences arise between the pulsed and sweep data.
Figure 52 - Drain current for devices running in saturation as a function of gate voltage pulse width. It is found that the thermal time constant for heating is > 100 µs. In addition, for the devices measured, steady state Joule heating occurs >50 ms.

Figure 53 - (a) linear $I_D$ vs $V_{DS}$ output characteristics for several values of $V_{GS}$ for a typical PEALD ZnO TFT on glass $[W/L = 200/5 \, \mu m, t_{ox} = 32 \, nm, \varepsilon_r = 8]$ compared using a DC sweep versus a pulsed gate measurement ($10 \, \mu s$ pulse 1.5% duty cycle). (b) log ($I_D$) vs $V_{CS}$ for both linear ($V_{DS} = 0.5 \, V$) and saturation regimes ($V_{DS} = 8 \, V$) comparing DC sweep and pulsed measurements for the same device. Also the square root of $I_D$ is shown for saturation sweep showing similar threshold voltage but a difference in mobility.
In order to understand the cause of the current difference observed between the DC and pulsed measurements, as described in Chapter 3.7 the PEALD ZnO devices have been measured as a function of temperature. For self-heating modest temperature increases from room temperature are most important so carefully measurements (using a heat chuck and surface mounted thermocouple) over the temperature range from 30 °C to 130 °C were performed. Figure 54 shows the result of those measurements. As described before, a nearly linear shift in threshold voltage over that range is observed with associated charge coefficient of ~ $1.7 \pm 0.05 \text{nC/cm}^2\text{K}$. In addition, it is found that the mobility (at constant $V_G-V_T$) has small activation energy $\sim 5 \pm 0.4 \text{meV}$. Using the weak activation energy for the mobility and the linear shift in threshold voltage, it is found that over modest temperature deviations from room temperature ($\Delta T < 200$ degrees), about ~20% of the increase in current results from a increase in mobility while ~80% is related to a shift in threshold voltage. Therefore, a linear shift in threshold voltage shift is the primary mechanism, resulting in the change in current with temperature. Future work should emphasize understanding and controlling the threshold voltage shift with temperature.
After determining the temperature dependent behavior for the PEALD ZnO TFTs, the difference in current between the DC and pulsed measurements is used to estimate the change in device temperature as a function of output power. In order to calculate the temperature change, a carrier accumulation dependent mobility is first extracted assuming constant threshold voltage and square-law device. Then measured activation energy for mobility is applied to this function (5 meV/K). Combining this change with the linear shift in threshold voltage, the change in temperature associated with the difference in current is calculated. The generalized formula used is shown in Equation 6.

\[
\Delta I_d(T) = C_{ox} \frac{W}{2L} \mu \left( V_g, \Delta T \right) \left( V_o - V_T(\Delta T) \right)^2 \quad \text{Equation 6}
\]

Figure 55 shows the calculated linear relationship between output power and the change in temperature, indicating that Joule heating is indeed the mechanism responsible for the
output conductance in these devices. In addition, from this plot it is possible to extract a thermal resistance using the relationship, \( \Delta T = P_{IN} R_{TH} \), where \( P_{IN} \) is the product of \( I_D \) and \( V_D \). The thermal resistance for this device structure on glass substrates is found to be \(~7000 \pm 200 \text{ K/W}.\) This calculation demonstrates that modest output powers result in large surface temperature changes for typical devices on low thermal conductivity substrates.

![Graph showing temperature change vs. output power](image)

**Figure 55** - Calculated change in temperature as based on the current difference between the pulsed and DC sweep shown in Figure 2. The change in temperature is found to be linear with output power as expected with Joule-heating with thermal resistance of \(~7000 \pm 200 \text{ W/K}.\)

However, it is also extremely useful to have a simple model to evaluate the thermal resistance of the substrate without having to compare pulsed and DC data. A simple thick substrate spreading resistance model was used (\( R_{TH} = \rho/4a \)) with a circular area of radius 20 \( \mu \text{m} \) (roughly the same area as the device channel, 200 x 6 \( \mu \text{m} \) (channel length...
calculated as $5 \mu m + 2 \times \text{transfer length} = 0.5 \mu m$) and thermal resistivity of glass ($\rho$) 0.76 m·K/W. Using this equation, a spreading resistance of 9600 K/W is calculated which, considering the simplicity of the model, is similar to the result extracted from the experimental data. This model allows a simple evaluation of the temperature effects on various substrates. For example, while this thermal resistance is significantly higher than would be expected for a device on silicon substrate (96 K/W) is it smaller than would be expected for a device on a low-cost flexible substrate (100,000 K/W) whose thermal conductivity is one order of magnitude lower than glass. Using these calculated thermal resistances, it is straightforward to roughly estimate temperature changes on various substrates at a given output power and the resulting change in device current.

There are other significant consequences of the Joule heating in the measurement of thin film transistors. The majority of oxide transistors that have been reported have a distinct deviation from ideality in their characteristics. They typically do not follow the standard “square-law” behavior predicted for long channel MOSFETs.[56] One component of the non-“square-law” behavior appears to be a carrier mobility which is a function of carrier accumulation. There have been a variety of explanations for this effect including thinning of potential barriers at grain boundaries changing the path length.[22, 84] However, as the majority of oxide transistors are reported in the saturation regime, the effects of Joule heating should also be considered as a cause of non-ideality. Figure 53 (a) shows transfer characteristics for DC and gate pulsed (10 μs pulse, 1.5% duty cycle) in both the linear regime ($V_{DS} = 0.5$ V) and saturation regime ($V_{DS} = 8$ V). The field-
effect mobility is extracted using the relationships in the linear and saturation regimes as shown below.

\[ I_{\text{g, sat}} = \frac{W}{2L} C_{\text{ox}} \mu_s (V_G - V_T)^2 \]

\[ I_{\text{g, lin}} = \frac{W}{2L} C_{\text{ox}} \mu_s (V_G - V_T) V_{DS} \]

Equation 7

A straightline fit to the square-root of \( I_D \) vs \( V_G \) allows the calculation of mobility and threshold voltage. While the pulsed and DC sweep in the linear regime both have nearly identical characteristics and extracted field-effect mobility of 18 cm²/V·s, Joule heating in the saturation regime results in a difference. In saturation, while the two curves have a similar threshold voltage \( \sim 1.5 \) V, the extracted mobility of the DC sweep is 25.5 cm²/V·s versus 16.5 cm²/V·s for the pulsed measurement. Based on the change in transconductance between pulsed and DC sweep in Figure 53 (top), this overestimation of field-effect mobility is expected to continue to grow as the drain voltage is increased. Using the thermal resistance calculated from the experimental data and output power, we find that the device temperature is expected to be \( > 200 \) °C and thus, an overestimation in extracted field-effect mobility of \( > 50\% \) is found. As many of the published oxide devices are measured with output powers \( > 100 \) mW/mm, it is expected that the local temperatures are large enough to result in significant overestimation of field-effect mobility. This overestimation will depend on the current changes with output power which will vary from one material to another depending on the mobility and threshold voltage temperature activation as well as many device parameters such as oxide thickness, device width, et cetera. Therefore, it is necessary to report the linear regime mobility where output powers are \( < 1 \) mW/mm and self-heating effects can be neglected. Additionally,
as devices move to low-cost plastic substrates this effect is expected to be exaggerated
and the maximum output powers will need to be further reduced to evaluate performance.

The next substantial impact that Joule-heating has on these ZnO TFTs is that it is
responsible for a thermal runaway breakdown mechanism. Because the mobility and
threshold voltage both result in increases in current, a feedback loop of heating and
increasing current ultimately leads to catastrophic breakdown. Figure 56 shows a
simple table of thermal conductivities for various materials and a graph of the power that
results in catastrophic breakdown (short between gate and source or gate and drain) on
various substrates. The devices on each substrate are biased at a voltage below
instantaneous thermal breakdown (~10%), and then as the device temperature increases
the power (I_DS x V_DS) of breakdown is noted. This measurement is repeated more than 10
times at various combinations of gate and drain voltages to arrive at the values in Figure
56 (a). The power to breakdown is strongly dependent on the substrate thermal
conductivity. Using the thermal resistance extracted from the glass sample (~7000 W/K),
the temperature of breakdown can be estimated and should be > 300°C at 225 mW/mm.
The linearity of Figure 56 (b) suggests that the temperature of thermal runaway is similar
on various substrates and may suggest that charge to breakdown in the Al₂O₃ dielectric as
shown in Figure 19 (b) is responsible. This is another reason that future development of
SiO₂ or HfO₂ dielectrics may increase the stable performance of these oxide TFTs.
It is also notable that the maximum output power on crystalline silicon substrates is two orders of magnitude higher than that on flexible polyimide. As a result, while it is possible to reach very large current densities (> 500 mA/mm) and high performance in oxide devices, this is also related to very large power densities and subsequent self-heating. It is therefore unlikely to be possible to achieve such results on low-cost substrates without significantly managing the thermal effects. As a simple example of significantly changing the thermal sinking characteristics, Cu-coated polyimide was used as a substrate. Figure 56 shows that more than an order of magnitude improvement in power to breakdown was observed compared to polyimide alone. However, the

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**Figure 56** - (a) Table 1 of output power where thermal runaway results in breakdown (device gate and either source or drain is shorted together and dark bubbles observed on device) on various substrates (device width = 200 μm) [*the thermal conductivities were evaluated using COMSOL multiphysics to roughly account for insulating layers and changes in thermal conductivity over the temperature range from 20-300 °C*] (b) Graph of power to breakdown as a function of substrate thermal conductivity. A linear relationship implies that the temperature at breakdown is similar on the different substrates.
additional parasitic capacitances means that further work to specifically design structures to sink heat on flexible substrates will be important.

In addition to structures which sink heat from devices, thermal management of high performance thin film circuits on low cost substrates will require design rules which consider thermal effects. For example, the thermal effects are dependent on many device parameters including the thermal conductivities and thickness of the substrate, gate metals, and source drain metals. By using highly thermally conducting gate and source drain metals of reasonable thickness, we have estimated experimentally and using finite element models (based in COMSOL Multiphysics[53]) improvements of approximately a factor of two by using moderately thick (300 nm) thermally conducting gates and source drain materials. Figure 57 shows the impact of the thermal conductivity of contact and gate metals. Approximately a 40% improvement is seen by replacing titanium contacts (22 W/mK) with aluminum contacts (235 W/mK), or by changing the chrome gate (94 W/mK) to gold (320 W/mK). In addition, thermal spreading is very dependent on the width of the transistor. Additionally, through experiment (see Figure 57), and by finite element modeling it is found that the local temperature decreases by a factor of two to three for the same output power as the device width is scaled from 200 μm to 5 μm (however only modest differences are expected at device widths > 1 mm). This means that narrow devices will be necessary to increase the power to breakdown and reduce the device output conductance.
Finally, while this work and most of the published reports on oxide TFTs are fabricated with thin gate dielectrics (32 nm of PEALD Al₂O₃ here), in some applications, the gate dielectric thickness may need to be as much as an order of magnitude thicker to ensure satisfactory yield. Assuming a fixed channel length (reasonable due to low cost lithographic tolerances), threshold voltage near 0V, and a constant current density, the output power in saturation increases as the square root of the change in oxide thickness. So for an order of magnitude increase in oxide thickness, the output power would increase by ~3x for the same current density.[56] Therefore, the aforementioned self-heating effects occur at considerably lower current densities with thicker dielectrics.

To this point, the discussion has focused on thermal effects and output conductance for PEALD ZnO TFTs. Interestingly, Figure 58 shows the output conductance for a variety...
of oxide semiconductor thin film transistors on glass and silicon substrates.[16, 38, 67, 90, 95] The devices were fit with a second order polynomial, which is roughly expected for self-heating in the saturation regime. The devices shown here were intentionally chosen from reports where the device stability was shown to be very good on the scale of the device sweep to eliminate the effects of current bias stress. It is notable that across a selection of devices from several different oxide materials (ZnO and amorphous IGZO) all show a correlation between output power and output conductance. [16, 38, 67, 90, 95] This suggests that changes in device current with increasing temperature are a more general problem which extends across many amorphous and crystalline oxide semiconductors. Figure 58 also clearly shows that devices on silicon substrates show considerably lower output conductance at comparable output powers because of the higher thermal conductivity compared to glass.
The apparent general dependence on temperature for oxide semiconductors is somewhat expected. In oxide semiconductors, the temperature dependence of the mobility is considerably smaller than other low temperature thin film materials, such as organic semiconductors and amorphous silicon. Because the conduction band minimum in most oxide semiconductors is formed by unfilled s-orbitals around heavy metal cations the symmetry allows for these materials to be significantly less sensitive to order.[9] These spherical s-orbitals are not significantly perturbed by disorder, and for that reason, the electron mobility for amorphous oxides such as indium-gallium-zinc oxide (a-IGZO) can be nearly as high as their crystalline counterparts (c-IGZO). Amorphous IGZO has been

Figure 58 - Output conductance \( (dI_D/dV_D) \) for a variety of oxide TFTs (\[*[16,38],**[67,90],***[95]\]) on glass and silicon substrates (Si/100 nm SiO\(_2\)) as a function of device power. The data is fit using a second order polynomial which is roughly expected for self-heating in the saturation regime.
previously reported to have a Hall mobility which is very weakly dependent on temperature for high carrier concentration films and a significantly more activated mobility for lightly doped films.[9] This was explained using a percolation model where small barriers above the mobility edge lead to differences in path length with temperature.[9] However, because the self-heating effects described here are primarily expected to occur in strong accumulation, the change in carrier mobility is expected to contribute only a relatively small component of the change in current with temperature.

The more significant portion of the current increase with temperature is a negative shift in device threshold voltage. A reversible temperature dependent shift in the threshold voltage may arise for a number of possible reasons including pyroelectric charge or defect generation. The materials shown in Figure 58 include (002) textured ZnO films deposited by PLD at high temperature[90] and by PEALD at low temperature (this work). While not fully understood in these devices, ZnO is a non-centrosymmetric crystal structure and may show pyroelectric effects with single crystal pyroelectric coefficient of $9.4 \mu \text{C/m}^2\cdot\text{K}$. Pyroelectric charge generated in the ZnO layer would result in a threshold voltage shift with temperature. It is notable that the threshold voltage shifts with temperature in the PEALD devices of this work are both highly linear and rapidly reversible. However, the polarity of the ZnO grains is not known and therefore it is unclear whether pyroelectric charge should be observed. Direct measurements of the piezoelectric and pyroelectric charge will be essential to elucidate the nature of this charge. In comparison, Figure 58 also shows ZnO devices deposited using spatial ALD which have a mixture of (100), (101), and (002) orientations at 200 °C.[38] While the
change in texture of these films may be expected to have a significant reduction in the effects of pyroelectric charge in the devices, only a modest change in thermally induced output conductance is observed. However, amorphous oxides such as indium-gallium-zinc oxide (IGZO) which are expected to have negligible pyroelectric charge have also been reported to have a shift in threshold voltage with temperature.[97, 98]

The shift in threshold voltage with temperature in these amorphous oxides has been attributed to defect generation in the a-IGZO layer or at the dielectric-semiconductor interface resulting in a reversible threshold voltage shift with long temperature dependent recovery time constants. This defect generation may be the cause of the output conductance shown for the a-IGZO device shown in Figure 58. However, this would then imply that the devices would have irreversible shifts after sweeps to high power. There are other potential effects that may occur as a function of temperature and shift the threshold voltage, such as charge injection into the dielectric layer; however, this effect is not expected to be fully reversible as experimentally observed.

To further increase the performance of low-cost electronics and in particular high performance oxide electronics, an emphasis on improvements which directly reduce thermal effects are necessary. By thoroughly understanding the mechanisms that result in threshold voltage and mobility changes, it may be possible to tune these effects to become nearly temperature independent. Recently, work on unique passivation schemes and different amorphous oxides such as Al-Sn-Zn-In-O has demonstrated a significant reduction in threshold voltage changes with temperature.[99] Additionally, processes
such as self-aligned-gate [100, 101], which improves circuit performance without increasing the power is particularly interesting. In addition, using CMOS technologies where the power is inherently lower and the peak supply current times are often very short during switching minimizing thermal effects. In Chapter 5.9, an example of hybrid CMOS will be described and while many groups have shown similar CMOS demonstrations [102, 103], much work still needs to be done in particular towards the development of new materials for p-channel transistors in order to enable high performance circuits on low-cost substrates.

4.3 Contacts

It is well known that parasitic resistances, such as contact resistance, substantially reduce the overall performance of many electronic devices including metal oxide TFTs. In the simplest model, a fixed resistance at the source and drain adds in series with the channel resistance. Generally, both the contact and channel resistance are a function of gate electric field; however, the channel resistance is directly correlated to the channel length where the contact resistance is independent of channel length. Therefore, devices with very low channel resistances (high mobility, short channel length) require low absolute contact resistances to ensure minimal contact impact.

For conventional semiconductors, including both single crystal and amorphous silicon, as well as GaAs, GaN, and SiC, ohmic contacts are most often formed using heavily doped semiconductor regions at metal-semiconductor interfaces. Heavy doping reduces the Schottky barrier depletion layer thickness sufficiently that carrier tunneling provides low-
resistance ohmic contacts, even for significant contact barrier heights. However, the oxide semiconductor devices described so far have not used intentional doping to help form ohmic contacts. Instead, metal electrodes (titanium or aluminum) directly contact semiconductor regions with low doping and may result in non-ohmic contacts. This section will describe commonly used approaches to reduce the contact resistance, as well as the impact of non-ohmic contacts on the TFT characteristics. In particular, the extraction of many parameters used to evaluate device performance, including mobility, threshold voltage, and subthreshold slope, can be affected by the nature of the contacts.

4.3.1 Contact Doping
As mentioned above, the use of intentionally doped ZnO to form ohmic contacts is an obvious choice. While it is very easy to form ZnO with carrier concentrations $>10^{19}/\text{cm}^3$ by intentional or unintentional doping, challenges with doping stability and integration have resulted in limited demonstrations. Attempts to use doped ZnO (both boron doped by PECVD [30] and aluminum doped by SALD) as top and bottom contacts yielded specific contact resistivity in the range of $10^{-4} \, \Omega \cdot \text{cm}^2$ (see Figure 59), worse than the best metal-ZnO contacts. These doped layers are fairly unstable and short anneals at low temperature (1 min at 200 °C) can create large changes in resistivity (more than a factor of 2). This may suggest that the ZnO-doped ZnO interface does not retain the high doping estimated from Hall-effect measurements. In addition, there is a lack of significant etch selectivity between doped and undoped material, making fabrication of structures more complicated. One approach would be to use an etch stop layer; however, as described in section 3.5 the passivation of ZnO is a challenge and still requires etch
selectivity (e.g. fluorine based chemistry to etch SiO₂). As a result of these challenges, most of the effort has been devoted to forming reasonable quality metal-ZnO contacts.

Processes have been developed to improve the metal-ZnO contacts. The primary approach employs a plasma treatment (oxygen, hydrogen, or argon) to dope or generate defects (and thus increase the free carrier concentration) beneath the source and drain regions of the device. [57, 58, 69, 104, 105] This process has also been employed to form self-aligned oxide TFTs; however, the parasitic resistances still significantly reduce the device performance. [72, 106] In this work, during device fabrication most TFTs source and drain regions were exposed to a short oxygen plasma (1 min RIE, 100W, DC bias: -100V) directly before metallization. This process was experimentally found to reliably reduce the specific contact resistivity (determined from transmission line measurements) from 10⁻³ Ω·cm² to 10⁻⁴ to 10⁻⁵ Ω·cm². This reduction in contact resistance increased the short channel length mobility as expected, which is highly desirable for fast circuits.

Figure 59 – Comparison of Al-SALD ZnO contacts and ZnO:B (PECVD)-SALD ZnO. (a) Al source drain contacts with oxygen plasma have specific contact resistivity 10⁻⁵ Ω·cm². (b) Doped ZnO contacts have specific contact resistivity >10⁻⁴ W/cm² and lower field effect mobility.
The use of various plasma treatments has been explored to improve the contacts to ZnO TFTs from both PEALD and SALD. One particular approach investigated was the use of a high energy argon ion beam (1 kV) to etch the surface and increase the free carrier concentration.[57] Hall measurements on SALD ZnO surfaces etched only 10-20 nm showed a decrease in sheet resistance from (>10^8 Ω/sq) to (7x10^3 Ω/sq). This change in sheet resistance came presumably from a large increase in sheet carrier concentration to 7 x 10^{13} /cm^2 with mobility of 10-15 cm^2/V·s. In comparison, PEALD ZnO has shown significantly lower sheet resistances (2x10^3 Ω/sq) with considerably higher mobility (40 cm^2/V·s) and sheet concentration (1x10^{14} /cm^3). Figure 60 shows the process flow for integrating this surface etching into the contacts for thin film transistors. The process is very similar to a conventional lift-off; however, before metallization a high energy ion beam etches the surface. The ZnO film was typically etched between 10 to 50 nm. As a result, the total film thickness for these etched contact samples was typically somewhat higher (80-100 nm).

A Monte Carlo simulation of ion impact on the surface of ZnO (stochiometry 1:1 density 5.606 g/cm assumed) with 1 kV Ar ion energy at 45° incident angle showed a penetration depth of ~ 5 nm into the ZnO film. This explains why, experimentally, a nearly constant sheet resistance is observed with etch time until the film thickness become < 10 nm. If we assume that the defects are generated uniformly through the top 5 nm that would result in a carrier concentration of >10^{20}/cm^3 based on the sheet concentration measured using the Hall-Effect. This should be more than high enough to create a fully tunnelable
thinned doped contact region for both SALD and PEALD. It is worth noting that the following discussion will be restricted to SALD primarily because metal contacts to PEALD devices form specific contact resistivity $<10^{-4} \ \Omega/\text{cm}$ and only modest reductions were observed with contact etching. In comparison, SALD devices with contact etching often had contact resistivity of $>10^{-3} \ \Omega/\text{cm}$.

Using this simple process to induce large sheet concentrations beneath the contacts SALD devices were fabricated with improved performance. Figure 61 (a) shows the result for contact etching on the performance of a relatively short channel device (5 μm). It is clear that the contact etched device has considerably higher mobility (8 cm$^2$/V·s for unetched, 15 cm$^2$/V·s for etched). This higher extracted mobility comes from a reduction

\begin{figure}[h]
\centering
\includegraphics[width=\textwidth]{argon_etch.png}
\caption{Process flow for argon ion beam etched contacts. A double layer resist pattern is used to etch only the contact regions of the device. Then metal is evaporated/sputtered and lifted off. Finally the devices are electrically isolated by patterning the ZnO layer.}
\end{figure}
in parasitic contact resistance. Figure 61 (b) shows that using transmission line measurements, an improvement in specific contact resistivity of more than two orders of magnitude is achieved by contact etching (from $2 \times 10^{-3} \ \Omega/cm^2$ to $1 \times 10^{-5} \ \Omega/cm^2$). While this is a very significant improvement, a major concern with this process is stability. The defects created during the etching process are not highly stable. For instance, a short anneal (1 min, 180 °C) in air completely removes measurable surface conductivity for these SALD films. The rate of this change is very different than that observed for PEALD (<2x increase for this anneal) and other SALD films; however, a careful correlation to understand the mechanism has not been carried out. It is clear that nearly all ZnO films with surface defects do show an increase in sheet resistance as a function of annealing time and temperature (from Hall-Effect this is related to decreases in both sheet concentration and mobility).

The stability of these contact improvements has been investigated. Figure 61 (b) shows that in air over the course of months almost no change was observed (in comparison, the sheet resistance of an etched surface exposed to air would increase by orders of magnitude over that time frame). This difference in stability can be explained because the etched surface of the device has a metal deposited which appears to stabilize the defects. However, even with the contact metal in place an anneal at 200 °C for 10 min increased the specific contact resistivity of both the etched and unetched devices. Ultimately, this process demonstrated a straightforward approach to minimizing the contact resistance for devices where metal alone made a poor contact. However, even after the contact etching, the contact resistance was $1.5 \ \Omega \cdot cm$ and the transfer length was
still ~ 200 nm and for applications with short channels and self-aligned contacts (see section 5.6) a significant parasitic resistance is still observed. In addition, the change with annealing puts significant constraints on the thermal budget for subsequent processing (e.g. passivation).

4.3.2 Gated Contact TFTs

The contact discussion described above demonstrated that even without doped contacts the use of plasmas to treat the contact interface was sufficient for reasonable contacts to typical ZnO TFTs described in this work. However, as the device performance increases (mobility increases, channel length decreases) the channel resistance will decreases putting a premium on high quality ohmic contacts. Several reports of high performance devices have used contact metallization schemes such as Ti/Au (annealed at >300 °C) to achieved specific contact resistivity $<10^{-5}$ Ω/cm² [16, 90, 107]; however, we have not achieved this low of values using similar contact schemes. It is interesting to note that many of the high mobility devices published make no mention of contact resistivity. The

Figure 61 - SALD device results for contact etching with Ar-ion beam. (a) log ($I_D$) and sqrt ($I_D$) versus $V_G$ for transverse head SALD device with W/L = 200/5 μm. The contact resistance is decreased by 2 orders of magnitude and the mobility is increased from 8 to 15 cm²/V·s. (b) Specific contact resistivity as a function of time in air and on a hot plate at 160 and 200 °C. The difference between etched and non-etched contacts is relatively well maintained over time and annealing.
following discussion will describe several cases where extremely high field-effect mobility is extracted but is not likely connected to real transport in these materials. This discussion will also provide a foundation to qualify many non-ideal devices such as organic transistors, where non-ohmic contacts are nearly ubiquitous.

Figure 62 shows the effect of a 15 min hydrogen plasma treatment (~0.05 W/cm²) on PEALD ZnO TFT (unpassivated devices with silicon substrate, 45 nm thermal oxide dielectric, and aluminum contacts. ZnO deposited using N₂O plasma in the large ring-fed system). There are two notable changes induced by the plasma treatment from the as-deposited devices. First, there is a large threshold voltage shift associated with doping the ZnO layer (> 50 V, >2.5 x 10¹³ / cm²). As described in the passivation section (section 3.5), this is not a large surprise. The role of hydrogen doping and/or reduction of the ZnO is known to lead to large increases in carrier concentration and resistivity in the <10⁻³ to 10⁻² ohm-cm.[108, 109] The second is a large increase in transconductance which results in peak differential mobility >200 cm²/Vs compared to ~8 cm²/Vs as deposited. However, the high mobility and increased carrier concentration is unstable and can be removed with a 2 minute bake in air at 200 °C. This instability makes even straightforward electrical characterization such as Hall-effect measurements challenging. As with other conducting films, it was found that that both the mobility and carrier concentration decrease with time. One possible explanation for the high mobility in hydrogen plasma treated devices is that the plasma induces an increase in carrier concentration. This increased carrier concentration minimizes the effect of grain boundaries or other defects responsible for the low as-deposited field-effect mobility.
The degradation in carrier concentration and mobility from Hall measurements seem consistent with field-effect measurements on H₂ plasma treated devices. Figure 62 shows that after 3 days in air the threshold voltage has shifted +20V (reduction in carrier concentration) and the peak mobility has decreased. The combination of a large threshold voltage shift (resulting in depletion mode transistors) and instability make this phenomenon very interesting but impractical for real device application. In addition, the device shown Figure 62 is the most substantial mobility improvement with H₂ plasma treatment. The variability from sample to sample was quite large with some PEALD and all spatial ALD samples showing large shifts in threshold voltage with little to no improvement in mobility. While the carrier concentration dependent mobility and grain boundary modulation may be a component of the problem, another explanation exists. If a Schottky-gated contact allowed the device to be turned off at the contact edge without fully depleting the channel, the device threshold voltage extracted would be completely incorrect. As this section proceeds, the distinct peak in differential mobility where the device turns on suggests that gated-contacts are responsible for the apparent increase in performance.
TCAD Sentaurus [75] has been used to model the potential impact of a gated contact. TCAD Sentaurus is a two dimensional drift diffusion modeling tool that is particularly well suited to study these effects because it includes non-local tunneling which is essential to modeling the behavior of Schottky contacts. Figure 63 (a) shows a schematic of the model used to simulate these staggered inverted ZnO TFTs. In the model a thin channel region (10 nm) of the device was lightly doped (5x10^{14} /cm^3). To model the impact of doping at the back interface (from hydrogen plasma treatment or passivation as will be described next), a 2.5 nm thick layer doped 10^{20} /cm^3 was inserted (same 2.5x10^{13} /cm^2 estimated from H_2 plasma treatment). The model used a 0.6 eV barrier at both the source and drain contacts. In addition, a constant mobility of 30 cm^2/V·s was defined in the ZnO material. Figure 63 (b,c) show device characteristics from the simulation. The first and most notable characteristic observed is a significant overshoot in differential mobility to 130 cm^2/V·s (more than 4x the defined constant material mobility). This overshoot in mobility continues well into strong accumulation and at V_{G-V_T} = 10 V the
mobility is still 50 cm$^2$/V$\cdot$s. The turn on for the device is also unexpected. From section 3.5, a relationship was developed to understand how the channel should deplete given the back channel charge and the series capacitance of the oxide and ZnO layer. If that model is applied to this simulation (50 nm Al$_2$O$_3$ with $\varepsilon_r = 8$, in series with 7.5 nm ZnO with $\varepsilon_r = 9.5$ and sheet charge of $2.5\times10^{13}$/cm$^2$), it is found that the device should have a $V_{ON}$ shift of $\sim 32$ V. However, only approximately 5 – 10 V of shift (calculated from zero barrier case not shown) is actually observed. This difference can be directly attributed to the large contact barrier. One way to view the device is effectively a very short channel at the source side of the device. At very high accumulation fields, the barrier becomes more and more transmissive, and the channel contribution becomes significant as the differential mobility approaches the defined material mobility. This overestimation of mobility is very counter intuitive as typically as non-ideal contacts are typically thought of a mechanism to reduce extracted mobility (e.g. non-plasma treated vs. plasma treated contacts described earlier in this section). Figure 63 (c) also shows that the output characteristics for the device are also non-ideal with considerable curvature at low $V_{DS}$ and poor saturation at high $V_{DS}$. This model explains relatively well the hydrogen plasma treated devices, particularly given that the peak mobility is sharp and a shift in turn on voltage was observed in both experiment and model. However, as will be described in the next section, neither of these appears to be fundamental and further modeling is needed to understand the key parameters which dictate this overshoot peak and width.
Other ways to unintentionally form these Schottky-gated diodes that do not involve the large shift in threshold voltage or the instability associated with the hydrogen treatment have also been found. As mentioned in the passivation section, there have been reports that for amorphous IGZO N$_2$O plasma treatments before the passivation can minimize the threshold voltage shift.[18] As a result, a N$_2$O plasma was used to form Al$_2$O$_3$ as a passivation material. Very interesting results were found. As mentioned in section 3.2.1, Al$_2$O$_3$ grown with N$_2$O is expected to have different physical and electrical properties, which may interact with the ZnO layer. Figure 64 shows the resulting devices after N$_2$O Al$_2$O$_3$ passivation. The device shown has exceptionally high mobility at very low voltage, and a very different shape to the differential mobility curve than observed before passivation. Similar to the model described above, a sharp peak in differential mobility (> 70 cm$^2$/V·s) is observed as the device turns on and then the mobility slowly tapers off but still remains > 40 cm$^2$/V·s even at large accumulation. Figure 64 (b) shows the less...
ideal output characteristics as the devices do not fully saturate as expected, but still a large signal mobility of > 50 cm²/V·s can be extracted assuming a threshold voltage near 0 V. Self-heating (as described in section 4.2) can be ruled out because the output conductance occurs at substantially lower output powers, and the temperature dependence of these devices is similar or less than without N₂O passivation. One of the most interesting characteristics of these devices is that while hydrogen plasma treatment or normal passivation back channel doping result in large threshold voltage shifts the turn on voltage for the N₂O passivated and unpassivated devices can be nearly the same. Figure 64 does show both a very interesting and promising device, however, it is important to note that this device behaves more like a conventional MOSFET in terms its square-law nature than most devices described earlier in this text. Issues with uniformity and reproducibility were common and while high mobility was always observed (> 200 cm²/V·s in some cases), the turn on voltage near 0 V and the smooth subthreshold slopes were not ubiquitous. It was also very common to observe a drain voltage dependent turn-on voltage and significantly more output conductance than shown here. These gated-contact devices also have many characteristics of very short channel MOSFETs and do not scale with channel length as would be expected for long channel MOSFETs. Therefore, the utility of these devices in many real applications is questionable. Overall, these devices demonstrate that it is possible to extract non-meaningful mobility values from devices with non-ohmic contacts. It also demonstrates that a large barrier can skew the meaning of threshold voltage and subthreshold slope. In the final discussion on contacts, a test structure to understand some of these effects will be introduced and preliminary results will be discussed.
4.3.3 Independent Contact Gate TFTs

In the examples described above, it is clear that the lack of reliable heavily doped contacts in these devices can lead to significant device misinterpretations. However, it is notable that at the largest accumulations (>10^{13} \text{ /cm}^2) in most of the devices described the specific contact resistivity was quite small (10^{-5} \text{ \Omega \cdot cm}^2). Therefore, for many of the devices described, it would be beneficial to accumulate carriers in the contact regions independently of the channel. These regions would effectively produce the same effect as doped contacts, but might be significantly easier to process. The structure developed to independently gate the contacts is shown in Figure 65. The structure is very simple and started by using a blanket gate layer (or patterned) and coating it with dielectric. The second gate layer is then deposited and patterned beneath the source and drain. A second dielectric layer and the ZnO layer are deposited in situ and the remainder of the process is the same as described. The electric field from the blanket gate is shielded by the metal contact allowing both the channel and contacts of the device to be gated independently.

\begin{figure}[h]
\centering
\includegraphics[width=\textwidth]{fig64.png}
\caption{(a) log (I DS) and differential mobility versus gate voltage in the linear and saturation regime for 10 nm ZnO layer passivated with N_{2}O based Al_{2}O_{3} resulting in gated-diode ZnO TFTs. (b) linear I DS versus V DS for the same TFT in (a). The significant output conductance in these devices is not from self-heating but rather from the gated contact.}
\end{figure}
The only drawback to this structure is that the dielectric layer has an additional interface introduced for the second gate.

![Figure 65](image)

**Figure 65** - (a) Schematic of double gated structure. (b) Cross-section of fabricated double gated structure. Glass and a blanket layer of chrome act as the channel gate. Pd is used as the contact gate.

Figure 66 shows initial results for the independent contact gating structure. Figure 66 (a) shows a device as the constant contact electric field is increased from 0 MV/cm to 3.75 MV/cm and the channel gate is swept from -1.25 MV/cm to 2.5 MV/cm. It is notable that the subthreshold slope is significantly higher for these devices than expected for typical devices. In addition, as expected the device mobility is a strong function of the accumulation beneath the contact regions. As a result, when the contact field is greater than the channel electric field, modest improvements in mobility are observed. This is consistent with the low specific contact resistivity measured at large accumulations.

Figure 66 (b) shows how the contacts can significantly impact the threshold voltage and subthreshold slope. The two lines show two different constant contact fields as in Figure 66 (a). The line with symbols is for the contact electric field equal to the channel electric field. This is how typical oxide TFTs. Surprisingly, the large hump in the subthreshold region of the device is completely removed (giving rise to \(\sim 3\) V difference in \(V_{ON}\)) and the subthreshold slope is improved. In addition, the threshold voltage is shifted by \(\sim 1\) V positive. This result suggests that the subthreshold region of the device characteristics is
not governed by diffusion current, but rather by contact turn on. This suggests that to a
degree, the contact gating that gave rise to an overestimate in mobility in the last section
is present in most of the PEALD devices. It also means conventional ways of evaluating
traps such as comparing the subthreshold slope to trap free values are not meaningful. It
also may explain the reason that the subthreshold slope increases at low temperature as
seen in Figure 41 (a). In particular, the contact resistance in strong accumulation was
found to be nearly temperature independent at temperatures < 150 K (see Figure 42).
However, in the subthreshold regime, it seems that modest barriers at the contacts may be
dictating the device characteristics.

Overall, forming high quality contacts to oxide TFTs presents technological challenges.
In particular, in this section contact non-idealities were described which lead to both
overestimation and underestimation of mobility. This fundamentally limits the
understanding and development of these new materials. Several methods, including plasma treatment of the contact regions and independently gating the contact regions, were shown to significantly reduce these effects. However, ultimately, stable doped contact integration should be developed to eliminate these effects all together.
Chapter 5
Thin Film Transistor Circuits

5.1 Background

To this point, this work has focused on the use of low-temperature processes to fabricate oxide thin film and devices. These devices are particularly interesting as pixel switches in large-area and especially OLED displays due to their high mobility and improved stability compared to other low-temperature devices such as a-Si:H and organic thin film transistors (TFTs). However, the application of oxide-based TFTs is not limited to simple switches, and the relatively high performance allows integration of thin-film analog and digital circuits as well as possibly microwave devices.[90] Recently, indium-gallium-zinc oxide ring oscillator circuits on silicon substrates with 0.5 μm channel length and 0.5 μm source-gate and source-drain overlap) were reported to operate at ~7 ns/stage with a saturated-load inverter design, and < 1 ns/stage with a novel bootstrapped inverter design.[110] In addition, high temperature ZnO TFTs (400 - 600 °C) deposited by pulsed laser deposition have shown high field-effect mobility >100 cm²/V·s, maximum channel current density >400mA/mm and interesting microwave performance with \( f_T = 2.45 \text{ MHz} \) and \( f_{\text{max}} = 7.45 \text{ MHz} \) on high resistivity Si wafers.[90] However, both of these recent demonstrations of high performance used high performance lithography with small alignment tolerances and single crystal silicon substrates.

In order to form low-cost circuits which are integrated with arrays, large area substrates such as glass or flexible materials are necessary. There has also been considerable interest in integrating the row and column drivers for AMOLED displays onto the same
backplane as the pixel switches. This requires a relatively high performance circuit technology. 3M was able to demonstrate ring oscillators on polyethylene naphthalate (PEN) substrates operating at 1.4 μs/stage at 40V, as well as fully operational 16 shift registers using a roll-to-roll process.[111] The slow speed is largely related to large parasitic capacitances which will be discussed in detail throughout this chapter. Very recently, transparent sputtered IGZO circuits were demonstrated with propagation delay of <48 ns/stage at 25 V.[112] Additionally, a half-bit shift register formed with sputtered amorphous IGZO TFTs was demonstrated at 40 kHz [113], and a variety of other circuits including DC:DC converters [114], and AC:DC converters have also been demonstrated [115]. Throughout this chapter, the development of thin film circuits on glass and flexible substrates will be described. These substrates present different challenges both with yield as well as thermal spreading. These circuit demonstrations served to both identify functionality for real application as well as confirm the lack of a large number of slow interface states in these ZnO devices. The chapter will describe a range of ZnO all-NMOS circuits from various techniques and how design impacts the performance of thin film circuits. A short discussion of thermal effects will be used to identify CMOS as an important building block for many future applications. The chapter will conclude with a discussion of initial work to integrate ZnO and organic materials to form simple high performance CMOS circuits.

5.2 Circuit Design, Layout, and Fabrication

Circuit fabrication was very similar to the process described in the Chapter 3. A 100 nm thick chromium gate layer was deposited by ion-beam sputtering on borosilicate glass.
The Al₂O₃ and ZnO layers were then deposited and patterned by photolithography and wet etching in H₃PO₄ (80 °C) and dilute HCl, respectively. 150 nm thick titanium (or aluminum) source and drain contacts were then deposited by sputtering (aluminum was evaporated) and patterned by photolithography and lift-off. Most circuits were not passivated, but several PEALD circuits had a 30 nm layer of ALD Al₂O₃ deposited from trimethylaluminum and H₂O at 200 °C.

In order to design and layout simple thin film transistor circuits, parameters for AIMSpice [116], a simple compact modeling tool have been extracted. The extraction procedure is somewhat cumbersome and parameters were determined primarily by trial and error. The model used was level 15 and was designed to model the characteristics of amorphous silicon TFTs. This model contains several characteristics which are very helpful in fitting ZnO TFTs. The mobility in amorphous silicon is a function of the Fermi level (and therefore gate voltage) and therefore a variable exponential (gamma parameter) for the gate voltage term is defined to fit this change.[88] During the extraction of these model parameters, there are some physical constants, such as device dimensions (W, L, tox), and easily measurable quantities, such as dielectric constants (eps, epsi), threshold voltage shift with temperature (kvt), and contact resistances (rd, rs), which are maintained at reasonable values. The rest of the parameters are varied to accurately fit the experimental data. An example can be seen in Figure 67. Typical extracted parameters are also seen in Table 3. This model is roughly correct as the channel length and width of the devices is varied, minus the thermal effects described in
Chapter 4. However, if the dielectric thickness is changed, the values for $v_{to}$ and $v_{fb}$ need to be adjusted accordingly.

Ring oscillators were selected for simple circuit demonstration. A ring oscillator is an odd number of inverters connected in series, to test the dynamic performance of our devices and demonstrate simple circuit functionality. The basic parameters of interest for designing ring oscillators including beta ratio, channel length, and overlap capacitance were examined. The beta ratio ($\beta$) is the geometric ratio of the unit inverter drive...
transistor to the load transistor ($\beta = (W/L)_{\text{drive}}/(W/L)_{\text{load}}$). The gain of an all-enhancement
mode inverter is ideally equal to the square root of the beta ratio for ideal devices, so for
real circuits, a beta ratio of $> 5$ is typically necessary. Figure 68 shows the simulated
changes in frequency as a function of beta ratio. For a 2x reduction in beta ratio
approximately a factor of 0.8 x increase in speed is observed. Similarly, Figure 68 shows
that scaling the channel length, device mobility, and overlap by 2x results in speed
increase of ~ 2.4x, 2x, and 1.2x respectively. Therefore, the experimental ring oscillators
had a variety of designs, but in the faster circuits had smaller beta ratios, high mobility
short channel devices with small overlaps. The overlap reduction will be described in
more detail in section 5.6 during a discussion of gate-self-aligned circuits.
The compact modeling described above used simple parameters which could be varied to increase speed. The final consideration was related to thermal effects in these circuits. As described in Chapter 4, thermal effects play a significant role in the maximum performance that can be reached on low-thermal conductivity substrates. LEdit was used to layout a variety of masks.[117] Figure 1 shows several different designs that have been used in the following circuit work. In the original design, a 7 inverter plus one
output stage loop was used. The device widths and the spacing between the unit inverters were relatively large. In the second design, much smaller widths were employed for the same beta ratio. As described in Chapter 4, for the same current density this results in better thermal spreading and considerably higher maximum current densities. These smaller inverters were surrounded by large metal bus lines which may also help to spread the heat. The smaller widths also resulted in a more compact design (original design used \( \sim 0.03 \, \text{cm}^2 \) while the improved design used \( \sim 0.02 \, \text{cm}^2 \)). In the following sections, the PECVD and SALD circuits were fabricated using the original design and the PEALD circuits were fabricated using the compact design (with the exception of the gamma radiation exposure circuits).

![Figure 69 – Mask layout for ZnO ring oscillators. (a) Original design with box and zoom in to a unit inverter. (b) Compact design to minimize thermal effects with box and zoom to unit inverter.](image)

5.3 PECVD ZnO TFT Circuits
The first low-temperature oxide circuits examined were deposited using PECVD ZnO TFTs. As noted in the TFT section, PECVD TFTs formed with large leakage current densities had large field effect mobility (>10 cm²/V·s) but circuits made from these devices did not operate. Figure 70 shows devices fabricated by using this lower leakage Al₂O₃ (<10⁻⁶ A/cm²) and a field effect mobility ~0.05 cm²/V·s, threshold voltage of 12 V, sub-threshold slope less than 1 V/dec, and a current on/off ratio > 10⁵ at V_DS = 40V were extracted. Devices also showed relative small hysteresis for unpassivated devices (<1 V or < 3 x 10¹¹/cm²). Five-stage ring oscillators with unit inverter dimensions L_drive = 5 µm, W_drive = 100 µm, L_load = 60 µm, W_load = 20 µm and source/gate and drain/gate overlap for this circuit was 2 µm, oscillated at 1.2 kHz or ~60 µs/stage at V_DD = 60 V [Figure 71 (a)]. The oscillation frequency and propagation delay as a function of V_DD is shown in Figure 71 (b). This low oscillation frequency is further evidence of slow interface traps commonly observed in many sputtered oxide TFTs.[24]
5.4 SALD ZnO TFT Circuits

The poor performance of the PECVD devices and circuits was countered by much better performance in collaboration with Eastman Kodak and the SALD devices. Ring oscillators were fabricated using SALD ZnO TFTs. Figure 72 shows results of a seven-stage RO with a beta ratio of 5 (L\text{drive} = 4 \, \mu m, W\text{drive} = 100 \, \mu m, L\text{load} = 4 \, \mu m, and W\text{load} = 20 \, \mu m) and gate-source and gate-drain overlap of 1.5 \, \mu m. Figure 72 shows an output waveform as well as operation frequency and propagation delay as a function of supply voltage for both measured and AIMSpice simulated ring oscillators. For V_{DD} = 25 V the circuit operated at a frequency of 2.3 MHz, corresponding to a propagation delay of 31 ns-stage and nearly 2000 times faster than the PECVD circuits described above and ~ 10 times faster than any other oxide circuits.[118] The agreement between the AIMSpice simulation and experimental results was fairly good, suggesting that the time dependent parameters not included in the simulation, such as interface states, do not strongly limit dynamic performance in these devices. These results were significant and together with
amorphous indium-gallium-zinc oxide circuits [118] (240 ns/stage) were amongst the first reported fast circuits fabricated using oxide TFTs. It is also important to note that the maximum speeds achieved are not limited by dielectric breakdown ($V_{DD} = 25$ V, $t_{ox} = 110$ nm, $E_{Field} = 2.3$ MV/cm), but rather, are limited by thermal effects. As described in Chapter 4, these thermal effects result in bias stress instability and positive threshold voltage shifts particularly in SALD devices, but ultimately, thermal runaway occurs as negative threshold voltage shifts lead to catastrophic breakdown. To further improve these speeds, thermal engineering will be necessary.

5.5 PEALD ZnO TFT Circuits

High performance circuits has also been fabricated from PEALD ZnO TFTs. Unit inverters were fabricated, and an example is shown in Figure 73. The inverter design shown here uses a saturated load with the gate and drain connected together. This is an easy way to form a load with an all enhancement mode unipolar system. It has the
problem of pulling up to $V_{DD-V_{load}}$, and therefore, logic level conservation can be an issue. The inverter gain is related to the geometric ratio as described in section 5.1. In the inverter shown in Figure 73, the designed beta ratio was 5 and the measured gain was ~1.5. This is somewhat lower than the expected gain of 2.2 (ideal inverter gain is the square root of the beta ratio, eg $\sqrt{5} = 2.2$). This may be related to several possible reasons. First, the ZnO pattern is larger than the source drain pads in both the load and drive and therefore the effective load width may be larger leading to a reduce beta ratio. Second, as mentioned in work on IGZO inverters, the geometric ratio does not accurately represent the ratio of conductances because the two devices are biased at difference points and the mobility of ZnO TFTs have a gate voltage dependent mobility.[118] Therefore, the effective mobility for the drive transistor is lower than the load at the inversion point, reducing the difference in conductance and the effective gain. The close fit between simulated and experimental inverters suggest that this gate voltage dependent conductance is the primary effect (this non-square law behavior is included in the model but width errors are not), reducing the beta ratio. In fact, in an effort to simulate high gain saturated load inverters a beta ratio of 10,000 ($W/L_{\text{drive}} = 1000/1$, $W/L_{\text{load}}=1/1000$, $t_{ox} = 32$ nm) was tried using a model for enhancement mode devices. An extracted gain of only 12 was found at $V_{DD} = 10$ V and increased to nearly 35 by $V_{DD} = 25$ V (near the breakdown field for real Al$_2$O$_3$), both significantly lower than the expected 100. Therefore, fabricating very high gain saturated load inverters using oxide TFTs with a highly gate voltage dependent mobility may present a significant challenge particularly, as large drive transistors will also introduce a large parasitic capacitance amplified by the Miller effect.[119] Despite these challenges, exceptionally high gain is not necessary for
a variety of digital circuits such as ring oscillators, and therefore, due to the ease of
fabrication, the ring oscillators in this chapter are all fabricated using saturated loads.

![Image](image.png)

**Figure 73** – (a) Schematic and optical micrograph of unit saturated load inverter from PEALD ZnO TFTs. (b) Output characteristics for inverter with beta ratio of 5 for various supply voltages (2, 4, 6, 8V).

In applications where gain is more important, such as in an analog amplifier, other
approaches must be used. Preliminary tests have been done using a depletion mode TFT
as a load. In a depletion mode load, the gate and source of the load transistor are
connected together and provide effectively constant current source. The change in
current over a wide range of $V_{DD}$ will be only a function of the output conductance in the
depletion load device, which, for low input powers, can be extremely low for oxide TFTs.

Figure 74 shows a schematic and an experimental demonstration of a high gain (>100)
inverter using PEALD ZnO TFTs. In this example, windows were photolithographically
defined over the load transistors and a hydrogen plasma treatment was used to shift the
threshold voltage. Other advantages of the depletion load can be observed particularly
full voltage retention at the low and high input voltages levels. Very recently, depletion
load inverters and circuits were also demonstrated using sputtered IGZO (two different active layer thicknesses gave different threshold voltages) with peak gain of ~ 35.[120] This approach requires very precise threshold voltage control for use in circuits such as operational amplifiers. The current source is varied by the threshold voltage of the depletion load and therefore setting an operational point requires a very precise current. Also, the frequency of the circuit is a strong function of the current source and nearly independent of V_{DD}. In order to achieve high speeds, relatively large currents need to be sourced. Figure 75 shows an AIMSpice simulation for the current as a function of V_{T}, as well as the frequency of ring oscillators made using these inverters. The threshold voltage was varied (from +0.5 to -8.5 V) by changing V_{FB} and V_{TO} in AIMSpice. Ring oscillators were simulated using very relaxed dimensions depletion loads with varied V_{T} (W/L = 5/10 \mu m) and enhancement drives (V_{T} = 0.5 V, W/L = 100/10 \mu m), and 2 \mu m overlap. The depletion load current with V_{DS} = 10 V was found to vary from 6 \times 10^{-11} to 5 \times 10^{-4} A by varying the threshold voltage from 0.5 to -8.5 V. Over this same range, the propagation delay decreased from 1.8 ms/stage to 348 ns/stage. Further reducing the channel length and overlaps would result in significant increases in speed. This simulation demonstrates that depletion load inverters may be useful for high speed, high gain, full-swing circuits. Initial tests of circuits using depletion load ring oscillators showed propagation delays of ~ 200 ns/stage; however, due to a poor mask design which left ungated regions on the load the current was not constant (much higher than modeled) and therefore the circuits were somewhat faster than modeled. The advantages of the depletion load circuits will ultimately need to be balanced against the cost of the additional processing required to fabricate two different threshold voltage TFTs.
Conventional 15-stage ring oscillator circuits using saturated load PEALD TFT inverters were fabricated and the result is shown in Figure 76. The 15-stage ring oscillators were
fabricated with a beta ratio of 5 (drive TFT W/L = 50/2.5 μm, load TFT W/L = 10/2.5 μm) and a source/drain to gate overlap of 1.5 μm. An output buffer stage was also used which had an identical beta ratio, but the device widths were doubled. An optical micrograph of the ring oscillator is shown in Figure 76. The frequency and propagation delay as a function of supply voltage is shown in Figure 76. The ring oscillators operated at 1.5 MHz at a supply voltage of 16 V, corresponding to a propagation delay of 22 ns/stage. The speed of these ring oscillators is ~30% faster than previously described 7-stage ring ZnO ring oscillators formed using SALD[66]. Similar to the SALD circuits, the PEALD circuits are roughly the same as the modeled behavior and therefore indicate that the TFT characteristics described previously are not limited by slow states.

These PEALD ZnO TFT circuits were fabricated using scaled channel lengths and overlap capacitances but were unpassivated, so inevitably suffered from instability. As a
result, once near enhancement mode passivated ZnO TFTs were developed, circuits were fabricated. Figure 77 shows the frequency, propagation delay, and power for 7-stage ring oscillators with similar dimensions: beta ratio = 5, channel length = 3 µm, and 1 µm source/gate and drain/gate overlap. The circuits notably operate at faster speeds at lower supply voltage as expected due to the increased current from the threshold voltage shift during passivation. More importantly, they are significantly more stable than the unpassivated circuits. They reach a minimum propagation delay <20 ns/stage at considerably lower fields (3 MV/cm compared to 5 MV/cm for unpassivated). These circuits, like all described above, are ultimately limited by thermal breakdown that occurs in this device when the supply power exceeds ~70 mW.

Figure 77 – (left) Frequency, propagation delay, and supply power for 7-stage ring oscillator with beta ratio = 5, channel length = 3 µm, and 1 µm source/gate and drain/gate overlap. (right) Run to run uniformity for passivated PEALD circuits on three different samples. RO1 had beta ratio = 5, channel length = 5 µm, and 4 µm source/gate and drain/gate overlap. RO2 had beta ratio = 5, channel length = 3 µm, and 2 µm source/gate and drain/gate overlap.

Figure 77 also shows the reproducibility and uniformity of passivated PEALD ZnO circuits. Two different ring oscillator designs RO1 (beta ratio = 5, channel length = 5 µm,
and 4 µm overlap) and RO2 (beta ratio = 5, channel length = 3 µm, and 2 µm overlap) were tested on 9 dies per sample, and the standard deviations are marked with error bars. The run-to-run device uniformity for the PEALD process was very good after every dielectric semiconductor stack was deposited in situ. The differences shown here are primarily related to lithography non-uniformities due to smaller offsets in rotational and lateral misalignments. RO1, which has much longer channel lengths and overlaps, shows considerably smaller standard deviations, as well as sample-to-sample variation. Regardless of process non-uniformities, it is clear that stable high speed PEALD circuits can be reproducibly fabricated.

5.6 Gate-Self-Aligned PEALD ZnO TFT Circuits

To further improve the performance of these PEALD circuits, the channel lengths could be further scaled; however, this would increase process cost as well as the device currents, and worsen heating effects, which are non-negligible on glass and polymeric flexible substrates, as described in Chapter 4. These earlier circuits were largely limited by the parasitic capacitance between the gate and source and drain contacts, which is shown in Figure 78 (a). In particular, the gate-drain overlap capacitance is particularly important as it is magnified by the Miller effect in the inverter. As an alternative approach, reducing parasitic capacitance would provide a significant performance improvement without introducing additional heating effects. As described before, a simple TFT model in AIMSpice [116] was used to simulate the performance of simple circuits. Using this model, the overlap capacitance in the model can be modified based on overlap distance between the gate and source and drain metal (∆L in Figure 78 (a)). The result is shown in
Figure 78 (b) and shows that nearly an order of magnitude improvement in speed is obtained by reducing the overlap distance from 5 μm to 0.1 μm. To achieve small overlap with low-cost lithography, a simple gate-self-aligned process is of interest for oxide circuits on low cost substrates.

Various techniques are possible to form self-aligned oxide TFTs. Park et al. used an Ar plasma to form conducting source and drain regions in indium-gallium-zinc oxide TFTs and self-aligned-gates with field-effect mobility of 5 cm²/V·s. [100, 106] However, this method relies on defect generation to produce the conducting regions, and therefore, thermal and process stability is likely to be a concern. In fact, as described in Chapter 4, argon plasma treatments have been used to increase the free carrier-concentration below the contacts; however, low temperature anneals in air resulted in increases in the contact resistivity. A gate-self-aligned process for amorphous silicon TFTs using a backside exposure has been reported previously for glass and flexible substrates.[121, 122] The backside exposure process has the added benefit of removing alignment errors in the
most critical alignment step (source-drain to gate) that can result in difference in circuit performance, as described in the passivated ZnO circuit uniformity. This rotational and lateral misalignment is particularly an issue with flexible circuits where the substrate dimensional instability can result in significant alignment errors, even on relatively small substrates (> 2 µm). In amorphous silicon, due to optical absorption in the relatively small bandgap semiconductor, thin a-Si:H films must be used for the backside exposure to be effective. In comparison, the wide bandgap of oxide films such as ZnO provides transparency for the backside exposure for exposure at wavelength longer than about 370 nm. The gate-self-aligned PEALD ZnO TFTs in this work [101] have a similar fabrication process to the previously described circuits. First, a 100 nm thick Cr gate layer was deposited by ion-beam sputtering and patterned by wet etching. Next, 32 nm thick Al₂O₃ and 30 nm thick undoped ZnO deposited at 200°C and patterned by wet etching. The difference in the self-aligned-gate process can be seen in Figure 79 (a-d). A backside exposure of a double layer resist (PMMA/Novolak 1811) is used to define the self-aligned channel region, and Ti is sputtered and lifted off to form the self-aligned source and drain contacts. The Ti layer was then isolated by photolithography and dry etched a CF₄/O₂ plasma. Finally, a second Ti layer was sputtered and patterned to connect the gate and source-drain metal layers where needed.
Figure 79 (e-f) shows optical micrographs for a discrete self-aligned-gate PEALD ZnO TFT. The device has a W/L of 205/12 μm and a gate-to-source/drain overlap of ~0.3 μm. Figure 80 (a) shows log(I_D) and I_D versus V_GS for V_DS = 0.5 V and 12 V. Figure 80 (b) shows I_D versus V_DS characteristics for several values of V_GS for the same device. From these characteristics, a linear region field-effect mobility of 16 cm²/V·s, a saturation field-effect mobility 20 cm²/V·s, a threshold voltage 6 V, a sub-threshold slope of 140 mV/decade, and a current on/off ratio > 10⁹ are extracted. Figure 81 shows that using transmission line measurements with large gate-contact overlap a specific contact resistivity of 2 × 10⁻⁴ ohm·cm² and a transfer length of 0.3 μm are extracted. This contact resistivity results in a significant contact resistance for the small overlap self-aligned devices. Because the source resistance acts as a negative feedback element for the mobility extraction, slightly lower field-effect mobility is extracted in these self-aligned TFTs compared to non-self-aligned devices. That is, the mobility extracted is not the
intrinsic field effect mobility in the TFT, but rather the extrinsic mobility of the TFT plus parasitic source resistance. Improved contacts will be required to allow further reduction of overlap and channel length without significant extrinsic mobility degradation.

Figure 80 – (left) $\log(I_D)$ versus $V_{GS}$ for $V_{DS} = 0.5$ V and $V_{DS} = 12$ V ($W/L = 205 \mu m/12 \mu m$, $t_{OX} = 32$ nm), (right) $I_D$ versus $V_{DS}$ characteristics for several values of $V_{GS}$ for the same device.

Figure 81 – Gated transmission line measurement for gate-self-aligned PEALD ZnO TFTs with titanium contacts.

Figure 82 (a) shows an optical micrograph of a 7-stage ring oscillator. The inverters of the ring oscillator have 2.8 $\mu m$ channel length and a beta ratio of 5 with a source/gate and
drain/gate overlap of 0.3 μm. Figure 82 (b) shows frequency and propagation delay for this ring oscillator, which oscillates at 7.3 MHz at a supply voltage $V_{DD} = 18$ V, corresponding to a propagation delay (inverse frequency divided by twice the number of stages) of 9.8 nsec/stage.[101] These ring oscillators are similar in performance to the best reported saturated-load oxide-semiconductor circuits [110], but with much longer channel length (> 5 × longer) and on glass rather than crystalline silicon substrates. These results are also expected to be considerably improved if shorter channel lengths, and passivated devices are used, and make < 5 ns/stage on glass an achievable target.

5.7 Flexible PEALD ZnO TFTs and Circuits

As previously mentioned, very high speed devices and circuits have been demonstrated on single crystalline substrates such silicon and GaAs. In the previous sections, high performance circuits were demonstrated on glass substrates. However, glass substrates are relatively heavy, rigid, and are easily shattered. For that reason, there is interest in
forming high performance devices and circuits on flexible substrates for a range of portable applications where lightweight durable substrates are highly desired. Flexible electronics using low-deposition-temperature semiconductor materials are of interest for use in applications such as active-matrix displays. In addition, as mentioned in section 3.8, there are a variety of applications where non-planar substrates may provide significant performance advantages and flexible substrates are one obvious pathway.

Flexible substrates such as plastics and thin metal foils provide significant technological challenges. The substrates contain a significantly higher density of defects, such as scratches, compared to electronic glass or crystalline substrates. It is possible to use planarization layers to significantly reduce the impact of these types of defects; however, this adds to the process complexity and in the case of metal foils can significantly reduce the thermal sinking properties of the substrate. The second important consideration is the thermal expansion coefficients of the substrate. In particular, for plastic substrates, large thermal expansion coefficients result in layer-to-layer alignment errors. Finally, plastic substrates will often take up solvent during wet chemical processing, and therefore, either careful processes (such as slowly heating the films) or barrier layers (inorganic insulators preferred such as SiNₓ, Al₂O₃, SiO₂, etc.) need to be employed to ensure that the solvent does not effect the depositing layers.

Despite these challenges, there have been reports of very high performance circuits on flexible substrates. Polysilicon TFTs with mobility ~200 cm²/V·s were fabricated on stainless steel substrates, and ring oscillators were shown with propagation of 1.38
However, the expensive, non-uniform laser recrystallization of polysilicon has many potential challenges in very large-area applications. Organic semiconductor based circuits are also a natural choice for flexible electronics; however, the general low field-effect mobility (≈1 cm²/Vs) makes very high speed demonstrations challenging. Despite the low device performance, ring oscillators have been demonstrated using spin coated diF TES-ADT TFTs on polyimide substrates with propagation delay of 3.3 μs/stage. There have also been several reports of oxide TFTs on flexible substrates using either stainless steel foils or plastic substrates [125-127]. Recently, Hsieh et al. reported five-stage ring oscillators using sputtered amorphous indium-gallium-zinc-oxide TFTs on a polyimide substrate with propagation delay of 350 ns/stage at a supply voltage of 20 V [128].

The flexible substrate work described here was led by Dalong Zhao from Electrical Engineering (more fabrication details can be found in his PhD thesis) and circuit design and some device testing was performed by myself. The flexible substrates used in this work were primarily polyimide substrates with a high glass transition temperature (T_g ≈354 °C) and relatively small coefficient of thermal expansion (CTE ≈16 ppm/°C). First, the 125 μm thick polyimide substrates were prebaked at 200 °C in a vacuum oven for 24 hours, and then laminated onto glass carriers with a silicone gel for ease of handling during device fabrication. The samples were then processed in the same procedure described in section 5.2. Due to challenges probing fully flexible substrates, most of the device testing was done while the samples were still laminated to the carriers. However,
some devices have been tested after the flexible substrate was delaminated from its carrier and only very minimal changes were observed.

The first important test for flexible circuits is the integrity of the thin PEALD gate dielectrics. As mentioned before, the plastic surfaces are rough and easily scratched so the dielectric needs to be highly conformal with low defect density. The polyimide substrates in this work were characterized by atomic force microscope (AFM), and the RMS surface roughness was found to be ~30 nm for a 10 μm scan as shown in Figure 83 (a). In order to test the defect density on polyimide substrates, test structures containing 8,000 crossovers with top and bottom metal layers separated by 50 nm of PEALD Al₂O₃ were fabricated (see Figure 83 (b)). Figure 83 (c) shows an example of a good 8,000 point crossover. A yield criterion was set at 10⁻⁷ A/cm² at an electric field of 3 MV/cm and we found an yield of > 80% for 28, 8,000 crossovers test structures as shown in Figure 83 (d). The test structures which failed typically had easily identifiable defects and would likely be improved by processing in a clean room environment. However, given the crude processing and the use of a dielectric thickness which is comparable to the RMS roughness, this demonstrates that PEALD Al₂O₃ can be extremely conformal and highly suited for devices on flexible substrates.
Figure 84 shows typical characteristics for a passivated polyimide substrate ZnO TFT with channel width and length of 50 μm and 20 μm, respectively. A linear region field effect mobility of 20 cm²/V·s, threshold voltage 2 V, sub-threshold slope of 350 mV/decade, and current on/off ratio >10⁷ were extracted from log(I_D) versus V_{GS} in linear region. Passivated devices also have small hysteresis of ~200 mV. These results are similar to those obtained on glass substrates described before, but with about 30% lower mobility and somewhat higher subthreshold slope.
Figure 85 shows an optical micrograph and frequency versus propagation delay for a 15 stage ring oscillator on polyimide. The ring oscillator had a beta ratio of 5 with drive transistor $L_{\text{drive}} = 1 \mu\text{m}$, $W_{\text{drive}} = 100 \mu\text{m}$, and load transistor $L_{\text{load}} = 1 \mu\text{m}$, $W_{\text{load}} = 20 \mu\text{m}$. The source/gate and drain/gate overlap was 2.5 $\mu\text{m}$ and, from the discussion in the previous section, is expected to have a significant effect on speed. The circuit operates at low supply voltages as small as 2 V and oscillates at slightly more than 2 MHz for a supply voltage of $V_{\text{DD}} = 18$ V, corresponding to a propagation delay of <20 nsec/stage. It is worth noting that the speed on plastic and glass substrates was similar. This is largely a function of design and device characteristics. While the overlaps were smaller on glass, the channel lengths were somewhat longer. Additionally, the flexible circuits were passivated which resulted in somewhat larger currents at lower voltage. In a closer comparison, the glass circuits are expected to be somewhat faster due to slightly higher mobility and better thermal sinking.
The designs for these circuits used relaxed layout rules (larger alignment tolerance) for the gate-to-source and gate-to-drain overlaps (2.5 μm) to compensate for dimensional stability limitations of the polyimide substrates. Even at this alignment tolerance, yielding uniform circuit performance over large substrates would be difficult. In that design, the gate lines are made large and perpendicular to the source and drain lines. The line width for the source and drain then sets the overlap so by making the line fine (1-2 μm), the parasitics can be low while still maintaining good rotational and translational alignment tolerance. However, this approach also has limitations. As the line width is reduced, the line resistance can become a non-negligible contribution to the contact resistance. Ideally, gate-self-aligned structures described in section 5.5 would be employed on plastic; however, this would require clear plastic substrates which are transparent to 400 nm light. However, most low-cost clear substrates such as polyethylene naphthalate (PEN) or polyethylene terephthalate (PET) have lower glass transition temperatures. Therefore, further understanding towards depositing PEALD ZnO at lower temperatures (<150 °C) will need to be developed before a wide range of high performance circuits can be reliably formed on plastic.
5.8 Radiation Hard ZnO Devices and Circuits

The radiation tolerance of electronic devices and circuits is of interest for space and some other harsh environment applications. For space applications, the development of large-area structures which are fully deployable requires a robust, lightweight technology which can withstand the harsh conditions. Properly designed deep submicron gate length Si MOSFETs can have small threshold voltage shift and leakage increase for doses of 100 kGy (10 Mrad) or even larger [129]. However, the functionality in this case needs to be dispersed over large areas (100 x 100 m), and therefore, picking and placing hundreds of thousands of silicon die presents significant technological challenges. Therefore, a uniform large-area deposited thin film transistor technology may be significantly easier to implement.

Figure 85 – (a) Optical micrograph and schematic of 15 stage ZnO ring oscillator plus output buffer stage. (b) Frequency and propagation delay for PEALD ZnO TFT ring oscillator on polyimide ($W_{\text{drive}} = 100 \, \mu\text{m}$, $W_{\text{load}} = 20 \, \mu\text{m}$, beta ratio = 5, $CL = 1 \, \mu\text{m}$, overlap = 2.5 \, \mu\text{m}$).
There is also interest in being able to fabricate integrated ultrasonic imaging systems on flexible substrates [130]. These integrated sensor arrays may have use in areas receiving radiation such as nuclear reactors, and would likely benefit from closely integrated thin film circuits. In section 5.6, we demonstrated the ability to fabricate high performance circuits on flexible polyimide substrates. As a next step towards harsh environment integrated arrays, initial measurements to understand how PEALD ZnO devices on glass and plastic might perform under exposure to radiation have been performed. Polysilicon thin film transistors (TFTs) show significant changes at low dose (< 1 kGy) [131] and a-Si:H TFTs have volt-range threshold voltage shift for 10 kGy dose [132]. The effects of gamma-ray irradiation on plasma enhanced atomic layer deposition (PEALD) ZnO TFTs and circuits have been investigated. This work was led by Dalong Zhao from Electrical Engineering however I was responsible for the sample fabrication, mask design, and testing described below. This was also made possible by Candace Davison from the Penn State Radiation Science and Engineering Center for providing assistance.

Compared to conventional covalent silicon materials, ZnO TFTs have the potential for excellent radiation resistance. In conventional covalent semiconductors (like silicon), the chemical bonds are $p$ or $sp^3$ orbitals with strong directivity and radiation damage can lead to strained bonds and deep trap states. In ZnO, the cations form states at the conduction band minimum from spherically extended $s$ orbitals of the metals, greatly reducing the role of damage and disorder for conduction band transport because of the large overlap between adjacent spherical orbitals.[9] For this reason, the mobility of amorphous and crystalline ZnO is expected to be very similar. Experimentally, this has been observed
for a similar oxide materials including amorphous and crystalline indium-gallium-zinc oxide.[9]

The ZnO TFTs and circuits for the radiation study were fabricated on both borosilicate glass and polyimide substrates as previously described. 54 nm thick Al₂O₃ and 10 nm undoped ZnO were deposited at 200 °C by PEALD, and devices were passivated by 30 nm ALD Al₂O₃. The layer thicknesses are of importance because the very thin Al₂O₃ and ZnO layers have a significantly lower capture volume compared to bulk silicon devices. After fabrication, unbiased devices and circuits were exposed to ⁶⁰Co gamma rays with dose from 10 kGy to 1 MGy. Figure 86 shows images of the samples and sample boxes after various exposure periods. Even after the shortest exposures (10 kGy), the samples and boxes both began to yellow, which is expected as color centers form [133].

![Figure 86](image-url) – Images of fluoroware containers and PEALD devices on glass ranging from no exposure (left) to 1 MGy exposure (right). The samples and boxes turn yellow as color centers form from the radiation.

The threshold voltage for these PEALD devices before irradiation was ~ -1 V and the linear region field effect mobility is ~ 18 cm²/V·s. Figure 87 (a) shows the linear region log(I_D) versus V_G characteristics for devices with ⁶⁰Co gamma ray dose from 0 to 1 MGy.
and Figure 87 (b) shows extracted threshold voltage and mobility changes. Irradiated
devices have a negative threshold voltage of ~ 1 V for 10 kGy dose, increasing to ~1.5 V
for 50 kGy, and increasing more slowly for larger dose. The irradiated device mobility is
nearly unchanged, but subthreshold slope increases somewhat, particularly at the highest
doses. To quantify this change in curve shape, the threshold voltage, \( V_T \) (Figure 87 (b)
straightline fit to transconductance) has been compared to the turn on voltage \( V_{ON} \)
(Figure 87 (c) \( V_{GS} \) where \( I_{DS} = 10^{-10} \) A). The turn on voltage is decreasing more rapidly
than the threshold voltage, indicating an increasing subthreshold slope. Surprisingly,
both the threshold voltage and turn-on shifts are nearly completely removed by annealing
at 200 °C for 1 minute (Figure 87 (c)), and some recovery is also seen even at room
temperature after several days (Figure 87 (c)). The slow saturation of threshold voltage
shift with dose may therefore indicate self-annealing at the irradiation temperature (35 –
40 °C). This means that in some harsh environment applications where the operating
temperature may be > 100 °C the devices may self anneal faster than they shift and be
completely stable with time.
The effect of $^{60}$Co gamma ray irradiation on 7-stage ZnO TFTs ring oscillators was also studied. Figure 5 shows the operation characteristics for oscillators as fabricated and after 10 kGy and 200 kGy gamma ray dose. The circuits were fabricated on 3 different passivated samples which were fairly uniform, as seen in Figure 77. The circuit dimensions were not as aggressively scaled as the fastest ring oscillators in order to ensure yield and process uniformity. Figure 88 shows the circuits operate well before and after irradiation, with an increase in starting voltage and increased oscillation frequency after irradiation. These changes are expected give the negative threshold voltage shift observed in the irradiated TFTs. Irradiation results for discrete devices on polyimide substrates was similar to those found on glass substrates; however, circuits did not function due to a via etching issue. These results demonstrate that PEALD ZnO TFTs and circuits are interesting candidates for radiation harsh environments, particularly those at elevated temperatures (> 100 °C) where any changes created may be actively annealed.
5.9 Hybrid Organic/ZnO CMOS Circuits

The demand for low-cost, high-mobility, thin-film transistor (TFTs) technologies has generated particular interest in low-temperature-process organic and metal oxide semiconductors. CMOS circuits are likely to be important for low-power and especially battery-powered applications and also because CMOS allows simplified and more robust circuit design. In particular, low-cost, low-temperature device fabrication processes often result in devices with a distribution of characteristics. For unipolar circuits, this typically results in digital circuits with varying response to input signals and varying output voltages. While this can be accommodated to some extent by appropriate circuit design, the result is often slower, less reliable, and lower yield circuits. Because CMOS digital circuits use complementary switches, they typically provide output logic levels at or close to the power supply rails. This allows many CMOS digital circuits to tolerate large

**Figure 88** – Ring oscillator performance after exposure to gamma radiation of 10 kGy and 200 kGy. The speed for the two different samples is similar (RO1 and RO2) and a significant increase in speed and the minimum operation voltage is observed with radiation. This is expected given the negative threshold voltage shift observed.
deviations from ideal device behavior and substantial variation in device-to-device characteristics.

ZnO is currently one of the most promising n-type semiconductors for thin-film applications because it allows high-quality thin films and high-mobility TFTs (>10 cm$^2$/V·s) using low temperature deposition processes. However, while n-channel ZnO TFTs have been widely reported [for example, [16], [87]], there are no reports of stable, high-mobility, p-channel devices. In contrast, p-channel organic TFTs typically have higher mobility and better stability than n-channel organic devices. While the stability and field-effect mobility of most organic TFTs are poor compared to ZnO TFTs, organic TFTs can be fabricated using very simple solution processing, which may provide a path to an inexpensive and simple to implement CMOS process.

There have been several previous reports of hybrid inorganic-organic CMOS processes. Katz et al. demonstrated CMOS inverters using amorphous silicon and α-hexathienylene TFTs fabricated on separate substrates, with field-effect mobility of <1 cm$^2$/V·s and <0.03 cm$^2$/V·s respectively [134]. Bonse et al. demonstrated ring oscillator circuits with a minimum propagation delay of 5 µs using a-Si:H and pentacene devices fabricated on a single substrate [135]. Low-voltage ZnO-pentacene CMOS circuits were demonstrated where both the ZnO and pentacene TFT mobilities were ~1 cm$^2$/V·s, and a ZnO-pentacene inverter was shown to respond up to a 10 Hz input frequency with rise and fall times of 4 ms and 13 ms, respectively [136, 137]. 5-stage hybrid CMOS ring oscillator circuits fabricated using indium gallium zinc oxide and pentacene TFTs operated with a
minimum propagation delay of 1 ms/stage at 10 V [103]. All of the previous reports used vacuum-based processes to deposit the gate dielectric layer, as well as both semiconducting layers. In addition, different metallization steps and patterning steps were required for the organic and inorganic semiconductor TFTs. These vacuum-based processes and additional mask steps result in a more complicated, expensive process. In addition to the complex processing, the dynamic performance of ZnO-based hybrid CMOS circuits thus far has been limited to >1 ms/stage. In this report, a simple 4-mask CMOS process with bifunctional Ti/Au contacts and ZnO/organic hybrid circuits operating at <150 ns/stage at a supply voltage of 35 V is demonstrated.

In section 5.3, fast SALD ZnO ring oscillators (<31 ns/stage for 4 μm channel length) were described [8]. Previous reports have shown that the organic semiconductor difluoro 5,11-bis(triethylsilylethynyl) anthradithiophene (diF TES-ADT) yields a different and more ordered microstructure on and near pentafluorobenzene-thiol-treated gold electrodes than on untreated oxide surfaces, resulting in high mobility (~0.1 - 1 cm²/V·s) and a self-patterning character for diF TES-ADT TFTs and circuits [124, 138-140]. The nature of this crystallization phenomenon and its impact on the electrical properties of the material and interfaces is related to contact treatments and molecular design and has been described in detail in several previous reports.[138-141] Using this self-patterning microstructure, simple all-organic circuits on polyimide substrates operating at 3.3 μs/stage with no direct patterning of the organic layer were demonstrated [124]. This section will describe an integrated approach that combines these two technologies in a simple way to form high-speed, low-temperature CMOS circuits.
The hybrid inorganic/organic CMOS circuits were fabricated on 2.5" \times 2.5" borosilicate glass substrates, with an ion beam sputtered and photolithographically patterned chromium layer used for both the organic and inorganic TFT gates. Spatial ALD was used to deposit 150 nm of $\text{Al}_2\text{O}_3$ and 100 nm ZnO at 200 °C and atmospheric pressure. Photolithography and wet etching were used to pattern the ZnO and $\text{Al}_2\text{O}_3$ layers. Next, using a double-layer photoresist (Novalak/PMMA) mask, the ZnO contact surface was first Ar ion beam-etched and then deposited Ti/Au (10 nm/100 nm) was ion beam-sputtered and patterned electrodes by lift-off. The ion beam etching of the contact area improves the contact resistance to the ZnO [57]. Ti/Au was used because the Ti bottom layer makes a good contact to the n-channel ZnO and the Au top layer makes a good contact to the p-channel diF TES-ADT, minimizing the processing and mask steps required for device fabrication. The Ti/Au electrodes were then treated with the self-assembled monolayer pentafluorobenzene thiol (PFBT), and the $\text{Al}_2\text{O}_3$ dielectric was treated with hexamethyldisilazane (HMDS). The diF TES-ADT organic semiconductor was then spin-cast from a 2.5 wt% solution in chlorobenzene with a chlorobenzene solvent vapor ambient maintained above the sample during spin-casting to promote uniform, large grain growth on and near the PFBT-treated contacts [141]. The solvent spinning combined with the contact related microstructure previously mentioned is a straightforward way to achieve a highly controlled organic crystallization. The samples received a 30 minute bake at 90 °C to remove residual solvent and were then tested. All devices and circuits were measured in air. A schematic cross-section and optical micrograph of a CMOS inverter and enlarged images showing the organic thin-film
differential microstructure on gold and oxide are shown in Figure 89. The differential microstructure between the treated gold electrodes and the untreated oxide areas provides enough device isolation for simple circuit operation without direct patterning of the organic semiconductor. The entire process required no vacuum processing to deposit the semiconducting and dielectric layers and only four masks and lithography steps.

Discrete n-channel ZnO and p-channel diF TES-ADT transistors were tested and the results are shown in Figure 90. The 150-nm-thick Al₂O₃ layer had a dielectric constant of 8. The n-channel ZnO transistors had mobility of 12 - 15 cm²/V·s and threshold voltage of ~0 - 1 V. The p-channel diF TES-ADT transistors had mobility of ~0.1 - 0.2 cm²/V·s
and threshold voltage of ~8 - 12 V. In both transistors, the off current was limited to ~1 μA due to residual leakage through the unpatterned organic layer and not through the ZnO layer, which is fully depleted even at 100 nm thickness. The off current of these devices would be improved by patterning the organic layer, but the circuits operate well without patterning. In addition, because the p-channel organic material covers the ZnO layer in the n-channel device, these devices are ambipolar. However, because the mobility for the ZnO is ~100× higher than the diF TES-ADT and the ZnO layer is relatively thick (100 nm), resulting in reduced gate capacitance, the p-channel channel formation in the organic layer on top of the n-channel ZnO devices has minimal impact and results mainly in a small shift in the n-channel threshold voltage (<3 V). This impact would also be removed by using a patterned organic layer. Plots of the drain current as a function of drain voltage for several gate voltages are shown in Figure 2 for both the n-channel and p-channel devices.

![Figure 90](image-url) – Drain current as a function of drain voltage for several gate voltages for discrete p-channel (left) and n-channel (right) devices. The p-channel device has a field-effect mobility of ~0.1 cm²/V·s and the n-channel device has a field effect mobility of ~ 12 cm²/V·s.
Figure 91 (a) shows the characteristics of a hybrid inorganic ZnO – organic diF TES-ADT CMOS inverter. The static off current and power consumption of the circuits were limited by the unpatterned diF TES-ADT organic layer, and the supply current peak is partially due to the depletion mode organic TFT with threshold voltage of 8–12 V. In addition, the inverter was designed with a $\frac{W_{p-channel}}{W_{n-channel}}$ ratio of 10, but the mobility was actually $\sim 100\times$ larger in the n-channel device. Patterning the organic material and optimizing the circuit design would allow for substantially improved gain and power consumption. However, despite these non-idealities, the robustness of CMOS digital circuits allows acceptable operation for a range of integrated circuit applications.

As an example, simple 7-stage ring oscillators were fabricated. Figure 91 (b) shows the propagation delay as a function of supply voltage for three different TFT channel lengths. For the organic TFTs, the mobility has significant channel length dependence. This is due to the treated contact-related microstructure self-patterning, which results in diF TES-ADT grains which extend completely across short channel length devices, but not longer channels, and thus in a mobility that increases with decreasing channel length. As a result, the decrease in propagation delay as a function of channel length is more substantial than would be expected for a constant mobility versus channel length devices. AIMSpice [15] was used to fit I-V curves for discrete 5 $\mu$m channel length diF-TES-ADT and ZnO TFTs and to simulate ring oscillator operation. The result is shown in Figure 91 ((a), dotted line) and shows a reasonable match to the experimental results. Because the AIMSpice model does not have time constants for charge states this reasonable match is evidence that slow-interface states do not dominate the electrical performance of these devices. Seven-stage ring oscillators fabricated with a beta ratio of 10, 3-$\mu$m channel
lengths, and 1-μm gate/source and gate/drain overlaps oscillated at a frequency >500 kHz, corresponding to a propagation delay of <150 ns/stage at a supply voltage of 35 V.[102] These results demonstrate the advantages and feasibility of a low-temperature thin film CMOS circuits.

Figure 91 – Output voltage and supply current for a unit CMOS inverter with a beta ratio of 10 (left). Experimentally measured propagation delay as a function of channel length for 7-stage CMOS ring oscillators with AIMSpice simulated propagation delay in the dotted line (right).
Chapter 6

6.1 Conclusions

This thesis has described the development of a new deposition process for low-temperature thin films particularly aimed at high performance ZnO TFTs. In particular, by understanding and comparing the strengths and weaknesses of SALD and PECVD, PEALD was developed. The PEALD ZnO films were dense, highly crystalline, and had high resistivity. These characteristics are important for TFTs and unachievable by other processes examined. Devices formed using PEALD ZnO and Al₂O₃ had mobility >20 cm²/V·s, representing more than an order of magnitude improvement over amorphous silicon, the current large-area thin film transistor technology. In particular, the electronic band structure of these oxide materials allows for transport which is weakly perturbed by order and temperature. Despite the significant advances in thin-film technology, many non-idealities exist in the materials and devices. An explanation for the carrier-dependent mobility was shown through temperature-dependent measurements and can be described by small barriers above the conduction band. Self-heating in oxide TFTs was found to set an upper limit for device performance on low cost substrates such as glass and plastic, and the need for thermal management in flexible electronics appears essential. Finally, these ZnO TFTs were used in simple integrated circuits on glass and plastic substrates. These circuits provided valuable information about the dynamic performance of the devices and pointed to several unique areas where the integration of high performance thin film technology may be interesting. It was determined that parasitic capacitance and self-heating were the primary factors limiting circuit performance. To reduce the parasitic capacitance, a back side exposure process was utilized to fabricate
gate-self-aligned TFTs and circuits. Using this process, circuits with propagation delay <10 ns/stage were formed and represent some of the fastest oxide circuits reported to date. Finally, hybrid organic-inorganic CMOS circuits were demonstrated as an approach to reduce the self-heating effects observed in unipolar circuits. This work represents the development of a flexible deposition process, its impact on ZnO TFTs, and the demonstration of several potential applications. While this work has established a good experimental base to fabricate oxide thin films at low temperature, there are plenty of areas where future work should focus.

6.2 Future Work

The first area for future work is a more fundamental understanding of the current technology. A more thorough materials study of the ZnO films including measurements of carbon incorporation, and crystallinity as a function of temperature may provide insight into some of the differences observed for different plasmas (section 3.4). This understanding will likely be essential to further reduce the deposition temperature while still retaining excellent device performance.

There are still a variety of challenges associated with the device technology including passivation, accumulation dependent mobility, and contacts. For instance, section 3.5 discussed the passivation of ZnO TFTs. While it was possible to use several different treatments to inhibit the threshold voltage shift, the mechanism for this shift is not well understood. Experimental studies with different surface and passivation processes will be essential in forming devices with highly reproducible threshold voltages. In addition, the accumulation dependent mobility described in Chapter 4 has tremendous impact on how
these devices are used in real applications. Initial temperature dependent measurements were used to show that barriers above the conduction band may cause the observed behavior. In this case, developing different deposition processes and understanding of materials particularly tuned to reducing the accumulation dependent mobility is essential. It would also be useful to understand the threshold voltage shift observed with temperature and the role of pyroelectric charge. A direct measurement of the piezoelectric and pyroelectric properties of these films should be done. Finally, section 4.3 outlined a variety of processes to form contacts to ZnO TFTs. However, dual gated devices suggested that the subthreshold slope was primarily dictated by contact turn-on. Further work on making doped contacts to ZnO is essential in forming reproducible devices.

The second major area for future work is integration of the current technology into application demonstrations. Chapter 5 described a variety of simple circuits and this work should be extended to more complex and applicable integrated analog and digital circuits. These circuits could be integrated into other active research projects including simple decoders for bioengineering samples [142, 143] or voltage multipliers for close coupled electronics.[144, 145] ZnO TFT arrays should also be developed. This will provide both a measure of uniformity but also the ability to potentially integrate into real displays and sensors. For instance, the changes in device current described in chapters 3 and 4 can be used as temperature sensors. Some initial work on single sensors with reasonable sensitivity >300 mV/°C in the subthreshold regime on glass and plastic substrates has been reported.[146, 147] However, in order to image using these devices,
integration into arrays will be necessary. Figure 85 (a) shows the mask layout for an 8x8 array with independently addressable devices. These arrays are currently being fabricated on plastic substrates and a setup to readout the devices will need to be developed. In addition to vastly improving the temperature sensitivity, it is interesting to integrate a material with a high pyroelectric coefficient. An example of this can be seen in Figure 85 (b) where a bilayer dielectric of lead-zirconium-titanate:lead-nickel-niobate (PZT:PNN) and PEALD Al₂O₃ is used. The PZT:PNN layer has a high dielectric constant and as a result the devices operate well at low voltage with steep subthreshold slopes. The temperature sensitivity as well as the ability to use these devices as memory TFTs should be explored.

![Image of mask layout for 8x8 array](image1)

![Image of ZnO TFT on PZT:PNN and Al₂O₃ buffer layer](image2)

**Figure 92** – (a) Layout for 8x8 array for temperature sensing ZnO TFTs on flexible substrates. (b) Initial results for ZnO TFTs on PZT:PNN (500 nm, εᵣ > 1000) and Al₂O₃ buffer layer (5 nm, εᵣ = 8). The subthreshold slope is ~100 mV/dec and mobility of 10-20 cm²/V·s is achieved at low voltage.

Overall, there are a variety of directions this work could continue towards, including both fundamental and applied research. As this work continues to grow, integration of these
oxide films into different types of applications will be essential. Preliminary work on implantable micro temperature sensors for seizure detection [147] as well as integration of PEALD Al2O3 onto III-V MOS-HEMTs [148, 149] suggest that a broad range of applications may benefit from high quality low-temperature deposited thin film oxides.
References


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**Paper and Presentations Resulting From This Work**
Papers


D. A. Mourey, D. A. Zhao, Y. V. Li, T. N. Jackson. “Contacts to Thin Film Transistors.” (Invited submission to *MRS Bulletin*).

D. A. Zhao, D. A. Mourey, T. N. Jackson. “Low 1/f noise in PEALD ZnO Transistors” (In preparation to be submitted to *IEEE Electron Device Letters*).

Y. Y. Li, D. A. Mourey, M. A. Loth, J. E. Anthony, T. N. Jackson. “Inkjet printed diF TES-ADT Thin Film Transistors.” (In preparation to be submitted to *Organic Electronics*).


Conference Presentations

1. D. A. Zhao, D. A. Mourey, H. R. Fok, Y. V. Li, T. N. Jackson. “ZnO Thin Film Transistors and Circuits on Flexible Substrates by Low-Temperature PEALD.” *Society for Information Display (SID) 2010*.


Vita

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