The Pennsylvania State University
The Graduate School
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ENGINEERING OHMIC CONTACTS TO III–V, III–N, AND 2D DICHALCOGENIDES: THE IMPACT OF ANNEALING AND SURFACE PREPARATION ON CONTACT RESISTANCE

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Abstract

A new era of smart interconnected systems of electronic devices has begun, with cloud computing (big data) and artificial intelligence amplifying the capacity and impact of these systems on human society. Behind this technological revolution lie Si-based complementary metal–oxide–semiconductor (CMOS) logic devices as well as high-power and high-frequency radio-frequency (RF) electronics, which are key enablers of the current progress. However, as we look into the future, the trend set by Moore's law for ever smaller, higher-performance, and more power-efficient devices is reaching its limit, and soon Si may no longer serve as the material of choice in some aggressively scaled transistors. For example, InGaAs is being considered as channel materials to replace Si. Similar efforts are also underway to replace Si with GaN in RF applications. Moreover, transition metal dichalcogenides such as MoS_2 are interesting for flexible electronics applications. As these new materials take hold, key processes such as contact metallization must be investigated and optimized in order to improve the performance of next-generation devices. This dissertation discusses studies of Ohmic contacts to GaN, InGaAs, and MoS_2, focusing on how surface preparation and annealing affect contact resistance.

During the first phase of this dissertation, we investigated Ti/Al contacts to N-polar GaN/AlGaN heterostructures. The resistance of Ti/Al-based contacts was found to depend sensitively on their interfacial composition. Limiting the thickness of the first layer deposited (either Al or Ti) to a few nanometers produced low contact resistances after annealing for 60 s at 500 °C. The lowest contact resistance of 0.10 Ω·mm (specific contact resistance, ρ_c, of 3×10^{-7} Ω·cm^2) was achieved with 3 nm of Al as the first deposited layer. Cross-sectional transmission electron microscopy (TEM) studies revealed a thin Ti–Al-Ga–N layer adjacent to the GaN in this annealed Al/Ti/Al contact, while the contact resistance was higher when the interfacial layer contained only Ti, Ga, and N. The simultaneous presence of Al and Ti next to GaN at the onset of reaction was found to be critical for achieving the lowest contact resistance.

Drawing from lessons learned about surface preparation and alloyed contacts to GaN, in the second phase of this dissertation, we investigated Ni-based alloyed contacts to InP-capped and uncapped n^+-$In_{0.53}Ga_{0.47}As$ ($N_D = 3\times10^{19}$ cm^{-3}). Contacts with specific contact resistances of $4.0 \times 10^{-8} \pm 7 \times 10^{-9}$ Ω·cm^2 and $4.6 \times 10^{-8} \pm 9 \times 10^{-9}$ Ω·cm^2 were achieved for the capped and uncapped

samples, respectively, after annealing at 350 °C for 60 s. By using a pre-metallization surface treatment of ammonium sulfide, ρ_c decreased further to $2.1 \times 10^{-8} \pm 2 \times 10^{-9}$ Ω·cm^2 and $1.8 \times 10^{-8} \pm 1 \times 10^{-9}$ Ω·cm^2 on epilayers with and without 10-nm InP caps, respectively. Cross-sectional TEM micrographs revealed that the ammonium sulfide surface treatment more completely eliminated the semiconductor's native oxide at the contact interface, which we believe caused the reduced contact resistance both before and after annealing.

In the third and final phase of this dissertation, alloyed Ag contacts to few-layer (FL)-MoS_2 were investigated. Similar to the two contacts investigated earlier in this dissertation, annealing was critical for achieving low contact resistance. The contact resistances of the as-deposited samples were 0.8–3.5 Ω·mm, while the annealed contacts exhibited lower contact resistances of 0.2–0.5 Ω·mm for MoS_2 from 5 to 14 layers or ~3 to 9 nm thick. TEM micrographs of the annealed contacts revealed that the Ag was epitaxial on MoS_2. Electron energy-loss spectroscopy (EELS) spectra collected near the Ag/MoS_2 contacts showed limited interdiffusion at the metal/semiconductor interface as well as the presence of Ag in the underlying MoS_2. Furthermore, thanks to the effective pre- and post-metallization surface preparation, no gross interfacial contaminants (oxygen and resist residue) appeared, indicating the formation of an intimate contact between the Ag and MoS_2.

Overall, this dissertation shows the importance of surface preparation and annealing in producing low-resistance Ohmic contacts to GaN, InGaAs, and MoS_2. Therefore, the contact metallization processes developed here may eventually aid in the development of next-generation electronics based on these semiconductors.

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Chapter 1

Introduction

1.1 Overview and motivation

In recent decades, we have witnessed a microelectronics revolution like no other. The emergence of the internet as a key information and communication venue along with the global adoption of personal computers and smartphones have accelerated the growth of microelectronic research and development. Now, we are at the verge of an even more exciting time for microelectronics. The emergence of cloud computing (big data) followed by a promising future for the internet of things along with the parallel development of self-driving electric vehicles, drones, and wearable electronics are opening up new opportunities, including military and space technologies. One important reason why these emerging technologies are interesting is that they all use arrays of sensors to collect data in real time. This data is shared between devices across multiple systems. Essentially, they are forming a digital ecosystem, continually communicating with each other and with the cloud servers gathering and processing data.[1]

Current and future interconnected systems of devices require at least two critical electrical components: logic operation (data processing and storage) and communication (RF noise, power and high-frequency operations) components. Both of these components use transistors as their main operating units. Transistors can be thought of as switches used for logic operations as well as for signal and power amplification. Most devices contain billions of these switches, depending on the application. To make cheaper, faster, and more power-efficient devices, the design and

fabrication of transistors must be improved. For example, microprocessors (the computational brain) used in laptop computers, smartphones, and servers must have high performance while remaining affordable. For the last few decades, this requirement was met by shrinking the transistors, doubling the number of transistors on a chip (integrated circuit) nearly every 18 months (**Figure 1-1**). As a result, the cost per chip decreased, the chip's clock frequency and the transistor's switching speed increased by orders of magnitude, and the operating voltage decreased following a similar trend.[2,3] This technology trend became known as Moore's law, named after Intel's co-founder Gordon Moore, who made the original projection.[4] Many passive components, such as radio-frequency (RF) devices, have followed Moore's law, though not at the same rate as microprocessors.[2,5]

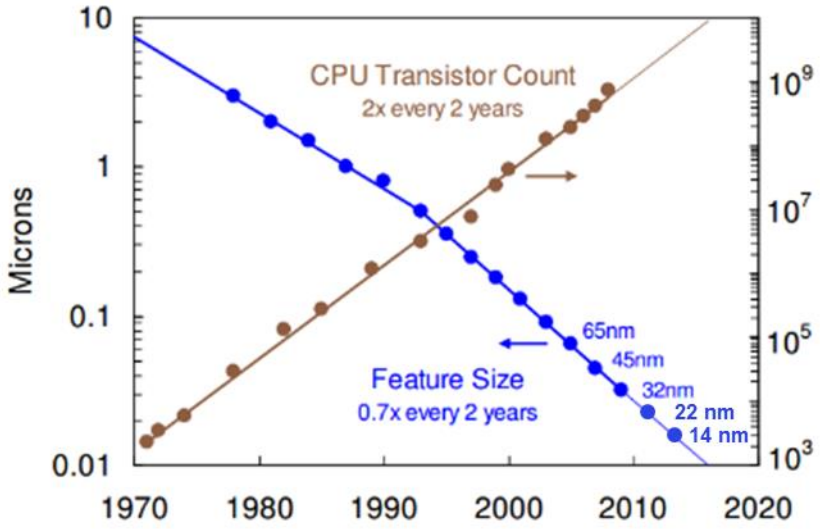

Figure 1-1 Moore's law scaling trend with technology node. Adopted from Holt *et al*.[6]

Despite the resilience of Moore's law for the past fifty years, now there is a consensus that we are approaching the fundamental material limits of Si, the material used to make most high-performance transistors.[2,3,7] With aggressive scaling of Si metal–oxide–semiconductor field-effect

transistors (MOSFETs), major challenges have emerged. Continued scaling has led to poor electrostatic control of the channel,[8] reduced channel mobility,[9] and increased source/drain series resistance,[10] which has limited progress. The reduced channel mobility and the short-channel effect have been partially mitigated by the adoption of non-planar tri-gate FinFET structures[8] along with high-κ dielectric[11] and strained Si/Ge technology.[12] However, scaling below the 10-nm technology node may require replacing Si with a new channel material that can achieve high ON currents at a lower supply voltage than that used in Si FinFETs.[13,14] Thanks to their high electron injection velocity, reasonably high channel density of states, and tunable heterostructures, III–V semiconductors such as InGaAs are prime candidates to replace Si in the very near future.[10,13]

Finding a replacement for Si in high-performance MOSFETs, however, is just one of the challenges ahead. With emergence of the internet of things and the possibility of billions of devices becoming interconnected wirelessly, it is now important to build robust, high-capacity wireless communication systems. Next-generation RF electronics used for communications, signal processing, and power management will require high-frequency microwave transistors. This is particularly true as standard wireless networks are upgraded from 4G to 5G, including the development of millimeter-wave functionality that allows for connections with high data density and high bandwidth.[15] To produce high-frequency microwave transistors such as those used in 5G networks, the power semiconductor industry is looking beyond the conventional technologies based on GaAs, Si/SiGe, and Si to group III nitrides such as GaN.[16,17,18] This is happening because GaAs and Si exhibit low breakdown electric fields of 0.4 MV/cm and 0.3 MV/cm, respectively.[19] In addition, Si exhibits a low electron saturation velocity of 1×10^7 cm/s, limiting its utility in high-power and high-frequency microwave transistors, which require high breakdown voltage and electron saturation velocity.[19,20]

In chapter 2, we will discuss two emerging materials, InGaAs and MoS_2. InGaAs could replace Si as a channel material in aggressively scaled transistors. Transition metal dichalcogenides such as MoS_2 are potential candidates to replace or complement silicon in applications such as flexible and wearable electronics. We will also discuss GaN, as it is already starting to replace GaAs, Si/SiGe, and Si in transistors used for high-power and high-frequency applications.

Despite the improved materials properties of emerging materials such as InGaAs and MoS_2 and the more-established GaN, some persisting challenges remain that are delaying the adoption of these materials in high-performance transistors. Aggressively scaled (gate lengths of less than 10 nm) InGaAs and MoS_2 MOSFETs as well as GaN HEMTs exhibit high source and drain (S/D) parasitic resistances, limiting their performance.[21-23] Among the parasitic resistances, the high S/D contact resistance between the metal and semiconductor plays a significant role (**Figure 1-2**). Moreover, as transistors scale down further, the ratio of S/D contact resistance to total parasitic resistance increases.[24] As contact dimensions are scaled down to a few nanometers, contact resistance increases by more than two orders of magnitudes over the required source and drain contact resistance of $<50\ \Omega\ \mu m$.[13,21,22] For the sub-32-nm CMOS technology node, the S/D contact resistance could be over 65% of the total parasitic resistance. Even though GaN-based HEMTs exhibit a less aggressive scaling trend than Si CMOS devices, the increase in contact resistance with scaling remains a threat to further improving performance.[22,25]

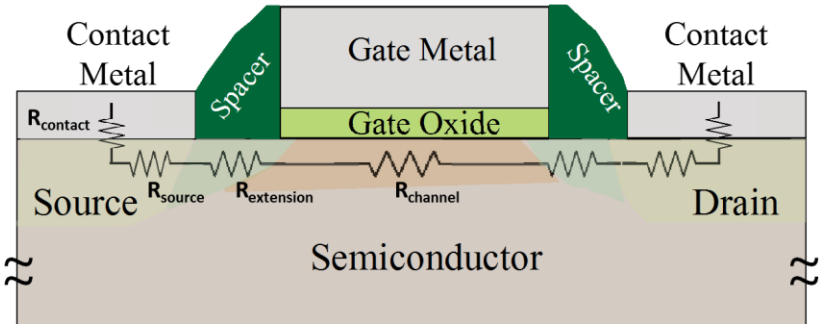

Figure 1-2 Cross-sectional view of a MOSFET with parasitic resistances.

As more and more electronics are embedded in hostile environments—such as server farms, cars, airplane engines, and industrial machinery—reliability issues related to operating temperature become a source of concern. Therefore, in addition to scaling, device processing and operation at high temperature should be considered, as high temperatures can affect device performance by increasing the contact resistance at the metal/semiconductor interface. Hence, developing scalable source and drain Ohmic contacts with low resistance, along with well-controlled morphology and thermal stability, is a major priority in order for any compound semiconductors to one day replace Si as a channel material, or for GaN to play a bigger role in the power semiconductor industry.

1.2 Research goal

In light of these challenges, we set out to explore and to develop methods for fabricating scalable, thermally stable, low-resistance Ohmic contacts to InGaAs, GaN/AlGaN HEMT heterostructures, and MoS_2. To achieve this goal, we focused on understanding, engineering, and optimizing three experimental processing conditions: surface preparation, metallization, and interfacial reaction between the S/D metal and the underlying semiconductor during annealing.

We found that these three processing conditions were critical in engineering the metal/semiconductors interfaces.

Before we delve into the details of the different metal/semiconductor processing conditions, however, it is important to first outline the underlying physics governing current transport across metal/semiconductor interfaces. The following sections give an overview of metal/semiconductor contacts, focusing on the origin of contact resistance at the interfaces of S/D contacts as it pertains to MOSFETs and HEMTs.

1.3 Metal/semiconductor contacts

1.3.1 Overview

Thin-film metallization plays an important role in the semiconductor industry because it is used to make direct electrical contact to semiconducting materials. Such contacts provide current paths in and out of semiconductor devices, such as transistors, connecting them to the outside world and to each other, as in integrated circuits.

Accordingly, there are at least two types of thin-film metallization: **contacts** (between metals and semiconductors in one device) and **interconnects** (between devices in an integrated circuit).[26,27] Contact metallization can further be classified in two categories: **Ohmic contacts** and rectifying **Schottky contacts**. This dissertation focuses on Ohmic contacts. An ideal Ohmic contact between a metal and a semiconductor exhibits no voltage drop across the contact, meaning the total resistance (R) across the metal/semiconductor interface is independent of the applied voltage (V) and current (I). Hence, an ideal Ohmic contact follows Ohm's law, $R = V/I$ = constant, and its I/V curve is linear. However, metal/semiconductor contacts are often not ideal due to the presence of interfacial layers, such as oxides or contaminants, which will be discussed in detail in

the following sections. As a result, the resistance across the metal/semiconductor interface is no longer independent of the applied voltage. However, if the voltage drop across the metal/semiconductor interface is negligible compared to that in the bulk metal and semiconductor active region (i.e., MOSFET channel), the contact does not affect the *I*–*V* characteristics of its device and the contact is still considered Ohmic. This behavior implies that metal/semiconductor interfaces are a key factor in the formation of low-resistance Ohmic contacts, which ultimately dictates device yield, performance, and reliability.

1.3.2 Metal–semiconductor interfaces and contact formation

Surfaces and interfaces are critical in many processes and applications, including contacts between materials, passivation, chemical cleaning, and etching.[28] Similarly, surfaces and interfaces are ubiquitous in microelectronic devices such as transistors. Almost all basic functions of transistors rely on multiple contact interfaces between various materials: metals, semiconductors, and oxides (see **Figure 1-2**). During typical transistor operation (when used as a switch), current flows from the source across a metal/semiconductor contact to the drain via a semiconducting channel. In a MOS transistor, voltage applied to the gate (metal/oxide/semiconductor junction) modulates the current flow through the channel, determining the on state (channel is present) and the off state (no channel).[29] The metal/semiconductor interfaces in a transistor may limit the on-state current by impeding mobile charge carriers across the interface, which increases the interfacial on-resistance and power dissipation, degrading device performance. Hence, it is critical to study the semiconductor surface before metallization and to understand the physical and chemical mechanisms behind the formation of metal/semiconductor contacts.

1.3.2.1 The Schottky–Mott model

Figure 1-3 shows a schematic energy band diagram before and after a metal and an n-type semiconductor are brought into contact. This model, put forward by Walter H. Schottky and Nevill Mott in 1938, provides a simple yet reasonably accurate description of an ideal metal/semiconductor contact. The Schottky–Mott model assumes that the metal and semiconductor surfaces are atomically clean with no surface states present and that the semiconductor is non-degenerately doped. Immediately before the two different materials are brought into contact (see **Figure 1-3**a), they are electrically neutral and physically separated. In **Figure 1-4**a, ϕ_M is the metal work function, which is the amount of energy required to excite an electron from the Fermi level (E_F) to the vacuum level (E_{vac}, the energy level of a completely free electron) outside the surface of the metal.[30] Similarly, ϕ_{sc} is the work function of the semiconductor, while χ_{sc} (the electron affinity of the semiconductor) is the potential difference between the bottom of the conduction band (E_c) and E_{vac} outside the surface of the semiconductor. E_v is the top of the valence band edge of the semiconductor.

When the metal and the semiconductor are physically separated, their energy bands remain flat. In the case shown in **Figure 1-3**a, the Fermi level of the n-type semiconductor ($\phi_{sc} < \phi_M$) is at a higher energy than that of the metal. The moment when the metal and semiconductor are brought into contact, electrons at the higher energy in the semiconductor flow into the metal, forming a depletion layer at the semiconductor surface that is void of mobile charges (see **Figure 1-3**b). The depletion layer is composed of static, uncompensated positive donor ions. The potential difference between the surface of the metal (−) and the depletion layer (+) creates an internal electric field. This behavior establishes thermal equilibrium, where the Fermi levels of the two materials coincide. Accordingly, the semiconductor energy bands bend up in the depletion layer, forming an

energy barrier at the interface. The height of this energy barrier, known as the Schottky barrier, depends on the potential difference between the metal work function and the semiconductor electron affinity, as given by Equation 1.1 for an n-type semiconductor. [30,31]

$$\phi_{SB} = \phi_M - \chi_{sc} \qquad [1.1]$$

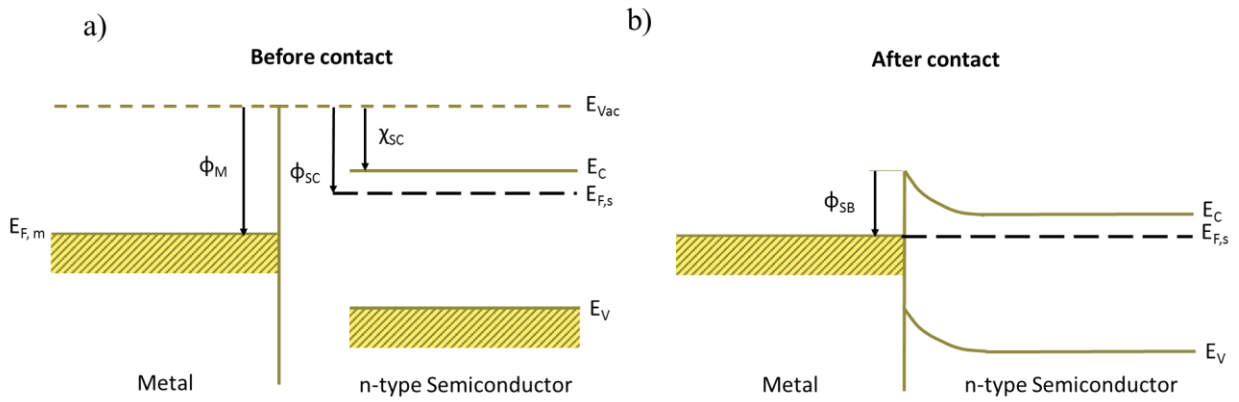

Figure 1-3 Schematic of electron energy band diagrams for a metal and semiconductor, according to the Schottky–Mott model (a) before and (b) after the two materials are brought into contact. Adopted from Brillson *et al.*[28]

After thermal equilibrium is reached, electrons in the metal must overcome the Schottky barrier to move across the interface. Hence, one way to enhance electrical current transport across a metal/semiconductor interface is to reduce the barrier height to zero by choosing a metal whose work function matches the electron affinity of the contacted semiconductor. However, in practice it is not trivial to modulate the Schottky barrier height by only varying the work function of the metal.[21,30,32] In fact, for most metal/semiconductor contacts, including those investigated in this dissertation, the barrier height only depends weakly on the work function of the metal. Multiple experiments have shown that the assumptions of the Schottky–Mott model—that the metal and semiconductor surfaces are clean and free from imperfections—do not hold for most materials systems.[28] On the contrary, most semiconductor surfaces, including those investigated here,

contain defects and imperfections that play an outsize role during contact formation, undermining the influence of the metal work function. The contact metal itself may also be a source of defects at the semiconductor surface, as we will see later.

The work functions of both the metal and semiconductor, as well as the electron affinity, are sensitive to surface dipoles, surface defects, and interfacial layers.[28,30] Surface dipoles originate from the nonsymmetric distribution of electron charge around the atoms near the surface, which means the centers of negative and positive charges do not coincide, producing a surface dipole layer. Meanwhile, surface imperfections come from surface atoms being arranged differently from bulk atoms. In a crystalline semiconductor such as Si or InGaAs, all bulk atoms are covalently bonded to their neighbors and there are no dangling bonds. In contrast, surface atoms are bonded only on one side, leaving them with uncompensated valence electrons or dangling bonds that act as donors or acceptors. (Transition metal dichalcogenides such as MoS_2 may be exceptions. See chapter 5). When exposed to atmospheric conditions, these dangling bonds make the semiconductor surface susceptible to surface relaxation and reconstruction, as well as to adsorption of chemical species such as carbon, hydrocarbon, and oxygen. These foreign species form interfacial layers, with thicknesses of a few atomic layers, that are often defective.[28,30] Ultimately, the presence of interfacial layers, surface dipoles, and defects such as vacancies change the density and occupation of states at the interface, often introducing local energy states within the band gap of the semiconductor. In this case, band bending occurs even without a metal contact, as electrons from the semiconductor fill the local surface states (see **Figure 1-4**a). This reality means that the height of the Schottky barrier is only weakly affected by the metal work function once the metal and semiconductor are brought into contact (see **Figure 1-4**b).

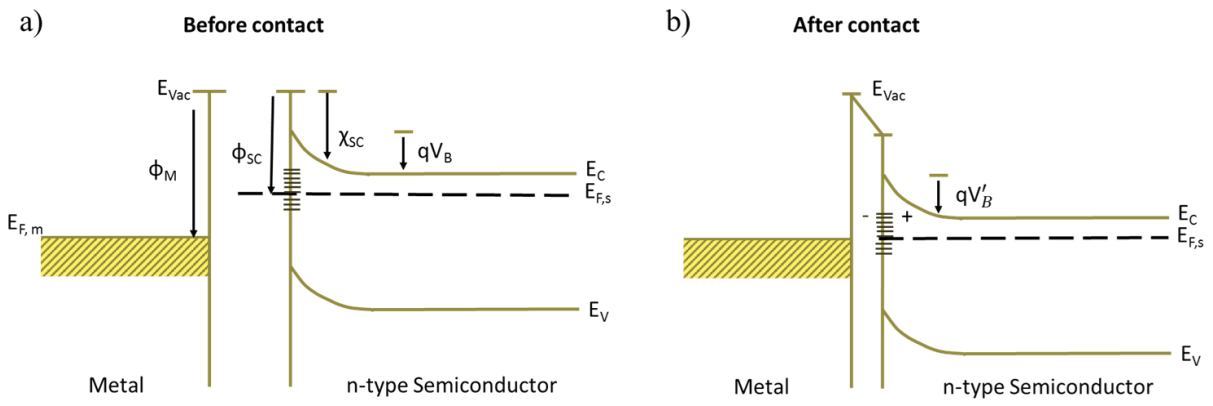

Figure 1-4 Schematic diagrams of metal and semiconductor electron energy bands, according to the Bardeen model (a) before and (b) after the two materials are brought into contact. Adopted from Brillson *et al*.[28]

1.3.2.2 The Bardeen limit and Fermi level pinning

To further explain the role of surface/interface states, John Bardeen in 1947 proposed the following model where the Schottky barrier height can be approximated by:[33]

$$\phi_{SB} = E_b - \phi_0 \qquad [1.2]$$

where E_b is the band gap energy and ϕ_0 is the charge neutrality level. ϕ_0 is described as the energy level (measured from the top of the valence band) at which the surface or interface is electrically neutral. To keep the metal/semiconductor interface neutral, negative charge on the metal surface must be balanced by positive charge in the depletion layer of the semiconductor. In the presence of the surface or interface states, the net charge from these states must be taken into account to achieve charge neutrality. Therefore, when the surface or interface states contain a net positive charge, ϕ_0 is positioned above E_F. As result, the amount of positive charge in the depletion region decreases to maintain charge neutrality. This behavior decreases band bending, which decreases the Schottky barrier height. The opposite happens if the net surface/interface charge is negative.

With this decreased or increased band bending, E_F respectively moves up or down (within a narrow energy range) to accommodate the band bending and preserve the charge neutrality of the interface. However, if the density of surface states is large enough (~10^{14} cm^{-2}), $\phi_0 \approx E_F$, so that any change in charge density is absorbed by these states.[28,34] Consequently, most of the potential difference (qV_B) between the metal and the semiconductor would not move the Fermi level because the surface states get filled or emptied instead. Hence, the Fermi level is said to be "pinned" by the surface states within a narrow range of energy in the semiconductor band gap (see **Figure 1-4**b).

1.3.2.3 Metal-induced gap states (MIGS)

In addition to surface/interface states, the metal contact itself has been suggested as a cause of Fermi level pinning. In 1965, Volker Heine proposed that when a metal and a semiconductor come into contact, the intrinsic surface states of the semiconductor will be immediately replaced by "metal-induced gap states" or MIGS.[30,31,35] MIGS originate from the tailing or attenuation of the conduction electron wave function in the metal into the band gap of the semiconductor at the interface. The tail of the metal wave function can extend several atomic layers into the semiconductor.[30,35] Similar to surface states, MIGS in high densities—which have been shown to be present at least in selected metal/semiconductor contacts[36]—can cause strong pinning of the Fermi level.

Contact preparation and processing conditions may also cause Fermi level pinning or change the Schottky barrier height.[30,37] During metal deposition, for example, energetic atoms may bombard the semiconductor surface, generating defects such as vacancies and anti-sites (atoms in incorrect sites), or they may cause interdiffusion between the metal and semiconductor.[38,39]

Vacancies and other defects generated through these processes can then create acceptor- or donor-like states at the metal/semiconductor interface, pinning the Fermi level through the mechanism postulated by Bardeen. Likewise, metallization and other contact processing steps such as annealing can cause interdiffusion and reaction between the metal and semiconductor, producing new interfacial compounds. These reaction products may have work functions different from the contact metal, or they may dope the underlying semiconductor, altering the effective Schottky barrier height and width at the contact interface.

Though Fermi level pinning and these surface/interface states that affect the Schottky barrier are obstacles to engineering ultra-low-resistance Ohmic contacts, they also provide ample opportunities to fine-tune metal/semiconductor interfaces. Through careful surface preparation and metallization, the surface and interface states can be mitigated or even turned advantageous.[40,41] This dissertation work provides examples of how such routes are key to engineering microstructurally and electrically uniform, thermally stable, and environmentally robust low-resistance Ohmic contacts to three compound semiconductors of technological relevance: GaN, InGaAs, and MoS_2. Fermi level pinning is common in these compound semiconductors, so it is not viable to produce low-resistance Ohmic contact by engineering the metal work function alone. Thus, any metal/semiconductor interface engineering must involve not only lowering the Schottky barrier height but also thinning its width. As such, it is important to understand the mechanisms of current transport over and through the barrier.

1.3.3 Current transport mechanisms

There are at least two current conduction mechanisms across a metal/semiconductor interface: thermionic emission (TE) and field emission (FE). When these two mechanisms work

simultaneously, this is called thermionic field emission (TFE). FE and TFE are the preferred current transport modes in Ohmic contacts.

i) **Thermionic emission (TE)** occurs at low to moderate doping ($N_D \leq 10^{17}$ cm^{-3} for Si),[32] where the depletion width (W_d) of the semiconductor is wide enough that the only way for majority carriers (electrons for n-type semiconductors) to move across the metal/semiconductor interface is to be thermally excited above the Schottky barrier (**Figure 1-5**a).

ii) **Field emission (FE)** occurs at high doping ($N_D > 10^{20}$ cm^{-3} for Si),[32] where W_d is thin enough that the majority carriers (electrons for n-type semiconductors) tunnel through the Schottky barrier (**Figure 1-5**b). In most metal/semiconductor contacts, only the region of the semiconductor right under the contact is heavily doped compared to the rest of the semiconductor, as shown in **Figure 1-5**c.

iii) **Thermionic field emission (TFE)** occurs at moderately high doping ($10^{17} < N_D < 10^{20}$ cm^{-3} for Si),[32] where W_d is moderately thin, such that both TE and FE contribute to current conduction across the metal/semiconductor interface (**Figure 1-5**d).

We can easily identify the dominant current transport mechanism in a metal/semiconductor contact by comparing the thermal energy, $k_B T$ (k_B is the Boltzmann constant), to the characteristic energy for tunneling, E_{00}.[42,43]

$$E_{00} = \frac{qh}{4\pi}\sqrt{\frac{N_D}{m_t^* \varepsilon_s}} \qquad [1.3]$$

where q is the charge of an electron, h is Planck's constant, N_D is the doping concentration, m_t^* is the effective mass of the tunneling charge carrier (electron), and ε_s is the permittivity (static dielectric constant) of the semiconductor. For $\boldsymbol{k_B T >> E_{00}}$, TE is the dominant mechanism, so

the contact behaves as a Schottky diode. For $k_BT << E_{00}$, FE dominates, and tunneling current increases exponentially with doping concentration. For $k_BT \approx E_{00}$, both TE and FE contribute, making TFE dominant.

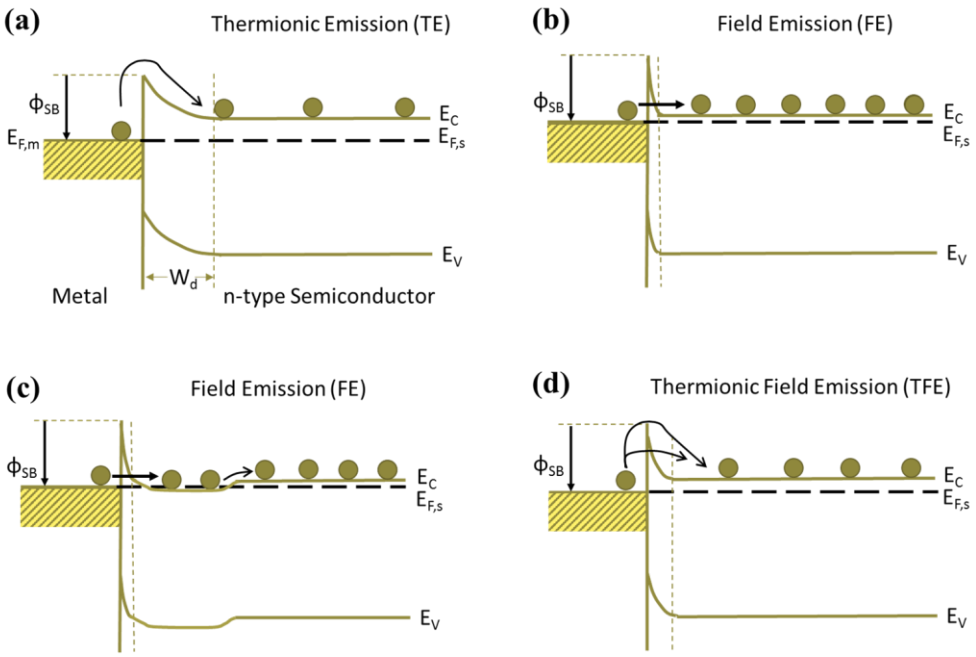

Figure 1-5 Schematics of metal and semiconductor electron energy bands showing the different current conduction mechanisms: (a) thermionic emission; (b) field emission; (c) field emission for a contact where only the semiconductor right under the contact is heavily doped compared to the rest of the semiconductor; (b) thermionic field emission. Adopted from Schroder *et al.*[32]

The depletion width for an n-type semiconductor can be approximated using the following equation:[29,44]

$$W_d = \sqrt{\frac{2\varepsilon_s (V_{bi} \pm V_A)}{qN_D}} \qquad [1.4]$$

where V_{bi} is the built-in voltage and V_A is the applied voltage. To clarify, qV_{bi} is the built-in potential barrier seen by the electrons in the semiconductor as they try to move across the metal/semiconductor interface, and it is a direct consequence of band bending. Note that W_d is proportional to $1/\sqrt{N_D}$, so the depletion width decreases with increasing doping concentration. As

the depletion width decreases, the field-emission (tunneling) current across the metal/semiconductor increases because electrons can now easily tunnel through the thin barrier.

1.3.3.1 Measuring the Schottky barrier height

To completely understand current transport across a metal/semiconductor interface, it is also important to know the effective barrier height, which can be found through temperature-dependent current–voltage measurements. Based on the thermionic emission theory, the thermionic current density and voltage characteristic is given by:[28,32]

$$J = J_s \left[\exp\left(-\frac{qV}{nk_BT}\right) - 1\right] \quad [1.5]$$

where J_s is the saturation current density, V is the applied voltage $\left(\geq \frac{3k_BT}{q}\right)$, T is the temperature, and n is the ideality factor. J_s is expressed as:

$$J_s = A^*T^2 \exp\left(\frac{-q\phi_{SB}}{k_BT}\right) \quad [1.6]$$

where A^* is known as the Richardson constant for thermionic emission:

$$A^* = \frac{4\pi q m^* k_B^2}{h^3} \quad [1.7]$$

Published values of A^* for various materials can be obtained from various sources.[31,32] Given A^*, the effective Schottky barrier height ϕ_{SB} can be found by *J–V–T* measurements as a function of temperature, usually from <77 K to >300 K. From the slope of $\ln(1/T^2)$ versus $1/T$, known as a Richardson plot, we can calculate ϕ_{SB}. However, this technique also requires knowing the ideality factor *n*, unless *J–V–T* measurements are conducted at various applied voltages. For a more detailed overview of *J–V–T* and other barrier height extraction techniques, see Schroder.[32]

1.3.3.2 The specific contact resistance

Even with the knowledge of the dominant current transport mechanism and a reasonable estimation of ϕ_{SB}, a parameter known as specific contact resistance, ρ_c, (measured in $\Omega \cdot cm^2$) is used as a figure of merit for Ohmic contacts. It is defined as the inverse of the derivative of current density as a function of voltage at zero bias:

$$\rho_c = \left(\frac{\partial J}{\partial V}\right)^{-1}\Big|_{V=0} \quad [1.8]$$

Specific contact resistance is used to characterize not just the metal/semiconductor interface but also nearby regions below and above the interface. Low ρ_c indicates less resistance to current transport across the interface and good Ohmic contact. Specific contact resistance is a particularly useful parameter to compare Ohmic contacts of different sizes, as it is independent of contact area.[32,42,44]

From Equation (1.3) and (1.5), the specific contact resistance for the three current conduction mechanisms are expressed as follows:

For TE,

$$\rho_c \propto \exp\left(\frac{q\phi_{SB}}{k_B T}\right) \quad [1.9]$$

For TFE,

$$\rho_c \propto \exp\left(\frac{q\phi_{SB}}{E_{00}\coth(E_{00}/k_B T)}\right) \quad [1.10]$$

and for FE,

$$\rho_c \propto \exp\left(\frac{q\phi_{SB}}{E_{00}}\right) \quad [1.11]$$

The effect of doping concentration N_D and barrier height ϕ_{SB} on ρ_c can then be easily expressed by substituting for E_{00} in Equation (1.11):

$$\rho_c \propto \exp\left(\frac{2\sqrt{\varepsilon_s m_n^*}}{\hbar} \cdot \frac{\phi_B}{\sqrt{N_D}}\right) \qquad [1.12]$$

This equation shows that the specific contact resistance of a metal/semiconductor contact depends strongly on ϕ_{SB} and N_D. Therefore, in the presence of Fermi level pinning, the main method to lower ρ_c is to increase the doping concentration in the semiconductor.

Moreover, forming contacts with a low Schottky barrier is more difficult in wide-band-gap semiconductors such as GaN than in conventional semiconductors such as Si. Accordingly, in such systems the specific contact resistance is decreased instead by surface preparation and metallization techniques. These contact engineering techniques may create heavily doped surface layers, remove or displace defective interfacial layers (i.e., residual oxides or contaminants), and may create interfacial phases with low resistivity, enhancing tunneling current.[26,28,30] From a practical point of view, these techniques are cost-effective alternatives to epitaxial regrowth techniques, which are commonly used to grow heavily doped layers in the contact region.[45,46,47] Hence, in this dissertation work we mainly lowered the contact resistance by surface preparation and carefully engineered metallization. Now, the question is: how do we measure ρ_c?

1.3.4 Extracting contact resistance using the transfer length method (TLM)

The transfer length method (TLM) is a common way to measure the specific contact resistance of metal/semiconductor contacts.[32,48] The basic TLM test structure consists of rectangular metal pads deposited on a semiconductor (see **Figure 1-6**). Typically, TLM structures have more than three contacts pads, with different spacings (*d*) between the contacts.[32] TLM

assumes that current flows laterally from one contact edge to another. Therefore, the region where the contacts are located is isolated from the rest of the substrate so that the contacts sit on a mesa. In **Figure 1-6**a and **Figure 1-6**b, W is the width of a contact pad, L_c is the length of a contact pad, and Z is the mesa width, where $Z \approx W$ in an ideal TLM structure. In this dissertation work, all contacts were fabricated simultaneously using the same processing conditions, so they are assumed to be identical.

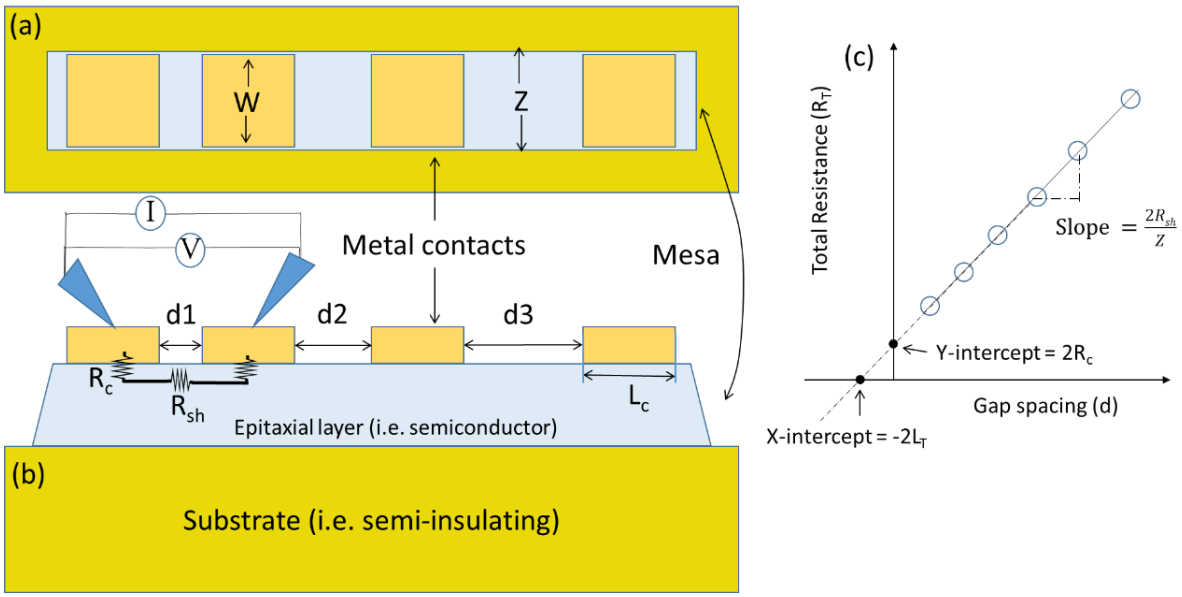

Figure 1-6 Schematic of a transfer length method test structure: (a) top view, (b) cross-sectional view. (c) Plot of total resistance versus contact gap spacing, showing all the electrical parameters that can be extracted from the plot.

To measure the contact resistance using a TLM test structure, current is sourced between two adjacent contact pads, and the voltage drop across the gap between the contacts is measured (**Figure 1-6**b). If the I–V curve is linear, using Ohm's law one can extract the total resistance (R_T). Plotting the total resistance versus the gap spacing (d) between contact pads yields a linear plot described by the following equation (**Figure 1-6**c).[43,49]

$$R_T = 2R_c + \frac{R_{sh}d}{W} \quad [1.13]$$

where R_c is the contact resistance (in Ω) and R_{sh} is the sheet resistance (in Ω/□). The slope of the R_T–d plot yields R_{sh}/W (W is independently measured), and the y-intercept corresponds to $2Rc$. Once R_c is known, the specific contact resistance is given by:

$$\rho_c = \frac{R_c L_c W}{\coth\left(\frac{L_c}{L_T}\right)} \quad [1.14]$$

where L_T is the transfer length, which is the length over which most (~63%) of the current is transferred from the metal to the semiconductor and vice versa (see **Figure 1-8**). The transfer length can be extracted from the x-intercept of the R_T–d plot, as shown in **Figure 1-6**c:

$$L_T = \sqrt{\rho_c / R_{sh}} \quad [1.15]$$

For $L_c \geq 1.5L_T$, which is true for all contacts investigated here, $\coth(L_c/L_T) \approx 1$ such that the effective contact area $A_{eff} = L_T W$ is smaller than the actual contact area $A_c = L_T W$. In this case, ρ_c can be approximated by:

$$\rho_c \approx R_c L_T W \quad [1.16]$$

As shown in Equations (1.13 to 1.16), TLM assumes that the sheet resistance of the semiconductor under the contacts is the same as that between the contacts. However, this assumption is not always valid, particularly for alloyed contacts where the semiconductor under the contact is modified during contact fabrication (see **Figure 1-7**).

A workaround to meet the TLM assumption is to use a thick epilayer while ensuring that only a small portion of the semiconductor is consumed by the alloying reaction.[50] In this case, the reaction depth must be accurately measured so that the reacted portion of the semiconductor can

be accounted for. We use this approach for the reacted Ni contacts to InGaAs epilayers investigated in this dissertation.[51] Alternatively, when there is extensive reaction between the metal and the semiconductor under the contact, or when there is limited knowledge of how the semiconductor under the contact is modified, one may decide to use R_c instead of ρ_c as a figure of merit for the metal/semiconductor contact. We use this approach for the reacted Ag contacts to exfoliated MoS_2 crystals investigated here. Here, R_c is described by:

$$R_c = \frac{2R_{sk}L_{Tk}}{W} \text{ so that } \quad R_T = \frac{2R_{sk}L_{Tk}}{W} + \frac{R_{sh}d}{W} \qquad [1.17]$$

In this modified expression for R_c, R_{sk} is the sheet resistance of the semiconductor under the contact, and $L_{sk} = \sqrt{\rho_c/R_{sk}}$. Therefore, R_{sk} must be known in order to extract ρ_c, while such information is not necessary in order to extract R_c. Typically, a more complex technique known as the end-resistance method can be used to determine R_{sk} and L_{sk}, allowing ρ_c to be calculated.[32,52,53] In this dissertation work we did not use the end-resistance method due to its complexity, though it remains a valuable technique for extracting the specific contact resistance of alloyed contacts unless the end resistance becomes too low to easily measure. To read more about the end-resistance method and for a complete derivation of Equations (1.13 to 1.17), refer to Schroder.[32]

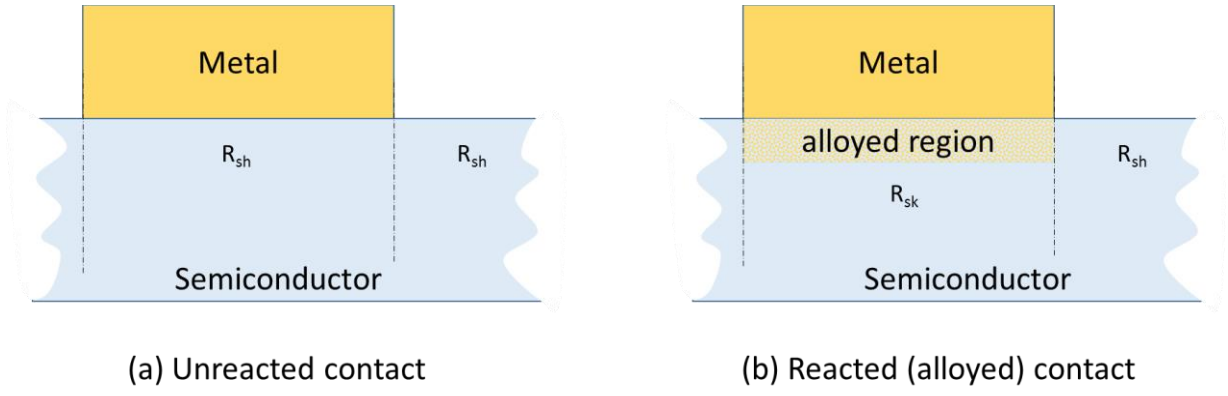

Figure 1-7 Schematic of (a) unreacted and (b) reacted contacts. Adopted from Shur *et al*.[53]

1.3.4.1 Additional considerations for using the transfer length method (TLM) to extract accurate specific contact resistances

Until now, only the specific contact resistance and the semiconductor sheet resistance have been considered as the main components of the total resistance (R_T) measured using a TLM test structure. However, when only two probes (**Figure 1-8**a) are used to source current and measure voltage at the same time, the probe resistance will contribute to R_T and could become a major source of error while extracting *Rc*. This concern is particularly serious for contacts to highly doped semiconductors with very low sheet resistance (such as n^+-InGaAs), but it is not a major concern for the highly resistive MoS_2 crystals investigated in this dissertation.[54,55] To measure such highly doped samples, we instead used a four-probe Kelvin technique, where two probes source current while the other two probes measure voltage using a high-impedance voltmeter (see **Figure 1-8**b).[56] Because the high-impedance voltmeter draws very little current, the voltage drop across the probes is reduced, becoming negligible for most practical applications. The four-probe technique also reduces the spreading resistance and the probe/metal contact resistance, which are also assumed to be negligible.

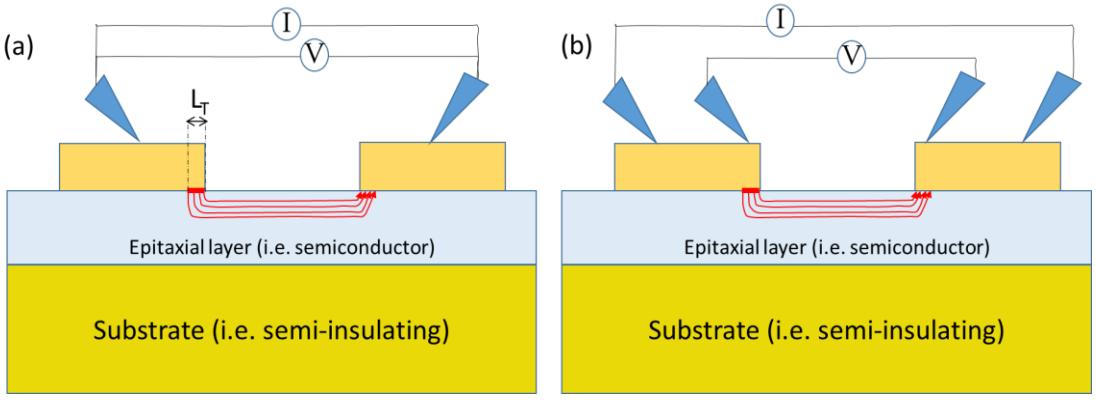

Figure 1-8 Schematic of the (a) two-probe and (b) four-probe methods used to source current and measure voltage using TLM test structures.

In addition to the probe resistance, a high contact metal sheet resistance can be a source of appreciable errors, often leading to overestimation of the specific contact resistance.[55,57,58] With high contact metal sheet resistance, the measurement of contact resistance becomes sensitive to probe placement, leading to unreliable and irreproducible results. To mitigate the effect of metal sheet resistance, often a stack of overlay metals is deposited over the contact metal. This stack consists of a thick and highly conductive Au layer, a thinner Pt diffusion barrier layer, and a Ti adhesion layer. The overlay metal stack lowers the resistivity of the contact metal, allowing for a more consistent and reliable measurement of contact resistance. In this dissertation work, we used an even more intricate TLM test structure, dubbed "refined TLM" (RTLM), in order to more accurately extract the specific contact resistance.[55] This method uses an optimized four-probe TLM test structure along with applied overlay metal stack, as discussed earlier, which allowed us to measure specific contact resistances below 10^{-8} $\Omega \cdot cm^2$. More details about RTLM are provided in chapter 4, where we discuss Ni contacts to heavily doped n-InGaAs.

1.3.4.2 Circular transmission line method (CTLM)

One important drawback of the TLM test structure is that it requires the isolation of the contact region using a mesa etch, which adds another lithography step, increasing cost. However, an alternative test structure known as the circular transfer length method (or circular transmission line method) can be used instead, at least for cases where other resistances are much larger than the contribution from metal sheet resistance.[32,58] As its name implies, a CTLM test structure consists of circular inner metallic pads with radius L separated from an outer metal field by gaps (where there is only semiconductor) of varying sizes (**Figure 1-9**). CTLM test structures can be fabricated using only one lithography step, not two. In addition, any error arising from the TLM

assumption that $W = Z$ (contact width equals mesa width) is avoided in CTLM. In CTLM test structures, current can only flow from the inner contact pads to the surrounding metal.

CTLM test structures can be studied with the four-probe method: two probes source current between the inner circular contact pad and the surrounding metal, while the other two probes measure the voltage drop across the gap (**Figure 1-9**a). All assumptions of TLM still hold in CTLM, mainly that the sheet resistance of the semiconductor under the metal is the same as the sheet resistance of the semiconductor in the gap. It also assumes that the metal sheet resistance and the probe resistance are negligible and that the inner contact pads and the outer metal field are equipotential surfaces.[58] Assuming all these assumptions are met, the total resistance between the inner circular contact pad and the surrounding metal is given by:

$$R_T = \frac{R_{sh}}{2\pi}\left[\frac{L_T}{L}\frac{I_0(L/L_T)}{I_1(L/L_T)} + \frac{L_T}{L+d}\frac{K_0(L/L_T)}{K_1(L/L_T)} + \ln\left(1+\frac{d}{L}\right)\right] \quad [1.18]$$

where R_{sh} is the sheet resistance of the semiconductor in the gap, L_T is the transfer length, L is the radius of the circular inner contact, and d is the gap spacing. Meanwhile, I_0, I_1, K_0, and K_1 are the modified Bessel functions arising from the circular geometry of the contact. Unlike the common practice for TLM, the R_T–d curve in CTLM is not linear and cannot be fit with a linear regression function. Here, we used an Excel solver function to extract Rc, L_T, R_{sh}, and ρ_c. For more details on this Excel solver, refer to the thesis by Downey *et al*.[59]

In summary, in this dissertation work we used TLM, RTLM, and CTLM test structures as needed to extract the specific contact resistance, within the limits of processing constraints, data accuracy, and cost. Therefore, for the Ti/Al contacts to N-polar GaN/AlGaN heterostructures, we used the CTLM test structure. For the Ni contact to InGaAs, we used the RTLM test structure; for Ag contacts to MoS_2, we used the TLM test structure with the two-probe method.

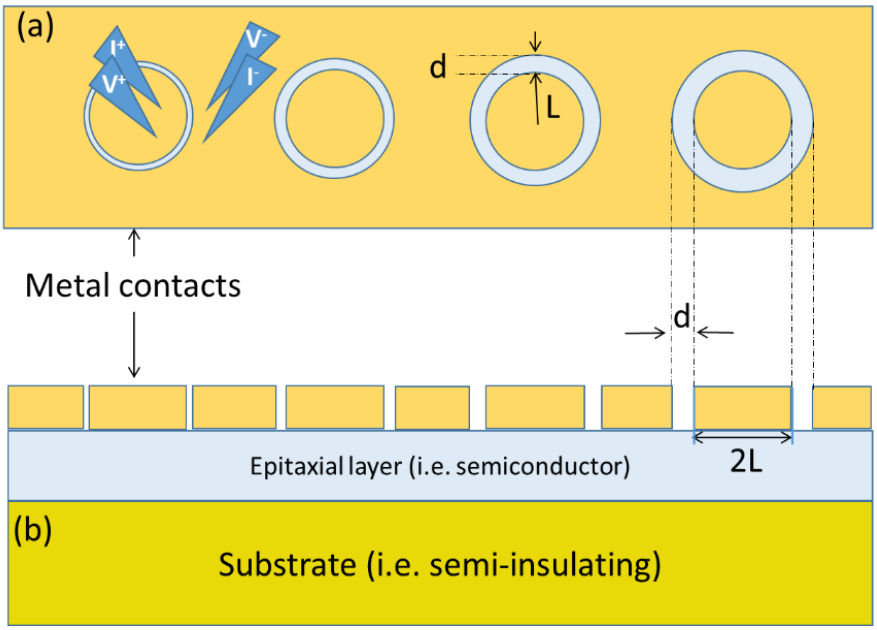

Figure 1-9 Schematic of a test structure for the circular transfer length method: (a) top view, (b) cross-sectional view.

1.4 Dissertation outline

This dissertation is divided into six chapters.

Chapter 1 describes the motivation behind this research and provides an overview of metal/semiconductor contacts, focusing on how to produce low-resistance Ohmic contacts, what factors are in play, and what main methods are used to extract the contact resistance experimentally.

Chapter 2 introduces the three material systems investigated in this dissertation: N-polar GaN, InGaAs, and MoS_2. Key material properties are described, and important material parameters are presented.

Chapter 3 discusses the successful development of Ti/Al-based contacts to an N-polar GaN/AlGaN HEMT heterostructure, focusing on how the compositions of interfacial compounds

affected the specific contact resistance. Contacts to Ga-polar and N-polar GaN are compared in order to highlight the effects of crystal orientation and polarity.

Chapter 4 describes encouraging results for self-aligned Ni-based contacts to n-InGaAs thin films, emphasizing the surface preparation techniques required to produce low-resistance Ohmic contacts.

Chapter 5 discusses alloyed Ag contacts to MoS_2, highlighting how annealing affects the contact resistance and the characteristics of field-effect transistors. Detailed contact processing techniques are presented.

Chapter 6 summarizes the research project, highlighting key achievements while outlining advice for future experimental work.

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Chapter 2

Materials Background

2.1 Overview

III–V semiconductors, primarily InGaAs, have emerged as primary candidates to replace Si as a channel material.[1,2] InGaAs is particularly attractive because it exhibits high electron mobility, high electron injection velocity, good interfacial quality with high-K dielectrics, and a sufficient band gap for use in logic transistors. The electron mobilities of InGaAs and InAs are up to ten times higher than that of Si at a comparable sheet density (see **Table 2-1**).[1] The higher mobility and injection velocity of InGaAs would allow for reduced operating voltage, while offering further scalability without compromising the superior electrostatic control provided by non-planar 3D structures. However, doubt remains about which material will replace Si in the long term. The International Roadmap for Semiconductors (ITRS)—which provides guidance to the semiconductor industry by collecting technological data and predicting future technology trends and requirements—has endorsed two-dimensional (2D) transition metal dichalcogenides such as MoS_2, WS_2, and WSe_2 as candidates to replace Si, particularly in niche applications such as sensors and flexible electronics.[3]

Table 2-1 Properties of semiconductors used in MOSFETs.[4-7]

Property	Si	Ge	$In_{0.53}Ga_{0.47}As$	MoS_2
Band Gap, E_g (eV)	1.12	0.67	0.75	1.2*
Electron mobility ($cm^2/V{\cdot}s$)	1,350	3900	>8000	>200
Hole mobility ($cm^2/V{\cdot}s$)	480	1900	350	480
Electron effective mass (m_e)	0.26	0.12	0.041	0.45
Lattice mismatch to Si	0	4%	8%	N/A
		pMOSFET	nMOSFET	***Tunable**

Gallium nitride (GaN) has emerged as a material of choice for future high-power and high-frequency transistors.[8,9,10] Unlike InGaAs, which has yet to replace Si in MOSFETs, GaN-based high-electron-mobility transistors (HEMTs) have already started to compete with GaAs HEMTs and Si laterally diffused MOSFET (LDMOS) devices.[10,11,12] GaAs HEMTs and Si LDMOS devices are the workhorses of the power electronics industry, particularly in RF power amplifiers, base stations of wireless communication systems, and ultra-high-frequency (UHF) and L-band power amplifiers in broadcast, communications, and radar systems.[8,10,11] GaN HEMTs, given their superior performance, are expected to disrupt the dominance of both GaAs- and Si-based technologies.[10,11]

Due to its wide band gap, GaN exhibits high breakdown voltage, which lets it operate at high voltages. GaN also exhibits high electron saturation velocity, over 2X higher than that of Si (see **Table 2-2**). This property allows GaN HEMTs to operate at high frequencies. Moreover, GaN possesses a unique advantage over other wide-band-gap semiconductors such as SiC: it can form heterojunctions with semiconductor alloys in the same family. Indeed, this advantage is what allows AlGaN/GaN and GaN/AlGaN HEMT heterostructures to be fabricated.[13] Accordingly, a high electron concentration is induced at the AlGaN/GaN or GaN/AlGaN interface, yielding a

high-mobility two-dimensional gas (2DEG) channel. The combination of high breakdown voltage, high electron saturation velocity, and 2DEG channels with high carrier density makes GaN HEMTs uniquely suited for high-power, high-frequency applications (up to the millimeter wave regime) needed for future 5G networks.[10,11,13]

Table 2-2 Properties of semiconductors used in high-frequency, high-power electronics applications at 300 K.[14,15]

Property	Si	GaAs	GaN	4H-SiC
Band gap, E_g (eV)	1.12	1.42	3.25	3.25
Breakdown field, E_{br} (MV/cm)	0.3	0.4	3.0	3.3
Electron mobility ($cm^2/V{\cdot}s$)	1350	8500	1500 (2DEG)	700
Electron saturation velocity, V_{sat} (10^7 cm/s)	1.0	2.0	2.5	2
Thermal conductivity (W/cm·K)	1.5	0.43	1.3	4.9
Dielectric constant, ε	11.8	13.1	9.7	10
Johnson's FOM* ($E_{br} \times V_{sat}$)/2π	1	3	80	60
*** Johnson's figure of merit measures the suitability of a semiconductor for high-power, high-frequency applications.**				

2.2 Indium gallium arsenide

III–V heterostructures such as $In_xGa_{1-x}As$/InAlAs and GaN/AlGaN HEMTs cannot be grown as large-area, high-quality bulk single-crystal structures. $In_xGa_{1-x}As$ is grown epitaxially on a single-crystal host substrate of GaAs or InP, while GaN/AlGaN HEMTs are grown heteroepitaxially on 4H-SiC or sapphire. Si is also an attractive host substrate because it is relatively economical. Single-crystal growth of one semiconductor on another is called epitaxy (from Greek: *epi* – upon, *taxis* – arrangement). This technique allows us to grow a variety of high-quality compound semiconductors with unique materials properties often superior to those of the

host substrate. However, epitaxial growth does not always produce defect-free single-crystal compound semiconductors. The quality of the grown material depends on its chemical and crystallographic compatibility with its substrate. In fact, heteroepitaxial growth is not always lattice-matched. In many cases, high-quality materials can be produced as pseudomorphic heteroepitaxial layers or through strain relaxation.

$In_xGa_{1-x}As$ is grown epitaxially with a wide range of compositions (x = 0 to x = 1). The composition of the ternary alloy will affect its lattice constants and material properties, such as band gap, producing a unique chemical and crystallographic relationship between each alloy and its host substrate. One technologically relevant alloy is $In_{0.53}Ga_{0.47}As$, which is lattice-matched to InP (**Figure 2-1**). In addition, $In_{0.53}Ga_{0.47}As$ can be grown as part of a lattice-matched heterostructure such as $In_{0.53}Ga_{0.47}As/In_{0.52}Al_{0.48}As$, which is used in many electronic and optoelectronics devices.[5,6] In this dissertation we mainly used these two heterostructures: uncapped $In_{0.53}Ga_{0.47}As/In_{0.52}Al_{0.48}As$ and capped $InP/In_{0.53}Ga_{0.47}As/In_{0.52}Al_{0.48}As$, both grown on InP.[5]

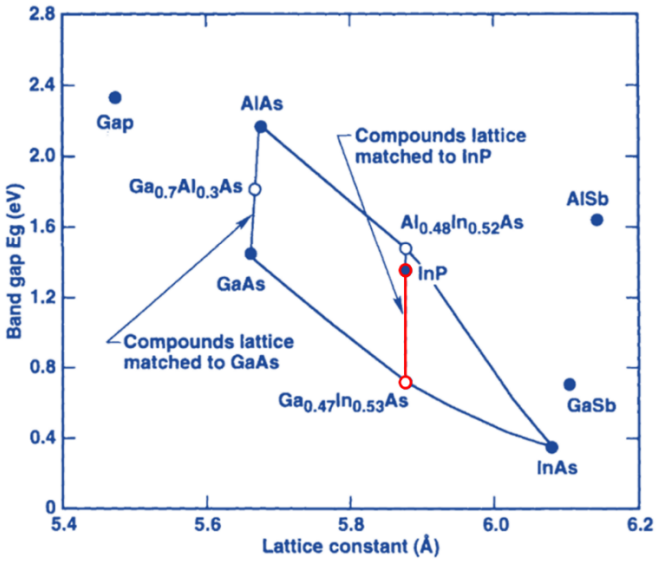

Figure 2-1 Band gap energy as a function of lattice constant for compound semiconductors containing Al, In, Ga, P, As, and Sb. Adopted from Asbeck *et al*.[16]

$In_{0.53}Ga_{0.47}As$ has a zinc-blende crystal structure with a lattice constant equal to that of InP, a = 5.868 Å (**Figure 2-1**). **Figure 2-2** shows a zinc-blende isomorph structure for InGaAs. The cation–anion distance in InGaAs, a ternary alloy, has been shown to equal those in binary alloys such as GaAs and InAs.[6] Because of its perfect lattice match with InP, $In_{0.53}Ga_{0.47}As$ does not exhibit strain or misfit dislocations. $In_{0.53}Ga_{0.47}As$ has a direct band gap of about 0.75 eV, and at room temperature it exhibits very high electron mobility, low effective mass, and high electron saturation velocity compared to Si, making it an attractive candidate to replace Si in MOSFETs (see **Table 2-1**). In general, InGaAs is doped *in situ* using Si or Sn because these donors have low activation energy. *Ex-situ* ion implantation doping of Si is limited to 10^{18} cm^{-3}; however, metal-organic vapor phase epitaxy (MOVPE) and molecular beam epitaxy (MBE) *in situ* doping can produce a doping concentration over 5×10^{19} cm^{-3}.[17]

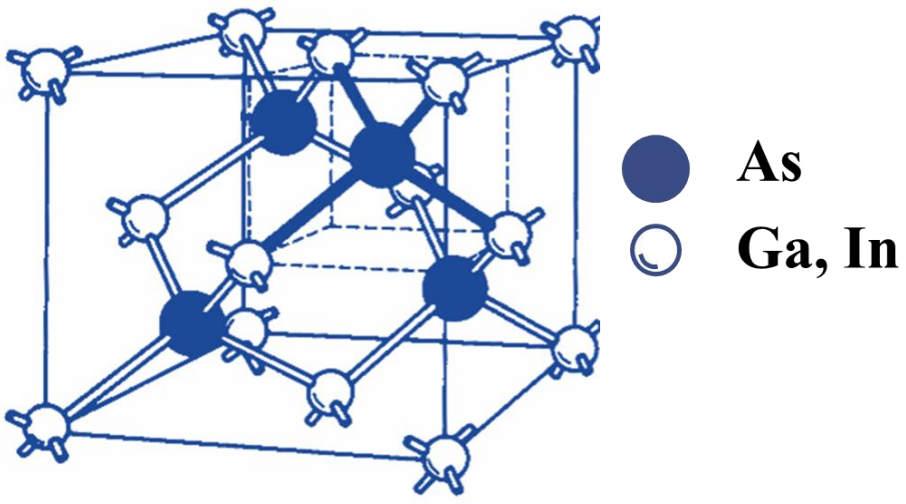

Figure 2-2 Zinc-blende crystal structure of InGaAs. Adopted from Pierret.[18]

2.3 Gallium nitride

Group-III nitrides have attracted significant attention in the last two decades because they have played an outsize role in the development of blue, green, and white light-emitting diodes (LEDs).[13,19,20] A less reported development is that GaN and its alloys are gaining ground in high-frequency, high-voltage RF applications.[10,11,21] The combination of GaN's wide direct band gap of 3.42 eV (at 300 K for the wurtzite structure) with its high breakdown field makes it ideal for RF applications. Thanks to its wide band gap, the extrinsic properties of GaN persist even at high temperatures,[13] giving it an edge in high-temperature applications over conventional semiconductors such as Si, Ge, and GaAs, which have relatively narrow band gaps. Furthermore, GaN and its alloys are resistant to radiation (protons, α-rays, and heavier ions) by orders of magnitude compared to GaAs with similar doping concentration.[22] This property makes it an attractive candidate for both commercial and military satellites as well as avionics applications where radiation damage is a major threat to device reliability and performance.

There is a lack of inexpensive, large-area (>1 cm), semi-insulating single-crystal bulk GaN substrates.[13,23,24] Therefore, GaN and its ternary and quaternary alloys are grown on host substrates such as sapphire, SiC, and Si with the assistance of buffer layers using MBE or MOVPE. However, GaN has a large lattice mismatch with sapphire (~16%) and with Si (~17%). Though the lattice mismatch between GaN and 6H-SiC is relatively small, only 3.5%, it can still lead to a high density of dislocations within the epitaxially grown GaN film.[15,25]

Surprisingly, even with a high dislocation density, GaN can still be used to produce high-quality LEDs and other electronic devices.[13,19] For example, blue LEDs made on GaN exhibit high internal quantum efficiency and commercial-grade device performance, even though the structure

contains many defects.[26,27,28] The threading and edge dislocations present in epitaxial GaN films are typically on the order of 10^8–10^{11} cm^{-2}, which is very high compared to conventional III–V materials such as GaAs, whose dislocation densities are less than 10^4 cm^{-2}.[19,28,29] This property makes GaN and its alloys fairly unique and in some ways advantageous, because it means a wide range of GaN-based electronic and optoelectronic devices can be fabricated without requiring the extremely high crystalline quality necessary with typical III–V semiconductors.[13,19]

Technologically relevant group-III nitrides—GaN, AlN, InN, and their alloys—crystallize in the wurtzite structure (**Figure 2-3**a).[13] Since wurtzite belongs to the hexagonal crystal system with the *P63mc* space group and *6mm* point group, it is inherently noncentrosymmetric (no inversion symmetry). Therefore, it is polar, with spontaneous polarization occurring parallel to the *c*-axis.[30,31] The magnitude of spontaneous polarization for III-nitrides can be as high as 30% of that for classical ferroelectrics such as $BaTiO_3$ (P_s = −0.81C/cm^2, −0.029 C/cm^2, and −0.032 C/cm^2 for AlN, GaN, and InN, respectively).[13,32] In addition, lattice mismatch at the AlGaN/GaN interface in HEMT heterostructures causes mechanical strain, inducing piezoelectric polarization. Thus, HEMT heterostructures grown along the *c*-axis of the wurtzite crystal experience strong polarization-induced electric fields.

One important consequence of these built-in electric fields is the formation of a 2DEG channel with high electron sheet density (over 10^{13} cm^{-2} without doping) at the AlGaN/GaN interface (Figure 1.4b).[33,34] This is a critical feature in HEMTs, as the electrons in the 2DEG region exhibit high mobility thanks partially to the absence of dopants. At room temperature, the peak saturation electron velocity in the 2DEG could be as high as 2.5×10^7 cm/s and its electron mobility is near 1500 $cm^2/V{\cdot}s$ (see **Table 2-2**). [21,33,34]

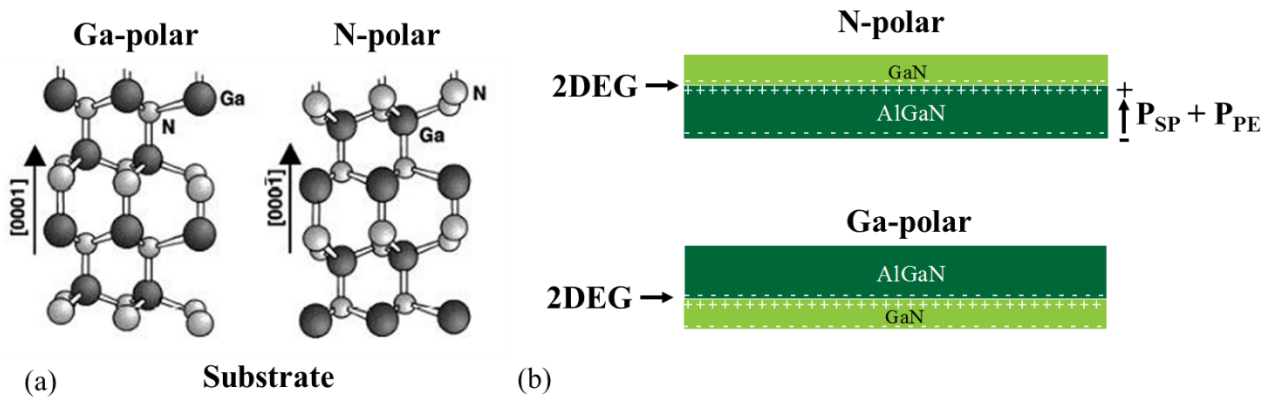

Figure 2-3 (a) Crystal structure of Ga- and N-polar GaN (adopted from Kang *et al*.[35]). (b) The top schematic shows typical N-polar GaN/AlGaN, and the bottom schematic shows Ga-polar AlGaN/GaN. P_{SP} and P_{PE} are the induced spontaneous and piezoelectric polarization fields. GaN HEMT heterostructures are grown on sapphire, Si, and SiC substrates with AlN, GaN, and AlGaN used as buffer layers.

Because wurtzite GaN is polar, it can be grown either in the (0001) or the (000$\bar{1}$) direction on substrates of *c*-plane sapphire, Si-face or C-face SiC, and (111) Si. GaN grown in the (0001) or (000$\bar{1}$) direction is commonly called Ga-polar and N-polar GaN, respectively (**Figure 2-3**a).[13] The polarity of the GaN film is determined by the chemical termination of the substrate's surface, by the initial growth conditions, and by the choice of substrate polarity. For example, GaN grown on Si-face SiC is Ga-polar, while GaN grown on C-face SiC is N-polar. The crystal orientation, and thereby the polarity, of GaN is easily identified by using *ex-situ* techniques such as etching or by using *in situ* techniques such as reflection high-energy electron diffraction (RHEED) during MBE growth. N-polar GaN is readily etched with a potassium hydroxide (KOH) solution, and it exhibits surface kinetics distinct from Ga-polar GaN.[36] In addition, N-polar GaN is more susceptible to incorporation of dopants and other residual impurities such as C and O compared to Ga-polar GaN.[13,36]

The two polarities of GaN have reversed bond direction and crystal structure (**Figure 2-3**a). Thus, N-polar GaN has a polarization field whose direction is opposite that of Ga-polar GaN. Thus, in Ga-polar HEMTs the 2DEG channel forms at the AlGaN/GaN heterointerface, while in N-polar HEMTs a GaN/AlGaN heterostructure is used to produce the 2DEG channel (**Figure 2-3**b).

With this in mind, even though the two polarities have the same bulk properties (such as the band gap and lattice constants), N-polar GaN offers several key advantages in HEMTs over Ga-polar GaN. For example, in N-polar HEMT heterostructures the electrons in the 2DEG channel are strongly confined by the wide-band-gap AlGaN back-barrier, which localizes the electrons at the GaN/AlGaN interface (see **Figure 3-1** in chapter 3). Accordingly, N-polar HEMTs exhibit less short-channel effect as well as better device characteristics compared to Ga-polar AlGaN/GaN HEMTs.[36,37] N-polar GaN is more scalable than Ga-polar GaN, particularly in HEMTs, because in N-polar GaN HEMTs the gate is closer to the 2DEG channel; the small band gap GaN is on top, rather than the wide-band-gap AlGaN being on top, as in Ga-polar GAN HEMTs. Therefore, the effective gate-to-channel separation can be proportionally scaled with gate length while maintaining higher capacitance.[36]

Moreover, the source and drain contacts are made to the "narrower" band-gap GaN channel in N-polar GaN HEMTs heterostructures, rather than to the wider-band-gap AlGaN, as in Ga-polar GaN HEMTs.[36,38] This allows for the formation of low-resistance Ohmic contacts, since the electron injection at the metal/semiconductor interface faces a smaller barrier in N-polar GaN HEMTs.[39] Chapter 3 of this dissertation is dedicated to discussion about Ti/Al contacts to N-polar GaN with low specific Ohmic contact resistance.[40]

2.4 Two-dimensional transition metal dichalcogenides

Many of the transition metal dichalcogenides (TMDs) grabbing the spotlight today have been studied and used in various applications in bulk form, alongside graphite, for at least fifty years. Thanks to their layered structure with weak bonding between layers, TMDs such as MoS_2 are common solid lubricants in vacuum systems and other industrial applications.[41] However, the discovery of graphene, a single atomic layer of graphite, in 2004 by Novoselov and Geim, brought layered materials into the spotlight again.[42] This renewed interest was initially driven by graphene's impressive material properties that led to new physics. Graphene exhibits very high carrier mobility (over 70,000 $cm^2/V{\cdot}s$), high steady-state carrier saturation velocity (4×10^7 cm/s), and zero effective mass; it is also flexible, has superior mechanical properties, and is transparent.[43] Despite being a wonder material, large-area graphene is unfortunately a semimetal with almost zero band gap.[43] At least for now, this property thwarts its prospects in transistor applications, but the fruits of graphene research have motivated the search for other 2D layered compounds with similar material characteristics but have a band gap.

Semiconducting TMDs such as MoS_2 have emerged as viable alternatives to graphene for electronic and optoelectronic applications including logic and RF transistors, plasmonic devices, photodetectors, and biosensors.[7,44] Similar to graphite, bulk MoS_2 is an *X-M-X* layered compound (*M*: transition metal, *X*: chalcogen). Each layer, approximately 6.5 Å thick, consists of hexagonally packed Mo atoms sandwiched between two layers of S atoms, all held together by covalent bonds.[44,45]

The metal atoms in MoS_2 have trigonal prismatic or octahedral coordination (**Figure 2-4**). Neighboring MoS_2 layers are bound together by weak van der Waals forces to form the bulk

crystal. Depending on the stacking sequence of the *X-M-X* layer and the number of each of these layers per unit cell, the MoS_2 crystal has at least three polymorphs (same composition but different structure). The unit cell in this case is defined by the *c*-axis, which is perpendicular to the *X-M-X* stack, and by the *a* and *b* axes parallel to the *X-M-X* stack.[7]

The most common structural polytypes (phases) of MoS_2 are 1T, 2H, and 3R.[46] Most natural MoS_2 crystals exhibit the 2H-phase (**Figure 2-4**), which is hexagonal (a = 3.162 Å, b = 12.29 Å) and contains two *X-M-X* stacks per unit cell. On the other hand, synthetic MoS_2 crystals may consist of the 3R-phase, which is rhombohedral and contains three *X-M-X* stacks per unit cell, while maintaining the same trigonal prismatic coordination of Mo atoms.[47] Both 2H- and 3R-MoS_2 are semiconducting. However, certain types of chemical processing such as intercalation of 2H-MoS_2 crystals with ionic species can cause a reversible transformation of the 2H phase into the metallic 1T phase, in which the Mo atoms assume octahedral coordination. This dissertation focuses on semiconducting MoS_2, with occasional reference to 1T-MoS_2.

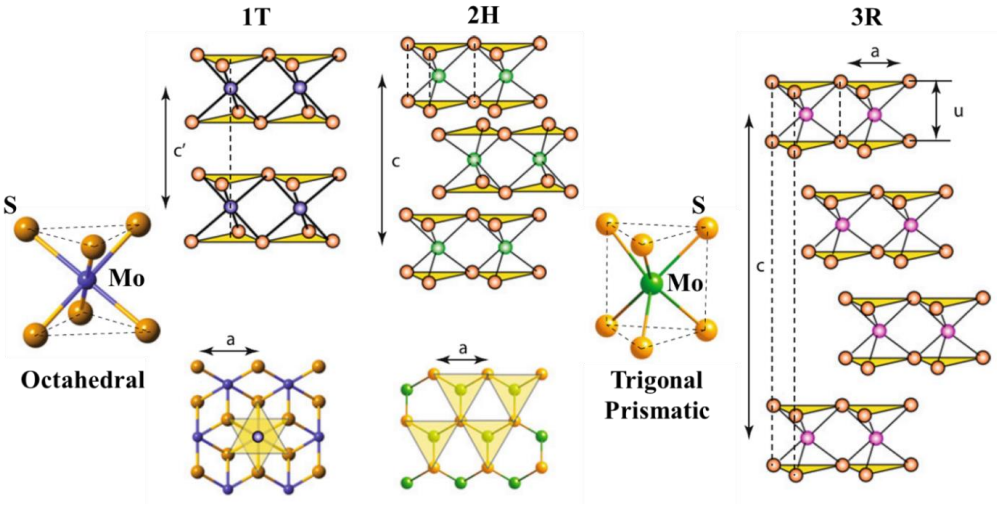

Figure 2-4 Crystal structures of MoS_2, from left to right: tetragonal 1T phase with octahedral Mo atomic coordination, hexagonal 2H (a = 3.162 Å, b = 12.29 Å), and rhombohedral 3R phases with trigonal prismatic Mo atomic coordination. The bottom two schematics show top views of the 1T and 2H phases. Adopted from Kolobov *et al.*[7]

MoS_2 and other semiconducting TMDs (for example, WS_2 and WSe_2) can be fabricated using a top-down or bottom-up method. Top-down methods take advantage of the weak coupling between the MoS_2 layers, which readily cleave (exfoliate) to form multi-layer (ML) or even single (SL) atomically thin sheets of MoS_2 analogous to graphene.[7,42] Bottom-up methods involve the use of chemical vapor deposition (CVD), MBE, or atomic layer deposition to synthesize often large-area SL (sometimes ML) MoS_2 crystals.[48,49] Though bottom-up methods offer a clear route for fabricating wafers of MoS_2-based electronic and optoelectronic devices, as of yet, large (>15 μm), continuous, multi-layer CVD-grown MoS_2 crystals are not readily available to achieve such objectives. Hence, in this dissertation work, we used only mechanically exfoliated MoS_2 crystals.

Mechanical exfoliation often produces highly crystalline and clean SL or ML MoS_2 crystals (or flakes) that are ideal for fabricating individual devices.[46,50] Unlike selenide (WSe_2) and telluride (WTe_2) exfoliated flakes, MoS_2 flakes are thermally stable and resistant to oxidation when left in air at temperatures up to 500 K.[7,51] The oxidation resistance of MoS_2 flakes is partially due to its weak physical adsorption of oxygen species, which leaves the crystalline MoS_2 surface structure intact.

Due to quantum confinement and the subsequent change in hybridization between p_z orbitals of S atoms and *d* orbitals of Mo atoms, exfoliated MoS_2 crystals have exhibited thickness-dependent properties.[46,52] For example, the band gap of MoS_2 gradually shifts from direct to indirect as it increases in thickness from a monolayer to a bulk crystal. Meanwhile, the band-gap energy of MoS_2 decreases from ~1.8 eV to ~1.3 eV going from monolayer to bulk (see **Figure 2-5**).[52] Thanks to these thickness-dependent band-gap properties, MoS_2 along with other semiconducting TMDs are attractive candidates for many electronic and optoelectronic applications, considering that single layer of some of the semiconducting TMDs have a direct band

gap.[46] Similar to their band gap, the mobility of TMDs is also affected by their thickness; however, it tends to degrade for SL and bilayer TMDs because of the increased role of surface phonon and roughness scattering mechanisms (see **Figure 2-5**b). For multilayer MoS_2 field-effect transistors (FETs), however, mobilities over 200 $cm^2/V{\cdot}s$ have been reported.[53]

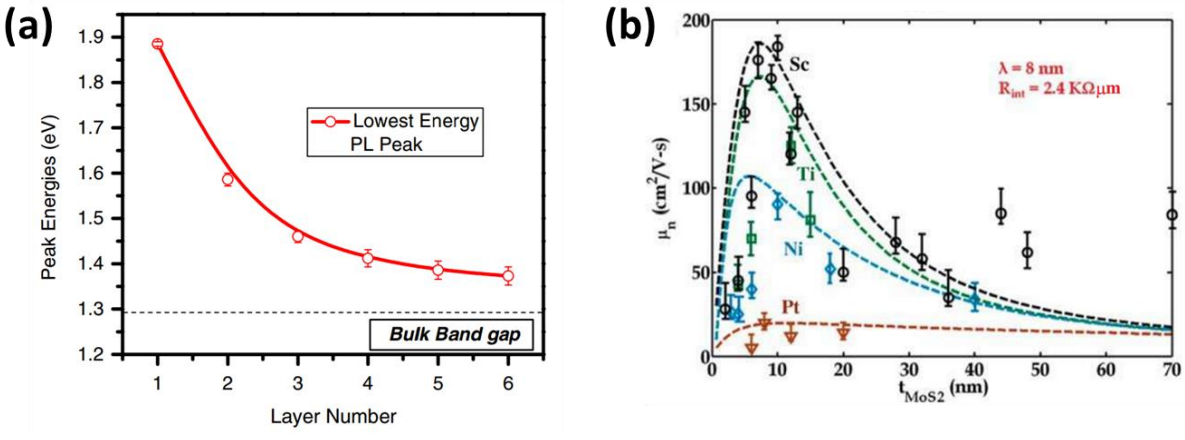

Figure 2-5 (a) Band-gap energy as a function of the number of layers of mechanically exfoliated MoS_2. Information extracted from photoluminescence (PL) measurements. Source: Mak *et al.*[52] (b) Field-effect mobility as a function of the number of mechanically exfoliated MoS_2 layers for Sc, Ti, Ni, and Pt contacts. Source: Das *et al.*[54]

In assessing whether TMDs are viable for various electronic and optoelectronic applications, doping is important to consider.[44] Currently available natural and synthetic bulk TMDs, including MoS_2 crystals—which are often used in device research—are only unintentionally doped (UID) and exhibit high sheet resistance. However, MoS_2 (unlike WSe_2, for example) may contain a high density of sulfur vacancies that induce mainly n-type behavior when brought in contact with various metals, including those with high work functions such as Au.[53,55] The observed weakened role of the metal work function is caused by Fermi level pinning, which might be partially caused by the sulfur vacancies near the surface (see chapter 1). Because they contain sulfur vacancies at sufficiently high concentration, MoS_2-based devices show device

characteristics that are more stable and reproducible than, for example, WSe_2 devices.[53,56] When TMD-based devices must be doped further, there are various methods to accomplish this. The first method is surface charge transfer doping, which relies on charge transfer between a material adsorbed on the TMD surface and the first few layers of the TMD. The second method is substitutional doping, which relies on substituting Mo or S atoms with foreign species such as Re, Nb, or even Cl.[44,57] Another is intercalation with electron or hole donors.[58] In this dissertation work, we used only UID MoS_2.

2.5 Summary

All three semiconductor compounds reviewed in this chapter exhibit unique electrical, mechanical, and physical properties that make them attractive candidates for future electronic and optoelectronic applications. As such, this dissertation work provides some insight into fabricating contacts to these semiconductors, emphasizing how surface passivation and annealing affect contact resistance.

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Chapter 3

Ti/Al-based contacts to N-polar GaN/AlGaN heterostructures*

*Note: Significant portions of this manuscript are already published in *Applied Physics Letters*.[1]

3.1 Introduction

Because GaN has a large band gap, high breakdown voltage, high carrier velocity, and good chemical stability, AlGaN/GaN-based high-electron-mobility transistors (HEMTs) are attractive for high-power microwave applications.[2,3] However, to improve their efficiency and high-frequency performance, it is necessary to minimize their parasitic resistances.[4] Hence, low-resistance source and drain Ohmic contacts are essential. The wide-band-gap AlGaN barrier layer and its associated conduction band discontinuities with GaN in Ga-face AlGaN/GaN HEMTs make it difficult to achieve low contact resistance.[5,6] On the other hand, for N-polar GaN/AlGaN HEMTs, the Ohmic contacts are made directly to GaN, potentially lowering the contact resistance because the wider-gap AlGaN barrier is beneath the GaN layer (**Figure 3-1**).

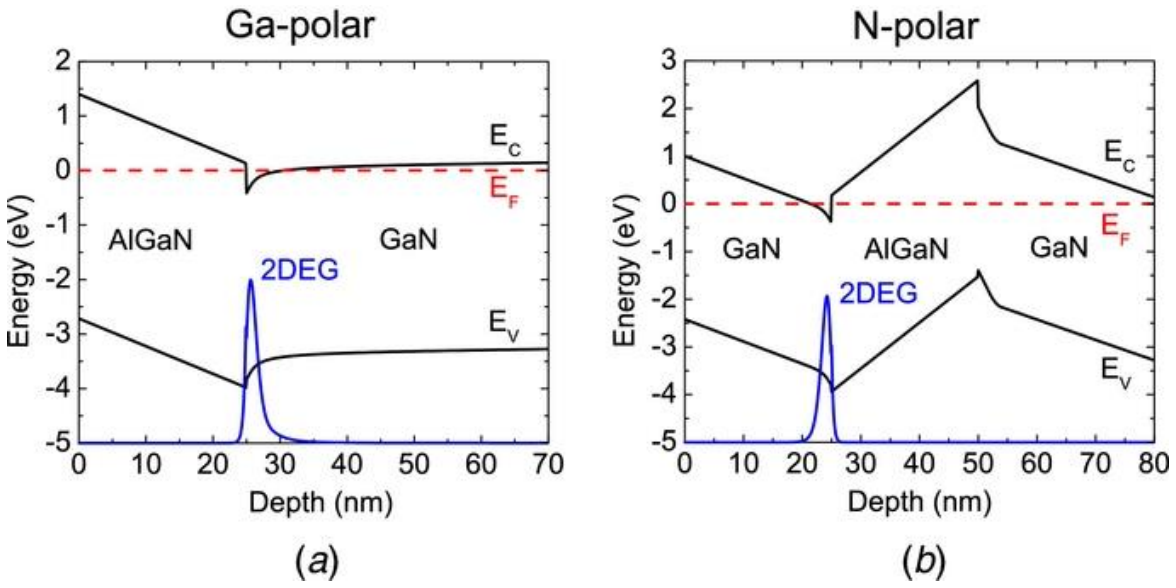

Figure 3-1 Equilibrium band diagram for (a) Ga-polar AlGaN/GaN and (b) N-polar GaN/AlGaN/GaN HEMTs. The blue curves represent the two-dimensional electron gas (2DEG) density (n_s). Source: Wong *et al.* [7]

Though using N-polar GaN/AlGaN is a promising way to reduce contact resistance, it has proven difficult to adopt conventional Ti/Al-based metallization to N-polar GaN/AlGaN HEMTs[8] and generally to N-polar n-GaN films, leading to high contact resistance.[9,10,11] To mitigate this, some researchers have added an extra processing step: regrowth of In(Ga)N[12] or n^+-GaN.[13,14]

The low resistance of Ti/Al-based contacts is often correlated with the formation of an interfacial nitride (such as TiN or AlN) and presumably the formation of nitrogen vacancies that serve as donors in GaN.[10,15,16,17] While the formation of an interfacial nitride may promote the formation of N vacancies, causing tunneling at the metal/semiconductor interface, prior work on Ti/Al-based contacts to N-polar GaN has suggested that AlN can form, which can be detrimental due to unfavorable polarization at the AlN/GaN interface.[9] In this dissertation work, we examined an N-polar GaN/AlGaN heterostructure, measuring its contact resistance and using transmission

electron microscopy to help explain the strong dependence of contact resistance on Ti:Al ratio as well as to reveal the interfacial reactions of the contact metals with GaN.

3.2 Experimental methods

3.2.1 Fabrication of test structure

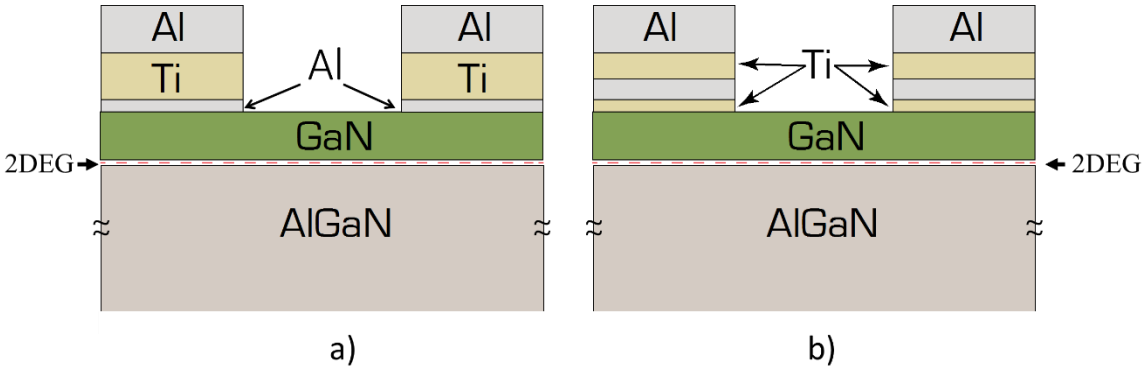

Figure 3-2 (a) Schematic cross-sections of an N-polar GaN/AlGaN HEMT device with "Al-first" source and drain contact metal stacks. (b) Same structure as (a), but with "Ti-first" source and drain metal stacks.

We used two-inch wafers of N-polar GaN/AlGaN heterostructures provided by Northrop Grumman Corporation (Dr. Ioulia Smorchkova). The heterostructures were grown on C-face SiC substrates by molecular beam epitaxy (**Figure 3-2**), and small square pieces were diced to make samples. The undoped GaN layer was 7 nm thick, and the wafers were capped *ex-situ* with silicon nitride. The average sheet resistance (R_s) of these samples was 508 **Ω**/□. Each sample was degreased sequentially in acetone, isopropanol, and deionized (DI) water for 5 min under continuous sonication, then blown dry with nitrogen. The specific contact resistance was measured using the circular transfer length method (CTLM).[14] The CTLM test structures were patterned using photolithography. Ten of these patterns were used, with gap spacings of 20, 18, 16, 14, 12, 10, 8, 6, 4, and 3 µm, each with an inner pad radius of 40 µm (see **Figure 3-3**).

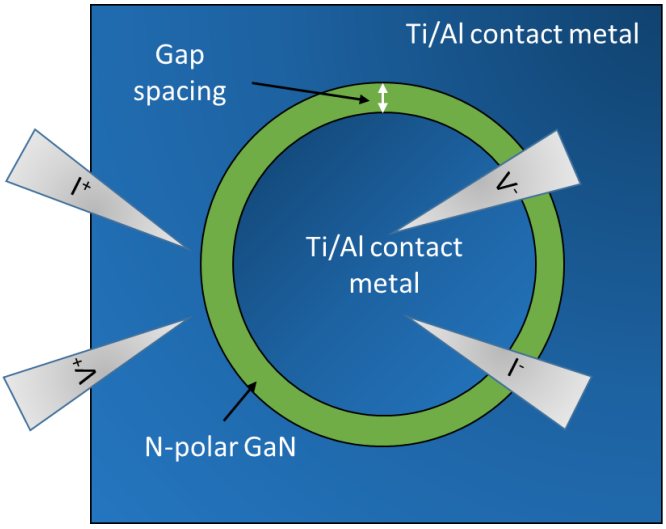

Figure 3-3 Schematic of a CTLM test structure with the four-terminal Kelvin test probe configuration.

Initially, we performed lithography with only two resists, both developed using tetramethylammonium hydroxide (TMAH; Microposite™ MF™ CD26). However, TMAH attacked the N-polar GaN, roughening the surface. Therefore, we developed a three-resist layer lithography process (**Figure 3-4**). First, poly(methyl methacrylate) (PMMA 950 A3, Microchem™) was deposited to protect the N-polar GaN from the TMAH developer. Then, lift-off resist (LOR 5A) was deposited to provide enough undercut for easy metal lift-off after metallization. Finally, the top imaging resist (Megaposit™ SPR 3012) was deposited.

After exposure to ultraviolet (UV) light using a contact aligner and a mask with CTLM patterns, the SPR 3012 and LOR 5A resists were both developed in TMAH (CD26). The underlying PMMA layer was then exposed to deep UV for 900 s and then developed in toluene. Once the desired CTLM patterns were produced, the samples were exposed to O_2 plasma. This step is important because it removes resist residue and other organic contamination from the

exposed semiconductor section of the CTLM pattern prior to metal deposition. A UV ozone clean is a possible substitute for the O_2 plasma clean.

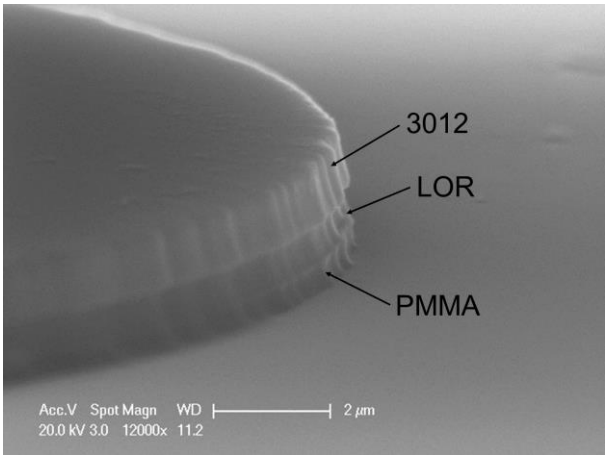

Figure 3-4 Three-layer resist profile used to fabricate CTLM patterns on N-polar GaN samples. Scanning electron microscopy image taken by Brian Downey.

3.2.2 Pre-metallization surface preparation

During the early stages of this work, we found that the N-polar GaN samples exhibited high contact resistance. This result was correlated with the presence of native oxide on the surface. To remove this native oxide, we attempted many *ex-situ* wet chemical treatments, including buffered oxide etch (BOE), citric acid, hydrogen peroxide (H_2O_2), and ammonium sulfide ($(NH_4)_2S$). All these treatments except for citric acid proved effective, producing low contact resistance at least in the annealed contacts (see Appendix 3.7.1).

Auger electron spectroscopy (AES) surface scans of $(NH_4)_2S$- and BOE-treated N-polar GaN show that each treatment reduced the amount of native oxide. These Auger results also show that $(NH_4)_2S$ passivated the surface, preventing re-oxidation for over a month (see Appendix 3.7.2). However, contacts treated with $(NH_4)_2S$ had high as-deposited contact resistance, which

improved only with annealing (see Appendix 3.7.1 and 3.7.3). In contrast, BOE-treated samples showed relatively low contact resistance both before and after annealing (see Appendix 3.7.1). BOE was also used to remove the silicon nitride capping layer along with the native oxide on the semiconductor. Hence, we adopted BOE as the main pre-metallization surface treatment.

After a BOE treatment (10:1 volume ratio of 40% NH_4F and 49% HF in water) for 2 min, followed by a DI H_2O rinse for 20 s and N_2 drying, samples were quickly loaded into an electron-beam (e-beam) evaporation physical vapor deposition system (Edwards Auto 306). As shown in Appendix 3.7.4, e-beam evaporated contacts exhibited relatively low contact resistance both before and after annealing, while as-deposited sputtered contacts had relatively high resistance due to sputter-induced surface damage, but their resistance lowered with annealing. Hence, we used only e-beam evaporation for the remainder of this work.

A turbomolecular pump reduced the base pressure of the e-beam chamber to 2×10^{-7} Torr by pumping overnight (for at least 12 h). Ti/Al/Ti/Al films were deposited while the sample stage rotated, producing uniform metal films. The thickness of the first Ti layer varied from 0 to 50 nm, while the Al concentration in the structure was kept at ~74 at.% or 84 at.%. The film thickness was measured using a calibrated quartz crystal monitor (FTM6). The layer thicknesses are shown in **Table 3-1**. After metallization, excess metal on the sample was lifted off in a bath of heated (85 °C) remover PG solution for 1–2 h.

Table 3-1 Calculated contact resistance and specific contact resistance for six samples with various Ti/Al metallizations. All samples were annealed at 500 °C for 60 s.

Samples	Metallization	Layer Thickness (nm)	Contact Resistance (R_c in Ω·mm)	Specific Contact Resistance (ρ_c in Ω·cm^2)
A	Ti/Al	50/150	1.03 ± 0.12	$2.7 \times 10^{-5} \pm 8.1 \times 10^{-6}$
B	Ti/Al/Ti/Al	5/15/45/135	0.43 ± 0.09	$4.8 \times 10^{-6} \pm 1.6 \times 10^{-6}$
C	Ti/Al/Ti/Al	3/9/47/141	0.27 ± 0.13	$2.2 \times 10^{-6} \pm 1.3 \times 10^{-6}$
D	Ti/Al/Ti/Al	1/3/49/147	0.28 ± 0.05	$1.9 \times 10^{-6} \pm 7.4 \times 10^{-7}$
E	Al/Ti/Al	3/50/147	0.10 ± 0.04	$2.7 \times 10^{-7} \pm 1.7 \times 10^{-7}$
F	Al/Ti/Al	75/50/75	1.68 ± 0.43	$4.0 \times 10^{-5} \pm 2.6 \times 10^{-5}$

3.2.3 Characterization

Current–voltage (*I–V*) curves were measured from the as-deposited and annealed samples by using four probes (**Figure 3-3**). The resistances between pairs of contacts were extracted for each *I–V* curve and plotted as a function of the gap spacing between the contacts. The contact resistance (R_c) and specific contact resistance (ρ_c) were then extracted by fitting the data of resistance versus gap spacing to expressions based on the transmission line model applied to circular contacts,[18] retaining three terms of a series expansion of the Bessel function. All contacts were annealed at 500 °C for 60 s in a rapid thermal annealing furnace (AG610) in gettered nitrogen. We optimized this annealing temperature for a high-resistance Ti (50 nm)/Al (150 nm) contact, and then used the optimized temperature for the other samples (**Figure 3-5**). We did not further optimize the annealing temperature for the other samples because some of them had very low resistance without annealing and because higher annealing temperatures are generally not desirable for contacts that may be used in transistors with very small dimensions.

Cross-sectional transmission electron microscopy (TEM) and scanning TEM (STEM) were performed on a JEOL EM-2010F microscope. Each TEM specimen was prepared from samples

bonded face-to-face and mechanically thinned using a polishing wheel, and then thinned to electron transparency in an ion mill (Fischione 1010). The interfacial reaction products at the metal/GaN interface were examined with electron energy-loss spectrometry (EELS).

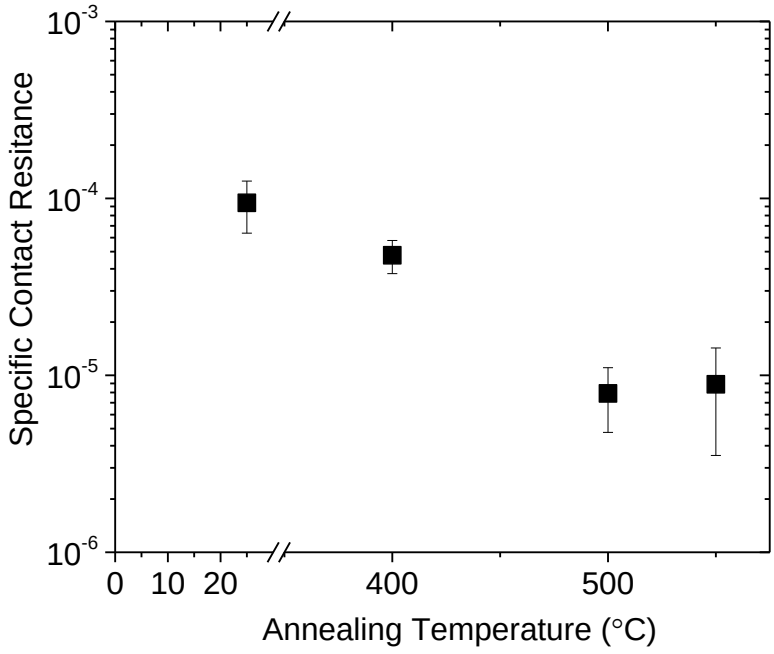

Figure 3-5 Optimization of annealing temperature by cumulatively annealing Ti/Al (50 nm/150 nm) contacts with 74 at.% Al on GaN/AlGaN HEMT heterostructure. The annealing time at each annealing temperature was 60 s.

3.3 Results

The first contacts to the N-polar GaN/AlGaN heterostructure investigated here were Ti (50 nm)/Al (150 nm) and Ti (30 nm)/Al (170 nm), with Al concentrations of 74 at.% and 84 at.%, respectively. These contacts were chosen based on work by Kwak et al.[19] and Gasser et al.[20], which showed that Ti-rich (defined as 74 at.% Al) contacts were thermally stable and exhibited smooth surface morphologies even after annealing at temperatures up to 1000 °C. However, contacts with 84 at.% Al exhibited rough surface morphologies upon annealing, although annealing could

produce low-resistance contacts. They correlated the rough surface morphologies with the presence of elemental Al in the contacts. This behavior is unlike that of the Ti-rich contacts, where the Al mainly existed in the intermetallic phases after annealing. Since the intermetallic phases have high melting points, they enable the high thermal stability and smooth surface morphologies observed in the Ti-rich contacts. Furthermore, the as-deposited and annealed Ti-rich contacts were both Ohmic. Hence, we only explored the Ti-rich contacts further in this work.

In the following sections, we will discuss how the ordering of Ti and Al and their layer thicknesses affected the contact resistance. First, contacts with a thick Ti layer deposited first are discussed, and then TEM results for as-deposited and annealed contacts are presented. Likewise, we will discuss multilayer Ti/Al contacts with thin Ti- and Al-first layers, along with the corresponding TEM data.

3.3.1 Ti/Al with thick Ti-first contacts

Table 3-1 shows all of the contacts studied in this work. The first Ti-rich contact we electrically characterized was sample A [Ti (50 nm)/Al (150 nm)]. The as-deposited sample A had a ρ_c of 3.3×10^{-6} Ω·cm^2, but after annealing at 500 °C for 60 s, its ρ_c increased to 2.7×10^{-5} Ω·cm^2. We believe this increase in specific contact resistance was caused by outdiffusion of Ga, generating Ga vacancies.[8,21] Since Ga vacancies act as acceptors, they compensate donors and increase the depletion width in the GaN beneath the contact, increasing the contact resistance. To further understand the metal/GaN interface and the composition of sample A, both as-deposited and annealed, we performed cross-sectional TEM along with high-magnification high-angle annular dark-field (HAADF) STEM, X-ray energy dispersive spectroscopy (XEDS), and EELS.

3.3.2 TEM characterization of thick Ti-first contacts

Figure 3-6 and **Figure 3-7** show low- and high-magnification HAADF TEM images, respectively, of the as-deposited Ti (50 nm)/Al (150 nm) contacts on N-polar GaN. Reaction between Ti and GaN or Ti and Al did not appear. The elemental profiles of the Al/Ti and Ti/Ga interfaces were sharp and abrupt (**Figure 3-6**c and **Figure 3-7**c), without obvious amorphous interfacial oxide layers. This result indicates that the BOE surface treatment effectively removed the native oxide from the interface and that no detectable re-oxidation happened during or immediately before metallization. This abrupt as-deposited Ti/GaN interface is consistent with its low specific contact resistance.

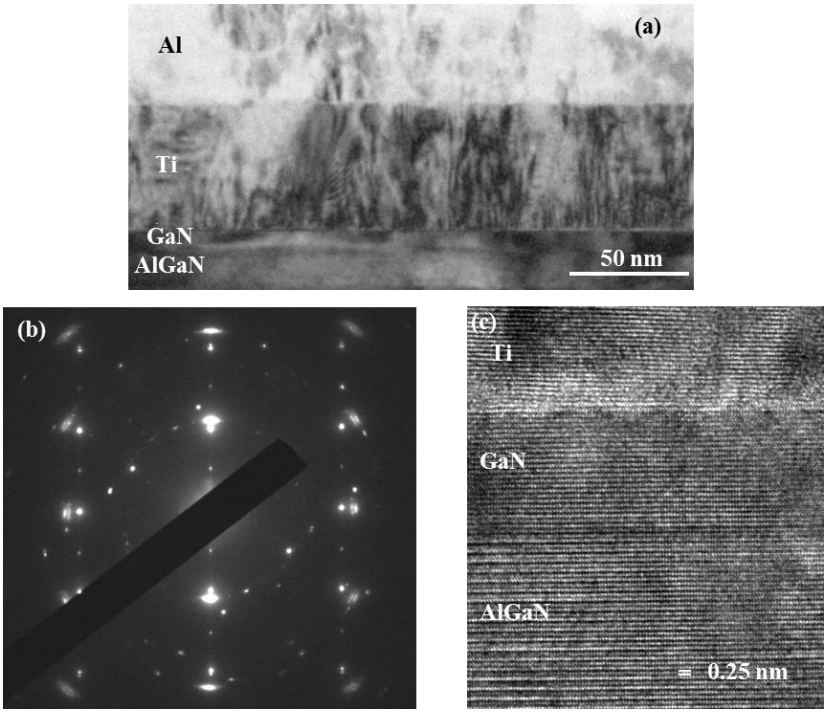

Figure 3-6 (a) Low-magnification image of the as-deposited structure. (b) Selected-area diffraction (SAD) pattern collected from a region consisting of Al/Ti/GaN/AlGaN. Only reflections from Ti and Al appeared, besides those from the nitrides, indicating the lack of interfacial reactions. The Ti film was highly textured, with $<11\bar{2}0>_{Ti}$ // $<11\bar{2}0>_{GaN}$ and $\{0001\}_{Ti}$ // $\{0001\}_{GaN}$. The Al film contained more randomly oriented grains, which resulted in spotty rings in the SAD pattern. (c) Higher-magnification bright-field image collected near the interface. The Ti/GaN and GaN/AlGaN interfaces appear to be sharp.

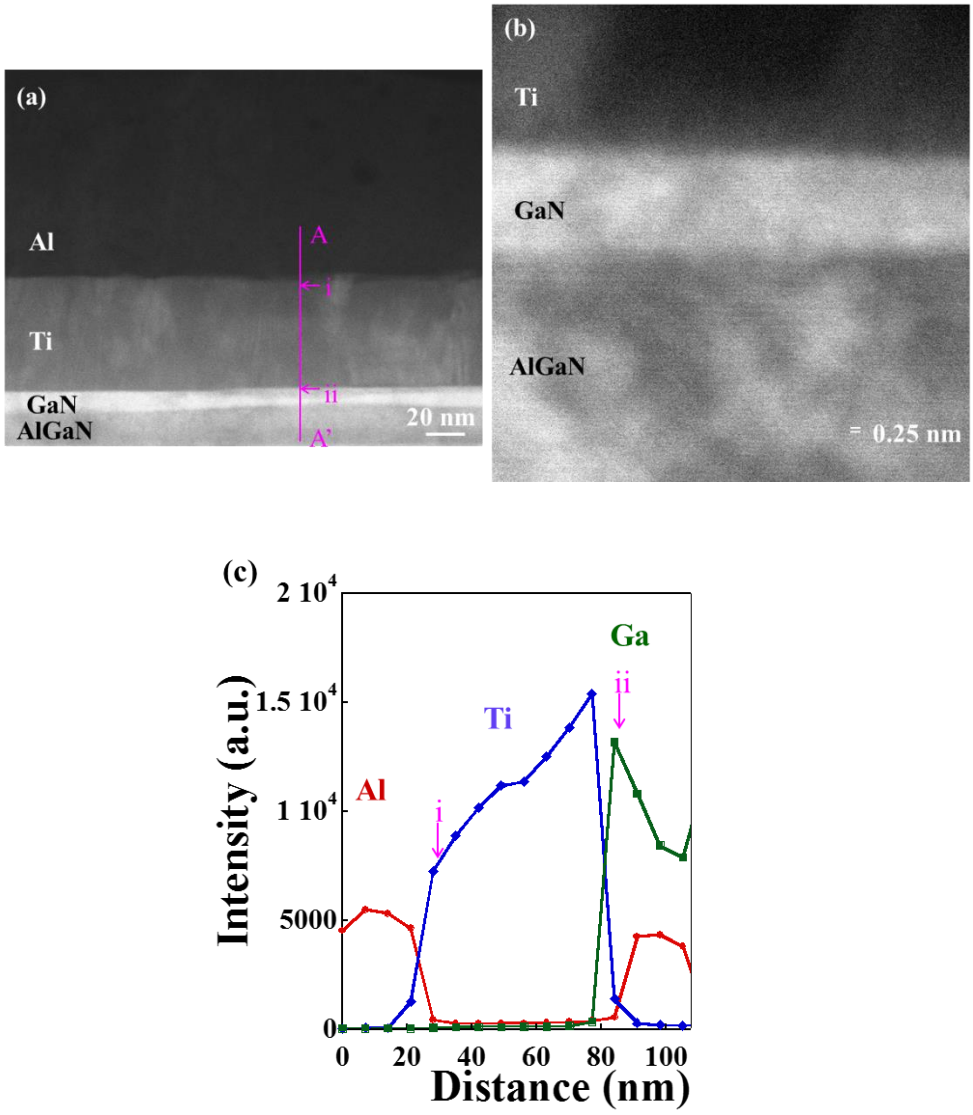

Figure 3-7 (a) HAADF-STEM image of the as-deposited sample shown in Figure 3-6. (b) High-resolution STEM image revealing the sharp Ti/GaN interface. (c) X-ray energy dispersive spectroscopy composition profiles collected along the AA' line in (a). The composition profiles at the interface are relatively sharp, indicating that little or no interfacial reaction occurred in the as-deposited sample.

Figure 3-8 shows cross-sectional HAADF STEM images of sample A after annealing at 500 °C for 60 s. As expected, annealing induced significant interdiffusion between Ti and Al layers. However, under these annealing conditions, Al did not diffuse through Ti to reach the Ti/GaN interface and react with the GaN layer.

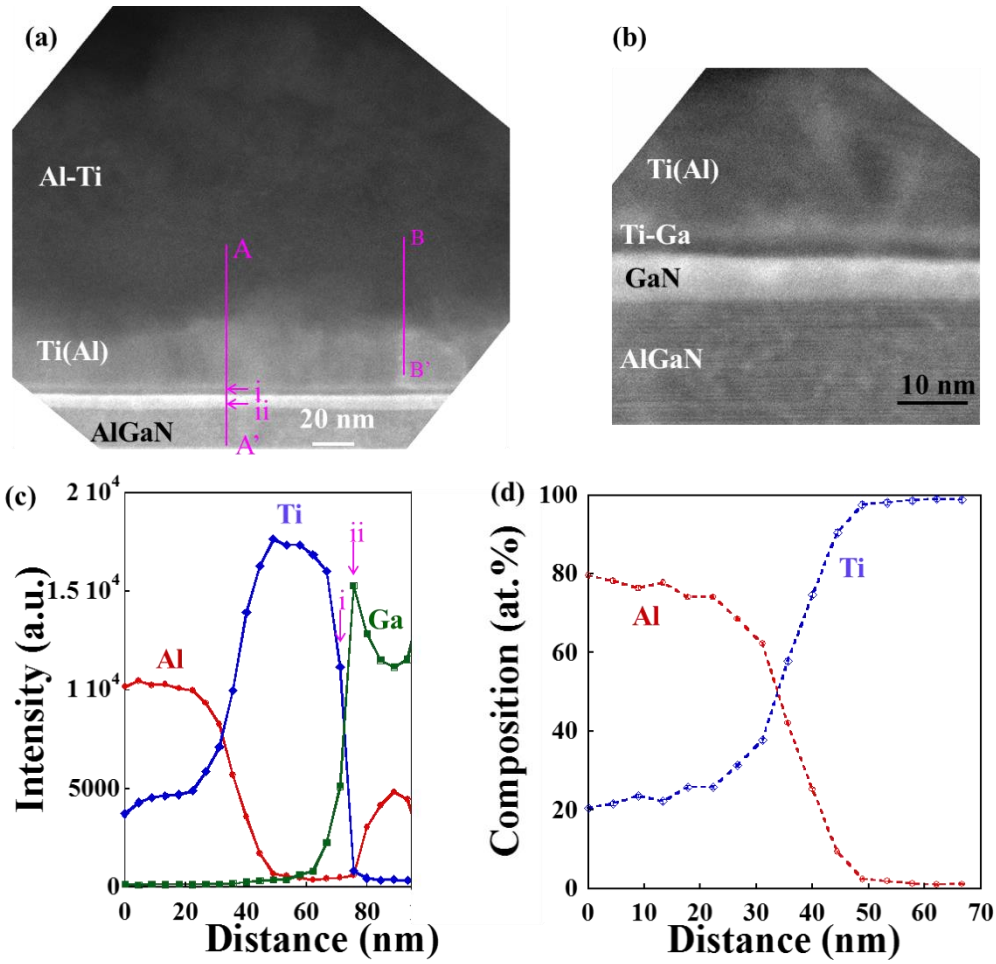

Figure 3-8 (a) and (b) HAADF STEM images of the Ti(50 nm)/Al(150 nm) sample annealed at 500 °C for 60 s. (c) Composition profiles, measured with X-ray energy dispersive spectroscopy, collected along the AA' line in (a). (d) Estimated composition profiles along the BB' line in (a), showing that much Ti diffused into Al during annealing, which produced a diffusive interface between the Al and Ti layers.

3.3.3 Multilayer Ti/Al with thin Ti- and Al-first contacts

We prepared three samples with initial Ti layer thicknesses of 5, 3, and 1 nm, fixing the Al concentration at 74 at.%. The total Ti/Al metal thickness was kept at 200 nm while dividing the Ti and Al into four layers (Ti/Al/Ti/Al). This multilayer metallization enhances the interdiffusion between the metal layers, ultimately forming thermally stable, uniform intermetallic layers above the N-polar GaN. Ti/Al-based intermetallic layers are more resistant to oxidation than contacts

with elemental Ti or Al. This property is important because oxidation can roughen the surface and ultimately increase contact resistance.

The contacts investigated were:

- sample B [Ti(5 nm)/Al(15 nm)/Ti(45 nm)/Al(135 nm)],
- sample C [Ti(3 nm)/Al(9 nm)/Ti(47 nm)/Al(141 nm)], and
- sample D [Ti(1 nm)/Al(3 nm)/Ti(49 nm)/Al(147 nm)].

All three as-deposited Ohmic contacts exhibited low contact resistance and ρ_c. The contact resistance and ρ_c for as-deposited sample B were 0.59±0.23 Ω·mm and 8.9 × 10^{-6} Ω·cm^2, respectively. After annealing the sample at 500 °C for 60 s, the contact resistance and ρ_c improved to 0.43±0.09 Ω·mm and 4.8 × 10^{-6} Ω·cm^2, respectively (**Figure 3-9**).

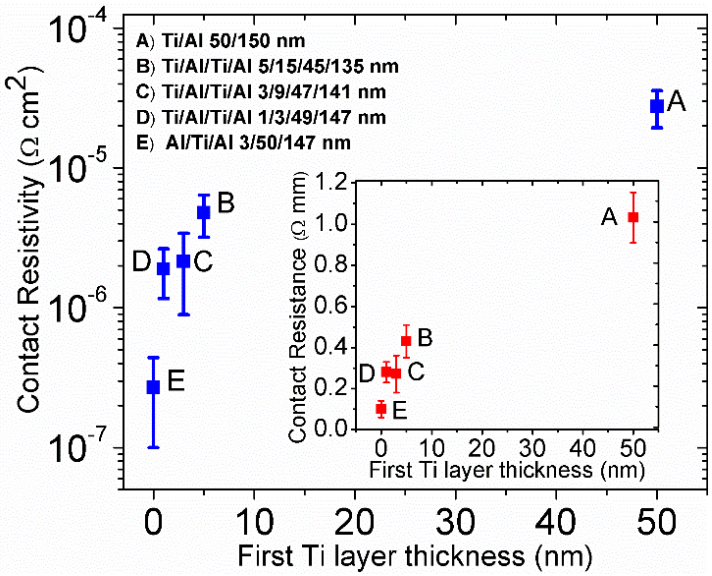

Figure 3-9 Specific contact resistance as a function of the thickness of the first Ti layer. The inset shows contact resistance as a function of the thickness of the first Ti layer.

By thinning the first Ti layer from 5 nm to 3 nm to 1 nm, the contact resistance and corresponding ρ_c decreased, as shown clearly in **Figure 3-9**. When sample D was annealed at 500

°C for 60 s, it exhibited a contact resistance as low as 0.28±0.05 Ω·mm and a ρ_c of 1.9 × 10^{-6} Ω·cm^2. This trend suggests that bringing the Al closer to the metal/GaN interface lowers the contact resistance. Each ρ_c reported above is the average of measurements taken from two samples, prepared separately.

To further investigate how interfacial Al affected the formation of low-resistance Ohmic contacts to N-polar GaN/AlGaN heterostructures, we prepared samples with Al(3 nm)/Ti(50 nm)/Al(147 nm) layers (Sample E in **Figure 3-9**). This metallization showed reproducible, very low contact resistances of 0.11±0.03, 0.11±0.05, and 0.09±0.05 Ω·mm, measured from three separately prepared, as-deposited samples. The sample with 0.11±0.03 Ω·mm was then annealed at 500 °C for 60 s, yielding a contact resistance of 0.10±0.04 Ω mm. The corresponding ρ_c values for this sample were 2.5 × 10^{-7} Ω·cm^2 before annealing and 2.7 × 10^{-7} Ω·cm^2 after annealing. In contrast, for Ohmic contacts with much thicker Al adjacent to the GaN, their as-deposited contact resistance was high, and annealing significantly increased their contact resistance. Sample F was prepared with a Al(75 nm)/Ti(50 nm)/Al(75 nm) metallization, and its ρ_c was 4.0 × 10^{-5} Ω·cm^2 after annealing at 500 °C for 60 s. Hence, proximity of Ti to GaN is also needed to produce a contact with very low contact resistance.

3.3.4 TEM characterization of thin Al-first contacts

The metal/GaN interfacial structure and composition of the annealed samples B and E were examined using TEM, STEM, and EELS. **Figure 3-10**(a) shows a HAADF-STEM image collected near the metal/GaN interface for sample E [Al(3 nm)/Ti(49 nm)/Al(147 nm)]. An Al–Ti intermetallic phase formed due to diffusion of Al from the top of the contact toward the contact interface (point 12). Along with Al, signals for Ti, N, and Ga also appeared immediately above the

metal/GaN interface (**Figure 3-10**b and **Figure 3-10**c). We therefore conclude that a layer comprised of Ti–Al–Ga–N formed above the GaN. The approximate boundaries of this layer are marked by two parallel lines in **Figure 3-10**(a). In addition, an Al signal appeared in each measurement of the GaN layer at position 8 in **Figure 3-10**(a), as shown in **Figure 3-10**(d). This observation could indicate the diffusion of Al into the GaN layer; however, it could also be an artifact related to electron-beam broadening, in turn caused by the increasing thickness of the TEM specimen on the substrate side of the contact.

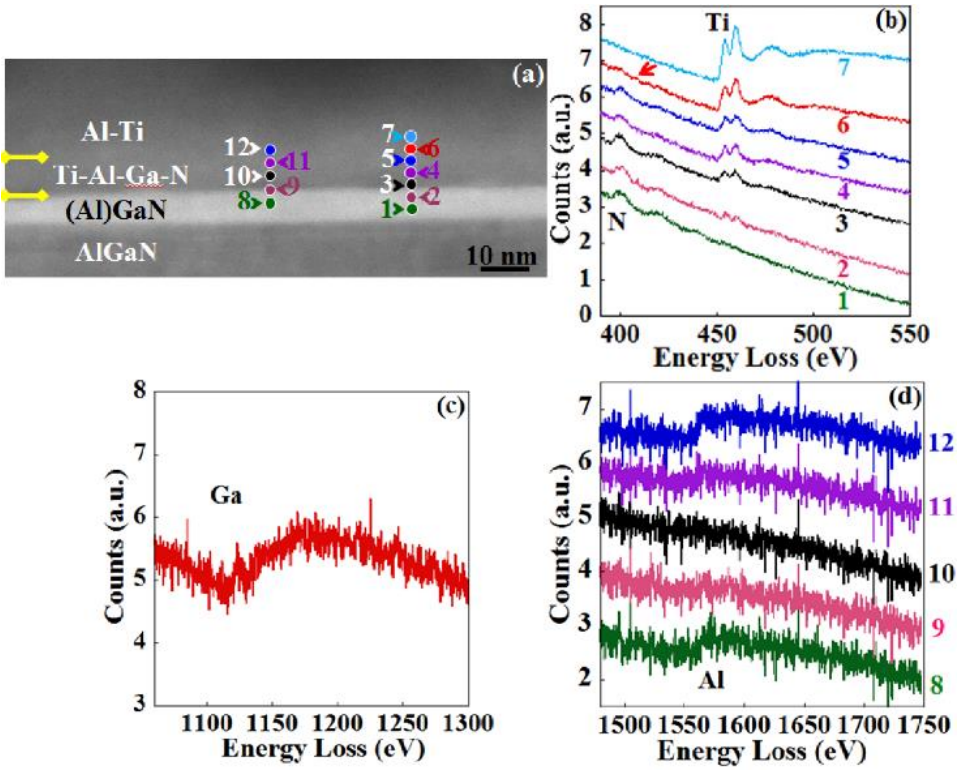

Figure 3-10 (a) High-magnification HAADF-STEM image collected near the metal/GaN interface of sample E [Al(3 nm)/Ti(50 nm)/Al(147 nm)] after annealing at 500 °C for 60 s. (b) EELS spectra collected from positions 1–7 in (a). As indicated by the arrow, N appeared in the metal layer ~6 nm away from the metal/GaN interface, indicating that the annealing may have caused a reaction between the metal and GaN. (c) EELS spectrum collected near position 5, which clearly shows the Ga edge. (d) EELS spectra collected from positions 8–12.

3.3.5 TEM characterization of thin Ti-first contacts

In contrast, for both sample A (with a thick 50-nm Ti layer, deposited first) and sample B (with a thin 5-nm Ti layer, deposited first), the Ti–Al–Ga–N interfacial layer did not form upon annealing. No Al reacted through the first Ti layer to reach the GaN. This situation was particularly evident for sample A because the first Ti layer was very thick (50 nm), as discussed in the previous section. A HAADF-STEM image of the as-deposited sample B is shown in **Figure 3-11**. Even with a thin Ti-first layer, the interfaces in (Ti(5 nm)/Al(15 nm)/Ti(45 nm)/Al(135 nm) appear to be sharp. A selected-area diffraction (SAD) pattern collected from a region containing all the layers is shown in **Figure 3-11**a. After annealing sample B at 500 °C for 60 s, however, the top Al and Ti layers reacted, and all of the top three layers transformed into Ti–Al intermetallics with clear Ti-rich and Al-rich layers (**Figure 3-12**). Beneath these layers, reaction between Ti and GaN appeared. EELS spectra from positions 2–6 in **Figure 3-12**(a,b) reveal the presence of Ti and N in both of the layers, called layers I and II. These layers also contained Ga (**Figure 3-12**c), but no Al appeared in layer I (**Figure 3-12**d). The lack of an interfacial layer containing Al in both samples A and B is correlated with their higher specific contact resistance relative to sample E.

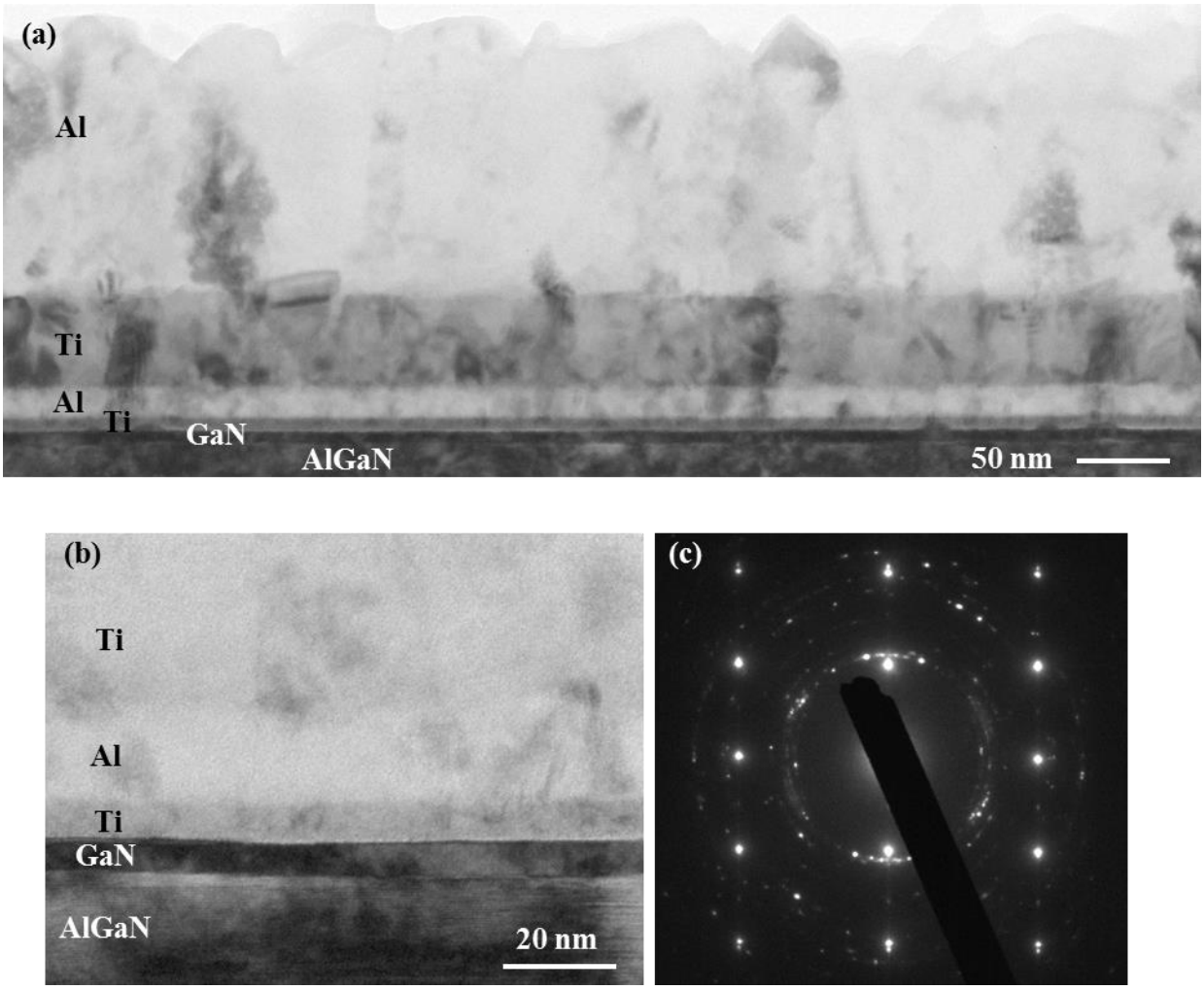

Figure 3-11 (a) Low-magnification and (b) higher-magnification bright-field TEM images of the as-deposited sample B. The interfaces between the layers appear to be sharp. (c) Selected-area diffraction pattern collected from a region containing all the layers shown in (a). The polycrystalline rings come from Al and Ti.

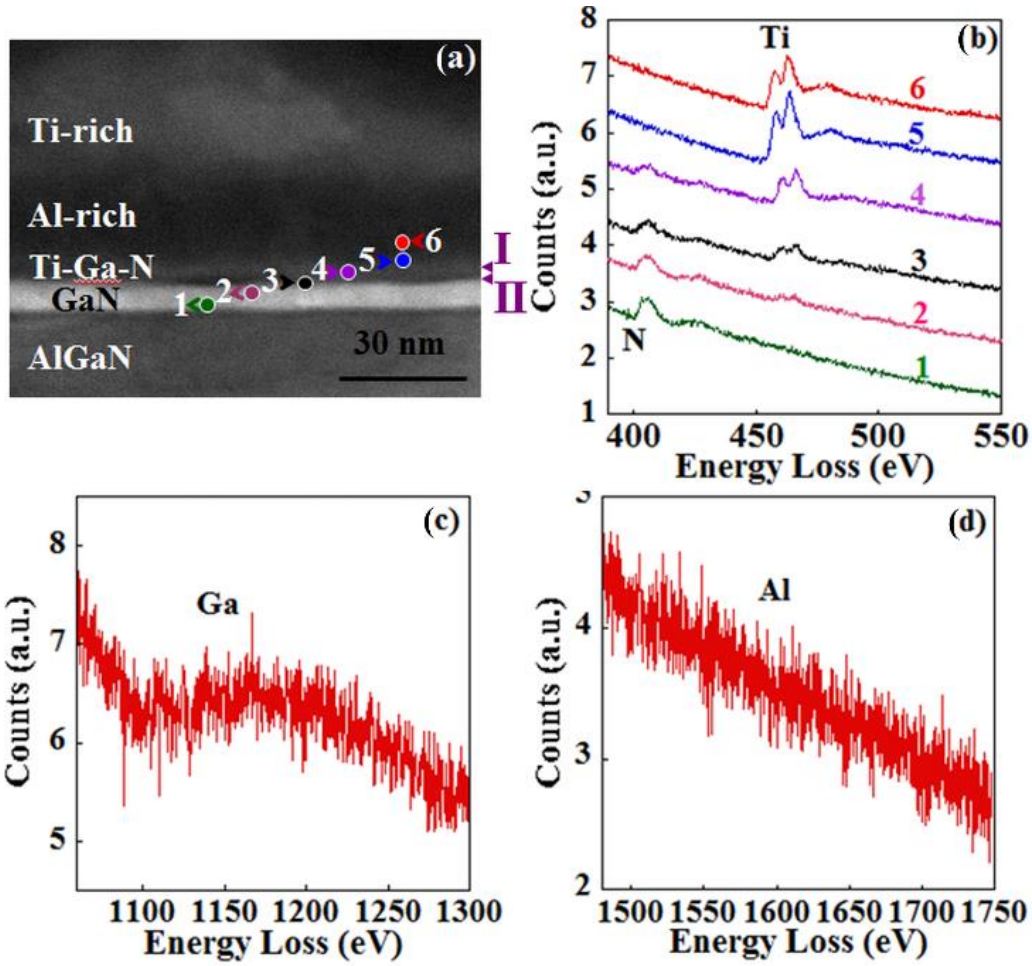

Figure 3-12 (a) Higher-magnification HAADF STEM image collected near the metal/GaN interface of sample B [Ti(5 nm)/Al(15 nm)/Ti(45 nm)/Al(135 nm)] after annealing at 500 °C for 60 s, revealing two very thin layers, layers I and II, indicated by the arrows. (b) EELS spectra collected from positions 1–6 in (a). (c) and (d) EELS spectra for Ga and Al collected from layer I. The Al edge is absent in (d). The Ti–Ga–N layers labeled I and II may have different Ti:Ga:N ratios. Layer I (spectrum 5) contains more Ti than layer II (spectrum 4), so it has higher average Z and brighter contrast.

3.4 Discussion

Because Ga appeared in the thin Ti–Ga–N or Ti–Al–Ga–N reaction product next to GaN, some GaN must have been consumed by reaction of the contact metals with GaN. However, the measured thicknesses of the GaN layers beneath the annealed contacts in samples A, B, and E varied by less than 0.5 nm (from 6.5 to 7.0 nm). Therefore, the observed variations in specific contact resistance must have been caused by changes at the contact/GaN interface rather than by a change in the GaN/AlGaN heterostructure. The original Ti and Al layer thicknesses determine whether Ti–Al–Ga–N or Ti–Ga–N forms adjacent to GaN, and the specific contact resistance appears to be sensitive to which phase forms.

The Ti–Al–Ga–N phase may have a lower work function than the Ti–Ga–N phase, lowering the Schottky barrier height[22] and reducing contact resistance. However, it is also possible that different point defect concentrations in GaN result from the different reactions between the contact metals and GaN. These defect populations can in turn affect tunneling through any Schottky barrier between the contact and GaN. The formation of N vacancies, which are donors, has long been speculated to enhance current transport in reacted contacts to n-GaN.[23] More recently, the addition of Ga has been found to reduce the resistance of Ohmic contacts to N-polar GaN,[11,21] and researchers have hypothesized that adding Ga and reducing outdiffusion of Ga might hinder the formation of unwanted Ga vacancies, which are acceptors. In our contacts, placing the group-III element Al adjacent to GaN might also hinder the formation of Ga vacancies, especially when Ti–Al–Ga–N forms, but also when the growth of Ti–Ga–N is severely limited by the formation of adjacent Ti–Al intermetallics when the initial Ti layer is thin.

3.5 Summary

We have shown that the formation of a Ti–Al–Ga–N interfacial phase reduces the resistance of Ohmic contacts to the N-polar GaN/AlGaN heterostructure, and that a low specific contact resistance to N-polar HEMTs can be achieved without a regrowth step. Even a minor variation in the Ti:Al ratio at the contact interface affects the interfacial phase formation, altering the specific contact resistance. In this dissertation work, the best contact metallization was Al(3 nm)/Ti(50 nm)/Al(147 nm), which as-deposited exhibited a ρ_c of 2.5×10^{-7} Ω·cm^2. When this contact was annealed at 500 °C for 60 s, its contact resistance barely changed, from 0.11 Ω·mm to 0.10 Ω·mm. This observation further demonstrates that the presence of both Al and Ti at the metal/GaN interface—prior to reaction of Ti with GaN to form a Ti–Ga–N layer—is critical to producing low-resistance Ohmic contacts to N-polar GaN/AlGaN HEMTs.

3.6 References

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3.7 Appendix

3.7.1 Impact of different surface treatments

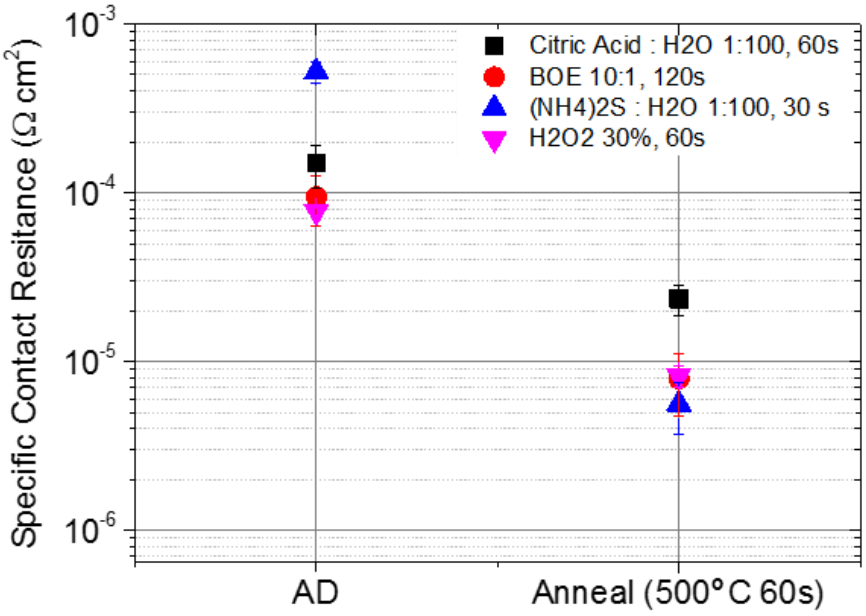
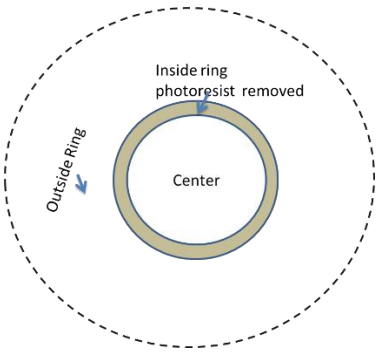


Figure 3-13 Specific contact resistances of Ti/Al contacts exposed to various surface treatments, before and after annealing at 500 °C for 60 s.

3.7.2 Surface elemental compositions analyzed using Auger electron spectroscopy for selected surface treatments

	Surface Treatment Parameters									
Sample Name	**Type of Treatment**	**Concentration**	**Time (seconds)**	**C/N**	**C/Ga**	**O/N**	**O/Ga**	**N/Ga**	**S/Ga**	**Comments**
Changing concentration experiment (diluted in DI water), same time of ammonium sulfide ($(NH_4)_2S$) treatment → 30 s										
Sample 1	Degreased	N/A	N/A	0.56	0.28	0.82	0.41	0.51	Noise	
Sample 2	$(NH_4)_2S$	10:1	30	0.39	0.25	0.23	0.15	0.66	0.06	
Sample 3	$(NH_4)_2S$	100:1	30	0.35	0.23	0.27	0.18	0.67	0.02	
Sample 4	$(NH_4)_2S$	24%	30	1.03	0.56	0.27	0.15	0.54	0.09	
Changing time experiment, same concentration of $(NH_4)_2S$ → 1:100 diluted in DI water										
Sample 5	$(NH_4)_2S$	100:1	300	0.46	0.29	0.28	0.18	0.62	0.06	
Sample 6	$(NH_4)_2S$	100:1	60	0.69	0.42	0.37	0.23	0.62	0.03	(average of 4 runs)
Sample 7	$(NH_4)_2S$ + Rinsed with IPA	100:1	120	0.33	0.24	0.27	0.19	0.70	0.04	
$(NH_4)_2S$ surface treatment shelf life experiment → sample analyzed after 1 month										
Sample 8	$(NH_4)_2S$	100:1	30	0.39	0.27	0.26	0.18	0.69	0.02	04/20/11-05/19/11
Buffered oxide etch surface treatment → BOE 10:1 treatment for 120s → H_2O rinse										
Sample 9	BOE	10:1	120	N/A	0.20	0.25	0.17	0.70	N/A	
CTLM patterned sample treated with → (30s $(NH_4)_2S$ treat + H_2O rinse + 1min 30% H_2O_2 treatment) X 5 → then photoresist is removed										
Outside Ring	$(NH_4)_2S$ → **H_2O_2**	100:1	N/A	0.71	0.45	0.24	0.15	0.63	0.02	Region where the photoresist was removed by CD26 developer
Inside Ring	$(NH_4)_2S$ → **H_2O_2**	100:1	N/A	0.80	0.43	0.71	0.39	0.54	Noise	Region where photoresist was removed by remover PG
Center	$(NH_4)_2S$ → **H_2O_2**	100:1	N/A	0.45	0.29	0.25	0.16	0.65	0.01	Region where the photoresist is removed by CD26 developer



3.7.3 Impact of annealing temperature and ammonium sulfide surface treatment

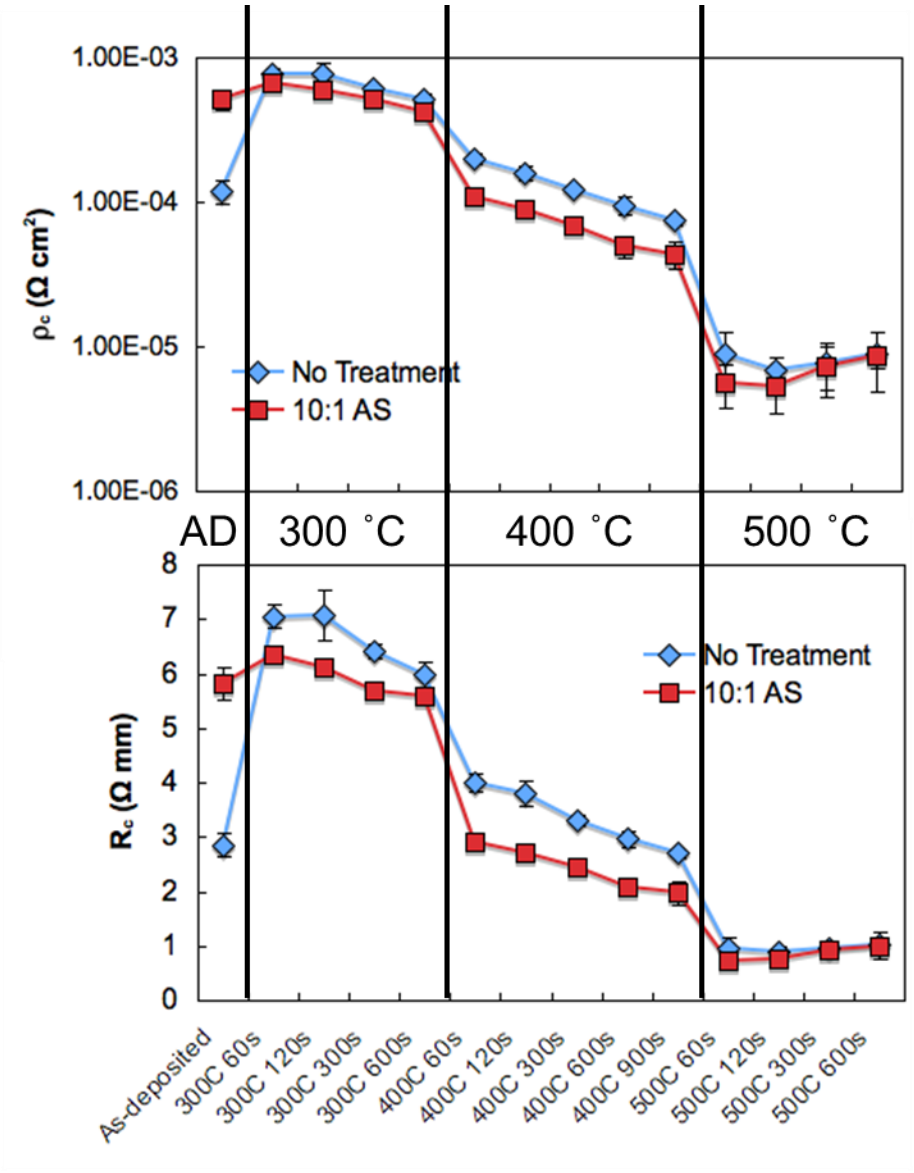


Figure 3-14 Specific contact resistance and contact resistance as a function of annealing temperature for two samples, one treated with ammonium sulfide ($(NH_4)_2S$ 1:10 diluted in DI water) and one untreated. The as-deposited $(NH_4)_2S$-treated samples exhibited higher contact resistance than the untreated samples. Courtesy of Brian Downey.

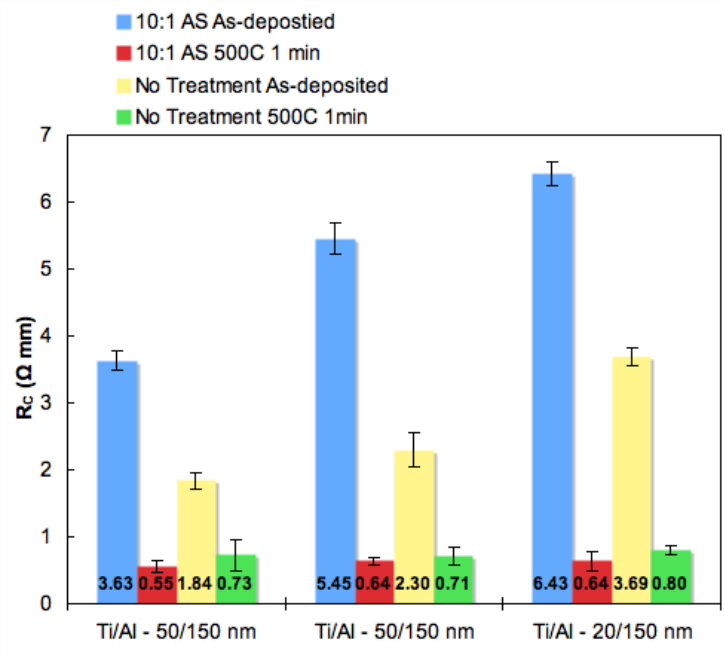


Figure 3-15 Contact resistance of as-deposited and annealed Ti/Al contacts (at 500 °C for 60 s), with and without $(NH_4)_2S$ surface treatment. After surface treatment with ammonium sulfide, contacts with thick and thin Ti-first layers yielded similar results.

3.7.4 Electron-beam evaporation compared with sputtering

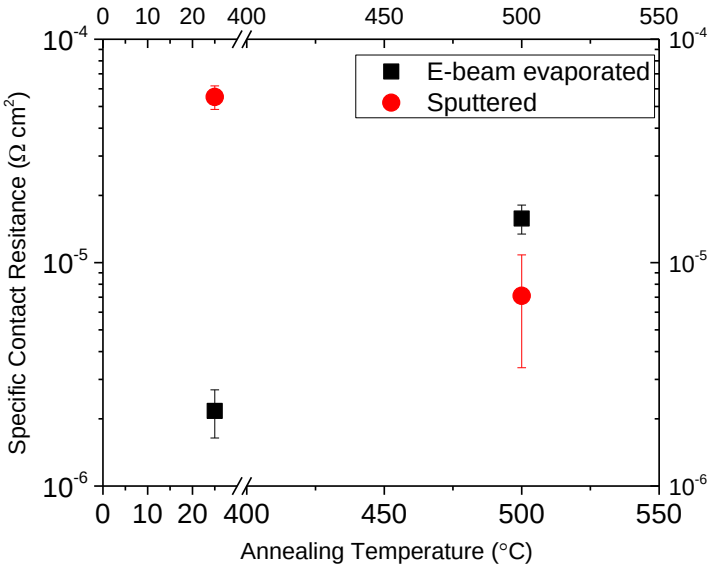


Figure 3-16 Specific contact resistance as a function of annealing temperature for Ti/Al contacts deposited using e-beam evaporation or DC magnetron sputtering.

Chapter 4

Self-aligned Ni contacts to InP-capped and uncapped n^+-$In_{0.57}Ga_{0.43}As$*

*Please note: Significant portions of this manuscript are already published in the *Journal of Applied Physics*.[1]

4.1 Introduction

InGaAs exhibits higher electron mobility and electron injection velocity than Si,[2] making InGaAs a prime candidate to replace Si as a channel material in metal–oxide–semiconductor field-effect transistors (MOSFETs). However, as the dimensions of MOSFETs shrink, their contact area shrinks, and their source/drain (S/D) resistance can dominate, limiting their drive current.[3,4] Therefore, the success of InGaAs FETs depends on the development of scalable Ohmic contacts to n-InGaAs with extremely low specific contact resistances (ρ_c), controlled morphologies, and simple process integration.

Recently, annealed Ni has been used as S/D contacts to n-InGaAs.[5,6,7,8] This interest in Ni results from the formation of a silicide-like compound, $Ni_xIn_yGa_{1-y}As$ (Ni_xInGaAs), upon annealing[9,10] Due to the availability of a selective etchant for unreacted Ni, this contact metallization allows for the self-alignment of S/D contacts to the gate electrode of MOSFETs.[5,7,8,11] Avoiding misalignment reduces the gate-to-S/D overlap parasitic capacitance. Simultaneously, excess space between the gate and S/D contacts can be avoided, further reducing

the transistor dimensions. Furthermore, self-alignment brings the S/D contacts close to the channel, lowering access resistance (**Figure 4-1**).[12]

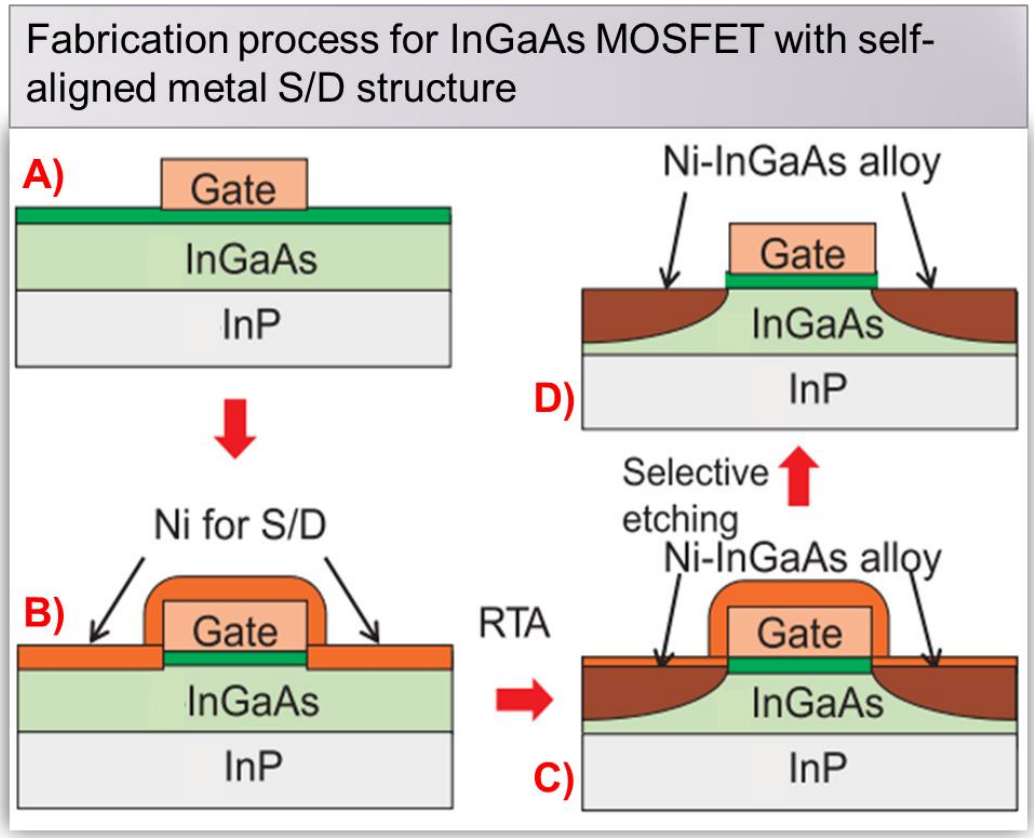


Figure 4-1 Schematic of a simplified process flow for Ni-based self-aligned contacts. Figure adopted from Kim *et al.*[13]

Progress has been made toward developing $Ni_xInGaAs$ contacts to n^+-InGaAs. Zhang *et al.*[7] reported a relatively high ρ_c of 1×10^{-6} Ω·cm^2 after depositing 13 nm of Ni on heavily doped $In_{0.53}Ga_{0.47}As$ ($N_D = 5 \times 10^{19}$ cm^{-3}) and then annealing for 60 s in N_2 ambient at 250 °C. Similar results showing encouraging device performance have been reported by other authors.[5,8,14] However, the specific contact resistances of Ni contacts are much higher than those reported for other state-of-the-art contacts to heavily doped n^+-$In_{0.53}Ga_{0.47}As$ (~10^{-8} Ω·cm^2).[15] Limited work

has been done to understand how annealing temperature affects the specific contact resistance of Ni contacts. Furthermore, earlier work on Ni contacts has relied on the traditional transmission line model (TLM) to extract ρ_c. This model assumes zero metal sheet resistance and equipotential metal contacts, potentially causing significant errors in determining the true ρ_c.

In this dissertation work, we demonstrate how annealing temperature and pre-metallization surface treatment affect the electrical properties of Ni contacts on both InP-capped and uncapped n^+-InGaAs. The electrical contacts were Ti(15 nm)/Pt(15 nm)/Au(100 nm) deposited on the Ni contact to minimize the metal sheet resistance, improving the measurement of specific contact resistance. Refined transmission line model (RTLM) test structures were then used to determine ρ_c. The RTLM test structure allows for uniform lateral distribution of the potential across the contact pad, better meeting one assumption of the transmission line model. Finally, TEM and AES were used to better understand how interfacial reactions and surface preparation affected the contact resistance.

4.2 Experimental

Ni-based alloyed contacts to n-InGaAs were fabricated on four sets of Si-doped $In_{0.53}Ga_{0.47}As$ (N_D = 3 × 10^{19} cm^{-3}) epilayers grown by MOVPE on semi-insulating InP wafers. The first and second sets of samples were prepared on 100-nm and 200-nm $In_{0.53}Ga_{0.47}As$ layers, respectively. We used two thicknesses in order to evaluate how the semiconductor sheet resistance increased from consumption of the InGaAs epilayer during reaction with Ni. The third set was prepared on 100 nm of heavily doped $In_{0.53}Ga_{0.47}As$ capped with 5 nm of InP, a structure used by Lee *et al.* to enhance the thermal stability of the Ni_xInGaAs contacts.[6] The fourth set was prepared on 100 nm of heavily doped $In_{0.53}Ga_{0.47}As$ capped with 10 nm of InP. Samples 1–4 listed in **Table 4-1** were

made from sets 1–4, respectively. Samples 5 and 6 were made from sets 4 and 1, respectively, but were passivated with sulfur before metallization.

Table 4-1 Nickel-based contact metal stacks and epilayers investigated in this work.

Sample	Structure
1	InGaAs(100 nm)//**Ni(10 nm)**/Ti(15 nm)/Pt(15 nm)/Au(100 nm)
2	InGaAs(200 nm)//**Ni(10 nm)**/Ti(15 nm)/Pt(15 nm)/Au(100 nm)
3	InGaAs(100 nm)/InP(5 nm)//**Ni(10 nm)**/Ti(15 nm)/Pt(15 nm)/Au(100 nm)
4	InGaAs(100 nm)/InP(10 nm)//**Ni(10 nm)**/Ti(15 nm)/Pt(15 nm)/Au(100 nm)
5	InGaAs(100 nm)/InP(10 nm)/(S-passivation)//**Ni(10 nm)**/Ti(15 nm)/Pt(15 nm)/Au(100 nm)
6	InGaAs(100 nm)/(S passivation)//**Ni(10 nm)**/Ti(15 nm)/Pt(15 nm)/Au(100 nm)

Before metallization, each wafer was cut into 1 × 1-cm pieces. Each piece was degreased sequentially in acetone, isopropanol, and deionized (DI) water for 1 min each under continuous sonication, then blown dry with compressed nitrogen. The samples were then dehydration-baked for 5 min at 115 °C immediately before lithography. The specific contact resistance was measured using refined transmission line method (RTLM) test structures[16] with nominal gap spacings of 0.7–10 μm. The test structures were defined using a dual-layer resist stack (NANO^{TM} PMGI SF9 and SPR3012) followed by exposure in a GCA 8000 i-Line Stepper tool. The resist was developed with CD-26 (>95% water, 2.4% tetramethylammonium hydroxide), then exposed to a deep UV flood, then finally developed with PMGI 101A.

After lithography, samples were placed in a UV/ozone chamber in flowing dry 80% N_2/20% O_2 for 10 min. UV/ozone surface treatment helps remove resist residue and other organic contaminants. Immediately before metallization, the surface oxide was etched using a 10:1 (NH_4F:49% HF) buffered oxide etch (BOE) solution for 2 min, rinsed with deionized (DI) water,

and dried with compressed N_2. In addition, two samples (see **Table 4-1**) were then exposed to a sulfide surface treatment of 1:100 (20% ammonium sulfide:DI water) for 10 s and then rinsed and dried with compressed nitrogen. After surface treatment, all samples were quickly loaded into an electron-beam evaporation chamber. After the chamber reached the desired base pressure of $< 2 \times 10^{-7}$ Torr, Ti was evaporated to getter oxygen from the chamber and to further lower the base pressure. Finally, Ohmic contact stacks of Ni(10 nm)/Ti(15 nm)/Pt(15 nm)/Au(100 nm) were deposited on the samples (see Appendix 4.6.1 for a schematic of the metal stack).

We chose the thickness of the Ni layer based on previous reports that yielded Ohmic contacts with relatively low resistance (but not as low as needed).[5,7] Excess Ni on 25-nm p-InGaAs layers on InP substrates has been shown to penetrate into the underlying InP substrate, forming Ni_xInP upon annealing at 250 °C for 1 min.[17] Excess Ni can also produce an extensive lateral reaction into the channel, degrading device performance. Hence, adding a very thin Ni contact layer helps prevent these problems. Because the thickness of Ni is directly correlated with the amount of Ni_xInGaAs formed, thinner as-deposited Ni forms a shallow Ni_xInGaAs layer upon annealing.[9,18] The shallowness of the reaction is particularly important for aggressively scaled contacts, as n^+/p S/D junctions are expected to be less than 10 nm thick.

An alternative approach reported by various authors but not applied in this dissertation work is two-step annealing. The first annealing step, at lower temperature, forms Ni_xInGaAs. Excess Ni is then selectively etched away using HCl without etching the Ni_xInGaAs. The second annealing step, at higher temperature, completes the formation of a lower-resistance interface with Ni_xInGaAs of the desired composition.[11]

Following contact deposition and lift-off, aligned RTLM mesas were defined lithographically (**Figure 4-2**). The patterned InGaAs was etched in acetic acid, phosphoric acid, anhydrous citric

acid, and hydrogen peroxide (6 mL : 1 mL : 1 g : 1 mL). For samples with an InP cap, hydrochloric acid was used to remove InP in the areas where the mesa was to be etched. Samples were then annealed at temperatures from 225 °C to 400 °C for 60 s in a rapid thermal annealing furnace (AG610) in gettered Ar.

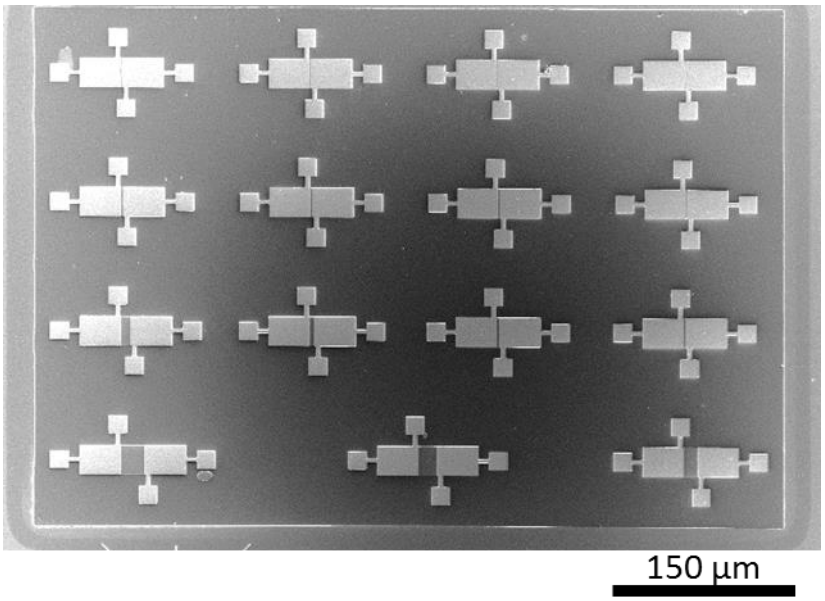


Figure 4-2 Typical set of 15 RTLM test structures after mesa etch, with gap widths of 0.6–10 µm. Only the structures with gap widths of 0.6–2 µm were used in this work.

Current–voltage measurements were done for both the as-deposited and annealed samples using four probes. Specific contact resistance, contact resistance, and semiconductor sheet resistance were extracted from the plots of total resistance versus gap spacing. Gap spacings were measured by scanning electron microscopy (SEM). Performing cross-sectional transmission electron microscopy (TEM) and scanning TEM (STEM) using a JEOL EM-2010F microscope and Philips CM300 equipped with a Noran Si:Li X-ray detector, we studied the interfacial morphology and extent of reaction of Ni with n-InGaAs. The elemental compositions of the samples were

determined with XEDS in the TEM and an AES depth profile measured on a scanning Auger microprobe (PHI 670).

4.3 Results and discussion

4.3.1 Specific contact resistance

The first contacts to n-InGaAs investigated in this work were Ni(10 nm)/Ti(15 nm)/Pt(15 nm)/Au(100 nm) on heavily doped n-InGaAs layers with thicknesses of 100 nm and 200 nm, both with no InP capping layer. The ρ_c values for the as-deposited contacts were $9.0 \times 10^{-8}\,\Omega\cdot\text{cm}^2$ and $6.0 \times 10^{-8}\,\Omega\cdot\text{cm}^2$ on the thinner and thicker n-InGaAs, respectively. Upon annealing below 250 °C for 60 s, the ρ_c increased by an order of magnitude. After annealing at temperatures higher than 250 °C, the ρ_c for both the 100-nm and 200-nm n-InGaAs samples started to decrease (**Figure 4-3**a). Minimum ρ_c values of $4.6 \times 10^{-8}\,\Omega\cdot\text{cm}^2$ and $5.3 \times 10^{-8}\,\Omega\cdot\text{cm}^2$ were achieved, respectively, when both samples were annealed at 350 °C for 60 s.

A relatively high scatter appeared in the plot of resistance versus gap spacing for the as-deposited samples and those samples annealed at 200–300 °C compared to samples annealed at 350 °C for 60 s. This data scatter is also reflected by the larger error bars for the standard deviation from different sets of test structures (see **Figure 4-3**a). InGaAs samples, capped with 5 nm and 10 nm of InP, after annealing for 60 s at 350 °C, exhibited ρ_c values of 4.8×10^{-8} and 4.0×10^{-8}, respectively (**Figure 4-3**b). The specific contact resistance increased slightly for both the InP-capped and uncapped InGaAs after annealing at 400 °C (**Figure 4-3**). In addition, the InP-capped samples showed less scattering in their plots of resistance versus gap spacing.

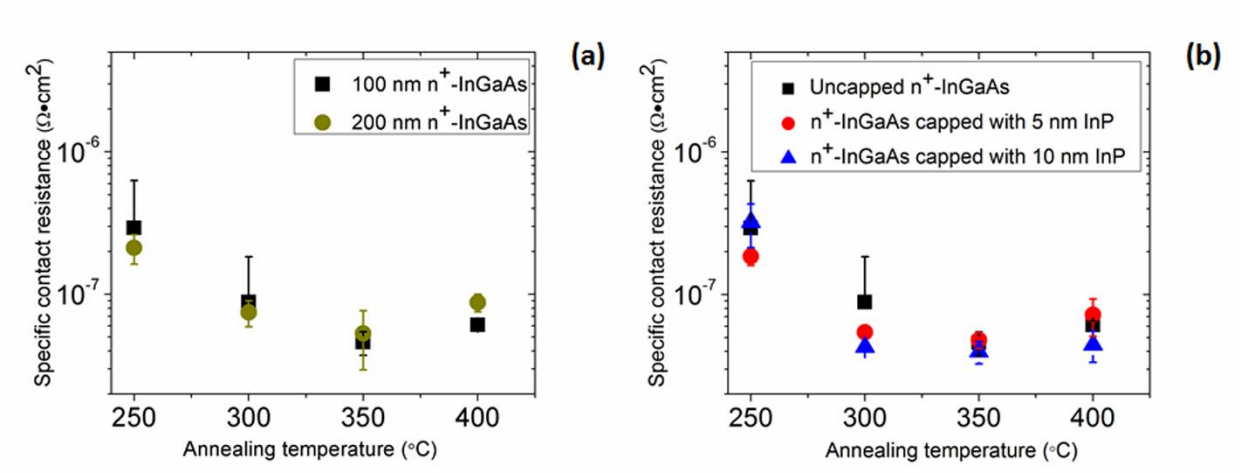


Figure 4-3 (a) Specific contact resistance as a function of annealing temperature on n^+-InGaAs with various epilayer thicknesses (b) Specific contact resistance as a function of annealing temperature on 100 nm of n^+-InGaAs with different thicknesses of InP caps. The annealing time for all samples is 60 s.

Even with BOE treatment before metallization, both InGaAs and InP surfaces re-oxidize before metal deposition, affecting current transport at the metal/semiconductor interface. However, surface treatments based on ammonium sulfide have been shown to provide an effective surface chemical passivation and prevent re-oxidation of the InGaAs surface.[19] To test how this surface treatment affects Ohmic contacts on InP-capped and uncapped InGaAs, two samples—one with a 10-nm InP cap on 100 nm of InGaAs, and one without the InP cap on 100 nm of InGaAs—were treated with ammonium sulfide for 10 s before metallization. Then, a Ni(10 nm)/Ti(15 nm)/Pt(15 nm)Au(100 nm) contact was deposited on both samples.

With the surface treatment, the as-deposited ρ_c of the InP-capped sample decreased from $1.3 \times 10^{-7}\,\Omega\cdot\text{cm}^2$ to $3.3 \times 10^{-8}\,\Omega\cdot\text{cm}^2$. Similarly, for the uncapped sample, ρ_c decreased from $9.8 \times 10^{-8}\,\Omega\cdot\text{cm}^2$ to $1.1 \times 10^{-8}\,\Omega\cdot\text{cm}^2$. Hence, the sulfide-treated samples had much lower ρ_c than samples treated with BOE only. After annealing at 350 °C for 60 s, the sulfide-treated samples

exhibited ρ_c values of $2.1 \times 10^{-8}\ \Omega\cdot\text{cm}^2$ and $1.8 \times 10^{-8}\ \Omega\cdot\text{cm}^2$ with and without the InP cap, respectively (see **Figure 4-4**).

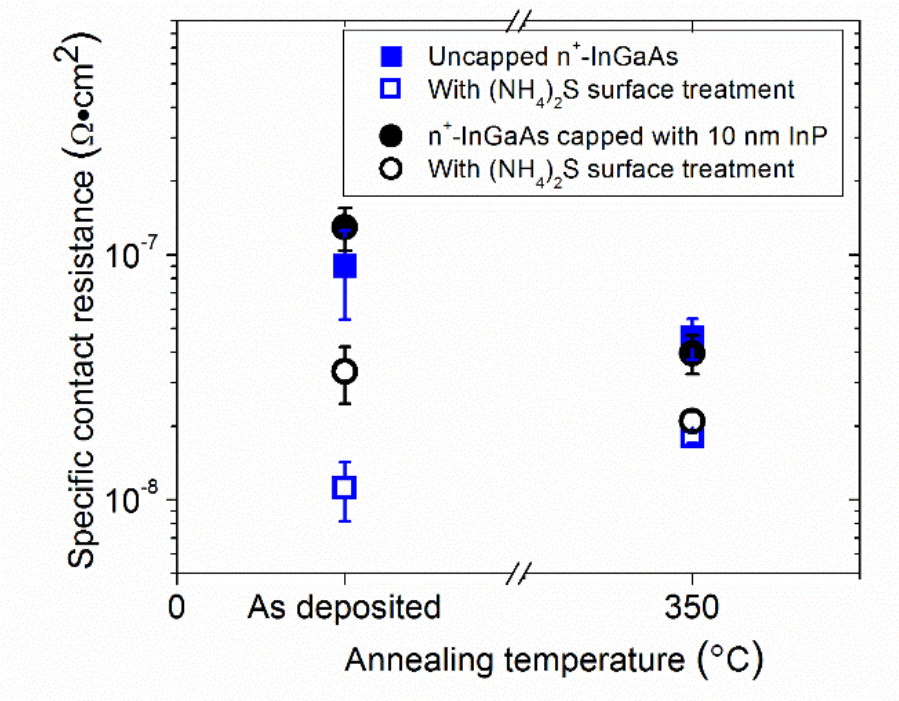


Figure 4-4 Specific contact resistance as a function of annealing temperature, showing the effect of $(NH_4)_2S$ surface treatment before metallization. The annealing time was held at 60 s.

4.3.2 Materials characterization

We performed TEM to further understand the contact interfaces and alloy formation between Ni and the underlying semiconducting epilayers. For the as-deposited contacts, the TEM micrograph in **Figure 4-5** shows that there was limited or no reaction between Ni and the underlying InGaAs. These micrographs also show that samples treated with ammonium sulfide formed an intimate contact between Ni and InGaAs with no oxide at the interface (**Figure 4-5**a). However, for the untreated samples, a thin native oxide layer was still present at the interface

(**Figure 4-5**b), explaining the higher specific contact resistance of the as-deposited untreated samples.

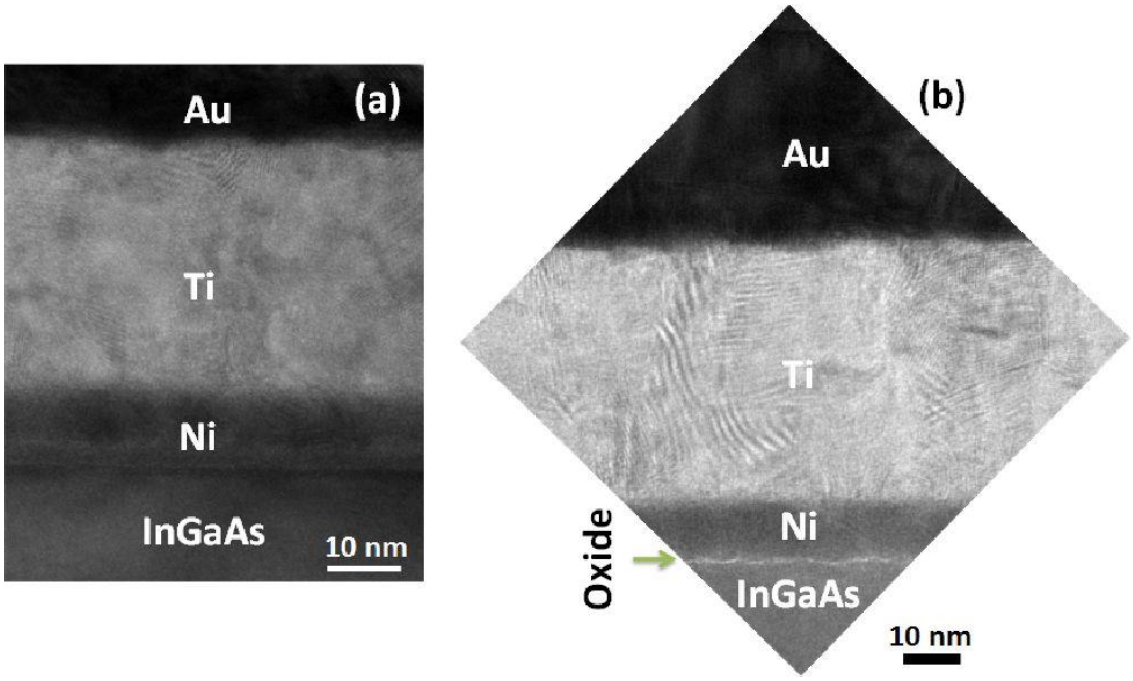


Figure 4-5 Bright-field TEM image of as-deposited Au(100 nm)/Ti(45 nm)/Ni(10 nm) on uncapped InGaAs (a) with $(NH_4)_2S$ surface treatment and (b) without $(NH_4)_2S$ surface treatment. The Pt layer was omitted from metal stack in these samples for ease of fabrication.

Figure 4-6 shows bright-field cross-sectional TEM (XTEM) images of Ni contacts annealed at 350 °C for 60 s on uncapped and 10-nm InP-capped n-InGaAs. Nickel reacted extensively with the uncapped InGaAs forming a uniform 20-nm Ni_xInGaAs layer, similar to that formed when Ni reacts with GaAs.[20]. Nickel reacted less with the InGaAs under the InP capping layers, particularly in samples with the 10-nm InP cap. In this case, Ni reacted first with InP, forming Ni_xInP, limiting the supply of Ni to react with the underlying InGaAs and forming a shallower contact. Hence, the InP cap is one way to control the penetration of the metallization into the InGaAs channel, which is important for aggressively scaled devices.

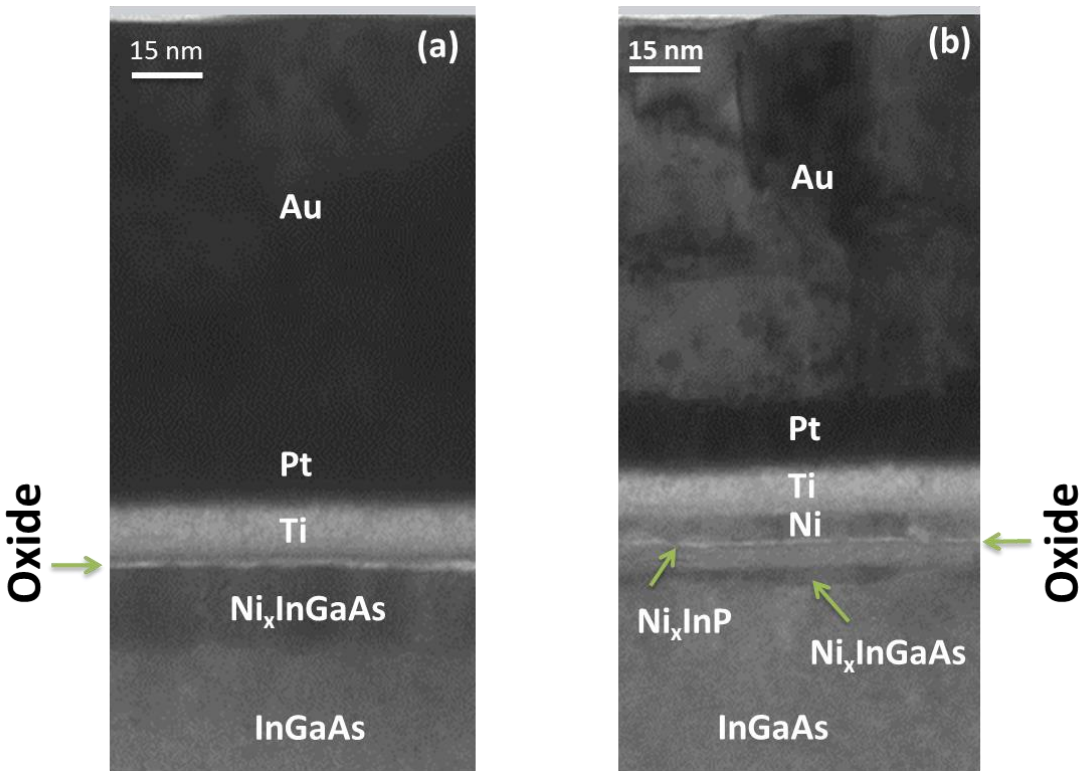


Figure 4-6 Bright-field TEM image of Au(100 nm)/Pt(15 nm)/Ti(15 nm)/Ni(10 nm) contacts on (a) uncapped InGaAs and (b) 10-nm InP capped InGaAs, both annealed at 350 °C for 60 s.

The Ni_xInGaAs phase formed by annealing appears to be crystalline with an epitaxial relationship with the underlying InGaAs layer. This finding is supported by earlier reports by Shekhter *et al.*[10] and Mehari *et al.*[17] They used TEM, X-ray photoelectron spectroscopy, secondary ion mass spectroscopy (SIMS) and X-ray diffraction (XRD) to study the composition and structural symmetry of Ni_xInGaAs. For samples with 6 nm of Ni on $In_{0.53}Ga_{0.49}As$ annealed at 250 °C for 1 min by rapid thermal annealing (RTA) in forming gas, the solid-state reaction yielded a uniform single phase of $Ni_2In_{0.53}Ga_{0.49}As$. Ni_2InGaAs exhibits a similar hexagonal crystal structure to NiAs (**Figure 4-7**a). The NiAs crystal structure is shared by other ternary phases such as Ni_xInP, Ni_xGaAs, and Ni_xInAs, where the composition parameter *x* ranges from 2 to 3 depending on the

thickness of the Ni and the annealing temperature (**Figure 4-7**). The In–As–Ni ternary diagram in **Figure 4-7**c shows that the Ni_xInAs phase represent a specific composition of the ζ solution phase.

$Ni_2InGaAs$ was characterized by the following epitaxial relationship to (001) InGaAs underlying layer.[9]

$$\{100\}_{InGaAs}||\{100\}_{NiInGaAs};\langle 011\rangle_{InGaAs}||[001]_{NiInGaAs}$$

We believe the processing conditions reported in this work also led to the formation of a quaternary phase similar in both symmetry and composition.

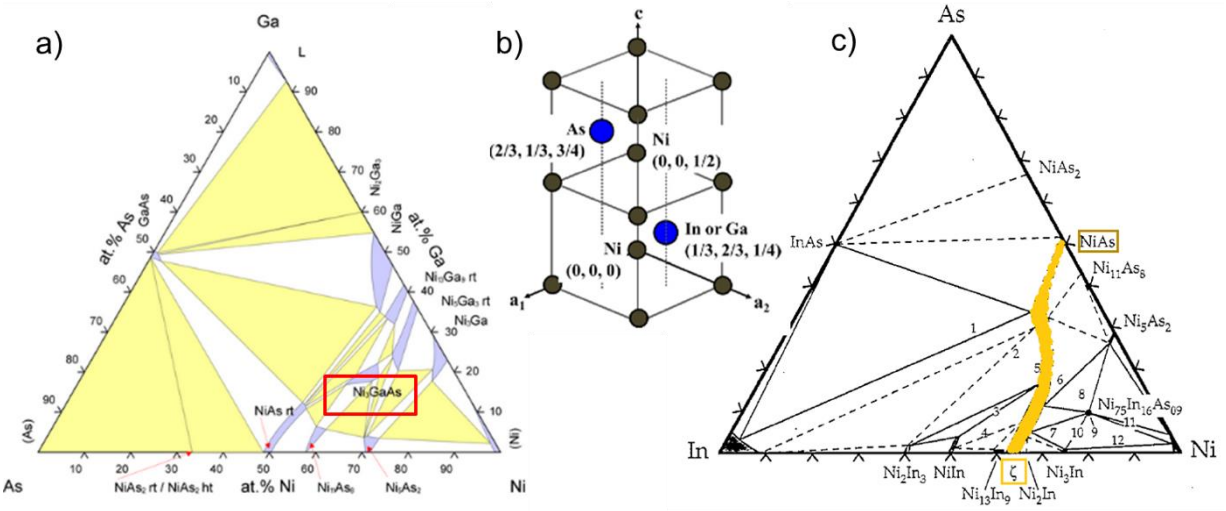


Figure 4-7 (a) Ni–Ga–As ternary phase diagram showing the presence of the Ni_3GaAs phase. (b) Hexagonal structure of NiAs, a structure prevalent among other silicide-like phases such as Ni_xGaAs, Ni_xInAs, and $Ni_xInGaAs$. (c) Ni–In–As ternary phase diagram showing Ni_xInAs as a specific composition of the ζ solution phase. Source: ASM Alloy Phase Diagram Database™.

The reaction of Ni with the underlying semiconductor(s), as described earlier, occurs despite the presence of the native oxide. The Ni penetrates the native oxide and appears above the reaction products.[21,22] This dispersion of the native oxide explains why ρ_c was higher for the as-deposited samples than the samples annealed at 350 °C for 60 s. However, after surface treatment with

ammonium sulfide, ρ_c remained relatively low before and after annealing because the native oxide was more completely eliminated (**Figure 4-6**). We can explain the observed trend by considering the following: For heavily doped InGaAs, such as that used in this work, current transport occurs by field emission (tunneling through the depletion region). The presence of the oxide layer at the interface imposes another resistance. Meanwhile, an oxide-free interface enables intimate contact between the metal and semiconductor, enhancing current transport. We can further compare our result with calculations by Lin *et al.* for contacts to n-InGaAs (**Figure 4-8**).[22] Given our lowest calculated specific contact resistance ($1.8 \times 10^{-8}\ \Omega\cdot cm^2$) and heavy doping of the InGaAs ($N_D = 3 \times 10^{19}\ cm^{-3}$), we expect a barrier height of approximately 0.24 eV. This value agrees well with the Schottky barrier height of 0.24±0.01 eV reported by Mehari *et al*. for reacted Ni contacts to lightly doped n-InGaAs.[23]

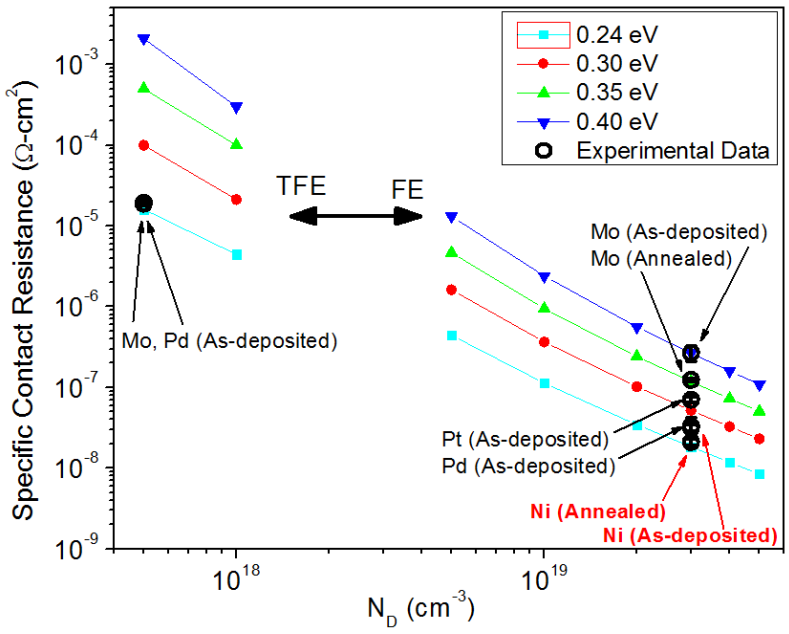


Figure 4-8 Calculated specific contact resistance as a function of doping concentration and barrier height for n^+-$In_{0.53}Ga_{0.47}As$. The open and closed black circles represent experimental data for the Pd, Pt, Mo, and Ni contacts. This figure, except for the Ni data, comes from work by Lin *et al*.[22]

XEDS and an AES depth profile helped us to identify the products of reaction of Ni with InP and InGaAs. No significant out-diffused Ga or As appeared in the Ti/Pt/Au layers. In addition, very little reaction between Ni and the overlying Ti/Pt/Au layers appeared for contacts annealed at 350 °C for 60 s (**Figure 4-9**, Appendix 4.6.2 shows the AES depth profile for an as-deposited contact). Therefore, the specific contact resistances we report should reflect the actual specific contact resistance for annealed Ni/InGaAs and Ni/InP/InGaAs contacts with no Ti/Pt/Au.

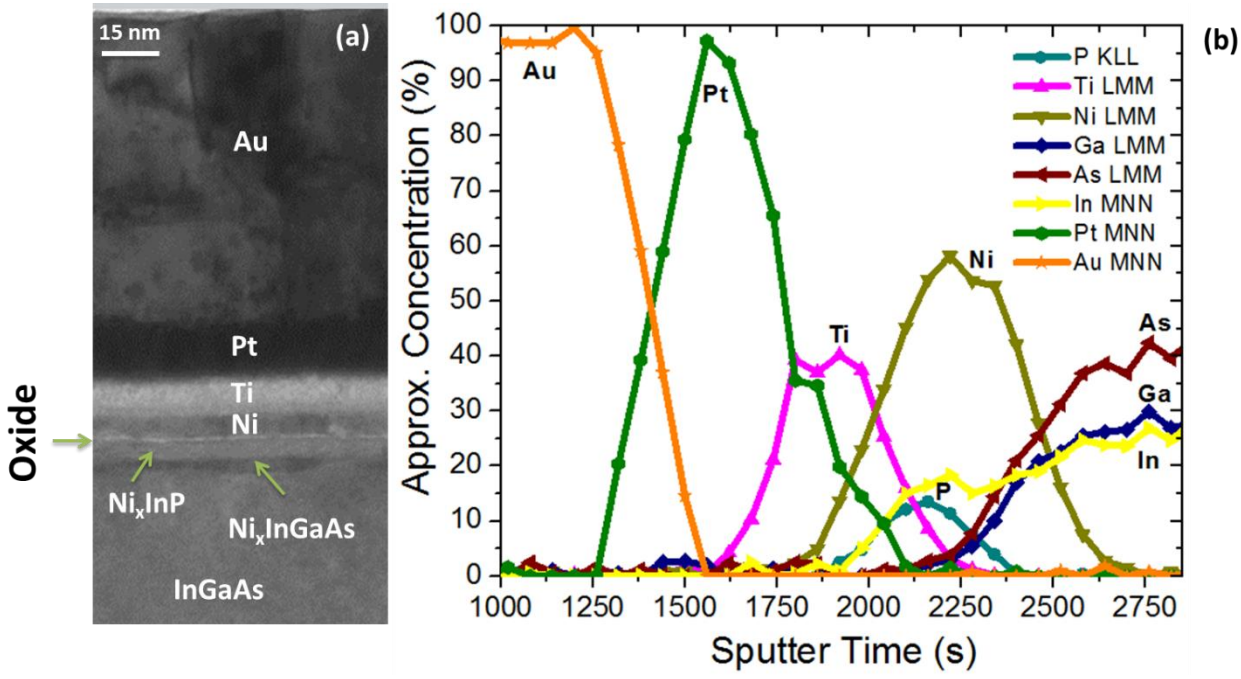


Figure 4-9 (a) Bright-field TEM image of Au(100 nm)/Pt(15 nm)/Ti(15 nm)/Ni(10 nm) on 10-nm InP-capped InGaAs annealed at 350 °C for 60 s. (b) AES depth profile of the same sample.

Finally, we will discuss the higher resistance of samples annealed at 200 °C for 60 s. The literature indicates that annealing at only 200 °C can induce a non-uniform reaction between Ni and InGaAs, forming only islands of reaction products at the interface.[9,20,17,24] For Ni/GaAs in particular, the presence of a residual native oxide at the Ni/GaAs interface has been shown to promote the formation of Ni–Ga and Ni–As compounds over the formation of the Ni$_x$GaAs ternary

phase.[25] These features of the reaction might have caused the increase in ρ_c measured after annealing at modest temperatures. Likewise, other work has shown possible phase separation and agglomeration of Ni_xInGaAs upon annealing above 450 °C.[6]

4.3.3 Accuracy of reported specific contact resistance measurements

In contrast to experiments reported in the literature[7,5], in this work we made three key adjustments to more accurately extract the specific contact resistance using the transmission line model. First, we deposited a low-resistance Ti (15 nm)/Pt(15 nm)/Au(100 nm) cap to minimize the effect of the Ni_xInGaAs sheet resistance. Neglecting a high metal sheet resistance produces appreciable errors, often leading to overestimation of ρ_c.[26,27,28,29]

Second, we used 100-nm- and 200-nm-thick InGaAs epilayers so that the sheet resistance of the semiconductor under the metal would be nearly the same as the sheet resistance of the semiconductor between the contacts. To show that we accomplished this goal, we estimated a corrected ρ_c by calculating using the reaction depth, measured by TEM, assuming that the semiconductor sheet resistance scaled simply with epilayer thickness.[22] The difference between the corrected ρ_c and the measured nominal ρ_c was no more than a 20%.

Third, we used a refined TLM test structure (see Dormaier *et al.*[16]) to promote uniform current flow across the contact width. Similar test structures have been used in other measurements of Ohmic contacts with very low resistance.[15] The test structure is composed of electrical contact pads with a high length-to-width ratio. The probes that source current are placed at the rear centers of the pads, while the voltage is measured at the fronts of the pads, ensuring that the potential is uniformly distributed laterally across the pads (see the inset of |To further justify our use of the refined TLM test structure and Ti/Pt/Au cap, we consider the case where these approaches are not

used. To do so, we apply a two-layer TLM model developed by Marlow and Das[26] and expanded by Finetti *et al.*[27] This model was originally developed to correct for finite metal sheet resistance (R_{sm}) when measuring ρ_c . It assumes uniform current flow across the contact width but takes into account the effect of metal sheet resistance when the voltage is not probed at the very front of the contact. An expression for the effective ρ_{c_eff} derived from the model is given below.[27]

$$\rho_{c,\mathrm{eff}} = R_s \left[\frac{\frac{\rho_{c,\mathrm{true}}}{a} + R_{sm}\ d' - a\ + \frac{aR_{\mathrm{sm}}^2}{R_s}}{R_s + R_{\mathrm{sm}}} \right]^2 \text{ where } a = \sqrt{\frac{\rho_{c,\mathrm{true}}}{R_s + R_{\mathrm{sm}}}} \qquad (1)$$

In Eq. 1 above, R_s is the sheet resistance of the semiconductor between the contacts. For the 100-nm-thick InGaAs used in this work, R_s = 24 Ω/□. When 10 nm of Ni reacts with InGaAs with no InP cap, it forms 20 nm of Ni$_x$InGaAs (**Figure 4-5**a). The metal sheet resistance for 20 nm of Ni$_x$InGaAs is not directly measured in this experiment, but it is reported to be R_{sm} = 43 Ω/□ by Zhang *et al.*[7] The length of the RTLM test structure in the direction of the current flow is d = 30 μm. However, to measure constant voltage across the contact pad, the position of the voltage measurement (d') is set at d' = 1/3d from the front of the contact. Finally, $\rho_{c,\mathrm{true}}$ is the true specific contact resistance for a contact prepared with an infinitely conductive metal layer (R_{sm} = 0 Ω/□).

The relationship between $\rho_{c,\mathrm{eff}}$ and $\rho_{c,\mathrm{true}}$ is plotted for various metal sheet resistances (**Figure 4-10**). For a high R_{sm} = 43 Ω/□ and no Ti/Pt/Au metal, $\rho_{c,\mathrm{eff}}$ is greater than the true specific contact resistance of 1.8 × 10^{-8} Ω·cm^2 by more than two orders of magnitude. This prediction agrees well with the data reported so far, and it provides a plausible explanation for why ρ_c reported in this work is about two order magnitudes lower than in previous work that does not use (or does not report using) a Ti/Pt/Au cap to minimize the influence of R_{sm}. Due to the high

metal sheet resistance[26-29] of $Ni_xInGaAs$ (R_{sm} of 15–43 Ω/□), the conventional TLM approach could lead to overestimation of ρ_c.[5,7,8]

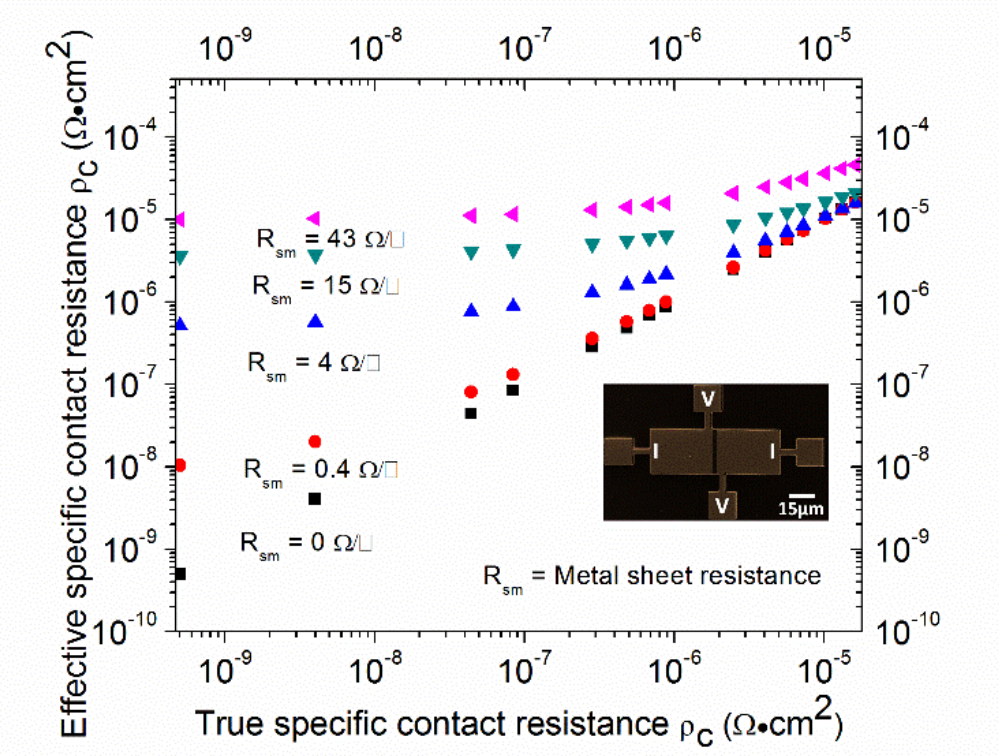


Figure 4-10 Effective specific contact resistance as a function of the true specific contact resistance for various values of metal sheet resistance. The inset shows a micrograph of the test structure used in this work.

4.4 Summary

We have studied the resistance of Ni-based contacts to heavily doped n-InGaAs, including epilayers with thin InP caps. The resistance of the contacts depended on the annealing conditions. After rapid thermal annealing at 350 °C for 60 s, a uniform $Ni_xInGaAs$ layer formed (beneath Ni_xInP when InP-capped epilayers were used), and low ρ_c values of $4.0 \times 10^{-8} \pm 7 \times 10^{-9}\ \Omega\cdot cm^2$ and $4.6 \times 10^{-8} \pm 9 \times 10^{-9}\ \Omega\cdot cm^2$ were achieved on InGaAs capped with 10 nm of InP and uncapped InGaAs, respectively. Similar samples subjected to an additional $(NH_4)_2S$ surface treatment before

metallization exhibited an as-deposited ρ_c about an order magnitude lower than that of the untreated case. In these samples, the specific contact resistance remained low, near $2 \times 10^{-8}\ \Omega \cdot cm^2$, after annealing at 350 °C for 60 s.

When contacts were prepared without the $(NH_4)_2S$ pre-metallization surface treatment, a native oxide appeared between Ni and the semiconductor. Nickel diffused through this oxide upon annealing at 350 °C, forming an oxide-free Ni_xInGaAs contact to n-InGaAs and reducing the specific contact resistance. Since the n-InGaAs was heavily doped ($N_D = 3 \times 10^{19}\ cm^{-3}$), the dominant current transport mechanism was tunneling through the Schottky barrier, and removing the interfacial oxide eliminated an additional resistance in series with the barrier. For $(NH_4)_2S$-treated samples, the interfacial oxide was eliminated, and even the as-deposited contacts exhibited low resistance due to formation of an oxide-free, intimate contact.

To avoid overestimation of ρ_c that may have occurred in other studies, we applied a Ti/Pt/Au cap on the Ni_xInGaAs and using a refined TLM test structure. With a further minor reduction in specific contact resistance, possibly by using more heavily doped epilayers, Ni_xInGaAs contacts should meet the needs of aggressively scaled self-aligned field-effect transistors with InGaAs channels.

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4.6 Appendix

4.6.1 Device schematic

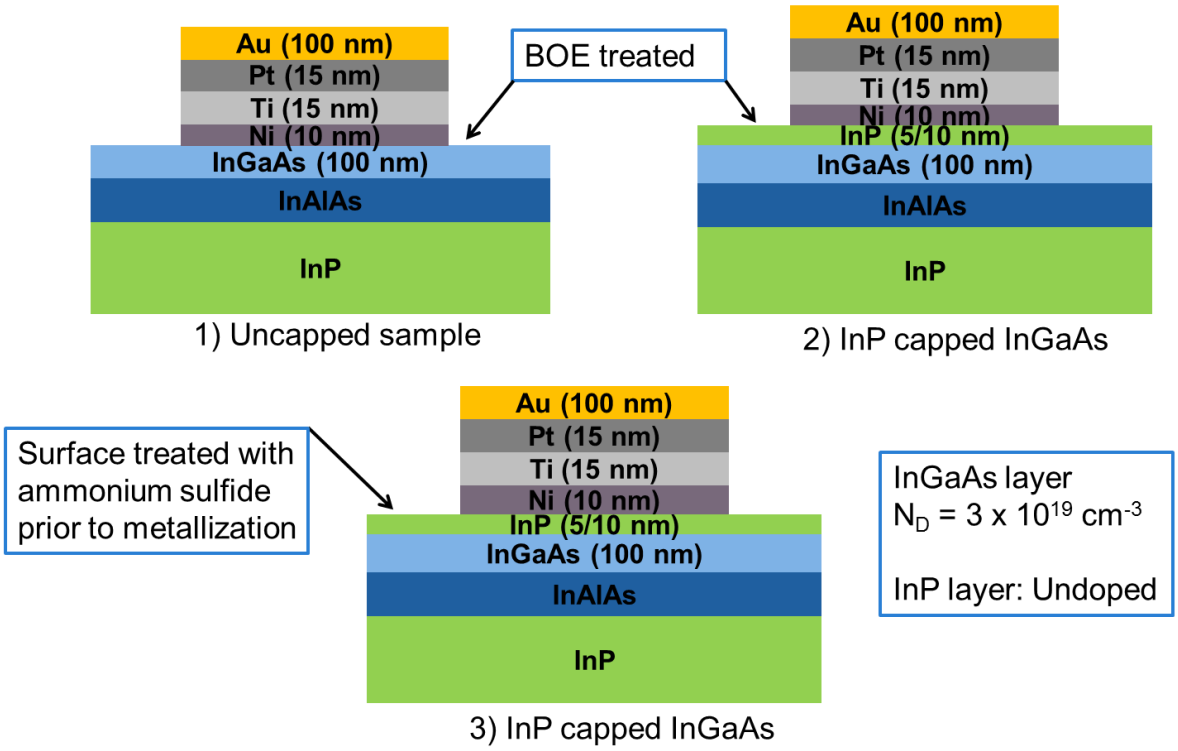


Figure 4-11 Device schematic showing cross-sectional views of metal stacks on InP-capped and uncapped InGaAs samples subjected to various surface treatments.

4.6.2 Auger electron spectroscopy depth profile for an as-deposited Ni contact

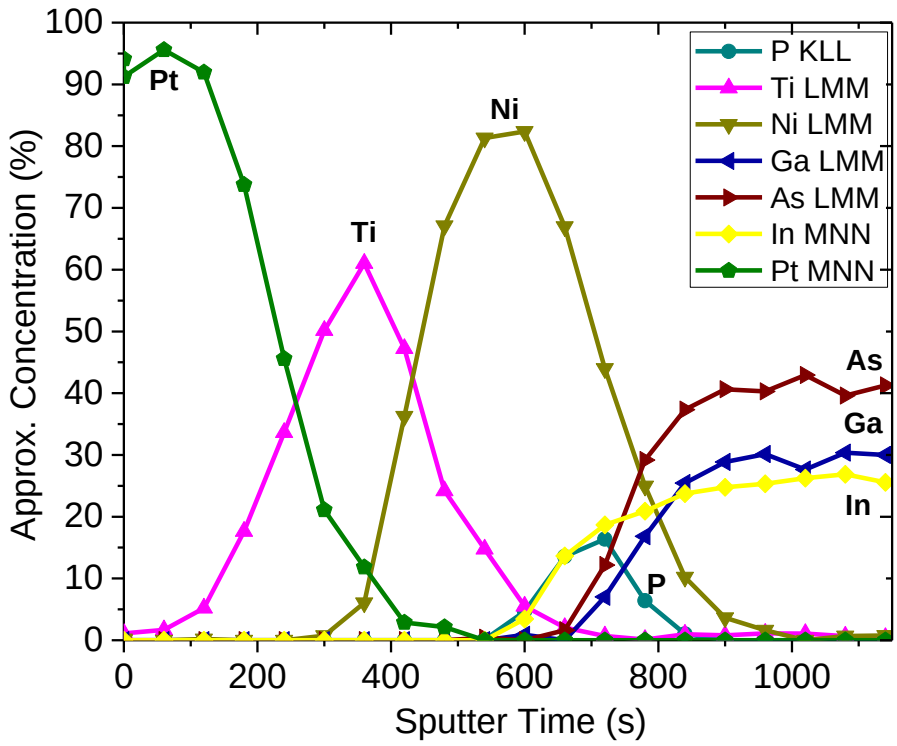


Figure 4-12 Auger depth profile for an as-deposited Au(100 nm)/Pt(15 nm)/Ti(15 nm)/Ni(10 nm) contact on 10-nm InP-capped InGaAs.

Chapter 5

Alloyed Ag contacts to few-layer MoS_2 Field-Effect Transistors

5.1 Introduction

Among layered two-dimensional (2D) transition metal dichalcogenides (TMDs), molybdenum disulphide (MoS_2) is currently at the forefront of promising materials for future nanoelectronic and optoelectronic applications.[1,2,3] MoS_2 is a semiconductor with tuneable band gap[4]. Even in its few-layered form, MoS_2 flakes can exhibit low surface roughness with few dangling bonds[5] and excellent environmental stability. Accordingly, MoS_2 FETs have been shown to exhibit high electron mobilities (>200 $cm^2/V\ s$).[6] Owing to the relatively large band gap and large effective mass of MoS_2, along with its two dimensional ultra-thin body[7], it is deemed attractive for low power, aggressively scaled logic devices.[8] MoS_2 in its single and few layer form is also mechanically flexible[9] and optically transparent, making it a potential candidate for flexible electronic applications.[10,11] Despite all these advantages, device operation and performance have been chronically limited by high contact resistance (R_c). For example, high source and drain contact resistance in MoS_2 based field effect transistors (FETs) degrades the field-effect mobility and the on/off current ratio, and it can severely limit the on-state current in these devices.[6,12] The impact of contact resistance is further amplified as device dimensions are scaled down.[13] Hence, Ohmic contacts with low resistance and well-controlled morphologies are necessary if MoS_2 is to be viable for future nanoscale electronics.

To date, there have been several approaches studied to lower the contact resistance mainly focusing on three fronts: work function engineering[6], molecular doping[14,15] and phase engineered contacts.[16] Various metals with different work functions have been used as contacts to MoS_2, including Sc[6], Ti[6], Ni[12,17,18], Au[12,13] and Pd[17]. Low work function metals such as Sc formed contacts with lower barrier heights, leading to higher current injection and lower contact resistances,[6] albeit with high susceptibility to oxidation,[19] which poses device processing and reliability challenges. However, only a weak correlation between the work function of the contact metal and the measured effective Schottky barrier height has been observed, indicating the presence of Fermi level pinning close to the conduction band of MoS_2.[6] This pinning limits the degree one can lower the contact resistance using work function engineering alone.

A second approach used to lower the contact resistance is by doping. Promising results have been achieved using n-type charge transfer dopants such as polyethylenimine (PEI) and chlorine doping.[14,20] However, such doping mechanisms have been applied only to an entire flake rather than just the source and drain regions. As a result, the channel of the MoS_2 FETs was modified, yielding devices with relatively poor on/off ratio.

An interesting alternative has been phase engineered contacts.[16] This scheme involves local and patterned conversion of the semiconducting 2H phase into the metallic 1T phase. Using this scheme, R_c as low as 0.2 kΩ μm were achieved. However, preparing the 1T phase involve the use of lithiation (n-butyl lithium) in a glove box, which could be cumbersome or incompatible with conventional device fabrication processes. In addition, the stability of phase engineered contacts at high device processing temperatures (>100°C) is unknown. This point is important because Ohmic contact degradation due to poor thermal stability is a common reliability issues for devices.

Hence, engineering contacts to MoS_2 that can withstand post contact-formation processing and packaging steps at elevated temperatures remains a key requirement.

In this report, we present both electrical and transmission electron microscopy results for alloyed Ag contacts to unintentionally doped few-layer (FL)-MoS_2. We report improved R_c with annealing in the range of 0.2–0.5 kΩ μm (evaluated at constant sheet resistance, R_{sh}, of 32 kΩ/□) for MoS_2 that is 5 to 14 layers or ~3 to 9 nm thick. The contact resistances were extracted using the transfer length method (TLM). Annealing was found to be critical for achieving low contact resistances. TEM study conducted on a cross-section of an annealed device showed interdiffusion at the Ag/MoS_2 interface. No evidence of interfacial oxide was found indicating an intimate contact between Ag and MoS_2. In addition, Ag was detected in the MoS_2 flake under the contacts, indicating possible incorporation of Ag into the MoS_2 matrix. As a result, it is speculated that Ag inside the MoS_2 make good electrical contact to all the individual MoS_2 layers helping reduce the contact resistance at the Ag/MoS_2 interface.

5.2 Experimental methods

5.2.1 Sample preparation and device fabrication

Highly doped (>10^{19} cm^{-3}) p-type Si wafers with a 50 nm dry thermal oxide were used. We chose a 50 nm thickness because it provided good contrast for easy optical identification of the number of layers of the MoS_2 flakes and it led to reasonable electrostatic control of the channel of our MoS_2-based devices when the SiO_2/Si substrate was used as a global back gate. The substrate wafer was then patterned with Ti(20nm)/Au(50nm) alignment markers. These markers were used to locate the exfoliated flakes. The wafer was then diced into 1cm x 1cm pieces. Each piece was degreased in acetone, isopropyl alcohol (IPA) and deionized (DI) water for 5 minutes under

sonication followed by a 5-minute bake at 125°C on a hotplate. Finally, all samples were placed in ultraviolet (UV) ozone (in flowing dry 80% N_2/20% O_2 gas) for 10 minutes. The latter two steps were used to remove adsorbed water and other species introduced during previous processing steps, and they enhanced the adhesion between the exfoliated flakes and the substrate. Once the substrate was cleaned, MoS_2 flakes purchased from 2D Semiconductors, Inc., were exfoliated onto the substrate. Each sample with exfoliated flakes was placed in acetone for 24 hours to clean tape residues. The effectiveness of acetone was further confirmed using Auger electron spectroscopy (AES) surface analysis, which showed reduced carbon contamination compared to samples without acetone cleaning. Optical contrast between the flakes and the SiO_2/Si substrate was used as a primary method to establish their layer thickness. However, atomic force microscopy (AFM), was later used to confirm the layer thickness after electrical characterization. For selected samples, cross-sectional TEM was used as an additional technique to confirm the thickness of the MoS_2.

After exfoliation and cleaning of the MoS_2 flakes, TLM test structures with varying channel lengths were patterned using e-beam lithography. Each flake had at least four devices with different channel lengths. We used double layer poly methyl methacrylate (PMMA 495 A6) from MicroChem followed by PMMA (950 A3) as e-beam resist because it can be developed using only 1 DI water: 5 IPA based developer.[21,22] This left less resist residue compared to the conventional methyl isobutyl ketone (MIBK):IPA based developers. The gap between the contacts was varied from 0.1–2.5 µm. No post-lithography surface preparation was used. Ag (140nm) was deposited using e-beam evaporation at a rate of <0.5 Å/s and at a base pressure < 5 x 10^{-7} Torr.

Originally, only 50 nm Ag was used; however, after annealing, the Ag film on the SiO_2 surface started to agglomerate forming small voids and hillocks. Previous studies have indicated poor adhesion of Ag to SiO_2.[23] Furthermore, Ag is also shown to form islands instead of a continuous

film on MoS_2 if Ag is too thin.[24] Hence, thicker (140 nm) Ag film was required to avoid the agglomeration of the metal. An additional 10 nm of SiO_2 was deposited on top of the Ag to protect the metal film from sulfidizing and agglomerating during annealing. The metal was then lifted-off in an acetone bath (at room temperature) overnight. A long lift-off time was needed to achieve clean devices with minimal resist residues and to limit line edge roughness upon lift-off. All samples were then vacuum annealed at 150°C for 24 hours inside a high vacuum (HV) system with base pressure on the order of 2–4 x 10^{-6} Torr. Vacuum annealing was mainly used to remove water adsorbates from the MoS_2/SiO_2 interface and to improve device stability.[13] Additional annealing was done in an AG610 rapid thermal annealing furnace in gettered ultra-high purity (UHP) Ar environment at temperatures ranging from 200°C–500°C. Electrical measurements were done on all samples before each annealing step. Finally, after completing all electrical measurements, the channel width and length were measured using a scanning electron microscope (SEM).

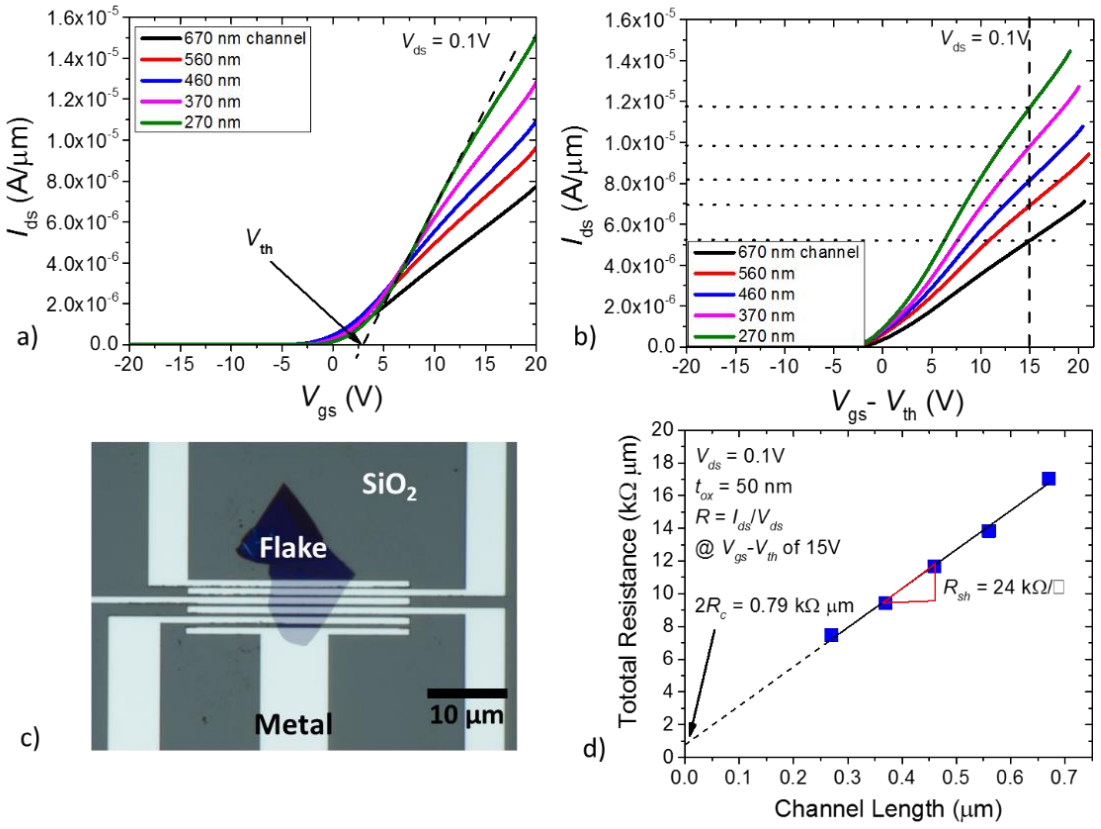


Figure 5-1 Extraction of contact resistance. (a) Linear extrapolation method used to extract threshold voltage, (b) I_{ds} vs. V_{gs}-V_{th} plot as a function of channel length, (c) optical image of TLM structure on MoS_2. Note, to better illustrate the shape of the flake, the image in (c) consists of two overlaid images of the flake before (top-transparent) and after (bottom) test structure fabrication. (d) Normalized resistance vs. channel length plot used to extract $2R_c$ (y-intercept) and the R_{sh} (slope) for a typical annealed sample (first annealed in vacuum followed by an RTA anneal at 250°C for 300 s).

5.2.2 Electrical characterization

Back-gated TLM measurements involve the characterization of a set of transistors with varying channel lengths. After fabricating our contacts, we measured the drain current (I_{ds}) *vs*. gate voltage (V_{gs}) at a constant drain voltage (V_{ds}) of 100 mV for each device. The I_{ds} vs. V_{gs} (transfer characteristic) curves were then used to extract the threshold voltages (V_{th}) using the linear extrapolation method[25] (**Figure 5-1**a) for each device with different channel length. For devices

characterized in air under standard atmospheric conditions, the transfer characteristics exhibited significant hysteresis, in the range of 5-10 V. In addition, we also observed device to device threshold variations in the range of 0-3V. To decrease the observed hysteresis pulsed voltage measurements were conducted in a Lake Shore Vacuum probe station for selected set of samples. A Keithely 4200-SCS was used for all pulsed measurements where the gate voltage pulse ON time was held constant at 5 ms with a constant OFF time of 500 ms. Unfortunately, the standalone Keithely 4200-SCS without the add-on pulsed measuring unit (PMU) did not allow us to set the pulse rise/fall time and the lowest possible pulse ON time was 5 ms. Despite this limitation, devices characterized with pulsed gate voltage under vacuum exhibited minimal hysteresis (see **Figure 5-2**). However, device to device threshold variations were still persistent.

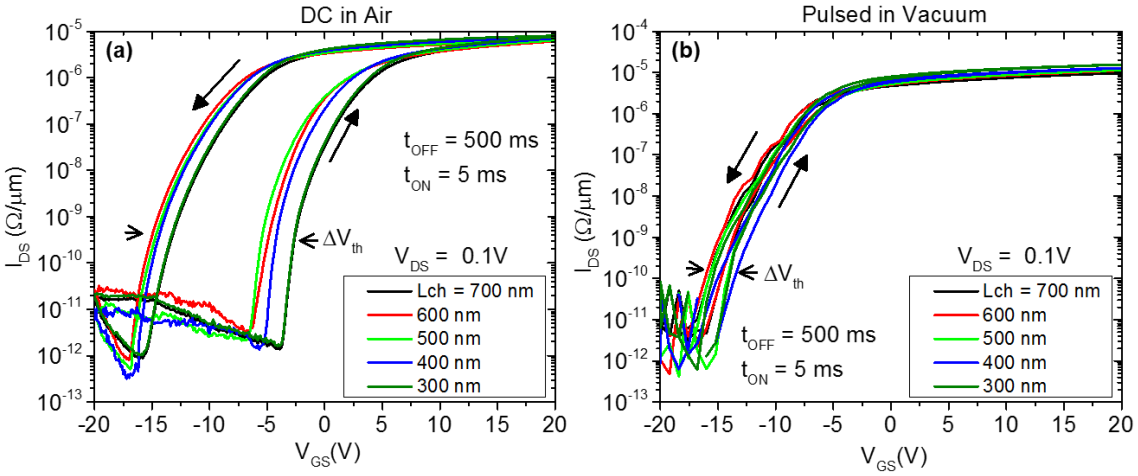


Figure 5-2 The effect of pulsed voltage measurement on the experimental transfer characteristics of back-gated MoS_2 FETs with varying channel length fabricated on the same flakes. (a) DC measurement in air at room temperature. (b) Pulsed gate voltage measurement (OFF time of 500 ms and ON time 5 ms) in vacuum at room temperature.

We then calculated the total resistance ($R = V_{ds}/I_{ds}$) from plots of I_{ds} *vs.* V_{gs}-V_{th} (the gate overdrive voltage). V_{ds} was held constant at 100 mV while I_{ds} was extracted from the plot at a

single value of V_{gs}-V_{th} for each device (**Figure 5-1**b). These data were used to extract contact resistance and semiconductor sheet resistance for each V_{gs}-V_{th}. However, we needed to account for slightly varying widths of the flakes (**Figure 5-1**c). Therefore, we plotted RW vs. L_{ch}, where R is the measured resistance, W is the width of the flake, and L_{ch} is the channel length (or the gap between the contacts)—instead of the more common approach of fitting a straight line to R vs. L_{ch} with W treated as a constant. This approach is shown in **Figure 5-1**d and can be used for uniform MoS_2 crystals with the same number of layers along the whole length of the flake.

It is important to note here that when the contact resistance is a small fraction of the total resistance, significant error can arise in extrapolation of the R_c from the y-intercept of the plot of RW vs L_{ch} (**Figure 5-1**d). Simple linear regression technique can be used to calculate y-intercept standard error. Typical standard error for R_c range from ± 0.2 kΩ-μm to ± 0.4 kΩ-μm. This is particularly true for TLM test structure with only few channels and large L_{ch}, because the total resistance is dominated by the channel resistance. It has been shown the error can be reduced by using multiple channels (>6) with L_{ch} down to 100 nm and by etching the flakes to consistent width.[13] An attempted was made to make such samples by dry etching the MoS_2 flakes right after exfoliation using BCl_3/Ar gas mixture then depositing Ag on the etched flake. However, the underlying SiO_2 layer was also etched leaving relatively thin gate oxide. After annealing the sample in RTA, the oxide became leaky possibly due to Ag diffusion into the etched oxide layer contacting the Si substrate, thereby shorting the Ag electrodes. Hence, in the case of devices with etched MoS_2 flakes reliable electrical data was extracted for only the as-deposited samples.

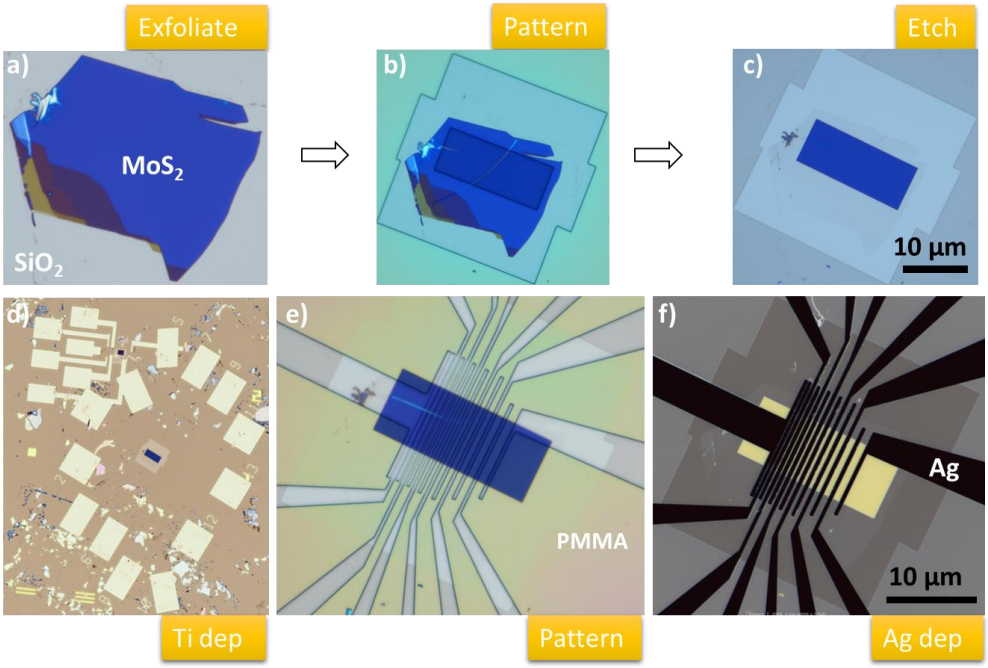


Figure 5-3 (a-f) Optical images showing the contact preparation steps for a TLM test structure fabricated on an etched uniform MoS_2 flake with Ti contact pad and Ag source and drain contact metal.

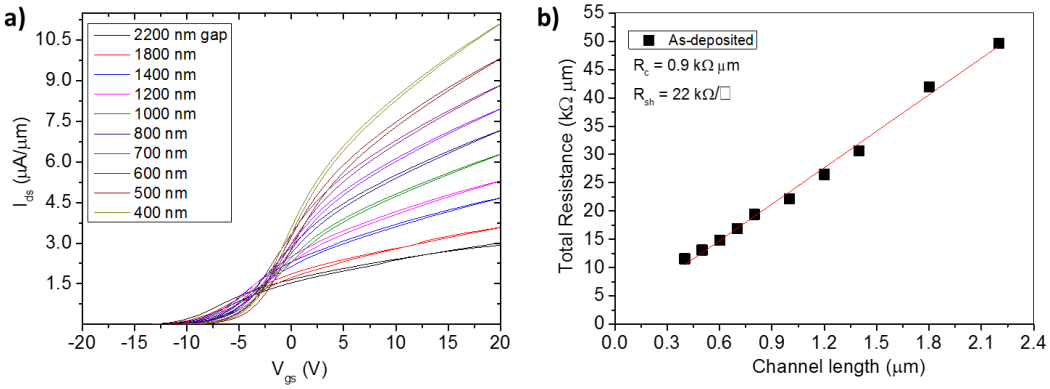


Figure 5-4 (a) Linear I_{ds} vs. V_{gs} characteristics for 10 devices shown on **Figure 5-3** and (b) the corresponding total resistance vs. channel length plot used to extract the contact resistance for the as-deposited Ag contact to MoS_2.

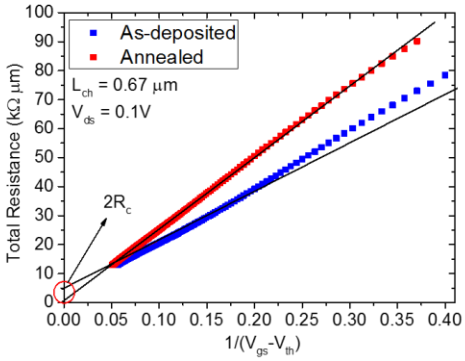
As a complement to TLM, an alternative approach known as Terada Muta's[26,27] (T&M) method was used to extract the contact resistance of Ag contacts to MoS_2. The T&M method, similar to TLM, relies on the total R derived from drain current equation in the linear region of the

output characteristics at low V_{DS} =0.1V. However, unlike TLM, T&M method requires only a single device to extract the contact resistance from the R vs. $1/(V_{gs} - V_{th})$ curve where again the y-intercept corresponds to $2R_c$ (see Figure 5.5a). Here, a constant range of (V_{gs} - V_{th}) of 7 to 15V were chosen to reliably compare R_c values across multiple samples.

$$I_{ds} = \mu_{\mathrm{FE}} C_{ox} \frac{W}{L} (V_{gs} - V_{th}) V_{ds}$$

$$R_{ON} = \frac{V_{ds}}{I_{ds}} = 2R_c + \frac{L_{ch} R_{sh}}{W} = R_{SD} + \frac{L_{eff}}{\mu_{eff} C_{ox} W (V_{gs} - V_t)}$$

T&M method assumes that R_c is independent of the gate overdrive voltage or gate bias. This assumption holds true in the case of the annealed contacts where Ag diffuses into MoS_2 changing the semiconductor under the contact. As a result, R_c remained independent of the overdrive voltage for V_{gs} - V_{th} = 7 to 15V (see Figure 5.7). However, the assumption is not fully applicable for as-deposited contacts possibly due to the limited Ag diffusion into MoS_2. Therefore, the T&M method can only be trusted for annealed contacts and the results were compared to those achieved by TLM method. Both methods led to comparable low R_c values for annealed contacts (see Figure 5.5b).



(a)

As-deposited	T&M (different gaps)					
Gap spacings (µm)	0.67	0.56	0.46	0.37	0.27	
Threshold voltage (V)	2.2	2	2.5	3.4	3.4	
Rc_T&M (kΩ µm) (7-15V)	1.9	1.3	1.5	1.3	1	
Rc_T&M Average (kΩ µm)						1.4
Rc_T&M Stdv (kΩ µm)						0.3
Rc_TLM (kΩ µm) @ 15V						0.9

Annealed	T&M (different gaps)					
Gap spacings (µm)	0.67	0.56	0.46	0.37	0.27	
Threshold voltage (V)	0.3	0	0.7	1.7	3	
Rc_T&M (kΩ µm) (7-15V)	0.3	0.2	0.5	0.5	0.5	
Rc_T&M Average (kΩ µm)						0.4
Rc_T&M Stdv (kΩ µm)						0.1
Rc_TLM (kΩ µm) @ 15V						0.4

(b)

Figure 5-5 Terada Muta's method used for the extraction of R_c. (a) Total resistance as a function of $1/(V_{gs} - V_{th})$ for the MoS_2 device annealed at 250°C for 300 s in a RTA furnace (device with channel length of 0.67 µm). (b) Table comparing R_c values extracted using T&M and TLM methods respectively for both as-deposited and annealed contacts.

The subthreshold slope ($SS = \frac{dV_{gs}}{d(\log(I_{ds}))}$) and the ratio of the on current to the off current were extracted from the I_{ds} vs. V_{gs} characteristics. Transconductance (g_m) at V_{ds} = 100mV was evaluated by taking the maximum slope of the linear I_{ds} vs. V_{gs} plot. Accordingly, the effective field effect mobility (μ_{FE}) was calculated using the equation $\mu_{FE} = \frac{L_{ch} g_m}{W C_{ox} V_{ds}}$, where L_{ch} is the channel length, W channel width, C_{ox} is the gate capacitance. In this calculation, it is assumed that the voltage drop across the channel is equal to V_{ds}. The method does not take in account the effect of contact resistance. In addition to the transfer characteristics, we measured the output characteristics (I_{ds} *vs.* V_{ds}) of our device at different V_{gs}. From the output characteristics, the maximum ON current at given V_{ds} and V_{gs} values was established.

Figure 5-6a shows a schematic of a backgated MoS_2 FET with Ag as a source and drain metal. Electrical characterization was performed on multiple of these MoS_2 FETs with varying channel lengths fabricated on a single MoS_2 flake as shown in **Figure 5-1**c in order to measure contact resistance. All electrical characterization was performed at room temperature under ambient conditions using a Keithley SCS 4200 semiconductor parameter analyzer and a Cascade shielded probe station. **Figure 5-1**b shows the total resistance normalized by the width of the channel (RW vs. L_{ch} plot) generated for a uniform 8 layer MoS_2 flake where the contact resistance ($2R_c$) is extracted from the intercept. R_c depends on multiple parameters such as contact metal, annealing condition, gate overdrive voltage and number of MoS_2 layers. Therefore, to directly and more reliably compare contacts before and after annealing, RW vs. L_{ch} plots were generated at a constant gate overdrive voltage of 15V and at a constant MoS_2 sheet resistance of 32 kΩ μm. This method allowed us to compare the R_c values reported in this work to those in the literature more reliably.

5.3 Results

5.3.1 The role of annealing on contact resistance

As-deposited contacts exhibited R_c ranging from 0.8–3.5 kΩ-µm without extra surface preparation (**Figure 5-6**c and **Figure 5-6**d). These results were already low compared to as-deposited contact resistances achieved using other metals such as Ti or Ni reported in the literature.[12,17,18,28] With annealing Ag on 5 to 14 layer MoS_2 flakes, R_c in the range of 0.2–0.5 kΩ µm was achieved, which is on par with R_c values reported for the state-of-the-art 1T phase-engineered contacts.[16] Our lowest R_c values were achieved for contacts annealed in vacuum first at 150°C for 24h followed by annealing at 250°C to 300°C for 300 s in a RTA furnace. In **Figure 5-6**c and **Figure 5-6**d, the contact resistance vs annealing temperature is plotted for both at constant channel sheet resistance of 32 kΩ/□ and constant gate overdrive voltage of 15V, which corresponds to a charge carrier density of ~6.5×10^{12} cm^{-2}. The carrier density n is calculated as $n = (V_{gs}-V_{th})C_{ox}/q$ where the gate capacitance $C_{ox} = \varepsilon_{ox}/t_{ox}$ and the elementary charge q = 1.6 x 10^{-19} C. For the 50 nm gate oxide used in this work $C_{ox} = \varepsilon_{ox}/t_{ox}$ = 69 x 10^{-4} nF/cm^2. In both cases, RTA annealed contacts exhibited contact resistance on average 3 to 5 times smaller compared to the as-deposited contacts. These results were also confirmed using Terada Muta's method[26,27] (see **Figure 5-5**). Based on a recent review paper comparing measured contact resistances at similar sheet resistances for ranges of TMDs, the values reported for the RTA annealed Ag contacts are among the lowest contact resistance values (ranging from 0.2–1 kΩ-µm, see Appendix 5.7.2, **Figure 5-21**).[13,29]

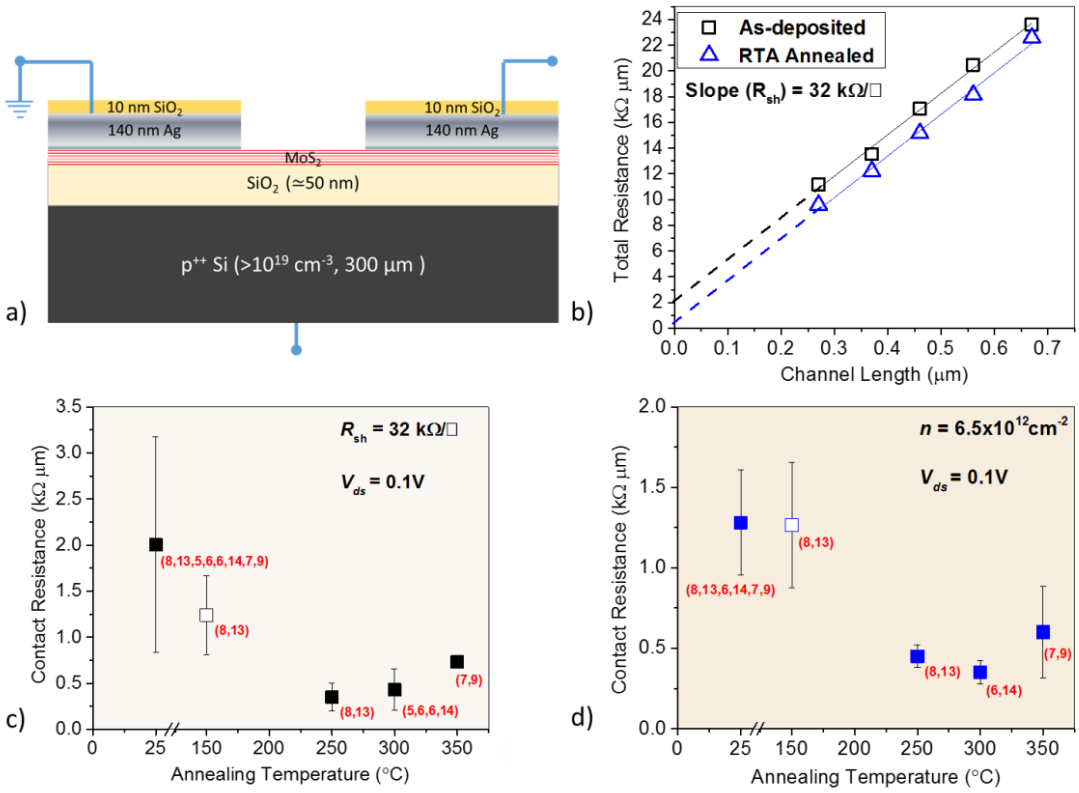


Figure 5-6 (a) Schematic of MoS_2 device with Ag contacts. (b) Normalized total resistance (*RW*) vs channel length (L_{ch}) measured by TLM. Contact resistance as a function of annealing temperature for multiple devices evaluated at the same (c) channel sheet resistance (R_{sh}) of 32 kΩ/□ and same (d) gate overdrive voltage of 15 V. The numbers in () represent # of layers for each MoS_2 device. Each device was first annealed in vacuum at 150°C for 24h followed by RTA annealing step at different annealing temperatures. The RTA annealing time is held constant at 300 s. Contact resistance measurement were conducted after each annealing step. Error bars represent the standard deviation of contact resistance due to sample-to-sample variation.

Figure 5-7 shows the extracted contact resistance as a function of carrier density for Ag contacts annealed to 300°C on an 8 layer MoS_2 flake compared to other contacts in the literature.[13] Overall, annealed Ag contacts reported in this work exhibited relatively low contact resistance values for wide ranges of carrier densities. One additional feature worth noting on **Figure 5-7** is that the contact resistance of the annealed Ag contacts showed weaker dependence on gate overdrive voltage compared to other contacts in the literature. This may indicate a heavily doped

contact region that is weakly affected by the gate. In this case the sheet resistance under the contact is also different than the sheet resistance between the contacts. Therefore, we do not extract a specific contact resistance nor the transfer length, as accurate extraction of this parameters using TLM requires the sheet resistance under and between the contacts to be the same.

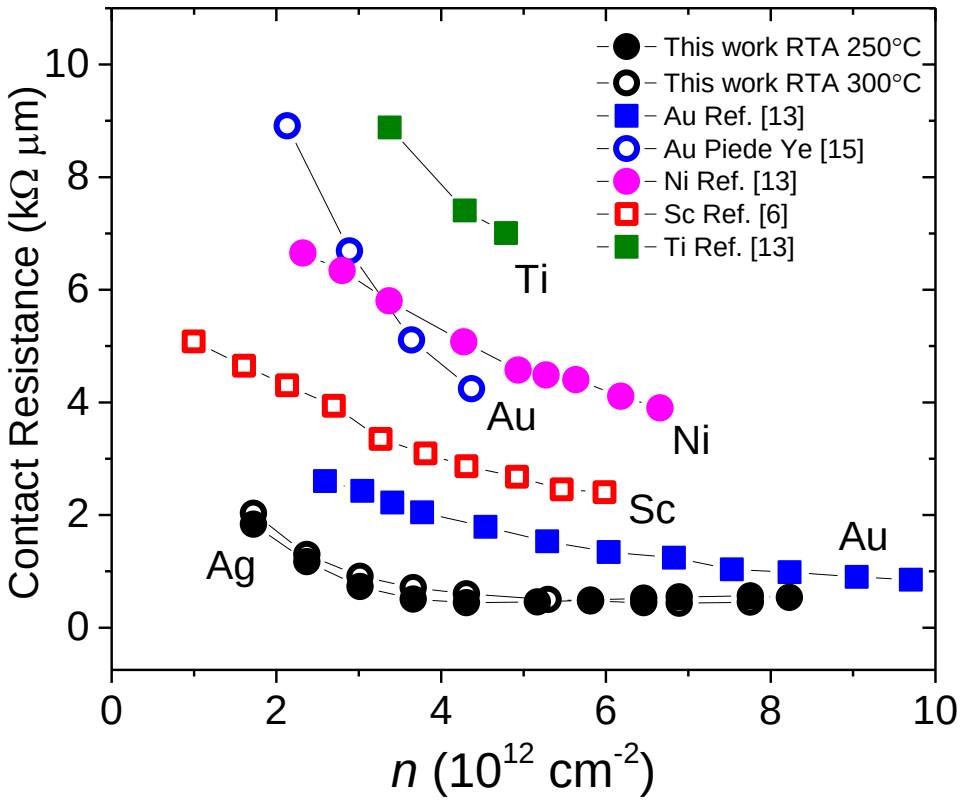


Figure 5-7 Extracted effective contact resistance as a function of charge carrier density calculated at different gate overdrive voltages in several studies on MoS_2. This plot is adopted from work by English *et al.*[13]

Figure 5-8a and **Figure 5-8**b show the transfer and output characteristics, respectively, for the same 8 layer MoS_2 FET on the 50 nm SiO_2/Si substrate discussed above with channel length of 670 nm. All devices with Ag contacts discussed above were tested by sweeping the gate voltages from 20 V to -20 V, and all exhibited n-type FET characteristics in agreement with previous observations.[30] The transfer characteristics (**Figure 5-8**a) showed an on/off ratio ~10^7 for the

device with both as-deposited and annealed contacts. Meanwhile, a subthreshold slope of 1206 mV/dec (averaged over 4 orders of magnitude in current) was extracted for devices with as-deposited contacts. The SS became steeper (500 mV/dec) with annealing. The overall ON current decreased after annealing; however, better saturation characteristics were observed for annealed contacts. An ON current of I_{ds} = 186 µA/µm was achieved after annealing for a carrier density of ~8.5×10^{12} cm^{-2} at V_{ds} of 5V. The field effect mobility also slightly decreased from 53 cm^2/(V-s) to 46 cm^2/(V-s) with annealing. These device characteristics still compare favorably with those reported in the literature (see Supporting Information, **Table 5-1**). [6,13,16,29]

Please note that the contact resistance of Ag/MoS_2 contacts investigated in this work increased with MoS_2 flakes thickness for flakes more than 15 layers thick (see **Figure 5-22**a, b). This is because the back gating mostly affected the bottom-most layers in contact with the SiO_2 layer, while the top most layers were weakly affected by the gate due to charge screening. Therefore, poor gating resulted in less electrostatic doping, which led to less tunneling current and higher contact resistance. In addition, the extracted room temperature field-effect mobility values were found to vary with flake thickness in a nonmonotonic fashion (see **Figure 5-22**c) as previously reported by Das *et al*.[6,31]

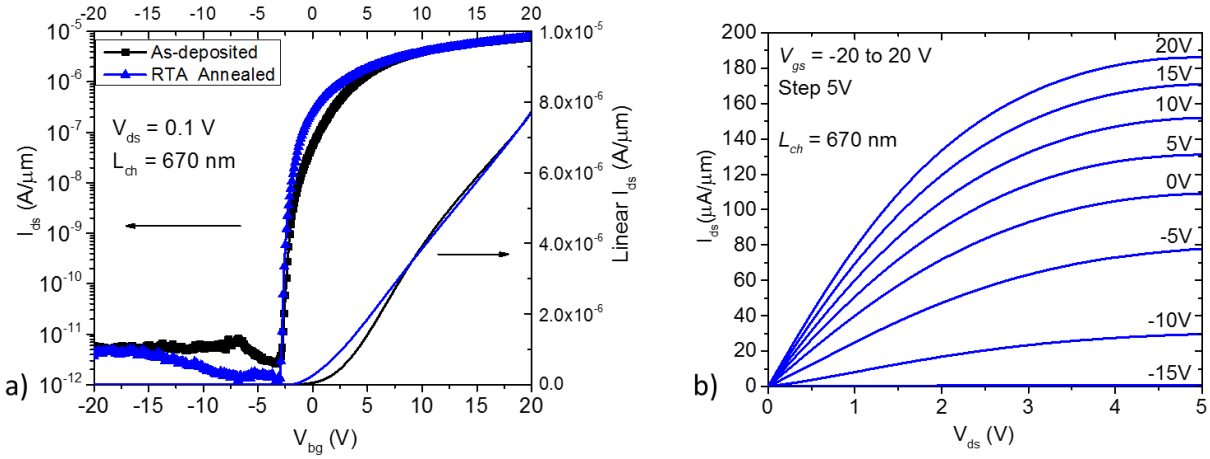


Figure 5-8 (a) Transfer and (b) output characteristic curves for an 8 layer MoS_2 FET with 670 nm channel length after annealing at 250°C for 300 s. The I_{ds} vs. V_{gs} is presented both in semilog and linear scale. The maximum ON current achieved for this device was 186 µA/µm at V_{ds} of 5V and back gate bias of 20V.

5.3.2 TEM characterization of annealed Ag contacts

To further understand the improvement of device characteristics and contact resistance with annealing, cross-sectional high resolution TEM and scanning TEM (STEM) were performed on a FEI Titan G2 aberration corrected microscope at 80kV and 300kV. High resolution Z-contrast imaging of the Ag/MoS_2 contacts were collected using high-angle annular dark-field (HAADF) to study the interface. Electron energy loss spectroscopy (EELS) was also performed to determine localized chemical composition of the Ag/MoS_2 interface and to establish the extent of the reaction.

Figure 5-9 shows high magnification HAADF STEM image and a corresponding EELS elemental map collected near the Ag/MoS_2 interface for a device annealed at 300°C for 300 s (see Appendix 5.7.1, **Figure 5-16**). The sample is oriented along a (211) zone axis of the Ag film. Several spectrum images were recorded at 300kV accelerating voltage. The high loss edges Ag

L2,3 (3360eV), S K (2460eV) and Mo L2,3 (2520eV) were used to calculate EELS elemental maps and line profiles while mitigating the effects of peak overlaps. Elemental maps were calculated for the area shown in the HAADF image using a power law for background extrapolation. **Figure 5-17**b (see Appendix 5.7.1) shows background subtracted spectra of all EELS transitions used for elemental mapping. It is important to note here that EELS measurements were conducted by passing a 300 kV electron beam (sub 0.5 nm probe diameter) through a thin cross-section of the sample. The cross-section was prepared using focused ion beam (FIB, FEI Helios Nanolab 660) to be thick enough that the surface produces a negligible fraction of the transmitted signal, at the same time the cross-section was thin enough (below 30 nm, that is $t/\lambda < 0.5$) to minimize the effect of multiple scattering.[32] This led to a more accurate high-resolution EELS chemical analysis.

HAADF image in **Figure 5-9**a shows that a uniform and epitaxial Ag film was formed with intimate contact to MoS_2. **Figure 5-9**b shows EELS elemental maps near the Ag/MoS_2 interface and **Figure 5-9**c shows the corresponding line-scans across the interface calculated from the elemental maps. The width of the line scans is about 1nm. The line scans show that Mo layers in the MoS_2 and the Ag (111) lattice planes are atomically resolved. The Ag layer at the interface (left blue dotted line) has a count-rate of approximately 60% compared to the Ag layers away from the interface. This indicates that the Ag layer at the Ag/MoS_2 interface is only partially occupied by Ag atoms, but the intermixing at the interface is limited to a single atomic layer (see **Figure 5-9**a and **Figure 5-19**a). Unlike low work function metals such as Sc, Ti, and Cr that easily oxidize upon deposition or annealing,[19] oxygen was not detected in the Ag film or at the metal/semiconductor interface.

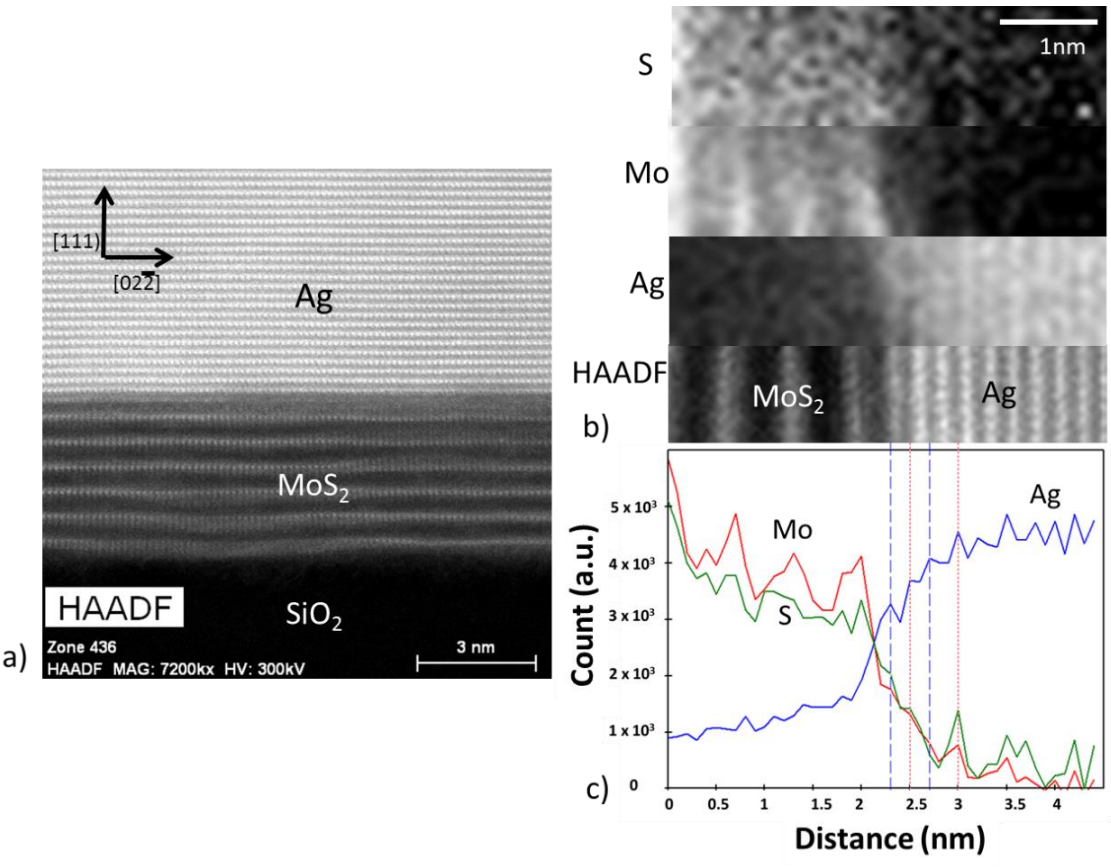


Figure 5-9 (a) High magnification STEM-HAADF image at 300 kV and b) a corresponding EELS elemental map collected near Ag/MoS_2 interface for a sample that was annealed at 300°C for 300 s. The S-K elemental intensity (counts) is multiplied 2.5X the original intensity. (c) EELS line scan acquired along a linear trajectory going from the MoS_2 layer toward the Ag contact layer as presented in (b). The dotted lines are meant to be visual guides.

In **Figure 5-9**c it is important to note that the S signal is noisy because the adjacent Mo L2,3 edge is at slightly higher energy and the Mo measurement is convoluted with the high-energy tail of the S-K peak (see Appendix **Figure 5-17**b). As result, the overall S-K EELS edge intensity is weak. Therefore, for a better reading the intensity has been magnified by factor of 2.5X. To double check the status of S and Mo at the Ag/MoS_2 interface, additional low loss EELS transitions at 80 kV were collected. In this case S-L peak does not overlap with Ag and Mo peaks (see **Figure 5-10**). Therefore, EELS line scans derived from elemental maps using S L2,3 (165eV), Mo M2,3

(390eV) and Ag M4,5 (367eV) at 80 kV provided additional and more reliable evidence of the extent of S and Mo diffusion into the Ag.

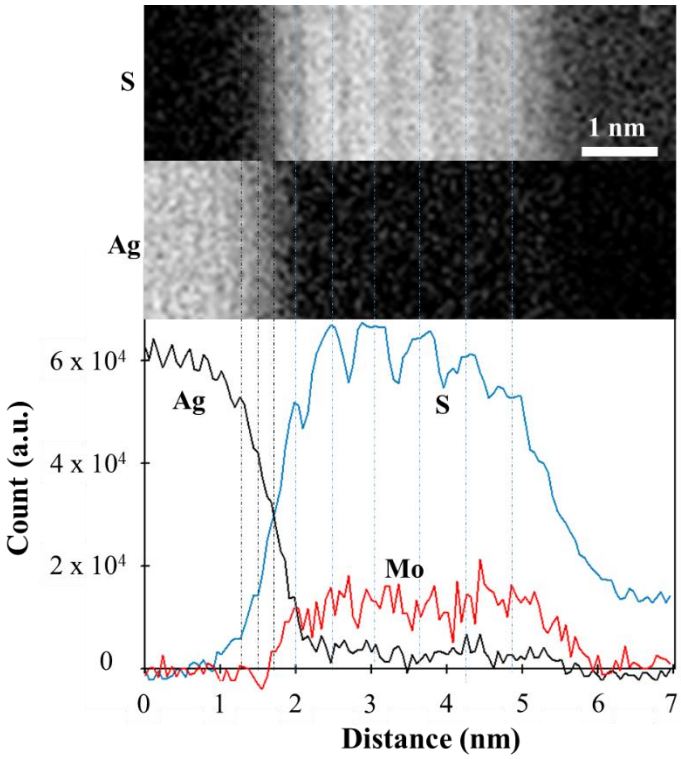


Figure 5-10 High resolution STEM-EELS elemental map for S and Ag at 80 kV and a corresponding EEL line profile across Ag/MoS_2 interface for a sample that was annealed at 300°C for 300 s. Black and blue dotted lines show Ag (111) lattice planes and MoS_2 layers respectively. The lines are meant to be visual guides.

Moreover, both at 80 kV and at 300 KV the EELS data show that Ag content does not go to zero inside the MoS_2 layer. The EELS line scan in **Figure 5-9**c and **Figure 5-10** shows that Ag diffused beyond the contact interface into the MoS_2 layers, parallel to the c-axis. Ag was detected at least 2 nm (~ 3 layers) into the MoS_2 flake. The STEM-EDX line profile collected at 80 kV across the Ag/MoS_2 also shows a small but lingering concentration of Ag inside the MoS_2 matrix supporting the EELS data (see Appendix 5.7.1 **Figure 5-18**).

To further evaluate the extent of Ag in-diffusion into MoS_2 more detailed analysis of the EELS data were conducted. In **Figure 5-11**, the inset image shows Ag EELS elemental map at the Ag/MoS_2 interface. The EEL spectra were collected at different regions of interest across the interface. Region 1 is inside the Ag film, region 2 is at the interface, while region 3 and 4 are both inside the MoS_2 flake at various distances from the interface. The dotted line along the first EELS spectra (green) shows the background extrapolated from the region before the Ag L transition. In region 1, only the Ag-L high energy-loss edge (energy window width of 392 eV) is visible with both Ag-L3 and L2 edges well defined, confirming the presence of mainly Ag in this region. On the other hand, in region 2 both S-K and Mo-L edges begin to emerge while the Ag-L edge maintained almost the same intensity indicating the presence of all three species in this interfacial region. In region 3 and 4 the definition of the Mo-L edge increased with both Mo-L3 and L2 edges clearly visible along with S-K edge. Meanwhile the intensity of Ag-L high energy-loss edge decreased, but still stayed above the background. This indicates the presence of Ag inside the MoS_2 flake even in region 4 that is at least 2 nm (~ 3 layers) away from the interface. Additional data acquired at 80 kV also show corroborating evidence of Ag in-diffusion into the MoS_2 matrix where Ag is detected across all the 6 layers (3.9 nm) of the MoS_2 flake (see **Figure 5-10**). The average spacing between the MoS_2 layers for the annealed samples were approximately 6.5 Å (see **Figure 5-12**)

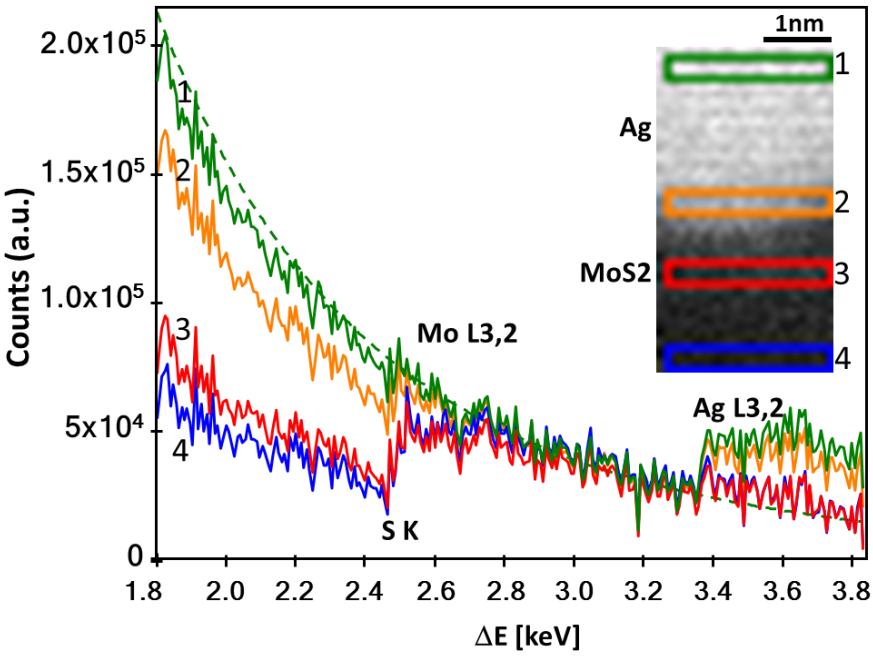


Figure 5-11 EEL spectra collected at 300 kV near Ag/MoS_2 interface for a sample that was annealed at 300°C for 300 s. The inset shows Ag-L edge elemental map. Colored boxes represent specific regions of interest where EELS data were collected.

Despite this clear evidence of Ag in-diffusion in the sample described above, not all samples analysed by TEM showed similar extent of diffusion. A sample prepared and analysed at a later date showed a more abrupt interface between Ag and MoS_2 with Ag right above the S layer at the surface. In this case, relatively less Ag in-diffusion inside the MoS_2 was observed (see Appendix 5.7.1, **Figure 5-19**). The discrepancy might be due to electric field induced Ag diffusion during electrical characterization in the first sample, as the latter sample was not characterized electrically before TEM analysis. This speculative explanation warrants further study. On the other hand, it is important to note here that the TEM sample also changed after prolonged storage (3 months). We observed some lateral diffusion of Ag into the channel region and Ag was also found at the MoS_2/SiO_2 interface. One way to explain our observation is that the TEM sample consists of a very thin (~30-50nm) membrane with a very high surface area to volume ratio. In this case,

room temperature surface diffusion of Ag during the long period of storage may be possible. In fact, we did not see similar occurrences for the latest TEM sample because it was analyzed within 10 days of preparation (using focused ion beam).

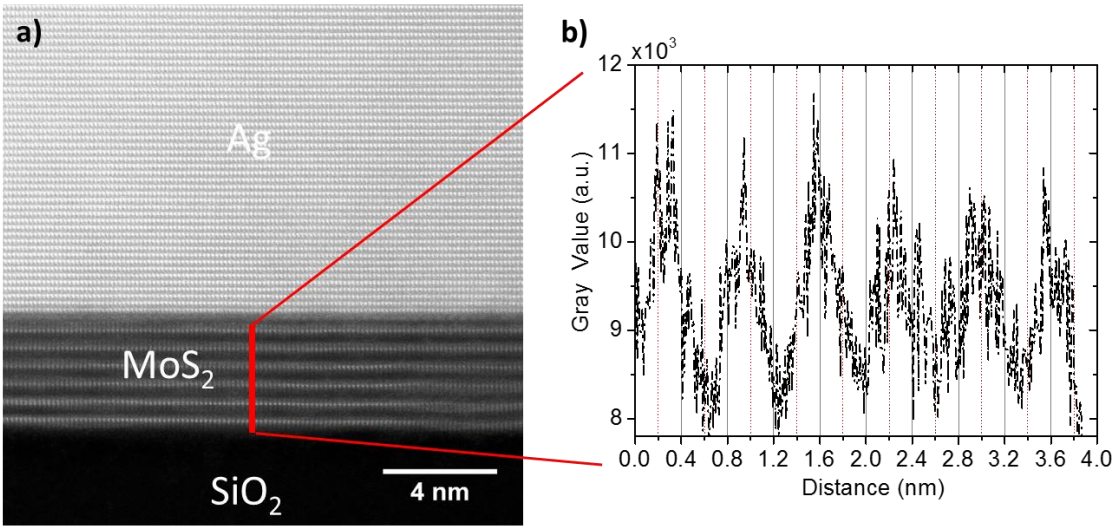


Figure 5-12 (a) High magnification STEM-HAADF image of Ag/MoS_2 contact at 300 kV for a sample that was annealed at 300°C for 300 s. (b) MoS_2 interlayer spacing profile measured using Image J.[33]

5.4 Discussion

Our findings are consistent with previous studies of annealed Ag/MoS_2 systems by Souder and Brodie.[34,35] They conducted radioactive tracer diffusion experiments to determine the effect of annealing of Ag contact to bulk (relatively thick compared to the few-layer MoS_2 crystal used in this work), natural MoS_2 crystals. By bulk, we mean flakes thicker than 10 nm. Accordingly, they reported the in-diffusion of Ag into MoS_2 layers, where the silver concentration, in the layers under the Ag contact, was found to be on the order of 10^{19} cm^{-3} for samples annealed between 400°C to 600°C for 5 minutes.[34] In this case, the resistivity perpendicular to the MoS_2 layers decreased so the current conduction across the MoS_2 crystal was more isotropic. (This was not true

for unannealed Ag/MoS_2 contacts. Because of the anisotropic nature of the MoS_2 layer structure, the resistivity of the material parallel to the c-axis was found to be up to 1200X smaller compared to the resistivity measured perpendicular to the layers. This was established theoretically and observed experimentally.[34]) As a result, they concluded that when Ag diffused into the MoS_2 crystal, it made good electrical contact between the MoS_2 layers increasing the current conduction across the layers. We believe the Ag in the alloyed contacts studied in this work played a similar role.

Additional evidence of the intercalation of Ag into MoS_2 with annealing was also reported by Li *et al.*[36] They studied Ag/MoS_x system *in-situ* using X-ray photoemission (XPS) and thermal desorption mass spectroscopy. MoS_x (which exhibited similar layered structure as MoS_2) was prepared by exposing Mo crystal to S_2 gas generated *in-situ* by the decomposition of Ag_2S in a solid state electrochemical cell.[36] Two monolayers (which corresponds to 1.43 x 10^{15} atoms/cm^2) of Ag were deposited *in-situ* onto a MoS_x film and annealed up to 327 °C. XPS spectra of the annealed sample showed negative binding-energy shifts of the S 2p and Mo $3d_{5/2}$ peaks (compared to metallic Ag peaks), which the author of the study associated with the diffusion of Ag into the MoS_x matrix forming a 'bimetal sulphide ($AgMoS_x$)'.[36] The shift in binding energy with annealing is also reported as evidence of silver to sulfur charge transfer, where Ag acts as an electron donor. The latter claim was backed by means of *ab initio* self-consistent-field calculations.[36]

Further evidence of Ag_xMoS_2 formation upon Ag interaction into MoS_2 has been reported by Allen *et al.*[37] In this case, however, instead of using solid state annealing to allow Ag to diffuse into the MoS_2, a method sometimes referred to as "exfoliation/restacking" was used. Exfoliation/restacking technique involves the intercalation of Li into the MoS_2 first by reacting natural MoS_2 crystal with excess $LiBH_4$. The MoS_2 layers are then exfoliated by soaking and then

rinsing $LiMoS_2$ in deionized water. Any excess Li is washed away as LiOH leaving negatively charged MoS_2 layers. Following, $AgNO_3$ is added into the MoS_2-deionized water solution. The Ag^+ ions in the solution allow the restacking of the exfoliated MoS_2 flakes by intercalating between the layers. Finally, the Ag_xMoS_2 product is filtered out from the solution and dried under vacuum. After the preparation of the restacked Ag_xMoS_2 compound, Allen *et al.*[37] conducted X-ray absorption fine structure (XAFS) and X-ray absorption near-edge structure (XANES) analysis to establish the oxidation state and coordination of Ag inside the MoS_2 matrix. Accordingly, they reported the formation of $Ag_{0.61}MoS_2$, where the Ag coordination in this compound was reported to be similar to that of Ag_2S because of the similarity of the XANES spectra between the two, while the heat treated $Ag_{0.61}MoS_2$ EXAFS spectra resembled that of pure silver foil indicating possible Ag-Ag interaction upon heat treatment of the $Ag_{0.61}MoS_2$ compound. Their work was partially supported by atomic pair distribution function (PDF) analysis conducted by Hwang *et al.*[38] In this dissertation work, we do not see evidence for a new compound. However, our result does indicate the presence of Ag inside the MoS_2 matrix for samples annealed at 300 °C and is correlated with low contact resistance between Ag/MoS_2, which is also manifested by the improved performance of the MoS_2 FETs.

At this point it is necessary to discuss the possible mechanisms for how annealing helped us achieve low resistance Ohmic contacts between Ag and MoS_2. In general, there are two popular methods to achieve low Ohmic contact resistance at the metal/semiconductor interface. One is to form an ultra-low Schottky (close to 0 eV) barrier height to promote current injection via thermionic emission. This goal sometimes can be achieved by choosing, for example, a low work function metals to form contacts to inject electrons. However, due to Fermi level pinning, there is in reality a weak correlation between metal work function and Schottky barrier height, making it

harder to achieve low contact resistances through this route. Alternatively, low contact resistance could be achieved by doping (for example by gating, electrostatic doping) the semiconductor such that the width of barrier is decreased, enhancing tunnelling.

To better understand the effect of the Schottky barrier at the annealed Ag/MoS_2 interface, temperature dependent I_{ds} *vs.* V_{gs} measurements were conducted under different gate voltage conditions at a fixed V_{ds} of 0.1V.[13] Using thermionic emission theory described in Section 1.3.3, an Arrhenius plot (see **Figure 5-14**a,b) was generated relating $\ln(I_{ds}/T^2)$ vs. $1000/T$ at different gate voltages. In this case $I_{ds} = AA^*T^2 \exp\left(\frac{-q\phi_{SB}}{k_BT}\right)\left[\exp\left(-\frac{qV_{ds}}{nk_BT}\right) - 1\right]$, where I_{ds} is the drain current, A is the area of the contact, A^* is the Richardson constant, q is the electronic charge, ϕ_{SB} is the Schottky barrier height, k_B is the Boltzmann constant, T is the temperature, V_{ds} is the drain voltage and n is the ideality factor. When V_{ds} is fixed, the ϕ_{SB} can be readily determined from the slope (S) of $\ln(I_{ds}/T^2)$ vs. $1000/T$ Arrhenius plot, S = $\frac{-q\phi_{SB}}{k_BT}$ for each gate voltage conditions.

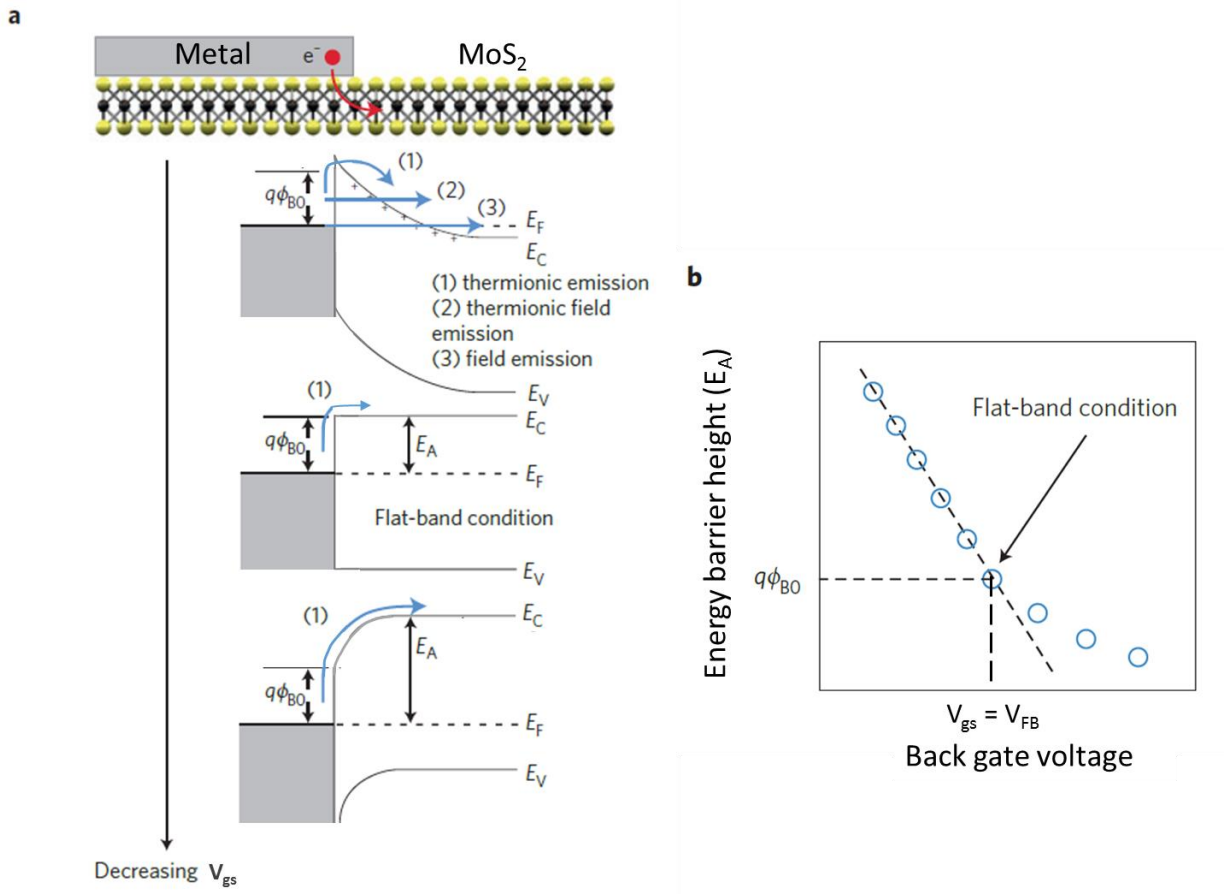


Figure 5-13 Schematic showing current transport mechanism (a) across a generic metal/MoS_2 interface as a function of decreasing back gate voltage. (b) A generic plot of the energy barrier (E_A) at the metal/MoS_2 interface as a function of back gate voltage. The flat band condition is achieved at the point where the energy barrier height is no longer linearly dependent on gate voltage. The effective Schottky barrier height is extracted at $V_{gs} = V_{FB.}$ Plot adopted from a review article by Allain *et al.*[29]

To accurately extract an effective Schottky barrier height, the flat band (V_{FB}) condition must be established from ϕ_{SB} vs. V_{gs}.[6,29] In this case V_{FB} represents the applied gate voltage such that there is no band bending in the semiconductor (see **Figure 5-13**a, b). Accordingly, $V_{gs} = V_{FB}$ corresponds to the gate voltage below which ϕ_{SB} is linearly dependent on the gate voltage so that thermionic emission dominates. However, at sufficiently high gate voltage condition (in this case $V_{gs} >$ -5V), tunneling current starts to contribute such that ϕ_{SB} vs. V_{gs} is no longer linear, deviating

from the thermionic emission equation. The effective Schottky barrier height is extracted at $V_{gs} = V_{FB.}$ For the annealed Ag/MoS_2 contacts the effective ϕ_{SB} ~ 90 meV, which is higher than the ϕ_{SB} reported for Sc and Ti, but it is lower compared to those reported for Au, Ni or Pt. In general, a smaller Schottky barrier height at the metal/MoS_2 interface corresponds to lower contact resistances despite the strong Fermi level pining reported for these type of contacts.[6] Hence, the modest contact resistance for Ag contacts to MoS_2 reported in this work can be partially attributed to the low Schottky barrier height.

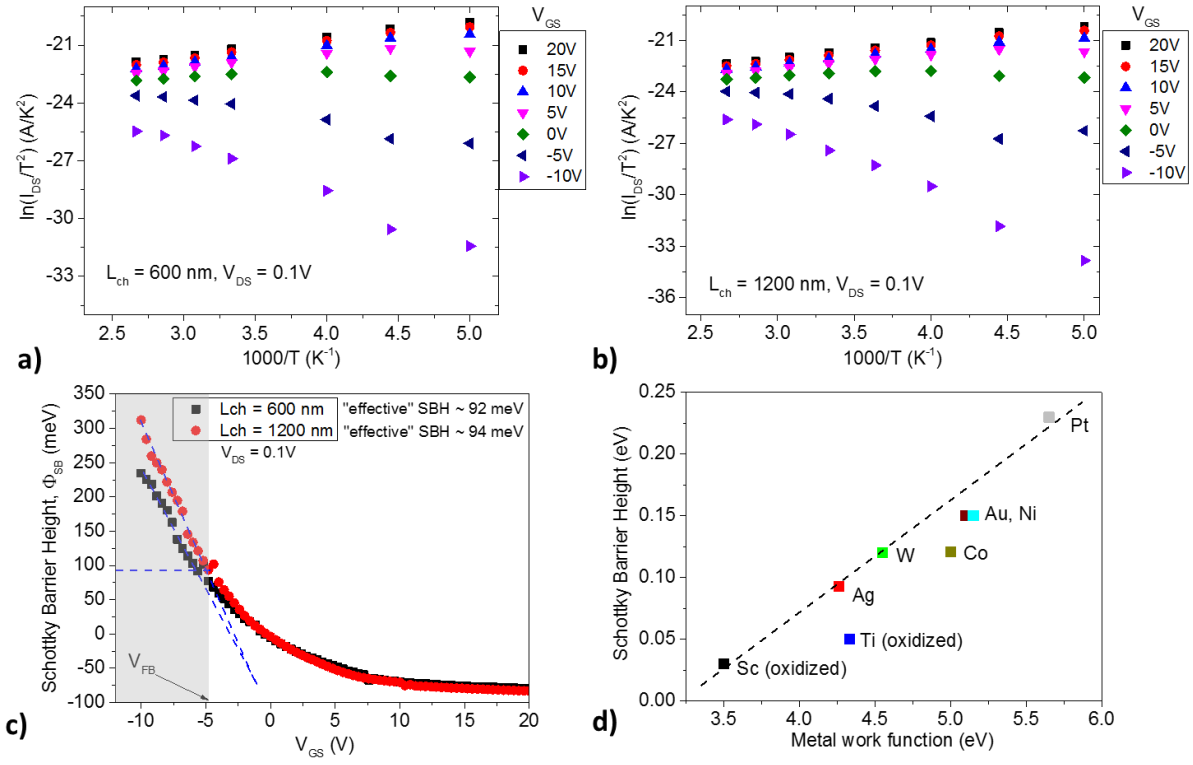


Figure 5-14 Measured temperature dependence of current transport and extraction of the Schottky barrier height. (a,b) Arrhenius-type plots of $\ln(I_{ds}/T^2)$ vs. $1000/T$ at various gate voltages for two annealed Ag/MoS_2 FET devices with different channel length. (c) Gate bias dependence of the Schottky barrier height and the extracted effective Schottky barrier height at $V_{gs} = V_{FB}$. (d) Extracted effective Schottky barrier height as a function of work function of Sc, Ti, W, Co, Au Ni, Pt (Ref 6, 23) and Ag (this work). The dotted line is meant to be a guide to the eyes.

Based on the TEM results, temperature dependent measurements and previous observation in the literature, we may speculate that annealing led to low contact resistance because of three reasons. First, the interdiffusion at the Ag/MoS_2 interface, even though limited to the first few layers, upon annealing might lead to an intimate Ag/MoS_2 contact, enhancing current injection at the interface (see **Figure 5-9**,**Figure 5-10**,**Figure 5-19** and the schematic in **Figure 5-15**). Secondly, Ag inside the MoS_2 matrix can potentially act as dopant of the underlying semiconductor, thereby lowering contact resistance by decreasing the Schottky barrier width.

Finally, as discussed earlier, Ag can also act as a "glue" between the layers. To see how this could work, first we need to take a look at a recent work by Das *et al*.[39] They argued that the effective contact resistance R_c, like the one reported in this work, is the sum of source/drain Schottky barrier resistance (R_{SB}) and an effective interlayer resistance (R_{inter}), which is due to weak coupling (van der Waals gap) between the layers.[39] A smaller R_{inter} contributes to lowering the total on-resistance in multi-layer MoS_2 FETs. Therefore, the incorporation of Ag into the MoS_2 matrix could lead to smaller R_{inter} by increasing the interlayer coupling, creating good electrical contact to each individual MoS_2 layer (**Figure 5-15**).[34,35] Therefore, this leads to lower effective contact resistance in annealed contacts than in the as-deposited ones. In this case, because of its metallic nature, MoS_2:Ag right under the Ag contact would be less affected by the gate voltage compared to the MoS_2 between the contacts. Since R_c scales with sheet resistance of the MoS_2:Ag (see **Section 1.3.4**), it should also be weakly affected by the gate bias. This is indeed the observed behavior of the annealed contacts investigated in this work **Figure 5-7**.

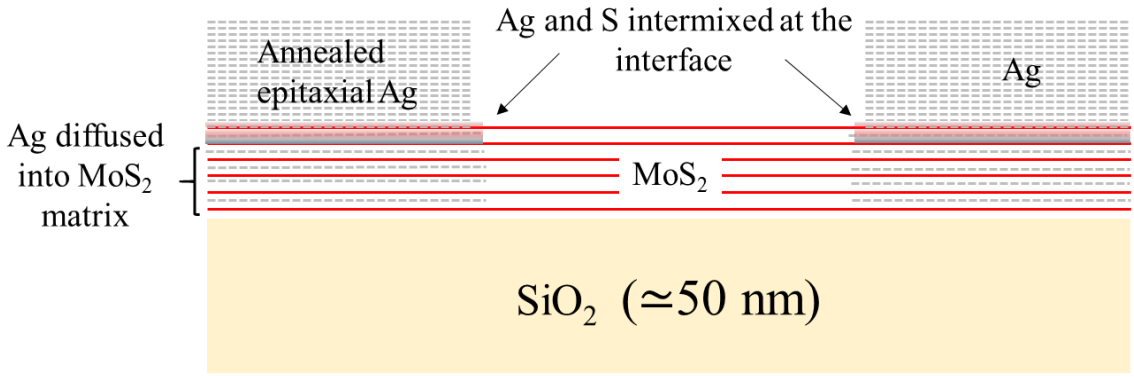


Figure 5-15 Schematic of a typical Ag/MoS_2 interface after annealing.

5.5 Summary

In conclusion, we have demonstrated contact resistances in the range of 0.2–0.5 kΩ μm for annealed Ag contact on MoS_2. Annealed MoS_2 FETs with Ag source and drain contacts also exhibited promising device characteristics. In order to provide some insight about the effect of annealing, we have presented cross-sectional TEM results with in-depth EELS analysis of the Ag/MoS_2 interface. The TEM data showed interdiffusion at the interface allowing the formation of an intimate contact. Furthermore, Ag was detected inside the MoS_2 flake, indicating Ag diffusion across the MoS_2 layers parallel to the c-axis. Accordingly, it was proposed that Ag in-diffusion into the MoS_2 enabled good electrical contact between the MoS_2 layers and also acts as a dopant (electron donor), thereby reducing the total resistance in the source and drain regions of the contact. Overall, annealed Ag contacts presented in this work provide promising and simple CMOS compatible processing technology for reducing the contact resistance in MoS_2 FETs.

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5.7 Appendix

5.7.1 TEM characterization

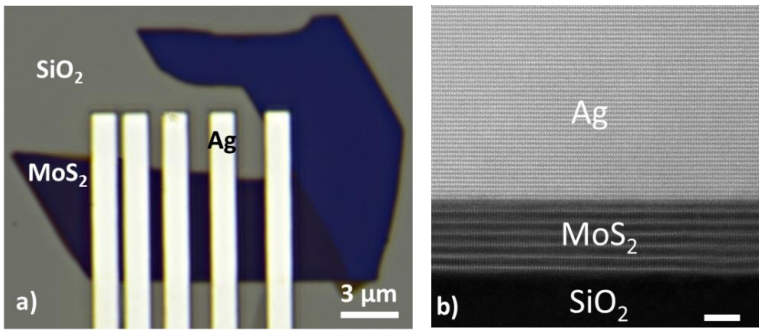

Figure 5-16 (a) Optical image of TLM structure on MoS_2. (b) High magnification STEM-HAADF micrograph (collected at 300 kV) of the same device in (a) showing Ag contact on top of a 6 layer MoS_2 flake. The MoS_2 flake was found to be consistent across multiple contacts, as required for the effective use of the TLM test structure to extract the contact resistance.

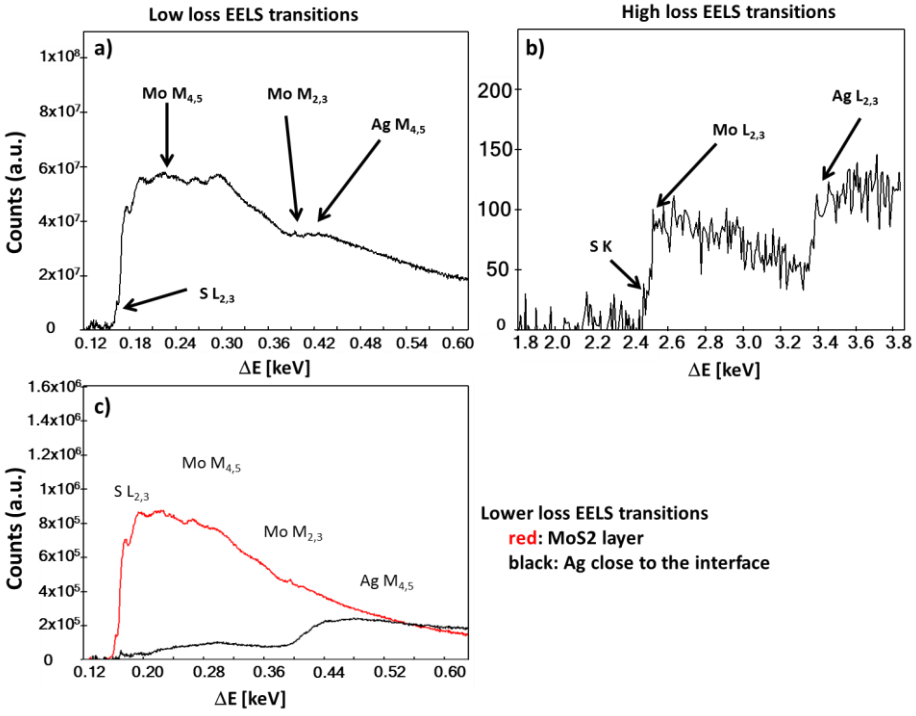

Figure 5-17 STEM-EEL spectra collected near Ag/MoS_2 interface at (a, c) 80 kV and (b) at 300 kV for the sample in **Figure 5-16** that was annealed at 300°C for 300 s. These EEL spectra represent the low loss (a, c) and the high loss (b) peaks for S, Mo, and Ag after background subtraction.

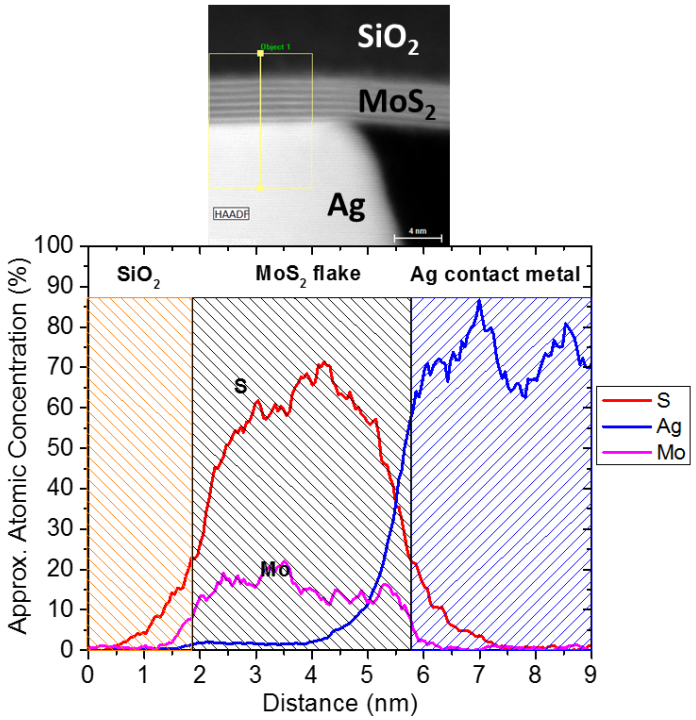

Figure 5-18 High resolution STEM-HAADF image collected at 80 kV and a corresponding STEM-EDX line profile of Ag, S and Mo across (a) Ag/MoS_2 contact interface for a sample annealed at 300°C for 300 s. The scale bar in the on the HAADF images represent 4 nm. The EDX line profile provided additional evidence that Ag signal does not go to zero inside the MoS_2 matrix in agreement with the EELS map and line profiles presented in the main body of this chapter.

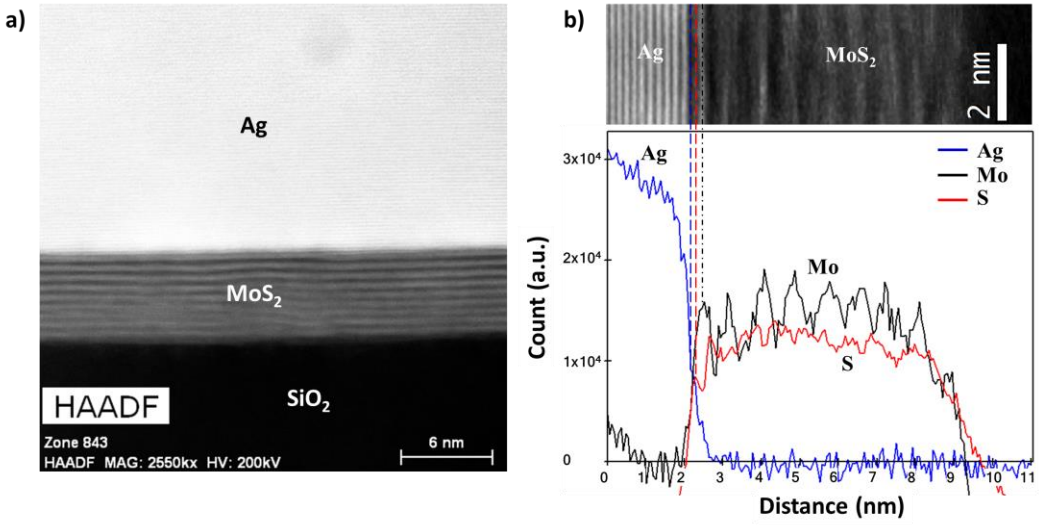

Figure 5-19 (a) High resolution STEM-HAADF image collected at 200 kV and a corresponding STEM-EELS line profile of Ag, S and Mo across (b) Ag/MoS_2 contact interface for a sample annealed at 300°C for 300 s.

5.7.2 Auger depth profile of annealed contacts

Results from Auger depth profiling also suggested the in-diffusion Ag into MoS_2. Two samples were prepared one with 30 nm Ag and the other sample with 30 nm blanket Au films deposited on freshly exfoliated, bulk-like MoS_2 flakes. Additional 10 nm SiO_2 capping layer was deposited to limit sulfidization of Ag film during annealing. The samples were then annealed at 350°C for 300 s in RTA under Ar environment and introduced into AES ultra-high vacuum (UHV) analytical chamber (at base pressure $<10^{-9}$ Torr). A 3 keV Ar^+ ions beam was used to sputter depth profile at etch rate ~0.5 Å/s or ~7.5 Å/cycle. Each sputtering cycle involved 15s etch time followed by 10 s intervals before AES analysis of newly etch surface using at least 5 sweeps/element.

AES spectra extracted from the depth profile show (**Figure 5-20**a and **Figure 5-20**b) persistent presence of Ag peak near the Ag/MoS_2 interface and deep into the MoS_2 flake suggesting in-diffusion of Ag into the MoS_2. On the other hand, no distinguishable Au peak was detected inside MoS_2 flake with annealed Au contact on top (Figure 7b). Limited out diffusion of Mo or S into the Ag or Au films was detected. Despite the agreement of AES result with the result obtained from our TEM study, it is important to note that AES depth profile results can still lead to an erroneous conclusion. The main reason being that the presence of a small peak overlap between Ag and Mo (see **Figure 5-20**c). Even though the Mo peak compared to Ag peak is significantly small (over 100X smaller), it might still affect the interpretation of Ag in-diffusion into the MoS_2 matrix, particularly if Ag diffuses in at a dopant level. In addition, factors such as ion bombardment induced diffusion (atomic mixing), thermal diffusion and preferential sputtering can lead to compositional alteration at the interface erroneously suggesting possible in-diffusion Ag upon annealing. Hence caution is needed in interpreting this result.

As a side note, the Auger depth profile showed conclusive evidence that the SiO_2 capping on Ag does not react with Ag. Therefore, the SiO_2 cap does not affect the electrical properties of the contact at the Ag/MoS_2 interface.

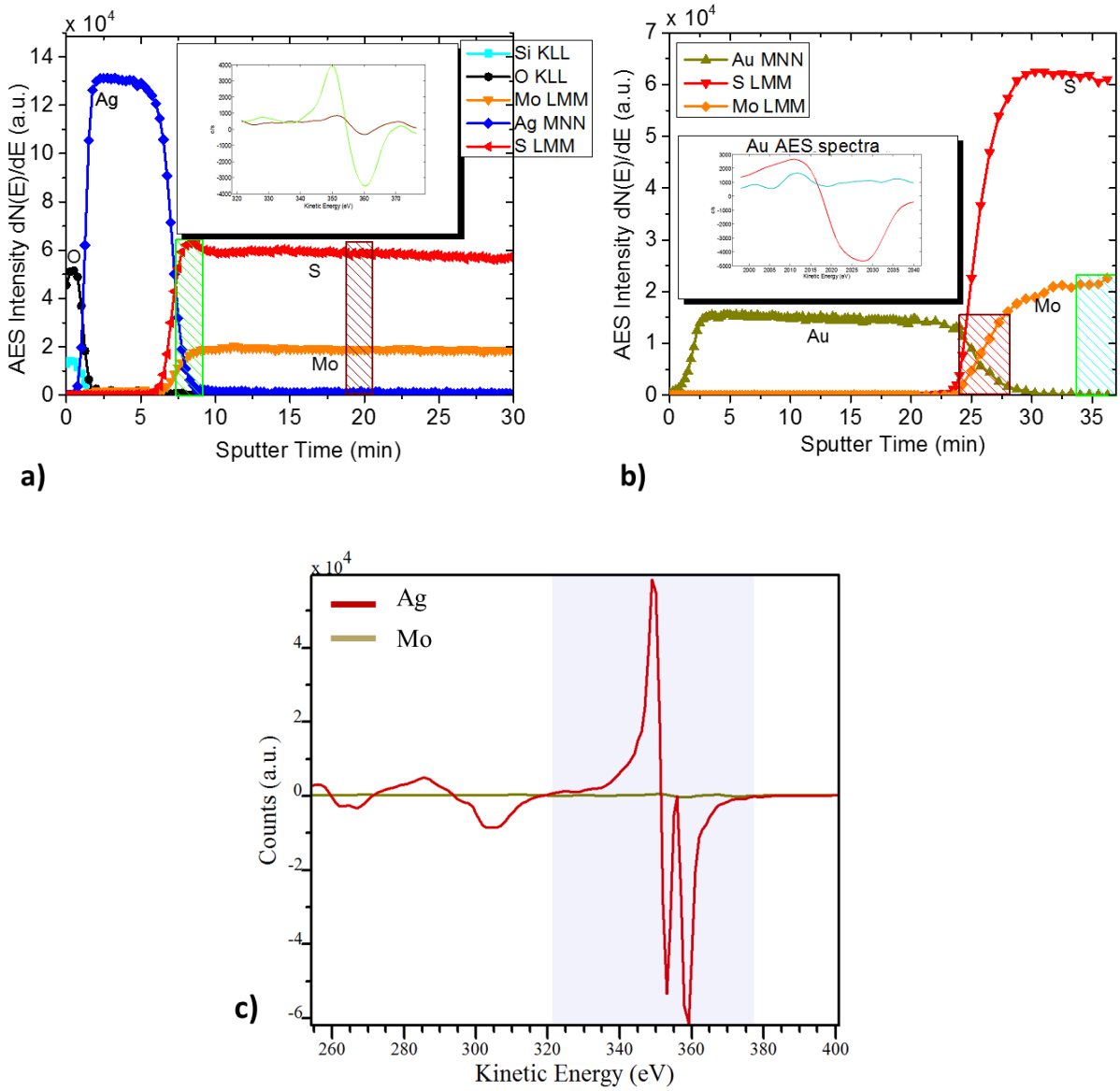

Figure 5-20 AES depth profiles of (a) 10 nm SiO_2 capped 30 nm Ag on bulk-like MoS_2 flake annealed at 350°C for 300 s in RTA under Ar environment. (b) 30 nm Au on bulk-like MoS_2 flake annealed at 350°C for 300 s in RTA under Ar environment. The inset on both graphs represent AES spectra extracted from select regions of the main depth profiles (represented by the highlighted regions). (c) AES spectra for pure Ag and Mo showing peak overlap at 359 eV. The intensity of the Mo peak at 358 eV is over 100X smaller compared to the Ag peak in the same region.

5.7.3 Comparing to literature data

Table 5-1 Summary of MoS_2 FETs characteristics comparing literature results (Ref. [15], Ref. [6], Ref. [16], Ref. [13] and Ref. [18]) to those reported in this work.

	Chlorine doped	Sc contacts	Phase Engineered	Au (UHV)	Ni/graphene	This work
EOT (nm)	90	100	100	90	285	50
L_{ch} (nm)	500	5000	1200	100	1000	670
R_c (kΩ µm)	0.5	0.65	0.2-0.3	0.7	0.2-0.3	0.2-0.4
I_{ds} (µA/µm) @ V_{ds}= 1V	250	3.5	85	N/A	200	78
I ON/OFF at V_{ds} of	6.3 x 10^5 at 1.2 V	10^7 at 1V	10^8 at 1V	N/A	10^5 at 0.2V	10^7 at 0.1V
Peak field effect mobility (cm^2/V-s)	50-60	184	46	35	80	46
Number of layers	6	15	3	7	25	8

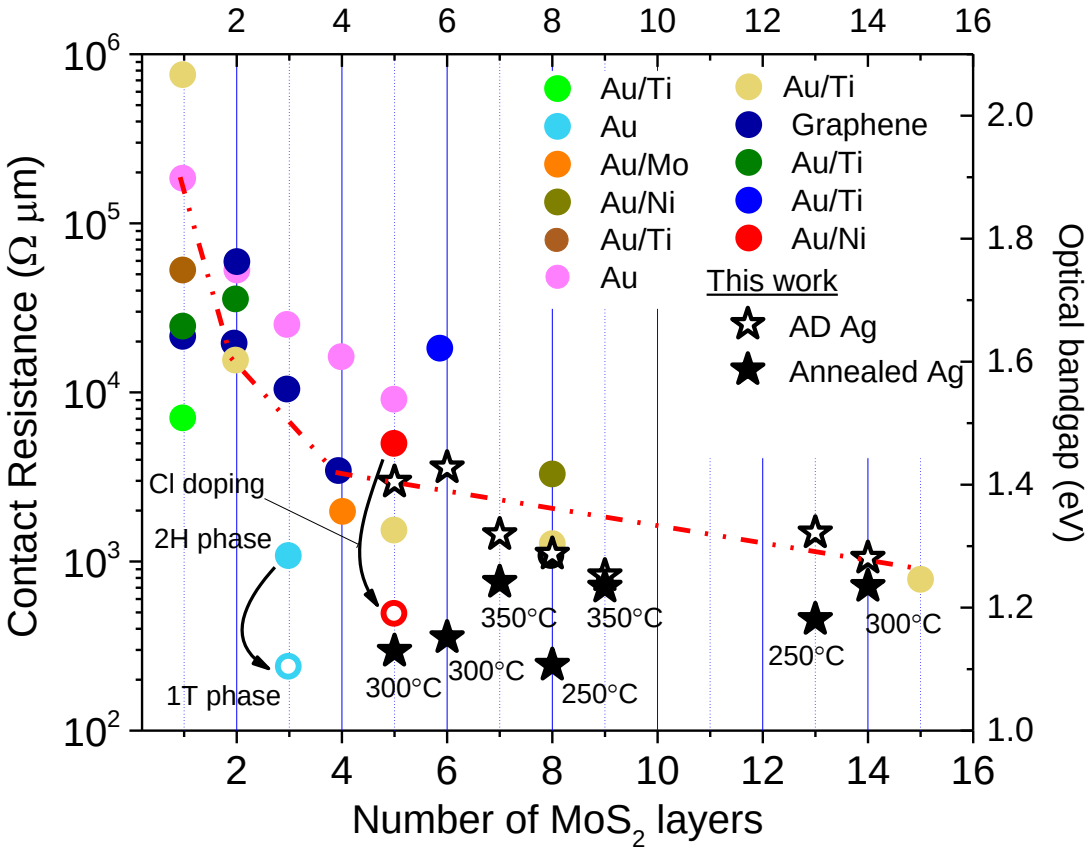

Figure 5-21 Contact resistance as a function of the number of atomic layers for several studies on MoS_2 including the results from this work. Plot adopted from a review article by Allain *et al.*[29]

5.7.3 Contact resistance and mobility as function of flake thickness

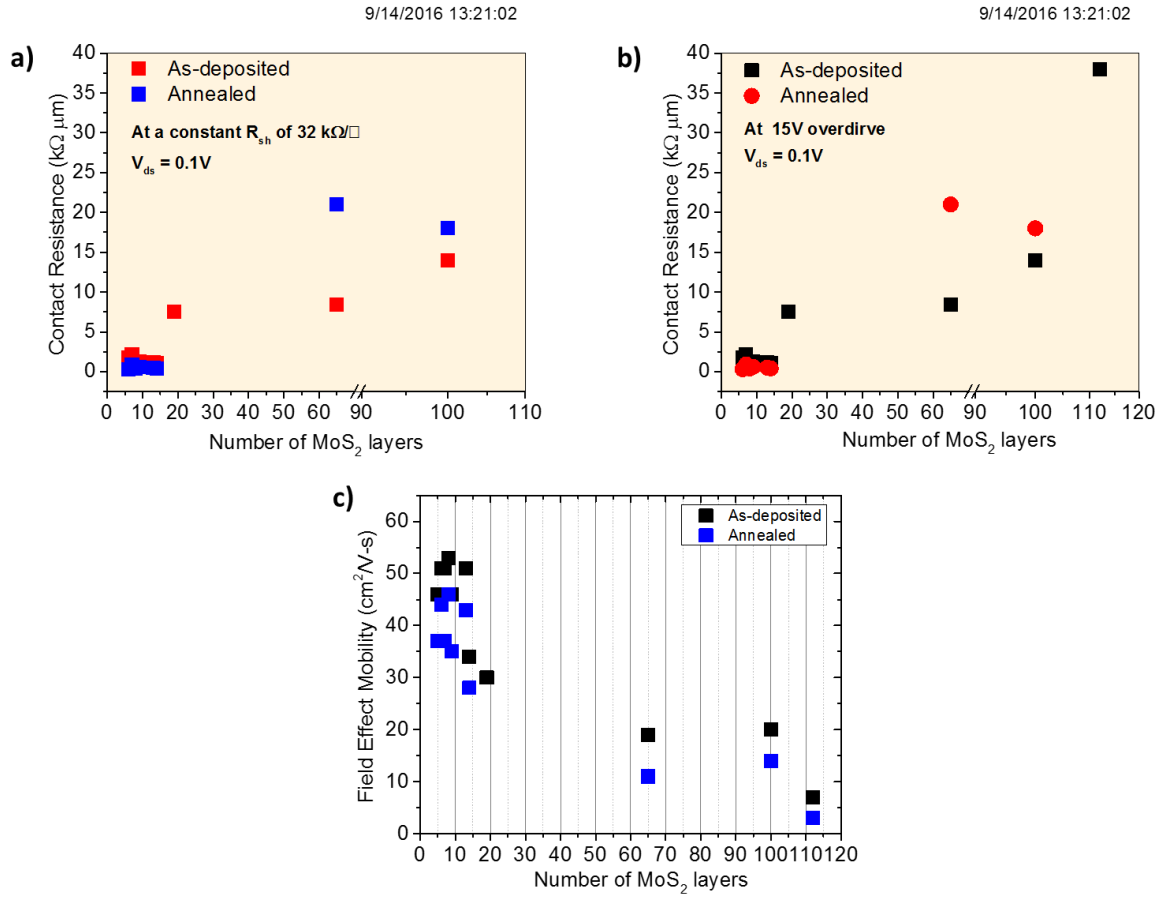

Figure 5-22 Contact resistance as a function of the number of atomic layers for several MoS_2 devices investigated in this work (a) evaluated at constant sheet resistance of 32 kΩ/□ and (b) at constant gate overdrive voltage of 15V. Gating mostly affects the bottom layers of the MoS_2 flakes. For thicker flakes, gating has reduced effect on the top most active layers of the MoS_2 device due to charge screening effect. (c) Room temperature field effect mobility as function of atomic layers for several MoS_2 devices investigate in this work. The mobility follows similar trend with flake thickness as previously reported by Das *et al.*[6,31]

Chapter 6

Summary and Future Work

6.1 Summary

This dissertation discussed the fabrication, characterization, and consequent fundamental studies of Ti/Al contacts to GaN/AlGaN HEMTs heterostructure, silicide-like Ni contacts to $In_{0.53}Ga_{0.47}As$ ($N_D = 5 \times 10^{19}$ cm^{-3}), and Ag contacts to MoS_2. The theme linking the three studies is that pre-metallization surface preparation and post-metallization annealing are important to lowering the contact resistance. The main conclusions from these studies are summarized below:

- **Ti/Al contacts to GaN/AlGaN HEMT heterostructure**. The formation of a Ti–Al–Ga–N interfacial phase reduced the resistance of Ohmic contacts to an N-polar GaN/AlGaN heterostructure, and we produced a contact with low specific contact resistance to N-polar HEMTs without the use of a regrowth step. Even a minor variation in the Ti:Al ratio at the contact interface affected the interfacial phase formation, altering the specific contact resistance. A ρ_c as low as 2.5×10^{-7} Ω cm^2 was achieved for as-deposited Al(3 nm)/Ti(50 nm)/Al(147 nm) contacts. After being annealed at 500 °C for 60 s, this contact did not change appreciably in contact resistance, only from 0.11 Ω mm to 0.10 Ω mm. This observation further demonstrates that the presence of both Al and Ti at the metal/GaN interface—prior to reaction of Ti with GaN to form a Ti–Ga–N layer—is critical to forming low-resistance Ohmic contacts to N-polar GaN/AlGaN HEMTs.

- **Silicide-like Ni contacts to $In_{0.53}Ga_{0.47}As$ (N_D = 5 × 10^{19} cm^{-3}).** Ni-based contacts to heavily doped n-InGaAs, including epilayers with thin InP caps, were investigated. The resistance of the contacts depended on annealing conditions. Upon rapid thermal annealing at 350 °C for 60 s, a uniform Ni_xInGaAs layer formed (beneath Ni_xInP when InP-capped epilayers were used), and low ρ_c values of 4.0 × 10^{-8} ± 7 × 10^{-9} Ω·cm^2 and 4.6 × 10^{-8} ± 9 × 10^{-9} Ω·cm^2 were achieved on InGaAs capped with 10 nm of InP and on uncapped InGaAs, respectively. Similar samples subjected to an additional $(NH_4)_2S$ surface treatment before metallization exhibited an as-deposited ρ_c about an order magnitude lower than that of the untreated samples. In the treated samples, the specific contact resistance remained low, near 2 × 10^{-8} Ω·cm^2, after annealing at 350 °C for 60 s.

  When contacts were prepared without a $(NH_4)_2S$ pre-metallization surface treatment, a native oxide appeared between Ni and the semiconductor. Nickel diffused through this oxide upon annealing at 350 °C, forming an oxide-free Ni_xInGaAs contact to n-InGaAs and reducing the specific contact resistance. Since the n-InGaAs was heavily doped (N_D = 3 × 10^{19} cm^{-3}), the dominant current transport mechanism was tunneling through the Schottky barrier, and removing the interfacial oxide eliminated an additional resistance in series with the barrier. For $(NH_4)_2S$-treated samples, the interfacial oxide was avoided, and even the as-deposited contacts exhibited low resistance due to the formation of an oxide-free, intimate contact.

  To avoid the overestimation of ρ_c that may have occurred in other studies, we applied a Ti/Pt/Au cap on the Ni_xInGaAs and using a refined TLM test structure. With further minor reduction in specific contact resistance, possibly by using more heavily

doped epilayers, the $Ni_xInGaAs$ contacts should meet the needs of aggressively scaled self-aligned field-effect transistors with InGaAs channels.

- **Ag contacts to MoS_2**. We demonstrated MoS_2 FET source and drain contact resistances of 0.2–0.5 kΩ μm for annealed Ag contacts along with promising device characteristics. To give some insight about the effect of annealing, we used cross-sectional TEM to conduct EELS analysis of the Ag/MoS_2 interface. The TEM data showed one or two monolayers of intermixed region at the interface, indicating the formation of an intimate contact. No gross interfacial contaminant species appeared, thanks to the effective pre-metallization surface preparation. Furthermore, Ag was detected inside the MoS_2 flake, indicating Ag diffusion across the MoS_2 layers parallel to the c-axis. Accordingly, it was proposed that Ag in-diffusion into the MoS_2 enabled good electrical contact between the MoS_2 layers and also acts as a dopant (electron donor), thereby reducing the total resistance in the source and drain regions of the contact.

6.2 Future work

Despite the promising results presented in this dissertation, there are several points that need clarification to better understand the electrical characteristics of the contacts under investigation. Below are suggested experiments for future work to help elucidate some of the key issues that were not fully addressed in this dissertation.

6.2.1 Contacts to GaN/AlGaN HEMT heterostructures

In Chapter 3, during the discussion of Ti/Al contacts to GaN, we found that low contact resistances were achieved only for contacts with Al, Ti, Ga, and N present at the

metal/semiconductor interface. Based on TEM results, we suggested that an interfacial phase formed that may have a low work function, which may have reduced the Schottky barrier height. In the future, however, *I–V–T* measurements can be conducted to measure the Schottky barrier height[1] of as-deposited and annealed Ti/Al contacts with different interfacial chemistries. Temperature-dependent measurement may also help explain the current transport mechanisms in the as-deposited and annealed Ti/Al contacts.[2]

6.2.2 Contacts to InGaAs

In Chapter 4, we found that depositing a thin InP capping layer above InGaAs can help to produce a shallow silicide-like Ni contact to InGaAs. This is possible because Ni reacts with the InP layer first before reacting with the underlying InGaAs. In addition, we claimed that the InP capping layer suppresses the outdiffusion of Ga at higher annealing temperature, increasing the thermal stability of the Ohmic contacts to the InP/InGaAs heterostructure.[3] Even though the contacts investigated in this work were annealed up to 400 °C for 60 s, we did not perform additional experiments to evaluate the thermal stability of Ni contacts to InP/InGaAs. This is particularly a concern for InGaAs because it must be compatible with pre-existing CMOS back-end-of-line (BEOL) processing. Some BEOL processes require long-term thermal stability at temperatures of 400–450 °C.[3] Therefore, it is imperative that future work involves a more comprehensive assessment of thermal stability, carefully evaluating the extent of Ga outdiffusion in uncapped and InP-capped samples. This could be partially accomplished by depositing thin (~10–20 nm) Ni films on samples and then performing AES surface analysis on the as-deposited and annealed samples. If Ga outdiffuses, it can be easily detected at the surface. XPS can also be used to provide chemical bonding information about the outdiffused Ga on the surface. In both

AES and XPS, the samples can be annealed *in situ* up to 500 °C to assess the time and temperature dependence of Ga outdiffusion.

The long-term thermal stability of Ni contacts to InP/InGaAs can be evaluated by annealing the samples at elevated temperature (≥400 °C) for up to 24 h in an inert environment (under Ar or N_2). Consequently, both the electrical and morphological characteristics of the contacts can be studied before and after heat treatment. Note that the thermal stability of the contacts also depends on the endurance of the overlay Ti/Pt/Au metals, if they are used. In this dissertation, we observed that a thicker Ti/Pt layer (>45 nm) may be required at high annealing temperature to prevent Au from reaching the metal/semiconductor interface.

6.2.3 Contacts to transition metal dichalcogenides

The preparation of Ag contacts to MoS_2 presented in this dissertation involved extensive pre-metallization surface preparation, focused on removing tape and resist residues from the surfaces of the MoS_2 flakes. For this purpose, we used only only acetone and vacuum annealing, along with optimized electron-beam resist (PMMA) developing solutions. However, there is at least one more surface preparation option, ammonium sulfide $(NH_4)_2S$, which proved effective in both of the experiments in which it was used in this dissertation.

During this work, the author, with the help of undergraduate student Yitian Zeng, briefly investigated how ammonium sulfide treatment affected the contact resistance of Ti contacts to MoS_2, using an $(NH4)_2S$:IPA solution with varying concentration. $(NH4)_2S$:IPA also served as a PMMA developing solution, which produced well-defined, high-resolution features. Preliminary results showed that all samples treated with the ammonium sulfide solution immediately before metallization exhibited significantly lower contact resistance than samples with no treatment (see

Figure 6-1). Samples treated with 1:10 $(NH_4)_2S$:IPA (High ST) for 90 s exhibited the greatest reduction in contact resistance. These promising results warrant additional investigations to better understand the role of ammonium sulfide at the metal/semiconductor interface. Cross-sectional TEM can be used to investigate the sulfide-treated metal/semiconductor contact, while temperature-dependent *I*–*V* measurements may reveal how the treatment affects interfacial contact characteristics such as the Schottky barrier height. This surface preparation may only be used with as-deposited Ag contacts because annealing can cause detrimental Ag:S reaction.

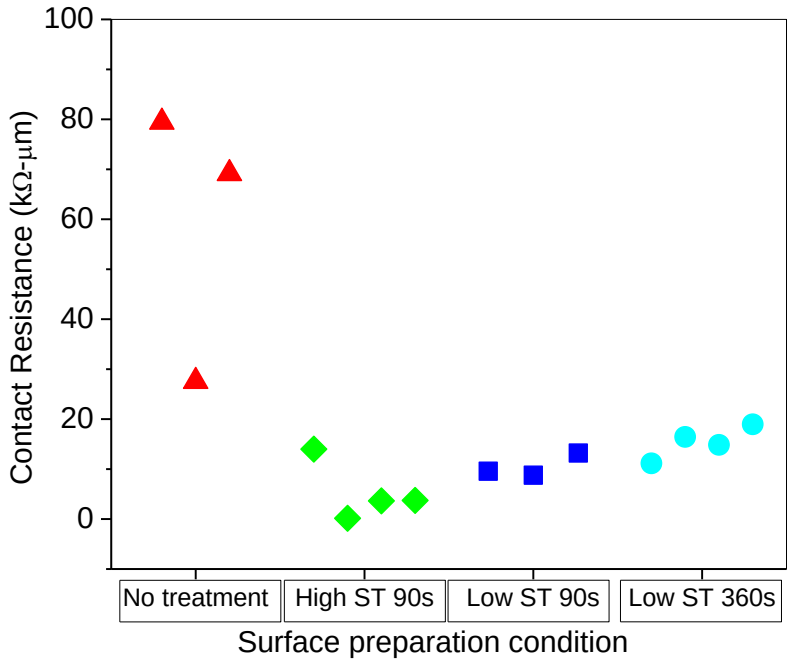

Figure 6-1 Extracted effective contact resistance for devices with various sulfur treatments. Each data point represents an individual sample. "High ST" denotes the 1:10 $(NH_4)_2S$:IPA solution, while "Low ST" denotes the 1:100 $(NH_4)_2S$:IPA solution, where $(NH_4)_2S$ comes from 24% stock solution.

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2. **M. Abraham**, S-Y.Yu, W. H. Choi, R.T.P. Lee, and S. E. Mohney, "Very low resistance Ni-based alloyed contacts to InP-capped and uncapped n^+- InGaAs" Journal of Applied Physics 116, 164506 (October 2014).
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