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COMPLIMENTARY III-V HETERO-JUNCTION TUNNEL TRANSISTORS FOR ENERGY EFFICIENT NANOELECTRONICS

A Dissertation in
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Abstract

As we venture into the era of Internet of Things, we witness a data explosion driven by network of intelligent electronic devices with multi-modal sensing capabilities. Consequently, there is a significant demand for low-latency high-performance data processing which is not only reliable but also energy efficient. The requirement of maintaining high performance at extremely low power is especially critical for mobile platforms.

The silicon MOSFET which is the workhorse of today’s semiconductor industry has addressed this demand through relentless shrinking of its dimensions and steady reductions to its operating voltage. However, the benefits wrought by reducing the size of the transistor, which are detailed in Moore’s law, are now under threat. If the threshold voltage of the silicon MOSFET were reduced to enable a scaling of the operating voltage, there would be an exponential increase in the off-state current and a corresponding explosion in energy loss. This is a prominent concern for circuit designers because the sub-threshold leakage power is as significant as the active power in microprocessors.

The high sub-threshold leakage power stems from the inability of the MOSFET to provide steep switching from the on-state to the off-state. The switching capability of MOSFET is measured by switching slope (SS) which is defined as the magnitude of switching voltage needed to produce a decade change in drain current, limited to 60 mV/decade in MOSFET at room temperature. Origin of this limit is the Boltzmann distribution describing the energy of carriers in the source region that are emitted thermionically over the barrier. This Boltzmann tyranny has driven efforts to look for alternative devices delivering steeper switching to extend supply voltage scaling without compromising performance.

Within this effort, one steep switching device that is piquing the interest of many is the tunnel FET (TFET). In this work, we explore III-V compound semiconductors based GaAs\(_{1-x}\)Sb\(_x/\)In\(_y\)Ga\(_{1-y}\)As Hetero-junction Tunnel Field Effect Transistors (HTFETs) for realizing energy-efficient complimentary logic. Both n-channel and p-channel HTFETs are fabricated and characterized, exhibiting best in class on-current
(I_{ON}) and on-off current ratio (I_{ON}/I_{OFF}) at |V_{DS}|=0.5V. To further improve the electrical performance of HTFET, we perform an in-depth characterization of critical semiconductor interfaces in HTFET and identify and prescribe metrics for high-performance HTFET design. Moreover, we also investigate HTFET circuit design elements and benchmark its performance against corresponding implementation in sub-threshold Si-FinFET technology. We conclude by presenting a course for enhancing group III-V HTFET technology besides providing a brief insight into potential alternatives for TFET design using group IV semiconductors.
# Table of Contents

List of Figures viii

List of Tables xviii

Acknowledgments xix

## Chapter 1

Introduction 1

1.1 Motivation 1

1.1.1 Why Tunnel FET for low power energy efficient applications? 3

1.1.2 Why III-V compound semiconductor based Hetero-junction Tunnel FET? 4

1.1.3 Complimentary TFETs: State of the Art 8

1.2 Organization of this thesis 9

## Chapter 2

High-κ/III-V Interface Engineered Gate Stack 12

2.1 Introduction 12

2.2 III-V surface preparation techniques 13

2.3 Gate Stack on Sb-channel PTFET 15

2.3.1 GaAs$_{0.35}$Sb$_{0.65}$ MOSCAP Fabrication 15

2.3.2 High-κ/GaAs$_{0.35}$Sb$_{0.65}$ Interface Characterization 16

2.4 Gate Stack on As-channel NTFET 19

2.4.1 In$_{0.53}$Ga$_{0.47}$As MOSCAP Fabrication 21

2.4.2 High-κ/In$_{0.53}$Ga$_{0.47}$As Interface Characterization 21

## Chapter 3

Complimentary HTFET fabrication and Electrical Characterization 26

3.1 TFET Device Fabrication 26
<table>
<thead>
<tr>
<th>Section</th>
<th>Title</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>3.1.1</td>
<td>Hetero-structures for complimentary HTFET</td>
<td>26</td>
</tr>
<tr>
<td>3.1.2</td>
<td>TFET Fabrication and high-κ dielectric integration</td>
<td>27</td>
</tr>
<tr>
<td>3.2</td>
<td>TFET Electrical Characterization and Performance Benchmark</td>
<td>30</td>
</tr>
<tr>
<td>3.2.1</td>
<td>DC Characterization</td>
<td>30</td>
</tr>
<tr>
<td>3.2.2</td>
<td>Fast I-V characterization</td>
<td>32</td>
</tr>
<tr>
<td>3.2.3</td>
<td>Complimentary TFET performance benchmark</td>
<td>34</td>
</tr>
<tr>
<td>4.1</td>
<td>Critical Interfaces in MOSFET</td>
<td>42</td>
</tr>
<tr>
<td>4.2</td>
<td>Critical Interfaces in TFET</td>
<td>42</td>
</tr>
<tr>
<td>4.2.1</td>
<td>Interface 1: Tunnel Hetero-junction Interface</td>
<td>44</td>
</tr>
<tr>
<td>4.2.1.1</td>
<td>Junction Abruptness</td>
<td>44</td>
</tr>
<tr>
<td>4.2.1.2</td>
<td>Dopant Profile Abruptness and Random Dopant Fluctuation</td>
<td>51</td>
</tr>
<tr>
<td>4.2.2</td>
<td>Interface 2: High-K dielectric/III-V channel Interface</td>
<td>54</td>
</tr>
<tr>
<td>4.2.2.1</td>
<td>Temperature dependent I-V</td>
<td>55</td>
</tr>
<tr>
<td>4.2.2.2</td>
<td>Degradation with time: BTI analysis</td>
<td>60</td>
</tr>
<tr>
<td>4.3</td>
<td>Prescription for high performance TFET design</td>
<td>69</td>
</tr>
<tr>
<td>4.4</td>
<td>Complimentary HTFETs: Technology Projection</td>
<td>69</td>
</tr>
<tr>
<td>5.1</td>
<td>Introduction</td>
<td>74</td>
</tr>
<tr>
<td>5.2</td>
<td>Electrical Noise Aware Differential Amplifier Design</td>
<td>75</td>
</tr>
<tr>
<td>5.2.1</td>
<td>Electrical Noise Mechanisms</td>
<td>76</td>
</tr>
<tr>
<td>5.2.1.1</td>
<td>Random Telegraph Noise (Low Frequency)</td>
<td>76</td>
</tr>
<tr>
<td>5.2.1.2</td>
<td>Flicker Noise (Low Frequency)</td>
<td>79</td>
</tr>
<tr>
<td>5.2.1.3</td>
<td>Shot Noise and Thermal Noise (High Frequency)</td>
<td>80</td>
</tr>
<tr>
<td>5.2.2</td>
<td>Electrical Noise: TFET vs. FinFET (Device Performance)</td>
<td>81</td>
</tr>
<tr>
<td>5.2.3</td>
<td>Differential Amplifier Circuit Design and Electrical Noise Assessment</td>
<td>82</td>
</tr>
<tr>
<td>5.3</td>
<td>Memory design: RTN Aware TFET SRAM Analysis</td>
<td>85</td>
</tr>
<tr>
<td>5.3.1</td>
<td>TFET Schmitt-Trigger based SRAM Design</td>
<td>85</td>
</tr>
<tr>
<td>5.3.2</td>
<td>RTN inclusion in SRAM Simulation</td>
<td>85</td>
</tr>
<tr>
<td>5.3.3</td>
<td>Noise Margin Evaluation</td>
<td>86</td>
</tr>
<tr>
<td>5.3.4</td>
<td>TFET vs. FinFET SRAM: Performance Benchmark</td>
<td>88</td>
</tr>
</tbody>
</table>
Chapter 6
Conclusion and Future Work
6.1 Summary and Conclusion ........................................... 90
6.2 Future work ............................................................ 93
   6.2.1 Improving III-V HTFETs ................................. 93
   6.2.2 Exploring TFET design in Group IV semiconductors .... 96

Appendix A
Complimentary Tunnel FET
fabrication procedure .............................................. 106

Appendix B
Fabrication method for ultra-thin body HTFETs ............. 114

Appendix C
DFT parameters for
phonon assisted indirect BTBT .................................. 117

Bibliography .............................................................. 119
List of Figures

1.1 (a) Data, sensors and connectivity form the fundamental blocks of next-generation electronics. (b) The design approach focuses on processing, power and reliability aspects to achieve holistic implementation. .......................................................... 1

1.2 (a) Intel CPU transistor-count, clock frequency and power dissipation trends. While transistor count has doubled every 2 years following Moore’s law, still clock frequency and power dissipated have been stagnant since 2003; (b) Power supply voltage (V$_{cc}$) scaling stopped around 1V due to of insufficient room for threshold voltage scaling; (c) Aggressive threshold voltage scaling in past decades has exponentially increased off-state leakage and hence sub-threshold power density in CMOS circuits (adapted from [1]). 2

1.3 (a) Future devices focus on threshold voltage scaling and transport enhancement. TFET provide steep-switching FET solution at ultra low V$_{cc}$; (b) Carrier-injection mechanism comparison between MOSFET and Tunnel FET. .......................................................... 4

1.4 Benchmarking of energy-delay performance of 32 bit adder implemented through beyond-CMOS devices (adapted from [2]). CMOS reference is also shown for comparison. Hetero-junction TFET (Het-JTFET in the figure) is one of the most promising candidate for beyond CMOS logic. .......................................................... 5

1.5 (a) Energy band diagram showing effective tunnel barrier height (E$_{Beff}$) reduction in heterojunction TFET; (b) Extracted band-alignment for lattice matched GaAs$_{1-x}$Sb$_x$/In$_y$Ga$_{1-y}$As hetero-junctions. Wide range of E$_{Beff}$ is obtained [3]. ................................. 6

1.6 Numerically simulated I$_{DS}$-V$_{GS}$ curves [3] for ultra-thin body double gate Tunnel FET (L$_g$=32nm, EOT=1nm) with (a) Homo-junction TFET; and (b) Hetero-junction TFET. Si-MOSFET is shown in both graphs for comparison .......................................................... 7
1.7 Switching slope (SS) vs. drain current ($I_{DS}$) benchmark of experimental demonstrations in literature for (a) p-channel TFET, and (b) n-channel TFET. For energy efficient high performance logic design, sub-$kT/q$ switching (<60 mV/decade at room temperature) is needed coupled with high on-current. This requirement directs the desired design space to the lower right corner of SS - $I_{DS}$ plot. 14 nm Si-FinFET is included for reference.

2.1 Figure adapted from [4, 5]: Numerous possible surface termination configurations in III-V semiconductors can result in drastically different interface on integration with high-$\kappa$ dielectrics compared to silicon. As a consequence, III-V/high-$\kappa$ interface exhibits pronounced presence of uncoordinated bonds, anti-site defects, etc.

2.2 (a) ALD-150LX reactor at Penn State nanofabrication facility, equipped with remote RF inductively coupled plasma (ICP) source; (b) PEALD process steps summarized.

2.3 (a) CV characteristics of p-type GaAs$_{0.35}$Sb$_{0.65}$ MOSCAPs with 3.5 nm HfO$_2$ with 1.5 min H$_2$ plasma surface clean; (b) $D_{it}$ extraction using Terman method. Gate leakage is shown in the inset.

2.4 Impact of change in substrate temperature: (a) 110°C, (a) 250°C and (a) 150°C, during pre-ALD H$_2$ plasma surface treatment on CV characteristics of GaAs$_{0.35}$Sb$_{0.65}$ MOSCAPs. Gate dielectric HfO$_2$ thickness (3.5 nm) and H$_2$ plasma clean duration (1.5 min) is kept constant at previously optimized values. Substrate temperature of 150°C is optimal for driving desorption of native oxide producing high accumulation capacitance density. It still maintains low mid-gap $D_{it}$ due to lower thermal budget of the H$_2$ plasma surface treatment process.

2.5 Optimized gate stack on p-type GaAs$_{0.35}$Sb$_{0.65}$ substrate for PTFET: (a) Capacitance voltage characteristics (3.5nm thick HfO$_2$)(b) $D_{it}$ vs. band-bending profile extracted through Terman method. Inset shows gate leakage current density (c) Normalized parallel conductance map with dotted line trace showing movement of the conductance peak maximum (d) Trap response time versus band-gap energy extracted using modified conductance method [6].

2.6 (a) CV characteristics of n-type In$_{0.53}$Ga$_{0.47}$As MOSCAPs with 3.5 nm HfO$_2$ with N$_2$ plasma/TMA clean; (b) $D_{it}$ extraction using Terman method. Gate leakage is shown in the inset.
2.7 Optimized gate stack on n-type In\textsubscript{0.53}Ga\textsubscript{0.47}As substrate for NTFET: (a) Capacitance voltage characteristics (4nm thick ZrO\textsubscript{2}) (b) D\textsubscript{it} vs. band-bending profile extracted through Terman method. Inset shows gate leakage current density (c) Normalized parallel conductance map with dotted line trace showing movement of the conductance peak maximum (d) Trap response time versus band-gap energy extracted using modified conductance method [6].

3.1 Starting hetero-structures and band-alignments for GaAs\textsubscript{0.35}Sb\textsubscript{0.65} channel PTFET and In\textsubscript{0.65}Ga\textsubscript{0.35}As channel NTFET.

3.2 (a) Fabrication sequence of planarized TFET process; (b) Separately optimized HfO\textsubscript{2} and ZrO\textsubscript{2} gate stacks procedures are used for P- and N-TFET respectively. Step by step details are included in the Appendix A.

3.3 (a) Schematic of complimentary PTFET and NTFET on common metamorphic buffer technology; (b) Cross-section TEM micrographs of fabricated PTFET and NTFET.

3.4 DC measurement: (a) Transfer, (b) Switching and (c-d) Output characteristics of PTFET. All measurements are at T= 300K, except the additional T= 77K data in sub-figure(d). NDR is visible in PTFET output characteristics at T= 77K, due to the suppression of trap response. N\textsubscript{S} denotes PTFET source doping concentration.

3.5 DC measurement: (a) Transfer, (b) Switching and (c-d) Output characteristics of NTFET. All measurements are at T= 300K, except the additional T= 77K data in sub-figure(d). NDR is distinctly visible in NTFET output characteristics at both T= 300K and 77K, due to lower D\textsubscript{it} compared to PTFET gate stack.

3.6 Simplified circuit set-up used for fast I\textsubscript{DS}-V\textsubscript{GS} measurements. The measurements were performed at National Institute of Standards and Technology, Gaithersburg MD.

3.7 Improvement in transfer and switching characteristics of (a-b) PTFET and (c-d) NTFET through Fast I\textsubscript{DS}-V\textsubscript{GS} characterization. PTFET achieves near 100mV/decade switching and NTFET delivers a sub-thermal switching of 55 mV/decade. All measurements are at T= 300K.
3.8 Switching slope (SS) vs. drain current ($I_{DS}$) benchmark of experimental demonstrations in literature for (a) p-channel TFET, and (b) n-channel TFET. For energy efficient high performance logic design, sub-$kT/q$ switching (<60 mV/decade at room temperature) is needed coupled with high on-current. This requirement directs the desired design space to the lower right corner of SS - $I_{DS}$ plot. 14 nm Si-FinFET is included for reference.

3.9 On-current ($I_{ON}$) vs. on-off current ratio ($I_{ON}/I_{OFF}$) benchmark of experimental demonstrations in literature for (a) p-channel TFET, and (b) n-channel TFET. $I_{ON}/I_{OFF} \geq 10^5$ coupled with $I_{ON} \sim mA/\mu m$ is typical in the state of the art high performance Si-FinFET technology which is also shown for reference. Tunnel-barrier engineering is the key to achieve this desired combination in TFET design. Benefiting from this, complimentary III-V TFETs show remarkable potential for next-generation energy efficient transistors.

4.1 (a) High-K dielectric/III-V semiconductor interface forms the critical interface in a III-V MOSFET; (b) Defects at this interface give rise to characteristics stretch-out and frequency dispersion observed in the capacitance voltage measurements.

4.2 Variations in critical interfaces of Hetero-junction TFET (HTFET) studied in this work.

4.3 (a) Tunnel junction is the first critical interface to TFET operation. In HTFET, this is a hetero-tunnel junction as source and the channel possess different III-V material compositions and this compositional switching occurs over a finite width which is defined as tunnel interface width ($T_W$). Finite $T_W$ spreads out the tunnel barrier on either side of the tunnel junction as indicated in simulated energy band-diagram (b) Junction parameters like tunnel barrier height ($E_{b_{eff}}$) and electric field directly impact tunnel transmission and hence the drain current.

4.4 Atom Probe Tomography (APT) set-up used to characterize the hetero-tunnel-junction in three-dimensional atomic scale resolution.

4.5 (a) Cross-section micro-graph of fabricated III-V HTFET (b) Tunnel junction specimen is characterized using APT with three dimensional ion map showing In ions forming the InGaAs layer and Sb and C ions forming the C-doped GaAsSb layer. The reconstructed volume is $100 \times 110 \times 620 nm^3$. (c) Side-on magnified view of the InGaAs/C-doped GaAsSb interface.
4.6 (a) Calculated composition profile at the InGaAs/GaAsSb interface. Dotted lines indicate the position of 10% and 90% concentration thresholds used to define tunnel interface width ($T_W$) of 2.4 nm; (b) RSM quantification of lattice mismatch in hetero-layer structure.

4.7 Impact of a non-abrupt tunnel interface is studied by assuming tunnel interface width ($T_W$) varying from 0 to 5 nm. (a) transfer-characteristics, (b) switching slope with varying $T_W$, (c) $I_{ON}$ is degraded by 61% whereas on-off current ratio is degraded by 10% due to change in tunnel width from 1nm to 5nm. EOT=0.7 nm, $T_{body}=7$ nm and $L_{g}=20$ nm is used for simulations.

4.8 (a) SIMS measurements depicting excellent abrupt (2 nm/decade) dopant profile at tunnel junction; (b) Sensitivity of HTFET transfer characteristics to source doping concentration ($N_S$). RDF in source is simulated using Sano’s approach [7], with 200 RDF profiles for each nominal $N_S$.

4.9 For optimal designed hetero-junctions with steep doping profiles (as in Fig.4.8a), RDF in source shows weak influence on HTFET threshold voltage and on-current, however significantly degrades the off-state current.

4.10 Traps give rise to significant parasitic conduction mechanisms which contaminate the intrinsic band-to-band tunneling process in TFET, thereby diluting the sub-thermal switching characteristics.

4.11 (a) Temperature dependent transfer characteristics of HTFET exhibit three distinct operation regimes; (b) Improvement in PVCR of NDR peak in low temperature $I_{DS}$-$V_{DS}$ characteristics due to suppression of excess current.

4.12 (a) $I_{OFF}$ is not limited by gate leakage current (b) SRH statistics yield an activation energy of 0.19 eV for $I_{OFF}$. This is in close proximity of mid-tunnel barrier height ($E_{b_{eff}}$).

4.13 Switching characteristics are modeled assuming Frenkel-Poole type of transport. $D_{it}$ contribution from energy levels at 0.55 eV (from $E_c$) at $V_{GS}=0.1$ V to 0.43 eV at $V_{GS}=0.7$ V is detected.

4.14 (a) $I_{ON}$ saturation at low temperature indicates BTBT as dominant transport mechanism in on-state; (b) Sub-0.1eV activation energy estimates onset of BTBT; (c) Temperature dependence of BTBT observed through experiments is explained accurately through temperature dependent non-local BTBT TCAD models.
4.16 Interface trap density profile shown in (a) is used to achieve consistent solution with SRH, TAT and BTBT physical models; (b,c) Breakdown of current-voltage characteristics and switching performance of HTFET. Parasitic charge conduction mechanism assisted through traps significantly dilute sub-thermal switching capability from BTBT.

4.17 (a) High leakage floor due to poor electrostatics from thick tunnel junction width \( T_{body} = 500 \text{ nm} \) aggravated with high SRH and TAT contributions hinders efficient sub-kT/q switching realization even on reducing \( D_{it} \) to \( 5 \times 10^{11} \text{ cm}^{-2} \text{ ev}^{-1} \); (b) HTFET with \( T_{body} = 50 \text{ nm} \) and low \( D_{it} \leq 10^{12} \text{ cm}^{-2} \text{ ev}^{-1} \) exhibits sub-kT/q switching over two decades of \( I_{DS} \), highlighting importance of simultaneous \( D_{it} \) and \( T_{body} \) scaling.

4.18 (a) Significant \( D_{it} \) contribution occurs from HTFET side-walls while integrating gate-stack developed on planar MOSCAP substrates; (a) Sidewall passivation hence becomes a key ingredient to lower \( D_{it} \) in vertical geometry HTFETs.

4.19 (a,b) III-V Hetero-junction TFET (HTFET), using low \( E_{b_{eff}} \), achieves highest electron band-to-band (eB2B) generation at tunnel junction compared to other TFETs. In conjunction with significant tunnel junction electric field (c) possible at low \( V_{DS} \) in HTFET due to abrupt junction design, PBTI evaluation is necessary especially with ultra-thin High-K dielectrics/III-V interfaces.

4.20 Capacitance-Voltage characteristics of \( \text{HfO}_2 \), \( \text{ZrO}_2 \) and \( \text{HfO}_2 + \text{ZrO}_2 \) bilayer gate stacks on n-type \( \text{In}_{0.53}\text{Ga}_{0.47}\text{As} \) substrate are shown for reference. Optimization details are reported elsewhere [8,9].

4.21 (a-c) Transfer and (d-f) Output characteristics of fabricated HTFET. Fabrication process details are reported in [8] and are similar to as described in chapter 3. Three different High-K gate stacks are used for PBTI assessment.

4.22 (a-c) Transfer characteristics of HTFETs with the three gate stacks on application of PBTI stress: \( V_{GS} - V_T = 0.85 \text{V} \) and \( V_{DS} = 0.05 \text{V} \). \( \text{HfO}_2 \) based HTFET shows superior performance. \( \text{HfO}_2 + \text{ZrO}_2 \) based HTFET exhibits excessive SS and \( I_{OFF} \) degradation.

4.23 Percent change in \( I_{OFF} \) (a), SS (b), and \( I_{ON} \) (c) from pre-stress measured values for HTFETs with three gate-stacks.
4.24 (a) Simplified model for off-state current degradation in HTFET from PBTI induced gate-oxide bulk traps and interface-traps; (b) Average switching slope for HfO$_2$ HTFET extracted using this model using PBTI data; (c) Peak transconductance degradation is negligible in HfO$_2$ gate stack and worst in HfO$_2$+ZrO$_2$ bi-layer stack.

4.25 PBTI induced $V_T$ shifts, extracted using constant current method. Threshold current is calculated from pre-stress transfer-curves, separately for each gate stack. HTFET based on HfO$_2$ exhibits power law dependence of $\Delta V_T = \alpha \times t^n$ with $n = 0.14$. ZrO$_2$ based HTFET show partial or no power law dependence due to off-current and switching slope degradation from PBTI induced high interface trap density.

4.26 III-V HTFET shows improved PBTI lifetime than III-V FinFET over entire stress voltage range.

4.27 Key learnings from interface characterization for improving TFET electrical performance.

4.28 HTFET TCAD numerical simulation set-up.

4.29 (a) Simulated Transfer characteristics of complementary HTFET with models described in Fig.4.28; (b) Energy vs. delay benchmark of a FO1 inverter comparing 22nm Si FinFET and III-V HTFET with 1% switching activity factor, at different operating voltages.

4.30 Device layout of (a) vertical P-HTFET and (b) vertical N-HTFET; (c) Layout illustration of a 9-metal-track standard cell library design. Layout area is determined by $9N \times \text{Gate-pitch} \times 9\text{metal-pitch}$. N is number of gate-pitches in the lateral direction. Inverter layout of (d) Si FinFETs at a maximum fin number of 4 and (e) proposed complementary vertical HTFETs; (f) Layout induced device drive strength enhancement (effective device width at a given device area) comparing the INV1 using 22 nm planar MOSFETs, 22 nm FinFETs and 22 nm vertical HTFETs.

5.1 (a) Steep switching characteristics of HTFET, and (b) higher $g_m/I_{DS}$ compared to subthreshold Si-FinFET are favorable for both digital and analog circuit design.
5.2 (a) Threshold voltage fluctuation $\Delta V_{Th}$ from RTN exceeds Random Dopant Fluctuation (RDF) induced $\Delta V_{Th}$ at sub-14 nm process technology nodes; (b) Calibration of TCAD RTN amplitudes against experimental results reported for p-Si-FinFET [88]. Inset: the Double-gate (DG) simulation structure; (c) Relative RTN amplitude dependence on trap depth and location along the channel for TFET and FinFET.

5.3 (a) Single charge trap reduces electric field near source-channel junction. The reduction in electric field is approximated assuming an effective charge $Q_{eff}$ in channel and applying Gauss Law; (b) Analytical model (Eqn. 5.1) shows good agreement with the TCAD numerical simulations for $V_{GS}$ in range of 0.1V-0.4V.

5.4 (a) Flicker noise is caused by trapping/emission of carriers by trap states in oxide. (b) In TFET the drain current is controlled by the tunneling distance of carriers at the source-channel junction ($L'$).

5.5 (a) Shot noise across tunnel junction can enhance due to individual contributions from forward and reverse tunnel currents; (b) Representation of flicker, shot, and thermal electrical noise models (noise current sources) implemented at transistor level.

5.6 (a) TFET RTN does not increase inversely with gate length scaling as tunneling distance of carriers shows weak dependence on gate length; (b) At 100KHz, TFET provides a $\sim 1.5 \times$ less input referred noise ($S_{V_G}$) from higher intrinsic gain ($g_m/I_D$); (c) At 10GHz, shot noise causes the input referred noise of TFET to cross-over and exceed the input referred noise of FinFET.

5.7 Differential amplifier (Diff-Amp) with active load: TFET versus FinFET. (a) Schematic and ac response; (b) Specifications of Diff-Amp design; (c) Input referred noise dependence on frequency; (d) Gain, input noise, and power dissipation of the design at different bias currents.

5.8 10-Transistor (10T) based ST2 SRAM: (a) Schematic in read mode; (b) Read Noise Margin (RNM) in presence of RTN in 1024 possible cell types; Worst case simulated RTN RNM for (c) FinFET, and (d) TFET.

5.9 Percent change in ST2 SRAM: (a) Read Noise Margin, and (b) Write Noise Margin indicates that TFET ST2 SRAM is more immune to RTN induced variation.
5.10 (a) RNM of 10T ST2 SRAM compared against 6T SRAM; (b) Average power consumption of 256 × 256 SRAM array with 5% activity factor; (c) Read-access delay; Note for TFET SRAM, plots for 2 different trap locations: trap at tunnel junction and at 2 nm away from tunnel junction (worst case RTN) are shown for reference; (d) Performance at Vcc-min limit with worst case RTN

6.1 DC measurement: (a-b) Transfer, (c) Switching and (d) Output characteristics of NTFET with 3nm-thick ZrO$_2$ gate dielectric. High gate-source current is observed, still efficient drain current modulation is achieved.

6.2 (a-c) Scaling of body thickness achieved to N$_2$/Cl$_2$ etch chemistry based dry etch optimized at 160°C. (d) P-i-n diodes with T$_{body}$ ∼ 50 nm fabricated using this method.

6.3 Digital etch is developed to achieve self-limiting etch of In$_{0.65}$Ga$_{0.35}$As layer to form HTFET sidewalls with minimal D$_{it}$.

6.4 (a) Gate stack optimization for GaAs$_{0.35}$Sb$_{0.65}$ channel p-type HTFET; (b) Lower band-edge D$_{it}$ is achieved however mid-Gap D$_{it}$ is still significant.

6.5 Hetero-junction PTFET fabricated on wafer (a) with gate stack from Fig. 6.4 using TFET fabrication procedure as described in Chapter 3; (b) Transfer, (c) Switching and (d) Output characteristics of PTFET.

6.6 Group IV semiconductors show lower mid-gap D$_{it}$ and higher conduction band DOS over III-V compound semiconductors.

6.7 Group IV semiconductors have large indirect band-gaps which results in inferior tunnel transmission compared to III-V semiconductors which possess smaller and direct band-gap. Efforts to reduce Group-IV semiconductor band-gap and turning them into direct band-gap materials (e.g., by introducing Sn in Ge) is necessary to harness their low D$_{it}$ advantage for high performance TFET design.

6.8 Ge$_{1-X}$Sn$_X$ band-structure calculated from first-principles DFT is combined with TCAD numerical simulation to model Ge-based p-TFET. Both direct as well as indirect BTBT are modeled.

6.9 Ge$_{1-X}$Sn$_X$ energy band-gap along with electron effective mass computed from DFT.

6.10 **Homo-junction Ge p-TFET**: Transfer ($I_{DS}$-$V_{GS}$) and switching (SS-$I_{DS}$) characteristics from direct and indirect BTBT.

6.11 **Homo-junction Ge$_{0.90}$Sn$_{0.10}$ p-TFET**: Transfer ($I_{DS}$-$V_{GS}$) and switching (SS-$I_{DS}$) characteristics from direct and indirect BTBT.
6.12 **Hetero-junction Ge/Ge\textsubscript{0.90}Sn\textsubscript{0.10} p-TFET**: Transfer (I\textsubscript{DS}-V\textsubscript{GS}) and switching (SS-I\textsubscript{DS}) characteristics from direct and indirect BTBT. .......................................................... 104

6.13 (a) I\textsubscript{DS}-V\textsubscript{GS} characteristics of complimentary TFETs using Ge/Ge\textsubscript{0.90}Sn\textsubscript{0.10} hetero-junctions; (b) I\textsubscript{60} benchmark of Group IV TFETs indicates that Ge/Ge\textsubscript{1-X}Sn\textsubscript{X} hetero-junctions are most suitable for high performance TFET design; (c) Hetero-junction Ge/Ge\textsubscript{0.90}Sn\textsubscript{0.10} p-TFET outperforms Si and III-V p-TFET at state of the art High-K/channel interface D\textsubscript{it}. ......................................................... 105
List of Tables

3.1 Benchmark of Si and III-V TFETs [8]. $V_{ON} (V_{MIN})$ corresponds to the gate voltage at $I_{ON} (I_{MIN})$. $|V_{ON}|$ is limited to 1.5V from $|V_{MIN}|$ 38

4.1 Measured lattice constants, dopant concentrations and layer compositions for the NTFET hetero-stack. Atomic percentage and atomic concentration are denoted by $at\%$ and $at/cm^3$ respectively. 49

A.1 Gate stack parameters for complimentary TFETs 109

C.1 Parameters for phonon assisted indirect BTBT in Group IV TFETs computed from DFT. 118
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Chapter 1  
Introduction

1.1 Motivation

Self-powered mobile electronics capable of performing complex tasks is going to play an increasingly important role in our modern society. It is of vital significance to leverage the latest advancements in emerging nanoscale devices to develop energy efficient circuits to satisfy this design space (Fig. 1.1). Since past few decades, meeting power and performance requirements in electronic-circuits has been addressed through continual scaling of power supply voltage and physical dimensions of silicon MOSFET, which forms the fundamental constituent of the circuit. In particular, integrated circuits have followed the guidelines of constant

![Figure 1.1: (a) Data, sensors and connectivity form the fundamental blocks of next-generation electronics. (b) The design approach focuses on processing, power and reliability aspects to achieve holistic implementation.](image-url)
electric-field scaling presented by Robert Dennard in his seminal paper [10]. Dennard scaling prescribed that transistor device dimensions (like oxide thickness, channel length) and operating voltage could be scaled by a constant factor to derive simultaneous benefits in switching speed, power dissipation along with transistor integration density. The opportunity extended by Dennard scaling fueled Moore’s law which delivered approximately $2\times$ increase in transistor density with every new technology generation [11].

Present microprocessors pack billions of transistors yielding to the unrelenting demand for performance. However on the same side it faces huge power budget constraint arising from not only the temperature management aspect of the chip, but also from providing energy efficient computing to cater the requirements of mobile platforms (Fig. 1.2a). The power supply voltage ($V_{cc}$) scaling which has been aggressively used to keep a check on power dissipated by MOSFETs, is now facing limitation due to lack of threshold voltage scaling [12] as shown in Fig. 1.2b. Subthreshold power density has become extremely critical in present generation MOSFETs [1], as shown in Fig. 1.2c. Further reduction in the threshold voltage of the Si-MOSFET is not possible without exponentially increasing the off-state current which is detrimental for energy efficiency.
As the benefits of conventional scaling approach physical limits, techniques like introducing strain to alter semiconductor band-structure and carrier effective mass along with band-gap engineering are in research to maintain MOSFET performance as predicted by Moore’s law. The improvements in microprocessor performance are now also fueled from software side by use of hyper-threading and multicore. The transistor aspect of microprocessor still in search for an ultra-low power solution as we approach closer to sub-10 nm process technology node. Future emerging devices aim to achieve both low threshold voltage and transport enhancement through judicious use of novel materials, strain and band-gap engineering, etc. (Fig. 1.3a).

1.1.1 Why Tunnel FET for low power energy efficient applications?

Tunnel FET (TFET) have garnered significant interest as they can provide sub-60mV/decade switching at room temperature. TFET differs from MOSFET primarily in the mechanism through which the majority carriers are injected into the channel (refer Fig. 1.3b). In MOSFET, the gate electrode modulates the source to channel barrier which induces the thermionic emission of carriers from the source into the channel region. In contrast, with a tunnel FET, carrier injection into the channel comes from inter-band tunneling from the source to channel region. The great merit of inter-band tunneling is that it filters out the high energy carriers in the Fermi-Dirac distribution that are present in the valence band of the source region. Thanks to this carrier ‘cooling’ effect, TFET can achieve sub-$kT/q$ switching to off-state.

Figure 1.4 shows performance of energy-delay metric of a 32 bit adder implemented through various beyond CMOS devices [2]. CMOS devices are also benchmarked for reference. The lower-left corner is the preferred design space. As observed from Fig. 1.4, Hetero-junction TFET is a strong candidate for post CMOS device solution, providing high performance at low power consumption.
1.1.2 Why III-V compound semiconductor based Hetero-junction Tunnel FET?

With a tunnel FET, careful selection of the material system is needed to ensure that when this device is operated at a very low voltage, it outperforms a MOSFET. The natural choice of material for making a tunnel FET is silicon, due to its high-quality native oxide, and the opportunity to produce the device in a state-of-the-art foundry. Silicon’s native oxide enables a high-quality interface with a low density of interface states it is $10^{11} \text{cm}^{-2} \text{eV}^{-1}$ or less and as a consequence, many groups have been able to report a device with very steep switching. However, these transistors suffer from a very low on-current, due to the large effective height of the tunnel barrier seen by carriers tunneling from the source to the channel. This current is so low that it rules out the use of silicon tunnel FETs for logic applications.

Turning to other semiconductor materials is no guarantee of success, either. With all homo-junction tunnel FETs there is a uniform band-gap in the source, channel and drain regions. This means that the effective height of the barrier equals that of the band-gap as shown in Fig. 1.5a. The on-current can be increased by reducing the band-gap, but the price to pay for this is the aggravation of parasitic leakage mechanisms - they include Shockley-Read-Hall generation-recombination within the reverse biased p-i-n diode, and band-to-band-tunneling leakage on the
Figure 1.4: Benchmarking of energy-delay performance of 32 bit adder implemented through beyond-CMOS devices (adapted from [2]). CMOS reference is also shown for comparison. Hetero-junction TFET (HetJTFET in the figure) is one of the most promising candidate for beyond CMOS logic.

The solution is to switch from a homo-junction to a hetero-junction. With the latter form of FET it is possible to reduce the height of the tunnel barrier beside the source channel junction, while maintaining large band-gaps in every other region (Fig. 1.5a). Armed with this architecture, tunnel FETs can realize a high on-current and a steep switching slope.

Several material systems have been explored in the pursuit of a tunnel FET for next-generation logic. Devices made with the combination of silicon and SiGe, and germanium and GeSn, suffer from a significant trade-off between on-current and the switching slope. To implement energy efficient complementary logic, this trade-off must be addressed while using a material system that is ideally capable of producing high-performance p-type and n-type devices. It is for that reason that we work with arsenide-antimonide hetero-junctions, because they offer a wide range of lattice-matched, compositionally tuneable effective tunneling barrier heights as
Figure 1.5: (a) Energy band diagram showing effective tunnel barrier height ($E_{b_{\text{eff}}}$) reduction in heterojunction TFET; (b) Extracted band-alignment for lattice matched GaAs$_{1-x}$Sb$_x$/In$_y$Ga$_{1-y}$As hetero-junctions. Wide range of $E_{b_{\text{eff}}}$ is obtained [3].
Figure 1.6: Numerically simulated $I_{DS}-V_{GS}$ curves [3] for ultra-thin body double gate Tunnel FET ($L_g=32\text{nm}$, EOT=1nm) with (a) Homo-junction TFET; and (b) Hetero-junction TFET. Si-MOSFET is shown in both graphs for comparison.

shown in Fig. 1.5b making them suitable for making n- and p-type tunnel FETs. As observed from Fig. 1.6b, Hetero-junction TFET enables high on-current along with high $I_{ON}/I_{OFF}$ ratio for $V_{cc} \leq 0.5\text{V}$, promising further $V_{cc}$ scaling suitable for future low power applications.

One of the biggest challenges associated with making any class of III-V transistor for logic applications is that it is tricky to engineer a high-quality interface between the compound semiconductor channel and the gate dielectric. Native oxides of III-Vs are vastly inferior to those associated with silicon, and this prevents the creation of a pristine interface with the channel. The problem stems from a III-V surface that is very reactive, with dangling bonds giving rise to a high density of interface states (they can hit $10^{14}\text{cm}^{-2}\text{eV}^{-1}$). These imperfections severely limit the ability of the gate field to effectively modulate the source-channel tunnel barrier. In turn, this degrades the performance of the tunnel FET.

In the last five years, however, research related to the gate stack has borne much fruit, with interface quality improving, thanks to high-quality surface treatments. These surface treatments consist of a combination of ex-situ wet-etch clean and in-situ pre-ALD $H_2$ or $N_2$ plasma based clean. They provide efficient removal of native oxide along with achieving high-quality surface passivation. Drawing on this success, we form InGaAs channel nFETs with excellent interfaces and a low density of interface traps, and p-type GaAsSb siblings with significantly improved
1.1.3 Complimentary TFETs: State of the Art

Experimental demonstrations of TFET have been reported in both Group IV and Group III-V based semiconductors. Figure 1.7a presents the switching slope (SS) vs. drain current (I_{DS}) for p-channel TFETs reported in literature. This plot is particularly useful because it gives collective information on minimum SS, the highest current at which 60 mV/decade SS is achieved (I_{60}), along with the I_{DS} range through which SS below 60 mV/decade is obtained [13]. The requirement of sub-kT/q switching (<60 mV/decade at room temperature) coupled with high on-current directs the desired design space to the lower right corner of SS - I_{DS} plot. It is evident that high-performance PTFET demonstrations are dominated entirely by Group IV semiconductors: primarily from Si, SiGe and Ge based material systems. This is expected, as p-channel devices in III-V material system suffer significantly from low on-current resulting from a low conduction-band density-of-states [14]. This becomes a severe limitation especially in a homo-junction TFET design. In similar context, the on-current is also a limitation in silicon TFETs too as a consequence of large tunnel barrier height which is same as silicon band-gap [15,16]. Additional alternatives have been explored to enhance the tunnel current, like integration of Si with Ge, use of strain engineering, along with Ge and GeSn based TFET designs [17–19]. However the results are mixed and only few experimental demonstrations feature the balance of high current-magnitude together with low switching slope that can be positioned on this SS - I_{DS} benchmark. In general, Si-TFETs exhibit sub-kT/q SS over a considerable range of I_{DS} leveraging from a high quality interface between Si channel and SiO₂ or high κ-gate dielectric.

Figure 1.7b presents the SS vs. I_{DS} benchmark for n-channel TFETs demonstrated in literature. III-V TFETs particularly using InGaAs and InAs have shown higher on-currents as a benefit of smaller band-gap. However achieving efficient sub-kT/q switching slope has been a challenge due to high density of defect states present at high-k gate dielectric and III-V channel interface. Reports of subthermal SS has been primarily at extremely low I_{DS} [20] or only at low V_{DS} [21]. Hetero-junction III-V TFETs like InGaAs/GaAsSb have achieved the highest on-currents thus far [22]. There does not appear to be a fundamental limitation in these systems
to achieving sub-thermal swings and these numbers can be expected to improve with gate stack optimization, better electrostatics with self alignment, and better passivation, which is the aim of this research work.

1.2 Organization of this thesis

Research contribution from this work are presented in the following structure:

- Chapter 2 is dedicated to high-κ gate dielectric/III-V channel gate stack engineering. High-performance gate-stacks with best in class Equivalent Oxide Thickness (EOT) are demonstrated on both GaAs$_{1-x}$Sb$_x$ and In$_y$Ga$_{1-y}$As channel substrates for p-channel and n-channel TFETs respectively.

- Chapter 3 describes TFET device fabrication sequence along with an in-depth electrical characterization of TFETs. We present first demonstration of an all III-V semiconductor system based complimentary hetero-junction TFETs that can operate at a low voltage ($V_{DS} \leq 0.5V$) and deliver a high on-current with steep switching performance.

- Chapter 4 is focused on characterization of semiconductor interfaces critical to TFET performance. To improve TFET on-current we characterize the tunnel junction using 3D-atom probe tomography to arrive at optimal doping and composition parameters for the tunnel junction. We also performed temperature and electric-field dependent high-κ/III-V channel interface characterization coupled with calibrated TCAD simulations to identify key bottlenecks towards efficient switching performance. Moreover, using accelerated stress measurements on TFETs we demonstrate TFET can out-perform conventional III-V FinFETs even in long term reliability aspect.

- Chapter 5 examines the elements of Hetero-junction TFET (HTFET) based circuit design. This was performed by employing TCAD and Spice simulations calibrated to experimental TFET characteristics. We evaluated digital/analog circuits as well as SRAM memory circuits based on TFETs and compared to corresponding CMOS implementations. Key design differences in HTFET design compared to conventional Si-FinFET are highlighted and performance comparison is performed.
Figure 1.7: Switching slope (SS) vs. drain current ($I_{DS}$) benchmark of experimental demonstrations in literature for (a) p-channel TFET, and (b) n-channel TFET. For energy efficient high performance logic design, sub-$kT/q$ switching (<60 mV/decade at room temperature) is needed coupled with high on-current. This requirement directs the desired design space to the lower right corner of SS - $I_{DS}$ plot. 14 nm Si-FinFET is included for reference.
• Chapter 6 summarizes the contributions of present work and presents a course for further improving TFET performance.
2.1 Introduction

Realizing high performance gate-stack on III-V materials is not a recent endeavor. III-V materials have been acknowledged as potential candidates for enhancing device performance over past five decades. However in comparison to the widespread use of Si-based devices in the semiconductor industry, devices based on III-V materials have only occupied certain specific segments.

The primary impediment towards comprehensive adoption of III-V materials in IC industry is the lack of a high quality gate dielectric for III-V substrates similar to SiO$_2$ for silicon substrates. Essential desired features in a gate dielectric to enable high performance MOSFETs are [23]: (a) a thermodynamically stable interface with the channel semiconductor with low interface defect density ($D_{it}$), (b) a high dielectric constant to enable EOT scaling, and (c) substantial band offsets with the channel semiconductor for low gate leakage current. Out of these three requirements, achieving a low $D_{it}$ interface with high-$\kappa$ gate dielectrics has been extremely challenging on III-V materials [4,24,25].

Compared to silicon, the native oxides of III-V semiconductors are vastly inferior, primarily due to their thermodynamic instability and unacceptably high interface trap density. In addition, the III-V semiconductor surface exhibits drastically different behavior compared to silicon from underlying complex surface reconstruction mechanisms as depicted in Fig. 2.1 [4,5]. The resulting surface is generally highly
reactive due to the presence of unsaturated bonds, anti-site defects, incomplete dimers etc. Each such defect state can form electrically active traps within the semiconductor band-gap. These trap states are not only present prior to high-κ dielectric deposition, but also can be generated during the deposition process itself. High interface trap densities prevent efficient Fermi level movement through the semiconductor band-gap or even cause Fermi level pinning. As a result, the ability of gate field in modulating the tunnel barrier and hence to control the charge injection from source to the channel region degrades thereby worsening both the switching characteristics as well as the on-current of TFET. Note this interface is common concern for both III-V MOSFETs and III-V TFETs. Engineering scaled high-κ gate dielectrics with high quality electrical interfaces with arsenide (As) and antimonide (Sb) channels is fundamental towards realizing efficient complimentary III-V TFET logic performance at ultra-low supply voltage applications.

### 2.2 III-V surface preparation techniques

Requirement of low Equivalent Oxide Thickness (EOT) to enhance the electrostatic control on the channel mandates the elimination of low-κ layer formed by native oxides at the interface of III-V channel and gate dielectric. The channel material for n-type TFETs is In(Ga)As. In(Ga)As semiconductor surface shows distinct presence of As$_2$O$_3$ and As$_2$O$_5$ [24], along with oxidation states of Ga$^{3+}$ and Ga$^{5+}$ as well as...
other oxide species such as Ga$_2$O [26]. On the other hand, the channel material for p-type TFETs is Ga(As)Sb. Ga(As)Sb surface has native oxides comprising of Ga$_2$O$_3$ and Sb$_2$O$_3$, Sb$_2$O$_5$ besides trace of elemental Sb [27–29]. An in-situ process with III-V native oxide removal followed by high-$\kappa$ dielectric atomic layer deposition (ALD) can eliminate the formation of low-$\kappa$ interfacial layer. Atomic layer deposition technique (ALD) is already a well-established process for dielectric deposition in semiconductor industry.

ALD HfO$_2$ and ZrO$_2$ are promising high performance gate dielectrics due to their higher dielectric constant favorable for EOT scaling. Realizing a TFET with high $I_{ON}$ and low $I_{OFF}$ relies significantly on the quality of high-$\kappa$ integration on III-V channels. Various dielectric intergation techniques are reported in literature focused on surface preparations prior to ALD that remove native oxides and passivate unsaturated bonds in order to ensure the best possible interface [30]. These approaches commonly involve native oxide removal using wet etches, such as HCl [27,31], HF [32], (NH$_4$)$_2$S [33], and NH$_4$OH [32,34]. However, due to the rapid re-oxidation of the III-V surface, additional interface cleaning methods are generally employed.

Interestingly, several recent gate stack demonstrated on III-V suggest that use of ALD precursor trimethylaluminum (TMA) can "self-clean" interfacial native oxides from III-V surfaces [29,34–36]. For improved efficacy this treatment is typically preceded by a wet chemical etch that removes the bulk of the native oxide. Moreover, hydrogen (H$_2$) and nitrogen (N$_2$) plasma based surface-clean have been identified as a promising candidate for efficient low temperature oxide removal alternative [37,38]. Particularly hydrogen (H$_2$) and nitrogen (N$_2$) plasma treatments in ultra-high vacuum can result in high quality, low D$_{it}$ and native oxide-free InGaAs and GaSb surfaces [30,36,39]. These observations suggest the usefulness of plasma treatments for surface preparation prior to ALD. To maximize the benefit from plasma-based surface clean, a rigorous optimization on III-V channels is needed, for both NTFET and PTFET. Hence, we first develop the individual optimized gate-stacks on GaAs$_{0.35}$Sb$_{0.65}$ substrate for PTFET and on In$_{0.65}$Ga$_{0.35}$As substrate for NTFET. We use a combination of wet-etch clean along with subsequent use of an in situ H$_2$ and N$_2$ plasma based surface-treatment prior to high-$\kappa$ ALD to obtain a best electrical interface quantified through capacitance-voltage (C-V) measurements.
2.3 Gate Stack on Sb-channel PTFET

The Fermi level movement is especially hindered in Sb-channel based PTFET due to the presence of high mid-gap D_{it}. GaSb interfaces using Al₂O₃ gate dielectric were demonstrated with Fermi level unpinning [29]. However low dielectric constant of Al₂O₃ (κ = 9) limits equivalent oxide thickness (EOT) scaling. Efficient removal of native oxide is essential prior to high-κ dielectric deposition on GaSb surface. Combining wet chemical ex-situ clean and in-situ H₂ plasma clean to remove native oxide, HfO₂/p-GaSb interfaces with EOT of 0.8 nm have been recently demonstrated with efficient gate modulation [40]. An equivalent treatment on mixed arsenide/antimonides is needed for GaAs₀.₃₅Sb₀.₆₅ channel PTFET, which is presented in this work.

2.3.1 GaAs₀.₃₅Sb₀.₆₅ MOSCAP Fabrication

A 300-nm-thick epitaxial p-type (doping 10¹⁷ cm⁻³) GaAs₀.₃₅Sb₀.₆₅ film was grown on a lattice mismatched InP substrate employing a linearly graded Al₁₋ₓInₓAs metamorphic buffer layer by molecular beam epitaxy (MBE). Samples were degreased in acetone and methanol for 10 min each, and rinsed in isopropyl alcohol (IPA) for 5 min. Wet chemical clean was performed by 40s dip in hydrochloric acid (HCl) and water solution (HCl:H₂O=1:1) in order to remove the native oxide. The samples were then immediately loaded into the ALD-150LX reactor (Kurt J. Lesker Co.) equipped with a remote 13.56 MHz RF inductively coupled plasma (ICP) source (Fig. 2.2a). After pump down and loading the samples into the ALD chamber, a 100W RF H₂ plasma surface treatment was performed with H₂ and Ar gas flows of 3 and 110 sccm respectively and a chamber pressure of 1 Torr. H₂ plasma treatments have been shown to be effective in reducing native oxide prior to high-κ ALD [41,42]. The substrate temperature during H₂ plasma surface treatment was set to 110 °C. Following the H₂ plasma surface clean, the GaAs₀.₃₅Sb₀.₆₅ surfaces were exposed to ten 50 ms long prepulses of trimethylaluminum (TMA) followed by ten 50 ms long pulses of H₂O, which hydroxylates the surface and facilitates subsequent nucleation of high-κ dielectric. The substrate temperature was ramped to 250 °C and a 3.5-nm-thick HfO₂ was deposited using alternate cycles of tetrakis(dimethylamino)hafnium [Hf(NME₂)₄] and H₂O. Individual steps
in this entire PEALD process are summarized on a single illustration presented in Fig. 2.2b. Post high-$\kappa$ deposition, an in-situ forming gas anneal (FGA) was performed at 350°C for 20 min, with an H$_2$/Ar ambient (40 sccm of H$_2$ and 110 sccm of Ar). A thermal evaporator was used to deposit 70-nm-thick Ni gate metal contacts through a shadow mask.

### 2.3.2 High-$\kappa$/GaAs$_{0.35}$Sb$_{0.65}$ Interface Characterization

Capacitance-voltage (CV) and conductance-voltage (GV) measurements were performed at room temperature with frequency range from 70 kHz to 1 MHz using Agilent 4284A LCR meter. For PTFET with GaAs$_{0.35}$Sb$_{0.65}$ substrate, optimized gate stack process leads to accumulation capacitance density ($C_{acc}$) of 2.6 $\mu$F/cm$^2$ (Fig. 2.3a). The maximum capacitance density achieved is still limited indicating the presence of persistent interfacial oxide layer. Besides, large frequency dispersion is observed in the depletion region of CV characteristics. This is attributed to significantly pronounced mid-gap $D_{it}$, which becomes apparent in $D_{it}$ vs. band-gap energy profile extracted using Terman method ($D_{it} = 10^{14}$cm$^{-2}$eV$^{-1}$) depicted in Fig. 2.3b. Gate leakage current at 1V is 100mA/cm$^2$ (shown in the inset of Fig. 2.3b).
Figure 2.3: (a) CV characteristics of p-type GaAs$_{0.35}$Sb$_{0.65}$ MOSCAPs with 3.5 nm HfO$_2$ with 1.5 min H$_2$ plasma surface clean; (b) D$_{it}$ extraction using Terman method. Gate leakage is shown in the inset.

which meets the requirement of ITRS 2013 for low power logic applications.

In order to further improve the accumulation capacitance density and lower D$_{it}$, it is imperative to achieve effective removal of interfacial native oxide. We explore further optimization of parameters in H$_2$ plasma surface-treatment specifically with regard to substrate temperature. Substrate temperature has direct impact on the rate of desorption of native oxides. However a high substrate temperature accelerates reduction of Sb$_2$O$_3$ into elemental Sb [29], particularly for temperatures exceeding 200°C. Enhanced rate of thermal desorption of Sb-oxides is also observed at such elevated temperatures [43, 44]. Figure 2.4 illustrates the result of substrate temperature change during H$_2$ plasma surface treatment. It is observed that performing plasma surface clean at high temperature (200°C) results in high maximum accumulation capacitance density ($C_{MAX}$) albeit it also produces significantly degraded frequency dispersion in the depletion region of CV characteristics. This dispersion manifests as a hump-like formation is attributed to rise in mid-gap D$_{it}$ owing to increased formation of elemental Sb. In contrast, using an intermediate plasma surface clean temperature of 150°C, the mid-gap D$_{it}$ hump in C-V characteristics is remarkably suppressed. Moreover the $C_{MAX}$ is also benefited compared to 110°C surface clean, as an advantage resulting from thermal assisted desorption of interfacial native oxides prior to HfO$_2$ gate dielectric.
Figure 2.4: Impact of change in substrate temperature: (a) 110°C, (a) 250°C and (a) 150°C, during pre-ALD H$_2$ plasma surface treatment on CV characteristics of GaAs$_{0.35}$Sb$_{0.65}$ MOSCAPs. Gate dielectric HfO$_2$ thickness (3.5 nm) and H$_2$ plasma clean duration (1.5 min) is kept constant at previously optimized values. Substrate temperature of 150°C is optimal for driving desorption of native oxide producing high accumulation capacitance density. It still maintains low mid-gap D$_{it}$ due to lower thermal budget of the H$_2$ plasma surface treatment process.

deposition.

The extraction of density of interface traps and associated trap time constants is performed subsequently. First we present the admittance measurement for the final optimized p-channel gate stack on GaAs$_{0.35}$Sb$_{0.65}$ MOSCAPs for frequencies down to 10KHz. Optimization of the H$_2$ plasma surface clean temperature at 150°C with 3.5 nm thick HfO$_2$ gate dielectric leads to the thinnest EOT=0.8 nm with lowest mid-gap D$_{it}$ (Figs. 2.5a and 2.5b) reported before on GaAs$_{0.35}$Sb$_{0.65}$ substrates. The maximum accumulation capacitance density achieved is improved to 3.5 µF/cm$^2$ and the corresponding equivalent oxide thickness (CET) is 1.2 nm. The difference between capacitance equivalent thickness and EOT arises from lowering of the semiconductor capacitance due to quantum capacitance [45] and centroid capacitance [46]. Quantum capacitance is outcome of fermi level reaching to higher sub-bands post-energy band splitting from quantum confinement, which is highly significant in material systems with low density of states effective mass. Quantum confinement can result from energy band-bending at channel-to-gate oxide interface. Centroid capacitance on the other hand originates from the particular
extended profile of the inversion layer charge distribution in the channel region. Low conduction band density of states in III-V material system can aggravate both of these capacitances thereby limiting semiconductor capacitance [47].

A noticeable hump in the depletion region is indicative of mid-gap $D_{it}$ which is still appreciable $\sim 10^{14} cm^{-2} eV^{-1}$ as observed from Fig. 2.5b. Maximum gate leakage current density is measured to be 20mA/cm$^2$ which is well within the requirement of state of the art CMOS technology ($\sim 1A/cm^2$). Figure 2.5c depicts the the normalized conductance map as a function of gate voltage and frequency. The normalized conductance peak values can provide an estimate of $D_{it}$ by multiplication with a factor of 2.5. Reading from the map, we observe a mid-gap $D_{it} \sim 10^{14} cm^{-2} eV^{-1}$ consistent with value obtained from Terman method. Moreover, these maps also reveal how efficient the Fermi level movement is across the band-gap with application of gate bias. A narrow and vertical trace of conductance peak maximum suggests larger band bending and hence efficient Fermi level movement in response to a change in gate bias. We observe from Fig. 2.5c that the conductance peak maximum trace spans over a wide range of gate voltage through depletion region (gate bias of 0.9V and onwards) and indicates sluggish movement to mid-gap. This sluggish movement of fermi level is an outcome of dominant mid-gap $D_{it}$ with slow characteristics response time. We extract the characteristics response time associated with these interface traps using the modified conductance method [6] which models both the CV and GV characteristics simultaneously besides accounting for gate leakage currents. The result of this analysis is plotted in Fig.2.5d which illustrates the variation of trap response time versus band-gap energy. This evidently quantifies the intrinsic slow-response time of mid-gap traps at high-\(\kappa\) HfO$_2$ gate dielectric and GaAs$_{0.35}$Sb$_{0.65}$ semiconductor interface.

2.4 Gate Stack on As-channel NTFET

NTFET is based on In$_{0.65}$Ga$_{0.35}$As channel on which high-\(\kappa\) gate stack development has achieved significant success [39, 48]. High-\(\kappa\) gate dielectrics with pristine interfaces with In$_{0.53}$Ga$_{0.47}$As substrates with midgap $D_{it}$ in the range of mid $10^{12}$ cm$^{-2}$eV$^{-1}$ have been recently demonstrated in literature [9, 48]. We aim to achieve low $D_{it}$ interface coupled with EOT scaling suitable for high performance TFET design. Extremely scaled gate stacks enhance the gate control on the tunnel junction
Figure 2.5: Optimized gate stack on p-type GaAs$_{0.35}$Sb$_{0.65}$ substrate for PTFET: (a) Capacitance voltage characteristics (3.5nm thick HfO$_2$) (b) $D_{it}$ vs. band-bending profile extracted through Terman method. Inset shows gate leakage current density (c) Normalized parallel conductance map with dotted line trace showing movement of the conductance peak maximum (d) Trap response time versus band-gap energy extracted using modified conductance method [6].
which is essential for high on-current and steep switching characteristics of TFET.

### 2.4.1 In$_{0.53}$Ga$_{0.47}$As MOSCAP Fabrication

For NTFET with In$_{0.65}$Ga$_{0.35}$As channel we first explore 3.5 nm thick HfO$_2$ high-$\kappa$ gate dielectric. Substrates for MOSCAP consisted of 300-nm-thick, n-type (doped $10^{17}\text{cm}^{-3}$) In$_{0.53}$Ga$_{0.47}$As layers grown by molecular beam epitaxy on InP substrate. The gate dielectric optimization steps are similar to those reported elsewhere [39]. Samples were cleaned in buffered HF for 3 min to remove native oxide before they were transferred into the ALD-150LX reactor (Fig. 2.2a). At a substrate temperature of 250°C, an alternating pre-cleaning sequence of *in-situ* a 125W RF N$_2$ plasma exposure optimized to 5 seconds followed by 40 ms long prepulse of trimethylaluminum (TMA) is performed for 5 cycles at a chamber pressure of 1 Torr to achieve low D$_{it}$ interface. The cyclic N$_2$ plasma/TMA treatment has been reported to provide superior interface passivation compared to H$_2$ plasma treatments on In$_{0.53}$Ga$_{0.47}$As substrates [39]. Following the N$_2$ plasma surface clean, ten 50 ms long pulses of H$_2$O, were used to hydroxylate the surface for subsequent high-$\kappa$ ALD. Lastly, 3.5-nm-thick HfO$_2$ was deposited using alternate cycles of tetrakis(dimethylamino)hafnium [Hf(NME$_2$)$_4$] and H$_2$O. Thermal evaporation of 70 nm thick Ni metal is performed through a shadow mask to form the gate contacts. The samples underwent a post-metal deposition anneal at 350°C for 15 min in flowing forming gas (100 sccm of H$_2$ and 100 sccm of Ar).

### 2.4.2 High-$\kappa$/In$_{0.53}$Ga$_{0.47}$As Interface Characterization

The capacitance-voltage (CV) characteristics of thus fabricated n-type In$_{0.53}$Ga$_{0.47}$As MOSCAPs, as measured using Agilent 4294A impedance analyzer with frequency ranging from 70 kHz to 1 MHz, are shown in Fig. 2.6a. High accumulation capacitance density of 3.0 µF/cm$^2$ with an EOT~0.85nm is obtained (Fig. 2.6a) along with relatively moderate average D$_{it}$ in the range of $10^{13}\text{cm}^{-2}\text{eV}^{-1}$ (Fig. 2.6b) compared to PTFET gate stack. The gate leakage current is well-controlled and measured to be 100mA/cm$^2$ at 1V.

We further investigate on scaling the EOT further to improve the accumulation capacitance density as it directly governs the on-current of TFET. Additional EOT scaling can be realized by using dielectrics with higher $\kappa$ than HfO$_2$, however
Figure 2.6: (a) CV characteristics of n-type In$_{0.53}$Ga$_{0.47}$As MOSCAPs with 3.5 nm HfO$_2$ with N$_2$ plasma/TMA clean; (b) D$_{it}$ extraction using Terman method. Gate leakage is shown in the inset.

at the same time maintaining a low D$_{it}$ interface with In$_{0.53}$Ga$_{0.47}$As substrate is equally important to ensure steep switching TFET operation. Recently ZrO$_2$ has been explored as a higher dielectric constant insulator alternative to HfO$_2$ on In$_{0.53}$Ga$_{0.47}$As channels [49,50]. However limited success was achieved in these works towards achieving low defect density interfaces which are mandatory for high performance FET design. A promising work is recently reported by Chobpattana et al. [9] from University of California, Santa Barbara (UCSB) to attain sub-nm EOT ZrO$_2$ gate stacks on on In$_{0.53}$Ga$_{0.47}$As substrates, with mid-gap D$_{it}$ in range of $10^{12}$cm$^{-2}$eV$^{-1}$. It uses cyclic in-situ nitrogen plasma/trimethylaluminum (TMA) pre-cleaning technique, similar to the one described in previous HfO$_2$ PEALD process. We collaborated with UCSB team to optimize and integrate this ZrO$_2$ gate stack process initially developed at UCSB, into the NTFET fabrication process at Penn State.

A brief description regarding the fabrication sequence of MOSCAP with ZrO$_2$ gate-dielectric on In$_{0.53}$Ga$_{0.47}$As substrates is provided here. For a more detailed treatment readers are referred elsewhere [9]. The substrate for MOSCAP is 300 nm thick, n-type In$_{0.53}$Ga$_{0.47}$As (doped with Si at $10^{17}$cm$^{-3}$) on (001) n+InP, grown using molecular beam epitaxy. Samples underwent a 3 min buffered HF clean followed by immediate transfer into the ALD reactor to prevent undesired regrowth.
of native oxide. At a substrate temperature of 300°C, the cyclic N₂ plasma/TMA surface clean is performed with cycle count optimized to nine cycles. This optimized cycle count achieves a balance between superior degree of interface clean while preventing any semiconductor damage due to overexposure to N₂ plasma. The ZrO₂ thickness deposited was 4 nm which is marginally increased from 3.5 nm optimized for HfO₂ gate stack (Fig.2.6) to keep gate leakage current density in check. Post forming gas anneal at 400°C for 15 min, Ni gate metal is deposited using thermal evaporation through a shadow mask to form gate contacts.

The admittance measurement on MOSCAPs with ZrO₂ dielectric in frequency range from 10KHz to 1MHz are depicted in Figs. 2.7a. Optimized ZrO₂ gate dielectric leads to the thinnest EOT=0.75 nm with lower mid-gap Dᵦ (Figs. 2.7a and 2.7b) compared to other demonstrations on In₀.₅₃Ga₀.₄₇As substrates in literature. The maximum accumulation capacitance density achieved is improved to 3.5 µF/cm² and the corresponding equivalent oxide thickness (CET) is 1.15 nm. The difference between capacitance equivalent thickness and EOT is again from the lowering of the semiconductor capacitance due to quantum capacitance [45] and centroid capacitance [46] as explained before in section 2.3.2. Amount of frequency dispersion in CV characteristics (Fig. 2.7a) specifically the hump in the depletion region is drastically reduced compared to PTFET gate stack (Fig.2.5a) which indicates substantial reduction in mid-gap Dᵦ. This is confirmed through Dᵦ vs. band-energy profile extracted using Terman method. Average Dᵦ on NTFET gate stack is $\sim 10^{13} cm^{-2}eV^{-1}$ as observed from Fig.2.7b which is approximately an order of magnitude lower than Dᵦ in PTFET gate stack (Fig.2.5b). In general high-κ dielectric integration on InGaAs (for n-type FETs) has achieved much progress whereas attaining pristine high-κ interface on GaAsSb (for p-type TFETs) is still a major challenge due to much more pronounced mid-gap Dᵦ. Additionally, the Dᵦ profile on In₀.₅₃Ga₀.₄₇As substrates using ZrO₂ gate dielectric is also improved compared to HfO₂ gate dielectric (Fig.2.7b vs. Fig.2.6b).

Maximum gate leakage current density (4nm thick ZrO₂) is measured to be 100mA/cm² (inset of Fig.2.7b) which adequately satisfies the requirement of state of the art CMOS technology ($\sim 1A/cm²$). Note that the inset in Fig. 2.7b also shows the gate leakage current density corresponding to 3.5 nm ZrO₂ dielectric thickness which is degraded over 4nm thick ZrO₂ dielectric. Hence 4nm ZrO₂ dielectric thickness is used in NTFET device fabrication. Figure 2.7c depicts
the normalized conductance map as a function of gate voltage and frequency. Estimation of $D_{it}$ from normalized conductance peak value (by multiplication with a factor of 2.5) yields a mid-gap $D_{it} \sim 10^{13} \text{cm}^{-2} \text{eV}^{-1}$ consistent with value obtained from Terman method. Moreover, a narrow and almost vertical trace of conductance peak maximum suggests larger band bending and hence efficient Fermi level movement through out the semiconductor band-gap with change in gate bias. Figure 2.7d plots the characteristics response time associated with the interface traps extracted using the modified conductance method [6] which models admittance characteristics and also accounts for loss from gate leakage current. The variation of trap response time versus band-gap energy in Fig.2.7d reveals that the mid-gap traps at ZrO$_2$/In$_{0.53}$Ga$_{0.47}$As interface are greater than ten times faster compared to HfO$_2$/GaAs$_{0.35}$Sb$_{0.65}$ semiconductor interface (Fig.2.5d).

Both P- and N-TFET gate stacks achieve a maximum accumulation capacitance density ($C_{\text{max}}$) of 3.5 $\mu$F/cm$^2$ along with record high CV modulation, $(C_{\text{max}}-C_{\text{min}})/C_{\text{max}} = 97\%$ at 1 MHz (where $C_{\text{min}}$ is the minimum depletion capacitance). Besides the $D_{it}$ magnitude demonstrated on complimentary gate stacks is best in class ever demonstrated on As, Sb based III-V compound semiconductor substrates. These attributes are fundamental towards realizing complimentary TFETs with high $I_{ON}$ and high $I_{ON}/I_{OFF}$ ratio combined with steep switching characteristics. Going forward we integrate these optimized gate stacks in fabrication sequence of P- and N-TFETs respectively, as described in the next chapter.
Figure 2.7: Optimized gate stack on n-type In$_{0.53}$Ga$_{0.47}$As substrate for NTFET:
(a) Capacitance voltage characteristics (4nm thick ZrO$_2$) (b) $D_{it}$ vs. band-bending profile extracted through Terman method. Inset shows gate leakage current density (c) Normalized parallel conductance map with dotted line trace showing movement of the conductance peak maximum (d) Trap response time versus band-gap energy extracted using modified conductance method [6].
Chapter 3
Complimentary HTFET fabrication and Electrical Characterization

3.1 TFET Device Fabrication

We fabricate three-dimensional vertical hetero-junction tunnel FET on wafers grown using molecular beam epitaxy (MBE). Fabrication of TFET is performed at Penn State MRI Nanofabrication Lab. Multiple steps of electron-beam-lithography (approximately 8) combined with plasma dry etch, wet etch, and metallization processes are used to sculpt TFET with vertical nano-pillar geometry. It requires judicious optimization at each step to achieve desired features while avoiding any damage to the device itself. The entire structure is planarized at the end to reduce parasitic capacitance to enable fast I-V measurements on TFET.

3.1.1 Hetero-structures for complimentary HTFET

Figure 3.1 shows the schematic layer structures of In$_{0.7}$Ga$_{0.3}$As/GaAs$_{0.35}$Sb$_{0.65}$ hetero-junction PTFET and GaAs$_{0.4}$Sb$_{0.6}$/In$_{0.65}$Ga$_{0.35}$As hetero-junction NTFET, grown on semi-insulating InP substrate using solid source molecular beam epitaxy (MBE). Linearly graded Al$_{1-x}$In$_x$As buffer was used to accommodate the lattice mismatch between the active layers and the InP substrate. MBE growth forms a defect-free tunnel-interface with abrupt doping profiles that maximizes the junction electric field, as detailed in the material characterization on these wafers reported
elsewhere [51,52]. InAs like surface termination was implemented while switching from Sb to As layers to maintain high quality the heterojunction [51]. The effective tunnel barrier height ($E_{b_{eff}}$) resulting from energy band alignment in this heterostructure for NTFET and PTFET is 0.31eV and 0.25eV respectively [53] (Fig. 3.1).

### 3.1.2 TFET Fabrication and high-$\kappa$ dielectric integration

Figure 3.2 shows the fabrication process flow of Tunnel FET which is an advancement of [22,54]. The modifications include development, optimization and intergation of high performance extremely scaled (0.8 nm EOT) ultra-high-$\kappa$ gate dielectrics onto complimentary TFETs [8] along with process improvements in etch and lithography to enhance device yield. Process details and numerical parameters of fabrication steps are presented in the Appendix A. The fabrication sequence of hetero-junction tunnel FET, illustrated pictorially in Fig.3.2, begins with the creation of nano-pillars. They are patterned using electron-beam lithography followed by plasma dry etch with a Ti/Cr layer acting as etch mask. Any damage to the sidewalls caused by dry etching is removed by citric acid/hydrogen peroxide based wet etch.
which also creates a structure providing shadow-effect, suitable for self-aligned gate metal deposition at the tunneling junction. Gate dielectrics are added by atomic layer deposition. Due to differences in the composition of the channels (As vs. Sb), NTFET and PTFET employ separately optimized HfO$_2$ high-$\kappa$ gate stacks. One of the biggest challenges associated with making any class of III-V transistor for logic applications is that it is tricky to engineer a high-quality interface between the compound semiconductor channel and the gate dielectric. We undertook a rigorous optimization of the gate stack using high-quality surface treatments and Plasma Enhanced Atomic Layer Deposition (PEALD) as presented in Chapter 2. These surface treatments consist of a combination of ex-situ wet-etch clean and in-situ pre-ALD H$_2$ or N$_2$ plasma-based clean. They provide efficient removal of native oxide along with achieving high-quality surface passivation. Drawing on this achievement, for GaAsSb channel based PTFET we demonstrate significantly improved interfaces using a 3.5 nm-thick HfO$_2$ gate dielectric and reduced D$_{it}$ using a H$_2$ plasma-based surface treatment and demonstrated thinnest capacitance equivalent thickness (CET) of 1.2 nm ever reported in GaAsSb material system. Similarly, we have formed InGaAs channel NTFETs with excellent interfaces to 4 nm-thick ZrO$_2$ gate dielectric using a N$_2$ plasma-based surface clean, with a CET of 1.1 nm and a low D$_{it}$.

Post high-$\kappa$ dielectric ALD, nickel gate-metal is deposited through thermal evaporation. Thermal evaporation is more suitable for gate-metal deposition as e-beam evaporation can damage the oxide-semiconductor interface from the x-rays generated in the e-beam evaporation process itself [55]. Subsequently, the source contact (NTFET) is formed by combination of electron-beam lithography and electron beam evaporation of Ti/Pd/Au metal stack followed by lift off in remover PG. Benzochlorobutane is coated as inter-layer dielectric (ILD), thereupon cured and etched back to define and deposit drain contact on the top (NTFET). In case of PTFET the source and drain contacts exchange roles in comparison to NTFET. After these steps, the entire structure is planarized by selective etching of ILD to create vias that enable the addition of contact pads on the top of ILD. This structure helps in minimizing gate leakage current and lowering parasitic capacitance which is necessary for high frequency or fast I-V measurements.

The schematic design of complimentary TFET on common metamorphic buffer technology is shown in Fig. 3.3a. The fabricated PTFET and NTFET devices
TFET Process flow
- Mo Sputter. Ti/Cr etch mask formation
- MESA dry etch, wet etch undercut
- Gate Dielectric Deposition
- Ni (Thermal Evap.) gate deposition
- Source contact definition (Ti/Pd/Au)
- ILD (BCB) planarization and etch back
- Drain pad definition (Ti/Pd/Au)
- Selectively dry etch ILD to form Gate/Source Via
- Gate, Source pad definition (Ti/Pd/Au)

Gate Dielectric Deposition Steps

**PTFET**
- Ex-situ 40s (1:1) HCl:H₂O wet etch
- In-situ 1.5 min H₂ plasma at 150°C
- 3.5 nm HfO₂ ALD at 250°C
- 20 min FGA [65% Ar, 35% H₂] at 350°C

**NTFET**
- Ex-situ 3 min BOE
- In-situ 9 cycles N₂/TMA at 300°C
- 4 nm ZrO₂ ALD at 300°C
- 15 min FGA [95% N₂, 5% H₂] at 400°C

Figure 3.2: (a) Fabrication sequence of planarized TFET process; (b) Separately optimized HfO₂ and ZrO₂ gate stacks procedures are used for P- and N-TFET respectively. Step by step details are included in the Appendix A
scrutinized by transmission electron microscopy which is depicted in Fig. 3.3.

3.2 TFET Electrical Characterization and Performance Benchmark

3.2.1 DC Characterization

DC electrical characterization of the fabricated N and PTFET was performed using an HP 4156A parameter analyzer. All measurements are performed at room-temperature unless explicitly stated. Experimental transfer ($I_{DS}$-$V_{GS}$), switching ($SS-I_{DS}$) and output characteristics ($I_{DS}$-$V_{DS}$) for the fabricated PTFET and NTFET are shown in Fig. 3.4 and Fig. 3.5, respectively. Both n-type and p-type TFETs show high on-current even at low $V_{DS}$ (0.5V and below) and steep switching performance first ever reported in a III-V material system.

GaAs$_{0.35}$Sb$_{0.65}$ channel PTFET achieves $I_{ON}=30\,\mu{A}/\mu{m}$ at $I_{ON}/I_{OFF}=10^5$ at $V_{DS}=-0.5V$. A negative differential resistance (NDR) peak in the forward bias region of TFET ($V_{DS}>0$ in PTFET output characteristics) is a signature of band-to-band tunneling as dominant carrier transport mechanism. However, at room temperature ($T=300K$) thermally activated parasitic conduction mechanisms associated with high mid-gap $D_{it}$ in PTFET obscures this NDR peak. On lowering the temperature to 77K, the contribution from the mid-gap interface traps gets significantly suppressed and the NDR peak manifests itself evidently in the PTFET output characteristics as shown in Fig. 3.4d), indicating efficient band-to-band tunneling. For the same reason, saturation in output characteristics is also pronounced at low temperature.

In$_{0.65}$Ga$_{0.35}$As channel NTFET delivers $I_{ON}=$275$\mu{A}/\mu{m}$ at $I_{ON}/I_{OFF}=3 \times 10^5$ at $V_{DS}=0.5V$. Due to an order of magnitude lower $D_{it}$ achieved in NTFET gate stack over PTFET gate stack, BTBT is remarkably pronounced which manifests as strong saturation of drain current along with distinct NDR peak, in the output characteristics of NTFET (Fig. 3.5c). NDR becomes even more strong at low temperature as observed from Fig. 3.5d, due to deactivation of thermally assisted conduction from traps, as mentioned before.
Figure 3.3: (a) Schematic of complimentary PTFET and NTFET on common metamorphic buffer technology; (b) Cross-section TEM micrographs of fabricated PTFET and NTFET
3.2.2 Fast I-V characterization

One major consequence of the slow response time associated with the mid-gap interface traps is that it causes the DC switching slope for both types of TFETs to exceed the Boltzmann limit of 60 mV/decade at room temperature, by restricting Fermi level movement. DC switching slope for PTFET is 171 mV/decade whereas for NTFET it is moderately improved to 102 mV/decade from lesser $D_{it}$ magnitude.

Figure 3.4: DC measurement: (a) Transfer, (b) Switching and (c-d) Output characteristics of PTFET. All measurements are at $T=300$K, except the additional $T=77$K data in sub-figure(d). NDR is visible in PTFET output characteristics at $T=77$K, due to the suppression of trap response. $N_S$ denotes PTFET source doping concentration.
Figure 3.5: DC measurement: (a) Transfer, (b) Switching and (c-d) Output characteristics of NTFET. All measurements are at T= 300K, except the additional T= 77K data in sub-figure(d). NDR is distinctly visible in NTFET output characteristics at both T= 300K and 77K, due to lower D\text{it} compared to PTFET gate stack.

(Fig 3.4b and 3.5b). As presented in Fig. 2.5d and 2.7d from chapter 2, each of the traps exhibits a characteristics response time associated with itself which decides the rate at which it can exchange charge with the conduction or valence band. Taking advantage of this, it is possible to suppress the impact of mid-gap interface traps on the switching slope by sweeping the gate voltage at a rate that is faster than the trap response time, as switching happens in typical circuit applications.

We took this approach, and performed fast I-V measurements to evaluate the
switching slope with an input gate voltage ramp. The Fast I-V circuit set-up is depicted in Fig. 3.6. Femto DHPCA-100 variable gain high speed current-to-voltage amplifier with $10^2$ to $10^8$ V/A trans-impedance gain, along with 200MHz bandwidth capability, was used to sense drain current with high signal to noise ratio across on-state, switching and off-state characteristics of TFET. Magnitude of drain voltage was fixed to 0.5V to assess steep-switching capability in conjunction with on-current. A low pass filter was inserted at the output of the drain supply to eliminate irregularities in voltage supply. The gate probe was terminated with 50 ohm impedance to avoid any reflections during the high frequency gate voltage ramp. Common ground for all probes along with a ground shield plane below the device under test was used to minimize transients. Ramp waveforms applied on gate terminal were generated using Agilent function generator and the voltage output from current-to-voltage amplifier was recorded in LeCroy oscilloscope. Displacement current was measured to be $50\times$ less than measured current range and the recorded data was corrected for it along with the skew compensation between the input applied voltage ramp and the output measured voltage on oscilloscope.

Fast $I_{DS}$-$V_{GS}$ measurements on TFETs were then performed with input gate voltage ramp with rise time varying from 10 $\mu$s to 300 ns to assess switching performance. Using these conditions, switching characteristics improved, and we achieved room-temperature values for the p-type and n-type TFETs of 115 mV/decade and 55 mV/decade, respectively as captured in Fig.3.7b and 3.7d. The high on-current with sub-60 mV/decade switching demonstration for n-TFET and high on-current with improved switching demonstration in the case of p-TFET is a direct consequence of engineering high-quality scaled gate dielectrics and tunnel barriers in the arsenide-antimonide system.

### 3.2.3 Complimentary TFET performance benchmark

To put our results in context, we benchmark experimental switching slope (SS) vs. drain current ($I_{DS}$) characteristics of complimentary TFETs developed in this work against other published results in literature. The SS vs. $I_{DS}$ benchmark was earlier presented in section 1.1.3 to capture the incumbent state of the art in TFET technology. This comparison includes both homo- and hetero-junction tunnel FETs made with silicon/SOI/SiGe materials. Note that the requirement of sub-$kT/q$
Sweep \(V_{GS}\) at a rate faster than trap response time.* Sub-threshold slope degradation can be suppressed by sweep rate faster than trap response time. The simplified circuit set-up used for fast \(I_{DS}-V_{GS}\) measurements is shown in Figure 3.6. The measurements were performed at National Institute of Standards and Technology, Gaithersburg MD.

Switching (<60 mV/decade at room temperature) coupled with high on-current directs the desired design space to the lower right corner of SS - \(I_{DS}\) plot.

The skewed distribution of Si/SOI/SiGe-based demonstrations in PTFET devices versus III-V-based TFET demonstrations in NTFET devices is conspicuous from Figs. 3.8a and 3.8b respectively. This is expected as in PTFET, low conduction-band density-of-states \([14]\) (especially critical for homo-junction TFETs) along with high mid-gap \(D_{it}\) on p-type substrates poses a daunting challenge for III-V material system. We addressed these challenges through use of tunnel-barrier engineering coupled with rigorous gate stack optimization using ultra-thin high \(\kappa\)-gate dielectrics to achieve moderate \(D_{it}\). This enabled us to demonstrate first p-type TFET on GaAs\(_{0.35}\)Sb\(_{0.65}\) channel with \(I_{ON}=30\mu A/\mu m\) and \(I_{ON}/I_{OFF}=10^5\) at \(V_{DS}=-0.5V\). It is observed that PTFETs demonstrated in Si/SOI/SiGe material system achieve steep switching, but not in conjunction with a high current because of large energy band-gap which reduces tunneling transmission significantly and hence lowers \(I_{ON}\).

Figure 3.8b presents the SS vs. \(I_{DS}\) benchmark for n-channel TFETs. Taking benefit from lower \(D_{it}\) on (n-type) InGaAs and InAs substrates, III-V TFETs...
Figure 3.7: Improvement in transfer and switching characteristics of (a-b) PTFET and (c-d) NTFET through Fast $I_{DS}$-$V_{GS}$ characterization. PTFET achieves near 100mV/decade switching and NTFET delivers a sub-thermal switching of 55 mV/decade. All measurements are at $T=300\text{K}$.

have been reported with higher on-currents as a benefit of smaller band-gap. On the other hand sub-$kT/q$ switching slope has still eluded researchers especially in conjunction with high on-current due to either lack of efficient $D_{it}$ passivation techniques employed at high-\(\kappa\) gate dielectric and III-V channel interface, or choice of material system, or poor electrostatics etc. Reports of sub-thermal SS have been primarily limited to extremely low $I_{DS}$ [20] or only at low $V_{DS}$ [21]. We combine tunnel barrier engineering with significantly improved gate stack on $\text{In}_{0.65}\text{Ga}_{0.35}\text{As}$
channel NTFET, to achieve the best in class demonstration of $I_{ON} = 275 \mu A/\mu m$ with sub-thermal switching of 55mV/decade at $V_{DS} = 0.5V$.

It is important to note that in SS vs. $I_{DS}$ benchmarks presented in Figs. 3.8a and 3.8b, TFET demonstrations based on Si, SiGe (Group IV) material system TFETs are not expected to show significant improvement in switching characteristics with fast I-V. This is expected because the state of the art gate stack on Si and SiGe substrates is already well-developed with very high quality interface to gate-dielectrics and low $D_{it} \sim 10^{10} cm^{-2} eV^{-1}$. On the other hand, use of fast I-V to evaluate actual switching potential in III-V TFETs is useful as it suppresses slowing of Fermi level movement from their high $D_{it} \geq 10^{12} cm^{-2} eV^{-1}$. Advancement in gate stack research will naturally benefit III-V TFETs to a significant extent. Additionally, tunnel barrier engineering utilized in this work provides the essential ingredient towards realizing a complimentary TFET technology with high $I_{ON}$ combined with high $I_{ON}/I_{OFF}$ current ratio, as illustrated in Fig. 3.9.

Table 3.1 provides a comparison of key electrical parameters of our complimentary TFETs with other state of the art demonstrations. Our antimonide-channel based p-type TFET deliver superior performance, and when partnered with our arsenide-channel based n-type TFET, it demonstrates the potential of III-V complimentary tunnel FET logic. This is first demonstration of an all 'III-V' material system based complimentary HTFETs at low $V_{DS}$ with high $I_{ON}$ and steep switching performance. Building on this work, our future research focuses on expanding the steep switching range over multiple decades of drain current with no-compromise on on-current. This sets the goal for our next chapter where we exclusively perform in-depth characterization of critical semiconductor interfaces in TFET to identify the bottlenecks towards realizing high performance TFETs.
### Table 3.1: Benchmark of Si and III-V TFETs [8]

<table>
<thead>
<tr>
<th>Structure</th>
<th>PTFET</th>
<th>NTFET</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>V_{DS} [V]</strong></td>
<td>0.6</td>
<td>0.3</td>
</tr>
<tr>
<td><strong>I_{ON} [µA/µm]</strong></td>
<td>1.8</td>
<td>10</td>
</tr>
<tr>
<td><strong>I_{MIN} [µA/µm]</strong></td>
<td>1.2X10^{-6}</td>
<td>2.0X10^{-6}</td>
</tr>
<tr>
<td><strong>I_{ON}/I_{MIN}</strong></td>
<td>1.4X10^6</td>
<td>5.0X10^3</td>
</tr>
<tr>
<td><strong>S_{MIN} [mV/dec.]</strong></td>
<td>30</td>
<td>90</td>
</tr>
<tr>
<td><strong>EOT [nm]</strong></td>
<td>4.5</td>
<td>0.7</td>
</tr>
<tr>
<td><strong>Lg [nm]</strong></td>
<td>140</td>
<td>200</td>
</tr>
</tbody>
</table>

**V_{ON} (V_{MIN})** corresponds to the gate voltage at I_{ON} (I_{MIN}). |V_{ON}| is limited to 1.5V from |V_{MIN}|
Figure 3.8: Switching slope (SS) vs. drain current ($I_{DS}$) benchmark of experimental demonstrations in literature for (a) p-channel TFET, and (b) n-channel TFET. For energy efficient high performance logic design, sub-$kT/q$ switching (<60 mV/decade at room temperature) is needed coupled with high on-current. This requirement directs the desired design space to the lower right corner of SS - $I_{DS}$ plot. 14 nm Si-FinFET is included for reference.
Figure 3.9: On-current ($I_{ON}$) vs. on-off current ratio ($I_{ON}/I_{OFF}$) benchmark of experimental demonstrations in literature for (a) p-channel TFET, and (b) n-channel TFET. $I_{ON}/I_{OFF} \geq 10^5$ coupled with $I_{ON} \sim mA/\mu m$ is typical in the state of the art high performance Si-FinFET technology which is also shown for reference. Tunnel-barrier engineering is the key to achieve this desired combination in TFET design. Benefiting from this, complimentary III-V TFETs show remarkable potential for next-generation energy efficient transistors.
Chapter 4  |  Interface Characterization

The primary benefit of Tunnel FET device technology is its potential to beat the so-called Boltzmann tyranny of $kT/q$ constrained switching plaguing Si-CMOS and operate under very low supply voltages without compromising on-state performance. Experimental demonstrations however have achieved limited success as presented earlier in section 3.2.3 and show significant trade-off between $I_{ON}$ vs. SS. This trade-off is a serious challenge and has to be addressed methodically by identifying the fundamental underlying physics and designing for optimal performance. Most of the experimental TFET demonstrations fall-short due to (a) lack of high-quality gate-stack, (b) material selection, (c) poor junction design, (d) inferior electrostatics resulting from un-optimized device geometry, which diminishes gate control on the tunnel-junction, or a combination of these factors. In this chapter our goal is to identify and quantify each bottleneck factor towards realizing high performance TFETs with high-$I_{ON}$, low $I_{OFF}$ and steep SS by performing rigorous interface characterization.

Being made from a combination of III-V materials integrated with extremely scaled Hi-K dielectrics, hetero-junction TFET (HTFET) absolutely require abrupt and pristine interfaces among dissimilar materials. Variability at these vital interfaces, or hetero-junctions, dramatically reduces device performance. We characterize each of these interfaces taking example of a n-type HTFET and subsequently quantify the impact on HTFET electrical parameters. We will start with highlighting key difference in interfaces characterization between MOSFET versus TFET. We will explain the need for new characterization techniques for TFET and detail on techniques we have used on our devices. Finally, we will conclude by presenting criteria for engineering quality interfaces to realize high performance HTFET.
4.1 Critical Interfaces in MOSFET

We briefly review the critical semiconductor interfaces in a conventional MOSFET. As we are exclusively dealing with III-V materials we will base this example on a III-V MOSFET, without loss of generality as same fundamentals apply to a Si-MOSFET too. In a MOSFET, the only critical interface is High-K gate dielectric with III-V channel shown in Fig. 4.1a. This interface is highly reactive with presence of dangling bonds and defect sites. This gives rise well-known interface trap density ($D_{it}$) distribution throughout the semiconductor band-gap. This $D_{it}$ slows the efficiency of Fermi level movement and dilutes switching performance of the MOSFET. In order to evaluate quality of High-K/III-V channel interface in MOSFET, the simplest approach involves building MOS capacitors and subsequently performing a capacitance-voltage (C-V) electrical characterization. By analyzing the stretch-out and frequency dispersion in C-V characteristics useful information regarding $D_{it}$ distribution and trap characteristic response time can be extracted (Fig. 4.1b). This very analysis was presented in chapter 2 for HfO$_2$ and ZrO$_2$ dielectric based gate stacks on p-type GaAs$_{0.35}$Sb$_{0.65}$ and n-type In$_{0.65}$Ga$_{0.35}$ channel TFETs respectively. Electrical characterization is most of the time sufficient for interface characterization in MOSFETs.

4.2 Critical Interfaces in TFET

In a Tunnel FET, in addition to High-K gate dielectric/III-V channel interface which is in common with MOSFETs, there exists another highly critical interface: the tunnel junction itself (Fig. 4.2). Tunnel FET relies on fundamental mechanism of quantum mechanical tunneling from source to channel region. So the tunnel junction becomes of paramount importance to TFET operation. In case of hetero-junction TFET (HTFET) which is the preferred candidate for high performance MOSFET replacement, the tunnel-junction is more sophisticated as it is a hetero-tunnel junction due to difference in the source and the channel material composition. In order to achieve efficient inter-band tunnel rate we need to ensure that the tunnel junction is abrupt not only in terms of compositional switching but also in terms of source dopant profile. Besides the hetero-tunnel junction, the ultra-thin High-K dielectric and III-V interface forms the second critical interface in HTFET. The
Figure 4.1: (a) High-K dielectric/III-V semiconductor interface forms the critical interface in a III-V MOSFET; (b) Defects at this interface give rise to characteristics stretch-out and frequency dispersion observed in the capacitance voltage measurements.

electrical properties of this interface is similar to III-V MOSFETs, however the key difference from MOSFET results from, in a tunnel FET inter-band tunneling is highly confined within few nm of tunnel junction. This localized high electron-band to band generation can trap carriers near the gate oxide near source which can impede efficiency of gate field to modulate the tunnel barrier.

With the addition of the hetero-tunnel junction as the critical interface, there is no direct experimental procedure to characterize it accurately. Hence for the first time, we present a 3 dimensional atomic resolution characterization of hetero-tunnel junction using a unique technique called Atom Probe Tomography. For the second interface: High-K dielectric and III/V channel, we will draw learnings from characterization techniques used for MOSFET and build upon it to improve both depth and accuracy of characterization. Particularly in this work we will use temperature dependent I-V with self-consistent TCAD models and BTI stress to assess different ultra-thin High-K dielectric (0.8 nm EOT: HfO₂, ZrO₂, HfO₂+ ZrO₂ bi-layer) interfaces to III-V channel.
Figure 4.2: Variations in critical interfaces of Hetero-junction TFET (HTFET) studied in this work.

4.2.1 Interface 1: Tunnel Hetero-junction Interface

4.2.1.1 Junction Abruptness

Hetero-tunnel junction comprises of switching of semiconductor material composition from GaAs$_{0.4}$Sb$_{0.6}$-based source to In$_{0.65}$Ga$_{0.35}$-based channel, the spatial extent of which we define as tunnel interface width ($T_W$). This spread of tunnel interface diminishes tunnel transmission for electrons injected from the source to the channel region (Fig. 4.3a and 4.3b). Additionally, the tunnel junction also incorporates a steep dopant profile at the junction itself to enable efficient inter-band tunneling through high junction field. The inter-band tunneling rate from source to channel region has exponential dependence on junction parameters: (i) tunnel junction electric field $\xi$ (governed by doping profile $N_S$ and gate field, $V_{GS}$), and (ii) effective tunnel barrier height ($E_b_{eff}$) which is determined by source-channel material selection and also $T_W$ which defines tunnel junction abruptness. A non-zero interface
Figure 4.3: (a) Tunnel junction is the first critical interface to TFET operation. In HTFET, this is a hetero-tunnel junction as source and the channel possess different III-V material compositions and this compositional switching occurs over a finite width which is defined as tunnel interface width ($T_W$). Finite $T_W$ spreads out the tunnel barrier on either side of the tunnel junction as indicated in simulated energy band-diagram (b) Junction parameters like tunnel barrier height ($E_{b,eff}$) and electric field directly impact tunnel transmission and hence the drain current. $T_W$ width is the correct depiction of tunnel hetero-junction as it naturally arises from ion intermixing during the MBE growth process during switching from mixed anion GaAsSb source to mixed cation InGaAs channel layers [51].

Irrespective of the junction formation technique, $T_W$ is always finite and generally expected in order of few nanometers corresponding to distance over which atomic switching happens. This effect is generally ignored in numerical simulations however we emphasize its importance especially in modeling hetero-junction TFETs. Finite $T_W$ produces undesirable spreading of $E_{b,eff}$ as depicted in Fig.4.3a and hence impedes the tunnel process. It is significant challenge to characterize hetero-junctions with precision in nanometer-scale devices. We characterize this critical interface in three dimensional atomic scale resolution using atom probe tomography (APT) to evaluate HTFET performance in presence of junction width variation [56].

APT is a unique measurement technique which combines atomic projection imaging and time-of-flight spectroscopy [57–59] (Fig. 4.4). The procedure begins with TFET sample preparation. First, a III-V specimen extracted over a length
straddling across TFET tunnel junction is cast into a needle-like shape and is cooled to a temperature of 50º Kelvin. Atoms are field evaporated from the specimen apex in a controlled fashion by creating a divergent electrostatic field about the needle-shaped specimen opposed by a counter electrode. For a specimen diameter in range of 100 nm, it's takes approximately 10kV to create electric fields on the order of $10^8$ V/cm at the apex which is necessary to induce field evaporation of atoms [59]. By varying the applied voltage such that single-atom evaporation dominates, it is possible to readily control the field evaporation. However, it is not possible to control which atom will evaporate.

To determine the time of departure of ions it is necessary to pulse field evaporation. Since field evaporation depends on the specimen temperature and applied field, either can be pulsed to create a pulsed field evaporation event. Thermal pulsing is accomplished by directing a laser at the apex of the specimen to induce a small temperature rise. In the case of this experiment, laser pulsing was used to facilitate the pulse field evaporation process. The APT measurement conditions were optimized to a temperature of 50K and reducing the laser pulse energy to 3pJ at a pulse frequency of 250kHz. The average detection rate of 0.01 ions/pulse was maintained throughout the experiment and the analysis direction was parallel to the growth direction. Very low pulse energies and base temperatures were chosen to minimize surface migration effects that may impact the spatial accuracy.

Each evaporated atom is identified and located by using time-of-flight mass spectroscopy. As we can accurately determine the identity and position of each atom in the specimen, we construct a 3D model of the specimen from all atoms hence collected on the detector, with a resolution of 0.2 nm (Fig.4.4). The 3D ion maps in Fig.4.5(b,c) and were reconstructed by means of the commercial software IVAS™. Atomic constituents are displayed as colored spheres in the 3D ion map of GaAs$_{0.4}$Sb$_{0.6}$(C-doped)/In$_{0.65}$Ga$_{0.35}$ tunnel junction interface as depicted in Fig.4.5(b,c). An ion map of the side-on view of the InGaAs/C-doped GaAsSb interface in Fig.4.5(c) illustrates the dual layer of C-doped GaAsSb. Additionally, the interfacial width of the hetero-tunnel junction is also determined by APT. In this analysis, the tunnel interfacial width ($T_W$) associated with this hetero-tunnel-junction is computed from 10% and 90% atomic concentration thresholds which is measured to be 2.4 nm as illustrated in Fig.4.6a.

X-ray reciprocal space map (RSM) measurements (Fig.4.6b) were utilized to
Atoms Removed 1X1
Layer by Layer

Data is collected and interpreted

Cryogenically cooled Nanoscale tip

Voltage Supply (0-15 kV)

Pulsed Laser

Time of Flight

2-D Position Detector

KEY PARAMETERS
• Data Collection Rate (ions/min): > 5M
• Field of View: > 200nm
• Depth Resolution: 1-3 Å
• Lateral Resolution: 2-6 Å
• Sensitivity: Several atoms per transistor

Figure 4.4: Atom Probe Tomography (APT) set-up used to characterize the hetero-tunnel-junction in three-dimensional atomic scale resolution.

Figure 4.5: (a) Cross-section micro-graph of fabricated III-V HTFET (b) Tunnel junction specimen is characterized using APT with three dimensional ion map showing In ions forming the InGaAs layer and Sb and C ions forming the C-doped GaAsSb layer. The reconstructed volume is 100×110×620 nm³. (c) Side-on magnified view of the InGaAs/C-doped GaAsSb interface.
Thicker tunnel interface in effect increases tunnel barrier

Abrupt design: 2.5 nm $T_W \rightarrow 1$ nm $T_W$: 38% $I_{ON}$ gain


In$_{0.65}$Ga$_{0.35}$As

Channel

C-doped GaAs$_{0.4}$Sb$_{0.6}$ Source

Experiment

In$_{0.65}$Ga$_{0.35}$As/GaAs$_{0.4}$Sb$_{0.6}$ Interface

Concentration (at %)

Distance along tunnel junction [nm]*

*post-sample prep.

Figure 4.6: (a) Calculated composition profile at the InGaAs/GaAsSb interface. Dotted lines indicate the position of 10% and 90% concentration thresholds used to define tunnel interface width ($T_W$) of 2.4 nm; (b) RSM quantification of lattice mismatch in hetero-layer structure.

Complement the APT analysis to complete the junction characterization. The relaxed lattice constant for each of the layers in the HTFET stack as determined from RSM characterization is presented in Table 4.1 along with information on composition of the device layers, obtained from APT.

We now evaluate the impact of a non-abrupt tunnel junction interface width (Fig.) centered around 2.4 nm as determined by APT, using calibrated numerical simulations [8]. As depicted in Fig. 4.7a and 4.7b, HTFET transfer ($I_{DS}$-$V_{GS}$) and switching characteristics ($SS-I_{DS}$) display significant variation with $T_W$. As observed from Fig. 4.7c, $I_{ON}$ degrades by 61% and $I_{ON}/I_{OFF}$ by 10% due to change in $T_W$ from 1 nm to 5 nm. $I_{OFF}$ does not change in the same proportion as $I_{ON}$ as gate field is non-existent in off-state and $I_{OFF}$ and it also significantly depends on the dopant profile of the tunnel junction. A compositionally abrupt hetero-junction with improved $T_W$ from present 2.4 nm will exponentially benefit HTFET on-current.
Table 4.1: Measured lattice constants, dopant concentrations and layer compositions for the NTFET hetero-stack. Atomic percentage and atomic concentration are denoted by at% and at/cm$^3$ respectively.

<table>
<thead>
<tr>
<th>NTFET layers</th>
<th>Relaxed lattice constant</th>
<th>MBE growth parameters</th>
<th>APT measured parameters</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Units Å</td>
<td>In at% Ga at% As at% Sb at% Si at/cm$^3$ C at%</td>
<td>In at% Ga at% As at% Sb at% Si at/cm$^3$ C at/cm$^3$</td>
</tr>
<tr>
<td>In$<em>x$Ga$</em>{1-x}$As (n+ Si)</td>
<td>5.917</td>
<td>65 35 - - 10$^{18}$ -</td>
<td>65 35 - - 10$^{18}$ -</td>
</tr>
<tr>
<td>In$<em>x$Ga$</em>{1-x}$As (i)</td>
<td>5.917</td>
<td>65 35 - - - -</td>
<td>65 35 - - - -</td>
</tr>
<tr>
<td>GaAs$<em>x$Sb$</em>{1-x}$ (p++ C)</td>
<td>5.874</td>
<td>- - 40 60 - 10$^{20}$ - - 50 50 - 6.7×10$^{19}$</td>
<td></td>
</tr>
<tr>
<td>GaAs$<em>x$Sb$</em>{1-x}$ (p+ C)</td>
<td>5.874</td>
<td>- - 40 60 - 5×10$^{19}$ - - 50 50 - 4×10$^{19}$</td>
<td></td>
</tr>
<tr>
<td>Al$_{1-x}$In$_x$As</td>
<td>5.915</td>
<td>- - - - - -</td>
<td>- - - - - -</td>
</tr>
<tr>
<td>InP</td>
<td>5.869</td>
<td>- - - - - -</td>
<td>- - - - - -</td>
</tr>
</tbody>
</table>
Figure 4.7: Impact of a non-abrupt tunnel interface is studied by assuming tunnel interface width ($T_W$) varying from 0 to 5 nm. (a) transfer-characteristics, (b) switching slope with varying $T_W$, (c) $I_{ON}$ is degraded by 61% whereas on-off current ratio is degraded by 10% due to change in tunnel width from 1nm to 5nm. EOT=0.7 nm, $T_{body}$=7 nm and $L_g$=20 nm is used for simulations.
4.2.1.2 Dopant Profile Abruptness and Random Dopant Fluctuation

In addition to compositional abruptness attribute of hetero-tunnel junction, it is highly significant to analyze the abruptness of the dopant profile. Dopant profiles were measured by secondary ion mass spectroscopy (SIMS). Figure 4.8a depicts nominal dopant concentration vs. distance along the tunnel junction obtained from SIMS characterization of HTFET. A slope of 2 nm/decade in source dopant profile at the tunnel junction indicates steep junction formation. A steep source dopant profile is necessary for maximizing junction electric field which dictates tunneling transmission. Any variation or fluctuation in source dopant concentration manifests distinctly in HTFET performance as described further.

We first investigate HTFET sensitivity to source doping concentration ($N_s$). We assume a uniform continuous source doping concentration ($N_s$) and perform numerical simulations of HTFET with $N_s$ varying from $10^{19}\text{ cm}^{-3}$ to $10^{20}\text{ cm}^{-3}$. Figure 4.8b illustrates impact of $N_s$ change on HTFET transfer characteristics. It is observed that $I_{OFF}$ exhibit a steep $83 \times$ change with $N_s$ varying from $10^{19}\text{ cm}^{-3}$ to $10^{20}\text{ cm}^{-3}$, on the contrary $I_{ON}$ changes only by 3 times. This is because the drain current depends on the electric field density at the tunnel junction. This electric field in-turn depends on both source doping profile (which governs intrinsic electric field of the p-n junction) and supplemental contribution from gate electric field. In off-state, lack of gate field causes the drain current ($I_{OFF}$) to become highly sensitive to changes in dopant profile. On the other hand, in on-state the gate field plays additional dominating role in facilitating inter-band tunneling and hence reduces impact on $I_{ON}$.

As observed from APT image presented in Fig. 4.5, the dopant atoms in the source region are discrete and randomly distributed unlike a continuous uniform doping profile normally assumed in numerical simulators. Hence we evaluate the impact of random dopant fluctuation (RDF) in the source region by assuming a nominal source doping concentration and subsequently performing doping randomization using Sano’s approach [7]. This approach assigns a doping function to each discrete dopant which models the long-range portions of charge density associated with discrete dopants [60]. The union of all such doping functions defines the final doping profile for the structure. Note that RDF originating from source region is the dominant contributor towards degrading TFET performance as reported elsewhere [61]. This is expected as source RDF directly impacts the tunnel junction.
Randomized source dopant profiles are generated as depicted in Fig.4.9 for two nominal \( N_S \): \( 6.7 \times 10^{19} \text{cm}^{-3} \) (APT) and \( 10^{20} \text{cm}^{-3} \) (MBE growth parameter). 3D TCAD simulation of 200 such randomized discreet dopant profile splits per nominal source doping concentration is performed [60]. The statistical distribution of \( V_T \) (threshold voltage, from constant current method, \( I_{\text{const}}=0.5 \mu\text{A/\mu m}, V_{GS}=V_{DS}=0.5 \text{V} \)), \( I_{\text{ON}} \) and \( I_{\text{OFF}} \) obtained from this simulation is summarized in Fig.4.10. It is observed that RDF in source causes 30% \( \sigma \)–variation in \( I_{\text{OFF}} \) (nominal \( N_S=6.7 \times 10^{19} \text{cm}^{-3} \)). This can be attributed to exponential dependence of \( I_{\text{OFF}} \) on the tunnel junction intrinsic electric field. In contrast, \( V_T \) and \( I_{\text{ON}} \) are impacted in relatively lower magnitude (3% only) as besides \( N_S \) change, gate field plays significant additional role in causing source-channel band crossing and enhancing tunnel current. Impact of source RDF diminishes to 16\% \( \sigma \)–\( I_{\text{OFF}} \) at higher nominal \( N_S \) of \( 10^{20} \text{cm}^{-3} \). However, increasing \( N_S \) to improve immunity of \( I_{\text{OFF}} \) against RDF comes with a trade-off with switching slope steepness. This trade-off is especially evident in p-type HTFETs where low conduction band density of states in source region exacerbates Fermi level degeneracy at high \( N_S \) which greatly hampers the sub-thermal switching capability of p-type HTFETs [62].
Figure 4.9: RDF in source is simulated using Sano’s approach [7], with 200 RDF profiles for each nominal $N_S$.

Figure 4.10: For optimal designed hetero-junctions with steep doping profiles (as in Fig.4.8a), RDF in source shows weak influence on HTFET threshold voltage and on-current, however significantly degrades the off-state current.
Figure 4.11: Traps give rise to significant parasitic conduction mechanisms which contaminate the intrinsic band-to-band tunneling process in TFET, thereby diluting the sub-thermal switching characteristics.

4.2.2 Interface 2: High-K dielectric/III-V channel Interface

High-K dielectric/III-V channel interface shares similar physics as in III-V MOSFET. Unsaturated bonds and defects states at gate dielectric/channel interface undermine the control of gate electric field on producing band-bending in the channel region, thereby worsening charge injection efficiency from source region. Traps provide ground for several parasitic charge conduction mechanisms which dilute the intrinsic ideal inter-band tunneling charge transport in TFET. Primary effects of traps manifested in TFET are: (a) Shockley-Read-Hall generation-recombination (G/R), (b) Trap assisted tunneling (TAT, or tunneling assisted G/R), and (c) Charge sharing with channel, which is an electrostatic effect. Out of these three, (a) and (c) are also present in MOSFET. High-K dielectric/III-V channel interface (trap density, \(D_{it}\)) form the principal source of defects in III-V HTFET. Particularly these traps in close proximity with hetero-tunnel junction can produce significantly complex transport mechanisms (Fig.4.11) with distinct electric-field (E-field) and temperature dependence. We will take advantage this E-field and temperature dependence to identify how carrier transport mechanisms in HTFET are shaped by \(D_{it}\).
Figure 4.12: (a) Temperature dependent transfer characteristics of HTFET exhibit three distinct operation regimes; (b) Improvement in PVCR of NDR peak in low temperature $I_{DS}-V_{DS}$ characteristics due to suppression of excess current.

4.2.2.1 Temperature dependent I-V

We perform temperature dependent $I_{DS}-V_{GS}$ measurements on n-type HTFET to investigate and quantify impact of High-k dielectric/III-V channel interface $D_{it}$ on dominant carrier transport mechanisms. N-type HTFET with 3.5 nm HfO$_2$ gate dielectric is used for this study. From the temperature dependent transfer characteristics of HTFET shown in Fig.4.12a three different operating regimes are distinctly evident: off-state, switching-state and on-state. In the negative differential resistance (NDR) region of HTFET output characteristics, shown in Fig.4.12b, it is observed that peak-to-valley current ratio (PVCR) improves at low temperature due to suppression of excess current [63].

We analyze off-state, switching characteristics and on-state sequentially. Firstly it is important to establish that gate leakage density is not limiting off-state performance. The gate leakage current is compared with drain-source off-state current in Fig.4.13a and found to be 50 times less than $I_{OFF}$ at all temperature range. This indicates high quality integration of ultra-thin ALD HfO$_2$ gate dielectric on In$_{0.65}$Ga$_{0.35}$As channel. In particular, $I_{OFF}$ can be described by Shockley-Read-Hall (SRH) generation-recombination (G/R) current in the reverse-biased hetero-junction diode. An activation energy ($E_A$) of 0.19 eV is extracted for SRH mechanism using an Arrhenius-type relationship plot (Fig. 4.13b). This is unlike homo-junction
Figure 4.13: (a) $I_{OFF}$ is not limited by gate leakage current (b) SRH statistics yield an activation energy of 0.19 eV for $I_{OFF}$. This is in close proximity of mid-tunnel barrier height ($E_{b_{eff}}$).

TFET where $E_A = E_g/2$ is typically obtained suggesting generation-recombination through mid-band gap traps ($D_{it}$) [63]. At the same time, activation energy of 0.19 eV is in close proximity of mid-tunnel barrier height ($E_{b_{eff}}/2=0.16$ eV [53]) which indicates $I_{OFF}$ is dominated by generation-recombination near the tunnel junction.

In order to capture the impact of $D_{it}$ on switching characteristics of HTFET we assume a Frenkel-Poole type of transport assisted through traps as shown in Fig.4.14 similar to homo-junction TFET [63]. Charge carriers from the valence band of source region tunnel into traps in the band-gap and subsequently undergo electric field-enhanced thermal excitation into conduction band the channel region. We use tunnel junction electric field ($F_s$) modeled through calibrated numerical simulations, and extract the effective thermal barrier height $\phi$ (relative to conduction band edge $E_C$) for the trapped carriers. Significant contribution from trap energy levels $\phi=0.55$ eV corresponding to $V_{GS}=0.1$V to $\phi=0.43$ eV corresponding to $V_{GS}=0.7$V is detected. This provides useful information regarding energy distribution of mid-gap $D_{it}$ relative to band-edges.

Saturation of $I_{ON}$ at low temperature in Fig.4.15a indicates band-to-band tunneling (BTBT) as dominant transport mechanism in the on-state. The onset of band-to-band tunneling (BTBT) is estimated from $E_A<0.1$eV threshold ($E_A$ for
Figure 4.14: Switching characteristics are modeled assuming Frenkel-Poole type of transport. $D_{it}$ contribution from energy levels at 0.55 eV (from $E_c$) at $V_{GS}=0.1V$ to 0.43 eV at $V_{GS}=0.7V$ is detected.

$BTBT \leq 4k_B T$ \[64,65\]) as shown in Fig.4.15b. Temperature dependence of $I_{ON}$ is explained reasonably well through temperature dependent dynamic non-local path direct BTBT models as observed in Fig.4.15c.

We now model all the three distinct operating regimes in the experimental HTFET transfer characteristics concurrently using numerical simulation. $D_{it}$ energy distribution mapped through Frenkel-Poole analysis of HTFET temperature dependent experimental characteristics is used to achieve continuous fit over all range of gate-bias. The $D_{it}$ profile thus obtained, shown in Fig.4.16a, achieves consistent solution with SRH physics, coupled with dynamic non-local path models for BTBT and Schenk TAT used in the numerical simulation. Figure 4.16b and 4.16c present individual $I_{DS}$ components (SRH, TAT and BTBT) and their impact on HTFET switching performance. It is observed that SRH G/R coupled with TAT and traps occupancy change (through charge sharing with channel region) are the primary bottlenecks towards realizing sub-thermal switching. HTFET design goal hence will focus on suppressing trap assisted tunneling and G/R mechanism to bring out intrinsic BTBT and hence the benefit of efficient sub-thermal switching.

Only reducing $D_{it}$ is however not sufficient for achieving sub-thermal switching over multiple decades of drain current. This is evident from SS versus $I_{DS}$ plot from numerical simulations calibrated to experimental data presented in Fig.4.17a. It is observed that in present fabricated TFETs with body thickness $T_{body}=500$
Figure 4.15: (a) $I_{ON}$ saturation at low temperature indicates BTBT as dominant transport mechanism in on-state; (b) Sub-0.1eV activation energy estimates onset of BTBT; (c) Temperature dependence of BTBT observed through experiments is explained accurately through temperature dependent non-local BTBT TCAD models.

nm, the benefits of lowering $D_{it}$ are over-shadowed by background leakage floor set by parasitic conduction mechanisms like SRH G/R, TAT and also from reduced control on tunnel junction due to poor electrostatics. This hinders efficient sub-kT/q switching realization even on reducing $D_{it}$ to $5 \times 10^{11}$ cm$^{-2}$ ev$^{-1}$ in present devices with thick $T_{body}$. To realize efficient sub-thermal switching in TFET spanning multiple decades of drain current, scaling $D_{it}$ has to accompanied with scaling of
Figure 4.16: Interface trap density profile shown in (a) is used to achieve consistent solution with SRH, TAT and BTBT physical models; (b,c) Breakdown of current-voltage characteristics and switching performance of HTFET. Parasitic charge conduction mechanism assisted through traps significantly dilute sub-thermal switching capability from BTBT.

the body thickness ($T_{\text{body}}$) in TFET. Extending calibrated simulation for HTFET to scaled $T_{\text{body}}=50$ nm and with low $D_{it} \leq 10^{12}$ cm$^{-2}$ eV$^{-1}$ reveals sub-kT/q switching over two decades range of $I_{DS}$ as shown in Fig.4.17b.

Scaling of $T_{\text{body}}$ can be achieved through use of Cl$_2$ based Reactive Ion Etch (RIE) for InGaAs, at elevated temperature which enables a nanometer-scale vertical-sidewall profile [66]. To scale $D_{it}$ further, gate stack optimization for complimentary TFETs are absolutely necessary. Equally important is achieving high-quality of sidewall-surface passivation before integrating high-performance gate stacks. Figure 4.18a depicts that the magnitude of mid-gap $D_{it}$ extracted on MOSCAPs on
Figure 4.17: (a) High leakage floor due to poor electrostatics from thick tunnel junction width ($T_{body}=500$ nm) aggravated with high SRH and TAT contributions hinders efficient sub-kT/q switching realization even on reducing $D_{it}$ to $5 \times 10^{11}$ cm$^{-2}$ ev$^{-1}$; (b) HTFET with $T_{body}=50$ nm and low $D_{it} \leq 10^{12}$ cm$^{-2}$ ev$^{-1}$ exhibits sub-kT/q switching over two decades of $I_{DS}$, highlighting importance of simultaneous $D_{it}$ and $T_{body}$ scaling.

planar InGaAs substrates is more than $5 \times$ less compared to $D_{it}$ computed through calibrated TCAD model of experimental TFETs. This aggravation of $D_{it}$ is likely due to contribution from unpassivated defects at MESA sidewall surface (Fig.4.18b) which are produced within the MESA creation process itself.

III-V TFETs have achieved significant high $I_{ON}$ through tunnel barrier engineering. To demonstrate steep sub-thermal switching over multiple decades of $I_{DS}$ in conjunction with high $I_{ON}$, it is fundamental to minimize trap assisted parasitic conduction mechanisms and enhance control of gate-field on tunnel junction. As explained before, this can be achieved through: (i) lowering $D_{it}$ from novel sidewall passivation techniques and High-K/III-V gate stack optimization, and (ii) scaling of HTFET body thickness in vertical configuration.

### 4.2.2.2 Degradation with time: BTI analysis

Degradation of High-K dielectric/channel interfaces over time commonly expressed bias temperature instability (BTI) is one of the most critical device degradation mechanisms in conventional High-K MOSFETs. It is of paramount importance to characterize High-K dielectric/III-V channel interfaces in a HTFET to identify which High-k dielectrics ($\text{HfO}_2$, $\text{ZrO}_2$) provide the most defect immune interface
Figure 4.18: (a) Significant $D_{it}$ contribution occurs from HTFET side-walls while integrating gate-stack developed on planar MOSCAP substrates; (a) Sidewall passivation hence becomes a key ingredient to lower $D_{it}$ in vertical geometry HTFETs.

to III-V channel, over time. We will first present a brief overview of BTI in a conventional MOSFET.

BTI refers to a time-dependent instability in transistors that occurs during normal transistor operation over long term usage but it can be accelerated using bias and temperature stress. This instability manifests as increase in the threshold voltage $V_T$ of the MOSFET which is subsequently followed by reduction in $I_{ON}$ depending on the magnitude of $V_T$ shift. This eventually lowers the operating speed of CMOS circuits. For p-channel MOSFETs the gate bias is negative hence the term negative bias temperature instability (NBTI) is used and like-wise for n-channel MOSFETs the degradation is called positive bias temperature instability (PBTI) since the corresponding gate bias conditions is positive.

In BTI, charges from channel (positive in p-type and negative in n-type device) become trapped within the High-K gate dielectric, or any interfacial oxide layer or at the interface of gate dielectric with channel itself [67,68]. The difference in the location of the trapped charge manifests as different degradation features in the measured transfer characteristics ($I_{DS}$-$V_{GS}$). Trapped charge situated away from the inversion channel, within the gate oxide, causes weak Coulomb scattering and hence low channel carrier mobility degradation. As a consequence, the $I_{DS}$-$V_{GS}$

61
characteristics only displays a $V_T$ shift governed by $\Delta V_T = Q_{ox}/C_{ox}$. On the other hand if charges are trapped at interface-states, then due to their close proximity to the inversion layer they can cause strong Coulomb scattering and worsen the channel carrier mobility. At the same time the switching slope also degrades compared to the pre-stress characteristics.

BTI effects display a remarkable dependence on gate voltage and is frequently modeled using either the exponential or the power-law voltage acceleration model. BTI stress tests are conducted under accelerated conditions and using a time-evolution model, the FET lifetime (typically 10 years) is predicted at acceptable performance threshold. A voltage acceleration model is used to project from high stress test voltages to operation supply voltages. In our analysis, we will use the power-law equation for capturing the time evolution of BTI induced $V_T$ shift:

$$\Delta V_T = A \times t^n \times V_{G,\text{stress}}^T \times \exp \left( -\frac{E_A}{k_B T} \right)$$ (4.1)

where $t$ is the stress duration $V_{G,\text{stress}}$ is the stress voltage, and temperature is $T$. Moreover, $A$, $n$, $\Gamma$ and $E_A$ are the pre-factor, the time evolution exponent, the voltage acceleration factor, and activation energy, respectively [69]. Typical values of the time exponent, $n$, is measured to be in the range of 0.1 to 0.25.

We now resume on BTI characterization of High-K dielectric/III-V interfaces in HTFET. Unlike MOSFETs, HTFET feature high electron band-to-band (e-B2B) generation rate resulting from low tunnel barrier design ($E_{b,eff}$) which is localized at and near the tunnel junction (Fig.4.19a). Additionally, HTFET show significant tunnel junction electric field associated with abrupt tunnel junction design. Figure 4.19b depicts HTFET shows 50× higher e-B2B generation than a III-V homo-junction TFET, and over a 1000× more than Silicon TFET. At the same time, they have similar range of tunnel junction electric field as shown in Fig.4.19c. Presence of intrinsic tunnel junction electric field along with gate electric field can induce high trap density at gate oxide-channel interface ($D_{it}$) and in gate oxide bulk ($Q_{ox}$) especially near the tunnel junction thereby impeding the ability of the gate field to modulate the tunnel barrier. This makes evaluation of ultra-thin High-K dielectric/III-V channel interfaces necessary with BTI stress in HTFET.

In order to examine BTI in our devices we will use a widely used measure-stress-measure technique. In this technique, first a pre-stress reference transfer
Figure 4.19: (a,b) III-V Hetero-junction TFET (HTFET), using low $E_b^{eff}$, achieves highest electron band-to-band (eB2B) generation at tunnel junction compared to other TFETs. In conjunction with significant tunnel junction electric field (c) possible at low $V_{DS}$ in HTFET due to abrupt junction design, PBTI evaluation is necessary especially with ultra-thin High-K dielectrics/III-V interfaces.

characteristics ($I_{DS}$-$V_{GS}$) is recorded. This is followed by application of BTI stress for a specified duration. The time period of the stress is normally chosen on a logarithmic time base to cover several decades progression in time. Terminal voltages and currents at gate, source and drain electrodes are recorded in each stress cycle which are used in degradation models for lifetime prediction.
We use n-type HTFETs with three separately optimized high-performance sub-nm EOT High-K dielectrics for BTI evaluation: 3.5-nm thick HfO$_2$, 4-nm thick ZrO$_2$, and 4-nm thick HfO$_2$+ZrO$_2$ bi-layer. Capacitance-Voltage characteristics of these three High-K dielectric on In$_{0.53}$Ga$_{0.47}$As substrate is shown in Fig.4.20 [9,56]. Experimental DC characteristics of fabricated HTFETs are summarized in Fig.4.21. From the transfer characteristics shown in Fig.4.21(a-c), a high on-off current ratio of $10^5$ along with high on-current exceeding $100 \mu A/\mu m$ at $V_{DS} = 0.5V$ is observed indicating high performance HTFET. The output characteristics presented in Fig.4.21(d-f) reveal a distinct NDR peak in all the three HTFETs which establishes BTBT as dominant transport mechanism in on-state.

PBTI stress-test results on HTFETs with three gate stacks are presented in Figs.4.22 and 4.23. HTFETs with ZrO$_2$ and HfO$_2$+ ZrO$_2$ gate dielectric show significant switching slope (SS) worsening and concomitant $I_{OFF}$ degradation (Figs.4.22a and 4.22b). HfO$_2$+ ZrO$_2$ bi-layer gate stack performs worse than all-ZrO$_2$ gate stack. This can be attributed to additional charge traps accumulating between HfO$_2$ and ZrO$_2$ interface in the bi-layer stack. On the contrary, this trend is virtually absent in HfO$_2$ gate dielectric HTFET shown in Fig.4.22c which exhibits
only $V_T$ shift with negligible SS degradation.

Figure 4.22: (a-c) Transfer characteristics of HTFETs with the three gate stacks on application of PBTI stress: $V_{GS}$-$V_T$=0.85V and $V_{DS}$=0.05V. HfO$_2$ based HTFET shows superior performance. HfO$_2$+ZrO$_2$ based HTFET exhibits excessive SS and $I_{OFF}$ degradation.

A simplified analytical model is used to relate $I_{OFF}$ to PBTI induced trapped oxide bulk charge $Q_{ox}$ and interface charge $D_{it}$ (Fig.4.24a). Using this model, high SS degradation observed in ZrO$_2$ and HfO$_2$+ ZrO$_2$ dielectrics (Fig.4.23) can be
directly linked to significant PBTI induced interface $D_{it}$ creation. At the same time, HfO$_2$ HTFET due to negligible PBTI induced SS degradation, demonstrates lower PBTI induced $D_{it}$ compared to ZrO$_2$ and HfO$_2$+ZrO$_2$ HTFET. The analytical model estimates the average SS of HfO$_2$ HTFET with reasonable accuracy as shown from plot of log $I_{OFF}$ vs. $V_T$ in Fig.???. The horizontal $V_T$ shift observed in the $I_{DS}$-$V_{GS}$ characteristics of HfO$_2$ HTFET indicates only $Q_{ox}$ creation. Moreover, HfO$_2$ HTFET exhibits no PBTI generated worsening of off-state leakage and transconductance (Fig.4.24c) which is favorable for maintaining ultra-low power operation coupled with high-performance over long term.

Figure 4.25 illustrates the PBTI induced threshold voltage shifts $\Delta V_T$ in HTFET modeled using power law dependence from eqn. 4.1. This empirical fit which models $\Delta V_T$ is particularly useful for circuit designers in traditional CMOS technology as conventional circuit design relies significantly on $V_T$. Threshold voltage $V_T$ for HTFET is extracted using constant current method [56]. HfO$_2$ HTFET shows definite power law dependence in $\Delta V_T$ with time exponent factor $n$ =0.14. On the contrary, ZrO$_2$ and HfO$_2$+ZrO$_2$ bi-layer HTFET show either partial or no power law dependence due to excessive $I_{OFF}$ and SS degradation. In order to evaluate new emerging device technologies we emphasize that and $I_{ON}$, $I_{OFF}$ and SS variation is highly significant indicator besides $\Delta V_T$.

Lastly we present the device reliability lifetime benchmark of III-V HTFET with HfO$_2$ gate dielectric against state of the art III-V FinFET and Si-FinFET in Fig.4.26. It is observed that HfO$_2$ HTFET exhibits improved PBTI lifetime over III-V FinFET. Apparently, high-eB2B generation with high tunnel junction electric field is not detrimental to III-V HTFET reliability unlike reported elsewhere.
**I_{OFF}/SS degradation explanation through simplified model**

\[ I_{DS} = A V_{TH} E \exp(-B/E) \]

Where \( V_{TW} \) is tunnel window from band-overlap

\( E \) is maximum tunnel junction field

At \( V_{GS} = V_{OFF} \) and \( V_{DS} \ll V_{DD} \)

\[ V_{TW} = U_{\theta} \exp \left( \frac{V_{OFF} - V_{T}}{U_{\theta}} \right) \]

Where \( U_{\theta} = \gamma_{\theta} (\eta kT/q) = SS \)

\[ V_{OFF} = 0 \Rightarrow I_{OFF} = I^{*} \exp \left( -V_{T}/SS \right) \]

\[ I_{OFF} \approx I^{*} 10^{-V_{T}(Q_{OX}\cdot D_{t})/SS(D_{t})} \]

\( Q_{OX} \) = Bulk oxide trap charge density

\( D_{it} \) = Interface trap charge density

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Figure 4.24: (a) Simplified model for off-state current degradation in HTFET from PBTI induced gate-oxide bulk traps and interface-traps; (b) Average switching slope for HfO$_2$ HTFET extracted using this model using PBTI data; (c) Peak transconductance degradation is negligible in HfO$_2$ gate stack and worst in HfO$_2$+ZrO$_2$ bi-layer stack.

for Si-TFETs [70–72]. This can be attributed to electron sweeping action of the lateral tunnel junction field which can reduce the rate of \( D_{it} \) formation locally [73]. Additionally, Fig.4.26 also suggests that the gate overdrive for III-V HfO$_2$ HTFET, considering a lifetime of 10 years, is around 0.2 V which given their ultra-low threshold voltage makes them ideal for sub 0.5V applications.
Power law dependence of PBTI induced $\Delta V_T$ with $n=0.14$. ZrO$_2$ based HTFET show partial or no power law dependence due to off-current and switching slope degradation from PBTI induced high interface trap density.

Figure 4.25: PBTI induced $V_T$ shifts, extracted using constant current method. Threshold current is calculated from pre-stress transfer-curves, separately for each gate stack. HTFET based on HfO$_2$ exhibits power law dependence of $\Delta V_T = \alpha \times t^n$ with $n = 0.14$. ZrO$_2$ based HTFET show partial or no power law dependence.

Figure 4.26: III-V HTFET shows improved PBTI lifetime than III-V FinFET over entire stress voltage range.
4.3 Prescription for high performance TFET design

We summarize the key learnings from HTFET interface characterization in Fig.4.27 mapped onto TFET electrical characteristics. For high on-current an abrupt hetero-tunnel-junction design is absolute necessity both in terms of compositional switching as well as dopant profile. Change of compositional abruptness from 2.5nm to 1nm alone gives 38% improvement in on-current. To improve HTFET switching performance, engineering the High-K/III-V interface to attain simultaneous mid-gap $D_{it}$ scaling along with body thickness scaling is required. This helps in eliminating parasitic conduction mechanisms due to traps and ensures BTBT governs the switching performance. We will also mention that in state of the art technology, HfO$_2$ high-K gate dielectrics are more suitable as they are more immune to BTI stress. And finally, we highlight that off-state relies on quality of both the critical interfaces: hetero-tunnel-junction and High-K/III-V interface. A high source doping keeps a check on RDF induced degradation of off-current. However it can impact switching performance due to high source degeneracy, so a design trade-off exists. Primary reductions to off-state stem from reducing parasitic leakage floor from SRH recombination and suppressing contribution from interface traps which are crucial for high performance HTFET demonstration.

4.4 Complimentary HTFETs: Technology Projection

We conclude interface analysis by presenting projected performance improvements in complimentary HTFETs enabled by ultra-thin body geometry combined with extremely thin high-K dielectrics with low $D_{it}$. We used TCAD based Sentaurus device simulator to numerically model the TFET experimental characteristics and extended it to perform projections at scaled $T_{body}$. Poisson equation is self-consistently solved with the carrier-continuity equation to generate the simulated transfer characteristics as shown in Figs.4.28 and 4.29a. Fermi-Dirac statistics, Shockley-Read-Hall (SRH) generation-recombination and non-local band-to-band tunneling are some of the key models used to accurately simulate the transfer characteristics of HTFETs. While the body thickness of the fabricated device is approximately 500nm and mid-gap $D_{it} \geq 10^{13}$cm$^{-2}$ev$^{-1}$, it is evident from the calibrated numerical simulations (Fig.4.29a) that a combination of ultra-thin body
Figure 4.27: Key learnings from interface characterization for improving TFET electrical performance.

(T_{body} \leq L_g/3 for SRH G/R leakage reduction and better electrostatics) and reduced interface trap density (D_{it}) \leq 10^{12} \text{cm}^{-2} \text{ev}^{-1} will be needed for realizing sub-kT/q switching slope over many decades of I_{DS} on III-V TFETs [8].

We provide a brief insight here on benefit of complimentary III-V HTFET technology over conventional CMOS using example of a digital logic inverter circuit. Additional details regarding circuit simulation methodology will be introduced in the following chapter. Fig.4.29b shows a comparison of the energy dissipated per cycle versus delay for the improved HTFET and the 22 nm Si-FinFET. It is seen that HTFET is more energy efficient than MOSFET technology logic applications operating with 0.3V and below supply voltages. Not only the performance gains exist in circuit electrical performance but also in circuit layout area. Figure 4.30 shows 9-metal-track based standard cell layout for an FO1 inverter using FinFETs and HTFETs. FinFET device width set by the maximum number of fins (e.g. 4 for a 9-metal-track standard cell) provides an effective drive strength improvement of 13% for an inverter (INV1) (2\times H_{fin}/\text{fin-pitch}) over a planar MOSFET, assuming a fin-pitch of 60 nm and fin height H_{fin} of 34 nm at 22 nm node (Fig.4.30) [74].
the same layout area, HTFET improves the effective drive strength by 100% over planar MOSFET and by 77% over 22 nm Si-FinFET, benefiting from the double mesa edge gate structure.

Minimizing parasitic leakage contributions and engineering high-quality interfaces is the key for realizing high performance HTFETs with steep sub-kT/q SS for energy efficient logic and to beat the incumbent FinFET based leading edge MOSFETs. In order to translate the benefits at device level to circuit level with maximum efficiency, circuit design topologies initially tailored towards convention CMOS have to be optimized for HTFETs. We will elaborate further on HTFET circuit design techniques, design trade-off involved and ways to address them to leverage most out of HTFET, in subsequent chapter.
Figure 4.29: (a) Simulated Transfer characteristics of complementary HTFET with models described in Fig.4.28; (b) Energy vs. delay benchmark of a FO1 inverter comparing 22nm Si FinFET and III-V HTFET with 1% switching activity factor, at different operating voltages.
Figure 4.30: Device layout of (a) vertical P-HTFET and (b) vertical N-HTFET; (c) Layout illustration of a 9-metal-track standard cell library design. Layout area is determined by 9N x Gate-pitch x 9metal-pitch. N is number of gate-pitches in the lateral direction. Inverter layout of (d) Si FinFETs at a maximum fin number of 4 and (e) proposed complementary vertical HTFETs; (f) Layout induced device drive strength enhancement (effective device width at a given device area) comparing the INV1 using 22 nm planar MOSFETs, 22 nm FinFETs and 22 nm vertical HTFETs.
Chapter 5  |  TFET Circuit Design And Performance Benchmark

5.1 Introduction

TFET has emerged as a strong alternative to conventional MOSFET for low-voltage and low power applications. Steep switching characteristics of Hetero-junction TFET (HTFET) over subthreshold Si-FinFET is favorable for ultra low voltage digital logic (Fig. 5.1a). Additionally HTFET has much higher transconductance per bias current ($g_m/I_{DS} \sim$ intrinsic gain) compared to subthreshold Si-FinFET (Fig. 5.1b) which is beneficial for analog circuits. This advantage stems from steeper switching slope (SS) of HTFET ($g_m/I_{DS} = \log(10)/SS$). We here analyze example circuit design aspects of HTFET and compare it against conventional Si-FinFET circuit design. Our analysis focuses on sub-0.5 V operation regime, which is suitable for low power electronic applications. The Si-FinFET used in our simulations has $V_{Th} \sim 0.4V$, hence we will draw comparisons based on near-threshold or subthreshold Si-FinFET design versus HTFET design at a nominal operating voltage of 0.3 V.

Ensuring optimum design performance at low operating voltages and at scaled technology nodes is a great challenge, where electrical noise poses a serious reliability concern [75,76]. The low frequency noise sources, such as the random telegraph noise (RTN) and flicker noise, scale reciprocally with design footprint, which degrades the performance of both analog, mixed-mode circuits [77] as well as semiconductor memories [78, 79]. The threshold voltage ($V_{Th}$) fluctuation from RTN is shown to
exceed $3\sigma V_{Th}$ variation due to random dopant fluctuation (RDF) at sub-14-nm nodes [80] as the dominant source of variation in subthreshold MOSFET [81] (also Fig. 5.2a). Furthermore, the high frequency white noise sources, such as the channel thermal noise and the shot noise are detrimental to analog/RF applications [82]. Hence, a detailed analysis of electrical noise in HTFETs, starting from device level and extending to circuit level evaluation is presented in this work.

### 5.2 Electrical Noise Aware Differential Amplifier Design

We start with a brief introduction to major electrical noise mechanisms in transistors. The aggregate effect of low frequency flicker noise and random telegraph noise (RTN), along with high frequency shot and thermal noise is examined at both transistor level and circuit level using analytical noise models integrated in circuit simulators.
5.2.1 Electrical Noise Mechanisms

5.2.1.1 Random Telegraph Noise (Low Frequency)

The source of Random Telegraph Noise (RTN) in both HTFET and Si-FinFET is attributed to capture and emission of channel carriers by the interface traps [83]. However, as it has been reported for Si-TFETs [84], the HTFET RTN can be more pronounced when the trap is located near the source end of the channel. This is because a trapped charge near the source end can alter the junction electric field and affect the inter-band tunneling rate. Our goal is to explore the effect of drain current fluctuations (RTN amplitudes) induced by a trapping of an electron charge in an interface state at the gate oxide-channel interface. The RTN analysis for both HTFET and subthreshold Si-FinFET has been presented in a comparative fashion to bring out the key differences.

The simulation setup consists of a 2-D double-gate structure (extended in 3-D, in device simulation) with a nominal gate length of 20 nm and width 40 nm, for both n-type HTFET and n-type Si-FinFET. We used Sentaurus TCAD simulator for device simulations [60]. The gate oxide has equivalent oxide thickness (EOT) of 0.7 nm. The n-HTFET has GaSb source doped $10^{19}$ cm$^{-3}$ p-type, intrinsic InAs channel and InAs drain doped $10^{17}$ cm$^{-3}$ n-type. The n-Si-FinFET has source/drain doped $10^{20}$ cm$^{-3}$ n-type and a $10^{16}$ cm$^{-3}$ doped p-type channel. The body thickness $T_{body}$ (fin width) of Si-FinFET is 12 nm while HTFET uses a scaled body thickness of 7 nm corresponding to 20 nm channel length as described in [85]. TCAD device characteristics of Si-FinFET are calibrated against experimentally demonstrated Si-FinFET device whereas the characteristics of HTFET are calibrated against full-band atomistic simulations, details of which are presented in [86,87]. A dynamic nonlocal band-to-band tunneling model [60] is used to account accurately for the inter-band tunneling transitions in HTFET. The tunneling path is determined dynamically based on the energy band profile of the source-channel tunnel junction and generation rate is obtained through non-local path integration.

RTN due to a single charge trap is modeled by confining the charge trap to a single node (with predefined coordinates) of mesh, which is suitably refined to limit the speed degradation, while maintaining computational accuracy. A mesh spacing of 2 Å was used around the gate-oxide/channel interface to capture field perturbation due to interface charge trap. The trap concentration is computed automatically.
Figure 5.2: (a) Threshold voltage fluctuation $\Delta V_{Th}$ from RTN exceeds Random Dopant Fluctuation (RDF) induced $\Delta V_{Th}$ at sub-14 nm process technology nodes; (b) Calibration of TCAD RTN amplitudes against experimental results reported for p-Si-FinFET [88]. Inset: the Double-gate (DG) simulation structure; (c) Relative RTN amplitude dependence on trap depth and location along the channel for TFET and FinFET.

by Sentaurus TCAD simulator such that a filled trap always corresponds to one electronic charge [60]. The trapping of electron in the interface trap causes a degradation $\Delta I_D$ in the nominal drain current magnitude $I_D$. This is expressed in terms of relative RTN amplitude, $\Delta I_D/I_D$. The calibration of normalized RTN
amplitudes extracted from TCAD simulations against experimental RTN data reported for p-Si-FinFETs [88] is shown in Fig. 5.2b. An excellent match is achieved assuming mid-channel trap location which authenticates the methodology used for capturing RTN impact.

We first analyze the relative RTN amplitude dependence on trap location: (1) in the channel, from the source toward the drain and (2) on varying trap depth: trap in oxide, trap at gate-oxide/channel interface, and trap inside channel. The trap depth inside channel and inside oxide has been limited to 4 Å from the gate-oxide/channel interface. As observed from Fig 5.2c relative RTN amplitude is maximum when the trap is located inside channel followed by trap at the interface and it is minimum when the trap is inside gate oxide. Since we consider the channel to be defect free, our (worst case) analysis is based on the trap located at the oxide-channel interface, which produces the highest RTN.

We also identify that, for HTFET, the RTN amplitude is highest for a trap near source end (distance from source-channel junction, $X_t = 2$ nm), but not for trap almost exactly at source-channel metallurgical junction ($X_t = 0.1$ nm). This can be explained as follows: a single charge trap positioned at the oxide-channel interface causes a local reduction in the electric field in the channel region on the source side of the trap location. On the other hand, the field enhances in the channel region toward the drain side of the trap location (refer Fig. 5.3a). Reduction in the tunnel junction electric field degrades electron band-to-band tunnel current. The trap at location $X_t = 2$ nm in "net" produces a greater reduction in the tunnel-junction electric field magnitude, and hence produces relatively higher RTN amplitude [87].

In the case of Si-FinFET, an electron trap near source end is screened due to the high electron concentration in the channel [89], whereas a trap located near the drain end produces a small RTN amplitude due to the presence of the drain field [90]. The maximum RTN amplitude occurs on the source-side of the mid-channel region, which corresponds to $X_t = 7$ nm in our simulations. For further analysis, we will assume trap locations that result in the worst case RTN in HTFET ($X_t = 2$ nm) and in Si-FinFET ($X_t = 7$ nm) unless stated explicitly otherwise.

We model the relative RTN amplitude in HTFET analytically as [87]:

$$\frac{\Delta I_D}{I_D} = \left(\frac{2}{F} + \frac{B}{F^2}\right) \frac{\eta q}{\epsilon_{eh}WL}$$  \hspace{1cm} (5.1)
where $F$ is tunnel junction electric field, $B$ is dependent on carrier effective mass and tunnel barrier, $\epsilon_{ch}$ is the electrical permittivity of channel region, $q$ is electronic charge and $\eta$ is a fitting parameter [87]. Relative RTN amplitude in Si-FinFET is modeled from [91].

5.2.1.2 Flicker Noise (Low Frequency)

Flicker noise is the dominant noise at low frequencies, which arises from trapping/detrapping of carriers in trap states in the gate oxide around quasi-Fermi level, as shown in Fig. 5.4a. The flicker noise model for HTFET used in our simulations is carrier number fluctuation-based [92]:

$$\frac{S_{id}(f)}{I_D^2} = \left( \frac{2}{F} + \frac{B}{F^2} \right)^2 \frac{q^2 N_t}{\epsilon_{ox}^2 W L' \alpha f} \tag{5.2}$$

where $S_{id}(f)$ is the drain current noise power, $\alpha$ is the attenuation factor of carriers in gate oxide, $N_t$ is the interface trap density, while $F$, $B$, and $L'$ are all as defined previously [92].

The flicker noise of Si-FinFET in subthreshold regime, from correlated fluctuations in both channel carriers and mobility can be approximated by the following
Figure 5.4: (a) Flicker noise is caused by trapping/emission of carriers by trap states in oxide. (b) In TFET the drain current is controlled by the tunneling distance of carriers at the source-channel junction ($L'$).

Expression [77]:

$$\frac{S_{id}(f)}{I_D^2} = \frac{AKT}{\alpha fWLN^*}$$  \hspace{1cm} (5.3)

where $S_{id}(f)$ and $\alpha$ are as defined in Eqn. 5.2. Parameter $A$ is approximated as effective oxide trap density and $N^*$ is a function of gate capacitance as defined in [77].

5.2.1.3 Shot Noise and Thermal Noise (High Frequency)

The subthreshold thermal noise model [77] is used for Si-FinFET. For HTFET, we use the thermal noise model of on-state MOSFET, which is proportional to the channel conductance at zero drain-source bias [93]. However, the dominant form of high frequency noise in HTFET is shot noise. A current of electrons has small random fluctuations, which due to discrete charge present on each electron, gives rise to shot noise in measured current. Shot noise in TFET modeled similar to that of case of tunnel diodes:

$$i_{shot}^2 = 2qI_D \Gamma$$  \hspace{1cm} (5.4)

where $\Gamma$ is the Fano factor, which models the deviation of shot noise magnitude from the nominal Poissonian value of $2qI_D$ in TFET [87]. Unlike MOSFET, TFETs show higher shot noise. This is typical for tunnel devices where the forward and reverse components of tunneling current across the tunnel junction ($I_{CV}$ and $I_{VC}$, as shown in Fig. 5.5a), can enhance shot noise due to their individual contributions [94].
Figure 5.5: (a) Shot noise across tunnel junction can enhance due to individual contributions from forward and reverse tunnel currents; (b) Representation of flicker, shot, and thermal electrical noise models (noise current sources) implemented at transistor level.

The device level HTFET and Si-FinFET electrical noise models were implemented as flicker and white noise sources in Verilog-A-based code for circuit level simulation in the Cadence Spectre circuit simulator (Fig. 5.5b). The corner frequency distinguishing flicker noise dominant noise spectrum against white noise (shot and thermal noise) for HTFET is typically \( \sim 1 \text{ GHz} \). We assume an interface trap density of \( 5 \times 10^{11} \text{ cm}^{-2} \) and \( 10^{12} \text{ cm}^{-2} \) for Si-FinFET and HTFET respectively. Both HTFET and Si-FinFET have width of 1 \( \mu \text{m} \), gate length of 20 nm, and equivalent oxide thickness (EOT) of 0.7 nm.

### 5.2.2 Electrical Noise: TFET vs. FinFET (Device Performance)

Figure 5.6a shows the trend of relative RTN amplitude on with physical gate length (L\text{g}) scaling. For Si-FinFET, the RTN amplitude increases with L\text{g} scaling which is consistent with [83]. However, in the case of HTFET, the RTN amplitude remains almost constant with physical gate length scaling. This is expected in HTFET, where the drain current is controlled by the tunneling distance of carriers at the source-channel junction [92] which remains constant and significantly small compared to L\text{g} as shown in Fig. 5.6a. This translates into approximately 40\% reduced percent fluctuations in the drain current in HTFET over Si-FinFET, at gate lengths of around 20 nm at 0.3 V, which is an important reliability measure.
Figure 5.6: (a) TFET RTN does not increase inversely with gate length scaling as tunneling distance of carriers shows weak dependence on gate length; (b) At 100KHz, TFET provides a $\sim 1.5 \times$ less input referred noise ($S_{V_G}$) from higher intrinsic gain ($g_m/I_D$); (c) At 10GHz, shot noise causes the input referred noise of TFET to cross-over and exceed the input referred noise of FinFET for RTN [90].

Figures 5.6b and 5.6c show the aggregate electrical noise performance consisting of flicker, shot and thermal noise at two different frequencies 100KHz and 10GHz respectively. HTFET benefits from its higher intrinsic gain ($g_m/I_D$) compared to FinFET, which reduces its input referred noise power ($S_{V_G}$) esp. at low frequencies (Fig. 5.6b). At a high frequency of 10GHz a cross-over in HTFET and Si-FinFET $S_{V_G}$ characteristics is observed as the shot noise of tunnel junction becomes more pronounced as seen in Fig. 5.6c.

### 5.2.3 Differential Amplifier Circuit Design and Electrical Noise Assessment

The electrical noise models for flicker, shot, and thermal noise were implemented in a differential amplifier with active load (a single stage op-amp.) to analyze the noise performance of HTFET versus subthreshold Si-FinFET-based circuit design. The circuit (schematic shown in inset of Fig. 5.7a) was optimized separately for subthreshold Si-FinFET and HTFET designs with load capacitance $C_L = 0.1 \text{ fF}$ (comparable with gate capacitance) to achieve a similar range of gain with certain design restrictions such as, minimum gain of 10 dB, maximum power dissipation of $\mu W$, and input referred noise in the range $\mu V/\sqrt{Hz}$.

The ac response of both HTFET design and Si-FinFET design is shown in
Fig. 5.7a. Figure 5.7b lists the specifications and performance metrics of the circuit for both HTFET and Si-FinFET design. Note that the HTFET design has same transistor sizing (iso-area design) as Si-FinFET for fair electrical noise comparison. The HTFET design offers two times higher gain at 17.4% less power as compared with the subthreshold Si-FinFET. The 3-dB cutoff frequency is 4.6 times higher in HTFET design with respect to Si-FinFET design. A high differential gain in HTFET design improves the power supply noise rejection capability by approximately six times over Si-FinFET.

Figure 5.7c compares the input referred noise of HTFET design and Si-FinFET-based diff-amp design. A higher gain of HTFET design reduces its input referred noise by approximately three times as compared with Si-FinFET. For a given bandwidth, e.g., 1 MHz, the input referred noise voltage for HTFET and Si-FinFET (which defines the minimum limit on input signal distinguishable from device noise) is 28 and 81 µV, respectively. Thus, HTFET design can detect smaller signal amplitudes without corruption from electrical noise.

The performance of HTFET and Si-FinFET design at different bias currents, with regard to gain, input referred noise (at 1-MHz bandwidth) and power dissipation metrics is compared in Fig. 5.7d. At low bias currents, the intrinsic gain $g_m$ of the transistors is small, which results in an overall small gain of the design. HTFET design still shows improved gain due to higher $g_m$ of HTFET as compared with Si-FinFET. At higher bias current, the gain of Si-FinFET design saturates at around 11 dB, as the output resistance of Si-FinFET degrades with increase in bias current, making the overall gain almost constant. Whereas in HTFET, the improvement in $g_m$ at higher drive current surpasses the degradation in output resistance, resulting in a net increased gain.

The input referred noise characteristics in Fig. 5.7d indicate HTFET design shows reduced input referred noise as compared with Si-FinFET, for bias currents of 0.7 µA and higher, which is attributed to improved gain of HTFET at increased bias current. Finally, Fig. 5.7d also shows that the HTFET design can be biased at higher ON-current to take advantage of high gain and reduced input referred noise features, while still maintaining a low power operation due to its reduced supply voltage as compared with Si-FinFET design.

Additionally, given the exponential dependence of drain current on threshold voltage coupled with low on-currents in the subthreshold regime, it is more difficult
In this work, we have performed an analysis of electrical specifications of HTFET-based analog mixed signal circuit design more suitable for low-voltage/low-power applications. The specifications make HTFET-based design a desirable feature for reliable biasing circuits. Hence, the overall design specifications make HTFET-based analog mixed signal circuit design more suitable for low-voltage/low-power applications.

**Figure 5.7:** Differential amplifier (Diff-Amp) with active load: TFET versus FinFET. (a) Schematic and ac response; (b) Specifications of Diff-Amp design; (c) Input referred noise dependence on frequency; (d) Gain, input noise, and power dissipation of the design at different bias currents.

<table>
<thead>
<tr>
<th>Specification</th>
<th>HTFET</th>
<th>Si-FinFET</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{dd}$</td>
<td>0.4 V</td>
<td>0.6 V</td>
</tr>
<tr>
<td>Power</td>
<td>1.9 μW</td>
<td>2.3 μW</td>
</tr>
<tr>
<td>Gain</td>
<td>17.3 dB</td>
<td>11.3 dB</td>
</tr>
<tr>
<td>3dB freq. ($f_c$)</td>
<td>457 MHz</td>
<td>100 MHz</td>
</tr>
<tr>
<td>Input noise (at 1MHz)</td>
<td>28 μV</td>
<td>81 μV</td>
</tr>
<tr>
<td>Phase Margin</td>
<td>92°</td>
<td>79.6°</td>
</tr>
<tr>
<td>CMRR</td>
<td>21.0 dB</td>
<td>25.8 dB</td>
</tr>
<tr>
<td>PSRR</td>
<td>28.5 dB</td>
<td>13.3 dB</td>
</tr>
</tbody>
</table>

W/L (same for both designs): | 77.5/0.02, 55/0.02, 2.5/0.02

M1-M2, M3-M4, Mb

(μm/μm)

Increased screening of the charge trap from higher channel carrier concentration in HTFET, accompanied by the weak dependence of RTN on the physical gate length scaling concerns. Our evaluation on flicker, shot and thermal noise in intrinsic gain and drive current of HTFET, besides benefitting reduced input referred noise, by taking advantage of high gain of HTFET at increased bias current. Lastly, HTFET design can be biased at higher on-current to take advantage of high gain and reduced output resistance as compared to subthreshold CMOS design. Additionally, given the power operation due to its reduced supply voltage as compared to Si-FinFET design. The input referred noise increases exceeding 0.3 V with frequency range of 10 GHz and higher. The effect of temperature change on HTFET on-current is negligible, which is another desirable feature for reliable biasing circuits. Hence, the overall design specifications make HTFET-based analog mixed signal circuit design more suitable for low-voltage/low-power applications.
5.3 Memory design: RTN Aware TFET SRAM Analysis

Random Telegraph Noise (RTN) is a prominent source of threshold voltage $V_{Th}$ fluctuation in MOSFETs. For sub-14 nm technology nodes, $V_{Th}$ fluctuation from RTN is expected to exceed that from random dopant fluctuation [80], which has been so far the dominant source of variation for sub-threshold MOSFETs. Since RTN scales inversely with the device footprint, it makes SRAM design most vulnerable to RTN due to minimum-sized transistors used in the cell. Hence, it is of great significance to explore RTN immunity of SRAM designs using CMOS and post CMOS device technologies.

5.3.1 TFET Schmitt-Trigger based SRAM Design

Due to the uni-directional conduction in HTFET resulting from its asymmetric source-drain architecture, 6T HTFET SRAM cannot perform simultaneous read and write operation [86]. 6T SRAM shows significant degradation in Read Noise Margin (RNM) due to RTN as shown later (Fig. 5.10a). Hence, we explore the RTN tolerance of Schmitt Trigger (ST) mechanism based ST2 SRAM topology which has been shown to exhibit variation immunity and to be suitable for ultra low Vcc operation [98]. We will use the same transistor sizing scheme as adopted in [86] in order to draw comparison between the RTN performance of HTFET and Si-FinFET based ST2 SRAM.

5.3.2 RTN inclusion in SRAM Simulation

Each transistor exhibits a variation of threshold voltage, $\Delta V_{Th}$, caused by trapping and de-trapping of the charge carriers at the interface trap site. Hence, the RTN in each transistor of an "n-Transistor" SRAM cell produces $2^n$ unique RTN cell-variants [99]. We analyze all $2^n$ combinations to identify the worst case impact on SRAM read/write noise margins from RTN and to examine the RTN induced variation immunity of the SRAM cell. A limitation of this approach [99] is it does not capture the time evolution of RTN. However, since we are quantifying the worst case RTN induced degradation across two different technologies, the current
The drain current fluctuation, $\Delta I_D$, from RTN as modeled analytically in section 5.2.1.1, is transformed into $\Delta V_{Th}$ through the transconductance $g_m$ at each bias point ($g_m = \Delta I_D / \Delta V_G$), similar to the approach used in [100]. This fluctuation in $V_{Th}$ due to RTN is integrated into the SRAM design for circuit level simulation in the Cadence Spectre circuit simulator.

5.3.3 Noise Margin Evaluation

A 10T ST2 SRAM cell in read mode is shown in Fig. 5.8a. Due to RTN in each transistor, a total of 1024 cell combinations are possible. The read noise margin (RNM) distribution is depicted in Fig. 5.8b at $V_{cc} = 0.25V$. The intrinsic RTN-free RNM for HTFET and FinFET ST2 SRAM is 83.9 mV and 81.7 mV, respectively.
Figure 5.9: Percent change in ST2 SRAM: (a) Read Noise Margin, and (b) Write Noise Margin indicates that TFET ST2 SRAM is more immune to RTN induced variation.

Higher $I_{on}$ and $I_{on}/I_{off}$ ratio of HTFET improves the intrinsic RNM of HTFET ST2 SRAM over Si-FinFET in the presence of worst case RTN (Fig. 5.8(c-d)).

Both read noise margin (RNM) and write noise margin (WNM) of the SRAM are computed in similar fashion as a function of supply voltage ($V_{cc}$). RTN can not only degrade noise margin (worst case RTN impact) but also can enhance it (best case RTN impact). Both class of changes in the SRAM noise margin are captured with $V_{cc}$ scaling in Fig. 5.9, which is essential to verify RTN tolerance of the SRAM cell. HTFET ST2 SRAM displays a symmetric change in noise margin (best case /worst case RTN) for both read and write operation whereas Si-FinFET SRAM shows significant RNM degradation (> 30%) sub-0.2V due to extremely low on-currents in RTN affected subthreshold devices (which also deteriorates Schmitt feedback mechanism [98] and hence the noise margins). Hence, HTFET ST2 SRAM exhibits overall better immunity against RTN induced variation in noise margin in contrast to subthreshold Si-FinFET ST2 SRAM, at ultra-low $V_{cc}$. At $V_{cc} = 0.15$ V, with worst RTN, HTFET ST2 SRAM offers 15.8% and 17.2% improvement in RNM and WNM over Si-FinFET.
5.3.4 TFET vs. FinFET SRAM: Performance Benchmark

It is important to compare the RTN performance of iso-area 6-Transistor (6T) Si-FinFET SRAM against 10T ST2 HTFET SRAM as the influence of RTN diminishes in upsized transistors. In order to meet the iso-area condition, the 6T Si-FinFET SRAM uses 4× sized transistors [86] which results in improved RNM over 1× sized 6T SRAM, as depicted in Fig. 5.10a. Still the RNM of 4× sized 6T Si-FinFET SRAM is 43% less that of 10T ST2 HTFET SRAM (with trap distance, $X_t = 2$ nm from tunnel junction) at $V_{cc} = 0.175$V, and hence the performance of ST SRAM design remains superior due to Schmitt feedback action. RNM of 10T ST2 Si-FinFET SRAM improves at higher $V_{cc}$ as Si-FinFET gains in on-current as it transitions out of subthreshold operation regime ($V_{Th} \sim 0.4$V).

The average power consumed by 256×256 SRAM array with an activity factor of 5%, using an approach similar to [86], is shown in Fig. 5.10b along with read access delay in Fig. 5.10c. At $V_{cc} = 0.175$ V, HTFET ST2 SRAM ($X_t = 2$ nm) exhibits 75× and 21× faster read-access times as compared to FinFET ST2 SRAM and FinFET 6T-4× sized SRAM respectively.

In HTFET, RTN from the trap at tunnel junction is prominent only for $V_{GS} < 0.1$V [87]. Hence, as $V_{cc}$ scales down to 0.13 V and below (Fig. 5.10a), RTN from trap at tunnel junction produces worse SRAM RNM than RTN from the trap at $X_t = 2$ nm. However, the lower limit on $V_{cc}$ (Vcc-min) is set by a minimum RNM requirement of 26 mV ($kT/q$, $T = 300K$). This Vcc-min exceeds 0.13 V for all SRAM designs discussed in this work (refer Fig. 5.10d). Hence the effect of trap at the tunnel junction is not pronounced for practical SRAM $V_{cc}$ range and consequently, the trap at $X_t = 2$ nm gives rise to the worst case RTN.

The average power consumption and read-access delay of Si-FinFET ST2 and 6T-4X sized SRAM, normalized against HTFET ST2 SRAM, at their respective Vcc-min for worst case RTN, is shown in Fig. 5.10d, indicating power savings (besides improved variation tolerance) in HTFET design at ultra-low Vcc applications.
Figure 5.10: (a) RNM of 10T ST2 SRAM compared against 6T SRAM (b) Average power consumption of 256×256 SRAM array with 5% activity factor; (c) Read-access delay; Note for TFET SRAM, plots for 2 different trap locations: trap at tunnel junction and at 2 nm away from tunnel junction (worst case RTN) are shown for reference; (d) Performance at Vcc-min limit with worst case RTN
6.1 Summary and Conclusion

We highlight key achievements in this dissertation below:

- **Ultra-thin High-K dielectric gate stack demonstration on III-V As-Sb substrates for complimentary HTFETs:** We developed extremely scaled (0.8 nm EOT) High-K gate dielectrics (HfO$_2$) on p-type GaAs$_{0.35}$Sb$_{0.65}$ channels for PTFET and (HfO$_2$, ZrO$_2$ [9]) on n-type In$_{0.65}$Ga$_{0.35}$As channel for NTFET. The gate dielectrics feature low gate leakage density $\leq 100$mA/cm$^2$ coupled with best in class $D_{it}$ ($= 10^{12}$-10$^{13}$cm$^{-2}$eV$^{-1}$, Terman method) demonstrated in As-Sb material system. Both P- and N-TFET gate stacks achieve a maximum accumulation capacitance density ($C_{max}$) of 3.5 µF/cm$^2$ along with record high C-V modulation, $(C_{max}-C_{min})/C_{max} = 97\%$ at 1 MHz ($C_{min}$ is the minimum depletion capacitance). High performance gate stacks are key ingredient towards realizing complimentary HTFETs with high $I_{ON}$ and high $I_{ON}/I_{OFF}$ ratio along with steep switching slope.

- **Complimentary III-V HTFETs device demonstration with high $I_{ON}$ and steep switching performance at $|V_{DS}|=0.5$V:** We demonstrated an all III-V semiconductor system based complimentary hetero-junction TFETs that can operate at a low supply voltage (<0.5V) and deliver a high on-current along with steep switching characteristics. The PTFET shows $I_{ON}=30$µA/µm at $I_{ON}/I_{OFF}=10^5$ at $V_{DS}=-0.5$V. At the same time, NTFET delivers $I_{ON} =275$µA/µm at $I_{ON}/I_{OFF}=3 \times 10^5$ at $V_{DS}=0.5$V. Using fast-$I_{DS}$-$V_{GS}$ measurements, a switching slope (SS) of 115 mV/decade in PTFET and
55 mV/decade in NTFET (sub-thermal SS) is demonstrated for the first time at room-temperature. The high $I_{ON}$ with sub-$kT/q$ SS demonstration for NTFET and high $I_{ON}$ with improved SS demonstration in case of PTFET, is a direct consequence of engineering high-quality scaled gate dielectrics and tunnel barriers in the As-Sb system.

- **Novel critical interface characterization techniques to boost HTFET device performance:** HTFETs comprise of combination of III-V materials along with ultra-thin High-K dielectrics which necessitates abrupt and uniform interfaces among dissimilar materials. Variation at these critical interfaces, e.g., III-V hetero-junctions, drastically degrades device performance. To improve TFET on-current we characterized the tunnel junction using 3D-atom probe tomography to arrive at optimal doping and composition parameters for tunnel junction. We explored the impact of tunnel junction abruptness and source dopant fluctuations on HTFET performance. We also performed temperature and electric-field dependent High-K/III-V channel interface characterization coupled with calibrated TCAD simulations to identify key bottlenecks towards efficient switching characteristics. Moreover, we evaluated extremely scaled High-K gate dielectric (0.8 nm EOT: HfO$_2$, HfO$_2$+ZrO$_2$ bi-layer, and ZrO$_2$) interface to III-V channel for defect tolerance using accelerated stress (BTI) measurements on TFETs. We show that III-V HTFET can out-perform conventional III-V FinFET even in long term reliability aspect.

- **Circuit design using III-V HTFETs:** It is highly significant to assess the performance of novel HTFET devices in circuit environment. This was accomplished by employing TCAD and Spice simulations calibrated to experimental TFET characteristics. We evaluated digital logic circuits as well as semiconductor memory and analog circuits based on TFETs and compared to corresponding CMOS implementations. HTFET circuits provided significance performance benefits along with energy savings in each of these categories. Comprehensive analysis of electrical noise in III-V HTFET is performed and compared against subthreshold Si-FinFET. HTFET exhibits superior electrical noise performance when contrasted with subthreshold Si-FinFET. It was found that Random Telegraph Noise (RTN) amplitude does not scale
inversely with gate length in HTFET and is governed by tunneling distance of carriers at source-channel junction. HTFET exhibits 40% less relative RTN amplitude at \( V_{cc} = 0.3 \text{V} \) at gate lengths around 20 nm, over subthreshold Si-FinFET. Aggregate analysis of flicker, shot, and thermal noise indicate HTFETs competitive noise performance in MHz frequency range, over Si-FinFET. However, in the frequency range exceeding 10 GHz, with \( V_{cc} > 0.3 \text{V} \), HTFET input noise becomes worse due to the dominance of shot noise. A differential amplifier with active load is used to demonstrate that high intrinsic gain, drive current, and output resistance of HTFET can be used to achieve superior mixed signal performance metrics in HTFET design over Si-FinFET design, at an improved electrical noise performance. Additionally we analyzed impact of RTN in HTFET based SRAM for the first time. HTFET Schmitt trigger (ST) mechanism-based SRAM offers 15% improvement in read-write noise margins along with better variation immunity from RTN over Si-FinFET ST SRAM. In addition, HTFET ST SRAM exhibits 48\( \times \) lower read access delay and 1.5\( \times \) reduced power consumption over Si-FinFET ST SRAM, operating at their respective \( V_{cc}\)-min.

- Evaluation of TFET design with group IV semiconductors: Extensive assessment of TFET design using group IV semiconductors is presented in section 6.2.2 with especial emphasis on PTFETs. TFETs using Group IV semiconductors in general suffer from extremely low on-current due to their large indirect band-gap which results in inferior tunnel transmission compared to III-V semiconductors with smaller and direct band-gap. Reducing Group-IV semiconductor band-gap and turning them into direct band-gap materials (e.g., by introducing Sn in Ge [101]) will enable TFETs with high-\( I_{ON} \) along with steep switching capability leveraging their low \( D_{it} \) advantage over III-V semiconductors. Ge and GeSn TFETs with homo- and hetero-junction design are presented starting from ab-initio DFT band-structure calculations and building to numerical TCAD simulations accounting for both direct and phonon assisted indirect BTBT processes (refer section 6.2.2). It is shown that hetero-junction Ge/Ge\(_{0.96}\)Sn\(_{0.10}\) p-TFET provide optimal \( I_{ON} \) and steep sub-\( kT/q \) SS at \( N_S \sim 10^{19}\text{cm}^{-3} \) through combined benefits of low source-to-channel tunnel barrier, reduced source degeneracy and dominant direct BTBT process.
Successful realization of ultimate energy efficiency is not easy and multiple challenges still exist towards making TFET a robust CMOS replacement. However, with further advances in engineering high-quality semiconductor interfaces, TFETs have strong potential for offering a complimentary low power alternative to CMOS.

6.2 Future work

6.2.1 Improving III-V HTFETs

We first discuss potential opportunities to boost n-type HTFET performance. As illustrated in Chapter 2 ZrO$_2$ gate dielectrics provide significant improvement in $I_{ON}$ and SS by tighter coupling of gate electric field to the tunnel-junction, a benefit from increased dielectric constant. However, interface reliability of present ZrO$_2$ is worse compared to HfO$_2$. One reason behind this limitation is the growth quality of ZrO$_2$ gate-stack itself which although provides significant improvement in $I_{ON}$ and SS, still is more leaky compared to HfO$_2$ films of same thickness which indicates inefficient nucleation of dielectric films.

EOT scaling can be enabled from using ZrO$_2$ compared to HfO$_2$, however first the ZrO$_2$ gate stack needs more interface optimization to check gate leakage. Figure 6.1 presents n-type HTFETs from 3 nm ZrO$_2$ gate stack. Superior DC characteristics and subthreshold slope (86 mV/decade compared to 102 mV/decade in earlier demonstration [8]) are obtained. On the other hand the gate leakage of 3nm-thick ZrO$_2$ is higher (Fig 6.1c). This is combined with large gate-pad and source-pad overlap in present device geometry which increases the gate-source current in excess of drain current. Still the gate field is able to effectively modulate the tunnel junction as is visible from high degree of drain current modulation even in presence of high gate-source current and also NDR in output-characteristics TFET (Figs. 6.1a and 6.1d). Further gate stack optimization particularly towards achieving high-quality scaled ZrO$_2$ films on III-V substrates with improved interface and low leakage current can drastically benefit on-state and switching performance of HTFETs.

Besides improving High-$\kappa$ dielectric/In$_{0.65}$Ga$_{0.35}$As interface $D_{it}$, body thickness ($T_{body}$) scaling was also highlighted as an crucial element to allow sub-thermal switching over wide range of drain current. Scaled $T_{body}$ III-V TFETs can be
realized by using of Cl₂ based plasma dry etch chemistry to perform high temperature In₀.₆₅Ga₀.₃₅As etch [66]. However in hetero-junction TFETs particularly GaAs₀.₄Sb₀.₆-In₀.₆₅Ga₀.₃₅As material system, etch optimizations become more sophisticated owing to two different material layers comprising the tunnel-junction. In Fig. 6.2, we show our recent effort on reducing T_{body} using Cl₂/N₂ plasma based etch optimized at 160°C. Detailed fabrication recipe is presented in Appendix B. We are able to scale diode MESA with T_{body} ~ 50 nm and even below as illustrated in Fig. 6.2a, 6.2b, and 6.2c. However p-i-n diodes fabricated from this process (Fig. 6.2d) show degraded diode ideality factor (n=1.4) signifying increased trap-
assisted generation/recombination. This is attributed to increased $D_{it}$ near tunnel junction resulting from interaction of $N_2$ plasma with GaAs$_{0.4}$Sb$_{0.6}$ source layer at elevated temperatures. From our work on pre-ALD surface treatments we have learnt that $H_2$ plasma is more suitable towards GaAs$_{0.4}$Sb$_{0.6}$ semiconductor surfaces, contrary to In$_{0.65}$Ga$_{0.35}$As which attains improved passivation in presence of $N_2$ plasma. Further optimizations are ongoing on this process, the most promising being controlled removal of the bulk of In$_{0.65}$Ga$_{0.35}$As channel layer using Cl$_2$/N$_2$ plasma dry etch till just before reaching the tunnel-junction and subsequently performing a digital wet etch on remaining In$_{0.65}$Ga$_{0.35}$As [102] to reach underlying GaAs$_{0.4}$Sb$_{0.6}$ layer. The digital etch recipe is also developed at Penn-State and illustrated in Fig. 6.3 and is essential for eliminating dry-etch damage and exposing the tunnel-junction with minimal $D_{it}$.

For III-V p-type HTFETs, engineering high quality interface with low $D_{it}$ particularly on GaAs$_{0.35}$Sb$_{0.65}$ channel is of prime necessity. We present our recent progress on this gate stack in Fig. 6.4. An interfacial-layer of Al$_2$O$_3$ is introduced before depositing 3.5 nm thick HfO$_2$. From the measured capacitance voltage characteristics shown in Fig. 6.4a, $D_{it}$ is extracted using Terman method (Fig. 6.4b). A moderate reduction in near band-edge $D_{it}$ is observed however near mid-gap $D_{it}$ shows no significant change. P-type HTFET made using this gate stack reveals definite improvement in minimum switching slope (Fig. 6.5) which improves from our earlier best demonstrated value of 171 mV/decade [8] to 155 mV/decade with this recipe. However further efforts towards reducing mid-gap $D_{it}$ are vital for steep switching in GaAs$_{0.35}$Sb$_{0.65}$ channel based p-type HTFETs.

Moreover III-V p-type HTFETs will also benefit from body-thickness scaling similar to n-type HTFETs. However as described before, the high temperature plasma dry etch necessary to achieve vertical sidewall profile has to be changed from $N_2$-based plasma to $H_2$-based plasma for suitability towards etching GaAs$_{0.35}$Sb$_{0.65}$ surface with low plasma induced semiconductor damage.

III-V TFETs have achieved significant high $I_{ON}$ through tunnel barrier engineering. To demonstrate steep sub-thermal switching over multiple decades of $I_{DS}$ in conjunction with high $I_{ON}$, it is fundamental to minimize trap assisted parasitic conduction mechanisms and enhance control of gate-field on tunnel junction. As explained before, future efforts should focus on: (a) lowering $D_{it}$ from novel sidewall passivation techniques and High-$\kappa$/III-V gate stack optimization, and (b) scaling
Figure 6.2: (a-c) Scaling of body thickness achieved to N₂/Cl₂ etch chemistry based dry etch optimized at 160°C. (d) P-i-n diodes with T\textsubscript{body} ∼ 50 nm fabricated using this method.

of TFET body thickness in vertical configuration.

### 6.2.2 Exploring TFET design in Group IV semiconductors

Group IV materials such as Germanium (Ge) are conducive to direct monolithic integration on silicon substrate with comparatively less defect density than compound semiconductors. Figure 6.6 presents the average mid-gap D\textsubscript{it} along with conduction band density of states (DOS) in state of the art group III-V and group IV semiconductor material systems. Unlike High-K gate-dielectric/III-V channel interface, where high density of interface states (D\textsubscript{it}) has become a significant chal-
Self-limiting sidewall digital etch (DE)

- InGaAs sidewall self-limiting surface oxidation in O₂/He low power plasma, 150s
- Native oxide reduction using Citric Acid, 60s

Etch rate = 2nm/cycle

Figure 6.3: Digital etch is developed to achieve self-limiting etch of In₀.₆₅Ga₀.₃₅As layer to form HTFET sidewalls with minimal Dᵢᵣ.

![Image of etch process](image)

Figure 6.4: (a) Gate stack optimization for GaAs₀.₃₅Sb₀.₆₅ channel p-type HTFET; (b) Lower band-edge Dᵢᵣ is achieved however mid-Gap Dᵢᵣ is still significant.

Challenge for achieving steep sub-kT/q switching slope (SS) in Tunnel FET (TFET) [8], High-K dielectric integration on Ge has achieved more success with lower Dᵢᵣ [103]. Benefit of higher DOS coupled with lower Dᵢᵣ is favorable for TFET design, however group IV TFETs in general have suffered from low on-currents from higher energy band-gaps. Recent technology advancements have demonstrated promise of low
Figure 6.5: Hetero-junction PTFET fabricated on wafer (a) with gate stack from Fig. 6.4 using TFET fabrication procedure as described in Chapter 3; (b) Transfer, (c) Switching and (d) Output characteristics of PTFET.

band-gap by tuning Sn composition in Ge to tailor it for low power TFET design (Fig. 6.7).

However indirect energy band-gap of Ge severely limits the tunnel efficiency and produces dominant relative contribution of indirect band-to-band tunneling (BTBT) versus direct BTBT [104]. Indirect BTBT in Ge is assisted by phonon absorption process resulting in a potential dilution of switching slope. With introduction of Sn in Ge the direct tunneling component increases and at it has been reported Ge$_{1-X}$Sn$_X$ transitions to a direct band-gap semiconductor around Sn mole-fraction X=8% [101]. However growing Ge$_{1-X}$Sn$_X$ with such high Sn mole-fraction without
Figure 6.6: Group IV semiconductors show lower mid-gap D_{it} and higher conduction band DOS over III-V compound semiconductors.

defects has been a significant challenge in past and is subject of active ongoing research.

Figure 6.7: Group IV semiconductors have large indirect band-gaps which results in inferior tunnel transmission compared to III-V semiconductors which possess smaller and direct band-gap. Efforts to reduce Group-IV semiconductor band-gap and turning them into direct band-gap materials (e.g., by introducing Sn in Ge) is necessary to harness their low D_{it} advantage for high performance TFET design.

In this work, we first perform a rigorous investigation of p-channel TFETs (p-TFET) in Ge and GeSn material system using a combined frame-work of first principles density functional theory (DFT) and device level TCAD simulation [105](Fig. 6.8). Trade-off between efficient realization of sub-kT/q SS coupled with high on-current (I_{ON}) is presented through detailed analysis of band-gap engineering, controlling source-channel tunnel injection through source doping concentration, and balancing the direct vs. indirect BTBT process.
In order to perform holistic TFET device characteristics assessment we need accurate information on semiconductor band-gap, band-alignment, DOS (Density of States), along with electron and hole carrier effective masses. We perform ab initio density functional theory (DFT) simulations to compute these parameter sets for Ge, Ge$_{1-X}$Sn$_X$, and Ge$_{1-X}$Sn$_X$ on Ge material systems. Figure 6.8 shows the band-structure computed for Ge$_{1-X}$Sn$_X$ at Sn mole-fraction X=2% and 10% respectively. Ge$_{1-X}$Sn$_X$ undergoes band-gap transition from indirect (Γ → L) at X=2% to direct (Γ → Γ) at X=10% as depicted in Fig. 6.9a. The electron and hole multi-valley band-structure along with dynamic non-local path BTBT models are implemented in TCAD numerical simulator [60]. As depicted in Fig. 6.8, BTBT at source/channel junction has two distinct components: (1) Indirect BTBT (Γ → L), and (2) Direct BTBT (Γ → Γ). We evaluate each of these two BTBT components.

Phonon-assisted indirect BTBT process parameters: energy and occupation number of transverse acoustic phonon, deformation potential and mass density, are also obtained from DFT, details on which are presented in Appendix. C. The simulated p-TFET dimensions are also shown in Fig. 6.8. A brief summary of carrier effective mass and band-gap as obtained from DFT is presented in Fig. 6.9b. It is noteworthy that Ge$_{0.90}$Sn$_{0.10}$ on Ge has 1.1% compressive bi-axial strain. This strain counteracts the band-gap reduction from Sn incorporation in Ge (Fig. 6.9b). This effect is taken into account in evaluation of hetero-junction Ge/Ge$_{0.90}$Sn$_{0.10}$ p-TFET. To encompass all possible tunnel junction designs in Ge$_{1-X}$Sn$_X$ material system we simulate p-TFET based on homo-junction Ge, homo-junction Ge$_{0.90}$Sn$_{0.10}$ and hetero-junction Ge/Ge$_{0.90}$Sn$_{0.10}$ at different source doping concentrations (N$_S$) to determine the most optimal p-TFET configuration.

Transfer (I$_{DS}$-V$_{GS}$) and switching (SS-I$_{DS}$) characteristics of p-TFETs based on homo-junction Ge, homo-junction Ge$_{0.90}$Sn$_{0.10}$ and hetero-junction Ge/Ge$_{0.90}$Sn$_{0.10}$ designs are presented in Fig. 6.10, 6.11 and 6.12 respectively corresponding to direct (Γ → Γ) and indirect BTBT (Γ → L). As a common observation across all Ge$_{1-X}$Sn$_X$ p-TFETs, direct BTBT is the dominant transport mechanism controlling I$_{ON}$. On the other hand, indirect BTBT (Γ → L) dilutes the switching characteristics particularly at low drain current. In homo-junction Ge p-TFET, direct BTBT manifests steep sub-kT/q SS in contrast to indirect BTBT (Fig. 6.10). Moving from homo-junction Ge to homo-junction Ge$_{0.90}$Sn$_{0.10}$ p-TFET produces a direct increase in I$_{ON}$ due to band-gap reduction (Fig. 6.11). However concomitant
Figure 6.8: Ge$_{1-x}$Sn$_x$ band-structure calculated from first-principles DFT is combined with TCAD numerical simulation to model Ge-based p-TFET. Both direct as well as indirect BTBT are modeled.

![Band-structure Diagram](image)

Figure 6.9: Ge$_{1-x}$Sn$_x$ energy band-gap along with electron effective mass computed from DFT.

<table>
<thead>
<tr>
<th>Material</th>
<th>Band Gap [eV]</th>
<th>Electron effective mass [m$_0$]</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Direct</td>
<td>Indirect</td>
</tr>
<tr>
<td>Ge</td>
<td>0.90</td>
<td>0.68</td>
</tr>
<tr>
<td>Ge$<em>{0.90}$Sn$</em>{0.10}$</td>
<td>0.45</td>
<td>0.53</td>
</tr>
<tr>
<td>Ge$<em>{0.90}$Sn$</em>{0.10}$ on Ge (1.1% Strain)</td>
<td>0.61</td>
<td>0.66</td>
</tr>
</tbody>
</table>

rise in off-current ($I_{OFF}$) prevents sub-kT/q SS realization in both direct and indirect BTBT characteristics. In addition, the indirect BTBT is also higher in homo-junction Ge$_{0.90}$Sn$_{0.10}$ p-TFET, a consequence of smaller indirect energy band-gap.

The hetero-junction Ge/Ge$_{0.90}$Sn$_{0.10}$ p-TFET has larger indirect and direct energy band-gap compared to homo-junction Ge$_{0.90}$Sn$_{0.10}$ p-TFET. This manifests in low $I_{OFF}$ and smaller indirect BTBT component as visible from Fig. 6.12.
The hetero-junction Ge/Ge\textsubscript{0.90}Sn\textsubscript{0.10} design distinctly presents reasonably high $I_{ON}$ coupled with steep sub-kT/q SS simultaneously. Due to significant source degeneracy at high source doping concentration ($N_S$), Ge\textsubscript{1−X}Sn\textsubscript{X} p-TFETs show favorable $I_{ON}$ and SS at intermediate $N_S \sim 10^{19}$ cm\textsuperscript{−3} [105].

Similar to p-TFET, n-TFET using Ge/Ge\textsubscript{0.90}Sn\textsubscript{0.10} hetero-junctions are also evaluated. We present $I_{DS}$-$V_{GS}$ characteristics of complimentary TFETs using Ge/Ge\textsubscript{0.90}Sn\textsubscript{0.10} hetero-junctions in Fig. 6.13a. To compare group IV TFET performance we use $I_{60}$ figure of merit which is described in [106] and is suitable to assess sub-60 mV/decade devices. $I_{60}$ is defined as the highest drain current where the $I_{DS}$ transitions from sub-60 to super-60 mV/decade switching slope. For TFETs to compete with MOSFETs an $I_{60} \geq 0.1 \mu$A/\mu m is desired. As observed from this benchmark presented in Fig. 6.13b, TFETs in group IV semiconductors based on Si...
and SiGe system exhibit extremely low $I_{60} < 0.1\text{nA}$ and hence not favorable for high performance TFET design. On the other hand, TFETs based on Ge/Ge$_{0.90}$Sn$_{0.10}$ hetero-junctions demonstrate $>500\times$ higher $I_{60}$, an advantage derived from direct BTBT. Lastly, we benchmark the switching characteristics of p-TFET in potential material systems with respective state of the art $D_{it}$ magnitudes. From the benchmark it is evident that p-TFET using Ge/Ge$_{0.90}$Sn$_{0.10}$ hetero-junctions demonstrate reasonable $I_{ON}$ and sub-thermal switching slope. Ge/Ge$_{1-X}$Sn$_X$ hetero-junctions are hence a strong candidate for steep switching high performance TFET design. With advances in material growth techniques to form abrupt Ge/Ge$_{1-X}$Sn$_X$ heterojunctions with minimal defect density, TFET technology can benefit significantly from Ge$_{1-X}$Sn$_X$ based semiconductors.

Figure 6.11: **Homo-junction Ge$_{0.90}$Sn$_{0.10}$ p-TFET**: Transfer ($I_{DS}$-$V_{GS}$) and switching ($SS-I_{DS}$) characteristics from direct and indirect BTBT.
Figure 6.12: **Hetero-junction Ge/Ge$_{0.90}$Sn$_{0.10}$ p-TFET**: Transfer ($I_{DS}$-$V_{GS}$) and switching ($SS-I_{DS}$) characteristics from direct and indirect BTBT.
Figure 6.13: (a) $I_{DS}$-$V_{GS}$ characteristics of complimentary TFETs using Ge/Ge$_{0.90}$Sn$_{0.10}$ hetero-junctions; (b) $I_{60}$ benchmark of Group IV TFETs indicates that Ge/Ge$_{1-x}$Sn$_x$ hetero-junctions are most suitable for high performance TFET design; (c) Hetero-junction Ge/Ge$_{0.90}$Sn$_{0.10}$ p-TFET outperforms Si and III-V p-TFET at state of the art High-K/channel interface $D_{it}$.
Appendix A
Complimentary Tunnel FET fabrication procedure

The fabrication details for complimentary TFETs are explained in detail below. Note that both PTFET and NTFET share similar sequence except for the difference in PEALD gate stack.

1. E-beam Lithography: Alignment Markers and Dry Etch Mask Definition

- Degrease the III-V sample with Acetone (10mins), Methanol (5mins) and IPA (5mins).
- Rinse with DI water for 1min and blow dry with N₂.
- Remove native oxide by 30 seconds dip in dilute HF (50:1, DI water:HF).
- Transfer the samples into load-lock of Sputter deposition tool.
- Pump down load-lock to below 10⁻⁵ Torr pressure range. Ensure base pressure in sputter chamber is in range of 10⁻⁷ Torr.
- Load samples into the sputter chamber and deposit 300 nm thick Molybdenum at 200W plasma power and 5mT pressure.
- Spin coat with MMA EL-6 resist at 2000 rpm for 1min.
- Bake at 150°C for 3min. Cool the sample for 2mins.
- Spin coat PMMA 950 A3 resist at 4000 rpm for 45secs.
- Bake 180°C for 3 mins. Cool the sample for 2 mins.
• Use E-beam lithography (EBL) to write the features. Write features smaller than equal to $5 \times 5 \mu m^2$ at dose of $900 \mu C/cm^2$ with beam size of 15nm. Write larger features with $420 \mu C/cm^2$ using beam size of 120nm.

• Develop the patterns using 1:3 MIBK: IPA for 1min and 30 secs, 1:1 MIBK: IPA for 20 secs followed by 30 secs dip in IPA.

• Rinse in DI water for 30secs and blow dry with N$_2$.

• Observe for clean and sharp patterns.

2. Dry Etch Mask Deposition: In this step, pillar hard etch mask will be defined using EBL and Lift-off technique.

• Load the developed sample into the evaporator.

• Load Ti and Cr crucibles and wait for vacuum.

• Start depositing once the base pressure comes below $10^{-6}$ Torr.

• Deposit 30 nm Ti followed by 60 nm Cr.

• Lift-off the patterns using Remover PG preheated to 80°C.

• Rinse in IPA, DI water and then blow dry with N$_2$.

• Observe under microscope for a clean lift-off.

3. Pillar Definition Using Dry Etch: In this step, pillars will be defined using Ti/Cr as the hard etch mask.

• Paste the sample on a carrier wafer using double sided thermal tape.

• Clean the back of the carrier wafer before loading into the ICP RIE chamber.

• Load and wait for the lock vacuum to reach below 100mTorr.

• Before running the actual sample for etch, perform chamber clean followed by chamber conditioning with Ar (20sccm) and SF$_6$ (40sccm). RF1 PWR=125W, RF2 PWR=120W.

• Etch Molybdenum using the same recipe for 400s.

• Perform chamber conditioning with Ar (20sccm), BCl$_3$(40sccm) and SF$_6$(10sccm). RF1 PWR=125W, RF2 PWR=500W.
• Etch III-V using the same recipe till bottom P+ source is reached.
• Use Profilometer to verify the total height of the pillar.

4. **Pillar Wet Etch Undercut:** In this step, wet etch is performed to remove dry etch damage and produce the undercut needed for self-aligned gate metal deposition.

  • Rinse the dry etched sample with DI water to remove any residue.
  • Create citric acid (100gm+100ml DI water stirred for 40mins) and H$_2$O$_2$ solution with 20:1 ratio. Store for 15 mins.
  • Etch the sample for 1 min to produce undercut in InGaAs of around 50nm.
  • Rinse with DI water and blow dry with N$_2$.

5. **High-κ Gate Stack Deposition:** In this step, ex-situ wet-etch pre-clean and in-situ H$_2$ and N$_2$ plasma clean are utilized to facilitate desorption of native oxide and achieve effective surface passivation. Subsequently high-κ dielectric Atomic Layer Deposition (ALD) is performed followed by Forming Gas Anneal (FGA). We present numerical details for PTFET and NTFET gate stack separately in Table A.1 and list common process steps below:

  • Clean and condition the ALD chamber for dielectric deposition.
  • Perform ex-situ wet-etch clean on III-V samples to remove native oxide.
  • Load the sample immediately into the load-lock of ALD chamber and pump down to achieve pressure of 10$^{-6}$ Torr
  • Transfer the samples in ALD chamber and wait for 20 min for samples to equilibrate with substrate temperature under constant inert gas flow (Ar, 110 sccms).
  • Start H$_2$ or N$_2$ plasma based surface treatment for PTFET or NTFET respectively.
  • For PTFET : perform 10 pulses of TMA followed by 10 pulses of H$_2$O.
  • For NTFET : perform 10 pulses of H$_2$O. (TMA treatment is performed with N$_2$ plasma)
Table A.1: Gate stack parameters for complimentary TFETs

<table>
<thead>
<tr>
<th>Gate Stack</th>
<th>PTFET</th>
<th>NTFET</th>
<th>NTFET</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dielectric</td>
<td>HfO$_2$</td>
<td>HfO$_2$</td>
<td>ZrO$_2$ [9]</td>
</tr>
<tr>
<td>Ex-situ</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>wet-etch</td>
<td>40 sec HCl:DI (1:1)</td>
<td>3 min BOE (10:1)</td>
<td>3 min BOE (10:1)</td>
</tr>
<tr>
<td>clean</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>In-situ</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>plasma</td>
<td>1.5 min H$_2$ plasma</td>
<td>6 cycles</td>
<td>9 cycles</td>
</tr>
<tr>
<td>clean</td>
<td>at 150°C</td>
<td>N$_2$-plasma/TMA</td>
<td>N$_2$-plasma/TMA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>cyclic treatment at</td>
<td>cyclic treatment at</td>
</tr>
<tr>
<td></td>
<td></td>
<td>250°C</td>
<td>300°C</td>
</tr>
<tr>
<td>ALD</td>
<td>3.5 nm HfO$_2$ at</td>
<td>3.5 nm HfO$_2$ at</td>
<td>4 nm ZrO$_2$ at</td>
</tr>
<tr>
<td></td>
<td>250°C</td>
<td>250°C</td>
<td>300°C</td>
</tr>
<tr>
<td>FGA</td>
<td>20 min, 110 sccm Ar</td>
<td>20 min, 100 sccm Ar</td>
<td>15 min, 95% N$_2$ and</td>
</tr>
<tr>
<td></td>
<td>and 40 sccm H$_2$ at</td>
<td>and 100 sccm Ar</td>
<td>5% H$_2$ at 400°C</td>
</tr>
<tr>
<td></td>
<td>350°C</td>
<td>350°C</td>
<td></td>
</tr>
</tbody>
</table>

- At a substrate temperature of 250°C deposit 3.5 nm thick HfO$_2$ using alternate cycles of TDMAH (Tetrakis(dimethylamino)hafnium) and H$_2$O.
- Perform 20 min FGA at 350°C (HfO$_2$ dielectric)
- Transfer samples to load-lock, cool down in vacuum to room-temperature and unload.

6. **Self-aligned Gate Contact Definition and Deposition:** In this step, gate contact is patterned using EBL and subsequently Ni gate metal is deposited using evaporation and lift-off technique.

- Spin coat with MMA EL11 resist at 4000 rpm for 45secs.
- Bake at 150°C for 3min. Cool the sample for 2mins.
- Spin coat PMMA 950 A3 resist at 4000 rpm for 45secs.
- Bake at 180°C for 3 mins. Cool the sample for 2 mins.
- Use EBL to write the features. Write larger features with 420μC/cm$^2$ using beam size of 120nm.
• Develop the patterns using 1:3 MIBK: IPA for 1min and 30 secs, 1:1 MIBK: IPA for 20 secs followed by 30 secs dip in IPA.
• Rinse in DI water for 30 secs and blow dry with N₂.
• Observe for clean and sharp patterns.
• Load into the evaporator and wait for pressure to reach below $10^{-6}$ Torr.
• Deposit 20nm Ni gate metal using thermal evaporation.
• Lift-off the patterns using Acetone followed by Remover PG preheated to 80°C.
• Rinse in IPA, DI water and then blow dry with N₂.
• Observe under microscope for a clean lift-off.

7. **Source and Gate Pad Definition and Deposition:** In this step, source and gate pad windows are created, high-κ is removed and the pads are formed using EBL, evaporation and lift-off techniques.

   • Spin coat with MMA EL11 resist at 2500 rpm for 45 secs.
   • Bake at 150°C for 3 min. Cool the sample for 2 mins.
   • Spin coat PMMA 950 A3 resist at 2000 rpm for 45 secs.
   • Bake at 180°C for 3 mins. Cool the sample for 2 mins.
   • Use EBL to write the features. Write larger features with $420 \mu C/cm^2$ using beam size of 120nm.
   • Develop the patterns using 1:3 MIBK: IPA for 1min and 30 secs, 1:1 MIBK: IPA for 20 secs followed by 30 secs dip in IPA.
   • Rinse in DI water for 30 secs and blow dry with N₂.
   • Observe for clean and sharp patterns.
   • Dry etch the high-k in ICP RIE using BCl₃ (10 sccm) and Ar (40 sccm): RF1 PWR: 75W and RF2 PWR: 500W, Time: 25 secs.
   • Load into the evaporator with Ti, Pd and Au crucibles.
   • Wait for pressure to reach below $10^{-6}$ Torr.
   • Deposit 20nm Ti, 20nm Pd and 30nm Au.
• Lift-off the patterns using Acetone followed by Remover PG preheated to 80°C.
• Rinse in IPA and DI water and then blow dry with N₂.
• Observe under microscope for clean lift-off.

8. **Planarization and Etch Back:** In this step, the pillars are planarized using BCB and the BCB is etched back till the top of Mo contact for the top contact formation.

- Spin Coat BCB at 5000rpm for 1min.
- Bake at 140°C for 10mins.
- Load into an oven with N₂ ambient while the hot plate is preset to 140°C.
- Gradually raise the temperature from 140°C to 250°C.
- Cure BCB at 250°C for 1 hr.
- Unload the cured sample once the temperature is below 150°C.
- Cool the sample and load into the RIE chamber.
- Etch BCB in O₂ (80sccm) and CF₄ (20sccm), Pressure 200mT, RF=200W (Capactively coupled RIE).
- Etch in steps until the BCB is below the pillar surface by 200nm. Check the height with Profilometer and or SEM.

9. **Drain Pad Definition and Deposition:** In this step, drain pads are formed in contact with the Mo on top of the pillars. EBL, E-beam evaporation and Lift-off technique is used.

- Spin coat with MMA EL11 resist at 2500 rpm for 45secs.
- Bake at 150°C for 3min. Cool the sample for 2mins.
- Spin coat PMMA 950 A3 resist at 2000 rpm for 45secs.
- Bake at 180°C for 3 mins. Cool the sample for 2 mins.
- Use EBL to write the features. Write larger features with 420µC/cm² using beam size of 120nm.
• Develop the patterns using 1:3 MIBK: IPA for 1min and 30 secs, 1:1 MIBK: IPA for 20 secs followed by 30 secs dip in IPA.
• Rinse in DI water for 30secs and blow dry with N₂.
• Observe for clean and sharp patterns.
• Remove O₂ plasma induced native oxide with high-κ etch recipe for 25 secs.
• Load into the evaporator with Ti, Pd and Au crucibles.
• Wait for the pressure to reach below 10⁻⁶ Torr.
• Deposit 20nm Ti, 20nm Pd and 60nm Au.
• Lift-off the patterns using Acetone followed by Remover PG preheated to 80°C.
• Rinse in IPA and DI water.
• Blow dry with N₂ and observe under microscope for a clean lift-off.

10. VIA Definition and Formation: In this step, VIA is created through BCB using Al as etch mask.

• Load the samples into the evaporator with Al crucible.
• Deposit 20 nm Al
• Spin coat with MMA EL11 resist at 2500 rpm for 45secs.
• Bake at 150°C for 3min. Cool the sample for 2mins.
• Spin coat PMMA 950 A3 resist at 2000 rpm for 45secs.
• Bake at 180°C for 3 mins. Cool the sample for 2 mins.
• Use EBL to write the features. Write larger features with 420µC/cm² using beam size of 120nm.
• Develop the patterns using 1:3 MIBK: IPA for 1min and 30 secs, 1:1 MIBK: IPA for 20 secs followed by 30 secs dip in IPA.
• Dry etch the Al in ICP RIE using Cl₂ (30sccm), BCl₃ (30sccm) and Ar (10 sccm): RF1 PWR: 50W and RF2 PWR: 600W, Time: 30secs
• Etch BCB in O₂ (80sccm) and CF₄ (20sccm), Pressure 200mT, RF=200W (Capacitively coupled RIE) for 120secs.
• Dry etch the remaining Al in ICP RIE using Cl₂ (30sccm), BCl₃ (30sccm) and Ar (10 sccm): RF1 PWR: 50W and RF2 PWR: 600W, Time: 30secs.

11. GSG Pad Definition and Deposition:

• Spin coat with MMA EL11 resist at 4000 rpm for 45secs.
• Bake at 150°C for 3min. Cool the sample for 2mins.
• Spin coat PMMA 950 A3 resist at 4000 rpm for 45secs.
• Bake at 180°C for 3 mins. Cool the sample for 2 mins.
• Use EBL to write the features. Write larger features with 420μC/cm² using beam size of 120nm.
• Develop the patterns using 1:3 MIBK: IPA for 1min and 30 secs, 1:1 MIBK: IPA for 20 secs followed by 30 secs dip in IPA.
• Load into the evaporator with Ti, Pd and Au crucibles.
• Wait for pressure to reach below 10⁻⁶ Torr.
• Deposit 20nm Ti, 20nm Pd and 60nm Au.
• Lift-off the patterns using Acetone followed by Remover PG preheated to 80°C.
• Rinse in IPA and DI water and then blow dry with N₂.
• Observe under microscope for clean lift-off.
Appendix B
Fabrication method for ultra-thin body HTFETs

Process steps for fabricating ultra-thin body HTFET with vertical sidewalls using T-shaped Cr/Ni etch mask and high temperature III-V etch is presented below. The wafers used for this recipe are same as NTFET wafers depicted in Fig. 3.1 with the only difference in reduced drain layer thickness of 50 nm. This lowers etch duration at high temperature and prevents etch mask degradation. Note that shadow effect obtained from T-shaped etch mask enables self-aligned gate metal deposition as depicted in Fig. 6.2c.

1. T-Shaped Dry Etch Mask Definition

- Degrease the III-V sample with Acetone (10mins), Methanol (5mins) and IPA (5mins).
- Rinse with DI water for 1min and blow dry with N₂.
- Remove native oxide by 30 seconds dip in dilute HF (50:1, DI water:HF).
- Transfer the samples into load-lock of Sputter deposition tool.
- Pump down load-lock to below 10⁻⁵ Torr pressure range. Ensure base pressure in sputter chamber is in range of 10⁻⁷ Torr.
- Load samples into the sputter chamber and deposit 20 nm thick Molybdenum at 200W plasma power and 5mT pressure.
- Spin coat PMMA 950 A3 resist at 4000 rpm for 45secs.
- Bake 180°C for 3 mins. Cool the sample for 2 mins.
• Spin coat MMA EL11 resist at 3000 rpm for 45secs.
• Bake 180°C for 3 mins. Cool the sample for 2 mins.
• Spin coat PMMA 950 A2 resist at 4000 rpm for 45secs.
• Bake 180°C for 3 mins. Cool the sample for 2 mins.
• Use E-beam lithography (EBL) to pattern MESA. A high dose of 1450\(\mu\)C/cm\(^2\) with beam size of 1nA is used. The excess-dose creates room for extra metal-etch mask fill to shadow effect for self-aligned gate metal deposition.
• Develop the patterns using 1:3 MIBK: IPA for 3min and 1 min in IPA.
• Rinse in DI water for 30secs and blow dry with \(\text{N}_2\).
• Observe for clean and sharp patterns.

2. Dry Etch Mask Deposition: In this step we form the T-shaped etch mask using e-beam evaporation and lift-off technique.

• Load the developed samples into the evaporator.
• Load Cr and Ni crucibles and wait for vacuum.
• Reduce stage temperature to 5°C to check deposition heat.
• Start depositing once the base pressure comes below \(10^{-6}\) Torr: 60 nm Cr followed by 90 nm Ni.
• Lift-off the patterns using Acetone followed by Remover PG preheated to 80°C.
• Rinse in IPA, DI water and then blow dry with \(\text{N}_2\).
• Observe under microscope for a clean lift-off.
• Scrutinize the samples in SEM. T-shaped Cr/Ni etch mask profile should be evident (Fig. 6.2a)

3. Ultra-thin body MESA creation: In this step we form III-V MESA with ultra-thin body vertical geometry using Cl\(_2\) based high temperature dry etch.

• Paste the sample on a carrier wafer using double sided thermal tape for room temperature etch of Molybdenum.
• Clean the back of the carrier wafer before loading into the ICP RIE chamber.

• Load and wait for the lock vacuum to reach below 100mTorr.

• Before running the actual sample for etch, perform chamber clean followed by chamber conditioning with Ar (20sccm) and SF6 (40sccm). RF1 PWR=125W, RF2 PWR=120W.

• Etch Molybdenum using the same recipe for 40s.

• Remove sample and paste it on a carrier wafer using kapton tape for high temperature III-V etch.

• Perform chamber cleaning and subsequently followed by conditioning at room temperature with Cl₂ (6sccm), N₂ (24sccm) at 5mTorr; 900W at coil and 60W stage power.

• Ramp the stage temperature to 160°C

• Etch III-V using Cl₂ (6sccm), N₂ (24sccm) plasma dry etch chemistry at 5mTorr pressure for 48 seconds; 900W at coil and 60W stage power. Etch depth∼200nm.

• Use Profilometer to verify the total height of the pillar and scrutinize the sidewalls using SEM (Fig. 6.2).

After creation of MESA pillar remaining process is similar to described in Appendix A.
Appendix C
DFT parameters for phonon assisted indirect BTBT

Phonon-assisted indirect band-to-band tunneling (BTBT) parameters for Ge$_{1-X}$Sn$_X$ along with Ge and Si are computed from first principles density functional theory (DFT) and subsequently used in numerical device level TCAD simulation. These parameters are described below:

\[
N_{TA} = \frac{1}{\exp \left( \frac{\epsilon_{TA}}{k_B T} \right) - 1} \tag{C.1}
\]

\[
\epsilon_{TA} = (1 - X) \epsilon_{TA}^{Ge} + X \epsilon_{TA}^{Sn} \tag{C.2}
\]

\[
D_{TA} = (1 - X) D_{TA}^{Ge} + X D_{TA}^{Sn} \tag{C.3}
\]

\[
\rho = (1 - X) \rho^{Ge} + X \rho^{Sn} \tag{C.4}
\]

where $N_{TA}$ is occupation number of the transverse acoustic phonon, $\epsilon_{TA}$ is transverse acoustic phonon energy; $X$ is mole fraction of Sn, $D_{TA}$ is deformation potential and $\rho$ is mass density. Numerical value of these parameters as computed from DFT, are summarized in Table C.1.
<table>
<thead>
<tr>
<th>BTBT Parameter</th>
<th>$\epsilon_{TA}$ (meV)</th>
<th>$D_{TA}$ (eV/m)</th>
<th>$\rho$ (kg/m$^3$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Si</td>
<td>19</td>
<td>$2.45\times10^{10}$</td>
<td>2329</td>
</tr>
<tr>
<td>Ge</td>
<td>8.6</td>
<td>$0.8\times10^{10}$</td>
<td>5323</td>
</tr>
<tr>
<td>Ge$<em>{0.98}$Sn$</em>{0.02}$</td>
<td>8.51</td>
<td>$0.8\times10^{10}$</td>
<td>5362</td>
</tr>
<tr>
<td>Ge$<em>{0.94}$Sn$</em>{0.06}$</td>
<td>8.33</td>
<td>$0.8\times10^{10}$</td>
<td>5440</td>
</tr>
<tr>
<td>Ge$<em>{0.90}$Sn$</em>{0.10}$</td>
<td>8.15</td>
<td>$0.8\times10^{10}$</td>
<td>5519</td>
</tr>
</tbody>
</table>

Table C.1: Parameters for phonon assisted indirect BTBT in Group IV TFETs computed from DFT.
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Vita

Rahul Pandey

Rahul Pandey received his Bachelor’s and Master’s degree in Electrical Engineering from Indian Institute of Technology Kanpur, India, in 2010. He joined Intel India in July 2010 as Graphics Full-Chip Physical Design Engineer where he worked towards tape-out of Intel Processor Graphics at 22 nm and 14 nm process technology nodes.

He embarked on Ph.D. in Electrical Engineering at Penn State in Dr. Suman Datta’s research group in Jan. 2013. He has worked extensively on design, fabrication and characterization of Tunnel Transistors as a replacement for conventional Silicon-CMOS transistors, for energy efficient operation in future process technology nodes. He has demonstrated significant performance breakthroughs in III-V semiconductor based Tunnel Transistors gathering highlights in prestigious conferences like VLSI 2015 (best student paper nomination) and IEDM 2015 (highlight paper, selected for conference publicity). He has worked in successful collaborations with research groups across universities (UCSB, Georgia Tech, IIT Bombay, etc.) and also within the industry (Intel, TSMC, Samsung etc.). He has maintained an excellent academic record with 4.0 GPA besides a strong research record with 16 conference and journals publications with 10 as the first author.

His research on III-V HTFET interface characterization was featured on the front-page of IEEE Electron Devices Society January 2016 newsletter. Moreover his work on complimentary III-V HTFET demonstration was featured in Compound Semiconductor magazine’s Jan.-Feb. 2016 edition. His current research interests include device-circuit co-design and characterization of emerging technologies for low power logic and memory applications. After completing his Ph.D. program at Penn State in August 2017, he will be joining Intel Corporation at Hillsboro, OR, where he will be working in the position of Device Engineer.