TOWARDS LIGHTWEIGHT AND FLEXIBLE HIGH PERFORMANCE NANOCRystalline silicon solar cells through light trapping and transport layers

A Dissertation in
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by
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ABSTRACT

This thesis investigates ways to enhance the efficiency of thin film solar cells through the application of both novel nano-element array light trapping architectures and nickel oxide hole transport/electron blocking layers. Experimental results independently demonstrate a 22% enhancement in short circuit current density \( J_{SC} \) resulting from a nano-element array light trapping architecture and a \( \sim 23\% \) enhancement in fill factor (FF) and \( \sim 16\% \) enhancement in open circuit voltage \( V_{OC} \) resulting from a nickel oxide transport layer. In each case, the overall efficiency of the device employing the light trapping or transport layer was superior to that of the corresponding control device. Since the efficiency of a solar cell scales with the product of \( J_{SC} \), FF, and \( V_{OC} \), it follows that the results of this thesis suggest high performance thin film solar cells can be realized in the event light trapping architectures and transport layers can be simultaneously optimized.

The realizations of these performance enhancements stem from extensive process optimization for numerous light trapping and transport layer fabrication approaches. These approaches were guided by numerical modeling techniques which will also be discussed. Key developments in this thesis include (1) the fabrication of nano-element topographies conducive to light trapping using various fabrication approaches, (2) the deposition of defect free nc-Si:H onto structured topographies by switching from SiH\(_4\) to SiF\(_4\) PECVD gas chemistry, and (3) the development of the atomic layer deposition (ALD) growth conditions for NiO.

**Keywords:** light trapping, nano-element array, hole transport layer, electron blocking layer, nickel oxide, nanocrystalline silicon, aluminum doped zinc oxide, atomic layer deposition, plasma enhanced chemical vapor deposition, electron beam lithography, ANSYS HFSS
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List of Abbreviations

**AFM** - Atomic force microscopy
**ALD** - Atomic layer deposition
**a-Si:H** - Hydrogenated amorphous silicon
**AZO** - Aluminum doped zinc oxide
**ARC** - Anti-reflective coating
**DSC** - Dye sensitized solar cell
**BCP** - Block copolymer
**CPW** - Cost per watt
**CVD** - Chemical vapor deposition
**EBE** - Electron beam evaporation
**EBE+A** - Electron beam evaporation followed by a thermal annealing treatment
**EBL** - Electron beam lithography
**ETL** - Electron transport layer
**FESEM** - Field emission scanning electron microscopy
**FF** - Fill factor
**FIB** - Focused ion beam
**FOTS** - Tridecafluoro-1, 1, 2, 2-tetrahydrooctyltrichlorosilane
**GIXRD** - Grazing incidence x-ray diffraction
**GPC** - Growth per cycle
**HFSS ANSYS** - High frequency structural simulator produced by the ANSYS Corporation
**HTL** - Hole transport layer
**ICP** - Inductively coupled plasma
**IOH** - Hydrogen doped indium oxide
**ITO** - Indium doped tin oxide
**IV** - Current-voltage measurement
**J<sub>-1V</sub>** - Current density at -1V reverse bias
**J<sub>SC</sub>** - Short circuit current density
**JV** - Current density-voltage measurement
**L<sub>abs</sub>** - Absorption length of a semiconductor
**Col**-Carrier collection length of a semiconductor

**LCCM**-Light and carrier collection management

**Litho**-Conventional positive optical lithography

**LOR**-Liftoff resist

**MFP**-Mean free path

**nc-Si:H**-Hydrogenated nanocrystalline silicon

**Ni(amd)**-Nickle bis (N,N’-di-tert-butylacetamidinate)

**OPV**-Organic photovoltaic

**PCE**-Power conversion efficiency (solar cell efficiency)

**PECVD**-Plasma enhanced chemical vapor deposition

**PEDOT**-Poly(3,4-ethylenedioxythiophene)

**PI**-Polyimide

**PV**-Photovoltaic

**RIE**-Reactive ion etching

**Si MM**-Silicon mastermold

**TCO**-Transparent conducting oxide

**TEM**-Transmission electron microscopy

**TFSC**-Thin film solar cell

**μc-Si:H**-Hydrogenated microcrystalline silicon

**UV-Vis**-Ultraviolet-visible spectrophotmetry

**V_{oc}**-Open circuit voltage

**ZEP**-Positive tone e-beam lithography resist
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Chapter 1: Introduction

1.1 Structure of this thesis

Chapter 1 will provide an introduction to solar energy beginning with the current economics pertaining to the solar energy market. Next the general operational mechanisms of solar cells will be discussed. Each of the three generations of solar cells will then be introduced.

Chapter 2 will provide background information pertaining to each of the two methods this thesis is seeking to employ in order to further enhance solar cell performance: light trapping and transport layers. Immediately following the explanations of each of these two methods the current status and state of the art work pertaining to each method will be reviewed.

In Chapter 3 the experimental work pertaining to nickel oxide transport layers will be discussed. This chapter will focus on the deposition methods and characteristics of nickel oxide thin films grown by multiple fabrication techniques. A discussion pertaining to the properties of nickel oxide thin films in relation to both their fabrication technique and their post deposition annealing treatment will also be had. At the end of Chapter 3 the performance of planar thin film solar cells employing nickel oxide transport layers will be presented and discussed.

Numerical modeling will be the focus of Chapter 4. This chapter will begin by briefly discussing the ANSYS HFSS Maxwell’s equation solver which was used for the simulations pertinent to this thesis work. The HFSS results for light trapping architectures will be presented and discussed in terms of their importance in guiding the subsequent fabrication decisions.

In Chapter 5 the device fabrication and characterization of light trapping solar cells will be presented. This chapter will begin with a detailed scientific discussion pertaining to the nc-Si: H absorber deposition onto the irregular topographies used to enhance light trapping. Here, a mechanism for the defect formation in the nc-Si: H upon its deposition onto irregular
topographies will be proposed and based on this mechanism a solution to eliminating this defect will be suggested. Aluminum doped zinc oxide (AZO) and indium tin oxide (ITO) top electrode depositions will also be discussed at this point. Next, the light trapping (bottom) electrode fabrication steps and final device fabrication will be presented for first a light trapping solar cell made using electron beam lithography and second for a light trapping solar cell made using a nano-molding approach. This chapter is intended to include an ample level of processing detail such that the methods used for fabricating the highly ordered nano-element array light trapping electrodes could be reproduced and fully understood by a future experimenter.

Chapter 6 will discuss in detail two additional nano-element electrode fabrication schemes which have been developed based upon the performance of the devices provided in Chapter 5. Again, an ample level of detail will be provided for each of these fabrication approaches such that the methods used for fabricating these light trapping structures could be reproduced and fully understood by a future experimenter. Lastly, in Chapter 7, the key results of this thesis work will be summarized and the perspective on future work of value based on the key findings of this thesis will be addressed.

1.2 The outlook of solar

In a world with continuously increasing energy demands a full dependence on renewable energy resources will quickly become a reality within the next few hundred years. Oil reserves are expected to last another 50 years, natural gas will last another 70 years, and coal reserves are expected to last another 250 years [1]. The sun is a sustainable energy resource that will last for the next 5 billion years [2]. The sun provides thousands of times more than enough energy to meet all of our planet’s energy demands. Realistically, there is no single energy resource which will simultaneously meet all of our energy demands, and a combination of resources will be
required to support our energy usage around the clock. Of all forms of renewable energy, however, the longevity and energy output from the sun makes it the resource with the single greatest potential to help in meeting our global energy demand as shown in Figure 1.

![Diagram of renewable energy resources]

**Figure 1:** The relative potentials of renewable energy resources [3]

In 2016 it is expected solar installations will reach 64.7 GW, with China, USA, and Japan accounting for roughly 2/3 of the total solar market [4]. Continued rapid growth is expected to take installations of photovoltaic (PV) modules to 100 GW by 2018 [5]. China will continue to lead the global PV market while the USA is expected to show the most robust growth in the upcoming year by passing the 10 GW mark and overcoming Japan. The solar market is continuously growing, as shown in Figure 2, but a slowing in the year over year (Y-O-Y) growth rate compared to 2015 suggests there should be an increased level of urgency for developing improvements which can make solar technology a more attractive energy resource [4].
A simple comparison between Figures 1 and 2 suggests that solar energy will account for approximately 0.43% of our total energy production in 2016. This relatively low, but still significant, utilization of solar energy is well known to be a result of the high investment and operating costs associated with this technology. The concept of grid parity has hindered the PV market due to the operating costs for solar energy dwarfing all other forms of both renewable and non-renewable energy. The high operating costs of PV modules are largely a result of solar panels using land inefficiently. Large land areas are required to house enough solar panels for appreciable industrial level power output: it takes 400 acres of collectors to generate a 75 MW capacity [6]. Combining inefficient land use with the high installation and maintenance costs associated with large and bulky solar panels presents a seemingly unavoidable increase to the cost per watt (CPW) for solar energy. Research striving to reduce the CPW of solar energy is a key economic driver in the PV industry. Making solar cells of cheaper, or less, material can serve to decrease the manufacturing costs while improving device efficiency can increase the
power output. Ideally, high material utilization is desired since a reduction in the weight of a solar panel will reduce both the material and installation costs. Over the last 10 years transitions to thinner wafers have improved material utilization from 16 grams per peak watt (g/Wp) to 6 g/Wp [7].

Over the past 5 decades the solar market has grown from a mere 0.5 MW in 1977 to approximately 60 GW today [8] and this market is expected to eclipse the 100 GW mark in 2018 [9]. Throughout this time the so called first generation solar cells utilizing wafer based silicon have dominated the PV market. Following a brief explanation of the operation of a generic solar cell each of the three solar cell generations will be introduced. A focus will be placed on the second generation (thin film) solar cell technologies since they will be central to this thesis.

1.3 Solar cell operation

Solar technology represents the extreme example of an interdisciplinary field as it bridges economics, materials science, electrical engineering, and optics. This makes the solar cell one of the most complex solid state devices in existence. Therefore, prior to the detailed discussion of the architectures and concepts unique to this thesis it is first necessary to discuss the fundamental operating mechanisms of a solar cell. A general understanding of the basic physics of a solar cell is a prerequisite to recognizing the logic and science motivating the highly specific modeling and fabrication conditions which will be used in this thesis.

Figure 3 shows a cross sectional schematic of a typical solar cell. Here, a relatively thick and lightly doped p-type Si base material is sandwiched between a thin and heavily doped n-type Si emitter and a thin and heavily doped p-type Si back surface field. The balancing of drift and diffusion currents inherent to p-n junctions induces a depletion region in the base of the solar cell in which very few free charge carriers (i.e. electrons and holes) are present. A strong electric
drift field exists in the depletion region due to the spatial separation between the ionized donor atom cores (+) and the ionized acceptor atom cores (-). Typical doping types, doping levels, and thicknesses for each of the layers shown in Figure 3 are provided in Table 1.

Figure 3: Cross sectional schematic of a typical solar cell

In Figure 3 a top metal grid contact serves as an electron collecting cathode. A grid structure is necessary to allow the majority of incident light to reach the base region of the solar cell for absorption. An ideal top metal contact should not cover more than 10% of the solar cell but still provide a high enough electrical conductivity to avoid resistive losses [10]. A blanket back metal contact serves as a hole collecting anode. A grid structure at the back metal contact is not necessary since the complete transmission of light through the device is undesirable; a fully reflective back metal contact will give unabsorbed light a second chance to pass through the absorbing base layer in the event it was not absorbed on its first pass through the solar cell. The incident light impinging on the device is the AM1.5G solar spectrum shown in Figure 4 [11]. The AM1.5G spectrum is normalized to 100 mW/cm² by adjusting the lamp intensity of the light
source used to simulate the solar cell’s current voltage (IV) characteristic. This is necessary to ensure all laboratories are defining efficiency in the same way. Since the efficiency of a solar cell is most simply defined as the ratio of the power output \( P_{\text{out}} \) to the power input \( P_{\text{in}} \). This 100 mW/cm\(^2\) power input is therefore used to ensure solar cell device characterization is being performed uniformly across the industry.

<table>
<thead>
<tr>
<th>Layer</th>
<th>Material</th>
<th>Doping</th>
<th>Thickness</th>
<th>Primary Role</th>
</tr>
</thead>
<tbody>
<tr>
<td>Emitter</td>
<td>n-Si</td>
<td>( \sim 10^{19}/\text{cm}^3 )</td>
<td>(~0.3 , \mu\text{m})</td>
<td>Electron conductor</td>
</tr>
<tr>
<td>Base</td>
<td>p-Si</td>
<td>( \sim 10^{16}/\text{cm}^3 )</td>
<td>(100''s , \mu\text{m})</td>
<td>Absorbing material</td>
</tr>
<tr>
<td>Back Surface Field</td>
<td>p-Si</td>
<td>( \sim 10^{19}/\text{cm}^3 )</td>
<td>(~0.6 , \mu\text{m})</td>
<td>Hole conductor</td>
</tr>
</tbody>
</table>

**Table 1**: Typical materials, doping levels, and thicknesses for a conventional silicon solar cell

![AM1.5G solar spectrum](image)

**Figure 4**: AM1.5G solar spectrum (blue line) used as a characterization standard [11]

When the solar cell is exposed to the AM1.5G spectrum some photons with energies \( (h\nu) \) above the band gap \( (E_G) \) of the semiconductor can be absorbed. Here \( h \) is Plank’s constant and \( \nu \) is the frequency of the photon. Next, some of these absorption events can lead to the creation of
electron hole pairs. When these electron hole pairs are generated within a minority carrier diffusion length from the edge of the depletion region the photogenerated carriers can be swept apart by the electric field present within the depletion region. As a result, electrons will drift towards the top metal contact due to their movement towards the positive potential introduced by the (+) atom cores of the ionized donor atoms. Similarly, holes will drift towards the bottom metal contact as a result of their movement towards the negative potential introduced by the (-) atom cores of the ionized acceptor atoms. When a typical solar flux of over $10^{15}$ photons/cm$^2$/sec is impinging the solar cell this process will be happening on the order of $10^{15}$ times per second for every square centimeter of the device. As a result, well over $10^{17}$ photogenerated electrons will be leaving a standard sized illuminated solar panel (i.e. 6” wafer) device every second. The macroscopic result of this mass of electron flow is a current. This current can then flow through an external load to perform useful work. For clarity, all of these basic operational steps of a solar cell are depicted in Figure 5.

![Figure 5: Basic operation of a solar cell: 1) light absorption creates electron hole pairs, 2) electrons and holes drift to contacts, 3) current flows out of device, 4) work is done on load](image-url)
In short, solar cells operate by converting sunlight’s energy into useful electricity. A higher efficiency solar cell will therefore convert a larger portion of the available solar spectrum into electricity. Equation 1.1 shows how the power conversion efficiency (PCE) of a solar cell is the product of the short circuit current density (J\textsubscript{SC}), the open circuit voltage (V\textsubscript{OC}), and the fill factor (FF) divided by the power input (P\textsubscript{in}) or equivalently the ratio of the power output (P\textsubscript{out}) to the power input.

\[ PCE = \frac{J\textsubscript{SC}V\textsubscript{OC}FF}{P\textsubscript{in}} = \frac{P\textsubscript{out}}{P\textsubscript{in}} \quad [1.1] \]

The electrical parameters J\textsubscript{SC} and V\textsubscript{OC} of equation 1.1 are directly obtained from the current density-voltage (JV) characteristic of the solar cell during its exposure to incident light. Figure 6 shows the general JV characteristic of a typical solar cell. The fill factor, defined by equation 1.2, is the ratio of the product of the current density at the maximum power point (J\textsubscript{MPP}) and the voltage at the maximum power point (V\textsubscript{MPP}) to the product of J\textsubscript{SC} and V\textsubscript{OC}.

\[ FF = \frac{J\textsubscript{MPP}V\textsubscript{MPP}}{J\textsubscript{SC}V\textsubscript{OC}} \quad [1.2] \]

Observation of the JV characteristic in Figure 6 illustrates that a solar cell in the absence of light has the same electrical characteristic as a large diode. The light exposure serves to shift the diode characteristic into the 4\textsuperscript{th} quadrant. Therefore, a solar cell has the electrical analog of a diode in parallel with a current generator. The diode characteristic results from the p-n junction while the current generator characteristic results from the photogenerated current.

In reality, all real solar cells also suffer from parasitic resistances. A good solar cell design seeks to minimize the series resistance (R\textsubscript{S}) by using highly conductive Ohmic contacts and at the same time maximize the shunt resistance (R\textsubscript{SH}) by avoiding processing induced defects (e.g. pinholes) in the absorber material. The complete electrical analog of a solar cell is shown in
Figure 7. Throughout the course of this thesis the importance of the process induced series and shunt resistances and their concurrent influences on device performance will be discussed.

Figure 6: JV characteristic of a typical solar cell. The JV characteristic is used to obtain the electrical parameters ($J_{SC}$, $V_{OC}$, and FF) and efficiency (PCE) of the device.

Figure 7: Electrical analog of a solar cell
The solar cells most similar in structure and operation such as that described by Figure 5 are the so called first generation solar cells which are comprised of crystalline wafer based silicon. The following three sections will introduce each of the three generations of solar cells.

1.4 First generation solar cell technologies

Silicates are the most abundant minerals in the earth’s crust, accounting for over 90% of the composition. So it comes as little surprise that over one quarter of the earth’s crust is composed of silicon [12]. This abundance of silicon coupled with wafer based silicon’s well established processing technology borrowed from the semiconductor industry makes wafer based silicon the dominant PV technology. First generation solar cell technology is based on the semiconductor material crystalline silicon (c-Si) coming in two predominant forms: monocrystalline silicon and multicrystalline silicon. Together, solar panels based on these two materials account for roughly 90% of the total PV production with multicrystalline Si making up ~56% of the total PV production [13].

In recent years, the wafer based Si technology has increased its market share relative to thin film solar cell technologies as a result of the increased production capacity of multicrystalline silicon as shown in Figure 8 [14]. Record efficiencies of 25.6% for monocrystalline Si and 20.8 % for multicrystalline Si have been obtained, with typical industrial grade efficiencies for such modules being in the range of 16-18% [13]. Despite the market dominance and high efficiencies of first generation Si solar cells this technology is more or less saturated as a result of already being very well understood and established as shown in Figure 9 [15]. This leaves comparatively little room for growth and innovation for the first generation wafer based silicon solar cells.
The bulkiness of the conventional silicon wafer based panels is unavoidable as a result of crystalline silicon’s relatively weak absorption coefficient [16]. Therefore, solar cells based on crystalline silicon must be sufficiently thick, on the order of several hundred µm, to absorb an appreciable portion of the solar spectrum and afford reasonable efficiencies. This bulkiness has the ultimate result of increasing the installation and maintenance costs associated with conventional silicon solar cells. Despite this drawback, silicon solar panels based on first generation technologies remain the most viable branch of solar energy. In October 2015 SolarCity introduced a new 22.5% efficient c-Si panel with a very competitive cost of only $0.55/W [17].
In order to reduce the installation costs associated with bulky wafer based panels a second generation of solar cells based on thin film semiconductor materials began to emerge in the early 1980’s. As witnessed by contrasting the density of data points for thin film technologies (green lines) and crystalline Si cells (blue lines) in Figure 9 it can be seen that in recent years the second generation thin film technologies have been attracting more research interest than the first generation technologies. This increased attention towards second generation photovoltaics stems from the stronger absorbing nature of these materials, which ultimately offers the potential for thinner solar panels with a higher specific power (kW/kg).
1.5 Second generation solar cell technologies

Thin film solar cells (TFSCs) are distinguished from conventional c-Si cells in three major ways: (1) TFSCs are fabricated on a foreign substrate such as glass, a metal foil, or a flexible polymer, (2) a transparent conducting oxide (TCO) is used as the front contact in place of the metal grid used with conventional c-Si cells, and (3) TFSCs can be fabricated in either a substrate or superstrate configuration. In the superstrate configuration the layers are deposited in the opposite order as the final operating orientation, that is, upon the completion of fabricating a superstrate solar cell the device will be inverted such that the TCO faces the incoming sunlight. Superstrate devices typically employ TCO coated glass in which the absorber material and back metal contact are subsequently deposited onto. The glass superstrate configuration is well suited for integrating solar panels into buildings as an architectural element [18].

Three major thin film technologies, differentiated by absorber type, currently dominate the 2nd generation solar cell market. The first variety is based on silicon thin films, namely: hydrogenated amorphous silicon (a-Si:H) and nanocrystalline silicon (nc-Si:H) which is also interchangeably referred to as microcrystalline silicon (µc-Si:H). Solar cells based on the semiconductor absorbing materials cadmium telluride (CdTe) and copper indium gallium diselenide (CIGS) round out the thin film solar cell market, which currently makes up roughly 10% of the total solar market [18]. All of these materials have appreciably higher absorption coefficients than c-Si and as a result solar cell devices based on these materials can be made much thinner. Typical thicknesses for thin film technologies are on the order of 100’s of nm to 1’s of µm. In comparison to the 100’s of µm thickness needed for c-Si this means second generation TFSCs have the potential to be hundreds to thousands of times thinner than first generation wafer based cells. This results in a significantly higher specific power (kW/kg) for
TFSCs; here, a less than twofold reduction in efficiency (kW) for TFSCs relative to c-Si can be easily compensated for by using orders of magnitude less material (kg). Additionally, this drastic reduction in thickness opens up the opportunity for thin film solar cells to be conducive to flexible substrates, high throughput printing techniques, and roll to roll processes for mass manufacture. Finally, the light weight of TFSC’s also reduces the inevitable installation costs associated with bulky c-Si based panels.

Currently, cells based on CdTe are the most utilized of the three thin film technologies. In recent years the PCE of CdTe modules has risen from 10.7% [19] to 16.1% [20]. This increase in efficiency has led to appreciable reductions in CPW; in fact, CdTe cells produced by First Solar have the lowest prices in the entire PV industry approaching $0.49/Wp [13]. A record lab based efficiency of 21% has been obtained for CdTe thin film solar cells [7]. In 2014 roughly 4% of the total PV production was from CdTe cells, with 1.9 GWp of installations [7].

Close behind CdTe is the CIGS based PV, which make up roughly 3.5% of the total PV production with 1.7 GWp of installations in 2014 [7]. Technology based on CIGS has also seen appreciable improvements in the last several years with efficiency improvements from 13.4% [21] to 15.7% [22]. Of the three thin film technologies, only the CIGS variety has increased its relative market share since 2010 [23]. A record laboratory efficiency of 20.5% has been obtained for thin film solar cells based on CIGS [7].

The third of the thin film technologies, based on Si containing absorbers, has been the slowest to grow in recent years with only marginal efficiency improvements over the past two decades. Thin films of a-Si:H seem to offer great promise as a solar cell material owing to this material’s strong absorption coefficient of $>10^4 \text{ cm}^{-1}$ for photons with energies ~0.2 eV higher than its band gap of 1.7-1.8 eV [24]. In addition, a-Si:H is easy to deposit and made of non-
toxic and abundant elements. Initial laboratory efficiencies for single junction a-Si:H cells have also been competitive with an efficiency mark of roughly 12% [18]. As shown in Figure 10 in the early 2000’s thin film a-Si:H solar cells dominated the thin film PV market [7]. However, in 2014 a-Si:H made up only 1.5% of the total PV market with only 0.8 GWp of installation. This low utilization and stagnant growth of thin film a-Si:H cells is primarily a result of the notorious Staebler-Wronski (SW) effect [25].

The SW effect causes light induced degradation to a-Si:H. As a result, gap state defects emerge in a-Si:H upon exposure to sunlight. These defects increase recombination and rapidly lower the efficiency of a-Si:H cells. This SW effect, which has still yet to be solved, causes the final efficiency of a typical a-Si:H solar cell to saturate at a timid 6-7% within months [26]. As a result of the SW effect methods seeking to use a-Si:H in solar cells are generally limited to multijunction and tandem cells. In these architectures, a very thin a-Si:H top cell is employed for the strong absorption of high energy photons (>1.8 eV) while a thicker bottom cell made of the more weakly absorbing nc-Si:H absorbs lower energy photons (>1.1 eV).

![Production 2011 (MWp)](image)

**Figure 10:** Emergence of CdTe and CIGS TFSC’s over a-Si:H in recent years [7]
In addition to its role as the bottom cell in multijunction devices nc-Si:H is also used as the conductive p-type and n-type contacts for single junction a-Si:H solar cells since doped a-Si:H is of inferior electronic quality. Due to the weak absorption of nc-Si:H this material was little investigated as a stand-alone absorbing material for TFSCs until the early 1990’s [27]. The lower efficiency of nc-Si:H cells compared to CdTe and CIGS cells led to very little investment of nc-Si:H as a solar cell material. In recent years, however, nc-Si:H has become a material of interest. The discovery of grain boundary passivation by atomic hydrogen has led to decreased recombination and increased the performance of single junction nc-Si:H cells. In the last few years the efficiency of thin film nc-Si:H cells has improved from 10.1% to 11.8% as a result of using textured substrates with hexagonal dimple arrays for improved light trapping [28,29].

The disadvantage of nc-Si:H is that this material is a weaker absorber than a-Si:H, and as a result thicker layers on the order of several μm are typically required for sufficient light absorption. The lower band gap of nc-Si:H (~1.1 eV) also reduces $V_{OC}$ relative to the larger band gap (~1.8 eV) a-Si:H. On the plus side, this lower band gap allows for the absorption of a wider range of energies since photons with energies between 1.1-1.8 eV, which were unavailable for absorption in a-Si:H, can now be absorbed. As a result, cells based on nc-Si:H typically have higher $J_{SC}$ values than those based on a-Si:H.

From a processing standpoint, both nc-Si:H and a-Si:H are most commonly deposited from the gas phase by plasma enhanced chemical vapor deposition (PECVD) with a silane/hydrogen gas chemistry ($\text{SiH}_4/\text{H}_2$). Typical deposition rates for nc-Si:H (few nm/min) are almost a full order of magnitude lower than those of a-Si:H (10’s nm/min) [18]. This reduction in throughput associated with nc-Si:H has introduced an economic hurdle to bringing nc-Si:H based cells to an appreciable market share. To circumvent this limitation, techniques are
being investigated to increase the deposition rate of nc-Si:H by using very high frequency (VHF) PECVD [30], high pressure PECVD [31], and hot wire chemical vapor deposition (HWCVD) [32]. Additionally, exfoliation techniques in which thin Si layers are peeled from bulk Si ingots are also being investigated to avoid gas phase processing altogether [33].

An alternative solution to the lower deposition rates inhibiting nc-Si:H would be to innovate ways to use thinner layers of nc-Si:H by increasing the effective thickness of nc-Si:H as a result of architecture variations conducive to light trapping. This route will be a primary focus of this thesis. Table 2 summarizes key features of first and second generation solar cells.

<table>
<thead>
<tr>
<th>Absorber material</th>
<th>PV Market share</th>
<th>CPW ($)</th>
<th>Max PCE</th>
<th>PCE Range</th>
<th>$E_g$ (eV)</th>
<th>Absorber thickness</th>
<th>Common deposition technique</th>
<th>Notable Company</th>
</tr>
</thead>
<tbody>
<tr>
<td>c-Si</td>
<td>&gt;90%</td>
<td>2.50-3.50</td>
<td>25.6%</td>
<td>13-18%</td>
<td>1.1</td>
<td>100's of μm</td>
<td>Crystal growth</td>
<td>SolarCity</td>
</tr>
<tr>
<td>CdTe</td>
<td>4%</td>
<td>0.49-1</td>
<td>21%</td>
<td>10.5-16%</td>
<td>1.5</td>
<td>1’s of μm</td>
<td>Sputtering</td>
<td>First Solar</td>
</tr>
<tr>
<td>CIGS</td>
<td>3.50%</td>
<td>0.6-1</td>
<td>20.5%</td>
<td>10-12%</td>
<td>~1.2</td>
<td>1’s of μm</td>
<td>Sputtering</td>
<td>Solyndra</td>
</tr>
<tr>
<td>a-Si:H</td>
<td>0.80%</td>
<td>2-2.50</td>
<td>13.60%</td>
<td>5-10%</td>
<td>1.8</td>
<td>100's of nm</td>
<td>PECVD</td>
<td>Dupont</td>
</tr>
</tbody>
</table>

Table 2: A comparison of some key features of various solar technologies

The absorber material of focus in this thesis will be thin film nc-Si:H. Despite the currently untapped market for this material illustrated in Table 2 nc-Si:H offers great promise with respect to the goals of this thesis. Reasons nc-Si:H has been chosen are: (1) thin film Si materials can be deposited with plasma enhanced chemical vapor deposition (PECVD) allowing for the conformal deposition on unique light trapping topographies such as the ones to be used in this thesis, (2) nc-Si:H has a higher tolerance to light soaking than a-Si:H does [34], (3) Si is far more abundant than all other thin film solar cell absorber materials, (4) Si is a benign material with no toxic elements, (5) Si is amphoteric, allowing for simple devices based on only one
absorber material, and (6) the gas phase deposition of Si thin films is already very well established and easily borrowed from the semiconductor processing industry.

As it will be further discussed in Chapter 5, the PECVD growth parameters strongly influence the structural quality of the nc-Si:H. This material is a complex hybrid composed of grains of crystalline silicon, amorphous content, and voids. The relative proportion of these materials is dictated by the PECVD growth parameters (gas types, gas flows, temperature, pressure, power) and the substrate (topography, chemistry). The key distinction between nc-Si:H and μc-Si:H is the size of the grains. Generally, nc-Si:H is taken to have grains with an average size of less than ~100 nm while μc-Si:H has grains with an average size between 100-1000 μm. However, since grain sizes can evolve with film thickness and a variety of other processing variables there is no clear cut off point between one material and the other and as a result the terms nc-Si:H and μc-Si:H are often used interchangeably in the literature.

Comparison between Figures 8 and 10 shows that between 2011 and 2014 TFSCs have reduced their total PV market share from ~14% in 2011 to ~10% in 2014. Despite the decrease in their relative market share the overall production of TFSCs has still increased over that same time period [18]. Novel fabrication methods and innovative device architectures, such as those which will be investigated in this thesis, may ultimately be required to increase the relative market share of TFSCs in order to keep pace with the continuously increasing production capacity of first generation c-Si technologies.

Together, first and second generation photovoltaics make up virtually the entire solar cell market. However, as shown in Figure 9, other types of solar cells including multijunctions and other emerging technologies have also been the subject of much research interest. Together, these two branches of solar technology are classified as third generation photovoltaics.
1.6 Third generation solar cell technologies

Traditional first and second generation solar cells are limited by a theoretical limit known as the Shockley-Queisser limit [35]. This limit essentially establishes a maximum efficiency for a given solar cell type based on the bang gap energy of the solar cell’s absorbing material as shown in Figure 11 [36]. For example, crystalline Si with a band gap of 1.1 eV has a maximum possible efficiency of ~31% according to the Shockley-Queisser limit [35].

In Figure 11 the pink area represents the losses as a result of below band gap photons, the green area represents the losses as a result of band edge relaxation for above band gap photons, and the blue region represents the balance of other losses. Third generation multijunction and tandem photovoltaic devices overcome one or more of these loss mechanisms in order to create devices which could theoretically overcome the Shockley-Queisser limit.

Figure 11: The Shockley-Queisser limit dictates a maximum efficiency based on the solar cell absorber material’s bandgap [36]
The purple and red lines in Figure 9 show the efficiency for third generation multijunction solar cells and emerging photovoltaics over time respectively. As seen by the purple line in Figure 9 multi-junction and tandem cells exceed all other types of solar cells in terms of performance; in fact, this is the only type of solar cell to exceed the 30% efficiency mark. These devices have extremely high efficiencies of up to 46%. For extra-terrestrial applications solar cells with extremely high efficiency are necessary, since the cost to get the device into space will alone be high. Therefore, the added fabrication costs associated with extremely complex but ultrahigh performance devices are not a concern. Currently, these multi-junction devices are far too complex and expensive for terrestrial use, and for this reason their relative share of the total PV market remains nominal.

The red line in Figure 9 represents all other types of solar cells. The balance of third generation solar cells is lumped into the category of emerging photovoltaics. These include organic photovoltaics (OPVs), dye sensitized solar cells (DSCs), quantum dot cells, inorganic cells using absorbers other than those already discussed, and the recently emerging perovskite based cells. Perovskite cells have attracted immense research interest in the last 5 years as a result of their rapidly increasing laboratory efficiencies. Over the last few years these devices have increased from ~10% in 2012 [37, 38] to over 20% today [39]. Since these cells are conducive to liquid phase processing high throughput and printing technologies are also possible. Realizing the full potential of perovskite PV will require time, however, since their long term stability and efficiency is still unknown as a result of this branch of PV still being in its infancy.

Although this thesis will focus on novel device architectures for second generation photovoltaics it is important to acknowledge much of the work done here may also be applicable and relevant to many of the branches of the emerging photovoltaics.
1.7 Contributions of this thesis

1. Investigated structure-properties-processing relations for solar cell materials including nickel oxide (NiO), aluminum doped zinc oxide (AZO), and nanocrystalline Si (nc-Si:H)

2. Identified various fabrication schemes for highly ordered nano-element arrays out of various materials over large lateral areas with a high degree of tunability on dimensions

3. Developed and established deposition conditions for the atomic layer deposition of NiO using a novel nickel amidinate precursor Ni(amd) and water.

4. Developed an alternate NiO fabrication method by establishing the thermal oxidation parameters required for the oxidation of metallic electron beam evaporated Ni

5. Exhaustively characterized, compared, and contrasted NiO films fabricated with methods corresponding to (4) and (5) above

6. Completed NiO HTL devices which demonstrated an increased efficiency relative to planar control devices due to a >20% enhancement in FF and ~9% enhancement in V_{OC}

7. Completed devices built on nanostructured polyimide elements which demonstrated an increased efficiency relative to planar control devices due to a >20% enhancement in J_{SC}

8. Identified topography induced defects explaining the lower V_{OC} values for the light trapping architecture relative to the planar architecture seen in (7) above

9. Developed a working model for the cause of the defect formation in nc-Si upon its deposition onto irregular light trapping topographies when using SiH_{4}/H_{2} gas chemistries.

10. Identified SiF_{4}/H_{2}/Ar as a more viable PECVD gas chemistry to deposit defect free nc-Si:H onto irregular light trapping topographies

11. Provided extensive experimental detail and important processing considerations for future experimenters to continue on this work in a timely and efficient fashion.
Chapter 2: Background

2.1 Light Trapping

When light impinges on a solar cell it can do one of three things: it can be transmitted, it can be reflected, or it can be absorbed. Since solar cells generate power by absorbing light to create photogenerated current it is of high importance to maximize the absorption of light by minimizing the reflection and transmission of light. Equation 2.1 shows the simple relationship between the wavelength dependent absorptance \( A(\lambda) \), reflectance \( R(\lambda) \), and transmittance \( T(\lambda) \). Equation 2.2 illustrates the value of minimizing \( R(\lambda) \) and \( T(\lambda) \) in order to increase \( A(\lambda) \) and thereby \( J_{SC} \). Increasing \( J_{SC} \) can then lead to PCE enhancements as shown in equation 1.1. Here, \( \phi(\lambda) \) is the input solar flux of the air mass 1.5G solar spectrum shown in Figure 4 [11].

\[
A(\lambda) = 1 - R(\lambda) - T(\lambda) \quad [2.1]
\]

\[
J_{SC} = e \int_{spectrum} A(\lambda) \phi(\lambda) d\lambda \quad [2.2]
\]

In order to reduce the contribution of \( R(\lambda) \) in equation 2.1 antireflective coatings (ARCs) have been used for many years. For a bare Si substrate \( R(\lambda) \) can be in excess 30% for many wavelengths, fortunately, these reflections can be reduced to under 10% when an appropriate ARC layer is employed [40]. For an ARC material with a particular index of refraction \( n \) a select wavelength \( (\lambda_{\text{min}}) \) can undergo minimum reflection by setting the thickness of the ARC equal to a quarter wavelength \( (\lambda_{\text{min}}/4) \) for destructive interference in accordance to equation 2.3.

\[
d = \frac{\lambda_{\text{min}}}{4n} \quad [2.3]
\]
Selecting materials to use for ARC coatings is relatively straightforward. Equation 2.4 shows how the refractive indexes of the two materials at the potential reflection interface, that is, air \((n_{\text{air}})\) and the absorber material \((n_{\text{abs}})\), dictate the optimum \(n\) value for the ARC coating.

\[
n^2 = n_{\text{air}} n_{\text{abs}} \quad \text{[2.4]}
\]

The refractive index of Si at \(\lambda=600\) nm is \(\approx 3.6\). Therefore, the optimum \(n\) value of an ARC coating for minimizing the reflection of photons with \(\lambda=600\) nm for Si is about 1.9 [41]. Coupling an \(n=1.9\) ARC material with equation 2.3 shows an ARC layer thickness of \(\approx 80\) nm would be employed to minimize the reflection of photons with \(\lambda=600\) nm for a Si solar cell.

Common ARC materials include TiO\(_2\) (\(n=2.3\)), SiN\(_x\)::H (\(n=1.85-3.3\)), Al\(_2\)O\(_3\) (1.8-1.9), and SiO\(_x\) (\(n=1.46-1.9\)) [40]. The PECVD of SiN\(_x\)::H is the most common system for the deposition of an ARC material for multicrystalline Si solar cells [40]. The efficiency improvements as a result of using an ARC coating can be significant for planar topographies: a spray coated TiO\(_2\) ARC affords a roughly \(\approx 30\%\) increase in efficiency for multicrystalline Si solar cells [41].

The use of TCOs for thin film solar cells in place of patterned bar structures reduces the need for an ARC with TFSCs since the TCO has sufficient ARC properties. In addition, when topographies deviate from planar, a more gradual variation in the effective cross sectional index of refraction will increase light in-coupling by impedance matching at interfaces. As a result, the improvements resulting from of an ARC layer become less significant as the topography becomes less planar. This thesis will not use an ARC layer since it will already be using non-planar TCO topographies with enhanced light in-coupling, however, an additional PECVD SiN\(_x\)::H step could easily be added if one were deemed necessary. Figure 12 depicts how structured topographies increase light in-coupling (thereby reducing \(R(\lambda)\)) relative to a planar
cell through impedance matching at interfaces. Here, aluminum doped zinc oxide (AZO) with $n \approx 2$ is used as a TCO and Si with $n \approx 3.6$ is used as the absorber.

![Planar topography and Structured topography](image)

**Figure 12:** Structured topographies reduce reflections through impedance matching at interfaces.

The topography shown on the right side of Figure 12 is also conducive to the concept of light trapping. Observation of equation 2.1 shows minimizing $R(\lambda)$ is only half the battle in maximizing $A(\lambda)$. The excess light entering the solar cell by reducing $R(\lambda)$ is only of use if it can be absorbed before it is transmitted. Therefore, much work has went into innovating schemes to reduce $T(\lambda)$ by innovating light trapping architectures for solar cells. As shown, when light trapping architectures induce geometry changes to the top surface of the solar cell such structures can simultaneously reduce $R(\lambda)$ through improved light in-coupling and reduce $T(\lambda)$ through light trapping. As a result, a good light trapping architecture can also mitigate the need for an additional ARC layer.

The concept of light trapping is a very active research area. In short, light trapping seeks to increase the optical path length of light within the absorber of a solar cell in order to increase
the probability light can be absorbed. Conventionally, light trapping has been achieved in TFSCs by randomly texturing the top TCO contact with a wet chemical etching step. Random texturing increases the scattering at interfaces between adjacent layers with different indexes of refraction and thereby enhances light trapping. This effect is shown in Figure 13 [42].

Common TCO materials used for light trapping through random texturing include textured aluminum doped zinc oxide (AZO) and textured fluorine doped tin oxide (SnO$_2$:F) developed by Asahi glass. Thin films of SnO$_2$:F prepared by CVD are one of the most common TCO materials used for the manufacturing of thin film Si solar cells. Alternatively, AZO has had much success as a TCO material at the research level since it can be deposited with a variety of common deposition techniques including sputtering, low pressure chemical vapor deposition (LPCVD), and atomic layer deposition (ALD). Sputtered AZO is highly conductive and smooth as deposited. A post deposition etch treatment of the AZO can modify the roughness over a wide range to afford a variety of topographies. As a result, sputtered AZO is a common material being used for optimizing light scattering effects for a variety of wavelength ranges.

**Figure 13:** Random texturing is most commonly used to increase light trapping in TFSCs [42]
For randomly textured TCO substrates the sizes and shapes of the features of the TCO will dictate the light scattering properties and thereby control the light trapping ability of the solar cell. Figure 14 shows typical randomly textured TCO structures: SnO$_2$:F grown by atmospheric pressure chemical vapor deposition (APCVD) (left) and sputtered AZO with a post deposition wet etch treatment (right). Here, it is of great importance that the feature sizes of the SnO$_2$:F are several times smaller than those of the AZO. This results in an over twofold increase in the root mean square (RMS) roughness of the AZO compared to the SnO$_2$:F [42]. Here, these two TCO materials perform similarly when using an a-Si:H absorber [43] but the larger features of AZO become significant when the larger wavelengths only available to nc-Si:H are to be optimally scattered for light trapping. The indirect band gap of nc-Si:H makes this material a relatively poor absorber. This results in nc-Si:H absorbing less than all of the available incident light in a single pass through the semiconductor. Here, the lower energy photons distinctly available to nc-Si:H are at the highest risk of not being absorbed in a single pass, therefore, the use of light trapping architectures should have the largest influence on absorbing more of the lower energy photons available to nc-Si:H. As shown in Figure 4, these lower energy photons (~800-1100 nm) make up a significant portion of the input AM1.5G spectrum, so their full absorption is desired for maximizing $J_{SC}$, and therefore PCE. In relation to Figure 14, the larger feature sizes of textured AZO have been shown to serve well in single junction nc-Si:H solar cells [44]. For this reason, among others to be discussed, AZO will be a TCO material of focus on this thesis.
The random nature of light trapping architectures such as those shown in Figure 14 makes it difficult to make direct correlations between the light scattering topography and the cell efficiency. In addition, the lack of periodic boundary conditions for such randomly textured architectures would make the optical simulation of solar cells employing such textures extensively time consuming and complex [28, 29]. Similar to the other state of the art work being done in the area of light trapping this thesis will use a highly ordered periodic nano-element array for light trapping. Ordered geometries permit more direct correlations between light trapping architectures and the device performance. This allows for a higher degree of process optimization through architecture tuning and greatly cuts down on simulation times.

The motivation for light trapping architectures stems from the inherent tradeoff between the absorption and collection abilities of conventional planar cell architectures. Planar cells using a thick enough absorber to capture all available photons will not be able to collect all of the photogenerated carriers as a result of the minority carrier diffusion length in the absorber being
less than the thickness of the absorber (Figure 15 left). As a result, some of the volume is wasted since photogenerated carriers in that volume do not contribute to the photocurrent. On the other extreme, very thin absorbers miss out on capturing all of the available light (Figure 15 center). By introducing vertical collection elements within the absorber the collection length ($L_C$) and absorption length ($L_{abs}$) of the semiconductor can be decoupled (Figure 15 right). Collectively, we term this the light and carrier collection management (LCCM) concept, since this architecture serves to assist with both the trapping of light and the collection of photogenerated carriers [45].

**Figure 15:** Thick planar cells waste volume (left) thin planar cells waste light (middle) LCCM cells decouple the absorption length ($L_{abs}$) and the collection length ($L_C$) to make maximum use of volume (white material). Dashed arrows show useful volume for planar architectures. [45]

In reality, for thin film Si absorbers, ordered light trapping arrays such as that seen on the right side of Figure 15 will serve to induce a nano-dome morphology on the surface of the absorber material similar to that shown in Figure 12 (right). This is a consequence of the conformal deposition techniques used for depositing thin film Si materials (*i.e.* PECVD). For the maximum lateral packing density of these nano-domes a 2D hexagonal arrangement is used.
Figure 16 (left) shows a standard arrangement of ordered light trapping nano-domes. The spacing between the domes (L) and thickness of the absorber (t) shown in Figure 16 (right) are critical geometrical parameters in establishing the light trapping capability of the solar cell. The geometric tuning of these dimensions and their specific influence on light trapping will be the focus of the numerical modeling work to be discussed in Chapter 4.

Devices in this thesis work employing the LCCM architecture will repeat the hexagonal nano-dome array over a large lateral area equal to the active area of the solar cell by using a variety of nanofabrication techniques to be discussed in Chapter 5. These nano-domes serve to increase the optical path length of light in the cell and shape wave fronts for the enhanced focusing of the electromagnetic field in the absorber material [46]. Such ordered periodic arrays have also shown to give rise to additional light trapping phenomena as a result of complex optical phenomena including Bloch modes, diffraction aided wave guiding, Mie resonances, and plasmonic effects [46]. The following section will briefly overview the current status of the research being done in the area of light trapping in solar cells.

Figure 16: Hexagonal assortment of nano-domes (left) cross section of nano-domes (right) [Adapted from 46]
2.2 Current status of light trapping technologies

The use of light trapping architectures for thin film solar cells is a current area of investigation for various research groups. In the state of the art work, a recurring theme for light trapping architectures is the use of periodically ordered structures (\textit{i.e.}, hexagonal lattice) with a period on the order of 100s to 1000s of nm [28, 29, 47-50].

A major hurdle for the inclusion of light trapping architectures into thin film silicon solar cells has been that the aggressive topographies most conducive to light trapping (\textit{i.e.} random pyramidal textures such as Figure 14 or periodic arrays such as Figure 16) have both been shown to induce defects in the subsequently deposited silicon absorber layer. Figure 17 shows how a randomly textured sharp ‘V-shaped’ pyramidal morphology, which is conducive to light trapping, leads defects in the $\mu$-Si:H absorber layer [51]. As a result, gains in $J_{SC}$ from enhanced light trapping are partially offset by losses in $V_{OC}$ and FF resulting from a reduction to the quality of the absorber layer. Therefore, defect formation in the absorber introduces a tradeoff between the electrical parameters which establish the efficiency of a solar cell.

To avoid defect formation in the absorber upon its deposition onto randomly textured pyramidal morphologies one common approach has been to use a surface treatment to smoothen such rough ‘V-shaped’ pyramidal morphologies to more gentle ‘U-shaped’ morphologies [51]. However, these smoother ‘U-shaped’ morphologies are less conducive to light trapping. Since both topographies shown in Figure 17 used identical PECVD parameters for the $\mu$-Si:H growth it follows that the TCO topography itself has an important influence on the structural integrity of the absorber material deposited on top of it.
Figure 17: Surface smoothening can be used to avoid defect formation in the absorber [Adapted from 51]

The defective regions of the absorber material are often referred to as ‘cracks’. The term crack can be misleading as these defective areas are not entirely void of material; instead, they are areas of low quality and low density porous amorphous tissue [51, 52]. Single junction p-i-n Si solar cell devices fabricated based on the topographies shown in Figure 17 were shown to have higher $V_{OC}$ and FF values on the defect free ‘U-shaped’ morphology than on the defective ‘V-shaped’ morphology [51]. This is a result of the defects in the absorber leading to increased recombination ($V_{OC}$ reductions) and degraded transport properties (FF reductions). Clearly, in the fabrication of light trapping solar cells, there is a tradeoff between a good light trapping architecture (increases in $J_{SC}$) and absorber material quality (decreases in $V_{OC}$ and FF).

The thickness of the absorber itself also has an influence on defect formation. It has been shown defects are more likely to form as the nc-Si:H film becomes thicker [52]. Therefore, well designed light trapping architectures seek to improve performance and ultimately decrease the CPW in multiple ways: (1) they can absorb an equivalent amount of light using a thinner...
absorber material which is less susceptible to defect formation, (2) since they use less material they will require a shorter deposition times for increased throughput, and (3) by using well-ordered textures a direct correlation between the device geometry and the electrical parameters \( (V_{OC}, \text{FF}, \text{and } J_{SC}) \) can be established. These relations provide the information needed for the iterative numerical optimization needed for obtaining an ideal light trapping architecture.

The Sai group in Japan is a current global leader in making such correlations between the geometry of ordered light trapping structures and solar cell performance. This group has fabricated and characterized over 200 n-i-p \( \mu \text{c-Si:H} \) cells on ordered honeycomb textures with various periods and absorber thicknesses. Recently, the Sai group improved the efficiency of single junction \( \mu \text{c-Si:H} \) solar cells from 10.1\% to 11.8\% as a result of the light trapping enhancement provided by their ordered hexagonal light trapping arrays [53]. To circumvent the defect formation in the \( \mu \text{c-Si:H} \) the Sai group observed a correlation between the period of their hexagonal array \( P \) and the thickness of their absorber \( t_i \). They found the condition \( P \sim t_i \) is needed to mitigate defect formation in the \( \mu \text{c-Si:H} \) [49]; when \( P \ll t_i \) defect formation occurs, and when \( P \gg t_i \) the light trapping properties are reduced as the topography of the absorber becomes more planar.

Figure 18 (left) shows the ordered periodic hexagonal array used by the Sai group with a period of 1.5 \( \mu \text{m} \) and a total absorber thickness of \( \sim 3 \mu \text{m} \). The cut line for the TEM image is also shown. The corresponding TEM image for the 1.5 \( \mu \text{m} \) period is shown to have defects in the \( \mu \text{c-Si:H} \) (Figure 18 middle) while the TEM image for a larger 3.5 \( \mu \text{m} \) period (with an identical 3 \( \mu \text{m} \) film thickness) has no defects (Figure 18 right). These results support their conclusion that \( P \sim t_i \) is ideal for avoiding defects in the absorber while maintaining sufficient light trapping properties.
Figure 18: The condition $P-t_i$ is required to avoid defect formation in periodic light trapping structures while maintaining sufficient light trapping properties [Adapted from 49]

The 3 $\mu$m layer shown in Figure 18 is composed of three stacks of 30 nm nc-SiO$_x$:H/900 nm $\mu$c-Si:H. This was done to get contrast for the cross sectional transmission electron microscope (TEM) observation in order to observe the interfacial growth characteristics between $\mu$c-Si:H and nc-SiO$_x$ which are characteristic to multijunction devices. Based on these observations the Sai group produced a-Si:H/$\mu$c-Si:H/$\mu$c-Si:H triple junction cell in the substrate configuration using a combination of thickness (4 $\mu$m) and period (4 $\mu$m) which avoided defect formation. This device had a 13.6% world record stabilized efficiency for a silicon thin film solar cell [49].

For single junction nc-Si:H cells efficiencies in excess of 11% have also been achieved by the Sai group as a result of their well-designed light trapping architectures. However, these single junction devices still have much room for improvement. The use of light trapping architectures coupled with hydrogen doped indium oxide (IOH) top contacts in single junction
devices have given J_{SC} values as high as 33 mA/cm^2 [49] but these devices had less than optimum V_{OC} and FF values. A high V_{OC} value of 0.607 V [54] and a high FF value of 0.738 [50] have been independently demonstrated in other works for single junction nc-Si:H cells. Therefore, in accordance to equation 1.1 an efficiency in excess of 14% is possible in the event V_{OC}, FF, and J_{SC} could be simultaneously optimized. The simultaneous optimization of J_{SC}, V_{OC}, and FF could prove to be a difficult task, however, since as it has been discussed the light trapping architectures which increase J_{SC} can also lead to defects in the absorber which decrease V_{OC} and FF through increased recombination and inferior transport properties respectively.

In our research we have also observed this defect formation occurring in the nc-Si:H upon its deposition onto our own periodic light trapping architectures. Chapter 5 will continue this discussion on defect formation in the nc-Si:H as it pertains to our work and how we sought to resolve it. In addition to eliminating, or at least reducing, the formation of defective regions in the nc-Si:H absorber another possible way in which the contact recombination and transport properties can be remedied while maintaining a light trapping architecture is through the use of a transport layer. The following section will introduce transport layers and their use in solar cells.

2.3 Transport layers

Most heavily used in third generation organic photovoltaic (OPV) cells, transport layers can be used to improve the asymmetric charge carrier movement in a solar cell [55]. Although the focus of this thesis is not on OPV cells a brief overview of their structure and mechanism is first necessary in order to clarify the principles of transport layers as they pertain to the field of organic photovoltaics. Knowledge of basic transport layer properties can then be extended to other types of first and second generation solar cells such as those which will be fabricated in this thesis work.
Organic solar cells employing the bulk heterojunction (BHJ) configuration commonly employ both a hole transport/electron blocking layer (HT/EBL) and an electron transport/hole blocking layer (ET/HBL) for efficiency enhancements. Often, HT/EBL and ET/HBL are further abbreviated as HTL and ETL respectively; some ambiguity does exist here since not all HTL’s are necessarily good EBL’s and not all ETL’s are necessarily good HBL’s. With this said, the BHJ absorbing material is most often comprised of a mixture of the polymers phenyl-C$_{61}$-butyric acid methyl ester (PCBM) and poly(3-hexylthiophene-2,5-diyl) (P3HT). Light absorption by the P3HT:PCBM heterojunction material leads to the creation of an exciton, which can be dissociated at the phase boundaries separating the P3HT and the PCBM. With the proper processing conditions of the BHJ active layer solution (weight %, relative P3HT:PCBM weights, thermal and solvent annealing conditions, etc.) the P3HT and PCBM can be phase separated at the nanometer level and therefore the dissociation of photogenerated excitons is very efficient. This allows the majority of the photogenerated excitons to be separated, affording free electrons and free holes. It follows that an ideal P3HT:PCBM absorber will be mixed such that it has phase domains between the P3HT and the PCBM which match the average exciton diffusion length in polymers, which is on the order of 10-30 nm [56]. Following exciton dissociation the PCBM acts as an electron acceptor and transports electrons to a low work function cathode (e.g. Al) while the P3HT acts as an electron donor and transports holes to a high work function anode (e.g. indium tin oxide (ITO)).

The insertion of a thin layer of poly(3,4-ethylenedioxythiphen)-poly(styrenesulfonate) (PEDOT:PSS) between the hole collecting anode (most often ITO) and the absorber layer is well known to enhance the efficiency of OPV solar cells by serving as an effective HTL. This PEDOT HTL can be thought of as a semi-permeable membrane for hole transport to the anode.
That is, the PEDOT will conduct free holes in the P3HT to the anode while simultaneously preventing free electrons in the PCBM from traveling to the anode. In much the same way, materials such as LiF can be used as an ETL to selectively transport electrons to the cathode. The insertion of HT/EBL and ET/HBL layers is valuable since they reduce recombination at the cell contacts and thereby improve device performance. Generic depictions of the regular and the inverted organic solar cell device architectures are shown in Figure 19 (left). The asymmetric charge carrier transport characteristics in OPV devices based on the energy levels of the active layer material, ETL, HTL, and electrodes are also shown in Figure 19 (right) [55].

Figure 19: General structures (left) and operational transport characteristics (right) of organic solar cells [55]

Figure 20 shows the JV performance of two organic solar cells made by the author in 2008. The control cell had the configuration ITO/P3HT:PCBM/LiF/Al and the device employing a PEDOT HTL had the configuration ITO/PEDOT/P3HT:PCBM/LiF/Al. Here, the insertion of a thin (~40 nm) layer of PEDOT enhanced the OPV device performance by close to 30% relative to the control cell as shown by the performance of these devices summarized in
Table 3. Here, it can be seen that the primary cause for the increase in efficiency is through the large increase in $J_{SC}$ provided by the PEDOT layer which provides a more conductive and asymmetric pathway for photogenerated holes to selectively exit the cell through the ITO anode.

![P3HT:PCBM Organic Solar Performance](image)

**Figure 20:** A comparison of JV characteristics between a control organic solar cell and an organic solar cell using a PEDOT HTL. The HTL enhances cell efficiency by close to 30%.

<table>
<thead>
<tr>
<th>Cell type</th>
<th>PCE</th>
<th>$V_{OC}$ (V)</th>
<th>$J_{SC}$ (mA/cm$^2$)</th>
<th>FF (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Control</td>
<td>2.67</td>
<td>0.59</td>
<td>7.59</td>
<td>0.6</td>
</tr>
<tr>
<td>PEDOT</td>
<td>3.45</td>
<td>0.6</td>
<td>9.16</td>
<td>0.63</td>
</tr>
<tr>
<td>% Change</td>
<td>29.2</td>
<td>1.7</td>
<td>20.7</td>
<td>5.0</td>
</tr>
</tbody>
</table>

**Table 3:** Performance of the organic solar cells with JV characteristics shown in Figure 20

The discussion up to this point hints that a strong understanding of energy band diagrams is necessary for selecting optimum HTL and ETL materials for a given absorber. The work function ($\phi_W$), electron affinity ($\chi$), and band gap ($E_G$) of a given absorber will dictate both (1) what types of metals are required to make Ohmic contacts and (2) what types of materials will be
suitable for use as transport layers. In addition to selecting a transport layer with the appropriate energetic parameters with respect to those of the semiconductor and contacts (\(\phi_{WF}, \chi, E_G\)) ideal transport layers should not have unfavorable chemical reactions with the semiconductor or contact layer materials on either side of it. At the same time, the transport layer must have good adhesion to the layers on either side of it. The transport layer should be able to be deposited at a temperature the absorber material can tolerate. In architectures employing the transport layer on the top of the device a high optical transparency of the transport layer is also required in order to minimize absorption losses. Finally, a high hole (or electron) conductivity is desired for a HTL (or ETL) respectively. Clearly, selecting an appropriate transport layer material for a given solar cell absorber material system is a demanding process. Table 4 summarizes key characteristics HT/EBL and ET/HBL transport layer materials.

<table>
<thead>
<tr>
<th>Type</th>
<th>(\phi_{WF}) value</th>
<th>(\chi) value</th>
<th>Energy step location</th>
<th>Chemistry</th>
<th>Desired conductivity</th>
<th>Examples</th>
</tr>
</thead>
<tbody>
<tr>
<td>HT/EBL</td>
<td>Forms Ohmic contact to anode</td>
<td>Similar or larger than absorber</td>
<td>In conduction band</td>
<td>Avoid reactions with p-absorber/anode</td>
<td>p-type</td>
<td>PEDOT, MoO(_3), NiO</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ET/HBL</td>
<td>Forms Ohmic contact to cathode</td>
<td>Smaller than absorber</td>
<td>In valence band</td>
<td>Avoid reactions with n-absorber/cathode</td>
<td>n-type</td>
<td>ZnO, TiO(_2), Nb(_2)O(_5)</td>
</tr>
</tbody>
</table>
Figure 21 (E_{VL}) to the strength of the internal electric drift field (E) across that region of the device (x).

\[ E = -\frac{dE_{VL}}{dx} \]  \[2.5\]

In addition to the electric field within the absorber breaking symmetry the introduction of HTL (blue) and ETL (purple) layers add effective fields to the energy band diagram which further break symmetry. An energy step in the conduction band level (E_C) is characteristic of a HT/EBL layer and an energy step in the valence band level (E_V) is characteristic of an ET/HBL layer. The energy step induced in E_C by an HT/EBL layer provides an energetic barrier for photogenerated electrons in order to prevent them from diffusing down the concentration gradient towards the anode which is intended to collect holes only. Essentially, the HT/EBL layer has no available states for the photogenerated electrons to travel through. Analogously, the energy step induced in E_V by an ET/HBL provides an energetic barrier for holes in order to prevent them from diffusing to the electron collecting cathode. In each case, the energy step location and magnitude are dictated by the \( \chi \) and \( \phi_{WF} \) values of the transport layer material relative to those of the solar cell absorbing material. The hypothetical ideal transport layers shown in Figure 21 are chosen to have \( \phi_{WF} \) values which match those of their respective contacts such that both the HT/EBL and ET/HBL form Ohmic contacts with the anode and cathode respectively. Green arrows represent the permissible direction of charge flow for the photogenerated carriers and red arrows represent directions of flow that are forbidden as a result of the energy barriers introduced by the HT/EBL and ET/HBL layers. As seen in Figure 21, \( \chi_{HTL} \leq \chi_{Absorber} \approx \chi_{ETL} \) and the HTL is slightly p-type while the ETL is slightly n-type, all in accordance to the qualifications of the ideal transport layer characteristics specified in Table 4.
Figure 21: Hypothetical band diagram of a p-i-n absorber (maroon) sandwiched between an ideal HTL (blue) and an ideal ETL (purple). Green arrows represent energetically valid directions for charge transport and red arrows indicate unlikely directions of charge transport.

The parameters $\phi_{\text{WF}}$, $\chi$, and $E_G$ are well documented for the common thin film solar cell materials nc-Si:H, a-Si:H, CdTe, CdS, and the CIGS system. As a result, ideal HTL and/or ETL candidate materials can be narrowed down based on energetic alignment alone. Some energetically favorable materials will be eliminated as a result of unfavorable reactions with these absorber materials. As shown in Table 4, several different HT/EBL and ET/HBL materials have already been employed in solar cell devices. The following section will investigate the applications and processing considerations for the various transport layer materials currently being employed in solar cells devices. An overarching focus will be placed on transport layers as they pertain to organic solar cells since this is the field of photovoltaics primarily utilizing these layers. An emphasis will be placed on transport layer materials which also have a particularly high potential in conjunction with the inorganic absorber materials being used in this thesis work (e.g. AZO, NiO).
2.4 Current status of transport layer technologies

To date, transport layers have been the most heavily investigated for their use in organic solar cells [55]. In recent years their use in the emerging perovskite solar cells has also rapidly increased [37-39]. Common ET/HBL layers currently being investigated include ZnO, TiO$_x$, Cs$_2$CO$_3$, and Nb$_2$O$_5$ while common HT/EBL layers include NiO, PEDOT:PSS, MoO$_3$, WO$_3$, and V$_2$O$_5$. Applications, processing considerations, and emerging developments for each of these transport materials will now be discussed.

**ZnO:** For ETLs based on ZnO it has been found that the surface morphology and roughness of the ZnO has a critical impact on its effectiveness as an ETL [57]. Increasing the surface roughness of the ZnO by altering the process conditions (*i.e.* deposition method, annealing temperature, solvent evaporation rate for sol gel techniques, etc.) has led to efficiency enhancements for OPV devices based on ZnO ETLs. Higher efficiencies for rougher ZnO ETL layers result from enhancements to $J_{SC}$ and FF. Improvements to $J_{SC}$ are caused by enhanced light absorption by the active layer due to the rougher ZnO surface doing a better job scattering light; as discussed earlier in this chapter, the randomly textured TCO architectures are here again acting as light scattering structures. Higher FF values are explained by an increase in the ZnO’s crystallization induced by the processing conditions used to obtain a rougher surface: for the sol gel ZnO method a slower solvent annealing rate leads to rougher films. A consequence of this slower annealing rate is a higher degree of ZnO crystallization. The FF is strongly related to the ability of interfaces to extract charge carriers [57], and for ZnO it has been shown this extraction efficiency is enhanced for more crystalline films [58]. The ZnO film cannot be made to be arbitrarily rough, however, as excessive roughness damages the subsequently deposited absorber causing increases to contact resistance and leakage current [59]. The degree of ZnO
crystallization varies with film thickness while the energy level alignment at devices interfaces does not [60]. Therefore, the thickness of the ZnO ETL may be modified over a large range in order to obtain the optimum combination of surface roughness, crystallinity, and optical transparency. Due to the large number of deposition techniques for ZnO and its correspondingly high degree microstructure tuning this is one of the single most attractive and commonly used ETL materials.

The electrical conductivity of ZnO can be significantly increased by doping this material with a few atomic percent of Al to form aluminum doped zinc oxide (AZO) in accordance to the defect chemistry reaction shown in equation 2.6.

$$\text{Al}_2\text{O}_3 \overset{\text{in ZnO}}{\longrightarrow} 2\text{Al}^\text{Zn} + 2\text{O}^{x}_\text{O} + \frac{1}{2} \text{O}_2 (g) + 2\text{e}^- \quad [2.6]$$

Common deposition techniques for AZO are the same as those for non-doped ZnO, namely: sputtering, atomic layer deposition (ALD), and sol gel. Non-doped ZnO deposited by ALD has a resistivity on the order of ~3x10^{-2} Ω cm. By doping the ALD grown ZnO with ~3 to 4 atomic percent Al the conductivity of the ALD grown AZO can increase by close to an order of magnitude to ~5x10^{-3} Ω cm [61]. This reasonably high conductivity allows AZO to serve as a standalone TCO electron collecting cathode when an adequate thickness is used. Coupling the reasonable conductivity of AZO with this material’s high optical transparency makes AZO one of the most popular TCO materials for solar cells. This ALD grown AZO has been one of the most heavily investigated materials throughout the course of this research. Chapter 5 will discuss in detail the process-properties relations of the ALD grown AZO used in this thesis work.

**TiO_x:** Traditionally the most common types of solar cells employing TiO_x as an ETL are the dye-sensitized solar cells (DSCs) [62]. Depositing uniform and dense layers of TiO_2 on ITO glass substrates has proven difficult and as a result the application of TiO_x in other types of solar cells
has been limited [63]. The emergence of perovskite solar cells has led to a resurged interest in 
TiO₂ as a solar cell transport layer material since the mesoporous nature of TiO₂ films, which is 
unfavorable to other solar cell architectures, serves as an effective scaffold for the perovskite 
absorber material to infiltrate [64]. The photo-excited perovskite injects electrons into the TiO₂ 
scaffold which selectively transports these electrons to the FTO contact. Figure 22 (left) shows 
how the porous nature of the TiO₂ allows the infiltration of the drip casted perovskite absorber. 
This TiO₂ layer also prevents valence band holes from reaching the electron collecting FTO 
contact. The effective band alignment of TiO₂ with the conventional lead based perovskite 
material (CH₃NH₃PBI₃) is also shown in Figure 22 (right).

Recent developments have found the incorporation of acetylacetonated-based additives 
(e.g. Zn, Y, Zr, Mo) into the TiO₂ lead to a better carrier extraction ability of the TiO₂ and 
thereby enhance device efficiency [65]. Since both the sol gel processed mesoscopic TiO₂ layers 
and the subsequent infiltration of a drip casted perovskite into this TiO₂ scaffold are fully 
amenable to printable technologies the perovskite solar cell device architecture is conducive to 
roll to roll manufacturing techniques for high throughput mass manufacturing. In the coming 
decades if a long term stability of perovskite based solar cells is realized ETLs based on TiO₂ 
should play a significant role in this new and upcoming technology.
**Cs$_2$CO$_3$:** This material has been much less investigated as an ETL than ZnO or TiO$_2$. Nonetheless, notable work has found that the $\phi_{\text{WF}}$ of Cs$_2$CO$_3$ can be tuned by low post deposition annealing temperatures below 200$^\circ$C [66]. The deposition method of Cs$_2$CO$_3$ itself has not been found to make a large change on its effectiveness as an HTL; Cs$_2$CO$_3$ fabricated by evaporation has a similar effectiveness as Cs$_2$CO$_3$ fabricated by spin coating [67]. The influence of UV ozone has been shown to enhance the carrier extraction ability of Cs$_2$CO$_3$ enhancing $J_{\text{SC}}$; however this same treatment also decreased $V_{\text{OC}}$ [68]. The major drawback to Cs$_2$CO$_3$ is that its energy band alignment does not do a sufficient job at blocking holes [69]. So although Cs$_2$CO$_3$ is an excellent ETL it is a poor HBL. This is an example in which the ambiguity between ET/HBL and ETL is significant. Overall, the use of Cs$_2$CO$_3$ transport layers has been limited.

**Nb$_2$O$_5$:** This has been the seemingly least investigated of the proven ETL materials. One report uses Nb$_2$O$_5$ as an ETL for an inverted organic solar cell (ISC) [70]. Similar to ZnO and TiO$_2$ great care must be taken for the exact thickness of the Nb$_2$O$_5$ when employing this layer as an
ETL. This is a result of tradeoffs between the films being too thin and therefore non-continuous and films being too thick and therefore too insulating. This has been found especially true for Nb$_2$O$_5$, where an inadequate layer thickness rapidly degrades performance [70].

**ET/HBL summary:** At the current time ZnO and TiO$_x$ are said to represent the best overall electron transport/hole blocking layer properties owing to their wide range of deposition techniques and their fulfillment of the majority of the requirements of an ET/HBL shown in Table 4 [58]. Doping ZnO with Al leads to conductivity increases further increasing the value of this material as an ET/HBL or a standalone contact. Perovskite cells are likely to employ TiO$_2$ as an ETL in the future. Although Cs$_2$CO$_3$ has excellent electron transport properties its band alignment is not sufficient for blocking holes. Nb$_2$O$_5$ also has an unfavorable energy level diagram aside from its use in organic systems based on the electron acceptor material PCBM.

One goal of this thesis work is to employ a HT/EBL for an inorganic solar cell. This is a departure from the typical OPV devices utilizing these layers. One material offering great potential as a HT/EBL for inorganic solar cell devices is NiO. This is a result of the favorable band alignment of NiO with common inorganic thin film solar cell materials such as CdTe and Si. Each of the HT/EBL materials currently being investigated will now be addressed. A strong emphasis will be placed on NiO as this will be the material of focus in Chapter 3.

**NiO:** Thin films of NiO have many desirable HT/EBL properties including a high work function, a high optical transparency, chemical stability, and effective band alignment for electron blocking [71]. Since NiO is inherently a p-type wide band gap semiconductor it can also do a sufficient job conducting holes. Since NiO can be deposited through liquid processes such as sol-gel [72] and other wet chemical solution processes [73] it is also conducive to highly
manufacturable roll to roll and printing technologies. Transport layers based on NiO have already been employed in OPV devices on various occasions [71, 74, 75].

As introduced in Figure 21 and exemplified in Figure 22 the effective band alignment of an ET/HBL or HT/EBL material is critical for its ability to enhance selective carrier transport. Figure 23 shows the effective band alignment of NiO with the thin film material CdTe as a result of NiO having a valence band level at around -5.0 eV and a conduction band level at around -1.7 eV [76]. These energies clearly create a large step in the conduction band and thereby allow NiO to serve as an excellent electron blocking layer. Devices with the architecture shown in Figure 23 were fabricated in this thesis and their results will be presented in the following chapter.

**Figure 23:** Effective band alignment of NiO with CdTe solar cells [77]

Recent work in 2015 by Hsu et al. employed NiO as a HTL in organic solar cells based on the prototypical bulk heterojunction P3HT:PCBM configuration [71]. Similar to the case which was discussed for other metal oxides (e.g. Nb$_2$O$_5$) their work also found the exact thickness of the NiO has a critical influence on its effectiveness as an HTL: they found a 3 nm NiO HTL layer gave a 2.62% efficiency OPV device, a 4 nm layer gave a 3.38% efficiency
device, and an 8 nm layer gave a 2.37% efficiency device. This was said to be a result of the thinnest 3 nm layer being discontinuous, the 4 nm layer was the sweet spot in which a continuous film was first achieved, and the 8 nm film caused the insulating properties of bulk NiO to take over and drastically reduce the FF. These results were extremely consistent with those observed during this thesis work. In fact, the 2015 work using NiO used the same deposition method (ALD) and the same precursor as those used in our research; therefore, the properties of the films are expected to be very similar. Their work used UV photoelectron spectroscopy (UPS) to obtain the work function of the ALD grown NiO, and they found the work function was 5.12 eV for the as deposited ALD NiO. This value is consistent with the value our research group used in making the original decision to pursue NiO in accordance to the expected band alignment of NiO as a HT/EBL with CdTe as shown in Figure 23 [77]. The details of the fabrication processes for the NiO used in this thesis will be discussed in the next chapter.

The 2015 work fabricating an optimized 3.38% efficient organic solar cell with a 4 nm thick ALD NiO layer also fabricated control devices using the most common HTL in OPV: PEDOT:PSS. The PEDOT:PSS control cell performed slightly better than the optimized NiO cell with an efficiency of 3.49%. This exemplifies the fact that PEDOT:PSS remains the go to HTL layer for conventional (non-inverted) OPV cells. The following section will address the characteristics of PEDOT:PSS which make it such an effective HTL layer for OPV systems.

**PEDOT:PSS:** The high work function of poly(3,4-ethylenedioxythiophene) polystyrene sulfonate (PEDOT:PSS or PEDOT) provides a good match to the highest occupied molecular orbital (HOMO) of typical donor polymers (e.g. P3HT) in organic solar cells [55]. The HOMO level can be thought of as an analog to the valence band energy level (E_v) for inorganic systems. This match allows PEDOT to selectively transport holes from the P3HT donor to the ITO anode.
The hydrophilic nature of PEDOT resulting from this material being water based causes problematic wetting issues when coating PEDOT on the hydrophobic organic absorber materials in the inverted OPV configuration. For this reason, PEDOT is most commonly coated on the ITO layer, and then the active layer is coated on the PEDOT once it has been dehydrated through a thermal annealing step, that is, the superstrate configuration is more favorable to PEDOT. Work has been done in which surfactants decreasing the hydrophilic nature of PEDOT such as Triton X-100 [78] can be used to increase the wetting of PEDOT on organic materials by reducing the hydrophilic nature of PEDOT. This is critical for the fabrication of inverted organic solar cells since better wetting properties are found to cause a more uniform and complete layer of PEDOT. The complete coverage of PEDOT increases the shunt resistance \( R_{\text{SH}} \) between the active layer and the ITO contact and thereby reduces charge recombination at the ITO contact [79]. At the same time the complete coverage of PEDOT decreases the series resistance \( R_S \) and enhances \( J_{\text{SC}} \) as a result of better charge extraction properties. If the PEDOT were discontinuous due to poor wetting the direct contact between the electron transport material of the active layer (i.e. PCBM) and the hole collecting ITO contact would lead to a decrease in \( R_{\text{SH}} \) and cause higher leakage currents which would decrease device stability. In short, uniform PEDOT layers help the stability of organic photovoltaic devices by minimizing shunt currents. On this end, in 2008 the author of this thesis did work supporting the idea that uniform PEDOT layers do indeed improve the stability of organic photovoltaic devices relative to PEDOT layers which do not completely cover the ITO electrode. Figure 24 shows the performance over time for conventional BHJ solar cells based on planar PEDOT (maroon squares), PEDOT nano-columns (green triangles), and no HTL controls (blue circles) which did not use a PEDOT layer. The PEDOT nano-columns were \(~170\) nm in height separated by several hundred nanometers.
time, the PEDOT nano-columns were intended to serve as a more optimum light scattering morphology and they were therefore expected to improve the device performance through \( J_{SC} \) enhancements. However, as shown in Figure 24, the incomplete coverage of the ITO resulting from the space between the PEDOT nano-columns caused a decreased stability of OPV devices as a result of the increased shunt current resulting from the direct contact between the ITO and the PCBM component of the active layer. The extreme case of the ITO directly contacting the active layer is observed for the devices with no PEDOT. As shown, the uniform PEDOT layer provides better device stability than both the PEDOT nano-columns which only partially cover the ITO and the control devices with no PEDOT. The primary reduction in performance was caused by \( V_{OC} \) reductions for the no HTL devices and FF reductions for the PEDOT nano-column devices, \( J_{SC} \) remained relatively constant over time for all configurations. Both the initial and the stabilized \( J_{SC} \) values were the highest for the planar PEDOT devices consistent with the decreased series resistance associated with the complete coverage of the PEDOT on the ITO electrode.

![Efficiency Vs. Time](image)

**Figure 24:** Complete PEDOT coverage improves OPV device stability through increased shunt resistance between ITO and active layer
It should be noted a more conductive formulation of the typical PEDOT formulation [80] called PH500 [81] was used in this study. Our previous experimental work found the PH500 was twice as conductive as the typical PEDOT formulations with the PH500 having a resistivity of $\sim 2 \times 10^{-2} \, \Omega \text{cm}$ and the conventional PEDOT having a resistivity of $\sim 4 \times 10^{-2} \, \Omega \text{cm}$.

Although this thesis will focus on completely inorganic devices based on inorganic absorbers and inorganic HTL layers, a key issue limiting PEDOT in OPV devices is the same reason this material is not well suited for the inorganic absorber materials we will use. Namely, the hygroscopic and acidic nature of PEDOT is detrimental to the high work function metal electrode materials (e.g. Ag) used as the hole collecting contact. It has been found PEDOT corrodes Ag through first promoting grain boundary grooves and then leads to grain segregation which results in separated Ag particles upon Ag’s exposure to PEDOT [82]. Since Ag will be a metal electrode material of use in this thesis the potential use of PEDOT as an HTL in our devices is eliminated. This acidic nature of PEDOT has resulted in the search for additional inorganic metal oxide materials which would be suitable as a HTL layer for OPV devices such as NiO, MoO$_3$, WO$_3$, and V$_2$O$_5$. It is important to note hybrid approaches using an organic hole transport layer such as PEDOT with an inorganic Si absorber have been studied and found to have some success affording efficiencies up to $\sim 13\%$ [83]. An additional limitation with PEDOT coupled with an inorganic absorber like Si is that the nano-texturing of Si required for light trapping leads to difficulties with conformally spin coating the PEDOT. As previously discussed, and experimentally supported, breaks and discontinuities in the PEDOT lead to a declination in the device stability through a decreased shunt resistance. To circumvent this issue recent work in 2014 began to investigate the use of transition metal oxides conducive to more conformal deposition techniques such as MoO$_3$ in conjunction with inorganic Si absorbers [84].
**MoO₃**: Despite the common use of the transition metal oxides with organic solar cells these metal oxides have surprisingly been very little investigated in conjunction with inorganic absorbers. Work in 2014 was the first reported time in which a transition metal oxide was used in conjunction with an n-type Si absorber. Here, a thin ~15 nm layer of MoO₃ served as a hole selective contact to an n-type Si absorber giving a 14.3% efficient single junction n-Si solar cell. This outperforms the 13% mark set by the best PEDOT/Si hybrid devices [84]. The effectiveness of MoO₃ as a hole selective contact stems from this material’s very high work function of 6.6 eV, which is significantly higher than any elemental metal. The relevance of this effective MoO₃ hole contact is that the typically p-type doped Si hole contact is no longer necessary and therefore a simple single junction n-Si device with an MoO₃ hole contact can be achieved with a competitively high efficiency.

As a result of its high work function, MoO₃ has also found success as an HTL with organic solar cells [85]. Once again, the precise thickness of the MoO₃ has a large impact on device performance: MoO₃ films less than ~5 nm in thickness lead to devices with reduced V_{OC} and FF values resulting from decreases to the shunt resistance. An optimum thickness of ~10 nm was required for this material to most effectively serve as a performance enhancing HTL [86]. The post deposition annealing process which has been found to be helpful for improving the transport properties of other metal oxides (*e.g.* ZnO) has a detrimental effect on MoO₃ based configurations. The adhesion of the commonly employed Ag hole contact to MoO₃ is rapidly deteriorated upon heat treatment, which forms an unfavorable Ag-MoO₃ alloy and rapidly reduces device performance [87]. Therefore, care has to be taken to avoid any high temperature steps following the deposition of the MoO₃.
**WO₃**: Another transition metal oxide which has been investigated in conjunction with Ag as a HTL is WO₃. Once again, WO₃ is selected on behalf of its relatively high work function of ~4.8 eV [88]. The same tradeoffs between thickness of the WO₃ and performance are once again observed: layers too thin give a decreased shunt resistance due to discontinuous films while layers too thick lead to the bulk insulating properties of the HTL taking over and increasing the series resistance. In the case of WO₃ an optimum thickness of ~5 nm was found, which is thinner than the optimum thickness of ~10 nm required for MoOₓ. Organic devices fabricated in parallel with optimum 5 nm thick WO₃ were found to slightly outperform devices with optimum 10 nm thick MoOₓ [89]. This is said to be the result of the smoother surface morphology and higher electrical conductivity of WO₃ compared to MoOₓ. In addition, for organic solar cells the band alignment of the conduction band of WO₃ to the P3HT lowest unoccupied molecular orbital (LUMO) gives a larger energy barrier, and therefore WO₃ serves as a more effective electron blocking layer than MoOₓ. At the same time, the valence band level of WO₃ is a better match to the P3HT highest occupied molecular orbital (HOMO) level than that of MoOₓ, resulting in WO₃ also being a more efficient hole transporter. In all, WO₃ seems to have great promise as a HTL in organic solar cells. In fact, work has been done showing WO₃ can perform as well as PEDOT as an HTL in organic solar cells when using a WO₃ nanoparticle solution. This is valuable since the solution processed WO₃ is also conducive to flexible applications [90].

**V₂O₅**: The ability to cast V₂O₅ from solution allows this material to also be conducive to mass manufacturing techniques. Roll to roll processed inverted organic solar cells based on V₂O₅ have been investigated [91]. The concentration of the V₂O₅ solution was found to have a large impact on the effectiveness of V₂O₅ as an HTL even when the spin speeds were adjusted to obtain a similar thickness. High concentrations of V₂O₅ sol gel solution (1:70) lead to degraded
performance while lower concentrations of V$_2$O$_5$ sol gel solution (1:150) lead to enhanced performance [92]. This is believed to be a result of the higher concentration leading to penetration of the sol gel solution into the active layer of the organic absorber material and damaging the P3HT chains. In all, V$_2$O$_5$ seems to offer some promise based on the material’s energetic alignment; however, its high toxicity may limit its overall validity as an HTL [55].

**HT/EBL summary:** The materials MoO$_3$ and VO$_3$ are said to offer the most promise for OPV devices as a result of their good electrical and optical properties coupled with their favorable band alignment to the electron donor material (i.e. P3HT) used in organic photovoltaic devices [55]. Although no single material can be definitively considered the absolute best HT/EBL material it seems as though WO$_3$ is perhaps the most promising material as a HTL for organic solar cells based on its superior performance relative to MoO$_3$ coupled with its ability to be processed from solution for high throughput applications. Although PEDOT has given some of the best results at the research level for organic devices its acidic nature leading to reactions with metal electrode materials ultimately limits its viability. The complete coverage of PEDOT over the ITO electrode is necessary for maximizing OPV device stability. Although V$_2$O$_5$ has good band alignment with organic solar cell materials its high toxicity may make it difficult to employ for practical applications. Both MoO$_3$ and NiO have found use with the inorganic absorber materials n-Si and CdTe respectively. At this point the motivation of this thesis to use light trapping structures and transport layer materials for enhancing solar cell performance has been established. The following chapter will discuss in detail our experimental work pertaining to the fabrication and characterization of the transport layer material nickel oxide.
Chapter 3: Nickel Oxide Transport Layers

3.1 Nickel Oxide

Nickel oxide (NiO) is a model p-type semiconductor with a band-gap energy ranging from 3.6 [93] to 4 eV [94]. This material can take on an assortment of structures and properties depending on its fabrication method. Thin films of NiO have been fabricated using a variety of techniques including chemical vapor deposition (CVD) [95], electrochemical deposition [96], sol gel [72], pulsed laser deposition [97], sputtering [98, 99], spray pyrolysis [100], chemical solution deposition [74, 101], atomic layer deposition (ALD) [71, 102-106], and thermal [107] or e-beam evaporation of metallic Ni combined with a thermal anneal (EBE+A) [108]. In this thesis work a comparison of the structures and properties between NiO films fabricated with the latter two methods (ALD and EBE+A) was conducted.

In addition to the promise of NiO as a transport layer, which is the focus here, there are a plethora of additional applications employing NiO thin films. Therefore, it is hoped that the fabrication conditions and the subsequent characterization results presented in this chapter could be of use to other research areas utilizing NiO such as chemical sensors [109], electronic displays [110], smart windows [111], catalysts [112], and switching RAM devices [113]. This large range of applications requires NiO thin films which are deposited with varying degrees of surface coverage, thickness precision, crystallinity, and throughput. As a result, understanding the relationships between the fabrication conditions and their consequent influences on material properties such as surface roughness, optical transparency, grain size, crystallinity, and electrical conductivity is critical for multilayer device construction. For instance, many solar cell fabrication schemes require high temperature steps following the deposition of the HTL; thus,
investigation of the post deposition annealing effects on the material properties of an HTL such
as NiO is important for device construction.

In Chapter 2 a trend between the thickness of the HTL (or ETL) and its success as a transport layer was established. As mentioned, recent work has shown the nanometer scale thickness precision and high surface coverage of NiO are critical parameters for optimizing the efficiency of organic solar cells [71]. To meet such requirements on thickness precision and conformal coverage ALD is the only suitable deposition technique. Precise sub nanometer thickness control is very difficult with CVD due to the gas residence time in the chamber while shutter based PVD techniques, which can achieve more precise thicknesses, will lead to coatings which are not fully conformal. For these reasons, the ALD of NiO will be one of the two fabrication methods of focus in this chapter. Since this chapter is also intended to provide broader insight onto the material NiO in general a second fabrication method for applications requiring thicker films of NiO in excess of ~100 nm will also be investigated since thick films are not realistically suited for a slow process such as ALD. In such cases, the electron beam evaporation of metallic nickel followed by a thermal annealing treatment in air (hereafter abbreviated as EBE+A) is an extremely simple and high throughput fabrication method of NiO.

A careful contrasting of the properties and structures of NiO thin films fabricated with high precision (ALD) and high throughput (EBE+A) fabrication techniques in a well controlled side-by-side experiment has yet to be conducted until this thesis work. The following sections will detail each of these fabrication methods and the resultant film properties. At the end of this chapter the results for an inorganic CdTe solar cell utilizing NiO as a transport layer will be presented. This is the first time to our knowledge an inorganic solar cell has successfully employed NiO as a transport layer.
3.2 Nickel Oxide Fabrication & Characterization Methods

**Atomic layer deposition:** The atomic layer deposition of NiO was done with a Savannah 200 ALD system (Cambridge Nanotech). The growth precursors were water and a novel nickel amidinate precursor, nickel bis (N,N’-di-tert-butyacetamidinate) (Ni(amd)) provided by Dow Chemical. Again, this is only the 2nd time to our knowledge this precursor has ever been used to grow NiO with the ALD [71]. The ALD growth was done at 200°C with the precursor preheated to 125°C. One ALD growth cycle consisted of alternating 0.015 s H₂O and 0.750 s Ni(amd) pulses which were followed by purge times of 15 s and 25 s respectively. The process pressure was ~0.6T and 20 sccm of N₂ was flowing through the chamber throughout the process. Growth was conducted on cleaned glass substrates and Si wafers using varying numbers of cycles to establish the growth per cycle (GPC). The number of cycles necessary to achieve 30 nm of NiO was then used for the follow up post deposition annealing and characterization studies.

**Electron beam evaporation + annealing:** To form NiO with the EBE+A method metallic nickel was blanket deposited onto cleaned glass substrates using a Semicore electron beam evaporation system pumped down to a base pressure of 2x10⁻⁶T. The thickness of the metallic nickel was chosen such that following the post deposition annealing treatment the resultant NiO thickness would be a close match to the 30 nm of NiO obtained with the ALD method.

**Post deposition annealing:** Films deposited onto glass substrates with both ALD and EBE were placed side by side on a hotplate at various temperatures in air. Films were simultaneously annealed for 20 minutes at probed temperatures of 295°C, 330°C, 385°C, and 435°C. All films were slowly cooled on the hotplate to prevent thermal shock to the glass substrates.

**Characterization:** Crystallinity was studied using grazing incidence x-ray diffraction (PAnalytical XpertPro MPD) with λ=1.54059 Å radiation with a scan range of 20-80° 2θ. Films
were indexed using Jade software. The surface topography and roughness were observed with atomic force microscopy in PeakForce tapping mode (Veeco Icon). The transmittance was measured with a UV-Vis-NIR spectrophotometer (PE Lambda 950) over a wavelength range of 300-1,300 nm. The thickness of the ALD NiO deposited onto a Si wafer was measured using an ellipsometer (Nanospec 8000) and was confirmed with FESEM (Zeiss Merlin) cross sectional measurements. All film thicknesses were also verified with a profilometer (Dektak 6M).

Electrical properties were assessed with a patterned bar method and IV measurements (Agilent 4156 power supply) using a voltage sweep range of -1 to 1 V with varying contact spacings.

3.3 Characteristics of ALD grown NiO

The growth per cycle (GPC) of the ALD grown NiO is shown in Figure 25. The GPC ranged from 0.20-0.45 Å/cycle which is in agreement with the 200°C rate of 0.43 Å/cycle reported by the manufacturers (Dow Chemical) of this precursor. This GPC is also in agreement with the rate of 0.39 Å/cycle found by the only other work using this precursor for NiO growth [71]. The minor deviations from linearity in the GPC are most likely a result of an evolving density of surface adsorption sites during growth [114]. As the morphology develops during the early stages of growth, so too will the availability of precursor adsorption sites. This in turn will cause chemisorption coverage to saturate at differing levels of precursor adsorption as growth commences, and thereby small deviations in the GPC are to be expected. It should be noted that the observed growth rate of 0.20-0.45 Å/cycle is appreciably less than the sizes of the Ni$^{2+}$ (0.70 Å) and O$^{2-}$ ions (0.140 Å) that construct the ALD grown NiO [115, 116]. It follows that this GPC will be significantly less than the thickness of a monolayer of the ALD grown material. This type of sub-monolayer growth is common in ALD, and in fact, the growth of a full monolayer for a single ALD cycle is quite rare. More commonly, due to intermediate reactions
occurring during ligand exchanges throughout the ALD process, a single ALD cycle will often give only 10-30% of a monolayer per cycle [114]. Here, as a first estimation, when comparing the value of one third of the 4.17 Å lattice parameter of NiO (due to NiO having 3 layers of atoms in the unit cell of the cubic rock salt structure with a=4.17 Å) to the upper limit of our experimentally observed growth rate of 0.45 Å/cycle, a cycle growth of ((0.45 Å/cycle)/((4.17 Å)/3)*100≈32% of a monolayer occurs. This means that roughly 3 ALD cycles are required to grow a monolayer of the ALD grown NiO. This notion is further supported by the fact the linear trend line in Figure 25 does not intercept the origin. As seen by the trend line an incubation period of ~60 cycles was required prior to growth. This same delayed growth behavior was observed by others growing ALD NiO with a different Ni(tmd)₂ precursor in a completely different geometry reactor [104].

![Figure 25](image)

**Figure 25:** Thickness variation of ALD grown NiO on a Si wafer at 200°C as a function of the # of ALD cycles using the precursors Ni(amd) and water

The concept of a monolayer in ALD can be viewed as the theoretical maximum for the GPC. This maximum is a useful measure when attempting to model ALD growth modes [117].
However, in ALD, interpreting the term “monolayer” can be very tricky. This is because the term “monolayer” can correspond to a layer of chemisorbed material on the substrate, a layer of physisorbed material on the substrate, or, a layer of ALD grown material on the substrate which will remain in the final thin film. To clarify the discussion in this section, we are referring to a monolayer as a layer of ALD grown material on the substrate that will remain in the final thin film following deposition \(i.e.\) no C or H. These effects are shown in Figure 26 [114].

![Figure 26: In ALD, there are three different types of monolayers: chemisorbed monolayers (the substrate before and after chemisorptions is shown) (a), physisorbed monolayers (b), and a monolayer of the ALD grown material (c) [114]](image)

This thesis’s work with the Ni(amd) precursor in 2014 was one of the first times this precursor had ever been used to grow NiO. To our knowledge the only other reported work using this precursor was not published until 2015. The significance of this is that we had to verify the novel Ni(amd) precursor provided by Dow Chemical was indeed depositing NiO based on our choice ALD processing conditions \(i.e.\) pulse time, purge time, chamber temperature, precursor temperature, etc.) for the reactor geometry we were working with. In most cases, an ALD process will grow a film regardless of whether or not it is the film intended; if the ALD process parameters are not optimized for a given set of precursors and reactor geometry the CVD of a highly contaminated and low quality material may result. Such unintentionally grown CVD
films do not possess the key attributes of true ALD films: self-limiting growth leading to high step coverage, minimal defects, and high thickness precision.

The most straightforward way to optimize the growth conditions for an ALD process (i.e. precursor pulse and purge times) with a new precursor is through the use of a quartz crystal microbalance (QCM). Use of a QCM allows one to plot the mass deposited as a function of precursor dose (i.e. precursor pulse time). Here, when optimizing a new ALD process one should observe the mass deposited for various pulse times. When the mass deposited begins to saturate in excess of a certain pulse time, this corresponds to the dose required for that particular precursor to completely cover the surface of the reactor at a given temperature [118].

This precursor pulse time, coupled with the optimized purge time to allow full removal of any unreacted precursor, can then be used to obtain the saturating and irreversible growth behavior which is characteristic of ALD. This same process optimization is required for both growth precursors. Once optimized, the pulse and purge time for each of the ALD precursors are programmed into the deposition recipe and these steps are simply repeated any number of times necessary to grow the thickness of film desired. Since the ALD system used in this thesis was not configured with a QCM it was necessary to validate in other ways that the pulse and purge times we were using to grow NiO with the new Ni(amd) precursor were leading to true ALD growth and not CVD. This was done by exhaustively characterizing the grown NiO films with various methods in order to verify the characteristics of true ALD behavior were occurring.

One key characteristic of true ALD behavior is the conformal nature of the film. To assess this, the surface morphology of the ALD grown NiO was also analyzed using atomic force microscopy (AFM). Self-limiting growth is evidenced by extremely conformal films mimicking the morphology of the underlying substrate. Figure 27 confirms the conformal nature of the NiO
grown in this thesis work. Here, the root mean square (RMS) surface roughness of the glass substrate was 0.999 nm while the RMS roughness for 30 nm of ALD grown NiO onto this glass substrate was 1.70 nm. An increase of less than 1 nm in RMS roughness for a film 30 nm in thickness suggests the ALD grown material is highly conformal to the glass substrate as the majority of the 1.70 nm RMS roughness comes from the underlying substrate itself.

![Figure 27: Surface morphology of glass substrate (left) compared to 30 nm of ALD grown NiO on glass (right) illustrating the conformal nature of the ALD NiO](image)

Since these NiO films are of interest to us as transport layers in solar cells we were also interested in the influence of a post deposition heat treatment on the film properties since these films may be subjected to high temperature steps following their growth. On this end, Figure 28 shows the influence of varying the post deposition annealing temperature on the surface morphology of the ALD grown NiO. Here, it is shown that the post deposition annealing temperature has a cyclic effect on the surface morphology in which the lowest and highest post deposition annealing temperatures of 295°C and 435°C roughened the surface while the intermediate temperatures of 330°C (not shown) and 385°C led to surface smoothening. The lowest annealing temperature increased the surface roughness with respect to the as deposited
NiO by 7% which is believed to be a result of grain growth perpendicular to the substrate. Higher annealing temperatures of 330°C and 385°C provide additional energy for grain growth and smoothened the film by promoting lateral grain growth, allowing the vertical grains induced at 295°C to coalesce. This effect is maximized at 385°C where the smoothest film is observed. For this condition, the RMS roughness is only 0.35 nm larger than the glass substrate, indicating an extremely smooth coating with this heat treatment. A further increase of temperature to 435°C increases the surface mobility of the atoms, and this increased diffusion at the surface leads to the secondary nucleation which drastically increasing the roughness. It should be noted that these are only rough speculations on the surface mechanisms occurring during annealing; a larger sample size of RMS roughness measurements should be conducted to develop a more complete model of the surface mechanisms occurring as a result of heat the treatment.

Figure 28: 3D rendered AFM images of the ALD NiO as a function of post deposition annealing temperature. The RMS roughness of each film is shown at the lower right of each image.
The extremely conformal nature of the NiO films shown in Figure 27 and the linear thickness versus cycles trend both support the fact our ALD recipe (i.e. choice of precursor pulse and purge times) was indeed leading to true ALD growth behavior. Interestingly, the only other work using the Ni(amd) precursor and H₂O to grow NiO suggested a low volatility and low surface reactivity of this precursor were responsible for the long pulse (6 s) and purge (60 s) times they found were required to obtain surface saturating ALD growth characteristics. However, we found good ALD growth characteristics using much shorter pulse (0.75 s) and purge (25 s) times for the same Ni(amd) precursor at the same ALD growth temperature of 200°C, the same precursor temperature of 125°C, the same N₂ carrier gas flow rate of 20 sccm, in a similar geometry Savannah ALD reactor at the same pressure of ~0.1’s of T. It has been previously reported that the Ni(amd) precursor has a sufficiently high vapor pressure of >1T at 90°C, which is just a few degrees higher than Ni(amd)’s melting point of 87°C [119]. The vapor pressure curve for Ni(amd) shows that at the precursor heater temperature of 125°C the vapor pressure is >8T [119], so we do not believe precursor volatility should be a limiting factor causing long exposure times. Therefore, the most likely causes for differences in pulse and purge times are variations in the reactor geometries and different substrate types leading to differences in early stage precursor interaction with the substrate.

Since many of the applications of NiO rely on this material’s optical transparency, including solar cells, we also investigated the transparency of the ALD NiO as a function of thickness and post deposition heat treatment. The optical data suggests the as deposited films contain a large portion of metallic Ni, as evidenced by a gray hue on the samples upon removal from the ALD. A post deposition annealing treatment in air improves the transmittance of these films by oxidizing the metallic Ni to NiO within minutes of placing the sample on the hotplate.
Such improvements in NiO transmittance with higher temperature processing are common and have been observed by others using various deposition techniques [72, 120]. The transparency of the ALD grown NiO as a function of thickness and post deposition annealing treatment are shown in Figure 29.

![Graph showing UV Vis spectra of ALD NiO](image)

**Figure 29:** UV Vis spectra of the ALD NiO as a function of NiO thickness. The improved transmittance upon the oxidation of metallic Ni to NiO upon annealing is also shown.

The deposition characteristics, surface morphology, and transmittance were also assessed for NiO films fabricated with the EBE+A method and will be discussed in the following section.

### 3.4 Characteristics of thermally oxidized Ni

Key characteristics of the NiO fabricated by thermally annealing metallic Ni are shown in Figure 30. Here, a 25 nm layer of blanket deposited Ni metal was patterned into a bar structure using conventional photolithography and a 6 minute immersion in a Nickel TFB etchant [121].
As a result of annealing this patterned 25 nm Ni layer at 435°C for 20 minutes the following changes were immediately observed: (1) the thickness increases by almost 300% from 25 nm to 70 nm, (2) the resistivity increases by close to seven orders of magnitude from $2.86 \times 10^{-5} \, \Omega \, \text{cm}$ to $2.40 \times 10^{2} \, \Omega \, \text{cm}$ and (3) the transparency in the visible range increases from less than 10% to greater than 70%. These are all clear signs that the Ni metal has been oxidized to NiO.

![Ni as deposited vs. Ni after 435°C 20 min in air](image)

<table>
<thead>
<tr>
<th>Ni as deposited</th>
<th>Ni after 435°C 20 min in air</th>
</tr>
</thead>
<tbody>
<tr>
<td>Thickness: 25 nm</td>
<td>Thickness: 70 nm</td>
</tr>
<tr>
<td>$\rho_{Ni} = 2.86 \times 10^{-5} , \Omega , \text{cm}$</td>
<td>$\rho_{NiO} = 2.40 \times 10^{2} , \Omega , \text{cm}$</td>
</tr>
<tr>
<td>$%T$ (visible) &lt; 10%</td>
<td>$%T$ (visible) &gt; 70%</td>
</tr>
</tbody>
</table>

**Figure 30:** Ni metal as deposited and patterned (left) This same Ni following a 435°C 20 minute anneal in air (right). The thickness, resistivity, and visible transmittance are shown for each.

Figure 31 shows that the surface morphology of the NiO fabricated with the EBE+A method is drastically rougher than that of the ALD grown NiO, which is to be expected since ALD is an extremely conformal deposition technique. Although it has been shown by others temperatures as low as 200°C can oxidize metallic Ni to amorphous NiO that process took a much longer time and the resultant NiO films were amorphous [108]. For this study we found temperatures of at least 330°C were required to significantly oxidize metallic Ni to NiO; the higher required temperature to induce this change is likely the result of the lower thermal
conductivity of the relatively thick glass substrates our Ni metal was deposited on. The lowest annealing temperature of 295°C does not permit enough oxygen to enter the film for oxidation during the 20 minute time used, and therefore these films were still dominantly metallic Ni. Evidence of oxidation was first observed visually as the opaque Ni metal turned translucent within minutes of placing on the hotplate at temperatures in excess of 330°C.

![AFM images](image)

**Figure 31:** 3D rendered AFM images of EBE+A NiO as a function of post deposition annealing temperature. The RMS roughness of each film is shown at the lower right of each image.

For the EBE+A films, a general trend between surface roughness and transmittance is again observed and once again the annealing temperature of 385°C provides the highest transmittance. Here, it is clear the NiO is only partially oxidized at 330°C as seen by the poor transmittance of films annealed at this temperature as shown in Figure 32.
In order to directly compare the properties of the ALD NiO to the EBE+A NiO a similar film thickness for each fabrication method is necessary. Based on additional experiments also showing a roughly 275-300% thickness increase results by thermally annealing Ni to NiO we chose to deposit 11 nm of Ni with the aim to oxidize this 11 nm Ni film to ~30 nm of NiO. The following section will compare the properties of 30 nm of NiO grown directly with ALD and 30 nm of NiO grown by oxidizing 11 nm of Ni to ~30 nm of NiO with the EBE+A method.

![UV Vis spectra of the EBE+A NiO as a function of the post deposition annealing temperature](image)

**Figure 32:** UV Vis spectra of the EBE+A NiO as a function of the post deposition annealing temperature

3.5 A comparison between ALD grown NiO and thermally oxidized Ni

Gaining insight on the similarities and differences between NiO grown with the ALD and EBE+A method is valuable for multiple reasons: (1) AFM morphology analysis helps further verify evidence of true ALD behavior by contrasting surface roughness’s for the same material.
with the same thickness, (2) UV-Vis provides contrasts between the transmittance of films which can be related and supported by the AFM morphology, and (3) GIXRD structural data provides insight onto film orientation and crystallinity differences for films grown with different methods. The influence of post deposition annealing treatment on crystallinity can be further investigated by comparing the electrical conductivity of the materials as a function of heat treatment.

As expected, Figure 33 shows the EBE+A NiO was rougher than the ALD NiO subjected to the same post deposition heat treatment. Both of these films were annealed at 435°C, which was the temperature shown to induce the roughest surface for both fabrication methods. The RMS roughness of 2.42 nm for the ALD NiO was appreciably less than the 3.65 nm value for the EBE+A NiO of the same thickness. Again, these results are consistent with good surface coverage and uniformity being achieved for the ALD grown NiO.

Interestingly, Figure 34 shows the NiO deposited with the EBE+A method had a slightly higher transparency than the ALD NiO (both annealed at 435°C). Although this is not consistent with the roughness data, this was believed to be a result of the 30 nm ALD NiO film (which thickness had been confirmed with both ellipsometry and cross sectional FESEM) being slightly thicker than the EBE+A film. Follow up studies patterned the EBE+A film and sure enough measured a true thickness of 27 nm, which supports the slightly higher transparency of this material relative to the 30 nm of ALD grown NiO.
Figure 33: AFM images comparing EBE+A NiO (left) to ALD grown NiO (right). Both films were annealed for 20 minutes at 435°C in air.

Figure 34: Comparison of the transmittance between ALD NiO and EBE+A NiO
In addition to contrasting the surface properties between ALD and EBE+A NiO the bulk properties and crystallinity of the NiO grown with each method are also of interest. Here, grazing incidence x-ray diffraction was used to study the influence of both (1) the deposition method and (2) the post deposition annealing temperature for these NiO films. The results of this analysis are shown in Figure 35.

The GIXRD data shows that the thermal oxidation of ~11 nm metallic Ni to ~27 nm of NiO requires temperatures in excess of 330°C when annealing in air for 20 minutes as evidenced by the peak shifts from metallic Ni to NiO upon annealing at temperatures of 330°C and above. The ALD NiO films are polycrystalline as deposited with the typical cubic rock salt structure of NiO with diffraction peaks corresponding to the (111), (200), (220), and (311) planes. Refinement methods showed the lattice parameter of the ALD NiO decreased from 4.20 Å (as deposited) to 4.17 Å following the 435°C post deposition annealing treatment. This is expected to be a result of the enhanced crystallization compacting the lattice towards the most energetically favorable crystal structure with the bulk lattice parameter of ~4.1759 Å [122].
Figure 35: GIXRD data for NiO films deposited with ALD (top) and EBE+A (bottom) as a function of post deposition annealing temperature

Once again, since care was taken to ensure the NiO films were roughly the same thickness for both the ALD and EBE+A methods a contrasting of the sharpness of the GIXRD peaks can provide information about the relative crystallinity of the films. Here, the sharper peaks for the ALD NiO indicate a higher degree of crystallinity for this film than the EBE+A grown NiO. In agreement with this observation a higher electrical conductivity ($\sigma$) of $6.5 \times 10^{-3}$ ($\Omega \text{ cm})^{-1}$ was measured for the ALD NiO than the EBE+A NiO when both films were subjected to the same 435°C heat treatment. The conductivity was obtained in accordance to equations 3.1
and 3.2 using a patterned bar method corresponding to the geometry of the films shown in Figure 30. In equation 3.1 \( \rho \) is the electrical resistivity, \( R \) is the resistance measured with a digital multimeter when placing the probes at either end of the patterned bar, \( A \) is the cross sectional area of the bar which is obtained by multiplying the bar width, \( w \) (0.3 cm), by the film thickness, \( t \) (~30 nm), and \( l \) is the length of the bar (1.05 cm). The as deposited ALD NiO and all of the EBE+A NiO films had conductivities too low to measure with this method.

\[
\rho = R \frac{A}{l} = R \frac{w \times t}{l} \quad [3.1]
\]

\[
\sigma = \frac{1}{\rho} \quad [3.2]
\]

This conductivity increase of the ALD grown NiO upon annealing is believed to be a result of the thermally activated hopping mechanism shown in equation 3.3. Here, baking the NiO puts \( Ni^{2+} \), \( Ni^{3+} \), and \( V''_{Ni} \) on the cation sites. The low required energy of tenths of an eV for the interaction shown in equation 3.3 has the manifestation of an increased room temperature conductivity for the NiO films following their post deposition annealing treatment. A simple experiment to support the validity of this mechanism was also conducted in which a continuously decreasing resistance was probed with the multimeter as the sample sat on a hotplate and the temperature was continuously increased.

\[
Ni^{2+} + h^+ \overset{10\text{ths of eV}}{\leftrightarrow} Ni^{3+} \quad [3.3]
\]

To further verify the conductivity increase of the ALD NiO following the post deposition annealing current voltage measurements were performed on both the as deposited ALD NiO and the 435°C annealed ALD NiO. Here, 200 nm thick Al contacts with various spacings were deposited onto the patterned NiO bar structures through a shadow mask using EBE. In agreement with the more crudely measured multimeter resistivities this method also showed the
annealing consistently reduced the resistance (obtained from the IV slope data) while varying the distance between the electrical contacts as shown in Figure 36.

**Figure 36:** Electrical characteristics of ALD as deposited (squares) and following the 20 minute anneal at 435°C (triangles) showing a decrease in R upon annealing for varying contact spacings

In this comparison, we also used the optical data to estimate the band gap \( (E_G) \) energies for all films through \((\alpha h \nu)^2 \) vs. \( h \nu \) plots based on the relation shown in equation 3.4 where \( \alpha \) is the absorption, \( h \) is Plank’s constant, \( \nu \) is the frequency, and \( C_1 \) is a proportionality constant. This method has been commonly employed elsewhere as well for obtaining the band gap of NiO [72, 123]. Here, we found a band gap ~3.5-3.55 eV for all NiO films.

\[
\alpha h \nu = C_1 \sqrt{(h \nu - E_G)} \quad [3.4]
\]

The influence of the post deposition annealing temperature on the NiO grain size was also investigated by coupling the GIXRD data with the Scherer’s method by utilizing equation 3.5 where \( d \) is the average grain size, \( \lambda \) is the x-ray wavelength, \( \beta \) is the full width half max of
the diffraction peak in radians, and θ is the diffraction angle this peak is centered on in radians.

\[ d = \frac{0.9\lambda}{\beta \cos \theta} \]  \[ [3.5] \]

As expected, higher annealing temperatures afforded larger NiO grain sizes with average grain sizes increasing from 19.2 nm for the as deposited ALD NiO to 24.1 nm for the 435°C annealed NiO, which is on the order of the 30 nm film thickness. The same trend was also observed by others for NiO films fabricated with the sol-gel technique [72]. For the EBE+A method, we observe slightly larger, but similar, grain sizes on the order of 25-27 nm. The similar grain sizes between the ALD and EBE+A methods for films annealed at 435°C are consistent with the optical spectra and diffraction patterns in each case, indicating many of the properties of NiO fabricated with ALD and EBE+A methods can be similar following an annealing treatment. Table 5 summarizes much of the key experimental data discussed throughout this chapter for all films characterized in this study.

<table>
<thead>
<tr>
<th>Method</th>
<th>Annealing Temperature</th>
<th>RMS Roughness</th>
<th>Average Grain Size</th>
<th>Band Gap</th>
<th>Average %T (400-1300 nm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>ALD</td>
<td>---</td>
<td>1.7</td>
<td>19.2</td>
<td>3.55</td>
<td>80.6</td>
</tr>
<tr>
<td>ALD</td>
<td>295</td>
<td>1.82</td>
<td>23.2</td>
<td>3.52</td>
<td>79.1</td>
</tr>
<tr>
<td>ALD</td>
<td>330</td>
<td>1.75</td>
<td>22.4</td>
<td>3.51</td>
<td>80.3</td>
</tr>
<tr>
<td>ALD</td>
<td>385</td>
<td>1.35</td>
<td>18.7</td>
<td>3.5</td>
<td>82.1</td>
</tr>
<tr>
<td>ALD</td>
<td>435</td>
<td>2.42</td>
<td>24.1</td>
<td>3.48</td>
<td>79.9</td>
</tr>
<tr>
<td>EBE+A*</td>
<td>---</td>
<td>1.87</td>
<td>---</td>
<td>---</td>
<td>27.0</td>
</tr>
<tr>
<td>EBE+A*</td>
<td>295</td>
<td>1.55</td>
<td>---</td>
<td>---</td>
<td>51.7</td>
</tr>
<tr>
<td>EBE+A</td>
<td>330</td>
<td>3.23</td>
<td>17.7</td>
<td>3.51</td>
<td>74.5</td>
</tr>
<tr>
<td>EBE+A</td>
<td>385</td>
<td>2.2</td>
<td>25</td>
<td>3.53</td>
<td>81.3</td>
</tr>
<tr>
<td>EBE+A</td>
<td>435</td>
<td>3.65</td>
<td>26.9</td>
<td>3.51</td>
<td>81.5</td>
</tr>
</tbody>
</table>

Table 5: Summary data of the NiO presented in Chapter 3 *these conditions correspond to films that were still metallic Ni.
For the broader range of applications utilizing NiO the relevance of all of the data and experimentation done in this chapter is that a simple hotplate approach can produce NiO thin films with transmittance levels and band gap energies similar to that of nickel oxide grown with atomic layer deposition. The surface morphology, crystallinity, optical, and electrical properties of NiO thin films can all be tailored by varying the post deposition annealing temperature. Regardless of the fabrication scheme, a post deposition annealing treatment of 385°C seems to be optimum for smoothening the NiO films and concurrently improving the transmittance. Insight on the interplay between the post deposition annealing, the deposition technique, and the material properties is vital for constructing multilayer devices incorporating NiO thin films.

For this thesis’s more specific aim to use NiO as an HTL the ALD fabrication method is imperative since (1) the exact HTL thickness has a large impact on cell performance, (2) highly conformal depositions are needed to obtain continuous films at the sub 10 nm thicknesses required for an ideal HTL, [124, 125], and (3) to obtain these sub 10 nm NiO films with the EBE+A method a starting Ni thickness less than a few nanometers would be required due to the ~300% thickness increase upon converting metallic Ni to NiO, however, this starting metal thickness is far smaller than the minimum thickness for a metal to be continuous. With this in mind, we sought to employ the ALD grown NiO as a HT/EBL in thin film CdTe solar cells based on the effective band alignment between these materials which was shown in Figure 23.

3.6 Thin film CdTe solar cells employing ALD NiO

Thin film CdTe solar cells employing ALD NiO were investigated. Cross sectional schematics of the device architectures used in this study are shown in Figure 37. Here, the three experimental variables investigated were the ALD NiO thickness (4 nm and 11 nm), the CdTe absorber thickness (0.5 μm and 2 μm), and the application of a 430°C post deposition annealing
treatment immediately following the ALD NiO growth. The device fabrication was a joint effort between Lucintech Inc. [126], a leader in thin film CdTe solar cell manufacturing, and Penn State University. The ALD of NiO and post deposition annealing steps were done at Penn State while all of the other processing steps and final device characterization were done by Lucintech.

<table>
<thead>
<tr>
<th>Control</th>
<th>NiO HTL</th>
</tr>
</thead>
<tbody>
<tr>
<td>Glass</td>
<td>Glass</td>
</tr>
<tr>
<td>TCO</td>
<td>TCO</td>
</tr>
<tr>
<td>0.5 μm CdTe</td>
<td>0.5 μm CdTe</td>
</tr>
<tr>
<td>50 nm CdS</td>
<td>0.6 nm Cu</td>
</tr>
<tr>
<td>20 nm Au</td>
<td>ALD NiO</td>
</tr>
</tbody>
</table>

**Figure 37:** Cross sectional schematics of control CdTe device (left) and CdTe device with a NiO transport layer (right)

For the construction of these cells Lucintech Inc. sent four plates fabricated in the superstrate configuration up through the deposition and CdCl₂ activation of and the CdTe layer to Penn State. Two of these plates had 2 μm thick CdTe while the other two plates had 0.5 μm of CdTe. Each of these plates was cut in half in order to obtain 8 samples such that an experiment with 3 binary variables could be conducted \((2^3=8)\). These variables were the CdTe thickness (0.5 μm or 2 μm), the NiO thickness (target thicknesses of 5 nm and 20 nm), and the NiO post deposition annealing treatment (as deposited or 430°C for 10 minutes). Table 6 summarizes the conditions for the CdTe solar cells employing an ALD NiO transport layer.
Table 6: Summary of experimental conditions used for CdTe solar cells employing NiO transport layers

<table>
<thead>
<tr>
<th>ID</th>
<th>CdTe Thickness</th>
<th>Target NiO thickness</th>
<th>NiO Bake</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>2 μm</td>
<td>5 nm</td>
<td>No</td>
</tr>
<tr>
<td>2</td>
<td>2 μm</td>
<td>5 nm</td>
<td>Yes</td>
</tr>
<tr>
<td>3</td>
<td>2 μm</td>
<td>20 nm</td>
<td>No</td>
</tr>
<tr>
<td>4</td>
<td>2 μm</td>
<td>20 nm</td>
<td>Yes</td>
</tr>
<tr>
<td>5</td>
<td>0.5 μm</td>
<td>5 nm</td>
<td>No</td>
</tr>
<tr>
<td>6</td>
<td>0.5 μm</td>
<td>5 nm</td>
<td>Yes</td>
</tr>
<tr>
<td>7</td>
<td>0.5 μm</td>
<td>20 nm</td>
<td>No</td>
</tr>
<tr>
<td>8</td>
<td>0.5 μm</td>
<td>20 nm</td>
<td>Yes</td>
</tr>
</tbody>
</table>

The equation of the linear trend line corresponding to the GPC characteristics for the ALD NiO presented in Figures 25 is shown in Figure 38. This equation was used to choose the number of ALD cycles for this experiment in order to deposit target thicknesses of 5 nm and 20 nm of NiO. Here, 164 cycles were used to target 5 nm and 467 cycles were used to target 20 nm. As it turns out, both of the NiO film thicknesses ended up being thinner than intended with 164 cycles giving closer to 4 nm of NiO and 467 cycles giving closer to 11 nm of NiO. In both cases the thinner than expected films suggest the different CdTe growth surface for this ALD NiO further hinders growth by the precursors either (1) having to overcome a larger nucleation barrier than that present with the Si wafer which was used to produce the trend line shown in Figure 38 and/or (2) a lower density of precursor surface adsorption sites on CdTe than on Si.

Following each of the two ALD NiO depositions samples 2, 4, 6, and 8 as defined in Table 6 were baked on a hotplate in air for 10 minutes, the probed temperature of the hotplate was 430°C. At this point, the 8 samples were sent back to Lucintech Inc. where the devices were completed by evaporating 0.6 nm of Cu followed by 20 nm of Au through a shadow mask used to define various cell areas for each of these 8 conditions. The performance results for all 8 of
these conditions along with the corresponding 2 control conditions (i.e. 0.5 μm and 2 μm thick CdTe layer solar cells with no ALD NiO and no 430°C annealing) are all shown in Table 7.

Figure 38: Linear trend line used to estimate the number of cycles to grow 5 nm and 20 nm of ALD NiO

<table>
<thead>
<tr>
<th>Cell ID</th>
<th>CdTe Thickness</th>
<th>NiO Bake?</th>
<th>Count</th>
<th>Average Values Based on Count</th>
</tr>
</thead>
<tbody>
<tr>
<td>In text ID</td>
<td>Thickness</td>
<td></td>
<td></td>
<td>PCE</td>
</tr>
<tr>
<td>2k</td>
<td>2 μm</td>
<td>None</td>
<td>N/A</td>
<td>19</td>
</tr>
<tr>
<td>2k_4</td>
<td>2 μm</td>
<td>4 nm</td>
<td>No</td>
<td>63</td>
</tr>
<tr>
<td>2k_4a</td>
<td>2 μm</td>
<td>4 nm</td>
<td>Yes</td>
<td>51</td>
</tr>
<tr>
<td>2k_11</td>
<td>2 μm</td>
<td>11 nm</td>
<td>No</td>
<td>47</td>
</tr>
<tr>
<td>2k_11a</td>
<td>2 μm</td>
<td>11 nm</td>
<td>Yes</td>
<td>43</td>
</tr>
<tr>
<td>500</td>
<td>0.5 μm</td>
<td>None</td>
<td>N/A</td>
<td>31</td>
</tr>
<tr>
<td>500_4</td>
<td>0.5 μm</td>
<td>4 nm</td>
<td>No</td>
<td>28</td>
</tr>
<tr>
<td>500_4a</td>
<td>0.5 μm</td>
<td>4 nm</td>
<td>Yes</td>
<td>19</td>
</tr>
<tr>
<td>500_11</td>
<td>0.5 μm</td>
<td>11 nm</td>
<td>No</td>
<td>30</td>
</tr>
<tr>
<td>500_11a</td>
<td>0.5 μm</td>
<td>11 nm</td>
<td>Yes</td>
<td>17</td>
</tr>
</tbody>
</table>

Table 7: Summary of results for CdTe solar cells employing NiO transport layers
The key result of this experiment was that the ALD NiO was a successful transport layer for solar cells based on 0.5 µm thick CdTe absorbers in the event there was no annealing treatment following the ALD growth of the NiO. The influence of each of the three variables investigated in this experiment will now be analyzed and discussed.

**CdTe Thickness:** A comparison between the control samples 2k and 500 shows an almost exact doubling of the efficiency from 6.57% to 13.13% upon increasing the CdTe thickness from 0.5 µm to 2 µm. This is expected behavior since the required thickness of CdTe to absorb 99% of the photons with energies above its band gap is 2 µm [127]. The ALD NiO layer was severely detrimental for the thicker 2 µm layer CdTe absorbers while it was helpful for the thinner 0.5 µm layer CdTe cells in the event the devices were not annealed. Since the ALD NiO most drastically reduced the FF for the thicker 2 µm cells this suggests for this thickness of the CdTe the additional process steps used to grow the ALD NiO significantly deteriorated the internal transport characteristics in these cells. For the 2 µm cells a direct trend between increased thermal budget and decreased performance is observed: sample 2k_4 (shorter ALD growth time at 200°C and no thermal annealing) was the least negatively affected while sample 2k_11a (longer ALD growth time at 200°C and thermal annealing) was the most negatively affected.

The thinner CdTe cells were more positively influenced by the use of the ALD NiO transport layer. As long as the films were not subjected to the annealing treatment the ALD NiO layer improved the device performance, regardless of the NiO thickness, as a result of appreciably increasing both the FF and the $V_{OC}$. This indicates for the 0.5 µm thick CdTe absorber the internal transport properties are enhanced and the recombination is reduced. The slightly lower $J_{SC}$ for the cells employing the ALD grown NiO is expected since this ALD grown NiO will be a less efficient at reflecting unabsorbed photons back into the absorber than the bare
metal back contact. These results illustrate for the first time that NiO can be a successful transport layer in inorganic CdTe solar cells.

**ALD NiO Thickness:** A very telling trend can be observed by comparing all of the samples using 4 nm of ALD NiO (2k_4, 2k_4a, 500_4, 500_4a) to their 11 nm of ALD NiO counterparts (2k_11, 2k_11a, 500_11, 500_11a). That being, the 4 nm layer of NiO outperforms the corresponding configuration with 11 nm of NiO in every case. There are multiple explanations for this. The most convincing explanation is that which has already been discussed throughout the past two chapters: there is an optimum thickness for transport layers in solar cells and in most cases that optimum thickness is less than 10 nm. The optimum thickness is generally the thickness at which the transport layer first becomes continuous. As discussed, the other work using ALD NiO with nearly identical growth conditions found that 4 nm of ALD grown NiO was the sweet spot for optimizing performance for OPV devices where both thicker (8 nm) and thinner (3 nm) layers of the ALD NiO degraded the performance by reductions to FF and V\textsubscript{OC} [71]. These results are in complete agreement with our findings for the CdTe solar cells.

A second, and much more subtle, possible cause for the 4 nm NiO layers consistently outperforming the 11 nm NiO layers should also be addressed. Through all of our experimental work with the Savannah 200 ALD system we have come to realize that a chamber conditioning process is always beneficial for improving the integrity of the ALD grown films, regardless of what the ALD grown material is. This is because the ALD system we are using is shared amongst various research groups and industry users. As a result, this same ALD tool is also used to deposit other materials including ZnO, Al\textsubscript{2}O\textsubscript{3}, HfO\textsubscript{2}, TiO\textsubscript{2}, and several others. The low vapor pressure of Zn can be particularly problematic in cross contaminating films immediately after a ZnO deposition. For this reason, by running a chamber conditioning recipe the entire ALD
system can be coated with the desired ALD material and ‘cover up’ potential sources of unwanted materials left behind from previous ALD runs. No chamber conditioning was performed for these devices, however, and the first deposition was the 11 nm deposition. The 4 nm deposition immediately followed the 11 nm deposition. Therefore, the 4 nm deposition had effectively been done in a conditioned chamber while the 11 nm deposition was not. The point here is that any future work on this project should seek to condition the chamber prior to depositing transport layers of any type in order to maintain the highest chemical integrity, and therefore properties, of the transport layer material.

**Post Deposition Annealing:** The effect of the post deposition annealing treatment was very obvious: a severe declination of performance results in any case a device was annealed. The intention of this anneal was to improve the electrical and optical properties of the ALD NiO since these were the effects observed during our study of the post deposition annealing influences of the ALD grown NiO, as shown earlier in this chapter. However, the benefits from these effects, if they were even occurring, were severely outweighed by the negative effects on device performance. Careful observation of the data in Table 7 shows the annealing significantly increases the series resistance ($R_S$) for every configuration. This suggests the annealing treatment is inducing a reaction between the ALD grown NiO and the adjacent CdTe layer which forms some type of high resistance interlayer between the two materials. All of the solar cell efficiency parameters ($V_{OC}$, $J_{SC}$, and FF) are reduced as a result of this annealing. What this ultimately suggests is that the device performance is highly dependent on the thermal budget after the CdCl$_2$ treatment used to activate the CdTe. Figure 39 illustrates how there is a direct correlation between increased post CdTe processing thermal budget and $V_{OC}$ for both absorber thicknesses. Therefore, a follow up experiment of value would be to deposit the ALD NiO at an
even lower deposition temperature than the 200°C we used in this work in order to investigate the full potential of the ALD NiO as a transport layer.

![Thermal budget vs. $V_{OC}$](image)

**Figure 39:** As thermal budget goes up $V_{OC}$ goes down for both 2 µm cells (blue diamonds) and 0.5 µm cells (maroon squares)

This study illustrates there is great potential for NiO as a HT/EBL transport layer in conjunction with thin 0.5 µm CdTe absorbers. However, the benefit of increasing the CdTe absorber thickness in order to absorb more of the available sunlight still greatly outweighs the benefit of the NiO with the thinner CdTe absorber. This hints that if a light trapping architecture could be employed for the thinner CdTe absorber the full benefits of the NiO transport layer could be realized. The following chapter will discuss the design and numerical modeling of such light trapping architectures and provide evidence that thinner absorbers with equivalent light absorption can indeed be achieved when using an appropriate light trapping architecture.
Chapter 4: Numerical Modeling for LCCM Architectures

4.1 ANSYS HFSS Maxwell’s Equation Solver

To evaluate the potential of the highly ordered nano-element array light trapping architectures introduced in Chapter 2 the ANSYS HFSS™ [128] (hereafter HFSS) software was used. This software is called upon to simulate the interactions between the full-wavelength range of electromagnetic radiation from the sun and the light trapping architectures used in this work. The HFSS software employs physical optics to solve Maxwell’s equations in order to establish relations between electromagnetic waves and the device architecture.

In order to solve equations in a practical time HFSS uses a unit cell approach. Here, a single unit cell is the smallest possible volume of the light trapping architecture still maintaining the properties of the entire cell. Figure 40 shows a typical light trapping input architecture (left) and the corresponding unit cell (right).

![Figure 40](image.png)

**Figure 40:** Typical architecture (left) and unit cell (right) input to HFSS. Input materials (left) and boundaries (right) are also listed. [Adapted from 129]
Periodic boundary conditions are required to simulate the full geometry of the light trapping architectures based on its corresponding unit cell. This is done by designating “master” and “slave” boundaries on the faces surrounding the unit cell. For the hexagonal array used in these simulations there will be six boundaries: three “slave boundaries” and three “master” boundaries directly opposite of their respective slave boundaries. In other words, master and slave boundaries will alternate around the unit cell. When combining unit cells to create a macroscopic array the “slave” of one unit cell would be matched to the “master” of the adjacent unit cell as shown in Figure 40 (right). In this way, the flow of the electric field can be accounted for and allow periodicity of the electric field from the unit cell to be extended to the bulk architecture. In essence, by using this approach, the direction and magnitude of the electric field will be identical at the slave boundary of one unit cell and the corresponding master boundary of an adjacent unit cell at the same geometric location in space.

An excitation Floquet port at the top of unit cell is the initiating site of electromagnetic wave propagation (i.e. input power) and the bottom Floquet port is the terminating site of wave propagation. Any reflected light is captured by the top Floquet Port and therefore this port measures the reflectance, \( R(\lambda) \), and any light transmitted through the solar cell is captured by the bottom Floquet port, and therefore this port measures the transmittance, \( T(\lambda) \). HFSS solves the Maxwell’s equations in each material and ultimately obtains the absorptance, \( A_i(\lambda) \) for each layer in the structure, where \( A_i \) is the absorptance in the \( i^{th} \) layer. When coupling the Floquet ports with the three pairs of master-slave boundaries this fully bounds the unit cell and no radiation escapes the cell as a result of the energy conservation condition established in equation 2.2.

To simulate light trapping architectures HFSS requires certain input parameters pertaining to the materials shown in Figure 40, namely, input information is required for the
absorber material (e.g. nc-Si:H), the top TCO (e.g. AZO), and the back reflector (e.g. Ag). Here, the user must input for each material the wavelength dependent complex refractive index $\tilde{n}$ and the wavelength dependent complex permittivity $\tilde{\varepsilon}$ which are defined by equations 4.1 and 4.2 where $n$ is the real index of refraction, $k$ is the extinction coefficient, and $\varepsilon'$ and $\varepsilon''$ are the real and imaginary permittivity respectively. The values of these materials are readily available in the literature for nc-Si:H [130], AZO [131], and Ag [132].

$$\tilde{n} = n + ik \quad [4.1]$$

$$\tilde{\varepsilon} = \varepsilon' + i\varepsilon'' \quad [4.2]$$

Equations 4.3 and 4.4 define the real and imaginary parts of the permittivity $\varepsilon'$ and $\varepsilon''$ respectively. In equation 4.4 $\varepsilon''$ is seen to directly relate to the extinction coefficient which describes the absorption of electromagnetic waves. It intuitively follows that $\varepsilon''$ will also relate to the weakening of the electromagnetic field as it moves through the material.

$$\varepsilon' = n^2 - k^2 \quad [4.3]$$

$$\varepsilon'' = 2nk \quad [4.4]$$

Finally, with these equations and input parameters in hand the relative permittivity ($\varepsilon_r$) and the dielectric loss tangent ($\tan \delta$) can be obtained through equations 4.5 and 4.6. Here, $\varepsilon_0$ is the permittivity of free space.

$$\varepsilon_r = \frac{\varepsilon'}{\varepsilon_0} \quad [4.5]$$

$$\tan \delta = \frac{\varepsilon''}{\varepsilon} \quad [4.6]$$

In essence, the purpose of equations 4.1 through 4.6 is to convert the literature available values of these parameters into input values that HFSS understands such that the HFSS software can then compute the absorptance ratio at each point in each material for each wavelength.
In order to make the calculation of the electric field at each point in the material more manageable HFSS employs the finite element method \cite{133} in which the input geometry is divided into many smaller and more easily computable tetrahedra. The culmination of these tetrahedra is known as a mesh. The Maxwell’s equations are then solved for each tetrahedra in the mesh in a piecewise fashion. This greatly reduces computation time relative to HFSS attempting to solve the entire structure continuously. Not surprisingly, a coarse mesh using fairly large tetrahedra will yield less accurate results but a faster calculation time than a fine mesh using smaller tetrahedra.

Following the user establishing the mesh conditions the simulation can commence. The excitation boundary is the source for input power in which a range of frequencies specified by the user can be simulated, for simplicity an input power of 1 W is typically used. Here, Maxwell’s equations are solved for each frequency step. Typical frequency ranges used in our research group were from 200-1000 THz using a step of 10THz between frequencies \cite{129}. This corresponds to a wavelength range of 300-1500 nm. Wavelengths below 300 nm are not of interest since their high energy will cause high absorption in the top TCO layer and therefore their penetration into absorber material will be negligible. Wavelengths above 1500 nm are not of interest since their energy is well below the band gap of the nc-Si:H absorber material (\textasciitilde 1.1 eV) so they will not be absorbed. Although HFSS calculates the absorptance ratio for each frequency in each material in the simulated structure we are truly interested in the absorptance in the nc-Si:H since those are the absorption events that can lead to photogenerated carriers and ultimately the efficiency metric $J_{SC}$.

Equation 4.7 is used to calculate the wavelength dependent absorptance ratio values $A_i(\lambda)$ for each frequency step in each material, where $A_i$ is again the absorptance ratio in the $i^{th}$ layer.
Here, \( dV \) is the infinitesimal volume in which the absorptance ratio will be calculated, \( E \) is the electric field that HFSS has been able to calculate through solving the Maxwell’s equations, \( c \) and \( \lambda_0 \) are the speed of light in vacuum and wavelength in vacuum respectively.

\[
A_i(\lambda) = \int_V \pi \frac{c}{\lambda_0} e''(\lambda_0)|E|^2 dV \tag{4.7}
\]

By coupling the HFSS calculated \( A_i(\lambda) \) for the layer \( i \) of absorbing material with the photon flux of the AM1.5G spectrum \( (\phi(\lambda)) \) the \( J_{SC} \) value can be obtained in accordance to equation 4.8. Here, the limits of integration can be adjusted as necessary to match the absorber/TCO combination by using a short wavelength limit pertaining to the strong absorption of the TCO and a long wavelength limit corresponding to the absorber material’s band gap. Multiplication by the elementary charge \( e \) puts the units of \( J_{SC} \) into the more familiar mA/cm².

\[
J_{SC} = \int_{300 \text{ nm}}^{1100 \text{ nm}} A_i(\lambda)\phi_0(\lambda)e d\lambda \tag{4.8}
\]

It is vital to note a key assumption in making this relationship between the HFSS calculated \( A_i(\lambda) \) and \( J_{SC} \): for this relationship an external quantum efficiency (EQE) of one is assumed such that each photon absorbed in the absorbing material leads to a charge carrier making it to the external circuit. From a modeling standpoint, incorporating this EQE=1 assumption is simple and HFSS will readily yield \( J_{SC} \) values for any variety of device architectures and material combinations input by the user. However, as it will be discussed in Chapter 5, from a fabrication standpoint many of these device architectures and material combinations will lead to deviations from the ideal case of EQE=1. Therefore, it is important to take the HFSS calculated \( J_{SC} \) values as the upper bound for what is possible for a given device architecture and set of materials.
4.2 HFSS architecture considerations

Ultimately, a key purpose of the HFSS software is to narrow down the number of possible light trapping solar cell device architectures which could potentially be fabricated. The focus of this thesis is on the highly ordered nano-element arrays for enhanced light trapping such as those shown in Figures 16 and 40. The two key geometric parameters for such architectures are the spacing between the nano-elements (L) and the thickness of the absorber layer (t) as depicted in Figure 41. Previous work by our group established the shape of the nano-element (i.e. cylinder vs. cone) does not make a large difference in performance since it is the nano-dome morphology induced by these nano-elements which has the most profound influence on the light trapping ability of a given architecture [129]. Since the nano-dome morphology is most strongly a function of L and t it follows these will be the most significant geometric variables relating to a given architecture’s light trapping potential. By defining optimum ranges for L and t for a given set of materials a framework for the device fabrication can be established.

![Diagram showing Nano-dome and Nano-element shapes](image)

**Figure 41**: L and t are key geometric parameters influencing the nano-dome shape, which has the most profound influence on light trapping for a given set of materials [adapted from 129]
The ultimate purpose of these highly ordered nano-dome light trapping architectures is to strongly focus the electric field from the sun within areas of the device we would like it to be (i.e. in the absorber) in order to enhance $A_i(\lambda)$. In accordance to equations 1.1 and 4.8 this enhancement in $A_i(\lambda)$ can then lead to efficiency enhancements through an increased $J_{SC}$ value.

Much of our early simulation work focused on a-Si:H as the absorber material. Advantages of employing light trapping architectures with thin films of a-Si:H are (1) single junction a-Si:H cells with effective light trapping structures could rival the efficiency of their more complex multi-junction counterparts, (2) a much thinner absorber can be used and therefore increase throughput, (3) no randomly textured TCO is needed, and (4) by using ordered nanostructures more direct correlations can be made between architecture variables (i.e. $L$ and $t$) and performance. In addition, when the light trapping architectures are made out of a conductive material they also serve as an increased surface area electrode contact for enhancing the collection of photogenerated carriers. Again, for these reasons, we often refer to these geometries as the light and carrier collection management (LCCM) architectures.

As a result of a-Si:H having a much lower collection length than c-Si this was an original absorber material of investigation since the periodic nano-element light trapping architectures can facilitate charge collection at the electrodes in addition to helping with absorption. Carrier collection in a-Si:H solar cells in the p-i-n configuration is through drift. The drift collection length ($L_{COL}$) in a-Si:H is on the order of 300 nm [134]. Therefore, the thickness of the a-Si:H ($t$) and the spacing ($L$) of the nano-element array in conjunction with an a-Si:H absorber should be chosen such that all points within the absorber are within 300 nm of an electrode. In turn, in order to ensure all photogenerated carriers are generated within a collection length of an electrode our modeling work investigated geometries in which all points within the absorber
volume were within a collection length of an electrode. Here, we define the quantity $L_{\text{TEST}}$, shown in Figure 42, as the longest possible distance a carrier would have to travel to reach an electrode for a given combination of absorber thickness and L spacing. This puts a bound on the simulation conditions by choosing a combination of L and t which always lead to $L_{\text{COL}}>L_{\text{TEST}}$.

For a given absorber thickness, simple geometry dictates there will be three regimes of surface topographies which can result from varying the L spacing. As shown in Figure 42 we define the point in which the domes are just touching upon completion of the absorber and top electrode deposition as the $L_{\text{touch}}$ condition. For a given absorber thickness the choice of the L spacing between the columns will therefore afford one of three possible types of nano-dome morphologies: (1) truncated domes which are beginning to merge towards a planar morphology when $L<L_{\text{touch}}$ (top right), (2) domes which are just touching when $L=L_{\text{touch}}$ (bottom left), and (3) undulated domes which are spatially independent of each other when $L>L_{\text{touch}}$ (bottom right).

![Diagram showing different regimes of surface topographies](image)

**Figure 42:** Planar control layers (top left), $L<L_{\text{touch}}$ condition (top right), $L=L_{\text{touch}}$ condition (bottom left), $L>L_{\text{touch}}$ condition (bottom right). $L_{\text{TEST}}$ is also shown for each light trapping architecture. [Adapted from 47]
Typical layers used are also shown for the planar control devices as shown in Figure 42 (top left). In the following section the influence the geometric variables L and t have on $A_i(\lambda)$, and therefore $J_{SC}$, will be illustrated by providing HFSS simulation results for various light trapping device architectures.

4.3 HFSS simulation results for light trapping architectures

The absorptance ratio $A_i(\lambda)$ in 200 nm thick a-Si:H cells as function of L-spacing is shown in Figure 43. This configuration used the following geometry as defined in Figure 42 (bottom right): AZO nano-columns with d=100 nm and h=550 nm and t=200 nm a-Si:H, this resulted in R=200 nm and $R^*_{150}$ nm. The anode material was 80 nm of AZO. Either 5 nm or 30 nm of planar AZO was used as the cathode layer B as depicted by the inset of Figure 43.

![Figure 43: $A_i(\lambda)$ in a-Si:H for varying L-spacings [48]](image)

Observation of Figure 43 shows an overall high absorbance (often used interchangeably with the more appropriate term absorptance) in the a-Si:H for photons with energies above the band gap for all L-spacings. The manifestation of the long wavelength differences in $A_i(\lambda)$ are
witnessed as the resultant $J_{SC}$ differences shown in Figure 44. A key result of Figure 44 is that the optimum L-spacing for a given absorber thickness appears to be near the $L=L_{touch}$ condition.

Based on these findings solar cells based on thin films of a-Si:H were fabricated. These devices had AZO nano-columns with $d=150$ nm, $h=525$ nm, and an L-spacing of $L=1290$ nm in order to achieve a condition slightly above the $L_{touch}$ condition in conjunction with a $\sim400$ nm thick absorber stack. This $\sim400$ nm thick absorber is composed of 320 nm of intrinsic a-Si:H sandwiched between a 13 nm p-type Si layer and a 60 nm n-type Si layer. Figure 45 shows the JV characteristic, performance, and cross sectional FESEM image of the completed device.

![Figure 44: $J_{SC}$ values for a-Si:H cells as a function of L-spacing. Two thicknesses (5 nm and 30 nm) of the planar AZO optical spacer are shown. A maximum in $J_{SC}$ is seen to occur near the $L=L_{touch}$ condition. [48]](image-url)
The 8.2% efficiency of the device shown in Figure 45 was a record setting performance for a single junction a-Si:H solar cell using a light trapping architecture at the time of that device’s fabrication. This work established that our research group’s promising HFSS simulation results could be successfully transferred to experimentally fabricated devices.

These results were then extended to the other thin film absorber material based on silicon: nc-Si:H. Since nc-Si:H is a better collector than a-Si:H (i.e. larger L<sub>COL</sub>) it follows that larger L-spacings can be used and still satisfy the condition L<sub>COL</sub>&gt;L<sub>TEST</sub>. This opens up the opportunity for depositing thicker nc-Si:H absorbers with larger L-spacings and still obtaining the L<sub>touch</sub> condition. Figure 46 shows the J<sub>SC</sub> as a function of L for nc-Si:H cells with an absorber thickness of 800 nm. In accordance to the geometry shown in Figure 42 (bottom right) the other geometric parameters for these simulations were: R= 800nm, R<sup>+</sup>=750nm, d=100nm, H=550nm, and t=800nm. Once again for the nc-Si:H cells the L=L<sub>touch</sub> condition is shown be close to the situation which affords the maximum possible J<sub>SC</sub> value.
The potential of light trapping architectures with nc-Si:H is clearly shown in Figure 46. Here, light trapping architectures outperformed the planar control cell regardless of the L spacing by exhibiting 17~55% higher $J_{SC}$ values than that of the planar control cell (18.84 mA/cm$^2$). It is apparent the variation of $J_{SC}$ is closely related with the spatial frequency of the undulation of the domes with the highest $J_{SC}$ value occurring for the spacing condition just above $L=L_{touch}$. This increased $J_{SC}$ value for the condition just above $L=L_{touch}$ is a result of enhanced inter-dome scattering when compared to the $L_{touch}$ condition. Figure 47 shows the $A_i(\lambda)$ characteristic leading to the $J_{SC}$ values for the control cell (blue line) and the $L=1600$ nm spacing condition (red line) shown in Figure 46. Both of these devices had a nc-Si:H thickness of 800 nm. To further illustrate the value of the light trapping architecture the $A_i(\lambda)$ characteristic of a much thicker absorber of 1350 nm (green line) in the planar configuration is also shown.
Figure 47: $A(\lambda)$ for LCCM cell with 1600 nm spacing and 800 nm thick nc-Si:H (red line), planar cell with the same 800 nm nc-Si:H thickness as the LCCM cell (blue line), and planar cell with 1,350 nm nc-Si:H thickness (green line) [48]

In Figure 47 the LCCM structure (red line) leads to an increased $A_i(\lambda)$ that is drastically higher than the planar value for the same absorber thickness (blue line) or thicker planar devices (green line) across all wavelength ranges. This again results in the increased $J_{SC}$ for the LCCM cell in accordance to equation 4.8. In fact, the $J_{SC}$ value of the LCCM cell is very close to $4n^2$ limit of Yablonovitch [135]. Table 8 summarizes key features of Figure 47 and illustrates how the $J_{SC}$ improvement resulting from the light trapping architecture drastically outweighs the $J_{SC}$ improvement from the conventional route of increasing the absorber thickness. Namely, a nearly 70% increase in absorber thickness leads to a 9% increase in $J_{SC}$ while the use of a light trapping architecture with a 0% increase in absorber thickness leads to a nearly 55% increase in $J_{SC}$. 


<table>
<thead>
<tr>
<th>Cell</th>
<th>Absorber Thickness (nm)</th>
<th>L Spacing (nm)</th>
<th>$J_{SC}$ (mA/cm$^2$)</th>
<th>% Increase in Thickness</th>
<th>% Increase in $J_{SC}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Control 1</td>
<td>800 nm</td>
<td>--</td>
<td>18.88</td>
<td>--</td>
<td>--</td>
</tr>
<tr>
<td>Control 2</td>
<td>1350 nm</td>
<td>--</td>
<td>20.6</td>
<td>68.8</td>
<td>9.1</td>
</tr>
<tr>
<td>LCCM</td>
<td>800 nm</td>
<td>1600 nm</td>
<td>29.2</td>
<td>0</td>
<td>54.7</td>
</tr>
</tbody>
</table>

**Table 8:** Summary information for the nc-Si:H solar cells with the $A(\lambda)$ characteristic shown in Figure 47.

A final consideration pertaining to the influence of the device architecture on light trapping and device performance is that of the aspect ratio of the nano-elements for a given L spacing and absorber thickness. The aspect ratio is defined as the ratio $h/d$ as shown in Figure 42. Figure 48 illustrates that higher aspect ratios enhance absorption in the short wavelength ranges. Whether or not the benefits of this enhanced short wavelength absorption is worth the added complexity of fabricating higher aspect ratio structures depends on how strongly the given absorber material absorbs such high energy photons in the first place.

**Figure 48:** Enhanced absorption at shorter wavelengths for higher aspect ratio structures [136]
4.4 Summary of HFSS modeling results

Our modeling work has led us to several important conclusions that will serve as a framework for establishing the processing conditions for device fabrication. The combination of nano-element spacing (L) and absorber thickness (t) leading to the condition in which the domes are just touching following the absorber deposition leads to a nearly optimum \( J_{SC} \) value. In addition, we found this condition holds for both a-Si:H and nc-Si:H.

It should be noted that this nano-dome morphology for a-Si:H and nc-Si:H is only possible as a result of the extremely conformal nature of the PECVD process used to deposit these materials. This is, in fact, the key reason we are not investigating the other common thin film absorber materials (CIGS, CdTe) or emerging solar cell materials (Perovskites, OPV) in conjunction with our highly ordered light trapping architectures. For instance, the deposition of CIGS typically employs co-evaporation [137] which is a highly non-conformal deposition method and therefore could not afford the nano-dome morphology upon which all of our simulation work was based. Similarly, CdTe is most frequently deposited with sputtering [127] which is slightly more conformal than co-evaporation but still far from the sufficient for creating conformal coatings on the high aspect ratio light trapping architectures being sought. The spincasting method used for perovskites and OPV would also not be able to provide the conformal coatings necessary to achieve the full potential of the light trapping architectures. Additionally, the high process temperatures in excess of 500°C required for the multistage co-evaporation process of CIGS devices and the ~400°C CdCl₂ treatment for CdTe cells would also limit both of these absorber materials to only high temperature substrates [127, 137]. Both of these temperatures are well in excess of the 309°C glass transition temperature of the flexible polyimide [138] substrate material we desire to develop high throughput fabrication processes.
for. Therefore, the low deposition temperatures of PECVD nc-Si:H (<200°C) are vital for maintaining the ability to work with the temperature sensitive polymer substrates we seek to use.

The following two chapters pertaining to the fabrication of light trapping solar cells represents the bulk of this thesis work. Both the detailed experimental conditions and the corresponding processing considerations which were discovered throughout the course of device fabrication will be presented. As it turns out, the high aspect ratio light trapping architectures simulated in this chapter led to the realization of additional design considerations which could not be foreseen through the modeling results alone; such as the topography induced defects introduced in Chapter 2. The following chapter will begin by detailing the origin of these topography induced defects and then discuss how they can be circumvented by altering the processing conditions. Next, top electrode deposition considerations will be addressed. This will be followed by the fabrication sequence and subsequent characterization of light trapping solar cells made with both an electron beam lithography approach and a nano-molding approach.
Chapter 5: Fabrication and Characterization of nc-Si:H LCCM Cells

To fabricate the highly ordered nano-element architectures introduced in Chapter 2 and simulated in Chapter 4 various fabrication approaches have been pursued. Approaches using electron beam lithography (EBL) methods in conjunction with both the substrate (Si wafer or flexible polyimide template) and superstrate (glass) configurations have been developed. For increased throughput and the potential for solution based processing conducive to printing techniques a block copolymer fabrication scheme eliminating EBL steps has also been developed. One thing common to all of these approaches is that the resulting highly ordered light trapping nano-element architectures have led to unforeseen difficulties with the subsequent deposition of the nc-Si:H absorber due to shadowing effects which are not present with the conventional planar topographies. The following sections will address this absorber layer deposition issue and discuss how a defect free nc-Si:H absorber can still be achieved even with an aggressive light trapping morphology which is highly susceptible to shadowing effects.

5.1 nc-Si:H absorber layer deposition considerations

The solar cells built in this thesis work were part of collaborative research efforts between Penn State University and two other research institutions: the PV and Renewable Energy Technology and Engineering Lab CH-2000 in Neuchâtel Switzerland (Swiss) [139] and LPICM-CNRS Ecole Polytechnique in France (France) [140]. The nano-element electrode arrays would be fabricated at Penn State while the absorber and top TCO would be deposited at either Swiss or France since these facilities have PECVD systems capable of depositing high quality layers of nc-Si:H.
It was introduced in Chapter 2 that light trapping architectures can produce defective filaments in the absorber as a result of shadowing effects. The deposition onto a structured topography will cause the growth rate to be different on the horizontal and vertical surfaces. These effects are particularly pronounced for the sputtering and PECVD techniques used to deposit the metal layers and nc-Si:H respectively; this is a result of the bombardment present during deposition [141]. Different step coverage is most directly explained by the different incident angles of the incoming metal atoms (for sputtering) or growth precursors (for PECVD).

Figure 49 shows top down (left) and cross sectional (right) images of a completed LCCM device fabricated based upon a polyimide template. Here, due to the structured topography, defects are seen to occur in the nc-Si:H. The cross sectional image showed a curtain of defects formed around the nano-elements with a density of $\sim 10^{14}/\text{cm}^2$ which was extrapolated from the estimate that these defective regions were $\sim 5$ nm in width as observed by the 30° tilted FESEM image [142]. It should be noted the small bright regions appearing as crystallites in Figure 49 are actually a result of contamination resulting from the FIB imaging process.

![Figure 49](image_url)

**Figure 49:** Top down and cross sectional view of a completed device based on the nano-molding approach. Defects in the absorber are seen in the cross sectional view. [Adapted from 142]
The fabrication method and device performance of the completed device shown in Figure 49 will be discussed later in this chapter. The aim of the following two sections is to address (1) how these defects form and (2) how they can be eliminated. Elimination of these defects is critical since these regions act as bad diodes in parallel to the solar cell since they serve as shunt paths for photogenerated current [51]. Additionally, the porous nature of these defective regions allows them to act as havens for the accumulation of contaminants (e.g. O₂, H₂O, dopants, etc.) leading to a more rapid declination in device performance over time [52].

5.2 A working model of the defect formation mechanism in nc-Si:H

The importance of developing a working model for the cause of the defect formation occurring in the nc-Si:H is that if the formation mechanism itself is known, the solution to fixing the occurrence of the defect can be more logistically approached. In the literature, the occurrence of physical defects in nc-Si:H on structured topographies is commonly reported. However, the cause of these defects is typically only vaguely explained and the cause is most commonly attributed to the self-shadowing effects resulting from the substrate topography.

In order to more deeply address the root cause of the defect formation issue, we have developed a simple working model based on the physical location in the nc-Si:H our defect occurs in. The location of this physical defect occurs at roughly a 45° angle with respect to the notched region on the growth template, as shown in Figure 50 (left). For clarity, the geometry of the initial growth surface that the model will be based on is redrawn in purple in Figure 50 (right). Based on this geometry, and the shape of the defective filament, a working model will be suggested. The working model is supported by the literature available information on the growth characteristics of nc-Si:H, attributes of PECVD growth, and geometric effects.
To begin, the structured PI/Ag/AZO substrates, which will be shown as a single purple layer in this growth model, are loaded into the PECVD for the deposition of nc-Si:H using a SiH\(_4\)/H\(_2\) plasma. After establishing the proper gas flow rates, pressure, and temperature in the PECVD system the 13.56 MHz RF power is applied and the plasma is quickly ignited and stabilized. As shown in Figure 51, during stage 1 of the growth an amorphous incubation layer will quickly passivate the growth surface. Such amorphous incubations layers are common in PECVD processes [143]. Owing to the differing electrode sizes between the electrode the sample is placed on and the size of the chamber, a negative self bias on the smaller electrode the sample is sitting on will develop. This negative self bias will attract positive ions from the plasma and lead to directional ion bombardment of the horizontal growth surfaces. This bombardment will serve to passivate the initially defective surface and further enhance the growth rate of the nc-Si in these directions relative to the sidewalls, which already are subject to a reduced precursor flux. Next, upon the collision of the quickly growing (green) nc-Si:H in the
vertical growth direction and the slowly growing nc-Si:H in the horizontal growth direction (red) a defective and porous region of low quality a-Si:H will result at the interface between these two growth modes. This defective region will propagate outwards with the film growth as the horizontal growth rate is slowly pushed out of existence. All of these effects in our proposed model of the defect formation in the nc-Si:H are shown in Figure 51.

By identifying a mechanism for the defect formation, a working solution to overcoming this problem can be more easily proposed. Since the defective region between growth fronts consists of voids and low quality porous a-Si:H a potential solution could be the use of a
different PECVD gas chemistry in which the defective material can be selectively (chemically) etched away before its burial and permanent incorporation into the final thin film.

5.3 Eliminating the defect formation mechanism in nc-Si:H

In order to eliminate these defects the most common route has been to use a less aggressive (*i.e.* smoother) substrate morphology such as the approach shown in Figures 17 and 18 in Chapter 2. However, since these nano-element topographies are inherent to the desired geometry of our light trapping nano-dome architecture we sought to take an alternative route to eliminate defect formation. While others chose to change the morphology upon which the nc-Si:H was deposited onto we chose to instead change how the nc-Si:H was deposited.

The nc-Si:H shown in Figure 49 was deposited with the conventional highly H₂ diluted SiH₄ plasma. This is the most common route for depositing nc-Si:H with PECVD [144-146]. However, with this gas chemistry, shadowing effects caused by the aggressive light trapping architectures coupled with a low surface diffusion of the adsorbed precursor species results in regions of low quality and porous amorphous material. The manifestation of this low quality material is the occurrence of the physical defects which originate at the notched (shadowed) regions. In addition to this geometric constraint imposed by nc-Si:H grown with SiH₄ there is also an economic constraint pertaining to high H₂ usage. For defect free nc-Si:H high dilutions of SiH₄ in H₂ are needed; further, the required [SiH₄/(SiH₄+H₂)] values of a few % will require extremely high values of H₂ (100’s of sccm) which is not ideal for industrial processes [147].

To circumvent these issues this thesis also investigated a fluorinated PECVD chemistry using SiF₄ to deposit nc-Si:H. What makes the SiF₄/H₂/Ar plasma chemistry more compatible with our topography is that the growth mechanism for this plasma chemistry features both a
deposition and an etching component; unlike the SiH$_4$/H$_2$ system which features only a strong deposition component [147]. During the deposition of nc-Si:H with the SiF$_4$/H$_2$/Ar system defective regions will still form temporarily during the deposition as a result of insufficient precursor flux in shadowed areas. However, by tailoring the plasma conditions, these defective regions can be etched away before they are buried, which affords a defect free material. This is a result of the amorphous phase of silicon being known to rapidly etch in the presence of F radicals. In short, the increased etch selectivity unique to the SiF$_4$ chemistry will be exploited to circumvent the shadowing effects imposed by nano-element morphologies.

From an energetic standpoint, these effects are explained by Table 9 which shows both the bond dissociation energies of the various combinations of F, H, and Si which could be present on the surface during growth along with the reaction energies corresponding to various precursor fragments present during growth and etching [148-152].

<table>
<thead>
<tr>
<th>ID</th>
<th>Bond</th>
<th>Dissociation Energy (eV) [148-149]</th>
<th>ID</th>
<th>Reaction</th>
<th>eV [150-152]</th>
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</thead>
<tbody>
<tr>
<td>b1</td>
<td>F-H</td>
<td>5.9</td>
<td>r1</td>
<td>SiF$_2$→SiF+F</td>
<td>6.8</td>
</tr>
<tr>
<td>b2</td>
<td>Si-F</td>
<td>5.6</td>
<td>r2</td>
<td>SiF$_4$→SiF$_3$+F</td>
<td>6.7</td>
</tr>
<tr>
<td>b3</td>
<td>H-H</td>
<td>4.5</td>
<td>r3</td>
<td>SiF→Si+F</td>
<td>5.6</td>
</tr>
<tr>
<td>b4</td>
<td>Si-Si</td>
<td>3.4</td>
<td>r4</td>
<td>SiH$_4$→SiH$_3$+H</td>
<td>3.5</td>
</tr>
<tr>
<td>b5</td>
<td>Si-H</td>
<td>3.1</td>
<td>r5</td>
<td>H$_3$Si-SiH$_3$+F→H$_3$Si+H$_3$SiF</td>
<td>3.4</td>
</tr>
<tr>
<td>b6</td>
<td>F-F</td>
<td>1.6</td>
<td>r6</td>
<td>F+H$_2$→HF+H</td>
<td>0.04</td>
</tr>
</tbody>
</table>

**Table 9:** Bond dissociation energies of various combinations of F, H, and Si present on the surface (left) reaction energies for various components present during growth (right) [148-152]

As shown in Table 9 the basis for this increased etch selectivity between the amorphous and crystalline phases of Si when using the fluorinated plasma chemistry is ultimately a result of the formation of HF being the most favorable on the surface during growth as shown by bond
energy b1 and reaction r6. This HF can directly etch amorphous material, or more likely, it will desorb back into the plasma where it will be dissociated into F and H radicals [147]. These F radicals can then combine with various amorphous SiF$_3$H$_x$ fragments on the surface and carry away the amorphous deposits as gaseous byproducts as exemplified by equation 5.1.

$$SiF_3H(a) + 2F \rightarrow SiF_4(g) + HF(g) \quad [5.1]$$

The enhanced etching provided by SiF$_4$ can be appreciated by contrasting the Si-Si bond strength (b4) to the dissociation energies of SiH$_4$ (r4) and SiF$_4$ (r2). For the SiF$_4$ chemistry, the removal of a SiF$_3$ precursor fragments by F radicals releases twice as much energy as maintaining Si-Si bonds in the growing film. For the SiH$_4$ chemistry, the etching of SiH$_3$ fragments by H radicals releases about the same amount of energy as maintaining Si-Si bonds in the growing film. It follows that the etching component during deposition will be much more significant for the SiF$_4$ chemistry than for the SiH$_4$ chemistry, and as a result the deposition rate for the SiF$_4$ chemistry will be lower. It is well known that lower deposition rates lead to higher crystallinity films and this is indeed the case when contrasting SiH$_4$ plasmas to SiF$_4$ plasmas for the growth of nc-Si:H.

The use of a halogenated precursor chemistry does not guarantee defect free and fully crystalline growth, however. In order to maximize crystallinity the gas chemistry must be carefully tuned for a given reactor geometry, deposition power, process temperature, substrate temperature and most importantly sample geometry. As it will be shown shortly, the switch to the SiF$_4$ PECVD gas chemistry is not a universal solution for all substrate topographies and in some cases defects will inevitably occur due to purely geometric effects.

For the SiF$_4$/H$_2$/Ar plasma chemistry the H$_2$ flow rate is the critical parameter in determining the crystallinity of the material. Low H$_2$ flow rates lead to a-Si:H while higher H$_2$
flow rates lead to nc-Si:H. Here, the full removal of F from the growing film corresponds to the amorphous to nanocrystalline transition point. For low H₂ flow rates the H₂ is completely depleted during its role in removing F from the film through reaction r6. Since the H₂ is depleted some F will remain in the deposited film and an amorphous structure results. Higher H₂ flow rates scavenge all of the F from the film and the excess H₂ leads to the processes inducing crystallization [147]. An increased process power will increase the flux of SiFx growth precursor fragments and therefore a higher H₂ flow rate will be needed to remove all of the F to ensure a crystalline film. Similarly, an increased pressure resulting from an increased SiF₄ flow rate will also require a higher H₂ flow rate to maintain crystallinity.

The influence of temperature on film crystallinity when comparing SiF₄ to SiH₄ PECVD chemistries is much less obvious, but equally significant, especially since this thesis work is aiming to work with temperature sensitive substrate materials such as PI. Therefore, crystallinity at a low PECVD deposition temperature is required. On this end, a study was done by others in which the etch rate of both a-Si:H and nc-Si:H by both H atoms and F atoms was conducted. This study concluded that the etching of a-Si:H and nc-Si:H by fluorine atoms have positive pseudo activation energies of $E_{a-Si:H} = 0.028$ eV and $E_{nc-Si:H} = 0.11$ eV respectively [143]. As expected, a larger energy barrier is required for etching the nc-Si:H phase than the a-Si:H phase. This means that as the temperature is lowered the etch selectivity, $E_s$, defined by equation 5.2, will increase when using the SiF₄ plasma chemistry. This is highly favorable since the etching of defective regions will in fact be more pronounced as the deposition temperature is decreased.

$$E_s = \frac{r_{a-Si:H}}{r_{nc-Si:H}} = \frac{ae^{-\frac{E_{a-Si:H}}{kT}}}{be^{-\frac{E_{nc-Si:H}}{kT}}} \quad [5.2]$$
This same study also found that the etching of a-Si:H and nc-Si:H by hydrogen atoms have negative pseudo activation energies of \( E_{a-Si:H} = -0.026 \) eV and \( E_{nc-Si:H} = -0.097 \) eV respectively. Therefore, with SiH\(_4\) higher deposition temperatures will result in an increased etch selectivity and thus a high deposition temperature is required to obtain fully crystalline material [143]. This study shows that strong etching selectivity at low temperatures is unique to SiF\(_4\) and this is ultimately what allows the growth of defect free nc-Si:H films at the low deposition temperatures (<200°C) used for the devices fabricated in this thesis work. To summarize, Table 10 contrasts key distinctions between SiH\(_4\)/H\(_2\) and SiF\(_4\)/H\(_2\)/Ar PECVD gas chemistries.

<table>
<thead>
<tr>
<th>Processing attribute</th>
<th>SiH(_4)/H(_2)</th>
<th>SiF(_4)/H(_2)/Ar</th>
</tr>
</thead>
<tbody>
<tr>
<td>Required H(_2) dilution for nc-Si:H</td>
<td>High (&gt;90% H(_2))</td>
<td>Low (&lt;5% H(_2))</td>
</tr>
<tr>
<td>Hydrogen content in nc-Si:H</td>
<td>High (5-20%)</td>
<td>Low (1-5%)</td>
</tr>
<tr>
<td>Film stability</td>
<td>Lower (more H)</td>
<td>Higher (less H)</td>
</tr>
<tr>
<td>Growth Source(s)</td>
<td>SiH(_x)-1</td>
<td>H, SiF(_x)-1</td>
</tr>
<tr>
<td>Primary Etchant During Growth</td>
<td>H</td>
<td>F</td>
</tr>
<tr>
<td>Low Temp Etch Selectivity: ( E_{a-Si}/E_{nc-Si} )</td>
<td>Low</td>
<td>High</td>
</tr>
<tr>
<td>High Temp Etch Selectivity: ( E_{a-Si}/E_{nc-Si} )</td>
<td>High</td>
<td>Low</td>
</tr>
<tr>
<td>Favorable Temp for nc-Si:H growth</td>
<td>T&gt;300°C</td>
<td>T&lt;200°C</td>
</tr>
</tbody>
</table>

**Table 10:** Comparison of processing attributes between nc-Si:H grown with SiH\(_4\) and SiF\(_4\) PECVD chemistries

Based on the potential for SiF\(_4\) to afford defect free nc-Si:H on our light trapping morphologies at low deposition temperatures we sought to make devices based on this gas chemistry through our collaboration with France whom have access to a PECVD with SiF\(_4\) gas chemistry. Figure 52 shows a completed device based on a EBL substrate nano-element fabrication approach, which will be discussed later in this chapter, in which defect free nc-Si:H was successfully deposited by France using the SiF\(_4\) PECVD chemistry.
Figure 52: Cross sectional FIB image illustrating the elimination of physical defects in the nc-Si:H by using SiF₄ PECVD plasma chemistry

The comparison between Figures 49 and 52 illustrates an important technical barrier pertaining to the fabrication of light trapping architectures based on nc-Si:H was overcome upon making this switch from SiH₄ to SiF₄ gas chemistry. Ultimately, the elimination of defective regions is necessary to preserve internal transport properties relative to that of a planar device (i.e. maintain FF) and to avoid increasing carrier recombination relative to the planar device (i.e. maintain Vₜₜ). If FF and Vₜₜ can be maintained for light trapping architectures by mitigating defect formation in the nc-Si:H then the increase in Jₜₚ owing to the light trapping architectures will lead to efficiency enhancements in accordance to equation 1.1.
As it was mentioned, switching to the SiF$_4$ gas chemistry is not a universal solution to depositing defect free films of nc-Si:H on the entire range of possible topographies. As shown in Figure 53, by reducing the L-spacing from 1,600 nm (Figure 52) to 1,400 nm (Figure 53) defective regions are induced when the flat areas between adjacent domes disappear. These defects originate between the domes at the top of the deposited layer as a result of the reduced precursor fluxes to the shadowed areas which occurs when the flat areas between the domes disappear. This same effect was also observed by Sai et. al. as was shown in Figure 18.

Figure 53: Cross sectional FIB image illustrating physical defects can still occur in the nc-Si:H with the SiF$_4$ PECVD plasma chemistry when the shadowing effects are severe.

To summarize, others have eliminated defect formation in the nc-Si:H by changing the physical nature of the surface by modifying the topography for a given deposition chemistry. We have instead eliminated defect formation by modifying the deposition chemistry for a given
topography. Avoiding these defects is imperative for maintaining FF and $V_{OC}$ to fully harness the gains in $J_{SC}$ provided by the light trapping architectures. In addition to the quality of the absorber material the characteristics of the top TCO layer which completes the solar cell device are also important for maintaining the FF and $J_{SC}$ by providing a low series resistance and high optical transparency Ohmic contact. The following section will discuss some key TCO attributes and considerations for this final processing step. Following this discussion the complete fabrication scheme will be presented for light trapping solar cells made with both an electron beam lithography (EBL) approach and a nano-molding approach. Immediately following each of these fabrication schemes the performance of the completed devices, such as that shown on the PI template in Figure 49, will be provided and discussed.

5.4 Transparent conductive oxide layer deposition considerations

For thin film solar cells the properties of the top TCO are extremely important in determining the overall efficiency of the device. As a most basic prerequisite, the top TCO must simultaneously have a high optical transparency (>~85%) in the visible range and a low sheet resistance (<~10 $\Omega$). For the nc-Si:H absorber material used in this thesis the long wavelength transmission of the TCO is particularly significant since nc-Si:H can absorb a larger range of photons than other thin film materials (e.g. a-Si:H) due to its lower band gap. As a result, the TCO needs to have a high optical transparency over a larger wavelength range (~400-1100 nm) for nc-Si:H than for a-Si:H (~400-750 nm) [153].

In the superstrate fabrication scheme the TCO must also provide a favorable growth surface and act as a good nucleation layer for the growth of nc-Si:H. Since the nc-Si:H in this thesis will be deposited from the gas phase process PECVD the TCO must also be inert to the H$_2$ rich plasmas used to grow nc-Si:H. One material meeting all of these requirements is AZO.
These characteristics are the reasons AZO has been a frequently encountered material in both our modeling and fabrication work.

Our repeated use of ALD grown AZO in our various nano-element fabrication approaches has led us to investigate some of this material’s processing-properties relations. We are particularly interested in the influence of the ALD growth temperature and the ZnO:Al₂O₃ cycles (i.e. doping) ratio on the resultant AZO’s resistivity since these are both parameters we can easily adjust. To investigate the influences of these variables we deposited a variety of AZO films with varying temperatures and doping ratios, all of which were the same thickness of ~40 nm. All films were patterned into bar structures and the average resistance of four patterned bars on a given substrate was used in conjunction with equation 3.1 to compute the resistivity for each condition. The influences of temperature and doping ratio on resistivity are shown in Figure 54.

**Figure 54:** Resistivity of ALD grown AZO as a function of temperature and ZnO:Al₂O₃ cycles ratio. All films were ~40 nm thick.

As the temperature rises the enhanced crystallization of the ZnO affords higher conductivity for a given doping ratio. For the AZO grown with the 60:1 doping ratio the two
largest increases in conductivity are observed when increasing the temperature from 100°C to 120°C and again when increasing the temperature from 175°C to 200°C. The most significant conductivity increase occurs upon increasing the temperature from 100°C to 120°C in which this 20°C increase in growth temperature increases the conductivity by roughly a factor of 80. This effect can hypothesized to be the result of an activation barrier for ligand desorption being overcome in this temperature range. As it has been explained and exemplified by others, ligands causing steric hindrance will lead to a less dense and more amorphous material. The thermally supported desorption of such reaction intermediate species can open up the most energetically favorable growth face and lead to a more crystalline material with a lower carbon content [114].

A trademark of ALD is most materials are grown amorphous and difficult to crystallize (e.g. Al₂O₃), with ZnO being one of the exceptions [154]. It follows that the further increase in conductivity by a factor of ~5 upon increasing the growth temperature from 175°C to 200°C is more likely a result of enhanced crystallization of the ZnO phase of the AZO. This is supported by the fact that the 20:1 increase in conductivity over the same temperature range is much less significant, owing to the lower relative amount of ZnO content in the 20:1 ratio material.

To gain more insight on the specific role of the doping ratio and its influence on conductivity various doping (i.e. cycle) ratios of ZnO:Al₂O₃ were investigated including 16:1, 18:1, 20:1, 24:1, 28:1, 60:1, 60:2, 60:3 and 40:2. The results of these experiments showed that a 20:1 ratio gives the most conductive AZO film in agreement with the literature on this material [155]. Beginning on the right side of Figure 55 a large initial decrease in resistivity occurs when a small amount of Al₂O₃ is added to the pure ZnO (pure ZnO vs. 60:1 AZO). This is a result of the substitutional doping of Al atoms on Zn sites such as the behavior shown in equation 2.5 [156]. The resistivity continues to decrease as the doping increases and reaches a minimum
value at a doping ratio of 20:1. Doping levels in excess of 20:1 are then seen to cause the resistivity to rise. It has been reported by others that in excess of ~4 atomic % Al the formation of insulating Al₂O₃ clusters cause the resistivity to rapidly increase since these clusters act as carrier traps instead of electron donors [157]. With respect to our experimental observations, these Al₂O₃ clusters became significant at the heavily doped 16:1 ratio.

![Graph showing resistivity of AZO deposited at 200°C](image)

**Figure 55:** Influence of ZnO:Al₂O₃ cycle ratio on resistivity of AZO deposited at 200°C. All films were 30 nm thick.

To further investigate this theory of Al₂O₃ clusters causing the significantly decreased conductivity for the 16:1 ratio condition a follow up experiment was conducted in which AZO films with the same absolute 20:1 doping ratio but different supercycle thicknesses were deposited. For the ALD tool used in this thesis work the known 200°C GPC values for ZnO grown with diethyl zinc and H₂O and Al₂O₃ grown with trimethyl aluminum and H₂O are 1.3 Å/cycle and 1.1 Å/cycle respectively. In this study supercycles composing ZnO:Al₂O₃ ratios of 20:1 (~2.7 nm thick), 40:2 (~5.4 nm thick), and 60:3 (~8.1 nm thick) were all investigated. All of these films have the same reduced ratio of 20:1 for ZnO:Al₂O₃, but the formation of clusters
should be most prominent for the 60:3 condition since this supercycle consists of 30 ZnO cycles, 3 Al₂O₃ cycles, and 30 ZnO cycles. The 3 consecutive Al₂O₃ cycles are expected to form insulating clusters with a thickness close to that of a full monolayer of the ALD grown Al₂O₃ which is ~3.8 Å [158]. The full monolayer thickness of ALD grown Al₂O₃ can be estimated by using the density of 3.0 g/cm³ for ALD grown Al₂O₃ at a similar deposition temperature of 177°C [159]. This affords a number density of \( \rho = 1.77 \times 10^{22} \) Al₂O₃ units/cm³, the monolayer thickness is therefore estimated as \( \rho^{-1/3} = 3.8 \) Å [158]. For this experiment the number of supercycles was varied to give total film thicknesses of ~30 nm for each of these ratios. Ratios of 60:2 and 60:1 with the same film thickness were also investigated as controls. The results of this study are shown in Figure 56 and clearly support the theory that insulating Al₂O₃ clusters are the cause for drastic resistivity increases.

![Graph](image)

**Figure 56:** Al₂O₃ clusters on the order of a monolayer thickness of ALD grown Al₂O₃ are the cause for the drastically increasing resistivity for excessive Al₂O₃ doping ratios in AZO

Tuning the growth temperature and ZnO:Al₂O₃ ratio both have a large influences on the AZO conductivity. In addition, these parameter modifications also influence the transparency of
the AZO since increasing the Al$_2$O$_3$ content will increase the transmittance due to band gap enhancement provided by the wider band gap material Al$_2$O$_3$. The net result of this is that the 20:1 AZO which has been settled on in this thesis has both a higher conductivity and a higher transparency than the 60:1 AZO material which was being used initially. These improvements in conductivity and transparency make the 20:1 AZO a more ideal TCO material for a solar cell.

The band alignment and n-type conductivity of AZO makes this a good electron collecting and transporting material. In many of our fabrication methods, these AZO nano-columns are often coated on an opaque material such as Si or a partially opaque material such as PI. It follows that the conductivity is the key property of importance for the AZO in this configuration, hence our much heavier investigation of the conductivity of this material than the transparency of this material. Since the AZO is typically not being used as a TCO for our light trapping architectures it follows that a different, hole collecting, TCO material should be used for the top electrode. The material we have used for this role is ITO owing to this material’s high conductivity and transmittance.

The ITO for our completed devices is applied by sputtering. Although this sputtering is most often done by Swiss of France following their deposition of the nc-Si:H a small side project in this thesis also briefly investigated some of the properties of in house sputtered ITO. Figure 57 shows the transmittance, conductivity, and morphology of ~240 nm of sputtered ITO on glass. The ITO was sputtered in a Kurt J Lesker sputtering system for 1600s at 300°C and 200W with an ITO target with 10% SnO$_2$ and a reactive sputtering gas containing <1% O$_2$ in N$_2$. This ITO is seen to possess a reasonable combination of transparency and conductivity. A resistivity value of $4.4 \times 10^{-3} \, \Omega \text{cm}$ was obtained by patterning the ITO into a bar structure by wet etching the 240 nm of sputtered ITO in a 3:1 solution of HCl:DI water (9 M HCl). It was found 90
seconds was required to fully etch the ITO. This is a significantly shorter etch time than that which was found required to etch commercial ITO purchased from Delta Technologies of similar thickness (200 nm) with the same wet etchant chemistry. This reduced etch time suggests our sputtered ITO is of higher amorphous content and is in agreement with the relatively high resistivity for this ITO. In the event it was desired to deposit the top ITO layer in house further optimization of the sputtering temperature and diluted O\textsubscript{2} gas flow rate would be required to obtain ITO with resistivity values closer to desirable 1x10^{-4} \ \Omega \text{cm} which is required for minimizing the series resistance of the top TCO. The relatively low conductivity of this ITO caused us to only briefly investigate this material in house.

**Figure 57:** Transmittance of ~240 nm of sputtered ITO. The inset shows the patterned bars used to calculate the resistivity along with the ITO morphology as observed with AFM
At this point the key processing considerations for the absorber layer and top TCO layer depositions pertinent to this work have been discussed. The following two sections will provide two different nano-element electrode fabrication schemes. Immediately following the complete fabrication scheme \(i.e.\) nano-element electrode fabrication, absorber deposition, top TCO deposition) the results of the completed devices will be provided and discussed.

5.5 Fabrication and characterization of LCCM cells based on the electron beam lithography substrate approach

Figure 58 shows the summary flow of steps used for fabricating light trapping electrode architectures based on the electron beam lithography (EBL) substrate approach. This method begins by patterning the positive tone e-beam resist ZEP 520a (ZEP) \([160]\) on a cleaned and dehydrated 4” Si wafer. Electron beam evaporation (EBE) is then used to deposit Cr through the patterned ZEP resist and a subsequent liftoff step removes the ZEP template leaving only the patterned Cr hard mask on the surface of the wafer. This Cr hard mask provides the high dry etch selectivity needed to drill high aspect ratio structures into the Si wafer using inductively coupled plasma (ICP) dry etching. A layer of SiO\(_x\) is next deposited with plasma enhanced chemical vapor deposition (PECVD) to smoothen the high aspect ratio silicon nano-pillar morphology and to electrically isolate the Si wafer used for fabrication from the solar cell itself. Next, an optional sputtering step can be performed to obtain a back reflector material on this SiO\(_x\). The highly ordered nano-element electrode architecture is completed by the atomic layer deposition (ALD) of the AZO back contact.
Figure 58: Summary flow of processing steps used for the EBL substrate approach. The sputter step in Stage 5 is optional.

Stage 1: Spinning ZEP and EBL

Figure 59 depicts the result of stage 1 of the EBL substrate method.

Spin ZEP: Starting with a clean 4” Si wafer is obviously vital to ensure no easily avoidable variability is presented in what will ultimately become an intricate sequence of fabrication steps. Wafers were cleaned using a standard acetone/IPA/DI water sequence followed by N₂ drying and a dehydration bake at 180°C for 3 minutes. Next, a ZEP520a:anisole (1:1) solution was
dynamically coated by applying the solution at 900 RPM for ~10 seconds followed by spinning the wafer at 4,000 RPM for 90 seconds. The ZEP was then baked at 180°C for 3 minutes. This gives a ZEP thickness of ~120 nm.

**EBL:** Next, a Vistec EBPG 5200 e-beam lithography writer was used to write a pattern file containing the highly ordered hexagonal geometry desired similar to that shown in Figure 60. Here, L is the spacing of importance corresponding to the modeling results presented in chapter 4 while X and Y are the macroscopic area dimensions the nano-element array will be repeated over. We have demonstrated we can repeat this pattern over large lateral areas of up to 6 mm x 6 mm. Since ZEP is a positive e-beam resist the pink dots in Figure 60 correspond to the areas which will be exposed to the electron beam during the writing and concurrently washed away during the following development. Following a dose array it was determined an optimum beam current of 25 nA and an exposure dose of 260 μC/cm² would be used for the writing.

**Figure 60:** Representative portion of the pattern file written with EBL for the substrate approach. Pink areas represent areas to be exposed by the electron beam
Following the e-beam writing samples were developed for 3 minutes in n-amyl acetate followed by 30 seconds in IPA. Samples were then gently squirted with IPA and dried with N₂.

**Stage 2: EBE of Cr and Liftoff steps**

Figure 61 depicts the result of stage 2 of the EBL substrate method.

**EBE Cr:** The patterned ZEP template was loaded into a Semicore electron beam evaporator on a stationary platform designed for liftoff. The system was pumped down to a base pressure of ~2×10⁻⁶ T and 75 nm of Cr was blanket deposited onto ZEP template at a rate between 1-2 Å/s.

**Liftoff:** Immediately following the evaporation the liftoff was performed by immersing the sample in MicroChem Remover PG [161] heated to 70°C for 10 minutes. The sample was then immersed in a fresh solution of Remover PG heated 70°C for an additional 10 minutes to avoid reticulation of metal flakes to the Si substrate. The sample was then squirted with acetone and IPA, rinsed with DI water, and N₂ dried.

Figure 62 shows an FESEM image of the Cr hard mask following liftoff. Here, the final hexagonal array in Cr corresponding to the exposed area of the pattern file shown in Figure 60 is clearly visible. Although this particular file used a spacing of L=1,250 nm a simple change in the EBL pattern file can afford any number of geometric spacings. We have explored spacings in this hexagonal array ranging from 500-2000 nm. Different spacings will require different
doses during the EBL writing. Larger spacings require larger doses due to less back scattered electron cross talk between adjacent features as a result of these features being further apart.

**Figure 62:** FESEM image of the hexagonal array Cr hard mask with L=1,250 nm on Si wafer

**Stage 3:** ICP dry etching step

Figure 63 depicts the result of stage 3 of the EBL substrate process:

**Figure 63:** Stage 3 of the EBL substrate method

Quite a bit of process optimization was required during this stage in order to obtain the highest aspect ratio Si pillars which we have found through our simulations to be a favorable light trapping architecture as discussed in Chapter 4. The base ICP conditions used for the
etching were a 850W coil bias, 5 mT, 20°C, with 45:5:10 sccm in C$_4$F$_8$:SF$_6$:Ar. Varying chuck biases (100W to 200W) and etch times (180s to 270s) were used in order to maximize the pillar height. Here, a slightly reduced temperature of 20°C is used to slightly reduce the reaction rate on the pillar sidewall in order to further increase anisotropy. The C$_4$F$_8$ is also used to increase anisotropy by sidewall polymerization while a small amount of SF$_6$ and Ar are added to establish the gas chemistry necessary to spark and stabilize a plasma at the low etching pressure of 5 mT. The 850W coil bias serves to form a high density of energetic ions and radicals such that a high etch rate can be obtained. In order to tune the energy of these anisotropic etchant ions the chuck bias can be adjusted. On one end, increasing the chuck bias will increase the energy of the etchant ions and thereby increase bombardment and anisotropic etching. However, in doing this the etch selectivity between the Si and the Cr hard mask will also be reduced, and therefore the ultimate height of the Si nano-pillars is expected to be less when using a higher chuck bias.

Figure 64 shows a key result of the ICP etching optimization study. Here, test samples exposed to varying etching conditions were imaged with the Veeco Icon atomic force microscope (AFM) in PeakForce tapping mode for the sole purpose of measuring the resultant Si nano-pillar heights. It was found a lower chuck bias does indeed afford the maximum possible pillar height as a result of the Cr hard mask surviving longer with the increased etch selectivity resulting from the reduced ion bombardment. The irregular shape of the features shown in Figure 64 are a result of the AFM probe tip having a difficult time tracking such high aspect ratio features spaced closely together. In any event, the purpose of the characterization done in Figure 64 was to obtain the absolute height of the nano-pillars, and the AFM was an effective way to measure the height of sub-micron features for a large array of sample conditions in a timely fashion. As expected, the 175W condition gives a slightly higher pillar height than the 100W
condition when using an etch time of 210 s as a result of the increased bombardment of the Si for the 175W condition. However, by adding an additional 30 s to the etch time for the 175W condition the entire 75 nm Cr hard mask is removed and at that point the fully exposed high surface area Si pillar rapidly etches away. This same 240s etch time at 100W preserves a small portion of the Cr hard mask and affords the highest pillar height of ~500 nm. In an attempt to further increase the nano-pillar height for the 100W condition an additional 30s was added to the etch time (not shown), however this 270s/100W etching condition caused the Cr hard mask to be completely etched away and a result similar to that shown in Figure 63 for the 240s/175W condition was observed. Therefore, an optimum etch time/chuck bias of 240s/100W was established for maximizing the nano-pillar height.

In the event even higher aspect ratio pillars were desired the spin speed of the ZEP could be reduced during stage 1 of this fabrication scheme. With the current ZEP thickness of ~120 nm, the upper bound on the Cr hard mask thickness is ~75 nm, as dictated by the ability to perform liftoff by avoiding the complete coverage of the ZEP sidewalls with Cr. Thicker ZEP layers are conducive to achieving thicker Cr hard masks due to the increased ability to perform liftoff. However, this new ZEP thickness would require an additional dose array during the EBL step. For this reason, we decided to optimize the ICP conditions instead of the EBL conditions owing to an increased ease of process optimization for ICP relative to EBL.
Figure 64: AFM images from the ICP etching optimization study which were used to establish the combination of etch time and chuck bias for maximizing Si nano-pillar heights

Stage 4: PECVD smoothening step

Figure 65 depicts the result of stage 4 of the EBL substrate process.

Figure 65: Stage 4 of the EBL substrate method

During this stage of the processing roughly ~280 nm of SiO_x is deposited onto the Si nano-pillars defined in the previous step. The SiO_x is deposited in an AMAT cluster tool
PECVD at 200°C and 3.5T for 200 sec at a power of 300W and 2000:25 in Ar/SiH₄. The purpose of the PECVD SiOₓ layer is primarily for the sake of geometry modification. The conformal nature of the PECVD SiOₓ will serve to smoothen the topography and make it more conducive to obtaining a conformal coating with a wider variety of deposition techniques. This opens up the opportunity to use sputtering in addition to ALD for the deposition of the subsequent TCO and/or metal electrode layers. In addition, the PECVD grown SiOₓ will electrically isolate the Si substrate the fabrication is performed on from the solar cell itself in order to ensure the substrate does not interfere with or contribute to the solar cell’s performance.

**Stage 5: Sputtering and ALD deposition steps**

Figure 66 depicts the result of stage 5 of the EBL substrate process.

![Figure 66: Stage 5 of the EBL substrate process. Sputtering is optional.](image)

**Sputter Cr:** The sputtering of various materials including Ag, Al, Cr, and ITO onto this topography has been investigated. Not surprisingly, of these materials, only Cr was found to fully and conformally wet the surface of the SiOₓ smoothened Si nano-pillars as a result of Cr’s strong ability to react with the oxygen in SiOₓ and favor layer by layer growth. Aluminum and ITO have intermediate surface coverage while Ag has poor wetting characteristics. It is well known noble metals do not bond well to Si or SiOₓ substrates and as a result island growth is favored for the Ag deposited on the SiOₓ substrate [141]. In order to obtain fully conformal sputtered films of Al or ITO on the topography depicted in Figure 66 additional process
optimization of the sputtering parameters \textit{(i.e.,} temperature, power, and pressure) would be needed. The fully conformal sputtering of Ag is unlikely with these high aspect ratio morphologies. For this reason, our recently developed superstrate approach, which will be discussed in the following chapter, is a much more promising fabrication scheme for employing Ag in conjunction with high aspect ratio electrode architectures.

Typical sputtering parameters, deposition rates, relative step coverage, and binding energies \cite{162} for each of the materials we have deposited using various Kurk J Lesker sputtering systems are shown in Table \ref{tab:material}. Binding energies are shown as they relate to the process power which relates to the plasma density and therefore the energy of the incident metal atoms upon sputtering. It can be hypothesized the reduced plasma density for Cr also serves to increase the average arrival energy of the sputtered Cr atoms as a result of the sputtered Cr atoms having a longer mean free path (MFP) during their transit from the target, through the plasma, and to the substrate. This higher average energy of the Cr atoms upon their arrival to the substrate may allow atoms to migrate to the most energetically favorable position on the substrate, consistent again with the full wetting of Cr experimentally observed.

<table>
<thead>
<tr>
<th>Material</th>
<th>Coverage</th>
<th>Rate (Å/s)</th>
<th>( E_{\text{B}} ) (eV) \cite{142}</th>
<th>Power (W)</th>
<th>Pressure (mT)</th>
<th>Temp (°C)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ag</td>
<td>Poor</td>
<td>4.2</td>
<td>58.3</td>
<td>200</td>
<td>5</td>
<td>18</td>
</tr>
<tr>
<td>Al</td>
<td>Moderate</td>
<td>0.6</td>
<td>72.5</td>
<td>200</td>
<td>5</td>
<td>18</td>
</tr>
<tr>
<td>Cr</td>
<td>Excellent</td>
<td>1.3</td>
<td>42.2</td>
<td>100</td>
<td>5</td>
<td>18</td>
</tr>
<tr>
<td>ITO</td>
<td>Moderate</td>
<td>1.5</td>
<td>73.5 (In)</td>
<td>200</td>
<td>15</td>
<td>300</td>
</tr>
</tbody>
</table>

\textbf{Table 11:} Material characteristics and deposition parameters for various materials sputtered onto the SiO\(_x\) smoothened Si pillars fabricated with the EBL substrate approach

\textbf{ALD AZO:} Following the PECVD of the SiO\(_x\) smoothening layer and the possible sputtering of a back reflector \textit{(i.e.,} Cr) the ALD is used to deposit an AZO optical spacer (or back electrode in
the event no metal is used). For these high aspect ratio topographies the ALD is the ideal deposition tool owing to its ability to conformally deposit defect free films on even the most aggressive topographies. During this step, we typically deposited ~80 nm of AZO at 140°C with a 20:1 ratio of ZnO:Al$_2$O$_3$ cycles for maximizing the conductivity of the AZO, as discussed earlier in this chapter. With these conditions we used 25 supercycles to obtain a thickness of 80 nm. One supercycle consists of 10 ZnO cycles, 1 Al$_2$O$_3$ cycle, and 10 ZnO cycles (i.e. 20:1 ratio). The ALD precursors used were diethyl zinc, trimethyl aluminum, and water. The high volatility of these materials allowed short pulse times of 0.015 sec to be used; however, the relatively low deposition temperature of 140°C requires a 30 sec dwell time after each pulse in order to avoid CVD and obtain fully self-limiting growth characteristics. A constant flow of 20 sccm of N$_2$ was flowing through the chamber, held at a pressure of ~0.6T, throughout the process. At this stage the nano-element electrode structure of the device is completed.

Figure 67 shows a cross sectional focused ion beam (FIB) image illustrating the sample cross section after this final stage of the nano-element electrode processing using the EBL substrate method. On this particular sample ~50 nm of Cr was conformally sputtered followed by the ALD of 80 nm of AZO. The small amount of Cr hard mask remaining on the Si pillars itself can also be seen. Excellent step coverage of the Cr on even a high aspect ratio (~2:1) SiO$_x$ smoothened Si nano-pillar morphology is seen.
Figure 67: Cross sectional FIB image after stage 4 of the processing for the EBL substrate method

Figure 68 illustrates the difficulty of conformally coating a noble metal, such as Ag, onto this topography. Even when using a less aggressive aspect ratio for the SiO$_x$ smoothened Si nano-pillars, such as the roughly 1:1 aspect ratio used in Figure 68, discontinuities are still observed in the sputtered Ag film. This is a large departure from the conformal deposition of Cr observed on the roughly 2:1 aspect ratio nano-pillar morphology which was shown in Figure 67. These breaks in the Ag have the ultimate result of introducing prohibitively high series resistances into the solar cell device which dwarf device performance. The performance of the completed device shown in Figure 68 will next be further assessed and discussed.
Figure 68: Completed nc-Si:H device illustrating the difficulty of conformally sputtering Ag onto the SiOx smoothened Si nano-pillars fabricated with the EBL substrate approach.

A concise listing of the processing steps for the EBL substrate approach is as follows:

1) Clean 4” Si wafer with acetone, IPA, DI, N₂ and bake 180°C for 3 minutes
2) Spin (1:1) ZEP520A:Anisole for 90 sec at 2,500 RPM and bake 180°C for 3 minutes
3) Align samples and expose using nano element pattern file shown with dose of 280 µC/cm², beam current of 12.5 nA, field size of 1 mm x 1 mm, 200 µm aperture, and measure map
4) Develop 3 minutes in n-amyl acetate, 30 seconds IPA, IPA squirt, N₂ dry
5) Blanket deposit 70 nm Cr then liftoff ZEP in 70°C PG remover for 10 minutes
6) ICP etch Si at 5 mT for 240 sec w/ 850W (coil)/100 W (chuck) and 45:5:10 sccm C₄F₈:SF₆:Ar at 20°C
7) PECVD ~280 nm SiOₓ at 200°C and 3.5T for 200 sec with 300W and 2000:25 in Ar/SiH₄
8) Sputter ~50 nm Cr at 18°C and 5T for 385 sec with 100W (optional)
9) Grow AZO (20:1 ratio) at 140°C and ~0.6T using 25 supercycles

The JV performance of a light trapping solar cell based on the EBL substrate approach is shown in Figure 69. The cross section of this device is next to the JV curve. This device used SiF₄ to deposit the nc-Si:H, and this processing adjustment successfully eliminated the defect formation in the nc-Si:H absorber. However, this device had a very poor efficiency of only 1.63% owing to breaks in the sputtered Ag layer leading to a prohibitively high series resistance.
as evidenced by the 24% FF. The $V_{OC}$ and $J_{SC}$ were also poor at 0.52 V and 13.0 mA/cm$^2$ respectively. The virtually horizontal dark JV curve and the slope of the light JV curve at the $V_{OC}$ point both indicate it was a detrimentally high series resistance caused by non-conformal sputtering of the Ag that deteriorated the performance of this device.

![Light and dark JV curves for a light trapping solar cell fabricated with the EBL substrate approach. Cell cross section is shown on right.](image)

**Figure 69:** Light and dark JV curves for a light trapping solar cell fabricated with the EBL substrate approach. Cell cross section is shown on right.

In addition to the poor performance of these cells owing to breaks in the bottom electrode structure, the fabrication of devices made with this method is fairly complex, since each cell requires an electron beam lithography and subsequent dry etching step. This would ultimately result in an increased cost per watt for this type of manufacturing technology. As a result, it was desired to develop a process which could be used to fabricate light trapping architectures in a more manufacturable way. The following section will outline a second fabrication approach which accomplishes this task by utilizing a nano-molding approach.
5.6 Fabrication and characterization of LCCM cells based on the nano-molding approach

Figure 70 shows the summary flow of steps used for fabricating light trapping electrode architectures for solar cells based on the nano-molding approach. The nano-molding approach begins by fabricating a silicon master mold (Si MM) using EBL and ICP etching steps. The increased manufacturability of this process stems from the fact this Si MM requiring EBL and ICP fabrication steps needs only to be created once, and once fabricated it can be used for the construction of many devices. Next, a monolayer of tridecafluoro-1, 1, 2, 2-tetrahydrooctyltrichlorosilane (FOTS) is then coated onto the Si MM to reduce the surface energy such that the subsequently spincasted polyimide (PI) layer can easily be removed from the mastermold following a baking step. This PI template is then used as the template which defines the nano-element topography of the subsequently deposited materials comprising the nano-element electrode structure.

![Figure 70: Summary flow of processing steps used for the nano-molding approach](image)
Stage 1: Spincasting ZEP and EBL

Figure 71 depicts the first step of the nano-molding approach.

**Spin ZEP:** Identical to the initial steps used for the EBL substrate approach this process begins with a cleaned and dehydrated 4” Si wafer. Next, a ZEP520a:anisole (1:1) solution was dynamically coated onto the wafer by applying the solution at 900 RPM for ~10 seconds followed by spinning the wafer at 4,000 RPM for 90 seconds. The ZEP was then baked at 180°C for 3 minutes. This gives a ZEP thickness of ~120 nm.

**EBL:** Once again, the Vistec EBPG 5200 e-beam lithography writer was used to write a pattern file containing the highly ordered hexagonal geometry desired similar to that shown in Figure 60. Following a dose array it was determined an optimum beam current of 12.5 nA and an exposure dose of 280 μC/cm² would be used for the writing. Following the e-beam writing samples were developed for 3 minutes in n-amyl acetate followed by 30 seconds in IPA. Samples were then gently squirted with IPA and dried with N₂.
**Stage 2: ICP etching to define master mold**

Figure 72 depicts stage 2 of the nano-molding approach.

![Diagram of Stage 2: ICP etching to define master mold](image)

**Figure 72:** Stage 2 of the nano-molding approach

During this step the ZEP is used as an etch mask to etch nano cavities into the Si. The Plasma-Therm ICP is used to define these nano cavities which are ~300 nm in diameter at the surface and 320 nm in depth. This is done by etching the sample for 180 seconds at 5 mT in 45:5:10 sccm of C$_4$F$_8$:SF$_6$:Ar at 20°C with 850W (coil)/100W (chuck). Following this etching residual ZEP is removed in a microwave asher by etching for 1 minute in a 100 mT O$_2$ plasma.

Together, stage 1 and stage 2 make the Si MM which can be reused hundreds of times to make hundreds of nano-element electrode light trapping solar cells. This is the primary advantage of the nano-molding approach, since these EBL and ICP steps must be repeated for every substrate (or superstrate) using the previous nano-element fabrication approach.

Similar to the previous approach, the nano-molding approach again offers a high degree of geometric tunability since the dimensions of the Si MM can easily be altered. Modifications to the EBL pattern file used during stage 1 can change the spacing between the nano-cavities, the base diameter, and the geometric arrangement (*e.g.* hexagonal array) and dry etching parameter adjustments during stage 2 can change the height and sidewall angle of the nano-cavities.
Stage 3: FOTS application and spincasting PI

Figure 73 depicts stage 3 of the nano-molding approach.

![Figure 73: Stage 3 of the nano-molding approach](image)

Apply FOTS: In order to reduce the surface energy of the mastermold and allow complete separation of the subsequently coated PI it is first necessary to apply a monolayer of tridecafluoro-1, 1, 2, 2-tetrahydrooctyltrichlorosilane (FOTS) to the surface of the Si MM. The FOTS is applied for 20 minutes in a vacuum desiccator. Exposing the Si MM to three small glass vials, each with 100 μL of FOTS, is sufficient to completely coat a monolayer of the FOTS molecule on the wafer in 20 minutes.

Spin PI: The PI is an extremely viscous material. A ~2” diameter puddle of material is poured onto the surface of the wafer. A 5 second throw off stage at 500 RPM first occurs and then the wafer is spun at 2000 RPM for 90 seconds. The wafer is then baked on a hotplate set to 200°C for 5 minutes, the temperature is then turned up to 300°C and the wafer remains on the hot plate for an additional 55 minutes. This results in a PI film ~35 μm in thickness. This initial baking step removes over 90% of the N-Ethylpyrrolidone (NEP) solvent the PI is suspended in. However, in order to avoid any reflow during subsequent high temperature solar cell deposition steps it is necessary to remove the final ~10% of the NEP. This is difficult to do when the PI is still in contact with the Si MM, so at this point the PI needs to be separated from the Si MM.
Stage 4: Separation

Figure 74 depicts stage 4 of the nano-molding approach.

![Figure 74: Stage 4 of the nano-molding approach](image)

Gently scraping around the entire circumference of the PI coated 4” Si MM with a razorblade will cause the PI film to peel off the Si MM. At this point the PI should be cut to size and mounted using metallic bind clips to a 2x3” glass substrate which has been previously coated with a thin (~10-20 nm) Ag layer. The Ag layer prevents the PI from sticking to the glass support substrate during the subsequent annealing step which will be used to drive out the remaining ~10% of the NEP solvent. The nano-element side should be facing the glass substrate. Finally, glass support slides should be used to stabilize the PI on the glass substrate.

This stack is then loaded into a furnace at room temperature. The furnace is ramped up to 350°C for 1 hour and then held at 350°C for 1 hour prior to slowly cooling to room temperature. No gases are flowing during this step. This treatment serves to make the film stable for the following sputtering and nc-Si:H deposition steps. Once the furnace returns to room temperature the stack is removed and the separation is complete. Figure 75 shows an FESEM image of a completed PI template at this stage in the processing with L=750 nm. This PI substrate had nano-elements with a base diameter of 300 nm and a height of 320 nm. The depiction of the template is shown on the right of the image. A thin 3 nm layer of Ag was sputtered on the template to
prevent charging effects during the FESEM observation. The non-conformal coating of this Ag is the cause of the black spots seen in the image.

![Figure 75: FESEM image of PI template (left) corresponding depiction (right) [142]](image)

**Stage 5**: Ag sputtering and ALD of AZO

Figure 76 depicts the final stage of the nano-molding approach.

![Figure 76: Stage 5 of the nano-molding approach](image)

Here, 5 nm of Cr is first sputtered to promote adhesion and wetting of the metal stack to the PI nano-dome surface. This is followed by the sputtering of 70 nm of Ag and 70 nm of AZO. At
this point the nano-element electrode based on the PI approach is complete and ready for the absorber deposition.

A concise listing of the processing steps used for the fabrication of nano-element electrodes utilizing the nano-molding approach is as follows:

1) Clean and dehydrate a 4” Si wafer
2) Spin ZEP520A for 90 sec at 2,500 RPM and bake 180°C for 3 minutes
3) Expose using pattern file shown in Figure 67 with dose of 280 μC/cm^2, beam current of 12.5 nA
4) ICP etch Si at 5 mT for 180 sec w/ 850W (coil)/100 W (chuck) and 45:5:10 sccm C₄F₈:SF₆:Ar at 20°C
5) Ash Si MM in 100 mT in O₂ plasma for 1 minute
6) Apply TFOS from 3 vials each with 100 μL of FOTS in vacuum dessicator for 20 minutes
7) Pour 2” puddle PI onto center of Si MM. Throw off 500 RPM 5 sec. Spin 2000 RPM 90 sec.
8) Bake 200°C for 5 minutes then 300°C for 55 minutes
9) Separate by scraping around perimeter of Si MM with razorblade. Cut PI to 2x3” rectangle.
10) Mount to 20 nm Ag coated glass slides with binder clips and glass support slides.
11) Place in furnace ramped to 350°C in 1 hour. Hold at 350°C for 1 hour. Remove at RT.
12) Sputter 5 nm Cr/70 nm Ag/70 nm AZO

It should be reiterated at this point the value of the nano-molding approach is that for each solar cell, only stages 3-5 are necessary after stages 1 and 2 have been done once. The FOTS application step in stage 3 also does not need to be repeated for every cell as long as the Si MM used to define the nano-elements remains clean. In the event the Si MM needs cleaned, an O₂ plasma treatment should be used, and following this treatment the FOTS should be reapplied.

The nano-molding approach takes a large step towards increased manufacturability due to largely eliminating EBL and ICP steps and using a flexible polymer substrate which is conducive to high throughput roll to roll and printing technologies. For the cells presented in this thesis, the final nc-Si:H absorber deposition, top ITO deposition, and cell characterization were completed by the group at Swiss. It is important to mention Swiss’s PECVD uses SiH₄, not the ideal SiF₄.

The performances of a light trapping (hereafter nano) solar cell based on the nano-molding approach and the corresponding planar control device are shown in Figure 77. Cross
sectional and 30° tilted FESEM images are both shown next to the JV curve. These devices used a spacing of L=1250 nm. The nominal thickness of the nc-Si:H was 700 nm. Table 12 shows the performance corresponding to each JV curve shown in Figure 77 along with the % change of each of the solar cell electrical parameters (i.e. PCE, V<sub>OC</sub>, J<sub>SC</sub>, and FF) between devices.

**Figure 77:** JV curves for light trapping “Nano” (blue) and “planar” (red) solar cells fabricated on PI substrates with the nano-molding approach shown on right [Adapted from 142]

<table>
<thead>
<tr>
<th>Cell type</th>
<th>PCE</th>
<th>V&lt;sub&gt;OC&lt;/sub&gt; (V)</th>
<th>J&lt;sub&gt;SC&lt;/sub&gt; (mA/cm²)</th>
<th>J&lt;sub&gt;1V&lt;/sub&gt; (mA/cm²)</th>
<th>FF (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Planar</td>
<td>2.64</td>
<td>0.53</td>
<td>14.67</td>
<td>16.5</td>
<td>34.14</td>
</tr>
<tr>
<td>Nano</td>
<td>2.87</td>
<td>0.48</td>
<td>17.84</td>
<td>21.5</td>
<td>33.51</td>
</tr>
<tr>
<td>% Change</td>
<td>8.71</td>
<td>-9.43</td>
<td>21.61</td>
<td>30.3</td>
<td>-1.85</td>
</tr>
</tbody>
</table>

**Table 12:** Comparison in performance between LCCM and planar cell fabricated with the nano-molding approach

Several important conclusions can be drawn from the performance of these devices. These effects will now be discussed in terms of each solar cell parameter.
**J_{SC} and J_{-1V}:** The nano-elements are successfully increasing absorption and thereby raising J_{SC} by close to 22% with respect to the planar device. Due to the poor internal transport characteristics of these devices (*i.e.* low FF and high Rs) the J_{SC} values do not reflect the full potential of the light trapping architecture since there is no external field (*i.e.* V=0) to help extract photogenerated carriers. Therefore, to get a better understanding about the full potential of the nano device architecture we also investigated the change in current density between the devices with an external bias of -1V. In this case the J_{-1V} value was ~30% higher for the nano cell than the planar cell.

**V_{OC}:** The nano-elements are causing defective regions in the nc-Si:H; which was deposited with SiH_{4}/H_{2}. Defects are occurring at the notched areas in the absorber, the origin of these defects was discussed in Figure 51. These defective filaments, which are unique to the nano cell, have the most detrimental effect on V_{OC} as this parameter drops by 9.43%. This suggests the defective regions are primarily hindering performance by acting as recombination centers.

**FF:** The extremely low, but equally poor, FF values for both devices indicates nothing unique is happening in the nano cell to impede transport characteristics. This low FF can be ascribed to the poor quality of the nc-Si:H layers [142]. The very thin top ITO electrode, which appears to be only ~40-50 nm in thickness as viewed from the cross sectional FESEM image, is also a contributor towards this low FF owing to the high series resistance of such a thin TCO layer. The relatively low slopes of both JV curves at their V_{OC} points also indicate a high series resistance was present in both of these devices.

**PCE:** For these devices the pros of increasing the J_{SC} by using a nano-element light trapping architecture outweighed the cons of decreasing V_{OC} caused by the defects in the absorber as the overall device efficiency improved by 8.71%. However, to fully harness the potential of the light
trapping architecture a defect free absorber of higher overall crystalline quality (to increase collection length) and a thicker top TCO layer must be achieved to maintain $V_{OC}$ and FF.

Although the overall device performance for these cells was still fairly low, these PI substrate cells marked a step in the right direction as they successfully proved the light trapping proof of concept simulated in Chapter 4 while using a manufacturable processing technology. The low efficiencies for the devices presented in this chapter are ascribed to detrimentally low FF values resulting from a prohibitively high series resistance due to incomplete coverage of the electrode material on a nano-element material made of an insulating material (i.e. SiO$_2$ coated Si pillars or PI). In the case of the PI cells the use of SiH$_4$ plasma chemistry resulting in defects in the notched areas of the absorber material led to additional efficiency reductions. In the following chapter a most recent fabrication scheme seeking to eliminate all of these issues is presented. This fabrication scheme seeks to create highly ordered nano-element array electrodes on a fully conductive surface such as ITO or Ag. This architecture is expected to illustrate the full potential of light trapping architectures for solar cells since it will eliminate series resistance problems while still being conducive to a defect free nc-Si:H absorber based on the work in this chapter illustrating defect free absorbers when using the SiF$_4$ plasma chemistry. The following chapter will discuss this third fabrication scheme along with an additional fabrication scheme that has been developed based on block copolymer lithography for the potential to transfer this technology to large area manufacturing.
Chapter 6: Additional LCCM Electrode Fabrication Schemes

The performance of the solar cells presented in Chapter 5 served as the motivation for the development of an additional nano-element array fabrication approach. The low FF values for the cells presented in Chapter 5 were clear indicators that these cells were profoundly influenced by electrode conductivity issues. The improvements to $J_{SC}$ resulting from light trapping architectures are only of use if they can be accompanied by reasonable $V_{OC}$ and FF values. Figure 78 depicts the geometric change which will be made to the electrode architecture in order to eliminate the series resistance problem which hindered device performance in the previous chapter. Here, by using a conductive “superhighway” beneath conductive nano-elements the series resistance will be decreased by using a decreased charge carrier diffusion length (L) to reach the external circuit. The following fabrication scheme was developed with this geometry in mind. Here, a highly ordered nano-element array of AZO nano-columns will be fabricated on top of a conducting “superhighway” made of a conducting material such as Ag or ITO.

![Figure 78: Electrode geometry modification to eliminate the series resistance problem](image-url)
6.1 Fabrication of highly ordered nano-element electrodes based on the electron beam lithography superstrate approach

The conformal deposition of certain metals over the high aspect ratio silicon nano-pillars fabricated in the previous chapter has proven to be difficult. This is a result of the line of site character typical of physical vapor deposition tools which are most often used to deposit metals coupled with the shadowing effects introduced by high aspect ratio morphologies. When metals with poor surface wetting characteristics such as Ag are used these effects are manifested as discontinuities in the deposited film. Therefore, if high aspect ratio metal electrodes are desired, a more promising fabrication method will be the following EBL superstrate approach since the nano-element material can be made of the metal itself as opposed to a silicon pillar coated with a thin film of metal. In addition, the superstrate approach allows for the use of a foreign substrate such as glass or a thin foil. In all, a much higher degree of process tunability on the electrode material(s) and substrate type are possible with the EBL superstrate approach.

Figure 79 shows the summary flow of steps used for fabricating high aspect ratio light trapping electrode architectures for solar cells based on the EBL superstrate approach. The superstrate approach begins by patterning a highly conductive back electrode structure (either ITO/AZO or Ag/AZO) on a glass substrate. Standard optical lithography is used to pattern these layers into a bar structure which will be used to define the final active areas of the cells. Next, a stack of layers is coated to form what we refer to as the template. This template consists of a relatively thick liftoff resist (LOR) layer [164] followed by a very thin layer of PECVD grown silicon nitride (SiNx) which is then coated with a layer of ZEP 520a e-beam resist. A thin Au layer is thermally evaporated onto the ZEP 520a to provide a conductive pathway to ground during the EBL writing step. This template is then aligned and exposed to a pattern file.
containing the highly ordered hexagonal array pattern to be written on the active areas of the cells. Following exposure the Au is removed and the exposed ZEP resist is developed. Next, a multi-step ICP dry etching sequence is used to transfer the pattern to the template by etching through the ZEP-SiN$_x$-LOR template. Atomic layer deposition is then used to grow AZO through this template. An ICP is again used to etch away AZO overgrowth and then the template is stripped away in remover PG. Following a final O$_2$ plasma cleaning to remove any residual LOR the nano-element electrode is complete. Here again, the solar cell is completed by using PECVD to deposit the nc-Si:H or a-Si:H containing absorber layers and sputtering to deposit the top ITO contact.

**Figure 79:** Summary flow of processing steps used for the EBL superstrate approach
Stage 1: Planar electrode deposition and patterning

During this stage we worked with two different configurations: Glass/ITO/AZO and Glass/Ag/AZO. The processing details for each of these configurations will be discussed.

**Glass/ITO/AZO:** Figure 80 depicts the result of stage 1 of the EBL superstrate process for the Glass/ITO/AZO configuration. For clarity, all depictions for the EBL superstrate fabrication approach will include top down and profile views of the sample.

![Top down view](image)

**Profile view**

---

**Figure 80:** Stage 1 of the superstrate EBL process for the Glass/ITO/AZO configuration

**Litho 1:** Here, 2x2” ITO coated glass substrates were purchased from Delta Technologies [165]. The ITO thickness is ~200 nm. The substrates were first cleaned by sonicating in acetone and IPA for 20 minutes each, followed by rinsing with DI water and drying. The ITO was patterned into a bar structure, identical to that shown in Figure 30, by using standard optical lithography: Shipley 1813 photoresist [166] was spincasted at 4,000 RPM, exposed to 365 nm UV (i-line) for 6.3 seconds, developed in CD-26 [167] for 55 seconds, and hard baked at 120°C for 10 minutes. The ITO was then patterned by wet etching for 8 minutes in a 3:1 solution of HCl:DI water (9 M
HCl). The photoresist was then removed by immersing in acetone for 5 minutes, IPA for 3 minutes, and thoroughly rinsing with DI water and N₂ drying.

**ALD AZO:** Patterned ITO glass substrates were loaded into a Savannah 200 ALD reactor for the blanket deposition of ~10 nm of AZO. The ALD deposition temperature was 200°C and once again a 20:1 ratio of ZnO:Al₂O₃ cycles was used to maximize the conductivity of the AZO. To obtain a 10 nm film 3 supercycles were used. Once again, one supercycle consists of 10 ZnO cycles, 1 Al₂O₃ cycle, and 10 ZnO cycles (*i.e.* 20:1 ratio). Due to the higher deposition temperature of 200°C (versus 140°C) a shorter dwell time of 10 seconds (versus 30 seconds) could be used after each pulse. A constant flow of 20 sccm of N₂ was flowing through the chamber, held at a pressure of ~0.6T, throughout the process.

**Litho 2:** Using the same conditions as the first lithography process photoresist bars were patterned directly over the previously patterned ITO bars with a simple alignment. The AZO was then wet etched by immersing in a dilute 3:1000 HCl:DI (0.036 M HCl) solution for 1 minute. It is well known the etch rate of AZO is very fast in HCl [168], so high dilutions are required to avoid excessive undercutting during the etching process. The photoresist was then removed with acetone, IPA, and DI water and then dried. This marks the end of stage 1 for the ITO/AZO electrode configuration patterning process. The following section will discuss the processing steps for stage 1 for the Ag/AZO electrode patterning process.

**Glass/Ag/AZO:** Figure 81 depicts the result of stage 1 of the EBL superstrate process for the Glass/Ag/AZO configuration.
**EBE Ag:** To begin the processing glass substrates were cleaned by sonicating for 30 minutes in a 5% Alconox detergent solution in DI water. Next, a Semicore electron beam evaporator pumped down to a base pressure of $\sim 2 \times 10^{-6}$ T was used to blanket deposit a 20 nm Cr adhesion layer followed by a 300 nm layer of Ag.

**ALD AZO:** The same ALD conditions used for the ITO process were used again here to blanket deposit a 10 nm layer of AZO on top of the Ag.

**Litho:** Once again, conventional positive photolithography was done to pattern these Ag/AZO stacks into the same bar structures as those used for the ITO/AZO configuration. Here, Shipley 1827 photoresist [166] was coated at 4,000 RPM, exposed to 365 nm i-line radiation for 10 seconds, developed in CD-26 for 1 minute, and hard baked for 5 minutes at 120°C. The sample was then wet etched by immersing in a 10:1000 HCl:DI (0.12 M HCL) solution for $\sim 50$ seconds. This HCl solution rapidly etches away the 10 nm AZO within the first few seconds and then causes the underlying metal to begin to flake away and peel off the substrate in the unprotected
areas. In order to avoid redeposition of the flaked metal the sample is sonicated in the etchant solution for the final 10 seconds of the etch and then immediately rinsed with DI water. At this point we confirmed the resistivity of the patterned Ag/AZO bar structure was low and on the order of $1 \times 10^{-5}$ $\Omega$ cm.

All of the subsequent processing steps for the EBL superstrate approach for the two different electrode configurations (*i.e.* ITO/AZO and Ag/AZO) were virtually identical, so from this point forward only the schematics based on the ITO configuration will be shown. All additional distinctions in processing between the two different electrode materials will be provided at the end of this section.

**Stage 2**: Template fabrication

Figure 82 depicts the result of stage 2 of the EBL superstrate method.

![Figure 82: Stage 2 of the EBL superstrate method](image)
**Spin LOR:** A 600 nm layer of LOR was first coated on the patterned bar electrode by spincasting LOR 5A at 2,500 RPM for 90 seconds. The LOR was then baked at 265°C for 30 minutes to reflow the film and prevent additional reflow during subsequent processing steps. A Tencor KLA P16+ Profilometer was used to confirm the LOR thickness. The purpose of this relatively thick LOR layer is to provide the majority of the thickness of the template in which the nano-elements will eventually be grown through.

**PECVD SiNx:** A 35 nm layer of SiNx was next deposited onto this LOR. The SiNx is deposited in an AMAT PECVD cluster tool at 165°C and 3.5T for 8 sec at a power of 300W and 2000:100:75 in N2/NH3/SiH4. The purpose of this thin SiNx layer is to serve as a dry etch mask during a future template etching sequence. The high etch selectivity between LOR and SiNx in an O₂ plasma will be employed to dry etch high aspect ratio features through the LOR template.

**Spin ZEP:** A 120 nm layer of ZEP e-beam resist was next coated on the SiNx by spincasting a ZEP520A:anisole (1:1) solution at 4,000 RPM for 90 seconds. The ZEP was then baked at 180°C for 3 minutes. Full wetting of the ZEP on the SiNx surface is difficult as a result of differences in hydrophobicity between the ZEP and the SiNx. In an effort to improve the wetting we attempted adhesion promoters such as OMNICOAT [169] and HMDS [170] in addition to a surfactant dip in SURPASS 4000 [171]. The conclusion of this study was that the wetting of the ZEP on the SiNx was not ideal in any case, and the best wetting of the ZEP with the least process induced contamination was obtained with the control treatment (i.e. coating ZEP directly on SiNx with no adhesion promoter or surfactant dip). This incomplete wetting of the ZEP is illustrated in the top down view in Figure 82. This ZEP layer will serve as the medium in which the pattern file containing the layout of the nano-element array will be written in.
**Evap Au:** A 10 nm Au layer was thermally evaporated onto this LOR/SiN$_x$/ZEP stack using a Kurt J Lesker Lab 18 evaporation system. The purpose of this layer is to provide a conductive pathway to ground in order to avoid charging and subsequent deflection of the electron beam during the e-beam lithography writing.

**Stage 3:** e-beam writing and template dry etching

Figure 83 depicts the result of stage 3 of the EBL superstrate method. As expected, this stage required the largest amount of process optimization.

![Stage 3 of the EBL superstrate method](image)

**Figure 83:** Stage 3 of the EBL superstrate method

**EBL:** A pattern file similar to that seen in Figure 60 was first used to write the nano-element array into the ZEP resist. However, the dose array used to optimize the exposure conditions for the EBL substrate method was not directly transferable to the EBL superstrate method as a result of the substrate type changing from Si to glass. The transparency of the glass substrate caused several issues during the EBL writing as a result of the mapped height being out of range for the glass substrate due to oblique reflections of the laser, which is used to map the height, off of the underlying grooves in the stainless steel sample holder. When such height errors occur the tool
will default to writing the pattern at the same height the previous exposure field was written at. If the writing height is off by too much, the beam will become blurred and the lower exposure energy resulting from this will afford an inadequate dose to clear the thickness of the exposed resist across the beam diameter. For clarification, these effects are depicted in Figure 84.

**Figure 84:** Height errors induced by transparent substrates during EBL writing cause certain exposure fields to be underexposed

To illustrate the manifestation of this problem a completed nano-element array architecture which was victim of this height error is shown in Figure 85. Here, the pale green luster is caused by interference effects resulting from of the nano-elements being spaced on the order of visible light. It is clear even with the naked eye that one of the nine exposure fields for each of the two nano-element electrodes patterned on this sample were written at an inadequate height to fully expose the ZEP within that exposure field. The ultimate result of this is that the entire exposure field written at an inadequate height has no nano-element array since the subsequent processing steps were unable to grow nano-elements through the template in that area as a result of no ZEP being patterned in that exposure field.
In order to circumvent this problem several processing modifications were necessary. First off, the aperture size used for the e-beam writing was decreased from 400 µm to 200 µm to give a larger tolerance for height ranges. In addition, the “measure map” feature was used such that all exposure fields would be written at a single height. In a sense, this was an all or nothing approach since this change would either cause all of the exposure fields to be written at an adequate height or none of the fields to be written at an adequate height. In order to maximize the chance this modification would write all of the exposure fields at an adequate height the back of the substrate was colored with a black sharpie marker over the entire exposure area in order to make the sample effectively opaque and avoid errors induced by the grooved sample holder. The culmination of these processing modifications successfully eliminated the height error problem and allowed us to obtain uniform nano-elements over the entire writing area on a transparent substrate. For the final e-beam writing we used a pattern file containing two nano-element
spacings of 1,000 nm and 1,200 nm in a hexagonal array to be written over two 3 mm x 3 mm areas aligned to the underlying patterned bar electrodes as illustrated in Figure 86. For the writing the optimized exposure dose was 280 $\mu$C/cm$^2$, the beam current was 12.5 nA, the exposure field size was 1 mm x 1 mm with the measure map feature, and the aperture size was 200 $\mu$m. The total writing time was less than 45 minutes.

![Diagram](image)

**Figure 86:** Depiction of the pattern file used for the EBL superstrate approach

Following the writing the black marker on the sample backside was first removed with an IPA swab. The Au was next removed by immersing the sample in KI/I$_2$ Au etchant [172] followed by a DI water rinse. The ZEP was developed by immersing in n-amyl acetate for 3 minutes followed by a 30 sec immersion in IPA and N$_2$ drying. At this point the nano-element pattern has been transferred into the ZEP resist. The next stage of processing uses the ICP to further transfer this nano-element pattern into the underlying SiN$_x$ and LOR layers.
**ICP template etching:** The second portion of stage 3 of the EBL superstrate method involves ICP dry etching through the template. Figure 87 illustrates the sample immediately after the EBL step (left) and then again after the completion of the ICP etching sequence through the template (right).

![ICP template etching diagram](image)

**Figure 87:** Depiction of the result of the ICP etching step of stage 3

A two-step dry etching process is required to etch through the template. First the SiN$_x$ is etched through the pattern defined in the ZEP and then the LOR is etched through the pattern defined in the SiN$_x$. A Plasma-Therm Versalock 700 ICP was used for these etching steps.

**SiN$_x$ etching:** A short etch time is required to etch through the SiN$_x$ in the opened (i.e. exposed) areas of the ZEP but preserve some of the ZEP in the unexposed areas such that the nano-element array pattern can be transferred to the SiN$_x$. This is the reason a relatively thin (~35 nm) layer of SiN$_x$ was chosen for the template. Completely etching through the SiN$_x$ was found to take ~10 seconds with the etching conditions used, so to ensure full removal and no residue a 14
second etch was used. It was confirmed over 75% of the ZEP still remained at this point. The process parameters for this step are shown in Table 10.

**LOR etching:** The high etch selectivity between organic materials (LOR and ZEP) and inorganic materials (SiNₓ) in an O₂ plasma allows the SiNₓ pattern defined in the previous etching step to serve as a hard mask while dry etching through the entire thickness of the LOR template. Completely etching through the LOR was found to take ~60 seconds with the process used, so to ensure full removal and no residue a 90 second etch was used. During this time, the ZEP is also fully removed and the underlying SiNₓ serves as an etch stop to preserve the pattern. It was confirmed over 90% of the SiNₓ still remained at this point. The process parameters for this step are also shown in Table 13. For both etches the chuck power was kept at 0W since the reduced selectivity from enhanced bombardment was not desired. At this point a high aspect ratio template has been defined.

<table>
<thead>
<tr>
<th>Order</th>
<th>Material(s) etched</th>
<th>Etch mask</th>
<th>Etch time (sec)</th>
<th>Coil Power (W)</th>
<th>Pressure (mT)</th>
<th>Chemistry</th>
<th>DC Bias (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1st</td>
<td>SiNₓ</td>
<td>ZEP</td>
<td>14</td>
<td>300</td>
<td>30</td>
<td>45 sccm CF₄</td>
<td>~710</td>
</tr>
<tr>
<td></td>
<td>LOR and ZEP</td>
<td>SiNₓ</td>
<td>90</td>
<td>500</td>
<td>10</td>
<td>45 sccm O₂</td>
<td>~990</td>
</tr>
</tbody>
</table>

**Table 13:** ICP dry etching parameters for SiNₓ and LOR during the EBL superstrate approach

**Stage 4:** ALD growth through template

Figure 88 depicts the result of stage 4 of the EBL superstrate method. In this stage the high aspect ratio pores defined in the template during the previous dry etching step are used to define the geometry of the AZO nano-columns which will ultimately serve as the light trapping architecture for this solar cell.
Figure 88: Stage 4 of the EBL superstrate method

As it was discussed in Chapter 3 for the ALD grown NiO we have found a chamber conditioning process is valuable in obtaining an ALD grown material with maximum integrity. Therefore, for this step the ALD chamber was first conditioned with a thin ~10 nm layer of AZO by using 3 supercycles at 175°C with the standard 20:1 ratio of ZnO:Al₂O₃ cycles. Following the chamber conditioning the AZO was then grown through the template using 30 supercycles at 175°C with this same 20:1 ratio and a 30 sec dwell time following each pulse.

**Stage 5: AZO overgrowth etching, template removal, and final cleaning**

Figure 89 depicts the 5th and final stage of the EBL superstrate method in which the AZO overgrowth and the remaining SiNx hard mask are first dry etched away in a ULVAC NE-550 ICP and then the remaining LOR template is stripped. Following a final cleaning process of the AZO around the perimeter of the sample and descumming residual LOR the process is complete.
**ICP:** The AZO overgrowth etching requires careful process optimization since by this point the sample has already been through a large amount of processing. Extra precaution has to be taken during this step since an excessive etch of the AZO overgrowth could easily etch away the entire template. The etch rates of SiNₓ and AZO in the ULVAC ICP were individually confirmed to be ~24 Å/s and ~20 Å/s respectively when using the optimized process conditions of 1200W chuck/150W coil at 5 mT in 30 sccm BCl₃. These parameters induced a DC bias of ~200V. A control planar sample with an equivalent layer stack was first etched before etching the sample which had been through all of the processing. Here, it was found that the room temperature etching used for this process optimization led to a problem with the film bubbling due to insufficient backside cooling. In order to circumvent this problem, the sample was etched in 10 second intervals. Eight 10 second intervals were required to fully remove the AZO overgrowth and remaining SiNₓ dry etch mask. For future work etch rates should be optimized for a lower etch temperature so a single etch can be used to etch the entire AZO overgrowth/SiNₓ stack.

![Diagram](image-url)

**Figure 89:** Stage 5 of the EBL superstrate method
**LOR strip:** Immediately following ICP dry etching of the AZO overgrowth samples were immersed in a solution of Remover PG heated to a probed temperature of 65°C for 20 minutes. Samples were then carefully squirted with acetone beginning at the corner of the glass substrate and flowing the acetone towards the center to avoid any potential damage to the nano-element areas which could be caused by directly squirting the nano-element areas while they were still hot from the PG immersion. Next, samples were placed in a fresh solution of 65°C Remover PG for an additional 20 minutes. The careful acetone squirt was repeated, followed by an IPA squirt, DI rinse, and N₂ dry.

**Final cleaning:** To avoid short circuits and shunt paths in the completed solar cell devices it was necessary to remove the unwanted AZO around the substrate perimeter at this point. This unwanted AZO was a manifestation of the ZEP not fully wetting the SiNx in stage 2. This was done by dipping a q-tip in a 10% HCl solution in DI water and very carefully scrubbing away the AZO in these areas. Images of an actual sample before and after this step are shown in Figure 90. Extreme precaution has to be taken during this step since the AZO nano-elements toward the center of the sample are equally susceptible to being etched by this chemistry. By using a diluted HCl solution the possibility of any HCl vapor from the q-tip traveling to the active areas and etching away the AZO nano-columns is eliminated. The remaining AZO seen around the outermost perimeter of the sample following the cleaning is AZO on the backside of the sample and therefore not of concern to the final device fabrication steps.
The following FESEM observation of the active (nano) area of the sample shown on the right hand side of Figure 90 showed there was still residual LOR present in these areas at this point. This LOR was removed using a final ashing treatment in the Versalock ICP. Figure 91 shows FESEM images illustrating how this LOR was removed by using a 15 second etch with 500W (coil)/200W (chuck) at a pressure of 30 mT and 45 sccm of O\textsubscript{2}. The induced DC bias for these conditions was \sim 560V.

<table>
<thead>
<tr>
<th>Before Final ICP O\textsubscript{2} cleaning</th>
<th>After Final ICP O\textsubscript{2} cleaning</th>
</tr>
</thead>
<tbody>
<tr>
<td><img src="image1.png" alt="Before" /></td>
<td><img src="image2.png" alt="After" /></td>
</tr>
</tbody>
</table>

**Figure 91:** Final ashing treatment to remove residual LOR
At this point the nano-element electrode fabrication is completed. Images of the completed samples illustrating the 3 mm x 3 mm nano-element arrays with both 1,000 nm spacing (in the 12:00 position) and 1,200 nm spacing (in the 3:00 position) on both ITO (left) and Ag (right) are shown in Figure 92. An FESEM image of the AZO nano-elements on ITO is shown in Figure 93. Imaging showed the final nano-element diameter was ~150 nm, the spacings defined with EBL were well maintained at 1,000 nm and 1,200 nm, and the height of the AZO columns was similar to the thickness of the LOR template at ~550 nm (not shown).

<table>
<thead>
<tr>
<th>ITO with AZO nano-elements</th>
<th>Ag with AZO nano-elements</th>
</tr>
</thead>
</table>

**Figure 92:** Images of completed AZO nano-element electrodes on ITO and Ag fabricated with the EBL superstrate approach

All processing differences between the ITO electrode and the Ag electrode are shown in Table 14. All other processing was done identically. The Ag sample was processed first. Careful observation of Figure 92 shows a small amount of exposure fields did not have the appropriate dose on the 1200 nm spacing nano-element electrode for the Ag sample. This was again a result of the height errors during the EBL step. This problem was solved for the ITO electrode sample. Future work should use the EBL condition used for the ITO for both electrode materials.
Figure 93: FESEM image of AZO nano-element array on ITO

<table>
<thead>
<tr>
<th>Electrode</th>
<th>Stage 1</th>
<th>Stage 2</th>
<th>Stage 3</th>
<th>Stage 4</th>
<th>Stage 5</th>
</tr>
</thead>
<tbody>
<tr>
<td>ITO</td>
<td>2x Optical Litho</td>
<td>LOR is 600 nm</td>
<td>Black marker/measure map/200 μm aperture/1 mm x 1mm fields</td>
<td>All identical</td>
<td>All identical</td>
</tr>
<tr>
<td>Ag</td>
<td>1x Optical Litho</td>
<td>LOR is 500 nm</td>
<td>No black marker/no measure map/400 μm aperture/1024 μm x 1024 μm fields</td>
<td>All identical</td>
<td>All identical</td>
</tr>
</tbody>
</table>

Table 14: Summary of differences in processing between ITO and Ag electrodes during the EBL superstrate method

The light trapping nano-columns made during this thesis work were composed of AZO. However, it should be emphasized that this superstrate EBL nano-element fabrication approach is also conducive to making highly ordered nano-columns with highly tunable dimensions out of a variety of other materials. For example, instead of growing ALD AZO through the template a plethora of other ALD available materials (e.g. Al₂O₃, HfO₂, TiO₂, etc.) could be chosen to suit other device applications. Alternatively, electroplating could be used to grow a wide variety of metals through the template (e.g. Ag, Au, Ni, etc.). The work in chapter 3 suggests NiO columns would also be possible by electroplating Ni and then thermally oxidizing these Ni columns.
A concise listing of the processing steps for the EBL superstrate approach is as follows:

1) Clean and pattern glass with Ag/AZO or ITO/AZO using photolithography and wet etching
2) Spin LOR5A for 90 sec at 2,500 RPM and bake 265°C for 30 minutes
3) PECVD ~35 nm SiNx at 165°C, 3.5T, 300W for 14 sec and 2000:100:75 sccm N2/NH3/SiH4
4) Spin (1:1) ZEP520A:anisole for 90 sec at 2,500 RPM and bake 180°C for 3 minutes
5) Thermally evaporate 10 nm of Au
6) Color backside of glass substrate with black sharpie marker over active areas to be written
7) Align samples and expose using pattern file shown in Figure 67 with dose of 280 μC/cm², beam current of 12.5 nA, field size of 1 mm x 1 mm, 200 μm aperture, and measure map
8) Remove black sharpie marker on backside with IPA swab, N2 dry
9) Etch Au by immersing in Au etchant for 1 minute, DI rinse, N2 dry
10) Develop 3 minutes in n-amyl acetate, 30 sec IPA immersion, IPA squirt, N2 dry
11) ICP etch SiNx at 30 mT for 14 sec w/ 300W (coil)/0W (chuck) and 45:5 sccm CF4:O2 at 20°C
12) ICP etch LOR at 10 mT for 90 sec w/ 500 W (coil)/0 W (chuck) and 45 sccm O2 at 20°C
13) Condition ALD chamber with AZO (20:1 ratio) at 175°C and ~0.6T using 3 supercycles
14) Grow AZO through template (20:1 ratio) at 175°C and ~0.6T using 30 supercycles
15) ICP etch AZO/SiNx at 5 mT for 10 sec w/ 1200W (coil)/150W (chuck) and 30 sccm BCl3.
16) Repeat step 15 seven additional times (8x10 sec=80 sec total etching)
17) Immerse in fresh 65°C PG remover for 20 minutes, careful acetone/IPA squirt, N2 dry
18) Repeat step 17 one additional time
19) Remove extra AZO on front side with 10% HCl on q-tip, careful DI rinse, N2 dry
20) ICP etch LOR residue at 30 mT for 15 sec with 400W (coil)/200W (chuck) and 45 sccm O2.

The list of steps above, coupled with all of the processing considerations discussed in this section, elucidates the fact this fabrication method is very complex. This method requires a large variety of nanofabrication tools and equipment to produce a single architecture: optical lithography and electron beam lithography, electron beam evaporation and thermal evaporation, PECVD and ALD, and multiple ICP dry etching systems. In addition, a variety of photoresists, solvents, and various other chemicals are also required. Despite this complexity, some research level tricks are also still necessary such as coloring the backside of the sample with a black marker and using a HCl q-tip to wipe away excess material. This all hints that a more manufacturable approach for such structures is highly desirable for mass manufacture and reasonable throughput. In the following section our efforts towards creating these nanoelement light trapping architectures in more manufacturable way will be discussed.
6.2 Fabrication of highly ordered nano-element electrodes based on the block copolymer approach

In many ways the block copolymer (BCP) approach is analogous to the EBL superstrate approach presented in the previous section. The primary distinction between these methods is that the ordered nano-scale phase separation characteristic of BCP materials is used to define the nano-elements instead of electron beam lithography. A block copolymer contains two polymer chains which are chemically different from each other and held together by a covalent bond at one end. These materials can self assemble into well-ordered domains over molecular length scales as a result of the tendency for the chemically dissimilar chains to phase separate and the imposed constraint of chain connectivity [173]. Further, the competition between these chain stretching energies and the interfacial energy imposed by the substrate will dictate the phase separation characteristics upon this material reaching equilibrium. By varying the relative volume fractions of the two chemical blocks the types of periodic micro-domains (e.g. spheres, cylinders, and lamellae) can be varied. Since these chemical blocks are mixed and casted onto the substrate in an appropriate solvent this allows for solution based processing to obtain nano-element architectures when using block copolymers in place of the far more complex electron beam lithography approaches. This has clear implications on throughput and ease of processing.

Figure 94 shows the summary flow of steps used for fabricating light trapping electrode architectures for solar cells based on the block copolymer approach. This approach once again begins by patterning a back electrode bar structure with ITO and AZO on a glass substrate with standard optical lithography. Next, a template is created by spin casting a liftoff resist (LOR) layer followed by a randomization polymer (rMat) layer and lastly a block copolymer (P722) layer. This P722 is composed of polystyrene-\(b\)-poly(methyl methacrylate) (PS-\(b\)-PMMA) blocks.
which phase separate into cylinders of PMMA in a PS matrix upon an annealing treatment with the proper processing conditions (\textit{i.e.} weight \%, solvent, thickness, and annealing conditions). Next, an RuCl$_3$ exposure selectively stains the PS matrix with RuO$_4$ and thereby further increases its etch resistance relative to the PMMA cylinders in an O$_2$ plasma. This allows the following reactive ion etching (RIE) dry etching step to drill through the ordered PMMA cylinder matrix of the template using the RuO$_4$ stained PS as a pseudo hard mask. This transfers the nano-scale phase separation of the BCP through the thickness of the LOR template. The ALD is once again used to grow AZO through this template. The ICP is again used to etch the AZO overgrowth and then the residual LOR and BCP materials comprising the template are lastly removed using an O$_2$ RIE treatment.

\textbf{Figure 94:} Summary flow of processing steps used for the block-copolymer approach
Stage 1: Patterning ITO/AZO bar structures

Figure 95 depicts stage 1 of the block copolymer approach

This patterning was done identically to that discussed for Stage 1 of the EBL superstrate approach for the ITO. Put succinctly: pattern the 200 nm of ITO by etching in 9M HCl for 8 minutes and then pattern the ALD deposited 10 nm of AZO directly on top of the patterned ITO using a lithography alignment and wet etching in 0.036 M HCl for 1 minute.

Stage 2: Spin cast template layers

Figure 96 depicts stage 2 of the block copolymer approach.
**Spin LOR:** A layer of LOR2A is spun at 5,000 RPM for 60 seconds and baked at 200°C for 30 minutes. Analogous to the EBL superstrate approach, the purpose of this LOR layer is to provide the bulk of the template thickness which the AZO will eventually be grown through. These conditions give an LOR layer which is ~200 nm thick.

**Spin rMat:** A 0.3 wt% rMat solution (HEMA) [174] in toluene is cast on the LOR at 500 RPM for 60 seconds and baked at 265°C for 30 minutes. This layer serves to randomize the surface and greatly improves the subsequent phase separation of the BCP which will be cast on top of it. The thickness of the rMat layer is ~30 nm. This step should ideally be performed in a nitrogen purged glove box due to the sensitivity of these materials to oxygen.

**Spin P722:** A 1.0 wt% P722 (PS-b-PMMA) [174] BCP solution in toluene is casted on top of the rMat layer at 6,000 RPM for 60 seconds. This gives a layer of P722 which is ~40 nm thick.

**Stage 3:** Phase separation and polystyrene staining

Figure 97 depicts stage 3 of the block copolymer approach.

![Figure 97: Stage 3 of the block copolymer approach](image)

**Anneal:** The phase separation between the PS and PMMA components occurs during an overnight annealing treatment in a vacuum oven at 170°C. The thickness of the BCP has a critical influence on the success of phase separation [175]. Work done in this thesis investigating various spin speeds for the BCP layer found slightly thicker (~40 nm) films have better phase
separation characteristics than thinner (~25 nm) films as a result of more the cylinders being oriented perpendicular to the surface as shown in Figure 98.

**Figure 98:** Thickness of BCP layer has critical influence on phase separation

**RuO₄ stain PS:** The PS is selectively stained with RuO₄ by mixing 0.100 g of RuCl₃ [176] with 5 mL of sodium hypochlorite in a small glass vial. A stir bar is placed in this vial and samples are taped to the lid of a staining chamber along with the stirring solution in the glass vial. Samples are stained for 30 minutes. The purpose of the RuO₄ staining process is to greatly enhance the etch resistance of the PS relative to the PMMA in the subsequent dry etching step. The RuO₄ stained PS is the lighter color (higher Z) matrix material shown in Figure 98.

**Stage 4:** Etch through template and grow AZO through etched pores

Figure 99 depicts stage 4 of the block copolymer approach.
**RIE:** The PMMA and underlying LOR layer are etched in a Plasma-Therm 720 RIE system at 500W and 10 mT with 45 sccm in O\(_2\). Careful optimization of the etch time was required for this step since the RuO\(_4\) stained PS is not an ideally strong etch mask. Therefore, etching too long will etch the entire matrix while etching too short will be insufficient for drilling through the entire LOR template. By etching a series of test samples for different times and then performing a deposition and liftoff the following FESEM observation showed that 30s was an ideal etch time. To be safe and ensure full removal of templates which could vary slightly in thickness a 35 second etch time was used for the fully optimized process.

**ALD AZO:** The Savannah 200 ALD system is used to deposit AZO at 160°C with 4 supercycles and a 60:1 ratio of ZnO:Al\(_2\)O\(_3\) cycles. Alternatively, a 20:1 ratio of ZnO:Al\(_2\)O\(_3\) could also be used with 12 supercycles if seeking a higher conductivity film. As it has been discussed in the previous chapter, tuning of the doping ratio of the ALD grown AZO is an easy way to make improvements to the electrical conductivity of the nano-element electrode material.

**Stage 5:** Etching of AZO overgrowth and template removal

Figure 100 depicts stage 5 of the block copolymer approach.
**ICP:** The Tegal 6500 ICP is used to dry etch the AZO overgrowth using two consecutive 20 second etches in a BCl$_3$ plasma at a pressure of 2 mT and a power of 500W. Again, the use of multiple etches is to avoid AZO bubbling induced by insufficient backside cooling during longer etch intervals.

**RIE:** The Plasma Therm 720 RIE is again used to etch the remaining LOR2A template using the same recipe as that used to etch PMMA and LOR in stage 3: 500W at 10 mT with 45 sccm O$_2$. After some optimization it was found 90 seconds was the ideal etch time for this step. This marks the completion of the fabrication of ordered AZO nano-pillars fabricated with the BCP approach.

A concise listing of the processing steps for the block copolymer approach is as follows:

1) Clean and pattern glass with ITO/AZO using photolithography and wet etching
2) Spin LOR2A for 60 sec at 5,000 RPM and bake 200°C for 30 minutes
3) Spin 0.3 wt% rMat (HEMA) in toluene for 60 sec at 500 RPM and bake 265°C for 30 minutes
4) Spin 1.0 wt% P722 in toluene for 60 sec at 6,000 RPM
5) Anneal overnight in vacuum oven at 170°C
6) RuO$_4$ stain by immersing in staining chamber with 0.100 g RuCl$_3$ in 5 mL of sodium hypochlorite
7) RIE etch PMMA and LOR at 10 mT for 35 sec w/ 500W and 45 sccm O$_2$ at 20°C
8) Grow AZO through template (60:1 ratio) at 160°C and ~0.6T using 4 supercycles
9) ICP etch AZO at 2 mT for 20 sec w/ 500 W and 30 sccm BCl$_3$ at 20°C
10) Repeat step 9 one additional time (2x20 sec=40 sec total etching)
11) RIE etch remaining PS and LOR at 10 mT for 90 sec w/ 500W and 45 sccm O$_2$ at 20°C
The biggest advantage to this BCP approach is that these nano-elements can be fabricated over extremely large areas dictated only by the size of the substrate. This allows laboratory scale devices based on this approach to be much more easily scaled up to the production scale relative to the nano-elements fabricated with the direct write EBL approach. It is important to note that the phase separation length characteristic of BCP materials needs to match the L spacing required to obtain the \(L=L_{\text{touch}}\) condition for the necessitated thickness of nc-Si:H to absorb adequate light. The typically small L spacings fabricated with the BCP approach (<200 nm) combined with the thickness of nc-Si:H necessary to absorb sufficient light would result in the condition \(L<<L_{\text{touch}}\), and therefore a virtually planar nc-Si:H architecture would result as discussed in Chapter 4 and illustrated in Figure 42. As it has been discussed, the nano-dome morphology of the nc-Si:H is a key attribute to its light trapping. Although there is some degree of tuning the characteristic phase separation length of BCP materials from anywhere from ~30 nm to greater than 180 nm by varying the molecular weight of the BCP [177] this entire range is still on the low end for the required thickness of nc-Si:H. Therefore, the BCP fabricated nano-element architecture is primarily of interest for more strongly absorbing (i.e. thinner) and weekly collecting absorber materials such as a-Si:H and organic absorbers such as the P3HT:PCBM bulk heterojunction architecture.
Chapter 7: Conclusions and Perspective

The seemingly inevitable tradeoff between reducing the thickness of a solar cell and fully harnessing all of the available sunlight can be overcome by a well-designed device architecture. Such architectures can employ both transport layers and/or light trapping arrays. In this thesis, the successful incorporation of both transport layers (NiO with CdTe) and light trapping arrays (LCCM architecture with nc-Si:H on PI substrate) have been independently demonstrated.

Transport layers based on ALD grown NiO offer great promise owing to their optimum performance occurring at a very low thickness (~4 nm). Since ALD is a low temperature and self-limiting surface growth process very large substrates can be uniformly coated and realistically the only limit on throughput is the size of the chamber. Roll to roll processing lines employing alternating exposures to ALD precursors is also possible. Therefore, the improvements shown to result for CdTe cells as a result of ALD NiO are scalable to high throughput technologies.

Numerical modeling has served to provide guidance on optimizing the geometries of light trapping architectures. The two most significant geometric variables in accordance to the HFSS simulations are the thickness of the absorber (t) and spacing between the elements (L) composing a highly ordered hexagonal array. The combination of t and L which afford nano-domes slightly above the L=\text{L}_{\text{touch}} condition has been found to maximize absorption and therefore J_{\text{SC}}.

To make these highly ordered hexagonal nano-element arrays various fabrication approaches have been developed. These approaches range greatly in scalability, complexity, geometric tunability, and material options. Approaches based on electron beam lithography offer the greatest control on tunability but will be more difficult to scale up; these methods can also be slow and complex. The nano-molding approach greatly increases throughput by employing only
a single electron beam lithography step to fabricate many dozens of devices. However, this approach is limited to substrate material types which can be molded and separated from a silicon mastermold such as polyimide. Such materials possess far from adequate transmittance and conductivity, so their sole purpose is for geometric modification. A block copolymer approach has also been developed. This approach is the most scalable to large area devices, however, the maximum possible length scale (L spacing) produced by this method is not conducive to the required thickness of the nc-Si:H absorber material which is of interest in this thesis. This method could be promising for more strongly absorbing materials in which a thinner absorber layer is permissible such as a-Si:H.

The fabrication of modeled device architectures led to unforeseen process induced defects in the nc-Si:H as a result of shadowing effects caused by the nano-elements. These defects were overcome by changing the PECVD gas chemistry from SiH₄/H₂ to SiF₄/H₂/Ar in order to exploit the high etch selectivity at low temperatures between defective and porous a-Si:H tissue and nc-Si:H.

Completed devices built on PI nano-element arrays successfully demonstrated light trapping by increasing J_{SC} by ~22%. However, this nano-element array also induced defects in the SiH₄ deposited nc-Si:H causing a 9.4% reduction V_{OC}, and this resulted in the overall device efficiency going up by 8.7% relative to the planar control structure. A low FF in both devices indicates higher quality nc-Si:H is needed for a high performance and lightweight device. The first step towards a higher quality nc-Si:H absorber is the elimination of topography induced defects. This was accomplished by changing the PECVD gas chemistry to SiF₄/H₂/Ar. Defect free absorbers were deposited onto nano-element array architectures susceptible to shadowing
effects. However, all devices built based on these architectures suffered series resistances which were too high to give reasonable efficiencies as a result of excessively low FF values.

The merger of a light trapping nano-element array architecture and a NiO HT/EBL would be the ultimate end goal of this thesis work. Here, $J_{SC}$ enhancements provided by the light trapping architectures could be complimented by $V_{OC}$ and FF enhancements provided by the NiO. These effects have been demonstrated independently, but in order to fabricate a lightweight and flexible high performance nc-Si:H solar cell both of these techniques should be employed simultaneously on a single device. Figure 101 depicts an idealized completed device employing both a transport layer and a light trapping architecture. This device would be fabricated with the nano-molding approach. Fabrication would begin with the creation of a PI template with an L spacing of ~1,200 nm and 1:1 aspect ratio PI domes. Next, a conformal 70 nm Ag/70 nm AZO back electrode would be sputtered followed by the ALD of a ~4 nm layer of NiO. The SiF$_4$/H$_2$/Ar PECVD gas chemistry would then be used to deposit ~700 nm of nc-Si:H. The sputtering of an 80 nm thick ITO top electrode would complete the device.

**Figure 101:** Cross section of an idealized device employing both a transport layer and a light trapping architecture
There is no reason to believe such a device could not be fabricated. In order to make this
device flexible and conducive to high throughput technologies the nano-molding approach would
be the proper approach to pursue. The low deposition temperatures permissible for the
sputtering of Ag and AZO, the ALD growth of NiO, and the PECVD of nc-Si:H with SiF₄ would
allow the PI substrate to be conducive to these layer depositions in terms of its temperature
tolerance. The ITO can also be sputtered in this low temperature range, however, the ideal
combination of electrical conductivity and transparency of the ITO may no longer be obtainable
at these relatively low (<300°C) temperature ranges [178]. Although this process may be
conducive to the temperature tolerance of PI there are still some concerns when working with
such thin (<50 μm) substrates pertaining to stress and handling. Such thin substrates are highly
susceptible to folding to relieve stresses resulting from layer depositions. Therefore, additional
process and fabrication approach optimization would be necessary to fully construct devices such
as that shown in Figure 101. One possible method to avoid these stresses associated with thin PI
substrates would be to transfer this process to a NaCl coated substrate. If the PI and subsequent
layers could be processed on a NaCl coated substrate of adequate thickness to provide
mechanical support (e.g. glass or Si) such stresses leading to film folding associated with film
depositions could be circumvented. In addition, handling would be much easier, as thin films
with no mechanical support substrate are highly susceptible to cracking if not handled extremely
carefully. Then, once all layer depositions are completed the flexible and thin film solar cell can
be lifted off the mechanical support substrate by immersing in DI water to dissolve the NaCl.

In the event these stresses were fully prohibitive and could not successfully be transferred
to a mechanical support substrate the EBL superstrate approach presented at the beginning of this
chapter could instead be used at the expense of reduced manufacturability. With this approach
NiO columns could be an interesting alternative to AZO columns owing to the possibility of heavily doping this material p-type such that it could be used a hole collecting electrode. Such columns could be achievable by electroplating Ni through the template and subsequently oxidizing it to NiO or by directly growing ALD NiO through the template.

In all, the sun provides enough energy in ~6 hours to fulfill all of our annual energy consumption demands. To take advantage of a larger portion of this energy will require a reduction in the cost of this type of energy conversion. Although conventional Si solar cells currently dominate the market, there is little room left for growth and innovation for this well-established technology. Reducing the cost per watt will ultimately require a reduction in both the fabrication costs and the installation costs. To achieve these goals simultaneously will require the fabrication of thinner cells using less material (reduced fabrication costs) which are lighter such that they can be more easily installed (reduced installation costs). This thesis has provided strides towards the fabrication of lightweight and flexible nc-Si:H solar cells by successfully demonstrating the use of both transport layers and light trapping architectures for improving the efficiency of thin film solar cells. Further optimization of the processes developed in this thesis has the potential to make solar technology a more prominent energy resource.
References

CHAPTER 1:


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CHAPTER 7:

VITA

Zachary R. Gray was born in Delaware County, Pennsylvania in 1985. After graduating from Garden Spot High School in 2003 he briefly attended Penn State Berks for Computer Science and Engineering. After 1 year at Penn State Berks he decided to enlist in the Navy, where he was accepted as a Nuclear Engineer. While waiting for his departure he obtained employment at a retail company. At this point he began taking classes at Reading Area Community College (RACC) in 2005 and decided to pursue a degree program in Nanofabrication Manufacturing Technology (NMT) instead of joining the Navy. He graduated with an A.A.S. degree from RACC in 2007. He then worked for three years as a process technician at a small State College PA based R&D Company called Solarity. He funded himself through his undergraduate study in Materials Science and Engineering at Penn State University Park where he received his B.S. degree in 2011. He then worked full time for Penn State University in State College PA for 2 years as the Lab Coordinator for the NMT program that he went through himself as a student in 2007. In 2013 he began graduate school in the intercollege of Materials Science and Engineering. Throughout his graduate study he has continued working with the NMT program and has sought to integrate additional nanofabrication knowledge learned throughout his graduate school study into the curriculum of the NMT program in order to increase the knowledge base and level of understanding gained by students taking the NMT program.

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