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**TWO-DIMENSIONAL MATERIALS FOR NOVEL ELECTRONIC APPLICATIONS:
THE GRAPHENE MIXER AND TaS₂ HYPER-FET**

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by

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Abstract

First successfully isolated in 2004, graphene is a two-dimensional crystal comprised of a one-atom thick layer of carbon atoms arranged in a honeycomb lattice. Initial demonstrations of the exceptional material and electronic properties of graphene sparked a period of accelerated research and investigation into two-dimensional material systems and the unique properties they offer. During this period, there have been continuous breakthroughs with regard to isolation, growth, and characterization of two-dimensional systems, enabling the number of known two-dimensional and layered materials to rapidly expand. As the number of two-dimensional and layered material systems investigated increases, so too does the number of potential applications. Currently, there exist several fundamental questions as to the role these materials might play in future electronic applications. As an example, graphene has been suggested for use as the channel material in high frequency transistors due to its exceptionally high carrier mobility, but also as an interconnect for integrated circuits due to its excellent thermal properties and ability to support very high current densities. Furthermore, there exist several fundamental challenges to implementing graphene and other two dimensional materials in many of the proposed applications. For the case of graphene this includes high contact resistivities and the inability to control edge morphology in highly scaled geometries.

This dissertation focuses specifically on the two-dimensional materials of graphene and tantalum di-sulfide in an attempt to elucidate some of the potential applications and challenges facing these two materials. It addresses several issues related to the development of a graphene based transistor for use in high frequency applications and the optimization of the graphene based transistor for mixing applications, including an analysis of graphene mixer design and the use of graphene nano-ribbon geometries to mitigate contact effects in highly scaled devices. In the final portion of the dissertation, the layered two-dimensional material 1T-TaS₂ is explored for potential applications in electronics, where use of its insulator-metal-transition could be utilized to implement a steep-slope transistor in order to overcome conventional constraints which currently limit performance of highly scaled silicon transistors.

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1. Graphene and the Rise of Two-Dimensional Materials

In 2004, Novoselov et al. experimentally demonstrated the first stable, free-standing two-dimensional crystal, graphene [1]. Prior to its discovery, the existence of two-dimensional crystals was thought impossible due to thermodynamic considerations [2, 3, 4]. With this landmark discovery, an immense world of opportunities for research into the previously unexplored areas of two-dimensional and layered materials was revealed. This revelation sparked an exciting period of intense research amongst the scientific community which has continued unabated for going on near a decade. Graphene crystals, as well as other two-dimensional crystals discovered in 2004, were found to be continuous and have a high degree of crystallinity [1, 5, 6, 7, 8] and were found to exist stably on non-crystalline substrates [5-7], in liquid suspension[1, 9] and as suspended membranes [8]. The existence of two-dimensional crystals has since been reconciled with thermodynamic theory by explaining the crystals as existing in a meta-stable state that has been quenched from bulk material. Since their discovery, two-dimensional materials have proven to be a rich experimental platform and have demonstrated interesting physical and electronic properties not found in bulk, three-dimensional materials.

1.1 Graphene Fundamentals: Structure and Physics

As the prototypical two-dimensional material, the structure of graphene is relatively simple, but this simple crystalline structure belies its unique physical and electronic properties. At its most basic level, graphene is simply a monolayer of graphite which has been sufficiently isolated from its environment as to be considered free standing [10]. In fact, the first experimental demonstration of

graphene was made by physically cleaving single layers of graphene from graphite sources composed of thousands to millions of layers of graphene [1]. Like graphite, graphene has a planar structure composed of carbon atoms which are arranged in a hexagonal lattice with an atomic separation of roughly 0.142 nm [11]. Within this structure, each carbon atom is connected to three others through three in-plane sp^2 hybridized σ -bonds to create a honeycomb pattern with an ideal bond angle of 120° between each atom. The one remaining electron orbital per carbon atom (p_z) exists as a highly delocalized π -orbital. Figure 1 shows the ideal hexagonal structure of graphene, where the two identical atoms of each unit cell are labeled as sublattice A and sublattice B.

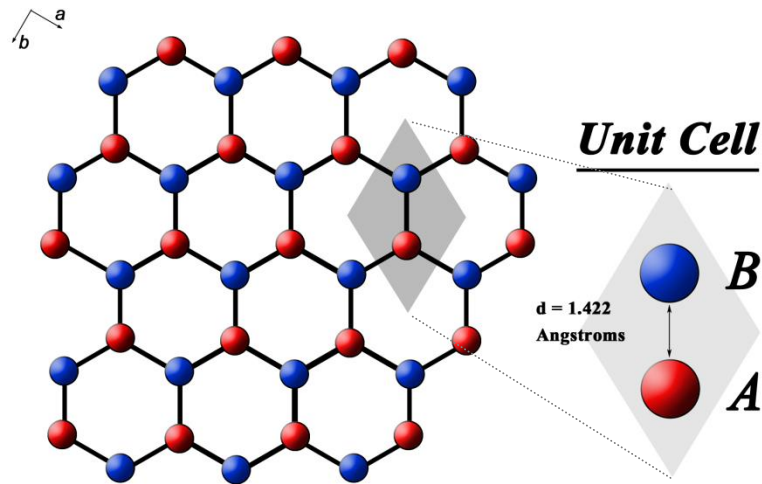


Figure 1. Ideal honeycomb structure of graphene. The two sublattices are labeled as A and B.

The two-dimensional structure of graphene can be manipulated to form other carbon allotropes. In this sense, graphene can be thought of as a building block for carbon allotropes of other dimensionalities. Zero-dimensional fullerenes are created by wrapping graphene into the shape of a sphere, one-dimensional carbon nanotubes are created by rolling graphene into tubes, and three-

dimensional graphite is formed by stacking graphene in a Bernal stacking order (ABAB), as shown in Figure 2.

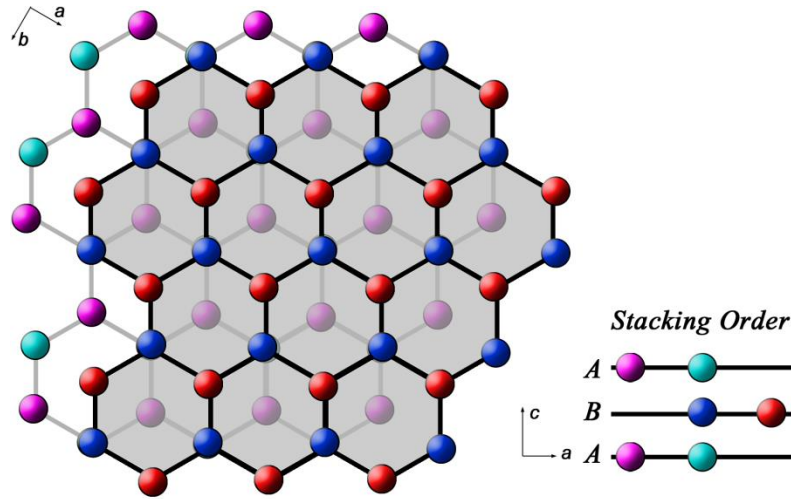


Figure 2. Bernal stacking of two layers of graphene. Repetition of these two layers in an ABABAB pattern produces bulk graphite.

Owing to its unique two-dimensional structure, graphene is host to many exceptional electronic and physical properties including a tensile strength of 130 GPa, which makes graphene the strongest material yet measured [12], and a thermal conductivity measured between 4800 and 5300 Wm⁻¹K⁻¹, higher than both diamond and carbon nanotubes [13]. Although graphene is host to many amazing properties, in the years following its discovery most research has focused on graphene's electronic properties and the underlying physics that explain them [10]. The interest in graphene's electronic properties is a result of, first, the fundamentally different way in which charge carriers in graphene are described as compared to other materials that came before it and, second, its exceptional electronic transport properties. These two aspects of graphene make it attractive as an experimental

platform and also as a novel material for the implementation of unique device architectures that make use of graphene's interesting properties or structure. For instance, by confining charge carriers to an isolated monolayer of atoms, graphene allows for direct access to the charge carriers by other materials such as superconductors or ferromagnetics and might allow for new ways to manipulate spin information or might allow for unique sensing applications.

While the Schrödinger equation is usually sufficient to describe the behavior of charge carriers in conventional materials, graphene's charge carriers are more naturally described using the Dirac equation (also known as the Dirac-Weyl equation) [14]. The (2+1)-dimensional Dirac equation (1) describes quasiparticles called massless Dirac fermions, which can be seen either as electrons that have lost their rest mass or as neutrinos that have acquired the electronic charge [14]. These quasiparticles display a linear dispersion relation (2) at low energies, where the particle energy is linearly related to the momentum through the Fermi velocity, $v_F = 1 \times 10^6 \text{ m s}^{-1}$.

$$(1) \quad \hat{H} = \frac{\hbar}{2\pi} v_F \begin{pmatrix} 0 & k_x - ik_y \\ k_x + ik_y & 0 \end{pmatrix} = \frac{\hbar}{2\pi} v_F \vec{\sigma} \cdot \vec{k}$$

$$(2) \quad E(\vec{k}) = \pm \frac{\hbar}{2\pi} v_F \sqrt{k_x^2 + k_y^2}$$

This relationship represents a significant departure from the Schrödinger equation, not only because of the linear dispersion relation (massless particle), but also because the Pauli matrix in the equation above, $\vec{\sigma}$, refers to pseudo-spin instead of real-spin. This difference of pseudo-spin arises because the electronic states near zero energy are composed of identical states on each of the two sublattices (A or B), which add an additional degree of freedom much like conventional electron spin does in bulk materials [14]. In this way, pseudo-spin represents “which lattice” and the two-dimensional Pauli matrix is used to specify pseudo-spin as opposed to real-spin. In graphene, pseudo-

spin related effects dominate over real-spin ones due to the fact that quantum electrodynamic (QED) specific phenomena are often inversely proportional to particle velocity, where $c/v_F \approx 300$ for the case of graphene [14]. Figure 3 shows three-dimensional $E-k$ diagrams for traditional “Schrödinger fermions” compared to Dirac-like particles.

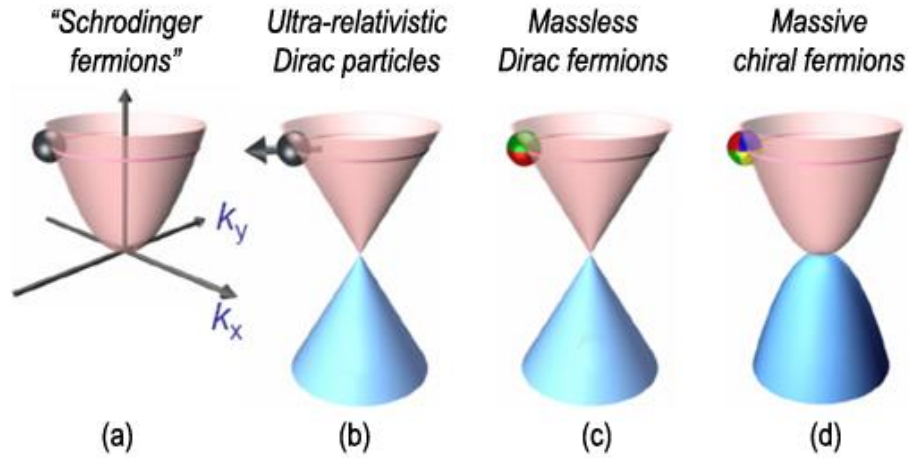


Figure 3. Comparison of $E-k$ diagrams for various quasiparticles. Conventional Schrodinger fermions show the expected parabolic dispersion relation (leftmost). Graphene charge carriers at low energies are best represented as massless Dirac fermions (center right), while charge carriers in bi-layer graphene are best represented as massive chiral fermions (rightmost). Different colors represent pseudo-spin of the charge carriers. Figure adapted from Ref. [10].

Conventional Schrodinger fermions display the expected parabolic dispersion relation, where particle energy is related to the square of momentum divided by the effective mass (Fig. 3a). In graphene, the conduction and valence bands display a linear, conical shape known as the Dirac cone (Fig. 3c). This is similar to ultra-relativistic Dirac particles (Fig. 3b) except that in graphene the speed of light is replaced by the Fermi velocity and the Pauli matrix represents pseudo-spin as opposed to

real-spin. For bi-layer graphene, the particles are best represented as massive chiral fermions (Fig. 3d), which exhibits four graphene sub-lattices.

In either single or bi-layer graphene, the electron energy bands (pink) and hole energy bands (blue) are three-fold degenerate at the two unique points of the sub-lattice (A and B), leading to six equivalent Dirac cones (differing only by pseudo-spin) that meet at the six corners of the two-dimensional, hexagonal Brillouin zone as shown in Figure 4 [15].

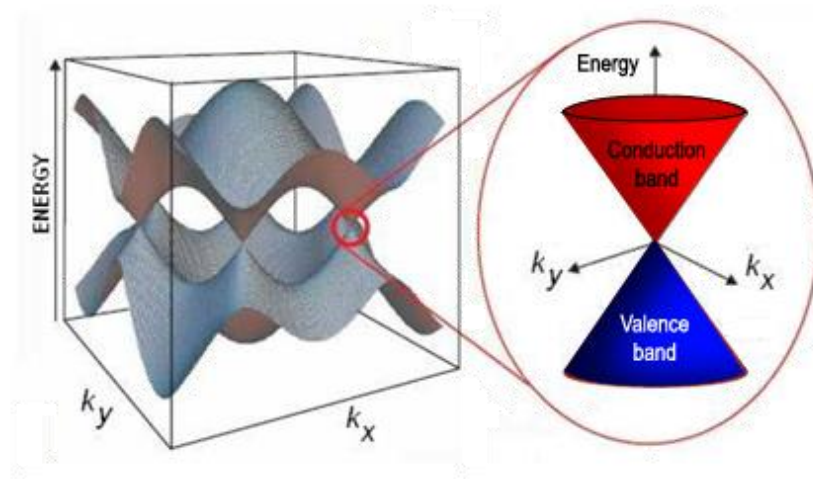


Figure 4. Three- dimensional band structure of graphene showing the six Dirac cones in the first Brillouin zone. Adapted from Ref. [15].

The meeting point between the two energy bands in k -space occurs at the Fermi energy of graphene (zero-energy) and represents a vanishing density of states. The vanishing density of states can also be thought of as a zero energy bandgap; and, for this reason, graphene is often referred to as either a zero-bandgap semiconductor or semi-metal. Although such a band structure suggests extremely high resistance at this zero-energy point, random thermal fluctuations and deformations of the graphene sheet lead to the generation of both electrons and holes and the formation of electron-hole puddles

which result in a universal minimum conductivity ranging between $4e^2/h$ to $8e^2/h$ ($5.8 - 2.9 \text{ k}\Omega$) [16]. Experimental studies of universal minimum conductivity in graphene have shown that it depends on the intrinsic impurity concentration at the graphene interface, as well as the number of layers of graphene. Besides pseudo-spin, charge carriers in graphene can also be described by another quantity, which is termed chirality. Chirality, or handedness, can be thought of as the projection of the two-dimensional Pauli matrix onto the direction of motion and is positive for electrons and negative for holes. The combination of pseudo-spin and chirality are important for understanding many of the phenomena of graphene, such as Klein tunneling.

1.2 Electronic Properties of Graphene

Although graphene's novel Dirac like particles and structure have been the focus of much work, it is the exceptional electronic transport properties, even at room temperature and high carrier concentrations, that have been the highlight of research focusing on practical applications for graphene. This is because the high crystalline quality of graphene samples and unique band structure of the material leads to extremely fast conduction of charge carriers, where mobilities greater than $200,000 \text{ cm}^2/\text{V}\cdot\text{s}$ have been reported for suspended samples in vacuum and at low temperatures [17] and values of $10,000 - 15,000 \text{ cm}^2/\text{V}\cdot\text{s}$ are routinely reported for exfoliated samples on SiO_2 at room temperature [1, 18]. These large mobilities lead to extremely long mean free paths for charge carriers and might allow for room temperature ballistic transport in graphene-based devices. Moreover, electron's and hole's demonstrate nearly symmetric transport properties as a result of the symmetry of the Dirac-cone about the zero energy point (Fermi energy). Figure 5 plots resistivity of graphene as a function of gate

bias (Fermi level), showing nearly symmetric hole- and electron-branches. E - k diagrams inset into the figure show the semi-metal transition across the Dirac point [15].

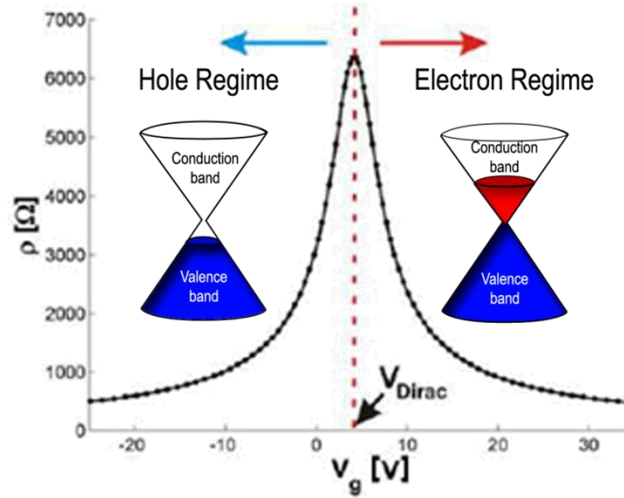


Figure 5. Resistivity of graphene as a function of back gate bias (carrier concentration) showing symmetric electron and hole-branches. Adapted from Ref. [15].

Additionally mobilities appear to be weakly dependent on temperature, indicating that transport is likely limited by remote charged impurity scattering and that these values may yet be improved. Importantly, mobilities remain high up to carrier concentrations on the order of 10^{13} cm^{-2} and carrier concentrations can be easily tuned between electrons and holes through electrical gating. Besides high mobilities, graphene also demonstrates high saturation velocity, with values up to $3 \times 10^7 \text{ cm s}^{-1}$ measured for graphene on SiO_2 at low carrier concentrations [19] and theoretical predictions of $4.6 \times 10^7 \text{ cm s}^{-1}$ for full-band Monte Carlo simulations of intrinsic graphene [20], and an extremely high current carrying capacity, with current densities as high as 10^8 A cm^{-2} reported for graphene nanoribbons with widths on the order of 20 nm [21]. These properties far surpass typical semiconducting materials.

Table 1 lists the bandgap, electron/hole mobility, thermal conductivity and intrinsic carrier concentration of several common semiconductors compared to graphene, where graphene excels in both carrier mobility and thermal conductivity.

Table 1. Bandgap, mobility, thermal conductivity, and intrinsic carrier concentration of common semiconductors as compared to graphene. Data sourced from Ref. [22].

material	band gap (eV)	electron mobility (cm² V⁻¹ s⁻¹)	hole mobility (cm² V⁻¹ s⁻¹)	thermal conductivity (W cm⁻¹ K⁻¹)	intrinsic carrier concentration at 300K (cm⁻³)
Si	1.12	≤1,400	≤450	1.3	1.10 x 10 ¹⁰
Ge	0.66	≤3,900	≤1,900	0.58	2.0 x 10 ¹³
GaN	3.39	≤1,000	≤200	1.3	3.4 x 10 ¹⁰
SiC (4H/6H)	3.23/3.0	≤900/≤400	≤120/≤90	3.7/4.9	~1 x 10 ⁻⁵
Diamond	5.46-5.6	≤2,200	≤1,800	6-20	~1 x 10 ⁻²⁷
GaAs	1.42	≤8,500	≤400	0.55	2.1 x 10 ⁶
InAs	0.35	≤40,000	≤500	0.27	1 x 10 ¹⁵
Graphene	0-0.2	≤200,000	≤200,000	48-53	~2.7 x 10 ¹⁶

1.3 Other Two-Dimensional Materials

Considering graphene's excellent electronic transport properties in combination with its near symmetric ambipolar conduction of both holes and electrons and unique Dirac-like description of charge carriers, it's easy to understand the great excitement generated by this material. In many ways, it is this excitement generated by graphene which has prompted further research into other two dimensional and layered material systems. After the experimental demonstration of graphene in 2004, other two-dimensional materials were quickly discovered. Isomorphs to graphene such as graphene, hexagonal boron nitride, and others were discovered or revisited with great interest. For example, hexagonal boron nitride (h-BN), which was in use in cosmetics and lubricants for several decades as a layered material, soon was proposed as the ideal two-dimensional mono-layer insulating supporting substrate for graphene. Transition metal dichalcogenides are another family of two-dimensional and layered materials which have seen an increase in interest to the scientific community due to the wide range of material and electronic properties they offer and the possibility for tuning those properties by changing the number of individual layers of a given material.

¹ Novoselov, K.S.; *et al.* Electric Field Effect in Atomically Thin Carbon Films. *Science* 2004, 306, 666-669.

² Peierls, R.E. Quelques proprietes typiques des corps solides. *Ann. I. H. Poincare* 1935 5, 177-222.

³ Landau, L.D. Zur Theorie der phasenumwandlungen II. *Phys. Z. Sowjetunion* 1937 11, 26-35.

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2. Graphene for High Frequency Mixing Applications

As discussed in the previous section, graphene exhibits several interesting electronic properties as a result of its unique band structure. Bilayer graphene (two layers of graphene with Bernal stacking) and graphene nano-ribbons share many of the same interesting electronic properties, yet also exhibit key differences. Of primary interest for high frequency radio frequency (RF) applications, graphene, bilayer graphene, and graphene nano-ribbons all exhibit excellent transport properties, with carrier mobilities greater than $200,000 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ reported for suspended monolayer graphene samples in vacuum and at low temperatures [23] and values of $10,000 - 40,000 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ routinely reported for exfoliated graphene samples on SiO_2 at room temperature [24, 25, 26]. Mobilities for bilayer and nano-ribbon graphene show significant reductions, yet are still predicted to reach values greater than $10,000 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ for small band-gaps [27]. Importantly, mobilities remain high up to carrier concentrations on the order of 10^{13} cm^{-2} and carrier concentrations can be easily tuned between electrons and holes through electrical gating. Besides high mobilities, graphene, bilayer graphene, and graphene nano-ribbons also demonstrate high saturation velocities, with values of $3 \times 10^7 \text{ cm s}^{-1}$ measured for graphene on SiO_2 at low carrier concentrations [28] and theoretical predictions ranging from $3 - 6 \times 10^7 \text{ cm s}^{-1}$ for graphene and its variations [29]. These properties far surpass typical semiconducting materials and make graphene and its alternative forms attractive for super high frequency and extremely high frequency operation. Specifically, the high mobility and saturation velocity of graphene suggests extremely high switching speeds for graphene based FETs. These characteristics are the primary driving force for research into potential high frequency electronic applications for graphene based devices.

Besides the potential for high frequency device operation as a result of high carrier mobilities, graphene and bilayer graphene also offer other unique traits which set them apart from conventional semiconducting materials. One of the key differences is the fact that both graphene and bilayer

graphene demonstrate nearly symmetric transport properties for electrons and holes as a result of the symmetric conduction and valence bands of the Dirac-cone about the zero energy point (Fermi energy). Combined with graphene's lack of bandgap or the exceedingly small bandgap that may be present in bilayer graphene, these symmetric transport properties result in an ambipolar device behavior exhibiting a unique, 'V'-shaped transfer curve with minimum conduction point occurring at the Dirac point (V_{Dirac}).

Combining this unique, ambipolar current-voltage (I-V) behavior with high carrier mobility and saturation velocity has generated significant interest to utilize graphene based devices in RF electronics and has allowed for several interesting novel RF applications including a single transistor triple-mode amplifier [30] and a single transistor, active ambipolar mixer [31]. Additionally, more conventional, passive mixer designs have also been implemented showing resistive [32], [33], [34] and drain mixing [35] as well as several experimental demonstrations of graphene FETs with current gain cutoff frequencies above 100 GHz [36] and as high as 427 GHz [36]. Of the proposed electronic applications for graphene, RF mixing is just one promising application; however, several key areas of graphene mixer performance remain unevaluated, making ultimate comparisons of graphene based mixers to conventional technologies incomplete. Furthermore, although technical and scientific progress has been rapid for the graphene based mixer, many important issues remain as barriers to practical implementations of the technology. Among these, high contact resistances, degraded transport properties with integration of top-gate dielectric, and degradation in symmetry and transfer characteristics of short-channel graphene based field effect transistors (GFETs) have significantly hampered implementation of GFETs for RF mixing applications.

For the case of degraded symmetry specifically, this challenge has severely hampered development of graphene based transistors as active mixing elements and led to a dramatic shift in focus to the GFET as a passive mixing element. Although a passive mixer configuration can be

beneficial in terms of linearity and reduces requirements on the gate stack, this configuration remains fundamentally limited to conversion loss of 3.9 dB, where gain is given as [37]:

$$(3) \quad Gain = \frac{(\Gamma_{max} - \Gamma_{min})^2}{\pi^2}$$

The inherent loss associated with passive graphene mixer necessitates additional design elements that can contribute to increased power consumption and incorporation of additional non-linearity for the transceiver. Additionally, passive mixers depend critically on large on-off ratios in order to minimize conversion loss (Eq. 3), which is typically less than 10 for the case of graphene FETs. This dependency necessitates a high power local oscillator (LO) input signal to ensure the greatest possible modulation in resistance and, thus, minimize conversion loss. These large LO power requirements and additional design elements can lead to significant RF and DC power draw for transceivers utilizing passive based mixers, especially as multiple stages or frequency channels are added (e.g., instantaneous frequency measurement (IFM) receiver). On the other hand, active mixers significantly relax LO power constraints due to their higher conversion gain (lower conversion loss). Preliminary experimental demonstrations of active graphene mixers have yielded the lowest conversion loss yet demonstrated by a graphene mixer [38] and simulations indicate that positive conversion gain is achievable with modest improvements to device performance and the use of input / output matching networks. Furthermore, direct comparison of passive and active configured graphene based mixers utilizing identical GFETs in each configuration indicates that an active configuration results in significantly reduced conversion loss (4dB) while maintaining comparable linearity to state of the art passive graphene mixers [38].

One of the main goals of this dissertation is to understand the key aspects of graphene device operation that impact performance of the active graphene mixer and, simultaneously, evaluate the benefits of the active graphene based mixer compared to passive configurations and conventional

technologies. In order to accomplish this, several goals are proposed, including: 1) generation of highly developed understanding of mixing operation in graphene devices; 2) optimization of graphene synthesis and dielectric integration techniques to improve RF performance of graphene transistors; 3) optimization of graphene transistor design for active mixing operation through improved understanding of electrostatics and scaling; and 4) fabrication and characterization of single stage graphene active mixers in terms of gain and operating frequency range. In this dissertation, the limiting factors for active graphene based mixer are explained and the advantages of nano-ribbon geometries for mixing applications are explained.

2.1 Importance of the Radio Frequency Mixer

A mixer is a three port active or passive device that is designed to yield both a sum and a difference frequency of two distinct input signals at a single output port. This process is often referred to as frequency conversion, or heterodyning, and is used in most communication systems in order to increase or decrease a signal's frequency. In RF receivers, frequency conversion is typically used to down-convert a high frequency RF input signal to an intermediate frequency (IF) at a lower-frequency. This is due to the fact that it is much easier to efficiently amplify and filter a signal when all of the subsequent IF stages in the receiver can be tuned and optimized for a single, low band of frequencies. The opposite process of up-converting an input signal to an output signal at a higher frequency is used in transmitters to prepare a signal for efficient transmission through space. In both cases, a local oscillator (LO) is normally used to supply a continuous waveform signal as the second input to the mixer. This LO signal is used for mixing with the other input signal (e.g., the RF signal received from the antenna), as shown in Figure 6.

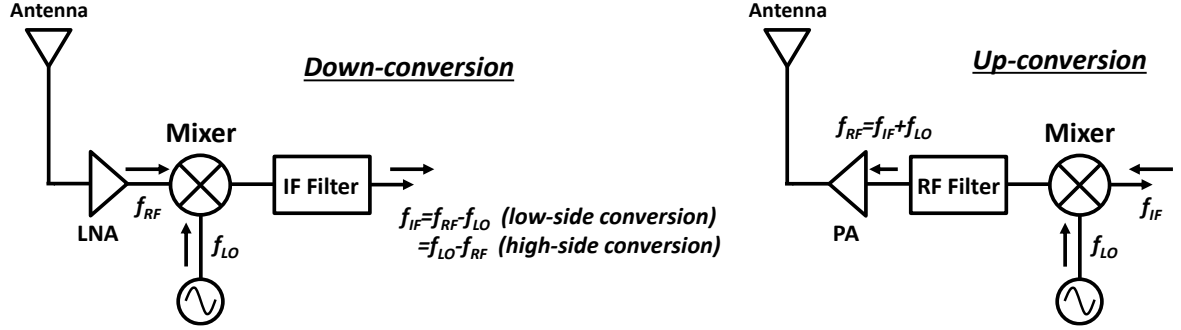


Figure 6: Schematic representations of RF receiver and transmitter showing mixing of RF and LO signals for down- and up-conversion, respectively.

Mixers operate using one of two basic methods to produce a non-linear transfer function in order to generate the desired frequency mixing: 1) use of device non-linearity or 2) use of time-varying switching or sampling. In both cases, the Taylor expansion of the non-linear transfer function gives rise to harmonics that result in the desired output signal as well as undesired intermodulation products. Although switching mixers typically have the advantages of lower noise figure and larger conversion gain by more closely approximating the behavior of an ideal commutator, it is often difficult or impossible to generate the required, square wave LO input signal at these high frequencies. Because of this limitation, mixers utilizing the non-linear nature of a device to achieve mixing action are able to far exceed the operating frequencies of switching mixers. Besides operating frequency, there are several important properties of an RF mixer that determine how the usefulness of a mixer and for what applications it is most suited. Table 2 details these properties and their impact on mixer performance.

Table 2: Important properties of mixers.

Conversion Gain	Reduces the noise impact to following stages in the transceiver
Linearity	Impacts the RF input power at which undesired intermodulation products dominate the output
Isolation	Minimizes interaction between input and output ports
Noise Figure	Impacts receiver sensitivity
Image Noise Suppression	Improves mixer noise figure
Operating Frequency Range	Determines the range of operation / application

2.2 Ambipolar Graphene Mixer

The ambipolar graphene mixer is a specific configuration of the active graphene mixer which utilizes graphene's (or bilayer graphene's) symmetric, ambipolar nature for suppression of odd order harmonics while simultaneously achieving peak conversion gain [31, 38]. As an active mixer, the ambipolar graphene mixer is able to surpass the conversion gain performance of passive mixers (i.e., resistive mixing, drain mixing), yet depends critically on the presence of a narrow, symmetric transfer curve as well as access to the Dirac point in order to do so. For this type of mixing (i.e., gate mixing, transconductance mixing), the LO and RF input signals are fed to the gate of the FET while the IF signal is sensed at the drain. The special case of ambipolar mixing is achieved when the graphene transistor is biased at V_{Dirac} . Figure 7 shows the measurement setup for ambipolar mixing.

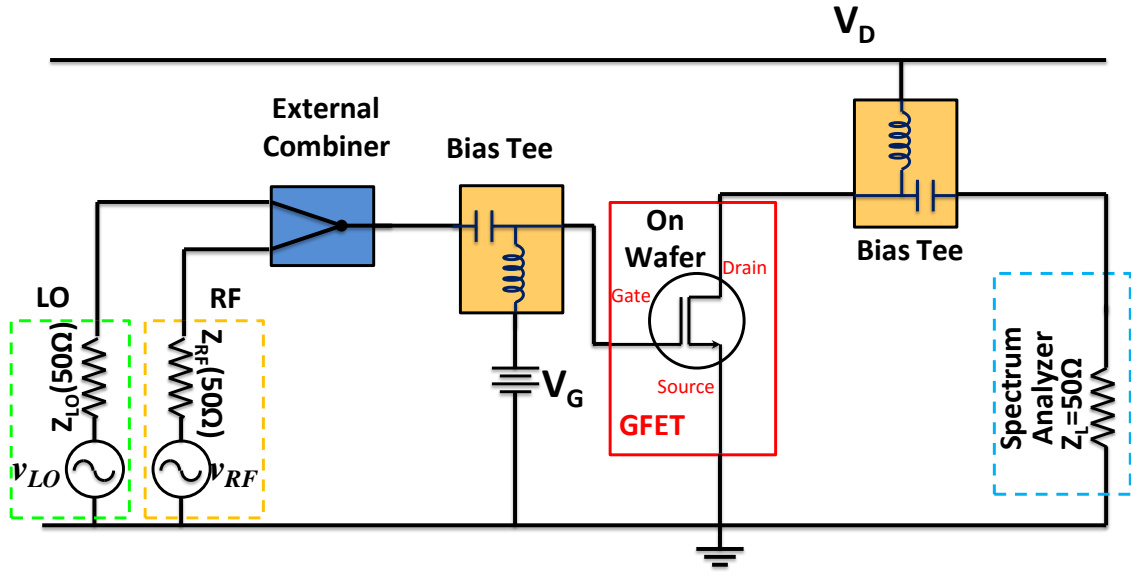


Figure 7: Measurement setup for single stage ambipolar graphene mixer.

To better understand the mixing ability of the graphene transistor, it is important to consider the distortion components of the small signal output current. Small signal output current (i_d) of a graphene transistor in terms of the small signal input voltage (v_g, v_d) can be written as:

$$(4) \quad i_d(v_g, v_d) = \frac{\partial I_d}{\partial V_g} v_g + \frac{\partial I_d}{\partial V_d} v_d + \frac{1}{2} \frac{\partial^2 I_d}{\partial V_g^2} v_g^2 + \frac{1}{2} \frac{\partial^2 I_d}{\partial V_d^2} v_d^2 + \frac{\partial^2 I_d}{\partial V_g \partial V_d} v_g v_d + \frac{1}{6} \frac{\partial^3 I_d}{\partial V_g^3} v_g^3 + \frac{1}{6} \frac{\partial^3 I_d}{\partial V_d^3} v_d^3 + \frac{1}{2} \frac{\partial^3 I_d}{\partial^2 V_g \partial V_d} v_g^2 v_d + \frac{1}{2} \frac{\partial^3 I_d}{\partial V_g \partial^2 V_d} v_g v_d^2 + \dots$$

(4) can be re-written in a simplified for the specific case of ambipolar mixing as:

$$(5) \quad i_d(v_{LO} + v_{RF}, 0) = g_m(v_{LO} + v_{RF}) + g_m'(v_{LO} + v_{RF})^2 + g_m''(v_{LO} + v_{RF})^3 + \dots$$

The symmetric transfer characteristics of the graphene transistor give rise to the ambipolar graphene mixer's unique ability to eliminate the output of odd order intermodulation products. This is a result of the fact that while the IF signal is proportional only to g'_m , the 1st and the 3rd order intermodulation products depend on g_m and g''_m , respectively. Figure 8a plots the transfer characteristics of a typical bilayer graphene transistor with $L_g = 750$ nm and biased at $V_{ds} = 1$ V, while Figure 8b shows the extracted 1st, 2nd and 3rd order components of the drain current. At the Dirac point where the slope of the transfer curve goes to zero, both g_m and g''_m similarly go to zero. On the other hand, g'_m reaches its maxima at the Dirac point where g'_m is proportional to the curvature of the transfer curve. Because of the unique shape of the I-V behavior, operation at the Dirac point simultaneously results in peak conversion gain while quenching odd order intermodulation products.

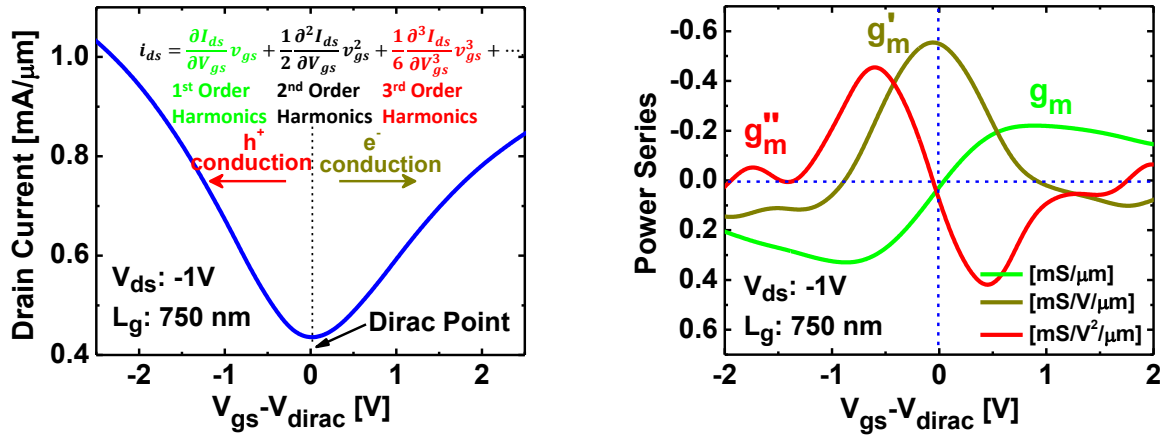


Figure 8: Ambipolar conduction leads to high conversion gain and suppression of odd order mixing products at transistor output. (a) Transfer curve of graphene FET showing ambipolar behavior. (b) Extracted first, second, and third order components of drain current showing peak g'_m as well as minimum g_m and g''_m at the Dirac point.

In order to benchmark the ambipolar graphene mixer against alternative graphene mixer configurations and conventional mixer technologies, it is important to consider the key properties of a mixer mentioned in Section 2.1. Plotting conversion gain as a function of LO power for several state of the art passive and active graphene mixers, Figure 9 shows a linear dependence of conversion gain until a LO power of about 0 dBm for the ambipolar mixer operating at 10 GHz. Although the ambipolar mixer exhibits the highest conversion gain of all graphene mixers, it is still limited to conversion loss greater than 10 dB. This is due to the absence of any matching network, as well as limited device transconductance due to relatively thick equivalent oxide thickness (EOT) of ~ 3 nm, long channel length (750 nm), and high contact resistances ($100\text{-}200\ \Omega\text{-}\mu\text{m}$).

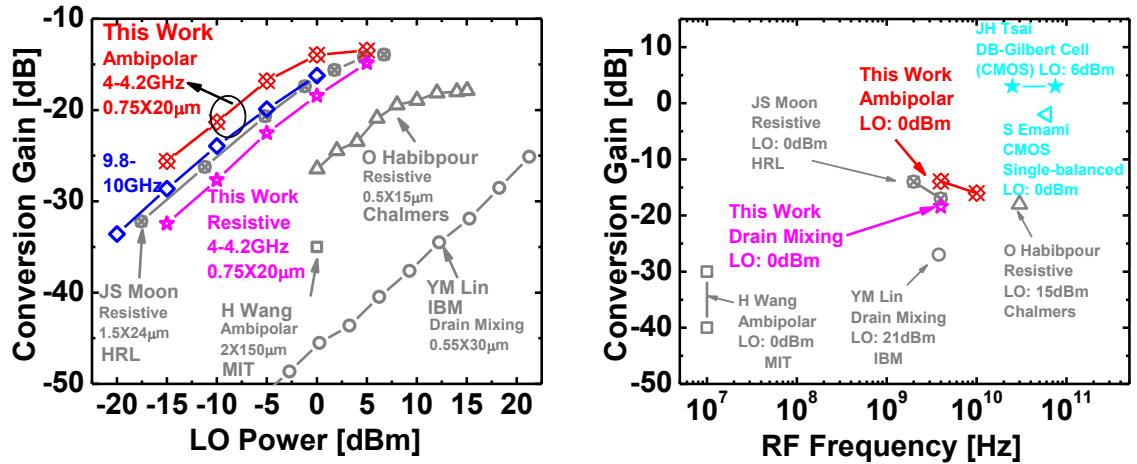


Figure 9: Conversion gain versus LO power (a) and conversion gain versus RF frequency (b) for state of the art passive and active graphene mixers.

Compared to conventional technologies, graphene remains limited to lower operating frequencies due to several key reasons (Figure 9b). These include the limited extrinsic frequency performance of graphene FETs due to external parasitic components as well as the lack of properly

designed and integrated matching networks utilizing micro-strip construction. In 2013, Habibpour et al demonstrated the highest operating frequency for a graphene based mixer utilizing a multi-channel graphene nano-constriction FET operating in a passive configuration at 30 GHz [34]. This record high operating frequency was realized through use of an integrated microstrip matching network with backside processing and scaled graphene device, with $L_{ch} = 500$ nm.

Although there is limited work examining the linearity performance of graphene mixers, current state of the art designs yield OIP3 values from -8.5 to 3 dBm. While passive configurations have demonstrated the highest linearity yet for a graphene mixer, competitive ambipolar configurations yield comparable OIP3 values after considering the effects of matching input / output networks (Table 3). Further work is needed to compare the linearity of highly optimized graphene mixers to conventional technologies, which often utilize multiple stages and balanced networks to improve linearity by canceling out unwanted spurious responses and intermodulation products. Alternatively, continued improvements to conversion gain of the graphene mixer are expected to lead to improved OIP3.

Table 3: Comparison of output third order intercept and gain for various graphene mixers.

Identical Devices	Graphene Mixers	PLO [dBm]	OIP3 [dBm]	Gain [dB]
	Passive Subharmonic (Chalmers) O. Habibpour, et al; MTT 2013.	15	-5.2	-18
	Passive Mixer (HRL) JS. Moon, et al; EDL 2013.	-3.5	3	-18
	Passive Mixer (PSU)	0	--	-18
	Active Mixer (PSU) Madan, et al; IEDM 2012. Without Matching	0	-8.5	-14
	Active Mixer (PSU) Madan, et al; IEDM 2012. With Matching	0	-1.5	-7.5

Benchmark of graphene mixer with conventional technologies with respect to noise is complicated due to the limited work done to characterize noise performance in graphene mixers. Of the various graphene based mixer topologies, only the resistive graphene mixer (passive) has been characterized, exhibiting a noise figure of 20-25 dB over the range of 2-5 GHz [39]. Importantly, this study was able to show that the noise figure is roughly equal to conversion loss for a passive mixer where thermal noise dominates (i.e., absence of significant gate leakage currents). These results indicate that significant advances can be achieved by improving the conversion gain, yet further work is necessary to characterize and understand the noise figure for the ambipolar graphene mixer.

In terms of conversion gain, the ambipolar graphene mixer is not yet able to approach the performance offered by highly optimized active mixers utilizing conventional materials (i.e., positive conversion gain: ~5-7 dB). For the ambipolar mixer, this is due primarily to the degradation in symmetry and transfer characteristics experienced by GFETs as they are scaled to short-channel

dimensions, yet the high mobility, saturation velocity, and unique quenching of third order intermodulation products due to symmetric transfer characteristics suggest that an optimized graphene device may fill a potential niche application for high frequency mixing. In the following sections, further discussion of the major issues limiting performance of the ambipolar graphene mixer are presented.

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3. Optimizing the Graphene Transistor for High Frequency Mixing Applications

While ambipolar mixer configurations were one of the first graphene based mixer configurations to be demonstrated [31] and have been shown to outperform alternative, passive configurations [38], recent demonstrations of graphene based mixers have focused predominantly on utilizing resistive mixing configurations [32, 33, 34, 35]. The shift away from ambipolar configurations can be attributed to the fact that conventional sheet-based graphene devices exhibit degraded transfer characteristics, loss of symmetry between p and n-branch, and a large shift in V_{Dirac} as channel length (L_{ch}) is scaled to $1\mu\text{m}$ and below [40, 41]. These undesired effects often make V_{Dirac} inaccessible and lead to degraded CG as well as increased odd order intermodulation products. These effects make ambipolar mixing configurations unfeasible for high frequency graphene mixer applications, which necessitate use of short-channel devices to ensure both high current gain cut-off frequency (f_T) and power gain cut-off frequency (f_{Max}).

To optimize the graphene transistor for ambipolar mixing applications, Dirac shift and asymmetry must be avoided. Additionally, as discussed in Section 2, the ultimate performance of the mixer depends directly on g'_m , which is itself the derivative of on g_m with respect to gate bias. In this way, a graphene transistor exhibiting a high degree of symmetry, access to the Dirac point, and a large peak transconductance represents the ideal graphene transistor for ambipolar mixing applications. Achieving this characteristics depends on preventing the observed phenomena of Dirac shift and asymmetry with reducing L_{ch} as well as preserving a high peak transconductance, where transconductance degradation often occurs as a result of parasitic resistances, degradation in mobility, or an inability to scale the gate dielectric to sufficiently small thicknesses (i.e., $EOT < 3\text{ nm}$). As a result, several key aspects of graphene transistor development and fabrication can be highlighted as limiting factors with regard to ultimate achievable performance. Among these, reliable large scale

synthesis of high quality graphene demonstrating excellent transport properties is one of the most fundamental problems to implementation of graphene based devices in practical applications. In this work, large scale synthesis is achieved using a controlled sublimation of Si from SiC wafers. Although this process is successful in producing relatively uniform mono- and bilayer graphene across large area substrates, it is complicated by a highly non-uniform surface morphology which often leads to degraded transport properties. Following graphene synthesis, materials integration of gate dielectric and contact metals with graphene can be considered two of the major fundamental challenges to implementing a high frequency graphene based device. In this section of the dissertation, graphene synthesis, dielectric integration, and contact effects will be considered with respect to high frequency operation.

3.1 Large Scale Synthesis Using Hydrogen Intercalated Epitaxial Graphene

While graphene's initial discovery was ground breaking in establishing the feasibility of two-dimensional crystals, the synthesis technique utilized to make this discovery has not been conducive to large-area, wafer-scale production of electronics based on graphene. The technique, referred to as exfoliation, relies on micro-mechanical cleaving of two-dimensional crystals from the three-dimensional graphite bulk by dragging highly-ordered pyrolytic graphite (HOPG) across the surface of a substrate [1] or by using scotch tape to peel several layers of carbon from HOPG which can be repeated many times on thinner and thinner crystals to eventually yield single-layer graphene [14]. The process of exfoliation is a relatively simple method to produce high-quality graphene and can produce crystallites as large as 10 μm , which may be large enough for subsequent processing and device fabrication; however, this process produces bi-layer and multi-layer crystallites as well. Because of the various thickness crystallites produced during exfoliation, optical microscopy or alternative characterization techniques must be utilized to search through the exfoliated crystals in order to identify single-layer graphene crystallites for further processing or testing. Although the graphene produced by

such mechanisms typically exhibits excellent electronic properties, the technique is impractical for large-scale manufacturing due to its time consuming nature as well as the small crystallite size. In recent years, synthesis by mechanical cleavage has become more efficient, incorporating the use of ultra-sonication to create suspensions of sub-micron graphene crystals which can be used to coat arbitrary substrates [42]; however, such a technique is still far too uncontrolled for most electronic device applications. On the other hand, the development and optimization of alternative synthesis techniques has allowed for wafer-scale synthesis of large-grained, polycrystalline graphene films and have provided promise for the eventual commercialization of graphene-based electronic technologies that require high quality, affordable graphene substrates. Two of the most promising synthesis techniques are chemical vapor deposition (CVD) and sublimation from SiC wafers.

Although both CVD and Si sublimation techniques are able to produce high quality graphene over a large area, they differ in their approach. CVD techniques typically operate through segregation of bulk-dissolved carbon at the surface of a transition metal or through surface decomposition of carbon-containing precursors (i.e., methane, propene, ethylene, etc.), also at the surface of a transition metal [43]. In both methods, the metal substrate is typically heated to 1000 °C. Due to the fact that the graphene is grown directly atop the metal substrate in either segregation or decomposition methods, graphene growth by CVD techniques necessitates a transfer step to move the graphene material from the metal growth substrate to a suitable supporting substrate for device fabrication. This is typically accomplished using a solution transfer method, although several methods now exist. Unlike CVD based synthesis techniques, growth of graphene through sublimation of Si from a SiC wafer requires no transfer step. Instead, the SiC growth substrate acts as a semi-insulating supporting substrate that is suitable for subsequent device processing [44]. Silicon sublimation occurs at high temperatures (~1300-1600 °C) and can take place either in ultra-high vacuum or in an inert, low pressure argon atmosphere. In the following section, we will discuss the synthesis and integration of epitaxial graphene for subsequent device applications.

3.1.1 Synthesis of Epitaxial Graphene

Synthesis of epitaxial graphene from SiC substrates is accomplished through the controlled, high-temperature sublimation of silicon from the underlying SiC [45, 46, 47]. Sublimation of silicon from the SiC leaves behind a reconstructed layer of carbon atoms, which ultimately rearrange to form a layer of graphene. This process can be considered bottom-up, where growth of each subsequent layer of graphene takes place below the previously grown layers, instead of above them. This is unlike most other growth processes, which can be considered top-down, where growth of subsequent layers typically takes place on top of previously grown layers. The growth kinetics and quality of the resulting graphene depends on the structure of the SiC surface that is used for growth. The most common substrates are 4H-SiC and 6H-SiC hexagonal structures [45, 46, 47]. Each of the two polymorphs is comprised of SiC bilayers, where each bilayer contains a plane of C atoms as well as a plane of Si atoms. 4H-SiC and 6H-SiC contain 4 and 6 SiC bilayers, respectively, and exhibit different stacking sequences [48]. The SiC crystal structures have a Si-terminated surface (0001) as well as a C-terminated surface ($000\bar{1}$). Figure 10 shows the crystal structure of these two SiC polymorphs.

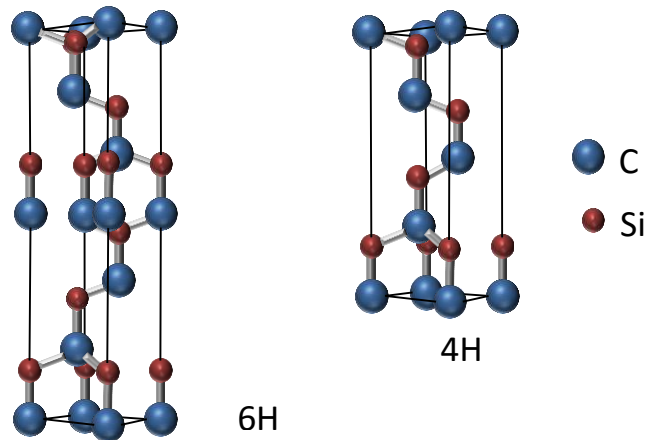
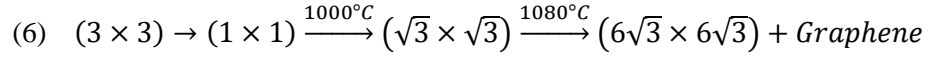


Figure 10. Crystal structure of the 6H and 4H SiC polymorphs showing stacking order.

Before graphitization, the SiC substrate is subjected to a H₂ etch step at elevated temperatures in order to create a regular array of atomically flat surfaces. The use of a hydrogen etch prior to graphene synthesis is effective in removing much of the residual surface damage caused by SiC polishing techniques [49]. Importantly, the hydrogen etch also leads to significant step-bunching and the formation of terraces across the SiC surface, which will be discussed at a later point [49]. The Si sublimation growth process follows and is used to grow graphene either in ultra-high vacuum (UHV) or in an inert argon atmosphere at about 1200 °C [50, 51, 52]. The use of argon during the sublimation process can help to improve film morphology, leading to reduced pitting and much larger domain sizes than achievable using high vacuum sublimation [49]. Growth can take place on either the Si-face or C-face of the SiC substrate and the final structure of the graphene depends on which face the growth takes place. Growth on the C-face is faster than on the Si-face, yet the graphene that grows on this face has a variety of orientations and can be considered rotationally faulted relative to the conventional Bernal stacking in graphite crystals [44]. The growth on the Si-face is significantly slower and produces Bernal stacked layers of graphene which have an orientation of 30° with respect to the underlying SiC plane [45, 53]. While graphene growth on the Si-face is sensitive to growth temperature, it is found to be relatively independent of growth time. Because of this fact, graphene growth on the Si-face is often considered a self-limited process [54]. Due to the additional control over film morphology provided by the slow growth speeds and well-ordered graphene stacking, Si-face growth processes are considered the most promising candidates for producing large, homogenous graphene substrates for wafer scale device fabrication. As a result, this section will focus primarily on the growth mechanisms that drive graphene formation on the Si-face.

Throughout the graphitization process, the Si-face goes through a sequence of surface reconstructions that ultimately result in the growth of a graphene sheet and a carbon buffer layer which exists between the graphene and the underlying SiC substrate. The series of surface reconstructions are listed below [55].



The process starts with a hydrogen etched sample and the preparation of the Si rich (3×3) phase. Heating this surface to about 950 °C leads to a $(\sqrt{3} \times \sqrt{3})\text{R}30^\circ$ phase. This phase can be considered as a 1/3 monolayer of Si adatoms atop the SiC substrate. Further annealing to 1100-1150 °C sublimes more silicon from the surface and leads to the formation of a well-ordered $(6\sqrt{3} \times 6\sqrt{3})\text{R}30^\circ$ phase, in which the SiC is covered by a carbon layer. The large surface unit cell of $(6\sqrt{3} \times 6\sqrt{3})\text{R}30^\circ$ comes into existence only because of the difference in lattice parameters of graphene and SiC (2.46 Å and 3.08 Å respectively). The side length of the $(6\sqrt{3} \times 6\sqrt{3})\text{R}30^\circ$ is approximately 32 Å and contains about 108 carbon atoms and 108 silicon atoms per SiC bilayer, which can be seen from Figure 11. The $6\sqrt{3} \times 6\sqrt{3})\text{R}30^\circ$ reconstruction is equivalent in size to a (13×13) graphene unit cell. The quasi-(6×6) honeycomb hexagons are slightly varying in size during these phase transitions [56]. These phases and patterns are observed using low energy electron diffraction (LEED) [56].

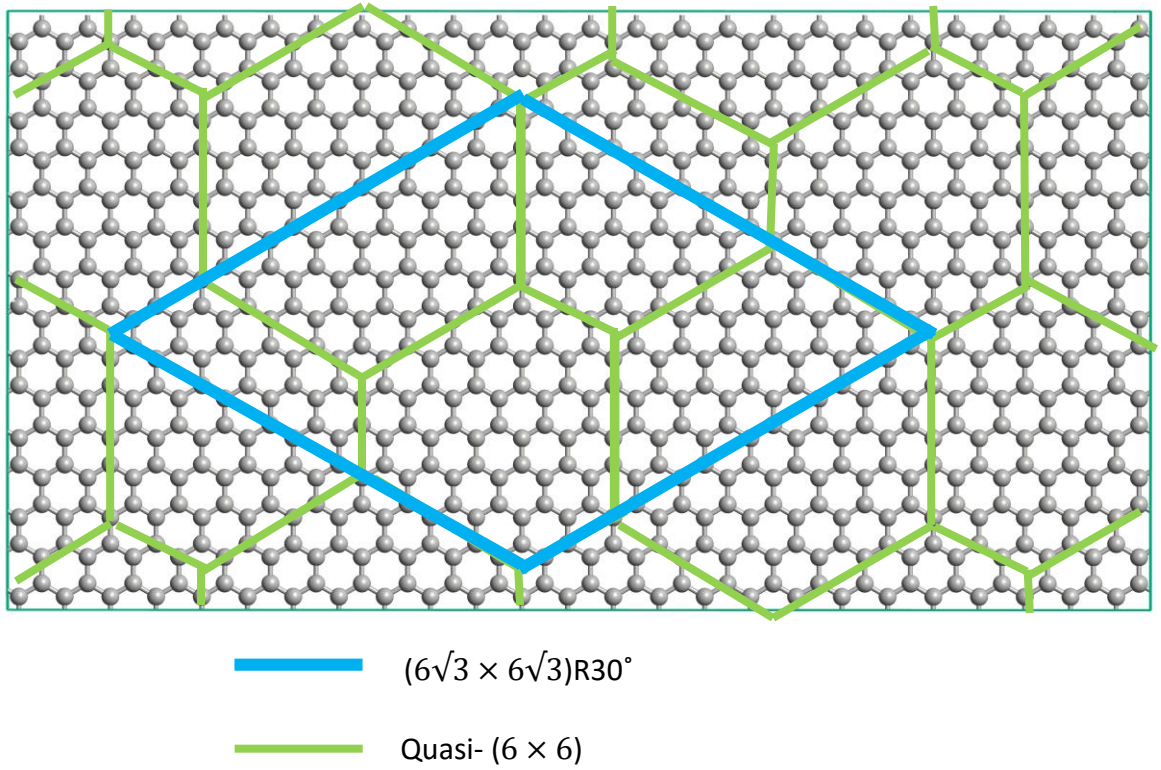


Figure 11. Structural model of the $(6\sqrt{3} \times 6\sqrt{3})R30^\circ$ reconstruction in top view showing the Si-terminated (1×1) -SiC substrate. The $(6\sqrt{3} \times 6\sqrt{3})R30^\circ$ unit cell and the three hexagons in quasi- (6×6) periodicity are indicated. Adapted from Ref. [56].

The $(6\sqrt{3} \times 6\sqrt{3})R30^\circ$ superstructure, which is often referred to as the carbon buffer layer, exists between the crystalline SiC substrate and the overlying graphene. It is sometimes referred to as “zerolayer graphene” as it represents the precursor to graphitization. It serves as a buffer layer for growth of epitaxial graphene layers. The carbon layer which sits atop the buffer layer represents the first carbon layer which can be considered graphene, although it does not actually grow on top of the buffer layer. Instead, each layer of graphene that sits atop the buffer layer is the result of the desorption of Si atoms from the underlying SiC bilayers. Desorption of Si atoms from a total of three SiC bilayers is required to form a single layer of graphene, which can be understood simply by counting the number of C atoms needed to form a single graphene monolayer and realizing that a single SiC bilayer yields only $1/3$ the required C atoms. Each new layer of graphene starts with the formation of a new $(6\sqrt{3} \times$

$6\sqrt{3}$)R30° buffer layer, during which the previous buffer layer is released of its covalent bonding with the SiC surface and is transformed into a true graphene layer. This process results in a stacking of graphene sheets all with a 30° rotation relative to the underlying SiC lattice. Although the graphene is rotated relative to the SiC lattice, additional layers of epitaxial graphene on the Si-face are found to be Bernal stacked relative to the first layer.

Examining the C 1s peak of the XPS spectra of the carbon buffer layer can provide valuable insight into its structure. In the XPS spectra, the C 1s level is comprised of several different peaks. Apart from the SiC bulk peak at 283.73 eV, there are two additional peaks called S1 and S2, at 284.99 eV and 285.60 eV respectively. A graphene peak is expected at 284.7 eV, yet neither S1 nor S2 are at that position. Instead, the $(6\sqrt{3} \times 6\sqrt{3})$ R30° layer has two non-equivalent, non-graphene-like carbon atoms. Since this layer is partially covalently bound to the substrate, S1 originates from the sp^3 bonded carbon atoms which are simultaneously bound to one Si atom of the Si(0001) layer and 3 C atoms in the overlying graphene and S2 originates from the remaining sp^2 bonded carbon atoms in the buffer layer [56]. The two components have a ratio of approximately 1:2 and thus, almost 1/3 of the carbon atoms in the initial layer are bound to the SiC substrate.

3.1.2 Step Edges on SiC Substrates

When discussing the growth and electrical properties of epitaxial graphene, it is important to address the impact of step edges. Currently, it remains difficult to obtain atomically flat SiC wafers and the nominally on-axis SiC substrate typically exhibits some small degree of off angle, resulting in atomic step-edges across the surface of the substrate. The aforementioned H₂ etch step is helpful in rearranging the SiC surface to achieve regions of atomically flat SiC for subsequent graphitization

according to the growth kinetics described previously. However, during the high temperature H_2 etch step significant step-edge bunching occurs across the SiC substrate. These step-edges coalesce into large $(1\bar{1}0n)$ inclined facets, which are separated by atomically flat (0001) plateaus. Although the growth of graphene on the Si-face described in the previous section is self-limited and highly controllable down to a single monolayer of graphene, the presence of step-edges across the substrate surface lead to regions of multi-layer graphene interspersed between few-layer regions. This phenomenon is a result of the fact that graphene growth on the $(1\bar{1}0n)$ crystal face differs from the (0001) face. Furthermore, several researchers have quantified the negative impact of step-edges on the ultimate carrier mobility of bulk Si-face epitaxial graphene. In these reports, step-edges have often been cited as a source of additional scattering, with reports of degradation of bulk mobility occurring with increasing step-edge density [57] as well as reports of conductivity anisotropy parallel and perpendicular to step-edges [58,59]. Recently, Ross *et al.* have utilized atomic scale measurements to directly measure the additional resistance introduced across the step-edge [60]. These results indicate that step-edges between the plateaus are important not only in determining the ultimate electronic properties of the material, but also in understanding the growth and nucleation kinetics of epitaxial graphene. In the following section, an experimental transport study is presented in an attempt to discern and understand the true impact on electronic transport properties as a result of step-edges across the SiC substrate.

The presence of multi-layer graphene at step edges has been studied extensively in the literature. This phenomenon is a result of the fact that graphene growth on the $(1\bar{1}0n)$ crystal face differs from the (0001) face, where growth on the $(1\bar{1}0n)$ face occurs at lower temperatures and is not self-limiting [61]. It is thought that step-edges serve as nucleation sites for the graphene film due to their high density of dangling bonds and defective nature [61]. Figure 12 shows a cross-sectional TEM micrograph of a step-edge that shows multi-layer graphene growth along the $(1\bar{1}0n)$ crystal face while the (0001) terrace ledges show no graphene [61]. For this sample, the graphitization temperature of

1325 °C is slightly lower than the typical temperature for graphitization of the (0001) face. The presence of multilayer graphene at the step-edge confirms the lower growth temperature and suggests that the $(1\bar{1}0n)$ face may serve as a nucleation site for graphene growth across the (0001) plateau. Researchers have shown that defects at the step edges can facilitate the sublimation of Si and hence, graphitization first occurs on the (0001) face where the step-edge meets the (0001) plateau. Low energy electron microscopy (LEEM) and scanning electron microscopy (SEM) of partial graphitization show that this reconstruction phase is initially concentrated at the step edges and then grows outward from the step-edge. These regions stretch out into the flat terraces of SiC and form islands which merge together to form graphene monolayer [62, 63].

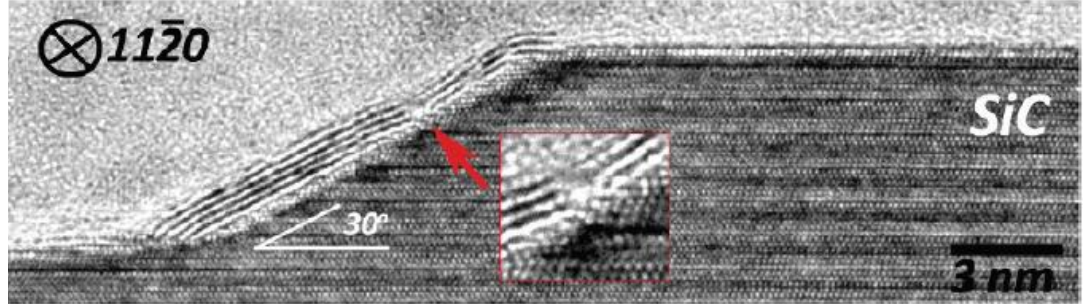


Figure 12. Cross-sectional TEM micrographs of graphene nucleated on the terrace step edge of SiC at 1325 °C. Many-layer graphene is possible along the $(1\bar{1}0n)$ plane and can occur before growth of graphene on the terrace face (0001). Adapted from Ref. [61].

Due to the unique growth kinetics present at the step-edge, graphene nucleation and subsequent growth occur rapidly, leading to multi-layer graphene over the step-edge [61]. Alternatively, graphene on the terrace plateau is primarily monolayer or bilayer, creating a striped morphology across the wafer.

This is schematically represented in Figure 13b, while Figure 13a shows the SiC morphology before the hydrogen etch step and subsequent graphitization.

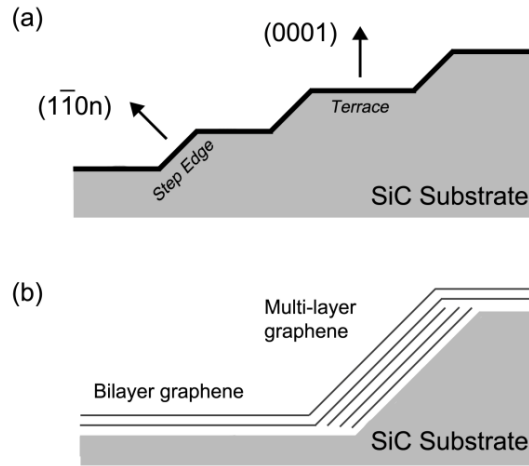


Figure 13. (a) Schematic representation of SiC surface before graphitization compared to (b) after high temperature graphitization and hydrogen passivation steps showing significant step-bunching in the substrate.

3.1.3 Quasi-free Standing Epitaxial Graphene

Quasi-free standing epitaxial graphene, or QFEG, is a form of epitaxial graphene on SiC where a hydrogen intercalation process is used to convert the carbon buffer layer into a second layer of graphene. QFEG is a direct result of recent work to cleave Si-face epitaxial graphene from the carbon buffer layer and has led to substantial improvements in electronic transport properties as well as reduced electron doping [64, 65, 66], suggesting that passivation or removal of the buffer layer is integral to high performance Si-face epitaxial graphene. These experiments are often able to improve mobility to

3000 cm²/V·s at similar carrier densities (1×10^{12} to 1×10^{13} cm⁻²).^{27,28} In this method, the epitaxial graphene is exposed to molecular hydrogen at elevated temperatures (1000 °C), whereupon the hydrogen acts to passivate the SiC substrate and is found to convert the carbon buffer layer to a layer of graphene. In this way, the technique can be used to convert a single carbon buffer layer to a monolayer of graphene atop the hydrogen passivated SiC substrate, effectively decoupling the graphene from the underlying substrate. This process is schematically represented in Figure 14. In the following pages, it is shown that the improved transport properties with hydrogen intercalation are mostly attributed to a reduction in remote charged impurity scattering, which are likely associated with the dangling bonds present in the carbon buffer layer [67].

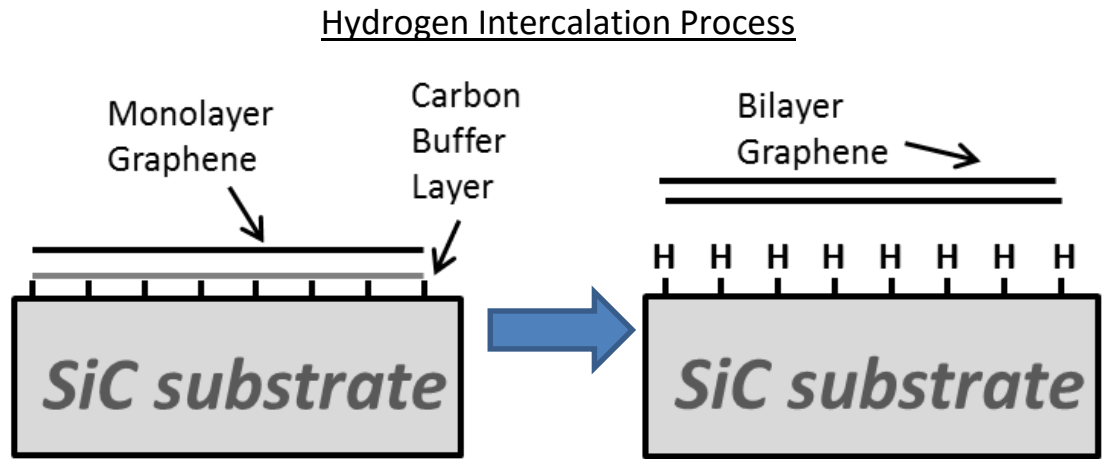


Figure 14. Schematic representation of hydrogen intercalation process whereby the carbon buffer layer (grey, left figure) is converted to an additional layer of graphene and the dangling bonds at the surface of the SiC substrate are passivated by hydrogen bonds (right).

3.1.4 Scattering Processes in Quasi-free Standing Epitaxial Graphene

In this section, we examine the transport properties of epitaxial graphene compared to quasi-free standing epitaxial graphene (QFEG). Bilayer QFEG is derived from epitaxial graphene (EG) via a hydrogen intercalation step that electrically isolates the graphene and SiC substrate, converting the carbon buffer layer into a second layer of graphene and resulting in improved transport properties relative to conventional EG on SiC (mobilities $\sim 3000 \text{ cm}^2 \text{ V}^{-1} \text{ sec}^{-1}$ at a carrier density of $\sim 1 \times 10^{13} \text{ cm}^{-2}$) [65]. After hydrogenation, charged impurity density as well as the extent of phonon scattering induced by the SiC substrate is found to correlate strongly with the presence of step-edges. It is found that additional scattering at the step-edge can often dominate the transport properties of the samples, highlighting the SiC substrate morphology as a key area that needs to be addressed in epitaxial graphene devices.

Acoustic phonon scattering and optical phonon scattering represent the *intrinsic* electron-phonon scattering mechanisms inherent to graphene and are explained using the models employed by Fang *et al* [68], while models for remote surface optical phonon [69] and remote charged impurity scattering [71] are utilized to explain the *extrinsic* scattering mechanisms introduced by substrate and dielectric coating. The intrinsic scattering due to acoustic phonons can be calculated according to Fermi's golden rule and are modeled according to the equation:

$$(7) \quad \frac{1}{\tau_{ac}(k)} = \frac{D_{ac}^2 k_B T}{2 \hbar^3 v_F^2 \sigma_m v_p^2} \times \mathcal{E}_k \quad [68]$$

Here k_B is the Boltzmann's constant, T is the temperature, $\mathcal{E}_k = \hbar v_f |k|$ is the kinetic energy, D_{ac} is the deformation potential, $v_F = 10^6 \text{ cm s}^{-1}$ is the Fermi velocity, $\sigma_m = 7.6 \times 10^{-8} \text{ g cm}^{-2}$ is the 2D mass density of graphene and $v_p = 2 \times 10^6 \text{ cm s}^{-1}$ is the acoustic phonon velocity in graphene. Both acoustic phonon absorption and emission are taken into account. For optical phonons, the scattering rate is given by:

$$(8) \quad \frac{1}{\tau_{op}(k)} = \frac{D_o^2 \left(N_{op} + \frac{1}{2} + \frac{1}{2} \right)}{2\hbar^2 v_F^2 \sigma_m \omega_0} \times [\mathcal{E}_k \pm \hbar\omega_0] \quad [68]$$

where D_o is the optical deformation potential of graphene, $\hbar\omega_0$ is the optical phonon energy and $N_{op} = \frac{1}{e^{\frac{\hbar\omega_0}{k_B T}} - 1}$ is the optical phonon number, \pm is for phonon absorption and emission respectively. For the

extrinsic scattering methods, surface optical phonon scattering is given by:

$$(9) \quad \frac{1}{\tau_{SO}(k)} = \frac{e^2 F_v^2 N_{SO} \sqrt{n_s}}{\beta \hbar \exp(k_0 z_0)} \times \frac{1}{\varepsilon_k} \quad [69]$$

where $k_0 \approx \sqrt{\left(\frac{2\omega_{SO}}{v_F}\right)^2 + \alpha n_s}$, z_0 is the van der Waal's distance between the deposited dielectric/substrate and the graphene, $F_v^2 = \frac{\hbar\omega_{SO}}{2\pi} \left(\frac{1}{\varepsilon_\infty + 1} - \frac{1}{\varepsilon_0 + 1} \right)$ is the Frohlich coupling parameter, $\hbar\omega_{SO}$ is the surface phonon energy, ε_0 and ε_∞ are the low- and high-frequency dielectric constants of the polar high- k , N_{so} is the occupation number of the SO phonons. β is used as a fitting parameter. The scattering rate due to charged impurities present in the graphene-dielectric interface is given by:

$$(10) \quad \frac{1}{\tau_{imp}(k)} = \frac{n_{imp}}{\pi \hbar} \left(\frac{e^2}{2\varepsilon_0 \varepsilon_{avg}} \right)^2 \frac{F(a)}{\varepsilon(k)} \quad [71]$$

where n_{imp} is the sheet density of impurities at the interface, $\varepsilon_{avg} = (\varepsilon_{top} + \varepsilon_{bottom})/2$ is the average relative dielectric constant of the two dielectrics surrounding graphene. Where $a = \alpha (k_F/k)$ and α is the fine-structure constant. $F(a)$ is given as 0.1 according to Jean (dimensionless), while $E_k = \hbar/2\pi v_F \sqrt{\pi n}$. The total scattering rate is calculated by cumulating the rates for each scattering mechanism:

$\tau_{tot} = (\tau_{ac}^{-1} + \tau_{op}^{-1} + \tau_{SO}^{-1} + \tau_{imp}^{-1})^{-1}$. The mobility is related to scattering time as $\mu = \frac{ev_F^2 \tau_{tot}}{E_F}$ [70].

The extrinsic scattering mechanisms of surface optical phonon scattering and remote charged impurity scattering are often cited as the major contributing factors limiting charge transport in practical graphene devices [71] and, in this work, are found sufficient to model the experimental results, although recent work by Ong *et al* suggests that a full understanding of the scattering processes can only be obtained by also considering the dynamical response of graphene plasmons to the surface polar phonon modes [72]. The consideration of coupling between graphene plasmons and surface polar phonon modes, as suggested by Ong *et al*, leads to the formation of interfacial plasmon-phonon modes that can lead to additional screening, or anti-screening, of the remote surface optical phonons [72]. In this work, the additional screening or amplification of remote surface optical phonons is partially captured by a fitting parameter which scales their contribution.

Remote charged impurity scattering has been investigated extensively within the literature [73] and is often the result of dangling bonds or charged defects at or near the substrate-graphene and dielectric-graphene interfaces that act as long-range scatterers. In graphene, remote charged impurity dominated transport exhibits a constant mobility away from the Dirac point, which is evidenced by a conductivity that is linearly dependent on carrier concentration. Due to the unique dispersion relation of graphene, these defects lead to degradation of carrier mobility that remains constant with temperature (*temperature independent*). Alternatively, remote surface optical phonon scattering leads to a degradation of carrier mobility that varies with temperature (*temperature dependent*). This type of scattering is a result of a non-vanishing decaying electric field at the surface of the substrate or dielectric which arises due to the presence of surface optical phonon modes that propagate longitudinally along the surface of the substrate and dielectric overlayer and in close proximity to the graphene. The presence of this non-vanishing, time-varying electric field at the graphene-substrate and graphene-dielectric interfaces leads to additional scattering of the carriers, which is based on the characteristic energy of the surface optical phonon modes as well as the degree of electron-phonon coupling across the interface.

In this work, an acoustic deformation potential of 4.8 eV, optical deformation potential of 25.6 eV \AA^{-1} [68, 74], and intrinsic optical phonon energy of 160 meV [75] are selected based on previous results and are utilized to explain the *intrinsic* scattering of the samples. On the other hand, *extrinsic* scattering is found to depend critically on both substrate and dielectric material. For the case of as-grown QFEG (no dielectric coating), room temperature Hall effect measurements show that the presence of step-edges in the SiC substrate lead to decreased mobility as well as increased hole doping in the graphene. Figure 15 confirms the presence of step-edges, using optical interferometry on the graphene Van der Pauw test structures to measure the step-edge height and density.

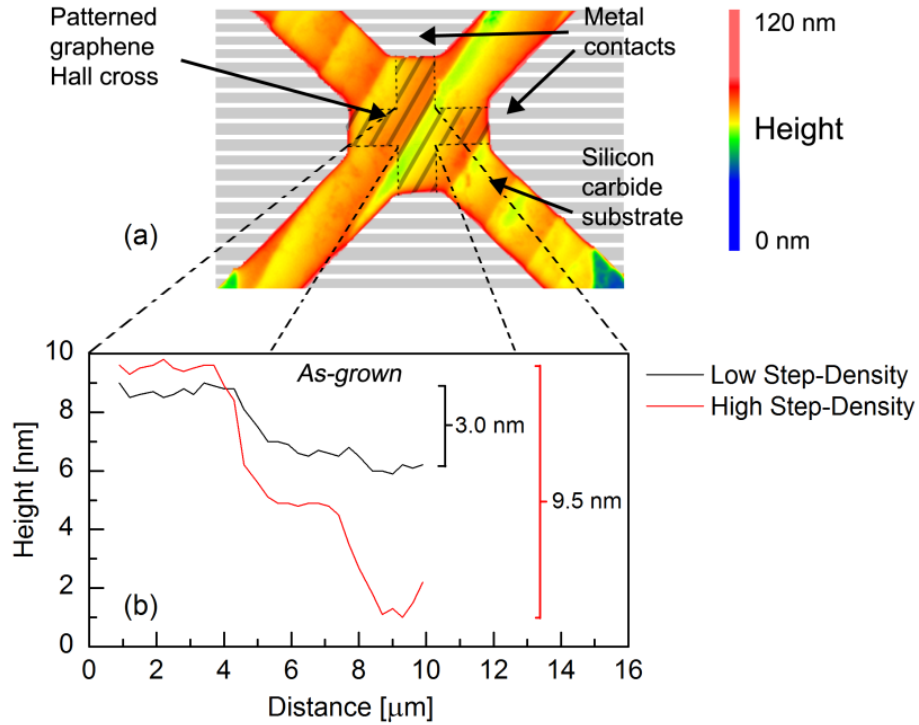


Figure 15. (a) Height map of Van der Pauw cross showing the presence of step-edges across the structure along with (b) extracted height profiles for low and high step-edge density samples

In Figure 15, the low and high step-edge density plots correspond to two different Van der Pauw test structures with varying amounts of step-edges. Figure 16a and 16b are 2-dimensional color maps of the full width half max of the 2D peak of the graphene Raman signature for two different these two samples. Here, bilayer graphene on the step terraces is typically $\sim 50 \text{ cm}^{-1}$ and multi-layer graphene on the step-edges is $\sim 75 \text{ cm}^{-1}$, identified by peak fitting [76,77]. Across the surface of the sample, the extent of step-bunching is found to vary, with some Van der Pauw test structures showing a large change in step height (high density of step-edges) across the active region, with others showing significantly less (low density of step-edges) (Fig. 16a, 16b).

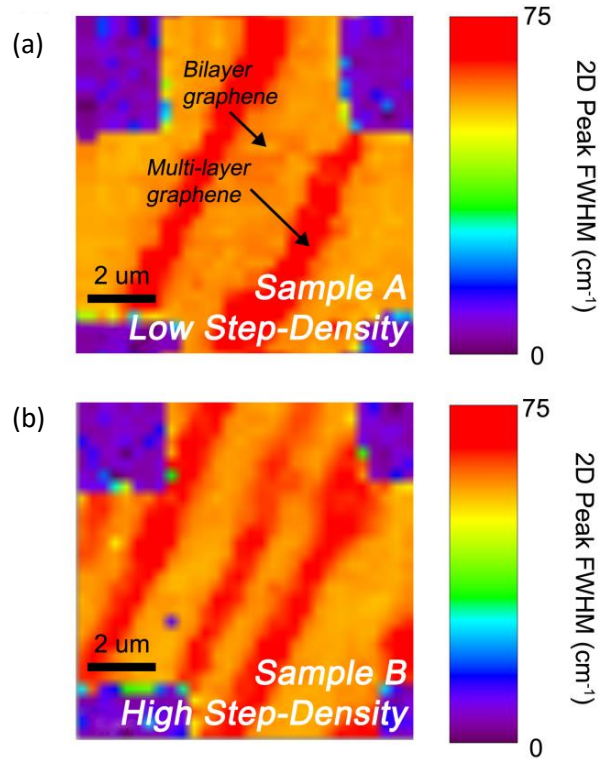


Figure 16. (a),(b) Raman maps of the 2D peak full width half max showing the presence of bilayer graphene across the step terrace and multi-layer graphene at the step-edge.

For these samples, the optical interferometry measurement is utilized to capture the surface topology of as-grown graphene Van der Pauw structures, shown in Figure 15a. From these surface maps, the absolute change in step height across the $5 \times 5 \text{ }\mu\text{m}$ structure is calculated, shown in Figure 15b. The low and high step-density height profiles shown in Figure 15b correspond to the low and high step-density Raman maps in Figure 16. For QFEG samples, the effect of step-edges on measured mobility is shown in Figure 17, where the room temperature Hall mobility and carrier concentration are plotted as a function of absolute change in step-height (i.e. total distance traveled along the vertical axis (c-axis)). As can be seen in Figure 17a,b, there is a strong correlation between Hall mobility, carrier concentration, and step-edge density. Increased absolute change in step-height (increased step-edge density) leads to decreased Hall mobility as well as increased hole concentrations, yet the expected dependency of mobility on carrier concentration at high carrier densities is found insufficient to explain the change in mobility between the low and high step-edge density samples. Fig 17b plots the measured Hall mobility versus carrier density as well as the simulated dependency of mobility on carrier concentration. These results suggest that not only are step edges a source of additional scattering, but that they also lead to an increase in hole doping. Although these and previous results within the literature clearly indicate step-edges as a source of additional scattering, little focus has been given as to what specific scattering mechanisms are responsible for the degradation in transport properties.

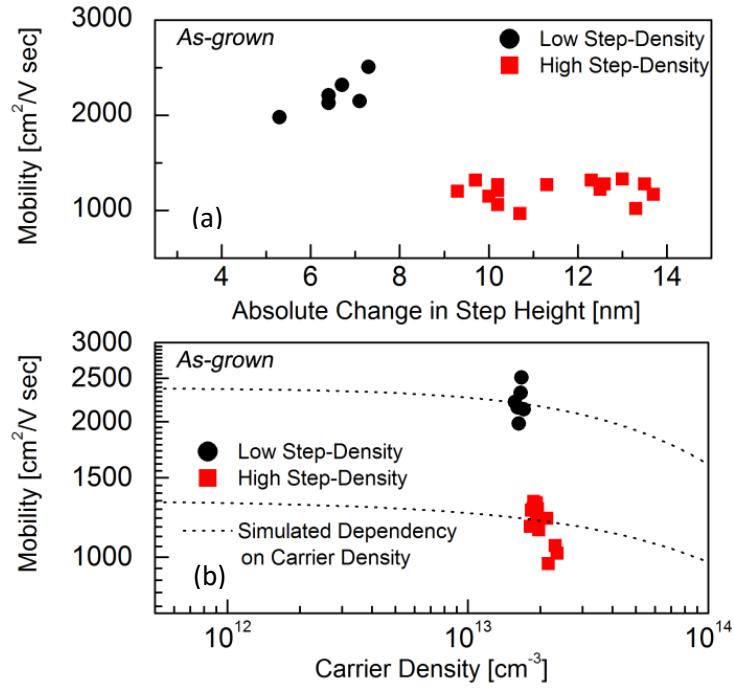


Figure 17. (a) Plot of room temperature Hall mobility versus extracted absolute change in step-height and (b) Hall mobility versus carrier density showing the negative impact of high step-densities on transport.

To understand the degradation of mobility at the step-edge for as-grown graphene samples, temperature dependent Hall measurements are used, showing an increase in remote charged impurity scattering and remote surface optical phonon scattering for high step-edge density samples. The extent of remote charged impurity scattering and remote surface optical phonon scattering is determined by applying the intrinsic and extrinsic scattering models to temperature dependent Hall effect measurements (Fig. 18).

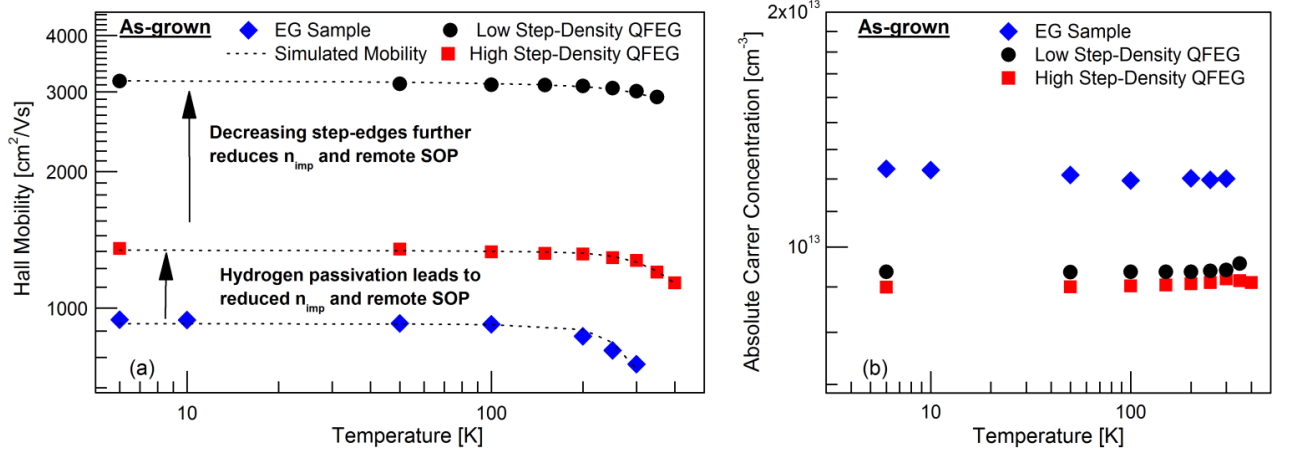


Figure 18. (a) Plot comparing as-grown EG to high and low step-density QFEG samples, showing the reduction in remote charged impurity and remote surface optical phonon (SOP) scattering with hydrogen passivation and with decreasing step-edge density, indicating that step edges are a likely source of both scattering processes. (b) Temperature dependency of carrier density for the samples.

An effective remote impurity concentration, n_{imp} , and a remote phonon scattering fitting parameter, β , as a function of step-edge density are then extracted from the simulated data. As mentioned previously, this remote phonon scattering fitting parameter allows us to account for the additional screening or anti-screening of remote phonons that occurs due the formation of interfacial plasmon-phonon modes and not accounted for in the models utilized in this work. Figure 18 plots the temperature dependent Hall mobility of two QFEG samples and one EG sample while Table 4 reports the extracted values of n_{imp} and β . Below 200 K, the QFEG and EG samples exhibit Hall mobilities that are temperature independent and limited by remote charged impurity scattering to values ranging from 1000 to 3000 $\text{cm}^2 \text{V}^{-1} \text{sec}^{-1}$ at carrier densities near $1 \times 10^{13} \text{ cm}^{-2}$. From this temperature independent region, the effective remote impurity concentration, n_{imp} , is extracted from the scattering model.

Table 4. Fitting parameters for as grown EG and QFEG samples

fitting parameter	EG Sample 1	QFEG Sample 1	QFEG Sample 3
D_{AC}	4.8 eV	4.8 eV	4.8 eV
D_0	25.6 eV A ⁻¹	25.6 eV A ⁻¹	25.6 eV A ⁻¹
$\hbar\omega_0/2\pi_{(\text{graphene})}$	160 meV	160 meV	160 meV
$\hbar\omega_{SO}/2\pi_{(\text{SiC})}$	116 meV	116 meV	116 meV
$\epsilon_{r,\text{substrate}}/\epsilon_{r,\text{air}}$	9.7 / 1	9.7 / 1	9.7 / 1
$B_{\text{substrate}}$	5.56	0.67	0.01
n_{sheet}	1.2e13 cm ⁻²	9.1e12 cm ⁻²	9.3e12 cm ⁻²
n_{imp}	8.4e12 cm ⁻²	5.8e12 cm ⁻²	3.7e12 cm ⁻²

As can be seen in Figure 18, hydrogen passivation of the SiC results in a substantial reduction of $2.4 \times 10^{12} \text{ cm}^{-2}$ in n_{imp} , which is attributed to the effect of increased spacing between the graphene and SiC substrate as well as the passivation of defects and dangling bonds at the graphene-SiC interface after hydrogen intercalation. Importantly, for the QFEG samples it is found that there is an additional reduction in n_{imp} of up to $1.7 \times 10^{12} \text{ cm}^{-2}$ by moving from a high step-edge density sample to one with low step-density. These results suggest that the step-edge is a primary source of remote charged impurities. Reducing the step-edge density leads directly to a reduction in charged impurities and, subsequently, remote charged impurity scattering and enhanced mobility. The reduction of n_{imp} with decreased step-edge density can also help to explain the dependency of carrier density on step-density which was observed in Figure 17, where charged impurities near the graphene can electrostatically dope the graphene.

Above 200 K, the effect of remote surface optical phonon scattering from the substrate (*extrinsic*) as well as phonon scattering within the graphene (*intrinsic*) leads to a decrease in Hall mobility with increasing temperature. In this temperature range, we find that there is a strong correlation between substrate morphology and the *extrinsic* phonon scattering fitting parameter, β , which quantifies the extent of remote surface optical phonon scattering induced by the underlying SiC

substrate. As can be seen in Figure 18, hydrogen passivation of the SiC can result in a significant reduction in remote surface optical phonon scattering, which is represented as a significant decrease in the fitting parameter (Table 4). A similar reduction in remote surface optical phonon scattering has been reported elsewhere [64] and is likely the combined effect of increased spacing between the graphene and SiC substrate and an alteration of the surface optical phonon dispersion after hydrogen termination. Furthermore, it is found that the reduction in remote surface optical phonon scattering with hydrogen intercalation is highly dependent on the presence of step-edges, where increasing step-edge density leads to increased contribution from phonon scattering. These results show for the first time that step-edges may be a source of additional phonon scattering. This may be a result of incomplete hydrogen passivation at the step-edge or, possibly, due to decreased phonon energy for phonons propagating in the c-axis of the SiC crystal. Alternatively, Langer *et al* showed that the presence of a high step-edge density can lead to damping of plasmon modes in graphene on SiC [78]. The damping of plasmon modes in the graphene could lead to reduced screening of remote phonons as shown by Ong *et al* [72]. Further work is needed to analyze how hydrogen passivation occurs at the step-edge as well as how it effects the phonon dispersion relation at the SiC surface. On the other hand, it is clear from Figure 18 that as step edge density is reduced for the QFEG samples, there is a dramatic reduction in β to the point that the underlying SiC substrate results in negligible additional scattering due to remote surface optical phonon scattering for the high mobility (low step-edge density) sample (QFEG Sample 3, Fig. 18). For this sample, the temperature dependence of Hall mobility can be explained using only the intrinsic phonon scattering model.

These results confirm that hydrogen passivation of the SiC can be extremely effective in reducing the contribution from both remote charged impurity and remote surface optical phonon scattering from the underlying substrate. Furthermore, these results suggest that additional scattering at the step-edge can often dominate the transport properties of the samples and highlight the SiC

substrate morphology as a key area that needs to be addressed in epitaxial graphene devices. By reducing step-edge density, mobility can be significantly improved more than $2\times$.

3.2 Integration of Dielectric Top-Gate with Graphene

In recent years, hexagonal boron nitride (h-BN) has gained interest as a material for use in graphene based electronics due to its unique material properties. Its two-dimensional structure, insulating properties, and close lattice match (1.7%) [79] to graphene have made it a natural candidate for dielectric integration, while its low surface roughness and lack of dangling bonds have been cited as potential characteristics that may lead to improved transport properties for graphene devices [80, 81, 82, 83, 84]. These unique features make h-BN suitable for use as supporting substrate or gate dielectric in graphene based transistors. Initial work has shown that use of h-BN for such functions can in fact lead to a $2\text{-}3\times$ enhancement of effective mobility and on-state currents compared to conventional dielectrics [80, 81, 82, 83, 84]. In these works, increased mobility has been attributed to a reduction in surface roughness scattering, remote charged impurity scattering, and remote surface optical phonon scattering relative to thermally grown SiO_2 substrates and ALD deposited high-k gates to which the h-BN integrated devices were compared; however, no comprehensive study of scattering processes on h-BN supported graphene has yet been performed. Additionally, these results suggest that h-BN may be suitable as a top-gate dielectric in other graphene devices (one's not supported by SiO_2 substrates) in order to improve device performance by reducing scattering from these same processes; yet, all work on h-BN integration has thus far focused on exfoliated or chemical vapor deposited (CVD) graphene, both of which are typically placed on SiO_2 supporting substrates. Alternatively, high-k dielectrics can lead to enhanced transport properties through dielectric screening of remote charged impurities [71,

85], yet are thought to lead to increased surface optical phonon scattering [71]. In order to achieve the highest possible device performance, the effects of h-BN integration must be understood. Although initial experimental work has shown excellent promise for h-BN integration with certain graphene systems, more work is needed to model and understand the scattering physics of this system and to identify the regimes and systems it is most applicable to.

In this section, we examine the large-area integration of synthetic h-BN with bilayer QFEG for the first time and compare it to the high-k dielectric, HfO₂. Bilayer QFEG is derived from EG via a hydrogen intercalation step. HfO₂ dielectrics (20 nm thick) are deposited using an oxide seeded ALD (O-ALD) technique previously described elsewhere [85]. Hexagonal boron nitride (10 nm thick) is grown on 99.8% pure Cu foils (Alfa Aesar, part #13382) in a 75 mm diameter horizontal tube furnace *via* a catalytic thermal CVD method utilizing a single ammonia borane (NH₃BH₃) precursor (Sigma-Aldrich, part #682098). The Cu foils are cleaned in a heated acetone bath and subsequently annealed at 800 °C, 1 Torr for 20 minutes under H₂/Ar (15% H₂) flow to remove the native oxide. Solid ammonia borane powder is sublimed at 135 °C and transported into the tube furnace by H₂/Ar carrier gas (5% of total flow rate). Growth occurs at 1050 °C and 250 mTorr with growth times between 5-30 minutes, depending on desired film thickness. After the growth procedure, the ammonia borane carrier gas is turned off and the furnace is allowed to slowly cool to room temperature in a 250 mTorr Ar/H₂ environment. The Cu substrate is removed using a ferric chloride solution, similar to previously reported techniques for transfer of CVD grown graphene from Cu [86]. The remaining PMMA/h-BN film is then transferred to a series of water baths to remove residual etchant and subsequently transferred to the final substrate. Electrical evaluations and large area development are accomplished using 2 × 2 square inch h-BN films transferred to 75 mm QFEG wafers previously patterned with ohmic level device structures. The PMMA is then removed with acetone and the h-BN / substrate is heated to 50 °C to drive off residual water. Removal of residual PMMA is accomplished *via* a post-transfer anneal at 400 °C for 20 minutes. For wafers with graphene devices, the h-BN dielectric layer is patterned and

etched with an Applied Materials MERIE using a CHF_4/CF_4 mixture to clear the ohmic contacts of h-BN. Thickness was determined through AFM measurements performed on the edges of the transferred h-BN films. The thickness of the h-BN film is controlled by varying the growth time, where films from a few layers up to 50nm thick have been grown and successfully transferred to arbitrary substrates. Temperature dependent Hall measurements of Van der Pauw test structures are acquired using a Lakeshore cryogenic probe station.

Although it is difficult to accurately model the complicated morphology of the QFEG on SiC samples, temperature dependent Hall effect measurements in conjunction with models for the scattering physics of ideal monolayer graphene (Section 3.1.4) are used to discern the relative effects of top-gate dielectric on carrier transport and confirm that integration of synthetic h-BN with QFEG is effective in reducing the relative density of remote charged impurity scatterers as well as remote surface optical scattering introduced by the dielectric overlayer and can be an excellent dielectric for preserving the charge transport properties of high mobility graphene samples, where step-edges are not dominant. The results show a 2x increase in mobility for h-BN dielectrics while the scattering model indicates that h-BN dielectrics can ultimately lead to a >5x increase in mobility relative to HfO_2 based dielectrics due to higher energy surface optical phonon modes and reduced scattering; however, the overall benefit of h-BN dielectrics is found to depend critically on the charged impurity density within the dielectric-graphene system, which acts to offset the benefit of synthetic h-BN dielectrics relative to high-k dielectrics such as HfO_2 .

3.2.1 The Benefit of h-BN as a Two-Dimensional Gate Dielectric

After dielectric integration the impurity density, n_{imp} , is found to increase for both h-BN and HfO_2 coated QFEG samples, indicating that both dielectrics introduce additional charged defects into the system. Yet while both dielectrics are found to increase n_{imp} , h-BN overlayers lead to an *increase*

in the hole concentration while HfO_2 overlayers lead to a *decrease* in the hole concentration, indicating p-type and n-type doping of the graphene, respectively. The n-type doping and p-type doping of graphene by HfO_2 and h-BN, respectively, has been reported elsewhere [66, 85, 86]. Figure 19 summarizes the results and plots the experimental data for two *high step-edge density* QFEG samples before and after dielectric integration as well as one *low step-edge density* QFEG sample after dielectric integration while Table 5 details the fitting parameters and room temperature sheet carrier densities.

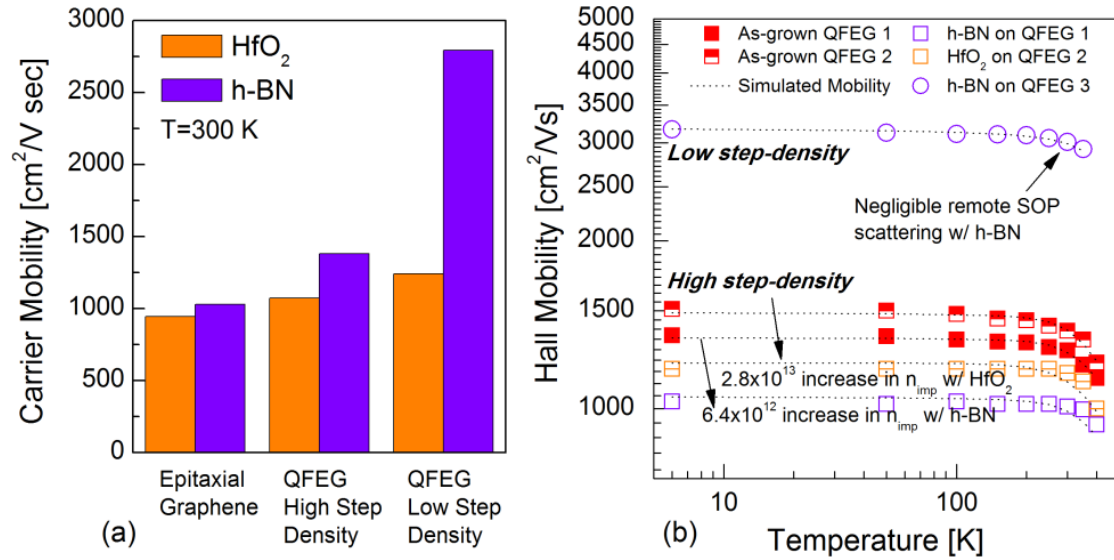


Figure 19. (a) Plot of carrier mobility for HfO_2 and h-BN coated samples on different substrates. (b) Temperature dependent mobility for as-grown and dielectric coated samples.

Table 5. Fitting parameters for dielectric coated QFEG samples and Ref. [87]

fitting parameter	HfO ₂ on QFEG1	h-BN on QFEG2	h-BN on QFEG3	CVD Graphene on SiO ₂
D_{Ac}	4.8 eV	4.8 eV	4.8 eV	4.8 eV
D₀	25.6 eV A ⁻¹	25.6 eV A ⁻¹	25.6 eV A ⁻¹	25.6 eV A ⁻¹
ħω₀/2π_(graphene)	160 meV	160 meV	160 meV	160 meV
ħω_{SO}/2π_(SiC)	116 meV	116 meV	116 meV	--
ħω_{SO1}/2π_(dielec.)	75 meV	160 meV	160 meV	70 meV
ħω_{SO2}/2π_(dielec.)	--	--	--	149 meV
ε_{r,substrate} / ε_{r,dielec.}	9.7 / 17	9.7 / 4	9.7 / 4	4/1
B_{substrate}	0.67	0.67	0.01	0.22
B_{dielectric}	0.25	0.01	0.01	--
n_{sheet}	5.4e12 cm ⁻²	1.3e13 cm ⁻²	9.3e12 cm ⁻²	1.0e12 cm ⁻²
n_{imp}	1.5e13 cm ⁻²	9.2e12 cm ⁻²	3.0e12 cm ⁻²	3.6e11 cm ⁻²
Δn_{sheet}	3.7e12 cm ⁻²	1.8e12 cm ⁻²	--	--
Δn_{imp}	6.6e12 cm ⁻²	3.4e12 cm ⁻²	--	--

QFEG Sample 1 is coated with oxide seeded ALD deposited HfO₂ while QFEG Samples 2 and 3 are coated with transferred synthetic h-BN. The results indicate that h-BN integration is most beneficial for low step-edge density samples, but shows little benefit for high step-edge density samples (Fig. 19a). Integration of h-BN leads to an increase in n_{imp} of $3.4 \times 10^{12} \text{ cm}^{-2}$ while integration of ALD deposited HfO₂ leads to a ~2x greater increase in n_{imp} ($6.6 \times 10^{12} \text{ cm}^{-2}$). These results suggest that use of h-BN can be beneficial by limiting the incorporation of additional remote charged impurities, yet Figure 20 shows that the overall change in mobility after dielectric integration is roughly the same for HfO₂ and h-BN coated QFEG samples 1 and 2 at a carrier density of $1 \times 10^{13} \text{ cm}^{-2}$ (20% and 21% degradation respectively).

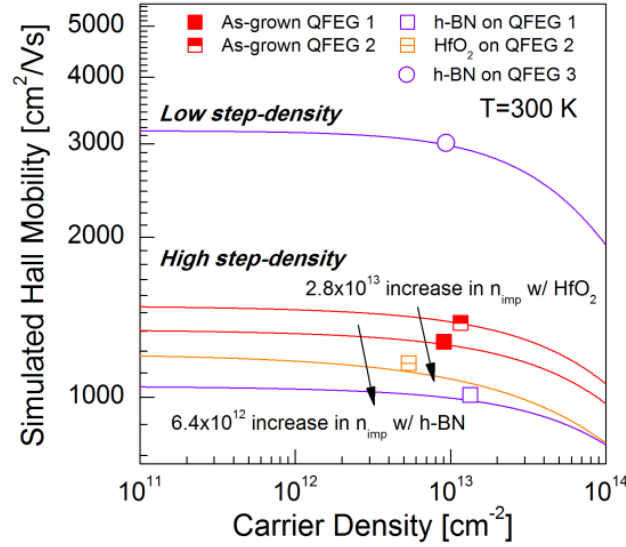


Figure 20. Simulated mobility as a function of carrier density before and after dielectric integration, showing the increased remote optical phonon scattering of the HfO₂ dielectric at high carrier concentrations.

These results are explained by the additional effect of the high-k dielectric to screen the graphene from remote charged impurities, whereby the larger dielectric constant acts to offset the additional charged impurities introduced by HfO₂. Alternatively, Figure 20 indicates that the benefit of dielectric screening will gradually lose out to increased remote surface optical phonon scattering as carrier density increases due to the lower energy surface optical modes and increased electron-phonon coupling of the HfO₂ coating. Figure 21 plots the percent contribution of the various scattering processes for the different samples, indicating that remote charged impurity scattering dominates all three samples and contributes as much as 94% of the total scattering at a carrier concentration of $1 \times 10^{13} \text{ cm}^{-2}$. Additionally, it is found that remote surface optical phonon scattering constitutes a higher *percentage* of the total scattering processes in the HfO₂ coated sample (11%) as compared to the h-BN sample (1-2%) due primarily to the fact that h-BN introduces negligible additional remote surface optical phonon scattering over that introduced by the SiC substrate. The integration of h-BN with *low*

step-edge density QFEG (QFEG Sample 3) shows minimal temperature dependency and confirms that h-BN introduces negligible additional remote surface optical phonon scattering, indicating that h-BN is excellent at preserving the mobility of high quality graphene samples.

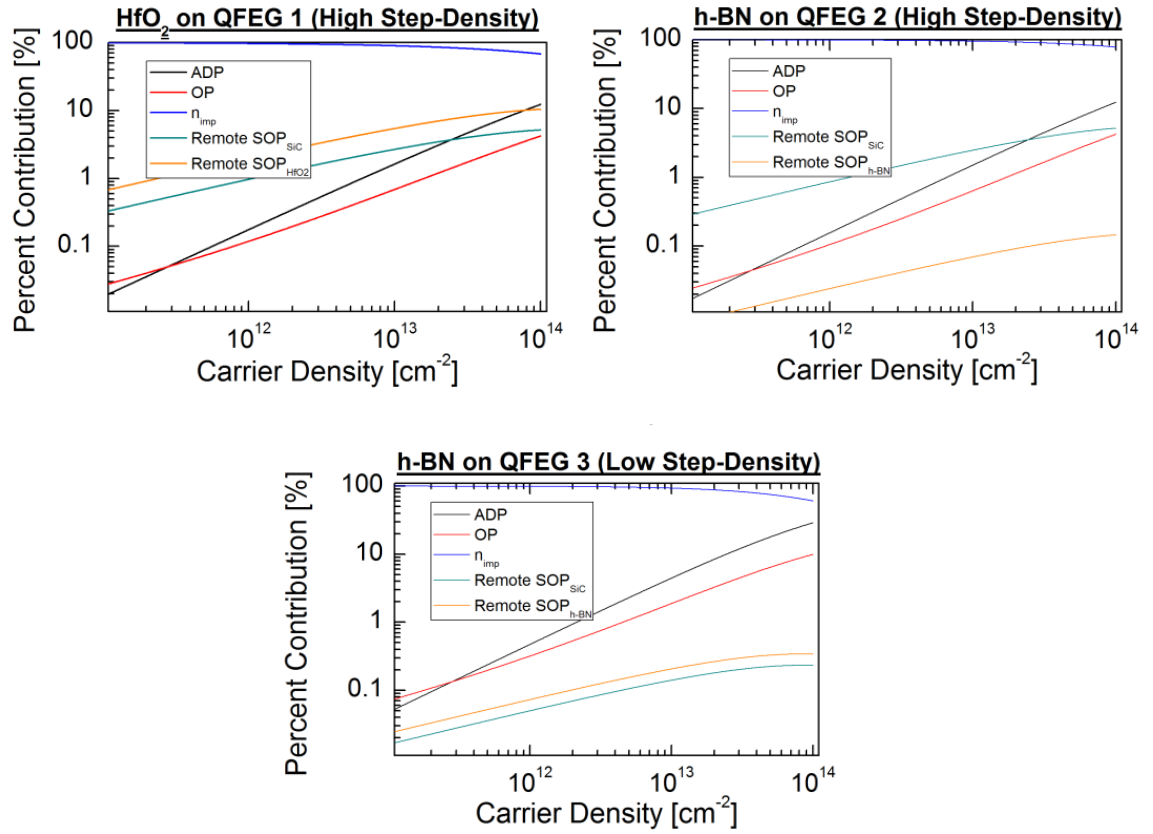


Figure 21. Percent contribution of the various scattering processes contributing to total mobility as a function of carrier density, showing the dominance of remote charged impurity scattering for both dielectrics and minimal contribution from remote surface optical phonon scattering with h-BN dielectric.

Although the integration of HfO₂ and h-BN with *high step-edge density* QFEG shows relatively little gain in performance when utilizing h-BN, *low step-edge density* QFEG benefits significantly with a $\sim 2.6\times$ increase in Hall mobility to values $>3000 \text{ cm}^2 \text{ V}^{-1} \text{ sec}^{-1}$, emphasizing that the overall benefit of

h-BN dielectrics is highly dependent on the effective remote charged impurity density, n_{imp} . To this end, Figure 22 plots the simulated percent increase in mobility when using h-BN over HfO₂ dielectrics on QFEG at a fixed carrier density of $1 \times 10^{13} \text{ cm}^{-2}$ along with the experimental results.

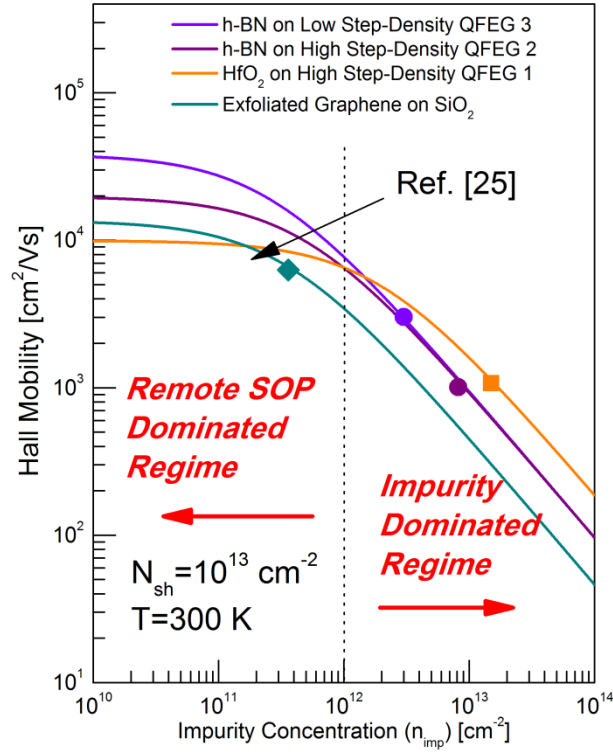


Figure 22. Plot of simulated Hall mobility as a function of remote charged impurity density showing the benefit of dielectric screening at high impurity densities and the benefit of low remote surface optical phonon scattering at low impurity densities at a fixed temperature of 300 K and carrier concentration of $1 \times 10^{13} \text{ cm}^{-2}$.

The results are also compared to exfoliated graphene on SiO₂ [87]. With impurity densities above $2 \times 10^{12} \text{ cm}^{-2}$, QFEG mobility is limited to values $< 6000 \text{ cm}^2 \text{ V}^{-1} \text{ sec}^{-1}$ for sheet carrier densities of $1 \times 10^{13} \text{ cm}^{-2}$. In this regime, remote charged impurity scattering is the dominant scattering mechanism and acts to quench the benefit of h-BN dielectrics, yet high-k dielectrics are able to recover

transport properties through dielectric screening and can outperform both h-BN and SiO₂. However, for impurity densities below $2 \times 10^{12} \text{ cm}^{-2}$, remote surface optical phonon scattering in the HfO₂ coated sample begins to contribute more significantly to the total scattering. In this regime and as impurity concentration continues to decrease, QFEG mobility for h-BN samples far surpasses that of HfO₂ coated samples and is predicted to increase to values $\sim 20000 \text{ cm}^2 \text{ V}^{-1} \text{ sec}^{-1}$ for high step-edge density samples (QFEG Sample 2) and $>40000 \text{ cm}^2 \text{ V}^{-1} \text{ sec}^{-1}$ for low step-edge density samples (QFEG Sample 3), similar to values reported for CVD graphene on h-BN substrates [80]. The large difference in mobilities between the h-BN and HfO₂ coated samples found at low impurity densities for this model is due to the reduced contribution of surface optical phonon scattering for h-BN relative to HfO₂. The authors note that these simulations do not take into account the effect of screening and anti-screening due to graphene plasmon - surface polarized phonon coupling and that a more complete treatment may show that remote surface optical phonons as a result of HfO₂ dielectrics may be significantly damped by the dynamic response of the graphene plasmons, as shown by Ong *et al* [72].

In this section, we have analyzed the scattering physics of h-BN coated epitaxial for the first time using temperature dependent transport measurements. It was shown that integration of synthetic h-BN with QFEG is effective in reducing the density of remote charged impurity scatterers as well as remote surface optical scattering and can be an excellent dielectric for preserving the charge transport properties of high mobility graphene samples. An increase in mobility of $2.6\times$ is found while the scattering model indicates that h-BN dielectrics can ultimately lead to a $>5\times$ increase in mobility relative to HfO₂ and SiO₂ based dielectrics due to higher energy surface optical phonon modes; however, the overall benefit of h-BN dielectrics is found to depend critically on the charged impurity density within the dielectric-graphene system, which acts to offset the benefit of synthetic h-BN dielectrics relative to high-*k* dielectrics such as HfO₂.

3.3 The Metal-Graphene Contact as a Limiting Factor in Graphene Based Mixers

Due to the fact that contact resistances often significantly contribute to parasitic resistances which reduce peak transconductance and limit the ultimate achievable cut-off frequency in graphene based RF applications, much research has been dedicated to the investigation into the properties and dynamics of the metal-graphene contact and its effect on graphene devices [40, 88, 89, 90]. Reported contact resistances range from less than 250 $\Omega\text{-um}$ [91] to greater than 1000 $\Omega\text{-um}$ [92] for the same metal and there is generally little agreement between research groups. In turn, there currently exist several explanations for the mechanics of the metal graphene interface and the limiting (controlling) factors which lead to high contact resistances.

Alternatively, it has become clear that as graphene devices are scaled to ultra-short channel lengths the effect of the contact on device performance may not be limited solely to high contact resistances. This is a result of a screening potential, or charge transfer region (CTR), that extends from the metal-graphene interface into the channel. The CTR occurs due to a difference in charge carrier densities underneath the metal contact and within the channel. Between the two regions there exists a transition region which leads to an effective charge transfer into the channel.

3.3.1 Understanding the Charge Transfer Region

Nagashio et al provided a succinct description of the CTR in their recent work [41], defining it as a region of additional charge that extends from the metal contact into the graphene channel as a result of the work function difference between the metal and graphene as well as the low density of states in graphene. This unique phenomenon differs from the case of metal-semiconductor and metal-metal junctions in several key ways.

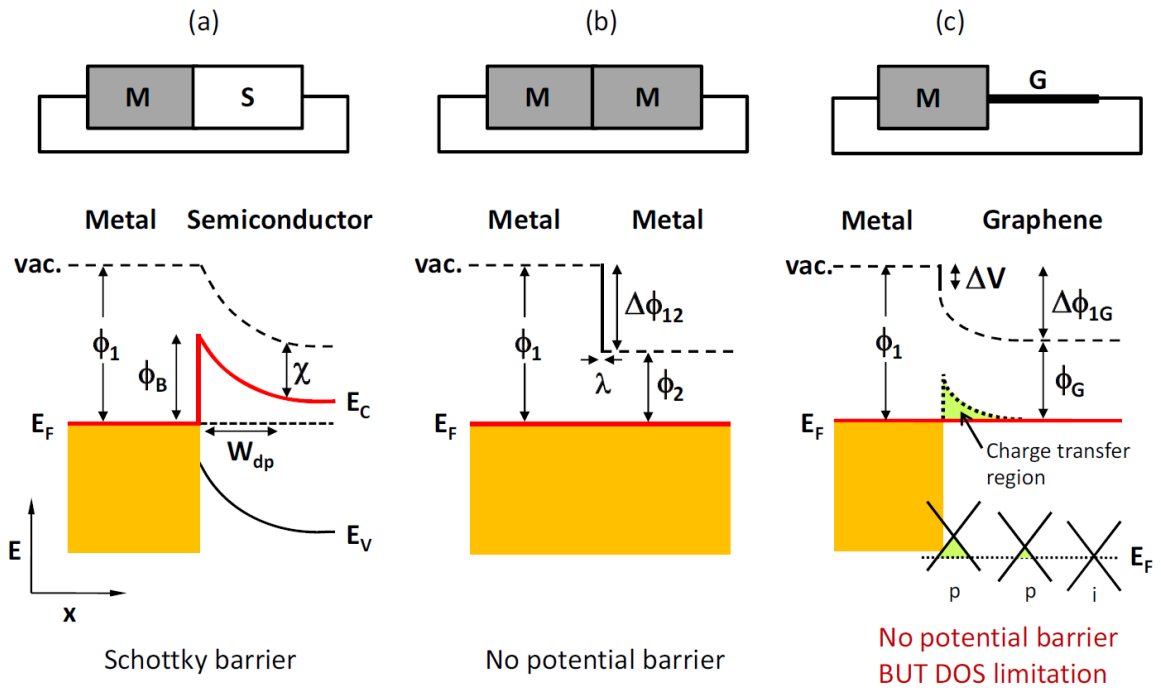


Figure 23: Energy band diagrams for metal-semiconductor (a), metal-metal (b), and metal-graphene junctions. Adapted from Reference [41].

For the case of the metal-semiconductor interface, charge flows between the two materials in order that their electrochemical potentials (i.e., Fermi levels) align. This results in the formation of a

potential barrier at the metal-semiconductor interface, often referred to as a Schottky barrier (Fig. 23a). A depletion layer is formed due to the small density of states in the semiconductor compared to the metal. For the case of a metal-metal junction, no depletion layer forms. This is a result of the fact that the high electron density in the metal can quickly screen the potential difference that occurs at the metal-metal interface (typically within <1 nm) [93]. This results in a sharp change in the vacuum level as shown in Figure 23b. For the case of the metal-graphene interface, the vacuum level is not able to abruptly change at the interface due to a density of states (DOS) limitation within the graphene. This is a result of the vanishing DOS in graphene about the Dirac point and results in the formation of the CTR.

Although no potential barrier forms at the metal-graphene junction as for the case of the metal-semiconductor junction, work by Giovannetti et al shows that a small amount of charge transfer occurs “just” at the metal-graphene interface, effectively doping the underlying graphene [88]. Utilizing density functional theory to study adsorption of various metals onto the surface of graphene [88] shows a shift in the graphene Fermi level by as much as 0.5 eV due to a metal overlayer. The pinned Fermi level of the underlying graphene leads to the formation of an interfacial dipole layer (ΔV) shown in Figure 23c, which depends upon the specific chemical interactions between the metal and graphene at their interface. Away from the metal-graphene interface, the low density of states in graphene and bilayer graphene leads to a long screening length over which this charge transfer decays. The result is a large region extending from the metal-graphene contact which is effectively doped with either electrons or holes due to the Fermi-level pinning at the interface, illustrated as a green region in Figure 23c and referred to as the CTR.

In 2013, [94] were able to measure the length over which the CTR extends to be on the order of 300 – 500nm for the case of mono-layer graphene on bare SiO_2 . Length scales on the order of a micron were measured in a photocurrent study of the metal-graphene contact on bare SiO_2 [95]. Alternatively, Khomyakov et al utilize density functional theory within the Thomas-Fermi

approximation to model the CTR for the case of ideal monolayer graphene on SiO₂ [96]. Their results confirm that screening in graphene is strongly suppressed and lead to the presence of a large CTR that extends as much as 100 nm away from the metal-graphene interface for the simulated case of Ti/Au contacts on graphene on SiO₂. Importantly, they were able to show that the CTR produces a potential decay that roughly follows an $x^{-0.5}$ dependency into the channel, given as [96]:

$$(11) \quad V(x) \approx \frac{V_B}{\left(\sqrt{x/l_{CTR} + \beta_2^2 + \beta_1 - \beta_2}\right)^{1/2} (x/l_{CTR} + \beta_1^{-2})^{1/4}}$$

Furthermore, they indicate that the screening potential remains relatively unchanged for the case of doped or gated graphene. Additionally, the results suggest that surrounding the graphene in a high- k dielectric environment extends the CTR, where the length scale of the potential decay, l_{CTR} , scales directly with the average dielectric constant of the surrounding environment [96].

The effects of the charge transfer region (CTR) have been reported variously throughout the literature [40, 41, 97] and cited as a potential cause for the loss of symmetry and degraded device performance for short channel GFETs. By pinning the Fermi-level at the contacts and introducing additional charge into the device, the CTR acts as an additional parasitic resistance and contributes to asymmetry in the transfer characteristics of the device through the formation of highly resistive p-n-p junctions across the device. These negative effects are particularly pronounced at L_{ch} below 1 μm , where the CTR can extend across a major portion of the active device, significantly shifting the Dirac point and altering the expected performance. Figure 24 schematically illustrates the effect of the CTR on the transfer characteristics and shows the introduction of bias dependent asymmetry into the device for the case of hole-type doping by the metal contacts.

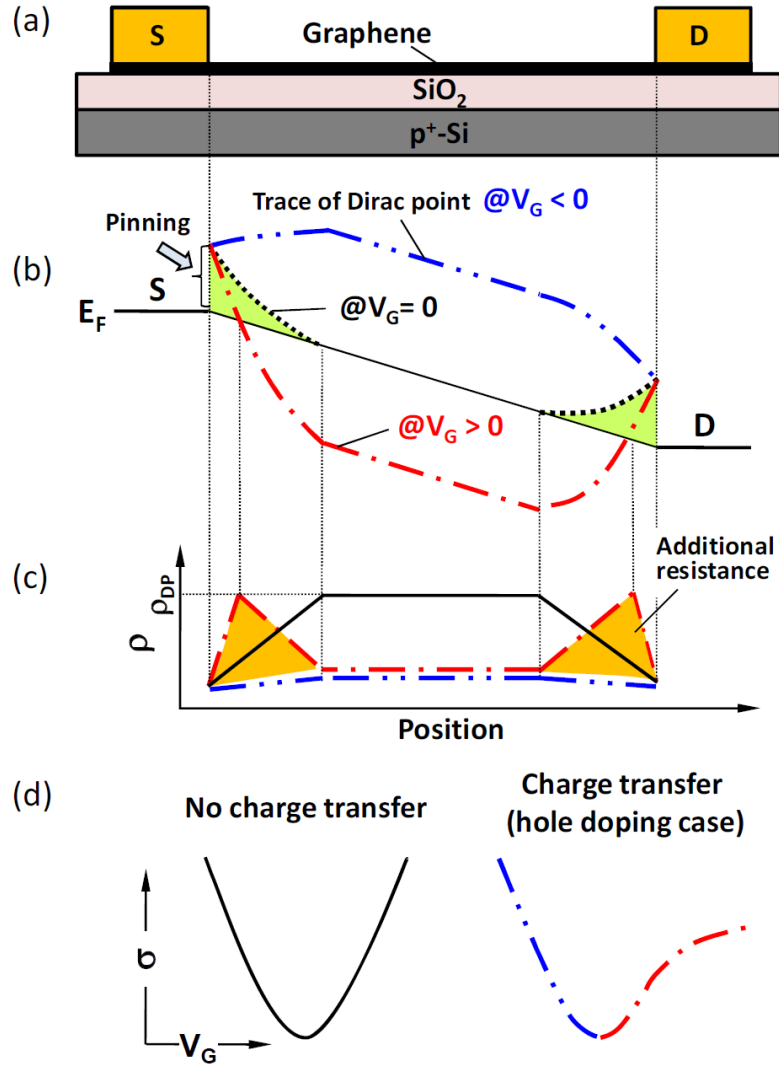


Figure 24: Schematic representation of GFET (a). Band diagram showing Fermi-level pinning and CTR for three different bias conditions (b) and associated resistivity as a function of position within the device (c). Transfer curves with and with out the effect of the CTR (d). Figure adapted from Ref. [41].

In Figure 24b, with no gate bias applied to the device, the CTR extends into the channel introducing hole doping; however, for the case of $V_g > 0$, Fermi-level pinning at the source and drain and the presence of the CTR lead to the formation of two p-n junctions across the device (one at each

metal contact). These p-n junctions act as additional parasitic resistances within the device, where the local resistivity across the channel is plotted in Figure 24c. Here, the local resistivity at the p-n junction is considered to be equivalent to the resistivity at the Dirac point. In contrast, for the case of $V_g < 0$, the CTR results in negligible additional resistance (Fig. 24b,c). This results in an asymmetric transfer characteristic as a result of the CTR (Fig. 24d). Nouchi et al were able to show improved symmetry using easily oxidizable metal contacts as a way to de-pin the graphene Fermi-level at the metal contact.

Besides the incorporation of additional asymmetry into the device, the presence of the CTR also leads to a shift in the minimum conductivity point (V_{Dirac}) [40, 41]. This becomes especially clear as the distance between the source and drain metal contacts is decreased when the CTR begins to comprise a greater and greater ratio of the total channel length. For such short-channel devices, the CTR effectively dopes the entirety of the device. Scaling to short-channel also has an impact on the degree of asymmetry. For the case of the long channel devices, the CTR comprises only a small portion of the total channel resistance, resulting in minimal quenching of the n-branch and a small shift in V_{Dirac} . For the short channel devices, the CTR can completely dominate the device behavior, leading to a significant additional resistance when the device is biased with $V_{gs} > 0$ and also limiting the on-off ratio of the device by lowering the maximum total resistance of the device. The increasing dominance of the CTR at short channel lengths leads to a significant total reduction in peak transconductance which severely degrades the ultimate RF performance of the GFET (Fig. 25b).

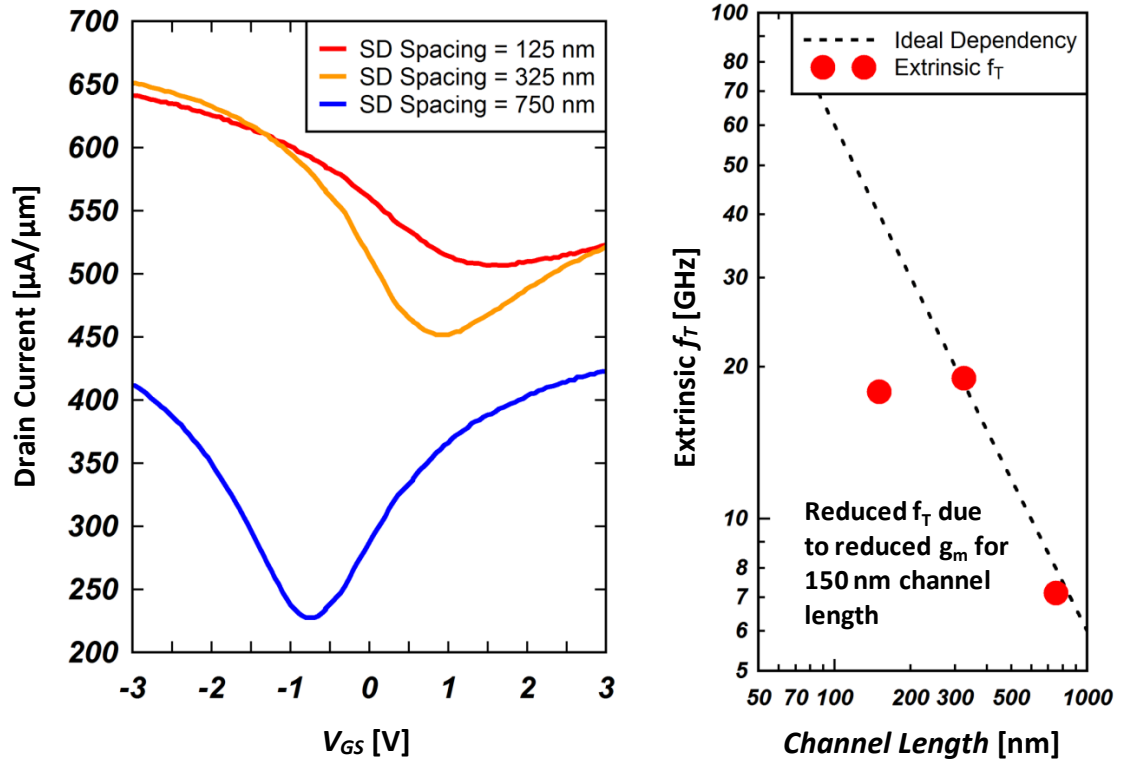


Figure 25: Transfer characteristics for three different channel length devices (a) and their extracted extrinsic current gain cut-off frequencies (b).

3.4 Effect of Nano-ribbon Geometries on Charge Transfer Region

Although great interest exists for the use of graphene nano-ribbons (GNRs) to improve RF device and mixer performance through the opening of a small transport gap, recent work has demonstrated enhanced performance using GNRs with relatively large widths. Ref. [98] reports an improvement in $f_{T,intrinsic}$ of $1.5\times$ to 60 GHz by moving from 100 nm to 40 nm wide nano-ribbons for their multi-ribbon graphene RF FET, while Habibpour *et al* was able to demonstrate an improved on-off ratio of 7 for their resistive graphene mixer utilizing 100 nm wide graphene nano-constrictions with a source-drain spacing of 700 nm [34]. Although these preliminary experimental results have shown

modest performance gains by moving to GNR geometries, GNRs of these widths exhibit modest room temperature bandgaps in the range of 2.5-10 meV [99], which, by themselves, are unlikely to have a significant impact on the room temperature transfer characteristics of these devices. On the other hand, researchers investigating graphene ribbons of even larger widths, ranging from 180 nm to 5 μm , have also shown evidence for improved device performance [100, 101, 102]. In these reports, increased conductivity, effective mobility, and on-off ratios compared to sheet geometries are attributed not to the opening of a small transport gap, but to enhanced conduction as the graphene ribbon is scaled to smaller widths. This enhanced conduction is a result of fringing fields between the ribbon and gate, which lead to accumulation of additional carriers in the ribbon as compared to conventional sheet devices. These reports of enhanced device performance for wide graphene ribbons suggest that a full understanding of the effect of increased gate coupling on device performance is necessary in order to explain the impact of GNR geometries on the performance of graphene based ambipolar mixers.

In order to investigate the effects of GNR geometries on the CTR, sheet and GNR samples are prepared using quasi-free-standing epitaxial graphene on SiC (growth and fabrication details are provided in Section 3.1). Various channel lengths and widths are prepared and HfO_2 gates are deposited in order to evaluate shift in the Dirac point of the transfer characteristics of the devices. Figure 26 shows typical transfer characteristics for sheet (Fig. 26a, blue) and 50 nm wide GNR devices (Fig. 26b, red). In these plots, several different channel lengths are plotted for each case, all with an applied drain bias of 50 mV. The results indicate that GNR geometries can have a significant effect on device performance, altering the shape, on-off ratio, and degree of symmetry of the transfer curve.

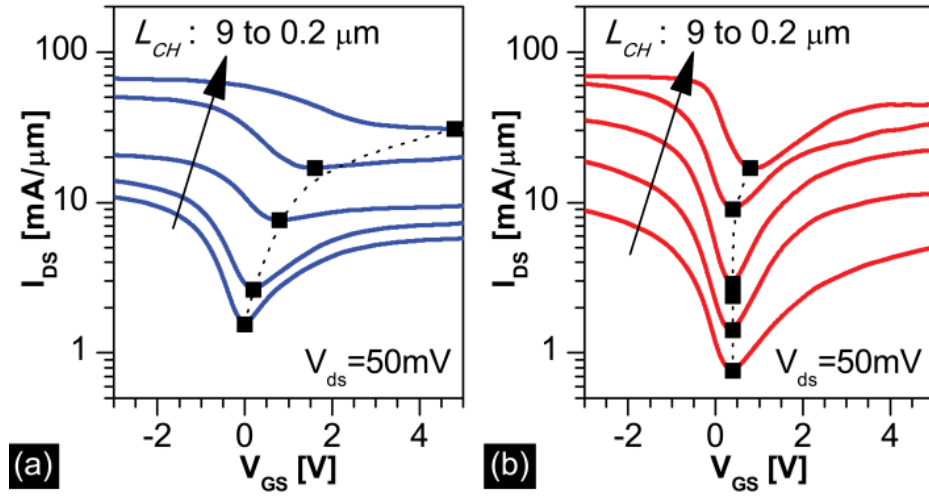


Figure 26: Family of transfer curves for sheet (a) and 50nm wide GNR (b) transistors, showing improved symmetry and reduced Dirac shift for GNR devices.

For both the sheet and GNR devices, the presence of a p-type CTR near the metal contact is expected to lead to a positive shift in V_{Dirac} and quenching of the n-branch as L_{ch} decreases. While the effect of the CTR in reducing p-n symmetry has been described before [41], [97]; it is important to examine how this behavior changes as a function of L_{ch} (short versus long channel) and channel width (sheet versus ribbon). Comparing use of sheet and 50 nm GNR geometries for the long channel case, we see that the Dirac points are close to 0 V for both cases; yet as L_{ch} is decreased, the sheet based devices show a large shift in V_{Dirac} to values greater than 5 V, while GNR devices show significantly reduced V_{Dirac} shift of < 1 V. These results can be explained with a reduction in CTR length for the nano-ribbon geometry. By reducing the CTR length, the additional parasitic resistance associated with the CTR can be minimized, leading to improved symmetry and enhanced transfer characteristics.

Alternatively, the opening of a bandgap may also impact the transfer characteristics or may be responsible for altering the effect of the CTR. Temperature dependent I-V measurements of the 50 nm GNR devices show a dramatic increase in on-off ratio as the sample is cooled below 100K, from ~10

at RT to > 200 at 6K. These results are plotted in Figure 27. The increase in on-off ratio with decreasing temperature matches well with similar results by Han et al, indicating the opening of a transport gap on the order of 5 meV [99].

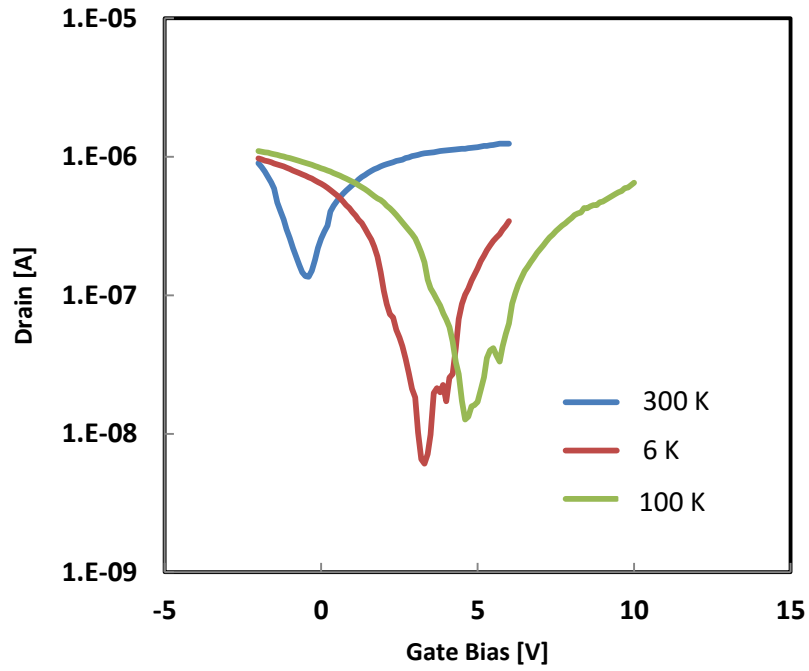


Figure 27. Temperature dependent I-V for 50 nm wide graphene nanoribbon with 6 μm long channel and Ti/Au contact metallization.

In order to pinpoint the effect of channel width on the CTR, samples are also prepared with graphene “ribbons” having widths of 1 and 5 μm . For these devices, on-off ratio improves slightly with decreasing temperature; however, the opening of a transport gap is unrealistic. Improved transfer characteristics are also found for the case of these wide graphene ribbons, which are summarized along with the sheet and 50 nm wide ribbon devices in Figures 28a-d. In these figures, we observe a monotonic increase in performance metrics as ribbon width is decreased. Figure 28a shows a $3\times$

improvement in on-off ratio from 5 to 15 for the long-channel devices. Short-channel on-off ratio also improves, although only from < 2.5 to ~ 3.5 .

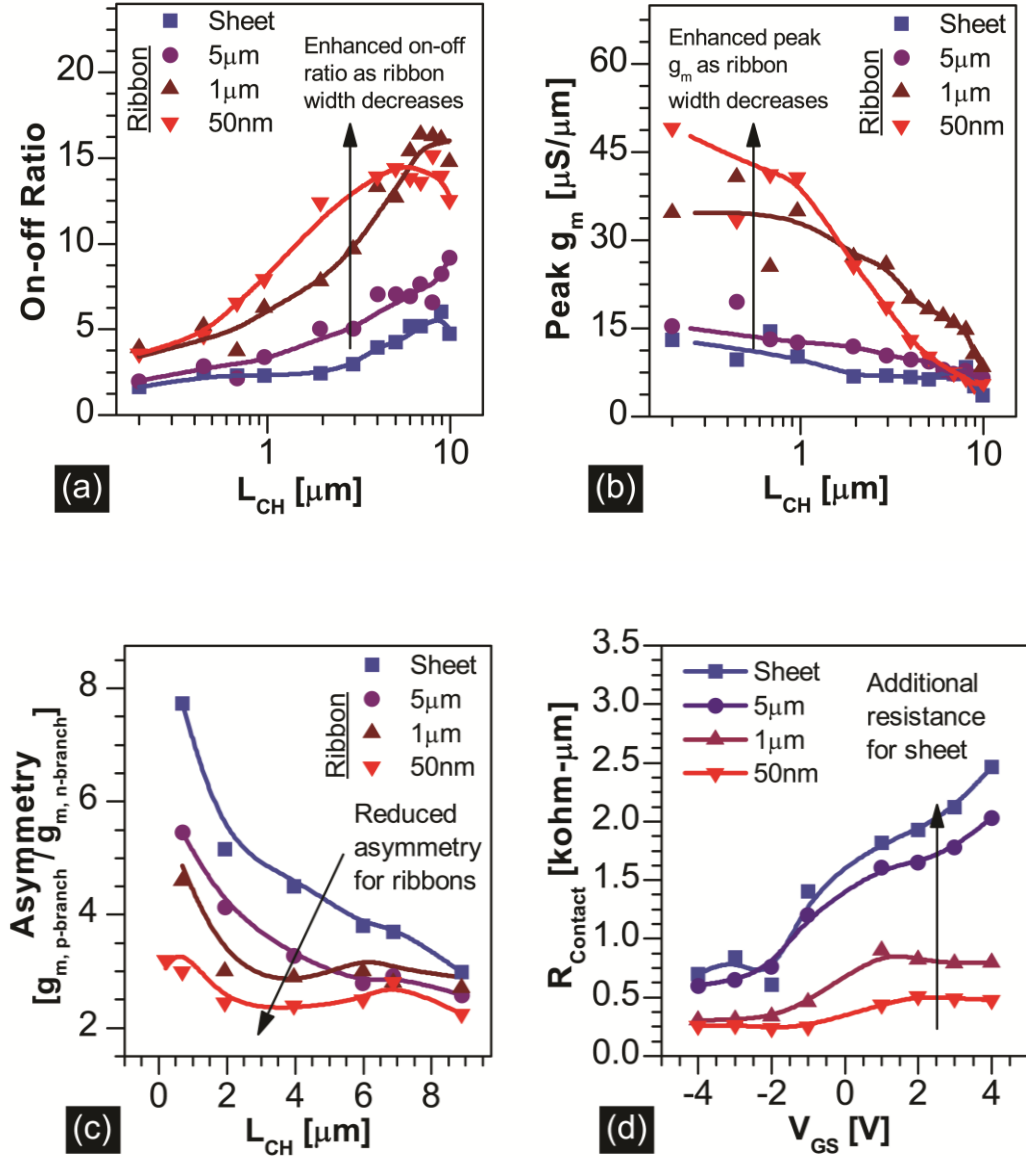


Figure 28: Enhanced on-off ratio (a), peak transconductance (b), and symmetry (c) are attributed to a reduction in parasitic resistance associated with the CTR. Gated TLM measurements directly measure this additional parasitic resistance (d).

Similarly, short-channel device transconductance improves with decreasing ribbon width (Fig. 28b), showing an increase of more than $3\times$ to $\sim 50\mu\text{S } \mu\text{m}^{-1}$ at a drain bias of 50 mV; however, we note that long-channel performance of the 50nm ribbon is significantly degraded compared to all other widths. This is attributed to additional edge roughness scattering for the 50 nm wide graphene nano-ribbon, where additional scattering is expected for GNRs with width less than 200 nm [101]. Although an increase in transconductance for decreasing ribbon widths is expected as a result of the increased gate coupling between ribbon and gate due to fringe fields, where $g_m \propto C_{gg}$, the significant reduction in asymmetry (Fig. 28c) and on-off ratio (Fig. 28a) cannot be explained through increased gate coupling alone. Here, asymmetry is calculated by taking the ratio of the peak g_m of the p-branch to the peak g_m of the n-branch. Only by also considering the effect of the CTR and its associated parasitic resistance on the transfer characteristics can we fully explain the width dependencies observed in this work.

Gated TLM measurements provide a direct way to measure this additional parasitic resistance as a function of gate bias, where any additional resistance due to the CTR region is extracted as part of the contact resistance at the metal-graphene interface. Figure 28d indicates a $> 5\times$ reduction in additional parasitic resistance from > 2.2 to $0.4 \text{ k}\Omega\text{-}\mu\text{m}$ by moving from sheet to 50 nm wide ribbon geometries for the highly resistive p-n-p biased devices ($V_{gs} > V_{Dirac}$). Interestingly, the gated TLM measurements also show a reduction in contact resistance for the case where $V_{gs} < V_{Dirac}$, where no resistive p-n junctions are expected to form, confirming that the use of ribbon geometries is effective in reducing contact resistance independent of effects related to the CTR, as showed by Smith *et al* [103].

3.4.1 Modeling the Reduction in Charge Transfer Region

In order to explain the effect of ribbon geometries in reducing the negative impact of the CTR, the gate-ribbon coupling (C_{gg}) between ribbon and gate is simulated and a characteristic length of the CTR (l_{CTR}) is extracted by fitting the experimental shift in V_{Dirac} with channel length. Figure 29 shows the measured V_{Dirac} shift as a function of L_{ch} for the various width graphene devices and plots the simulated fit. Here, V_{Dirac} shift is given as the difference between V_{Dirac} at a given L_{ch} compared to V_{Dirac} for the long channel case ($L_{ch} = 10 \mu\text{m}$). A first order model of V_{Dirac} shift as a function of L_{ch} is developed to fit the data. In this model, an exponential potential decay from the metal contact into the channel defines the CTR, following Kohmyakov et al [96] (Equation 11), where the length scale of the decay, l_{CTR} , is used as a fitting parameter. This potential decay depends on the Fermi level pinning at the metal-graphene interface, as well as the dielectric environment and the various boundary conditions, producing a potential decay that roughly follows a $(x/l_{CTR})^{-1/2}$ dependency.

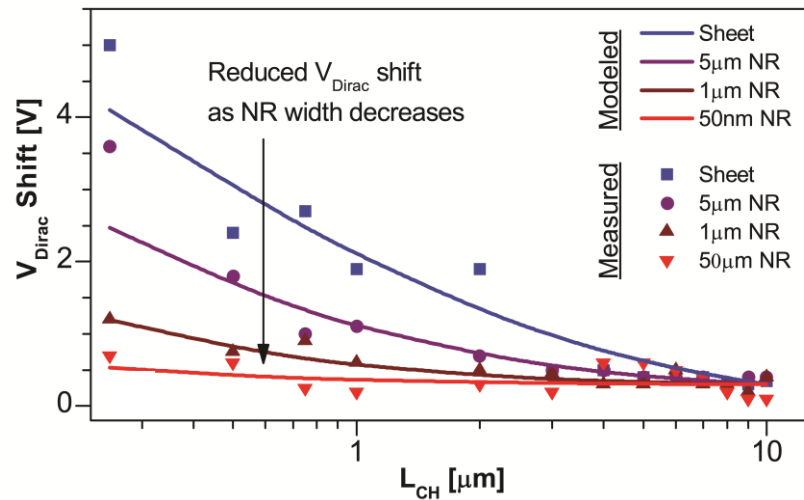


Figure 29: Experimental and modeled V_{Dirac} shift as a function of channel length for various width graphene ribbons.

V_{Dirac} shift is calculated according to $\Delta V_{Dirac} = Q_{CTR} / C_{gg}$, where Q_{CTR} is the additional charge transferred into the device by the CTR and C_{gg} is the simulated coupling capacitance between ribbon and gate according to Figure 30b. These values were extracted from 2D simulations of the metal-oxide-graphene structure as shown in Figure 30a.

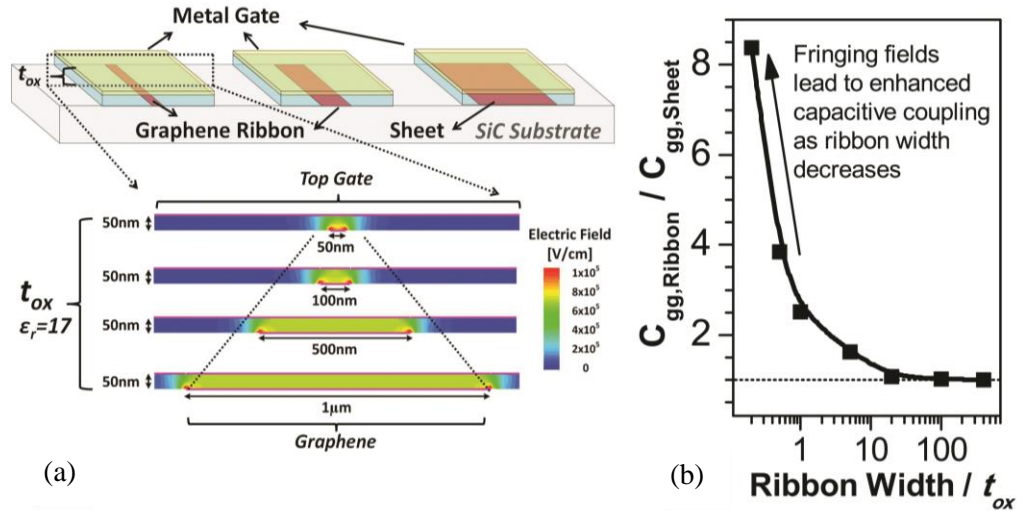


Figure 30: Modeling of capacitive coupling (C_{gg}) between gate and graphene ribbon compared to sheet as a function of ribbon width / t_{ox} (a,b).

A dielectric thickness of 50 nm and dielectric constant of 17 were used to replicate the experimental design of the GNR FETs with 50 nm thick HfO_2 gate dielectric. The results confirm a significant increase in capacitive coupling between the graphene channel and the metal gate due to fringing fields. $C_{gg, ribbon}$ increases 2× compared to $C_{gg, sheet}$ as ribbon width is decreased from sheet to 50 nm. Figure 31 shows the extracted I_{CTR} (left axis) along with $C_{gg, ribbon} / C_{gg, sheet}$ (right axis) as a

function of ribbon width / t_{ox} . For the case of sheet graphene a l_{CTR} of 110 nm is extracted. With $l_{CTR} = 110$ nm, the CTR extends more than 800 nm from the metal-graphene interface before the potential reaches equilibrium with the channel.

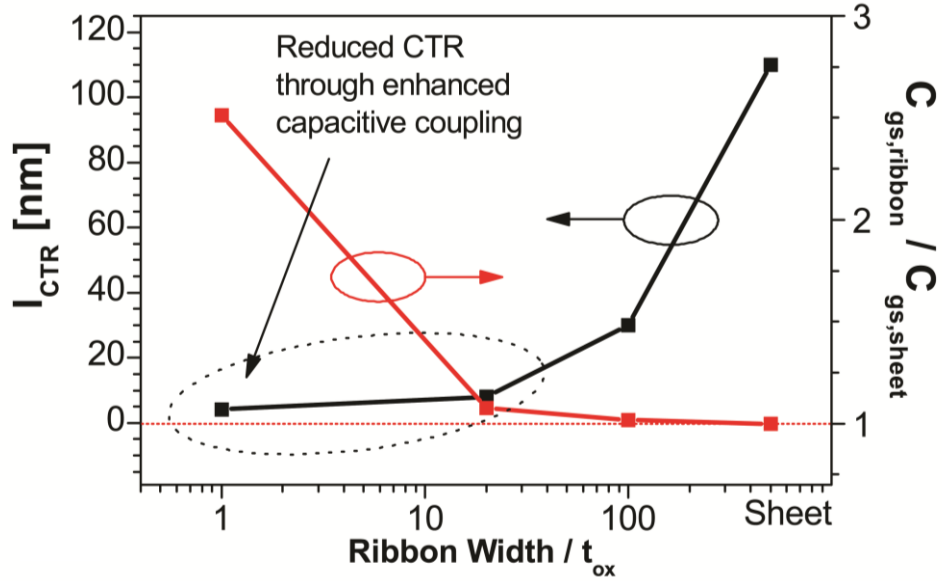


Figure 31: Extracted l_{CTR} as a function of ribbon width plotted along with the ratio of $C_{gs, ribbon}/C_{gs, sheet}$.

This almost micron long CTR compares well with recent direct measurements of the CTR reported by Nagamura et al which show the CTR to be on the order of 300 – 500 nm in length [94] and photocurrent studies of the CTR region indicating length scales on the order of a micron [95], both for the case of mono-layer graphene on bare SiO₂. Constraining the graphene sheet into a 50 nm ribbon geometry leads to a > 95% reduction in l_{CTR} to 4 nm, which is attributed to enhanced charge control in graphene nano-ribbon devices due to fringing fields. The reduction in l_{CTR} extracted from the experimental model of V_{Dirac} shift explains the enhanced on-off ratios and symmetry for these ribbon devices as a direct result of a reduction in the additional parasitic resistance associated with the CTR.

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4. Graphene Nano-ribbon Based Transistors for RF Mixing

Considering the effect of GNR geometry to improve both transconductance as well as p-n symmetry, the benefit of this geometry for graphene based ambipolar mixers can be significant. This is a result of the fact that for the case of the graphene ambipolar mixer, conversion gain is directly related to the derivative of transconductance with respect to gate voltage, g'_m , which depends both on the ultimate transconductance of the device as well as the symmetry of the transfer curve (i.e., curvature at the Dirac point). Although increased C_{gg} acts to offset these gains, the reduction in parasitic resistance due to mitigation of the CTR region is expected to lead to an overall improvement in performance for mixers utilizing GNR geometries. To this end, we design and fabricate two-finger, ground-signal-ground configured RF GNR FETs using multi-ribbon GNR channels.

Although the single ribbon devices with $t_{ox} = 50$ nm show dramatic improvements in g_m , on-off ratio, and symmetry using ribbon widths as large as 1 and 5 μm (Section 3.4); design of graphene transistors for high performance RF applications necessitates L_{ch} and t_{ox} scaling to much smaller dimensions. By scaling t_{ox} by a factor of four from 50 to 12.5 nm, the electrostatics dictate that, to first order, GNR width must also decrease four times to 12.5 nm in order to produce the same reduction in CTR length observed for the thick dielectric case with 50 nm graphene nano-ribbons. At these small widths, edge roughness scattering is expected to significantly degrade GNR mobility, counteracting the benefits achieved by reducing the impact of the CTR. In this Section, RF graphene FETs fabricated using multi-ribbon graphene channel with NR widths ranging from 100 to 50 nm are presented and analyzed.

4.1 Fabrication of Graphene Nano-ribbon Transistors

Graphene nano-ribbon test structures and RF devices are synthesized from quasi-free-standing epitaxial graphene (QFEG). QFEG is prepared on (0001) oriented, semi-insulating 6H-SiC substrates through a combination of sublimation and hydrogen intercalation [66], previously discussed in Section 3.1. Sublimation of Si takes place at 1625 °C for 15 minutes under a 1 Torr Ar ambient, producing primarily n-type, monolayer graphene on the step plateaus and mobilities $\sim 1000 \text{ cm}^2/\text{V}\cdot\text{sec}$ at an electron density of $2 \times 10^{13} \text{ cm}^{-2}$. Hydrogen intercalation is a key step in improving the transport properties and is achieved by exposing the epitaxial graphene samples to a 600 Torr Ar/H₂ mixture at 1050 °C for 120 minutes, producing primarily bilayer QFEG across the (0001) oriented step plateaus enhancing mobilities $\sim 3 \times$ to $3000 \text{ cm}^2 \text{ V}^{-1} \text{ sec}^{-1}$ at a hole density of $1 \times 10^{13} \text{ cm}^{-2}$. This synthesis technique yields wafer-scale, homogenous bi-layer graphene across the SiC substrate, although multi-layer graphene often exists at the SiC step-edge and can contribute to additional charge scattering as discussed in Section 3.1.

After graphene synthesis, device fabrication for the graphene transistors begins by patterning the graphene nano-ribbons (GNRs). Besides patterning of the ribbons, this step also achieves the goal of isolating the graphene devices from each other. Isolation represents an important step in the fabrication process by eliminating any shunt conductances in the devices and due to the fact that metal contacts often delaminate when deposited directly onto large areas of graphene. In this work, devices consists of two-finger, ground-signal-ground configured RF GNR FETs using multi-ribbon GNR channels as shown in Figure 32.

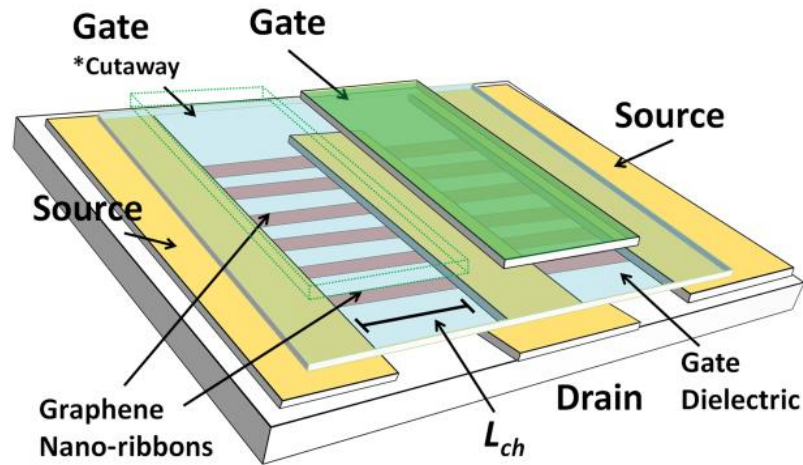
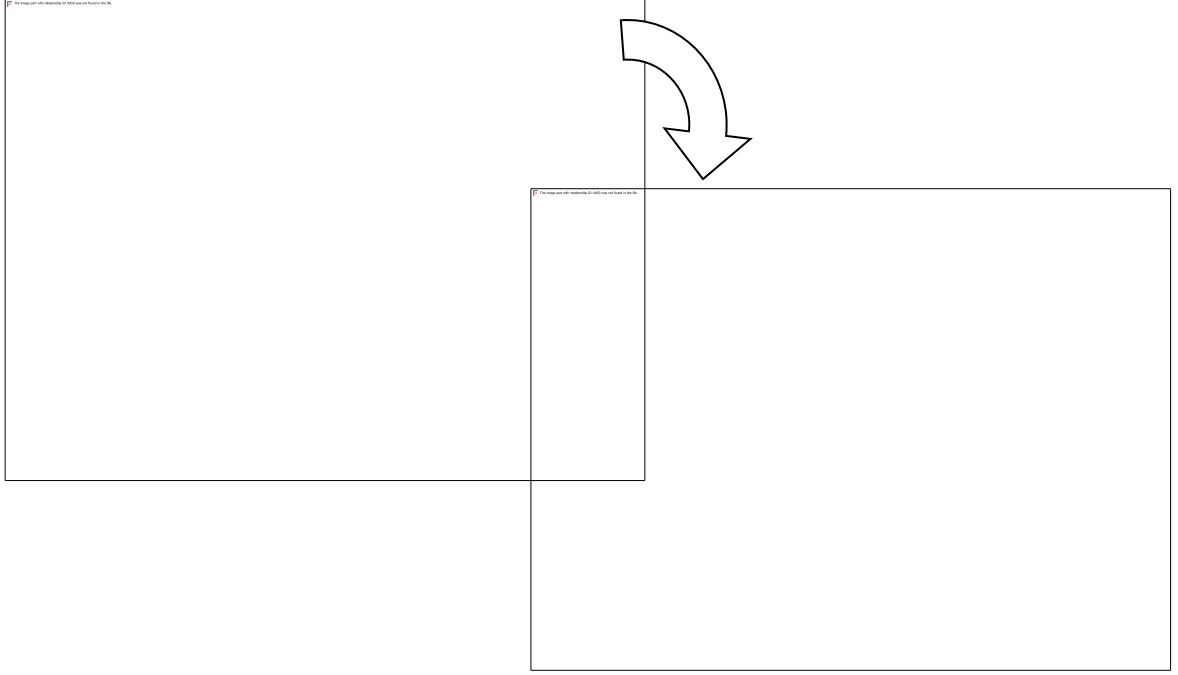


Figure 32: Schematic representation of two-finger, multi-ribbon, GNR RF FET.

For these devices, the high density multi-ribbon pattern prevents use of a negative e-beam resist as a result of poor exposure contrast, which precludes patterning of ribbons smaller than several hundred nanometers. Furthermore, attempts at utilizing a negative e-beam process lead to significant resist footing and line edge roughness (LER). Instead, a two-step isolation process is implemented using an initial lithographic step to pattern the GNRs followed by a second lithographic step to isolate the graphene channels. For this process, the first lithographic step is achieved using e-beam lithography with a positive e-beam resist on the Vistec 5200 e-beam tool, while the second step utilizes a GCA 8000 stepper tool due to its higher tolerances for misalignment.

Initial Step: GNR Isolation Etch



Final Step: Channel Isolation

Figure 33. Schematic representation of two-step GNR patterning for multi-ribbon graphene channels.

In order to pattern high ribbon densities with ribbons as small as possible, a dilute ZEP 520A positive e-beam resist is used to achieve a high exposure contrast. Additionally, a 7 °C dilute cold-develop is implemented to improve exposure contrast, while LER is improved using a 4× multi-pass exposure as well as a large exposure bias. The fabricated RF FETs have L_{ch} ranging from 100 nm to 1.3 μm with a device width, W_{Dev} , of 50 μm . The total channel width, W_{ch} , for these devices depends on the density and number of GNRs that comprise the channel. Nano-ribbons ranging in width from 50 to 100 nm are prepared with spacings between the ribbons ranging from 75 to 100 nm, leading to ribbon densities of 40-50% for the RF GNR FETs. Figure 33 shows a high resolution SEM of an array of 50 nm wide ribbons.

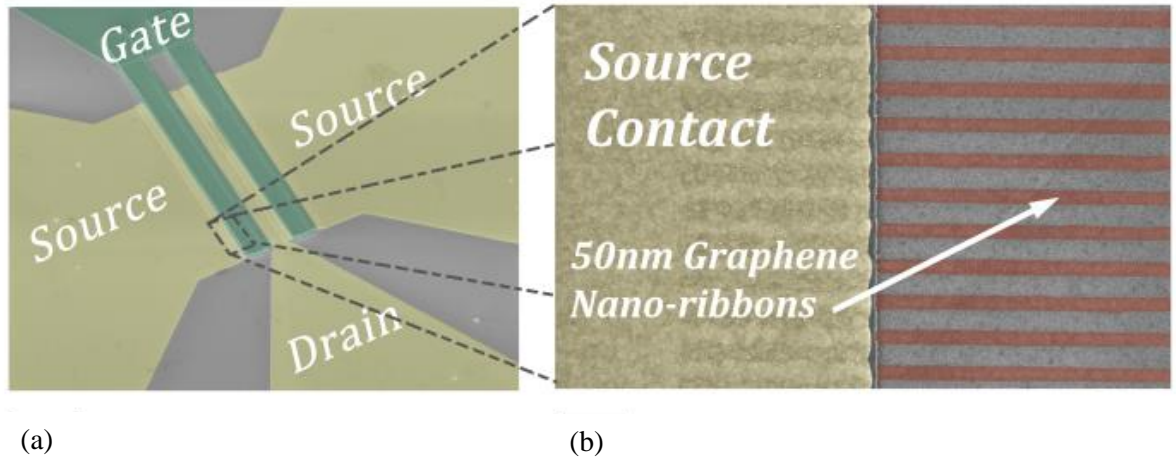


Figure 34: High magnification SEM showing (a) finished two-finger RF GNR FET and (b) metal pad making contact to multi-ribbon channel.

Source/drain contacts (Ti/Au 10/10 nm) are patterned in order to make direct contact to the GNRs, with a 750 nm overlap between the graphene and metal pads as shown in Figure 34b. For the RF GNR FETs, gate dielectrics are deposited using an e-beam physical vapor deposition (EBPVD) seeded atomic layer deposition (ALD) process (2.5 nm HfO_2 seed / 10 nm ALD HfO_2) [104]. Although significant work has shown an appreciable benefit to transport properties by replacing the conventional high- k dielectric with the two-dimensional dielectric h-BN, in this work the necessity for a very thin EOT precludes the use of h-BN. This is a result of the inability to repeatedly produce high-quality, thin layers of h-BN atop graphene RF transistors due to the inability to directly grow h-BN on graphene. This inability necessitates the use of a solution transfer process which has only produced insulating, repeatable gate dielectrics with thicknesses of ~ 50 nm.

In addition to the graphene transistors, Van der Pauw (VdP) Hall cross structures ($5 \times 5 \mu\text{m}$) are prepared, confirming mobilities as high as $2200 \text{ cm}^2/\text{V}\cdot\text{sec}$ at carrier densities of $1 \times 10^{13} \text{ cm}^{-2}$ after dielectric integration.

4.2 Enhanced DC and RF Performance

Figures 35a and 35b show transfer curves for the sheet and multi-ribbon RF GNR FETs with 50 nm wide ribbons for four different channel lengths. Just as for the ribbon devices in Section 3.4 with increased fringing fields, an enhancement in on-off ratio, transconductance, and symmetry is observed for graphene nano-ribbon geometries compared to sheet-based devices. Similarly, a reduction in V_{Dirac} shift from > 2 V to ~ 0.5 V is observed. Despite the fact that the highly scaled RF GNR FETs do not achieve the same ribbon width / t_{ox} ratio as the GNR FETs with 4 \times thicker gate dielectric (50 nm, Section 3.4), they still display significant improvement in transport properties compared to sheet based devices.

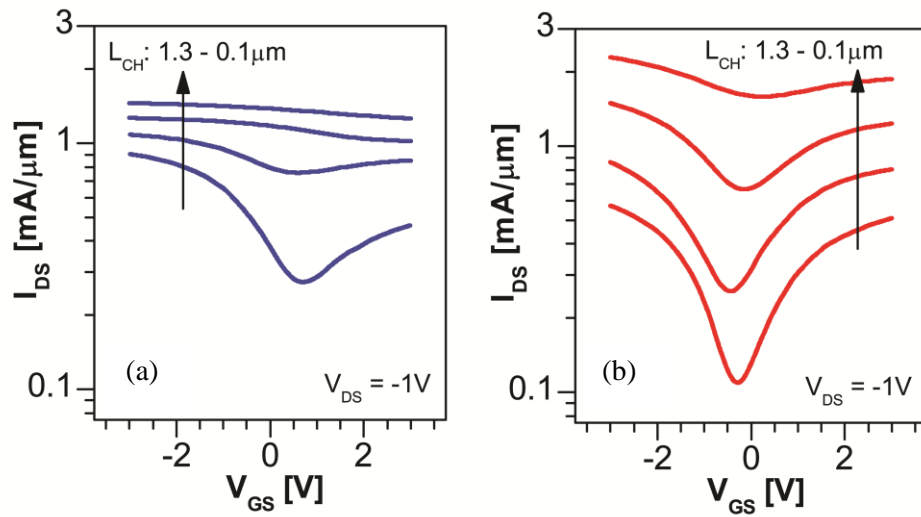


Figure 35: Transfer curves for (a) sheet and (b) multi-ribbon GNR RF FETs as a function of L_{ch} showing an increase in gm as ribbon width decreases.

Figures 36a and 36b summarize the improvements in transfer characteristics for the multi-ribbon GNR FETs with 50, 70, and 100 nm wide ribbons relative to the sheet based ones by plotting

peak g_m and peak g'_m as a function of channel length. Looking closely at the trends of g_m with L_{ch} for the various width devices, we see that for the sheet devices, peak g_m decreases monotonically as channel length is decreased. This degradation in transfer characteristics with decreasing channel length emphasizes the dominance of the CTR at these short channel lengths for the sheet-based device (where $l_{CTR} = 350$ nm). For the nano-ribbon devices ($l_{CTR} < 100$ nm), we instead see an initial increase in peak g_m as L_{ch} is scaled from $1.3\text{ }\mu\text{m}$ down to 300 nm, after which all three GNR widths show a decrease in peak g_m for the $L_{ch} = 100$ nm case, confirming the use of GNR geometries as a technique to reduce l_{CTR} and mitigate the negative impact of the CTR.

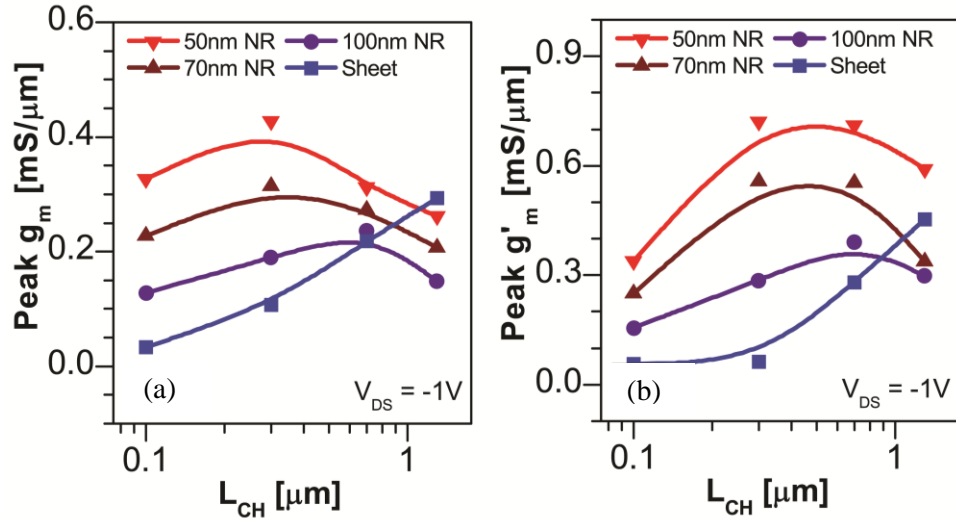


Figure 36: (a) Peak g_m and (b) peak g'_m for sheet and multi-channel GNR RF FETs as a function of L_{ch} showing an increase in g_m as ribbon width decreases. For $L_{ch}=1.3\text{ }\mu\text{m}$, reduced performance compared to sheet is attributed to edge scattering.

The importance of GNR geometries for highly scaled devices is illustrated by plotting peak transconductance versus drive current (Figure 37). In this plot, although smaller ribbon widths lead to decreased mobility for long-channel devices compared to sheet, they also allow scaling to smaller L_{ch}

before the effect of the CTR leads to degraded transfer characteristics, thus resulting in higher peak g_m as well as smaller devices. These results are particularly important for highly scaled RF devices for ambipolar mixing applications, where high transconductances, short channel lengths, and excellent p-n symmetry are desired.

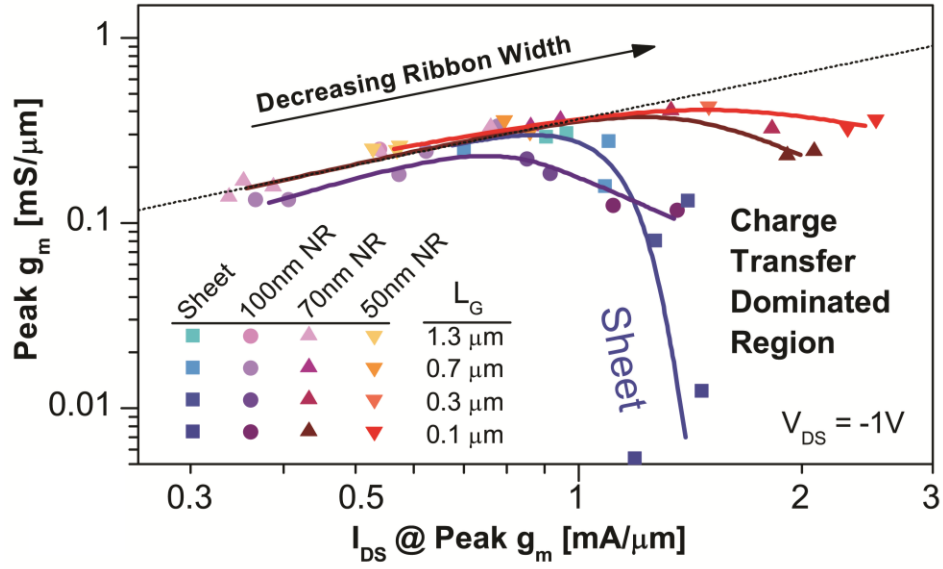


Figure 37: Peak transconductance versus drive current shows the effectiveness of ribbon geometries in allowing scaling to shorter channel lengths in order to achieve the highest possible transconductance.

RF characterization of the GNR FETs confirms the benefit of GNR geometries for improving the transfer characteristics of short-channel devices. Comparison of RF performance between the sheet and ribbon devices was achieved by extracting the de-embedded current gain cutoff frequency (f_T).

Figure 38 shows that GNR FETs with $L_{ch} = 300$ nm are able to achieve $\sim 3\times$ higher f_T than sheet devices, which is attributed to the mitigation of the CTR arising from enhanced gate coupling.

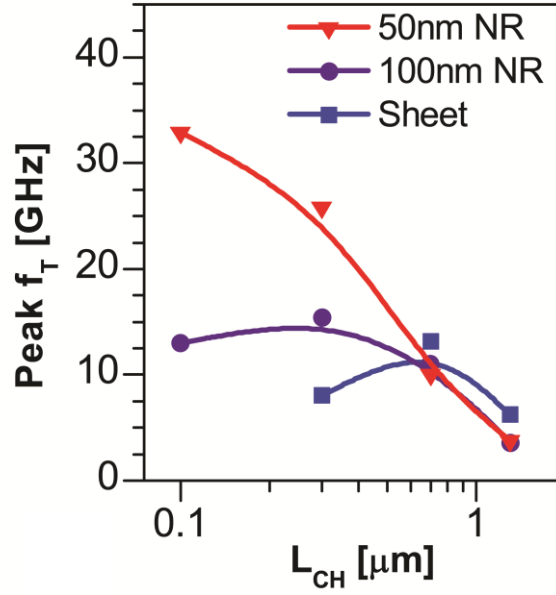


Figure 38: Intrinsic cutoff frequency for sheet and GNR devices as a function of ribbon width and channel length

4.3 Enhanced Ambipolar Mixing

To evaluate the benefit of GNR geometry for the ambipolar graphene mixer, the intrinsic graphene mixer is simulated using the harmonic balance simulator in the Agilent Advanced Design System (ADS). Ambipolar mixing is achieved by mixing of the local oscillator (LO) and RF input signals (4.2 and 4 GHz, respectively) at the gate, giving an intermediate frequency (IF) output signal at

200 MHz ($f_{LO} - f_{RF}$). The intrinsic parameters of the graphene FET are evaluated from the measured S-parameters (Fig. 39a) using the small signal model shown in Figure 39b.

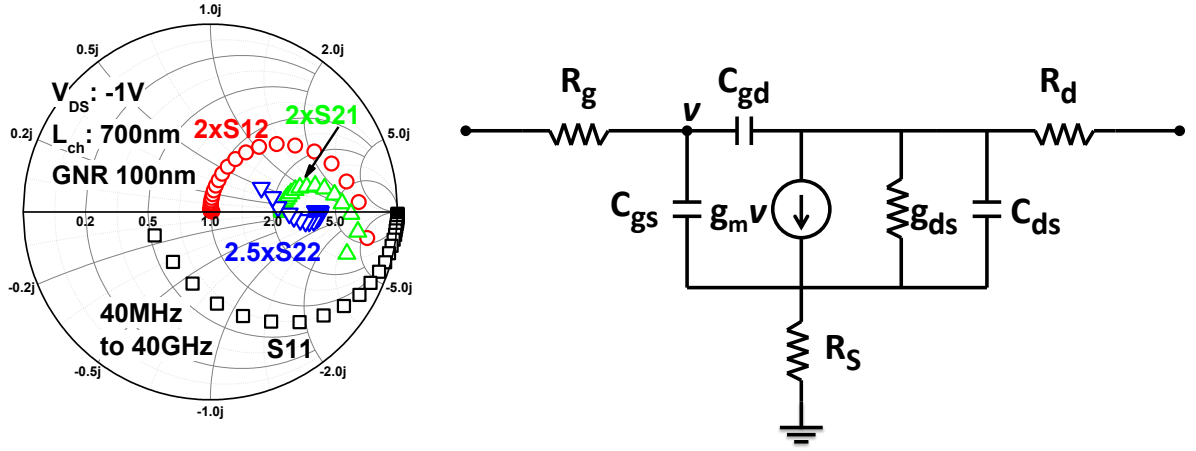


Figure 39: De-embedded S-parameters used for small signal parameter extraction (a). Small signal model of multi-channel RF GNR FET (b).

The following equations were utilized to evaluate the small signal components:

$$(12) \quad g_m = \text{Re} [Y_{21}] \quad @ \quad (\omega^2 = 0)$$

$$(13) \quad g_{ds} = \text{Re} [Y_{22}] \quad @ \quad (\omega^2 = 0)$$

$$(14) \quad R_g = \text{Re} [Y_{11}] / (\text{Im} [Y_{11}])^2$$

$$(15) \quad C_{gd} = -\text{Im} [Y_{12}] / \omega$$

$$(16) \quad C_{gs} = [\text{Im} [Y_{11}] + \text{Im} [Y_{12}]] / \omega$$

Using the evaluated intrinsic components of the RF graphene FET, a large signal model is developed to fully capture the non-linearity and asymmetry introduced by the CTR (Fig. 40).

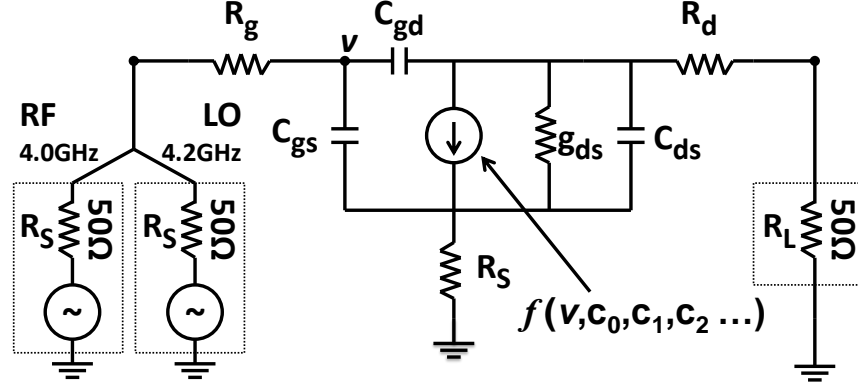


Figure 40: Large signal model of multi-channel RF GNR FET using polynomial fit of I_{ds} - V_{gs} to capture the non-linearity and asymmetry of the transfer curves due to the CTR.

In this large signal model, the parameters of the non-linear voltage controlled current source are selected in order to match the measured transfer characteristics of the RF graphene FETs. Figure 41a shows the measured transfer curve for a RF GNR FET using GNRs with a width of 100 nm for a channel length of 0.7 μm and the extracted parameters and fit for the non-linear current source. The large signal model is then simulated using the harmonic balance simulator in Agilent's Advanced Design System (ADS). For the simulation an input RF signal of 4.0 GHz and input LO signal of 4.2 GHz were used, producing an output IF signal at the drain of 200 MHz. Figures 41b plots the evaluated conversion gain (P_{IF}/P_{RF}) as a function of LO power.

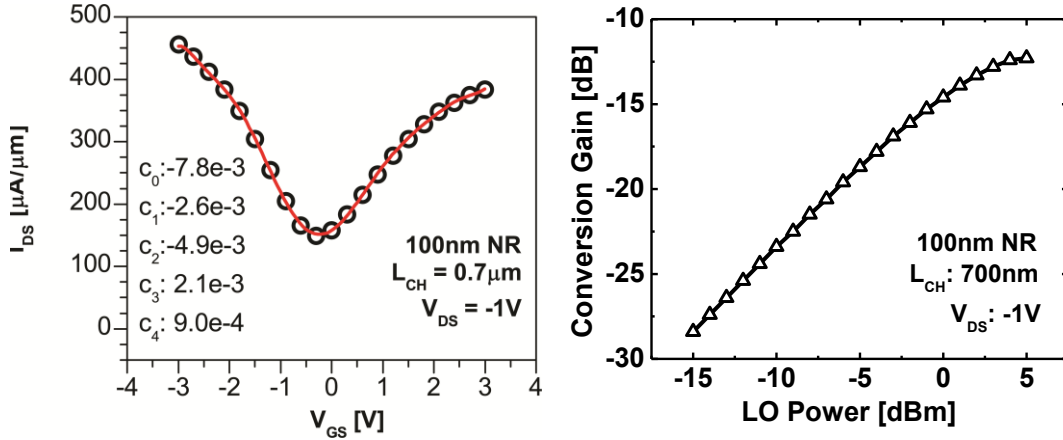


Figure 41: Polynomial fit of the transfer curve, capturing the non-linearity and asymmetry due to the CTR (left). Simulated conversion gain of the intrinsic RF GNR FET as a function of LO power (right).

Figure 42 plots simulated CG as a function of L_{ch} for the 50 and 100 nm wide GNR FETs compared to the conventional sheet based device at an LO power of -5 dBm. At $L_{ch} = 1.3 \mu m$, the degraded mobility of the GNR devices due to enhanced edge scattering leads to degraded CG relative to the sheet based device for the 100 nm wide GNR FET. On the other hand, short-channel GNR FETs exhibit significantly improved CG. While sheet devices show a sharp decrease in mixing performance as L_{ch} is decreased due to the dominant effects of the CTR, GNR devices maintain symmetry and show improvement in CG as L_{ch} is scaled to 300 nm, leading to 20 dB improvement in CG over sheet devices at the same L_{ch} and directly showing the benefit of GNR geometries in preserving CG at small channel lengths. At $L_{ch} = 100$ nm, the CTR begins to dominate the transfer characteristics of the GNR FETs and, subsequently, CG degrades.

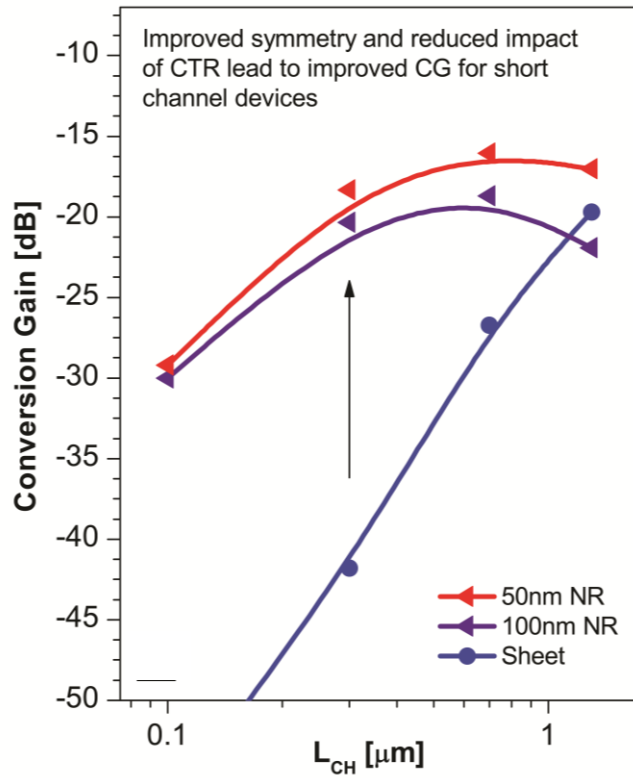


Figure 42: Simulated CG as a function of channel length for the 50 and 100nm wide GNR FETs compared to the conventional sheet based device.

In order to benchmark these results against state-of-the-art graphene transistors, conversion gain with input and output matching networks was simulated using the developed large signal model. For this simulation, discrete, lumped elements were used to achieve narrow band matching. A schematic representation of the matching network is shown in Figure 43a.

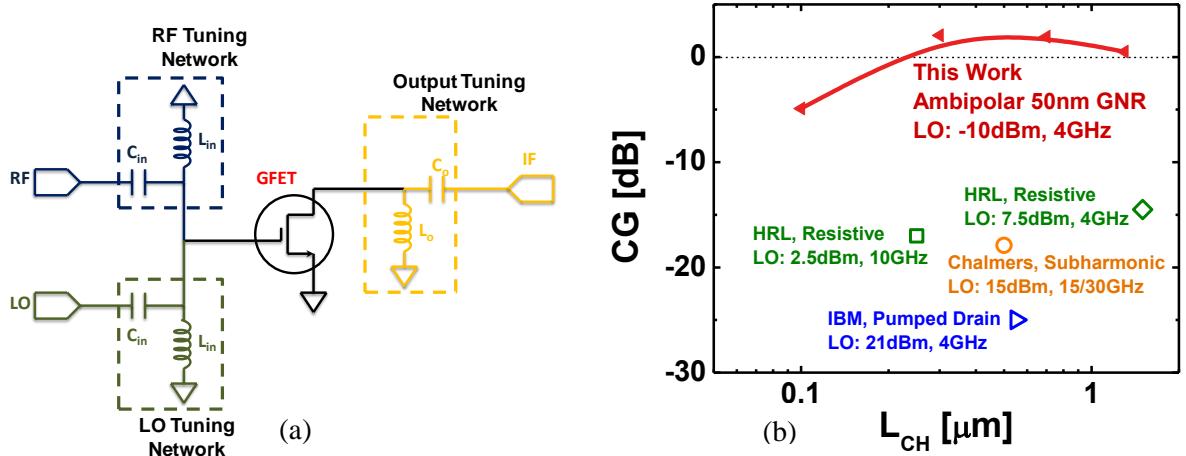


Figure 43. (a) Schematic representation of discrete, lumped element matching network and (b) simulated conversion gain as a function of channel length (red) compared to state-of-the-art graphene based mixers.

The simulated conversion gain is plotted as a function of channel length for the best case, 50 nm wide nanoribbon RF FET (Fig. 43b). In this simulation, an LO power of -10 dBm is utilized for the ambipolar, multi-ribbon graphene RF FET. Comparing to the highest reported conversion gain for graphene based mixers in the literature, it is clear that significantly enhanced conversion gain can be achieved utilizing the ambipolar mixer. The ambipolar mixer demonstrates a peak achievable conversion gain of approximately 3 dB, which is more than an order of magnitude greater than the next best reported conversion gain. The enhanced gain is a direct result of the use of an active mixer configuration, whereas all other plotted data points adopt a passive configuration and are thus fundamentally limited to conversion loss. These results further emphasize the key role of graphene nanoribbon geometry to mitigate contact effects and allow scaling of the graphene RF transistor to ultra-short channel lengths while preserving transfer characteristics.

¹⁰⁴ Hollander, M.J.; LaBella, M.; Trumbull, K.A.; Cavalero, R.; Hughes, Z.; Zhu, M.; Weng, X.; Hwang, E.; Snyder, D.W.; Datta, S.; Robinson, J.A. Enhanced Transport and Transistor Performance with Oxide Seeded High-k Gate Dielectrics on Wafer-scale Epitaxial Graphene. *Nano Lett.* 11 (9), 3601-3607. 2011.

5. TaS₂ for Scaled Two-dimensional Steep Slope Transistors

The transition-metal dichalcogenide 1T-TaS₂ is a 2-dimensional, layered material exhibiting interesting and complex behavior as a result of interplay between electron-electron and electron-phonon interactions. Below 600K, 1T-TaS₂ is host to several distinct charge-density-wave (CDW) phases which exist as a result of Fermi-surface driven CDW instabilities (i.e., Fermi-surface nesting) that lead to a distortion of the crystal lattice and subsequent periodic charge density modulation. These charge and structural distortions eventually become fully commensurate with the lattice below a critical temperature of $\sim 180\text{K}$, after which electron-electron interactions lead to the formation of an insulating state through a Mott-Hubbard transition [105, 106]. Recent work has explored ultra-fast melting of the insulating, Peierls-Mott state using pulsed optical or electronic means in order to partially collapse the Mott gap or to produce meta-stable states of intermediate resistivity and variable duration [107, 108, 109, 110]. In this Section, we demonstrate abrupt, resistive switching between insulating and conducting states through electronic means. Both DC and voltage pulse are used to trigger an abrupt resistive switching from the insulating Mott phase to the metallic phase. After the applied electric field is removed, the 1T-TaS₂ undergoes a second abrupt transition and returns to its equilibrium insulating state. In this fashion, the material functions as an abrupt electrically-driven volatile switch. In this way, the material could be developed for use in fabrication of a steep-slope switching device that can surpass the ‘Boltzmann limit’ inherent to conventional MOSFET semiconductor switching devices.

The ‘Boltzmann limit’ is a fundamental limit to the switching slope of a MOSFET which is determined by considering the thermal energy of the charge carriers. For the case of a MOSFET, especially at low voltages, the fundamental minimum amount of voltage needed to increase the device current by one order of magnitude is 60 mV decade^{-1} (at room temperature). In this work we consider a device where the abrupt switching nature of 1T-TaS₂ is used to overcome this limit due to the

collective nature of the transition. By placing the 1T-TaS₂ in series with the channel material of a conventional MOSFET, the abrupt transition can be triggered according to the applied gate bias (V_{gs}). Upon switching, the rapid reduction in voltage across the TaS₂ results in an abrupt amplification of the gate drive on the channel material of the device. This device is often referred to as a hyper-FET within the literature.

Importantly, the IMT transition in 1T-TaS₂ is shown to occur at a critical resistivity of 7 m Ω -cm and the transition time of 3 nanosecond appears to be significantly smaller than similar abrupt transitions observed in other small gap Mott insulating materials, which have been attributed to avalanche breakdown mechanism. These results suggest that the observed transition may be caused or facilitated by a carrier driven collapse of the Mott gap or charge ordering which results in a fast (3ns) collapse of the insulating state.

5.2 The Abrupt Insulator-Metal-Transition

Figure 44 shows the atomic structure of 1T-TaS₂ as well as the characteristic “Star-of-David” distortion of the Ta lattice. This distinctive distortion is the result of Fermi-surface nesting and is accompanied by out-of-plane distortions of the coordinating S atoms such that the sulfur lattice bulges slightly around the center of the “star” [106,111,112]. As the temperature is varied from 600 - 0K, three distinct phases of 1T-TaS₂ are observed. Figure 45 plots resistivity versus temperature of a 10nm thick 1T-TaS₂ flake and captures these three equilibrium phases.

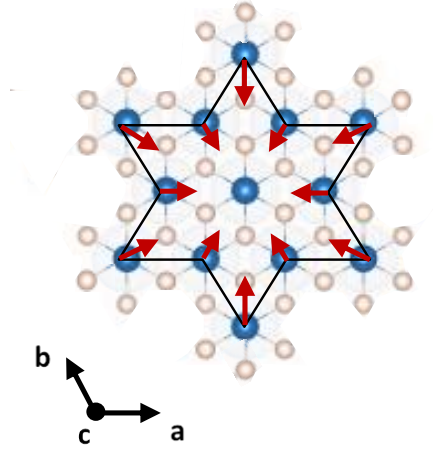


Figure 44. Schematic representation of 1T-TaS₂ structure.

The low temperature insulating phase is structurally the most simple of the three. This phase is referred to as the commensurate CDW (CCDW) phase due to the fact that, in this phase, the “Star-of-David” distortions interlock to form a triangular superlattice which is fully commensurate with the crystal lattice. In the CCDW phase, the twelve surrounding Ta atoms contract towards the thirteenth central Ta atom and become strongly bonded to each other. This results in two low-lying three-band sub-manifolds (B1 and B2 in Fig. 1e) representing the 12 outer atoms and one narrow band at the Fermi energy, E_F , corresponding to the central Ta atom [113].

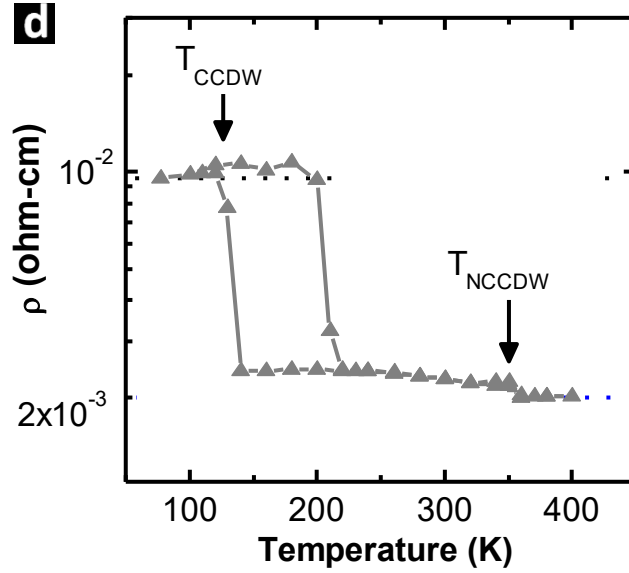


Figure 45. Resistivity of low and high-field resistivities extracted from current-voltage sweep at 77K superimposed on resistivity versus temperature.

Due to the small width of this band ($\sim 100\text{meV}$) and its half-filled nature, it has been proposed that Mott localization occurs as a result of electron-electron interaction [106]. The opening of a Mott gap (200 meV) leads to a sharp jump in resistivity and insulating behavior below $\sim 180\text{K}$. Above this temperature, the ‘Star-of-David’ distortions remain, but no longer form the interlocking triangular superlattice that is commensurate with the lattice. Instead, they form roughly hexagonal domains that are commensurate with the lattice and separated by small triangular regions which are incommensurate with the lattice [112]. This phase is referred to as the nearly commensurate CDW (NCCDW) phase and does not exhibit the insulating behavior of the CCDW phase. The NCCDW phase exhibits a resistivity range of approximately 5 - 0.5 $\text{m}\Omega\text{-cm}$, roughly $10\times$ reduced from the CCDW phase. This resistivity range is a common feature of the $1\text{T-TaS}_x\text{Se}_{1-x}$ material family and is of importance in the sense that it is centered about 3 $\text{m}\Omega\text{-cm}$, which is the resistivity value if one were to assume the universal value of the maximum metallic resistivity for each 2-dimensional layer of the crystal [106].

Above 350K, the distortions become completely incommensurate with the underlying lattice and 1T-TaS₂ undergoes a $2\times$ drop in resistivity; this is referred to as the incommensurate CDW phase (ICCDW).

Although previous works have investigated interplay between these phases by examining the collapse of the insulating Mott phase using time resolved, angle resolved photo-electron spectroscopy in an ultra-fast pump-probe configuration, these studies focused primarily on understanding the mechanisms which govern charge and lattice reordering under non-equilibrium conditions and under influence of electric field [107,108]. Alternatively, Stojchevska et al have recently presented work showing the presence of hidden metastable states below 50K which are reached after a short excitation pulse (~ 30 fs) is applied to the CCDW phase. It is thought that these states are a result of voids due to hole recombination with the conduction electron isolated on the central Ta atom [109]. These voids are distributed across the sample and contribute to conductivity through formation of incommensurate states [109]. The authors postulate that if they can be stabilized with some kind of long range order before they can annihilate, then the material can be locked in a quasi-stable low resistivity state. After entering the hidden state, the 1T-TaS₂ remains there until an erase pulse is applied to the sample for a long enough time to allow thermalization of the electron-hole variations or by heating the sample. Most recently, Vaskivskyi et al have probed these hidden metastable states using electrical means. In their work, these states are reached after applying a short voltage pulse in order to asymmetrically introduce charge to the CCDW system [110]. The original CCDW state cannot be recovered by increasing the applied voltage pulse magnitude or duration. Instead, application of a longer duration pulse only partially recovers the insulating behavior of the CCDW. Although, as in previous work, these hidden states can be completely erased by heating the sample.

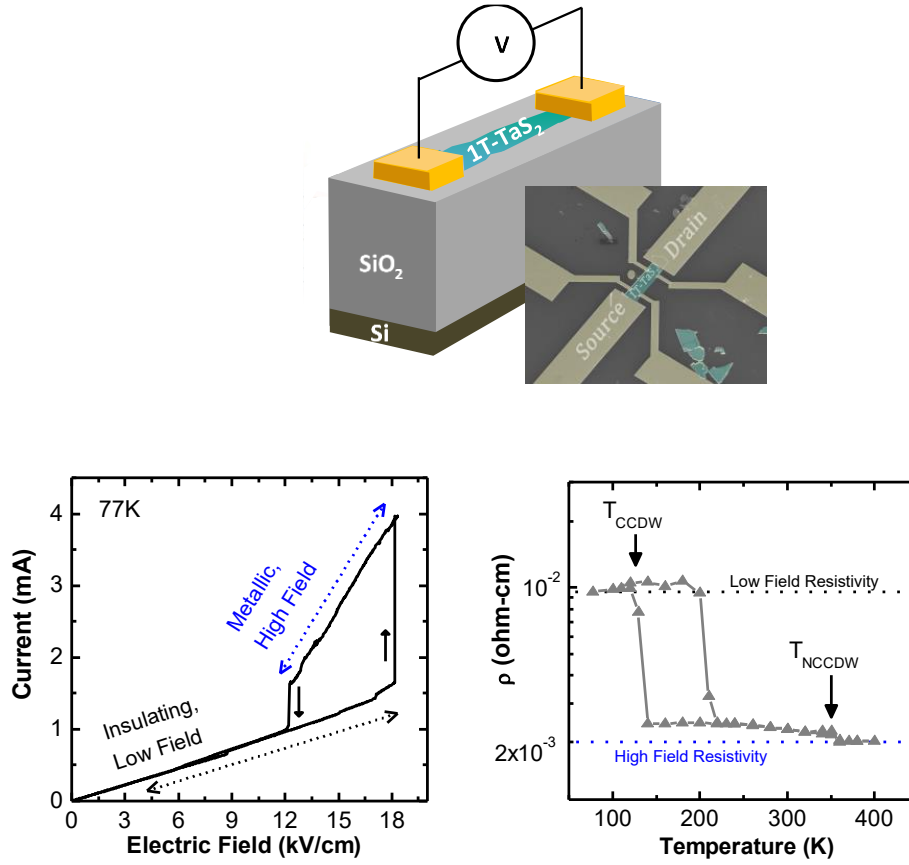


Figure 46. Schematic representation of two terminal device (a). Inset shows colorized SEM micrograph of Hall bar structure. Typical current-voltage sweep showing abrupt transition to metallic phase and return to insulating phase (b). Resistivity of low and high-field resistivities extracted from current-voltage sweep at 77K superimposed on resistivity versus temperature (c).

In this work, two-terminal, DC and pulsed voltages and currents are used to demonstrate abrupt, resistive switching between the various phases of 1T-TaS_2 over a range of temperatures (77-150K). Figure 46a shows a schematic representation of a two-terminal device along with a colorized SEM micrograph. 1T-TaS_2 flakes on SiO_2 substrates (190 nm) are prepared from bulk 1T-TaS_2 crystals using an exfoliation process. Flakes are identified optically and metal contacts are patterned using electron beam photolithography (Ti/Au, 10/50 nm). Flake thickness is measured by atomic force microscopy, with flakes ranging in thickness from 8 – 55 nm (14 – 95 atomic layers). A representative current-

voltage (I-V) measurement is plotted in Figure 46b showing an abrupt reduction in resistivity after reaching a critical field. This measurement is performed at 77K in high vacuum for a 1T-TaS₂ flake with length 8.4 μm , width 6.6 μm , and thickness 10 nm (17 layers). Figure 44c plots the resistivity versus temperature of the same flake acquired from two-terminal measurements. For this voltage-mode measurement (V-mode, Fig. 46b), the voltage across the device is swept from 0-20 V and back to 0 V while measuring the current through the device. In the low field regime, the flake exhibits a linear I-V response with a resistivity of approximately 9 m Ω -cm. We find that the resistivity of the flake in this regime remains constant over a broad range and matches closely with the resistivity of the CCDW phase (which is the equilibrium phase at this temperature). Figure 46c superimposes the extracted low-field resistivity from the 2-terminal I-V characteristics (black dashed line) on the resistivity versus temperature plot. After reaching a critical threshold electric field and threshold current (18 kV cm⁻¹, 1.5 mA), the current through the flake increases abruptly. After this abrupt transition, the I-V response remains linear in nature, but indicates a resistivity roughly 10 \times lower than the initial insulating CCDW phase. This reduced resistivity (blue dashed line) matches with the resistivity of the NCCDW or ICCDW phases (Figure 46c), suggesting that the flake has undergone an abrupt transition from the insulating to metallic phase. On the return sweep back to zero bias, the flake undergoes another abrupt transition after reaching another critical point (12 kV cm⁻¹, 1 mA). In this transition, the flake switches from the metallic state back to its original insulating state.

The abrupt and reversible change in resistivity observed in this work may be a result of one of several mechanisms. An insulator-to-metal transition (IMT) can occur in conventional insulating materials by mechanisms such as avalanche or Zener breakdown where application of large electrical field leads to impact ionization or direct tunneling of the carrier across the band gap, respectively. For Mott insulators, an IMT can occur through an additional mechanism: the collapse of the Mott gap. This can be realized by surpassing a critical carrier concentration such that the electron-electron interactions which lead to Mott-Hubbard localization can be screened out. The critical carrier

concentration at which the Mott gap collapses is defined according to the Mott criterion: $n_c / 3a_0 \approx 0.25$ [114]. Here, a_0 is the Bohr radius and n_c is the critical carrier density. Additionally for the case of CDW materials, abrupt changes in resistivity can be realized through sliding CDW conduction, where CDWs that are initially pinned at a defect can be triggered by application of an external field [115,116]. Although sliding CDW conduction leads to an abrupt increase in conduction through the material, it does not lead to a sharp jump to higher currents, but instead exhibits a kink or elbow in the I-V relationship [117,118]. Furthermore, the critical field at which CDW sliding occurs are typically below 1 V cm^{-1} , which is several orders of magnitude lower than the critical field observed in this work [118]. Furthermore, IMTs may occur without field assistance (i.e., avalanche and Zener breakdown) or carrier assistance (i.e., satisfying the Mott criterion). Many IMTs are thermally driven, such as the case for perovskite rare-earth nickelates. Other IMTs may be driven by local Joule heating as current flows through the material.

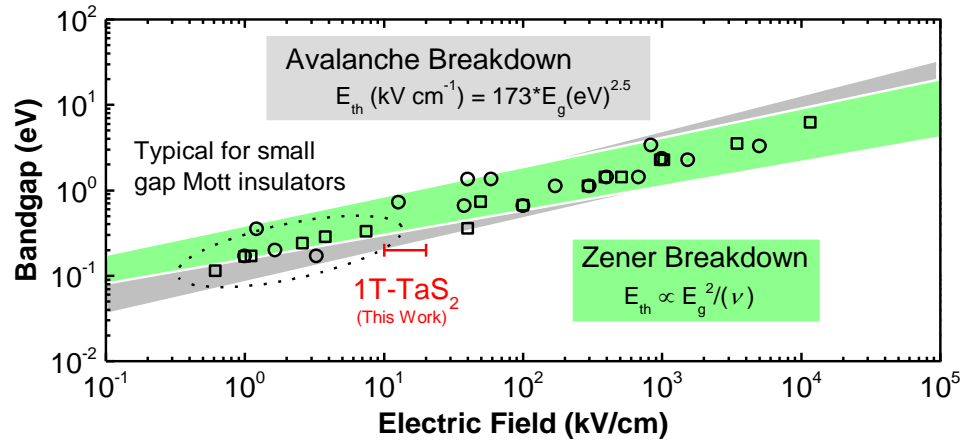


Figure 47. Plot of critical fields for avalanche and Zener breakdown mechanisms as a function of bandgap.

Figure 48 plots the critical fields for avalanche and Zener breakdown as a function of bandgap and the typical range of critical fields observed in this work for the IMT in 1T-TaS₂ (marked with red line). Although dielectric breakdown in Mott insulators has been investigated theoretically in various studies, few experimental reports exist detailing the phenomenon. Recently, Guiot et al studied resistive switching of several small gap Mott insulators in the GaTa₄Se_{8-x}Te_x family induced by electronic breakdown of the Mott insulating state [119]. In their work, a dependency on the critical threshold field for the IMT was found according to the universal law of $E_{th} \propto E_{gap}^{2.5}$ for avalanche breakdown. According to their results, this dependency predicts a critical threshold field of roughly 3 kV cm⁻¹ for 1T-TaS₂ in the Mott insulating state ($E_g = 200$ meV). In this work, the observed threshold fields for 1T-TaS₂ range from 10-20 kV cm⁻¹. Although the observed E_{th} is substantially larger than that predicted for avalanche breakdown, they are significantly lower than that predicted for Zener breakdown by tunneling across the Mott gap [120].

5.3 Characterizing the Insulator-Metal-Transition

To probe the field, temperature, and carrier dependency of the IMT in 1T-TaS₂, voltage and current mode measurements were performed as a function of temperature. Figure 49a plots V-mode measurements as a function of temperature from 77 to 150K. Above ~150K, 1T-TaS₂ exists in the metallic NCCDW phase as its equilibrium state. Again, the voltage across the device is swept from 0 – 20 V and back to 0 V while measuring the current through the device. Current mode (I-mode) measurements are also performed (Fig. 49b), wherein the current sourced through the flake is swept from 0 – 3 mA and back to 0. For both measurement techniques, an abrupt transition from CCDW to metallic phase is observed. The absolute field and current at the insulator-to-metal transition (IMT) and metal-to-insulator transition (MIT) points are plotted as a function of temperature for the V and I-

mode measurements in Figure 49c and 49d. The threshold field (E_{th}) and threshold current (I_{th}) appear to be independent of measurement mode. Both V and I-mode measurements show E_{th} and I_{th} that monotonically decrease with increasing temperature. Although the low-field (low-current) I-V response exhibits linear behavior, we note that as the transition point is approached, the I-V response begins to show a super-linear behavior while others have reported exponential behavior [110]. Exponential dependency of current density on voltage may be indicative of an increase in carrier density due to impact ionization, which can be thought of as a doping process which introduces additional carriers to the system [121]. Importantly, extracting the resistivity at the transition point (Fig. 49e), we find a critical resistivity that is independent of both temperature and measurement mode. This resistivity corresponds to the measured resistivity just at the transition point on the resistivity versus temperature plot (Fig. 46c) when sweeping from CCDW to NCCDW and suggests that the observed IMT may be a carrier driven collapse of the Mott gap.

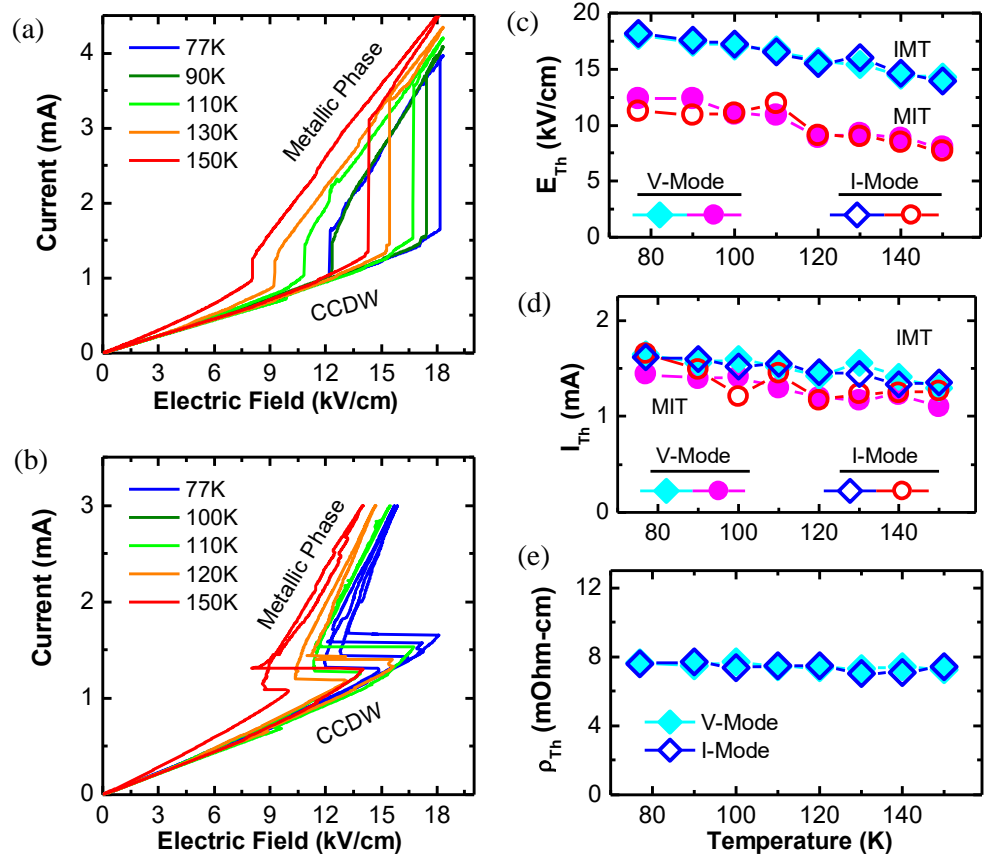


Figure 48. Voltage-mode measurements (a) and current-mode measurements (b) of 1T-TaS₂ as a function of temperature. Critical electric field (c), current (d), and resistivity (e) at the IMT point as a function of temperature for voltage and current-mode measurements.

In order to probe the IMT further, a V-mode measurement was performed with varying resistances in series with the 1T-TaS₂ flake. Figure 50a shows a schematic representation of the measurement setup while Figure 50b plots the measured results for different series resistances at 110K. Here, the current through the device is calculated by considering the bias conditions and series resistor. An I-mode measurement is plotted for comparison. Viewing the ideal current source as an open circuit, one may consider the I-mode measurement equivalent to a V-mode measurement with series resistance which is effectively infinite. Use of a resistor in series with the flake produces a negative differential

resistance across the IMT as well as the MIT transition where the slope of the negative differential resistance can be related to the series resistance (R_{Load} , Fig. 50b). Here, the ‘s’-shaped shape of the I-V characteristics and the negative differential resistance point to a carrier(current) driven process. Negative differential resistance is also observed for avalanche breakdown, which can be viewed as, effectively, a carrier driven process [119].

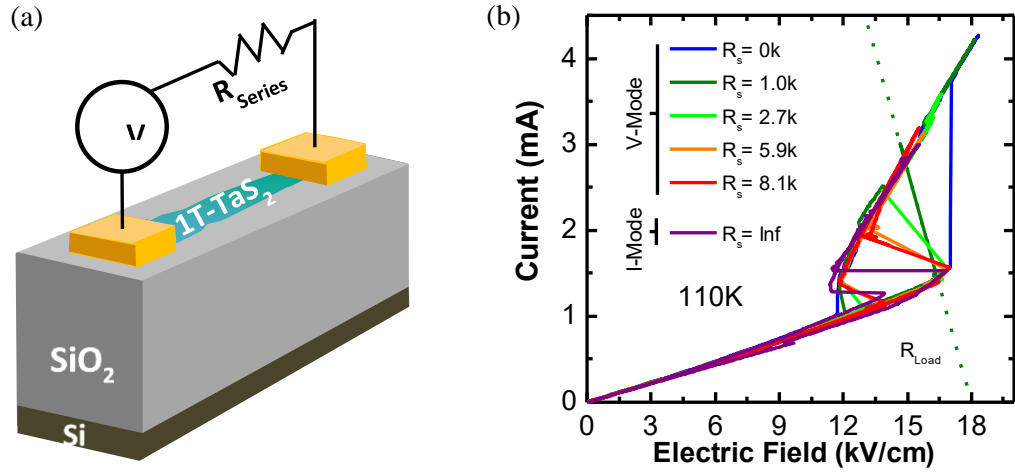


Figure 49. Schematic representation of measurement set-up (a). Current-voltage characteristics as a function of series resistor (b) showing abrupt switching and negative differential resistance for the insulator-metal and metal-insulator transitions.

The time scale of the IMT transition was investigated using pulsed V-mode measurements. In order to capture the voltage across the 1T-TaS₂ flake while pulsing, a load resistor (R_s) was placed in series with a flake and the output waveform was captured as the voltage measured across R_s . In this experiment, the flake used was 4 μm long and roughly 20 nm thick. Figure 51a shows a schematic representation of the setup while Figure 51b shows the input voltage waveform. A triangular pulse was used so that the IMT could be captured in the output waveform and the critical field, resistivity, and

currents could be extracted for each pulsed measurement. The pulse width was varied from 3 s to 30 μ s. Figure 51c shows a pair of representative input and output waveforms ($t_{pulse} = 300 \mu$ s).

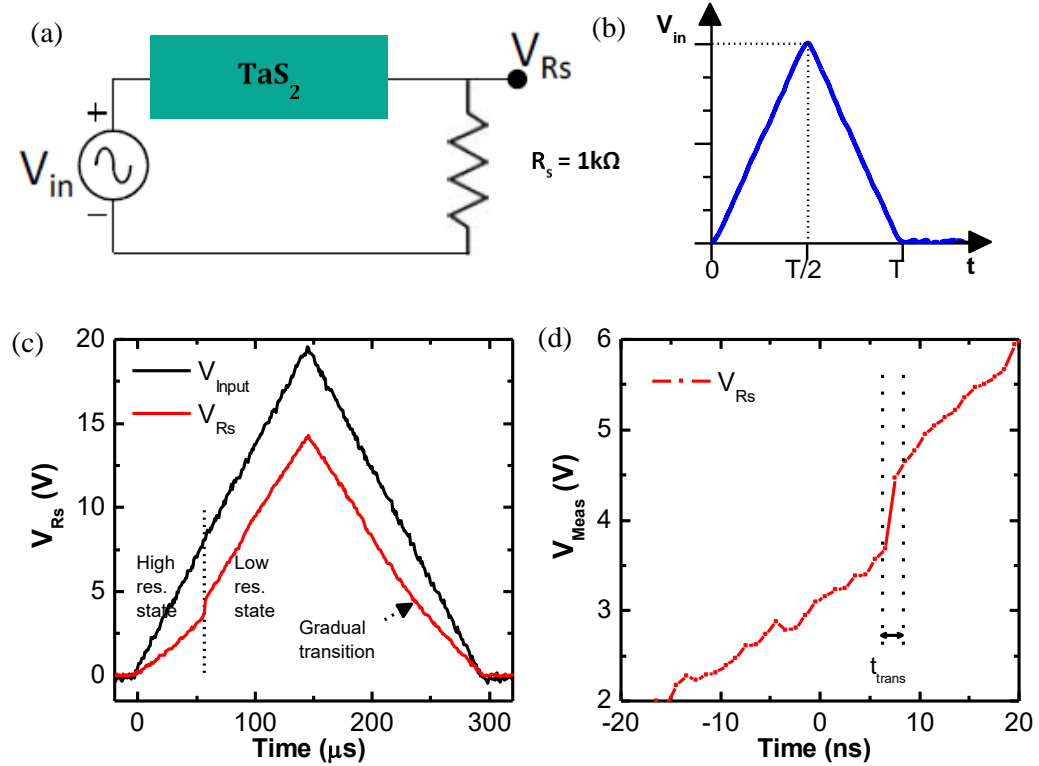


Figure 50. Schematic representation of pulsed I-V measurement set-up (a) and representative input waveform (b). Input and measured voltage across R_s for a 300 μ s pulse (c). Zoomed in view of abrupt, sub-10ns IMT (d).

Within the measured output waveform, an abrupt transition from lower voltage to higher voltage is observed. This behavior indicates an IMT within the 1T-TaS₂, where an abrupt reduction in TaS₂ resistance leads to a sharp increase in voltage dropped across R_s . The time duration of the IMT is found to be less than the time resolution of the oscilloscope (<10 ns) (Fig. 51d). Higher resolution oscilloscope captures show a $t_{trans} \sim 3$ ns, which is significantly smaller than other narrow gap Mott

insulators ($10 \mu\text{s}$ - 1 ms) [119]. Such short transition times, as well as the significantly higher critical field observed in this work compared to avalanche breakdown in other small gap Mott insulators may indicate that the abrupt IMT in 1T-TaS_2 is not an avalanche breakdown process. On the other hand, previous work has shown that collapse of the Mott gap and charge re-ordering in 1T-TaS_2 can take place in the sub-picosecond time scale, while subsequent re-ordering of the lattice follows within picoseconds [107, 108].

By calculating the voltage across the 1T-TaS_2 flake as well as the current through the device, a pulsed I-V plot can be constructed for each discrete pulse. Figure 52a plots the pulsed I-V data for 5 different pulse widths.

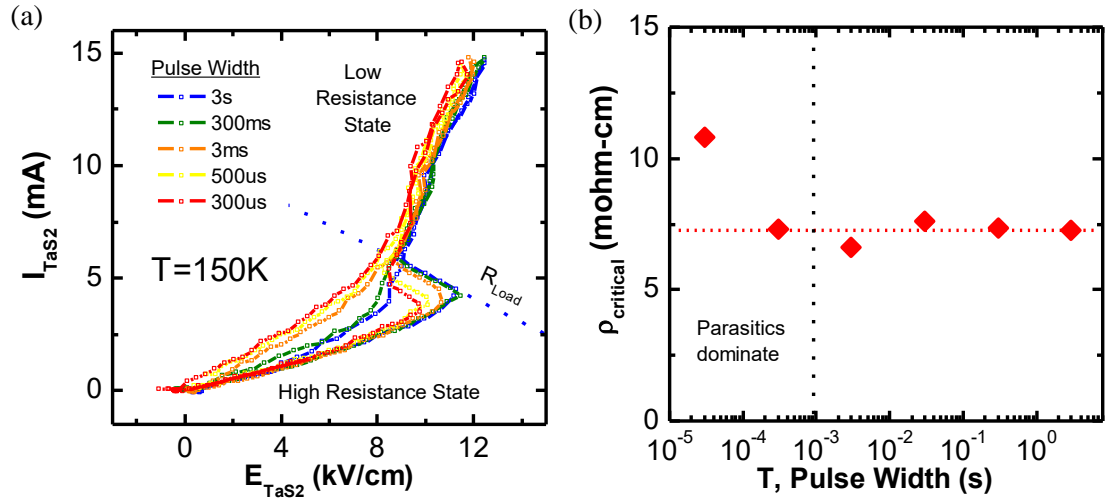


Figure 51. Reconstructed pulsed I-V curves as a function of pulse width showing negative differential resistance (a). Extracted critical resistivity as a function of pulse width (b).

Similar to the DC results, the pulsed I-V shows an abrupt transition at a critical field of 11 kV cm^{-1} . Here, we plot a smoothed and interpolated trace of the pulsed I-V data as a result of significant

noise introduced by subtraction of the two captured waveforms. The change in resistivity across the IMT is found to be roughly $10\times$, which is expected for a transition from CCDW to NCCDW. Additionally, the critical resistivity for the IMT can be extracted from the pulsed IV. It is plotted as a function of pulse width in Figure 52b. The critical resistivity for IMT from pulsed I-V matches with the DC data and does not vary for pulse widths from 3 s down to 300 μs . Below this point, RC time delay from parasitic capacitances in the cabling and measurement setup begin to dominate.

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6. Summary and Conclusions

In this dissertation, the two-dimensional materials of graphene and TaS₂ were examined in detail. The goal of this dissertation was to attempt to elucidate some of the potential applications and challenges facing these two materials. Several issues related to the development of a graphene based transistor for use in high frequency applications and the optimization of the graphene based transistor for mixing applications were presented. A comprehensive transport study on epitaxial, quasi-free-standing epitaxial graphene was used to show the effect of hydrogen intercalation as well as the role of step-edges in degrading the ultimate transport properties of the as-grown graphene. The scattering models developed to understand graphene were applied to study the impact of various dielectric overlayers, comparing the two-dimensional h-BN to the conventional high- k dielectric HfO₂. Finally, an analysis of graphene mixer design was utilized to highlight the benefit of the use of graphene nano-ribbon geometries to mitigate contact effects in highly scaled devices.

In the second portion of the dissertation, the layered two-dimensional material 1T-TaS₂ was explored for potential applications in electronics, where use of its insulator-metal-transition could be utilized to implement a steep-slope transistor in order to overcome conventional constraints which currently limit performance of highly scaled silicon transistors. To do this, the insulator-metal-transition was studied. The results suggest a carrier driven collapse of the insulating state which operates on the ns time scale.

6.1 Graphene Ambipolar Mixer

In this dissertation, the operation and limiting factors of the ambipolar graphene mixer were explained. The results of the transport studies on EG and QFEG confirm that hydrogen passivation of the SiC can be extremely effective in reducing the contribution from both remote charged impurity and

remote surface optical phonon scattering from the underlying substrate. Furthermore, they demonstrate for the first time that step-edges can be a significant source of additional impurity scattering as well as remote surface optical phonon scattering. Comparing the use of h-BN and HfO₂ dielectric top-gates, it was shown that use of the two dimensional h-BN represented a trade-off between reducing the incorporation of additional remote charged impurity scatterers versus preserving a high dielectric constant environment to screen charge carriers within the graphene from these same remote charged impurities. The ultimate effectiveness of the h-BN overlayer was found to depend critically on the initial impurity concentration of the as-grown graphene.

It was shown that the CTR and its associated phenomena of Dirac shift and increased asymmetry for short-channel devices significantly degrade the performance of the ambipolar graphene mixer. The advantages of nano-ribbon geometries for mixing applications are examined, and preliminary simulations of the benefits of multi-ribbon RF nano-ribbon GFETs for active mixing applications are presented, showing a 20 dB improvement in gain at $L_{ch}= 300$ nm.

However, several key areas of the ambipolar GNR mixer remain unevaluated, including linearity and noise benchmarking against sheet based ambipolar mixers and conventional technologies, optimization of the GNR FET electrostatics, how choice of metal can affect the CTR, and investigation into other forms of graphene with higher mobilities.

Significant optimization of the GNR FET for mixing is possible. First, ribbon width and density should be selected in order to optimize the electrostatics to maximize g'_m as shown in Figure 52. On the other hand, degradation in mobility due to enhanced edge scattering for ribbons with widths < 100 nm has been reported by many researchers in the field. Therefore, electrostatics and edge scattering must be accordingly balanced in order to achieve peak conversion gain. In order to complete this task, a more complete understanding of edge scattering as a function of ribbon width is necessary, which can be accomplished with the fabrication of Hall bar structures or gated TLM structures to extract Hall mobility or effective mobility as a function of ribbon width.

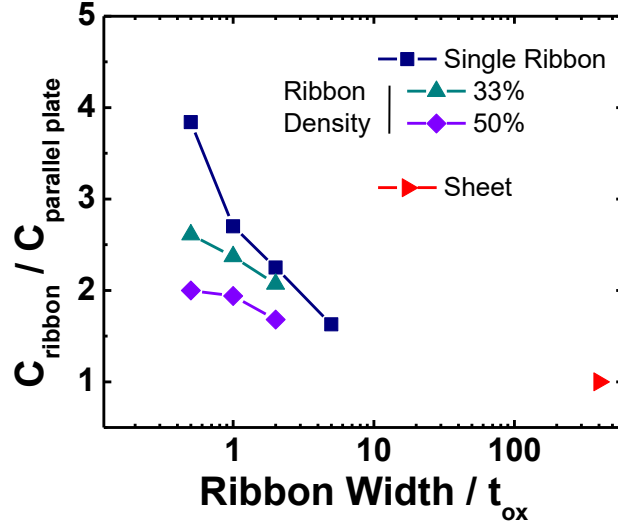


Figure 52: Simulated dependency of ribbon density on capacitive coupling.

Similarly, further scaling of t_{ox} can also lead to improved electrostatics and can benefit ultimate mixing performance. On the other hand, it remains to be seen if continued scaling of t_{ox} to $EOT < 1\text{nm}$ precludes use of nanoribbons to enhance gate coupling. This is due to the fact that at exceedingly small EOT, the necessary ribbon widths to achieve any enhanced gate coupling over the sheet case may be unrealistically small for conventional lithographic means. In order to understand these aspects of ambipolar mixer design and facilitate optimization of the graphene mixer, we propose development of an I-V simulator that fully captures the behavior of the CTR as a function of dielectric environment, channel length, and graphene ribbon width. This simulator should be calibrated to experimental results and can be used to predict the optimal ribbon width and density to achieve the highest performing ambipolar mixer.

6.2 1T-TaS₂ for Steep Slope Devices

1T-TaS₂ represents an interesting material for study of correlated phases in low-dimensionality materials, with several competing equilibrium states and a Mott insulating phase. Recent work has explored ultra-fast melting of 1T-TaS₂'s insulating Mott state using pulsed optical or electronic means to produce meta-stable states of intermediate resistivity and variable duration. In this work, we have probed the abrupt, resistive switching between equilibrium states using DC and pulsed voltages as well as DC current sourcing. An abrupt reduction in resistivity corresponding to a phase transition from the Mott state to the metallic phase is observed for both V-mode and I-mode as well as pulsing down to a minimum pulse width of 30 μ s. Importantly, this phase transition is shown to occur at a critical resistivity of 7 m Ω -cm and the transition time appears to be significantly smaller than other small gap Mott insulating materials where avalanche breakdown occurs in a time range of 10 μ s – 1 ms. These results suggest that the observed transition is facilitated by a carrier driven collapse of the Mott gap or charge ordering within the TaS₂ which results in a fast (3 ns) collapse of the insulating state.

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Vita

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Matthew J. Hollander was born in Allentown, Pennsylvania in October of 1986. He earned his undergraduate degree in Electrical Engineering from the Schreyer Honors College at the Pennsylvania State University in 2009, with distinction and honors in Materials Science and Engineering and minors in Materials Science and Engineering as well as Physics. His undergraduate thesis focused on the effect of deposition parameters and oxygen annealing on gadolinium oxide films for radiation dosimetry and was supervised by Prof. Douglas Wolfe and Joshua A. Robinson. Continuing his academic career, Matthew joined the research group of Prof. Joshua Robinson to begin his work on the two-dimensional material graphene. During this period, Matthew began to focus more narrowly on device applications for graphene, working to understand the transport properties of graphene coated by various dielectric overlayers. After receiving his M.S. in Materials Science and Engineering in 2011, Matthew continued his work with Prof. Joshua Robinson, but returned to the Electrical Engineering Department to work towards his Ph.D. while being co-advised by both Prof. Joshua Robinson and Prof. Suman Datta. He received his Ph.D. from the Department of Electrical Engineering in 2015. Matthew is currently employed by Micron Tehcnology, Inc. where he is working as an Emerging Memory Engineer in Boise, Idaho.

During his PhD, Matthew published 20 journal and conference papers, of which 6 were first author. His work on hexagonal boron nitride for use in high frequency graphene radio frequency transistors earned him the best student paper award at the 2012 Device Research Conference. Matthew can be reached via email (concatenate@gmail.com).