DESIGN AND CHARACTERIZATION OF NOVEL RF CIRCUITS
BASED ON EMERGING MATERIAL SYSTEMS

A Dissertation in
Electrical Engineering

by
Himanshu Madan

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The dissertation of Himanshu Madan was reviewed and approved* by the following:

Suman Datta  
Professor of Electrical Engineering  
Dissertation Advisor  
Co-Chair of Committee

Joshua Robinson  
Corning Faculty Fellow  
Assistant Professor of Materials Science and Engineering  
Co-Chair of Committee

Srinivas Tadigadapa  
Professor of Electrical Engineering

Julio Urbina  
Associate Professor of Electrical Engineering

Kultegin Aydin  
Professor of Electrical Engineering  
Head of the Department of Electrical Engineering

*Signatures are on file in the Graduate School
ABSTRACT

Novel material systems like Transition Metal Oxides (TMO) and 2-dimensional materials have garnered a lot of interest amongst researchers due to their unique properties. Currently, there exist several fundamental questions as to the role these materials might play in future electronic applications. My research has focused on the application of these novel materials towards radio frequency (RF) circuits by exploiting their unique properties. More specifically, I have demonstrated an electrically triggered vanadium di-oxide (VO₂) RF switch with a record 26.5 THz cut-off frequency, and a graphene RF ambipolar mixer with a record low conversion loss (14dB) for a single graphene field effect transistor (GFET) design.

This dissertation primarily focuses on VO₂, a TMO that undergoes a solid state phase transitions, which is accompanied by an insulator-to-metal transition (IMT). First, the quantitative mapping of both thermally and electrically induced inhomogeneous IMT in VO₂ at the nanoscale, using Scanning Microwave Microscopy (SMM) is demonstrated. Next, the switching dynamics using a numerical model is discussed. Finally, this dissertation presents how the unique switching physics of VO₂ can be used to develop an electrically triggered VO₂ RF switch. This demonstration provides evidence to support that VO₂ switches can achieve good isolation and high frequency of operation that is typical of MEMS based switches, and also simultaneously achieve the high speed operation and form factor that is typical of solid state switches.

The later part of this dissertation covers a detailed study of the graphene RF mixer, comparing ambipolar and drain mixing for the first time. Transfer and output characteristics of the graphene transistor were also analyzed in order to achieve the highest performance for both mixing configurations. The optimized graphene RF mixer achieved a high conversion gain of -14 and -16 dB at LO power 0 dBm at 4.2 and 10 GHz, respectively, 20dB higher than previously reported ambipolar mixer.
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Chapter 1

Introduction and Organization

I. Introduction to Vanadium Di-oxide (VO$_2$)

Vanadium di-oxide (VO$_2$) is a transition metal oxide which undergoes a thermally driven structural change from the monoclinic (M1) to tetragonal (rutile, R) phase with increasing temperature centered around a transition temperature ($T_c$) of approximately 341K [1]. This transition is accompanied by a rapid change in optical properties as well as a change in the electronic conductivity over several orders of magnitude. Additionally the insulator-to-metal transition (IMT) can be induced by mechanical [2], optical [3], or electrical stimuli [4]. The rapid nature of this transition, which can occur as quickly as ~100fs [3], has sparked significant interest in the material for possible applications including, but not limited to, coupled oscillators [5], radio frequency (RF) switches [6], [7], and thermochromic devices [2], [8].

Figure 1-1: Visualized of (a) monoclinic and (b) rutile lattice structures where cyan represents vanadium atoms and red oxygen atoms.
Figure 1-1 shows the schematic representation of the VO$_2$ lattice structure in the monoclinic and the rutile phase. In the rutile phase, the lattice exists in a high order symmetry, whereas in the monoclinic phase the lattice exist in a lower order symmetry due to presence of dimerization of vanadium atoms [9]. The non-magnetic nature of the VO$_2$ monoclinic phases, the doubling of unit cell, the pairing of metal atoms, and the presence of dimerization in the low temperature (T<T$_c$) suggests that VO$_2$ represents a typical case of Peierls insulator. However, the presence of 0.6eV large bandgap [10], a large change in the conductivity (>10$^4$) [11], and the presence of a partial dimerized phase (M2) which is still insulating [12], rules out a purely Peierls-type mechanism [13], and instead suggests that VO$_2$ also behaves like a strongly correlated Mott-Hubbard [14], [15] system. The driving mechanism of this phase transition is still debated and no clear consensus has been reached on whether it is a Mott or a Peierls transition [4], [16]–[18]. Regardless of the driving mechanisms of this transition, it is crucial to understand the nanoscale evolution of the insulator to metal phase transition for the development of practical devices for electronic application. In this work we will focus on the dynamics of this phase transition and take advantage of the accompanying large conductivity change to demonstrate an electrically triggered VO$_2$ RF switch with record performance.

**Organization**

Chapter 2 introduces the near-field scanning microwave microscopy (SMM) and uses it to quantitatively map the spatially inhomogeneous IMT in vanadium di-oxide with a lateral resolution of 50nm. SMM is used to measure spatially resolved electronic properties of the phase coexistence in an unstrained VO$_2$ film during the electrically as well as thermally induced IMT. A quantitative impedance map of both the electrically driven filamentary conduction and the thermally induced bulk transition is established. This was modeled as a 2-D heterogeneous resistive network where
the distribution function of the IMT temperature across the sample is captured. Applying the resistive network model for the electrically induced IMT case, we reproduce the filamentary nature of electronically induced IMT, which elucidates a cascading avalanche effect triggered by the local electric field across nanoscale insulating and metallic domains. Chapter 2 uses material from author’s reference [19]. The copyright of this reference belongs to © 2015 ACS Nano.

In chapter 3, we discuss the application of VO₂ for RF switch application. In particular, we demonstrate an electrically triggered VO₂ RF switch with a record switching cut off frequency (F_{CO}) of 26.5THz. The switch exhibits a low 0.5dB insertion loss and isolation better than 35dB up to 50GHz. The switch shows a highly linear response with 1-dB compression point (P_{1dB}) better that 15dBm and output third-order intercept point (OIP₃) better than 44dBm. Furthermore, the fast insulator to metal-transition (IMT) switching nature of the VO₂ materials enables the switch to have a turn on delay of less than 25ns. Chapter 3 uses material from author’s reference [20]. The copyright of this reference belongs to © 2015 IEEE.

II. Introduction to Graphene

Graphene was discovered in 2004 [21], and ever since its discovery it has garnered a lot of attention within the scientific community. Graphene is a 2-dimensional material with carbon atoms arranged in a hexagonal honeycomb like structure. Figure 1-2 shows the honeycomb lattice structure for graphene. Each carbon atom is bonded with three neighboring carbon atoms with a bond angle of 120° and C-C atomic separation of 0.142nm. The lattice consists of two types of C-C bonds. First, an in-plane σ-bond formed from sp² hybridized orbitals connects the carbon node to its neighboring three carbon atoms. Second, the remaining π-electron orbital forms a highly delocalized π-orbital. The high order of symmetry and two-dimensional nature of graphene leads to exceptional mechanical [22], [23] and electrical properties [24], making graphene a potential
candidate for new and upcoming applications. The applications include but are not limited to high frequency electronics [25], energy storage [26], composite materials [27] and optoelectronics [28].

Figure 1-2. Honeycomb graphene lattice structure with identical sublattices labeled as A and B.

Figure 1-3. Three dimensional band structure of monolayer graphene honeycomb lattice.
Figure 1-3 shows the energy momentum distribution of the monolayer graphene lattice in the first Brillouin zone. The conduction band and the valance band meet at 6 corners in the $k$-space and the point where the two band meet is called the Dirac point. Graphene is often referred as a semi-metal due to presence of zero bandgap. The energy dispersion ($E(k)$) relation around the Dirac point is described by Eq. 1-1.

$$E(k) = \pm \hbar v_F \sqrt{k_x^2 + k_y^2}$$  \hspace{1cm} \text{Eq. 1-1}

Here $v_F$ is the fermi velocity and, for a monolayer large area graphene, it is equal to $10^6$ m/s. It is important to note that the linear dispersion relation described by the Dirac equation is classically different form the parabolic energy dispersion relation (Schrödinger equation) for a conventional semiconductor. Consequently, the charge carriers in graphene behave like massless Dirac fermions and graphene is treated as a 2 dimensional gas of particles [29].

The lack of bandgap in graphene leads to a poor on-off ratio ($I_{ON}/I_{OFF}$) in graphene based FETs, making large area graphene unsuitable for logic gate applications. Researchers have been able to open bandgap in graphene to a varying degree of success by either patterning nano-ribbons [30], [31] or by strain engineering [32]. More specifically, they have succeeded in opening bandgaps of $>200\text{meV}$ for graphene nano-ribbons [30]. However, in doing so, they have introduced line edge roughness and impurities into the system and that has compromised the mobility and transfer characteristics of graphene FETs. Despite the current progress, graphene based logic technology is still far from being practical. However, graphene is an excellent candidate for analog and RF applications and has received a lot of attention in the RF and analog research community.
Figure 1-4. Unity current gain cut-off frequency vs gate length for state of the art graphene FETs [33]–[35] compared to conventional semiconductor [36]. Adapted from Ref [36].

Much of graphene’s promise for RF applications comes from its potential to operate at ultra-high frequencies, which is a result of high carrier mobilities (>10,000 cm²/Vs) [37] as well as high effective carrier velocities [38]. Here in Figure 1-4 we see a plot of $f_t$ (unity current gain cut-off frequency) versus gate length ($L_g$) for recent experimental graphene device demonstrations compared to state of the art InP, GaAs, and Si technologies. The demonstration of graphene FETs with $f_t$ >400GHz [33] shows the competitiveness of the relatively young graphene technology as compared to more mature conventional technologies. With continued optimization and development, graphene has the potential to surpass these conventional technologies in analog applications, although there remain several barriers to be overcome such as dielectric engineering, contact resistance, output conductance, etc.

Besides its excellent transport properties, graphene also exhibits symmetric electron and hole conduction, as a result of its unique, symmetric band structure about the Dirac point (i.e. equal $v_F$ for electron and hole). Symmetric electron-hole conduction and graphene’s lack of band gap leads to an ambipolar behavior that produces graphene’s unique ‘V’-shaped transfer characteristics.
In recent time, this ambipolar response has been used for variety of applications [39], [40] and in this dissertation we specifically exploit this characteristic to design and demonstrate a graphene based ambipolar RF mixer.

**Organization**

In chapter 4, a graphene RF transistor with a gate length of 750 nm, a width of 20 μm, and an equivalent oxide thickness (EOT) of ~2.5 nm was fabricated and used to demonstrate an ambipolar graphene mixer with a record high conversion gain of -14 and -16 dB (LO power 0 dBm) at 4.2 and 10 GHz, respectively. The ambipolar graphene RF mixer performance was also compared to resistive configuration, highlighting the suppression of odd order intermodulation products and superior conversion gain for the ambipolar mixer configuration. Chapter 4 uses material from author’s reference [41]. The copyright of this reference belongs to © 2012 IEEE.
Chapter 2

Mapping Phase Transition in Vanadium Di-oxide (VO₂) using Scanning Microwave Microscopy (SMM)

As the potential VO₂ based device technologies scale into the decananometer regime, novel characterization techniques are required to locally probe the structural, optical, and electronic properties at the nanometer scale. This is, in part, due to the coexistence of both the metallic and insulating phases within the span of the IMT [16]. Within VO₂, there remains much interest in imaging the domain size and unraveling the nature of the IMT in order to shed additional light on the transport mechanisms and fundamental length scales involved. Thus, spatially mapping the exact nature of the IMT at the nanoscale has been the subject of intense research through a variety of scanning techniques: scanning tunneling spectroscopy (STS) [42], scanning transmission x-ray microscopy (STXM) [43], [44], optical microscopy [44], [45], broadband near-field infrared microscopy [16], and, most recently, scanning microwave microscopy (SMM) [46], [47]. Table 1 summarizes the key aspects of these spatial mapping techniques. Each of these techniques have evolved from a need for nanometer scale characterization of material and device properties and are beginning to offer researchers powerful new insight.

Table 2-1. Comparison summary of various solid state RF switch from literature.
Scattering near-field optical microscopy (s-SNOM) is a nanoscale measurement sensitive to the complex dielectric function of a material [48]. Here an incident laser is used to generate a dipole interaction between an atomic force microscopy (AFM) tip and the local sample area, causing scattering. The measured scattered fields then contain information on the complex dielectric function at the nanoscale. In s-SNOM the resolution limitation falls on the radius of curvature of the tip which has so far allowed for lateral resolutions of 20nm [16]. Classical x-ray diffraction (XRD) has been modified to scanning transmission x-ray microscopy (STXM) which has been used to probe the lattice structure at the nanoscale [43], [44]. However, advanced photo sources such as the 2-ID-D beamline at Argonne National Laboratory to achieve a spot size of 250nm are required. STM, on the other hand, provides an alternate perspective where only an interrogation of the immediate surface takes place. This has revealed the existence of residual insulating/metallic surface domains deep into either the metallic or insulating macro state of the VO₂ transition [42]. Meanwhile, SMM has emerged as a means for electrical characterization at the nanoscale level. SMM is a high frequency microwave scanning probe technique where sensitivity is derived from a transformed nanoscale complex impedance at the AFM tip. Sensitivity of up to attofarad capacitances using SMM have already been demonstrated [49]. However translation of the measured electrical data into an impedance map has proved to be a limitation, with demonstrations being limited to MOS capacitors [50]–[52] and other silicon and silicon dioxide test structures [53]. Here, through a calibration of the SMM acquired microwave response using finite element modeling (FEM), an extraction of the nanoscale R and C values seen at the SMM tip is realized. The nanoscale R and C values can then be plotted as a spatially resolved impedance map. Thus, a direct probing of the nanoscale conducting and insulating domain resistances is now possible, and are, for the first time, demonstrated during both thermal and electrically driven phase transition.
I. Introduction to Scanning Microwave Microscopy

SMM is a high frequency microwave scanning probe technique which measures a transformed nanoscale complex impedance at the AFM tip during a 1-port reflectivity measurement. Changes in the reflection coefficient ($\Gamma$) are recorded at the VNA port ($\Gamma_{port}$). The changes in $\Gamma_{port}$ are due to a change in the resonant frequency caused by variations in the local impedance beneath the SMM tip. These changes in the output signal of the SMM are recorded in two channels, $\text{abs}(\Gamma_{port})$ and $\text{phase}(\Gamma_{port})$.

Setup

Figure 2-1. SMM setup visualized in contact with VO$_2$ sample. VNA is connected to half wavelength coaxial resonator terminating in Pt conducting AFM tip in conjunction with a 50 ohm shunt.

Figure 2-1 is a schematic representation of the SMM setup where an AFM is used in conjunction with a vector network analyzer (VNA). Here, a commercially available Agilent 5420 AFM is used with an Agilent E8364C VNA and scanning microwave nosecone assembly (N9546A-
CFG001 to carry out measurements. Imaging must be performed in contact mode for a properly synced response between the AFM and VNA sweep. A conductive Platinum (Pt) tip (manufactured by Rocky Mountain Nanotechnology) made from a solid conically etched Pt wire with a terminating radius of approximately 25nm is affixed to a Pt cantilever. The cantilever is then mechanically attached to a sapphire chip completing the tip package. The tip has a height of 80μm, which is significantly larger than that of coated silicon tips at 30μm. The increased tip height results in a reduction of fringe capacitance between the cantilever shank and the sample under test, thereby improving the measurement accuracy. The tip is mounted on a SMM nose cone that consists of a half wavelength (λ/2) coaxial resonator in conjunction with a 50Ω shunt resistor. A λ/2 resonator is required due to the mismatch in the impedance between the characteristic 50Ω impedance of the transmission line and the large impedance seen by the SMM tip. Without the λ/2 impedance transformer, total reflection would be measured regardless of the changes in the impedance at the tip during the imaging. With the inclusion of the λ/2 transformer and 50Ω shunt, variations around a very large impedance at the SMM tip are converted to variations around 50Ω. By establishing a resonant frequency condition of approximately every 2.57GHz (Figure 2-2(a)), the λ/2 resonator allows for the highest measurement sensitivity to be located in a narrow frequency range around the λ/2 condition. The measurement frequency is set in this narrow frequency range and the VNA is set to record the changes in abs(Γ_{port}) and phase(Γ_{port}) as the AFM tip scans the sample. However, due to the inclusion of a λ/2 coaxial resonator, Γ_{port} at the VNA is representative of a transformed impedance at the tip and not of the true nanoscale impedance (Z_{tip}).
Figure 2-2. (a) $\text{abs}(\Gamma_{\text{port}})$ amplitude parameter collected at the VNA port for a lifted tip with no sample under test. The chosen scan frequency is highlighted by the red box. (b) Close up of the resonance peak used during SMM scanning. $\text{abs}(\Gamma_{\text{port}})$ response amplitude shown in black, phase($\Gamma_{\text{port}}$) in blue.

A standard resonance response of the SMM nose cone from 1 to 18GHz is shown in Figure 2-2(a). The resonant frequency at 16.024GHz was used for all scans due to a very sharp peak allowing for a high dynamic range. The peak can be more closely examined in Figure 2-2 (b). The frequency sweep was taken while the tip remained elevated above the sample under test. The steep slope of the resonance peak (75dB/MHz and 530°/MHz) allows for small shifts in the resonance to generate large resolvable changes in the $\text{abs}(\Gamma_{\text{port}})$ and phase($\Gamma_{\text{port}}$) channels respectively. Additionally, in comparison to other low frequency and DC c-AFM techniques, the inclusion of a second electrode is not required in SMM imaging. This is due to the inclusion of ground plane inbuilt to the SMM nose cone located directly underneath the sapphire SMM tip holder as illustrated in Figure 2-1. Completion of the microwave path to the ground plane occurs by capacitive coupling ($C_{\text{ground}}$) through air. A large coupling capacitance to the ground plane is required for meaningful imaging to take place, otherwise the measured reflection will be indicative of $C_{\text{ground}}$. In order to
realize an effective coupling capacitance a low resistance path must be made available to the signal through the substrate.

II. VO₂ Test Structure

The structure used for this study is composed of a 100 nm-thick VO₂ film that is electrically isolated from a highly conductive n+-Si substrate by a 100 nm-thick thermally grown SiO₂ layer. A single-phase VO₂ film was formed using a two-step process. The VO₂ film was grown by initially performing pulsed DC mode sputtering with a solid vanadium target at 5mTorr with 97.5% argon and 2.5% oxygen flow on SiO₂(100nm)/Si(675μm) sample. The total sputtering time was 15 minutes. This resulted in VOₓ where the oxygen content (x) is less than 2. Thereafter, the vanadium film was annealed at 598K for 10 minutes with 10 standard liters per minute (slpm) argon flow and 0.1 slpm oxygen flow. Characterization of the VOₓ film using x-ray diffraction (XRD) showed that a single phase VO₂ film was formed. 20nm Pt/40nm Au contacts were lithographically defined and deposited by e-beam evaporation. Two terminal devices were patterned in an array with channel lengths and widths each ranging from 2μm to 160μm.
Figure 2-3. X-Ray diffraction scan performed on the unpatterned VO₂ film upon completion of growth.

Formation of a single phase VO₂ film was confirmed by XRD measurement which can be seen in Figure 2-3 of the supporting information. The conducting (0.1Ω-cm) Si substrate is used to produce a large coupling capacitance to the ground plane, which is required for meaningful SMM imaging. The measured resistivity vs. temperature characteristics of the VO₂ film shown in Figure 2-4(a) confirm the transition temperature is near the expected value of 341 K for unstrained VO₂. In addition, the VO₂ film exhibits reversible electric-field-induced IMT switching properties as shown in Figure 2-4(b).
III. Thermal IMT

SMM allows nanoscale imaging of the emergence and coalescence of nanoscale metallic domains as VO$_2$ undergoes a temperature induced phase transition. All SMM scans were taken over the same 2.5μm by 2.5μm scan area on the VO$_2$ sample. Upon stepping the temperature a 5 minute wait period was taken to allow for the sample surface to reach thermal equilibrium before SMM measurement was performed. The thermal drift was compensated for manually. Since contrast in SMM is derived from variations in the local impedance directly under the SMM tip, a change in the local impedance due to the presence of metallic and insulating domains will create a change in the response of abs($\Gamma_{port}$) and phase($\Gamma_{port}$). In order to clearly identify the insulating phase response without the presence of metallic domains an initial baseline scan was taken at 310K.
Figure 2-5. (a) 2.5µm x 2.5µm AFM topography scan at 310K, (b) corresponding abs(Γ_{port}) response. (c) Horizontal line trace of normalized AFM topography taken 1.8µm from the bottom of the scan, (d) corresponding line trace of normalized abs(Γ_{port}) response.

Figure 2-5 shows the measured (a) normalized topography and (b) normalized abs(Γ_{port}) during the fully insulating phase at 310K. The amplitude response, abs(Γ_{port}), only varies with the topography as demonstrated by the horizontal line cut in Figure 2-5c-d. The horizontal cut is taken at a position of 1.8µm from the bottom of the scanned region. Since no large deviations in the abs(Γ_{port}) response from the topography are seen this indicates that the contrast pattern is the result of variations in solely the capacitance between the SMM tip and the substrate arising from surface roughness. Here it is important to note that the purely insulating state only leads to changes in
abs(Γ_{port}) of about 0.15dB, this confirms the previous statement the abs(Γ_{port}) variations are due to surface roughness as the presence of metallic domains cause a much larger change in abs(Γ_{port}).

![Figure 2-6](image.png)

Figure 2-6. (a) abs(Γ_{port}) response to insulating and conducting regions at 332.5K and the corresponding (b) phase(Γ_{port}) response. Large distinct changes between insulating and metallic domain response are observed in both traces.

The dramatic difference in the local impedance between the insulating and metallic domains would lead to a significant change in the abs(Γ_{port}) resonance response. The contrasting frequency responses of Γ_{port} corresponding to the metallic and insulating domains, encountered during the IMT, are shown in Figure 2-6(a) and (b). The frequency dependent sweeps were collected by taking sweeps of the abs(Γ_{port}) and phase(Γ_{port}) channels with the tip contacting different regions corresponding to insulating and metallic domains upon completion of imaging. At the measurement frequency of 16.024 GHz a change of 22dB and 55° in the abs(Γ_{port}) and phase(Γ_{port}), respectively, is recorded between metallic and insulating domains. This is in stark contrast to the 0.2dB and 4° observed at the insulating temperature (310K) (Figure 2-5).
Domain Evolution during Thermal IMT

Figure 2-7. (a-c) Normalized AFM topography of a 2.5µm x 2.5µm size scan region at 327.5K, 332.5K, and 337.5K, respectively. Lighter regions are peaks while dark regions are valleys; maximum range of surface topography is 6nm. (d-e) Corresponding abs($\Gamma_{\text{port}}$) for each of the given temperatures. Expansion of the metallic phase (red) is observed while the (blue) insulating phases diminish with increasing temperature.

The metallic phase first appears at 315K and expands throughout the sample as the applied temperature progresses through the IMT. In Figure 2-7(d-f) the spatial abs($\Gamma_{\text{port}}$) response is plotted documenting a subset of the IMT. The red regions are that of the conducting domains while the blue regions are the insulating domains. As the temperature is increased the coverage fraction of the metallic phase begins to approach total coverage and reaches the maximum possible coverage at a temperature slightly beyond 353K.

Figure 2-8 show the line scan of Figure 2-7 (b,e) (332.5K) where conducting domains have appeared within the insulating matrix. Here the large changes in abs($\Gamma_{\text{port}}$) ($\Delta$abs($\Gamma_{\text{port}}$) = 27dB) are
due to the large change in impedance between insulating and metallic domains which coexist in the scan area. The response is no longer pinned to the topography suggesting that a modulation of the capacitance due to film roughness can no longer be the source of the large change in abs(Γ_{port}) and phase(Γ_{port}) but must be indicative of the true electrical properties of the insulating and metallic phases coexisting within the film. In Figure 2-8(b,c) the insulating domain response can be seen at -60dB abs(Γ_{port}) and 20° phase(Γ_{port}), as indicated by dashed line. For the metallic domains, the value of the abs(Γ_{port}) and phase(Γ_{port}) response is at -33dB and 79° respectively.

![Figure 2-8](image)

Figure 2-8. Line trace at 332.5K taken at 1.5μm from the bottom of Figure 2-7(b,e). (a) Topography, (b) corresponding abs(Γ_{port}) response, (c) accompanying phase(Γ_{port}) response.

The SMM imaging of the phase coexistence in VO₂ yields results that are consistent with previous measurements and established models for the IMT. A full set of the SMM scans can be found in the Appendix B and all scans were found to be repeatable. Here it is observed that throughout the IMT transition nanoscale metallic domains appear within the insulating matrix and with increasing temperature reach a threshold radius of approximately 100nm before coalescing to form larger regions. The observed phase coexistence is indicative of the film being comprised of
nanoscale domains with varying transition temperatures owning to defects, composition, and local strain. This observation motivates modeling the film as a 2-D heterogeneous domain network which is representative of the macro-scale response seen in SMM.

Simulation Model

Figure 2-9(a) shows the 2-D heterogeneous resistive network model where each nanoscale VO₂ domain is taken as a node with four perpendicularly placed resistors. Each cell is representative of a single nanoscale domain which when placed together in an \( m \times n \) network describe the behavior of the macroscale sample. In accordance with the measured domain size of \( \sim 100 \text{ nm} \), a single domain is taken to be 100nm in length and width. As such the model was run at 50x50 domains, modeling an area of 5μm x 5μm. Each node can be in the insulating or metallic state. The insulating state resistivity is defined by Eq. 2-1 [54] where \( E_a \) is the activation energy (0.19eV), and \( \rho_1 \) is a fitting parameter (1.29x10⁻⁵Ω·cm).

\[
\rho_{m1}(T) = \rho_1 e^{\left(\frac{E_a}{k_B T}\right)}
\]  
Eq. 2-1
Figure 2-9. (a) Nanoscale domain network used to model VO$_2$. The network consists of $m \times n$ domains each with a specific insulator to metal transition temperature, $T_{ij}^{\text{IMT}}$. (b) Comparison of simulated and measured resistivity. (c) Comparison of simulated and SMM measured metallic domain fraction. The SMM metallic domain fraction was calculated by weighted average of the measured $|\Gamma_{\text{port}}|$ response. And the metallic state resistivity $\rho_r$ is $5.53 \times 10^{-4} \, \Omega \cdot \text{cm}$. By assuming that each cell in the network has a specific transition temperature, $T_{ij}^{\text{IMT}}$ & $T_{ij}^{\text{MIT}}$ and distributing the transition temperatures of the individual domains across a Gaussian distribution centered on the macroscopic $T_c^{\text{IMT}}$ and $T_c^{\text{MIT}}$ [55] (distributions are shown on the Y2-axis in Figure 2-9(b) as wells as Figure 2-9(a)) the insulator to metal transition can be reproduced. In the model a domain is considered to
undergo a metal to insulator transition once the temperature of the sample has exceeded the transition temperature \( T_{i,j}^{\text{IMT}} \) of the given domain \( i,j \) (for heating). After each temperature the resistivity is calculated from the resistance which comes from solving the potential at each node in the domain network as described in Poklonski et al [56]. The simulated resistivity is then plotted against the physically measured values shown in Figure 2-9(b). Figure 2-9(c) shows the metallic fraction (percentage of total domains that are in the metallic state) computed during the simulation as a function of temperature. This is overlaid upon the metallic fraction taken directly from SMM measurements. The SMM measured fraction is taken from \( \text{abs}(\Gamma_{\text{port}}) \) and was calculated by a weighted scaling of the measured \( \text{abs}(\Gamma_{\text{port}}) \), where the maximum value was considered to be completely metallic and the lowest value was considered to be completely insulating. The intermediate values were taken to be linearly proportional to metallic fraction. The strong correlation between the measured and simulated metallic fractions as well as measured and simulated resistivity indicates that the assumption of a 2-D heterogeneous resistive network is reasonable.

**Impedance Mapping**

In order to further use SMM to characterize the nanoscale domain structure of the thermally driven IMT in VO\(_2\) the \( \text{abs}(\Gamma_{\text{port}}) \) and \( \text{phase}(\Gamma_{\text{port}}) \) response must be transformed to true nanoscale impedance \( Z_{\text{tip}} \). This has proved to be a major hurdle that has been the subject of recent research in calibration of the \( \text{abs}(\Gamma_{\text{port}}) \) and \( \text{phase}(\Gamma_{\text{port}}) \) that are collected at the VNA port. A successful calibration of \( \text{abs}(\Gamma_{\text{port}}) \) and \( \text{phase}(\Gamma_{\text{port}}) \) will yield a spatial map of the resistance and capacitance seen locally at the SMM tip. In order to relate \( \Gamma_{\text{port}} \) to \( Z_{\text{tip}} \) we employ a standard single-port VNA calibration where three known impedances from a model are used to solve a nonlinear system of equations. This begins by relating \( \Gamma_{\text{port}} \) and \( Z_{\text{tip}} \) in the following equations [52], [57].
\[ \Gamma_{port} = e_{00} + \frac{\Gamma_{tip} e_{01}}{1 - e_{11} \Gamma_{tip}} \]  
\[ \text{Eq. 2-2} \]

\[ \Gamma_{tip} = \frac{Z_{tip} - Z_{ref}}{Z_{tip} + Z_{ref}} \]  
\[ \text{Eq. 2-3} \]

Eq. 2-2 is a complex non-linear equation with three unknowns, namely \( e_{00}, e_{01}, e_{11} \). In order to solve Eq. 2-2 three known values of \( \Gamma_{tip} \) must be taken from a model. COMSOL multiphysics modeling [58] was used to determine three impedances for calibration on each scan in Figure 2-7. These three known impedances can be related to \( \Gamma_{tip} \) by Eq. 2-3. In order to accurately model the VO\(_2\) and the underlying SiO\(_2\)/Silicon substrate, impedance spectroscopy was performed vertically between patterned gold pads and a grounded chuck at multiple temperatures. A COMSOL model was designed at the full scale of the sample and the material values were tuned to fit the measured impedance spectroscopy results and determine correct parameters for the underlying substrate. These fitting results can be found in the Appendix C. The model showed that the leakage current through the oxide and substrate increased slightly with temperature, however the values largely remained the same and did not affect the output impedance more than a tenth of a percent between the scans. Utilizing the calibrated COMSOL model three values of the VO\(_2\) impedance were simulated where resistivity was taken corresponding to an average resistivity at the scan temperature, metallic state resistivity, and insulating state resistivity. The complex non-linear system of Eq. 2-2 were then solved to evaluate \( e_{00}, e_{01}, e_{11} \) at each scan temperature in Figure 2-7. Once \( e_{00}, e_{01}, e_{11} \) are obtained they are then used to calibrate the impedance map by solving Eq. 2-4 at each point of the map from the abs(\( \Gamma_{port} \)) and phase(\( \Gamma_{port} \)) to evaluate \( \Gamma_{tip} \). From Eq. 2-5 \( \Gamma_{tip} \) can be converted to a local impedance at the tip [52], [57].

\[ \Gamma_{tip} = \frac{\Gamma_{port} - e_{00}}{e_{01} + e_{11}(\Gamma_{port} - e_{00})} \]  
\[ \text{Eq. 2-4} \]
\[ Z_{tip} = Z_{ref} \frac{1 + \Gamma_{tip}}{1 - \Gamma_{tip}} \]  

\text{Eq. 2-5}

Figure 2-10. (a-c) Extracted \( R_{tip} \) values from equations (6) and (7). Blue regions represent the metallic phase and hence exhibit resistances of around 130\( \Omega \), while the red insulating regions are approximately 7000\( \Omega \). (d-e) Extracted \( C_{tip} \) values which are smaller for the insulating domains as compared to the metallic domains. This results from the capacitance being primarily due to the SiO\(_2\) layer and the conducting regions provide a larger area from which to couple to the Si substrate.

\( Z_{ref} \) is an arbitrarily chosen reference impedance for satisfaction of equations (3) and (5), a value of 10k\( \Omega \) is chosen as was done in [52] but any value will suffice. The resulting calibrated impedance maps are shown in Figure 2-10(a-f). Further, COMSOL modeling reveals that \( R_{tip} \approx R_{V_{VO2}} \) within an error range of 1%–23% with the greatest accuracy occurring in the metallic regions. The \( C_{tip} \) value however is primarily due to the SiO\(_2\) and the underlying Si substrate. In Figure 2-10(a-c) the blue regions correspond to the metallic domains and the red pertain to the insulating regions. In the \( C_{tip} \) map the red regions are the conducting domains and exhibit a larger capacitance to the large area with which the signal is capacitively coupled to the silicon substrate.
IV. Electrical IMT

The use of SMM to study the IMT in VO₂ has implications extending into the device characterization. Here SMM can be utilized for *in-situ* mapping of an electrically induced phase transition. In order to image the IMT induced by an electrical stimulus two terminal devices were patterned on the VO₂ film as can be seen in Figure 2-11(a). The devices were lithographically defined with a channel length of 6µm and width of 20µm. Pd(20nm)/Au(60nm) contacts were deposited through e-beam evaporation. In order to bias the devices during scanning the contact pads were extended far away from the device to accommodate the size of the SMM nose cone. The contact pads were then wire bonded to a standard chip carrier package which was subsequently connected to a Keithley 4200 semiconductor characterization system. The temperature of the device was raised from room temperature to 315K to allow switching to occur at lower voltages. A current *vs.* applied electric field sweep is shown in Figure 2-11(b) where it can be seen that the device switches at an electric field of 12kV/cm, a current compliance was set to 20mA.
Filamentary Conduction during Electrical IMT

Figure 2-11. (a) Device schematic for SMM imaging of the electrically induced IMT. (b) Current vs. electric field sweep take of the device under test at 315K. (c-f) In-situ abs(Γ) maps of electrically induced phase transition. A thin conductive filament forms across the channel and expands with the applied current. (c) The smallest achievable conducting filament which forms at 3.25mA (7µm x 7µm). (d-f) abs(Γ) maps show the growth of the filament as the device is subjected to higher currents (24µm x 24µm).

SMM scans were then performed at individual current input biases from 3.25mA to 20mA in order to spatially resolve the IMT within the device channel. This was performed by biasing the device with a Keithly 4200 semiconductor parameter analyzer set in current mode to the desired current value (3.25-20mA) for the duration of the scan. As the current bias was applied between the contact pads non-uniform conduction across the channel is identified within abs(Γ_{port}) and phase(Γ_{port}) of the SMM response. It can be clearly seen from Figure 2-11(c-f) that a metallic filament appears first within the insulating matrix as the conduction path. It is further observed that
as the current is increased the filament expands and eventually consumes the entire width of the channel of the device. This dependence of filament width to the applied input bias can be seen in Figure 2-12(b). Below the threshold switching current, 3.25mA in this case, no filament formation is seen within the device channel.

Impedance Mapping

Abs($\Gamma_{port}$) and phase($\Gamma_{port}$) maps are transformed into an impedance map by the process described earlier. An in-situ nanoscale mapping of the resistance characterizing the conducting filament is shown in Figure 2-12(a). In order to fit the observed filament width dependence on the applied current a uniformity factor, $\beta$ needs to be introduced. The uniformity factor provides the percentage of metallic domains that are present in the volume of the measured filament in order to account for the inhomogeneous nature of the measured filament. The filament width ($W_{fil}$) is given by Eq. 2-6.

$$W_{fil} = \frac{JW - W}{E \frac{\rho_m}{\beta} - \frac{1}{\rho_i} + \frac{1 - \beta}{\rho_i}}$$  \hspace{1cm} Eq. 2-6

Where $J$ is the current density, $\rho_m$ and $\rho_i$ are the metallic and insulating domain resistivity respectively, $L$ and $W$ are the physical device dimensions, and $E$ is the applied field. $\beta$ is a unit less factor from 0 to 1 which is extracted from the imaged filament by means of a weighted average. Extracted values for $\beta$ are within the range of 0.27-0.39 for all scans. A $\beta$ of 0.35 is used in Eq. 2-6 to fit the measured filament width in Figure 2-12(b). This directly demonstrates the ability of SMM to directly image the nanoscale conduction within scaled VO$_2$ based switches.
Figure 2-12. (a) Extracted resistance map of Figure 2-11(c) (7µm x 7µm). The blue color corresponds to conducting VO₂ regions which form a small 1.3µm wide filament spanning the device channel. The red regions corresponds to the remaining insulating portion of the channel. The black regions at the top and bottom are that of the highly conductive Au contacts. (b) The measured dependence of filament widths as a function of applied input current bias.

Simulation Model for the Filamentary Conduction

Furthermore, the 2-D heterogeneous resistive network model can be used to simulate the VO₂ sample under an applied field. This is schematically illustrated in Figure 2-13(a) where one end of the sample is grounded while the other is set to the applied voltage. Again the assumption is made that each domain can individually switch between the insulating to metallic states. As such, the probability of a domain undergoing an IMT is given by Eq. 2-7 [59].

$$P_{IMT} = e^{-\left(\frac{E_B - q\Delta V}{\gamma k_B T}\right)}$$

Eq. 2-7

Here, ΔV is the average voltage drop across the domain and E_B is the energy barrier between the stable insulating and metallic states and γ (0.35) is a geometric factor to account for the simulation grid size. Figure 2-13(b) shows how ΔV is calculated, while Figure 2-13(c) shows...
how $\Delta V$ is used to modulate the possibility of traversing the energy barrier that separates the insulating and metallic states. The probability of the domain to switch back to the insulating phase is controlled by the $(E_B - E_C)$ difference [59].

$$P_{MIT} = e^{\frac{(E_B - E_C)}{k_B T}}$$

Eq. 2-8

![Diagram](image)

Figure 2-13. (a) Nanoscale domain network used to model VO$_2$ under electrical bias. Red domains are those which have transitioned to the metallic state and while green are those that remaining insulating. (b) $V_1$, $V_2$, $V_3$, and $V_4$ are used to calculate $\Delta V$. (c) Energy landscape where the stable Mott insulating state and the correlated metal state are separated by an energy barrier $E_B$. 
The quasi-static simulation is performed by applying a voltage across the 2-D heterogeneous resistive network and calculating the potential at each node. The probability that a domain undergoes an insulator to metal transition, \( P_{IMT} \), is then calculated using the \( \Delta V \) derived from the calculated potentials at each node [56]. Based on these calculated probabilities and the probability for MIT, \( P_{MIT} \), the current state of the node is determined (0 - insulating and 1 - metallic) followed by recalculation of the potential at each node. At this point, \( P_{IMT} \) is re-evaluated using those potentials and the domain state is determined once again. This process is then repeated revealing the formation process of the filament.

Figure 2-14. Discrete simulation steps within the electrically induced IMT just as the filament formation occurs, the higher potential is applied to the right electrode. (a) The resulting voltage drop across each domain during the formation of the metallic filament is shown. The domain phase map across the device resulting from those voltage drops is shown in (b) where the red domains are insulating and the yellow domains are metallic.

From the simulation we see a small conducting phase front form near the metal contact at higher potential. The size of this metallic phase front swells to a maximum as a conducting pathway
is completely formed across the device. To understand this, consider an insulating domain surrounded by other insulating domains. The application of a large voltage across the domains will eventually cause one of the domains to switch to a lower resistance state. When this initial domain switches to a metallic state, the potential drop across this domain is significantly reduced, and is re-distributed to the neighboring domains. The increase in potential across the neighboring domains due to this redistribution of field subsequently increases the probability that one of these neighboring domain also transitions to the metallic state. In this manner, a conducting filament is formed within the device channel. Due to the interplay between the domains, the formation of the filament is an abrupt process. This process is visualized in Figure 2-14 where the voltage across each domains is shown in Figure 2-14(a) and the resulting calculated domain state from that potential drop is shown in Figure 2-14(b).

The stabilized 2D heterogeneous resistive network represents the DC state of the system in the quasi-static limit. Once this state has been determined, the voltage is stepped and the process is repeated. In this way the I-V relationship can be recreated for forward and reverse voltage sweeps, as is shown in Figure 2-15(a). The model successfully captures the abrupt nature of the IMT and closely mimics the electrical transition, including its hysteretic nature. Figure 2-15(b) shows the resulting domain state at the indicated star in Figure 2-15(a). The formation of the metallic filament across the device can be explained by the switching behavior of the domains. The barrier height $E_B$ and $E_C$ for the simulation was set to 0.55eV and 0.47eV respectively.
Figure 2-15. (a) Measured and simulated I-V characteristics, measured I-V was set to compliance of 20mA in order to prevent device failure under high currents. (b) Simulated filamentary conduction of 6μm long and 20μm wide device (with 100nm domain size) at the bias condition highlighted by * in the I-V characteristics. Metallic domains are yellow while insulating domains appear as red.

V. Conclusion

In summary, we employ SMM to study the dynamic phase coexistence and nanoscale domain structure of VO$_2$ in an unstrained film during both thermal and electrically driven IMT at 16GHz with a spatial resolution of 50nm. By modeling the nanoscale domain structure as a 2-D heterogeneous resistive network the experimental results of the thermal and electrical phase transition have been precisely reproduced. In the thermally induced IMT the results are demonstrative of a distribution of nanoscale domains with slightly varying transition temperature. The domains in turn cluster and eventually coalesce to form total metallic coverage within the film. Further, during an electrically stimulated IMT, the presence and growth of a filamentary conducting pathway is monitored and quantitatively characterized across multiple bias points. Through implementation of the 2-D heterogeneous resistive network it is shown that the nature of the
filament formation is the result a cascading avalanche effect where in the redistribution of the field across a transitioning domain upon its adjacent domains results in an abrupt switch. This work provides a quantitative framework to extract spatially resolved impedance values for a well-established IMT oxide such as VO$_2$ or other phase transition devices as they undergo phase transition and reveal their transport and switching properties.
Chapter 3

RF Switch using Epitaxial VO$_2$-On-Sapphire (VOS)

I. Introduction to RF Switch and Figure of Merit (FOM)

RF switches are an integral part of wireless technology and one of the most used components in a wireless system. They can be found in modules such as filters, antenna selectors, transmitter/receiver selectors and delay networks. RF switches perform the essential task of routing high frequency RF/microwave signals, essentially guiding these signals to appropriate transmission path. This allows a transceiver system to operate multiple RF channels independently, significantly expanding the utility and function of the wireless system. Figure 3-1 shows a circuit schematic of a diode based RF channel selector. By controlling the voltages at nodes, Bias 1 and 2, one can choose between the RF signal paths to the antenna.

Figure 3-1. Circuit schematic, illustrating the use of diode RF switch in transceiver system to select between two RF channels.
An RF switch can be either in series or shunt configuration (Figure 3-2 (a)) and in some cases have elements of both. The RF switch shown in Figure 3-1 illustrate an example with both series and shunt elements. Figure 3-2 (b) shows the working of switch in a series configuration. In the OFF-state, the series element blocks the input signal by reflecting majority of the signal back. Switch in this state is represented by a RC ($R_{off}$, $C_{off}$) parallel combination. For a good isolation between the ports, i.e. minimal transmission, it is required to have a very high $R_{off}$ and a low $C_{off}$. As the frequency of operation approaches GHz regime, the contribution from the $\omega C_{off}$ term becomes a significantly dominating component to the RF leakage path. Similarly, in the ON-state, series element provides a low-loss connection between ports, transmitting majority of the input signal with minimum distortion and reflection. ON-state is often represented by a series RL ($R_{on}$, $L_{on}$) combination and for low insertion loss it’s required for the switch to have very low $R_{on}$ and $L_{off}$. On the other hand, for a RF switch in a shunt configuration, the input to output isolation is achieved by bypassing the input RF signal to ground. Circuit designers use a combination of series and shunt elements depending on the isolation and bandwidth requirements of the design.

Figure 3-2. (a) Circuit schematic of a RF switch in series and shunt configuration. (b) Working of a RF switch in series configuration.
In majority of the RF switch design the ON-state and OFF-state impedance of a switch can be approximated to \( Z_{sw, on} = R_{on} \) and \( Z_{sw, off} = \frac{1}{i\omega C_{off}} \). The transmission and reflection ratio of a RF switch in series configuration can then be evaluated by Eq. 3-1 to Eq. 3-4).

\[
S_{11, on} = \frac{1}{R_{on} + 2Z_0} \quad \text{Eq. 3-1}
\]
\[
S_{21, on} = \frac{2Z_0}{R_{on} + 2Z_0} \quad \text{Eq. 3-2}
\]
\[
S_{11, off} = \frac{i\omega C_{off}}{1 + i2\omega C_{off} Z_0} \quad \text{Eq. 3-3}
\]
\[
S_{21, off} = \frac{i2\omega C_{off} Z_0}{1 + i2\omega C_{off}} \quad \text{Eq. 3-4}
\]

Figure 3-3. Simulated transmission response for series RF switch with different \( R_{off}, C_{off} \).

Figure 3-3 shows a simulated transmission response of a RF switch. The low frequency regime in the OFF-state transmission is often dominated by the real term of the OFF-state impedance and the response is frequency independent. As we move to higher frequency regime the
leakage from OFF-state capacitance dominates the response as can be seen from Figure 3-3. To compare the frequency of operation and insertion loss to isolation ratios of two or more types of switch, performance metric FOM and $F_{CO}$ (cut-off frequency) are often used. $F_{CO}$ is defined as the frequency at which the OFF-state switch impedance equals to the ON-state switch impedance. $F_{CO}$ can be defined in terms of the ON-state resistance ($R_{on}$) and OFF-state capacitance ($C_{off}$) as

$$F_{CO} = \frac{1}{2\pi R_{on} C_{off}}$$  \hspace{1cm} \text{Eq. 3-5}$$

The product $R_{on}C_{off}$ is referred as FOM and is measured in units of time.

### II. MEMS vs Solid State RF Switch

RF switches can be categorized into two main categories: switches based on micro-electromechanical systems (MEMS) and those based on solid state systems. MEMS switch generally consists of a fixed electrode, movable electrode and an actuator. By electromechanically moving the actuator, either the gap between two electrodes is varied to achieve a change in capacitive coupling between the electrodes or a physical connection between the electrodes is realized. Since in most MEMS based switches the ON-state connection is formed by a physical contact between the electrodes and an OFF-state by air gap, it results in a switch with a very low insertion loss and high isolation. Additionally, these switches also offer a highly linear response and have the ability to operate at very high frequency. But despite these advantages, MEMS switches performance is limited by poor speed of operation, high cost, poor reliability and high voltage/current drive requirements. Solid state switches on the other hand use their semiconducting property to implement a variable resister as a switching element. Within the overall category of solid state RF switches, conventional devices can be further grouped into several sub-categories, including PIN diodes, GaAs PHEMTs [60, 61], GaN HEMTs [62, 63], silicon on insulator (SOI)
[64] and silicon on SiC [65]. Solid state enjoys the benefit of a more matured fabrication process and demonstrate high reliability and have low cost per unit as compared to MEMS switch. As solid state switches don’t have any moveable part, they can operate at much faster speed. However, performance of solid state switches are often limited by high insertion loss, low frequency of operation and higher nonlinearity than MEMS based switches.

In recent times, researchers have started exploring alternate materials such as phase change material [66], [67] and transition metal oxides [6], [68]–[70] to implement a solid state RF switch. By utilizing these new material systems, which operate on fundamentally different physical mechanisms, researchers have demonstrated RF switches that outperformed conventional solid state switches. These novel switches can achieve good isolation and high frequency of operation typical of MEMs based switches while simultaneously achieving the high speed operation and form factor typical of solid state switches. Table 3-1 compares the MEMS and solid state switch performance parameters to the VO$_2$ based RF switch.

Table 3-1. Operating parameter comparison between MEMS, VO$_2$, and solid state based RF switches.

<table>
<thead>
<tr>
<th>Parameters</th>
<th>MEMS</th>
<th>VO$_2$</th>
<th>Solid State</th>
</tr>
</thead>
<tbody>
<tr>
<td>Frequency</td>
<td>High</td>
<td>High</td>
<td>Low</td>
</tr>
<tr>
<td>Insertion Loss</td>
<td>Low</td>
<td>Low</td>
<td>High</td>
</tr>
<tr>
<td>Return Loss</td>
<td>Good</td>
<td>Good</td>
<td>Good</td>
</tr>
<tr>
<td>Reliability</td>
<td>Poor</td>
<td>Good</td>
<td>Good</td>
</tr>
<tr>
<td>Switching Speed</td>
<td>in ms</td>
<td>in ns</td>
<td>in ns</td>
</tr>
<tr>
<td>Power Handling</td>
<td>High</td>
<td>Low</td>
<td>Low</td>
</tr>
</tbody>
</table>
When comparing $F_{CO}$, MEMS based switches outperform both solid state devices and VO$_2$ switches, but their switching speed remains low (2-200μs) due to the fundamental limitation of a mechanical switching mechanism. For a simplistic model of a metal contacting RF MEMS switch, $F_{CO}$ can be calculated as [71]:

$$F_{CO} = \frac{Ga_e}{2\pi\varepsilon_0\rho l}$$

Eq. 3-6

$\varepsilon_0$ is the permittivity of the free air, $\rho$ is the resistivity of the movable electrode, $l$ is the length of the movable electrode, $G$ is the air gap between the actuator and the fixed contact, and $a_e$ is the effective area factor. Alternatively, solid state devices are limited to $F_{CO}$ at least 2-3 orders lower than MEMS due to high $R_{on}$ and high $C_{off}$. Optimization of solid state device geometry to lower $R_{on}$ results in an increase of $C_{off}$ and vice versa. This establishes an inherent, fundamental limit to the frequency of operation of conventional solid state devices. The fundamental $F_{CO}$ limit for a volume of semiconductor is defined by [71]

$$F_{CO} = \frac{1}{2\pi\varepsilon_0\varepsilon_r\rho}$$

Eq. 3-7

where $\varepsilon_r$ is the semiconductor dielectric constant and $\rho$ is semiconductor resistivity. Solid state switch $F_{CO}$ is tied to only fundamental semiconductor properties, and does not include any geometric degree of freedom that can improve the $F_{CO}$. Furthermore, a more practical design using solid state devices, such as MOSFET or PIN diodes that also have additional elements for instance parasitic capacitance, depletion capacitance, and fringe capacitance, increase the OFF-state leakage and consequently degrade the RF switch $F_{CO}$. However, due to lack of any p-n junction or oxide capacitance, VO$_2$ based RF switch do not suffer from parasitic capacitance contributions and can truly achieve the fundamental $F_{CO}$. Figure 3-4 shows the measured $F_{CO}$ data points from literature plotted against the device $R_{on}$ and $C_{off}$ and highlights the design space for different technologies.
Figure 3-4. Schematic representation of various RF switch technologies plotted as a function of $C_{off}$ vs. $R_{on}$. The z-axis represents the cut-off frequency, $F_{CO}$. PCM and TMO material systems can bridge the gap between MEMS and solid state switches.

III. Film Growth and Device Fabrication

To date, demonstrations of VO$_2$ based RF switches have been limited to film grown by pulse laser deposited (PLD) [6], [68] and sputtering,[69], [70]. These deposition technique lack precise control over film stoichiometry and produce films with varying degree of crystallinity and stain, leading to a degradation in the abruptness of the IMT. Furthermore, the ultimate $R_{off}/R_{on}$ ratio is limited by the presence of metallic / insulating grains due to the poor growth morphology and imperfect control over the film. In this work, I demonstrate for the first time, a VO$_2$ RF switch on an epitaxial VO$_2$ film grown by MOMBE [11].

MOMBE growth of VO$_2$ films involves co-deposition of vanadium metal and vanadium oxytriisopropoxide (VTIP) in high vacuum. VO$_2$ stoichiometry was optimized by precise engineering of vanadium valence state through local oxygen activity tuning. Under optimized
conditions, wafer-scale epitaxial VO$_2$ was grown on sapphire substrate. Figure 3-5 (a) shows the high resolution transmission electron microscopy (TEM) micrograph of the VO$_2$ film grown on sapphire. TEM highlights the ordered growth of VO$_2$ film and lack of transition layer between sapphire and VO$_2$. EELS scan along the growth direction that shows equal ratios of vanadium peaks beyond the sapphire-VO$_2$ interface, further confirms the lack of any transition layer (Figure 3-5 (b)).

![VO$_2$ TEM micrograph](image)

Figure 3-5. (a) High resolution TEM cross-section of the single crystal epitaxially grown VO$_2$-on-sapphire (VOS). (b) EELS scan along the growth direction showing sharp interface between VO$_2$ and Al$_2$O$_3$ (denoted by equal ratio Vanadium peaks beginning 2nm in).

Figure 3-6(a) shows the measured resistivity versus temperature curve by standard van der pauw measurement and Figure 3-6(b) shows the contour map of the VO$_2$ resistivity ratios in the monoclinic and rutile phase. The VO$_2$ film shows a resistivity ratios ($\rho_m/\rho_r$) of $10^4$ and an IMT at 341K. This resistivity ratio is among the highest value achieved for thin film VO$_2$ and further emphasizes the excellent film morphology using MOMBE.
Figure 3-6. (a) Resistivity versus temperature curve for the 35nm thick VO$_2$ measured by van der pauw measurement. Material exhibits an IMT at 341K with $\rho_m / \rho_r$ of approximately $10^4$. (b) Contour map with wafer scale resistivity ratios ($\rho_m(298\text{K}) / \rho_r(353\text{K})$).

Figure 3-7. (a) False color SEM micrograph of the two terminal VO$_2$ GSG RF test structure. (b) Zoomed in SEM micrograph, showing the 24 parallel structures with width of 1$\mu$m and 100nm length. (c) Process flow for the device fabrication.
To facilitate DC and RF testing 2-terminal ground signal ground (GSG) device structures were fabricated on the VO$_2$. Figure 3-7 (a) shows the false colored SEM micrograph of the fabricate GSG structure. The pad structure were lithographically defined and Pd(20nm)/Au(60nm) contacts were deposited using e-beam evaporation. To resolve dimension of 100nm and less, a parallel device configuration was incorporated. The active device consists of 24 parallel devices with 1µm width and 100nm length. Figure 3-7 (b) shows the zoomed in view of the active device area.

IV. Electrically Activated VO$_2$ RF Switch

To test the DC switching characteristics of the 2-terminal device Keithley 4200 semiconductor characterization system was used. Figure 3-8 shows the current-voltage (I-V) characteristics of the device. The graph shows an abrupt transition from resistive state (M1) to metallic state (R) with the application of the bias. The measurement current was limited to 25mA to avoid device degradation. VO$_2$ device show an IMT at 1.1V and hysteresis of 0.95V. The device was measured at 323K.

Figure 3-8. DC current versus voltage characteristic of the 2-terminal device at 323K. The device shows an abrupt IMT with the applied voltage bias.
Figure 3-9. (a) Measurement schematic of the 2-terminal on wafer RF switch. (b) Schematic representation of the VO$_2$ RF switch operation. In OFF state (I$_{DC}$=0) VO$_2$ is in resistive monoclinic phase (M1) and the switch can be represented by a parallel RC combination; whereas under the DC bias (ON state, I$_{DC}$=I$_{ON}$) VO$_2$ switches to conductive rutile phase (R) and the switch can be represented by series RL combination.

Figure 3-9(a) shows the on-wafer measurement setup for 2-terminal VO$_2$ switch RF testing. On wafer device connections was made using GSG probes. To enable simultaneous DC and RF biasing a PSPL5542-219 bias tee was used. RF signal was applied using an Agilents N9310A signal generator and measured on Agilents N9320B spectrum analyzer. Figure 3-9(b) illustrates the operation fundamental of VO$_2$ RF switch. With no DC bias (i.e. I$_{DC}$ = 0mA), VO$_2$ is in its resistive M1 phase and acts as an attenuator between port 1 and 2. VO$_2$ in the OFF-state can be represented by a RC ($R_{off}$, $C_{off}$) parallel combination. For a good isolation between the ports in the OFF-state it
is required to have a very high $R_{\text{off}}$ and a low $C_{\text{off}}$. As the frequency of operation approaches GHz regime, the contribution from the $\omega C_{\text{off}}$ term becomes a significantly dominating component to the RF leakage path. When a DC bias is applied (i.e. $I_{\text{DC}} = I_{\text{ON}}$), VO$_2$ undergoes an IMT transition, converting into the R phase. In this phase, VO$_2$ offers a very low resistance to the RF signal leading to a minimal insertion loss during the ON-state. The switch can be represented as a series RL ($R_{\text{on}}, L_{\text{on}}$) combination. To design a good RF switch the VO$_2$ film needs to have a high resistivity ratio ($\rho_{\text{md}}/\rho_{\text{r}}$) and very low film capacitance in the monoclinic phase.

**RF Switching Characteristics**

Agilent’s vector network analyzer E8364C was used to measure the frequency response of the RF switch from 10MHz to 50GHz under DC bias. Each of the measured S-parameter response was de-embedded using on-wafer open and short structure. Figure 3-10 (a) shows the magnitude response of the de-embedded $S_{21}$ transmission. The switch shows flat response till 10GHz with zero DC bias (OFF-state). As the DC current bias is increased above $I_{\text{crit}}$, a metallic filament is formed within the VO$_2$ device. This filament forms the RF path between the two ports. With an increase in the $I_{\text{DC}}$ above $I_{\text{crit}}$, the metallic filament inside the VO$_2$ device grows in width and eventually covers the whole width of the device. At $I_{\text{DC}}$ of 25mA (ON-state) the VO$_2$ switch has a near flat $S_{21}$ response till 50 GHz. Figure 3-10 (b) shows the attenuation at 1GHz as a function of $I_{\text{DC}}$. The switch shows an attenuation of 35dB in OFF-state ($I_{\text{DC}} = 0$mA) and 0.55dB in ON-state ($I_{\text{DC}} = 25$mA). The sudden jump in attenuation at $I_{\text{crit}}$ highlights the formation of the metallic filament.
Figure 3.10. (a) $S_{21}$ transmission response vs. frequency at 323K with DC bias stepped from 0 to 25mA. (b) Switch attenuation at 1GHz of operation as a function of applied DC current bias.

To further characterize the intrinsic properties of the switch the measured S-parameters were converted into Z and Y format. In the OFF state the $R_{off}$ and $C_{off}$ can be evaluated from the measured Y-parameter from the following equations.

$$ R_{off} = \frac{-2}{\Re(Y_{12} + Y_{21})} \quad \text{Eq. 3-8} $$

$$ C_{off} = \frac{-\Im(Y_{12} + Y_{21})}{2\omega} \quad \text{Eq. 3-9} $$

Here, $Y_{12}$ and $Y_{21}$ are the corresponding elements from the 2-port admittance matrix and $\omega$ is the angular frequency. Similarly in the ON-state the $R_{on}$ and $L_{on}$ can be evaluated from the measured Z-parameter from the following equations.

$$ R_{on} = 2 \Re \left( \frac{Z_{11}Z_{22} + Z_{12}Z_{21}}{Z_{12} + Z_{21}} \right) \quad \text{Eq. 3-10} $$

$$ L_{on} = \frac{2}{\omega} \Im \left( \frac{Z_{11}Z_{22} + Z_{12}Z_{21}}{Z_{12} + Z_{21}} \right) \quad \text{Eq. 3-11} $$

Here, $Z_{11}, Z_{12}, Z_{21}$ and $Z_{22}$ are the corresponding elements from the 2-port impedance matrix.
Figure 3-11 (a) shows the evaluated switch RF conductance ($R_{on}$ and $R_{off}$) compared with DC conductance as a function of current bias. The switch conductance follows the similar trend as the switch attenuation response. Figure 3-11 (b) shows the extracted $C_{off}$ and $L_{on}$ as a function of current bias. Unlike a thermally induced IMT in VO$_2$ where the VO$_2$ capacitance undergoes a divergence at $T_{IMT}$, in electrically induced IMT VO$_2$ shows an abrupt transition from capacitance to inductive domain. Additionally, as the operating temperature is away from the $T_{IMT}$, $C_{off}$ is relatively small and switch doesn’t suffer any penalty from the divergence of the dielectric permittivity. The switch demonstrates $C_{off}$ of 41.6 fF/mm (1fF) and $R_{on}$ of 0.146 Ω-mm (6 Ω).

![Figure 3-11](image_url)

Figure 3-11: (a) Measured DC device conductance compared with the extracted RF conductance as a function of applied DC current bias at 1GHz. (b) Extracted device capacitance and inductance as a function of applied DC current bias at 1GHz.

**Non-Linearity Performance**

To study the non-linearity performance of the switch, a two tone measurement and gain compression study was performed on the VO$_2$ switch. Figure 3-12 (a) and (b) shows the output
power (Pout) response of the two tone measurement in the ON-state (I=25mA) and OFF-state (I=0mA) respectively. Two RF signal, at 2GHz ($f_1$) and 2.1GHz ($f_2$) were combined using an external combiner and fed to the input of RF switch. Absence of any third order products at 1.9GHz ($2f_1-f_2$) and 2.2GHz ($2f_2-f_1$) in the output response highlights the highly linear response of the VO$_2$ RF switch in the ON-state. The input RF power was limited to 6.5dBm due to the dynamic range limitation of the measurement setup. The switch demonstrates an output third order intercept (OIP$_3$) > 44dBm (limited by dynamic range of set up). In the OFF-state, the switch demonstrates an OIP$_3$ of -11dBm with the corresponding input third order intercept (IIP$_3$) of 22.65dBm. By moving the OFF-state temperature further away from the IMT, the OIP$_3$ can be further improved by driving the VO$_2$ into more uniform insulating phase.

![Figure 3-12](image)

Figure 3-12. Measured output response for (a) on-state (I=25mA) and (b) off-state (I=0mA) of a two tone measurement ($P_{in} = 6.5$dBm, $f_1 = 2$GHz and $\Delta f = 100$MHz). Input power was limited to 6.5dBm due to the dynamic range limitation of the instrumentation.

Additionally, the VO$_2$ switch also shows a highly linear response to the input power. Figure 3-13 (a-b) shows the measured output power as the input power is swept from -27dBm to 15dBm. The switch shows a constant insertion loss response for the entire input power range. The VO$_2$
switch has an ON-state 1dB compression point better than 15dBm (measurement limited by tool capability).

Figure 3-13. Extrinsic output power response vs. input power in the (a) ON-state and (b) OFF-state of the VO\textsubscript{2} switch.

**Turn-on Characteristics and Endurance**

A 250ns pulse with 2V amplitude was used to activate the VO\textsubscript{2} switch. A 50 MHz RF signal was combined with the trigger pulse and fed to the input of RF switch. The output response shows a turn on time of less than 25ns (Figure 3-14 (a)). Figure 3-14 (b) demonstrates the endurance of the VO\textsubscript{2} switches, where only minimal degradation occurred when the device was cycled for 6.8x10\textsuperscript{8} times and a breakdown was never observed. Cycling was performed with 100 kHz pulse with 20% duty cycle.
Figure 3-14. (a) Timing diagram of a VO$_2$ pulse switch with a 250ns activating pulse and 50MHz RF signal highlighting the <25ns turn on timing of the VO$_2$ RF switch. (b) Measured normalized $R_{ON}/R_{OFF}$ ratio for a VO$_2$ switch under constant cycling for $6.8\times10^8$ cycle.

**Self-biasing Characteristics**

Researchers have observed an RF power induced IMT in VO$_2$.[7] This self-biasing characteristic was examined, by sweeping RF power at the input port, while maintaining a zero DC bias condition. We found that as the RF power increases and crosses a critical power, the VO$_2$ undergoes an IMT, essentially turning on the RF switch under the influence of only applied RF power. The RF turn-on also shows a hysteretic response similar to DC turn-on characteristics.

Figure 3-15(a) shows the measured self-biasing characteristics with a measured turn-on at RF power of 13dBm. This critical power sets an upper limit for the maximum RF power allowed through the RF switch. However, by optimizing the thickness, the length and the width of VO$_2$ RF switch, the maximum allowed power through the RF switch can be tuned to meet the requirements
of the desired application. The trade-off between high power capabilities, turn-on time, and insertion loss are the scope of future investigation.

Figure 3-15(b) shows the effect of RF power on the performance of the switch under an applied DC bias. The figure shows a reduction in insertion loss with increase in RF power, after the formation of the initial filament (\( I_{DC} > I_{crit} \)).

![Figure 3-15](image)

Figure 3-15. (a) Output power vs. input power response of the switch under 0 DC bias condition showing the self-biasing characteristics of the VO\(_2\) RF switch. (b) RF switch insertion loss as a function of DC current with varying input RF power.

VI Switch Characteristics during Thermal IMT

The measurement of on-wafer switching properties as a function of thermal stimulus was also studied and can be visualized in Figure 3-16(a), where a thermal heating chuck was used to control the on-wafer temperature. S-parameters were measured as the temperature was swept from 298K to 360K in order to capture the change in complex impedance across the thermally induced IMT. Figure 3-16(b) shows the measured \( S_{21} \) at 1 GHz as a function of sample temperature. At IMT
an abrupt 30dB drop in $S_{21}$ corresponding to $10^3$ change in resistivity and divergence in the measured capacitance is observed (Figure 3-17(a-b)). Intrinsic $F_{CO}$ limit of 44THz, for the switch, was evaluated under a thermal activation (where $T_{OFF}$ was set to 298K and $T_{ON}$ to 358K).

![Diagram](image_url)

Figure 3-16. (a) Schematic representation of an on-wafer characterization of VO$_2$ switching properties under a thermal stimulus. The sample temperature was swept from 298K to 360K and on-wafer s-parameters were collected by a vector network analyzer. (b) Measured $S_{21}$ at 1 GHz as a function of the swept sample temperature. As the temperature cross the VO$_2$ IMT we observe an abrupt drop of 30dB. Using the measured s-parameter the VO$_2$ impedance was extracted as a function of temperature.
Figure 3-17. (a) Measured VO$_2$ resistivity from the impedance extraction as a function of temperature. (b) Measured VO$_2$ $L$ and $C$ as a function of temperature. We observe the characteristic divergence in capacitance at the IMT.

VII. Benchmarking

Figure 3-18 shows the comparison $S_{12,off}/S_{12,on}$ ration for a various switching elements in series configuration. This graph highlights the improvement of about 10dB in the switching ratios at 20GHz as compared to the state of the art GaN SCLFET [63]. Figure 3-19 benchmarks the cut-off frequency of the current solid state technology, PCM switches and VO$_2$ RF switch from literature as a function of the ON-state resistance of the switch. VO$_2$ switch outperforms conventional FETs, HEMT and GeTe (PCM) RF switch with cut-off frequency $F_{CO}$ of 26.5 THz (at 0.14$\Omega$-mm $R_{on}$). GeTe switches [66] with $F_{CO}$ of 12.5 THz have been demonstrated but are limited by their long turn on and turn off time due to incorporation of inline resistive heater. The isolation of the GeTe switches also suffer from RF leakage through the resistive heater in the OFF-state. On the contrary VO$_2$ switches suffer from the disadvantage of continuous DC power...
requirement during the ON-state. Intrinsic $F_{CO}$ limit of 44THz, for the switch, was evaluated under a thermal activation (where $T_{OFF}$ was set to 298K and $T_{ON}$ to 358K).

![Figure 3-18](image1.png)

Figure 3-18. Comparison of $S_{21,off}/S_{21,on}$ ratios for VO$_2$ RF switch in this work with other VO$_2$ [69], GaN [63], GeTe [66] and InP PHEMT [72] switch from literature.

![Figure 3-19](image2.png)

Figure 3-19. Figure of merit benchmark of switch cut off frequency for various FET technology[61], [62], [72], [73], PCM[66], [67] and VO$_2$ RF switch[74].
Table 3-2. Comparison summary of various solid state RF switch from literature.

<table>
<thead>
<tr>
<th>Material</th>
<th>IL* [dB]</th>
<th>RL* [dB]</th>
<th>Iso* [dB]</th>
<th>R_{ON} [Ω.mm]</th>
<th>C_{OFF} [pF/mm]</th>
<th>F_{CO} [THz]</th>
<th>P_{1dB,in} [dBm]</th>
<th>OIP3 [dBm]</th>
<th>Reference</th>
</tr>
</thead>
<tbody>
<tr>
<td>VO_{2} (Electrically)</td>
<td>0.5</td>
<td>25</td>
<td>35</td>
<td>0.146</td>
<td>0.041</td>
<td>26.5</td>
<td>&gt;12</td>
<td>&gt;44</td>
<td>This Work</td>
</tr>
<tr>
<td>VO_{2} (Thermally)</td>
<td>0.2</td>
<td>31</td>
<td>37</td>
<td>0.072</td>
<td>0.05</td>
<td>44.2</td>
<td>-</td>
<td>-</td>
<td>This Work</td>
</tr>
<tr>
<td>GeTe</td>
<td>0.18</td>
<td>-</td>
<td>15</td>
<td>0.027</td>
<td>0.47</td>
<td>12.5</td>
<td>-</td>
<td>-</td>
<td>[66]</td>
</tr>
<tr>
<td>GaN SLCFET</td>
<td>0.7</td>
<td>18</td>
<td>25</td>
<td>0.41</td>
<td>0.19</td>
<td>2.1</td>
<td>36</td>
<td>62</td>
<td>[75]</td>
</tr>
<tr>
<td>InP HEMT</td>
<td>1.7</td>
<td>19</td>
<td>15.5</td>
<td>0.48</td>
<td>0.394</td>
<td>0.84</td>
<td>-</td>
<td>-</td>
<td>[72]</td>
</tr>
<tr>
<td>GaAs PHEMT</td>
<td>1.6</td>
<td>-</td>
<td>42</td>
<td>1.5</td>
<td>0.24</td>
<td>0.48</td>
<td>-</td>
<td>-</td>
<td>[76]</td>
</tr>
<tr>
<td>SOI</td>
<td>1.4*</td>
<td>-</td>
<td>-</td>
<td>0.8</td>
<td>0.312</td>
<td>0.63</td>
<td>-</td>
<td>-</td>
<td>[73]</td>
</tr>
<tr>
<td>Si-on-sapphire</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>1.6</td>
<td>0.280</td>
<td>0.35</td>
<td>-</td>
<td>-</td>
<td>[65]</td>
</tr>
</tbody>
</table>

* measured at 20GHz, # measured at 10GHz

VIII. Conclusion

In conclusion, we demonstrate, for the first time a VO_{2} RF switch on an epitaxially grown thin film VO_{2} on sapphire. The switch outperforms the conventional solid state RF switch with a figure of merit F_{CO} of 26.5 THz. Due to the high quality of the VO_{2} thin film, with a high resistivity ratios (\(\rho_{m}/\rho_{r}\)) and low film capacitance, a switch with very low insertion loss (0.55dB) and high isolation (35dB) was developed. Due to near instantaneous nature of VO_{2} electrical switching, the RF switch can be turned on in less than 25ns. RF switch also exhibits a highly linear response with OIP3 better than 44dBm and gain compression better than 15dBm. Use of VO_{2} in this application can allow us to bridge the design space between MEMS and solid state, taking advantage of the unique switching physics to achieve high F_{CO} while maintaining low turn on time and low insertion loss.
Chapter 4

Graphene RF Mixer

I. Introduction

Mixers are the integral part of radio frequency (RF) systems. Mixers in a receiver system perform two main tasks. First, mixer stages are used to down-converting the incoming signal from an antenna to the baseband frequency for demodulation. And second to up-convert the outgoing signal, to an antenna, to its transmission frequency. Diodes, RF MOSFETs, and HEMTs are the obvious choice for the design of a frequency mixer circuit. However, the operation of these devices in the nonlinear regime not only gives the desired frequency multiplication but also results in high-order harmonic distortion to the system. These unwanted harmonics and their subsequent mixing are of great concern as the order of cascade stages in receiver is increased. For a single-ended mixer topology, a filtering and matching circuit is added to reject the unwanted harmonic components. This limits the mixer to a narrow-band frequency operation. Traditionally, balanced mixer designs are used to reject odd harmonics by mixing out-of-phase signals from two or more individual single-ended mixers. But these balanced mixers are limited in their performance due to mismatch, interconnect parasitic and increased size. In this work we concentrate on a graphene based, single device mixer solution, which gives a wideband performance with harmonic suppression.

Graphene is a zero band gap semiconductor. Figure 4-1(a) shows the Dirac cone representation of graphene band-gap. The intersection point of the valence and the conduction band is called the Dirac point also referred as the minimum conductivity point. In recent years, graphene has gained interest for use in RF electronic devices due to its high carrier mobility, symmetric electron and hole conduction, and ambipolar behavior. These unique properties have allowed for
new RF applications, including a single transistor triple-mode amplifier [39] and a single transistor ambipolar mixer [77]. Additionally, more conventional mixer designs have also been implemented showing resistive [78] and drain mixing [79].

Graphene’s ambipolar nature allows for suppression of odd order harmonics at the Dirac point as well as peak conversion gain. This makes graphene transistor prime candidate for single device mixer design. Figure 4-1(b) shows how a graphene transistor, biased at the Dirac point showing a frequency doubler action. Initial demonstrations of graphene mixers have been successful but the performance has been limited by high contact resistance, low mobility, and low transconductance. By analyzing the DC/RF output characteristics of the graphene transistor, we identify the key areas to improve mixer performance, leading to record high conversion gain.

![Dirac cone representation of zero band gap graphene system. The intersection of conduction and valence band is called the Dirac point.](a)

![Frequency doubling for an ideal graphene transistor biased at Dirac point.](b)

Figure 4-1. (a) Dirac cone representation of zero band gap graphene system. The intersection of conduction and valence band is called the Dirac point. (b) Frequency doubling for an ideal graphene transistor biased at Dirac point.
II. Transistor Fabrication

Two-finger graphene RF devices are synthesized from quasi-free-standing epitaxial graphene (QFEG) on (0001) oriented, semi-insulating 6H-SiC substrates silicon carbide substrates. Here the use of a semi-insulating substrate is beneficial in limiting the extrinsic parasitics of the RF devices. QFEG is prepared through a combination of sublimation and hydrogen intercalation, previously discussed elsewhere [80]. Sublimation of Si takes place at 1625°C in 1 Torr Ar, while hydrogen intercalation follows at 1050°C in 600 Torr Ar/H₂, producing primarily bilayer graphene across the hydrogen passivated SiC surface with sufficient uniformity to allow for wafer-scale fabrication. Hydrogen intercalation is a key step in maintaining a high carrier mobility for the epitaxial graphene by converting the carbon buffer layer to an additional layer of graphene and enhancing mobilities more than 3× from conventional epitaxial graphene to 3000 cm²/V sec at a hole density of 1x10¹³ cm².

Figure 4-2. (a) False color SEM micrograph of two-finger graphene RF transistor with T-gates. (b) Schematic cross-section of graphene transistor with Lg=750nm and W=20μm. 10nm HfO2 gate oxide was grown by oxide seeded ALD.

Graphene transistors were patterned using standard photolithographic techniques. After graphene synthesis, the graphene channel is isolated using an argon/oxygen plasma etch. Source/drain contacts (Ti/Au 10/10nm) are patterned using an oxygen plasma pre-treatment to remove resist residue and improve contact resistance, as detailed elsewhere [81]. This optimized
source/drain metallization leads to contact resistances as low as 100 ohm-μm, allowing channel length scaling to deep sub-micron channel lengths before contact resistances begin to dominate the transfer characteristics of the RF FETs. For the RF graphene FETs, gate dielectrics are deposited using an e-beam physical vapor deposition (EBPVD) seeded atomic layer deposition (ALD) process (2.5nm HfO$_2$ seed / 10 nm ALD HfO$_2$), described elsewhere [82]. For the gate dielectric, use of the two-step EBPVD seeded ALD process allows for scaling the EOT to ~2.5 nm while maintaining uniform coverage and without significantly degrading transport properties [82]. Figure 4-2(b) is a schematic representation of a two-finger, RF graphene transistor, while Figure 4-2(b) shows an SEM of the finished device with T-gates to minimize gate resistance. RF transistors with gate lengths of 75, 250, and 750 nm and total gate width 20 μm were prepared and characterized. The 750 nm long devices were chosen for the mixer analysis and comparison due to their excellent symmetry compared to the smaller channel lengths. Further scaling of $t_{ox}$ or use of a graphene nano-ribbon geometry to enhance gate coupling through fringing fields is expected to allow for further scaling of $L_g$ to < 500 nm. In addition to the graphene transistors, Van der Pauw (VdP) Hall cross structures (5x5 μm) are prepared, confirming mobilities as high as 3000 cm$^2$/V sec at carrier densities of 1x10$^{13}$ cm$^2$ after dielectric integration. Figure 4-3 summarizes the device layer and process conditions for each step.
III. DC Characterization

For a \([10\mu m \times 0.75\mu m] \times 2\) device \((W \times L_g) \times \# \text{ of gate fingers}\), family of DC transfer and output characteristics were collected using a Keithley-4200 semiconductor parameter analyzer. Figure 4-4(a) shows the measured drain current \((I_d)\) as function of gate bias \((V_g)\) for a drain bias \((V_d)\) ranging from \(-50mV\) to \(-1V\). The device exhibits ambipolar transfer characteristics with near symmetric electron \((e^-)\) and hole \((h^+)\) branch. The on-off ratio for the measured device is greater than 2. Figure 4-4(b) shows the output characteristics for the device with excellent drive current of 1.1 mA/\(\mu m\) at \(V_d = -1V\).

Figure 4-5 (a-b) show the color map of transconductance \((g_m)\) and output-conductance \((g_d)\) as a function of \(V_g\) and \(V_d\). Peak transconductance is found to be 330 \(\mu S/\mu m\), which is attributed to
the relatively small EOT for these devices (~2.5 nm) as well as the high mobility of the hydrogen passivated epitaxial graphene.

Figure 4-4. (a) Transfer curves (Ids-Vgs) from Vds=50mV to 1V exhibiting VDirac near Vgs=0V and near symmetric electron and hole branches. (b) Family of curves (Ids-Vds) from Vgs=0 to -3V showing weak saturation behavior.

Figure 4-5. (a) Color maps of absolute transconductance (g_m) and (b) output conductance (g_d) as a function of drain bias (Vds) and gate bias (Vgs) indicating a peak transconductance of 330 μS/μm.
IV. RF Characterization

S-parameter characteristics of the device were measured using Anritsu 37397D VNA from 40MHz to 40GHz. Device shows excellent RF performance, exhibiting peak intrinsic current gain cutoff frequency \( f_T \) of 110 GHz at a gate length of 75 nm with \( V_{ds} = -1V \) (Figure 4-6(a)), where intrinsic \( f_T \) was extracted from measured S-parameters using a standard short-open de-embed process to remove the effect of probe and pad parasitics. Intrinsic \( f_T \) is found proportional to the inverse of \( L_g \), although extrinsic performance is limited by parasitics at small gate lengths. Still, we report an excellent peak extrinsic \( f_T \cdot L_g \approx 5 \text{ GHz} \cdot \mu \text{m} \) (Figure 4-6(b)). Effective injection velocity between 1.1 and 2.5x10^7 cm/sec is extracted from the small signal parameters as a function of \( L_g \).

![Figure 4-6](image-url)

Figure 4-6. (a) Short circuit current gain and unilateral power gain of graphene transistor at \( V_{ds} = -1V \) and \( V_{gs} = 1.5V \). Intrinsic values are extracted using a short-open de-embed process in order to remove probe and pad parasitics. (b) Intrinsic and extrinsic \( f_T \) as a function of gate length, showing increasing effect of parasitics on extrinsic device performance as well as the expected dependency of \( f_T \) on \( L_g \).

The measured extrinsic s-parameter was also modeled using Agilent’s Advance Device System (ADS). The small signal modeling helps us to understand the effect of extrinsic parasitic and intrinsic device capacitance. Figure 4-7 shows the small signal model with intrinsic and
extrinsic device elements. The measured S-parameters and simulated curves are shown in Figure 4-8 with simulation parameters given in Table 4-1.

Figure 4-7. Small signal model for graphene FET including extrinsic parasitics.

Figure 4-8. Measured and modeled S-parameter output (frequency 40MHz to 40GHz).
Table 4-1. Small signal simulation parameters.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Modeled</th>
<th>Parameter</th>
<th>Modeled</th>
</tr>
</thead>
<tbody>
<tr>
<td>$g_m$</td>
<td>-1.5 mS</td>
<td>$L_s$</td>
<td>113pH</td>
</tr>
<tr>
<td>$r_0$</td>
<td>79 Ω</td>
<td>$R_s$</td>
<td>10 Ω</td>
</tr>
<tr>
<td>$C_{gs}$</td>
<td>27 fF</td>
<td>$L_d$</td>
<td>98 pH</td>
</tr>
<tr>
<td>$C_{gd}$</td>
<td>31 fF</td>
<td>$R_d$</td>
<td>2 Ω</td>
</tr>
<tr>
<td>$C_{ds}$</td>
<td>3 fF</td>
<td>$C_{gs_ext}$</td>
<td>30 fF</td>
</tr>
<tr>
<td>$L_g$</td>
<td>48pH</td>
<td>$C_{ds_ext}$</td>
<td>20 fF</td>
</tr>
<tr>
<td>$R_g$</td>
<td>25 Ω</td>
<td>$C_{gd_ext}$</td>
<td>5 fF</td>
</tr>
</tbody>
</table>

V. RF Mixer

RF Mixers are a three port non-linear electrical circuit which combines two input signals yielding sum and difference of the input signal or the harmonic combination of its input signal. RF mixers play an important role in modern RF communication systems. If the frequency of the output signal of a mixer is lower than the input signal, then it is called down-conversion and if it is higher than the input signals, then it is referred as up-conversion. The Figure 4-9 shows the schematic representation of a mixer. The two input signals to a mixer are usually local oscillator signal and the RF signal (incoming signal from receiver, or outgoing signal from transmitter). The output signal of a mixer is referred as Intermediate Frequency (IF).

Mixer types can be divided into following three broad divisions [83], single device mixer, single balanced mixer and double balanced mixer. A single device mixer is essentially a mixer composed of only one non-linear element (diodes, FET, HEMTS etc). Such mixers have the disadvantage of high distortion and very low port to port isolation. To improve the performance of it is essential to incorporate input/output matching networks and filters in the overall design. Due to the presence of filters and matching network, the performance of single device mixers is limited to a very small bandwidth and low conversion gain.
Balanced mixers (single/double) are made of two or more non-linear elements and have significant advantages over single device mixer. One of the advantages is an inherent LO to RF isolation. Other advantages include high conversion gain. They also have a better power handling capability compared to single device mixers as the power is divided between multiple devices. The performance of a balanced mixer is limited by the parasitic contribution of multiple interconnects between several devices (FETs). This puts a limit on the frequency of operation of the mixers. Another limitation of FET based balanced mixer is the need of multiple hybrids. Addition of these hybrids increases the overall mixer dimensions significantly, in some cases making them impractical for MMIC design.

In this work graphene FET based single device mixer topologies are explored. I have studied the performance of the graphene mixer in ambipolar and resistive mixer configurations. The measured conversion gain is also benchmarked with published results from the literature. Following sections describe and detail the experimental results.
Ambipolar Graphene RF Mixer

For gate mixing/transconductance mixing, the LO and RF input signals are fed to the gate of the FET and the output of the mixing is sensed at the drain terminal. The special case of ambipolar mixing is achieved by biasing the graphene transistor at the Dirac point. Figure 4-10 shows the measurement setup for ambipolar mixing. In current measurement setup, LO and RF input signal are fed through an external combiner to the gate of the transistor. Bias tees are used to setup the DC bias conditions. On-wafer device are connected using GSG probes (Ground-Signal-Ground).

\[
\begin{align*}
\frac{\partial I_d}{\partial V_g} v_g + \frac{\partial I_d}{\partial V_d} v_d + \frac{1}{2} \frac{\partial^2 I_d}{\partial V_g^2} v_g^2 + \frac{1}{2} \frac{\partial^2 I_d}{\partial V_d^2} v_d^2 + \frac{\partial^2 I_d}{\partial V_g \partial V_d} v_g v_d + \frac{1}{6} \frac{\partial^3 I_d}{\partial V_g^3} v_g^3 + \frac{1}{6} \frac{\partial^3 I_d}{\partial V_d^3} v_d^3 + \frac{1}{2} \frac{\partial^3 I_d}{\partial V_g^2 \partial V_d} v_g^2 v_d + \frac{1}{2} \frac{\partial^3 I_d}{\partial V_g \partial V_d^2} v_g v_d^2 + \ldots
\end{align*}
\]

Eq. 4-1 can be re-written in a simplified form as

Figure 4-10. Circuit schematic showing an unmatched single stage ambipolar graphene mixer.
\[ i_d(v_g, v_d) = g_m v_g + g_d v_d + \frac{1}{2} g'_m v_g^2 + \frac{1}{2} g'_d v_d^2 + g_m g_d v_g v_d + \frac{1}{6} g''_m v_g^3 + \frac{1}{6} g''_d v_d^3 + \frac{1}{2} g''_m g_d v_g v_d + \frac{1}{2} g''_m g_d v_g v_d^2 + \ldots \] \quad \text{Eq. 4-2}

For ambipolar mixing the small signal input are \( v_g = v_{LO} + v_{RF} \) and \( v_d = 0 \), simplifying Eq. 4-2 as

\[ i_d(v_{LO} + v_{RF}, 0) = g_m (v_{LO} + v_{RF}) + \frac{1}{2} g'_m (v_{LO} + v_{RF})^2 + \frac{1}{6} g''_m (v_{LO} + v_{RF})^3 + \ldots \] \quad \text{Eq. 4-3}

For a sinusoidal LO and RF of equal amplitude \((v_0)\) Eq. 4-3 can be simplified into the individual frequency components as shown in Table 4-2.

<table>
<thead>
<tr>
<th>Mixer Output Frequency</th>
<th>Order</th>
<th>Component</th>
</tr>
</thead>
<tbody>
<tr>
<td>( IF_d = f_{LO} - f_{RF} )</td>
<td>2nd</td>
<td>( \frac{1}{2} g'_m v_0^2 )</td>
</tr>
<tr>
<td>( 2f_{RF} - f_{LO} )</td>
<td>3rd</td>
<td>( \frac{1}{8} g''_m v_0^3 )</td>
</tr>
<tr>
<td>( f_{RF} )</td>
<td>1st</td>
<td>( g_m v_0 + \frac{3}{8} g''_m v_0^3 )</td>
</tr>
<tr>
<td>( f_{LO} )</td>
<td>1st</td>
<td>( g_m v_0 + \frac{3}{8} g''_m v_0^3 )</td>
</tr>
<tr>
<td>( 2f_{LO} - f_{RF} )</td>
<td>3rd</td>
<td>( \frac{1}{8} g''_m v_0^3 )</td>
</tr>
<tr>
<td>( 2f_{RF} )</td>
<td>2nd</td>
<td>( \frac{1}{4} g''_m v_0^2 )</td>
</tr>
<tr>
<td>( IF_u = f_{LO} + f_{RF} )</td>
<td>2nd</td>
<td>( \frac{1}{2} g'_m v_0^2 )</td>
</tr>
<tr>
<td>( 2f_{LO} )</td>
<td>2nd</td>
<td>( \frac{1}{4} g''_m v_0^2 )</td>
</tr>
</tbody>
</table>

Ambipolar transfer characteristics of graphene transistors, provides it a unique ability to eliminate odd harmonics in the output if operated at Dirac point. The IF signal is proportional only
to $g_m'(d^2I_d/dV_g^2)$, whereas the 1st and the 3rd order harmonics depend on $g_m$ and $g_m'' (dI_d/dV_g, d^3I_d/dV_g^3)$. Figure 4-11(a) shows the transfer characteristics of a graphene transistor biased at $V_{ds}$ of 1V for a 750nm $L_g$ transistor. Figure 4-11(b) shows the extracted 1st, 2nd and 3rd order component of the output current. One can observe that at the Dirac point $g_m$ and $g_m''$ are 0 and $g_m'$ reaches maxima. Hence device operating at the Dirac point will give maximum conversion gain and rejects odd harmonics.

Figure 4-11. (a) Transfer curve of graphene FET showing ambipolar response with high degree of symmetry between n and p branch. (b) Extracted $g_m$, $g_m'$, and $g_m''$ showing peak $g_m'$ as well as minimum $g_m$ and $g_m''$ at the Dirac point. For a graphene FET, at the Dirac point, the ambipolar conduction leads to peak conversion gain and suppression of odd order mixing products.

A plot of $g_m'$ ($P_{IF} \propto g_m'$) versus $V_g$ and $V_d$ identifies the Dirac point at $V_d$ = -1V as the optimal bias point for maximum conversion gain (Figure 4-12). The LO and RF inputs of 4.2 (10) and 4 (9.8) GHz, respectively, were combined using an external power combiner. Figure 4-13(a) shows the output spectrum at the Dirac point for LO power 0 dBm and RF power -15 dBm, displaying record conversion gain of -14 dB. Mixer performance was also evaluated as a function of gate bias showing suppression of odd order harmonics at the Dirac point as well as confirming peak conversion gain at the Dirac point (see Figure 4-13(b)).
Measured $g'_m$ ($P_{IF} \propto g'_m$) as function of $V_{gs}$ and $V_{ds}$ shows peak $g'_m$ and indicates that maximum conversion gain should occur at the Dirac point.

Figure 4-13. (a) Output spectrum for graphene ambipolar mixer, showing first, second, and third order mixing products as well as record high conversion gain of -14 dB at LO 0 dBm. (b) Measured output spectrum as a function of $V_{gs}$ shows suppression of odd order harmonics and confirms peak conversion gain at the Dirac point.
Resistive Graphene RF Mixer

Another standard FET mixer configuration is resistive/drain mixing. In this configuration RF input is fed to the gate and LO input and the IF output is configured at the drain of transistor. This configuration has an advantage of very good RF to LO port isolation but presents a drawback of LO power leaking to the output. Figure 4-14 shows the schematic for the drain mixing setup.

For drain mixing \( v_g = v_{RF} \), \( v_g = v_{LO} \) and Eq. 4-3 can be written as

\[
i_d(v_{RF}, v_{LO}) = g_m v_{RF} + g_d v_{LO} + \frac{1}{2} g_m' v_{RF}^2 + \frac{1}{2} g_d' v_{LO}^2 + g_m g_d v_{RF} v_{LO} + \frac{1}{6} g_m^2 v_{RF}^3 + \frac{1}{6} g_d^2 v_{LO}^3 + \frac{1}{2} g_m g_d v_{RF} v_{LO}^2 + \ldots \]  

Eq. 4-4

For a sinusoidal LO and RF of equal amplitude (\( v_0 \)) Eq. 4-4 can be simplified into the individual frequency components (see Table 4-3). In contrast to ambipolar gate mixing, drain mixing doesn’t have region of harmonic rejection as we can see from Figure 4-15(a). The IF signal
\( \propto g_m g_d \) follows the RF signal \( \propto g_m \) at the output and we see high LO leakage \( \propto g_d \) at the output.

A plot of \( g_m g_d \left( d^2 I_d / dV_g dV_d \right) \) versus \( V_g \) and \( V_d \) identifies \( V_d = 0 \) V as the optimal bias conditions for drain mixing (resistive mixing) due to the fact that \( P_{IF} \propto g_m g_d \) (Figure 4-15(b)). The LO and RF inputs (same as gate mixing) of 4.2 and 4 GHz, respectively, were used to characterize mixer performance. A conversion gain of -18.5 dB is observed at LO power of 0 dBm (Figure 4-16(a)), while a sweep in \( V_g \) confirms the lack of suppression of odd order harmonics (Figure 4-16(b)).

Table 4-3. Output frequency components of a drain mixing product.

<table>
<thead>
<tr>
<th>Mixer Output Frequency</th>
<th>Order</th>
<th>Component</th>
</tr>
</thead>
<tbody>
<tr>
<td>( IF_d = f_{LO} - f_{RF} )</td>
<td>2\text{nd}</td>
<td>( \frac{1}{2} g_m g_d v_0^2 )</td>
</tr>
<tr>
<td>( 2f_{RF} - f_{LO} )</td>
<td>3\text{rd}</td>
<td>( \frac{1}{8} g'_m g_d v_0^3 )</td>
</tr>
<tr>
<td>( f_{RF} )</td>
<td>1\text{st}</td>
<td>( g_m v_0 + \frac{1}{8} g'_m v_0^3 + \frac{1}{4} g_m g'_d v_0^3 )</td>
</tr>
<tr>
<td>( f_{LO} )</td>
<td>1\text{st}</td>
<td>( g_d v_0 + \frac{1}{8} g'_d v_0^3 + \frac{1}{4} g'_m g_d v_0^3 )</td>
</tr>
<tr>
<td>( 2f_{LO} - f_{RF} )</td>
<td>3\text{rd}</td>
<td>( \frac{1}{8} g_m g'_d v_0^3 )</td>
</tr>
<tr>
<td>( 2f_{RF} )</td>
<td>2\text{nd}</td>
<td>( \frac{1}{4} g'_m v_0^2 )</td>
</tr>
<tr>
<td>( IF_u = f_{LO} + f_{RF} )</td>
<td>2\text{nd}</td>
<td>( \frac{1}{2} g_m g_d v_0^2 )</td>
</tr>
<tr>
<td>( 2f_{LO} )</td>
<td>2\text{nd}</td>
<td>( \frac{1}{4} g_d v_0^2 )</td>
</tr>
</tbody>
</table>
Figure 4-15. (a) Extracted $g_m$, $g_d$, and $g_mg_d$ component of the drain current. (b) Measured $g_mg_d$ ($P_{IF} \propto g_mg_d$) as function of $V_g$ and $V_d$ indicating peak values near $V_d=0V$, thus resistive mixing with $V_d=0V$ should produce the highest conversion gain.

Figure 4-16. (a) Output spectrum for graphene mixer, showing first, second, and third order mixing products and conversion gain of -18.5dB. (b) Measured output spectrum at $V_d=0V$ as a function of $V_g$, showing no suppression of odd order output products as occurs for the ambipolar gate mixing case.
VI. Performance Benchmarking

Conversion gain was also studied as a function of LO power. Here in Figure 4-17 (a) both resistive and ambipolar mixer shows linear performance up to 0 dBm for both ambipolar and resistive drain mixing. This work represents the highest performance graphene based ambipolar mixer yet reported (20dB higher than ref. [77] at 0dBm LO power). We also show comparable resistive mixing performance, ~2dB lower than the best reported resistive mixer performance [84] for 0dBm LO power at 4 GHz. Figure 4-17 (b) shows the comparison of conversion gain versus frequency of operation for graphene based mixer compared to gilbert cell and cmos single balance mixer. The excellent performance is attributed to highly scaled EOT, high mobility, and low contact resistances (Table 4-4).

![Conversion Gain vs LO Power and Frequency](image)

Figure 4-17. Conversion gain versus (a) LO power and (b) frequency showing higher conversion gain for ambipolar gate mixer as compared to other state of the art ambipolar graphene mixer [77], resistive graphene mixer [84], [85] drain mixer [79] and CMOS mixer [86], [87].
Table 4-4. Comparison summary of various solid state RF switch from literature.

<table>
<thead>
<tr>
<th>Reference</th>
<th># of FETs</th>
<th>$L_g$ [μm]</th>
<th>$W$ [μm]</th>
<th>$t_{ox}$ (seed/oxide)</th>
<th>Peak $g_m$ [μS/μm]</th>
<th>$V_{gs}$ [V]</th>
<th>$V_{ds}$ [V]</th>
<th>$R_{con}$ [Ω·μm]</th>
</tr>
</thead>
<tbody>
<tr>
<td>This Work (Ambipolar)</td>
<td>1</td>
<td>0.75</td>
<td>20</td>
<td>2/10 (HfO$_2$)</td>
<td>330</td>
<td>0</td>
<td>-1</td>
<td>100</td>
</tr>
<tr>
<td>This Work (Resistive)</td>
<td>1</td>
<td>0.75</td>
<td>20</td>
<td>2/10 (HfO$_2$)</td>
<td>330</td>
<td>-</td>
<td>0.5</td>
<td>100</td>
</tr>
<tr>
<td>[77]</td>
<td>1</td>
<td>2.0</td>
<td>150</td>
<td>5/25 (SiO$_2$/Al$_2$O$_3$)</td>
<td>5.5</td>
<td>-</td>
<td>0.2</td>
<td>--</td>
</tr>
<tr>
<td>[79]</td>
<td>1</td>
<td>0.55</td>
<td>30</td>
<td>2/20 (Al$_2$O$_3$)</td>
<td>80</td>
<td>-3</td>
<td>2</td>
<td>600</td>
</tr>
<tr>
<td>[85]</td>
<td>1</td>
<td>0.5</td>
<td>15</td>
<td>2/25 (Al$_2$O$_3$)</td>
<td>--</td>
<td>--</td>
<td>0</td>
<td>--</td>
</tr>
<tr>
<td>[87]</td>
<td>10</td>
<td>--</td>
<td>--</td>
<td>--</td>
<td>--</td>
<td>--</td>
<td>--</td>
<td>--</td>
</tr>
<tr>
<td>[86]</td>
<td>2</td>
<td>0.13</td>
<td>80</td>
<td>--</td>
<td>--</td>
<td>--</td>
<td>--</td>
<td>--</td>
</tr>
</tbody>
</table>

VII. Conversion Gain Projection

In order to evaluate the two configurations in terms of the absolute achievable gain, we simulated the ambipolar mixer gain, using the harmonic balance simulation in Agilent's ADS simulator. A typical MIMIC realization would require input and output matching network as shown in Figure 4-18(a). The simulated conversion gain shows an improvement of >7dB compared to the unmatched configuration for the ambipolar mixer. Further scaling and improvement of operating frequency will enable a co-planar or a microstrip matching network design instead of the discrete lumped element design shown here. With continued improvements to device performance, ambipolar mixers can achieve a positive gain.

For the resistive configuration, the matching network circuit configuration is shown in Figure 4-18(a). A combination of a high pass and low pass filter match is required at the output in
order to get matching as well as to maintain a good isolation between IF and LO. The maximum gain for the resistive mixer is given by the following equation:[88].

\[
\text{Gain} = \left( \frac{\Gamma_{\text{max}} - \Gamma_{\text{min}}}{\pi} \right)^2 \quad \text{Eq. 4-5}
\]

Figure 4-18. Circuit schematic for an impedance matched (a) ambipolar and resistive graphene mixer. (b) Comparison of measured conversion gain to a simulated impedance matched ambipolar mixer and absolute conversion gain limit of the resistive mixer.

In Eq. 4-5 \( \Gamma = \left( R_{ch} - Z_0 \right) / \left( R_{ch} + Z_0 \right) \) is the reflection coefficient seen at the drain. The graphene FET in this work has an on/off ratio of \(~4:1\) (Vds:25mV) which gives a maximum conversion gain of -13.5dB (Figure 4-18(b)). Even with an improved on/off ratio of 10:1 (increase in on-current, keeping the off-current same) the maximum achievable gain is only \(~ -10\)dB. The ultimate performance of the resistive mixer with an on-off ratio of infinity is still limited to a conversion loss of 3.9 dB, whereas the ambipolar mixer has the potential to achieve positive gain. Although, these simulations show that the ambipolar configuration has a significant potential to outperform the resistive configuration, there are several key challenges that need to be overcome to achieve such a positive gain. Firstly, oxide thickness scaling is critical in maintaining sufficient
gate control, leading directly to high peak transconductance and, thusly, higher $g'_m$. Additionally, when we scale channel length in order to achieve higher peak transconductance and higher operating frequencies, we experience a shift in dirac point, a loss in symmetry, and a degradation in transconductance. Although the degradation in performance is partially due to increased dominance of contact resistance, it is in large part due to the effect of what is known as the Charge Transfer Region (CTR). As shown in other work [89], enhanced gate coupling, either through increased oxide scaling, or the use of a graphene nanoribbon geometry can lead to a reduction in the length scale of this CTR as it decays into the channel. This leads directly to enhanced gate control which in turn helps maintain symmetry between the p and n branches of the transfer curve, reduces $V_{dirac}$ shift, and also improves the on-off ratio and transconductance. Finally, interface states ($D_{it}$) needs to be controlled, as increased interface states lead directly to degraded $g_m$ and $g'_m$. This is a significant limitation in graphene due to its lack of bandgap and the lack of any high quality, scalable oxide deposition technique.

**VIII. Conclusion**

In conclusion, hydrogen intercalated graphene transistors with highly scaled EOT were used to demonstrate record high conversion gain for a single graphene transistor ambipolar mixer, achieving a small circuit footprint. Ambipolar gate mixing was shown to suppress odd order harmonics and was found to outperform resistive drain mixing. Increased performance is anticipated through further reducing $D_{it}$ and scaling EOT, indicating that the graphene based ambipolar mixer may soon become competitive with conventional Gilbert cell mixers.
Appendix A

SMM Scans on Si/SiO$_2$ Staircase Structure

To verify the process of converting the measured $\Gamma_{port}$ to $\Gamma_{tip}$, impedance mapping on a standard Si/SiO$_2$ staircase structure is performed using SMM. The test structure consists of a 500µm thick doped silicon substrate with a layer of SiO$_2$ on top. The SiO$_2$ layer is grown into a staircase pattern with step heights of 50nm, 100nm, 150nm, and 200nm respectively. Au pads of varying diameter (1, 2, 3, and 4µm) are deposited on top of the SiO$_2$ structure to complete a parallel plate capacitor structure with the two plates corresponding to the Au pads, and the doped Si substrate. Figure A-1(a) shows the cross-section schematic of the test structure and Figure A-1(b) shows the AFM scan of the test structure illustrating the alignment of the top gold pads on the staircase structure.

Figure A-1: (a) Schematic and (b) 45µm x 45µm AFM topography scan of the Si/SiO$_2$ test structure.
During the SMM scan, the change in the oxide thickness and the variation in the Au cap area will lead to shift of the resonant frequency as well as change in the Q factor of the SMM resonance peak. This variation is recorded in the abs(\(\Gamma_{\text{port}}\)) and phase(\(\Gamma_{\text{port}}\)), measured at the scan frequency of 2.2436 GHz. The normalized abs(\(\Gamma_{\text{port}}\)) and phase(\(\Gamma_{\text{port}}\)), as shown in Figure A-2, highlights the sensitivity of the SMM tool to distinguish the change in capacitance across the test structure. Looking at the scans we can see that as we move from left to right, i.e. from 200nm SiO\(_2\) thickness to 50nm thickness, the SMM response increases for a given area of the gold pad, owing to the reduction in oxide capacitance, as can also be seen from the cross-section cut of the abs(\(\Gamma_{\text{port}}\)) in Figure A-3(a). Also, with the increase in pad area, the net capacitance increases and this is duly reflected in the increased abs(\(\Gamma_{\text{port}}\)) and phase(\(\Gamma_{\text{port}}\)) response, and can be seen in the plot of abs(\(\Gamma_{\text{port}}\)) vs cap area (Figure A-3(b)).

![Figure A-2](image_url)

**Figure A-2.** Normalized (a) abs(\(\Gamma_{\text{port}}\)) and (b) phase(\(\Gamma_{\text{port}}\)) of the measured SMM response of the calibration substrate. Measurement scan frequency was set at 2.2436GHz.
Figure A-3. (a) Linear cut of the abs(Γ_{port}) across the 4µm, 3µm, 2µm and 1µm Au pads across the SiO₂ staircase. (b) Linear dependence of abs(Γ_{port}) plot as a function of capacitor pad area.

The linear relation between the capacitance seen at the tip, C_{tip}, and the measured abs(Γ_{port}) can be mathematically defined with a calibration fit proportionality factor α (units fF/dB) (Eq. A-1) [51]. Furthermore, the net capacitance under the Au pad, seen by the SMM tip, can be written as the series combination of the SiO₂ oxide capacitance and the substrate capacitance (C_{sub}) coming from the doped silicon substrate (Eq. A-2). Combining Eq. A-1 and Eq. A-2, we can evaluate the calibration parameter α and the C_{sub} by performing a linear fit of the $abs(\Gamma_{port})^{-1}$ vs the oxide thickness plot.

\[ C_{\text{tip}} = \alpha abs(\Gamma_{\text{port}}) \]  
\[ \frac{1}{C_{\text{tip}}} = \frac{1}{C_{\text{SiO}_2}} + \frac{1}{C_{\text{sub}}} \]  
\[ \frac{1}{\alpha abs(\Gamma_{\text{port}})} = \frac{t_{\text{ox}}}{A\varepsilon_{\text{ox}}} + \frac{1}{C_{\text{sub}}} \]
Based on the extracted value of $\alpha$ of 1.2292 fF/dB and $C_{sub}$ of 2.06 fF, the measured $\text{abs}(\Gamma_{port})$ was converted to $C_{tip}$ and the resultant map is shown in Figure A-4. The measured $\text{abs}(\Gamma_{port})$ and $\text{phase}(\Gamma_{port})$ was also converted to $C_{tip}$ and $R_{tip}$ (series combination) by the method described earlier in chapter 2 and can be seen in Figure A-5. Instead of using a rigorous comsol simulation to obtain three known impedance for the transformation of $\Gamma_{port}$ to $\Gamma_{tip}$, the impedance mapping was performed by using the theoretical $Z_{tip}$ value. The resultant map shows comparable maps of the $C_{tip}$ and confirms the accuracy of impedance mapping of SMM scans.

Figure A-4. Extracted capacitance after performing the capacitance calibration

Figure A-5. Extracted impedance map, (a) $C_{tip}$ and (b) $R_{tip}$ of the staircase structure
Appendix B

SMM Scans During Thermal IMT in VO$_2$
Figure B-1. Full spatially resolved abs($\Gamma_{\text{port}}$) and phase($\Gamma_{\text{port}}$) scans across the thermally induced IMT. Scans have been normalized from 0 to 1 where 1 is the metallic phase and 0 is the insulating phase. As the temperature is stepped the metallic coverage grows until near total coverage is reached at 352.5K.

Normalized SMM scans showing the evolution of the thermally induced IMT can be seen in Figure B-1. All scans are of the same 2.5μm by 2.5μm area and have been normalized to a 0 to
1 scale where 0 is insulating and 1 is conducting. Metallic domains are first observed at 315K in both the abs(Γ_{port}) and phase(Γ_{port}) channels. As the temperature is gradually increased we can observe an increase in the number of metallic domains which eventually merger and form large metallic regions approaching total coverage.
Appendix C

COMSOL Simulation of Impedance Spectroscopy

Figure C-1. Impedance spectroscopy measurement set up. Measurement was performed vertically between gold (Au) contact pads and a grounded chuck at multiple temperatures.

Impedance spectroscopy was performed with an Agilent 4294A Precision impedance analyzer on a Summit 11000 AP Cascade probe station. The sample was placed on a grounded chuck and contact was made to rectangular contact pads with dimensions of 170μm x 100μm. The set up can be easily visualized in Figure C-1. Cole-Cole plots were generated from 40Hz to 10MHz for 327.5K, 332.5K, and 337.5K.

A 2D axisymmetric COMSOL model is used to fit the measured Cole-Cole plots. The simulation was performed on the scale of the sample in order to account for all spreading resistance due to the conducting nature of the VO₂ film. 100nm VO₂ was modeled atop 100nm SiO₂, and the underlying Si substrate was modeled at 1μm thickness for computational purposes. The length of the model was 5500μm, which is half the length of the physical sample due to the implementation
of rotational symmetry in the model. The ground plane was placed 350μm away from the tip contact in accordance with the actual SMM tip package. The dielectric constants and resistivity values of the SiO$_2$ and Si representative layer were tuned until an ideal fit to the measured Cole-Cole plot was achieved.

Figure C-2. Cole-Cole plots of measured and simulated complex impedance of the sample system. Measured data is displayed as open shapes while the solid lines are the simulated Cole-Cole plots of the calibrated COMSOL model.

The resulting Cole-Cole plots are shown in Figure C-2 and properly reproduce the measured data. Upon calibration of the COMSOL model parameters, the model was used to evaluate three impedances for SMM calibration. For this the top contact was replaced with the SMM tip to scale (as seen in Figure C-3) and simulation were carried out at the scan frequency, and an impedance from the tip to ground plane was obtained. These impedances were used to calibrate the $\text{abs}(\Gamma_{\text{port}})$ and $\text{phase}(\Gamma_{\text{port}})$ to impedance maps. The model can be fully visualized in Figure C-3 where the dimensions of the simulation are shown. The COMSOL model was carried out under the quasi-static approximation in the AC/DC module of COMSOL v4.3.
Figure C-3. Schematic representation of the COMSOL model used to determine the three impedances associated with $|\Gamma_{port}|$ and $\text{phase}(\Gamma_{port})$.

The near tip mesh that was used can be visualized in Figure C-4(a). Grid spacing is set to 1.33nm per point in the first 200nm surrounding the tip. Beyond the 200nm point the grid spacing was graded from a spacing of 32.5nm/pt to 2.5µm/pt beyond the ground point. The corresponding electric potential is shown in Figure C-4(b).
Figure C-4. (a) Close up of mesh used during impedance spectroscopy simulation. (b) Corresponding simulated electric potential with a 250mV applied bias representing an insulating domain at 327.5K.
Bibliography


[57] A. Note, “Agilent AN 1287-3 Applying Error Correction to Network Analyzer Measurements.”


Himanshu Madan hails from Pune, Maharashtra India. He did his high school from K.V. Ganeshkhind Pune, and ranked 2nd in the All India Secondary School Certification Exam (AISSCE) in the Pune Metropolitan Area of India. He received his B.Tech degree from College of Engineering Pune (COEP) in Electronics and Telecommunication. During his undergraduate study he interned with National Center for Radio Astrophysics (NCRA, TIFR) at Giant Meterwave Radio Telescope (GMRT), where he worked on microstrip filter design and the modelling and improvement of GMRT L-band front-end receiver.

To pursue his interest in high-frequency circuit design Himanshu joined the Nanoscale Device and Circuit Laboratory (NDCL) at PennState in 2008, where he worked under the guidance of Dr. Suman Datta. While at NDCL, Himanshu’s work contributed towards research on conventional semiconductors and novel materials for RF circuit applications, in particular the development of high-frequency graphene based mixer and vanadium dioxide based RF switches. Both these works were selected to be presented at the prestigious International Electron Device Meeting (IEDM). During his graduate study Himanshu also interned with SEMATECH research consortium Albany, NY for a year, where he worked on optimization of semiconductor/high-κ interface. He obtained his Ph.D. degree in 2015 from the Department of Electrical Engineering at Penn State. After his PhD, he is headed to Intel Corp. where he will be working as a Device Engineer in the Logic and Technology Development Group in Hillsboro, OR.

During his Ph.D., he has co-authored 10 journal and 17 conference publication, of which 9 were first author. His work on Gallium Antimonide high-κ interface optimization with Ashkar Ali earned them the best student paper award at the 2010 Device Research Conference. He can be contacted at his email himanshu.madan@yahoo.com.