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IMPROVING THE QUALITY OF CVD GRAPHENE BASED DEVICES AND TRANSPORT STUDIES OF FEW-LAYER WSE_2

A Dissertation in

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by

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ABSTRACT

This dissertation consists of two main topics: a) advances on the synthesis and quality of chemical vapor deposited graphene and devices; b) electrical and thermoelectrical transport studies of semiconducting transition metal dichalcogenides (TMDC), in particular few-layer WSe_2.

Chapter 1 introduces the band structures of graphene and TMDC, as well as the novel physics and potential applications of both materials.

Chapter 2 describes the chemical vapor deposition (CVD) synthesis of graphene on copper using gaseous precursors of methane and hydrogen. Experimenting with the etching of carbon by hydrogen gas during and post growth, we demonstrate successful suppression of multilayer graphene growth, which is a common problem of the field. Next, we show that incorporating a diluted SC-2 cleaning step into the transfer process of CVD grown graphene removes metallic contaminations effectively and leads to a significant improvement of carrier mobility from several thousand cm^2/Vs to 18,000 cm^2/Vs at room temperature. These studies contribute to the improvement of graphene-based devices towards practical applications.

Chapter 3 focuses on the characterization of various TMDC materials including MoS_2, WS_2, and WSe_2 using microscopy and spectroscopy. We obtain the crystal structure of WSe_2 using high-resolution transmission electron microscopy (TEM) and X-Ray diffraction (XRD). The layer number-dependent intensity ratio of two Raman modes (2LA and A_{1g}) is studied and used to identify the layer number in few-layer WS_2. The size of the direct band gap (monolayer) and indirect band gap (few-layer to bulk) of

WSe_2 is obtained from photoluminescence (PL) spectroscopy. In monolayer WSe_2, the width of the A-exciton emission peak decreases with decreasing temperature and saturates at low temperatures to around 15 meV, demonstrating good sample quality. PL spectra of ion irradiated WS_2 reveal additional emissions attributed to defect-bound excitons. Various atomic force microscopy (AFM) based imaging techniques, such as topographic AFM, Kelvin probe force microscopy (KPFM), and scanning thermal microscopy (SThM) are employed to study the morphology, work function and thermal conductivity of few-layer WSe_2 and WS_xSe_{2-x} alloys. These studies provide valuable information on the physical properties of the TMDC materials.

Chapter 4 focuses on the electrical transport properties of few-layer WSe_2 field-effect transistors. We study the gate-dependent conductance of the transistor in the subthreshold regime and demonstrate that the resistance of the Schottky barrier contacts dominates the two-terminal resistance. The transmission mechanism through the contact is found to be thermionic field emission (TFE), which arises from a large amount of impurity states inside the band gap. Applying the TFE model, we self-consistently determine the density of the impurity states to be approximately $1\sim2\times10^{13}$ cm^2/eV. We determine these impurity states are due to internal contributions rather than originating from the substrate by comparing devices fabricated on different substrates. The large number of impurity states leads to high mobility-edge carrier density (~ 1.1×10^{13} $/cm^2$ in our devices) and low carrier mobility (~ 200 $cm^2V^{-1}s^{-1}$ in our devices), Our studies shed light on the electrical transport properties of TMDC materials and highlight the material quality challenge of the field.

Chapter 5 presents preliminary thermoelectric transport study of few-layer WSe_2. Using micro-patterned thermometer and heaters, we obtain preliminary results on the Seebeck coefficient of a 5-layer WSe_2 device. The magnitude of the Seebeck coefficient increases as the Fermi level is increased towards the conduction band edge and exceeds 200 μV/K at high carrier densities.

Chapter 6 summarizes the studies discussed in this dissertation.

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Many of the experiments that were accomplished in this thesis are the results of help from group members and collaborations with different research groups. My sincere thanks to Minh An Nguyen, Daniel Rhodes, Jiaqiang Yan, from whom I obtained the TMDC crystals. I feel grateful to Dr. Bei Wang who taught me the synthesis of CVD graphene and device fabrication techniques when I joined Jun's group. I thank Jing Li for sharing with me many of the device fabrication techniques and helping me in solving problems in many electrical measurements. I thank Simin Feng for helping me with the Raman and Photoluminescence measurements.

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Finally, I would like to thank my parents and grandparents for their love, support, and confidence in me. I dedicate my dissertation to them.

To my beloved parents and grandparents

谨以此论文献给我敬爱的父母和祖父母

Chapter 1

Introduction

Scientific research in two-dimensional (2D) materials have been developing at a fast pace ever since the first experimental discovery of single-layer graphene in 2004.[1-3] Due to the confinement of charge carriers and phonons, 2D materials possess novel physical properties and show great application potentials. Although active experimental explorations have only been slightly more than 10 years, theoretical studies of the 2D materials can trace back to more than 50 years ago. For example, the electronic band structure of graphene was first proposed by P. R. Wallace in 1947[4].

Formed by a layer of carbon atoms, monolayer graphene can be viewed as the base material of sp^2-hybridization based carbon nanomaterials, such as zero-dimensional fullerenes, one-dimensional carbon nanotubes, and three-dimensional graphite. Many excellent experiments have demonstrated graphene as an ideal platform for fundamental studies and a wonder material with superior material properties.[5-7] Recently, research in 2D materials have gone beyond graphene with new atomically thin materials being synthesized and explored, among which semiconducting transition metal dichalcogenides (TMDC), which have a common chemical formula MX_2 (M=Mo, W; S=S, Se, and Te), have received intense scientific attentions. While monolayer graphene is a zero-gap material, semiconducting TMCD possesses a band gap of 1 ~ 2 eV depending on the actual composition, and shows interesting electronic, optical, and valleytronic properties.[8] Therefore, graphene and the semiconducting TMDC are usually viewed as the metal and semiconductor building blocks in the family of 2D materials.

This chapter makes an introduction to both materials on topics including the crystal and electronic band structures, as well as some of the novel physics and potential applications.

1.1 Graphene

1.1.1 Lattice structure

Monolayer graphene consists of a layer of carbon atoms that are arranged in a hexagonal lattice plane. Within the lattice plane, the bonds between two nearest-neighbor carbon atoms are formed from sp^2 hybrid orbitals. When multiple monolayer graphene sheets are stacked through van der Waals interactions, they form one of the most common carbon materials, i.e. graphite.

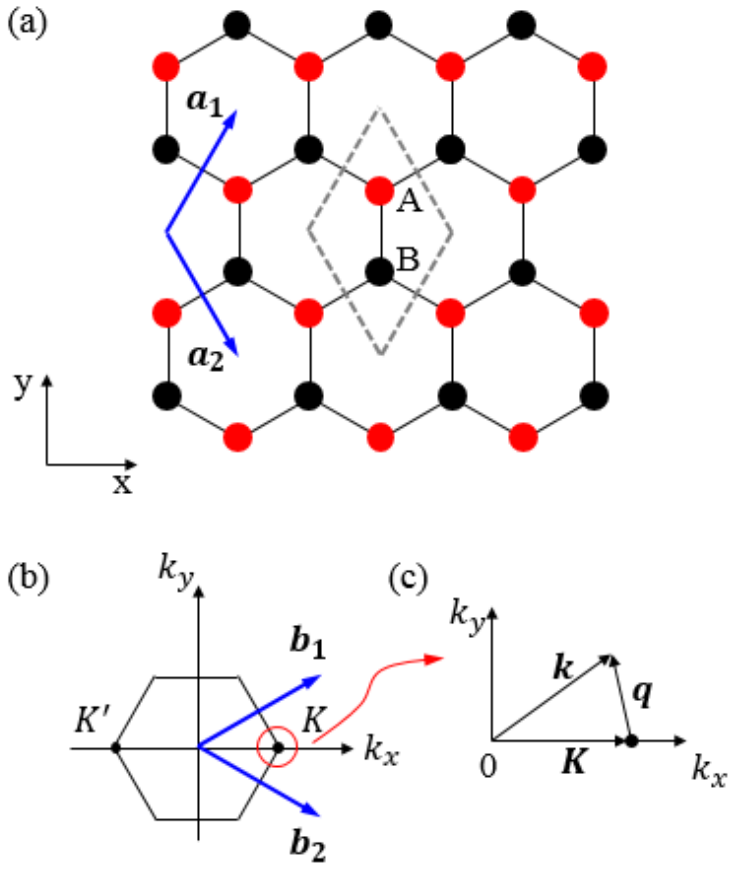


Figure 1-1. Schematics of (a) lattice structure of monolayer graphene, (b) Brillouin zone, and (c) k-space near the K or K' point.

Figure 1-1(a) is a schematic drawing of the lattice structure for a single-layer graphene. There are two sublattices, represented by the red and black symbols, and they are labeled as A

and B carbon sites. There are two carbon atoms in each unit cell. The nearest-neighbor carbon-carbon bond length is $a_{CC} = 1.42$ Å. $\boldsymbol{a_1}$ and $\boldsymbol{a_2}$ are the unit cell vectors and are given by

$$\boldsymbol{a_1} = \left(\frac{a}{2}, \frac{\sqrt{3}a}{2}\right), \qquad \boldsymbol{a_2} = \left(\frac{a}{2}, -\frac{\sqrt{3}a}{2}\right) \tag{1.1}$$

where $a = |\boldsymbol{a_1}| = |\boldsymbol{a_2}| = \sqrt{3}a_{CC}$ is the graphene lattice constant.

The corresponding reciprocal lattice vectors $\boldsymbol{b_1}$ and $\boldsymbol{b_2}$ are given by

$$\boldsymbol{b_1} = \left(\frac{2\pi}{a}, \frac{2\pi}{\sqrt{3}a}\right), \qquad \boldsymbol{b_2} = \left(\frac{2\pi}{a}, -\frac{2\pi}{\sqrt{3}a}\right) \tag{1.2}$$

Figure 1-1(b) plots the hexagonal Brillouin zone of monolayer graphene based on the two reciprocal lattice vectors. While there are six corners in the Brillouin zone, only two of them are nonequivalent and they are labeled as K and K' points. Their coordinates in the k-space are

$$K = \left(\frac{4\pi}{3a}, 0\right), \qquad K' = \left(-\frac{4\pi}{3a}, 0\right) \tag{1.3}$$

As will be discussed next, it is the unusual electronic band structure at the six corners of the Brillouin zone that makes graphene an amazing material.

1.1.2 Electronic band structure

The electronic band structure of monolayer graphene E($\mathbf{k}$) is deduced from tight-binding approximation by considering one $2p_z$ orbital from the two carbon atoms in one unit cell. An analytical expression of E($\mathbf{k}$) can be obtained by solving a secular equation

$$det(H_1 - ES_1) = 0 \tag{1.4}$$

where H_1 and S_1 are the transfer and overlap integral matrices, respectively. E($\mathbf{k}$) is then given by

$$E_{\pm}(\boldsymbol{k}) = \frac{\epsilon_{2p} \pm \gamma_0 |f(\boldsymbol{k})|}{1 \mp s_0 |f(\boldsymbol{k})|} \tag{1.5}$$

$$f(\boldsymbol{k}) = e^{ik_y a/\sqrt{3}} + 2e^{-ik_y a/2\sqrt{3}} \cos(k_x a/2) \tag{1.6}$$

Here E_+ and E_- represent the two energy bands above and below the Fermi level, respectively. E_+ is also known as π^* band and E_- as π band. ϵ_{2p} is energy of the $2p_z$ orbital, γ_0 and s_0 are the nearest-neighbor transfer and overlap integrals, respectively. $f(\boldsymbol{k})$ describes the hopping between A and B atoms and serves as an indicator of the coupling strength between the two sublattices. Exactly at the K and K' points, $f(\boldsymbol{k}) = 0$, indicating there is no coupling between the two sublattices.

Around the $\boldsymbol{K}(\boldsymbol{K'})$ point, as shown in Fig. 1-1(c), the $\boldsymbol{k}$ vector can be expresses as

$$\boldsymbol{k} = \boldsymbol{K} + \boldsymbol{q} \tag{1.7}$$

where $\boldsymbol{q}$ is a small vector measured from the $\boldsymbol{K}(\boldsymbol{K'})$ point. Substituting Eq. (1.7) into Eqs. (1.5) and (1.6), the energy dispersion relation around the $\boldsymbol{K(K')}$ can be expressed as

$$E_{\pm}(\boldsymbol{q}) - \epsilon_{2p} \approx \pm\hbar|\boldsymbol{q}|v_F \tag{1.8}$$

and

$$v_F = \frac{\sqrt{3}\gamma_0 a}{2\hbar} \tag{1.9}$$

is the Fermi velocity, whose value is experimentally determined to be $1.0 \sim 1.1 \times 10^6$ m/s in the linear dispersion regime.[9] Because Eq. (1.8) takes the same form of massless Dirac equation, the $\boldsymbol{K}(\boldsymbol{K'})$ point is also known as the Dirac point. Figure 1-2 shows a calculated 3D representation of the electronic band structure and the linear dispersion near the $\boldsymbol{K(K')}$ point.

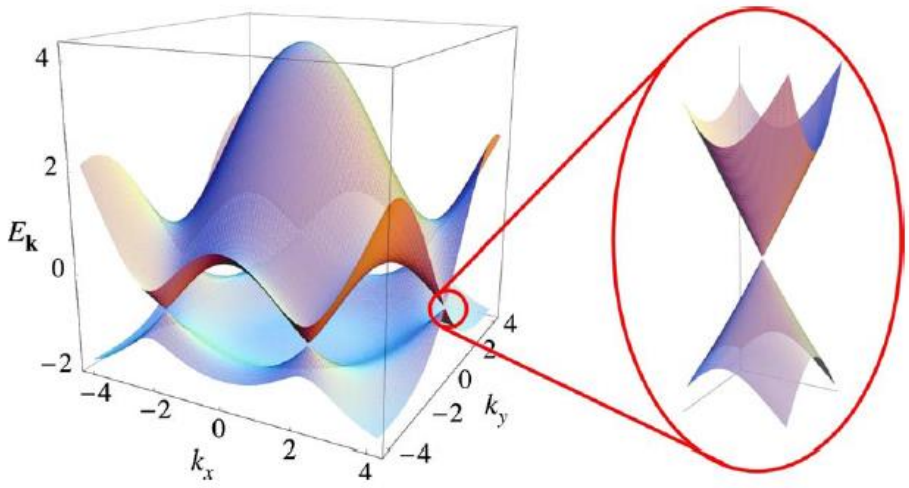


Figure 1-2. Electronic band structure of monolayer graphene. Adapted from Fig. 3 of Ref. [9]

1.1.3 Novel physics and potential applications

Over the past decade, graphene has been demonstrated as a unique two-dimensional electron gas system (2DEGs) where novel physics have been theoretically predicted and/or experimentally observed, such as half integer quantum hall effect (QHE)[3, 10], Klein tunneling[11], quantum spin hall effect[12], spin polarized edge states[13], etc.

Besides being an ideal material for fundamental research, graphene also shows great potential in a variety of applications due to its excellent electronic, optical, thermal, and mechanical properties. Graphene is a superior conductor with extremely high carrier mobility (e.g., exceeding 2×10^5 $\mathrm{cm}^2/\mathrm{Vs}$ at room temperature[6]) and ability of sustaining ultrahigh current density (on the order of 10^8 $\mathrm{A/cm}^2$[14]). It has a high optical transmittance for visible lights with an absorptance of 2.3% per layer[15]. With a room-temperature thermal conductivity of ~ 5,000 W/mK[16], graphene is the most thermally conductive material up to date. Graphene also shows superior mechanical strength with a Young's modulus of 1 tesla pascals[17], which is the strongest material ever measured. Besides these intrinsic properties, graphene can also be

chemically functionalized to extend its application potentials, such as through hydrogenation[18], fluorination[19-21], etc.

The application potential of graphene has been demonstrated in many areas including electronics, optics, optoelectronics, etc. A common graphene-based electronic structure involves using graphene as the conduction channel in field effect transistors (FETs). So far, various functions have been realized by integrating graphene FETs, such as radio frequency transistors[22], biosensors[23], etc. Due to its excellent electrical, optical and mechanical properties, graphene has been demonstrated as an ideal material for flexible and transparent electrodes[24], which is very promising in replacing the currently widely used indium tin oxide (ITO)[25]. When graphene is functionalized with fluorine atoms, i.e. fluorographene, the original sp^2 carbon-carbon bonds transform into sp^3 hybridizations. This opens up a large band gap (~ 3.8 eV[26]) in fluorographene, which is now the world's thinnest insulating material[27].

1.2 Semiconducting transition metal dichalcogenides (TMDC)

1.2.1 Lattice structure

Transition metal dichalcogenides (TMDC) is another class of layered materials with strong covalent intra-layer bonds and weak inter-layer van der Waals interactions. It has the chemical formula MX_2, where M is the transition metal W and Mo, and X is the group-IV chalcogenides S, Se, and Te. Monolayer MX_2 consists of an M layer sandwiched between two X layers. Figure 1-3(a) is a top view schematics of the monolayer lattice structure exhibiting a hexagonal pattern. Here, the top and bottom layer X atoms overlap at the same position. Each primitive unit cell contains one M atom and two X atoms as is outlined by the dashed grey lines.

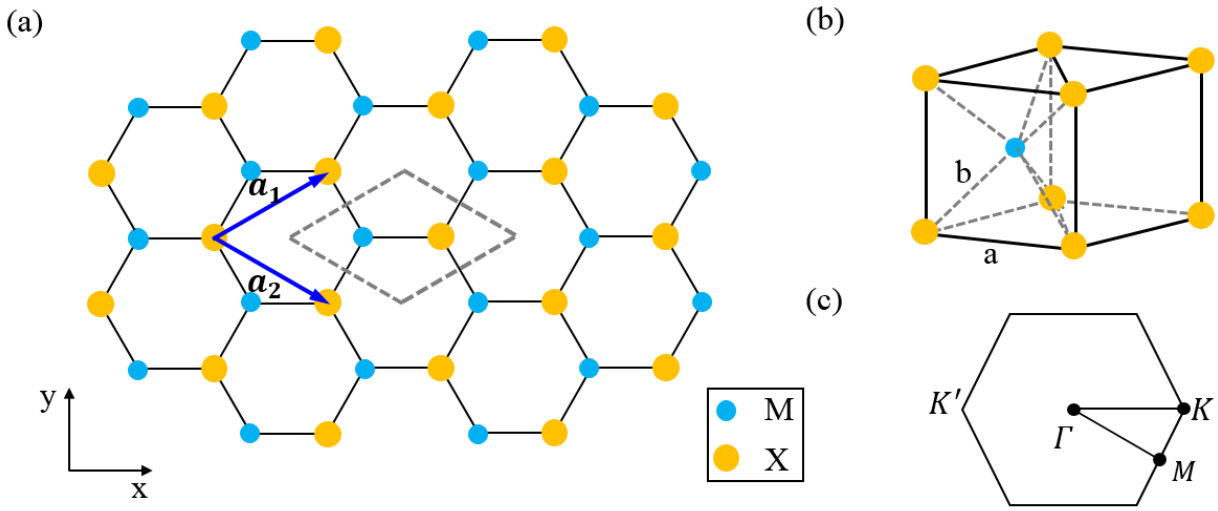


Figure 1-3. Schematics of (a) lattice structure, (b) unit cell, and (c) Brillouin zone of monolayer MX_2.

A three-dimensional (3D) view of the unit cell is shown by Fig. 1-3(b) where the M and X atoms are arranged in a trigonal prism coordination. *a* is the in-plane lattice constant. b is the bond length between the nearest-neighbor M and X atoms.

$\boldsymbol{a_1}$ and $\boldsymbol{a_2}$ are the unit cell vectors and are given by

$$\boldsymbol{a_1} = \left(\frac{\sqrt{3}a}{2}, \frac{a}{2}\right), \qquad \boldsymbol{a_2} = \left(\frac{\sqrt{3}a}{2}, -\frac{a}{2}\right) \tag{1.10}$$

where $|\boldsymbol{a_1}| = |\boldsymbol{a_2}| = a$ is the in-plane lattice constant.

The corresponding reciprocal lattice vectors $\boldsymbol{b_1}$ and $\boldsymbol{b_2}$ are then given by

$$\boldsymbol{b_1} = \left(\frac{2\pi}{\sqrt{3}a}, \frac{2\pi}{a}\right), \qquad \boldsymbol{b_2} = \left(\frac{2\pi}{\sqrt{3}a}, -\frac{2\pi}{a}\right) \tag{1.11}$$

Same as graphene, the Brillouin zone of monolayer MX_2 is also hexagonal with two inequivalent *K* and *K'* points. When multiple layers are stacked to form 3D crystals, the bulk property can be quite different depending on the stacking orders and coordination of the transition metal atoms. There are three polytypes: a hexagonal 2H form, a rhombohedral 3R

form, and a 1T form.[28] The stacking order of the 2H-phase is shown in Figure 1-4, where one unit cell consists of two monolayers.

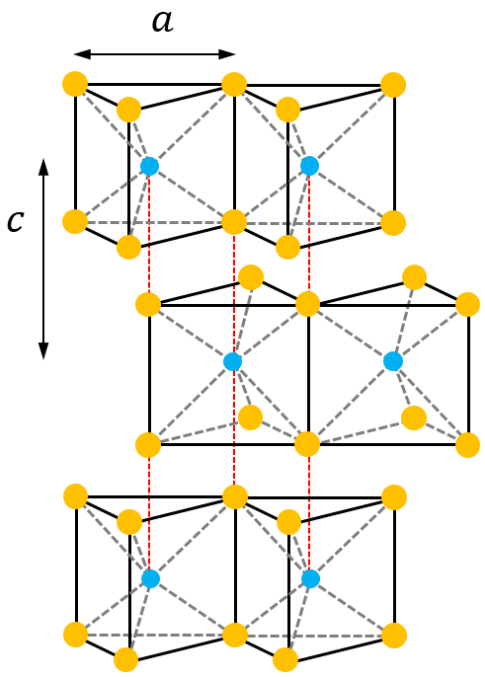


Figure 1-4. Schematics of 2H-TMDC structure.

In this dissertation, our work on the TMDC material are based on crystals with the 2H structures.

1.2.2 Electronic band structure

The electronic band structures of monolayer (1H) and 2H-bulk TMDC have been systematically studied by Kumar *et al.*[29] using first principles calculation. For monolayer TMDC, the energy bands that are close to the Fermi level are primarily formed by the metal d orbitals. For example, Figure 1-5(a) shows a calculated electronic band structure and the corresponding partial and total density of states (DoS) of monolayer WSe_2 from Ref. [29].

Energy states close to the Fermi level are predominantly contributed by the W_5d orbital states, while the Se orbital states only make up a small portion of the total energy states.

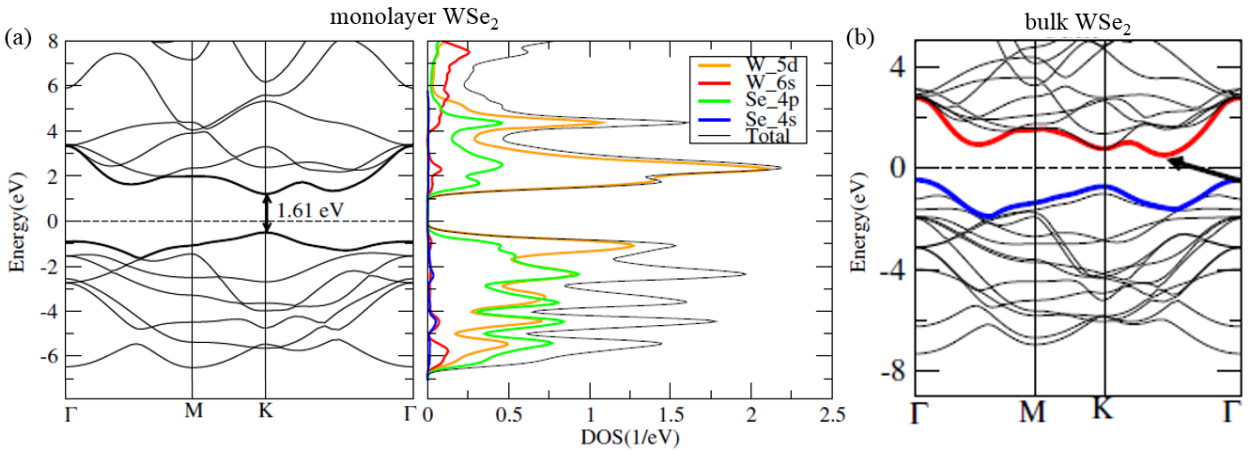


Figure 1-5. (a) Electronic band structure and total and partial density of states of monolayer WSe_2. Adapted from Fig. 7 of Ref. [29]. (b) Electronic band structure of bulk WSe_2. Adapted from Fig. 13 of Ref. [29].

In the monolayer limit, MX_2 band gap is direct with the conduction and valence band extrema appear at the *K(K')* point, as shown by the monolayer WSe_2 example in Fig.1-5(a). As the layer number increases, the band gap becomes indirect due to inter-layer interactions.[29] The conduction band minimum is shifted to somewhere between the *Γ* and *K* points, while the valence band maximum is found at the *Γ* point, as shown in Fig. 1-5(b). Table 1-2 lists the band gaps of different MX_2 for both monolayer and 2H-bulk forms. Gap sizes from theoretical calculations are labeled with (cal.), and the experimentally measured ones are labeled with (exp.).

Table 1-1 Experimental and theoretical band gap sizes of monolayer and 2H-bulk TMDC.

TMDC	$E_{g,1L}$ (eV)	$E_{g,bulk}$ (eV)
MoS_2	1.8[30] (exp.)	1.23[31] (exp.)
	1.78[32](cal.)	1.29[33] (exp.)
$MoSe_2$	1.49[32](cal.)	1.09[31] (exp.)
		1.1[33] (exp.)
$MoTe_2$	1.13[32](cal.)	1.0[33] (exp.)
WS_2	1.93[32](cal.)	1.35[33] (exp.)
WSe_2	1.61[29](cal.)	1.20[33] (exp.)

Due to a strong spin-orbit coupling of the heavy transition metal atoms, there are splitting in both the valence and conduction bands of monolayer TMDC.[29, 34] The conduction band splitting is in the meV range, while that of the valence band is in general a few hundred meV, e.g. 0.148 eV (MoS_2), 0.430 eV($MoSe_2$), 0.430 eV(WS_2), and 0.466 eV(WSe_2).[35]

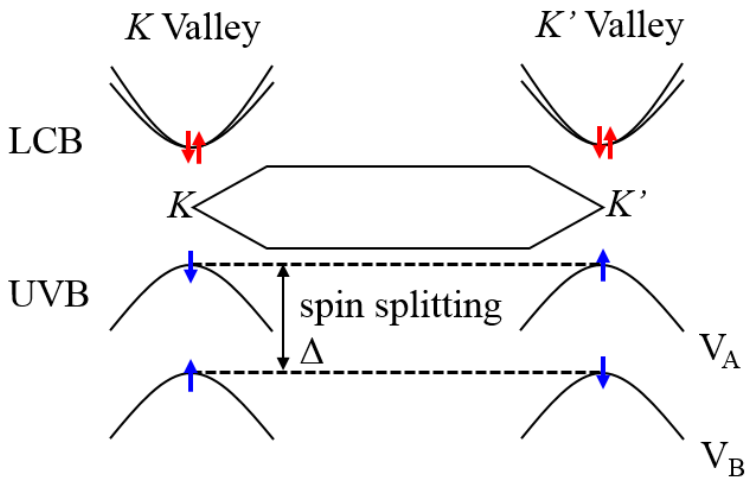


Figure 1-6. Valence band splitting and coupling between the spin and valley degrees of freedom in monolayer TMDC.

Another important property of monolayer TMDC is the coupling between spin and valley degrees of freedom. Due to the valence band splitting and inversion symmetry breaking, energy states at these two valleys are no longer the same even though they occupy the same energy levels.[36] Hence, the spin distribution at the *K* and *K'* valleys are opposite, as is schematically shown in Fig. 1-6.

With these interesting features, TMDC has become an important 2D material for fundamental research and potential applications, which will be discussed next.

1.2.3 Novel physics and potential applications

Many interesting physics in the TMDC systems are associated with their spin and valley properties. Valley-dependent optical selection rules have been theoretically proposed in monolayer MoS_2 and other MX_2 monolayers.[36] Control of valley polarizations, i.e. selective population of one valley, has been experimentally realized in monolayer MoS_2 through optical pumping with circularly polarized light.[37, 38] Using the same method, an anomalous Hall effect, i.e. valley Hall effect, is observed in monolayer MoS_2 transistors where the sign of Hall voltage depends on the helicity of excitation light, which determines the valley polarization.[38] It has also been predicted in Ref. [36] that the Berry-phase-driven spin Hall effect coexists with the valley Hall effect in monolayer MX_2 systems for both electrons and holes.

Besides being an excellent laboratory for the exploration of interesting and novel physics, TMDC has also shown great application potentials in electronics, optoelectronics, and spin-valleytronics. Large current on/off ratio exceeding 10^7 has been demonstrated in monolayer MoS_2 transistors[39], and a further increase to $> 10^{10}$ is predicted.[40] Electronic circuits with logic operation functions have been demonstrated based on mono- and bilayer MoS_2.[41, 42]

Utilizing the visible-range direct bandgap property, monolayer TMDC has been demonstrated as a promising material in photovoltaics and photodetectors.[43, 44] Another advantage of the TMDC is its potential as a thermoelectric material with enhanced figure-of-merit. An ultralow cross-plane thermal conductivity (~ 0.05 W/mK) has been reported in disordered thin WSe_2 films.[45] With proper engineering to enhance the Seebeck coefficient and electrical conductivity, TMDC-based thermoelectric materials with superior performance may be realized in the future.

Chapter 2

The synthesis and characterization of graphene

Graphene has demonstrated itself as a ‘miracle material’ in both scientific research and potential applications due to its excellent electrical, thermal, optical and mechanical properties.[5, 6, 15] Monolayer graphene was first extracted from bulk graphite crystals into a free-standing form using a mechanical exfoliation technique in 2004.[1] Ever since then, this technique has been widely used in laboratories to produce graphene sheets with the highest quality. However, the lateral sizes of these graphene sheets are usually limited to a few micron to a few tens of microns, while the location of their appearance is random. Such inconvenience hardly poses a problem for laboratory research, but becomes a serious issue for future industrial applications. In this respect, chemical vapor deposition (CVD) has been demonstrated to be promising for graphene production in a large-scale and cost-effective way.[24] This technique involves using transition metal films, such as Cu, Ni, Ru, Pt, Co, Pd, and Re, as the growth substrates for graphene formation.[46-52] During a typical CVD process, hydrocarbon precursors are decomposed at the transition metal surface into carbon radicals in a hot reactor. These carbon radicals then arrange themselves into hexagonal patterns and form graphene sheets of various thickness. A third way of synthesizing graphene is through the sublimating of Si atoms at SiC wafer surface.[53]

This chapter focuses on the CVD synthesis of graphene on copper and electrical tests of graphene field effect transistors (GFETs). It first makes an introduction to two characterization techniques, i.e. Raman spectroscopy and scanning electron microscopy (SEM), which are commonly used in characterizing graphene (Section 2.1). Then, in section 2.2, we discuss three CVD methods used in graphene synthesis and the suppression of multilayer growth. Section 2.3

describes GFET fabrication procedures. Electrical test results of the GFETs are discussed in Section 2.4.

2.1 Graphene characterizations

Raman spectroscopy is widely used in graphene studies providing important information, such as defects density[54, 55], layer number identification[56], and electron-phonon interactions[57, 58]. SEM is another useful tool for direct imaging of the surface morphology of the synthesized the graphene. In this dissertation, we primarily use SEM to find MLG coverage percentage to correlate with different growth conditions to achieve the goal of complete MLG suppression.

2.1.1 Raman spectroscopy

2.1.1a Raman scattering theory

Raman scattering describes an interaction process where incident photons are inelastically scattered from an atom or a molecule through the interaction with an excitation, such as phonons, molecular energy level transitions, etc.[59] After the atom or molecule absorbs the incident photon energy $h\nu_0$, they are first excited to a virtual energy state and then relaxes back to the initial energy state through emitting another photon.

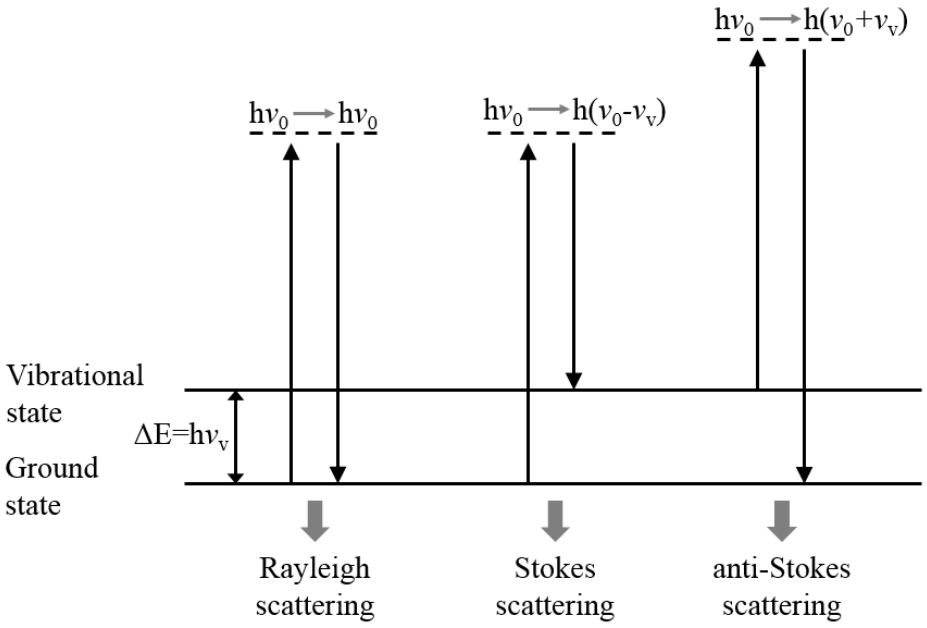


Figure 2-1. Schematic diagram of Raman scattering process.

Depending on the energy difference ΔE between the scattered and incident photons, there are three scattering processes, as shown in Fig. 2-1. $h\nu_{\mathrm{v}}$ is the energy difference between the first vibrational state and the ground state. If the initial or final energy state of the atom or molecule does not couple to other excitation energy besides the incident photons, the emitted photon will have the same energy as the incident photon. This process is called Rayleigh scattering and is the dominant process. The Stokes and anti-Stokes scattering processes result in the emitted photons with energies lower and higher than the incident photon energy $h\nu_0$ by $h\nu_{\mathrm{v}}$, respectively. However, their occurrence probability is very low (approximately 1 in 10 million) except in the case of resonant scattering, where the incident photon energy matches an electronic transition energy. In graphene, the resonant Raman scattering condition is met, which generates strong Raman response as will discussed next.

2.1.1b Raman spectra of graphene

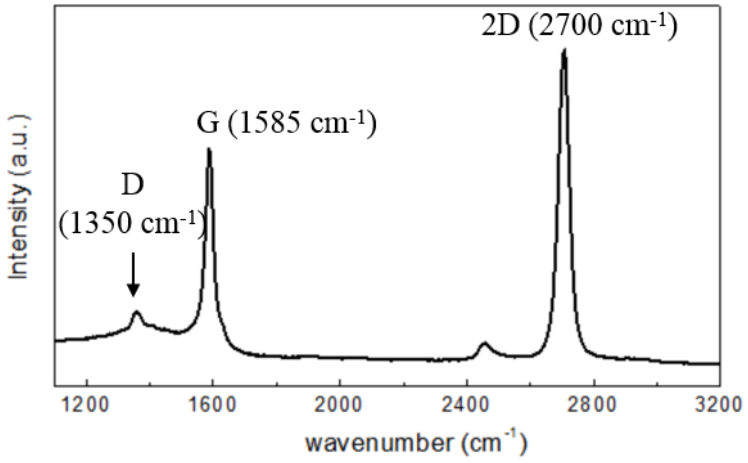


Figure 2-2. Raman spectrum from a defective monolayer graphene. 514 nm excitation laser line.

Raman spectroscopy probes the graphene phonon modes via inelastic scattering of the incident laser excitation.[60] In a Raman spectrum of pristine monolayer graphene, there are two prominent peaks around 1585 cm^{-1} and 2700 cm^{-1}, which are called G band and 2D band, respectively. When defects are present in the lattice, a disorder-induced D-band appears around 1350 cm^{-1}. Figure 2-2 is a Raman spectrum from a defective CVD graphene monolayer showing all three Raman peaks.

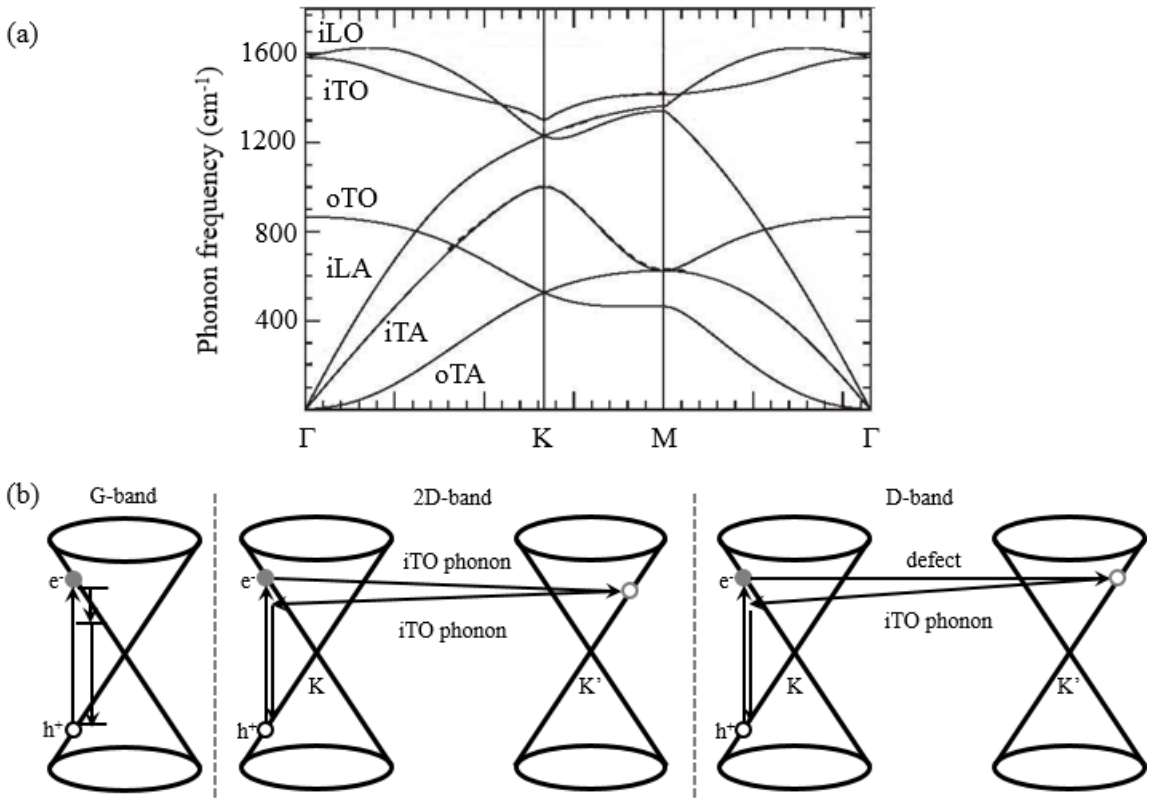


Figure 2-3. (a) DFT calculated phonon dispersion of monolayer graphene. Adapted from Fig. 1 of Ref. [61] (b) Resonant scattering process for G-band (left), 2D-band (middle), and D-band in graphene Raman.

The origin of the three Raman-active modes can be well understood by correlating their peak positions with the phonon dispersion of monolayer graphene. Since each unit cell has two carbon atoms, monolayer graphene possesses three acoustic phonon modes and three optical phonon modes. Figure 2-3(a) shows the phonon dispersion of graphene from density-function theory (DFT) calculation.[61] The Raman scattering process for the G-band is a first-order scattering process involving the zone-center degenerate phonons (Γ) iTO and iLO. iTO is the in-plane optical phonon mode and iLO is the in-plane longitudinal optical phonon mode. The 2D-band, on the other hand, arises from a second-order scattering process involving two iTO phonons near the *K* point. The D-band also originates from a second-order scattering process but can only be

activated in the presence of at least one defect point. Figure 2-3(b) illustrates the first and second order scattering processes associated with the three graphene Raman modes.

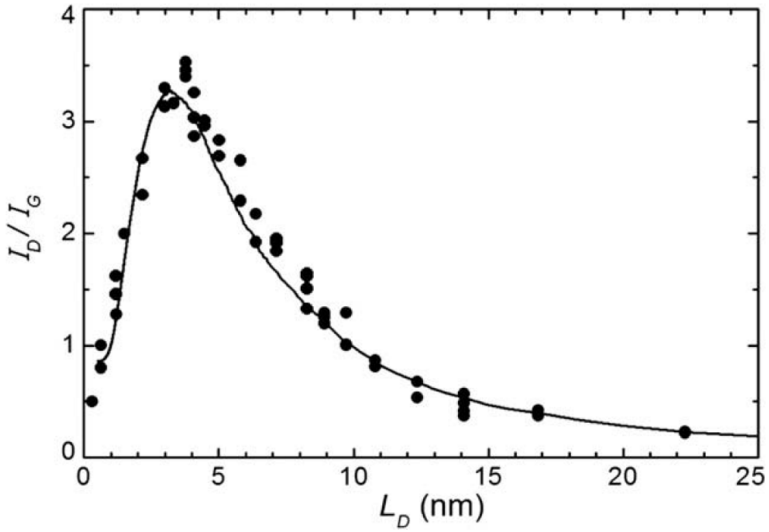


Figure 2-4. I_D/I_G vs the average spacing L_D for monolayer graphene. Adapted from Fig. 4 of Ref. [55].

Raman spectroscopy has also been demonstrated as an important and useful tool in the studies defects in graphene.[54, 55, 62] A Raman-based quantitative model for the density of defects in graphene has been reported by Lucchese *et al*.[55]. They correlated the Raman intensity ratio between the defect-inducted D-band and the G-band, i.e. I_D/I_G, with the average defect spacing L_D obtained from scanning tunneling microscopy (STM) measurements, and found that I_D/I_G does not follow a monotonic relation with L_D but rather reaches a maximum value around L_D =4 nm, which corresponds to a defect density ~ 0.2%. In the less defective regime, i.e. L_D >4 nm, I_D/I_G increases in a non-linear fashion as L_D decreases. After crossing the saddle point, it then sharply decreases to below 1. Figure 2-4 shows the I_D/I_G vs L_D relation from Ref. [55].

2.1.2 Scanning electron microscopy (SEM) of graphene

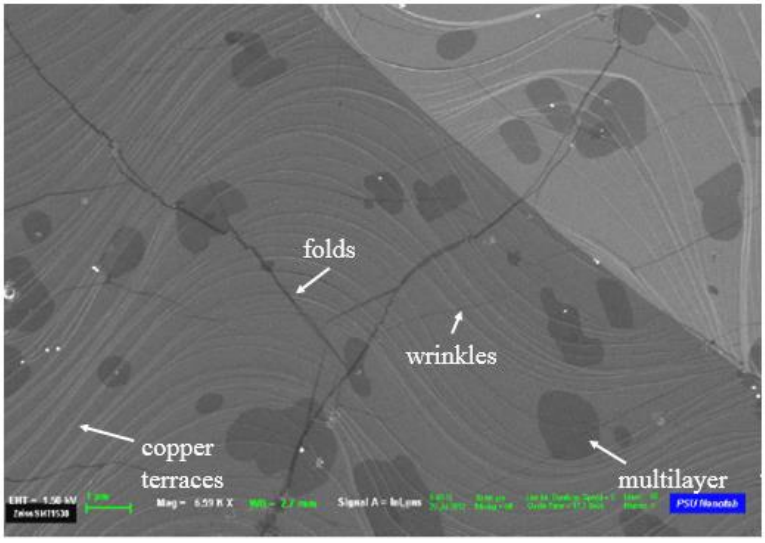


Figure 2-5. A typical SEM image of graphene on copper grown by a standard CVD method. Common features such as graphene folds, wrinkles, and multilayer islands, as well as copper terraces are indicated by arrows.

SEM is employed in characterizing the surface morphology of as-grown CVD graphene on copper substrates. Through quantitative analysis on the SEM images using an open-source software ImageJ, we are able to determine the MLG size and coverage in as-grown graphene films. Figure 2-5 is an SEM image of graphene on Cu showing features such as multilayer graphene islands, graphene folds and wrinkles, as well as copper terraces, in addition to the monolayer background. The large regions with different contrast correspond to different copper domains.

2.2 Graphene synthesis via low-pressure chemical vapor deposition (LPCVD)

Among the many transition metal substrates, polycrystalline Ni and Cu films are the two most studied for CVD graphene synthesis.[46, 63, 64] Due to a large difference in carbon

solubility, graphene growth on Ni and Cu occur via two different mechanisms. Because of a large carbon solubility and high carbon diffusivity[65], graphene growth on Ni happens in two steps, i.e. precipitation and segregation of carbon atoms.[64] First, hydrocarbon molecules are decomposed at the Ni surface followed by diffusion into the body and forming Ni-C solid solutions. This step happens at high temperatures and is usually controlled to last for a short time such that the amount of carbon atoms stored in Ni is limited. Then, as the reactor temperature decreases, carbon atoms segregate from Ni due to a reducing solubility and form graphene films. The thickness of the graphene film is shown to depend on the cooling rate. It has been demonstrated in Ref. [64] that large-area graphene films of several layers can be synthesized with a controlled cooling rate. Figure 2-6 shows an optical image of CVD graphene transferred to SiO_2/Si substrates after synthesis using Ni.[66] The light pink areas are monolayer graphene as pointed by the red arrow. The additional irregular-shaped patches with colors varying from light purple to gold are thick graphene patches.

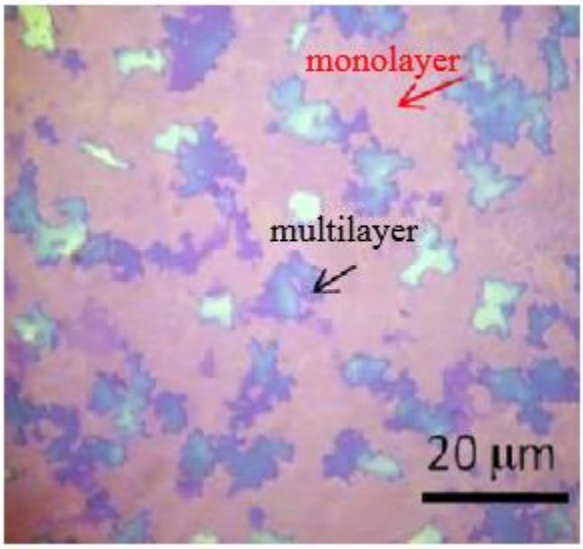


Figure 2-6. An optical image of CVD graphene transferred on SiO2/Si substrates from Ni. Adapted from Fig. 4 of Ref. [66]

Contrary to nickel and other transition metals, copper has a much lower carbon solubility which enables large-area monolayer graphene growth.[46] During the CVD process, hydrocarbon precursors decompose into carbon radicals at Cu surface in a hot reactor. Instead of diffusing into the Cu body, the majority of the atoms directly form small monolayer graphene islands at different nucleation sites and then expand laterally. At the same time, a small portion of the carbon atoms get stored at defect sites in the Cu substrate via diffusion where the carbon solubility is large. As soon as all individual monolayer islands coalesce and fully cover the catalytic Cu surface, decomposition of the hydrocarbon molecules ceases. Without further supply of carbon atoms, the growth process stops even if there is still ample hydrocarbon molecules. Hence, the growth of graphene on Cu is a self-limiting process and the majority of the graphene film is monolayer. In a standard CVD process, the hydrocarbon precursor is supplied continuously. In this dissertation, we refer to it as continuous-CVD. As already shown by the SEM image in Fig. 2-5, the synthesized monolayer graphene film is usually accompanied by multilayer islands at random locations. The multilayer formation mechanism is related to the additional carbon atoms stored at Cu defect sites and will be discussed in detail later in this section. One of the initial motivations behind the work discussed in this chapter is to achieve multilayer-free graphene growth for the consideration of using CVD graphene for real applications, which have a high requirement on the uniformity of the synthesized graphene films.

2.2.1 Continuous-CVD synthesis

In our group, we first adopt a low-pressure continuous-CVD method using copper as the growth substrate following Ref. [46]. Figure 2-7(a) shows a schematic drawing of the CVD system. We use are thin copper foils with thickness of 25 μm and purity of 99.8% that are

purchased from Alfa Aesar. Methane and Ar/H_2 (9:1) are used as precursors. Their flow rates are controlled by the mass flow controllers (MFC) located at the upstream of the system. A mechanical pump at the downstream can reduce the reactor pressure to ~ 1T during growth. Figure 2-7(b) shows the real CVD system.

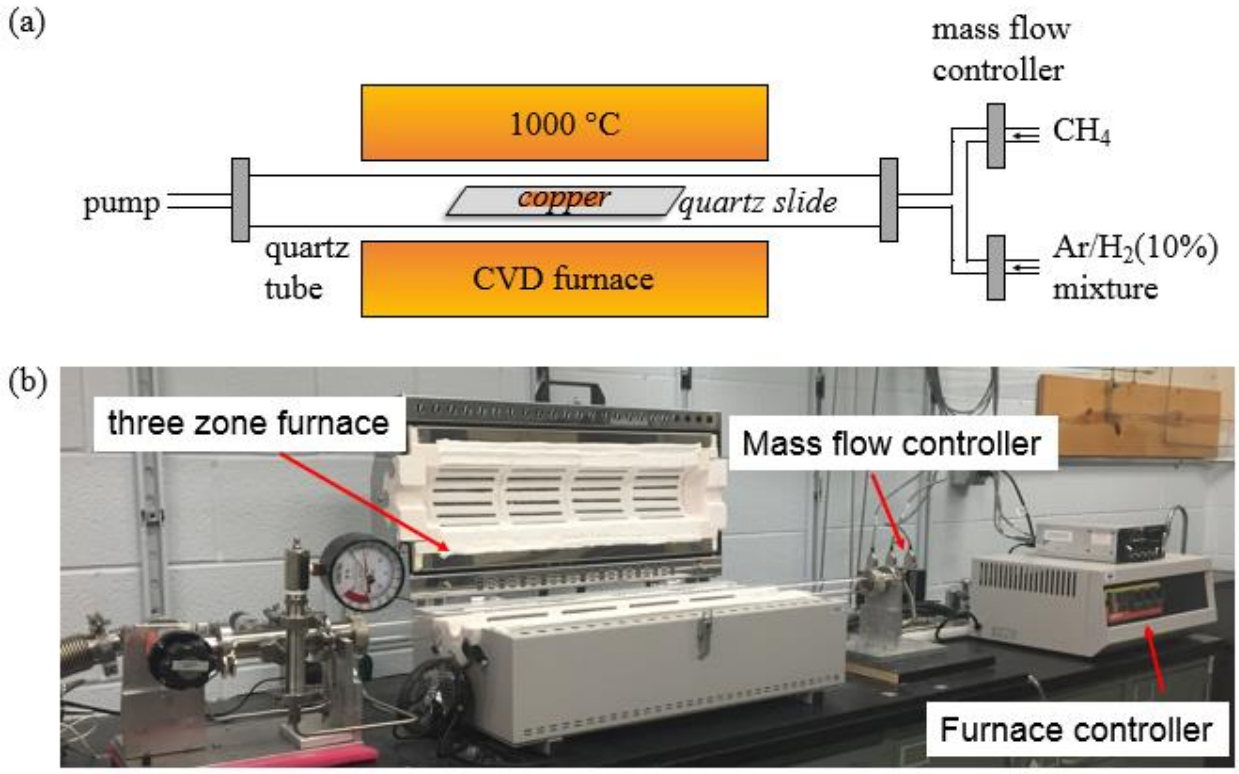


Figure 2-7. (a) Schematics and (b) an optical picture of the CVD system used in our laboratory.

Before starting the growth process, a small piece of copper foil is soaked in diluted hydrochloric acid (1 parts 97% HCl and 3 parts DI water) for ~ 5 min. This step removes native oxide layer from the Cu surface. Then it is rinsed with large amount of DI water to wash off any acid residues before blown dry by nitrogen gas. The cleaned Cu foil piece is placed on a quartz slide and inserted into the quartz tube inside a horizontal furnace (HZS 12/600, Carbolite). The

CVD system is first pumped for ~ 10 minutes to evacuate air inside all the tubes. Then the pump is turned off and the system is filled back with Ar/H_2 to atmospheric pressure. After that, the exhaust valve is opened to allow a continuous flow Ar/H_2 through the growth tube at 200 s.c.c.m. for at least 30 minutes to purge out any residual air.

Figure 2-8 shows the growth profile in our LPCVD process. Ar/H_2 flows through the growth tube continuously and constantly during the whole CVD process. Before reaching 1000 ℃, the pump is at off state and system pressure is at 1 atm. The furnace temperature is first raised to 600 ℃ at a rate of 20 ℃/min followed by a 10 min dwell time. This step further removes the native copper oxide through a redox reaction with hydrogen. Then the temperature is elevated to 900 ℃ at a rate of 20 ℃/min followed by a 10 min dwell time. This is the copper foil annealing stage. After that, the reactor temperature is raised to the growth temperature of 1000 ℃, at a rate of 10 ℃/min. Once the reactor is at 1000 ℃, the pump is turned on to bring pressure in the growth tube to 800 ~ 1000 mTorr. Then methane is introduced for graphene growth. The growth stage at 1000 ℃ usually last for 10 ~ 20 minutes depending on the flow rate of methane. After that, the furnace temperature is gradually reduced back to room temperature.

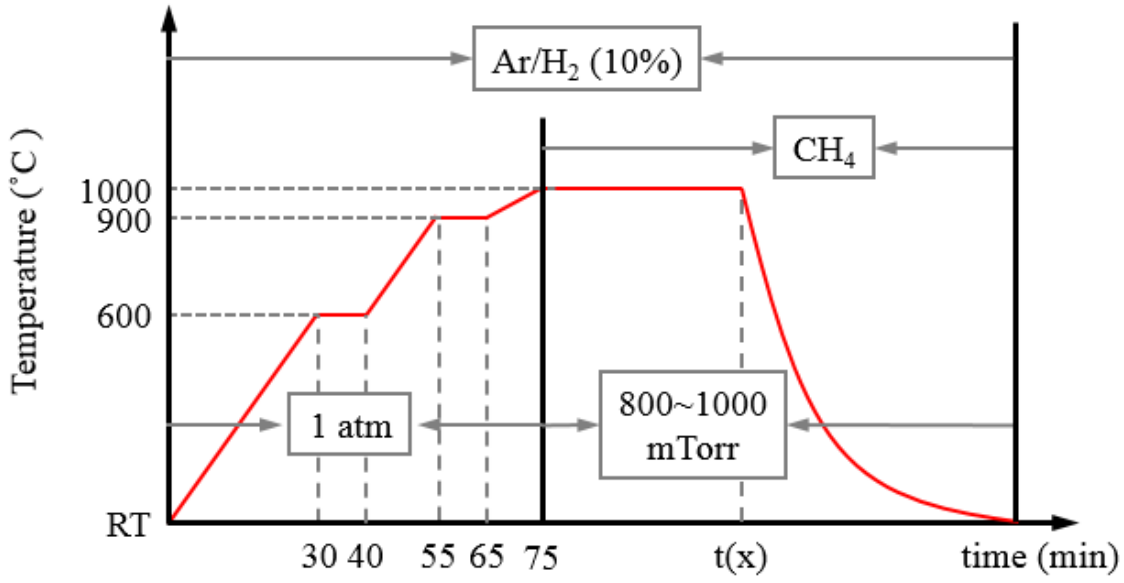


Figure 2-8. Growth profile of the tube furnace during the CVD process. The system pressure and flows of methane and $Ar/H_2(10\%)$ are also indicated on the diagram.

In our early growth recipe, we use the continuous CVD method with the methane flow rate varies between 5 s.c.c.m. to 30 s.c.c.m. We find a total methane flow of 200 s.c.c. is sufficient for graphene to fully cover the Cu surface in our CVD system. Figure 2-9 shows two SEM images of graphene on copper for methane flow of 100 s.c.c. (10 s.c.c.m. flow rate for 10 min, left) and 200 s.c.c. (10 s.c.c.m flow rate for 20 min, right). As can be seen, 100 s.c.c. methane flow is not enough for individual graphene islands to coalesce and leaves gaps in between. At 200 s.c.c. methane flow, a continuous film is formed. Because graphene growth on Cu is a self-limiting process, there is no need to flow methane more than 200 s.c.c.

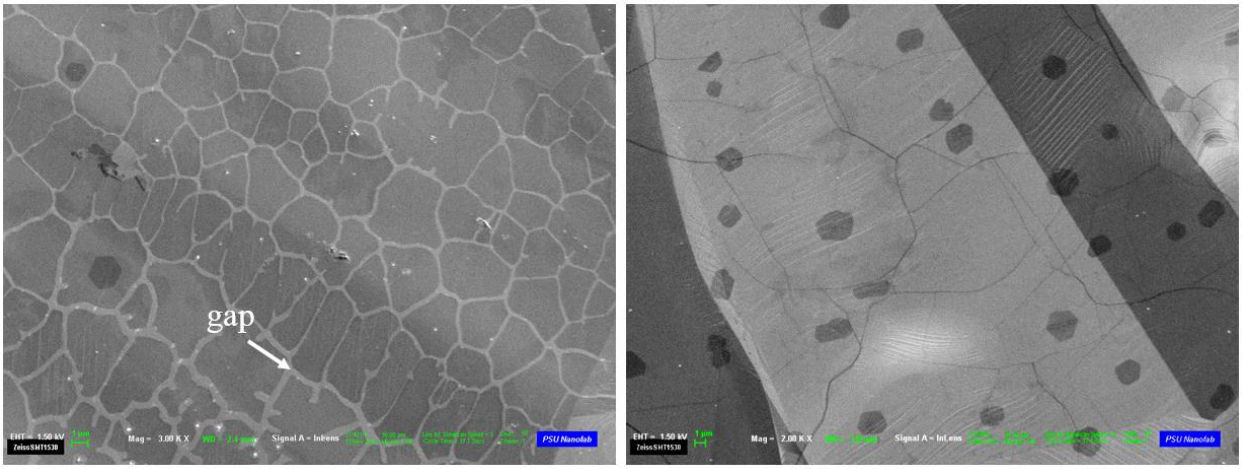


Figure 2-9. SEM images of graphene on copper from continuous CVD growth with total methane flow of 100 s.c.c. (left) and 200 s.c.c. (right). The white arrow points at copper surface that is not covered by graphene yet.

In general, we find graphene synthesized from the continuous-CVD method usually contains about 10% ~ 20% multilayers. Raman spectra from the monolayer regions show small D-band

intensity with the I_D/I_G ratio less than 0.1. Carrier mobilities of graphene field effect transistors show a distribution centered around 5,000 cm^2/Vs.[67]

2.2.2 Pulsed-CVD synthesis

Later, the dual role of hydrogen in CVD graphene synthesis is revealed by Vlassiouk *et al*.[68]. According to their experimental study, hydrogen serves as an activator of the surface bound carbon and as an etching reagent for carbon atoms. This motivates us into modifying the continuous growth recipe to take advantage the etching ability of H_2 at high temperature, i.e. 1000 ℃, to prevent the occurrence of the multilayer patches. Inspired by another paper by Han *et al*.[69], where they show the suppression of MLG patches can be achieved by introducing the methane in a pulsed fashion, i.e. pulsed-CVD method, we experiment with this idea and work out a recipe for our own CVD system.

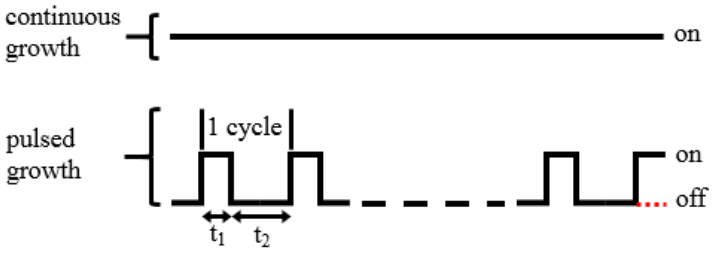


Figure 2-10. Schematics of methane flow during the graphene growth process at 1000 ℃ for continuous (top) and pulsed (bottom) CVD methods.

First, we define the growth parameters for the pulsed-CVD method. Figure 2-10 schematically compares the flow patterns of the methane for the two methods. Unlike the continuous-CVD growth, methane is alternatively turned on and off during the pulsed-CVD process. Hence, we break the whole growth process at 1000 ℃ into a number of cycles. Each

cycle contains a t_1 growth period followed by a t_2 etching period. During the growth period, methane is applied at a flow rate of f_{CH4}. Then it is cut off in the following etching period leaving only Ar/H_2 flowing though the reactor. It should be noted that the Ar/H_2(10%) is constantly applied during the growth process for both continuous- and pulsed-CVD methods. Its flow rate is denoted by f_{H2}. As will be shown later, we obtain complete suppression of the multilayer islands over a large area (hundreds of μm in lateral sizes) with optimized growth conditions, i.e. f_{CH4}, f_{H2}, t_1 and t_2.

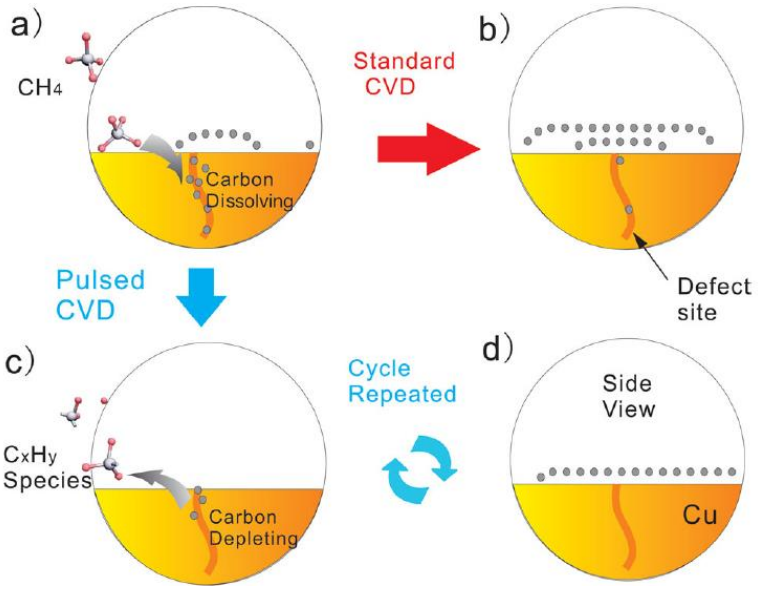


Figure 2-11 Schematic illustrations of a)&b) the formation of multilayer graphene patches near a defect site on copper during the continuous-CVD process, and c)&d) suppression mechanism in the pulsed-CVD process. Adapted from Fig. 4 of Ref. [69].

Next, we discuss the origin of the MLG formation and the suppression mechanism in pulsed-CVD method following Ref. [69]. Because the polycrystalline copper substrates (99.8% purity) always contain certain amount of defects that have large carbon solubility, carbon atoms can

diffuse into these defect sites, as shown in Fig. 2-11(a). Then, in the continuous CVD process, these carbon atoms diffuse to the copper surface and form additional graphene patches as the reactor cools down (Fig. 2-11(b)). As discussed above, H_2 can react with carbon atoms such as those at the growth front of the graphene lattice and the ones stored at the copper defect sites, through forming C_xH_y species. Hence, by cutting off the methane for a short period of time in cycles, the H_2 molecules can deplete the carbon atoms in the defect sites. If the depletion is complete, there should be no more carbon supplies for the multilayer to form. This is illustrated in Fig. 2-11(c) and (d). Another way to suppress the MLG growth is to use ultra-high purity (99.999%) copper substrates.

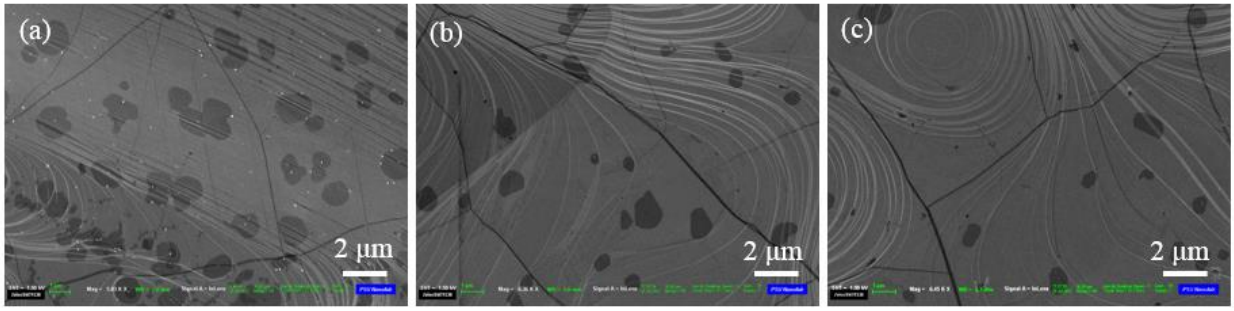


Figure 2-12. SEM images from three pulsed-CVD graphene synthesizes. From (a) to (c), the growth condition t_1/t_2 and MLG coverage are: 2min/2min, 15.7%; 1min/2min, 8.2%; and 0.5min/2.5min, 3.7%, respectively. For all three growth, methane and Ar/H_2(10%) flow rates are fixed at t $f_{CH4} = 10$ s.c.c.m. and $f_{H2} = 200$ s.c.c.m. with a total amount 200. s.c.c. methane.

As there are four growth parameters that can be controlled during the pulsed-CVD process, we first show results from growth tests where the methane and Ar/H_2(10%) flow rates are fixed at $f_{CH4} = 10$ s.c.c.m. and $f_{H2} = 200$ s.c.c.m.. Figure 2-12 show typical SEM images from three combination of t_1/t_2, i.e. (a) 2min/2min, (b) 1min/2min, and (c) 0.5min/2min. Statistical results of

the MLG average sizes and coverage percentages from multiple SEM images for each growth are: (a) (0.62±0.58) μm^2, (15.7±2.4) %; (b) (0.79±0.68) μm^2, (8.2±2.1) %; (c) (0.37±0.37) μm^2, (3.7±1.1) %. The total amount of methane applied is kept at 200 s.c.c. for all three growth conditions. As can be seen from the graphs and statistical results, both the average size and coverage of MLG patches progressively reduce with shorter t_1 and longer t_2. We also experiment with the flow rate of methane by keeping t_1 and t_2 constant.

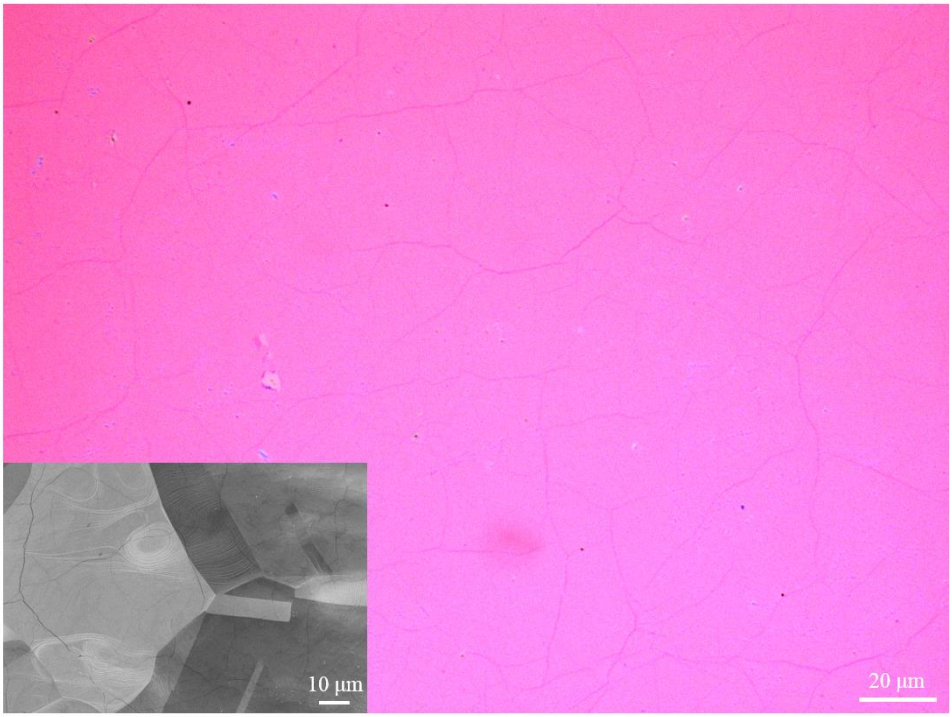


Figure 2-13. An optical image of pulsed-CVD graphene transferred on SiO_2(290nm)/Si substrate. No MLG patches are visually observed. Inset shows an SEM image of graphene from the same growth batch.

After many trials, we are able to produce MLG-free monolayer graphene films using a growth recipe of $t_1 = 30$ s, $t_1 = 60$ s, $f_{CH4} = 5$ s.c.c.m., $f_{H2} = 200$ s.c.c.m. and 80 growth cycles. Figure 2-13 is an optical image of the pulse-CVD graphene transferred onto

SiO_2(290nm)/Si substrate. The color contrast of the graphene film is uniform and no MLG patches are found visually. The size of the graphene film is 180 μm×250 μm. The inset shows an SEM image of graphene on copper from the same growth batch at a smaller scale. No MLG patches are observed either.

This result confirms the etching ability of hydrogen at high temperatures, i.e. 1000 ℃. So we made another modification to the continuous CVD process by adding a post-growth etching step, to also achieve the multilayer-free growth. This is realized by cutting off the methane flow immediately after the graphene film is formed while still maintaining the 1000 ℃ growth temperature so that the carbon atoms at the defect sites are still dissolved. Then the hydrogen molecules can deplete them through forming hydrocarbon species. Figure 4-14 shows a schematic of this modified CVD process and an SEM image of the growth result with the absence of multilayer graphene islands. The growth recipe is 5 s.c.c.m. CH_4, 200 s.c.c.m Ar/H_2(10%), 40 min continuous CH_4 flow followed by 80 min H_2 etching at 1000 ℃.

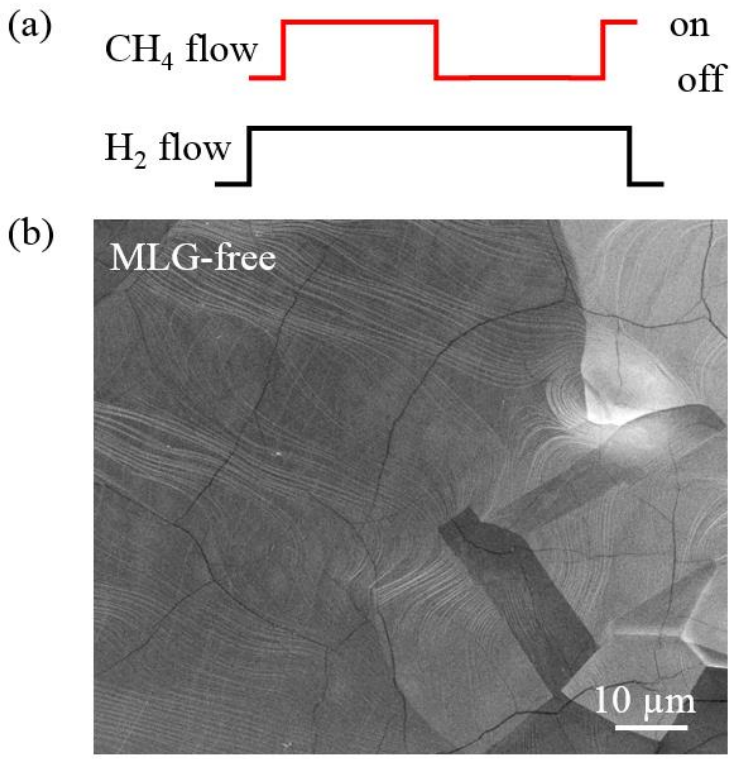


Figure 2-14. (a) Schematics of the modified CVD process with the post-growth etching step. (b) An SEM image of multilayer-free graphene on copper.

So by utilizing the etching ability of hydrogen either during or post the graphene growth, the multilayer islands that are commonly observed in standard CVD growth can be fully suppressed. The significance of a multilayer-free graphene synthesis mainly lies in the potential application aspect of graphene where uniformity plays a critical role in mass production at high volume. For example, one of the promising applications is using graphene as transparent and flexible conducting electrodes.[70, 71] Since both the electrical conductivity and transmittance (~ 2.3% white light absorption rate per layer[15]) are layer number dependent, the presence of any multilayer patches will cause fluctuation in device performance, which must be avoided from the view point of industrial production.

2.3 Fabrication of CVD-graphene field effect transistors (GFETs)

To further evaluate the quality of graphene films grown by both continuous- and pulsed-CVD methods, we fabricate arrays of GFETs and perform electrical tests on these devices. This section describes the device fabrication procedures, including *transfer, photolithographic patterning, etching, metal deposition, and passivation.*

Polymer-assisted transfer.

Step 1 (Fig. 2-15(a)): Cut graphene-covered copper foils into desired shape and tape all edges to a spin wafer. Make sure the piece lies as flat as possible on the wafer. Then spin-coat with 495K A3 PMMA (2000 ~ 4000 r.p.m., 30 sec), followed by hot-plate baking (95 ℃, 1 min). The baking reduces solvent concentration and increases adhesion of the PMMA film with graphene. Then, carefully peel off the tapes to release the foil from the spin wafer. Make sure it is still flat after the peel-off.

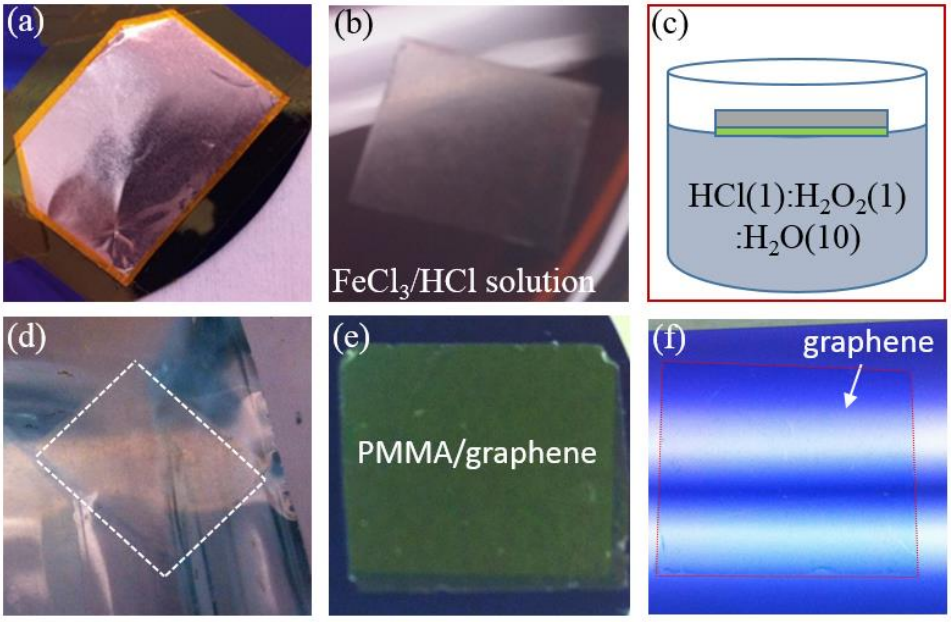


Figure 2-15. Polymer-assisted transfer process for CVD graphene.

Step 2 (Fig. 1-15(b)): Copper etchant CE-100 (ferric chloride ($FeCl_3$), hydrochloride acid (HCl)) is used to etch away the Cu foil. The etchant solution is preheated to 40 ℃ for optimal reaction rate. It is important to remove the copper completely as even trace amount of it can degrade the device quality through scattering in carrier transport. In our initial trials, we experiment with extended etch time. However, we find long time etching increases the defectiveness of the transferred graphene films. Figure 2-16 shows the Raman I_D/I_G ratio of transferred graphene films for Cu etch time of 15, 40 and 60 minutes. As discussed in Section 2.1, higher I_D/I_G indicates more defects in graphene. Hence, long etching time is not a good solution. However, the etching time should be at least 15 minutes for Cu foil to be visually dissolved completely.

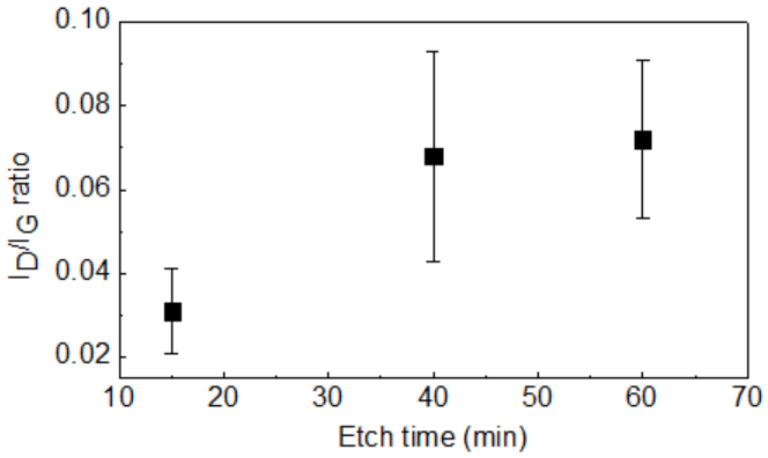


Figure 2-16. I_D/I_G from monolayer regions of CVD graphene transferred on SiO_2/Si substrate with 15min, 40min, and 60min Cu etch time during the transfer process.

Step 3 (Fig. 2-15(c)): In order to remove any trace amount of Cu residues, we add this diluted SC-2 cleaning step to our initial transfer recipe. This step is the only modification we make. The

solution is made by mixing 1 part of aqueous H_2O_2 (hydrogen peroxide, 30%), 1 part of aqueous HCl (hydrogenchloric acid, 39% by weight), and 10 parts of DI water. Before transferring into the SC-2 solution, we usually transfer the PMMA/graphene film into clean DI water first to clean off most of the etching solution residues for ~ 10 min. The cleaning time in dilute SC-2 is usually 10 minutes. After that, PMMA/graphene film is transferred into fresh DI water and wait for 10 minutes to clean off SC-2 solution residues. This step is usually repeated twice.

Step 4 (Fig. 2-15(d&e)): The PMMA/graphene film is then fished out from DI water using a cleaned SiO_2(290nm)/Si wafer with pre-patterned alignment markers for subsequent photolithography. Cleaning of the SiO_2/Si wafer is involves soaking in Nanostrip (90 % sulfuric acid) at 60 ℃ for at least half an hour followed by large amount DI water rising first and then sonication in DI water for 5 min. This treatment cleans the SiO_2 surface and makes it highly hydrophilic, which is critical for the subsequent device fabrication process. After transfer, the PMMA/graphene film is left to dry naturally for ~ 12 hours.

Step 5 (Fig. 2-15(f)): As the last step, the PMMA top layer is removed by soaking in Acetone for ~10 min followed by IPA rising and then blow dry.

Before starting the photolithography step, the transferred graphene film must be annealed at 450 ℃ in Ar/H_2(10%) (500 s.c.c.m. flow rate) using a tube furnace. The annealing time should be no less than 2 hours. This treatment drives away most of the water moistures trapped between graphene and SiO_2 and increases bonding with the SiO_2 surface. Without this step, transferred graphene film will have a high probability of flying away in the subsequent spin-coating process.

Photolithography patterning and etching

We use photolithography (GCA 8000 Stepper) to pattern the GFET arrays in two steps: a) graphene channel patterning; and b) contact electrode patterning.

Graphene channel patterning. First, the graphene/SiO_2/Si wafer is spin-coated with photoresist 3012 (4000 r.p.m., 45 sec) followed by hot-plate baking (95 ℃, 1 min). Then the wafer is transferred into the photolithography tool for UV light exposure. The exposure time is 0.55 sec for the GCA 8000 Stepper. CD-26 is used for photoresist develop. The develop time starts with 30 seconds, followed by DI water soaking and rinsing before blow dry by N_2 gas. If the exposed photoresists are not dissolved completely, then repeat this step a few times until the exposed regions are visually clean.

Oxygen plasma etching. Oxygen plasma is used to etch the graphene film into arrays of rectangular bars in a Plasma-Therm Versalock 700 system. The etching recipe is 25 s.c.c.m O_2, 20 mTorr pressure, 100 W power. Etching time varies each time depending on the thickness of the photoresist residual layer (a few nm). We usually start with 10 seconds and add additional time with 10s increment until all the exposed graphene regions are etched away. Then the photoresist covering the graphene bars are dissolved away in Nano PG Remover.

Contact electrode patterning. In this step, a bilayer photoresist stack is needed. First, the wafer is spin-coated with photoresist LOR 2A (4000 rpm, 45 s), followed by hot-plate baking (170 ℃, 5 min). Then photoresist 3012 is spin-coated and then baked at 95 ℃ for 1 min. The exposure time is the same 0.55 sec. Also, same develop procedure is used after the exposure.

Metal deposition and lift-off.

Ti/Au (5nm/45nm) stack is deposited as metal contacts using a Lab-18 system (Kurt J. Lesker). The deposition rate for Ti and Au are 0.5 Å/s and 1.5 Å/s, respectively. For metal lift-

off, the wafer is soaked in hot PG Remover solution (60 ℃) until all parts of the metal film except the contact electrodes are lifted off.

Passivation.

Finished devices are passivated with a layer of 30nm HfO_2 to prevent ambient doping to the graphene channels. The HfO_2 layer is grown by atomic layer deposition (ALD) at 110 ℃. Detailed description of the ALD process is available in Appendix A.3.

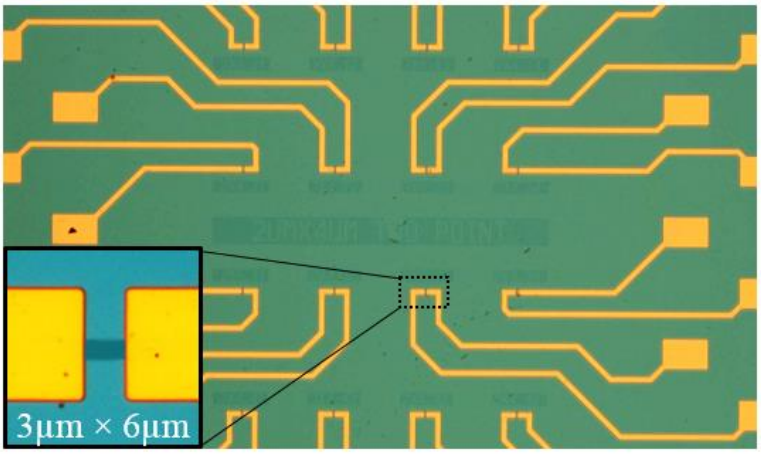


Figure 2-17. An optical image of GFET arrays with 16 two-terminal transistors. Inset is an SEM (false colored) zoom-in of the graphene channel. Image courtesy of Dr. Bei Wang.

Figure 2-17 is an optical image of one device die consisting 16 two-terminal GFETs. The inset is a zoom-in optical image of one device showing a 3 μm wide, 6 μm long graphene channel.

2.4 Electrical characterization of GFETs

2.4.1 Two-terminal electrical measurement set-up

GFETs are fabricated using graphene films grown by the continuous- and pulsed-CVD methods. Carrier density in the graphene channel is modulated by the SiO_2/Si backgate structure, which has a gating efficiency $\alpha = 7 \times 10^{10}\ /\mathrm{cm}^2$ for 290nm±5% SiO_2 (NOVA Electronic Materials). All devices are measured in ambient environment using a probe station.

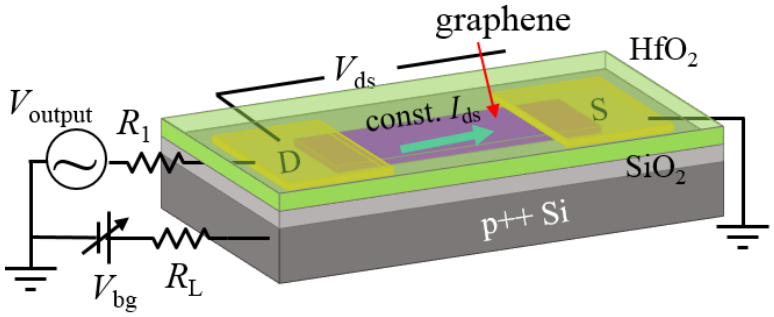


Figure 2-18. Schematics of the two-terminal GFET structure and the electrical measurement configuration using a constant current excitation method.

We employ a low-frequency (i.e., 47Hz) standard Lock-in technique and a constant current excitation method to measure the gate-dependent conductance. Figure 2-18 shows a schematic of the measurement set-up. A GFET device is connected in series with a large resistance resistor R_1. The maximum GFET resistance with a 3μm ×6μm graphene channel is usually less than 10 kΩ. In order to generate a constant current source, R_1 needs to be much larger than 10 kΩ such that the gate-modulated R_{GFET} change is only a negligible perturbation to the total resistance of the circuit. Hence, we use 100 MΩ for R_1. V_{out} is the output a.c. voltage from the Lock-in instrument (SR830, Stanford Research Systems) and is set at 5V. The corresponding current is then $I_{ds} =$ 50 nA. The backgate voltage V_{bg} is applied to the highly doped silicon gate. By simultaneously

measuring the voltage difference V_{ds} across the source (S) and drain (D) electrodes, we obtain the two-terminal gate-dependent conductance as,

$$G(V_{\mathrm{bg}}) = \frac{I_{\mathrm{ds}}}{V_{\mathrm{ds}}(V_{\mathrm{bg}})} \tag{2.1}$$

A typical $G(V_{\mathrm{bg}})$ curve is shown in Fig. 2-19(a). The black and red arrows indicate the gate sweep directions. The minimum conductance point V_{D} of the downward sweep is shifted ~ 15 V toward the negative side from that of the forward sweep. The direction of the hysteresis indicates capacitive coupling at play as shown in Fig. 2-19(c).[72] This is likely due to the presence of a thin water dipole layer underneath graphene, which is usually introduced during the transfer step. The effect is that it enhances the local electric field near graphene and increases the density of the majority carriers.[72-74] Besides capacitive coupling, there is another coexisting charge transfer mechanism, which leads to minimum conductance point shift in the opposite direction.[72]

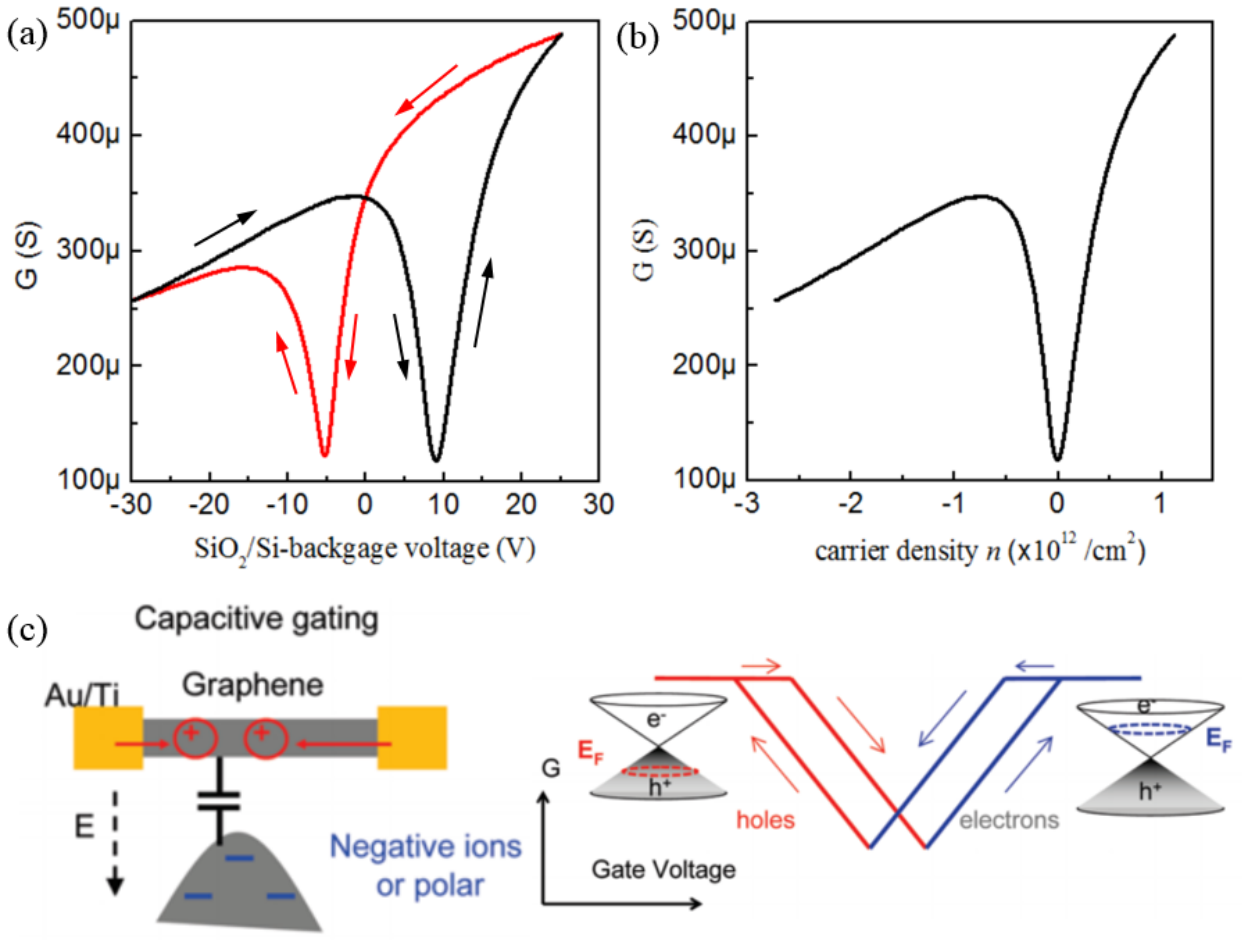


Figure 2-19. (a) A typical hysteretic transfer curve of GFET. (b) The same forward Vbg-sweep conductance curve in (a) plotted as a function of carrier density. (c) Schematics of the capacitive gating model and the resulting hysteresis direction. Adapted from Ref. [73].

For experiments or applications where accurate determination of the real V_D is critical, such as graphene biosensors[23], the elimination of hysteresis is important and necessary. This can be done using a pulsed-gating technique. However, in our measurements, hysteresis is not an issue because it does not affect the determination of carrier mobility, which only depends on the shape of the curve near V_D. Hence, in the following discussion, we use $G(V_{bg})$ from the forward gate sweep.

Next, we use Fig. 2-19(b) to describe the characteristic features of the transfer curve. It re-plots the black curve in Fig. 2-19(a) as a function of carrier density. The conduction is ambipolar with a finite minimum conductance at $n = 0$. Electron and hole branches have the same curve shape for $|n| < 0.5 \times 10^{12}$ /cm^2. The asymmetry at high carrier densities is due to p-n junction resistance and will be discussed in Section 2.4.3. The conductance shows a linear dependence on n at small carrier densities. As n further increases, the conductance deviates from the linear trajectory and bends towards lower values. The symmetry of the conductance curve around $n = 0$ or V_D indicates that the carrier mobilities for electrons and holes are close. In the next section, we will make an introduction to the charged-impurity scattering theory and a practical formula for carrier mobility extraction.

2.4.2 Charged-impurity scattering theory

As is the case of our GFETs, the most common device structure has graphene supported on a backgate structure, such as SiO_2/Si, where the properties of the dielectric layer significantly affect carrier transport in graphene. In theory, carrier transport in graphene not too close to the Dirac point is diffusive and follows the simple Drude model,

$$\sigma = |n|e\mu \tag{2.2}$$

Here σ is the graphene sheet conductance, n is the carrier density, and μ is the carrier mobility. At the Dirac point, $n = 0$, which leads to zero conductivity as shown by the black curve in Fig. 2-20. As n increases, σ follows a linear increasing trend.

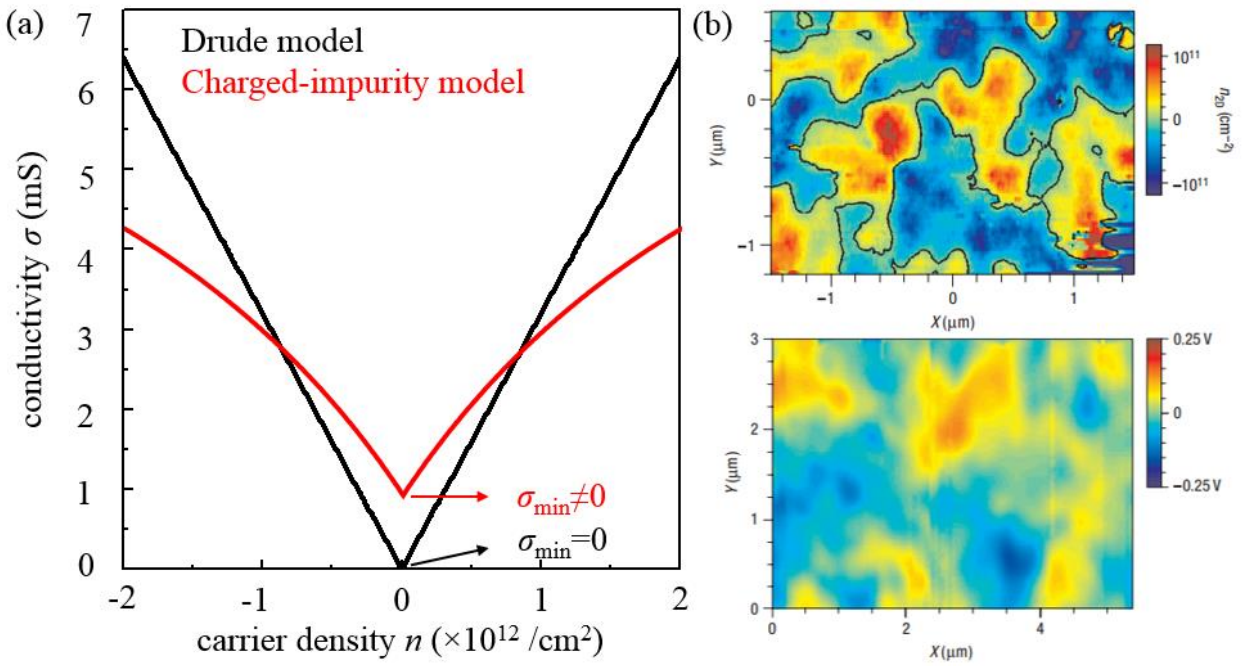


Figure 2-20. (a) Graphene sheet conductance vs carrier density from the Drude model (black line) and the charged-impurity model incorporating short-range scattering (red curve). (b) A color map of the spatial density variation in graphene flake (top) and a surface potential map of the bare silicon oxide surface near the graphene flake in the top graph. Adapted from Fig. 3 of Ref. [75]

However, the experimentally measured $\sigma(n)$ always possesses a finite minimum plateau, σ_{min}. In realistic samples studied here, this finite σ_{min} originates from charged impurity scattering and the resulting electron-hole (e-h) puddles.[76] The e-h puddles have been experimentally observed in graphene by Martin *et al.*[75] using a scanning single-electron transistor. Figure 2-20(b) shows a spatial density map in graphene (top) and a map of the surface potential measured above the bare silicon oxide surface near the graphene flake. Another characteristic is bending at high carrier densities even though the linear relationship is still preserved for small carrier densities close to $n = 0$. These two characteristics are shown by the red curve in Fig. 2-20(a).

Adam *et al*. [76] proposed an analytical model based on charged-impurity scattering to quantify both the width and magnitude of the minimum conductivity plateau, as expressed by

$$\sigma(n-\overline{n}) = \begin{cases} \frac{20e^2}{h}\frac{n^*}{n_{\text{imp}}} & \text{if } n-\overline{n} < n^* \\ \frac{20e^2}{h}\frac{n}{n_{\text{imp}}} & \text{if } n-\overline{n} > n^* \end{cases} \tag{2.3}$$

Here n_{imp} is the density of the charged impurities. n^* and $\overline{n}$ are two density quantities depending on n_{imp}.

The charged impurities considered in formulating Eq. (2.3) act as scattering centers through long-range Coulomb interactions. Their impacts on graphene transport are two folds: a) create a minimum plateau; b) limit carrier mobility. However, as Eq. (2.3) shows, σ still linearly depends on n at high carrier densities. Hence, other scattering mechanisms need to be considered. Weak short-range scatters, such as physisorbed neutral molecules, contribute a constant resistivity ρ_{short}.[77] It is in series with the resistivity deduced from Eq. (2.3) and leads to sublinearity at high carrier densities.

Empirically, the conductivity from charged impurity scattering can be expressed as

$$\sigma_{\text{long}} = ne\mu_{\text{FE}} + \sigma_{\text{res}} \tag{2.4}$$

Here σ_{res} is the residue conductivity depending on n_{imp} and is usually very small. μ_{FE} is the field-effect mobility and is given by

$$\mu_{FE} = \frac{20e^2}{h}\frac{1}{n_{\text{imp}}} \tag{2.5}$$

Hence the complete model incorporating both long-range and short-range scatterings can be express as

$$\rho = \frac{1}{\sigma} = \frac{1}{\sigma_{\text{long}}} + \rho_{\text{short}} \tag{2.6}$$

For two-terminal transistors, the contact resistance R_c cannot be separated from the total resistance, but is often treated as a constant. The carrier density is given by

$$n = \alpha \times \left|V_{\mathrm{bg}} - V_{\mathrm{D}}\right| \tag{2.7}$$

where V_{D} is the gate voltage at the minimum conductance point, also called charge neutrality point (CNP). α is the gating efficiency in units of cm^{-2} and is given by

$$\alpha = \frac{\varepsilon_0 \varepsilon}{et} \tag{2.8}$$

where ε_0, ε and t are the vacuum permittivity, gate dielectric constant, and thickness of the dielectric layer, respectively.

The practical fitting equation used for mobility fitting is then give by

$$G = \frac{1}{\frac{L}{W}\rho + R_c} = \frac{1}{\frac{L/W}{e\alpha\left|V_{\mathrm{bg}} - V_D\right|\mu_{\mathrm{FE}} + \sigma_{\mathrm{res}}} + R_c'} \tag{2.9}$$

where $\frac{L}{W}$ is the geometry factor of the graphene channel and

$$R_c' = \frac{L}{W}\rho_{\mathrm{short}} + R_c \tag{2.10}$$

is the modified contact resistance that contains graphene channel resistance due to short-range scattering and the contact resistance.

2.4.3 Discussion on electron-hole asymmetry at high carrier densities

As Fig. 2-19(a) shows, there is a large electron-hole asymmetry in $G(V_{\mathrm{bg}})$. The origin of the hysteresis is initially considered as due to the difference in charged-impurity scattering cross-sections between electrons and holes.[14] Later, it is found by Huard *et al*.[78] that the asymmetry is due to the formation of p-n junctions between the channel graphene and that underneath the metal contacts. Due to charge transfer, graphene in contact with the contact metal

is pinned to be either p type or n type depending on the metal workfunction. For example, it is found that graphene contacted by palladium is pinned to p-type.[78] This result is reasonable as the workfunction of Pd (~ 5.1 eV) is higher than the predicted workfunction of graphene (4.5 eV[79]) As both carrier density and type are modulated by the gate voltages, the channel graphene can be switched between p type and n type. Hence, if the graphene in the contact region is pinned to p-type, a p-n junction will form when the channel graphene is modulated to n-type. And a p-p junction will form for p-type channel graphene. This is the case observed in graphene devices reported by Huard *et al*.[78]

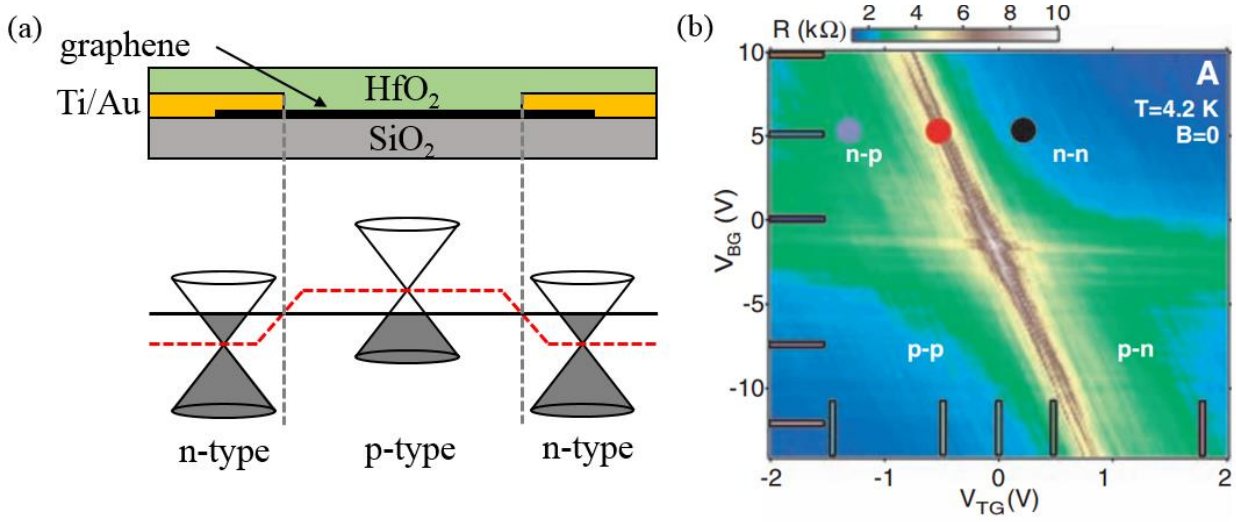


Figure 2-21. (a) Schematics of the p-n junction formation at negative backgate voltages. (b) A color map of graphene p-n junction resistance. Adapted from Fig. 2 of Ref. [80].

The e-h asymmetry observed in our GFETs has high resistance at large negative gate voltages. This indicates a p-n junction is present when the graphene channel is p type, thus making the graphene underneath the contact metal to be n-type. This situation is illustrated in Fig. 2-21(a). Such pinning result is expected as the workfunction of Ti and Au are $\Phi_{Ti} \approx 4.3$ eV

and $\Phi_{Au} \approx 5.1$ eV, respectively. The thickness of the Ti layer is at least 5 nm. Graphene should then primarily see the workfunction of Ti which tends to pin graphene Fermi level into the conduction band, i.e. n-type. This is also consistent with the theoretical study by Giovannetti *et al*.[79] where they find the transition between p-type and n-type doping in graphene happens for a metal workfunction of ~ 5.4 eV. Besides, the resistance difference between the electron and hole conduction branches is in the few kΩ range, which is also consistent with the reported graphene p-n junction resistance magnitude, as is shown in Fig. 2-21(b)[80].

2.4.4 Electrical test results of GFETs

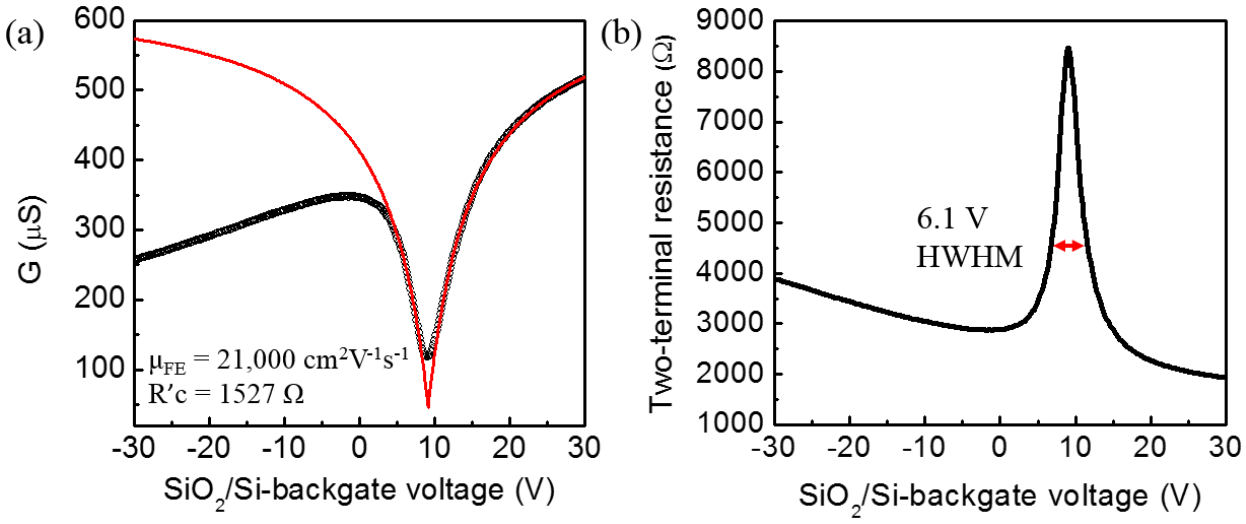


Figure 2-22. (a) An example of applying Eq. (2.9) to a $G(V_{bg})$ curve. μ_{FE}= 21,000 cm^2/Vs and Rc'=1527 Ω. (b) Same curve in (a) plotted in resistance for measurement of the FWHM. The narrow 6.1 V width further attests to the high mobility obtained in (a).

GFET carrier mobilities are obtained by fitting Eq. (2.9) to $G(V_{bg})$ curves from forward gate sweep. Because the e-h symmetry near V_D, we will not differentiate the carrier mobilities

between electrons and holes. This is also supported by the fitting result shown in Fig. 2.22(a). First we choose a segment of data on the electron branch as input to Eq. (2.9), then the fitted curve is extended to the whole gate voltage range. As can be seen, the red fitting curve overlaps very well with the hole branch from $V_{bg} = +3$ V to close to V_D. This indicates the fitted mobility value also works for holes. For this particular device, $\mu_{FE} \approx 21{,}000\ \mathrm{cm}^2/\mathrm{Vs}$ and $R'_c \approx 1.5\ \mathrm{k\Omega}$. We also measure the full-width-of-half-maximum (FWHM) of $R(V_{bg})$ curve for each device to check with the mobility. This is because the narrower the FWHM is, the higher the mobility according to Eq. (2.9). Figure 2-22(b) plots the same data in $R(V_g)$ format, and the FWHM is measured to be ~ 6.1 V. This narrow width further attests to the high carrier mobility obtained. The same analysis procedures are applied to all GFETs.

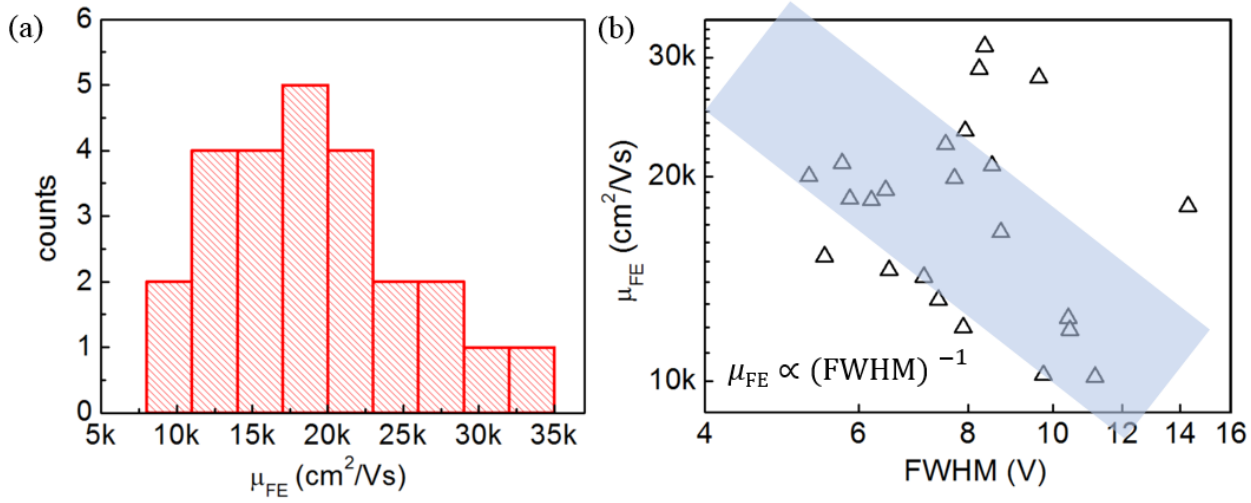


Figure 2-23. (a) Histogram distribution of field effect mobility μ_{FE} obtained from a total of 25 GFETs. (b) Log-log plot of μ_{FE} vs FWHM.

Our mobility analysis from many devices made from both continuous- and pulsed-CVD graphene do not show significant difference. This is more or less expected as the advantage of

pulsed-CVD mainly lies in the suppression of the multilayer graphene. So we do not distinguish them in the statistical distribution of μ_{FE} shown in Fig. 2-23. For a total of 25 devices, μ_{FE} centers on 18,000 cm^2/Vs. Figure 2-23(b) is a log-log plot of μ_{FE}vs FWHM. According to the charged impurity model and Eq. (2.9), μ_{FE} should approximately be proportional to the inverse of FWHM, i.e. $\mu_{FE} \sim (\mathrm{FWHM})^{-1}$. The slop of the light blue band is -1 in the log-log plot. As can be seen, the data follows the trend well. So both the high mobility and narrow FWHM confirm the high quality of our GFETs. In fact, they are even comparable to the best SiO_2-supported devices made from exfoliated graphene[81], and are much higher than $\mu_{\mathrm{FE}} < 5{,}000\ \mathrm{cm}^2/\mathrm{Vs}$, commonly reported in the literatures for CVD graphene transistors[82-84]. We suspect the high mobility comes from a much cleaner graphene interface as a result of the diluted SC-2 cleaning.

Chapter 3

Properties of mono- to few-layer TMDC and compounds

In this chapter, we discuss various material characterization results from semiconducting transition metal dichalcogenides (TMDC), including MoS_2, WS_2, and WSe_2. In Section 3.1, we describes the chemical vapor transport (CVT) synthesis method of WSe_2 crystals. Section 3.2 will be devoted to sample quality characterizations by various techniques such as Transmission Electron Microscopy (TEM), X-ray Diffraction (XRD), Raman and Photoluminescence (PL) spectroscopy. In Section 3.3, we discuss characterization results from atomic force microscopy (AFM) and other AFM-based techniques, such as Kelvin probe force microscopy (KPFM) and scanning thermal microscopy (SThM). We study the morphology, workfunction, and thermal conductivity of exfoliated sheets from TMDC and their alloys.

3.1 TMDC synthesis

Our WSe_2 samples are obtained through collaborations with three laboratories. They all use a chemical vapor transport technique to synthesize bulk crystals. Below are descriptions of the CVT process as obtained from the students who perform the growth.

WSe_2 crystals grown by Minh An Nguyen from Prof. Thomas Mallouk's group at the Pennsylvania State University. Their CVT technique first synthesizes WSe_2 powder by heating a mixture containing stoichiometric amounts of tungsten (Acros Organics 99.9%) and selenium (Acros Organics 99.5+%) together at 1000^{o}C for 3 days in an evacuated and sealed quartz ampoule (10 mm ID, 12 mm OD, 150 mm length). The mixture was slowly heated from room temperature to 1000^{o}C for 12 hours to avoid any explosion due to the strong exothermic reaction. Chemical vapor transport was then used to grow WSe_2 crystal from the powder using iodine (Sigma-Aldrich, 99.8+%) as the transport gas at 2.7 mg/cm^3 for 10 days in an evacuated and

sealed quartz ampoule (10 mm ID, 12 mm OD, 127 mm length). The source and growth zones were kept at 995ºC and 851ºC, respectively. The resulted crystals was washed with hexane and dried in vacuum to remove any residual iodine and hexane.

WSe_2 crystals grown by Daniel Rhodes from Prof. Luis Balicas' group at Florida State University. Their CVT technique uses either iodine or excess Se as the transport agent. 99.999% pure W powder and 99.999% pure Se pellets were introduced into a quartz tube together with 99.999% pure iodine. The quartz tube was vacuumed, brought to 1150 ºC, and held at this temperature for 1.5 weeks at a temperature gradient of < 100 ºC. Subsequently, it was cooled to 1050 ºC at a rate of 10 ºC per hour, followed by another cool down to 800 ºC at a rate of 2 ºC per hour. It was held at 800 ºC for 2 days and subsequently quenched in air.

Our recent CVT-grown WSe_2 crystals are synthesized by Michael Koehler and Dr. Jiaqiang Yan from Prof. David Mandrus' group at University of Tennessee.

In this dissertation, we identify CVT-grown crystals from the above three laboratories as PSU-MX_2, FSU-MX_2, and UT-MX_2 according to their affiliations. We also make MoS_2 transistors using CVD-synthesized monolayer triangles grown by Kehao Zhang from Prof. Joshua Robinson's laboratory. For the MoS_2 device, we label is as CVD-MoS_2.

3.2 TMDC crystal quality characterizations

3.2.1 Transmission electron microscopy (TEM) characterization

Transmission electron microscopy (TEM) is often considered as the ultimate analysis technique due to its ability in providing detailed information about the internal composition of a specimen and extremely high magnifications, e.g. atomic resolution. In a basic TEM operation, a beam of electrons is focused and accelerated to high energies (a few hundred keV) and then directed to pass through an ultra-thin specimen. Due to interactions with internal structures of the

specimen, transmitted electrons can be used to analyze various aspects of the specimen, such as crystal structure, defect formation and elemental analysis.

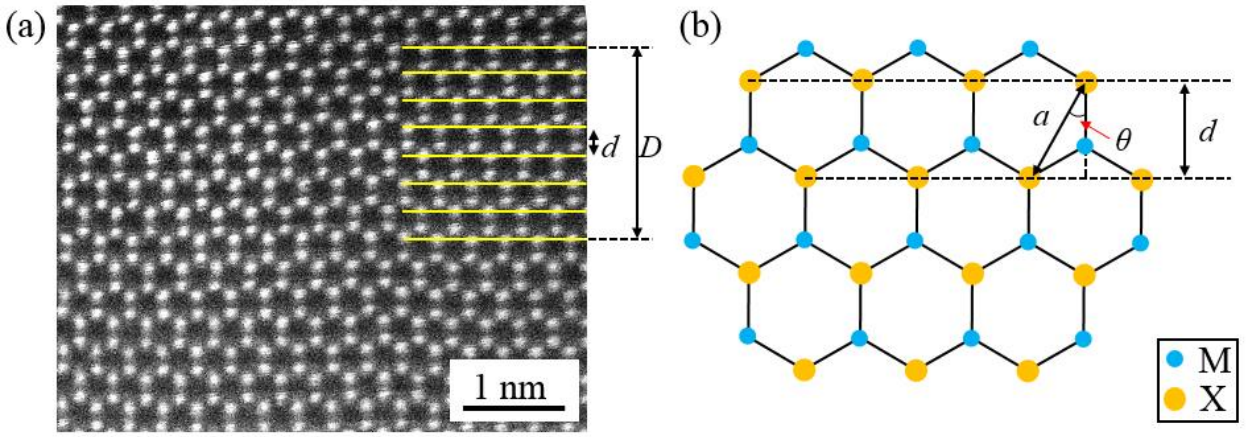


Figure 3-1. (a) High-resolution HAADF TEM image of a CVT-grown FSU-WSe_2 crystal and imaged along the [110] plane of both W and Se atoms. The hexagonal lattice confirms the 2H crystal structure. Image courtesy of Daniel Rhodes. (b) Schematics showing the relation between in-plane lattice constant and spacing d, i.e. $d = a \times \cos(\theta)$.

Figure 3-1(a) shows a high-angle annular dark field (HAADF) TEM image of an FSU-WSe_2 crystal along the [110] plane with both W and Se atoms. A clear hexagonal lattice confirms the 2H crystal structure and its high crystallinity. From this TEM image, we obtain the in-plane lattice constant a. The parallel yellow lines in Fig. 3-1(a) mark the spacing d between rows of same atoms, W or Se. The total spacing for eight rows, i.e. $7d$, is measured to be $D = 18.69$ Å according to the scale bar. So $d = 2.67$ Å. Figure 3-1(b) shows the mathematical relationship between a and d, and it is given by

$$d = a \times \cos(\theta) \tag{3.1}$$

where $\theta = 30°$ for the hexagonal lattice. Using $d = 2.67$ Å, the in-plane lattice constant of WSe_2 is obtained to be 3.08 Å, which is in good agreement with literatures.[85]

3.2.2 X-ray diffraction (XRD) characterization

An X-ray diffraction pattern is generated when a beam of incident x-rays are diffracted into specific directions by different lattice planes in a crystal, as is schematically shown in Fig. 3-2. θ is the angle between the incident x-ray beam and the lattice. In order to form a diffraction spot, the reflected beam arrays need to satisfy the constructive interference condition given by the Bragg's law:

$$2d \times \sin(\theta) = \lambda \tag{3.2}$$

where d is the spacing between two adjacent diffracting planes. λ is the wavelength of incident x-rays. Hence, XRD is a useful technique in determining the lattice structure of crystalline samples.

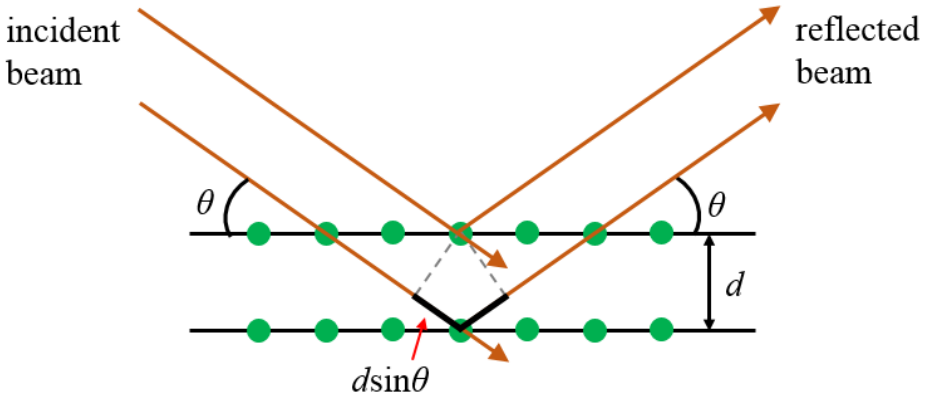


Figure 3-2. Schematics of x-ray diffraction process.

Figure 3-3 shows an x-ray diffraction (XRD) pattern of the PSU-WSe_2 crystals. The in-plane and out-of-plane lattice constants a and c can be obtained from any two peaks from the spectrum.

First, the spacing *d* of crystal planes corresponding each peak is calculated using Eq. (3.2). The x-ray wavelength is $\lambda = 0.154$ nm from copper K_α lines. Then the two lattice constants can be obtained from the following formula[86, 87]

$$\frac{1}{d^2} = \frac{4}{3}\left(\frac{h^2 + hk + k^2}{a^2}\right) + \frac{l^2}{c^2} \tag{3.2}$$

Here (*h k l*) are the Miller indices. Using the (0 0 2) and (1 0 0) peaks, we obtain $a = 3.28$ Å and $c = 12.95$ Å. This result agrees well with prior reports on the crystal structure of 2H-WSe_2.[88]

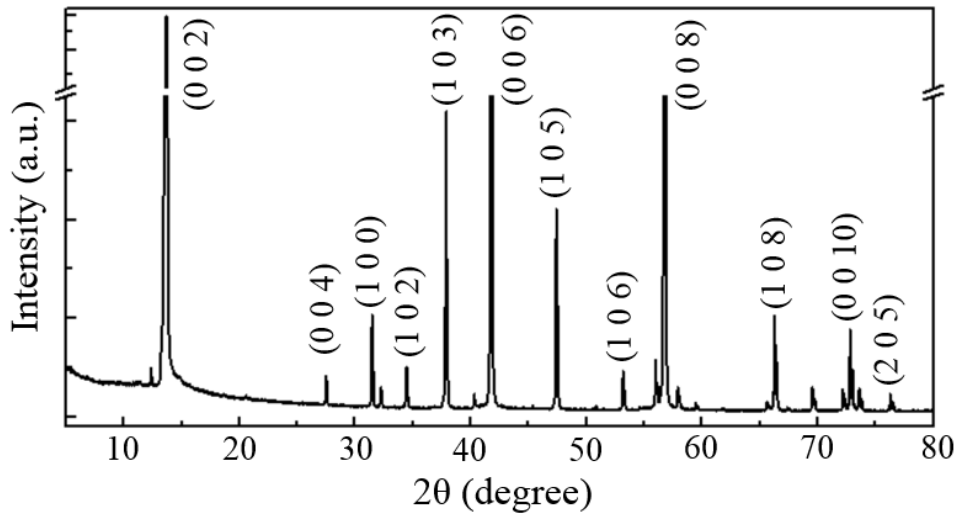


Figure 3-3. XRD spectrum of a CVT-grown PSU-WSe_2 crystal measured with the Kα line of copper. The peaks are indexed by Miller indices. The in-plane and out-of-plane lattice constants are a=3.28 Å and c=12.95 Å. Image courtesy of Minh An Nguyen.

3.2.3 Raman spectroscopy characterization of WS_2

Similar to graphene, resonant scattering is also present in the TMDC material, resulting in a plethora of Raman-active modes. It was found by Berkdemir *et al*.[89] that there exists a characteristic peak intensity ratio I_{2LA}/I_{A1g} in the Raman spectra of WS_2 when taken using 514

nm laser line excitation. This intensity ratio is demonstrated to effectively identify mono-, bi- and tri-layer WS_2. This method may also be extended to other TMDC materials using laser excitation with proper wavelength.

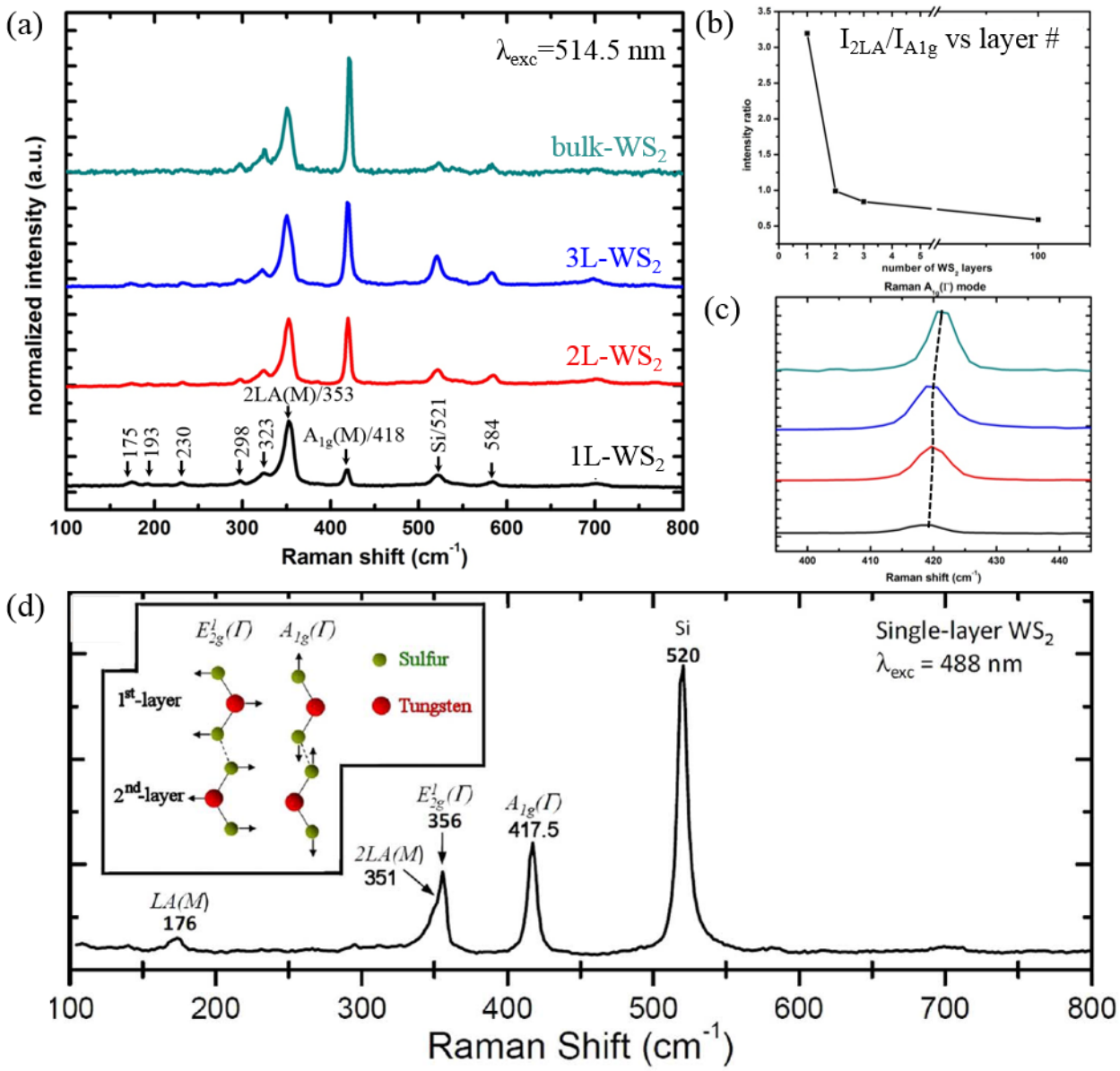


Figure 3-4. (a) Raman spectra of exfoliated mono-, bi-, tri-layer and bulk PSU-WS_2 on SiO_2/Si substrate. 514.5 nm excitation laser line. (b) I_{2LA}/I_{A1g} vs layer number. (c) Blue shift in $A_{1g}(\Gamma)$ peak position with increasing layer number. (d) Raman spectrum of a CVD-grown single layer WS_2 obtained using 488 nm

laser excitation. Inset shows the lattice vibrations for $E_{2g}(\Gamma)$ and $A_{1g}(\Gamma)$ modes. Adapted from Fig. 1 of Ref. [89]

Figure 3-4(a) shows Raman spectra from exfoliated mono-, bi-, tri-layer and bulk PSU-WS_2 with 514 nm laser excitation. The positions of the Raman peaks are labeled for the monolayer spectrum. Among all the peaks, the 2LA(M) at 353 cm^{-1} and $A_{1g}(\Gamma)$ at 418 cm^{-1} are prominent. For other laser excitation wavelengths such as 488 nm, an additional Raman peak $E_{2g}^{1}(\Gamma)$ at 356 cm^{-1} is also strong (Fig. 3-4(d)[89]). Here, it is obscured by the 2LA(M) mode. The inset of Fig. 3-4(d) shows the lattice vibration situations for $E_{2g}^{1}(\Gamma)$ and $A_{1g}(\Gamma)$ modes. $E_{2g}^{1}(\Gamma)$ is an in-plane phonon mode involving the movements of both W and S atoms, while $A_{1g}(\Gamma)$ is generated only from out-of-plane vibrations of S atoms. The 2LA(M) mode is due to a second-order Raman scattering process, which involves the scattering of two first-order LA(M) phonons. The LA(M) phonon is a longitudinal acoustic mode arising from the in-plane collective vibrations of all atoms.

As Fig. 3-4(b) shows, I_{2LA}/I_{A1g} experiences a sharp decrease from > 3 to around 1 as the layer number increases from 1 to 2. Then, it only shows a small decrease to slightly less than 1, i.e. 0.8, at 3 layer before saturating around 0.6 for bulk. Hence, for layer number exceeding 3, I_{2LA}/I_{A1g} is no longer a good indicator. This layer-number dependence exhibited in WS_2 Raman using 514 nm excitation has been systematically studied by Ayse *et al*.[89], and is confirmed as an accurate and fast way of layer number identification for WS_2.

In addition to the change of I_{2LA}/I_{A1g}, the peak position of $A_{1g}(\Gamma)$ mode exhibits a blushift with increasing layer number, as shown in Fig. 3-4 (c). This is due to an increase in the restoring force caused by the interlayer interaction of the sulfur atoms.

3.2.4 Photoluminescence spectroscopy (PL) characterization

TMDC possess a direct band gap in the monolayer limit. This property gives rise to a strong PL response. As the layer number increases, PL signals become weak but usually show two peaks from the direct and indirect band gap emissions. In this section, we use results from exfoliated FSU-WSe_2 to discuss the various aspects of MX_2 PL spectra.

Photoluminescence describes a phenomenon where the interaction process of incident photons with a specimen leads to emission of new photons. These emitted photons carry important information of the specimen under examination, such as electronic states, disorder, excitons, etc. Using direct-gap semiconductors as an example, Fig. 3-5(a) shows a schematic diagram of the PL emission process. After the incident photon energy is absorbed, an electron is excited from the valence band to the conduction band, leaving a hole behind. The created electrons and holes usually first relax to the conduction and valence extrema and then recombine through emitting a photon. However, unlike the free e-h pairs created in an electrical transport system, these e-h pairs are bound together through long-range Coloumb interactions, i.e. forming excitons. Because of the binding energy Δ of the excitons, the band gap obtained from PL measurements, i.e. optical band gap, is always less than the electronic band gap E_g by Δ. In systems with small binding energy, such as Si (14.7 meV[90]) and GaAs (4.2 meV[91]), the optical band gap is close to E_g. However, if the e-h Coloumb interaction is strong, Δ could be large, as in the case of monolayer TMDC systems.[92-95] For example, the exciton binding energy of monolayer WS_2 is measured to be around 0.71 eV while its PL emission energy is ~ 2.1 eV. This implies an electronic band gap of ~ 2.8 eV.[95]

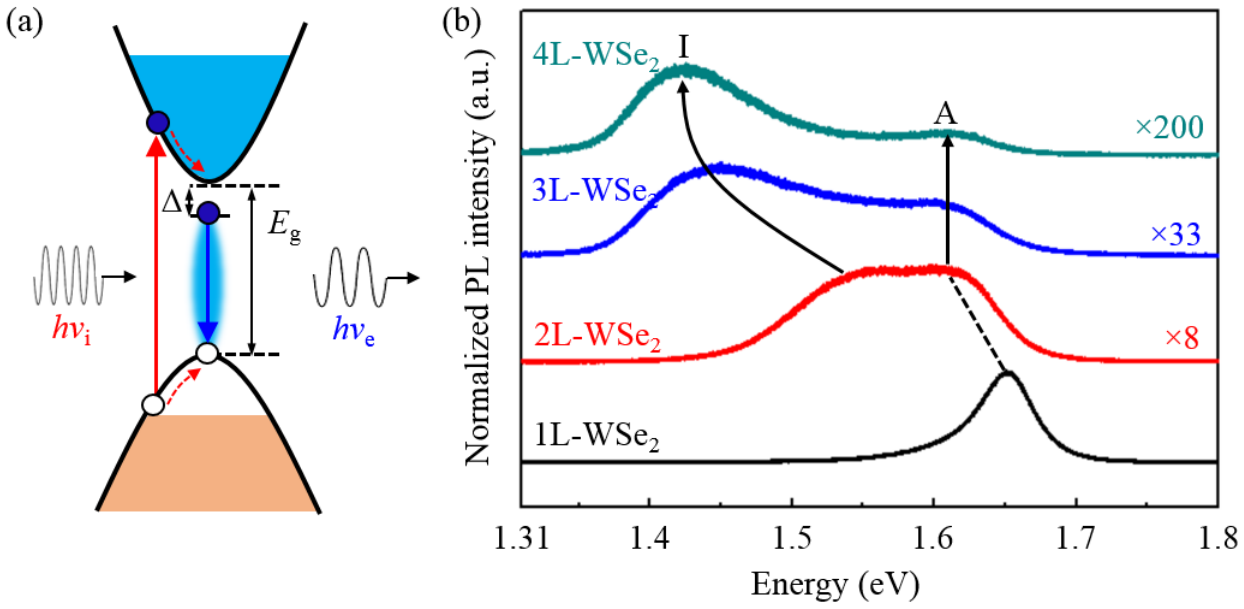


Figure 3-5. (a) Schematics of PL emission process. (b) PL spectra of exfoliated 1- to 4-layer FSU-WSe_2 on SiO_2/Si substrate. 488 nm laser excitation. Image courtesy of Simin Feng.

Fig. 3-5(b) shows PL spectra from 1L to 4L FSU-WSe_2 taken at room temperature. The excitation laser wavelength is 488 nm. PL peaks corresponding to direct-gap and indirect-gap emissions are labeled as A and I, respectively. The A-exciton peak is associated with the top of the splitted valence bands, i.e. the V_A valence band shown in Fig. 1-6. The black arrows track the evolution of both peaks as the layer number increases. The indirect band gap emission shows a significant redshift in energy with increasing layer numbers. This is primarily due to lowering of the conduction band minima, while the valence band maxima almost remain at the same energy level.[96] From the PL spectra, we obtain the direct optical gap size for monolayer WSe_2 to be 1.65 eV. The indirect optical gap sizes for 2- to 4-layer WSe_2 are 1.56 eV, 1.45 eV, and 1.43 eV, respectively.

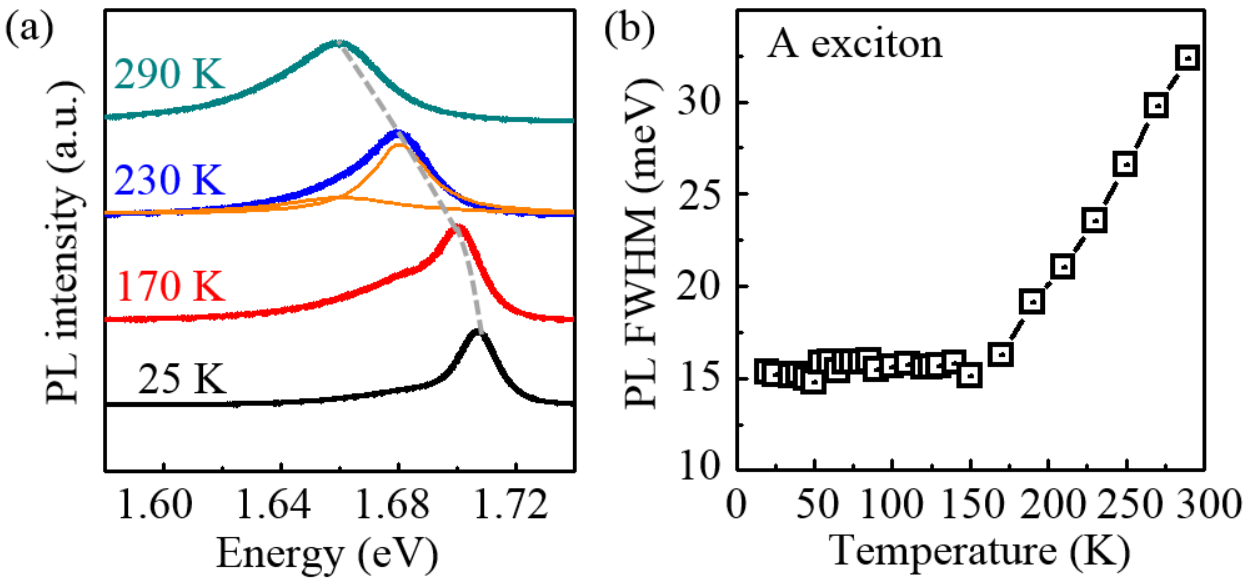


Figure 3-6. (a) PL spectra of exfoliated monolayer FSU-WSe_2 on SiO_2/Si substrate at selected temperatures from 25K to 290K. The position of the A exciton peak is indicated by the dashed line. Fits to the 230K trace are shown underneath the data. (b) Temperature dependence of the FWHM of the A-exciton peak. The low-temperature width of 15 meV indicates the high crystal quality.

Another important characteristic is the temperature-dependent FWHM of the A-exciton emission peak in monolayer WSe_2. Figure 3-6(a) plots PL spectra from a monolayer FSU-WSe_2 sheet at selective temperatures. The excitation laser wavelength is 488 nm. Using the 230K PL spectrum as an example, Lorentzian fittings reveal two peaks, which we attribute to the A-exciton and the trion emission following the literature.[97] In addition to thermal broadening, defects and electrostatic inhomogeneity also increase the width of the PL. The FWHM of the A-exciton emission peak at low temperature is a good indicator of the sample quality. A narrow width usually corresponds to high sample quality. As Fig. 3-6(b) shows, the FWHM exhibits significant temperature dependence between 150K and 300K primarily due to thermal broadening. The width saturates at ~ 15 meV at low temperatures. In the literature, the narrowest

reported width is about 5 ~ 10 meV.[97, 98] The quality of our WSe_2 crystals is quite high among contemporary samples, although compared to the FWHM < 1 meV exhibited by high-quality GaAs crystals[99], there is plenty room for improvement.

3.2.5 Discussion on PL spectroscopy of defective TMDC monolayers

It has been well studied that heavily doped semiconductors possess band tails with localized states inside the band gap.[100] When excitons are generated in such disordered-systems, they tend to relax to these sub-gap states and become localized. Hence, PL spectroscopy can be an important and useful tool to study the interactions between disorders and excitons.

In pristine TMDC monolayers, localized states can originate from intrinsic structural defects (more in Chapter 4) and/or Coulomb impurities in the surrounding environment. A new, sub-bandgap peak was reported by Tongay *et al*.[101] in PL studies of defective monolayer MoS_2, $MoSe_2$ and WSe_2, that were bombarded by α-particles or treated with thermal annealing. Here we describe a series of experiments where we intentionally introduce lattice defects to exfoliated PSU-WS_2 monolayers via bombardment by low-energy Ar^+ beams and use PL to assess the outcome.

The Ar^+ beam is generated using an integrated ion source in a custom designed Lab-18 system (Kurt J. Lesker). We control the ion irradiation energy and dose through the discharge voltage V_{dis} and emission current I_{e} of the ion gun. The actual incident energy or dose of the ions cannot be obtained due to the system design and functionality of the Lab-18 system. However, the density of defects should increase with increasing V_{dis} as the ions gain more energy from the ion gun. The emission current of the ion gun and irradiation time are kept at constant at $I_{\mathrm{e}} = 0.4$ A and $t = 2$ s. Figure 3-7(a) shows PL spectra from pristine (black curve) and defective (red

and blue curves) PSU-WS_2 taken in ambient environment. The excitation laser wavelength is 488 nm. The irradiation conditions are $V_{dis} = 25$ V and 50 V for the red and black curves, respectively. All three spectra display a strong PL peak at the same position of 2.01 eV, which is due to the A-exciton emission. We associate the new peak X_B at 1.87 eV with defect-bound exciton emissions. The relative intensity of X_B to the A-exciton peak increases as more defects are generated by the Ar^+ bombardment. The A-exciton emission peak intensity from the defective WS_2 sheets are significantly weaker than that from the pristine monolayer by at least 5 times.

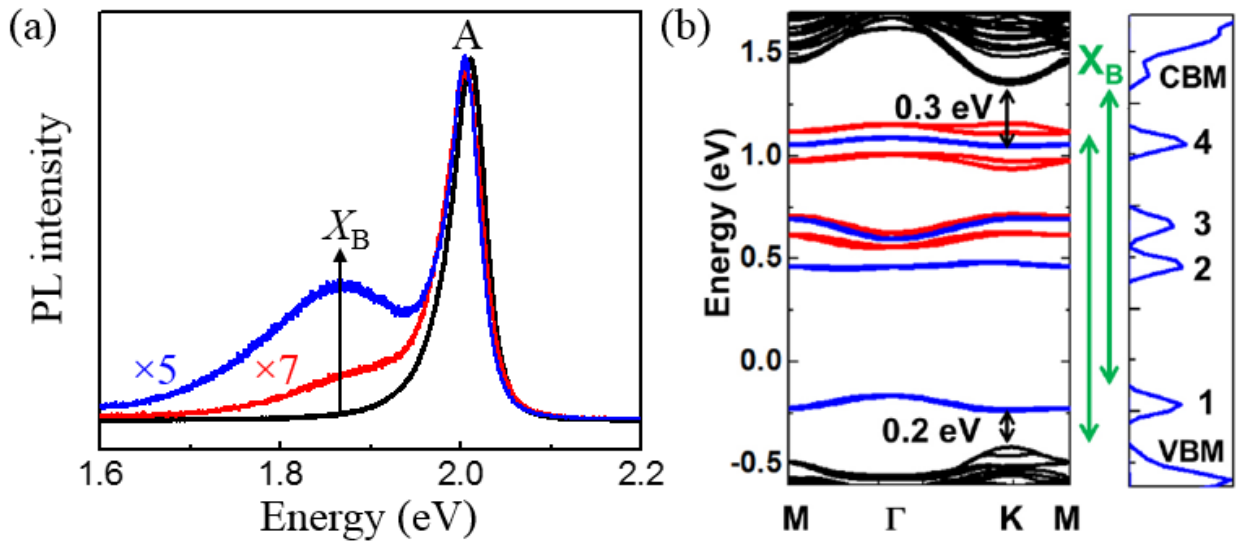


Figure 3-7. (a) PL spectra of exfoliated pristine (black curve) and defective (red and blue curves) PSU-WS_2 monolayers. 488 nm laser excitation. (b) Calculated electronic band structure of monolayer MoS_2 in the presence of di-S vacancies. Right panel: Total density of states of the monolayer MoS_2 with S vacancies in the presence of N_2. Adapted from Fig. 5 of Ref. [101].

Next, we discuss the origin of the defect-bound exciton emissions following the discussion in Ref. [101] as the point defects created in our WS_2 monolayer are also likely to be sulfur

vacancies. According to their DFT calculation of band structure and density of states (DoS) for defective monolayer MoS_2, the formation of di-sulfur vacancies and their interaction with N_2 or O_2 molecules that are physic-sorbed at these defect sites introduce discrete energy states within the band gap, as illustrated in Figure 3-7(b). Sub-gap energy levels in red are due to the formation of di-sulfur vacancies alone. After interacting with N_2 molecules, these energy levels are renormalized to the blue lines, which are located 0.3eV and 0.2eV from the conduction and valence bands respectively. Similarly, interaction with O_2 molecules introduces discrete energy states, among which those that are ~ 200 meV close to the conduction and valence bands contribute to the defect-bound exciton emissions. The X_B energy shift from the A-exciton peak in our defective monolayer WS_2 is ~ 0.14 eV, which is also consistent with their DFT calculations for MoS_2 in the case of interaction with O_2 molecules.

3.3 Atomic force microscopy (AFM) and AFM-based characterizations

3.3.1 Topography measurement by AFM

One of the most common applications of an AFM microscope is to measure the surface morphology of samples with the advantage of high spatial resolution. Depending on the sharpness of the AFM tip, it can resolve features as small as a few nanometers such as a nanowire. Before discussing the measurement results, we first make an introduction to the basic operation principles of AFM.

The operation of AFM depends on the accurate detection of the interaction force between an AFM probe tip and the sample surface. This is realized by mounting the tip at the end of a cantilever which is supported on a piezoelectric element. Figure 3-8(a) shows a schematic diagram of the AFM measurement configuration. The tip-sample force is sensed by the deflection of the long cantilever of the AFM probe. A beam of highly directional light emitted

from a photodiode (PD) is directed at the reflective back of the cantilever. The reflected light is then detected by a positive-sensitive diode (PSD), which consists of four quadrants. Before scanning, the position of the cantilever is adjusted to allow the reflected beam light to pass the center of the PSD.

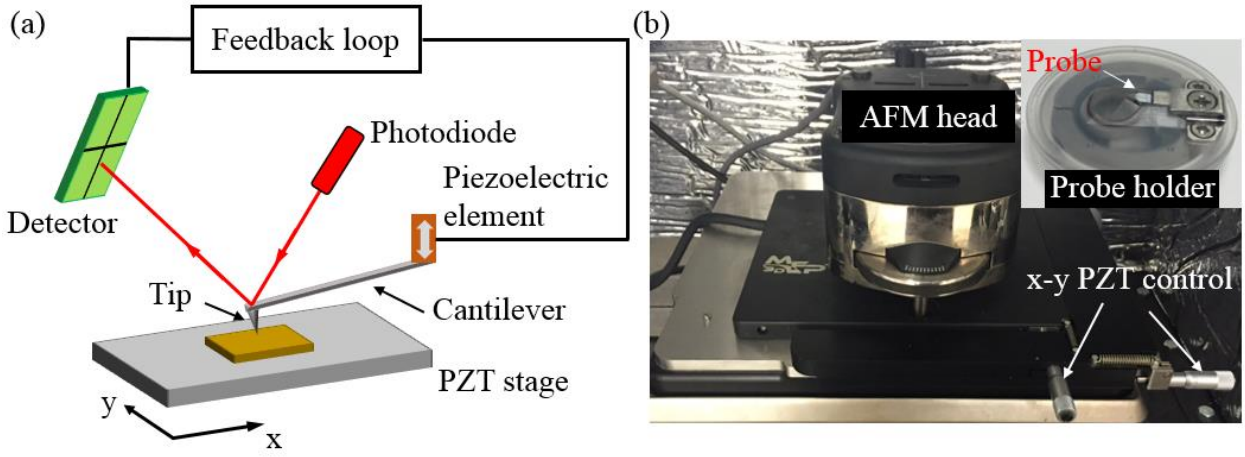


Figure 3-8. Schematic diagram of the AFM measurement setup. (b) An optical picture of our AFM instrument.

During the topography measurement, there are two operation modes: a) tapping mode and b) contact mode. In a tapping mode scan, the cantilever is oscillated at or slightly off (-5%) off its mechanical resonance frequency with a fixed oscillation amplitude. As the tip scans over the sample, it will intermittently contact the sample surface at the bottom of its oscillation; and therefore the tapping mode is also called intermittent contact mode. The constant oscillation amplitude is maintained through a feedback loop which uses the output voltage signals from the PSD to adjust the height of the probe. The height change data at each scan point is then processed by the AFM software and reconstructed into maps showing the topography of the sample surface. The same process also applies to the contact mode scan, except that the

cantilever is in contact with the sample surface and mechanically bent with a fix deflection throughout the scan. The amount of force exerted on the sample from the tip is determined by the defection of the cantilever and its spring constant. Hence, this image mode is often used to scan hard materials while the tapping mode is more common for soft materials.

In this thesis, we primarily use the tapping mode to determine the layer number and monolayer thickness of various 2D materials, such as graphene, MoS_2, WS_2, WSe_2, $GaSe_2$, and h-BN.

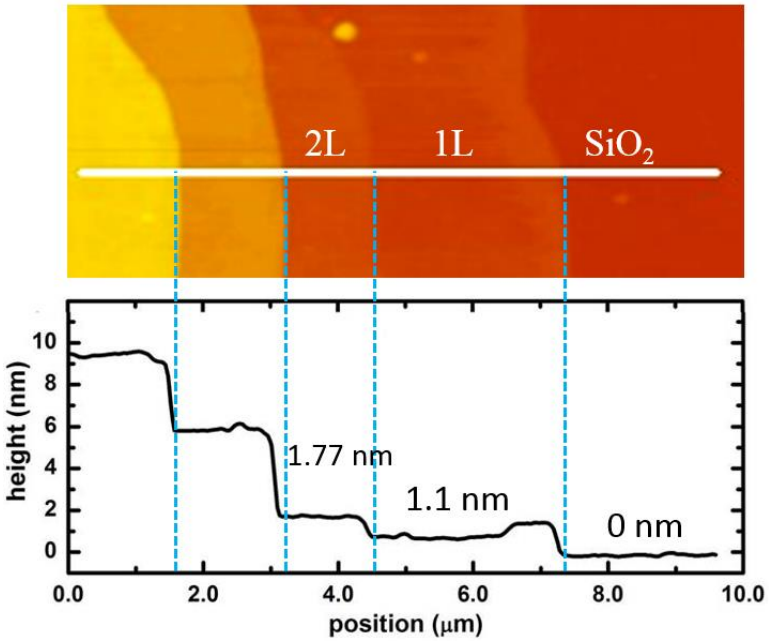


Figure 3-9. Top: Tapping mode AFM height map of an exfoliated PSU-WS_2 on SiO_2/Si with regions of identified layer numbers. Bottom: Height profile along the while line in the height map.

However, the tapping mode measurement has an inherent problem when measuring the height across two different materials. That is there is always an offset embedded in the measured height. This is because the interaction between the AFM tip and sample surface not only depends

on the tip-sample distance but is also affected by the composition of the sample. For example, Fig. 3-9 shows a tapping mode height map of an exfoliated PSU-WS_2 flake on SiO_2/Si substrate. The height profile at the white line-cut is plotted below. Here, we set the SiO_2 surface to be at zero height. For the monolayer and bilayer WS_2, the measured heights are 1.1 nm and 1.67 nm, respectively. Hence, the real monolayer thickness is 0.67 nm rather than 1.1 nm as measured from the 1L region to its nearby SiO_2 surface. In this case, the offset is 0.43 nm and positive. The offset is usually a few Å and varies from sample to sample. So one should be very careful in using the tapping mode to measure samples with thickness less than 1 nm.

The contact mode scan, on the other hand, does not have the offset issue. This is because the tip is in constant contact with the sample surface and height measurement is not affected by material difference. However, the sharp AFM tip might cause damage if the sample is softer than the tip, which is mostly made of silicon.

3.3.2 Work function study by Kelvin Probe Force Microscopy (KPFM)

The significance of measuring the workfunction of WSe_2 as well as other TMDC materials is that it can inform the choice of metal to use when making contacts. The KPFM technique can also provide important information regarding the band alignment in heterostructures made of dissimilar materials. Before discussing the measurement results, we first make an introduction to the basic operation principles of KPFM.

KPFM is a technique that can measure the local work function of a material by measuring the potential offset between the sample surface and a metallic probe tip. It utilizes of an AFM microscope and applies the same principle as a macroscopic Kelvin probe.

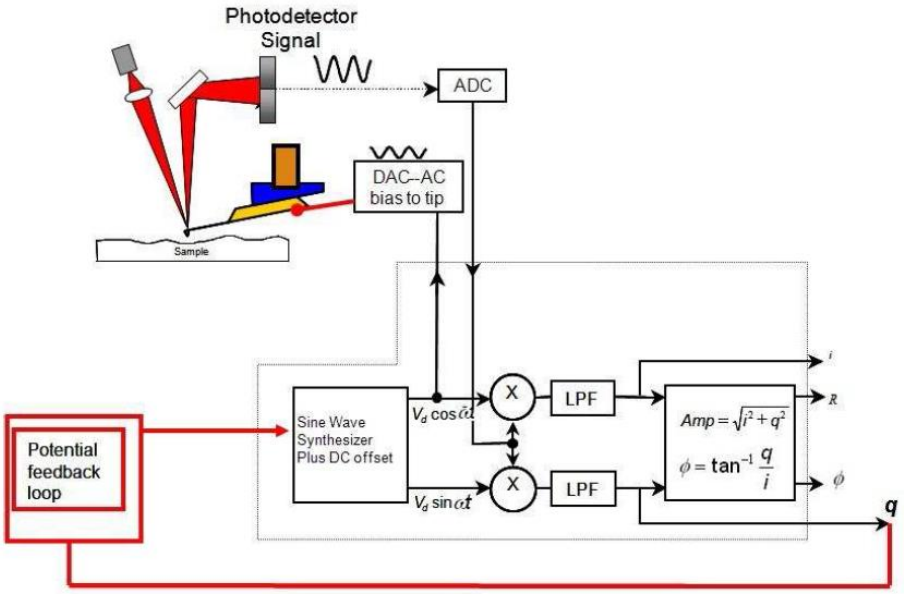


Figure 3-10. Schematic diagram of the KPFM measurement configuration. Adapted from Fig. 10.1 of Ref. [102]

During the KPFM scan, the metallic probe tip forms a parallel-plate capacitor with the local sample surface underneath. Based on this model, the tip-sample interaction force is given by

$$F = \frac{1}{2}\frac{\partial C}{\partial z}V^2 \tag{3.3}$$

where C is the capacitance of the tip-sample parallel-plate capacitor, z is the tip-sample spacing. V is the total tip-sample potential difference. Usually, the sample is prepared on a conductive substrate, e.g. gold coated silicon wafers, which is grounded during the scan. Both an AC ($V_{\mathrm{ac}} \sin(wt)$) and a DC bias (V_{DC}) are applied to the metallic probe from the AFM microscope. Figure 3-10 shows a schematic diagram of KPFM measurement setup.[102] Besides the applied voltages, there a third component in the total tip-sample potential difference , and it is the potential offset V_{sp} due to the tip-sample workfunction mismatch. Hence, V is given by

$$V = \left(V_{\mathrm{DC}} - V_{\mathrm{sp}}\right) + V_{\mathrm{ac}} \sin(wt) \tag{3.4}$$

For our KPFM system, V_{sp} is defined as

$$V_{\mathrm{sp}} \equiv \frac{W_{\mathrm{sample}} - W_{\mathrm{tip}}}{e} \tag{3.5}$$

where W_{tip} and W_{sample} are the workfunction of the metallic tip and sample, respectively.

Substituting Eq. (3.4) into Eq. (3.3), the electrostatic force *F* can then be expressed as

$$F = \frac{1}{2}\frac{\partial C}{\partial z}\left(\left[\left(V_{\mathrm{DC}} - V_{\mathrm{sp}}\right)^2 + \frac{1}{2}V_{\mathrm{ac}}^2\right] + 2\left[\left(V_{\mathrm{DC}} - V_{\mathrm{sp}}\right)V_{\mathrm{ac}}\sin(wt)\right] - \left[\frac{1}{2}V_{\mathrm{ac}}^2\cos(2wt)\right]\right) \tag{3.6}$$

There are three components contributing to the vibration of the tip caused by the electrostatic force: a DC term $\left[\left(V_{\mathrm{DC}} - V_{\mathrm{sp}}\right)^2 + \frac{1}{2}V_{\mathrm{ac}}^2\right]$, a first harmonic order term $\left(V_{\mathrm{DC}} - V_{\mathrm{sp}}\right)V_{\mathrm{ac}}\sin(wt)$, and a second harmonic order term $V_{\mathrm{ac}}^2\cos(2wt)$. The design of the KPFM system is that it only enhances the tip vibration caused by the 1*wt* signal. A feedback loop is employed to constantly adjust the applied DC bias V_{DC} such that the tip oscillation at 1*wt* is nulled. This goal is met only at

$$V_{\mathrm{DC}} - V_{\mathrm{sp}} = 0 \tag{3.7}$$

Hence, by recording the applied DC bias, one essentially measures the potential offset between the tip and sample.

Nap mode.

The scan pattern in a KPFM measurement is different from a standard topographic scan, where each line across the sample surface is measured by a trace and a retrace scan, i.e. 1 pass. During the KPFM process, each line across the sample surface is scanned by 2 passes. This is done in a nap mode.

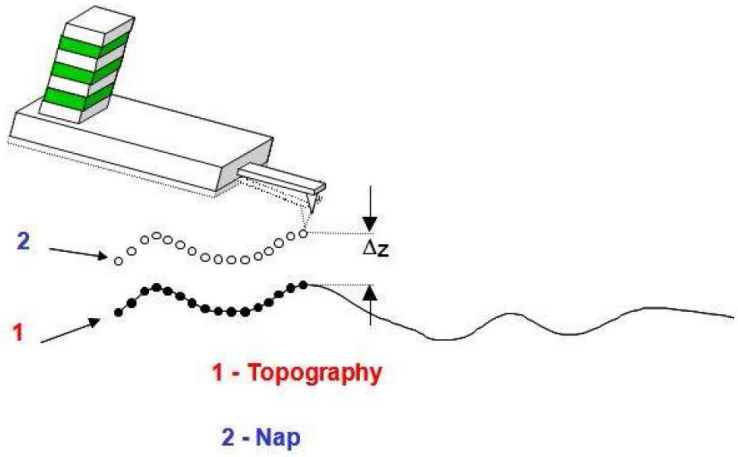


Figure 3-11. Schematic diagram of the Nap mode scan. Adapted from Fig. 10.2 of Ref. [102]

Figure 3-11 is a schematic diagram of the nap mode scan.[102] In this mode, each line across the sample surface is scanned with 2 passes. The first pass is a standard topographic scan, which acquires the height profile along the line. This is done in tapping mode. For the second pass, the mechanical oscillation in the 1st pass is turned off, and the tip is raised up to a distance Δz away from the sample surface. Then, the tip scans the same line at constant Δz while the DC bias is varied to oppose V_{sp} at each scan point. Before taking the final image, Δz needs to be adjusted to optimize the spatial resolution of the potential map. Figure 3-12 compares the height and potential maps of an exfoliated graphene sheet on Au/Si obtained simultaneously during a KPFM scan. Using the slopes of the height and potential profiles, we find the spatial resolutions of the KPFM scan to be 0.33 Å/nm and 200 μeV/nm.

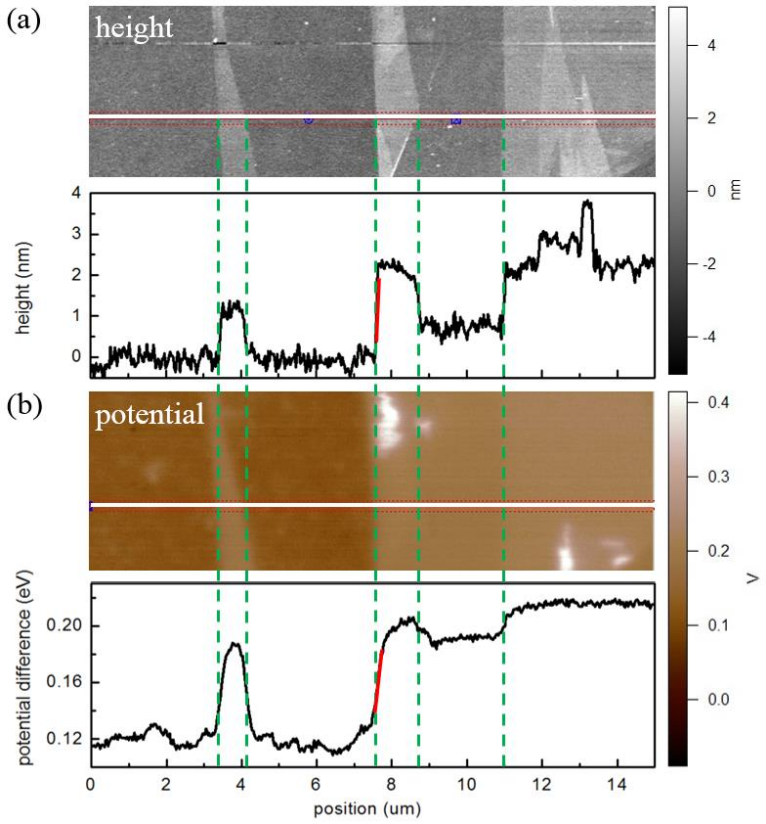


Figure 3-12. (a) KPFM height map of an exfoliated graphene on Au/Si and a height profile along the white line. (b) KPFM potential map of the same region in (a) and the potential profile along the same line.

Figure 3-13 shows a KPFM potential map of an exfoliated UT-WSe_2 sheet on Au/Si with the layer number identified. According to Eqs. (3.5) and (3.7), if the sample work function is lower than the tip, one gets a negative reading from the graph, and vice versa. From this graph, one can see that monolayer WSe_2 has the highest workfunction, and it decreases with increasing layer number until saturates at large layer number (> 20 layers)

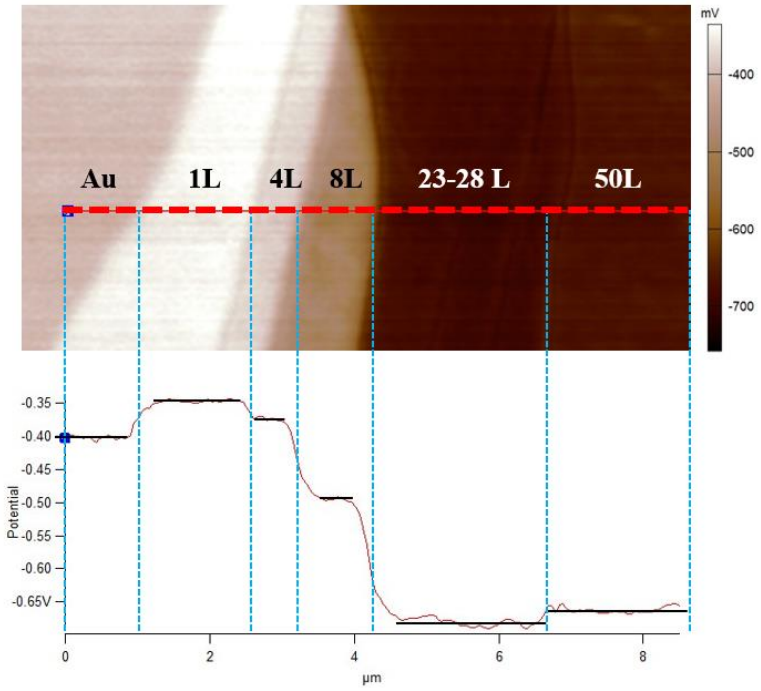


Figure 3-13. KPFM potential map of exfoliated UT-WSe_2 on Au/Si substrate with regions of identified layer number. The bottom graph is the potential profile along the red line in the potential map. Image courtesy of Jacob Shevrin.

Another study we carry out using the KPFM technique is to systematically characterize the workfunction evolution of WS_xSe_{2-x} alloys as the concentration index increases from 0 to 2 (i.e. from WSe_2 to WS_2). Figure 3-14 plots the WS_xSe_{2-x} workfunction vs the alloy concentration x from multiple samples. All the workfunction values are extracted using the graphite workfunction $W_{graphite} = 4.5$ eV as reference point. The referencing scheme is described in Appendix B.2. The yellow color markers are the gold substrate workfunction from measurement for each concentration x. The narrow band indicates good reproducibility of our measurements. The purple band shows the trend that as the sulfur concentration increases, the alloy workfunction increases. This trend is consistent with the trend suggested by DFT-calculated workfunction of WS_2 and WSe_2 by Gong *et al.*[103], as marked by the two red triangles on the

graph. However, the workfunction of WSe_2 from their calculation is 4.21 eV, which is much lower than our measured values by at least 0.25 eV. There is a fairly good agreement for the WS_2 workfunction between their calculated 4.73 eV and our measured range from 4.70 eV to 4.82 eV.

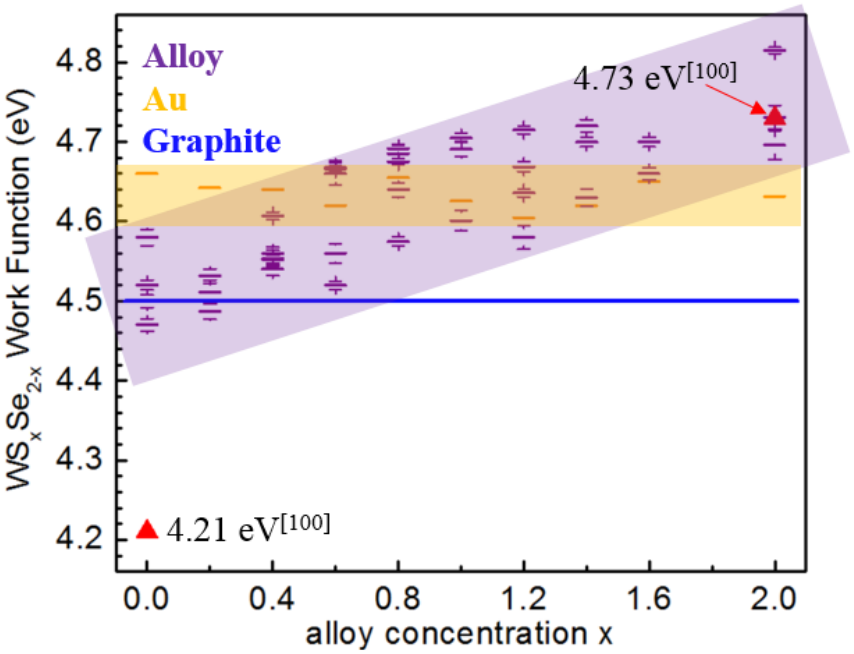


Figure 3-14. Workfunction evolution of PSU-WS_xSe_{2-x} alloy as a function of the alloy concentration x.

3.3.3 Thermal conductivity study by scanning thermal microscopy (SThM)

SThM is another useful AFM-based microscopic characterization technique. It takes the advantage of the sharp AMF-probe tip to image local thermal conductivity or temperature profile of a specimen with high spatial resolutions.[104] During the SThM measurement, heat exchange between the tip and sample is detected by a specially designed probe with temperature-sensing ability. At the end of the probe tip, there is usually a thermal-couple junction or a thin-film resistor whose resistance change is measured and correlated with the local thermal properties or temperature of the sample under examination. Our discussion of SThM measurements will focus

on imaging using the resistive probes with a thin-film resistor fabricated at the end of the probe tip.

The thin-film resistor in our SThM probe is made of palladium (supplied by Asylum Research). It can provide sub 100 nm topographic and thermal spatial resolution, with a temperature resolution of 0.1 K. The resistance is measured by placing the probe in a balanced Wheatstone bridge. For our SThM measurements, the tip is constantly in contact with the sample, so the primary cause of the probe resistance change is attributed to heat flow between the tip and sample.

Two operation modes are available depending on the magnitude of the excitation voltage applied to the probe resistor. When a large excitation voltage is applied and causes joule heating of the resistor at the tip apex, heat flows from the hot probe tip to the sample. This is called active mode. The amount of heat dissipation depends on the local thermal conductivity of the sample. At regions with high thermal conductivity, heat transfer is more efficient and faster, causing a larger decrease in the tip temperature. As the tip scans over the sample surface, a temperature map reflecting the thermal conductivity variation in the sample can be generated. The other operation mode is the passive mode, where a small excitation voltage is applied just for probe resistance measurement without inducing the joule heating. In this case, the sample is heated by external sources, such as a local heater or a global heater. Heat flows from the hot sample to the tip causes fluctuations in the probe resistance. Hence the temperature profile of the sample can be mapped out as the tip scans over it.

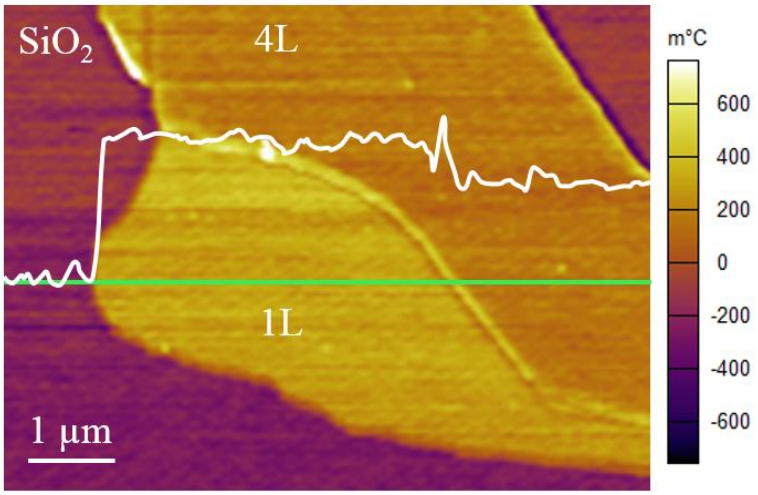


Figure 3-15. SThM temperature map of an exfoliated UT-WSe_2 flake on SiO_2/Si and is measured using active mode scan. The temperature on the graph is linearly proportional to the real temperature by an unknown factor. Higher temperature corresponds to lower thermal conductivity.

Figure 3-15 is an SThM temperature map of an exfoliated UT-WSe_2 sheet on SiO_2/Si using the active mode scanning. The temperature values displayed on the graph is not the actual tip temperature as our system is not calibrated yet. However, the map can still reflect the relative thermal conductivity strength with higher "temperature" corresponding to lower thermal conductivity. This flake contains a 1-layer region and a 4-layer region. The white line is the temperature profile along the green line showing the 4-layer WSe_2 has a larger overall thermal conductivity than the monolayer. In the following, we speculate on the mechanism for this observation. A quantitative understanding can be obtained by modeling the thermal transport in a COMSOL software package.

The thermal conductivity κ of WSe_2 has been reported to exhibit a large anisotropy with the in-plane κ (1.2 ~ 1.6 W/mK) values 30 times higher than the cross-plane κ, which is primarily due to its 2D layer structure and disorder effects.[45, 105] For the conductivity measurement

shown in Fig. 3-15, the exfoliated WSe_2 sheet is supported on SiO_2. Even though heat conduction in the out-of-plane direction is much less favorable than the in-plane path, it may still be more efficient than the heat transfer from WSe_2 to the underlying SiO_2 layer. Under this assumption, a higher overall thermal conductivity in thicker WSe_2 sheet should be expected, which is what we observed here.

Chapter 4

Electrical transport in few-layer WSe_2 field-effect transistors

In this chapter, we describe electrical transport studies in few-layer WSe_2 field-effect transistors, focusing on the gate-modulated conductance in the sub-threshold regime.

Section 4.1 is an introduction to the charge transport at metal/semiconductor interface. Three transmission mechanisms, i.e. thermionic emission (TE), thermionic-field emission (TFE), and field emission (FE), as well as their impacts on the conduction behaviors are discussed.

Section 4.2 describes the fabrication techniques of WSe_2 transistors supported on various substrates and problems encountered. We also discuss various electrical measurement techniques used in acquiring electrical transport data in this chapter.

Section 4.3 first describes the general electrical features of MX_2 transistors including ambipolar conduction, electron-hole symmetry, hysteresis and its elimination, and vacuum annealing effect. Then we discuss room-temperature and low-temperature electrical transport measurements on few-layer WSe_2 field-effect transistors. The focus is on the gate dependence of the two-terminal conductance in the subthreshold regime. We find that the contact resistance dominates the resistance of the device and charge transport across the contact Schottky barrier is dominated by thermionic-field emission. This behavior is due to a large number of impurity states inside the WSe_2 band gap. Using the TFE model and experimentally measured sub-threshold swing values, we self-consistently determine the density of the sub-gap impurity states to be approximately $1\sim2\times10^{13}\ /\mathrm{cm}^2/\mathrm{eV}$. This result is consistent with the high metal-insulator transition (MIT) carrier density ($\sim1\times10^{13}\ /\mathrm{cm}^2$) observed in our WSe_2 devices as well as MoS_2 devices reported by other groups.[106, 107]

4.1 Introduction to charge transport mechanisms at metal/semiconductor interface

Metal-semiconductor (M-S) contacts is among the most important and extensively studied topics in semiconductor physics and device applications.[108] In the study of semiconducting TMDC, the difficulty in making ohmic contacts poses a serious challenge for exploring the intrinsic electronic properties by means of electrical transport measurements. Recent studies suggest that contact resistance plays a dominant role in the field effect of TMDC transistors.[109] Hence, a good understanding of the charge transport across the M-S interface is important and necessary for both fundamental researcxh and potential applications of TMDC.

For semiconductor materials with moderate and large bandgaps, such as silicon (1.1 eV), gallium arsenide (1.4 eV), TMDCs (1.1~2.1 eV), and GaN (3.4 eV) , an energy barrier often forms at the interface between the semiconductor and the contact metal. The maximum barrier height can be affected by various factors, such as the metal workfunction, Fermi level pinning by surface states[110], etc. The shape of the barrier, i.e. the width of the depletion layer and curvature of the band bending near the interface, is mainly determined by the doping concentration of the semiconductors. These two features of the energy barrier play important roles in the charge transport across the M-S interface.

In this section, we first make an introduction to the formation of the Schottky barrier under the ideal condition considering only the metal workfunction and bulk properties of the semiconductor. Then, the Fermi level pinning phenomenon by surface states is discussed. After that, we discuss three major charge transport mechanisms, i.e. thermionic emissions (TE), field emissions (FE), and thermionic-field emissions (TFE), and their impacts on carrier transmission through the M-S interface.

4.1.1 Formation of Schottky barrier and Fermi level pinning

The energy barrier formed at a M-S interface is widely known as Schottky barrier, named after Walter H. Schottky for his significant contribution to the development of semiconductor device theory. Using n-type semiconductor as an example, and ignoring the effect of any surface chemistry at the M-S interface, the energy-band diagram situation can be obtained in the following. Due to diffusion of electrons from the n-type semiconductor to the metal, a depletion layer is formed in the semiconductor region adjacent to the interface with only positively charged ionized donors (or negatively charged ionized acceptors for p-type semiconductor). These ionized donors (or acceptors), also called space charges Q_{SC}, are fixed around their spatial locations. They can create strong electric fields with the negative charges accumulated at the metal surface. These built-in electric fields prevent more electrons being depleted from the semiconductors. When thermal equilibrium is established between the two systems, their Fermi levels line up, and the Schottky barrier with a maximum height of $\Phi_{B,n}^{0}$ and a depletion region of x_{dep} extended into the semiconductor is formed. This band diagram formation is schematically illustrated in Fig. 4-1. ϕ_M is the metal workfunction, χ_S is electron affinity of the semiconductor, and ϕ_n is the energy difference between the semiconductor conduction band minimum E_{CBM} and its Fermi level before the Schottky barrier formation. V_{bi} is the built-in electric potential after the energy barrier is formed.

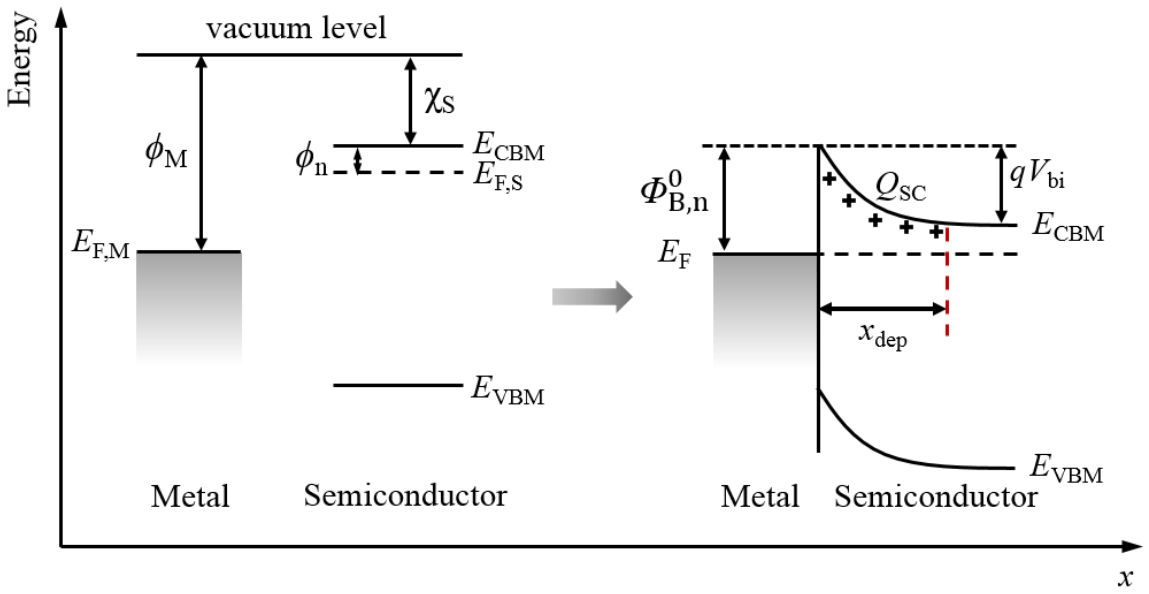


Figure 4-1.Schematic band diagram of the Schottky barrier formation at the metal/semiconductor interface for ideal condition.

In the ideal case, the barrier height only depends on the energy difference between ϕ_M and χ_S, and is given by

$$\Phi^0_{B,n} = \phi_M - \chi_S \tag{4.1}$$

The width and energy band profile of the depletion region is given by Eqs. (4.2) and (4.3), respectively. They are obtained from solving the one-dimensional Poisson equation under the abrupt approximation for charge density distribution, i.e. $\rho = eN_D$ within the depletion region and $\rho = 0$ outside it.

$$x_{dep} = \sqrt{\frac{2\varepsilon_s V_{bi}}{eN_i}} \tag{4.2}$$

$$E_c = \Phi_{B,n}^0 - \frac{e^2 N_D}{\varepsilon_s}\left(x_{dep}x - \frac{x^2}{2}\right) \quad (4.3)$$

where ε_s is the dielectric constant of the semiconductor. N_i is the impurity density, i.e. donor (acceptor) concentration in the case of n-type (p-type) semiconductors.

However, the simple model given by Eq. (4.1) rarely gives the correct barrier height as observed in most experimental systems due to its lack of incorporation of other factors that can significantly affect the barrier height. Here, we describe the Fermi level pinning phenomenon which causes a relatively fixed Schottky barrier height independent of the choice of contact metals. This is due to the presence of a large density of interface states at the semiconductor surface. The energies of these surface states (SS) are located within the bandgap as shown in Fig. 4-2. The surface states close to the valence band are of donor type while those close to the conduction band are of acceptor type. The energy level that separates the two types of surface states is called the neutral level which is labeled by its energy difference Φ_0 with the valence band top at the semiconductor surface. When the Fermi level at the surface is above the neutral level as is the case shown in Fig. 4-2, the net surface-state charges Q_{SS} is negative; otherwise, Q_{SS} is positive. Because the surface and bulk of the semiconductor need to reach thermal equilibrium even without the contact of metal, the Fermi level in the bulk region will line up with that of the surface at certain energy level depending on the polarity and density of the surface-state charges, i.e. Fermi level pinning. Hence, the Schottky barrier height only weakly depends on the metal workfunction as the Fermi levels of both the metal and the semiconductor are pinned by the interface-trap states. In the limit where the density of the interface-trap states is infinitively large, the Schottky barrier height only depends on the energy position of neutral level. In the case of n-type semiconductor, it is given by

$$\Phi_{B,n}^{0,SS} = E_g - \Phi_0 \tag{4.4}$$

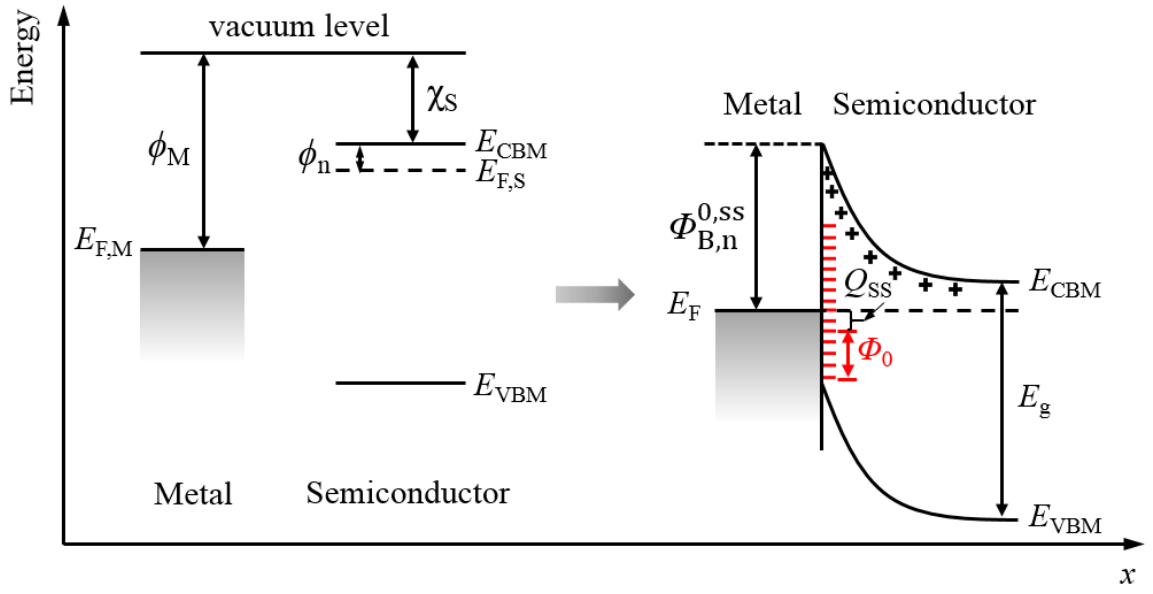


Figure 4-2. Schematic band diagram of the Schottky barrier formation in the presence of surface states.

The Fermi level pinning phenomenon has been widely observed in the experimental studies of semiconducting materials, such as silicon, GaAs[111] and more recently in TMDC[112].

4.1.2 Charge transport mechanisms at the metal-semiconductor interface

In this section, we describe three charge transport processes through a Schottky barrier contact: a) thermionic emission (TE); b) field emission (FE): c) thermionic-field emission (TFE). Figure 4-3 is a schematic diagram of the three transmission processes. Here, we consider the ideal condition for an n-type semiconductor.

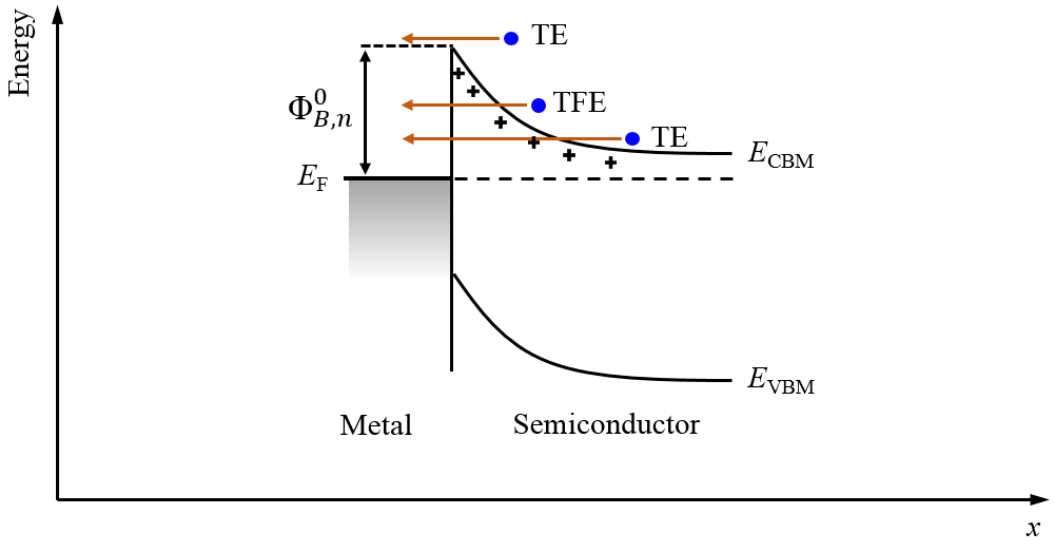


Figure 4-3. Schematics of three carrier transport process at the metal/semiconductor interface, i.e. thermionic emission (TE), thermionic field emission (TFE), and field emission (FE).

Thermionic emission mechanism.

The thermionic emission process describes the injection of the majority carrier, i.e. electron for n-type semiconductors and holes for p-type semiconductors. Their transmission across the barrier happens by first being thermally excited from around the Fermi level to energy levels above the Schottky barrier and then transmit.

The net current density J_{TE} under a small bias V across the M-S interface is given by

$$J_{TE} = J_{S\to M} + J_{M\to S} \tag{4.5}$$

where $J_{S\to M}$ is current density from the semiconductor to the metal and $J_{M\to S}$ is current density in the reverse direction. For the n-type semiconductor, only electrons at energy levels higher than the Schottky barrier, i.e. $E > E_0 = E_F + \Phi^0_{B,n}$, contribute to the current from the semiconductor to the metal. Hence $J_{S\to M}$ is given by[108]

$$J_{S\to M} = \int_{E_0}^{\infty} ev_x dn = A^* T^2 \exp\left(-\frac{e\phi_{Bn}}{k_B T}\right)\exp\left(\frac{eV}{k_B T}\right) \tag{4.6}$$

and

$$A^* = \frac{4\pi e m^* k_B^2}{h^3} \tag{4.7}$$

is the three-dimensional effective Richardson constant.m^* is the effective mass of electrons. $\Phi_{B,n}^0 = e\phi_{Bn}$, where ϕ_{Bn} is the Schottky barrier potential. $J_{M\to S}$ can then be obtained by considering the zero bias $V = 0$ situation where the net current $J_{TE} = 0$.

$$J_{M\to S} = -A^* T^2 \exp\left(-\frac{e\phi_{Bn}}{k_B T}\right) \tag{4.8}$$

Hence J_{FE} can be expressed as

$$J_{FE} = A^* T^2 \exp\left(-\frac{e\phi_{Bn}}{k_B T}\right)\left[\exp\left(\frac{eV}{k_B T}\right) - 1\right] \tag{4.9}$$

Here, the exponential term $\exp\left(-\frac{e\phi_{Bn}}{k_B T}\right)$ captures the strong temperature dependence of the thermionic emission model with the thermal excitation energy $k_B T$ in the denominator.

Field emission mechanism.

Field emission describes the process where carrier transport occurs via quantum mechanical tunneling through the potential barrier. This usually happens for heavily doped semiconductors where the barrier width is narrow. In this case, the tunneling becomes more efficient. The respective tunneling current densities for $J_{S\to M}$ and $J_{M\to S}$ are given by[108]

$$J_{S\to M} = \frac{A^{**} T^2}{k_B T} \int_{E_F}^{E_F + \Phi_{Bn}} F_S T(E)(1 - F_m) dE \tag{4.10}$$

$$J_{M\to S} = \frac{A^{**} T^2}{k_B T} \int_{E_F}^{E_F + \Phi_{Bn}} F_M T(E)(1 - F_S) dE \tag{4.11}$$

where F_S and F_M are the Fermi-Dirac distribution functions for the semiconductor and the metal, respectively. T(E) is the barrier-width dependent tunneling probability. The analytical expression for the net field-emission current density under forward bias V_F is given by[113]:

$$J_{FE} = \frac{A^{**}T\pi \exp[-q(\phi_{Bn} - V_F)/E_{00}]}{c_1 k \sin(\pi c_1 k_B T)} \tag{4.12}$$

$$c_1 \equiv \frac{1}{2E_{00}} \log\left[\frac{4(\phi_{Bn} - V_F)}{-\phi_n}\right] \tag{4.13}$$

$$E_{00} \equiv \frac{q\hbar}{2}\sqrt{\frac{N_i}{m^* \varepsilon_s}} \tag{4.14}$$

Here E_{00} is an import parameter in energy scale, and its significance will be discussed later.

Thermionic-field emission mechanism.

The thermionic-field emission process combines both TE and FE processes. First electrons are thermally excited from around the Fermi level to higher energy levels but below the potential barrier top. Then these electrons can quantum mechanically tunnel through the thinner barrier at higher energy levels. The TFE current density under forward bias V_F is given by[113]:

$$J_{TFE} = \frac{A^{**}T\sqrt{\pi E_{00} e(\phi_{Bn} - \phi_n - V_F)}}{k_B \cosh(E_{00}/k_B T)} exp\left[\frac{-q\phi_n}{k_B T} - \frac{q(\phi_{Bn} - \phi_n)}{E_0}\right] exp\left(\frac{qV_F}{E_0}\right) \tag{4.15}$$

$$E_0 \equiv E_{00} \coth\left(\frac{E_{00}}{k_B T}\right) \tag{4.16}$$

The actual current through a metal-semiconductor interface usually includes contributions from all three charge transport processes. The dominant process can be determined by comparing the energy-scale parameter E_{00} with the thermal energy $k_B T$. When $k_B T \gg E_{00}$, TE dominates and conduction happens primarily though carriers that have been thermally excited over the barrier top. When $kT \ll E_{00}$, the depletion region is usually narrower with a strong electrical

field, making quantum mechanical tunneling (FE) more efficient. When $kT \approx E_{00}$, TFE is the main mechanism for conduction. In Section 4.3, we will use this criteria to determine the dominant charge transmission mechanism in our WSe_2 field effect transistors.

4.2 Device fabrication and measurement techniques

4.2.1 Device fabrication procedures

We make few-layer WSe_2 field effect transistors (FETs) using various backgate structures. The WSe_2 sheets are exfoliated from CVT-grown crystals obtained from three laboratories mentioned in Section 3.1 of Chapter 3. The exfoliated sheets are transferred onto prefabricated backgate structures using a PMMA/PVA stamp[114] or a van der Waals transfer method[115]. The backgate structures include SiO_2/doped-Si, h-BN/graphite, HfO_2/Au, and h-BN/HfO_2/Au. Their gating efficiencies range from 6×10^{10} to 3×10^{12} $/\mathrm{cm}^2/\mathrm{V}$. Electron-beam lithography is employed to pattern the contact leads. To contact the WSe_2, we have deposited metal contacts such as Ti/Au and Pd, as well as using exfoliated few-layer (< 10 layers) graphite electrodes. Detailed device fabrication procedures are given below.

PMMA/PVA-assisted transfer.

We follow similar procedures described in Ref. [114] in our transfer process. First a PMMA/PVA/Si wafer needs to be prepared. We make 5% PVA (polyvinyl alcohol) solution by dissolving PVA powders in DI water at 80 ℃. A magnetic stir bar is used to facilitate the dissolving of PVA powders until the solution becomes crystal clear. Before spin-coating PVA, HMDS is spun on the silicon wafer as an adhesion layer for PVA. Then the PVA is spin-coated at ~ 2500 r.p.m. for 1 min, followed by hot-plate baking at 130 ℃ for 3 min. Then PMMA (950K A3) is spin-coated at 4000 r.p.m. for 1 min. No baking is need afterwards. A successful

PMMA/PVA/Si wafer should have similar color as a silicon wafer with 290 nm thermally-grown SiO_2. This color is critical as it gives correct color contrast for layer number identification under an optical microscope.

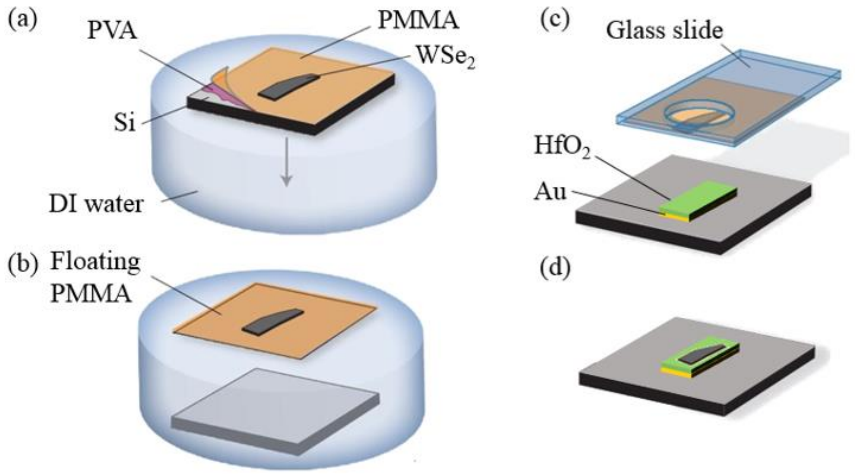


Figure 4-4. PMMA/PVA-assisted transfer process. Adapted and modified from Fig. 1 of Ref. [114].

The WSe_2 sheets are directly exfoliated onto PMMA/PVA/Si chips and then examined under an optical microscope first. Candidate pieces are measured by AFM to determine the thickness and layer number. Then, the WSe_2/PMMA/PVA/Si chips are floated in a container filled with DI water, as shown in Fig. 4-4(a). Because the PVA layer is water soluble, the Si substrate will detach from the PMMA layer by the time the PVA layer is completely dissolved, as is shown in Fig. 4-4(b). Then an aluminum slide with a hole in the center is used to fish the PMMA film out. During this process, we use a plastic straw to guide the position of the film such that the region with target WSe_2 sheets is suspended approximately over the center of the hole. Then the slide is flipped with the side containing the PMMA film facing downward and put into a closed desiccant container. It usually takes a few hours for the film to dry completely.

To transfer the WSe_2 sheets onto backgate substrates, the aluminum slide is attached to the arm of a micro-manipulator stage and then positioned under an optical microscope. The WSe_2 piece is located under the microscope and adjust to hang right over the gate structure, e.g. HfO_2/Au locate gates, as shown in Fig. 4-4(c). Then the slide is lowered gradually to reduce the gap size between WSe_2 and substrate. During this process, the position of the WSe_2 sheet needs to be constantly adjusted to make sure it is right on top of the target area on the substrate. Then a heater is turned on to heat up and relax the PMMA film. Further adjustment of the WSe_2 position is needed as the relaxation of PMMA film may cause shift of the WSe_2 sheet by more than 10 μm. The PMMA film release temperature should be above 100 ℃, e.g. ~ 105 ℃, to drive away water moistures on the substrate surface. After waiting for a couple of minutes, a nitrogen gun is used to blow the suspended PMMA film onto the substrate, as shown in Fig. 4-4(d). The transfer accuracy could be as good as less than 1 μm. As the last step, the PMMA layer is dissolved away in Acetone for a few minutes.

Fabrication of backgate structures.

SiO_2/Si wafer is purchased from Nova Electronic Materials, Ltd. with 290nm±5% thermally-grown dry oxide. The gating efficiency is 7×10^{10} /cm^2/V.

h-BN/graphite backgate substrates are fabricated in our lab. First graphite sheets are exfoliated from bulk crystals, i.e. Kish graphite or HOPG graphite, onto SiO_2/Si substrates. Then high-quality h-BN sheets are exfoliated and transferred onto few-layer graphite piece using the PMMA/PVA-stamp method. The h-BN crystals are obtained from Dr. K. Watanabe and Dr. T. Taniguchi's laboratory in Japan. We usually use uniform h-BN sheets of 20 ~ 40 nm thick as the gate dielectric. After removing the PMMA layer in Acetone, the h-BN/graphite gate stacks are

annealed in a tube furnace with flowing gases of 50 s.c.c.m O_2 and 500 s.c.c.m Ar/H_2(10%) mixture at 450 ℃ for 4 hours. AFM measurements show that the h-BN surface after anneal is free of PMMA residues. The dielectric constant of h-BN is determined to be 28 ± 1 through quantum hall measurements of graphene field effect transistors by Jing Li.

HfO_2/Au backgate substrates are fabricated by first etching trenches (~60nm) in SiO_2/Si substrates using RIE etching (PT 720 Versalock) followed by Au deposition to fill up the trenches to the SiO_2 surface. Then a layer of HfO_2 (~ 40nm) is grown over the entire SiO_2/Si substrate via atomic layer deposition (ALD). For 30 nm HfO_2 layer, the gating efficiency is ~ 3×10^{12} /cm^2/V as determined from capacitance measurement. Detailed fabrication procedures can be found in Appendix A.2.

h-BN/HfO_2/Au backgate substrates combines the strength of the clean h-BN surface and the high gating efficiency of HfO_2/Au gate structure. The h-BN sheets are exfoliated directly onto a polydimethylsiloxane (PDMS) stamp which is pre-treated with ozone (5 min, 50 ℃). For this type of backgate structure, we usually use very thin h-BN sheets with thickness ~ 10 nm. Then the h-BN sheet is released from the PDMS onto the HfO_2/Au substrate at temperature ~ 60 ℃. The positioning of the h-BN sheet is done using the micro-manipulator stage in a similar fashion as in the PMMA/PVA transfer method. Since we cannot anneal the finished h-BN/HfO_2/Au heterostructures, there is always a thin layer of PDMS residue on the h-BN surface. AFM measurements (AC mode) reveal the residue layer has a roughness ranging from 0.3 ~ 1.5 nm.

For use of the SiO_2/Si and HfO_2/Au substrates, a cleaning step is needed. The substrates are first soaked in Acetone with sonication for 30 min. Then, they are soaked in IPA with another 30 min sonication. The last step is ozone cleaning (Samco UV&Ozone Dry Stripper) at 50 ℃ for 30 min.

Electron-beam lithography patterning.

Two positive e-beam resists, PMMA and MMA/MAA copolymer, are used in e-beam lithography patterning. The MMA/MAA copolymer is first spin-coated (3000 r.p.m. 45 s) followed by hot-plate baking (180 ℃, 3 min). Then the PMMA is spin-coated (4000 r.p.m., 45 s) followed by hot-plate baking (180 ℃, 3 min)

E-beam writing is performed using a Vistec EBPG5200 system. The electron beam dose used in exposing the PMMA/MMA-MAA bilayer needs to be carefully chosen. For graphene devices, a 330 $\mu C/cm^2$ e-beam dose is sufficient to fully expose the resist bilayer such that the graphene surface at the exposed region is clean with negligible resist residues after develop. The contacts are ohmic for Ti/Au (5nm/45nm) electrodes. However, we consistently find that a thin resist residue layer is present at the exposed MX_2 (e.g. MoS_2, WS_2, and WSe_2) surface after develop when 330 $\mu C/cm^2$ e-beam dose is used.

To illustrate this problem, we use results from MoS_2 as an example. After develop, we perform AFM measurements in the e-beam exposed MoS_2 regions. Figure 4-5(a) shows a thin layer of soft material can be consistently removed by AFM tips (contact mode scanning) and accumulates at the borders of the scanning areas. This soft material is attributed to be resist residues as the same AFM scanning does not remove anything from a clean, freshly exfoliated MoS_2 surface. The thickness of the resist residues varies from 0.6 ~ 0.9 nm on different samples.

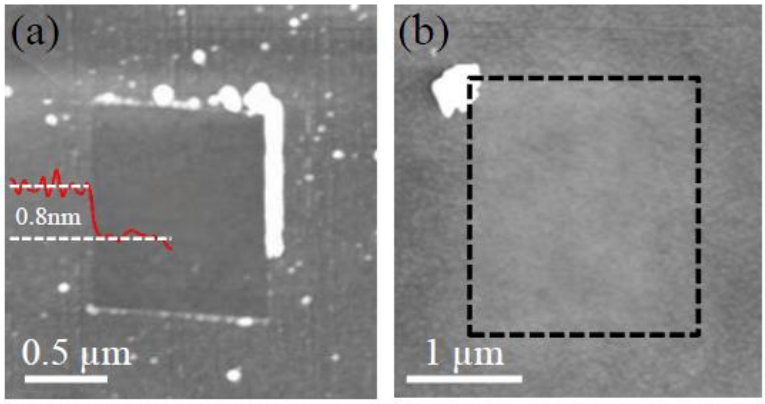


Figure 4-5. (a) AFM tapping mode image shows resist accumulation at the borders of a square area scanned by the tip in contact mode prior to the acquisition of this image. The line cut reveals a resist layer thickness of 0.8 nm. (b) Another AFM tapping mode image shows a clean surface after low-energy Ar^+ bombardment.

To remove the resist residues, we employed an *in-situ* gentle Ar^+ cleaning prior to contact metal deposition. This is the same technique discussed in Section 3.2.5 of Chapter 3. Using a discharge voltage $V_{\text{dis}} = 75\,\text{V}$ and emission current $I_e = 0.4\,\text{A}$, and irradiation time $t = 2\,\text{s}$ recipe, the resist residue layer is completely removed at the sacrifice of a small damage to the MX_2 sheet. Figure 4-5(b) is an example of a clean MoS_2 surface after the Ar+ cleaning. The image is taken using AFM tapping mode.

Later, we find using a larger e-beam dose of 510 $\mu C/cm^2$ gives a much better result, and this is the recipe we use now.

For resist develop, we use the following procedure. First, the chips are soaked in MIBK:IPA (1:1) solution (2 min), IPA solution (40 s), and DI water sequentially. After blow dry with N_2 gas, the exposed and developed regions are checked under an optical microscope. If no resist residues or signs of over develop are found visually, the chips are put back into the develop

solutions to over develop slightly. This time, the soaking time in MIBK:IPA (1:1) and IPA are 30 s and 10 s, respectively.

Metal deposition and lift-off.

The contact metals are deposited using a Lab-18 evaporation system (Kurt J. Lesker). Ti/Au (5nm/45) bilayer stacks are used for our early WSe_2 and WS_2 devices using exfoliated sheets from CVT-grown crystals and MoS_2 devices using CVD-grown monolayers. The deposition rate for Ti and Au are 0.5 Å/s and 1.5 Å/s, respectively. Later, we find Pd makes better contacts with exfoliated WSe_2. The deposition rate for Pd is 1.5 Å/s and the deposition thickness is 50 nm.

4.2.2 Electrical transport measurement techniques

Standard low-frequency (i.e. 4.3 Hz) Lock-in technique is employed in two-terminal and four-terminal electrical measurements.

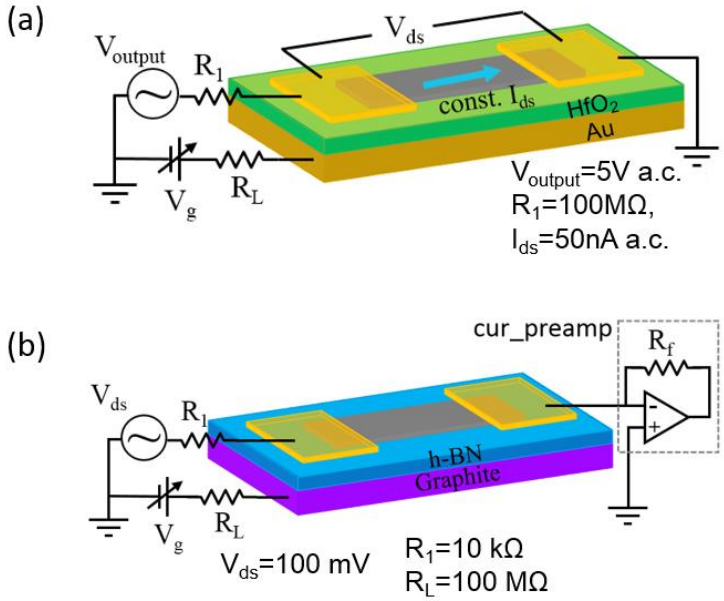


Figure 4-6. Schematics of electrical measurement setup for (a) constant current excitation and (b) constant bias excitation.

Two excitation methods, i.e. constant current and constant bias excitations, are used for conductance measurements depending on the impedance of the device. Figure 4-6 shows schematic diagrams of the measurement circuitry for the two excitation methods. The constant current excitation method is already discussed in Section 2.4.1 of Chapter 2. The only difference is the resistance of R_1 is 100 MΩ or 1 GΩ due to the large resistance of MX_2 devices. Because of the requirement in generating constant current source, this method can only be used to measure the high conductance state of the device. The advantage is that only a small current, e.g. a few nA to few tens of nA, is restricted to pass through the device to avoid joule heating and protect the device.

In order to measure the high resistance regime of the device, i.e. more than 10 MΩ, the constant bias excitation is employed. As Fig. 4-6(b) shows, the device is usually connected in series with a protective resistor R_1 (e.g. 10 kΩ or 100 kΩ), which serves to regulate the maximum circuit current when the device becomes very conductive. The current passing through the device is collected and amplified by the integrated current preamplifier of the Lock-in. It can detect current down to the level of pA accurately for our measurements. For measurements using this excitation method, the applied bias is usually small, e.g. 10mV to 100 mV at room temperature, so that device is operated in the linear IV regime.

The backgate voltage V_{bg} is applied either continuously using Keithley 2400 or in a pulsed fashion using a DAQ card (National Instrument). The advantage of pulsed gating is that it can eliminate hysteresis in electrical transport measurements as will be discussed later. The measurement protocols of this technique are designed by Dr. Bei Wang.[116]

4.3. Electrical transport measurement results

4.3.1 General electrical transport features of TMDC transistors

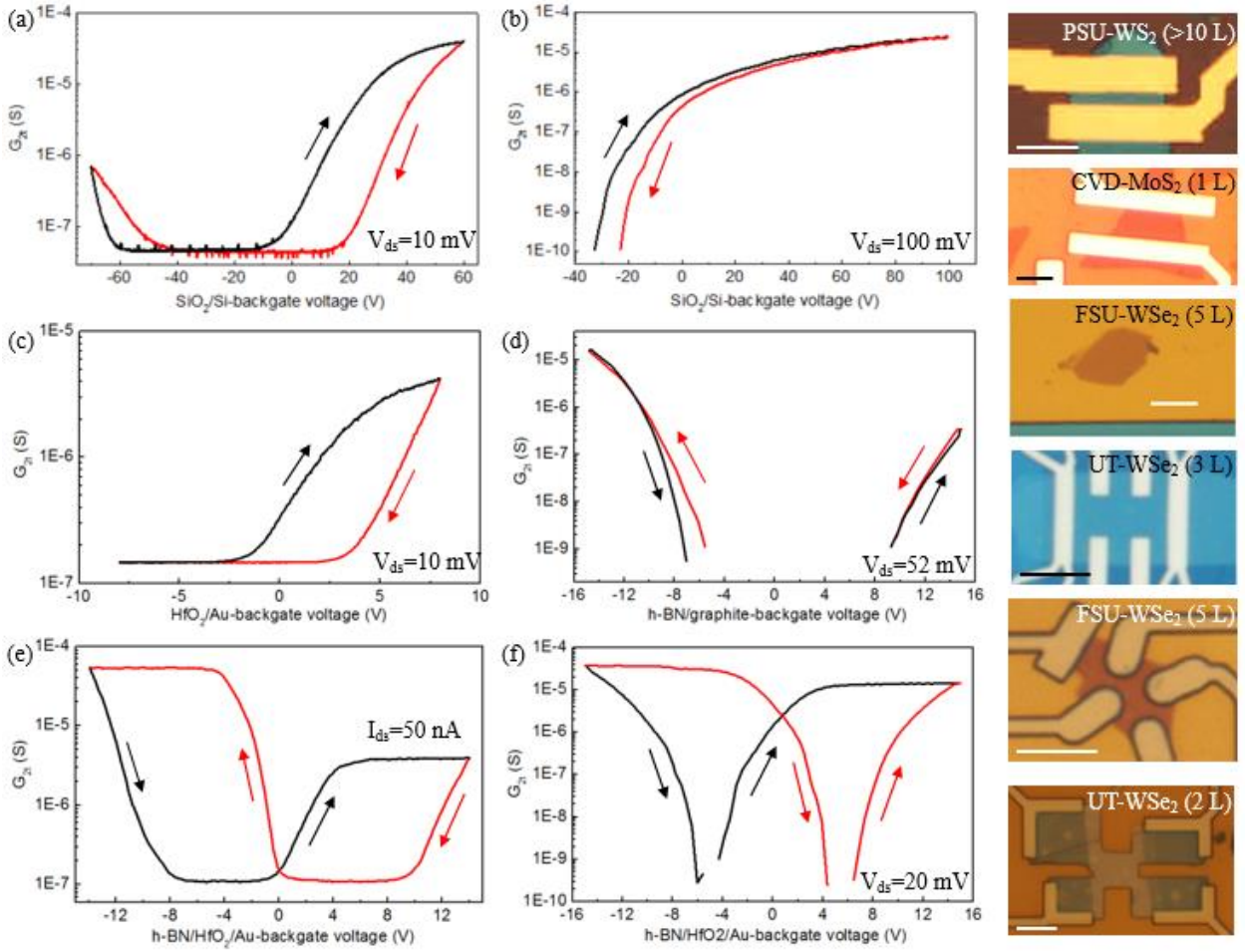


Figure 4-7. Representative two-terminal gate-dependent conductance curves shows common transport characteristics including ambipolar conduction with e-h symmetry and hysteretic transfer.

As described in Section 4.2, our TMDC devices are supported on various backgate structures. Figure 4-7 shows examples of room-temperature two-terminal gate-dependent conductance curves measured from (a) Ti/Au-contacted >10-layer PSU-WS_2 device supported on SiO_2/Si substrate; (b) Ti/Au-contacted 1-layer CVD-MoS_2 device supported on SiO_2/Si substrate; (c)

Ti/Au-contacted 5-layer FSU-WSe_2 device supported on HfO_2/Au substrate; (d) Pd-contacted 3-layer UT-WSe_2 device supported on h-BN/graphite substrate; (e) Ti/Au-contacted 5-layer FSU-WSe_2 device supported on h-BN/HfO_2/Au substrate; and (f) graphite-contacted h-BN sandwiched 2-layer UT-WSe_2 device supported on HfO_2/Au substrate. The gating efficiency from (a) to (f) are 7×10^{10} /cm^2/V, 7×10^{10} /cm^2/V, 3×10^{12} /cm^2/V, 6.1×10^{11} /cm^2/V, 1.3×10^{12} /cm^2/V, and 1.4×10^{12} /cm^2/V. The right panel shows optical pictures of the devices from (a) to (f). All scale bars are 5 μm.

First we describe the general features exhibited in these devices. They all show large current on/off ratios of $10^4 \sim 10^6$ due to the semiconductor band gaps. Ambipolar conduction behaviors with good electron-hole symmetry are usually observed in WS_2 and WSe_2 devices with small initial doping. MoS_2 devices only show conduction for electrons due to a large initial doping concentration, e.g. $> 3\times10^{12}$ /cm^2 for Fig. 4-7(b) and/or large Schottky barrier for holes. Hysteresis is usually present in devices with SiO_2/Si and HfO_2 backgate structures. According to the hysteresis direction, the origin is attributed to the excitation of slow charge traps residing in the oxide layers while the backgate voltage is applied continuously. As will be shown next, such hysteresis can be eliminated using a pulsed-gating technique. For devices supported on clean h-BN surface, the hysteresis is either absent or very small as is shown by Fig. 4-7(d). The hysteresis shown in Fig. 4-7(e) and (f) are not due to the charge traps as the WSe_2 sheets are supported on h-BN. As will be also discussed next, such hysteresis is found to be related to the applied gate voltage range, and only occurs after the gate voltage exceeds certain threshold values. Since it prevents accurate determination of the initial doping level in the TMDC devices, which is important for subsequent data analysis, the hysteresis needs to be eliminated.

4.3.1a Hysteresis elimination

First, we discuss the elimination of hysteresis in oxide-supported devices using a pulsed-gating technique. In this case, the hysteresis is caused by the excitation of slow charge traps in the oxide layer. In this technique, the gate voltage is applied in pulses with short duration, e.g. μs ~ ms, to quickly probe the charged state of the device. The probing time is short enough to avoid the excitation of slow charge trap states. This technique has been demonstrated to effectively suppress the hysteresis in carbon nanotube transistors.[117, 118] In our group, this technique has also been demonstrated to be effective in eliminating hysteresis in CVD-graphene transistors for bio-sensing applications.[23]

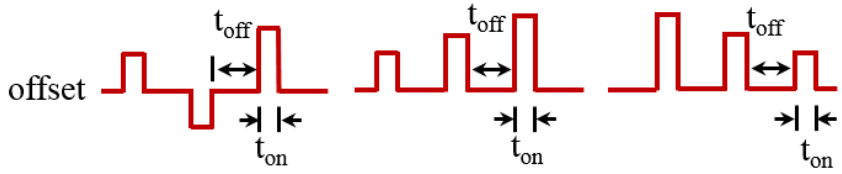


Figure 4-8. “p+-”, “p++” and “p--” pulse patterns used in pulsing-gate measurements.

Typically, three pulse patterns are involved in the pulsing-gate measurement, as shown in Fig. 4-8. Following Dr. Bei Wang’s definition, we name the three pulse patterns as “p+-”, “p++”, and “p--”. The offset value, where the gate voltage returns after pulsing, can be adjusted and is usually set at 0 V for most of the measurements discussed in this dissertation. t_{on} is the pulsing time and t_{off} is time at offset voltage in each cycle. It is found that $t_{on} = 25$ ms is sufficient and does not cause the slow charge traps to be activated.

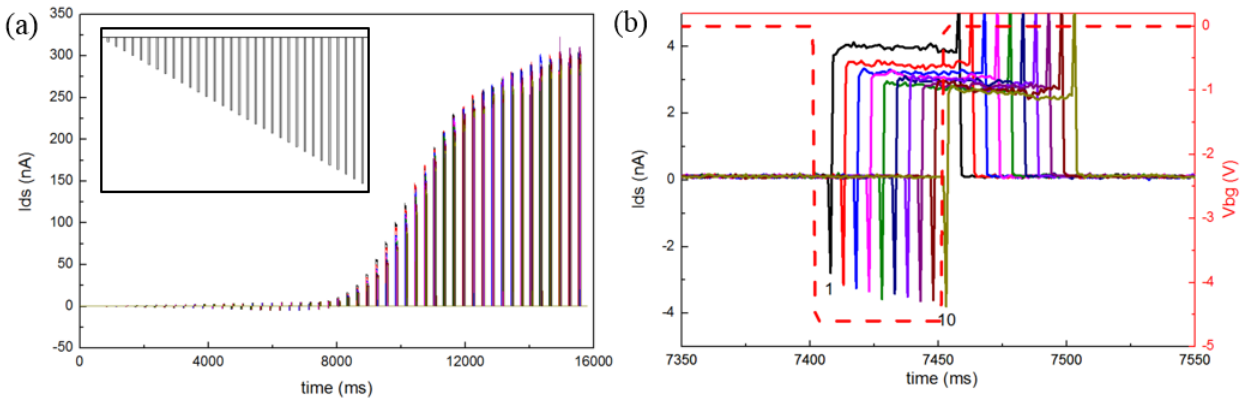


Figure 4-9. (a) Example of source-drain current response I_{ds} in pulsed-gating measurements. Inset shows the gate pulse pattern used. (b) A zoom-in plot of Ids for $V_{bg} = -4.5$ V.

In the pulsing-gate measurement, a small source-drain bias is applied in the linear IV regime of the device. For each measurement, the gate voltage sequence is repeated several times (cycles) in order to obtain stable source-drain current response, I_{ds}. Figure 4-9(a) plots I_{ds} for 10 cycles of the gate voltage sequence (inset). Figure 4-9(b) shows a zoom-in of I_{ds} for a pulsing gate voltage of V_{bg}= -4.5 V. The plateau region in each cycle is the actual current response, while the spikes are due to the digital switch between the gate offset and pulses. Also, there is a 5-tick delay from the Labview program, which shifts the I_{ds} curves from each other as Fig. 4-9(b) shows. The 1st and 10th cycle responses are indicated in the plot. As can be seen, the 1st (black) and 2nd (red) current plateau values are off from the rest by more than 0.5 nA. In general, the beginning 2 to 5 cycles are not stable and need to be taken out in averaging I_{ds}.

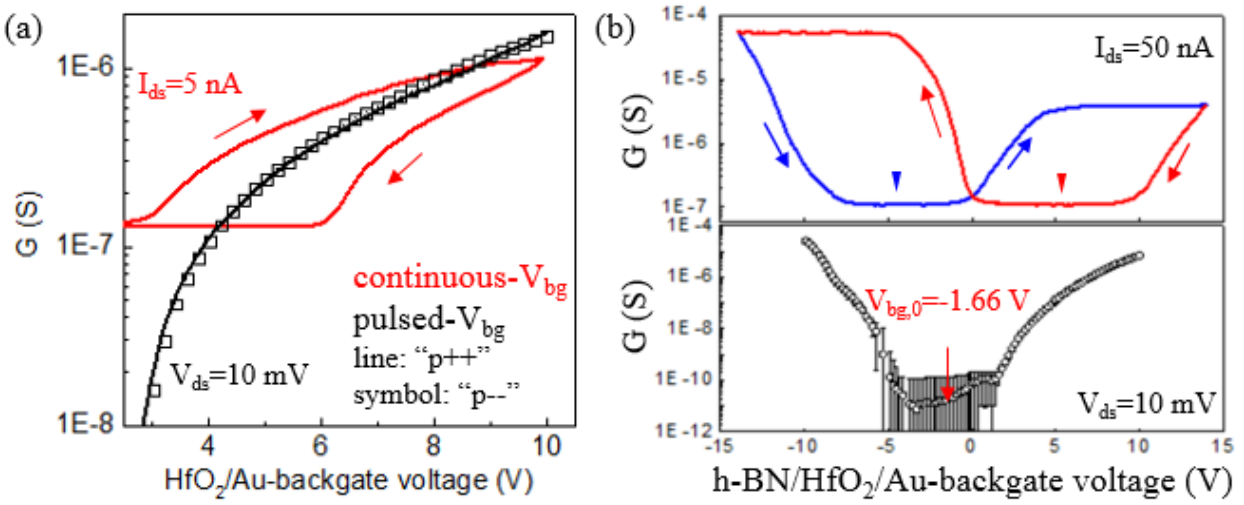


Figure 4-10. Comparison of $G(V_{bg})$ measured using the continuous and pulsed-gating techniques from (a) a 3-layer MoS_2 transistor and (b) a 5-layer FSU-WSe_2 transistor.

Next, we show an example of the hysteresis elimination. To mimic the forward and downward continuous gate sweeps, the "p++" and "p--" patterns are used to obtain the gate-dependent $G_{2t}(V_{bg})$ in Fig. 4-10(a) from an HfO_2-supported 3-layer MoS_2 device. The MoS_2 sheet is exfoliated from a commercial MoS_2 crystal (2D Semiconductors) The black line and symbol represent "p++" and "p--" pulsing-gate sweeps. As can be seen clearly, they overlap with each other very well, indicating the hysteresis is absent. As a comparison, the hysteretic transfer curve (red line) from continuous gate sweep is also plotted in the same graph with the hysteresis direction marked by the red arrows. The cut-off at ~ 10 MΩ is due to the constant current excitation method used in acquiring the data. Figure 4-10(b) compares $G(V_{bg})$ from continuous gate measurement (upper graph) and pulsing gate measurement (lower graph). Instead of having two fake CNP points, as marked by the blue and red triangles, the real CNP can be clearly determined from the pulsing-gate $G(V_{bg})$ curve, i.e. $V_{bg,0} = -1.66\,\mathrm{V}$. The corresponding initial

doping level is 2.16×10^{12} /cm^2/V using the gating efficiency $\alpha = 1.3 \times 10^{12}$ /cm^2/V and it is electron doped.

Now, we discuss the origin of the hysteresis exhibited in h-BN/HfO_2/Au supported devices, using the device shown in 4-7(f) for illustration. Hysteresis due to charge traps is usually very small or absent at low temperatures as most of the trap states are frozen. However, we find this is not the case for the hysteresis in h-BN/HfO_2/Au supported devices where the h-BN layer is usually very thin (< 10 nm). As Fig. 4-11(a) shows, the hysteresis persists at low temperatures down to 10 K. Hence, the origin of this type of hysteresis is not due to charge traps. Later, we find the magnitude of the hysteresis shows strong dependence on the gate sweep range. Figure 4-11(b) plots the conductance curves for three gate sweep ranges at 10 K. As can be seen, the hysteresis is reduced as the gate sweep range decreases from [-18V, +18V] to [-13V, +13V]. It is almost absent for the [-11V, +11V] gate sweep. Such behavior suggests there exists a threshold gate voltage, e.g. $V_{bg} = \pm 11$ V for Fig. 4-11(b), beyond which hysteresis starts to develop.

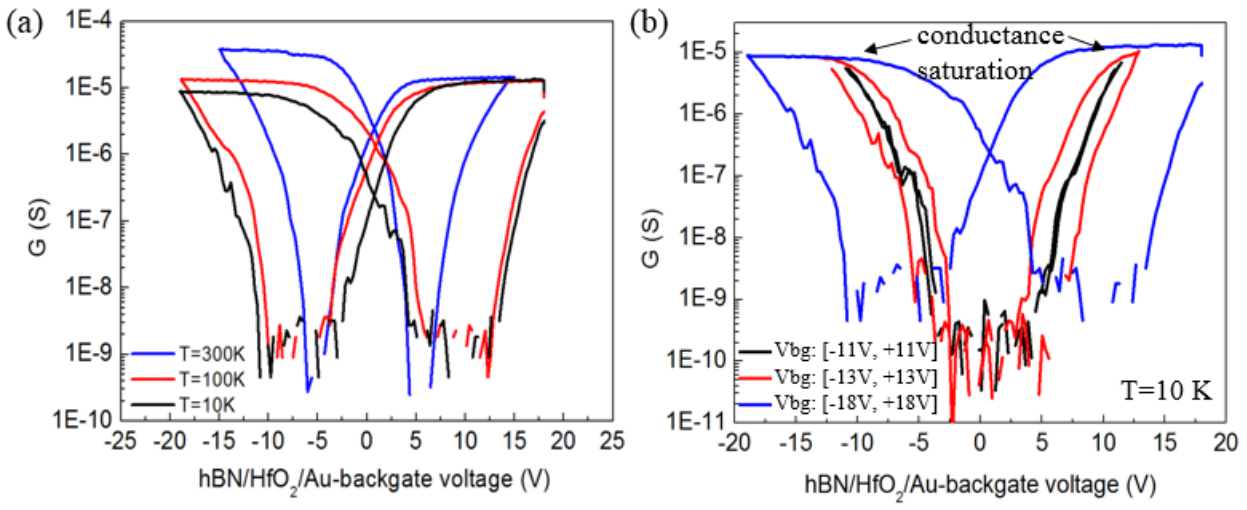


Figure 4-11. (a) Hysteretic $G(V_{bg})$ at T = 300K, 100K, and 10K. (b) $G(V_{bg})$ measured with different gate sweeping ranges at 10K.

In order to explain such unusual hysteretic behavior, we consider the breakdown situation of the thin h-BN layer (<10 nm). Here the quantum capacitance of WSe_2 is not considered. The h-BN layer in the device shown in Fig. 4-11 has a thickness of 5.8 nm and dielectric constant of 2.8, which corresponds to a capacitance per area $C_{\mathrm{h-BN}} = 0.42\ \mu\mathrm{F/cm^2}$. The bottom HfO_2 layer is 30 nm thick and has a capacitance $C_{\mathrm{HfO2}} = 0.48\ \mu\mathrm{F/cm^2}$ as determined from capacitance measurement. Using an in-series capacitor model, the gate voltage dropped across the h-BN layer is given by

$$\Delta V_{\mathrm{bg,h-BN}} = \frac{C_{\mathrm{HfO2}}}{C_{\mathrm{HfO2}} + C_{\mathrm{h-BN}}} V_{\mathrm{bg}} \tag{4.17}$$

Like any dielectric materials, the h-BN sheet also has a break down electric field strength E_{BD}, which is found to be dependent on the h-BN thickness according to the experiments in Ref. [119, 120] and [119, 120]. The h-BN crystals studied in the two reports and ours are all provided by Dr. K. Watanabe and Dr. T. Taniguchi's laboratory in Japan. According their experiments, E_{BD} of 5.8 nm h-BN sheet should be ~ 1.2 V/nm, which corresponds to an applied gate voltage of V_{g} =12.9 V from Eq. (4.17). This voltage is close to the hysteresis activation voltage of ±11V observed in Fig. 4-11(b). As V_{bg} further increases, the h-BN sheet can no longer sustain the excessive electric field and starts to break down. However, due to the existence of the bottom HfO_2 layer, the leakage current through the h-BN/HfO_2 stack is still small (less than 0.5 nA). So the breakdown of the h-BN sheet is reversible. The effect is the accumulation of mobile ions in h-BN which effectively shields the electric field, causing hysteresis in $G(V_{\mathrm{bg}})$ measurements and conductance saturation at high gate voltages.

4.3.1b Vacuum annealing effect

It has been reported that vacuum annealing at high temperatures (e.g. 120 ℃), leads to significant improvement in the contact resistance of MoS_2 devices supported on SiO_2/Si substrates.[121] We also test the vacuum annealing effect on our h-BN-supported WSe_2 devices.

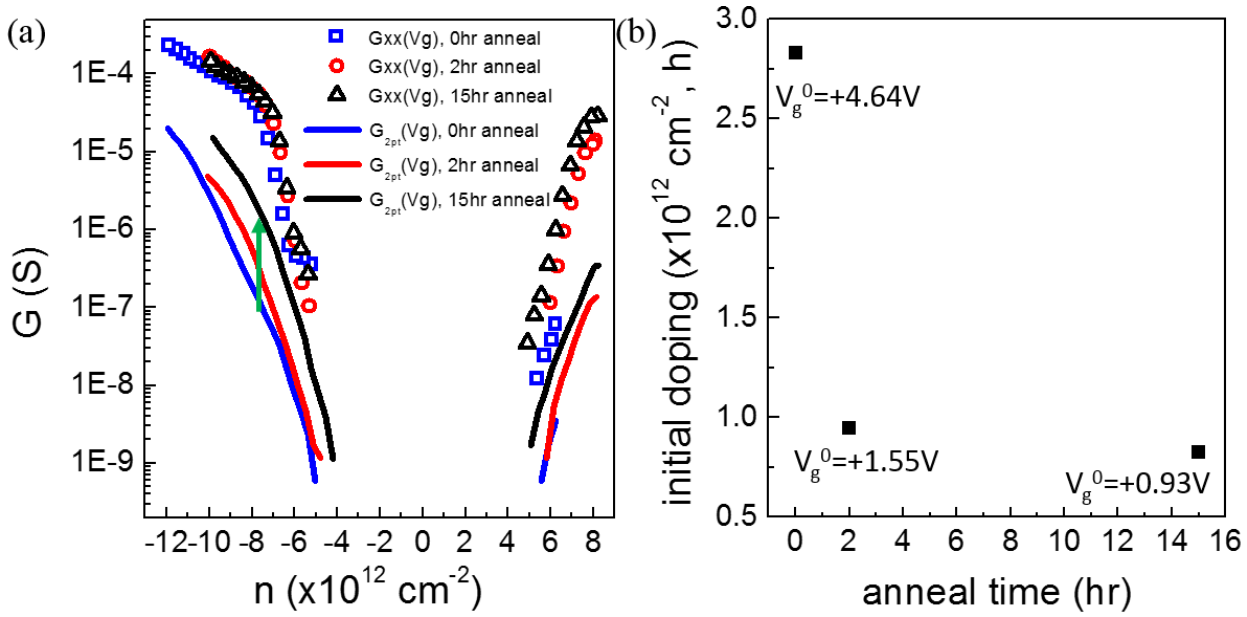


Figure 4-12. (a) Two-terminal and four-terminal $G(V_{bg})$ from a 3-layer UT-WSe_2 transistor at 300K after 0hr, 2hr, and 15hr accumulated vacuum annealing. (b) Initial doping level vs the accumulated vacuum annealing time.

Figure 4-12(a) shows the two- and four-terminal conductance G vs carrier density n as obtained from the hBN-supported 3-layer UT-WSe_2 device shown in Fig. 4-7(d). The device is measured in vacuum at 300K after being vacuum annealed for different time. The annealing is done at 400 K in a PPMS chamber. The top surface of WSe_2 is exposed to vacuum during the annealing and electrical measurements. The two-terminal conductance (solid lines) shows an enhancement by an order of magnitude as indicated by the blue arrow. However, the four-

terminal conductance, which is proportional to the sheet conductance, is almost not affected by the annealing. Figure 4-12(b) plots the initial doping level as a function of the accumulated annealing time. The initial 2 hour anneal causes a dramatic change in the initial doping density primarily due to the removal of charged dopants. After that, the shift in initial doping becomes very small, indicating that the neutral dopants are left and the effect is reducing the Schottky barrier height. However, the sub-threshold swings (SS) of the two-terminal conductance curves stay the same even after 15 hr anneal. This observation is consistent with the discussion in Section 4.3.4 where we demonstrate the SS is determined by the density of impurity states inside the WSe_2 band gap.

In the remaining of this chapter, we focus on WSe_2 transistors to discuss the gate-modulated conduction in the subthreshold regime and the metal-insulator transition (MIT) phenomenon.

4.3.2 Discussion on sheet conductance vs contact resistance of WSe_2 transistors

Because our analysis of the subthreshold conduction in WSe_2 transistors are based on two-terminal electrical transport measurements, we first show here a comparison between contact resistance and sheet resistance in Fig. 4-13 using the device shown in Fig. 4-7(d).

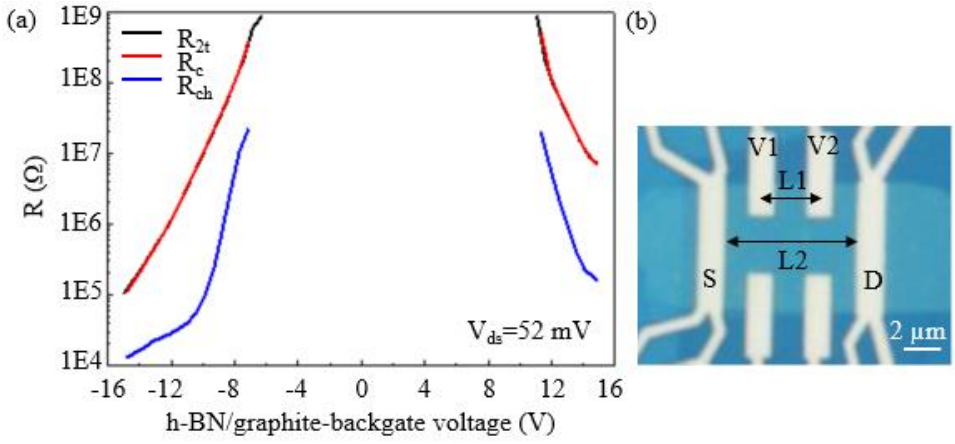


Figure 4-13. (a) Comparison of total, contact, and channel resistant from a 3-layer UT-WSe_2 transistor. (b) An optical image of the device.

The two-terminal resistance R_{2t} and four-terminal resistance R_{4t} are measured simultaneously using a standard low-frequency (4.3) Hz Lock-in technique and the constant voltage exciton method. The source-drain excitation bias is 52 mV. The WSe_2 channel resistance R_{ch} is estimated using a geometry factor L2/L1 by

$$R_{\mathrm{ch}} = \frac{L2}{L1} R_{4\mathrm{t}} \tag{4.17}$$

L2 is the edge-to-edge distance between the source and drain electrodes. L1 is the center-to-center distance between the two voltage probes used for four-terminal measurement. $\mathrm{L2/L1} = 2.2$. The contact resistance R_c is then obtained by subtracting R_{ch} from R_{2t}. As Fig. 4-3(a) clearly shows, R_c dominates over R_{ch} by at least an order of magnitude for conduction in the sub-threshold regime. The same conclusion is also reached by Liu *et al.*[122] through a systematic study of R_{ch} and R_{c} using a transfer length method. They find that R_{c} increases more rapidly than R_{ch} as the Fermi level E_{F} approaches the mid gap.

Hence, in the following analysis, we assume that $R_{\mathrm{c}} \gg R_{\mathrm{ch}}$ holds true in the deep subgap regime, where four-terminal measurements become impossible. This assumption is self-consistently justified following the analysis of Fig. 4-18 as will be discussed later.

4.3.3 Metal-insulator transition (MIT) in WSe_2 transistors

When disorders are present in a material, they give rise to localized states inside the band gap of the material. These states were first proposed by P. W. Anderson[123] and have the characteristics such that the wave functions of the charge carriers are localized in a small region

of space, i.e. Anderson localization. The energy level E_c (E_v) that separates the localized states from the de-localized states of the conduction (valence) band is known as mobility edge, as shown in Fig. 4-14(a). When a system is in the localized states, transport happens through quantum mechanical hopping from site to site. And the conductance pursues an insulating temperature dependence such that it decreases with decreasing temperatures. As the Fermi level moves beyond the mobility edge and into the conduction (valence) band, i.e. through doping enough electrons (holes), the system transitions into metallic state where the conductance now increases as temperature decreases. So, around the mobility edge carrier density n_c, there is a metal-insulator transition (MIT). For the TMDC material, the MIT phenomenon is commonly observed at carrier densities on the order of 10^{13} /cm^2.[106, 121, 124, 125] Figure 4-14(b) shows an example of the MIT in a single-layer MoS_2 transistor.[106] The highlighted red curve separates the insulating temperature dependence of the MoS_2 sheet conductance at low carrier densities from the metallic temperature dependence at high carrier densities. The mobility edge carrier density for this particular device is around 1×10^{13} /cm^2. This means there is a large amount of localized states inside the MoS_2 band gap, which need to be filled before the mobility edge is reached.

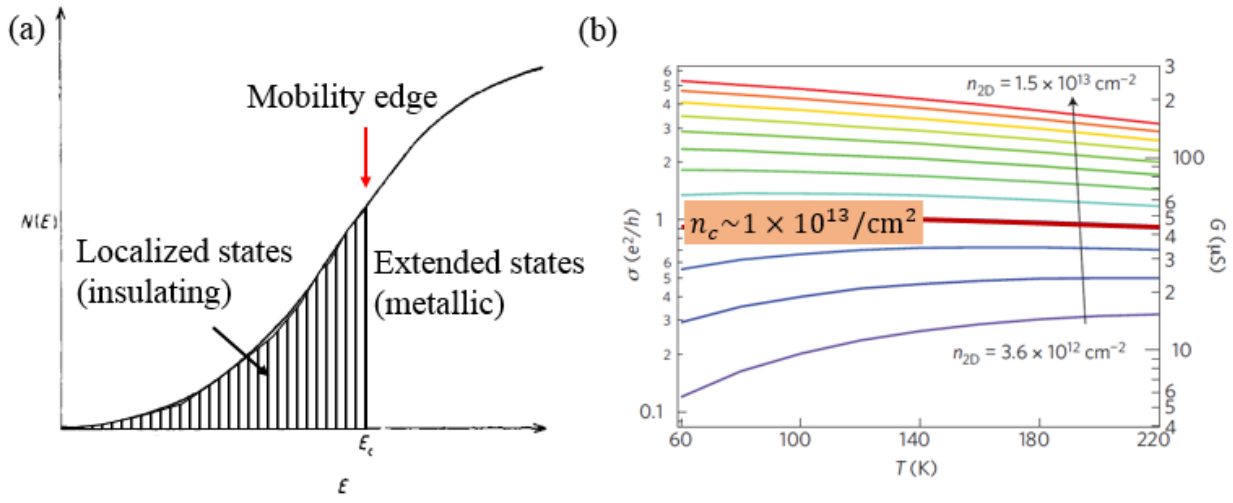


Figure 4-14. (a) Density of states $N(E)$ in a material with disorders showing the mobility edge Ec. Adapted from Fig. 1 of Ref. [126]. (b) Temperature dependence of the MoS_2 sheet conductance shows the presence of MIT. Adapted from Fig. 3 of Ref. [106].

The sheet conductance σ at the mobility edge carrier density n_c in the TMDC material and other systems, such as Si-MOSFET[127], is generally ~ e^2/h. This leads to

$$\sigma(n_c) = \frac{2e^2}{h} k_F \cdot l_e \sim \frac{e^2}{h} \tag{4.17}$$

$$k_F \cdot l_e \sim 1 \tag{4.18}$$

where $k_F = \sqrt{\pi n_c}$ is the Fermi wave vector and l_e is the carrier mean free path. Hence, if the mobility edge is reached at higher n_c, the mean free path will be shorter and sample quality is lower.

We perform temperature dependence measurement on the sheet resistance ρ(T) of the 3-layer UT-WSe_2 shown in Fig. 4-7(b). The result is shown in Fig. 4-15 for conductance with holes. The ρ(T) starts from strongly insulating at 0.88×10^{13} /cm^2 and becomes weaker as the hole density increases. For the high temperatures from 200K to 300K, the temperature dependence

behavior becomes metallic at large densities. However, this metallic behavior does not persist to lower temperatures due to the presence of a tipping, where the sheet resistance increases with decreasing temperature. This shows that a true MIT transition has not been reached at this carrier density and we caution the use of high temperature data to identify the MIT transition density. At 1.1×10^{13} /cm^2 the tipping becomes a log(T) dependence, i.e. weak localization for metals, and the sheet resistance is now below h/e^2. Hence, we estimate the mobility edge carrier density in this 3-layer WSe_2 is around 1.1×10^{13} /cm^2.

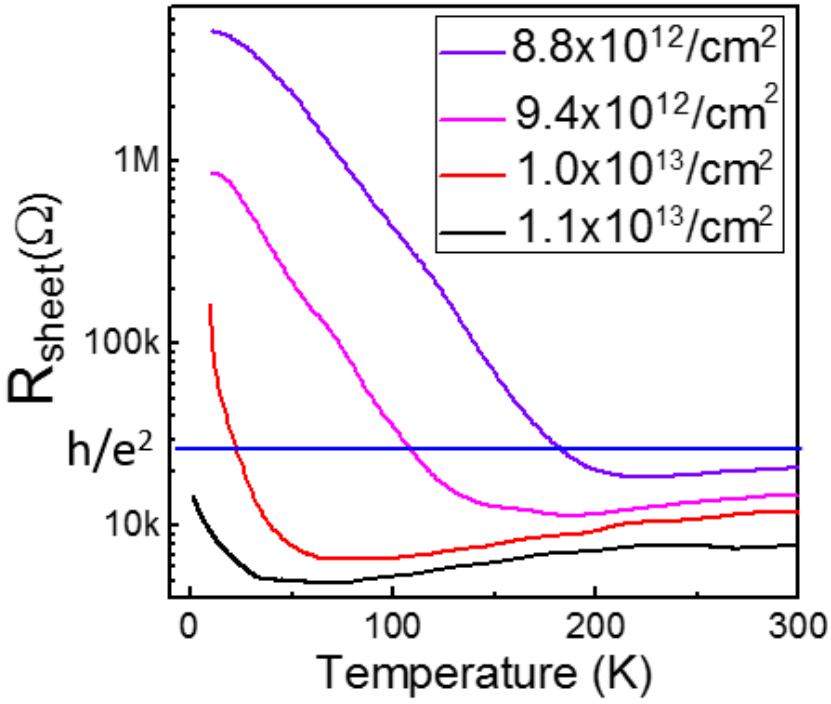


Figure 4-15. Temperature dependence of sheet resistance from the 3-layer UT-WSe_2 transistor at different carrier densities.

4.3.4 Electrical transport study of conduction behavior in the subthreshold regime

In this section, we focus on room-temperature conduction of WSe_2 transistors in the subthreshold regime, i.e. the movement of Fermi level is within the band gap. As already demonstrated in Section 4.3.2, the two-terminal device resistance is dominated by the contact resistance. Hence, we study the charge transport mechanisms at the metal-WSe_2 interface using the gate-modulated two-terminal conductance.

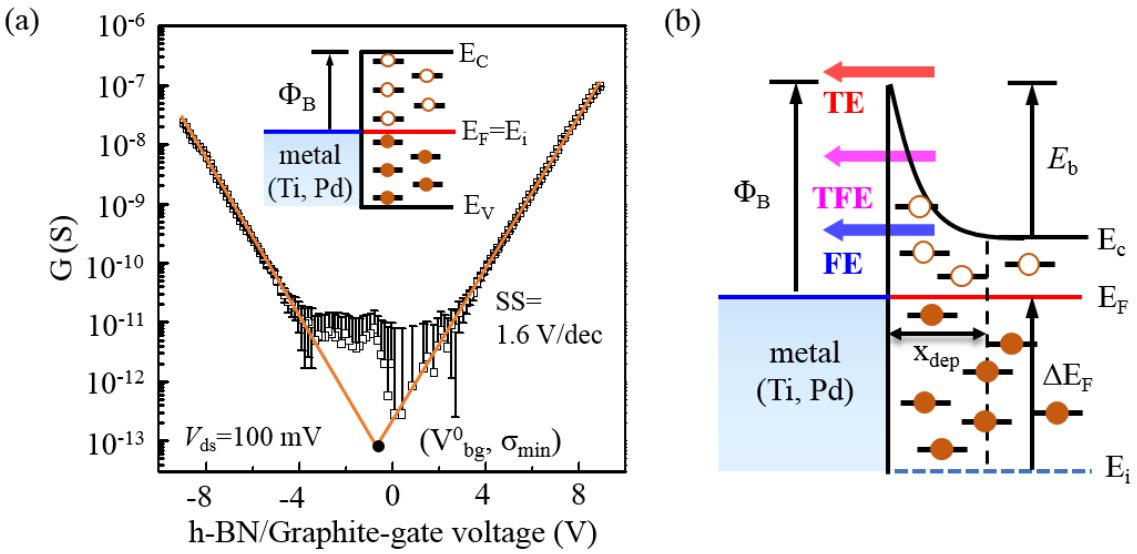


Figure 4-16. (a) Two-terminal $G(V_{bg})$ for a 3-layer FSU-WSe_2 transistor on h-BN in a semi-log plot. The absence of hysteresis indicates trap-free interface. Fits to log G vs V_{bg} yield SS of 1.6 V/dec for both electron and hole. The charge neutrality point occurs at V_{bg}^0= -0.58 V and G_0=8.7×10^{-14} S, the band diagram at which is shown in the inset. (b) Band diagram near the metal contact in the case of electron doping.

Figure 4-16(a) plots $G(V_g)$ of a Ti/Au-contacted 3-layer FSU-WSe_2 device supported on an h-BN/graphite substrate. The clean h-BN surface leads to no hysteresis in continuous V_{bg} sweep. A constant 100 mV source-drain bias is applied at 4.3 Hz. The symmetry between the electron

and hole conduction branches suggests the work function of Ti/Au contacts roughly aligns with the middle of the band gap E_i, as illustrated by the inset. As will be shown in Fig. 4-19 The same phenomenon is also observed in Pd- and graphite-contacted devices despite the different workfunction values. This suggests Fermi level pinning close to E_i, presumably by defect states of the WSe_2.[110] In the literature, the work function of a variety of contact metals is found to all lie close to the conduction band in MoS_2 transistors, presumably due to Fermi level pinning as well.[112] We approximately locate the charge neutrality point, where $E_\mathrm{F} = E_\mathrm{i}$, by extrapolating $G(V_\mathrm{g})$ of both carriers to the intersection of $V_\mathrm{bg}^0 = -0.58$ V and $G_0 = 8.7 \times 10^{-14}$ S. Here, the contact resistance is dominated by thermionic emission (TE) over the barrier $\Phi_\mathrm{B} = \Phi_\mathrm{B,n} = \Phi_\mathrm{B,p} = 1/2\, E_\mathrm{g}$. The two-dimensional current density J_TE is given by[108]

$$J = A_{2D}^{*} T^{3/2} \exp\left(-\frac{e\phi_\mathrm{B}}{k_\mathrm{B}T}\right) \times \left[\exp\left(\frac{eV_\mathrm{ds}}{k_\mathrm{B}T}\right) - 1\right] \tag{4.19}$$

and

$$A_\mathrm{2D}^{*} = \frac{(8\pi k_\mathrm{B}^3 m^{*})^{1/2} e}{h^2} \tag{4.20}$$

is the two-dimensional Richardson constant. In the linear IV regime, where V_ds is a small quantity, the exponential term $\exp\left(\frac{eV_\mathrm{ds}}{k_B T}\right)$ can be approximated as $\exp\left(\frac{eV_\mathrm{ds}}{k_\mathrm{B}T}\right) \approx 1 + \frac{eV_\mathrm{ds}}{k_\mathrm{B}T}$. Hence Eq. (4.19) can be rearranged to obtain the CNP conductance σ_0 as,

$$\sigma_0 = \frac{A_\mathrm{2D}^{*} T^{3/2} W}{k_\mathrm{B}T/e} \exp\left(-\frac{e\phi_\mathrm{B}}{k_\mathrm{B}T}\right) \tag{4.21}$$

Here W is the width of the WSe_2 channel. Using $m^*=0.5\ m_0$[92, 94, 128] and $W = 3$ μm for the WSe_2 device, we obtain an estimate of $\Phi_\mathrm{B} = 0.69$ eV and $E_\mathrm{g} = 1.38$ eV . This result agrees very well with the PL emission energy of 1.45 eV observed for 3-layer WSe_2 in Fig. 3-5(b).

The application of a positive (negative) V_{bg} moves E_F towards the conduction band edge E_c (E_v), creating band bending near the contacts as illustrated in Fig. 4-16(b). As is discussed in Section 4.1, the shape of the band and the width of depletion region depend on the impurity concentration N_i. In the case of WSe_2, N_i corresponds to the sub-gap impurity states as no dopants are intentionally introduced during the CVT synthesis process.

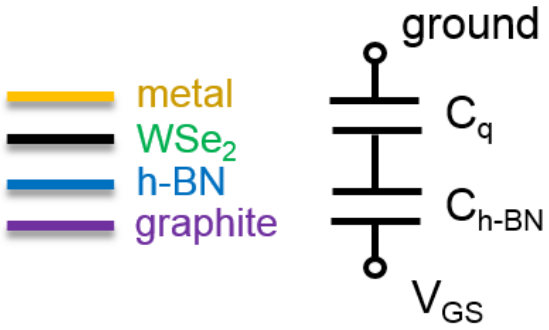


Figure 4-17. Schematics of two parallel-plate capacitors connected in series.

These impurity states lead to a non-zero quantum capacitance of the WSe_2 sheet. Hence the change of the Fermi level ΔE_F inside the WSe_2 band gap is only a portion of the applied gate voltage V_{bg}. An analytical expression for ΔE_F can be obtained using a two in-series capacitor model as shown in Figure 4-17. Here $C_q = e^2\rho(E)$ is the quantum capacitance of the WSe_2 sheet per area and $\rho(E)$ the DoS of the impurity states inside the band gap. C_{h-BN} is the capacitance of the h-BN layer. ΔE_F corresponds to the voltage dropped across the WSe_2 layer and is given by

$$\Delta E_F = E_F - E_i = \frac{eC_{h-BN}}{C_{h-BN} + C_q}\left(V_{bg} - V_{bg}^0\right) \tag{4.22}$$

Depending on the dielectric layer materials of the backgate structures, C_{h-BN} in Eq. (4.22) should be replaced with capacitance of the corresponding dielectric layer. It should be noted that Eq. (4.22) does ***not*** include the contribution of the charge trap states, since they are either absent

(in h-BN/graphite devices) or are not activated in measurements done with the pulsed-gating technique. Fast trap states with response time less than a few milliseconds have densities $\lesssim 1\times10^{12}$ /cm^2 for typical oxides[129], which is an order of magnitude smaller than C_q values extracted below.

Equation (4.21) has two limits. In the limit of $C_q \ll C_{h-BN}$, which can be realized in very clean samples or using electrolyte gating[130], $\Delta E_F = e\Delta V_{bg}$, i.e. the movement of E_F follows that of the gate voltage. In the opposite limit of $C_q \gg C_{h-BN}$, which corresponds to a large number of impurity states inside the band gap, moving E_F through the band gap requires a large gate voltage range of

$$e\Delta V_{bg} = \left(\frac{C_q}{C_{h-BN}}\right) \times E_g \tag{4.23}$$

The presence of the impurity states, however, reduces the depletion width of the Schottky barrier x_{dep} and promotes quantum tunneling through it, i.e. field emissions (TE) and thermionic field emissions (TFE), in addition to thermionic emission (TE) over the barrier.[131-133] As discussed in Section 4.1, the TFE mechanism combines both thermal excitation and quantum tunneling. Its 2D current density J_{TFE} (in the small V_{ds} limit) can be adapted from Eq. (4.15) and reads as:

$$J_{TFE} = \frac{A_{2D}^{**}\, T^{1/2}\sqrt{\pi E_{00} E_b}}{k_B \cosh(E_{00}/k_B T)} \exp\left[-\frac{E_c - E_F}{k_B T}\right] \exp\left[-\frac{E_b}{E_0}\right] \tag{4.24}$$

where $E_b = \Delta E_F$ is the band bending shown in Figure 4-16(b). The expressions of E_{00} and E_0 are already given in Eqs. (4.14) and (4.16), respectively.

The two exponential terms in Eq. (4.24) capture the two key ingredients of the TFE process, i.e. thermal activation to the conduction band edge and the tunneling process characterized by $\exp\left[-\frac{E_b}{E_0}\right]$. E_0 and E_{00} are important energy scales of the problem. A large N_i leads to large E_{00}

and E_0, which enhance the tunneling probability. Tunneling at the band edge, i.e. field emission, occurs when $E_{00} \gg k_B T$, e.g. in heavily doped semiconductors or at low temperature. When $E_{00} \ll k_B T$, carriers need to be thermally excited over the barrier (TE). TFE occurs in between the two limits, where tunneling occurs somewhere along the barrier as illustrated in Figure 4-16(b).

Equations (4.22) and (4.24) together lead to the expression for the sub-threshold swing $SS \equiv \left[\frac{d\log J}{dV_{bg}}\right]^{-1}$, and is given by

$$SS = \left(\frac{E_0}{E_0 - k_B T}\right)\left(1 + \frac{C_q}{C_{bg}}\right) \times \frac{k_B T}{e} \ln 10 \ /\text{dec} \tag{4.25}$$

Here, we neglect the weak V_{bg} dependence of the prefactors in Eq. (4.24). The 2D impurity density in a thin WSe_2 sheet is given by $N_i\, t$, where t is the thickness of the WSe_2 sheet. Assuming each impurity provides ~ one subgap state, $N_i\, t$ is approximately the same as the total number of subgap states, i.e.

$$N_i t = \rho(E) E_g = C_q E_g / e^2 \tag{4.26}$$

Here, we treat $\rho(E)$ and C_q as average quantities and replace integration with simple multiplication. $\rho(E)$ does appear to be approximately constant for a large range of subgap energy in our devices, as revealed by the linear log$G$-V_{bg} relation in Fig. 4-16(a) and Fig. 4-19 Equations (4.14), (4.16), (4.25) and (4.26) together allow us to self-consistently estimate the microscopic parameters N_i and $\rho(E)$ using the measured SS.

Equations (4.25) and (4.26) are combined to find E_0 as a function of N_i,

$$E_0 = \frac{k_B T}{1 - \left(1 + \frac{N_i t e^2}{C_{bg} E_g}\right)\frac{k_B T \log 10}{SS}} \tag{4.27}$$

From Equations (4.14), (4.16) and (4.26), E_0 and N_i also follows

$$E_0 = \frac{e\hbar}{2}\sqrt{\frac{N_\mathrm{i}}{m^* e}}\coth\left(\frac{e\hbar}{2k_\mathrm{B}T}\sqrt{\frac{N_\mathrm{i}}{m^* e}}\right) \tag{4.28}$$

To find the solutions for N_i and E_0, both Eqs. (4.27) and (4.28) are plotted in the same graph for each device. We then read the numeric values of the cross-over point to obtain N_i and E_0. We use m^*=0.5 m_0 and $\varepsilon = 4.63$ in our calculations.[134-136]

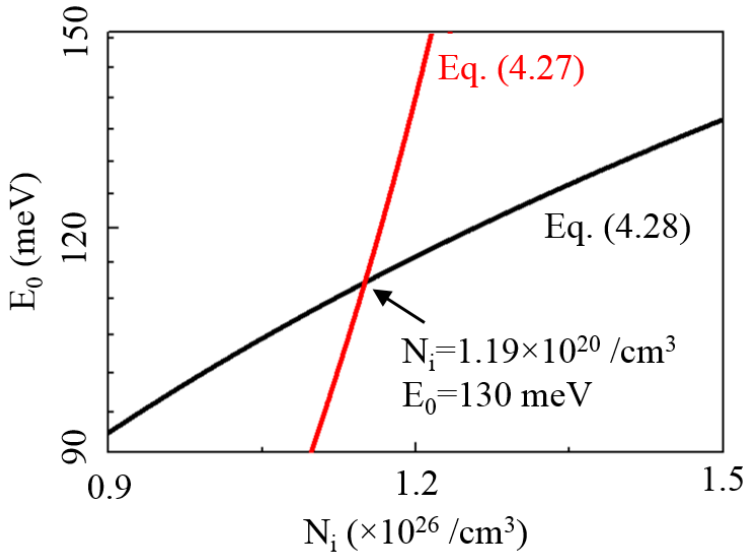


Figure 4-18. An example of the self-consistent determination of N_i and E_0.

Using SS = 1.6 eV and t = 2 nm for the 3-layer WSe_2 device in Fig. 4-16, we obtain $N_i = 1.19 \times 10^{20}$ /cm^3 and $E_0 = 130$ meV from the intersection point in Fig. 4-18. Then, the average density of impurity states ρ(E) can be obtained using Eq. (4.26) and $E_\mathrm{g} = 1.45$ eV. For this device, $\rho(\mathrm{E}) = 1.6 \times 10^{13}$ /cm^2/eV. E_{00} is 130 meV from Eq. (4.16) and equals to 5 k_BT at room temperature. This result validates the applicability of the TFE regime. $\rho(\mathrm{E}) = 1.6 \times$

10^{13} /cm^2/eV also predicts a mobility edge carrier density of $n(\mathrm{MIT}) = \rho(\mathrm{E}) \times (E_g/2) = 1.2 \times 10^{13}$ /cm^2, which is consistent with the observed values in our WSe_2 devices..

Similar analysis are performed on eight few-layer (1-5L) WSe_2 devices with different backgate structures as shown in Fig. 4-19. Overall, we find N_i to be in the range of 0.3-1.3×10^{20} /cm^3 and E_{00} in the range of 3-5 k_BT. The subgap localized DoS $\rho(E)$ ~ 1-2×10^{13} /cm^2/eV. Such large N_i is equivalent to heavy doping in conventional semiconductors, where TFE and FE transmissions are found to occur at room temperature.[108, 131, 132] The large N_i will also lead to substantial hopping conduction through the localized states in the WSe_2 channel. Since $\rho(E)$ is roughly a constant for a large range of subgap energies, this hopping conductivity maintains at a relatively high level. In contrast, the transmission through the Schottky barrier contacts exponentially decays as E_F moves towards mid gap. The different energy dependence provides a self-consistent justification of $R_c >> R_s$ in the subgap regime and explains the observations of ours and Liu *et al*.[137].

The above analysis makes it clear that the gate modulation of G_{2t} in our few-layer WSe_2 transistors is primarily achieved by controlling the transmission through the Schottky barrier contacts. This type of behavior, i.e. a Schottky barrier transistor, is also found in semiconducting carbon nanotubes.[138] Furthermore, the transmission through the contact barrier is a combination of thermal excitation and tunneling, due to a large number of states present inside the band gap that lead to reduced barrier width near the contacts.

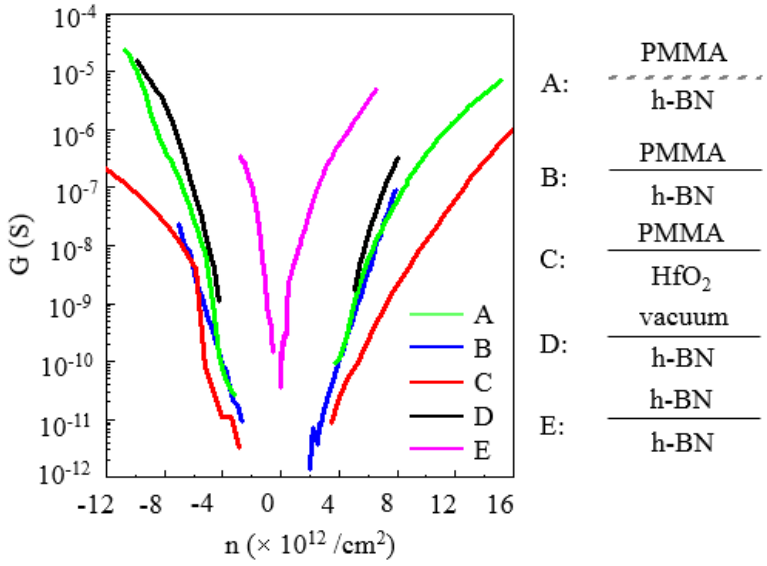


Figure 4-19. Comparison of devices in different dielectric environment. Two-terminal conductance *G* vs carrier density *n* for devices 5L-A, 3L-B, 5L-C, 3L-D and 4L-E. Schematics indicate the dielectric layers adjacent to the WSe_2 sheet. After accounting for the gating efficiencies, the SS slopes are very similar over a large range of subgap energies despite the large differences in substrate surface chemistry.

We have fabricated WSe_2 devices embedded in a variety of dielectric environment/encapsulation (combination of vacuum, PMMA, h-BN, SiO_2, and HfO_2) to shed light on the origin of the subgap states. Overall, we have not found any systematic dependence of $\rho(E)$ on the choice of the environment. As an example, Figure 4-19 compares G (n) of five devices embedded in different environment. All five exhibit similar SS slopes in the subgap regime while the chemistry of the substrate differs greatly. The *SS* remains large even in devices encapsulated by clean h-BN (device 4L-E). This indicates that at the level of 1×10^{13} /cm^2/eV, the subgap states are dominated by internal contributions rather than interface states that are known to exist in oxides. This is consistent given that oxide charge traps are typically on the order of 10^{11}-10^{12} /cm^2[129, 139, 140], which is too small to account for the $\rho(E)$ observed here. It should also be emphasized that scenarios explored here pertain to the range of E_F not too close to the

band edge. As Fig. 4-19 shows, G_{2t} (n) curves as E_F approaches E_c or E_v, suggesting the appearance of additional impurity states. Substrate-related impurity states are primary candidates.[141, 142] In addition, the assumption of $R_c >> R_s$ may not hold anymore as E_F approaches E_c or E_v and the contacts become transparent. Analysis of this regime thus requires the separation of the two, via four-terminal measurements for example.

Recent experiments and simulations have shown that a rich variety of structural defects, such as chalcogen vacancies and dislocations at grain boundaries, can create defect states with a wide span of subgap energies.[101, 143-145] Defect density on the order of 1%, such as that observed in STM studies of MoS_2[145] can potentially account for the phenomena observed here. In addition, few-layer TMDC devices are vulnerable against the degradation caused by interactions with the environment (e.g., oxygen, humidity), which may also play a role in creating additional impurity states.

4.4 Summaries

In summary, we studied the electrical transport properties of few-layer WSe_2 transistors in the subgap regime. We demonstrate that the gate modulation of the two-terminal conductance originates from controlling the thermionic field transmission through the Schottky contact barrier. Underlying such behavior is a large number of localized states inside the band gap of the material. Further understanding and elimination of these impurity states will prove essential towards improving the qualities of TMDC materials and devices, thus opening the door to the exploration of fundamental phenomena in these fascinating 2D systems.

Chapter 5

Thermoelectric transport properties of few-layer WSe_2

5.1 Introduction to thermoelectric (TE) materials and basic theory

Thermoelectric materials generally refer to materials with the conversion ability between thermal and electrical energies. An electrical potential can be induced when a temperature gradient is established in these materials, and vice versa. This phenomenon is called thermoelectric effect, which was first discovered by Thomas Johann Seebeck in 1821. So far, three types of the thermoelectric effect have been identified, i.e. Seebeck effect, Peltier effect, and Thomson effect.[146, 147]

Seebeck effect describes a direct conversion into electricity from a temperature difference across junctions of two different conductors. The strength of such effect is described by a Seebeck coefficient *S*, which will be discussed later in this section.

Peltier effect is the opposite way of energy conversion, where a current flow causes heating or cooling effects at junctions of two different metals with excellent electrical conductivity. This effect was first discovered in 1834 by French physicist Jean Charles Athanase Peltier.

Thomson effect describes the thermoelectric effect exhibited in an electrically homogenous material, involving both Seebeck and Peltier effects. Basically, if the Seebeck coefficient of a material has a temperature dependence, a series of thermal and electrical energy conversions can occur in the presence of a temperature gradient and current flow. This effect was theoretically proposed and later experimentally observed by Lord Kelvin in 1855.

The quality of a thermoelectric material is characterized by a dimensionless figure-of-merit[146]

$$Z = \frac{\sigma S^2}{\kappa} \tag{5.1}$$

where σ and κ are the electrical and thermal conductivities of the material. It represents a thermoelectric material's efficiency in generating thermoelectric power. Hence, enhancing Z is always the goal in thermoelectric material engineering. In order achieve this goal, enormous efforts have been devoted to find a material that is electrically highly conductive, i.e. large σ, but highly insulating thermally, i.e. large S and small κ.[146, 148-151]

In the remaining of this section, we will focus on discussing the Seebeck coefficient S, which is also known as thermoelectric power (TEP), and its relation with the electrical conduction σ. Compared with three-dimensional systems, low-dimensional nanomaterials has an advantage in enhancing the Seebeck coefficient. This is due to an increase in the density of states near the band edges when the charge carriers are confined in one or two dimensions.[152, 153]

The Seebeck coefficient is defined as

$$S = -\frac{\Delta V}{\Delta T} \tag{5.2}$$

where ΔV is the thermoelectric voltage created by the temperature difference ΔT. Due to the diffusion of charge carriers from high temperature to low temperature, an internal electric field builds up and opposes further diffusion of the charge carriers. Hence, depending on the carrier type, i.e. electrons or holes, S can be either negative or positive in the case of semiconductors.

For metals and doped semiconductors, the relationship between the electrical conductivity σ and Seebeck coefficient S is usually given by the semiclassical Mott relation[147, 154] as,

$$S = -\frac{\pi^2}{3}\left(\frac{k_B^2 T}{e}\right)\frac{1}{\sigma}\left(\frac{d\sigma}{d\varepsilon}\right)\Big|_{\varepsilon=\varepsilon_F} \tag{5.3}$$

Here the differential term $\left(\frac{d\sigma}{d\varepsilon}\right)\Big|_{\varepsilon=\varepsilon_F}$ is associated with the density of states (DoS) at a particular energy level. Therefore, S is more sensitive to the details of the electronic structure than σ.

The Mott relation has been successfully employed in providing quantitative explanations to the experimentally measured S for low-dimensional nanomaterials such as carbon nanotubes[155] and graphene[156].

Among the candidate thermoelectric materials, two-dimensional TMDC shows great potentials for enhancing the figure-of-merit through material engineering. An ultra-low cross-plane thermal conductivity of 0.05 W/mK has been reported in disordered WSe_2 thin films.[45] Seebeck coefficient of few-layer MoS_2 has been recently reported by Kayyalha *et al*.[157] showing carrier density dependence. *S* values exceeding 400 μV/K are observed at room temperature in bilayer MoS_2. [157] The goal of our study is to measure the Seebeck coefficient *S* in few-layer WSe_2 sheets and understand its carrier density and temperature dependences and their relation to electrical conductivity.

5.2 Preliminary thermoelectric transport measurements of few-layer WSe_2

The fabrication of WSe_2 thermoelectric field-effect transistors (TE-FETs) utilizes the same device fabrication techniques as described in Section 4.2 of Chapter 4. In our early devices, few-layer WSe_2 sheets are supported on SiO_2(300nm)/Si backgate structures. Finished devices are passivated with a layer of ALD-grown HfO_2 to isolate the device from ambient doping. Later, we adopt the h-BN/graphite backgate structure to take advantage of its clean h-BN surface and large gating efficiency to reach high doping level close to $1 \times 10^{13}\ /\mathrm{cm}^2$, so that we can study thermoelectric transport in the metallic state. In this case, exfoliated WSe_2 sheets are transferred to the h-BN/graphite substrate via the PMMA/PVA-stamp method.

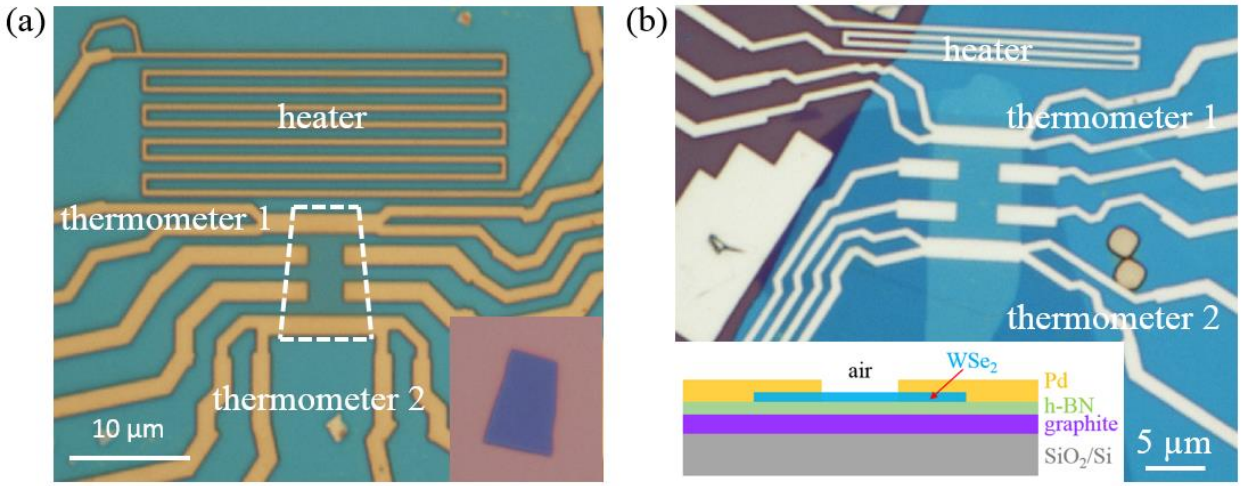


Figure 5-1. (a) An optical image of a 5-layer FSU-WSe_2 TE-FET. The inset shows an optical image of the WSe_2 sheet. (b) An optical image of a 3-layer UT-WSe_2 TE-FET. The inset shows a schematic cross-section view of the device structure.

Figure 5-1 shows two representative devices from (a) an SiO_2-supported Pd-contacted 5-layer FSU-WSe_2 TE-FET with HfO_2 passivation; and (b) an h-BN/graphite-supported 3-layer UT-WSe_2 TE-FET with no encapsulation layer. The inset of Fig. 5-1(a) is an optical image of the WSe_2 sheet. The inset of Fig. 5-1(b) is schematic diagram of the cross-section view of the device. The width of the heater wire is 0.4 μm and center-to-center distance between adjacent wires is 0.8 or 1.0 μm. The heater length L is usually designed to be 3 times the width of the WSe_2 piece such that heat diffusion along the device is close to uniform. The resistance change of the two thermometers is used to measure the temperature fluctuation. Because the device in Fig. 5-1(b) has a design issue which caused one of the 4 leads of thermometer 1 broken, hence it can no longer be used as a temperature sensor. So we focus on discussing thermoelectric measurement results from the device shown in Fig. 5-1(a).

5.2.1 Two-terminal electrical measurement results

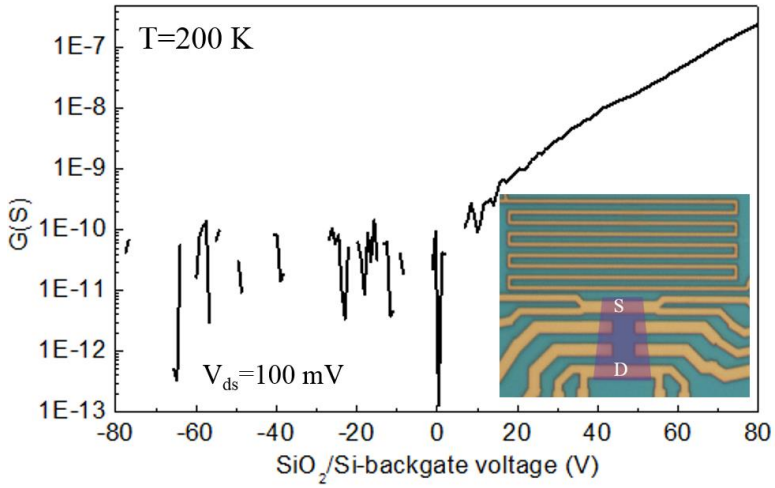


Figure 5-2. Two-terminal G(V_{bg}) at 200K. The inset shows an optical image of the device.

Figure 5-2 shows the 2-terminal conductance measured using the source and drain electrodes at 200K. The curve is acquired using the constant voltage bias method with $V_{\mathrm{ds}} = 100$ mV. The device only shows conduction on the electron side with a large contact resistance even at the maximum applied gate voltage, i.e. ~ 10 MΩ at $V_{\mathrm{bg}} = +80$ V. Because the hole conduction does show up, we can only estimate the initial electron doping is more than 2.8×10^{12} /cm^2 using $V_{\mathrm{bg},0} = -40$ V and $\alpha = 7 \times 10^{10}$ /cm^2/V. Such high initial doping levels might be due to the HfO_2 passivation layer or introduced during the ALD growth process, as FSU-WSe_2 devices without the HfO_2 capping layer usually show initial doping levels much less than 1×10^{12} /cm^2, as discussed in Chapter 4. Because of the large contact resistance, we are not able to perform four-terminal measurements to obtain the sheet conductance.

5.2.2 Preliminary Seebeck coefficient measurements

Now we discuss measurements of the Seebeck coefficient of the 5-layer FSU-WSe_2 TE-FET shown in Fig. 5-1(a).

5.2.2a Thermal test and measure protocols

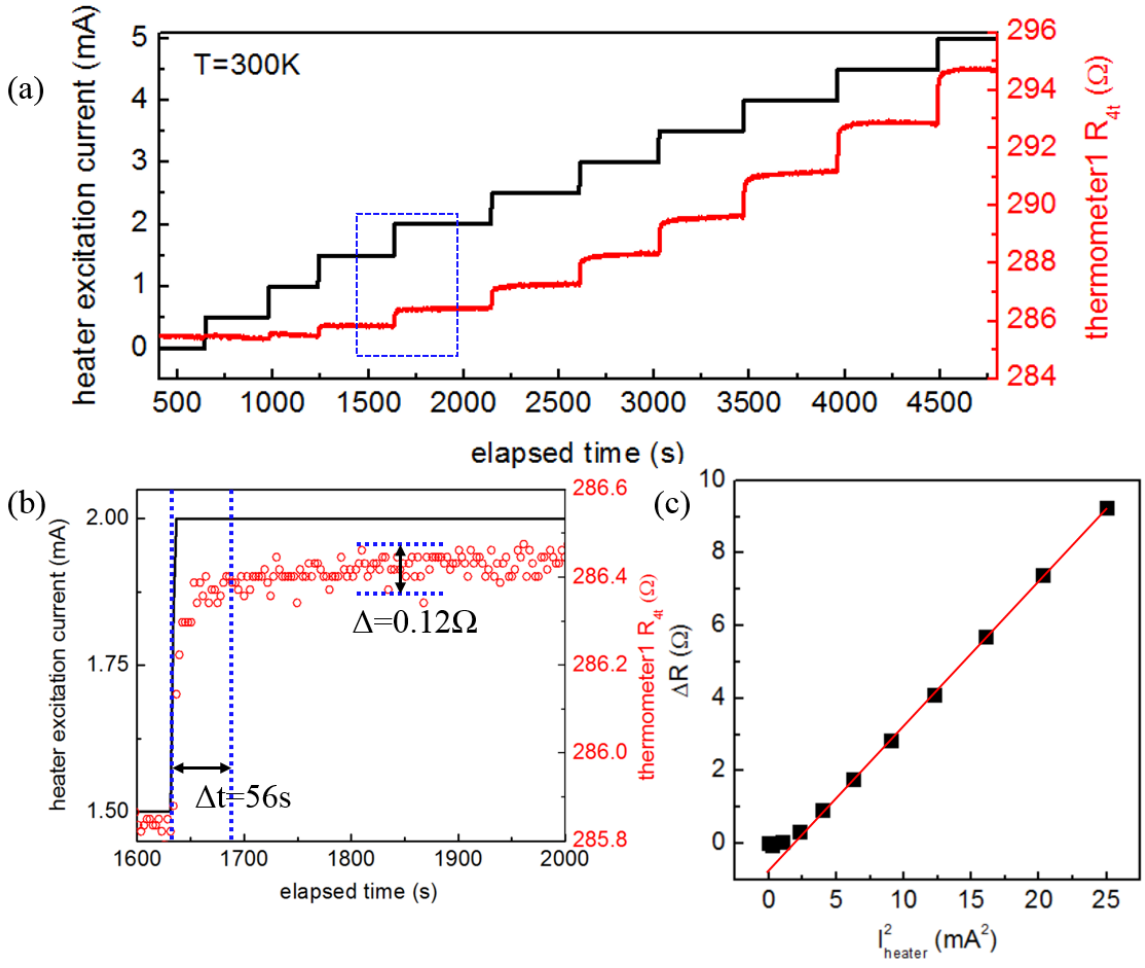


Figure 5-3. (a) Heater excitation current I_{heater} and the corresponding thermometer resistance as a function of the elapsed time. (b) Zoom-in of the circled region in (a). The peak-to-peak resistance fluctuation is 0.12 Ω. The rise time to a steady resistance reading is ~ 56s. (c) The thermometer resistance change as a function of I_{heater} square shows a linear relation.

We first check the applicability of the thermometers. This is done in ambient environment and using dummy devices which have the same electrode and heater structures but without the WSe_2 sheet. Figure 5-3(a) plots the applied heater excitation current I_{heater} (black line) and the corresponding thermometer resistance (red line) as a function of the elapsed time. Here the width, length and thickness of the thermometer are 0.3 μm, 30 μm and 71 nm, respectively. Figure 5-2(b) is a zoom-in on the region outlined by the blue dashed box in Fig. 5-3(a). As I_{heater} jumps from 1.5 mA to 2.0 mA, the thermometer resistance rises slowly at first until reaching a steady state. The rising time Δt is between 50 to 60 seconds. The peak-to-peak fluctuation of the thermometer resistance in a steady state is ~ 0.12 Ω, which cause an uncertainty Δ≈ 0.06 Ω in the measured thermometer resistance. Compared with the resistance change $\Delta R = 0.925\ \Omega$ from $I_{\text{heater}} = 0$ mA to $I_{\text{heater}} = 2.0$ mA, the uncertainly is about 6% of ΔR. Figure 5-2(c) plots the thermometer resistance as a function of the heater power, which is represented by the square of I_{heater} assuming a constant the heater resistance. The small deviation from the linear trend at small I_{heater} is probably due to the heating power being too small to cause temperature change at the thermometers or the heater is not heated up yet.

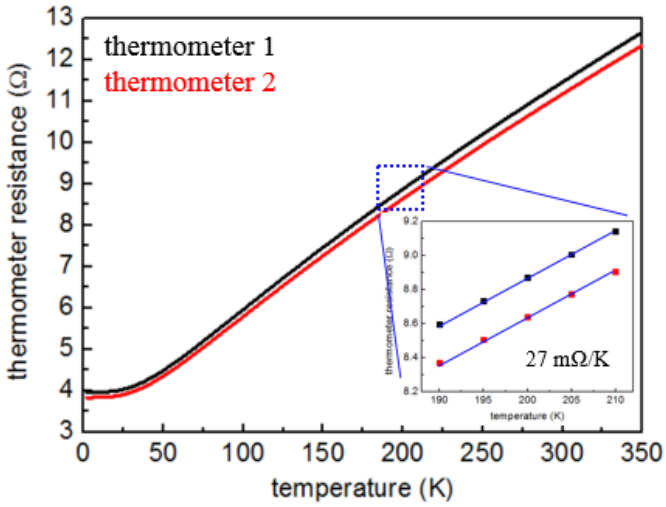


Figure 5-4. Temperature calibration of the Pd thermometer resistance. Inset is a zoom-in plot around T=200K showing good linear dependence within ±10K range.

Temperature calibration of the Pd thermometers is carried out using a physical parameter measurement system (PPMS). Figure 5-4 shows the temperature-dependence of the thermometer resistances of the 5-layer WSe_2 device. The inset is the *R-T* curve in the vicinity of $T = 200$ K showing good linear relationship at least within ±10 K range. The temperature sensitivity *sens.(*T*)* is obtained from linear fitting, and for $T = 200$ K, it is 0.027 Ω/K. The thermometer temperature change ΔT at any temperatures can then be obtained by

$$\Delta T = T - T_0 = \frac{R(T) - R(T_0)}{sens.(T_0)} \tag{5.4}$$

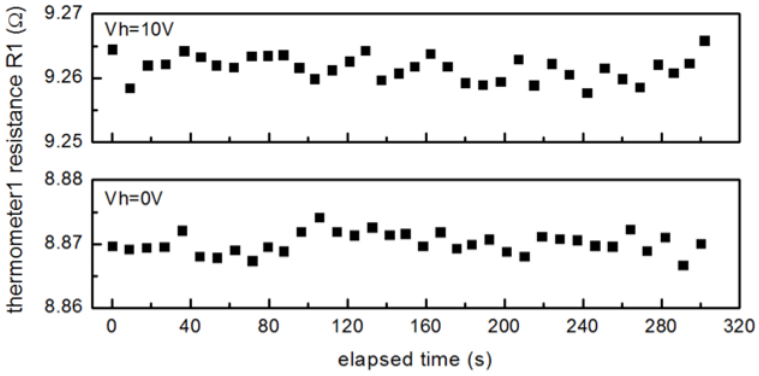


Figure 5-5. Thermometer 1 resistance stability check at V_h=0V and 10V. The base temperature is 200K.

To illustrate the measurement protocols for the Seebeck coefficient *S*, we use measurement results at 200 K base temperature. Constant DC voltage excitation V_h is applied to heat up the local heater. Figure 5-5 shows the resistance of thermometer 1, R_1, as a function of elapsed time at $V_h = 0$ V and 10 V. Overall, R_1 shows good stability with fluctuation less than 0.004 Ω. Thermometer 2 shows similar behavior with fluctuation less than 0.003 Ω. Using Eq. 5.4 and

$sens.(200\text{K}) = 0.027\ \Omega/\text{K}$, we obtain the temperature difference between the two thermometers to be $\Delta\text{T} = 2.889$ K due to the local heating at $V_\text{h} = 10$ V.

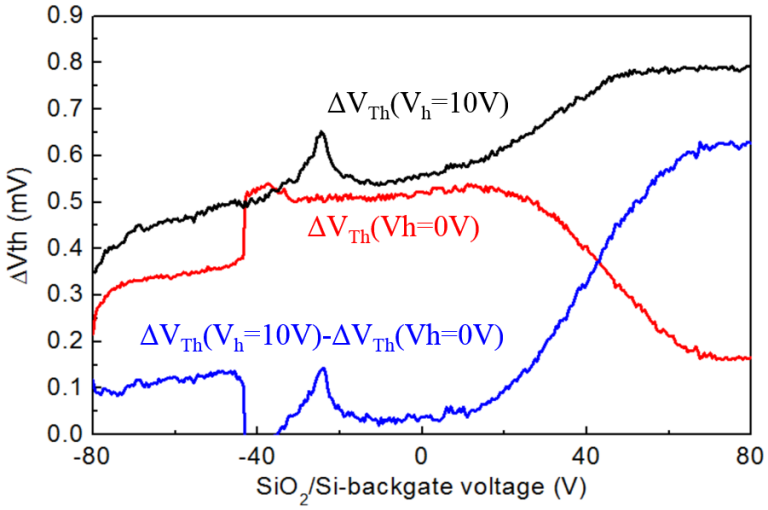


Figure 5-6. Thermoelectric voltage ΔV_Th vs V_bg for V_h=0V (red curve) and 10V black curve). The blue curve is obtained by subtracting the red curve from the black.

After determining ΔT, the two thermometers are used as voltage probes to measure gate-dependence of the thermoelectric voltage ΔV_Th. The backgate voltage is initially applied in a continuous fashion for carrier modulation while the ΔV_Th is recorded simultaneously. Figure 5-6 shows ΔV_Th as a function of V_bg for $V_\text{h} = 0$V (red curves) and $V_\text{h} = 10$V (black curves). The blue curve is obtained by simply subtracting the red curve from the black one. Surprisingly, we see a background ΔV_Th signal with V_bg dependence when the heater is off, i.e. $V_\text{h} = 0$V. Theoretically, V_bg should be 0 at all backgate voltages as there is no temperature gradient along the WSe_2 piece. But the non-zero, V_bg-dependent ΔV_Th at $V_\text{h} = 0$ V suggests that there is current flowing between the two thermometers. Assuming this is primarily due to the current flowing through the WSe_2 piece as the 300 nm SiO_2 is much insulating compared with WSe_2. The order of magnitude of the

V_{bg}-induced current $i(V_{bg})$ can be estimated using the two-terminal conductance $G(V_{bg})$ shown in Fig. 5-2, and it is given by

$$i(V_{bg}) = \Delta V_{Th}(V_h = 0V) \times G(V_{bg}) \quad (5.5)$$

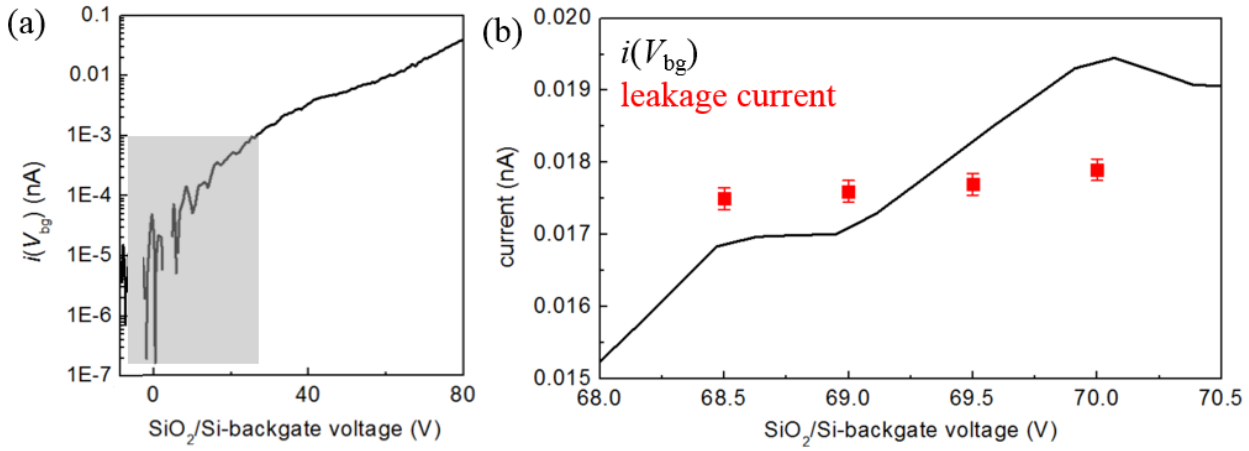


Figure 5-7. (a) $i(V_{bg})$ vs Vbg obtained using Eq. (5.5). (b) Zoom-in for V_{bg} from +69.0V to +70,5V. The discrete red symbols are leakage current measured by parking V_{bg} at selected voltages.

To test this assumption, we connect both thermometer electrodes to a current preamplifier to collect and measure the current that passes through the two thermometers, i.e. leakage current, when V_{bg} is parked at different values. Figure 5-6(a) plots the calculated current $i(V_{bg})$ obtained using Eq. 5.5. $i(V_{bg})$ and $G(V_{bg})$ shown in Fig. 5-2. The data corresponding to current less than 1 pA is not reliable as Eq. 5.5 is based on the assumption that the WSe_2 sheet is more conductive than the SiO_2 layer. Figure 5-7(b) shows $i(V_{bg})$ at large V_{bg} from +68.0 V to +70.5 V, where the WSe_2 sheet becomes less insulating with $R(V_{bg})$ on the order of 10 MΩ. The red symbols are leakage currents measured at different parked gate voltages. Based on the assumption expressed by Eq. (5.5) $i(V_{bg})$ should be comparable to the leakage current, and this is indeed the case.

Unfortunately, such background $\Delta V_{\mathrm{Th}}(V_{\mathrm{bg}}, V_{\mathrm{h}} = 0\mathrm{V})$ due to a small current (<0.1 nA) flowing through the WSe_2 piece itself cannot be avoided.

In order to obtain the actual $\Delta V_{\mathrm{Th}}^{*}(V_{\mathrm{bg}}, V_{\mathrm{h}} = 10\mathrm{V})$, we subtract the background $\Delta V_{\mathrm{Th}}(V_{\mathrm{bg}}, V_{\mathrm{h}} = 0\mathrm{V})$ from the measured $\Delta V_{\mathrm{Th}}(V_{\mathrm{bg}}, V_{\mathrm{h}} = 10\mathrm{V})$, as is shown by the blue curve in Fig. 5-6.

$$\Delta V_{\mathrm{Th}}^{*}\big(V_{\mathrm{bg}}, V_{\mathrm{h}} = 10\mathrm{V}\big) = \Delta V_{\mathrm{Th}}\big(V_{\mathrm{bg}}, V_{\mathrm{h}} = 10\mathrm{V}\big) - \Delta V_{\mathrm{Th}}(V_{\mathrm{bg}}, V_{\mathrm{h}} = 0\mathrm{V}) \qquad (5.6)$$

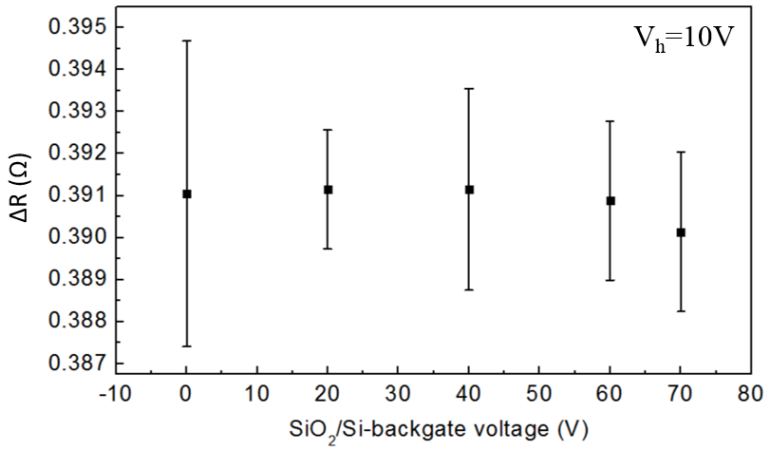


Figure 5-8. Thermometer resistance change ΔR vs V_{bg} at 10V heater excitation voltage. 200K base temperature.

The effect of V_{bg} on the thermometer resistance change when the heater is excited with $V_{\mathrm{h}} = 10\mathrm{V}$ is also studied, and the result is shown in Fig. 5-8. Since the thermometer resistance is usually measured by passing a large excitation current, e.g. a few hundred nA, the small leakage current can be neglected. Hence, there should be no V_{bg} dependence, which is exactly what Figure 5-8 shows.

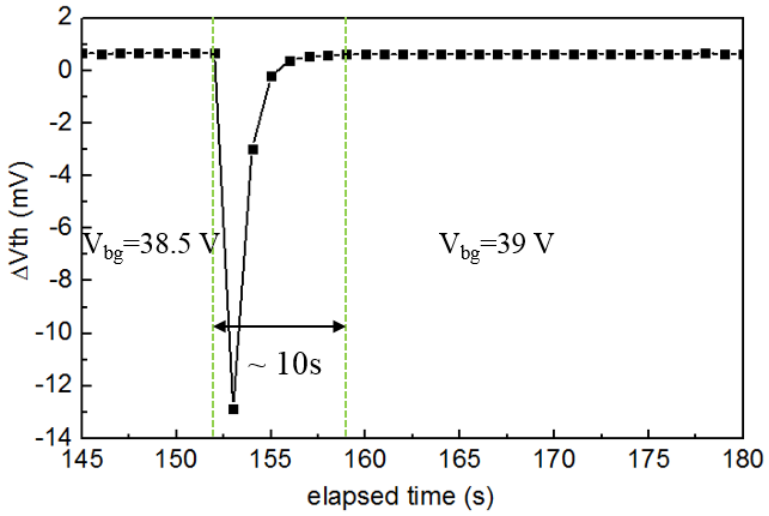


Figure 5-9. Thermoelectric voltage ΔV_{Th} vs time as Vbg is stepped from +38.5V to +39V. It takes about 10s for ΔV_{Th} to become steady.

Besides measuring ΔV_{Th} as V_{bg} is swept continuously, we also record the time response of ΔV_{Th} as V_{bg} is switched between two voltages. As an example, Figure 5-9 plots ΔV_{Th} as a function of elapsed when V_{bg} is steped from +38.5 V to +39 V. The sharp dip is caused by the switching of V_{bg}. It takes about 10 seconds for ΔV_{Th} to become stable after V_{bg} is increased to +39V. Such long stabilization time may cause the ΔV_{Th} measured in a continuous V_{bg} sweep to be underestimated.

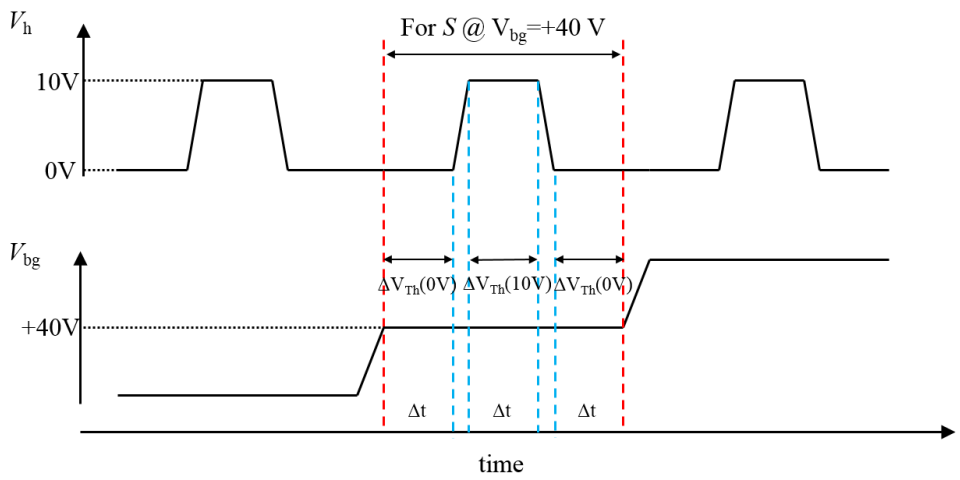


Figure 5-10. Schematics of the Seebeck coefficient measurement protocols for future experiments. ΔV_{Th} is only taken at parked V_{bg}.

Hence, for future measurements of the gate-dependent Seebeck coefficient $S(V_{\mathrm{bg}})$, we adopt the following measurement protocols as schematically shown in Figure 5-10. For example, after V_{bg} is ramped to +40 V from previous voltage, it is parked there and triggers the heater excitation voltage V_{h} to be applied to the heater. V_{h} is first kept at 0 V for a time interval of Δt to measure the background ΔV_{Th}; then it is ramped up to 10 V and parked there for another Δt to measure the corresponding ΔV_{Th}; after that, V_{h} is ramped back to 0 V and hold for another Δt while ΔV_{Th} is measured again for stability check later. When this dwell at $V_{\mathrm{h}} = 0$ finishes, it triggers V_{bg} to go to the next voltage.

5.2.2b Preliminary results of Seebeck coefficient

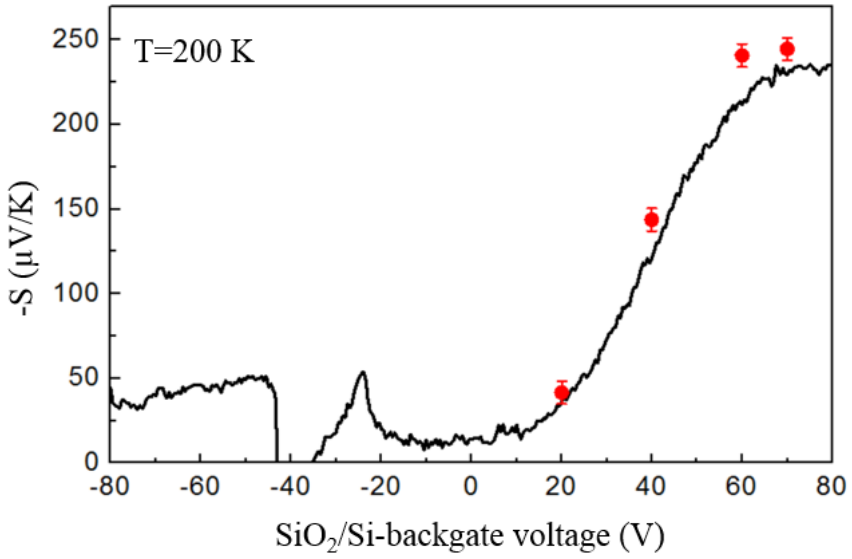


Figure 5-11. Seebeck coefficient S vs V_{bg} at T=200K. The black curve is obtained using ΔV_{Th} from continuous V_{bg} sweep, and the red symbols are generated using ΔV_{Th} measured at parked V_{bg}.

Figure 5-11 shows the gate-dependent Seebeck coefficient S calculated using $\Delta T(V_h = 10V) = 2.889$ K. ΔV_{Th} used in plotting the black curve is from the continuous V_{bg} sweep shown by the blue curve in Fig. 5-6. The red discrete data points are obtained using ΔV_{Th} when V_{bg} is parked at +20V, +40V, +60V, and +70V, each with a dwell time of 30 seconds. As can be seen from the graph, |S| of the red data points are consistently larger than the black curve. This result points out the importance of measuring ΔV_{Th} at parked V_{bg} rather sweeping continuously. Despite the discrepancy between the two measurements, they all show the same trend that as V_{bg} increases, S increases. Similar behaviors have been observed in MoS_2 devices, where S at high carrier densities (hole type) reaches a few hundred μV/K. [157]

5.3 Summaries

In conclusion, we have performed measurements on the Seebeck coefficient *S* from a 5-layer WSe_2 TE-FET device. Preliminary results show that as the backgate voltage modulation moves the Fermi level from close to the middle of band gap to the conduction band edge, S shows an increasing trend and reaches beyond 200 μV/K, which is much larger than the reported values for carbon nanotube[155, 158] and graphene[156]. However, due to the limited gating capability of the SiO_2/Si gate and large initial hole doping concentration (i.e. 2.8×10^{12} /cm^2 for the 3-layer WSe_2 device), we are not able to move the Fermi level above the mobility edge to study the thermoelectric transport in the conduction band. We also notice that a small current of a few tens of pA due to the application of the backgate voltages causes a non-zero thermoelectric voltage background. This background signal is more prominent in the deep subthreshold regime and gets smaller as WSe_2 becomes more conductive. As it cannot be avoided, careful attention should be paid in measuring the thermoelectric voltages. In order to systematically study the correlation between the Seebeck coefficient and electrical conductivity, as well as various intrinsic and extrinsic scattering mechanisms, new batches of devices need to be fabricated using gate structures with capability of doping carriers beyond 1×10^{13} /cm^2, such as using high-quality ALD-grown HfO_2 as the gate dielectric.

Chapter 6 Conclusions

Graphene and TMDC serve as important metallic and semiconducting building blocks in the family of two-dimensional materials. Their interesting and novel properties in electronics, optoelecronics, mechanics, etc., have attracted intense attention in both fundamental studies and exploration for future applications. We have discussed in this dissertation our work in the experimental studies of both materials and provide directions for future studies.

Low-temperature pulsed-CVD method for graphene synthesis on copper is demonstrated to effectively reduce the occurrence of multilayer patches in terms of size, density and total coverage percentage through controlling the growth parameters, i.e. flow of Ar/H_2 and methane precursors, growth and etching time in each growth cycle. Monolayer graphene films with complete suppression of multilayers have been achieved under optimized growth condition. Carrier mobility obtained from all GFETs shows a distribution which centers around 18,000 cm^2/Vs. The achievement of such high mobility is attributed to a significant reduction of metallic contaminations attached to the graphene film. This is realized by introducing a diluted SC-2 cleaning step.

Physical properties of different TMDC crystals and alloys grown by the CVT technique are characterized by TEM, XRD, Raman, PL, AFM, KPFM, and SThM. TEM and XRD give both in-plane and out-of-plane lattice constants and confirm the 2H structure of our WSe_2 crystals. 2LA(M)-to-$A_{1g}(\Gamma)$ intensity ratio from Raman spectra of WS_2 using 514 nm laser excitation is shown to be a characteristic feature to identify mono-, bi-, and tri-layer WS_2. Using PL spectroscopy, we observe strong luminescence signal due to direct gap emissions in WSe_2 monolayers. The presence of lattice defects give rise to another PL peak at lower energies, which is associated with defect-bound exciton emissions. The FWHM of PL spectra from monolayer

WSe_2 is found to shrink with decreasing temperatures until 150 K, below which it saturates at a narrow width of 15 meV. Such narrow width indicates the high sample quality. The workfunction of WS_xSe_{2-x} alloys are studied using KPFM with various concentration *x*. We find the alloy workfunction increases from ~4.52 eV to ~ 4.74 eV as *x* increases from 0 to 2.

We also study the gate-modulated conduction of few-layer WSe_2 FETs in the subthreshold regime. We find conduction in the threshold regime is dominated by contact resistance and shows Schottky barrier transistor behaviors. Our results demonstrate the dominant carrier transport mechanism through the metal contacts is the thermionic field emission in the subthreshold regime. Such behavior is due to a large number of localized states inside the band gap of WSe_2, whose density is self-consistently determined to be approximately $1\sim2\times10^{13}\ /\mathrm{cm}^2/\mathrm{eV}$. The origin of these impurity states is suspected to come from the material itself rather than the dielectric environments. In order to study the intrinsic electronic properties of WSe_2 and other TMDC materials, the density of these impurity states need to be either reduced through improved synthesis or completely filled using gate structures with doping capabilities well beyond $1\times10^{13}\ /\mathrm{cm}^2$.

The carrier density dependence of Seebeck coefficient *S* of few-layer WSe_2 is measured by modulating the applied gate voltages. Our preliminary results show *S* increases as the Fermi level approaches the conduction band edge and reaches beyond 200 μV/K at high carrier densities. Further experiments are required to systematically study the thermoelectric transport properties of WSe_2 as well as other TMDC materials.

Appendix A

Lithography recipes

A.1 Metal contacts deposition on TMDCs

As discussed in Chapter 4, Ti/Au or Pd are used for contacts in TMDC devices. The deposition is carried out in a thermal/electron beam evaporator (Kurt J. Lesker Lab-18) in the cleanroom of the Penn State Nanofabrication Lab. The system has a load locked deposition chamber which is always maintained at a low pressure (10^{-7} to 10^{-8} Torr). Inside the deposition chamber, there is a rotating substrate stage with cooling capability to -20 ℃ located at the top, and sources for e-beam/thermal deposition are at the bottom. On the side wall is a Kaufman-Robinson ion source which can generate diffusive argon ion beams with energies from 35 to 150 eV. Figure A-1 is a schematic drawing of the deposition chamber.

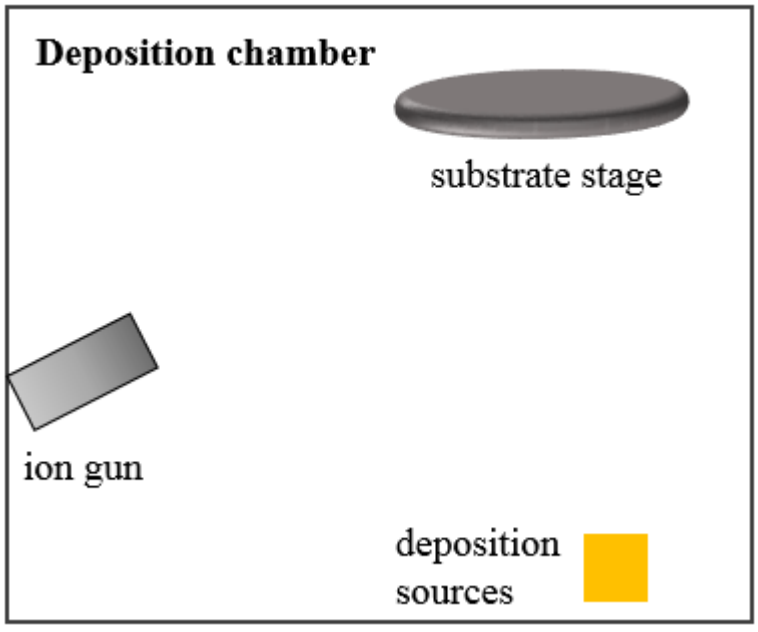


Figure A-1. Schematics of the Lab-18 deposition chamber with an integrated ion gun.

Generally, we set the substrate stage temperature to 10 ℃ for Ti/Au and Pd deposition to avoid overheating of the e-beam resist or photoresist. Lower temperature, such as 0 ℃, is also used when depositing Pt, which often requires larger electron beam power and leads to higher chamber temperature. It is also important to check the pressure in the deposition chamber prior to loading the sample in it. If the chamber pressure is greater than 5×10^{-7} Torr, then we usually do a dummy deposition of titanium (1.5 Å/s, 50 nm) to bring the pressure down to ~ 1×10^{-8} Torr level before transferring the real samples in. During the deposition, we keep the substrate stage rotating.

For the Ti/Au deposition, we usually deposit 5 nm Ti at 0.5 Å/s, followed by 45 nm Au at 1.5 Å/s.

A.2 Embedded local backgate fabrication process

To fabricate the embedded local backgates, we first use photolithography to pattern the local backgate structures on a 4 inch SiO_2(290 nm)/Si wafer(Nova Electronic Materials). Using the photoresist layer as a mask, the top SiO_2 layer is etched down by ~ 60 nm using chlorine plasma. The actual etching depth is determined with AFM measurement. As the last step, Ti/Au bilayer is deposited into the etched regions such that the Au surface is close to the nearby un-etched SiO_2 surface.

A.2.1 Backgate structure patterning

The photolithographic patterning process includes *photoresist spin-coating*, *UV light exposure, resist develop*.

Photoresist spin-coating: The 4 inch SiO_2/Si wafer surface is first rinsed with IPA and blown dry with clean N_2 gas. Then it is spin-coated with photoresist 3012 at 4000 r.p.m. for 45 seconds followed by 1 minute, 95 ℃ baking on a hot plate.

UV light exposure: The backgate structure patterns are projected onto the resist-covered SiO_2/Si wafer from the photolithography mask using a Stepper system (GCA 8000), as is shown in Figure A-2(a). The exposure time is set to be 0.55 seconds.

Resist develop: The wafer is then soaked in a CD-26 developer solution for 1 minute to dissolve away the UV-exposed photoresists, and followed by soaking and rising in DI water for before blown dry with N_2 gas.

A.2.2 Etching

After develop, photoresist at the un-exposed regions remains and acts as a mask for the SiO_2 etch. Chlorine plasma generated in an inductively coupled plasma (ICP) etcher (PT Versalock 700) is used for etching. After etch, a small piece is cut off from the 4 inch wafer and the photoresist on it is washed off using PG Remover. The exact etching depth is then measured by AFM. It should be noted that long etching time is not necessary as it could remove the protective photoresist layer or etch through the SiO_2 layer. Usually, we aim for an etching depth between 50 nm to 100 nm. The last etching time of 130 seconds removed ~ 60 nm SiO_2.

A.2.3 Metal deposition

Au is deposited into the SiO_2 trenches such that the Au surface has nearly the same height as the nearby SiO_2 regions. We use Lab-18 for the deposition. The actual deposition thickness is always larger than the target thickness by ~ 50%. So to accurately control the deposition

thickness, the over-deposition percentage, α, needs to be known. Then the set-point thickness for Au is given by SiO_2 trench depth/(1+ α). A 5 nm Ti layer is deposited prior to Au deposition as an adhesion layer. The deposition recipe is the same as in A.1. After deposition, the photoresist layer is washed off in PG Remover.

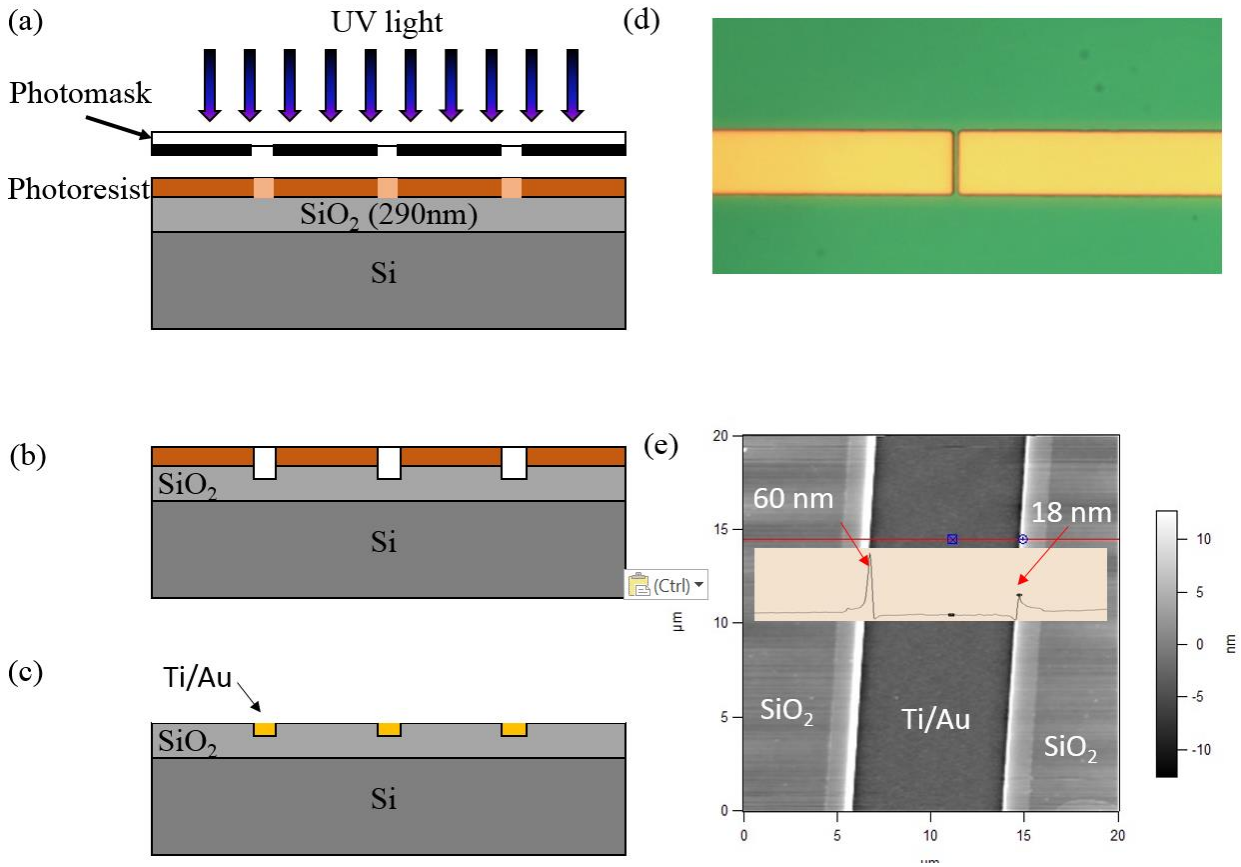


Figure A-2. Fabrication process of the embedded local backgates.

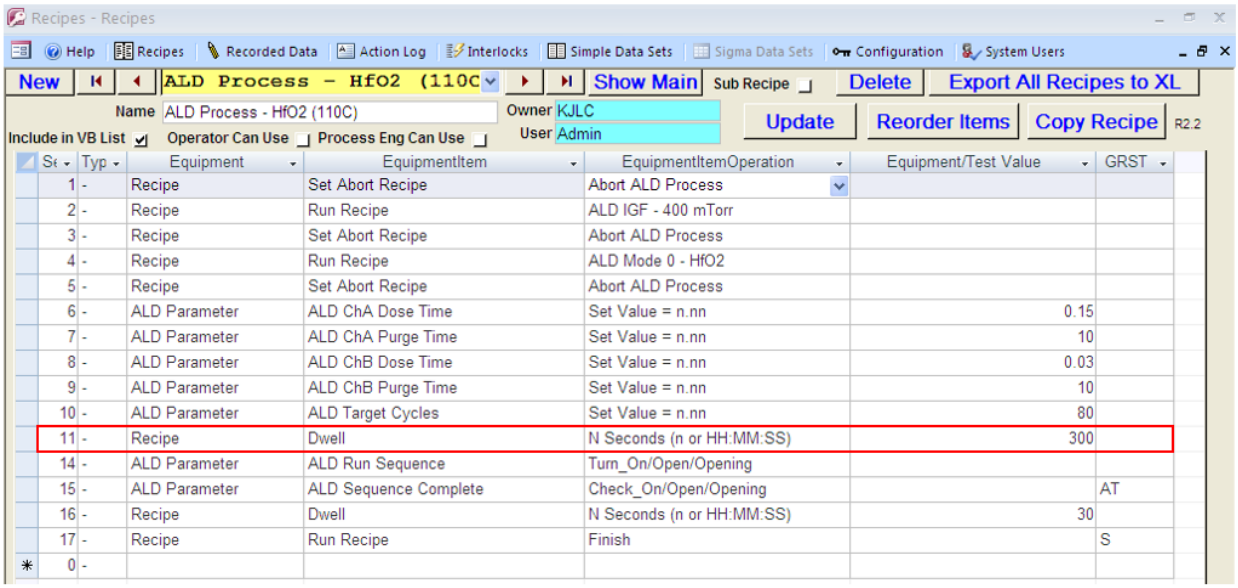
A.3 ALD growth of HfO_2, leakage test and capacitance measurement

A.3.1 ALD growth of HfO_2

We use atomic layer deposition (ALD) to grow thin film of HfO_2 (30 or 40 nm) over different materials, such as graphene, SiO_2, and thin film metal. The ALD equipment is Kurt J.

Lesker ALD150LX. The ALD process for HfO_2 involves two vapor phase precursors, i.e. hafnium and water vapor, which are alternatively pulsed into the deposition chamber to grow HfO_2 at the atomic level via self-limiting surface reactions. Each growth cycle begins with a t_1 pulse dose of hafnium vapor followed by t_2 N_2 purging. Then a t_3 pulse dose of water vapor is supplied for oxidation followed by t_4 N_2 purging before the next cycle begins. The recipe we use for HfO_2 deposition is: t_1=0.15 s, t_2=10 s, t_3=0.03 s, and t_4=10 s. The growth rate per cycle is 1.26 Å/cycle. We normally grow 30 ~ 40 nm HfO_2. The growth temperature is 110 ℃. It is recommended to put a piece of bare silicon wafer and a piece of gold-coated silicon wafer alongside the deposition wafer. After the deposition, the HfO_2 covered Si wafer can be used to accurately determine the as-deposited HfO_2 film thickness by ellipsometry. The HfO_2/Au/Si wafer is used for subsequent leakage test and capacitance measurement of the as-deposited HfO_2 film.

After loading samples into the deposition chamber, there is usually a 5 minutes pumping and baking step before the growth starts. This step is highlighted by the red box in Figure A-3, which is a screenshot of the recipe program for 110 ℃ HfO_2 ALD. It is ok to have this purging step if no polymer seeding layer is required for the growth. For HfO_2 growth on graphene, a seeding layer (MMA-MAA copolymer residues) is necessary for successful growth, otherwise the growth will result in pin holes. In order to preserve the seeding layer, the dwell time of the pumping and baking (step 11) must be set to 0 so that the deposition cycles begin immediately after all the temperatures reach their set points.



St	Typ	Equipment	EquipmentItem	EquipmentItemOperation	Equipment/Test Value	GRST
1	-	Recipe	Set Abort Recipe	Abort ALD Process		
2	-	Recipe	Run Recipe	ALD IGF - 400 mTorr		
3	-	Recipe	Set Abort Recipe	Abort ALD Process		
4	-	Recipe	Run Recipe	ALD Mode 0 - HfO2		
5	-	Recipe	Set Abort Recipe	Abort ALD Process		
6	-	ALD Parameter	ALD ChA Dose Time	Set Value = n.nn	0.15	
7	-	ALD Parameter	ALD ChA Purge Time	Set Value = n.nn	10	
8	-	ALD Parameter	ALD ChB Dose Time	Set Value = n.nn	0.03	
9	-	ALD Parameter	ALD ChB Purge Time	Set Value = n.nn	10	
10	-	ALD Parameter	ALD Target Cycles	Set Value = n.nn	80	
11	-	Recipe	Dwell	N Seconds (n or HH:MM:SS)	300	
14	-	ALD Parameter	ALD Run Sequence	Turn_On/Open/Opening		
15	-	ALD Parameter	ALD Sequence Complete	Check_On/Open/Opening		AT
16	-	Recipe	Dwell	N Seconds (n or HH:MM:SS)	30	
17	-	Recipe	Run Recipe	Finish		S
*	0	-				

Figure A-3. ALD recipe program for HfO_2 growth at 110 ℃.

A.3.2 Gating efficiency measurement and breakdown voltage

The aforementioned HfO_2/Au/Si wafer is then deposited with circular gold pads using an aluminum shadow mask, as is shown in Figure A-4(a). To measure the break down voltage, V_{BD}, and the gating efficiency α of the as-deposited HfO_2 film, we perform DC and AC measurement using the Au/HfO_2/Au capacitors, whose area is defined by the top god pads. Figure A-4(b) shows a schematic of the capacitance measurement using a probe station and a lock-in instrument. The two tungsten needles are used to make contacts to the bottom gold layer and top gold pads. One should be careful in probing the gold pads with gentle force, otherwise, the tungsten needle can easily break through the HfO_2 film and short the circuit. The amplitude of the sinusoidal excitation voltage, i.e. output voltage of the Lock-in, is kept constant at 100mV. The resulting sinusoidal current is collected by the integrated current preamplifier and cross-referenced. As the frequency-dependent amplitude relationship between the excitation voltage v_o and the measured current i is given by $i = \frac{v_o}{X_c}$, where $X_c = {}^{1}/_{(2\pi f C)}$ is the reactance of the

Au/HfO_2/Au capacitor. Hence the capacitance of each capacitor can be determined by measuring the current signal at different excitation frequency while keeping the excitation voltage constant. Figure A-4(c) shows an example of the i vs f plot, where the slope of the linear fitting line is equal to $2\pi v_o C$. The intercept point should be set to pass through (0,0) when using Origin to perform the fitting. We usually measure the capacitance from at least 5 capacitors for statistics. The area A of the each gold pad can be calculated from their optical image by using an open-source software ImageJ. Then the gating efficiency of the HfO_2 film can be calculated as $\alpha = {C}/{eA}$. Due to the difference in the gold pad area, the fitted capacitance may differ from each other by as large as 10%, but the gating efficiency values from different capacitor should be very close to each other with less than 1% difference.

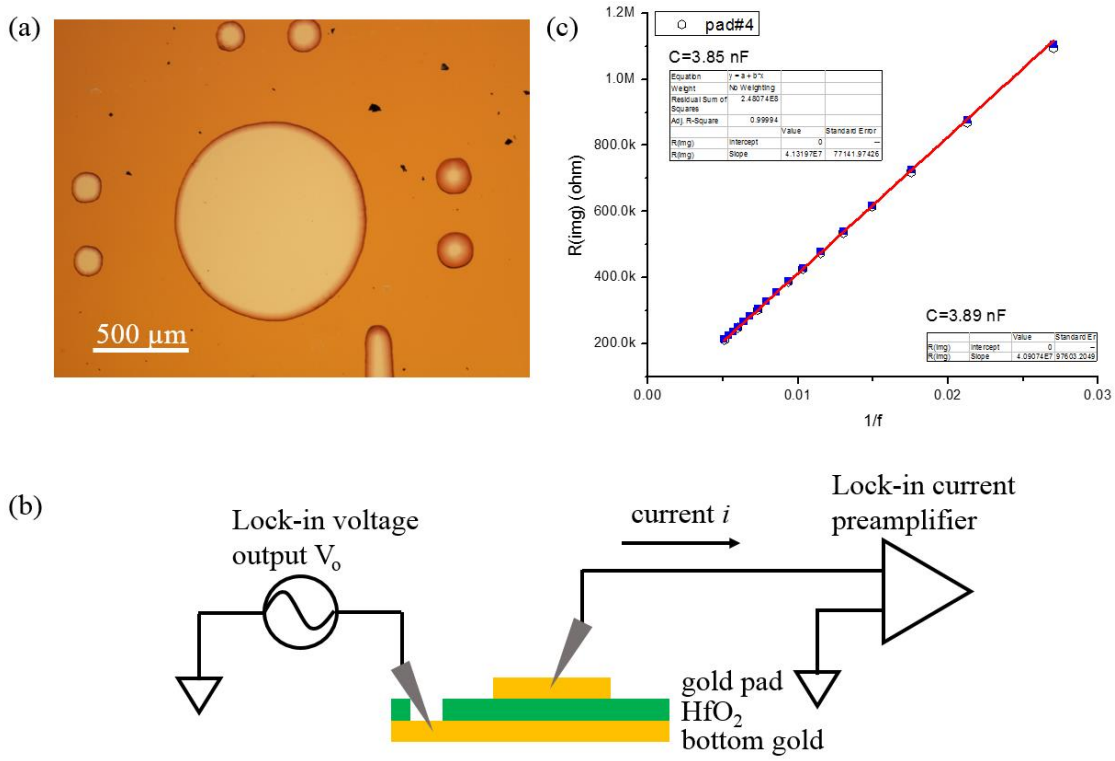


Figure A-4. Capacitance measurements for ALD-grown HfO_2.

The breakdown voltage of the as-deposited HfO_2 film can be obtained using the same measurement configuration by replacing the AC voltage excitation and Lock-in current preamplifier with a DC voltage source (Keithley 2400) and a stand-alone current preamplifier. We usually first manually increase the voltage output (increment size of 10 mV) and monitor the current reading displayed on the Keithley 2400 front panel, which is also related to the leakage current of the capacitor. At first, the current reading should be less than 0.5 nA until at some voltage point V^* it begins to fluctuate around 1nA, indicating the HfO_2 film is close to break down. Then, we quickly dial down the voltage to zero. After manually estimating the breakdown voltage, we then use LabVIEW programs to control and sweep the DC voltage to a maximum value of (V^*+0.5V) to record the behavior of the leakage current.

Appendix B

Atomic Force Microscopy (AFM) based measurements

B.1 Conductive AFM (c-AFM)

Conductive AFM is an electrical measurement technique that utilizes the set-up of an AFM system. It measures the current between a conductive AFM tip and a sample while a voltage excitation is applied between the two. The conductive AFM probe we use has a Ti/Pt (5nm/20nm) coated silicon tip (model#: Olympus AC240TM). To perform the c-AFM measurement, we use a standard ORCA holder, a bias wire which needs to be screwed into the flat tip screw as is shown in Figure B-1(a), and an ORCA sample holder where the clip and pads are gold-coated for optimal conduction as is shown in Figure B-1(b). The ORCA holder has a simple transimpedance amplifier circuit which allows it to detect small current signals. The gain of the amplifier is 5E8 (500 MΩ feedback resistor) and together with the maximum output voltage of ±10V leads to a sensitivity of 2 nA/V and a saturation current of 20 nA. After loading the ORCA holder on the AFM, the iron lead end of the ORCA wire must be attached to one of the two pads that is connected to the clip, as is shown in Figure B-1(c). The pads are magnetic so the wire will be secured in position via magnetic force. Figure B-1(d) is a schematic of the c-AFM measurement circuit. The conductive AFM tip is connected to the amplifier and is at virtual ground. The DC voltage excitation is applied through the ORCA wire to the conductive substrate the sample is mounted on or attached to. When performing the c-AFM measurement, the conductive tip is in direct contact with the sample to complete the current loop.

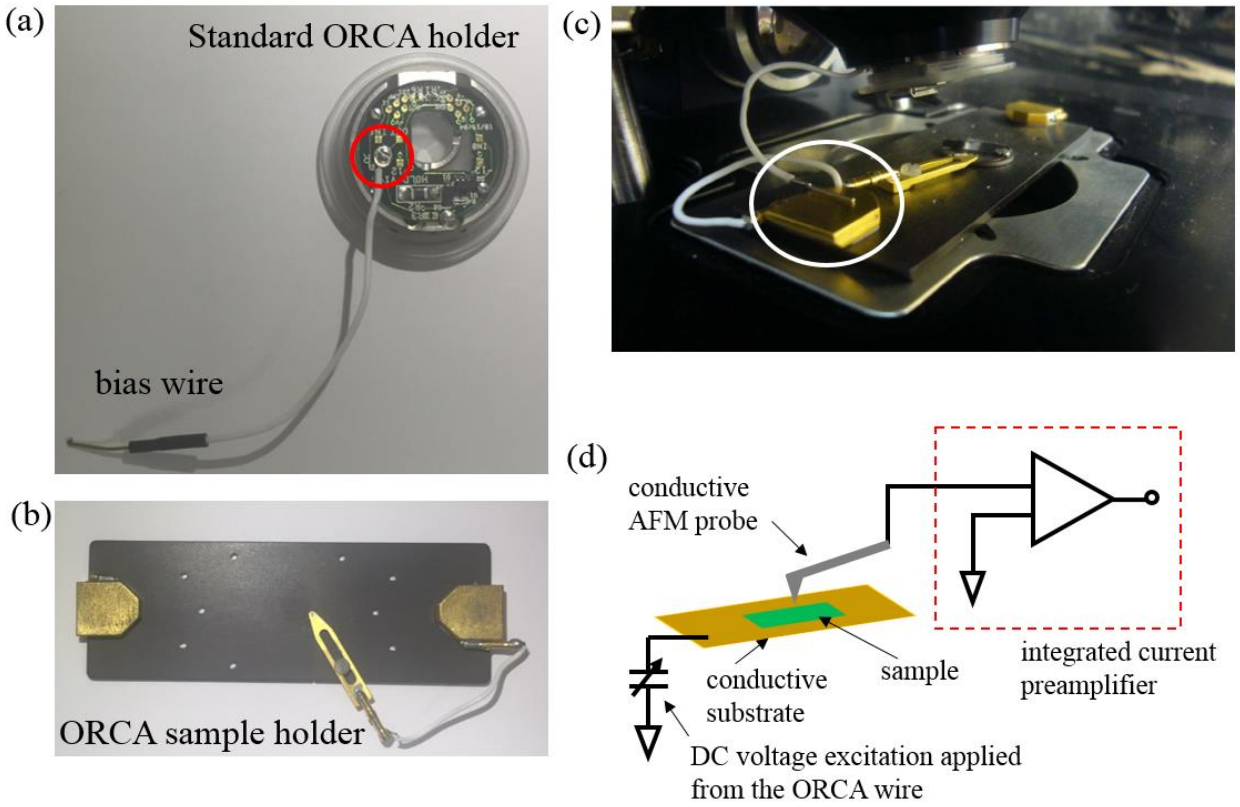


Figure B-1. Optical images and schematics for KPFM measurements. (c) Image courtesy of Asylum Research.

Operation procedures for current mapping:

1. Set the system to operate in AC mode and perform a topography mapping over a relative large area. Then select the desired region for current mapping. Zoom into that region and perform another AC mode scanning.
2. Change to c-AFM mode. Open the *Mode Master* panel, select *Electrical* mode → *Orca*. Check to make sure the current channel is selected and the corresponding current window is displayed. If not, go to the channel panel and add current as channel type. Now the AFM is operated in contact mode with the capability of current mapping. Record the

Deflection value displayed in the Sun and Deflection Meter window while the tip is free in air.

3. Engage the tip to the sample surface and start scanning with a gentle force, i.e. set the "Set Point" in the Master Panel window to be 0.05 higher than the Deflection value recorded in step 2. The Set Point in the contact mode controls the deflection of the cantilever which determines the force applied by the tip to the sample together with the spring constant of the cantilever.
4. As the scan goes on, slowly raise the Sample Voltage, which is the voltage applied by the ORCA holder to bias the sample, until current signals start to show up in the current window. The Sample Voltage can then be further increased for a large signal-to-noise ratio. The maximum bias voltage can be applied is ±10 V.
5. After decent current signals are obtained at certain Sample Voltage, the "Set Point" value should be further increased slowly with an increment size of 0.05. This usually leads to an increase in the current signals as the tip-sample contact resistance is reduced with increasing tip-to-sample force. According to the operation manual from Asylum Research, a net deflection of 0.2~0.3 V is typical for the AC240 based cantilevers. This corresponds to a Set Point that is 0.2~0.3 higher than the recorded Deflection in step 2. It should be noted that if the "Set Point" is set to a very large number (maximum is 10), there are two consequences: a) the sharp tip could damage the sample if it is softer than the tip; b) the tip apex could be deformed if the sample is harder than the tip and the Ti/Pt coating will wear off faster.

B.2 Kelvin Probe Force Microscopy (KPFM)

The Kelvin Probe Force Microscopy is another type of local electrical measurement that takes advantage of an AFM set up. It measures the work-function difference between a conductive AFM tip and a sample. The operation principles are already discussed in Chapter 3. The KPFM measurement set up involves the standard AFM holder used for topography measurement and a conductive AFM probe (Olympus AC240TM) for applying the DC bias. The samples are usually mounted on a conductive substrate such as gold-coated silicon wafer. The KPFM measurement only gives the work function difference between the tip and the sample surface. However, the work function of the conductive tip (usually Ti/Pt coated) is not calibrated and un-stable, as it often is affected to the environment, such as humidity and molecular contamination. In order to determine the actual work function of a sample, we use graphite as a reference material as its work function has been found to be stable and universal as long as the thickness of the graphite flake exceeds certain number. In the following, I will use WSe_2 as an example to describe the KPFM operation procedures.

Sample preparation.

WSe_2 and graphite sheets are mechanically exfoliated onto the same gold-coated wafer as is schematically shown in Figure B-2. The wafer is then mounted onto the ORCA sample holder. After loading the ORCA holder on the AFM scanner, the wafer needs to be grounded by attaching one end of a metal wire to the gold pad of the sample holder and the other end to metal plate of the scanner to avoid arbitrary offset to the work function measurement.

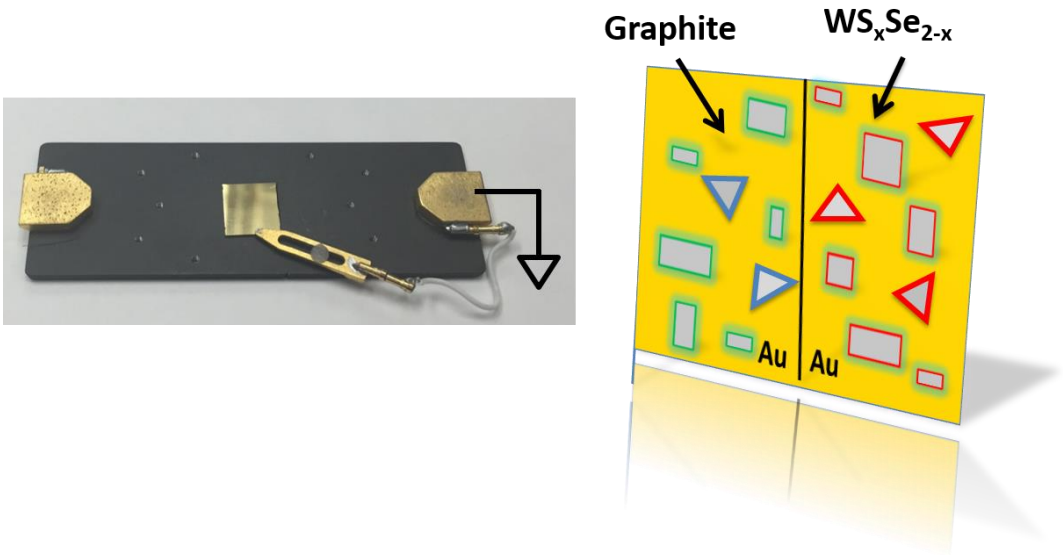


Figure B-2. An optical image of a sample mounted on the KPFM sample holder and Schematics of sample preparation.

AFM operation procedure.

1. Operate the AFM in AC mode to scan a large area to include the feature WSe_2 or graphite flakes. Then zoom-in on the WSe_2 or graphite flakes and do another scan in AC mode.
2. Open the Mode Master Panel and select Electrical → SKPM.
3. Click the Tune tab in the Master Panel. Under Auto Tune, set the Target Amplitude and the Target Percent to be 1.0V and -5%, then click the Auto Tune button. This finds the resonance frequency of the cantilever when it is driven mechanically.
4. Engage the tip to the sample surface by slowly lowering it down until the Z Voltage reading on the Sum and Deflection Meter is close to 70.
5. Select the Electric Tune Panel to find the resonance frequency of the cantilever when it is driven by an AC bias. First, the tip needs to be placed just above the sample surface by

performing a force-distance curve. Set Above the Surface to 300 nm, Trigger Channel to AmpVolts, and Trigger Point to 800 mV. Then click the Single Force button.

6. Click the arrow button to copy the Drive Frequency under the Normal column to the one under the Electric column. Then click the Electric Tune button, which applies an AC bias with frequencies around the Drive Frequency and display the corresponding oscillation amplitude of the cantilever in a Cantilever Tune window. Then click the Center Phase button.
7. Now select the Nap Panel. Set the Delta Height and Start Delta Height to be 40 nm at the beginning.
8. Go to the Main Panel and set the Set Point to 780 mV and start scanning by clicking either the Frame Up or Frame Down button. First, slowly increase the Drive Amplitude in the Main Panel until the trace and retraces curves in the Height Retrace windows follow each other. Then decrease the Delta Height and Start Delta Height at the same time and by the same amount. This increases the lateral resolution of the potential image. It is found that a height value between -30 nm ~ -40 nm usually gives the best lateral resolution.

Sample work function calculation.

We use the work function of few-layer graphene, $W_{graphite}$, as reference for the determination of work function of different TMDC sheets and alloys. We assume the work functions of the gold surface and Pt coating of the tip are stable over the time span of each measurement, which usually lasts for 2 to 3 hours. The mathematically equations used to find the sample work function are given below:

$$CPD_{graphite} = \frac{\left(W_{graphite} - W_{tip}\right)}{e}$$

$$CPD_{sample} = \frac{\left(W_{sample} - W_{tip}\right)}{e}$$

where $CPD_{graphite}$ (CPD_{sample}) are the measured potential difference between graphite (sample) and the Pt-coated tip. CPD stands for contact potential difference. Hence, by eliminating the work function of the tip W_{tip}, one can obtain the expression for the sample work function as

$$W_{sample} = W_{graphite} + e\left(CPD_{sample} - CPD_{graphite}\right)$$

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