The Pennsylvania State University

The Graduate School

College of Engineering

ZnO Thin Film Electronics for More than Displays

A Dissertation in

Electrical Engineering

by

Jose Israel Ramirez

Submitted in Partial Fulfillment

of the Requirements

for the Degree of

Doctor of Philosophy

August 2015

The dissertation of Jose Israel Ramirez was reviewed and approved* by the following:

Thomas N. Jackson
Robert E. Kirby Chair Professor of Electrical Engineering
Dissertation Adviser
Chair of Committee

Suman Datta
Professor of Electrical Engineering

Susan Trolier-McKinstry
Professor of Electrical Engineering and Ceramic Science and Engineering

Mark W. Horn
Associate Professor of Engineering Science and Mechanics

Kultegin Aydin
Professor of Electrical Engineering
Department Head

*Signatures are on file in the Graduate School.

Abstract

Zinc oxide thin film transistors (TFTs) are investigated in this work for large-area electronic applications outside of display technology. A constant pressure, constant flow, showerhead, plasma-enhanced atomic layer deposition (PEALD) process has been developed to fabricate high mobility TFTs and circuits on rigid and flexible substrates at 200 °C. ZnO films and resulting devices prepared by PEALD and pulsed laser deposition (PLD) have been compared. Both PEALD and PLD ZnO films result in densely packed, polycrystalline ZnO thin films that were used to make high performance devices. PEALD ZnO TFTs deposited at 300 °C have a field-effect mobility of ~ 40 cm^2/V-s (and > 20 cm^2/V-S deposited at 200 °C). PLD ZnO TFTs, annealed at 400 °C, have a field-effect mobility of > 60 cm^2/V-s (and up to 100 cm^2/V-s).

Devices, prepared by either technique, show high gamma-ray radiation tolerance of up to 100 Mrad(SiO_2) with only a small radiation-induced threshold voltage shift (V_T ~ -1.5 V). Electrical biasing during irradiation showed no enhanced radiation-induced effects. The study of the radiation effects as a function of material stack thicknesses revealed the majority of the radiation-induced charge collection happens at the semiconductor-passivation interface. A simple sheet-charge model at that interface can describe the radiation-induced charge in ZnO TFTs.

By taking advantage of the substrate-agnostic process provided by PEALD, due to its low-temperature and excellent conformal coatings, ZnO electronics were monolithically integrated with thin-film complex oxides. Application-based examples where ZnO electronics provide added functionality to complex oxide-based devices are presented. In particular, the integration

of arrayed lead zirconate titanate (Pb(Zr, Ti)O_3 or PZT) thin films with ZnO electronics for microelectromechanical systems (MEMs) and deformable mirrors is demonstrated. ZnO switches can provide voltage to PZT capacitors with fast charging and slow discharging time constants. Finally, to circumvent fabrication challenges on predetermined complex shapes, like curved mirror optics, a technique to transfer electronics from a rigid substrate to a flexible substrate is used. This technique allows various thin films, regardless of their deposition temperature, to be transferred to flexible substrates.

Finally, ultra-low power operation of ZnO TFT gas sensors was demonstrated. The ZnO ozone sensors were optimized to operate with excellent electrical stability in ambient conditions, without using elevated temperatures, while still providing good gas sensitivity. This was achieved by using a post-deposition anneal and by partially passivating the contact regions while leaving the semiconductor sensing area open to the ambient. A novel technique to reset the gas sensor using periodic pulsing of a UV light over the sensor results in less than 25 milliseconds recovery time. A pathway to achieve gas selectivity by using organic thin-film layers as filters deposited over the gas sensors tis demonstrated. The ZnO ozone sensor TFTs and the UV light operate at room temperature with an average power below 1 μW.

Table of Contents

List of Figures

Acknowledgements

This work is a byproduct of the encouragement, discussions, and support I have had by numerous people inside and outside of academia. Over the course of my time at Penn State I have been fortunate to meet many individuals that have positively impacted me academically, professionally, and personally. A person who impacted my growth in each of those areas is my academic advisor, Dr. Tom Jackson. His immense knowledge in this field, patience, and commitment to mentoring was crucial in fostering an environment that generated fruitful discussions that developed into new research directions. Aside from being an excellent mentor, his culinary knowledge was also greatly appreciated outside the lab.

I would also like to thank my committee members: Dr. Suman Datta, Dr. Susan Trolier-McKinstry and Dr. Mark Horn, for their participation and time they devoted to reviewing and guiding this doctoral thesis. In particular, I want to express my appreciation to Dr. Susan Trolier-McKinstry for her patience explaining Materials Science concepts.

The collaborations and camaraderie of past and present members of Jackson's electronic research group (JERG) at Penn State is also gratefully acknowledged. In particular, I thank Dr. Dalong Zhao and Dr. Yuanyuan Li for imparting me their knowledge and for their selfless assistance since day one in the group. The collaboration with Dr. Trolier-McKinstry's group students Hong-Goo Yeo and, particularly, Margeaux Wallace was elemental in expanding my research directions and resources. Many fruitful discussions and collaborations with people outside of Penn State from Air Force Research Labs, Smithsonian Astrophysical Observatory, and North

Carolina State University are also acknowledged. Particularly, the many discussions over the years with Dr. Gregg Jessen from AFRL helped broaden my thinking about the ZnO material system.

Finally I thank my family Jose, Carmen, Liliana, and Abigail for their unconditional love and for tolerating my idiosyncrasies. This achievement was easier with your support.

None of this work would have been possible without the financial assistance of different government and private agencies including: Defense Microelectronics Activity (DMEA), Defense Threat Reduction Agency (DTRA) through the Asian Office of Aerospace Research and Development (AFOSR/AOARD), National Science Foundation (NSF) through Nano-systems Engineering Research Center (NERC) for Advanced Self-Powered System of Integrated Sensors and Technologies (ASSIST), National Aeronautics and Space Administration (NASA), and Corning Incorporated and Alfred P. Sloan Foundation for awarding me fellowships.

Chapter 1

1.1 Introduction and Background

Interest in large-area electronics for ubiquitous applications is partly because of the relatively low-cost of the materials used and the simplicity to fabricate such electronics. For example, manufacturing the front-end of a liquid crystal display (LCD) backplane, the exemplary process for large-area electronics, consists of as little as four mask steps. This is in contrast to some technologies such as c-Si CMOS which can afford to use high-cost materials and processes because they have high value per unit area. For large-area electronics fast, inexpensive, and low temperature processes are favored in order to provide a path to have electronics on low-cost substrates. Amorphous silicon (a-Si:H) is an established and successful technology for large-area displays; however, its electrical performance limits useful applications for more than displays and X-ray imagers [1]. In response to the shortcomings of a-Si:H, a variety of inorganic and organic semiconductor materials have been explored as potential candidates to replace a-Si:H, all with different advantages and disadvantages [2-5]. Among some of the requirements for material selection is the ability to deposit the material at low temperatures to be compatible with polymeric substrates and to have good electrical performance and stability to realize useful large-area electronic applications. An emerging class of semiconductors that fulfill these requirements is metal-oxide semiconductors.

Amorphous silicon (a-Si:H) owes its low carrier mobility to the localized electronic states throughout its bandgap [6, 7]. A portion of these states make up the conduction and valence band tails and as it has been shown, the conduction band-tail slope dictates the field-effect mobility in

a-Si:H TFTs [6]. This is as of consequence of the strong directivity of the hybridized sp^3 orbitals causing bond angle fluctuation, thereby altering the electronic levels and causing high density deep tail-states [6]. The disruption in the bond angle and bond length is a consequence of the preferred low temperature deposition process to make the material compatible with low-cost substrates. Oxide semiconductors do not have this issue because of their inherently different ionic bonding. In oxide semiconductor materials like zinc oxide, ZnO, the large difference in electrostatic potential between zinc and oxygen leads to a large ionization energy from lowering the energy levels in the oxygen ions and raising the levels in the zinc ions until the enthalpy of atomization is reached [8]. Thus, a large bandgap is realized (3.37 eV). In ZnO, and other oxide semiconductors with high ionicity, the states near the bottom of the conduction band are formed from isotropic empty *s*-orbitals of the zinc cation that may have some overlap with adjacent *s*-orbitals [9-11]. This overlap of neighboring *s*-orbitals is largely unaffected by bond angle and bond length as is the case in materials with sp^3 hybrid bonding (valence band) and anti-bonding (conduction band) like a-Si:H [9, 11, 12]. Therefore, the degenerate band conduction and large electron mobility seen in ZnO is a unique property of ionic bonding in oxide semiconductors and not seen in covalent amorphous semiconductors like a-Si:H.

As mentioned earlier, a number of oxide semiconductors have been explored for large-area electronic applications. These oxide semiconductors, generally n-type, are largely either a binary system like ZnO or derived from it to form ternary or quaternary alloys like indium-zinc-oxide (IZO) and indium-gallium-zinc-oxide (IGZO). In this work, the ZnO semiconductor is used to build electronics for large-area applications. ZnO is a versatile semiconductor with electronic uses in its thin and thick film form for electronic and optoelectronic applications [13-15]. The

wide bandgap (E_g = 3.37 eV) makes it transparent to IR and visible light. Moreover, because of its large bandgap, the semiconductor can achieve low leakage current, high temperature operation, and high voltage operation [3, 16, 17].

This thesis presents the use of polycrystalline ZnO thin film for electronic applications outside of the backplane technology. A novel plasma-enhanced atomic layer deposition (PEALD) system using a showerhead to dispense the reactants is discussed. This deposition process was key in depositing high performance and reproducible films over large substrates. ZnO films prepared by PEALD used in TFT structures have field-effect mobility of ~40 cm^2/V-s when deposited at 300 °C and ~25 cm^2/V-s when deposited at 200 °C. Pulsed-laser deposited ZnO thin films are also reviewed and used as a benchmark for PEALD ZnO thin films because the field-effect mobility of those films is closer to bulk Hall-effect mobility. While the two different deposition techniques produce ZnO films with slightly similar electrical characteristics, there are some subtle microstructural differences. Nevertheless, the similar performance highlights the material's insensitivity to the energy used during deposition. The radiation hardness of ZnO TFTs deposited by both PLD and PEALD further highlights the intrinsic ionic bonding characteristics that make ZnO insensitive to disorder. A simple model is developed to explain the small radiation-induced changes in ZnO TFTs. A general model to reduce radiation-induced changes in staggered bottom-gate thin film transistors is presented. Potential applications for more than displays where large-area electronics would be useful are described. Given the high radiation tolerance of ZnO TFTs, the TFTs are ideal candidates for large-area space applications. Integration of ZnO electronics with lead zirconate titanate ($Pb(Zr, Ti)O_3$ or PZT) thin films was developed to add functionality to PZT actuators, in particular for adaptive optics in X-ray

telescopes. Finally, ultra-low-power ZnO TFT gas sensors for ubiquitous gas sensing applications have been developed.

Chapter 2 provides an overview of the different deposition techniques used to deposit oxide semiconductors. The design and development of a PEALD system that allows deposition over relatively large substrates (20 cm diameter) is presented. The system uses a showerhead to dispense the reaction materials, proving excellent uniformity and with the potential to allow fast deposition rates because of its gas configuration. System optimization was carried to produce high-quality Al_2O_3 and ZnO thin films used throughout this work in TFT structures. Next, ZnO TFTs with the active layer deposited by PLD are presented. Chapter 2 concludes with a comparison of the electrical and materials characteristics of ZnO thin films deposited by both techniques.

Chapter 3 describes the radiation tolerance of ZnO TFTs with the active layers deposited by both PEALD and PLD. While extensive research has been done on the radiation hardness for silicon and III-V FETs, less is known about radiation-induced effects in oxide-based TFTs. In this work, the intrinsic radiation tolerance of ZnO, and by extension other oxide-based TFTs, is demonstrated. A radiation tolerance up to 100 Mrad(SiO_2) is shown with no degradation in field-effect mobility and minimal negative threshold voltage (V_T) shift. Contrary to the enhanced radiation effects in Si CMOS with electrical bias, ZnO TFTs are insensitive to electrical bias. Measurement artifacts in electrically biased ZnO TFTs during irradiation are identified and a framework is proposed to eradicate the artifacts in ZnO and other TFTs with a staggered bottom-gate structure. Chapter 3 concludes by investigating the physical locations of charge trapping due

to irradiation in ZnO TFTs is investigated and found that the ZnO surface is the most sensitive to radiation-induced charge trapping.

Chapter 4 builds on the fact that ZnO TFTs are substrate agnostic, due to the low deposition temperature and conformal deposition technique, and applications are explored where TFTs may provide added functionality to other technologies. An example of integrating ZnO passive electronics with barium strontium titanate ($Ba_{1-x}Sr_xTiO_3$ or BST) thin films for tunable RF filters is described. Furthermore, the integration of ZnO electronics with PZT thin films used for a range of actuators is shown. A robust process was developed to integrated passive and active ZnO-based electronics on different substrates with BST and PZT films without degrading their performance. The radiation-hardness of ZnO TFTs led to explore space-related applications where large-area electronics might be desired such as adaptive x-ray optics using PZT thin films to deform the optics. The ZnO TFTs were used as switches to provide the desired voltage to the PZT thin films and consequently reduce the number of electrical connections needed to address pixels in the adaptive optics. A ZnO-based electrostatic discharge (ESD) circuit was designed and tested to reduce ESD events in the PZT-ZnO array. An array of PZT capacitors were actuated through ZnO TFTs and deformation of the thin flat glass substrate is demonstrated. Chapter 4 concludes by introducing a potentially useful processing technique to build electronics on thin polymeric substrates to avoid problems using conventional microlithography techniques on curved substrates, because the adaptive optical mirrors will ultimately have a conical shape.

Chapter 5 demonstrates ultra-low power ZnO TFTs for ubiquitous gas sensing applications. The ZnO-based gas sensor TFTs were optimized to operate at low temperature with excellent

electrical stability by using a post-deposition anneal and by partially passivating the TFT structure with the active semiconductor area open for gas sensing. The ZnO ozone sensors operate at room temperature with an average power below 1 μW. A novel way, using pulsed ultraviolet (UV), to reset and achieve low power consumption of the ozone sensors is described. Different ozone levels were detected by looking at the $\partial I / \partial t$ after the UV reset pulse. Ozone was detected down to 110 ppb. Chapter 5 concludes by pointing at possible methods and techniques to achieve gas selectivity in ZnO TFTs while keeping the same overall power operation.

Chapter 6 concludes the discussion of exploring the use of ZnO electronics for other applications besides displays and provides suggestion for future work. In order for this technology to be more attractive for broader applications a further understanding of the material properties is needed to be used as guideline to modify the deposition parameter conditions to achieve higher performance films. An iterative and comprehensive study relating different deposition parameters to the energy level transitions by photoluminescence (PL) and connecting it to the device performance is discussed. Also, further application-oriented demonstrations, using the current technology, are proposed. For example, leveraging the radiation-hardness of the ZnO TFTs to develop a backplane integrated with photodiodes for a flexible, low-cost detector is described. Lastly, an application-oriented opportunity is proposed for a system level integration of a self-powered gas sensor node system using PZT as energy harvester, an active ZnO rectifier, and ZnO gas sensors.

Chapter 2

2.1 Thin Film Deposition Processes for Oxide Semiconductors

A wide range of deposition techniques has been used to deposit metal-oxide semiconductors. These deposition techniques vary in the energy used during growth; typical types of energy provided during film deposition are thermal, chemical or electromagnetic. Different techniques such as metal organic vapor deposition (MOCVD), pulsed laser deposition (PLD), sol-gel, and sputtering have been researched to deposit oxides [18-21]. These deposition techniques have advantages and disadvantages and are generally selected depending on the thin-film application. Most of the recent interest and research effort has focused on using sputtering, particularly for thin-film transistors. The interest is partly because sputtering is a scalable technique and the manufacturing infrastructure is already in place in the large-area display industry. This technique has been comprehensively optimized to deposit amorphous oxide thin films such as indium gallium zinc oxide (IGZO) and indium zinc oxide (IZO) [21, 22]. However, for IZO, controlling the defect concentration is often difficult resulting in small current on/off ratios; therefore, the addition of gallium provides better concentration control making it a robust process [22]. The process has matured to the point that some display manufacturers have partially ramped up IGZO-based TFT backplanes to drive active-matrix organic LED (AMOLEDs) [23, 24]. Some of the advantages of oxide semiconductors over the established a-Si:H technology are electrical-stress stability, higher field-effect mobility, and lower power consumption.

While the field-effect mobility of IGZO-based TFTs deposited by sputtering can be over 30 cm^2/V-s, in reality, the average field-effect mobility for TFTs used in backplane manufacturing

can be as low as 4 cm^2/V-s [25]. This field-effect variation is partly due to ZnO thickness variation which has been reported to be as high as 23.5% variation over ~15 in^2 [25]. Another drawback of sputtering oxide-based thin films is the inherent relatively poor step coverage over substrate defects or complex topography. This is particularly problematic if the use of polymeric substrates, for flexible electronics, is desired. In the following sections, two different techniques to deposit ZnO thin films are presented: pulsed laser deposition (PLD) and plasma-enhanced atomic layer deposition (PEALD). While PLD is hardly scalable to be compatible with large-area electronics, the material grown by PLD was used as a benchmark for TFT electrical performance. On the other hand, an ALD-based deposition technique has a potential pathway to be scalable and compatible with large-area electronics and provides excellent step coverage over inherently complex substrate topology known in polymeric substrates.

The growth and the majority of the fabrication of PLD ZnO TFTs shown hereafter were done at Air Force Research Labs (AFRL) and the device characterization was carried out at Penn State. For the PEALD ZnO TFTs, the growth and fabrication of films was done at Penn State. Films grown by two different techniques allowed comparing and contrasting the materials and electrical characteristics. While different deposition and post-deposition temperatures were investigated throughout this work, the bulk of the effort was focused on depositing films by PEALD at 200 °C to be compatible with polymeric substrates.

2.2 Showerhead Plasma-Enhanced Atomic Layer Deposition

Atomic layer deposition (ALD) is a technique that was developed in the 1960s by V.B. Aleskovskii et al. [26]. ALD is a self-limiting process that takes advantage of the sequential use of a gas phase chemical process. Most ALD reactions use two chemicals, often referred as precursors. Given the half-reaction nature of the process, ALD provides excellent uniformity and conformality; covering aspect ratios of $L/d \approx 5000$, where L is film thickness and d initial pore diameter, have been reported [27]. This feature makes the ALD technique an excellent candidate to deposit uniform thin films on a range of substrates, including substrates with high root mean square (RMS) roughness. The technique has been studied to deposit a range of materials such as dielectrics, ferroelectrics, metals, and semiconductors [28-31]. In particular, the ALD technique was very important in the development and introduction of high-k gate dielectric in the 45 nm node in Si CMOS technology [32]. The technique was an attractive option for this application because of its excellent thickness control, even for ultra-thin films, and relatively low deposition temperature. However, its major limitation is its slow deposition rate when thick films are desired. This is not an issue for high-k gate dielectric deposition in state-of-the-art CMOS because the films need to be ultra-thin. However, for applications where relatively thick films are needed the technique becomes less attractive due to its low throughput. A typical deposition rate is 0.5-1 nm per minute. Atmospheric spatial ALD (SALD) is an approach that has been investigated to overcome this drawback [33]. SALD deposition technique uses a head with reactive gases separated by a purge gas to avoid free reaction. The head is then moved over the sample at fast speeds achieving up to 25 nm/min deposition rates [33]. Initial work has been done to assess whether a showerhead system configuration could achieve high throughput.

The ALD process can be slightly modified to use plasma in conjunction with a weak-oxidant to produce the second half of the reaction, acting as an oxidizer. This variation is typically known as plasma-enhanced ALD (PEALD). There have been reports of a variety of oxide thin films such as ZnO, Al_2O_3, ZrO_2, and HfO_2 deposited by PEALD [31]. It has been reported that plasma chemistry significantly reduces the incorporation of –OH groups, which are related to conduction in ZnO and defects in oxide-based dielectrics [31, 34]. Using plasma as an energy source for the chemical reaction allows lowering the deposition temperature while still producing high quality thin films [34, 35]. Moreover, the use of plasma has proven to be beneficial in suppressing interface states and Fermi-level unpinning in III-V MOS interfaces [34].

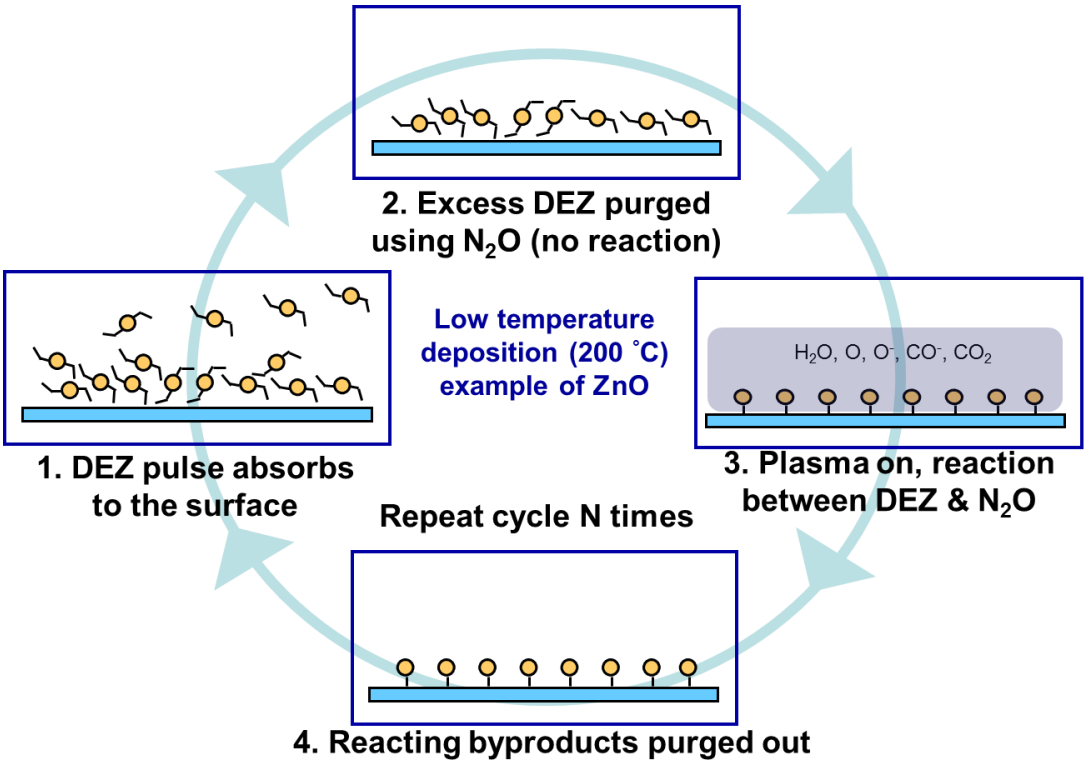


Figure 1. An example of a plasma-enhanced atomic layer deposition (PEALD) cycle to deposit ZnO using diethylzinc (DEZ) as the zinc precursor and a weak oxidant (N_2O in this example) as both oxidizer (when the plasma is tuned-on) and purge gas.

The majority of PEALD processes use O_2 coupled with plasma as a precursor, creating the oxidizing species in a remote plasma and transporting these species downstream to the substrate [31]. A slightly different approach has been taken in this work similar to the work by Mourey D. et al. [30]. Figure 1 shows a typical PEALD process cycle. The process starts by introducing the metal organic precursor (Zn precursor in the example) in to the chamber to saturate the surfaces with at least a monolayer. Next, the excess metal organic is purged out with a low-reactivity gas, typically CO_2 and N_2O. Weak-oxidant gases have been chosen over high reactivity gases so the gas can be used as both purge gas and oxidizer when the plasma is turned on. After the excess metal organic is purged out, the plasma is ignited and the oxide layer is formed. The plasma is generated using an Advanced Energy RF power generator RFX-600 (13.56 MHz). The matching network used to ensure close-to 50-ohm impedance at the RF generator was an MFJ-989C 3 kW versa tuner. A high voltage supply (7.5 kV) attached to a thin tungsten wire through a simple vacuum feed through with a sharpen end is used to provide a source of electrons to the plasma when it is first started. This is particularly important to reliably start the plasma at low power densities which is, as will be shown later, important to have high performance thin films. The cycle is completed by purging out the reaction byproducts and the cycle is repeated until the desired thickness is reached. Typically, both, ALD and PEALD use a soak and purge time dictated by the specific chamber volume, inlet and outlet port location in order to achieve film uniformity. During a cycle, there are soaking times (time during the metal organic is introduced and the plasma is turned-on) and purge times. The soak and purge steps during a cycle result in relatively large changes in pressure throughout a cycle. These deposition systems are typically configured with inlet and outlet ports opposite of each other [36, 37]. This configuration helps uniformity and step coverage because the mass transport partially relies on diffusion to deliver

the metal organics and oxidizer agents everywhere in the chamber. In this work the possible advantages of modifying the gas handling and delivering in the PEALD process by using a showerhead reactor were studied.

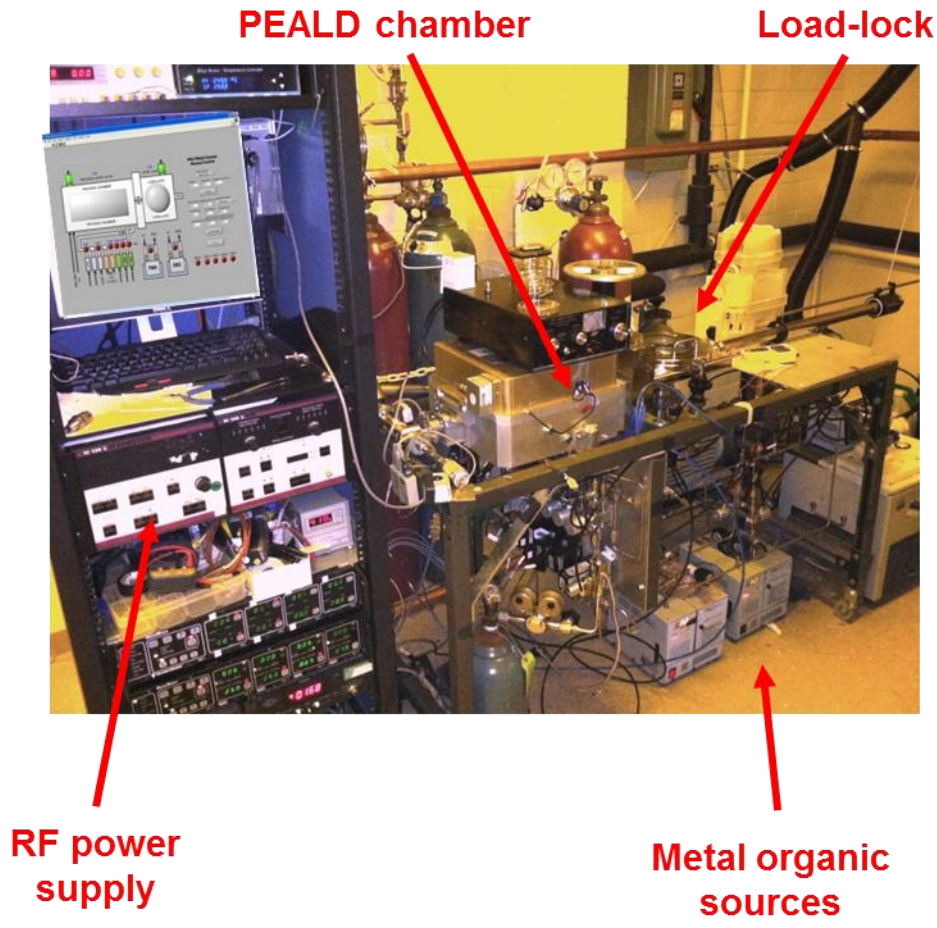


Figure 2. A picture of the showerhead PEALD deposition system with a load-lock chamber. The load-lock chamber was added to the system to minimize moisture in the deposition chamber. A custom-made LabView program was developed to control various deposition parameters.

The deposition system described here uses a modified commercially available showerhead reactor, P5000, manufactured by Applied Materials. The P5000 is a single-wafer chamber often configured in clusters for chemical vapor deposition (CVD), etch and/or photoresist strip applications. The chamber was heavily modified to be used as a single-wafer chamber.

Originally the chamber had a mechanical system for wafer loading compatible with a cluster system design. This was modified by using a loading chamber and a manual valve in between the two chambers, as shown in Figure 2. The load-lock chamber not only provides a convenient way to load a sample but it also helps prevent the process chamber from being exposed to atmosphere, thereby minimizing the moisture intake in it. The original lamp heater was replaced by a simple 15 cm stainless steel heater plate where a 20 cm substrate holder is placed. The showerhead consists of two plenums with spatially asymmetric holes in the innermost showerhead and spatially equidistant holes in the showerhead dispensing the gas to the sample, as show in Figure 4. This geometry provides gas uniformly across a 20 cm Ø substrate. A schematic of the chamber is shown in Figure 3 (left).

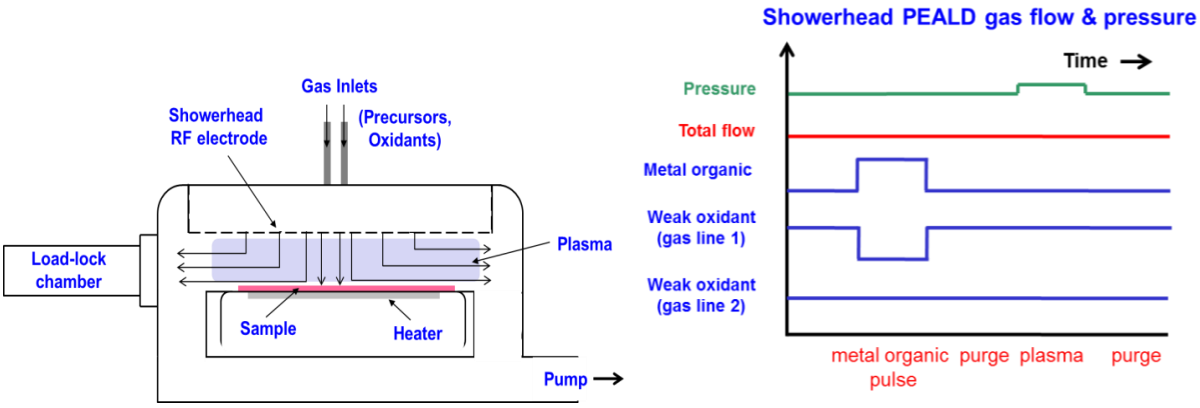


Figure 3 (left) Modified Applied Materials P5000 chamber used as a PEALD chamber. The system can handle substrates up to 20 cm; (right) schematic of the pressure and gas flow as a function of time used to operate the showerhead deposition system.

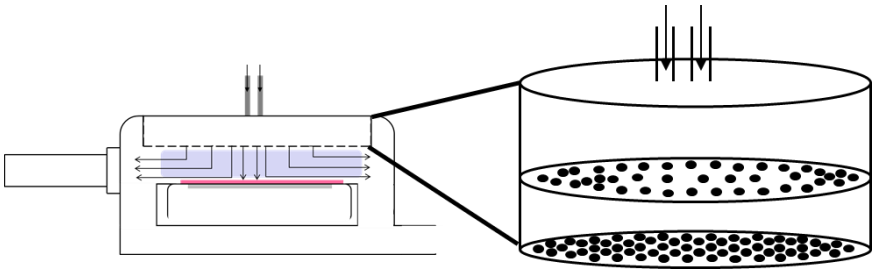


Figure 4. A detailed schematic of the plenums in the showerhead. The showerhead consists of two plenums with spatially asymmetric holes in the innermost showerhead and spatially equidistant holes in the showerhead dispensing the gas to the sample.

As previously mentioned, the gas delivery system designed and built for this chamber is different from convention ALD systems. A detailed schematic of the gas handling is shown in Figure 5. The showerhead PEALD system uses a run/vent gas delivery method; similar to a method often employed in metal-organic chemical vapor deposition (MOCVD) systems, to run at nearly constant chamber pressure. During a typical PEALD deposition the metal organic and one of the weak oxidants gas lines are alternated to keep a constant flow and constant pressure in the process chamber. The gas not dispensed to the chamber is delivered to a secondary pump. This operation mode reduces start-up effects and insures the plasma is contained right above the sample and not inside the showerhead plenums. A schematic of the gas flow and pressure as a function of one cycle is shown in Figure 3 (right). Because the gas is delivered directly above the substrate, in conjunction with the relatively small (~1 L) chamber volume, and the typical flow rates (~1 slpm), a short residence time can be achieved (~100 mseconds). This short residence times, in theory, indicates very short cycles (<0.5 secs) could be achieved. The parameter space in the short cycle regime has been initially explored and deposition rates of ~4 nm/min have been achieved. However, further investigation and optimization is still needed.

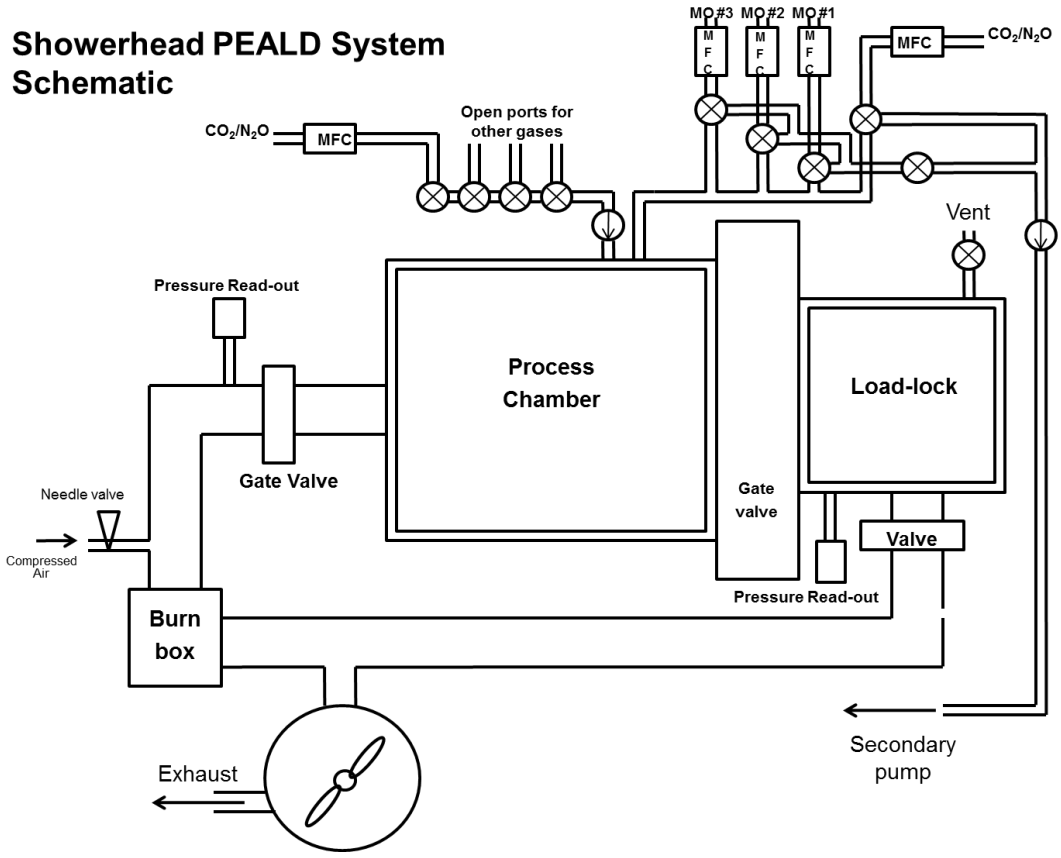


Figure 5. A schematic of the showerhead PEALD system including the gas handling. The gas handling operates in a run/vent mode (either gases are introduced to the chamber or taken to the secondary pump).

A system optimization was carried out to understand the trade-offs using an atypical gas delivery method, chamber geometry, constant-flow, and constant-pressure in a PEALD system. Next, films deposited using the showerhead system were characterized in the context of deposition rate, refractive index, and electrical measurements.

2.2.1 Showerhead PEALD Thin Film Properties and Devices

The most well studied material deposited by ALD is Al_2O_3 using trimethylaluminum (TMA) as precursor and water (H_2O) as oxidizer [38]. Therefore, as a starting point of system optimization

the properties of PEALD Al_2O_3 were characterized. The deposition rate of Al_2O_3 is fairly insensitive to deposition parameters partly because of the beta elimination between the TMA and the –OH terminated surfaces which limits the reaction to about one monolayer per cycle [38]. The same chemisorption mechanism also takes places in PEALD-deposited Al_2O_3 films. The amount of metal organic dispensed (metal organic valve open time × flow rate, at a fixed metal organic temperature and carrier gas pressure); purge time, plasma time, process pressure, and plasma power density were investigated. The minimum metal organic dose needed to saturate all the surfaces (including the substrate) was calculated by estimating the total surface area (cm^2) of the chamber that the metal organic would need to cover and by estimating the surface density of Al_2O_3 (atoms/cm^2). Using these values a dose volume was estimated for a given temperature (typically ~15 °C) and pressure of the bubbler (typically pressurized with argon at ~1500 Torr) containing the metal organic precursor. A diluted dose (argon + metal organic) in the order of ~0.04 Torr-L (~8 cm^3) was found to be sufficient to form about a monolayer on the substrate and still have good material utilization. The initial optimization of the rest of the parameters was guided by using the refractive index of the deposited films (in general, a higher the index of refraction approaching the bulk material's characteristics, corresponds to high film density). This optimization was followed by electrical characterization as those characteristics were the most relevant to this work. Typical values of parameters for optimized thin films are shown in Figure 6.

Typical deposition parameters for the showerhead PEALD	
Metal organic valve open Metal organic flow rate	2 seconds 250 sccm
Purge time Weak oxidant flow rate	4 seconds 250 sccm
2nd weak oxidant flow rate (always open)	650 sccm
Plasma time Plasma power density Plasma purge time	2 seconds 0.06 W/cm^2 2 seconds
Process pressure	1 Torr

Figure 6. Typical deposition parameters for optimized thin films deposited using the showerhead PEALD system.

Films thicknesses and refractive index were determined by spectroscopic ellipsometry. Optimized deposition parameters for Al_2O_3, deposited at 200 °C yielded a deposition rate of ~1.03 nm/cycle with a refractive index of ~1.64-1.65 at 633 nm. This value is higher than other reported values for films deposited by ALD at 177 °C (1.6 at 633 nm) but, as expected, lower than sapphire (~1.76 at 633 nm) [39, 40]. **Error! Reference source not found.** (left) shows the eposition cycle as a function of thickness for PEALD Al_2O_3 films. This deposition rate is consistent with ALD and PEALD deposition rates reported in the literature [39, 41].

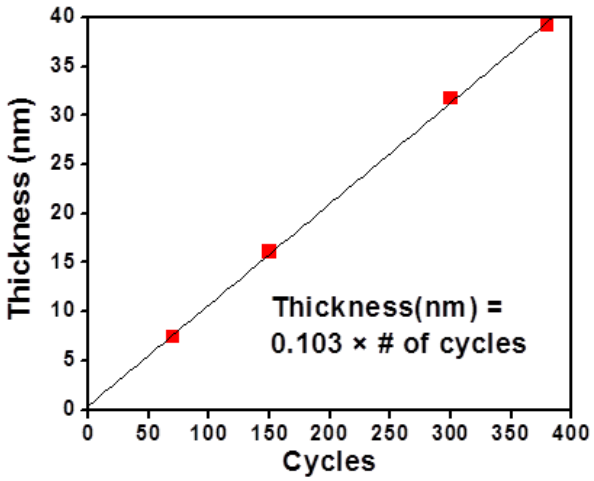


Figure 7. Deposition rate of PEALD Al_2O_3 using TMA precursor and CO_2 plasma at 200 °C. The deposition rate was found to be 0.103 nm per cycle.

While a refractive index value similar to the bulk material is indicative of dense thin-film, in this work the electrical properties of the PEALD thin films are of outmost importance to maximize the transistor performance. Figure 8 (left), shows the leakage current as a function of electric field for two 30-nm-thick PEALD Al_2O_3 films, deposited using two different power densities. The dielectric constant for both films was found to be ~8 by C-V measurements. The deposition rate, refractive index, and breakdown voltage were found to be relatively independent of the deposition details, as shown in Figure 8 (left). The current-voltage characteristics shown in Figure 8 (right) show two clear regions of conduction mechanism. The second region has an exponential increase in current density which can be attributed to the onset of Fowler-Nordheim (FN) tunneling dominance. Subsequent Al_2O_3 films shown in this chapter were deposited using the optimized conditions as shown in Figure 6.

Power Density (W/cm^2)	Deposition rate (Å/cycle)	Refractive Index at 633 nm	Soft Breakdown (10^{-7} A/cm^2) (MV/cm)
0.25	1.03	1.63	~ 6.5
0.064	1.03	1.64	~ 7

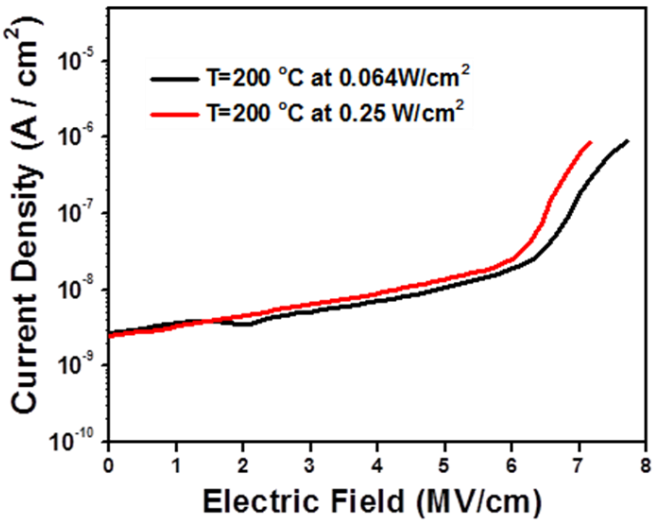


Figure 8. (left) Deposition rate and refractive index for PEALD Al_2O_3 are fairly insensitive to deposition parameters; (right) leakage current density as a function of applied field for Al_2O_3 metal-insulator-metal structures deposited at two different power densities.

Unlike Al_2O_3 deposited by either ALD or PEALD using TMA as precursor, ZnO deposition parameters, using diethyzinc (DEZ) as precursor, can drastically vary the deposition rate, material density, and crystal orientation. The majority of the parameter space investigated was at a fixed temperature of 200 °C. Other deposition temperatures were also investigated, as shown later, but 200 °C was primarily investigated because of its compatibility with low-cost substrates like plastics and glass. ZnO deposition parameters were investigated to maximize field-effect mobility. Choosing field-effect mobility as a parameter to be optimized assumes Ohmic contacts to ZnO; however, experimental and simulation evidence show a 0.1 eV contact barrier [42]. This means that the extracted field-effect mobility may be masked by contact effects. Using a similar approach to the Al_2O_3 thin-film deposition optimization, various deposition parameters were investigated to optimize ZnO thin films. While the growth rate is dependent on the metal organic (DEZ) pulse time, as shown in Figure 9 (left), the most important parameter, apart from

deposition temperature, to obtain high field-effect mobility in ZnO thin films is the deposition plasma power density. The deposition rate for optimized ZnO thin films is shown in Figure 9 (right).

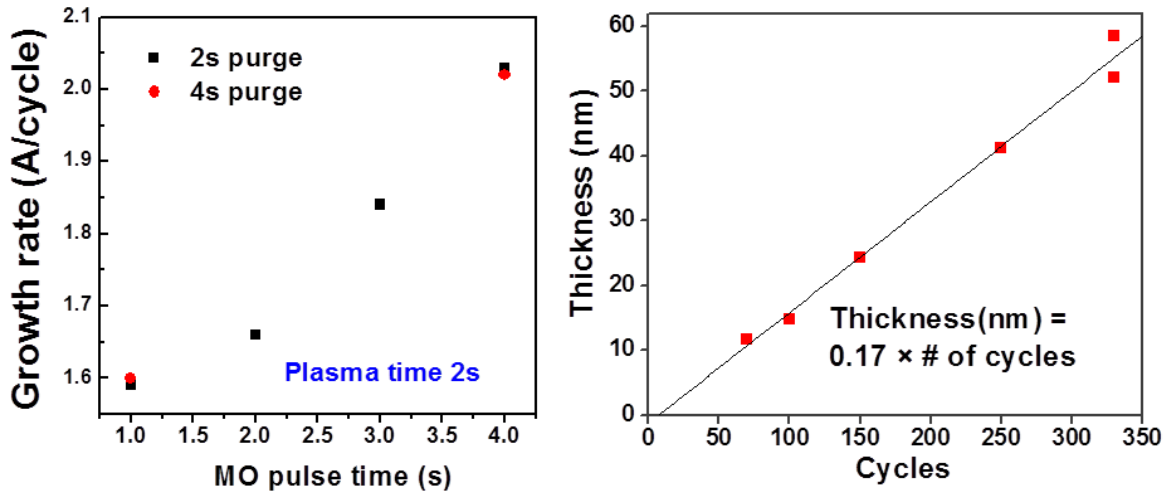
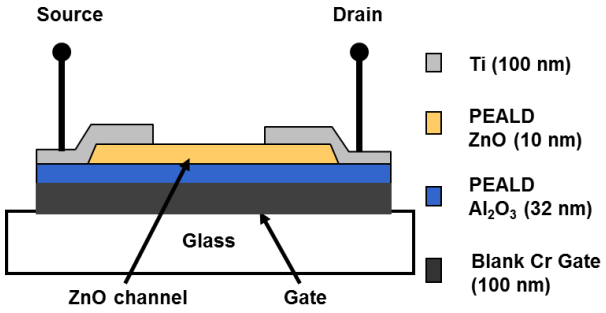


Figure 9. Deposition rate of PEALD ZnO using DEZ precursor at 200 °C. (left) PEALD ZnO growth rate as a function of DEZ pulse time, the other parameters were fixed. (right) ZnO deposition rate is 0.17 nm per cycle and depended on the deposition parameters.

The effect of plasma power density was investigated by depositing films and fabricating ZnO TFTs. Plasma power is known to create defects and/or sputter off material when operated at high densities [31]. Simple devices, using a blanket gate, were fabricated with 32-nm-thick PEALD Al_2O_3 as gate dielectric and 10-nm-thick PEALD ZnO as active layer. The gate dielectric for all the samples was deposited under the same optimized conditions while the active layer was deposited using different plasma power densities. Deposition parameters, including the different plasma power densities, are shown in Figure 10 (right). After Al_2O_3 and ZnO deposition, 100-nm-thick Ti contacts were formed by lift-off. The ZnO was then isolated to reduce the OFF-current. The devices were not passivated to avoid a threshold voltage (V_T) and turn-on voltage

(V_{ON}) shift induced by a chemical reaction between the semiconductor and the ALD-deposited Al_2O_3 passivation layer [43]. A cross-sectional schematic of the TFT structure is shown in Figure 10 (left).



Power Density	0.06, 0.24, and 0.77 W/cm^2
Pressure	1 Torr
Total Flow	900 sccm
DEZ Flow	250 sccm

Figure 10. (left) Unpatterned bottom-gate ZnO TFT cross-sectional schematic. This structure was used for rapid device fabrication; (right) Summary of deposition parameters used to deposit ZnO thin films.

Figure 11 (left) shows drain current (I_{DS}) versus gate voltage (V_{GS}) at a drain voltage of V_{DS} = 8 V with a W / L = 200 µm / 20 µm for ZnO deposited at three different power densities. While a direct comparison is slightly complicated because of the different V_{ON} and V_T as a function of plasma power density, the slope and current drive above threshold clearly shows that ZnO films deposited at 0.06 W/cm^2 have the highest ON-current (~307 µA/mm). Figure 11 (right) shows the extracted linear region field-effect mobility as a function of different deposition plasma-power densities for the ZnO thin films. Lower power density was investigated but no further improvement was seen and striking plasma reliably at very low powers is not trivial.

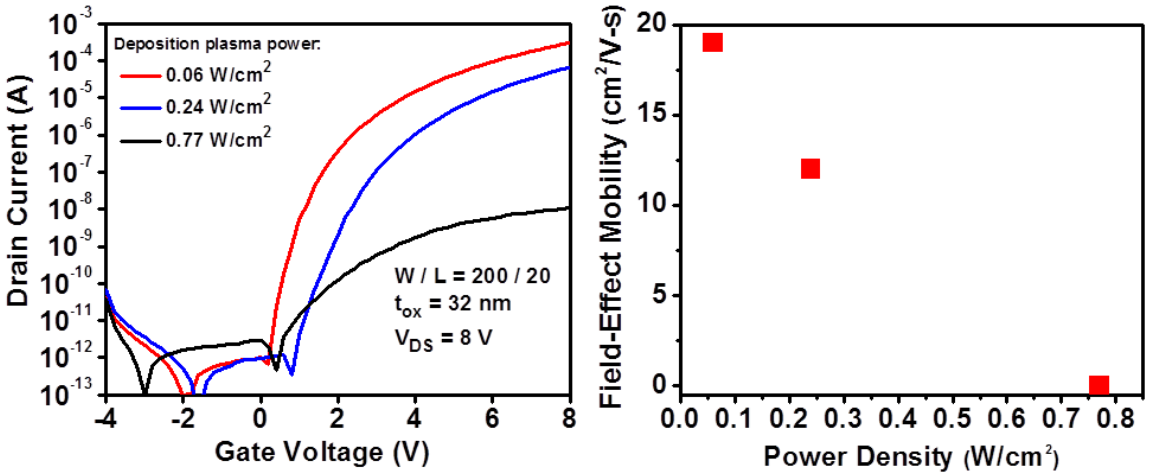


Figure 11. (left) Linear region (V_{DS} = 0.5V) I_{DS} versus V_{GS} for ZnO films deposited at different plasma power densities; (right) extracted linear-region field-effect mobility as a function of deposition power density. Low deposition power density for ZnO films yields higher electrical performance.

In order to understand changes in the microstructure of the ZnO thin films as a function of plasma power density, ZnO films deposited on oxidized silicon wafers were examined by X-ray diffraction and spectroscopic ellipsometry. Under spectroscopic ellipsometry small changes in refractive index were seen, within the measurement and model error. Figure 12 shows a 2-theta X-ray diffraction scan for the ZnO films deposited at the same power densities as the active layers were deposited for TFTs in Figure 11. The 100 diffraction peak is reduced with decreasing deposition plasma power density, while the 002 peak is preferred. The strong 002 preference indicates the majority of the grains are aligned perpendicular to the surface. Having well-aligned and textured polycrystalline ZnO films yields a highly resistive material that can be used as a depleted semiconductor. Thick non-stoichiometric ZnO films have been shown to have a decrease in film resistivity due to the generation of conduction carriers at the grain boundaries in non-stoichiometric ZnO films and with the crystallite orientations playing a role in the grain boundary heights [44, 45].

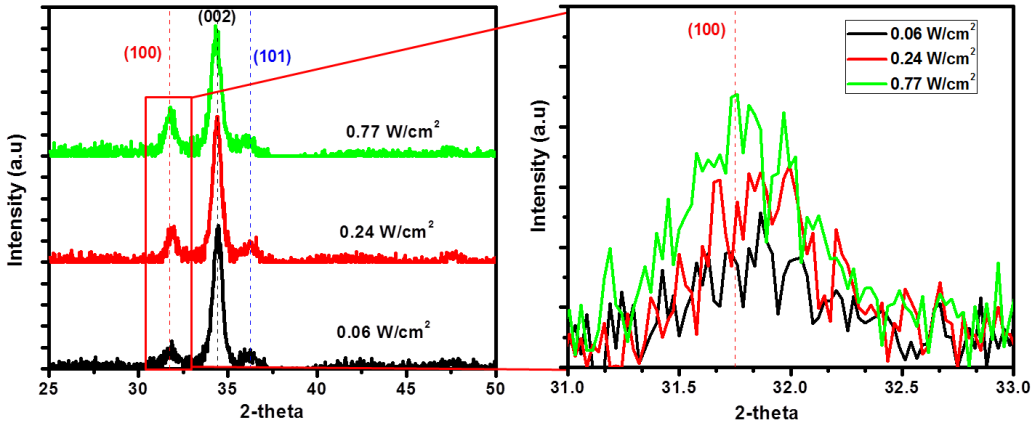


Figure 12. 2-theta X-ray diffraction scan of PEALD ZnO thin films deposited at various plasma power densities according to Figure 10 (right) parameters. As the deposition power density decreases, the 100 peak diminishes with respect to the 002 peak.

Lastly, for exploration completeness of the deposition parameter space, the deposition temperature was briefly surveyed. However, a systematic study to fully optimize the PEALD deposition temperature of the Al_2O_3 gate dielectric and ZnO is still needed. Here, an initial survey of the effect of deposition temperature in electrical performance of the ZnO TFTs is presented. ZnO TFTs were fabricated using the structure shown in Figure 10 and were also unpassivated. The deposition parameters were fixed based on the results shown above and only the deposition temperature was varied. In one case, the gate dielectric was deposited at 200 °C while the active layer was deposited at 280 °C. This particular ZnO deposition temperature was simply selected as a starting point to examine the higher-temperature parameter space without compromising the chamber's seals (fluorocarbon O-rings). Figure 13 (left) shows the I_{DS} versus V_{GS} at V_{DS} = 8 V with a W/L = 200 µm / 20 µm. In these devices the ZnO was not patterned (isolated); therefore the continuous ZnO films over the entire sample also resulted in a slight increase in the OFF-current level. The field-effect mobility, extracted at the same electric field

(2.5 MV/cm) as previous devices, increased to ~31 cm^2/V-s by simply increasing the deposition temperature. This corresponds to a ~60% increase in mobility compared to the ZnO TFTs deposited at 200 °C. Next, ZnO TFTs were fabricated with both the Al_2O_3 gate dielectric and ZnO deposited at 300 °C. Figure 13 (right) shows the I_{DS} versus V_{GS} at V_{DS} = 0.5 V with a W/L = 200 µm / 50 µm. The extracted field-effect mobility in this case increased to ~39 cm^2/V-s. This corresponds to almost a 2-fold increment in mobility, compared to the ZnO TFTs deposited at 200 °C. Further increase of the deposition temperature was not possible because of the heater temperature limitation and the type of O-rings used to seal the chamber. This, nevertheless, highlights a pathway to develop high performance ZnO TFTs deposited by PEALD.

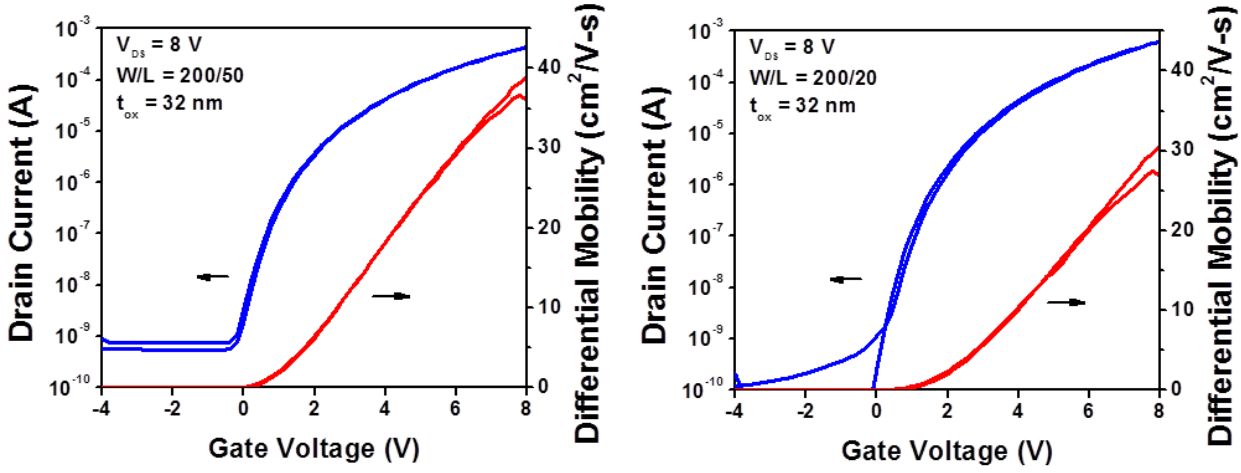


Figure 13. (left) Saturation region (V_{DS} = 8 V) I_{DS} versus V_{GS} for a ZnO TFT with the Al_2O_3 gate dielectric deposited at 200 °C and the active layer deposited at 280 °C. The peak field-effect mobility was ~31 cm^2/V-s. (right) I_{DS} versus V_{GS} for a ZnO TFT with, both, the Al_2O_3 gate dielectric and the ZnO active layer deposited at 300 °C. The peak field-effect mobility was ~39 cm^2/V-s.

2.2.2 Typical ZnO Thin Film Transistors

Thus far, ZnO TFTs deposited under different parameters and in the showerhead PEALD deposition system have been presented. Previous work by this group has shown similar device performance for films deposited at 200 °C using a more conventional pump/purge PEALD deposition system [30]. Also, all the device results shown up to now do not have a passivation layer. However, extensive work has been shown that a passivation layer is very important for many oxide semiconductors to achieve good electrical stability; this is also the case for PEALD ZnO TFTs [43, 46-48]. Because the bulk of the work shown throughout this document is focused on ZnO TFTs with films deposited at 200 °C, prepared either using the showerhead PEALD or the conventional PEALD system, the representative characteristics of passivated devices shown in this section are for the aforementioned deposition temperature. The passivation layer used is Al_2O_3 deposited by ALD at 200 °C [30]. Previously, simple devices with a blanket gate metal were presented. However, to be able to independently address each transistor, particularly when used in a circuit or array application, the gate electrode should be patterned. Figure 14 shows a cross-sectional schematic of a typical bottom-gate staggered PEALD ZnO TFT. The process starts by sputtering and patterning 100-nm-thick chromium to form the gate metal. 32-nm-thick Al_2O_3 gate dielectric and 10-nm thick ZnO active layer are deposited by PEALD. Next, vias through the Al_2O_3 to contact the bottom gate metal are made by wet etching using H_3PO_4 at 80 °C for 50 seconds. The ZnO is then patterned using dilute HCL (4000:1). Ti is deposited by sputtering and patterned by double layer resist (PMMA/1811) lithography and lift-off to form source and drain contacts. Finally, a 30-nm-thick ALD-based Al_2O_3 passivation layer is deposited to complete the device fabrication.

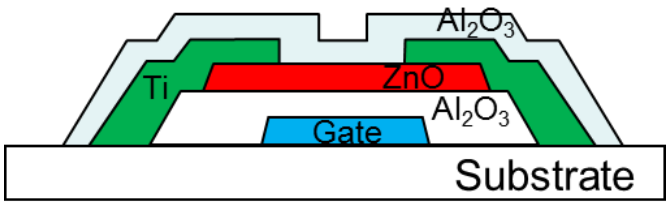


Figure 14. Cross-sectional schematic of a patterned gate PEALD ZnO TFTs with Al_2O_3 and ZnO as gate dielectric and active layer, respectively. The ZnO TFTs are completed with an ALD-based Al_2O_3 passivation layer.

Figure 15 (left) shows representative I_{DS} versus V_{GS} at V_{DS} = 0. 5 V for a passivated ZnO TFT with W/L = 200 µm / 20 µm. Figure 15 (right) shows a representative I_{DS} versus V_{DS} at various V_{GS} values for the same device with good current saturation above threshold. The linear field-effect mobility for passivated ZnO TFTs is typically > 20 cm^2/V-s. The passivation induces a negative voltage shift attributed to back-channel (top ZnO interface) doping due to the chemistry reaction when passivated [43]. The TFT has a turn-on voltage, V_{ON}, (defined here as V_{GS} for I_{DS} = 0.1 nA / mm) of ~ -2 V, making it a depletion mode device. While V_{ON} is shifted negative, the shift is not significant enough to prevent the use of the TFTs in circuit applications. In fact, the passivation layer provides greater benefits, namely excellent electrical stability necessary for stable circuit applications. Previous work by this group have shown similar device performance and a threshold voltage shift (V_T), for passivated devices, of 50 mV after 20 000 seconds of constant stress at 80 °C [30]. Hereafter, the majority of the work presented in this document will use passivated PEALD ZnO TFTs.

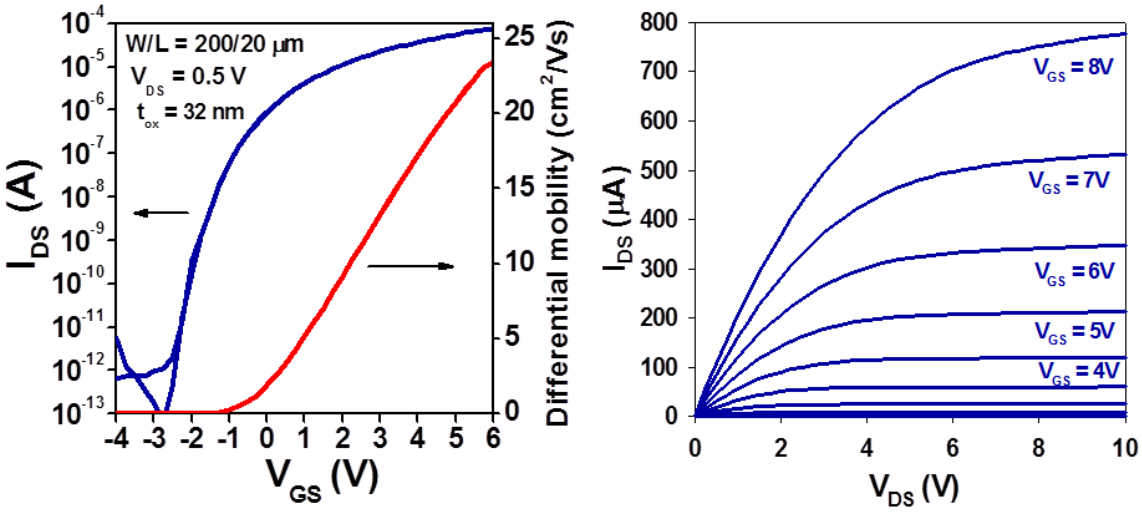


Figure 15. (left) Linear region (V_{DS} = 0.5V) I_{DS} versus V_{GS} for an ALD Al_2O_3 passivated ZnO TFT (W / L = 200 µm / 20 µm) with field-effect mobility over 20 cm^2/V-s; (right) I_{DS} versus V_{DS} characteristics for several values of V_{GS}.

2.3 Pulsed Laser Deposition

The use of a pulsed laser as a directed energy source to evaporate materials for thin film growth has been explored soon after the first laser was built in 1960. The earliest report, in 1965, by H.M. Smith and A.F. Turner describes the use of a ruby laser to deposit a range of materials like Stibnite (Sb_2S_2) and ZnTe among others [49]. Since then, pulsed laser deposition (PLD) has been refined and has been used to deposit a variety of inorganic and organic thin films such as superconductors, semiconductors, metals, insulators, polymers and even biomaterials [50]. PLD is a physical vapor deposition technique that shares some similarities with sputtering and molecular beam epitaxy (MBE). The principle of PLD is relatively straightforward; the laser, operated at a high energy density, ablates some small amount of the target material, creating a plasma column. The process is graphically described in Figure 16. This plasma column provides the material flux to the substrate for film growth. An important advantage of this technique is

that films grown by PLD can have the same stoichiometry as the material from the target (although, not trivial to achieve) [51].

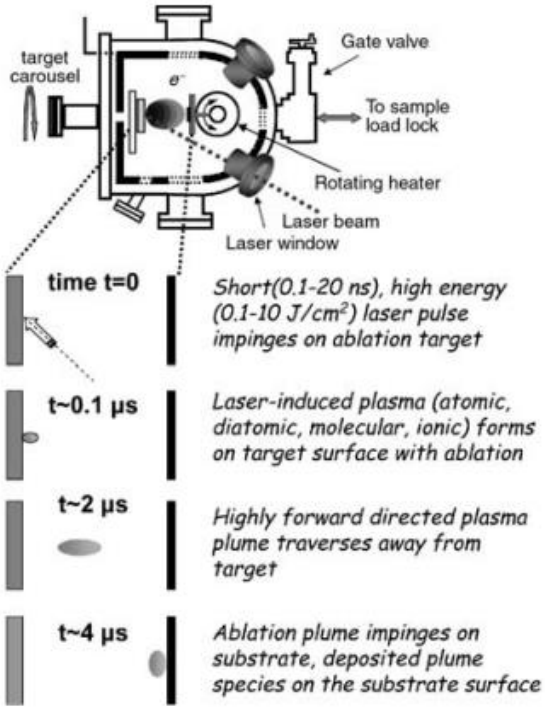


Figure 16. Schematic of a PLD chamber and a schematic of the deposition process. Schematic taken from [51].

PLD technique is an attractive deposition technique to grow high quality, nanocrystalline ZnO thin films on a range of substrates from lattice-matched single crystal to amorphous substrates. Depending on the targeted application, which are quite diverse (i.e. LEDs, solar cells, photodiodes, and as semiconductor), and desired film stoichiometry the deposition parameters like laser wavelength, pulse duration, fluence, oxygen pressure, substrate temperature, substrate-target distance, and even selection of substrate, play a role in the film characteristics [51]. The PLD technique is of particular interest to grow epitaxial band-engineered ZnO/$Zn_{1-x}Mg_xO$ heterostructures because quantum confinement can be achieved by tuning the well width. By

varying the *x* ratio of Mg in the film, the bandgap can be engineered from 3.37 eV up to 4 eV while still maintaining the wurtzite structure [51]. The ability to tune the bandgap is of interests for applications such as UV photodetectors, UV LED (in conjunction with a p-type semiconductor), resonant tunneling diodes (RTDs), and HEMTs. There has also been an interest in using PLD to deposit, under the right parameters, well-oriented, ordered, ZnO polycrystralline films that can be used as semiconductor active material [52-54]. The ZnO film stoichiometry can be widely varied depending on the deposition parameters. This plays an important role in the conductivity of ZnO films as the intrinsic defects such as zinc interstitials, oxygen vacancies, and hydrogen act as donors and the defect density can dictate the film's conductivity [15, 55]. Depending on the application, certain type of defects might be desired in order to tune the emitted light color in LEDS or to reduce optical losses in waveguides. Generally speaking defects in the bandgap are undesirable if the material is used as an active material in a transistor configuration.

2.3.1 ZnO Thin Film Transistors with Active layer Deposited by PLD

There have been various reports of PLD deposited ZnO thin films for TFT applications with different device structures and gate dielectrics with field-effect mobilities ranging from as low as 0.31 cm^2/V-s up to 110 cm^2/V-s [52-54]. The field-effect mobility of polycrystalline ZnO is, of course, not only dictated by the trap distribution in the semiconductor but is also affected by the MOS interface and the quality of the gate dielectric. Bayraktaroglu B. et al. at Air Force Research Labs (AFRL) have demonstrated thin film transistors with ZnO active layers pulsed laser deposited, and post-annealed at 400 °C, with a high field-effect mobility of 110 cm^2/V-s,

and f_T = 500 MHz f_{MAX} = 400 MHz with channel length of 2-µm on semi-insulating GaAs substrates [54]. The device performance of these ZnO TFTs is comparable to polysilicon TFTs. In this work, in collaboration with Dr. Gregg Jessen, Dr. Kevin Leedy and Dr. Burhan Bayraktaroglu from AFRL, the electrical characteristics of PLD ZnO TFTs were measured and compared to PEALD ZnO TFTs. Also, the material similarities and differences are explored in the following section. This comparison was an important piece to better understand the radiation effects in ZnO TFTs, deposited by both techniques, shown in chapter 3.

Figure 17 shows a cross-sectional schematic of the PLD ZnO TFTs. A silicon wafer was used as both substrate and bottom gate. A 30-nm SiO_2 grown by PECVD, at 250 °C, served as gate dielectric. A 50-nm-thick ZnO layer was deposited by PLD using a ZnO target with oxygen background gas followed by a 1-hour anneal in air at 400 °C. The laser operated with an energy density of 2.6 J/cm^2 and a pulse rate of 30 Hz; deposition details can be find in [54]. Lastly, Ti/Pt/Au metal was deposited by evaporation and patterned to form source and drain contacts. The device performance has been optimized by AFRL without a passivation layer and the investigation of a passivation layer for PLD ZnO TFTs is outside of the scope of this work.

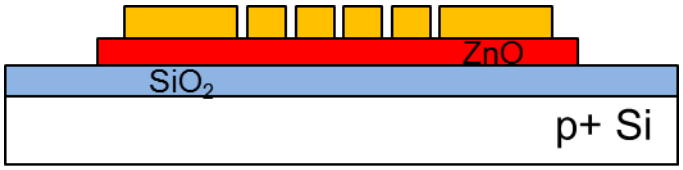


Figure 17. Cross-sectional schematic of a blanket gate PLD ZnO TFTs with SiO_2 and ZnO as gate dielectric and active layer, respectively.

Figure 18 shows representative I_{DS} versus V_{GS} at V_{DS} = 0. 5 V for a PLD ZnO TFT with W/L = 400 µm / 10 µm. The TFT has a turn-on voltage, V_{ON}, (defined here as V_{GS} for I_{DS} = 0.1 nA /

mm) of ~ -0.9 V, making it a depletion mode device. The linear field-effect mobility for the device shown here is ~90 cm^2/V-s; this mobility is 4.5x larger than PEALD ZnO TFTs deposited at 200 °C. A field-effect mobility spread between 60-110 cm^2/V-s was seen across many different PLD-deposited ZnO samples and devices tested. The average field-effect mobility in PLD ZnO TFTs is still larger than the mobility in PEALD ZnO TFTs which encourages a survey of the materials' characteristics.

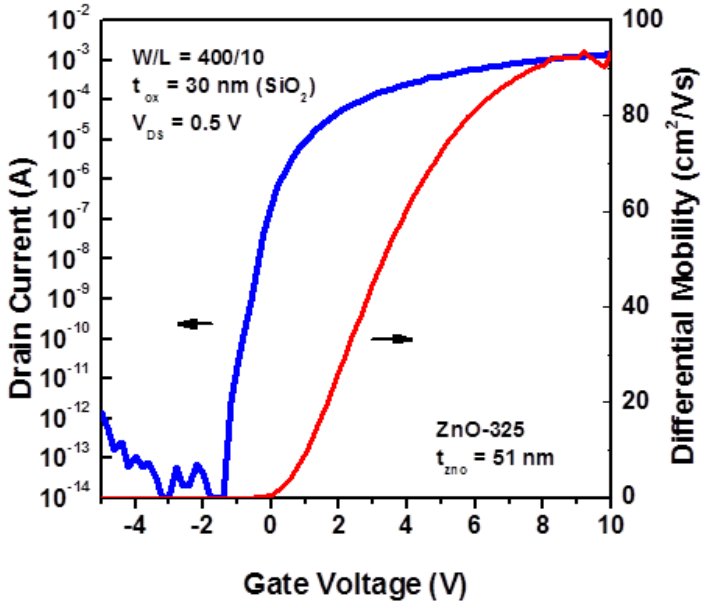


Figure 18. Linear region (V_{DS} = 0.5V) I_{DS} versus V_{GS} for a PLD ZnO TFT (W / L = 200 µm / 20 µm) with a PECVD deposited SiO_2 gate dielectric. In this device the field-effect mobility is 90 cm^2/V-s. The field-effect mobility measured in these devices ranged from 60-110 cm^2/V-s.

2.4 Materials Comparison of PEALD and PLD ZnO Thin Films

Representative ZnO thin films (~50 nm) deposited by PLD and PEALD, were characterized by grazing-incidence x-ray diffraction (GIXRD). The scans shown in Figure 19 highlight the similarity of diffraction peak orientation for both ZnO films used in this work independent of the

growth technique. These results indicate both films are highly textured with a preferential (002) growth orientation. The intensity counts were normalized to facilitate comparison.

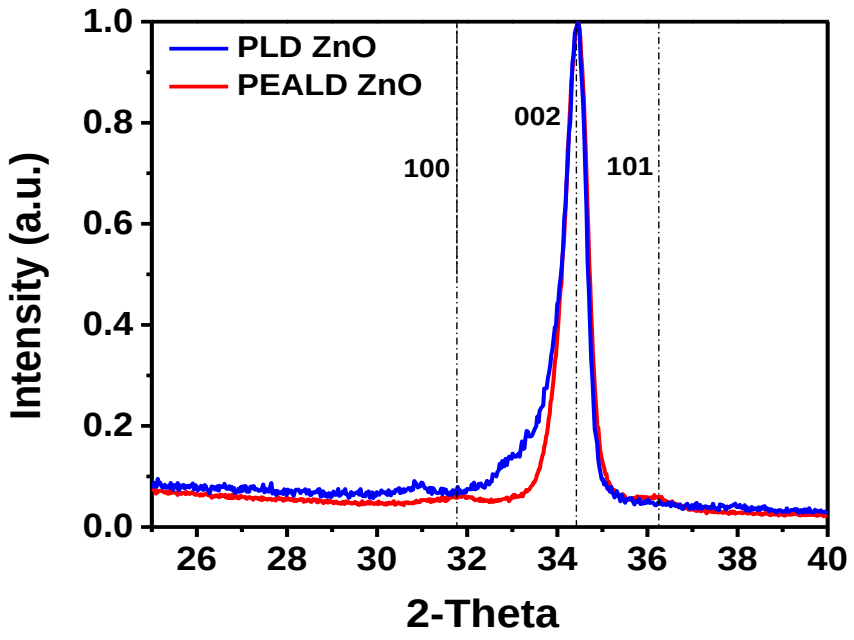


Figure 19. Grazing incidence XRD of ZnO thin films (50 nm) deposited by PLD and PEALD both show highly textured films with (002) orientation and similar coherence length suggesting similar grain size. The coherence length for PEALD and PLD ZnO films is estimated, using Scherrer's equation, to be ~7 nm and ~7.2 nm, respectively.

The coherence length for both films was estimated using Scherrer's equation, where K is the shape factor, λ is the X-ray wavelength, B is the line broadening at full-width half maximum (FWHM), and θ the Bragg angle.

$$\tau = K\lambda / B\cos\theta$$

The Scherrer's formula provides a lower bound of the film's crystallite size because a variety of other factors can contribute to the width of a diffraction peak including instrumental effects, inhomogeneous strain, grain boundaries, and stacking faults to name a few [56]. Without taking

into account the exact details of the diffraction shape and size, an estimated coherence length for PEALD and PLD ZnO films was found to be ~7 nm and ~7.2 nm, respectively.

To further investigate the ZnO thin films' grain size, cross-sectional transmission electron microscopy (TEM) was carried out on standard device structures with the active layer deposited by both PEALD and PLD. The TEM and SEM pictures of the PEALD ZnO TFT were taken by Brandon Smith in Chemical Engineering at Penn State. Figure 20 (left) shows a cross-sectional scanning electron microscope (SEM) picture of a PEALD ZnO TFT structure on a glass substrate with the material stack comprising of 100-nm chromium gate metal, 32-nm Al_2O_3 gate dielectric, 10-nm ZnO active layer, and 30-nm Al_2O_3 passivation layer. Figure 20 (right) shows a cross-sectional TEM image with columnar and closely packed grains extending through the film thickness which is consistent with the preferential (002) texturing seen by XRD. The ZnO grain size, estimated from TEM images, varies from ~7-12 nm, comparable to the film thickness (10 nm).

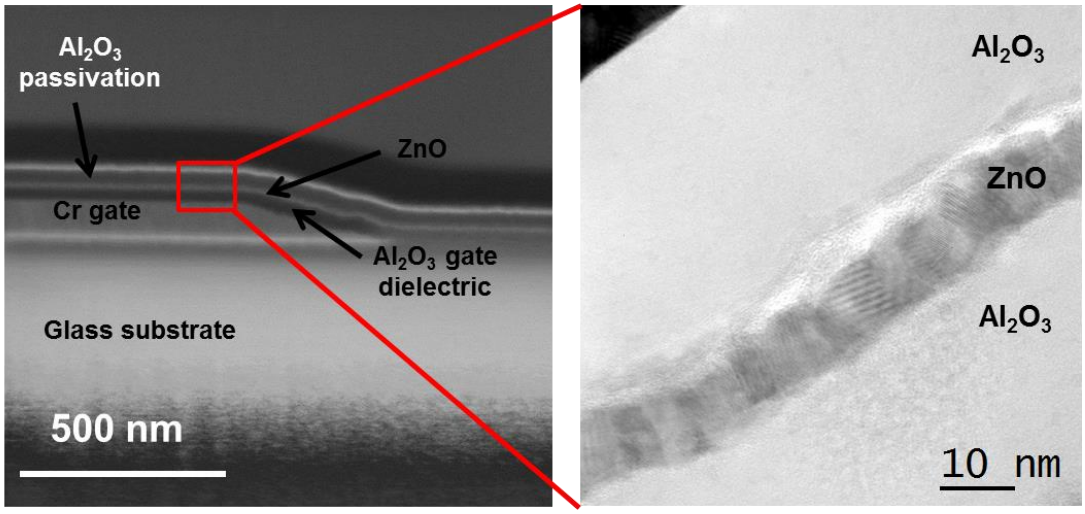


Figure 20. (left) Scanning electron microscope (SEM) image of a PEALD ZnO TFT; (right) transmission electron microscope (TEM) over the channel region of the TFT. PEALD ZnO TFTs shows a densely packed polycrystalline structure with grain size of the order of the thickness (~10 nm).

Similarly, TEM images of PLD ZnO TFTs were taken at AFRL. Figure 21 shows a cross-sectional TEM image of a TFT structure with PLD ZnO TFT on an oxidized silicon substrate with the material stack comprising of a Ni/Au gate metal, PECVD-deposited ~20-nm SiO_2 gate dielectric, and ~55-nm ZnO active layer. Similarly to the PEALD-deposited ZnO thin-film, the PLD-deposited ZnO thin-film also shows a microstructure with grains preferentially aligned perpendicular to the surface. This is also consistent with the XRD scans taken for the PLD films (as shown in Figure 19). . From the TEM image, the ZnO grain size is estimated to be ~20-40 nm, substantially larger than the grain size seen in TEM images of PEALD ZnO film.

The difference in grain size between PLD and PEALD ZnO thin films could be a cause of the relatively lower field-effect mobility seen in the PEALD ZnO films. Hossain F. M. et al., have modeled the effect of grain boundaries in polycrystalline ZnO TFTs [57]. The analysis in [57] makes several assumptions such as a defect-free MOS interface, equally-spaced grain

boundaries, and a single-valued Gaussian defect distribution (both donor-like and acceptor-like defects) at the grain boundaries. The trap distribution will cause band bending at each grain boundary (double Schottky barrier or potential barrier height) in order to reach electrostatic equilibrium. Therefore, the number of grain boundaries across the channel length can affect the field-effect mobility. Hossain F. M. et al., show simulated I_{DS} versus V_{GS} characteristics as a function of effective number of grain boundaries (2-dimensionally) resulting in a decrease in field-effect mobility as the number of grain boundaries across the channel length increases. While the assumptions made in their formalism may also affect the field-effect mobility, the relatively smaller grain size in PEALD films compared to PLD films suggests that the lower device performance may be, at least, partly related to the film's grain size (and work by Liu Y.-C. [42] suggests different trap densities for ZnO PLD and PEALD films also play a role in field-effect mobility).

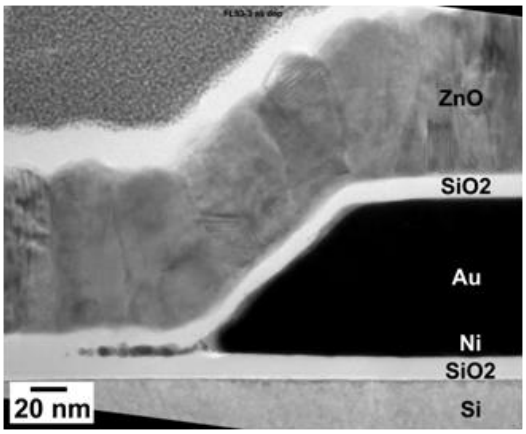


Figure 21. Transmission electron microscope (TEM) of PLD ZnO TFT. The ZnO thin film shows a densely packed polycrystalline structure with grain size in the order of 20-40 nm.

Spectroscopic ellipsometry was used to look for differences in optically active defects in the materials (PEALD and PLD films) by measuring polarization (electric polarizability), ε_1, as a

function of photon energy. The curve fitting was done by Dr. David Saint-John from Materials Science and Engineering at Penn State. The measured ZnO films (50 nm) were deposited over their respective optimized gate dielectric (PECVD SiO_2 for PLD ZnO films and PEALD Al_2O_3 for PEALD ZnO films) on oxidized silicon substrate. The films were measured and fitted in from 1 eV to 5 eV with excellent agreement between the experimental and model data. The ZnO films were fitted to a two-layer model using two Tauc-Lorentz oscillators (for the bulk of the ZnO) and an effective medium approximation (to account for inhomogeneity) with a fit of < 5% void fraction.

The complex dielectric function, $\boldsymbol{\varepsilon} = \varepsilon_1 + i\varepsilon_2$, contains information regarding the electric polarizability (ε_1) and absorption (ε_2) of the material. The second component of the complex dielectric function (the absorption coefficient, ε_2) starts contributing to the dielectric functions when the ZnO material starts to absorb. The absorption coefficient is extracted from the complex dielectric function, using the parameterization described above. Comparing ε_2 for ZnO grown by PLD and PEALD, as shown in Figure 22, indicates PLD-deposited ZnO has a sharper on-set absorption slope than PEALD-deposited ZnO. This suggests ZnO deposited by PEALD likely has a broader tail-state distribution than ZnO deposited by PLD. The implication of these states below the conduction band minimum in the TFT characteristics result in a "softer" turn-on voltage (near $V_{GS} \approx V_T$) of the device (as these states need to be filled as the Fermi level is moved up); thus, the I_{DS} versus V_{GS} characteristics deviate from the ideal square-law long-channel MOSFET theory. In section 3.1.2 a compact model to account for this and other non-idealities is discussed. The broader tail distribution in PEALD ZnO TFTs, below the conduction band minimum, has been qualitative replicated in modeling experiments using an exponential

function, as shown in Figure 23 (left) [42]. On the other hand, PLD ZnO TFTs does not require this exponential function to fit the experimental results, as shown in Figure 23 (right). The presence of subgap tail states is consistent with the analysis of a similar oxide semiconductor (IGZO) by Kamiya T. et al where tail states where found 10-150 meV below the conduction band minimum [58].

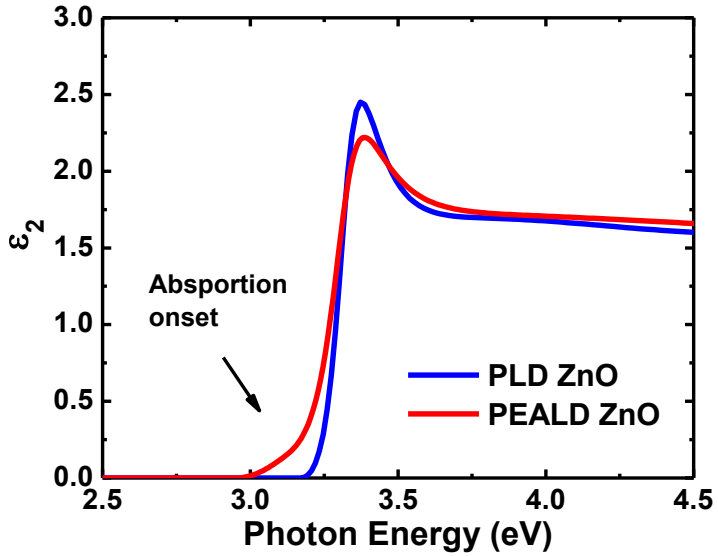


Figure 22. Absorption coefficient extracted by parameterization using spectroscopic ellipsometry. PEALD ZnO films have a slower absorption onset than PLD ZnO films suggesting a broader tail-state distribution for PEALD ZnO films.

Lastly, to qualitatively connect the observations of the materials differences with the electrical characteristics and suggest a possible density of states, temperature-dependent DC voltage-current measurements of PEALD and PLD ZnO TFTs taken by Yi-Chun Liu revealed a weaker V_T dependence with increasing temperature for PLD ZnO TFT compared to PEALD ZnO TFTs [42]. The temperature dependent I-V in conjunction with quasi-static C-V characteristics, for both PEALD and PLD, were used to calibrate a technology computer aided design (TCAD) model (using drift-diffusion physics) representative of the device characteristics. To account for

the non-idealities in the I-V characteristics, such as the "softer" turn-on voltage near the subthreshold region, trap distributions had to be included into the model [42]. Figure 23 shows the density of states used to model both the PEALD and the PLD ZnO TFTs. While the trap distributions' shape and magnitude are not unique, they give a picture of the different trap distribution in ZnO films deposited by each technique. The key aspect is that only 2 defect energy levels, with smaller magnitude, are needed to fit the ZnO PLD TFTs compared to 3 defect energy levels, with larger magnitude, needed to fit the ZnO PEALD TFTs. The additional defect distribution above conduction band minimum is needed to match the I-V characteristics when V_{GS} is much larger than V_T. According to preliminary low temperature photoluminesce (PL), cubic inclusions are seen in PEALD ZnO films and not in PLD ZnO films. This could be a reason of the need to include this above conduction band trap distribution and the tail states only in PEALD ZnO films. In section 6.2, more information regarding the preliminary PL data is given and future work is suggested to further investigate the dominating factors in the electronic transport of polycrystalline ZnO and guide the material's growth conditions to obtain higher performance films. Kamiya T. et al., have demonstrated similar trap distributions in IGZO oxide semiconductor (for both crystalline and amorphous form) to the density of states shown in Figure 23 [58, 59]. In the study, the carrier transport was examined based on a percolation conduction model [59]. Percolation conduction can be simply explained as a series of different carrier (electrons) conduction paths with different potential fluctuations (barrier heights) causing different conductance for electron transmission over the potential barriers; thereby dependent on temperature (the transmission probability is governed by the exponential dependence on temperature according to Boltzmann distribution) [59, 60]. This model does not take into account the in-grain mobility for a polycrystalline material because it assumes that the potential barriers

are the dominant factor determining the carrier transport. Based on the trap distributions shown in Figure 23, with trap distributions below and above the conduction band minimum, a percolation model may also explain the carrier transport mechanism in polycrystalline ZnO films; although, the distribution of potential barriers and height above the conduction band minimum is likely to be different for PEALD and PLD ZnO films, as suggested by the weaker V_T dependence in PLD ZnO films and the field-effect mobility.

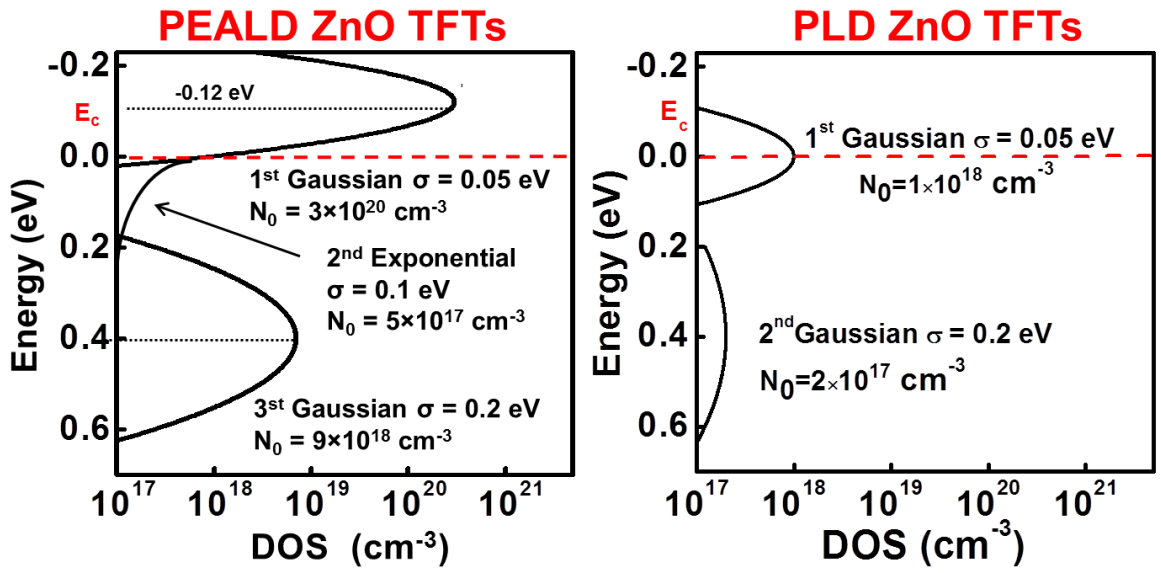


Figure 23. Trap distributions used to fit the experimental data to model ZnO TFTs with active layers prepared by both PEALD and PLD.

The subtle differences in the microstructure of PEALD and PLD ZnO thin films may play a role in the lower performance of the PEALD ZnO TFTs compared to PLD ZnO TFTs. Nevertheless, they both exhibit relatively high mobility compared to other material systems deposited at similar temperatures. In the next chapter it will be shown that regardless of the subtle microstructure differences polycrystalline ZnO TFTs are equally radiation resistant.

Chapter 3

3.1 Radiation-Hard ZnO TFTs

Radiation tolerant electronics are of interest for applications such as radiation sensors, nuclear reactors, x-ray imagers, and high-energy particle accelerators. While properly designed Si MOSFETs are radiation hard (>1 Mrad(SiO_2) tolerance), most thin-film transistors (TFTs), including polysilicon and a-Si:H, are severely degraded by relatively low irradiation doses (often much less than 1 Mrad(SiO_2)) [61-63]. Recently, reports on oxide-based semiconductors like indium-zinc-oxide (IZO) and indium-gallium-zinc-oxide (IGZO) TFTs have shown severe degradation (V_{ON} shift > -15 V) for <2 Mrad(SiO_2) gamma ray exposure [64, 65]. A radiation resistant thin-film transistor technology would open up new applications for large-area imaging, detection, or monitoring in high radiation environments.

ZnO has the potential for improved radiation tolerance compared to conventional covalent semiconductors, such as silicon or GaAs. In metal oxides the bonding is strongly ionic and energy states near the conduction band minimum derive primarily from cation (Zn) σ-orbitals [8]. This is in contrast to covalent semiconductors where sp^3 hybrid orbital bonding is sensitive to both bond angle and bond length disorder and localized states can be easily created by radiation effects. In ionic semiconductors, like ZnO, the nearly spherical σ-orbitals result in electron transport that is largely unaffected by bond angle or bond length disorder [10, 11].

*Some of the results in this chapter were previously reported in the peer-review publication:
Ramirez J.I. et al. IEEE TNS 62, no. 3 (2015): 101109

Good radiation tolerance has been demonstrated for single crystal ZnO [66, 67]. In this chapter the effects of gamma ray exposure on polycrystalline ZnO TFTs are investigated. The bottom gate TFTs in this work used ZnO semiconductor thin films deposited by two different growth techniques: pulsed laser deposition (PLD) and plasma-enhanced atomic layer deposition (PEALD). The effects of gamma ray irradiation on ZnO TFTs deposited by both techniques are investigated. The similarities and differences between them are addressed. Next, a study of the effect of electrical bias during irradiation on ZnO TFTs is described. Very little difference in radiation effects for electrically biased and unbiased devices is found. In section 3.5, measurement artifacts for bottom gate TFTs, similar to some seen in radiation testing of fully-depleted Si SOI FETs [68], are identified and recommendations are made to prevent them. Lastly, a systematic study was carried out to identify the physical location of irradiation-induced charge in ZnO TFTs. The work described in this chapter was in collaboration with Dr. Gregg Jessen, Dr. Kevin Leedy and Dr. Burhan Bayraktaroglu from Air Force Research Labs.

Irradiation of samples was done at the Gamma Irradiation Facility of the Radiation Science and Engineering Center at Penn State University with ^{60}Co sources (1.17 and 1.33 MeV gamma rays). Two ^{60}Co irradiators were used for this work: an irradiator with a dose rate of ~0.5 Mrad(SiO_2)/hour for high dose experiments; and an irradiator with a dose rate of ~0.01 Mrad(SiO_2)/hour for lower dose experiments. Doses are provided in equivalent SiO_2 dose for convenience in comparing to other work.

3.1.1 ZnO Device Structures under Radiation Test

PEALD was used to grow the thin-films for the first set of ZnO TFTs with a structure shown in Figure 24. Borosilicate glass was used as substrate with 100-nm Cr layer deposited by sputtering and patterned to form gate metal. 32-nm-thick Al_2O_3 gate dielectric and 10-nm-thick ZnO active layer were deposited at 200 °C by weak oxidant PEALD using trimethyl aluminum and diethyl zinc, respectively [30]. Ti (100 nm) was deposited by sputtering and patterned by lift-off to form source and drain contacts. The ZnO PEALD TFTs were completed with a 30-nm ALD Al_2O_3 passivation layer.

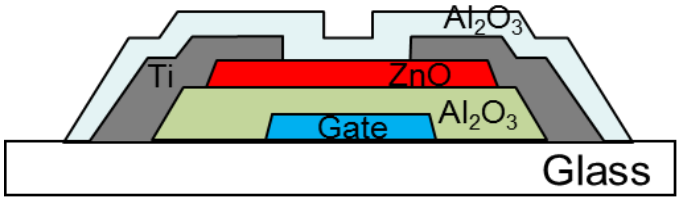


Figure 24. Bottom-gate PEALD ZnO TFT schematic cross-section. The TFT uses a 100-nm Cr gate, 32-nm PEALD Al_2O_3 gate dielectric, 10-nm PEALD ZnO active channel, Ti source-drain contacts, and 30-nm ALD Al_2O_3 passivation layer fabricated on a glass substrate.

The second set of ZnO TFTs used an active channel region grown by PLD and had a structure as shown in Figure 25. A p+ silicon wafer was used as both substrate and bottom gate. A 30-nm SiO_2 grown by PECVD, at 250 °C, served as the gate dielectric. A 50 nm ZnO layer was deposited by PLD at 200 °C using a ZnO target in a O_2 ambient followed by a 1 hour 400 °C anneal in air [54]. Lastly, Ti/Pt/Au metal was deposited by evaporation and patterned to form source and drain contacts.

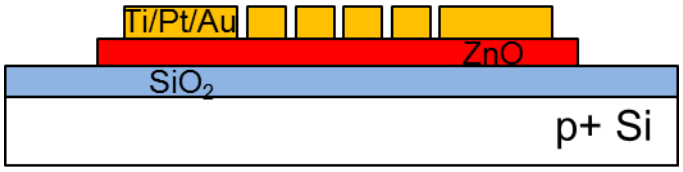


Figure 25. Bottom gate PLD ZnO TFT schematic cross-section. The TFT uses a 30-nm PECVD SiO_2 gate dielectric, 50-nm PLD ZnO active channel, and Ti/Au source-drain contacts on Si as substrate and gate.

The ZnO films deposited by both PEALD and PLD are polycrystalline films composed of densely compacted, columnar grains that often extend through the thickness of the film [30]. ZnO films from both deposition methods exhibited only a (002) orientation, determined by X-ray diffraction [30, 54, 69].

3.1.2 Accounting for Non-idealities in ZnO devices for Accurate Parameterization

The TFT turn-on voltage (V_{ON}), defined here as V_{GS} for I_{DS} = 0.1 nA / mm, field-effect mobility, and threshold voltage (V_T) were extracted from the current-voltage characteristics. To extract threshold voltage, a modified threshold voltage extraction method was used to account for the non-idealities commonly seen in oxide-based TFTs [70] as discussed in section 2.4.

For a MOSFET where the field effect mobility is not a function of gate voltage and when velocity saturation is not important the current-voltage characteristics in saturation are well-described by

$$I_D = K(V_{GS} - V_T)^2 \quad \text{where } K = \frac{\mu_n C_{ox}}{2}\frac{W}{L}.$$

Such MOSFETs are often referred to as square law devices because for $V_{GS} > V_T$ a plot of $\sqrt{I_D}$ versus V_{GS} results in a straight line and the threshold voltage, V_T, is easily found by extrapolating to $I_D = 0$. However, for some MOSFETs and particularly for many thin film transistors, including ZnO, IGZO, and a-Si:H devices, the field-effect mobility increases with increasing$V_{GS} - V_T$. This behavior can result from trap distributions [42], band edge barriers [71], or other factors (some of these factors are discussed in section 2.4). The details can be complicated, but it has been found that the current-voltage characteristics for such devices can often be fit by

$$I_D = K(V_{GS} - V_T)^m$$

where *K* and *m* are fitting parameters [70]. For this approach,

$$H(V_G) \cong \frac{\int_{V_T}^{V_G} I_{D,sat}(V_G)dV_G}{I_{D,sat}} \text{ and } (V_G) = \frac{(V_G - V_T)}{m+1}$$

H (V_G) versus V_G is linear for $V_{GS} > V_T$ and extrapolating to $I_D = 0$ gives a value for V_T that does not depend on V_G. We have used this approach to extract V_T in this work.

3.2 ^{60}Co Irradiation of Electrically Unbiased ZnO TFTs

Current-voltage characteristics for PEALD and PLD TFTs were measured before and after 10 Mrad(SiO_2) ^{60}Co gamma ray exposure. For both device types the TFTs still operate after gamma ray exposure with little change in mobility or off-current. Figure 26 shows I_{DS} versus V_{GS} characteristics at V_{DS} = 0.5 V for a PEALD ZnO TFT with dimensions W / L = 200 µm / 20 µm before irradiation, after 10 Mrad(SiO_2) ^{60}Co gamma ray irradiation, and after a 200 ˚C, 1 minute

anneal in air. The turn-on voltage, V_{ON}, for devices before irradiation is -2 V and the threshold voltage, V_T, extracted as described above, is -0.6 V. After 10 Mrad(SiO_2) exposure the irradiation induced shift, ΔV_{ON}, is -0.9 V and ΔV_T is -0.6 V. The extracted linear region field-effect mobility is ~15 cm^2/V-s for V_{DS} = 0.5 V before and after irradiation. Some earlier reports for other oxide semiconductor TFTs exposed to radiation found an increase in field-effect mobility, for testing both with and without bias during irradiation [64, 65]. This apparent increase in mobility is due to a negative V_T shift with irradiation, together with the well-known accumulation dependent field effect mobility in oxide TFTs [72].

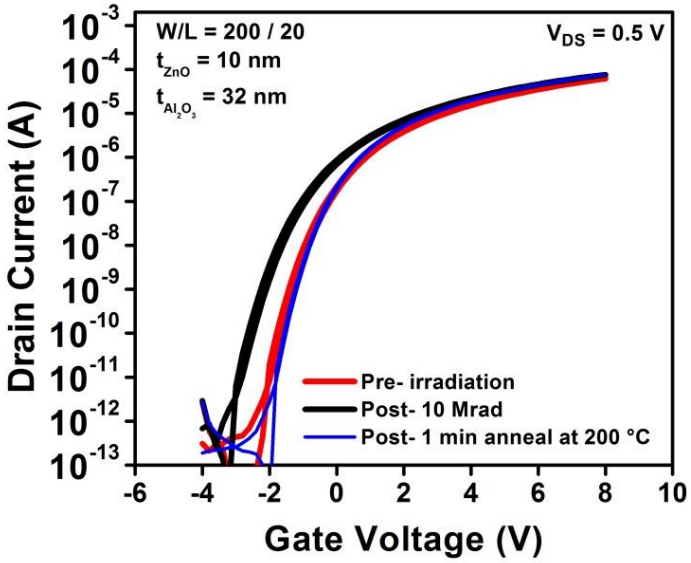


Figure 26. Linear region (V_{DS} = 0.5 V) I_D versus V_{GS} for a PEALD ZnO TFT before irradiation, after 10 Mrad(SiO_2) ^{60}Co gamma ray irradiation, and after irradiation and a 200 ˚C, 1 min anneal in air.

Figure 27 shows I_{DS} versus V_{GS} characteristics at V_{DS} = 0.5 V for a PLD ZnO TFT with dimensions W / L = 400 µm / 10 µm before irradiation, after 10 Mrad(SiO_2) ^{60}Co gamma ray irradiation, and after a 200 ˚C, 1 minute anneal in air. The turn-on voltage, V_{ON}, for devices before irradiation is -0.9 V and the threshold voltage, V_T, is 0.2 V. The linear region field-effect

mobility before irradiation is 60 cm^2/V-s. Device characteristic changes after 10 Mrad(SiO_2) ^{60}Co gamma ray irradiation for PLD ZnO TFTs are similar to PEALD ZnO TFTs. The linear field-effect mobility, accounting for an irradiation induced negative V_T shift, decreased slightly to 55 cm^2/V-s (<10% decrease). After 10 Mrad(SiO_2), the PLD ZnO TFTs had a V_{ON} shift of -3.4 V and a V_T shift of -1.8 V.

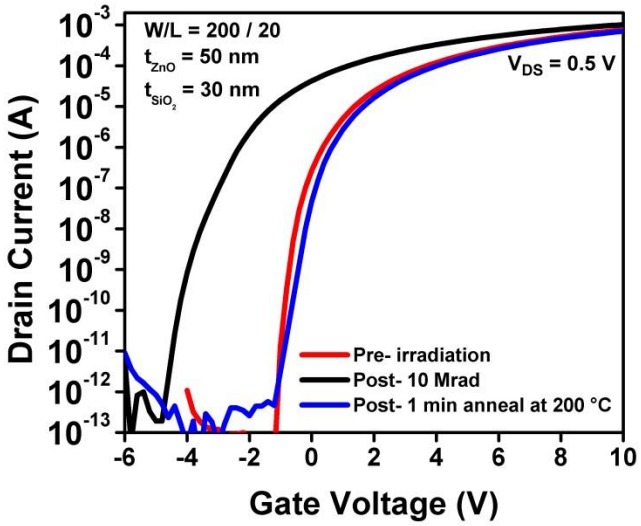


Figure 27. Linear region (V_{DS} = 0.5 V) I_D versus V_{GS} for a PLD ZnO TFT before irradiation, after 10 Mrad(SiO_2) ^{60}Co gamma ray irradiation, and after irradiation and a 200 ˚C, 1 min anneal in air.

The larger irradiation-induced shift in V_{ON} compared to V_T can be explained by assuming that irradiation results in charge at the back of the ZnO active layer (that is, the ZnO interface farthest from the gate). Work related to passivation of ZnO TFTs by Mourey et al. found, by two-dimensional modeling, that a charge sheet at the back interface results in a larger shift in V_{ON} than V_T [43]. A back interface charge model can also explain the larger shift in V_{ON} for PLD ZnO TFTs with irradiation than for PEALD ZnO TFTs. Charge at the back interface acts across the series combination of gate dielectric and depleted ZnO layer capacitances. That is, gate

dielectric and active semiconductor act as two capacitors in series. For PEALD TFTs with 32 nm thick Al_2O_3 gate dielectric and 10 nm thick ZnO active layer and using $\varepsilon = 8\varepsilon_0$ for both Al_2O_3 and ZnO gives a capacitance of 180 nF / cm^2. The irradiation induced V_{ON} shift of -0.9 V corresponds to a charge of $\Delta Q = C \cdot \Delta V_{ON} = 1\times10^{12}$ electronic charges/cm^2. For the PLD TFTs with 30 nm thick SiO_2 gate dielectric and 50 nm thick ZnO active layer and using $\varepsilon = 3.9\varepsilon_0$ for the SiO_2 and $\varepsilon = 8\varepsilon_0$ for the ZnO gives a capacitance of 61 nF / cm^2. The irradiation induced V_{ON} shift of -3.4 V corresponds to a charge of $\Delta Q = C \cdot \Delta V_{ON} = 1.3\times10^{12}$ electronic charges/cm^2. This suggests the apparent larger shift in V_{ON} for PLD ZnO TFTs is related to the smaller capacitance per unit area in this structure, but when converted into charge per unit area, the radiation-induced shifts are similar for both device types. Figure 28 summarizes the comparison between PEALD and PLD ZnO TFTs for 10 Mrad(SiO_2) irradiation.

	ΔV_{ON} (V)	ΔV_T (V)	ΔField effect mobility (cm^2/V-s)	ΔQ (/cm^2) (Induced by radiation)
PEALD ZnO TFTs	-0.9	-0.6	0	1×10^{12}
PLD ZnO TFTs	-3.4	-1.8	-5	1.3×10^{12}

Figure 28. Comparison of device characteristics for PEALD and PLD ZnO TFTs before and after 10 Mrad(SiO_2) gamma ray irradiation.

3.3 Hardware and Software Setup for In-Situ Radiation Testing

For silicon MOSFETs electrical bias during irradiation can significantly modify radiation effects. Because the semiconductor charge collection volume for thin film transistors with a thin channel

(10-50 nm) is very small, it is expected that the effect of electrical bias during irradiation to be less. This theory, of course, needed to be confirmed with experimental evidence.

Over the course of the project two different measurement capabilities for in-situ temperature monitoring and DC-IV device characterization during irradiation for the ^{60}Co source and neutron reactor were developed. The first iteration of measurement capabilities used an HP 4141B and Keithley 708A switch matrix controlled by LabView. Figure 29 shows the sample fixture with integrated thermocouple used for in-situ radiation experiments and sample fixture loaded into ^{60}Co gamma cell. The drawback of this first-generation measurement setup was that only up to 3 devices could be measured during an experiment. While the first-generation of measurement capabilities was valuable to provide initial results, a second-generation of measurement capabilities expanding the number of DUTs was developed.

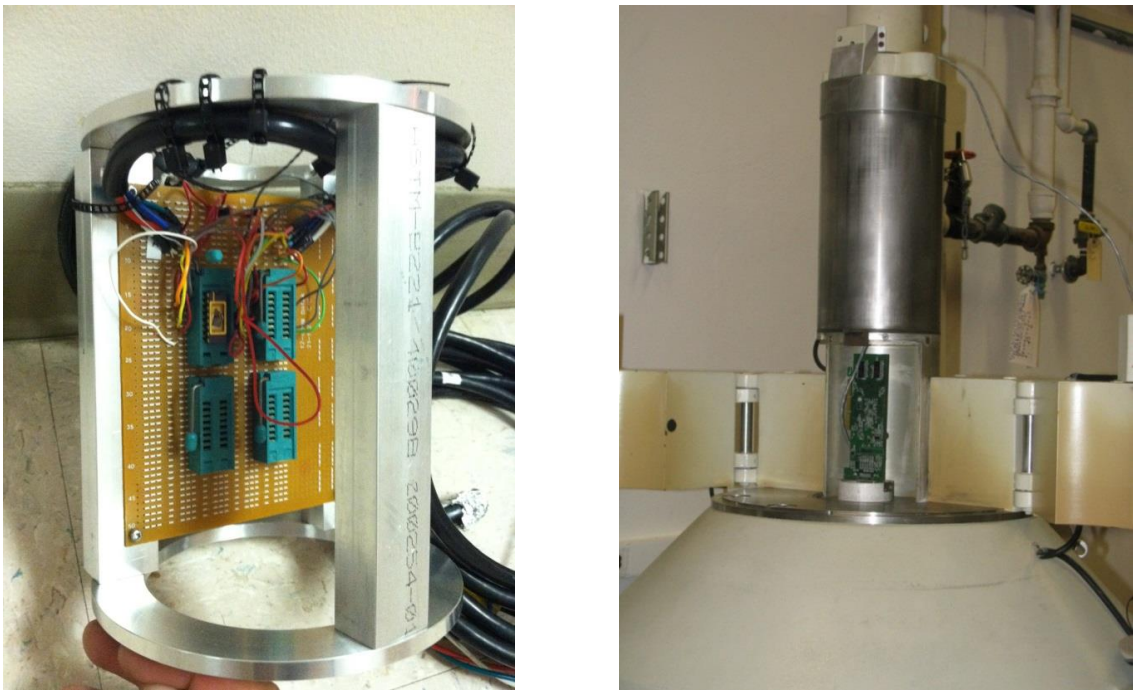


Figure 29. (left) In-situ bias sample fixture with integrated thermocouple. (right) Sample fixture loaded in ^{60}Co gamma cell.

The second-generation measurement setup is capable of supporting up to 12x12 ZnO TFT arrays. The previous test equipment used a HP4141B DC source/monitor and a Keithley 708A switching system, limiting characterization to only three devices per exposure. The second-generation of measurement equipment was upgraded to a Keithley 7075 multiplexer card, as shown in Figure 30. Adding the Keithley 7075 multiplexer card with eight 1x12 banks resulted in the ability to measure up to 12x12 TFT arrays during irradiation.

Figure 30. Measurement setup for in-situ measurement of ZnO TFTs modified for increased multiplexing capabilities.

Custom software was developed in Visual C++ primarily by Dr. Hitesh Basantani to support measurement of I_{DS}-V_{GS} sweeps and I_{DS}-time. Groups of devices can be biased in saturation while other groups of devices can be biased in the linear region all during the same exposure. Additionally, the sampling period was reduced from ~1800 seconds to ~140 seconds when compared with the original equipment and software. The timing diagrams for both the old and new configuration are shown in Figure 31. For the arrayed TFTs, I_{DS} versus V_{GS} is measured by sweeping a row with one column held at a given V_{DS}. During this sweep, the other rows are held at V_{GS} = -6 V (OFF state) and the other columns at I_{DS} = 0. Different drain biasing conditions can be selected for the different drain lines. The gate leakage current is also monitored on every

device. The software can be modified in almost real-time to customize bias conditions. The current software version is configured to measure a 4x4 array.

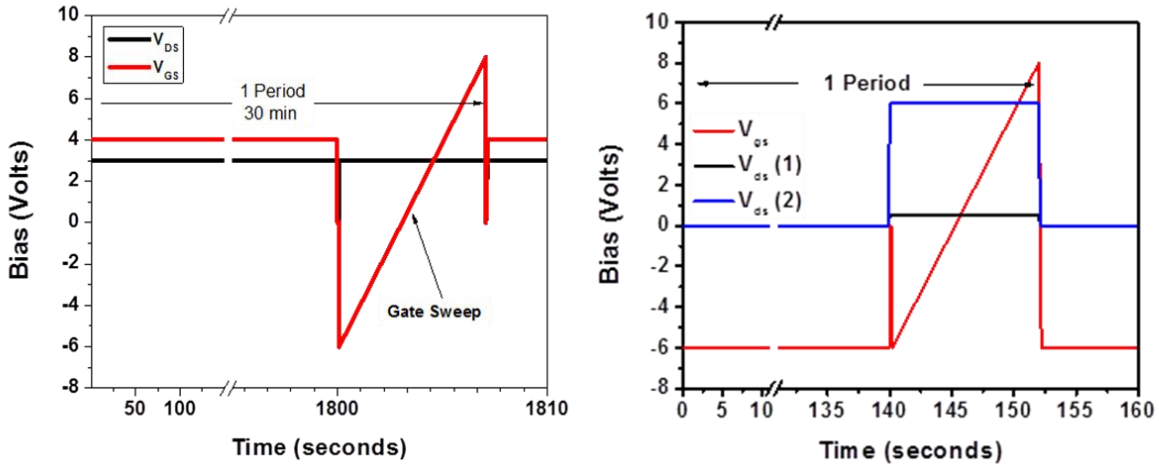


Figure 31. The original timing diagram shown on the left is from the prior period of performance and limited to a sampling rate of about 30 minutes. The timing diagram on the right depicts the system improvements with sampling rates of about 2 minutes and multiple drain bias configurations.

The custom hardware and software allowed the ability to generate statistically significant measurements of bias effects in irradiated devices. The new system offers increased measurement flexibility in terms of bias conditions and number of samples.

3.4 Electrically Biased and ^{60}Co Irradiated ZnO TFTs

For this work, 4x4 arrays of PEALD TFTs were fabricated and wired bonded in dual in-line packages. The fabrication details are identical as discussed in section 3.1.1. Figure 32 shows an optical micrograph and schematic of a 4x4 array.

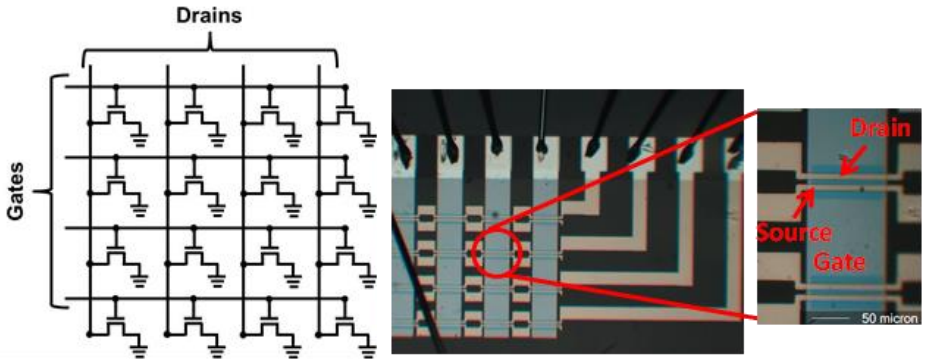


Figure 32. Circuit schematic and optical micrograph of the 4x4 array of PEALD ZnO TFTs used in electrical bias and radiation measurements.

For oxide TFTs, both electrical stress and radiation exposure can cause changes in TFT characteristics, so it is important to measure the effects of each. A control experiment is required to differentiate electrical stress effects on ZnO TFTs in the presence and absence of radiation. Figure 33 shows I_{DS} versus V_{GS} characteristics for V_{DS} = 6 V, for a PEALD ZnO TFT with dimensions W / L = 100 µm / 5 µm for a DC stress test for over 50 hours. The large off-current and off-current noise is an artifact of the long ribbon cables used for this measurement, necessary for measurements during irradiation. After 50 hours of electrical stress a V_{ON} and V_T shift of +0.5 and +0.2 V was found, respectively. The origin of this positive shift is not certain, but may be related to mobile charge movement in the Al_2O_3 dielectric or charge injection from the channel to the dielectric [73].

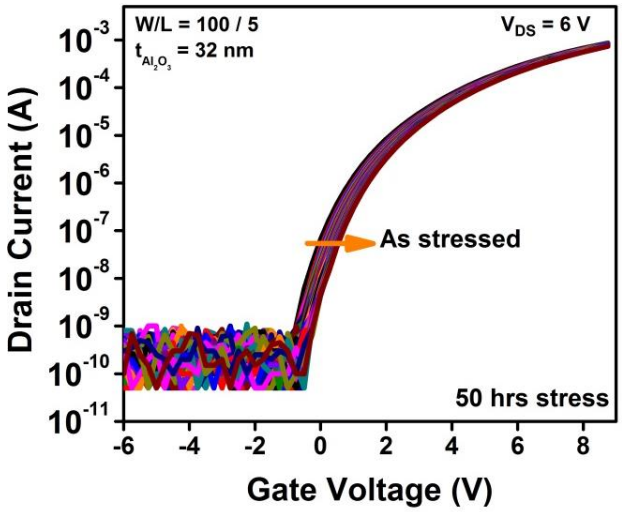


Figure 33. A group of I_D versus V_{GS} curves in saturation region (V_{DS} = 6) for a PEALD ZnO TFT stressed for 50 hours. A ΔV_{ON} of +0.5 V and a ΔV_T +0.2 V was observed.

Electrical measurements were made for devices biased during irradiation using the same timing arrangement used for the electrical stress only tests. Different PEALD ZnO TFTs were biased in the linear (V_{DS} = 0.5 V) and saturation regions (V_{DS} = 6 V) and measured under irradiation to a cumulative dose of 25 Mrad(SiO_2), equivalent to 50 hours in the irradiator used for this test. Figure 34 shows a representative I_{DS} versus V_{GS} for V_{DS} = 6 V characteristic for a device in the array before, during, and after irradiation. During irradiation the TFT low-current characteristics, including the apparent off-current and the subthreshold characteristics near V_T, are significantly perturbed. This is attributed to charge collection on the surface of the TFTs and unshielded wiring in the ionizing radiation environment, a detailed discussion of this artifact is explained in the following section.

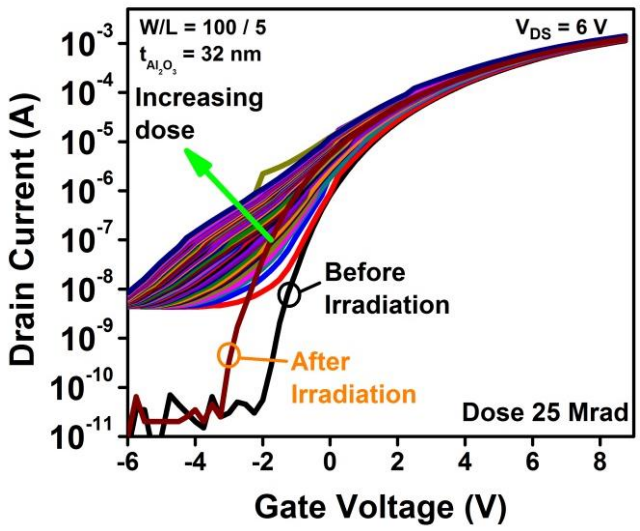


Figure 34. A group of I_D versus V_{GS} curves in saturation region (V_{DS} = 6 V) for a PEALD ZnO TFT electrically stressed and exposed to a cumulative dose of 25 Mrad(SiO_2), equivalent to 50 hours. After 25 Mrad(SiO_2) a ΔV_{ON} of -1.1 V and a ΔV_T +0.6 V was observed.

3.5 Measurement Artifacts during In-Situ Irradiation

During irradiation ions and electrons are created by interactions between gamma rays and the air in the irradiator [74, 75]. This charge is collected by the device test wiring, and leads to artifacts in the low current TFT characteristics. Measurements of device test wiring with bias, but with no TFT connected, show significant leakage current inside the ^{60}Co irradiator, though not as large as the measured TFT low current effects during irradiation. An additional contribution, to the subthreshold current, comes via charge collection at the back interface of the TFT during irradiation. Similar artifacts have been seen in irradiated fully-depleted Si SOI FETs and can even lead to an inverted back surface that can create a conducting path that is seen as additional current in the subthreshold region [68].

Unlike silicon MOSFETs, in bottom gate TFTs the gate electric field is not contained during all regions of device operation. For ZnO TFTs, when the device is biased to form an electron accumulation channel (the TFT on state) the gate electric field terminates on channel charge. However, when the TFT is biased in the off-state the gate charge may not be balanced by minority charge (holes). For this case the gate electric field extends through the device back interface and terminates on the device contacts or other nearby features. This fringing field can also attract mobile charge, present as ions and electrons in the irradiation environment. For the TFT biased with $V_{GS} < 0$ the TFT back interface is expected to attract positive ions. This positive charge layer, which will depend on details including the irradiation ambient and time, will act to shift the apparent turn-on voltage for the TFT. The charge at the TFT back interface is not stable and may be lost when the TFT gate is biased positive or compensated by additional adventitious charge in the irradiant ambient. The charge is only partially bound and even a positive gate voltage is sufficient to remove much of the charge.

To confirm that irradiation-induced charge at the TFT back interface plays a role in the low-current regime during irradiation test; devices with shielding added to avoid back interface charge accumulation were prepared. The conductive shield electrode is connected to ground and maintains the back surface potential at zero. Two sets of PEALD ZnO TFTs were prepared used with the previously described device structure in section 3.1.1. The first set of devices (structure shown in Figure 35 left) was used as a control group to be exposed to the same radiation dose and dose rate. The second set of devices had a ~3 μm thick layer of chemical vapor deposited poly(p-xylylene) (parylene) over them and silver paint was used to connect to ground and to provide simple shielding over the device area, as shown in Figure 35 (right). Test devices were

then exposed to ^{60}Co (0.01 Mrad(SiO_2) / hr) for 24 hours for a cumulative dose of ~240 krad(SiO_2). Representative group of I_{DS} versus V_{GS} for the control devices are shown in Figure 35 (left). The drain current below V_T rapidly increases only after few krad(SiO_2) cumulative dose like it was seen in Figure 34. On the other, the I_{DS} versus V_{GS} characteristics below V_T for the shielded devices (Figure 35 right) do not exhibit the increase in subthreshold current. When the sample is first introduced to the irradiator there is an increase in the apparent TFT off-state current, though much less than for unshielded devices. After a few minutes of irradiation the TFT off-state current is reduced further and remains constant for the remaining cumulative dose. The initial larger off-state current may be related to charge accumulation on the measurement cables. The steady-state off-state current in the irradiator is similar to the current measured for biased device test wiring with no TFT and is likely due to charge collection in the ionizing irradiator environment.

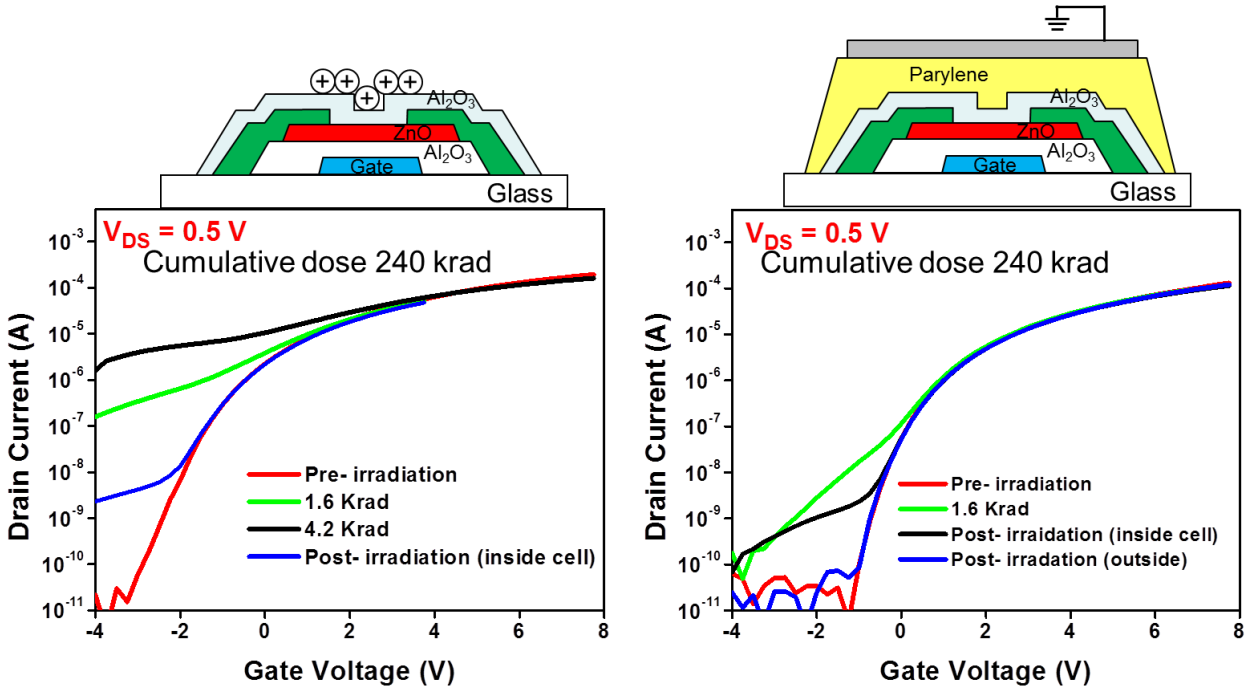


Figure 35. (left) Bottom gate PEALD ZnO TFT (same structure as used in previous experiments) and I_{DS} versus V_{GS} (V_{DS} = 0.5 V) showing a rapid increase in subthreshold current after only several krad dose. (right) The same TFT structure as used before but with an additional low-k dielectric and a conductive film over it connected to ground.I_D versus V_{GS} (V_{DS} = 0.5 V) for a PEALD ZnO TFT with the top surface shielded. Both structures were exposed to 240 krad(SiO_2). Anomalies in the low current region are reduced with proper shielding.

With the artifacts related to the ionizing irradiation environment suppresed, the effect of electrical bias on gamma-ray radiation-induced changes in ZnO TFTs is very small. As shown in Figure 34, PEALD ZnO TFTs biased as described and exposed to a cumulative dose of 25 Mrad(SiO_2), have a V_{ON} shift of -1.1 V and V_T shift of -0.6 V. The small difference in shifts between biased and unbiased devices with irradiation is likely caused by the effects of electrical stress noted above. 25 Mrad(SiO_2) dose required about 50 hours exposure in the irradiator used for this experiment. The control experiment of electrical stress with no irradiation resulted in V_{ON} and V_T shifts of 0.5 and 0.2 V, respectively, for 50 hours of the bias conditions used during irradiation. Subtracting the control electrical bias shift from the observed electrically biased

during irradiation shifts gives V_{ON} and V_T shifts of -1.6 and -0.8 V, respectively, close to the irradiation-induced shifts observed for unbiased devices.

These results are in strong contrast to experience on bulk Si where a "worst case bias" is often used to benchmark radiation effects in FETs because of bias-dependent degradation under irradiation [76, 77]. For those devices electrical bias can greatly increase radiation exposure related to device changes [77]. The difference may be simply related to the thin film transistor structure used for the ZnO devices. In these thin channel (typically 10-50 nm), bottom gate devices, there is no significant semiconductor volume for bias to influence charge collection from, and no buried oxide and underlying substrate for radiation-related charge generation and trapping. Thus, unbiased radiation testing provides a good estimate of "worst case bias" while avoiding bias-stress effects.

3.6 Wider Irradiation Dose Range

Figure 36 shows the shift in TFT threshold voltage, V_T, for ^{60}Co irradiation dose up to 100 Mrad(SiO_2). Figure 36 includes data for both biased and unbiased devices, but is uncorrected for the shifts related to electrical stress. Notably, the threshold voltage shift is not linear with dose rate, but slows with increasing dose. A simple exponential function provides a useful fit to device changes with irradiation, both with and without bias, but it is not yet connected to the underlying physics. As noted above, a short anneal at 200 °C removes most of the irradiation induced device changes and some reduction take place even at room temperature. V_T shift recovery post- 200 °C, 1 minute anneal is shown for devices exposed to 50 Mrad(SiO_2). It is

expected that self-annealing during irradiation also affect the results. The two irradiators operate at different nominal temperatures (~34 °C for the high dose rate irradiator, ~30 °C for the low dose rate irradiator).

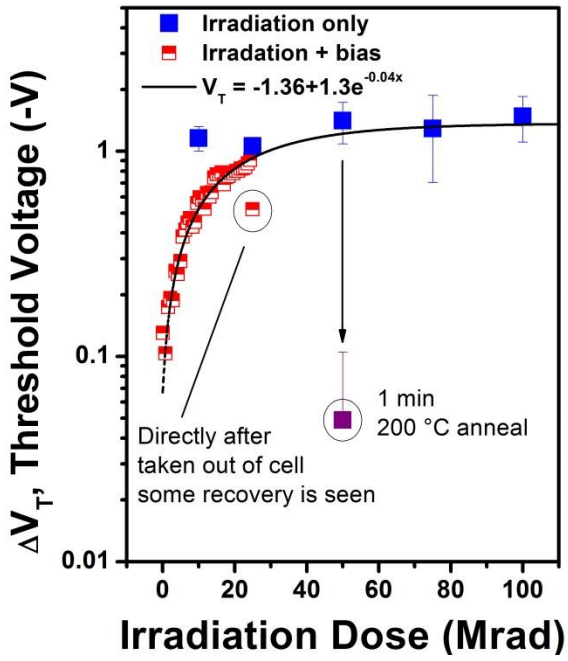


Figure 36. Threshold voltage as function of irradiation dose for irradiation only and irradiation with electrical bias for doses to 100 Mrad(SiO_2). A 1 minute anneal at 200 °C nearly removes the radiation-induced V_T shift.

Despite some scatter related to biased and unbiased devices and different dose rates and irradiation temperatures the data is quite consistent. This high cumulative dose of 100 Mrad(SiO_2) underlines the intrinsic radiation hardness of ZnO TFTs and the number of applications where they may be useful like space applications (although unlikely for high doses to be reached) but may be useful for extreme environments like in nuclear reactor monitoring, to name a few.

3.7 Physical Location of Radiation-Induced Changes in ZnO TFTs

In the previous section it has been shown that properly designed ZnO TFTs can withstand up to 100 Mrad(SiO_2) doses with a small radiation-induced negative V_T shift. This change in V_T indicates that while these ZnO devices are very radiation hard, some radiation-induce charge is accumulated within one of the materials or interfaces. In order to have a preliminary understanding of the physical location of the radiation-induced charge accumulated in the TFT structure, a systematic study of ionization-induced surface charge and passivation was carried out. To attempt to deconvolve the effects on each layer of the device structure, TFTs with various active layer and gate dielectric thicknesses were fabricated. This information was used to develop a model based on the experimental results. All devices were exposed to 5 Mrad (SiO_2) gamma-ray and were evaluated in terms of total induced charge on the stack ($\Delta Q = C \cdot \Delta V$).

This set of experiments used PEALD ZnO TFTs with a metal gate and Al_2O_3 gate dielectric because vast information is known about this material stack. Irradiation-induced effects were studied as a function of different passivation schemes, active layer thickness, and gate dielectric thickness. Figure 37 shows cross-sectional schematics of the different device permutations investigated.

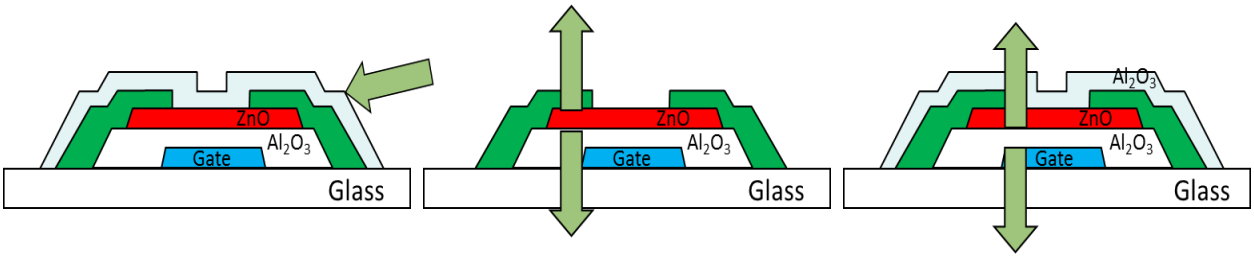


Figure 37. Multiple device permutations were studied for PEALD ZnO TFTs to understand which interface was affected the most by irradiation.

Three different passivation schemes were investigated: unpassivated, ALD-passivated, and tri-layer. While a passivation layer is typically added post- device processing to improve electrical stability, devices can function without a passivation layer as shown in Figure 38 (left). The baseline device stack, ALD-passivated, was also included to have a comparison to our previous work, Figure 38 (middle). Finally, a tri-layer structure was compared, Figure 38 (right). The tri-layer structure has the same material stack as the baseline device but the gate dielectric, active layer, and passivation are all grown in one step without breaking vacuum. This method prevents the channel region from being exposed to air and/or chemicals during fabrication, and giving enhanced electrical stability over post- processing ALD-passivated ZnO TFTs [46].

Figure 37 shows I_{DS} versus V_{GS} for ZnO TFTs with dimensions W / L = 200 µm / 20 µm using different passivation schemes. The V_T shift induced by 5 Mrad gamma-ray radiation is -0.14 ± 0.12 V for unpassivated devices, -1.43 ±0.10 V for ALD-passivated devices, and -0.59 ±0.08 V for tri-layer devices. This experiment suggests that passivation variations result in significant changes in charge from radiation exposure. While unpassivated PEALD ZnO TFTs offer limited electrical stability, they appear to be the most radiation-hard. Also, processing-related methods can have an effect on the amount of charge collected at the ZnO/passivation interface.

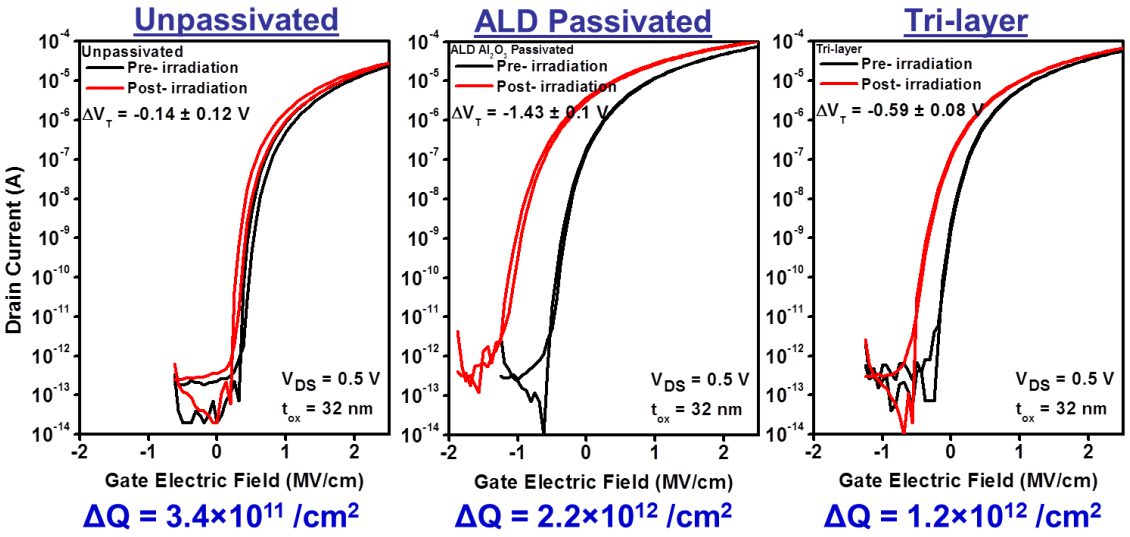


Figure 38. PEALD ZnO TFTs with different passivation schemes. Passivation variations result in significant changes in radiation-induced charge.

Next, irradiation-induced effects were studied as a function of ZnO film thickness variation. Three different thicknesses were chosen, 10 nm, 33 nm and 58 nm, over same thickness gate dielectric (32 nm) and no passivation. These PEALD-grown ZnO TFTs were not passivated because it has previously been shown a significant degradation in the subthreshold characteristics for ZnO active layer films >20 nm [43]. The hump induced by the Al_2O_3 passivation in the subthreshold region is associated with a conductive layer at the ZnO/passivation interface [43]. Figure 39 shows I_{DS} versus V_{GS} for ZnO TFTs with different active channel thicknesses. While there is a variation in the negative V_{ON} shift, by the devices between thin (10 nm) and the thicker (38-nm and 58-nm) active channels, the V_{ON} shift is significantly less than the change in V_{ON} in the passivation variation, pointing to semiconductor/passivation as the most radiation-sensitive interface.

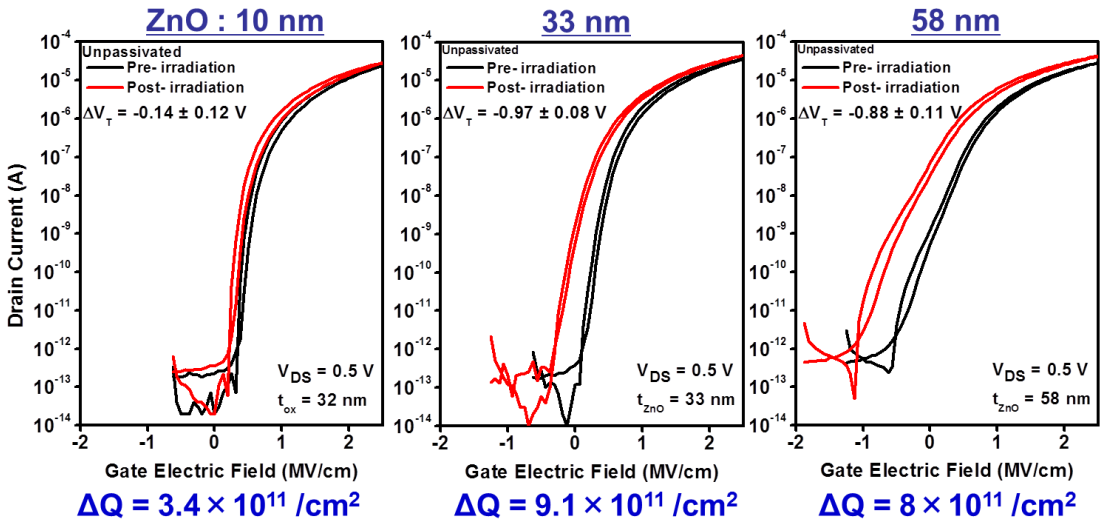


Figure 39. PEALD ZnO TFTs with active channel thicknesses and no passivation. ZnO film thickness variations result in some variation of radiation-induced charge after 5 Mrad (SiO_2).

Lastly, irradiation-induced effects as a function of gate dielectric thickness variation were examined. Three different gate dielectric thicknesses where chosen: 16 nm, 33 nm and 58 nm, with a fixed 10-nm thick ZnO film and same ALD passivation. Figure 40 shows I_{DS} versus V_{GS} for ZnO TFTs with different gate dielectric thicknesses. The variation in gate dielectric thickness had negligible effects on the radiation-induced charge collected in the device after 5 Mrad suggesting negligible trapping in the bulk of the Al_2O_3 gate dielectric up to the thicknesses grown here.

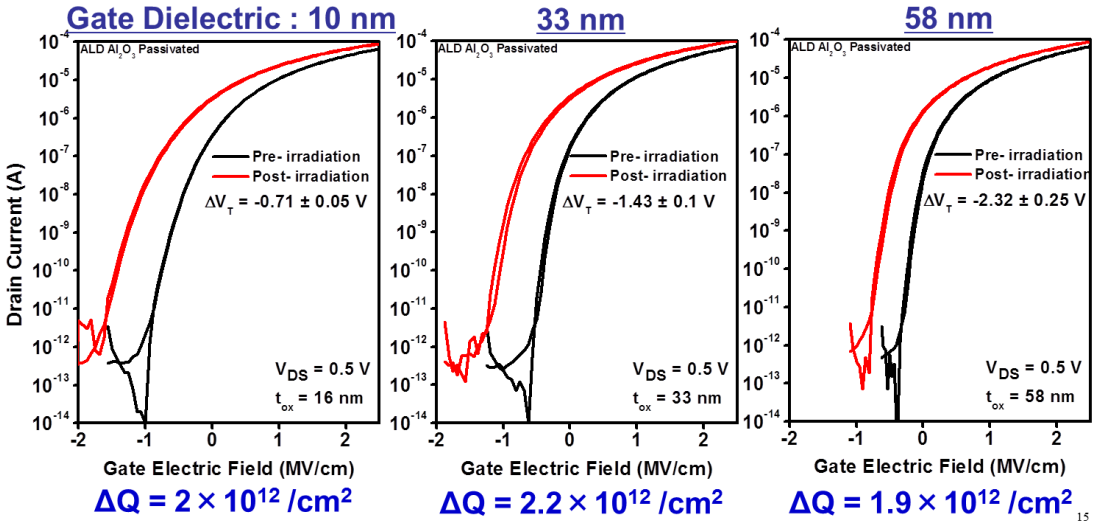


Figure 40. PEALD ZnO TFTs with varying gate dielectric thickness, fixed active channel thickness, and same ALD passivation. Gate dielectric thickness variations result in negligible change in charge for 5 Mrad (SiO_2) dose.

To summarize and compare the changes in the different device permutations shown above, V_{ON} and V_T shifts were plotted as function of total film thickness stack for a cumulative dose of 5 Mrad, as shown in Figure 41. The V_{ON} shift is larger than V_T shift, particularly for thicker films. If the radiation-induced charge was captured by the bulk of the materials, the V_{ON} shift would be similar to the V_T shift for all cases. The largest change observed for V_{ON} for pre-/post- irradiation was for passivated ZnO films indicative that the passivation/ZnO interface dominates the radiation-induced charge collection in the device.

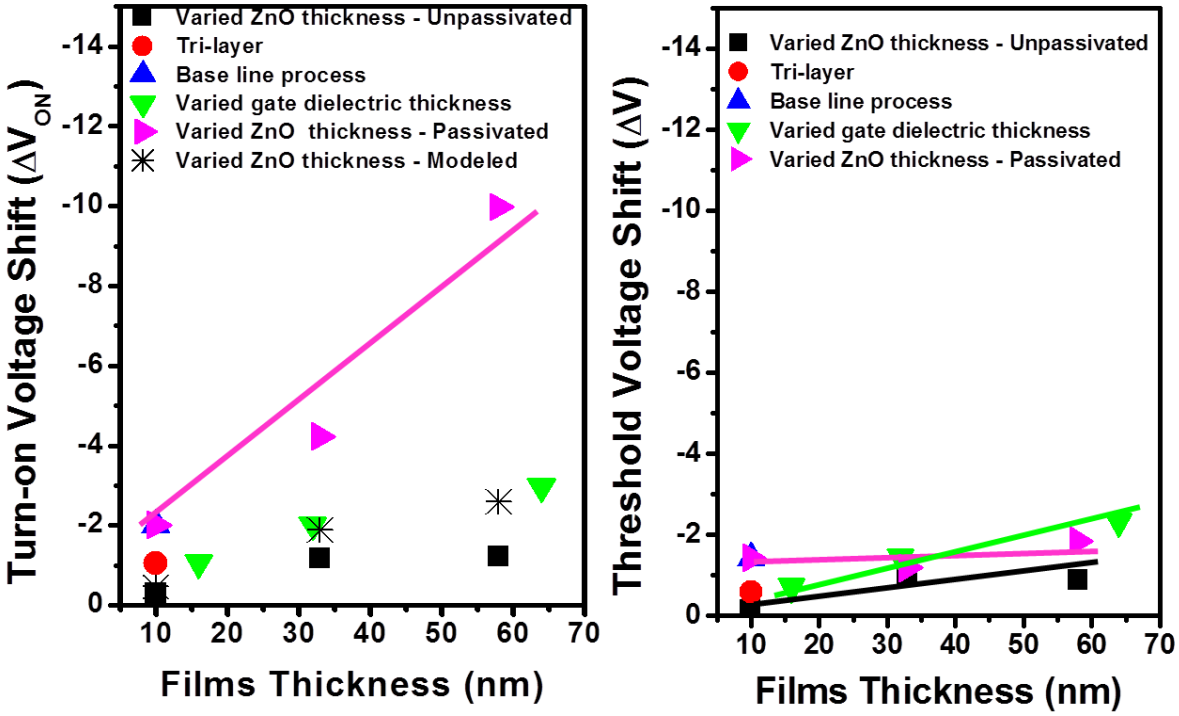


Figure 41. Summary of changes in V_{ON} (left) and V_T (right) as a function of process varients for TFTs exposed to 5 Mrad (SiO_2) of ^{60}Co gamma radiation

When all the device permutations are analyzed in terms of irradiation-induced ΔQ, as shown in Figure 42, results show two clear groups of charged-induced on TFTs with passivation and without passivation. The active layer thickness variation with a passivation shows greatest ΔQ with irradiation. These results are consistent with a model that charge accumulation is at the ZnO/passivation interface. This charge can be modeled as simple sheet charge at this interface.

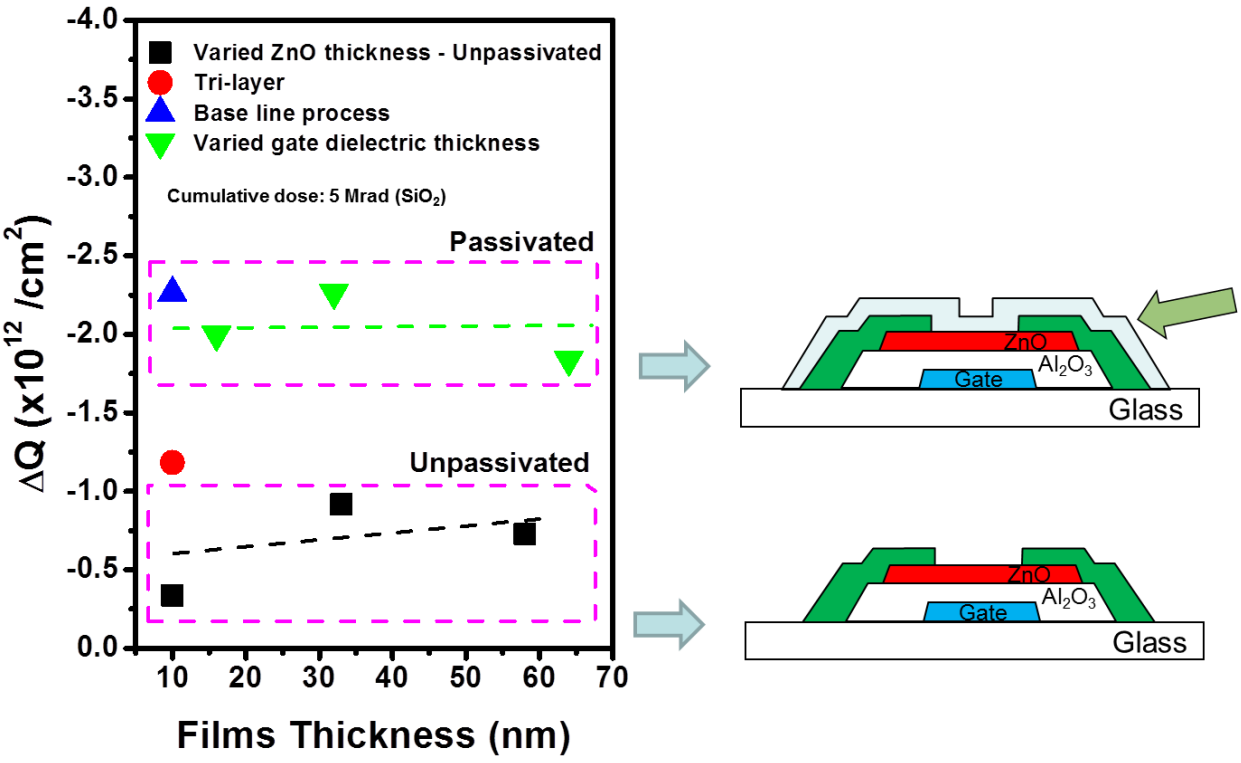


Figure 42. Summary of changes in charge showing passivation/ZnO interface is most critical.

In this chapter radiation tolerance of ZnO TFTs up to 100 Mrad (SiO_2) cumulative dose and recovery after a low-temperature, short duration anneal has been demonstrated. Moreover, the importance of properly shielding the bottom gate TFT structure can mitigate ionization-induced artifacts for measurements of TFT operation under irradiation. In this comprehensive study of ZnO TFTs, it was found that there is little or no difference for radiation exposure effects on ZnO TFTs with and without electrical bias. These results indicate that ZnO TFTs have improved radiation tolerance compared to other current TFT technologies [63, 64, 78]. ZnO TFTs using two different deposition techniques, PEALD and PLD, to grow the active ZnO layers, show the semiconductor is radiation-hard regardless of the deposition technique. While a deeper

understanding of the degradation and radiation-hard tolerance mechanism is needed, intrinsic radiation tolerance increases the likelihood that ZnO TFTs will find applications where robust radiation-hard TFTs are desired.

Chapter 4

4.1 Integration of ZnO Electronics with Complex Oxides Thin Films

The excellent conformality in thin films deposited by PEALD allows fabrication of electronics on almost any substrate. This is relevant to many thin film-based technologies, one example being solar-cells, which take advantage of this inherent feature of the ALD-based process to deposit conformal conductive thin films on high aspect ratio features [27]. In this chapter, monolithic integration of ZnO passive and active electronics with complex oxides is described. One of the advantages of on-chip integration of electronics with complex oxides is the reduction of parasitic capacitances, which can allow for higher sensitivity in sensors and actuator applications [79]. Integration of ZnO electronics on arbitrary substrates including with complex oxide thin films is possible because of the excellent conformality of the PEALD process and its low processing temperature (200 °C). This is in contrast with conventional CMOS processing technology where a Si wafer is required and the temperature budget can be well over 900 °C.

Complex oxides, such as barium strontium titanate ($Ba_{1-x}Sr_xTiO_3$ or BST) and lead zirconate titanate ($Pb(Zr,Ti)O_3$ or PZT) often require specific substrates or underlying thin films to be able to obtain the desired crystal orientation of the complex oxide thin films [80]. There have been efforts on integrating complex oxides with Si CMOS technology and while monolithic integration has been demonstrated, the process is complicated due to reactive cations sometimes present in complex oxides (e.g. Pb, Ba) as well as other concerns. Thus, integration of complex oxide and CMOS in industrial applications is still a challenge [81]. For a robust multi-level process integration of CMOS and oxides thin films, the processing temperature needs to be

reduced compared to the preceding temperatures used to avoid degradation of previous layers. However, the temperature budgets used in CMOS and thin film oxides is comparable making it difficult to integrate oxides following completion of the CMOS process. Specifically, oxides which require high crystallization temperatures (e.g. > 500 °C) could cause aluminum contacts to oxidize or dopant profiles to become mobile [82]. Moreover, a long-standing challenge integrating these two technologies is the thermal stability of noble metal electrodes, such as platinum, a widely adopted choice of metal for different complex oxide thin films. If metals such as Pt were to be integrated, contamination studies would first need to be performed. Also, there is a concern regarding cross contamination between CMOS processing and often Pb containing ferroelectric materials [81, 82]. Another issue is the passivation layer commonly used to passivated Si CMOS typically introduces hydrogen, which is known to degrade the piezoelectric properties of oxides [82]. Other efforts have focused on solder-bonding bulk ceramics on Si wafers [83].The majority of these bonding processing techniques use bulk ceramics and, after bonding, use thinning techniques to achieve thinner ceramic films. However, there still are several limitations like specific substrate preparation, materials, and processing parameters to make this a robust process [84-86]. Additionally, for applications which require large array control, this process is not preferred as it drastically increases the number of wires necessary. Therefore, developing a process to monolithically integrate electronics with thin film complex oxides would be beneficial. In this chapter, by taking advantage of the good conformality, low-temperature process, and substrate-agnostic of the PEALD ZnO thin film process, a straightforward and simple integration of thin film electronics with thin film complex oxides is demonstrated without perturbing the electrical or mechanical characteristics of the thin films.

4. 2 Integrating AZO Thin Films with BST Thin Films on Alumina Substrates

BST is an attractive dielectric material, that under certain compositions it shows paraelectric properties making it an attractive material for high-frequency tunable filters, preferred over conventional semiconductor materials, because of its low loss, fast tuning speed, and small physical dimensions [87-90]. ZnO thin films integrated with BST provided design flexibility of the tunable filters by enabling the design and fabrication of multiple RF filers in one substrate without space constraints to accommodate surface mounted resistors. The work described here was a collaborative work between Penn State and Dr. Peter Lam, Jon-Paul Maria, Dr. Vrinda Haridasan, and Dr. Michael Steer from NC State University to develop tunable microwave filters using BST as thin film varactors. Dr. Lam and Dr. Maria focus was in the BST material development. Dr. Haridasan and Dr. Steer were responsible for the filter design. The process development, including the monolithic integration of ZnO thin films with BST thin films was led by Penn State.

Section 4.1.1 will focus in the process integration development of Al-doped ZnO (AZO) thin film resistors in order to provide a more resistive trace and increase the isolation between the bias capacitor (DC circuitry) and the tunable capacitor (RF circuitry) in a two-pole filter. [91]. The process integration development in this work led to integration of active electronics with other electroceramic thin films as shown in the following sections.

4.2.1 Al-doped ZnO Thin Films Deposited by Atomic Layer Deposition (ALD)

Al-doped ZnO (AZO) is an attractive conductive material for applications where transparency might provide an advantage over opaque conductive films. AZO has similar electrical properties to indium-tin-oxide (ITO) making it attractive for solar cell applications. AZO is widely deposited by sputtering but other methods such as chemical vapor deposition (CVD) and ALD are also used depending on the application [92, 93]. The ALD technique is preferred for devices over large step heights due to the ability of ALD to provide continuous films over large aspect ratio features. In this section AZO deposition by ALD was investigated with the goal to integrate AZO resistors with BST thin films on polished polycrystalline alumina substrates. This work also led to the use of AZO thin films to make contacts in high aspect ratio solar cells [94]. The thin films were optimized for the lowest resistivity previous to being integrated with the BST-based tunable filters. Details of the integration of the optimized resistors with the filters are described below.

Multilayered laminates, alternating ZnO and Al_2O_3 cycles, have been demonstrated as a method to deposit AZO by ALD by several groups [93, 95]. Deposition details determined whether discrete layers or pseudo-homogenous alloys are formed. A typical method to deposit AZO by ALD is by controlling the ratio of Zn to Al cycles. In this work, ALD was chosen over PEALD because PEALD produces high resistivity films. The high resistivity in PEALD ZnO films is likely a product of the oxidizing species produced right over the substrate via the plasma. This results in fast kinetics, which may reduce the number of point defects, such as oxygen vacancies,

formed. In ZnO, the oxygen vacancies produce conducting electrons, which contribute to the reduced resistivity.

$$Zn_{Zn}^{X} + O_{O}^{X} \rightarrow Zn_{Zn}^{X} + V_{\ddot{O}} + \frac{1}{2}O_2(g) + 2e^{-}$$

AZO films grown by ALD have been demonstrated with resistivity as low as $3 \times 10^{-3}\ \Omega\cdot$ cm [95]. In this work, AZO films were grown by ALD using diethylzinc (DEZ) as the metal organic precursor for Zn and trimethyl aluminum (TMA) as the precursor for Al. H_2O was used as the oxidant. Films were deposited at 200 °C. ZnO films deposited at lower temperatures (<110 °C) yield high resistivity films with poor thermal stability [96]. Zn- and Al- cycles were alternated in in an ABAB (A = X number of ZnO cycles, B = Y number of Al_2O_3 cycles) sequence. The number of cycles in A and in B was investigated as function of thin-film resistivity. Figure 43 shows a simple schematic of the deposition sequence used to deposit AZO.

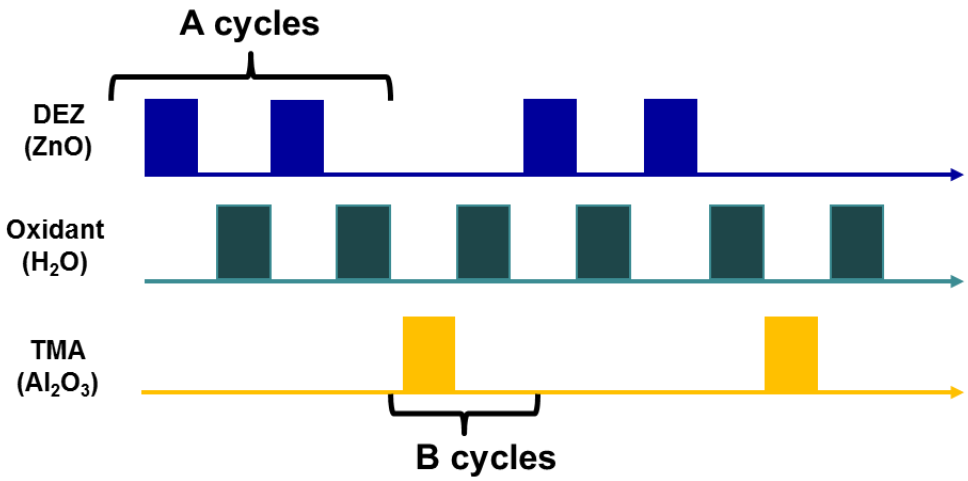


Figure 43. Schematic of the deposition sequence used to deposit Al-doped ZnO by ALD

A series with different ratios of ZnO cycles to Al_2O_3 cycles was carried out; the results of which are summarized in Figure 44 (left). It was found that a ratio of 25:1 (ZnO:Al_2O_3) cycles gave the lowest lateral resistivity of $2.5 \pm 0.5 \times 10^{-3}$ Ω· cm. This resistivity is comparable to reported literature values. ALD ZnO films with no Al content have a resistivity of 10^{-1} Ω· cm. Less than 1% variation in thickness was seen across 15 cm wafers. Following optimization of deposition cycles, the thickness dependence on resistivity of AZO was investigated. The A: B ratio was fixed to 25: 1 and this ratio of ZnO: Al_2O_3 cycles was repeated 4, 8 and 16 times. It was determined that films <20 nm show higher resistivity than >30 nm thick films, as shown in Figure 44 (right). The thickness dependence on resistivity, favoring the thicker films, may be because TMA preferentially etches Zn from the surface of the film causing stoichiometry defects [93]; while defect sites are needed for Al to occupy, as the film gets thinner the ZnO volume is very small, increasing the likelihood of forming Al_2O_3 layers instead of having Al sitting in an interstitial position in the film. Through-film resistivity measurements were also investigated and found to be 10^4 Ω· cm, about ~7 orders of magnitude higher than lateral resistivity. This anisotropy is likely because complete monolayers of Al_2O_3 are formed, providing a barrier for electrons. Lee D. J. *et al.* has shown high-angle annular dark-field cross-sectional TEM images of single Al_2O_3 layer formation in multilayered AZO laminates [95]. In this work, the lateral conductivity of the AZO thin films was of primary importance and thus the high through-resistivity was not an issue here.

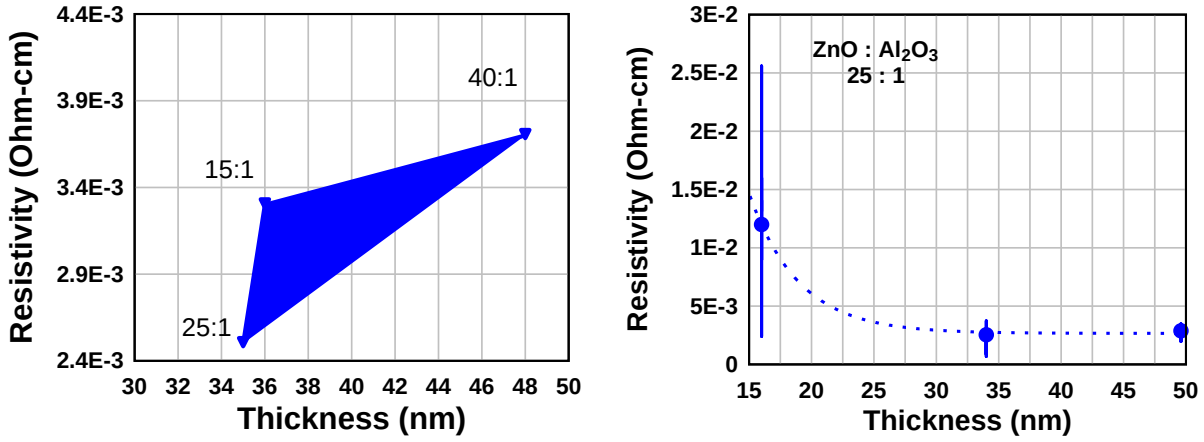


Figure 44. (left) Lateral resistivity of Al-doped ZnO thin films as a function of ZnO: Al_2O_3 cycles; (right) at a fixed 25:1 ratio of ZnO:Al_2O_3 cycles, resistivity as a function of thickness was examined. Films over > 30 nm show the lowest resistivity.

After the deposition process was optimized, AZO thin films were integrated into the fabrication process flow of the RF BST filters to provide isolation between the DC circuitry and RF circuity. The design constraint was to have a bias line resistance of ~10 kΩ. The nominal R_s for AZO is 1000 Ω/□ so by designing a resistor with a L/W ratio of 500 µm / 50 µm, the desired resistance was obtained. AZO resistors replaced the surface mounted resistors in the tunable filers. Prior to integrating AZO resistors, the yield of the tunable filters was uncertain and low because of user-error when placing the surface mounted resistors with conductive epoxy over the thin-film tunable filter. Integrated AZO thin-film resistors and fabrication optimization increased the yield of the microwave filters without degrading the BST characteristics. The filter modification is shown in Figure 45.

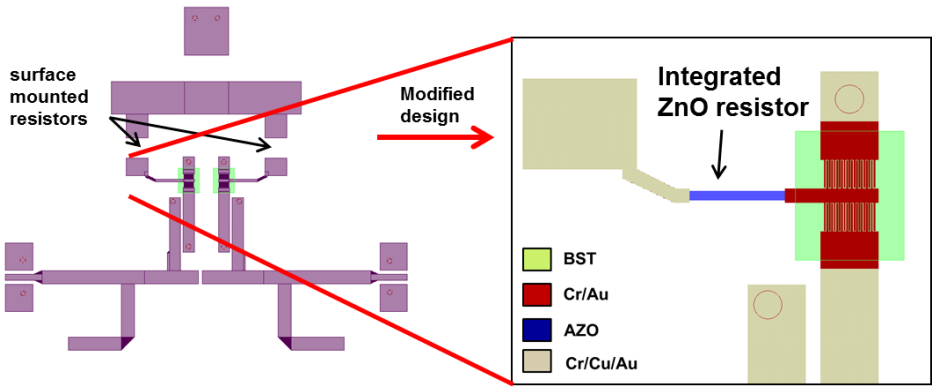


Figure 45. BST-based two-pole tunable X-band filter with integrated Al-doped ZnO resistor

This very simple integration of passive ZnO-based thin films on an alumina substrate led to further exploration of integrating active TFT devices with other complex oxide thin films. In the next section, the integration of ZnO TFTs with PZT thin films is demonstrated and examples of two applications are described.

4.3 Integrating ZnO Thin Film Transistors with PZT Thin Films

Piezoelectric thin films, such as $Pb(Zr,Ti)O_3$ (PZT) are useful in MEMS devices such as actuators, RF switches, and mechanical energy harvesters [97-99]. PZT specifically is of interest in these applications because of its high electro-mechanical response. For devices which require high piezoelectric and dielectric properties, compositions of PZT close to the nearly temperature independent morphotropic phase boundary are typically used: ($PbZr_{0.52}Ti_{0.48}O_3$) [100, 101]. The monolithic integration of ZnO electronics with PZT actuators was investigated to enable local control of the voltage provided to PZT elements. Direct integration of ZnO electronics may provide an advantage over the conventional bonding approaches of electronics with PZT actuators and the reliability issues related to the bonding process. The approach was to first develop a robust methodology to co-process ZnO and PZT thin films without degrading their

electrical and mechanical characteristics. With a robust process flow, the ZnO TFT-PZT capacitor integration is demonstrated. This is followed by application-oriented examples where this integration may provide a significant advantage. The work described here was collaboration with Dr. Susan Trolier-McKinstry and Margeaux Wallace from the Department of Materials Science and Engineering at Penn State. This work was led by Margeaux Wallace; however, the author was responsible for the ZnO electronics integration, circuit design, mask design, and TFT electrical characterization.

4.3.1 Addressing Many PZT Elements in a Row-Column Scheme

In applications where a large number of PZT elements need to be controlled independently, either for sensing or actuating, the use of active electronics to select a particular sensor or actuator can greatly reduce the number of connections to the outside world are needed. The basis of this approach is similar to the operation of an active matrix display. In Figure 46 a representation of $M \times N + 1$ elements is shown (the extra connection is for a common ground). Without any active electronics, the number of electrical connections needed to the elements would be $M \times N + 1$ connections. On other hand, if each one of these elements has a three terminal switch, namely a transistor, each element can be independently addressed and the number of connections is reduced to $M + N + 1$ connections. In the following section a process flow is described to integrate ZnO TFTs and PZT capacitors in order to address them in a row-column scheme.

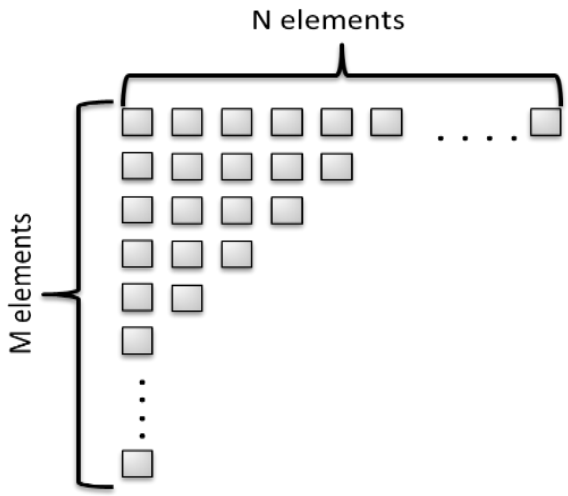


Figure 46. Connections to M×N + 1 elements can be reduced to M+N+1 connections by using a transistor connected to each element.

4.3.2 Co-Processing ZnO TFTs and PZT Capacitors

Both thin-film deposition and fabrication processes have been optimized independently by the respective research groups [30, 102]. A process flow to co-process ZnO TFTs and PZT capacitors is described in this section. After the process flow was optimized, electrical characteristics for discrete and integrated ZnO TFTs and PZT capacitors are shown.

In this work the PZT thin films were deposited using chemical solution deposition. PZT thin films can also be deposited by sputtering, as it will be shown in section 4.3.4. Margeaux Wallace did the PZT solution preparation, film depositions, PZT dry etching optimization, and electrical characterization of discrete PZT capacitors.

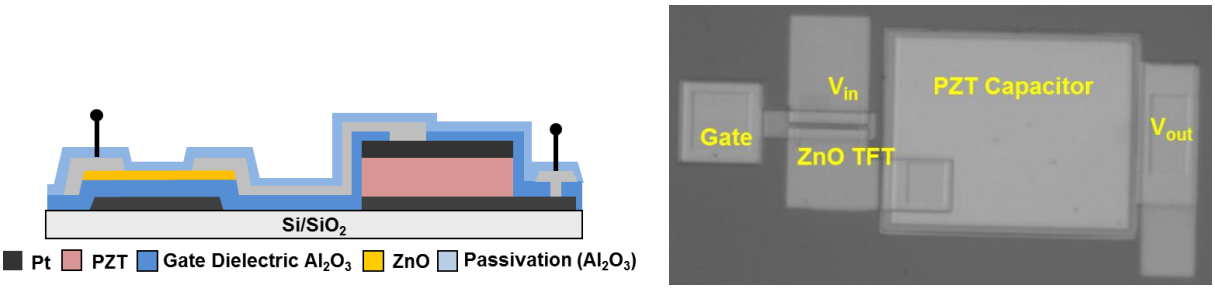


Figure 47. (left) Cross-sectional schematic of a ZnO TFT monolithically integrated with a PZT capacitor; (right) Top-view, optical micrograph of the integrated ZnO TFT-PZT capacitor.

ZnO TFTs were monolithically integrated with PZT capacitors. Figure 47 (left) shows a cross-sectional schematic of the ZnO TFT connected to a PZT capacitor. Prior to the ZnO TFT fabrication, PZT thin films were deposited using chemical solution deposition (sol-gel) on platinum coated, thermally oxidized silicon substrates. Details regarding the PZT solution preparation and film deposition are found elsewhere [103, 104]. A typical-coat, pyrolysis and crystallization sequence for PZT produces ~100 nm thick layer. This sequence is repeated until the desired thickness is achieved. Next, a thick layer (> 2 μm) of photoresist is spun-on and patterned to serve as a mask to dry etch discrete PZT capacitors. Following this, a separate mask was used to pattern bottom electrodes for each capacitor. At this time, the Pt gate for the TFTs was also defined via RIE. Optimization of dry etching conditions was carried out to minimize sidewall damage of the PZT and prevent failure of the PZT capacitors at electric fields lower than the norm. Figure 48 shows scanning electron microscope (SEM) images comparing PZT sidewalls after dry etching for unoptimized and optimized processes.

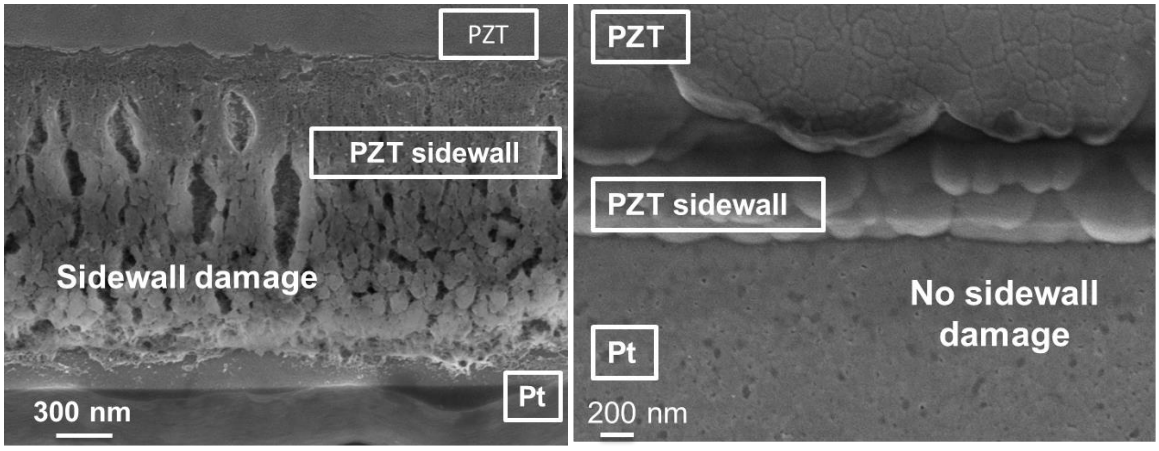


Figure 48. Side-view SEM images comparing PZT sidewall damage for (left) unoptimized and (right) optimized dry etching conditions.

After the Pt/PZT mesas were patterned, Pt was deposited as top contact for the PZT and patterned by lift-off. Al_2O_3 was used as gate dielectric and ZnO as active material, both deposited by PEALD. Here the PEALD process is preferred as transistor functionality has been demonstrated to be superior to ALD for both Al_2O_3 and ZnO thin films to improve with this deposition technique [30]. Following gate dielectric and semiconductor deposition, the ZnO was patterned using dilute HCl. Next, vias were opened to contact the TFT gate and the capacitor contacts using wet chemistry. In this process flow, the Al_2O_3 dielectric served as both gate dielectric and interlayer dielectric (ILD) to simplify the process. Because the Al_2O_3 was used as an ILD, the thickness was optimized to 90 nm to withstand the electric field across the metal-Al_2O_3-metal over the PZT sidewalls. Titanium was used for both TFT contacts and interconnects between TFTs and capacitors. Finally, an ALD-based Al_2O_3 passivation layer was deposited to stabilize the ZnO TFTs. The use of metal layers and dielectric for dual purposes allowed the process to be reduced to a 6-step lithographic process. This highlights the simplicity integrating

ZnO electronics with electroceramic thin films. Figure 47 (right) shows an optical micrograph of the completed ZnO TFT-PZT capacitor process.

Next, to show the electrical properties of the ZnO TFTs and the PZT capacitors were unperturbed, discrete devices were measured. Figure 49 (left) shows I_{DS} versus V_{GS} for a discrete ZnO TFT with 90 nm-thick Al_2O_3 gate dielectric and W/L = 200 µm / 20 µm, co-processed with PZT thin-film capacitors. ZnO TFTs show similar characteristics in terms of V_{ON}, V_T, subthreshold slope and field-effect mobility, as the TFTs fabricated on various other substrates shown throughout this work. Figure 49 (right) shows polarization as a function of electric field of PZT capacitors pre- and post- ZnO TFT fabrication, exhibiting no changes in the P-E characteristics. There were no measureable changes in dielectric constant, loss tangent, remanent polarization, coercive field in the PZT capacitors post- ZnO TFTs fabrication.

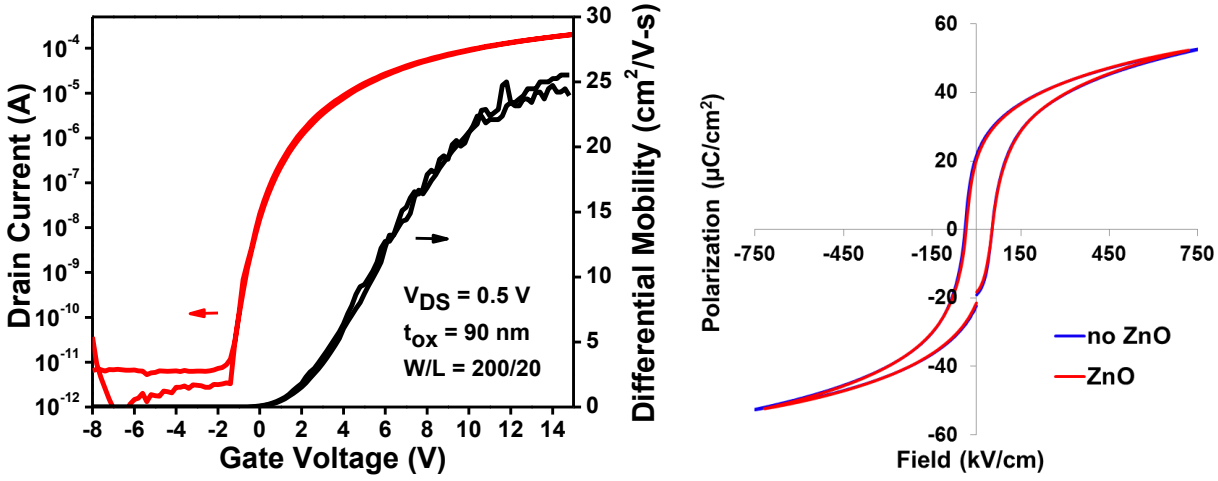


Figure 49. (left) Linear region (V_{DS} = 0.5 V) I_{DS} versus V_{GS} of a discrete ZnO TFT with W/L = 200/20 µm co-fabricated with PZT capacitors; (right) polarization as a function of applied field (P-E) for PZT capacitors pre- and post- ZnO TFT fabrication show nearly identical characteristics.

After the discrete electrical characteristics of each component were confirmed to not degrade during co-processing of the devices, a TFT connected to a PZT capacitor was tested. A good

switch for a capacitor must have low-leakage in the off-current state to not interfere with the discharge time constant of the capacitor. Measurement of the off-current in ZnO TFTs (particularly for relatively big channel widths (>200 μm)) is limited by the parameter analyzer detection limit (~10^{-13}A) and the cabling used. A detailed study of the off-current in oxide-based TFT (IGZO semiconductor) with a channel width of 100,000 μm estimated the off-state current to be as small as 50×10^{-24} A/μm (at 85 °C) [105]. The extremely low off-current typically seen in ZnO-based devices is because of the wide bandgap in oxide semiconductors. Therefore, it is expected that the ZnO TFT switch will not interfere with the discharge time of the PZT capacitor. Using a ZnO TFT (W/L = 150/5) connected to a PZT capacitor (~3 nF), as shown in Figure 50 (left), a voltage (V_{DS} =10 V) was supplied to the capacitor when the gate voltage was pulsed V_{GS} = ±10 V (+10 V to turn the TFT on, -10 V to turn it off). The capacitor's voltage was monitored as a function of time. Figure 50 (right) shows the capacitor voltage as a function of time as it is charged through the TFT and discharged. A charging time constant (TFT ON-state) of < 3 msecs and a discharge time constant (TFT OFF-state) of ~70 sec were found. Since the TFT off-state current is expected to be very low, as discussed above, the discharge time constant is likely dominated by the PZT capacitor self-discharge. The long discharge time constant provides flexibility on the refresh rate use in an array of PZT sensors or actuators, potentially minimizing the power consumption of a system.

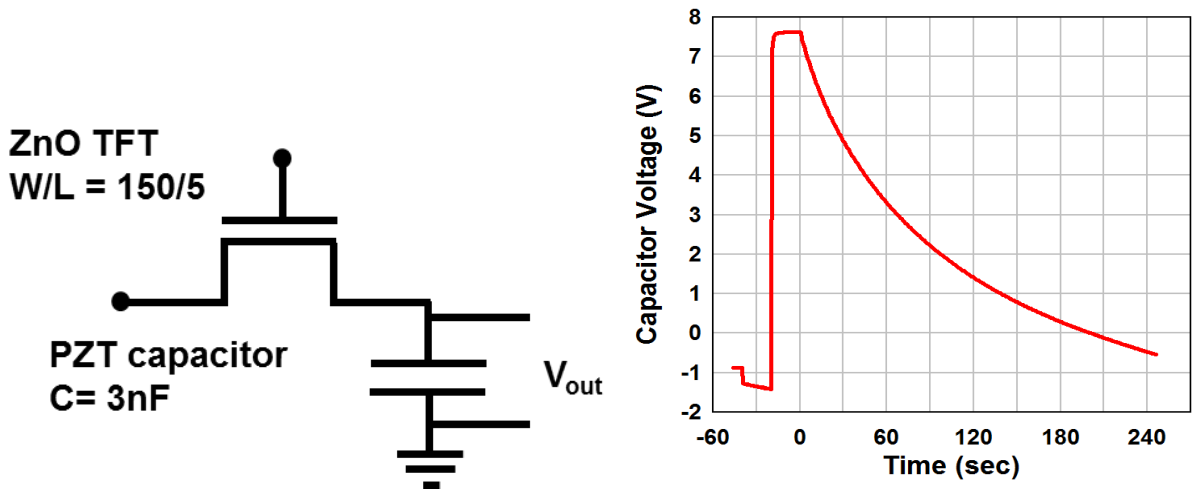


Figure 50. (left) Schematic of ZnO TFT with a W/L ratio of 150/50 connected to a 3 nF PZT thin film capacitor; (right) The capacitor's voltage as a function of time after applying voltage through the ZnO TFT. A charging and discharging time constant of ~ 3 msecs and 70 secs was found, respectively.

4.3.3 Integration of ZnO Ring Oscillators to Actuate PZT Cantilevers

The next logical step to demonstrate the possible advantages integrating ZnO electronics with PZT thin films is to show integrated ZnO electronics with some functionality beyond a switch. An array of PZT cantilevers with ZnO ring oscillators was designed and fabricated as a demonstration. The PZT cantilevers, designed by Margeaux Wallace, were designed to operate at low frequencies (~50 kHz) and to be able to easily detect deflection with a CCD camera.

4.3.3.1 ZnO Ring Oscillator Circuit Simulation, Design and Layout

AIM-spice compact model software was used to simulate discrete ZnO TFTs. The model level 15, developed for amorphous silicon TFTs, was modified based on experimental I-V characteristics. Figure 51 shows a comparison of the I_{DS} versus V_{GS} for experimental and

simulated ZnO TFTs. The drain current in the simulated TFT, particularly above threshold, where the devices will operate in the ring oscillator, matches well with the experimental data.

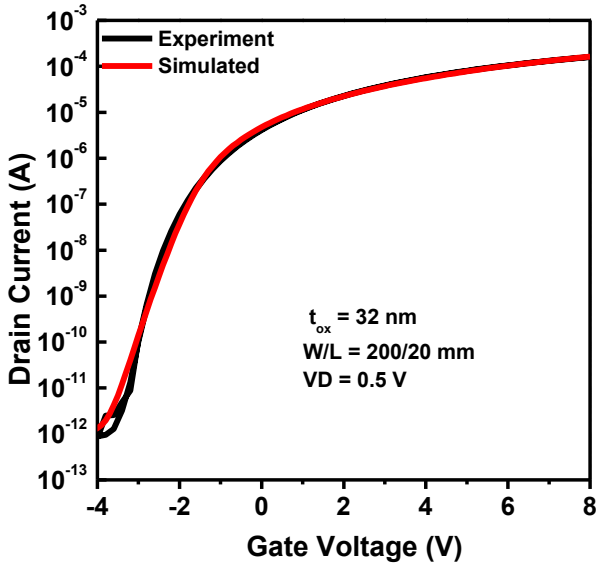


Figure 51. Linear region (VDS = 0. 5) I_{DS} versus V_{GS} comparison of experimental and AIMSpice simulated ZnO TFT.

PEALD ZnO ring oscillators have been demonstrated to operate up to 3.5 MHz at a supply voltage of 17 V [46]. For this application, the ring oscillators were designed to operate at a low frequency range to match the PZT cantilever design. A saturated-load inverter with a drive TFT W / L = 5 µm / 5 µm and a load TFT W/L = 5 µm / 60 µm (β_{ratio} ~ 12) and source/drain-to-gate overlap of 4 µm was simulated and designed as building block for the ring oscillator. Figure 52 (left) shows a circuit schematic of the saturate-load inverter and Figure 52 (right) the simulated logic transition curves for various supply voltages.

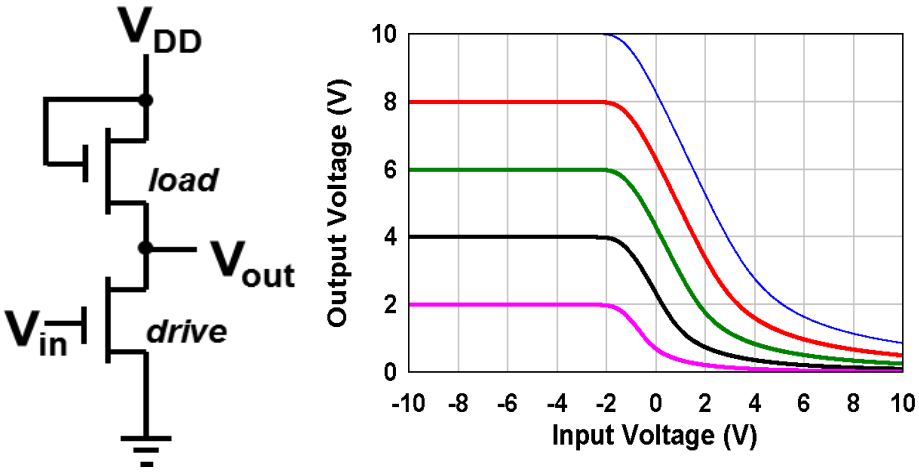


Figure 52. (left) A circuit schematic for a saturated-load inverter. The simulated ZnO inverter has a β_{ratio} ~ 12; (right) logic transition curves at various supply voltages.

While a saturated-load ring oscillator can be tuned by varying the supplying voltage ($f \propto V^2$) a lower limit in operating voltage exists ($V_{DD} = V_T$). Therefore, in order to achieve the desired low frequency operation to match the cantilevers resonance frequency, capacitors were added to the 7-stage ring oscillator design. Figure 53 (left) shows the schematic of a 7-stage ring oscillator with a capacitor on every stage. Simulated operating frequency and delay per stage as a function of supplying voltage is shown in Figure 53 (right). The desired ~50 kHz resonating frequency was achieved using 20 pF capacitors per stage. Other approaches may include increasing C_{GS} and C_{GD} and increasing the number of stages in the ring oscillator because everything else being equal, frequency $\propto$ 1/N where N is the number of stages.

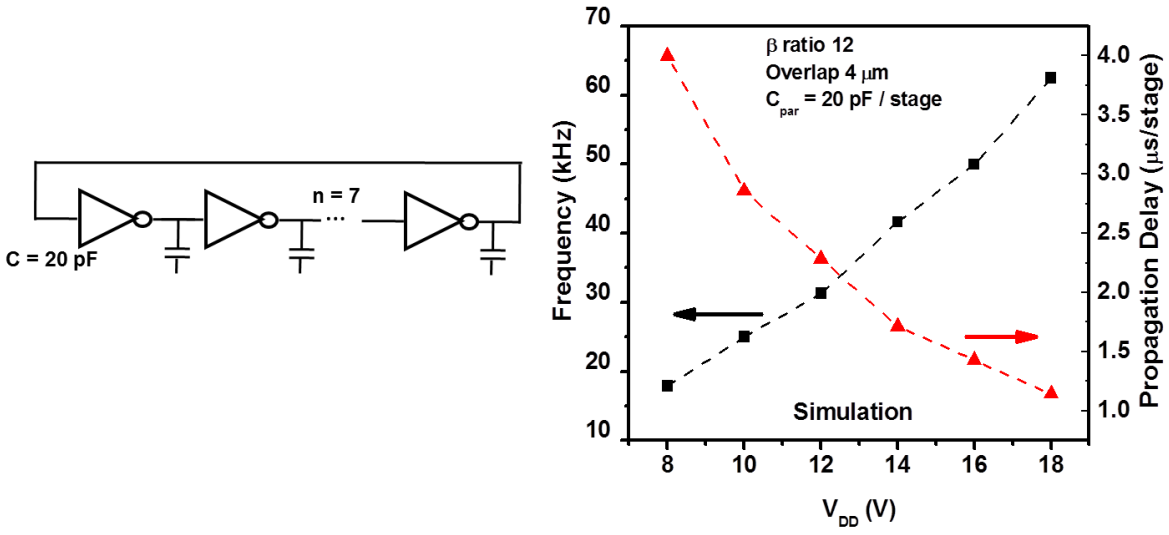


Figure 53. (left) Circuit schematic of a simulated 7-stage ring oscillator with a capacitor on each stage to match the resonating frequency of the PZT cantilevers; (right) frequency as a function of supply voltage for the simulated ring oscillator.

A 3x3 array with each array element consisting of a 7-stage ring oscillator, with the geometry parameters used in the compact model, integrated directly on top of the cantilevers was designed. Figure 54 shows the layout design of the 3x3 array with a select TFT (W/L = 200 μm /16 μm) per cantilever to be able to address the array in a row-column scheme.

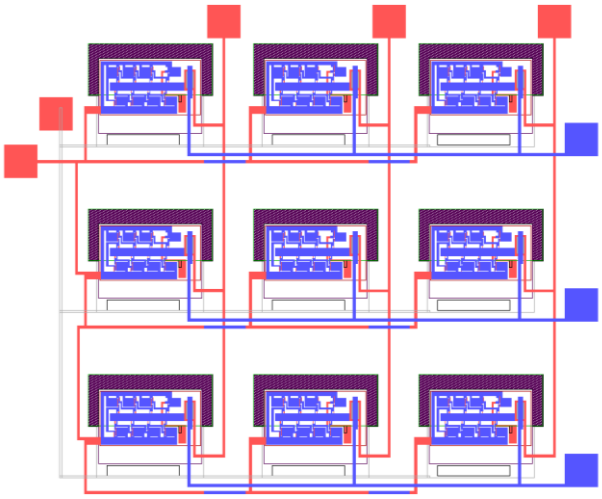


Figure 54. Layout schematic of a 3×3 array of PZT cantilevers with ZnO ring-oscillators on top each cantilever.

The fabrication process is similar to the process flow described in section 4.3.2. In the previous section, it was demonstrated that it was possible to have ZnO electronics alongside PZT thin films. In this work, ZnO electronics right on top of the PZT cantilever is demonstrated. Photo-patternable benzocyclobutene (BCB), a commonly used interlayer dielectric (ILD), was used to electrically separate the ZnO electronics and the PZT cantilevers. The BCB was spin-coated, patterned for via connections to the cantilever, and cured at 225 °C in an inert gas. Additionally, to increase adhesion of the TFT gate to the BCB, Ti was chosen as the gate metal and deposited and patterned via sputtering and lift off. The rest of the ZnO circuit fabrication is the same as the process described in section 4.3.2. To release the cantilevers, the Bosch process was used in a deep reactive ion etching (DRIE) tool. The Bosch process provides nearly isotropic plasma etch. The gas chemistries used were an alternation of SF_6 and CF_4. Figure 55 (left) shows a cross-sectional schematic of a released PZT cantilever integrated with ZnO electronics. Figure 55 (right) shows an optical micrograph of a 7-stage ring oscillator on top of a PZT cantilever before release. Using a CCD camera, the actuation of the PZT cantilevers was monitored. The PZT cantilevers were actuated by applying a DC voltage to the ZnO electronics resulting in an oscillating voltage input to the PZT cantilevers. Figure 56 shows two different video frames showing the deflection of a PZT cantilever. Because it is somewhat difficult to see the deflection in the frames, Figure 56 has red boxes to highlight the change in contrast in the frames.

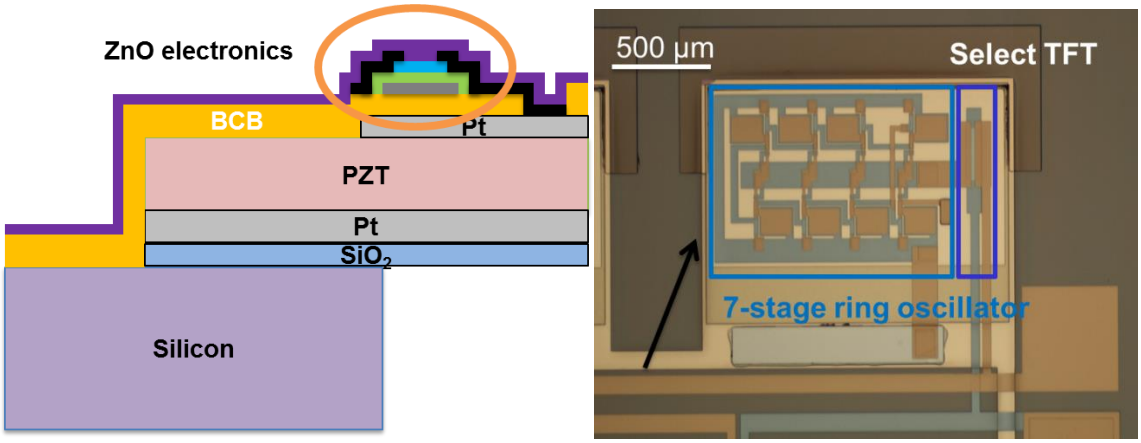


Figure 55. (left) Cross-sectional schematic of PZT cantilevers on a Si substrates with ZnO electronics fabricated right on top of the cantilever. (right) Top-view optical micrograph of a 7-stage ring-oscillator with a select TFT in a 3x3 elements array.

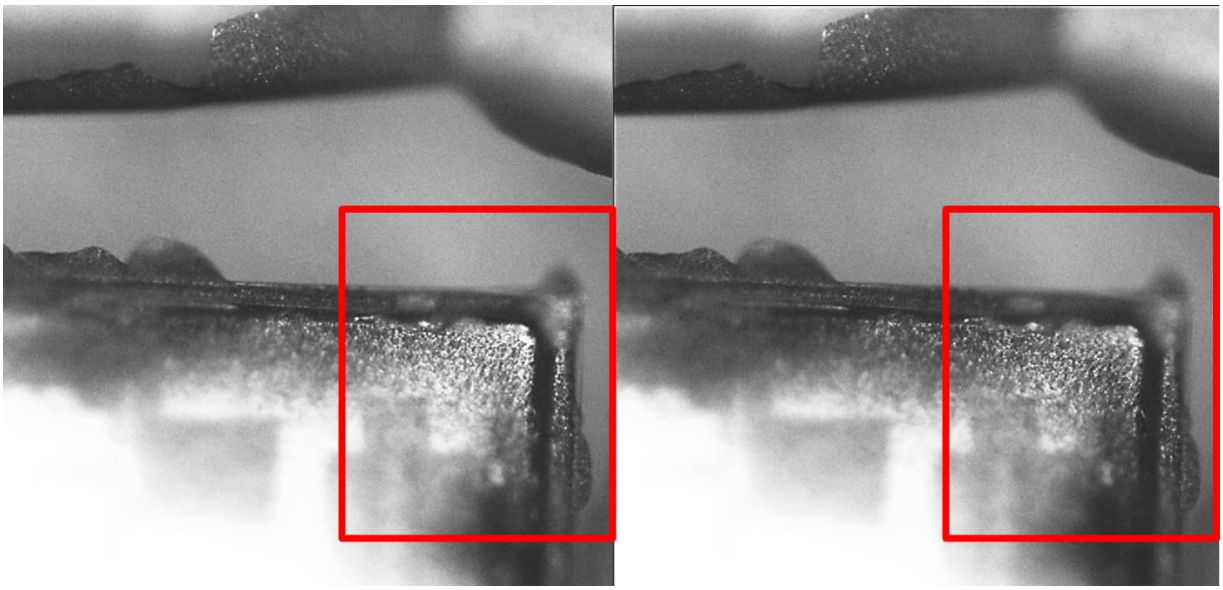


Figure 56. Representative video frames of the deflection of a PZT cantilever integrated with the ZnO electronics.

4.4 Integrated ZnO-PZT Thin Films for Adaptive Optics X-ray Telescopes

Adaptive optics are used to reduce the effect of wavefront distortions in various optical systems. The technology is used to correct deformations of an incoming wavefront by measuring the distortions in the wavefront and adjusting (deforming) the mirror to account for the distortions. Figure 57 shows a schematic of a deformable mirror used to correct wavefront aberrations. Some examples of application areas for this technique are in astronomical telescopes, microscopy, and ocular wavefront sensing [106-109]. This technique is needed in optical systems where a single focal distance may not exist because of the lens thickness or fabrication imperfections.

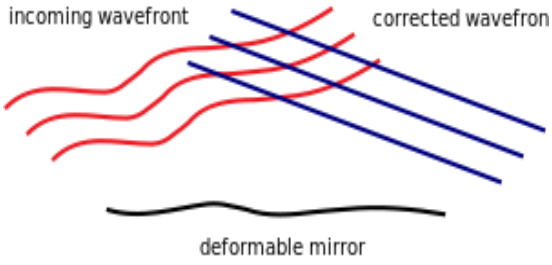


Figure 57. Schematic of adaptive optics used to correct aberrations of an incoming wavefront. "Deformable mirror correction" Licensed under CC BY-SA 3.0 via Wikimedia Commons

The work described hereafter focuses on the use of adaptive optics for astronomical telescopes. In x-ray telescopes, the maximum amount of light emitted from the source (i.e. star, nebula) needs to be collected by the detectors in order to increase the image resolution. Because the incoming light is not collimated a segmented mirror is needed to correct for aberrations and direct the maximum amount of light to the detector. By employing adaptive optics in x-ray telescopes wavefront aberrations can be minimized.

Current state of the art X-ray telescope Chandra observatory has helped revolutionize the understanding of the universe due to its excellent 0.5 arcsecond angular resolution. Figure 58 shows a comparison of X-ray imaging of the Crab Nebula using the previous X-ray telescope, ROSAT, and by Chandra. The high spatial resolution has allowed astrophysicists to better understand the universe.

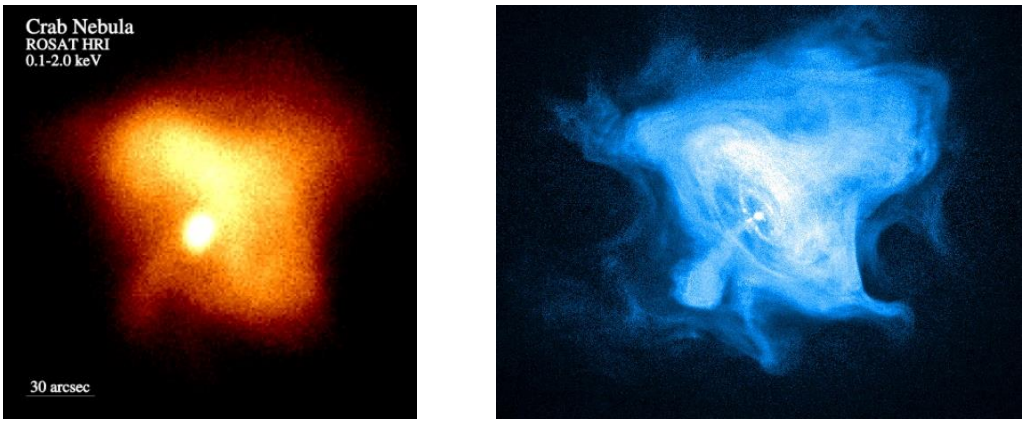


Figure 58. X-ray images of the Crab Nebula from (left) ROSAT and (right) Chandra. (ROSAT Credit: S.L. Snowden, NASA/GSFC. Chandra Credit: NASA/CXC/SAO)

While Chandra Observatory has produced superb images due its excellent angular resolution, the collecting area of the mirror assembly is relatively small (~0.08 m^2 at 1 keV) [106]. The relatively small collecting area was mainly limited by the weight of the optics (~1500 kg) with a total mass of ~4790 kg [110, 111]. For the next generation X-ray telescope mission the design parameters require equivalent angular resolution as Chandra (0.5 arcsec) while increasing (~ 30 times) the effective area per unit mass without substantially increasing the cost. This puts a big premium on the weight of the optics. One proposed solution is to use thin glass that can be deformed by using a piezoelectric thin film on the backside to produce the correct mirror shape for the high spatial resolution needed over a large collective area.

The square meter arc second resolution X-ray telescope (SMART-X) mission is a development effort to provide a potential next-generation astronomical telescope. The SMART-X mission aims to deliver a 0.5 arcsec resolution with an estimated collective area of 2.4 m^2 at 1 keV [106] while keeping the total estimated mass around 2900 kg (with the mirror assembly mass about 1100 kg) [111]. In collaboration with the Smithsonian Astrophysical Observatory and Penn State University, a scalable adaptive optics technology is being developed using pixelated PZT piezoelectric thin films on the back of the mirror to provide the strain needed to deform the mirror and correct for wavefront aberrations. Figure 59 shows a cross-sectional schematic of a glass substrate (mirror) with a reflective coat (typically Cr/Ir) on the front. The back of the glass substrate has a common Pt/Ti metal electrode, PZT thin film, and segmented top Pt electrodes to allow independent address of areas of the mirror. By applying a voltage across the PZT cell, a strain parallel to the mirror surface is produced causing a localized deflection.

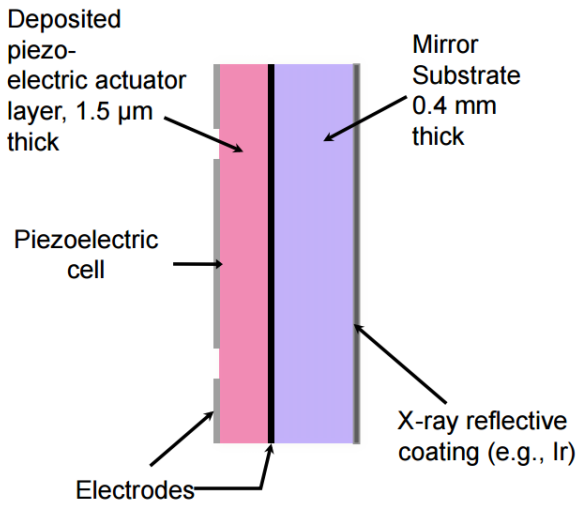


Figure 59. A cross-sectional schematic of mirror with PZT piezoelectric cells to correct for incoming wavefront aberrations. Photo taken from "Integrated Control Electronics for Adjustable X-ray Optics" S. Trolier-McKinstry. Early State Technology Workshop, Astrophysics and Heliophysics.

Cotroneo V. *et al.* has demonstrated controlled deflection of a 0.4 mm thick flat glass mirror by using a 1.6 um thick PZT thin film deposited by RF sputtering [112]. Figure 60 (left) shows a schematic of 33 PZT elements with one row of 6 elements activated [113]. Figure 60 (right) shows the influence function (the difference in substrate shape after cell activation) as a function of position for PZT cells driven at 10 V [113]. The experimental and simulated results agree well. While this demonstration is a key proof-of-concept that PZT thin films can be used to deform thin glass, the scaling of the system remains to be demonstrated. In order to achieve the collective area requirements of SMART-X, an estimated of 800 mirror panels with 400-800 PZT elements per each panel are needed [114]. Without using any switching/addressing scheme the number of connections can quickly become cumbersome and impractical. In the previous sections, integration of ZnO TFTs with PZT thin films has been demonstrated with excellent discharge time constants making ZnO TFT technology a strong candidate to use for PZT pixel-level control in a row-column addressing scheme helping reduce the number of connections to the PZT pixels from M × N to M + N+1.

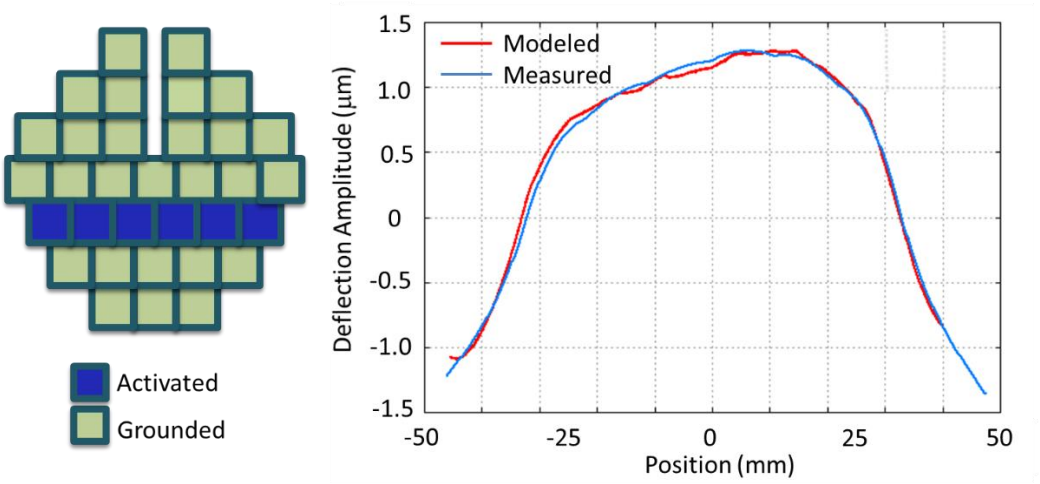


Figure 60. (left) 33 PZT elements with separate connections. A voltage was applied to 6 actuators in a row. (right) Comparison of the experimental and modeled influence functions for 6 PZT actuators. Figures taken from reference [113].

4.4.1 Mask Design of ZnO TFTs Controlling PZT Actuators for Adaptive Optics

To integrate PZT actuators with ZnO TFTs for adaptive optics, a mask layout was designed. Using the process flow described in section 4.3.2 and 4.3.3, a mask layout for a 5 x 5 array of 1 cm^2 PZT elements for a 10 cm substrate was implemented. Figure 61 shows the layout design. The PZT elements are individually controlled through ZnO TFTs with W/L = 200 µm / 5 µm dimensions. For the array, the scan and data line connections were designed to be compatible with off-the-shelf ribbon cables with 250 µm lines and 250 µm spacing. The connections to the array were made using anisotropic conductive film (ACF). Preliminary finite-element model has shown that ACF bond causes very minimal distortion on the glass for the dimensions of the connections (250 µm). To enable testing flexibility, discrete connections were also fabricated to allow single element addressing of each PZT element, bypassing the TFT array. The contacts connecting the PZT elements to the ZnO TFTs were designed to be relatively large to

accommodate future experiments of bonding ZnO electronics on a flexible substrate to the PZT array on a curved glass substrate. More details of this methodology are explained in a later section. Various test structures including process control monitors (PCM), discrete ZnO TFTs, and single element and 1D arrays of PZT capacitors were also included in the mask layout.

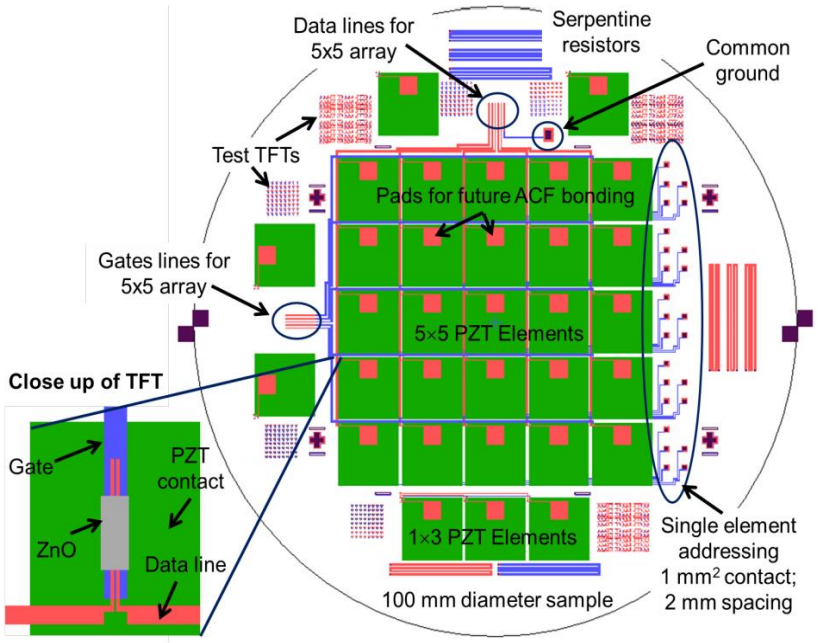


Figure 61. A mask design for a 5×5 array of PZT elements with ZnO TFTs integrated to address the array in a row-column scheme.

Next, fabrication of the PZT actuators and control ZnO TFTs on a 100 mm glass substrate was completed. Discrete ZnO TFT characteristics were measured. Figure 62 (left) shows the I_{DS} versus V_{GS} and (left) the I_{DS} versus V_{DS} for V_{GS} = 0-12 V with a 2 V/step characteristics of a discrete ZnO TFT with W/L = 200 µm / 20 µm fabricated on the same substrate. The device characteristics are nearly identical to TFT characteristics measured on other substrates.

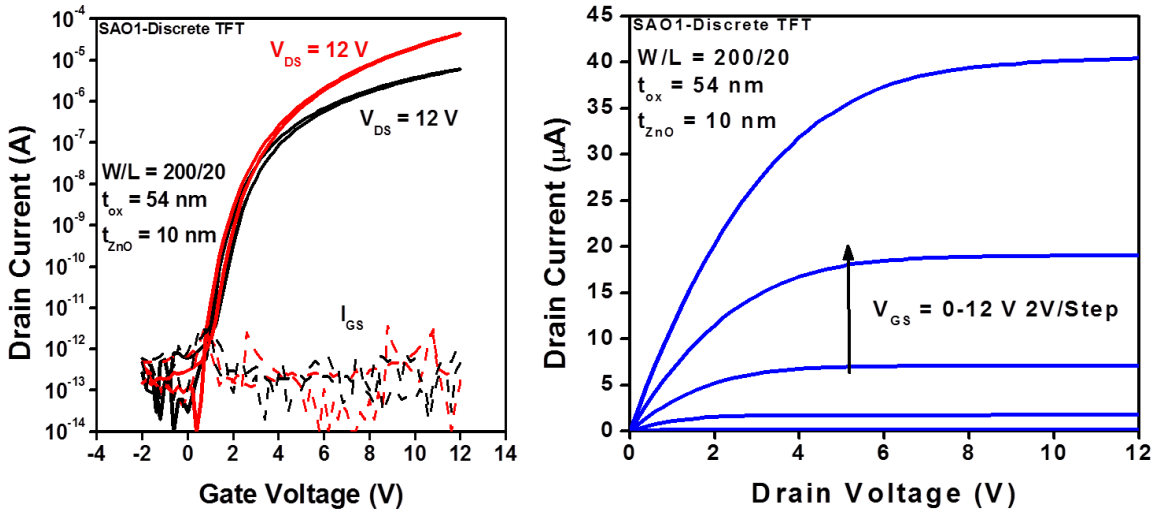


Figure 62. (left) I_{DS} versus V_{GS} for a discrete ZnO TFT co-processed with PZT actuators for adaptive optics (right) I_{DS} versus V_{DS} for the same discrete ZnO TFT. The gate dielectric is 54 nm thick.

While discrete devices functioned properly when tested in a probe station, there were issues due to processing and electrostatic discharge (ESD) with the array after ACF bonding. Nevertheless, preliminary characterization of pixel-level PZT actuation with voltage provided through a shorted ZnO TFT was performed with an optical profilometer. A custom-made box controlling output voltages for each row and column was developed by Dr. Zachary Prieskorn from Astrophysics at Penn State.

Figure 63 (left) shows optical profilometry data for a 1-cm^2 PZT pixel with no voltage (0 V) applied. Figure 63 (right) shows the same pixel with 10 V applied to it. While there is clear distinction, based on the color difference, quantification of the height difference was difficult because the sample was imaged on the side were the thin films were fabricated, making it complicated for the optical profilometer to focus on a single layer. While it is preferable to image

the sample on the front (mirror) side, it was proven difficult to align the optical profilometer to a pixel without any alignment marks. As such, present results are difficult to quantify.

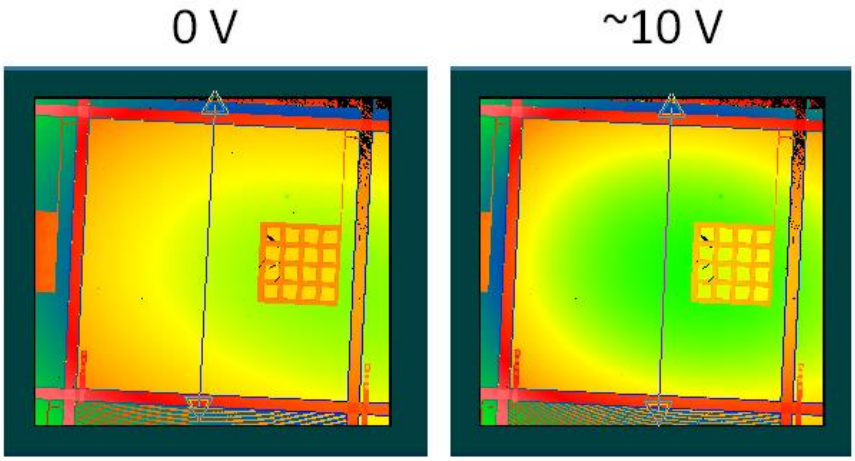


Figure 63. (Left) An optical profilometer image of a 1-cm^2 pixel with no voltage applied to it (0 V); (right) the same pixel with an applied voltage of 10 V. There is a clear change in the shape of the pixel at 10 V, indicating that the PZT has been actuated. Color changes denote the deflection.

ESD-induced failure prevented further testing of the array because the majority of the TFTs were shorted. A pathway to protect the array inputs against ESD events is described in the following section.

4.4.2 Adaptive Optics Array with integrated Electrostatic Discharge (ESD) Input Protection

Electrostatic discharge (ESD) in microelectronic components without any protection can cause electronics to malfunction. ESD is often overlooked in research environments because electronic devices are typically not fabricated using automated equipment and are measured on probe stations where ESD is rarely an issue. However, ESD problems are likely to arise when connections to the electronics are made by other methods besides probing (wire bonding, anisotropic conductive film, flip chip etc.) ZnO electronics integrated with PZT pixels were not

the exception of ESD-induced failure after anisotropic conductive film (ACF) bonding. While preventive, off-chip, procedures were set in place to minimize ESD-induced damage; these procedures were not sufficient to prevent damage of ZnO electronics. Consequently, on-chip ESD-protective circuitry was designed for each scan and data line of the array to prevent damage or malfunction of the ZnO TFTs addressing each PZT pixel.

The purpose of an on-chip, integrated with array, ESD protection circuit is to automatically create a shunting path to safely discharge static electricity. Design of ESD protection circuits vary widely depending on circuit requirements, applications, and electrical stress level. A common ESD protection circuit used in display arrays is to have two diode-connected TFTs, in parallel, and connected between a scan/data line and a common potential ring, as shown in Figure 64. The diode-connected TFTs are placed in two directions to prevent ESD events with either positive or negative sign. The ESD-protection circuit is designed to have low impedance in the case of an ESD event compared to other possible current paths (array) and high impedance during normal array operation.

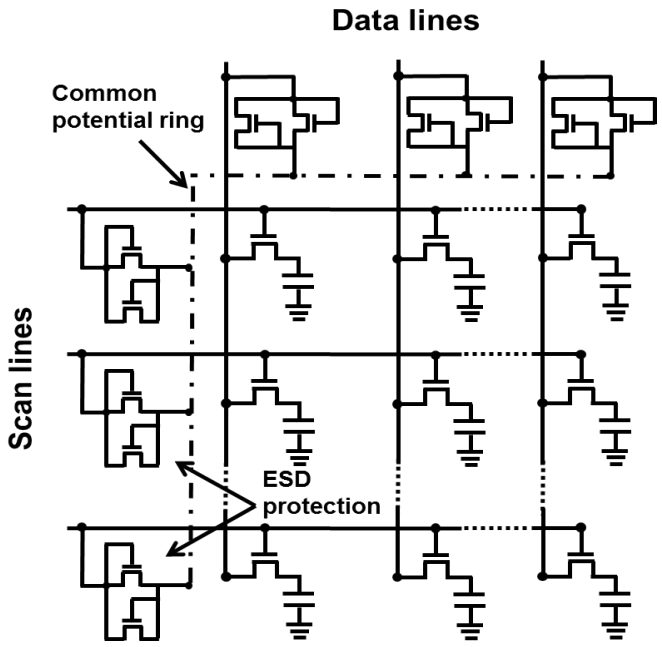


Figure 64. ESD protected scan and data line input using diode-connected TFTs in parallel, connected to a common potential shorting ring.

Using AIM-Spice compact model software, an ESD protection circuit based on ZnO TFTs was designed. There are different models to characterize ESD damage on electronics. The Human Body Model (HBM) is the most commonly used model and represents the discharge from an individual to the device under test (DUT). There are different voltage sensitivity classifications within the HBM; the circuit designed here was based on Class 1A sensitivity, for a voltage range below 500 V. HBM circuit is modeled as a 100 pF capacitor discharged at t = 0 seconds, when the ESD event happens, through a 1.5 kΩ resistor in series and into the DUT, as show in Figure 43 (left). Here, the DUT is two diode-connected ZnO transistors with a W / L = 1000 µm / 500 µm, as shown in Figure 65 (right). The 1.5 kΩ resistor models skin resistance.

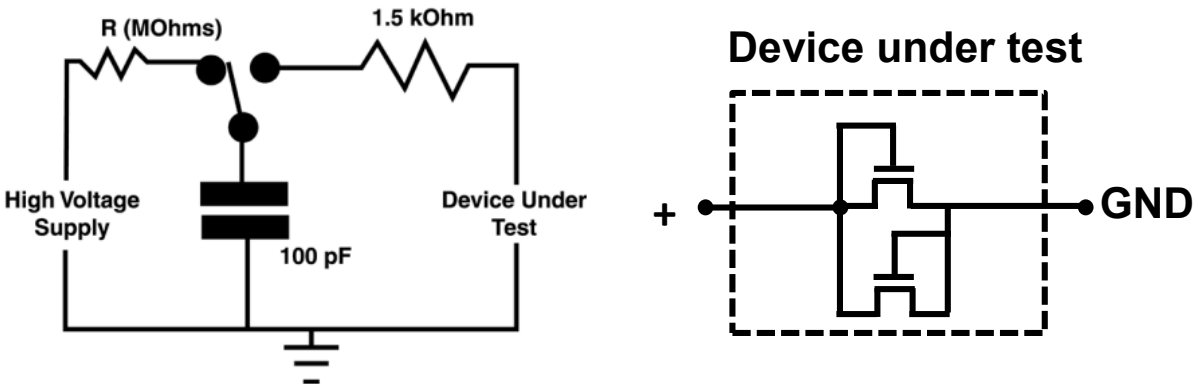


Figure 65. (left) Typical Human Body Model (HBM) circuit (right) ESD protection circuit comprises of two diode-connected ZnO TFTs.

Transient analysis was carried out to understand the dynamic impedance response of the ESD circuit. To prevent gate dielectric breakdown, the TFT was designed and optimized to have a peak transient voltage lower than 2.5 MV/cm. The width and length dimensions were chosen to allow a high dynamic capacitance. That is, as the semiconductor layer is depleted, the semiconductor capacitance changes. This prevents a large peak voltage by increasing the RC the time constant. Figure 66 shows a transient analysis simulation of the ZnO-based ESD protection circuit for a 100 pF discharge. Simulation shows the circuit can discharge an ESD event while maintaining an electric field smaller than 2.5 MV/cm across a 55-nm thick gate dielectric.

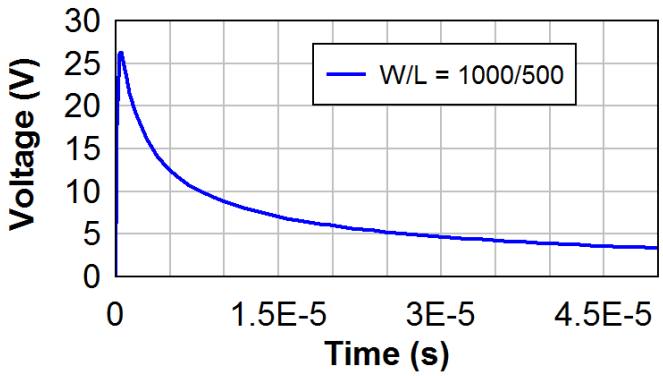


Figure 66. Transient analysis simulation of two diode-connected TFT with W/L = 1000/500 with a peak voltage of 27 V for a 100 pF discharge.

The circuit design was incorporated to the array design, as shown in Figure 67. The ESD protection circuit was fabricated to validate simulation results and integrate it into the PZT array to reduce ESD-related failures in the array.

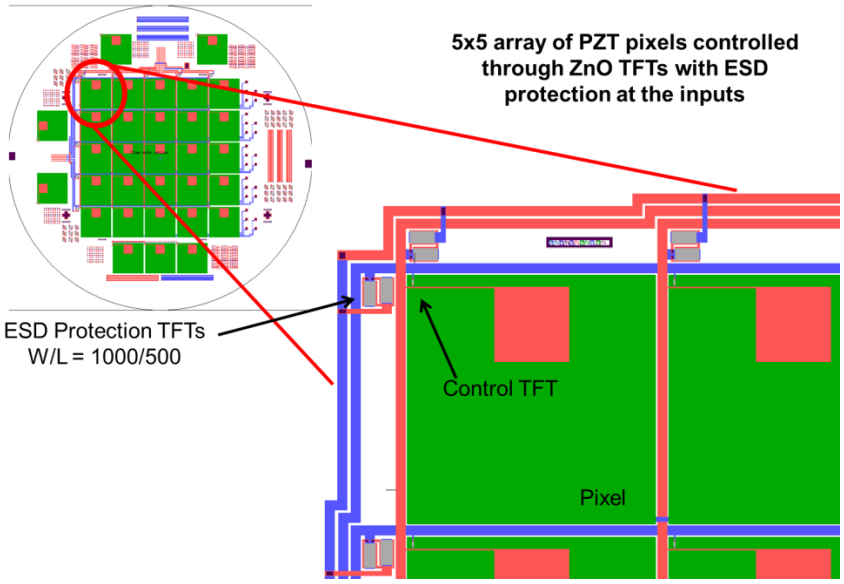


Figure 67. A modified PZT array mask design with ZnO-based ESD protection at the inputs of the select and data lines.

Discrete ESD Protection TFTs were characterized and the I-V characteristics were compared to a TFT with the same dimensions as in the array, as shown in Figure 68. During normal operation of the array, at maximum voltage of V_{GS} = V_{DS} = 10 V, the ESD protection TFTs will have a leakage current of ~50 µA. This current level will not be an issue because the off-chip control electronics used to address the pixels have a maximum output impedance of 0.1 Ω. Figure 68 (right) shows an optical micrograph of the fabricated ESD protection TFTs.

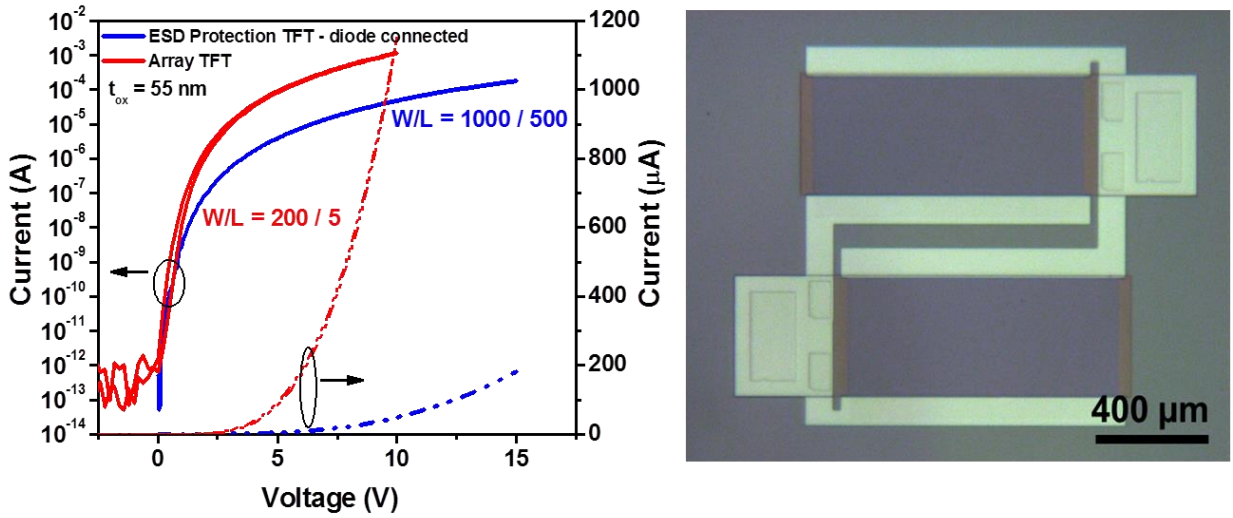


Figure 68. (left) I-Vcharacteristics comparison a TFT in the array and a diode-connect TFT used for input protection against ESD events (right) Optical micrograph of a fabricated ESD-protection TFTs.

Next, a discrete ESD protection circuit (DUT) was connected in to a HBM circuit, as shown in Figure 65, for transient analysis. A 120 pF capacitor was used. A power MOSFET was used as a switch between the power supply and the DUT. The DUT voltage was monitored using a semiconductor parameter analyzer. The measurement time resolution was limited by the parameter analyzer's 10 μs resolution. Figure 69 shows the DUT voltage as a function of time. The peak voltage seen is ~ 5 V. Although this is not a precise measurement of the peak voltage because of the poor time resolution, the DUT still functioned after this test; suggesting the peak voltage did not reach a critical voltage to cause gate dielectric breakdown.

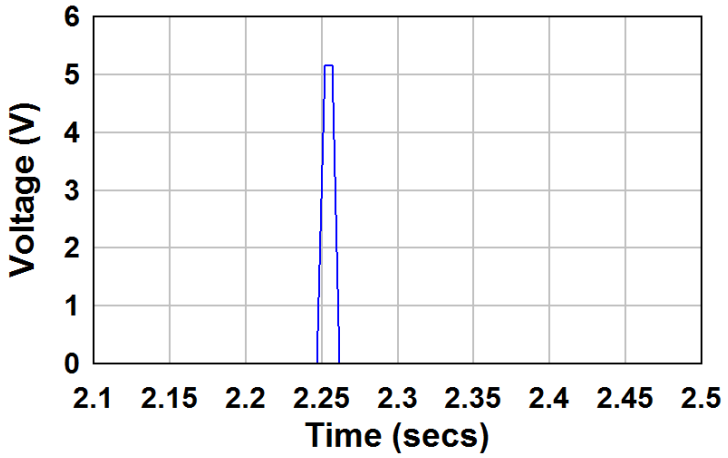


Figure 69. Transient measurement of two diode-connected ZnO TFT with W/L = 1000/500, in an HBM circuit, with a peak voltage of ~6 V for a 120 pF discharge.

Initial mirror deformation measurements on a sample with the ESD protection inputs have been carried out using an optical profilometer on the front of the sample with a Cr/Ir surface (mirror side). Because a method to register the optical profilometer position with respect to the pixels is not in place yet, several rows and columns of PZT pixels were energized through the ZnO TFTs to look for big changes in mirror deformation. Also, in order to look for small changes the mirror needs to be well-mounted on to a fix system to avoid drift (noise) during the measurement. Nevertheless, relative changes in mirror deformation were clearly seen in the order of ~1 μm when 10 V was applied. Further, and more rigorous, and quantitative testing is needed and is underway, including measurements using a wavefront sensing system where quantitative results as function of applied voltage through the TFTs should be able to obtain.

4.4.3 Integrating ZnO Electronics on Curved Mirrors

While it has been shown that ZnO electronics can be integrated with PZT thin films for adaptive optics applications, the demonstration thus far has been on flat substrates. Per the SMART-X requirements, Wolter-I or Wolter-Schwarzschild (conical shape) type mirrors are required for X-ray telescopes. Fabrication of PZT pixel elements have been demonstrated on pre-slumped curved glass substrates (Corning Eagle glass) [115]. Patterning of the pixel elements on a curved substrate is possible because their relatively large size requirements (1 mm^2 – 1 cm^2) [111]. Patterning down to 0.5 cm^2 has been demonstrated using flexible photolithography masks [115]. While it is possible to pattern coarse features (>500 μm) onto a curved substrate by using primitive lithography techniques, finer features (<100 μm) are needed to fabricate ZnO electronics. The approach explored to integrate electronics on a curved substrate is to fabricate the ZnO TFT array on a thin polyimide flexible substrate and then overlay the flexible substrate on to the curve substrate. A thin flexible polymer (PI-2611) is selected as the substrate for the ZnO electronics. Using a thin substrate would minimize introducing local distortion of the mirror after bonding of the electronics to the mirror. Figure 70 shows a conceptualized picture of a curved mirror with PZT elements with a flexible substrate over it with the ZnO electronics.

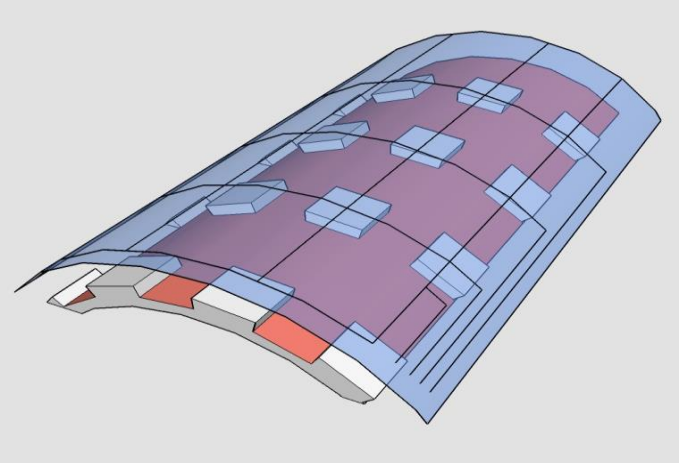


Figure 70. Conceptualized schematic of PZT elements on a curved mirror segments with the ZnO electronics on a thin flexible substrate bonded onto the curved mirror.

There are different approaches to fabricate electronics on flexible substrates. Some of these approaches to flexible electronics include using a temporary adhesive to bond a polyimide thin film onto a rigid substrate or using a liquid-based polyimide that can be spin-casted onto a rigid substrate [116, 117]. Since the flexible substrates are temporarily bonded to a rigid substrate, the processing equipment and methods are compatible to conventional methods used in the semiconductor industry. Figure 33 (right) shows a picture of ZnO TFTs on a 5 μm thick flexible substrate after releasing from the carrier wafer.

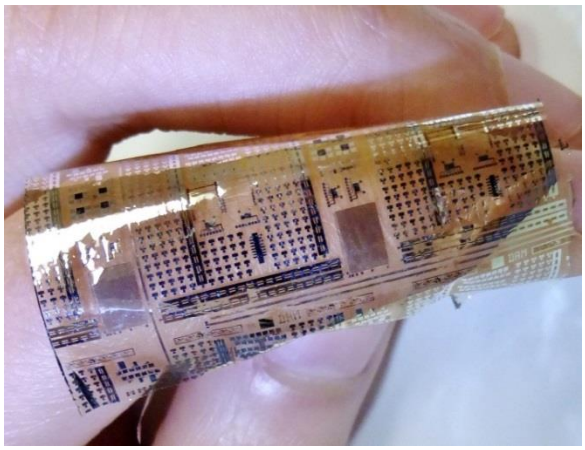


Figure 71. ZnO TFTs fabricated on 5-μm thick spin-casted polyimide. Photo taken from reference [117] .

While the previously described approaches to fabricate electronics can potentially be used to fabricate ZnO electronics on a flexible substrate they have some limitations. The first limitation is the maximum process temperature is limited to ~300 °C. This is not an issue for the ZnO TFT fabrication process but limits putting other thin films with higher processing temperatures on a flexible substrate. Another drawback, which is more crucial, is these processes utilize mechanical delamination of the flexible substrate from the rigid substrate. This mechanical release likely puts high strain on the electronics. A processing method to circumvent the aforementioned issues was developed.

The process starts with the deposition of a sacrificial layer on a rigid substrate. Figure 72 shows a cross-sectional schematic of a ZnO TFT with the flexible substrate spin-coated at last. The choice of a sacrificial layer has been limited to inorganic thin films that can be relatively easily etched in benign wet chemistry. Some examples of sacrificial layers include ZnO, VO_x, and GeO_x. In this example, 50-nm of ZnO deposited by ALD was used. Next, a metal layer is patterned to form the gate electrode and pads for source and drain contacts. The rest of the ZnO TFT process is identical to the process described throughout this document. After the TFT fabrication is completed a solution-based organic layer is spin-coated and cured. In this example, PI-2611 was spin-coated and then cured at 200 °C in air with a ramp rate of 3 °C/min for 8 hours. Finally, to release the electronics on the flexible substrate, the sample is put in a chemical bath (dilute HCl). The etching rate can be accelerated by agitating the solution. For a 2-inch substrate the flexible substrate is fully released from the rigid substrate after ~6 hours. The etching speed of the sacrificial layer can be further increased by making holes through the

flexible substrate in areas not occupied by the electronics so the wet chemistry can attack the sacrificial layer from different directions. This processing method can also be used to fabricate other thin films deposited at high temperature on a flexible substrate. Initial experiments by Margeaux Wallace have shown PZT can be put on a flexible substrate using this method.

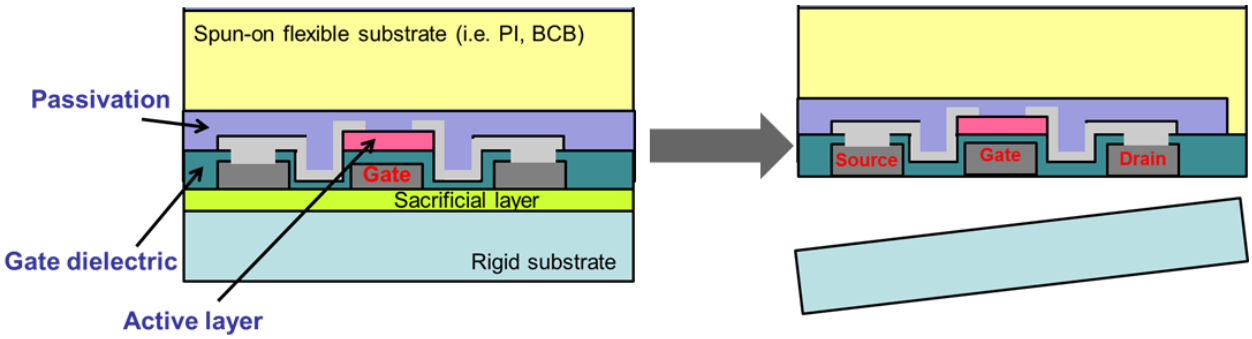


Figure 72. Cross-sectional schematic of a fabrication process for thin film electronics on a flexible substrate.

Figure 73 (left) shows an optical micrograph of a completed ZnO TFT after the flexible substrate was released from the rigid substrate. The active channel region is underneath the gate metal area, facing down.

Figure 73 (right) shows the I_{DS} versus V_{GS} characteristics for a ZnO TFT fabricated using the process described above. The field-effect mobility is comparable to field-effect mobility reported on thin polyimide [117].

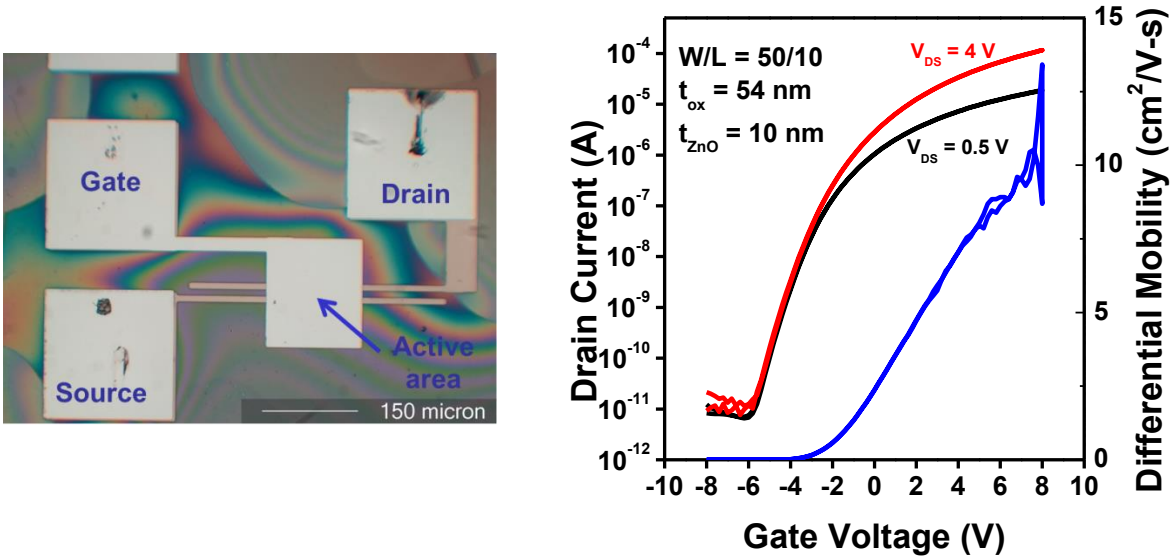


Figure 73. (left) Optical micrograph of a ZnO TFT after the flexible substrate was released from the rigid substrate; (right) I_{DS} versus V_{GS} characteristics of a ZnO TFT fabricated on a rigid substrate and transferred to a flexible substrate.

In this chapter a fairly general monolithic integration process was developed to add more functionality to complex oxide-based thin film devices with ZnO thin films electronics. Integration of ZnO electronics on arbitrary substrates is possible because of the excellent conformality of the PEALD process and its low processing temperature. ZnO active electronics and complex oxide thin-films were demonstrated to have similar performance after integration. Furthermore, it was shown that it is also possible to monolithically fabricate circuits right on top of PZT transducers. This demonstration may be beneficial in sensor or actuator applications where high signal sensitivity is desired (by having on pixel amplification). ZnO TFTs integrated with PZT capacitors (on a flat substrate) in an array scheme were shown to be a promising technology for next-generation X-ray adaptive optics. Finally, a pathway to build electronics on a flexible substrate, in order to integrate them onto conical mirrors was presented. While further testing of the mirror deformation on a flat substrate is still needed the technology is encouraging for the SMART-X mission.

Chapter 5

5.1 Ultra-Low Power ZnO Ozone Sensors Using Pulsed UV Light

Metal-oxide gas sensing devices are commercially available and widely used in industrial and automotive applications. These sensors use bulk metal-oxide semiconductors like SnO_2, InO_2, ZnO, and TiO_2 [118]. It is also possible to use these materials in their thin-film form [119]. Thin films gas sensors have been demonstrated at operating temperatures ranging from room temperature to >400 °C [120-122]. Thin film-based sensors operating at elevated temperatures have good sensitivity, response time, and, at different operating temperatures, provide some gas selectivity, but these features come at the cost of high power consumption (>100 mW) [119, 123]. Power consumption is an important parameter for low-power applications such as wearable health monitoring systems and wireless sensor nodes [124, 125]. Ultra-low power gas sensor operation (<1 μW) would open up a pathway to use energy harvesting devices to self-power such systems [126].

There are a number of parameters that make a good electronic gas sensor [127], these include: electrical stability when nothing is being detected, good sensitivity to the target gas, fast response time and reversibility (that is, the sensor should not be a sense-once device), and good gas selectivity. In this work the first three requirements are addressed while keeping the sensor power operation below 1 μW. The target gas was limited to ozone in this work but a discussion towards gas selectivity in the ZnO TFT gas sensors is discussed in section 5.5.

In this work, ZnO-based ozone sensor thin-film transistors (TFTs) were optimized for ultra-low power operation. The ZnO TFT ozone sensors operate at room temperature with an average power of ~0.8 μW. The TFT configuration allows varying the sensor operating conditions over a wide range. The gas sensors were optimized to have minimal electrical drift during operation by partially passivating the TFT structure and annealing of the material stack prior to fabrication. A novel way to reset and achieve low power consumption of the ozone sensors is described. Ultraviolet (UV) light periodic pulsing (25 mseconds every 40 seconds) was used to reset the ozone sensor. Different ozone levels were detected by looking at the $\partial I / \partial t$ after the UV reset pulse. Ozone was detected down to 110 ppb.

5.2 Electrical Stability of ZnO TFT Gas Sensors

The ZnO TFT gas sensors used in this work have a staggered, bottom-gate structure and have been fabricated on both glass and oxidized silicon substrates. 100-nm thick Cr deposited by sputtering was used as the gate layer and patterned by wet etching. Next, a 32 nm thick Al_2O_3 layer as gate dielectric and a 10 nm thick ZnO layer as the active channel material were deposited at 200 °C by plasma-enhanced atomic layer deposition (PEALD) [43]. After patterning the gate dielectric and active layer by wet etching, 100 nm Ti source and drain contacts were deposited by sputtering and patterned by lift-off. After metal contacts have been deposited, the TFT can serve as a gas sensor, with a structure as shown in Figure 74a. Similar TFT structures are typical in electronic gas sensors [122, 128, 129]. However, when the TFTs are used in circuit applications, a passivation layer is used to protect the active semiconductor surface from the ambient and to significantly improve device stability [130], as shown in Figure 74b. Al_2O_3

deposited by ALD or PEALD is typically used as a passivation layer and have demonstrated good device stability [43, 130]. However, for gas sensing applications the TFT active area needs to be open to the sensing environment. The electrical stability of a partially passivated TFT structure, as shown in Figure 74c, was investigated as an avenue to have both good stability and gas sensitivity. The structure has an Al_2O_3 passivation layer everywhere including the contact regions with an opened window to the active layer to allow gas interactions with the ZnO semiconductor. The partially-passivated TFTs were fabricated by opening windows in the active area region using a pH-controlled wet etch with a selectivity of >1:400 for Al_2O_3 over ZnO [131].

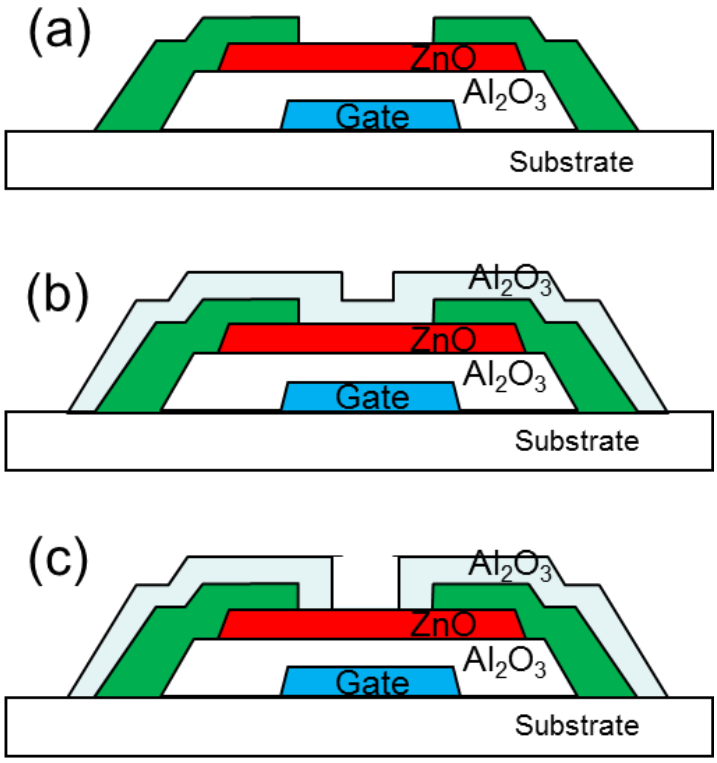


Figure 74. Cross-sectional schematic of the three different ZnO TFT structures used to investigate the electrical stability in air and the ozone sensitivity. (a) ZnO TFT without a passivation layer (b) ZnO TFT with a passivation layer (c) ZnO TFT partially passivated with the active area exposed to the ambient.

The three-terminal TFT-based structure used in the work provides significant advantages compared to two-terminal gas sensors. For bulk or ungated thin film sensors it is necessary that the device have useful initial conductivity and the conductivity cannot simply be adjusted. A transistor structure allows the use of thin films that have few free carriers with the gate used to accumulate mobile charge to provide the desired conductivity. The operating point can easily be varied from sensor currents less than a nA to greater than 1 mA. By fabricating the ZnO TFT-based sensors on low thermal conductivity substrates such as glass or polyimide, operation at high current can also provide self-heating for sensor operation or clearing at high temperature [132].

Initial testing of the ZnO TFT gas sensors, using ozone as the target gas, was done at room temperature with the device biased in the subthreshold regime with a drain current of a few hundred nA. Unpassivated ZnO TFT gas sensors, with a structure as shown in Figure 74A, were sensitive to ozone exposure well below 1 ppm. For devices measured at constant bias, ozone exposure in the low ppm level leads to a rapid (few second or less) decrease in drain current of about 2% per ppm. Unfortunately, the unpassivated sensors also have undesirable characteristics that make them difficult to employ as useful sensors. Once exposed to ozone, the sensors are slow (minutes to many minutes) to recover their unexposed response. Heating the sensor gives faster recovery, but a cost of greatly increased operating power [119, 123, 132].

Even more problematic, the unpassivated sensor current is not stable even while it is not exposed to ozone or other gases. Figure 75 (black curve) shows I_{DS} versus time for an unpassivated ZnO gas sensor in zero air. After 1800 seconds, at a constant bias with $V_{GS} = V_{DS} = 2$ V, the drain

current drops 31% from its original value. A TFT structure with a 30-nm ALD Al_2O_3 passivation layer, as shown in Figure 74b, has much better electrical stability, but is not useful for gas sensing because the passivation layer blocks the target gas from the sensor. For comparison, a passivated ZnO TFT was also stressed for 1800 seconds, with V_{GS} = 2.5 V and V_{DS} = 2 V (the bias was selected to obtain a similar operating current). Figure 75 (red curve) shows I_{DS} versus time for an Al_2O_3-passivated ZnO TFT with a 4.5% decrease from its initial I_{DS} value after 1800 seconds. For gas sensing applications, a TFT that has the active material exposed to the ambient, but has the electrical stability similar to the passivated TFT is desired.

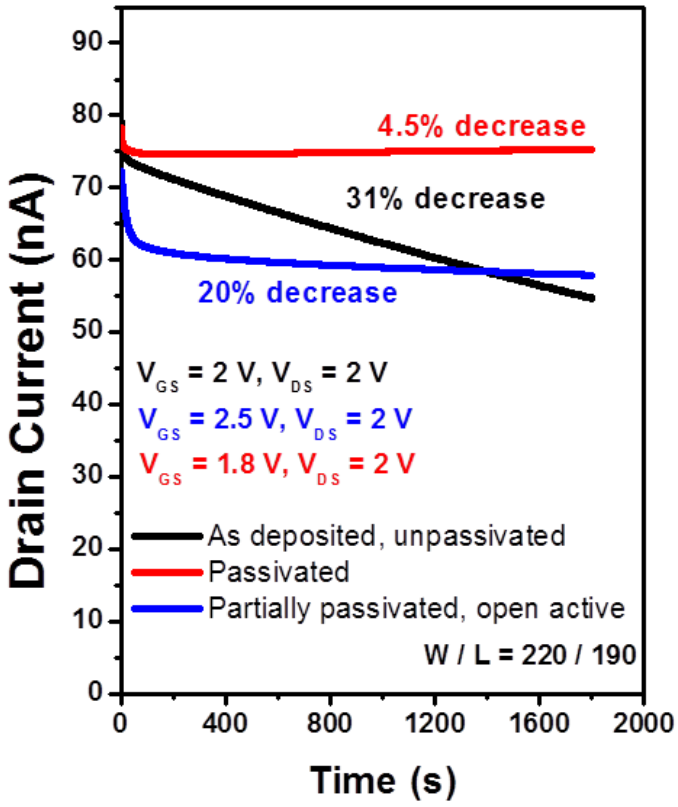


Figure 75. Drain current as a function of time for ZnO TFTs (black curve) unpassivated (red) passivated (blue) partially passivated. The gate voltage was adjusted in each case to provide similar drain current. A partially passivated ZnO TFTs has a good trade-off between electrical stability and the ability to sense gases.

Figure 74c shows a TFT structure with passivated contacts and the active area open to the ambient. This device structure provides good electrical stability and is able to sense a gas. Figure 75 (blue curve) shows I_{DS} versus time for a partially passivated ZnO TFT. After 1800 seconds the drain current decreases 20% from its initial value. This is an improvement greater than 10% in electrical stability, compared to unpassivated ZnO TFTs, by simply passivating the contacts. This suggests a possible chemical interaction (oxidation) at the perimeter of the Ti metal contact-ZnO interface. This electrical stability might be adequate for gas sensing applications, particularly by observing the two different pronounced time constants dominating the drain current drop as a function time. It can be conceivable to wait for the drain current to stabilize (enter the second time constant region) and then use the TFT as a gas sensor in the more stable region. On the other hand, the shape of the drain current as a function of time for the unpassivated ZnO TFT (black curve) has a rapid and consistent decrease as a function of time making it more challenging to realize an electrically stable gas sensor. Another parameter that can have an effect in ZnO thin films' electrical stability is post-deposition annealing [4, 133]. ZnO thin films were annealed and their electrical stability was compared as a function of annealing temperature.

Annealing of oxide semiconductors in certain ambient conditions can drastically change the material's structure and is known to help reduce the trapping sites in ZnO-based materials [4, 134, 135]. Improvement in electrical stability as a function of annealing temperature in unpassivated ZnO TFTs has been reported [133]. Different physical mechanisms have been proposed for the structural changes in ZnO as function of annealing temperature, pointing to the annealing of either Zn interstitial Zn_i or O vacancies V_O [136, 137]. A number of annealing

ambient conditions, techniques, and temperatures have been reported to improve oxide-based TFTs electrical stability [133, 134, 138, 139]. These conditions widely vary because the ZnO thin film stoichiometry varies depending on the deposition technique, oxygen partial pressure, deposition temperature, and precursor used to deposit the thin films [4, 140, 141].

The annealing effects of polycrystalline ZnO thin films were studied in the context of TFT electrical stability for gas sensor application. The ZnO films were annealed prior to TFT fabrication to avoid the Ti metal contacts and the passivation layer to react with the underlying ZnO thin film. The annealed ZnO TFTs were measured unpassivated, passivated and partially passivated. Because the interest in this work is to have an electrically stable ZnO TFT gas sensor, the results shown hereafter will focus on the annealed and partially passivated structures shown in Figure 74. Figure 76 (right) shows the percentage change in drain current as function of time (1800 seconds) for three ZnO TFTs: as deposited at 200 °C (black curve), annealed at 400 °C (red curve), and annealed at 600 °C (blue curve) for 1 hour in air. The gas sensor devices were measured at similar current densities of ~320 nA / mm. Different gate voltages were used for each TFT because of an induced V_{ON} shift with annealing temperature. As deposited ZnO TFT (black curve), as shown previously, has a 20% decrease in current from its initial value. A ZnO TFT annealed at 400 °C and with open windows on the active area (red curve) shows a ~2.4% decrease in current from its initial value. This drain current percentage drop in 400 °C annealed and partially passivated ZnO TFT is superior to Al_2O_3-passivated ZnO TFT at 200 °C, making this structure an excellent room temperature operated gas sensor. A ZnO TFT annealed at 600 °C and with open windows on the active area (blue curve) show a ~1.7% decrease in current from its initial value. While the further increase in annealing temperature slightly improves the

electrical stability of the ZnO TFT, the improvement appears to plateau. Also, annealing temperatures over 400 °C greatly limits the number of substrates that can be used. This is particularly an issue if low-cost or flexible substrates are desired. There, ZnO TFTs annealed at 400 °C were used in subsequent ozone gas sensing experiments. Figure 76 (left) shows an optical micrograph representative of the gas sensors with open active area and passivated contacts.

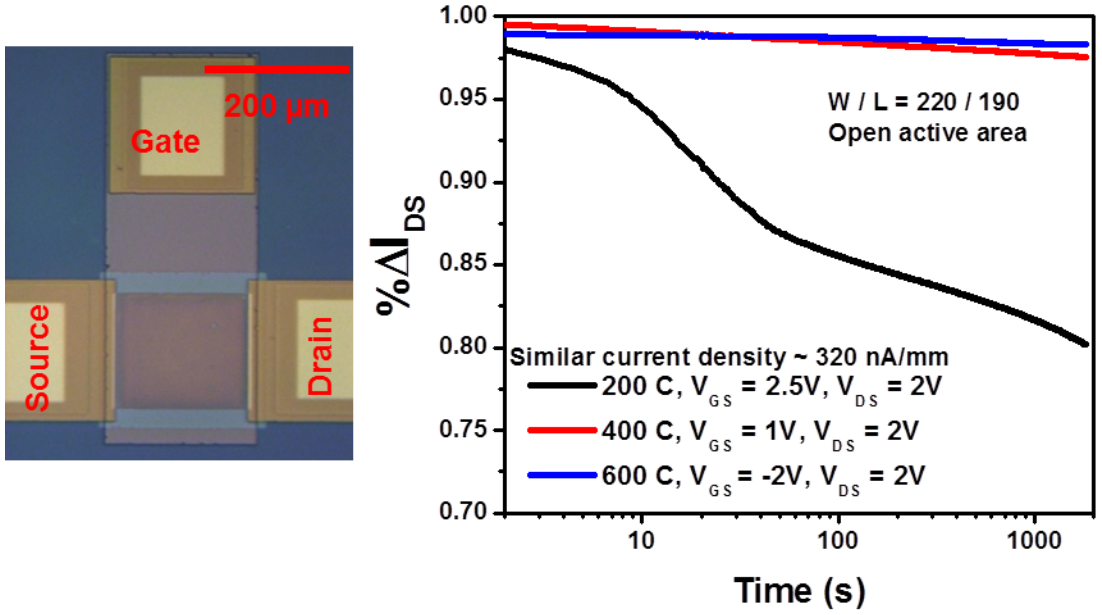


Figure 76. (left) Optical micrograph of a fabricated ZnO TFT with open active area region to thee ambient (right) Drain current percentage change as function of time for ZnO TFTs annealed at different temperatures. The stability is improved with increasing annealing temperature.

5.3 Ozone Sensing Test Setup

To test the ZnO TFT gas sensors for detection of ozone a test chamber and a system was developed, as shown in Figure 77. The chamber was made out of polytetrafluoroethylene (PTFE) with a volume of ~1 liter. The ozone was generated using a UV photometric ambient ozone calibrator TECO 49PS. An industrial ozone analyzer was connected at the outlet port of the test

chamber to monitor the ozone concentration after the chamber. A Philips PM 5771 pulse generator was used to pulse the UV light. Gas sensors were wired bonded in dual-in-line packages, and inserted in a zero-insertion-force connector board in the chamber. An HP 4156 parameter analyzer was used to measure I_{DS} versus time for several TFT sensor variations. The measurements were done either in room air or in dry zero air. No differences were seen between the two.

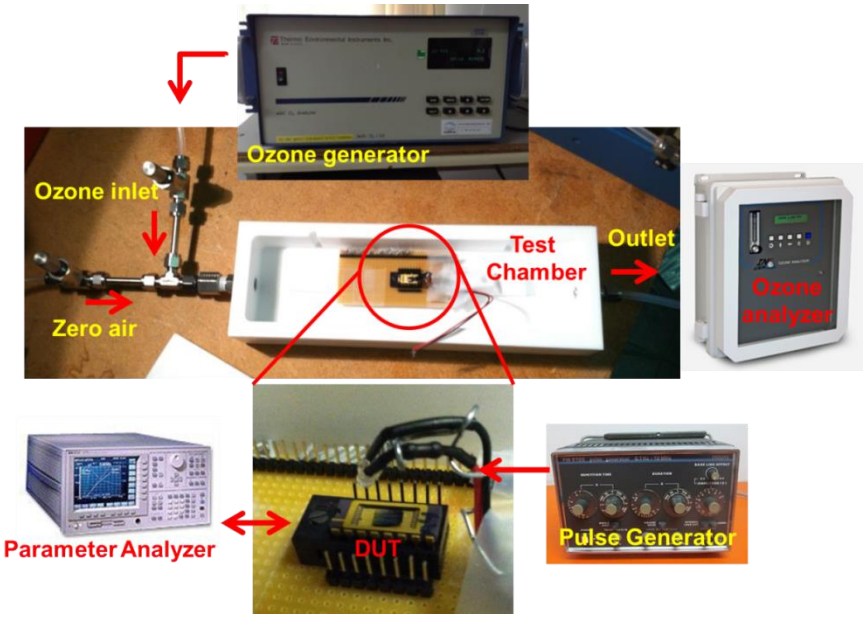


Figure 77. The gas sensor measurement setup consists of a PTFE chamber with the DUT sample in. A UV LED is pulsed with using a pulse generator. An ozone generator is used to provide ozone to the chamber and an industrial ozone analyzer is connected at the chambers outlet. A parameter analyzer is used to monitor the change in current as a function of time of the ZnO gas sensor.

5.4 Ozone Gas Sensor Recovery using UV Light

Thus far, a pathway to make a good electronic gas sensor with excellent electrical stability and good sensitivity to the target gas (ozone in this work) has been shown. Next, a method to have a fast sensor's recovery time after ozone exposure, without using a heating element, is described. Operating gas sensors at room temperature limits the sensors recovery time because the gas

absorption and desorption time constants tend to be long [142-144]. ZnO thin films have been shown to exhibit photoconductivity when subjected to UV light [3, 120, 145]. The photoconductivity arises from the absorption of photons with energy higher than the energy band gap of the ZnO leading to the generation of electron-hole pairs by light absorption. UV light has been used in metal oxide gas sensors to activate the sensors before gas sensing operation [121, 145]. A drawback of using this method is that it takes a long time (>10 minutes) for the ZnO to reach a steady state current prior to ozone exposure [121]. While this provides a pathway to circumvent using elevated temperatures to have fast recovery times in the gas sensors, the gas sensor "activation" is not stable over a long time. UV light was used in a novel way to quickly recover the ozone sensors.

The approach to return the sensor to a baseline, using UV light, during ozone exposure is as follows: the sensor is illuminated with UV light periodically (40 seconds in this case, arbitrarily chosen to keep the overall power low) and with a pulse of 25 milliseconds. After the illumination pulse, different ozone level can be detected by looking at the $\partial I / \partial t$. Figure 78 (left) shows the percentage change in current for a ZnO TFT with open windows in the active area, annealed at 400 °C, exposed to different levels of ozone concentration: 110 ppb (blue curve), 170 ppb (pink curve), 370 ppb (red curve), and 550 ppb (green curve). The ZnO gas sensor is reset periodically (every 40 seconds). After the UV pulse, the slope of the drain current is dependent on the ozone concentration. This slope is used to detect different ozone levels while keeping the sensor power consumption low.

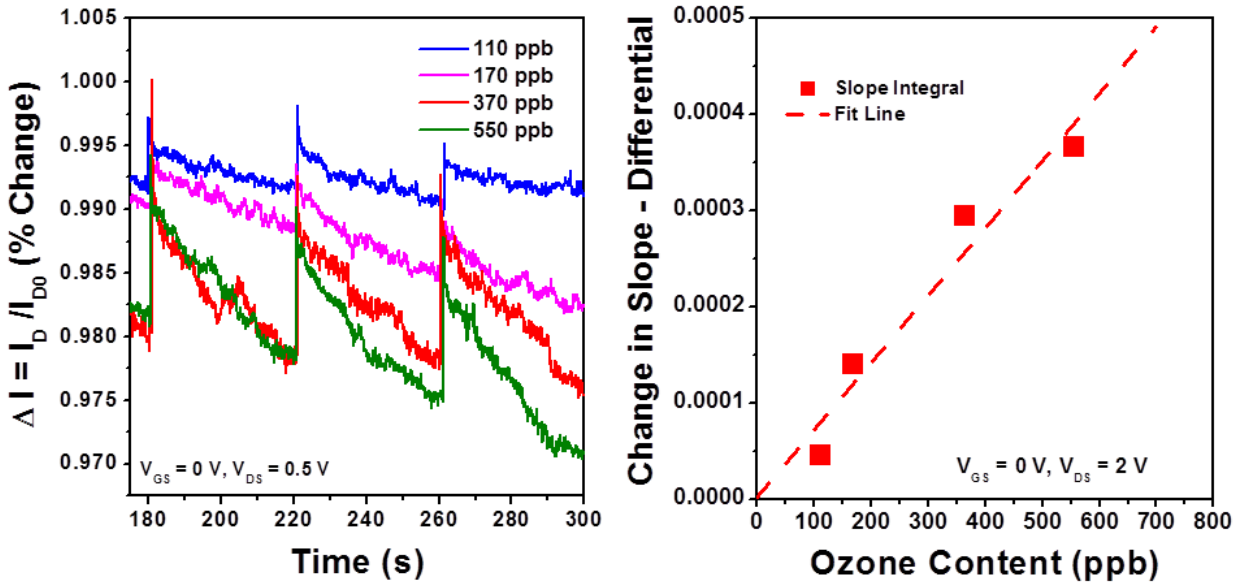


Figure 78. (left) Percentage of change in current for an optimized ZnO gas sensor with ozone gas detection as low as 110 ppb. The sensing limit was mainly limited by the ozone generator. The periodic increase in current corresponds to when the UV LED is pulsed. (right) The extracted differential slope for each trace correlated the slope with the ozone content.

For the different ozone concentrations, the change in slope was extracted as a function of ozone concentration, as shown in Figure 78 (right). Similarly, an integral under the curve can also be used. The change in slope is somewhat linear as a function of ozone concentration and is reversible. Using this method, ozone concentration down to 110 ppb can be detected without the need to use a heating element to operate the gas sensor. Testing of lower ozone concentrations was not possible due to the ozone generator's lower limit. This could be circumvented by diluting ozone with an inert gas.

By optimizing the electrical stability of the ZnO TFT gas sensors, using a partially passivated structure, a post-deposition anneal, and using pulsed UV light, a gas sensor with an average power of 0.8 µW has been achieved.

5.5 Towards Gas Selectivity

Thus far, the discussion of the ZnO TFT gas sensor has largely been focused on having an electrically stable and low-powered device. Of course, a gas sensor needs to have selectivity otherwise it is difficult to target particular gases. An approach to achieve gas selectivity without the need of a heater is to use organic materials over the ZnO active region to act as filters. An advantage of the gas sensors used in this work is that they are operated at room temperature so using organic layers is possible without perturbing the relatively low thermal stability in a lot of the organics. Phtalocyanine has been used as sensing material and has been shown to have selectivity towards ozone over nitrogen dioxide [146]. Likewise, indigo dye has been used to detect ozone concentration in water by the change in color in dye from the reaction between ozone and indigo [147]. A preliminary survey of thermally-evaporated indigo dye over the ZnO TFT gas sensors to achieve gas selectivity is presented.

Optimized ZnO TFT gas sensors, annealed and partially passivated, were used to thermally evaporate ~30 nm of indigo. After indigo deposition, the gas sensors were tested under the same conditions as in section 5.4. Figure 79 shows the combined results, previously shown in Figure 78, of the drain current percentage change as a function of time with the response of a ZnO gas sensor with indigo films over it. For the sensors with indigo thin film, the trend of the percentage

change in current is not consistent but there is a clear difference showing little current drop for different ozone levels compared to the sensors without indigo film. A more detailed study, including the use of other target gases, is needed to confirm these results. Nevertheless, the use of organic layers is a possible pathway to have gas selectivity in room-temperature operated gas sensors.

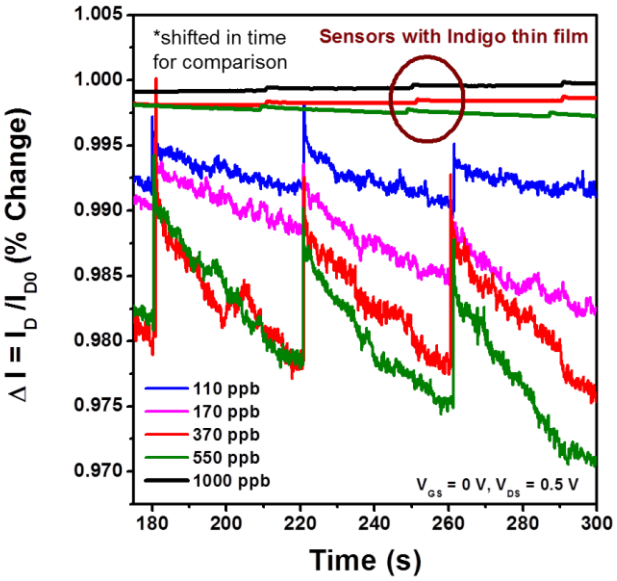


Figure 79. Percentage of change in current for an optimized ZnO gas sensor without any organic layer (as previously shown in Figure 78) and ZnO gas sensor with ~30-thick indigo film over the gas sensor. The drain current on the ZnO gas sensor with indigo film appears to not change as a function of ozone concentration.

Chapter 6

6.1 Conclusions

This thesis has explored various applications, outside of the display industry, where the high-mobility, fast circuit speed, and substrate-agnostic process of this technology could provide differential advantage over the established large-area technology (a-Si:H). The development of a novel showerhead PEALD system led to examine the deposition parameter space to obtain high performance ZnO TFTs. Under optimized conditions ZnO films have a mobility of >20 cm^2/V-s deposited at 200 °C and ~39 cm^2/V-s at 300 °C. The study of ZnO films deposited by PLD helped comparing similarities and differences in material and electrical characteristics to PEALD films. ZnO devices formed using either technique have at least an order of magnitude enhancement in performance over a-Si:H devices. The improvement is partly owed to the intrinsically different chemical bonding resulting in oxide semiconductors being fairly insensitive to disorder. This feature of ZnO is exploited to demonstrate radiation hardness of TFTs. Similar high-energy irradiation effects observed on ZnO devices with different material stacks and deposited by different techniques further confirmed the intrinsic insensitivity to disorder of the semiconductor. A simple sheet-charge model at the semiconductor's back interface can account for the small changes in V_T and V_{ON}. Unlike bulk Si CMOS technology, electrical bias during irradiation was found to be negligible for ZnO TFTs. This can be simply explained by the enormous difference in capturing volume in a thin film device compared to a bulk device. An apparent increase in subthreshold characteristics, during electrical bias and irradiation, was found related to the inverted-staggered structure many TFT structures commonly use. Unlike bulk devices, where the gate field always terminates at the bulk of the material, in an

inverted-staggered TFT structure the gate field is not contained during all regions of device operation. It was determined that the gate fringing field causes the apparent increase in subthreshold current because it attracts mobile charge while biasing the device during irradiation. This anomaly can be circumvented by simply forcing the top surface to a zero potential. The low-temperature process and radiation-hardness of ZnO devices lend themselves to integrate them with PZT devices to provide added functionality to the aforementioned devices for a space-specific application. A monolithically integrated array of PZT cells with ZnO electronics was demonstrated for adaptive optics X-ray telescopes. Finally, ZnO-based gas sensors were optimized to operate at ultra-low power (<1 μW) for potential ubiquitous gas sensing applications. The excellent gas sensitivity and stability was achieved by using a post-deposition anneal and partially passivating the sensor with only the active sensing area open to the ambient. A key enabler to achieve ultra-low power operation was to use pulsed UV-light to reset the gas sensor. The use of UV-light yielded very short gas sensor recovery time (milliseconds). This work showcases different application-driven areas where ZnO thin-film electronics could provide added functionality to existing systems or devices using simple a straightforward integration process.

6.2 Future Work

The first recommendation for future work is to gain a better understanding of the basic ZnO material characteristics in its thin film form as function of processing variants. While high performance using ZnO films deposited by PEALD has been demonstrated in section 2.2 there is room for improvement compared to PLD-deposited (section 2.3) films and to single crystal

films. As discussed in section 2.4, there are many apparent similarities between films deposited by PEALD and PLD; though, experimentally calibrated models shed some light on the different defect energy levels needed to fit the electrical characteristics of each respective material. A thorough study correlating the material's microstructure to changes in electrical characteristics may provide a guideline to not only achieve higher performance but to further increase the electrical stability in ZnO devices. In section 2.2, a short survey of the deposition temperature yielded in mobility improvement. Similarly in chapter 5, annealing of ZnO films helped the TFT's stability but no improvement in mobility was observed. Understanding the effects of energy and ambient conditions used either during film growth or post-growth in the ZnO microstructure is needed. Figure 80 shows preliminary low-temperature photoluminescence (PL) of ZnO films deposited at 200 °C (black curve) and annealed at 400 °C (red curve) for 1 hour. Near band-edge emission at 3.36 eV is seen in both cases, as expected. Phonon replicas (longitudinal optical phonons give rise to equidistant replicas), typically only expected for single crystal material and indicative of high quality crystals [148], near band-edge are somewhat surprisingly observed in as deposited films. On the annealed film, the near band-edge emission peak appears to have merged with at least one defect level below the conduction band minimum. An understanding of the associated energy level transitions, particularly near the conduction band minimum, as function of deposition and post-deposition temperature can help tune the electrical characteristics of the ZnO TFTs.

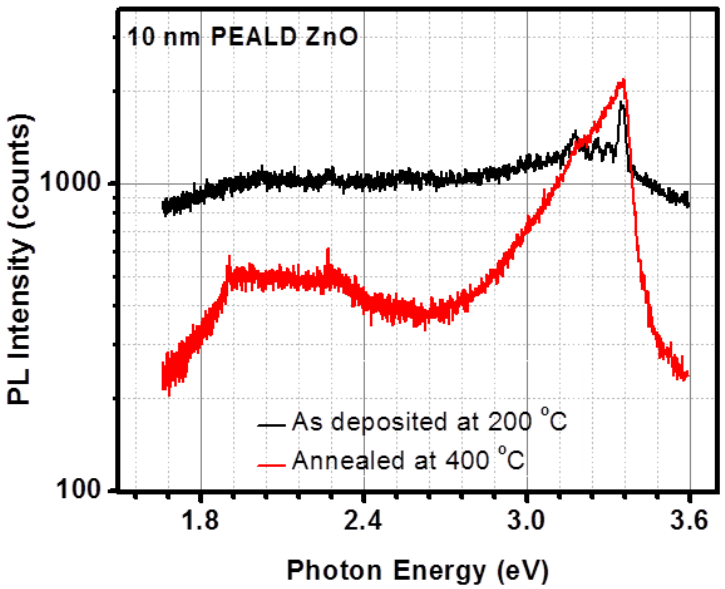


Figure 80. Photoluminescence spectra obtained at 11 K for PEALD ZnO films as deposited (200 °C) and annealed in air at 400 °C. Understanding of the defect energy levels as function of processing conditions could lead to tune the material for high performance device applications.

The second major area for future work is to further develop application-driven demonstrations using the features of this technology. Examples of possible demonstrations build upon the work described in this thesis will be described next.

The ZnO TFTs' radiation-hard feature and substrate-agnostic process can be combined with photodiodes and a scintillator, potentially on light-weight and flexible substrates, for applications such as medical dosimetry, nuclear reactor monitoring, or X-ray imagers. Current X-ray radiation detection systems are developed on rigid substrates (glass). While these systems are acceptable for applications where weight and footprint are not an issue, they become cumbersome or impossible to use in the field. The issue of weight and footprint is even more obvious in 3-dimensional X-ray (computerized axial tomography) CAT scan systems. An advantage of using ZnO TFTs as the backplane for imaging applications is that the electronics

can be fabricated on flexible, light-weight substrates. Commercially available X-ray imagers use amorphous a:Si-H p-i-n diodes as the sensing material. Also, materials like organic semiconductors have been shown to have good light absorption with good sensitivity and response time used as bulk heterojunction photodiodes [149, 150]. Integration of both a:Si-H and organic semiconductors with ZnO electronics have been previously demonstrated [52, 151, 152]. For gamma-ray radiation dosimetry polymers like metal phthalocyanines are potential candidates because they have shown good gamma ray sensitivity and are compatible with a low-temperature process [153]. A circuit design would have to be designed, fabricated and tested. Existing equipment described in section 3.3 could be used to monitor/source voltages of an imager array.

Chapter 4 describes in detail the integration of piezoelectric films with ZnO electronics for generic actuation applications. Ultrasound transducers used for actuation, imaging or sensing [154] could benefit from having ZnO electronics directly integrated onto each transducer. The ZnO electronics could provide pixel-level voltage amplification and reduce the number of wiring traces by using a row-column addressing scheme for a large number of transducer elements in an array. The decrease in wiring traces can not only reduce the connections' complexity but can also allow higher system resolution by increasing the element density over the same area.

A good platform to bring together the recent advancements made in materials, processing, and circuit demonstrations in the PZT and ZnO thin film technologies would be the demonstration of a self-powered gas sensor node system. The majority of the pieces to realize this system have been independently developed and tested. Yeager C. has optimized PZT thin films for MEMS mechanical energy harvesting [155]. Initial work on transferring similar PZT thin films to

flexible substrates using the method described in 4.4.3 has been successful. By transferring the piezoelectric onto a thin, flexible substrate the system can use for gas sensor nodes in industrial or commercial areas with ventilation ducts. Low-power AC-to-DC rectification has been recently reported using ZnO electronics which could be used to rectify the energy harvester's output voltage [156]. And for gas sensing, the sensors described in chapter 5 are a natural addition to the system because they have been optimized to operate at ultra-low power. This entire system can be monolithically integrated onto one flexible substrate. The use of both sides of the flexible substrate is possible by simply making vias through it during the process. Conceptual art of the self-powered gas sensor node system is shown in Figure 81.

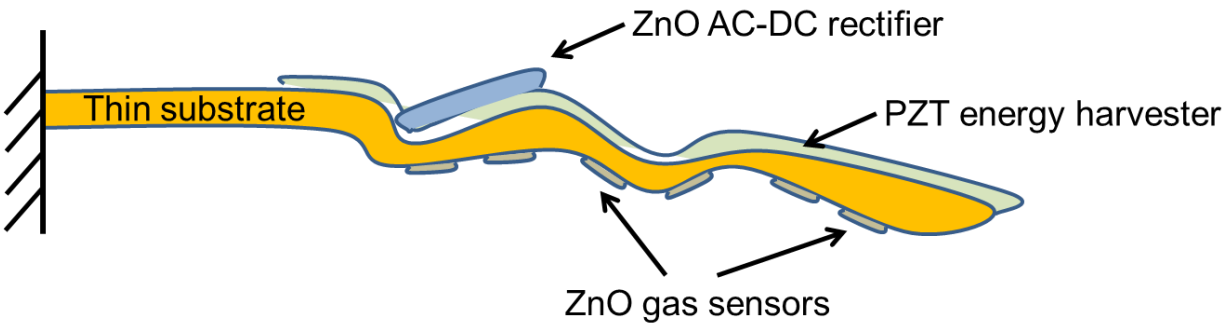


Figure 81. Conceptual art of a self-powered gas sensor node system using PZT as the energy harvesting material and ZnO electronics for AC-to-DC rectification and for gas sensing.

Appendix A: List of Symbols

I_{DS}	drain current	L	channel length
V_{GS}	gate voltage	W	channel width
V_{DS}	drain voltage	t_{ox}	gate oxide thickness
V_{ON}	turn on voltage	μ	field-effect mobility
V_T	threshold voltage	E_g	bandgap
C_{OX}	oxide capacitance per unit length	R_s	sheet resistance

Appendix B: Elements and Element Compounds

Zn	zinc
O_2	oxygen
Al	aluminum
Ba	barium
Cr	chromium
Ti	titanium
Pt	platinum
Au	gold
Mg	magnesium
Ir	iridium
Pb	lead
Si	silicon

ZnO	zinc oxide
$Pb(Zr, Ti)O_3$ or PZT	lead zirconate titanate
$Ba_{1-x}Sr_xTiO_3$ or BST	barium strontium titanate
Al_2O_3	aluminum oxide
H_2O	water
Sb_2S_2	stibnite
ZnTe	zinc telluride
AZO	aluminum doped zinc oxide
SiO_2	silicon dioxide
$Zn_{1-x}Mg_xO$	zinc magnesium oxide
ITO	indium tin oxide
IGZO	indium gallium zinc oxide
IZO	indium zinc oxide

Appendix C: Abbreviations

TFT	thin film transistors
MEMs	microelectromechanical systems
FET	field-effect transistor
MOS	metal-oxide-semiconductor
CMOS	complimentary MOS
HEMT	high-electron mobility transistor
RTD	resonant tunneling diode
LED	light emitting diode
UV	ultra violet
ESD	electrostatic discharge
DOS	density of states
ppb	parts per billion
PEALD	plasma-enhanced atomic layer deposition
MOCVD	metal-organic vapor deposition
PLD	pulsed laser deposition
ALD	atomic layer deposition
CVD	chemical vapor deposition
MBE	molecular beam epitaxy
DEZ	diethylzinc
TMA	trimethylaluminum
LCD	liquid crystal display
RMS	root means square
slmp	standard liter per minute
sccm	standard cubic centime per minute
TCAD	technology computer aided design

References

[1] Y. Kuo, *Thin film transistors. 1. Amorphous silicon thin film transistors* vol. 1: Springer Science & Business Media, 2004.

[2] Y. Y. Lin, D. J. Gundlach, S. F. Nelson, and T. N. Jackson, "Stacked pentacene layer organic thin-film transistors with improved characteristics," *Electron Device Letters, IEEE,* vol. 18, pp. 606-608, 1997.

[3] R. L. Hoffman, B. J. Norris, and J. F. Wager, "ZnO-based transparent thin-film transistors," *Applied Physics Letters,* vol. 82, pp. 733-735, Feb 3 2003.

[4] K. Hoshino, D. Hong, H. Q. Chiang, and J. F. Wager, "Constant-voltage-bias stress testing of a-IGZO thin-film transistors," *IEEE Transactions on Electron Devices,* vol. 56, pp. 1365-1370, Jul 2009.

[5] B. Hekmatshoar, S. Wagner, and J. C. Sturm, "Tradeoff regimes of lifetime in amorphous silicon thin-film transistors and a universal lifetime comparison framework," *Applied Physics Letters,* vol. 95, Oct 5 2009.

[6] M. Shur and M. Hack, "Physics of amorphous silicon based alloy field-effect transistors," *Journal of Applied Physics,* vol. 55, pp. 3831-3842, 1984.

[7] S. Sherman, S. Wagner, and R. A. Gottscho, "Correlation between the valence- and conduction-band-tail energies in hydrogenated amorphous silicon," *Applied Physics Letters,* vol. 69, pp. 3242-3244, Nov 18 1996.

[8] Z. Jarzębski, *Oxide semiconductors* vol. 4: Pergamon, 1973.

[9] S. Narushima, M. Orita, M. Hirano, and H. Hosono, "Electronic structure and transport properties in the transparent amorphous oxide semiconductor 2 $CdO{\cdot}GeO_2$," *Physical Review B,* vol. 66, pp. 035203, June 2002.

[10] M. Orita, H. Ohta, M. Hirano, S. Narushima, and H. Hosono, "Amorphous transparent conductive oxide $InGaO_3(ZnO)_m$ ($m \leq 4$): A Zn 4s conductor," *Philosophical Magazine B,* vol. 81, pp. 501-515, 2001.

[11] H. Hosono, N. Kikuchi, N. Ueda, and H. Kawazoe, "Working hypothesis to explore novel wide band gap electrically conducting amorphous oxides and examples," *Journal of Non-Crystal Solids,* vol. 198, pp. 165-169, May 1996.

[12] N. F. Mott, "Silicon dioxide and the chalcogenide semiconductors; similarities and differences," *Advances in Physics,* vol. 26, pp. 363-391, Jan 1977.

[13] K. Mukae, K. Tsuda, and I. Nagasawa, "Capacitance-vs-voltage characteristics of ZnO varistors," *Journal of Applied Physics,* vol. 50, pp. 4475-4476, 1979.

[14] D. M. Bagnall, Y. F. Chen, Z. Zhu, T. Yao, S. Koyama, M. Y. Shen, *et al.*, "Optically pumped lasing of ZnO at room temperature," *Applied Physics Letters,* vol. 70, pp. 2230-2232, Apr 28 1997.

[15] U. Ozgur, Y. I. Alivov, C. Liu, A. Teke, M. A. Reshchikov, S. Dogan, *et al.*, "A comprehensive review of ZnO materials and devices," *Journal of Applied Physics,* vol. 98, Aug 15 2005.

[16] T. P. Chow and R. Tyagi, "Wide bandgap compound semiconductors for superior high-voltage unipolar power devices," *IEEE Transactions on Electron Devices,* vol. 41, pp. 1481-1483, Aug 1994.

[17] D. C. Look, "Recent advances in ZnO materials and devices," *Materials Science and Engineering B-Solid State Materials for Advanced Technology,* vol. 80, pp. 383-387, Mar 22 2001.

[18] Y. Liu, C. R. Gorla, S. Liang, N. Emanetoglu, Y. Lu, H. Shen, *et al.*, "Ultraviolet detectors based on epitaxial ZnO films grown by MOCVD," *Journal of Electronic Materials,* vol. 29, pp. 69-74, Jan 2000.

[19] E. M. Kaidashev, M. Lorenz, H. von Wenckstern, A. Rahm, H. C. Semmelhack, K. H. Han, *et al.*, "High electron mobility of epitaxial ZnO thin films on c-plane sapphire grown by multistep pulsed-laser deposition," *Applied Physics Letters,* vol. 82, pp. 3901-3903, Jun 2 2003.

[20] M. Ohyama, H. Kozuka, and T. Yoko, "Sol-gel preparation of ZnO films with extremely preferred orientation along (002) plane from zinc acetate solution," *Thin Solid Films,* vol. 306, pp. 78-85, Aug 28 1997.

[21] H. Yabuta, M. Sano, K. Abe, T. Aiba, T. Den, H. Kumomi, *et al.*, "High-mobility thin-film transistor with amorphous $InGaZnO_4$ channel fabricated by room temperature rf-magnetron sputtering," *Applied Physics Letters,* vol. 89, Sep 11 2006.

[22] R. Martins, P. Barquinha, I. Ferreira, L. Pereira, G. Goncalves, and E. Fortunato, "Role of order and disorder on the electronic performances of oxide semiconductor thin film transistors," *Journal of Applied Physics,* vol. 101, Feb 15 2007.

[23] J. F. Wager, "Flat-panel-display backplanes: LTPS or IGZO for AMLCDs or AMOLED displays?," *Info. Display,* vol. 30, pp. 26-29, 2014.

[24] S.-H. K. Park, J. W. Kim, M. Ryu, I. Y. Eom, J.-E. Pi, O. Kwon, *et al.*, "Invited paper: High mobility oxide tft for large area high resolution amoled," *SID Symposium Digest of Technical Papers,* vol. 44, pp. 18-21, 2013.

[25] J. H. Lee, D. H. Kim, D. J. Yang, S. Y. Hong, K. S. Yoon, P. S. Hong, *et al.*, "World's largest (15-inch) XGA AMLCD panel using IGZO oxide tft," in *2008 SID International Symposium*, 2008, pp. 625-628.

[26] A. M. Shevjakov, G. N. Kuznetsova, and V. B. Aleskovskii, "Interaction of titanium and germanium tetrachlorides with hydrated silica " in *Chemistry of high temperature materials. Proceedings of 2nd USSR conference on high temperature chemistry of oxides*, Nauka, Leningrad, USSR, 1967, pp. 162-168.

[27] J. W. Elam, D. Routkevitch, P. P. Mardilovich, and S. M. George, "Conformal coating on ultrahigh-aspect-ratio nanopores of anodic alumina by atomic layer deposition," *Chemistry of Materials*, vol. 15, pp. 3507-3517, Sep 9 2003.

[28] M. Vehkamaki, T. Hatanpaa, M. Kemell, M. Ritala, and M. Leskelaa, "Atomic layer deposition of ferroelectric bismuth titanate $Bi_4Ti_3O_{12}$ thin films," *Chemistry of Materials*, vol. 18, pp. 3883-3888, Aug 8 2006.

[29] H. Kim, "Atomic layer deposition of metal and nitride thin films: Current research efforts and applications for semiconductor device processing," *Journal of Vacuum Science & Technology B*, vol. 21, pp. 2231-2261, Nov-Dec 2003.

[30] D. A. Mourey, D. A. L. Zhao, J. Sun, and T. N. Jackson, "Fast peald ZnO thin-film transistor circuits," *IEEE Transactions on Electron Devices*, vol. 57, pp. 530-534, Feb 2010.

[31] H. B. Profijt, S. E. Potts, M. C. M. van de Sanden, and W. M. M. Kessels, "Plasma-assisted atomic layer deposition: Basics, opportunities, and challenges," *Journal of Vacuum Science & Technology A*, vol. 29, Sep 2011.

[32] K. Mistry, C. Allen, C. Auth, B. Beattie, D. Bergstrom, M. Bost, *et al.*, "A 45nm logic technology with high-k plus metal gate transistors, strained silicon, 9 Cu interconnect layers, 193nm dry patterning, and 100% Pb-free packaging," in *2007 IEEE International Electron Devices Meeting, Vols 1 and 2*, 2007, pp. 247-250.

[33] P. Poodt, D. C. Cameron, E. Dickey, S. M. George, V. Kuznetsov, G. N. Parsons, *et al.*, "Spatial atomic layer deposition: A route towards further industrialization of atomic layer deposition," *Journal of Vacuum Science & Technology A*, vol. 30, Jan 2012.

[34] A. Ali, H. S. Madan, A. P. Kirk, D. A. Zhao, D. A. Mourey, M. K. Hudait, *et al.*, "Fermi level unpinning of GaSb (100) using plasma enhanced atomic layer deposition of Al_2O_3," *Applied Physics Letters*, vol. 97, Oct 4 2010.

[35] S. X. Lao, R. M. Martin, and J. P. Chang, "Plasma enhanced atomic layer deposition of HfO_2 and ZrO_2 high-k thin films," *Journal of Vacuum Science & Technology A*, vol. 23, pp. 488-496, 2005.

[36] S. M. George, "Atomic layer deposition: An overview," *Chemical Reviews,* vol. 110, pp. 111-131, Jan 2010.

[37] K. Doering, C. J. Galewski, P. N. Gadgil, and T. E. Seidel, "Processing chamber for atomic layer deposition processes," ed: Google Patents, 2001.

[38] R. L. Puurunen, "Surface chemistry of atomic layer deposition: A case study for the trimethylaluminum/water process," *Journal of Applied Physics,* vol. 97, pp. 121301, Jun 15 2005.

[39] M. D. Groner, F. H. Fabreguette, J. W. Elam, and S. M. George, "Low-temperature Al_2O_3 atomic layer deposition," *Chemistry of Materials,* vol. 16, pp. 639-645, Feb 24 2004.

[40] I. H. Malitson, "Refraction and dispersion of synthetic sapphire," *Journal of the Optical Society of America,* vol. 52, pp. 1377, 1962.

[41] J. Koo, S. Kim, S. Jeon, H. Jeon, Y. Kim, and Y. Won, "Characteristics of Al_2O_3 thin films deposited using dimethylaluminum isopropoxide and trimethylaluminum precursors by the plasma-enhanced atomic-layer deposition method," *Journal of the Korean Physical Society,* vol. 48, pp. 131-136, Jan 2006.

[42] Y.-C. Liu, "Experimentally calibrated simulation of zno thin film transistors including traps," Ph.D. dissertation, Pennsylvania State University, University Park, Pa., 2014.

[43] D. A. Mourey, M. S. Burberry, D. A. Zhao, Y. V. Li, S. F. Nelson, L. Tutt, *et al.*, "Passivation of ZnO TFTs," *Journal Society Information Display,* vol. 18, pp. 753-761, Oct 2010.

[44] M. J. Brett and R. R. Parsons, "Structural properties of non-stoichiometric zinc oxide films," *Journal of Materials Science,* vol. 22, pp. 3611-3614, 1987/10/01 1987.

[45] S. N. Bai and T. Y. Tseng, "The effect of grain-boundaries on the electrical-properties of zinc oxide-based varistor," *Journal of Electronic Materials,* vol. 21, pp. 1073-1079, Nov 1992.

[46] Y. Y. V. Li, K. G. Sun, J. I. Ramirez, and T. N. Jackson, "Trilayer ZnO thin-film transistors with in situ al2o3 passivation," *IEEE Electron Device Letters,* vol. 34, pp. 1400-1402, Nov 2013.

[47] K. Nomura, T. Kamiya, and H. Hosono, "Highly stable amorphous In-Ga-Zn-O thin-film transistors produced by eliminating deep subgap defects," *Applied Physics Letters,* vol. 99, Aug 1 2011.

[48] K. Nomura, T. Kamiya, and H. Hosono, "Stability and high-frequency operation of amorphous in–ga–zn–o thin-film transistors with various passivation layers," *Thin Solid Films,* vol. 520, pp. 3778-3782, 2012.

[49] H. M. Smith and A. F. Turner, "Vacuum deposited thin films using a ruby laser," *Applied Optics,* vol. 4, pp. 147, 1965.

[50] D. B. Chrisey, A. Pique, R. A. McGill, J. S. Horwitz, B. R. Ringeisen, D. M. Bubb, *et al.*, "Laser deposition of polymer and biomaterial films," *Chemical Reviews,* vol. 103, pp. 553-576, Feb 2003.

[51] R. Eason, *Pulsed laser deposition of thin films : Applications-led growth of functional materials*. Hoboken, N.J.: Wiley-Interscience, 2007.

[52] P. K. Shin, Y. Aya, T. Ikegami, and K. Ebihara, "Application of pulsed laser deposited zinc oxide films to thin film transistor device," *Thin Solid Films,* vol. 516, pp. 3767-3771, Apr 30 2008.

[53] S. Masuda, K. Kitamura, Y. Okumura, S. Miyatake, H. Tabata, and T. Kawai, "Transparent thin film transistors using ZnO as an active channel layer and their electrical properties," *Journal of Applied Physics,* vol. 93, pp. 1624-1630, Feb 1 2003.

[54] B. Bayraktaroglu, K. Leedy, and R. Neidhard, "Microwave ZnO thin-film transistors," *IEEE Electron Device Letters,* vol. 29, pp. 1024-1026, Sept. 2008.

[55] C. G. Van de Walle, "Hydrogen as a cause of doping in zinc oxide," *Physical Review Letters,* vol. 85, pp. 1012-1015, Jul 31 2000.

[56] A. K. Singh, *Advanced x-ray techniques in research and industry*: IOS Press, 2005.

[57] F. M. Hossain, J. Nishii, S. Takagi, A. Ohtomo, T. Fukumura, H. Fujioka, *et al.*, "Modeling and simulation of polycrystalline zno thin-film transistors," *Journal of Applied Physics,* vol. 94, pp. 7768-7777, Dec 15 2003.

[58] T. Kamiya, K. Nomura, and H. Hosono, "Present status of amorphous In–Ga–Zn–O thin-film transistors," *Science and Technology of Advanced Materials,* vol. 11, p. 044305, 2010.

[59] T. Kamiya, K. Nomura, and H. Hosono, "Electronic structures above mobility edges in crystalline and amorphous In-Ga-Zn-O: Percolation conduction examined by analytical model," *Journal of Display Technology,* vol. 5, pp. 462-467, Dec 2009.

[60] D. Adler, L. P. Flora, and S. D. Senturia, "Electrical conductivity in disordered systems," *Solid State Communications,* vol. 12, pp. 9-12, 1973.

[61] E. H. Lee, A. Indluru, D. R. Allee, L. T. Clark, K. E. Holbert, and T. L. Alford, "Effects of gamma irradiation and electrical stress on a-Si:H thin-film transistors for flexible electronics and displays," *J. Display Technol.,* vol. 7, pp. 325-329, June 2011.

[62] L. Zhou, T. N. Jackson, E. Brandon, and W. West, "Flexible substrate a-Si: H tfts for space applications," in *Device Research Conference, 2004. 62nd DRC Conference Digest*, 2004, pp. 123-124.

[63] V. Davidovic, D. N. Kouvatsos, N. Stojadinovic, and A. T. Voutsas, "Influence of polysilicon film thickness on radiation response of advanced excimer laser annealed polycrystalline silicon thin film transistors," *Microelectronics Reliability*, vol. 47, pp. 1841-1845, Sep-Nov. 2007.

[64] Y. Liu, W.-J. Wu, Y.-F. En, L. Wang, Z.-F. Lei, and X.-H. Wang, "Total dose ionizing radiation effects in the indium-zinc oxide thin-film transistors," *IEEE Electron Device Letters*, vol. 35, pp. 369-371, Mar. 2014.

[65] A. Indluru, K. Holbert, and T. Alford, "Gamma radiation effects on indium-zinc oxide thin-film transistors," *Thin Solid Films*, vol. 539, pp. 342-344, July 2013.

[66] W. Vehse, W. Sibley, F. Keller, and Y. Chen, "Radiation damage in ZnO single crystals," *Physical Review Letters*, vol. 167, p. 828, Mar. 1968.

[67] D. C. Look, D. Reynolds, J. W. Hemsky, R. Jones, and J. Sizelove, "Production and annealing of electron irradiation damage in ZnO," *Applied Physics Letters*, vol. 75, pp. 811-813, 1999.

[68] V. Ferlet-Cavrois, O. Musseau, J. L. Leray, J. L. Pelloie, and C. Raynaud, "Total dose effects on a fully-depleted soi nmosfet and its lateral parasitic transistor," *IEEE Transactions on Electron Devices*, vol. 44, pp. 965-971, June 1997.

[69] B. Bayraktaroglu, K. Leedy, and R. Neidhard, "Nanocrystalline ZnO microwave thin film transistors," in *Proc. SPIE 7679, Micro- and Nanotechnology Sensors, Systems, and Applications II*, 2010, pp. 767904-1-12.

[70] A. Ortiz-Conde, A. Cerdeira, M. Estrada, F. J. García Sánchez, and R. Quintero, "A simple procedure to extract the threshold voltage of amorphous thin film MOSFETs in the saturation region," *Solid State Electronics*, vol. 45, pp. 663-667, May 2001.

[71] X. Xu, J. Yang, A. Banerjee, S. Guha, K. Vasanth, and S. Wagner, "Band-edge discontinuities between microcrystalline and amorphous hydrogenated silicon alloys and their effect on solar-cell performance," *Applied Physics Letters*, vol. 67, pp. 2323-2325, Oct. 1995.

[72] T. Kamiya, K. Nomura, and H. Hosono, "Origins of high mobility and low operation voltage of amorphous oxide TFTs: Electronic structure, electron transport, defects and doping," *Journal of Display Technology*, vol. 5, pp. 468-483, July 2009.

[73] J. J. Siddiqui, J. D. Phillips, K. Leedy, and B. Bayraktaroglu, "Bias-temperature-stress characteristics of ZnO/HfO_2 thin-film transistors," *IEEE Transactions on Electron Devices*, vol. 59, pp. 1488-1493, May 2012.

[74] Z. I. Kertesz and G. F. Parsons, "Ozone formation in air exposed to cobalt-60 gamma radiation," *Science,* vol. 142, pp. 1289-1290, 1963.

[75] J. W. Broxon and G. T. Merideth, "Measurements of gamma-ray ionization currents in air at high pressures and high gradients," *Physical Review Letters,* vol. 54, pp. 1-9, 1938.

[76] P. S. Winokur, H. E. Boesch, J. M. McGarrity, and F. B. McLean, "Field- and time-dependent radiation effects at the SiO_2/Si interface of hardened mos capacitors," *IEEE Transactions Nuclear Science,* vol. 24, pp. 2113-2118, Dec. 1977.

[77] D. M. Fleetwood, "Total ionizing dose effects in MOS and low-dose-rate-sensitive linear-bipolar devices," *IEEE Transactions Nuclear Science,* vol. 60, pp. 1706-1730, June 2013.

[78] E. H. Lee, A. Indluru, D. R. Allee, L. T. Clark, K. E. Holbert, and T. L. Alford, "Effects of gamma irradiation and electrical stress on a-si:H thin-film transistors for flexible electronics and displays," *Journal of Display Technology,* vol. 7, pp. 325-329, Jun 2011.

[79] A. Wung, R. V. Park, K. J. Rebello, and G. K. Fedder, "Tri-axial high-G CMOS-MEMs capacitive accelerometer array," in *MEMS 2008: 21st IEEE International Conference on Micro Electro Mechanical Systems, Technical Digest,* 2008, pp. 876-879.

[80] C. T. Shelton, P. G. Kotula, G. L. Brennecka, P. G. Lam, K. E. Meyer, J. P. Maria, *et al.*, "Chemically homogeneous complex oxide thin films via improved substrate metallization," *Advanced Functional Materials,* vol. 22, pp. 2295-2302, Jun 6 2012.

[81] R. E. Jones and S. B. Desu, "Process integration for nonvolatile ferroelectric: Memory fabrication," *MRS Bulletin,* vol. 21, pp. 55-58, Jun 1996.

[82] K. Rho, S. Zurn, D. Markus, and D. L. Polla, "Integration of a CMOS preamplifier with a lead zirconate titanate resonant frequency microsensor," *Journal of the Electrochemical Society,* vol. 149, pp. J53-J57, Jul 2002.

[83] E. E. Aktakka, R. L. Peterson, and K. Najafi, "A CMOS-compatible piezoelectric vibration energy scavenger based on the integration of bulk PZT films on silicon," *2010 International Electron Devices Meeting - Technical Digest,* 2010.

[84] T. Rogers and J. Kowal, "Selection of glass, anodic bonding conditions and material compatibility for silicon-glass capacitive sensors," *Sensors and Actuators A: Physical,* vol. 46, pp. 113-120, Jan 1995.

[85] P. Ramm, J. J. Q. Lu, and M. M. V. Taklo, *Handbook of wafer bonding*: Wiley, 2011.

[86] W. P. Maszara, G. Goetz, A. Caviglia, and J. B. Mckitterick, "Bonding of silicon-wafers for silicon-on-insulator," *Journal of Applied Physics,* vol. 64, pp. 4943-4950, Nov 15 1988.

[87] A. Tombak, J. P. Maria, F. T. Ayguavives, Z. Jin, G. T. Stauf, A. I. Kingon, *et al.*, "Voltage-controlled RF filters employing thin-film barium-strontium-titanate tunable capacitors," *IEEE Transactions on Microwave Theory and Techniques,* vol. 51, pp. 462-467, Feb 2003.

[88] T. Ayguavives, A. Tombak, J. P. Maria, G. T. Stauf, C. Ragaglia, J. Roeder, *et al.*, "Physical properties of (Ba,Sr)TiO_3 thin films used for integrated capacitors in microwave applications," *Proceedings of the 2001 12th IEEE International Symposium on Applications of Ferroelectrics, Vols I and II,* pp. 365-368, 2001.

[89] J. Nath, D. Ghosh, J. P. Maria, A. I. Kingon, W. Fathelbab, P. D. Franzon, *et al.*, "An electronically tunable microstrip bandpass filter using thin-film barium-strontium-titanate (BST) varactors," *IEEE Transactions on Microwave Theory and Techniques,* vol. 53, pp. 2707-2712, Sep 2005.

[90] T. M. H. Lee, I. M. Hsing, and C. Y. N. Liaw, "An improved anodic bonding process using pulsed voltage technique," *Journal of Microelectromechanical Systems,* vol. 9, pp. 469-473, 2000.

[91] V. Haridasan, P. G. Lam, Z. Feng, W. M. Fathelbab, J. P. Maria, A. I. Kingon, *et al.*, "Tunable ferroelectric microwave bandpass filters optimised for system-level integration," *Microwaves, Antennas & Propagation, IET,* vol. 5, pp. 1234-1241, 2011.

[92] H. Sato, T. Minami, T. Miyata, S. Takata, and M. Ishii, "Transparent conducting ZnO thin-films prepared on low-temperature substrates by chemical-vapor-deposition using $Zn(C_5H_7O_2)_2$," *Thin Solid Films,* vol. 246, pp. 65-70, Jun 15 1994.

[93] J. W. Elam and S. M. George, "Growth of ZnO/Al_2O_3 alloy films using atomic layer deposition techniques," *Chemistry of Materials,* vol. 15, pp. 1020-1028, Feb 25 2003.

[94] H. T. Shen, Y. W. Yu, X. Wang, J. I. Ramirez, Y. Y. V. Li, Y. Ke, *et al.*, "Effect of c-Si doping density on heterojunction with intrinsic thin layer (HIT) radial junction solar cells," in *2013 IEEE 39th Photovoltaic Specialists Conference (PVSC)*, 2013, pp. 2466-2469.

[95] D. J. Lee, H. M. Kim, J. Y. Kwon, H. Choi, S. H. Kim, and K. B. Kim, "Structural and electrical properties of atomic layer deposited Al-doped ZnO films," *Advanced Functional Materials,* vol. 21, pp. 448-455, Feb 8 2011.

[96] S. Kwon, S. Bang, S. Lee, S. Jeon, W. Jeong, H. Kim, *et al.*, "Characteristics of the ZnO thin film transistor by atomic layer deposition at various temperatures," *Semiconductor Science and Technology,* vol. 24, Mar 2009.

[97] S. J. Gross, S. Tadigadapa, T. N. Jackson, S. Trolier-McKinstry, and Q. Q. Zhang, "Lead-zirconate-titanate-based piezoelectric micromachined switch," *Applied Physics Letters,* vol. 83, pp. 174-176, Jul 7 2003.

[98] F. F. C. Duval, R. A. Dorey, R. W. Wright, Z. R. Huang, and R. W. Whatmore, "Fabrication and modeling of high-frequency PZT composite thick film membrane resonators," *IEEE Transactions on Ultrasonics Ferroelectrics and Frequency Control,* vol. 51, pp. 1255-1261, Oct 2004.

[99] D. Shen, J. H. Park, J. Ajitsaria, S. Y. Choe, H. C. Wikle, and D. J. Kim, "The design, fabrication and evaluation of a mems pzt cantilever with an integrated Si proof mass for vibration energy harvesting," *Journal of Micromechanics and Microengineering,* vol. 18, May 2008.

[100] S. Trolier-McKinstry and P. Muralt, "Thin film piezoelectrics for MEMs," *Journal of Electroceramics,* vol. 12, pp. 7-17, Jan-Mar 2004.

[101] B. Jaffe, H. L. C. Jaffé, and W. R. Cook, *Piezoelectric ceramics,* 1971.

[102] F. Xu, S. Trolier-McKinstry, W. Ren, B. Xu, Z.-L. Xie, and K. J. Hemker, "Domain wall motion and its contribution to the dielectric and piezoelectric properties of lead zirconate titanate films," *Journal of Applied Physics,* vol. 89, pp. 1336-1348, 2001.

[103] S. K. Dey, K. D. Budd, and D. A. Payne, "Thin-film ferroelectrics of PZT by sol-gel processing," *IEEE Transactions on Ultrasonics Ferroelectrics and Frequency Control,* vol. 35, pp. 80-81, Jan 1988.

[104] F. Chu, F. Xu, J. Shepard, and S. Trolier-McKinstry, "Thickness dependence of the electrical properties of sol-gel derived lead zirconate titanate thin films with (111) and (100) texture," *MRS Proceedings,* vol. 493, pp. 409-414, 1998.

[105] Y. Sekine, K. Furutani, Y. Shionoiri, K. Kato, J. Koyama, and S. Yamazaki, "Success in measurement the lowest off-state current of transistor in the world," in *2011 International Conference on Semiconductor Technology for Ultra Large Scale Integrated Circuits and Thin Film Transistors* 2011, pp. 77-88.

[106] D. A. Schwartz, R. Allured, J. A. Bookbinder, V. Cotroneo, W. R. Forman, M. D. Freeman, *et al.*, "Technology requirements for a square meter, arcsecond resolution telescope for x-rays: The SMART-X mission," in *SPIE Optical Engineering+ Applications,* 2014, pp. 920806-920806-8.

[107] J. M. Beckers, "Adaptive optics for astronomy: Principles, performance, and applications," *Annual Review of Astronomy and Astrophysics,* vol. 31, pp. 13-62, 1993.

[108] M. J. Booth, *Adaptive optics in microscopy* vol. 365, 2007.

[109] P. Godara, A. M. Dubis, A. Roorda, J. L. Duncan, and J. Carroll, "Adaptive optics retinal imaging: Emerging clinical applications," *Optometry and Vision Science,* vol. 87, pp. 930-941, Dec 2010.

[110] The Chandra X-Ray Center (CX) (July 10th). *About chandra*. Available: http://cxc.harvard.edu/cdo/about_chandra/

[111] D. A. Schwartz, R. Allured, J. A. Bookbinder, V. Cotroneo, W. R. Forman, M. D. Freeman, *et al.*, "Technology requirements for a square meter, arcsecond resolution telescope for X-rays: The SMART-X mission," 2014, pp. 920806-920806-8.

[112] V. Cotroneo, W. N. Davis, V. Marquez, P. B. Reid, D. A. Schwartz, R. L. Johnson-Wilke, *et al.*, "Adjustable grazing incidence X-ray optics based on thin PZT films," in *Adaptive X-Ray Optics II*, 2012.

[113] V. Cotroneo, W. N. Davis, V. Marquez, P. B. Reid, S. McMuldroch, J.-W. R. L., *et al.*, "Deformable mirrors enable a leap forward in X-ray telescope performance," *SPIE Newsroom*, January 2013.

[114] R. L. Johnson-Wilke, R. H. T. Wilke, M. Wallace, J. I. Ramirez, Z. Prieskorn, J. Nikoleyczik, *et al.*, "ZnO thin film transistors and electronic connections for adjustable X-ray mirrors: SMART-x telescope," in *Adaptive X-Ray Optics III*, 2014.

[115] R. H. T. Wilke, R. L. Johnson-Wilke, V. Cotroneo, S. McMuldroch, P. B. Reid, D. A. Schwartz, *et al.*, "Fabrication of adjustable cylindrical mirror segments for the SMART-X telescope," *IEEE Transactions on Ultrasonics Ferroelectrics and Frequency Control*, vol. 61, pp. 1386-1392, Aug 2014.

[116] D. L. Zhao, D. A. Mourey, and T. N. Jackson, "Fast flexible plastic substrate ZnO circuits," *IEEE Electron Device Letters*, vol. 31, pp. 323-325, Apr 2010.

[117] H. Y. U. Li and T. N. Jackson, "Oxide semiconductor thin film transistors on thin solution-cast flexible substrates," *IEEE Electron Device Letters*, vol. 36, pp. 35-37, Jan 2015.

[118] G. Korotcenkov, "Metal oxides for solid-state gas sensors: What determines our choice?," *Materials Science and Engineering: B*, vol. 139, pp. 1-23, 4/25/ 2007.

[119] H. Meixner, J. Gerblinger, U. Lampe, and M. Fleischer, "Thin-film gas sensors based on semiconducting metal oxides," *Sensors and Actuators B: Chemical*, vol. 23, pp. 119-125, 2// 1995.

[120] M. Bender, E. Fortunato, P. Nunes, I. Ferreira, A. Marques, R. Martins, *et al.*, "Highly sensitive ZnO ozone detectors at room temperature," *Japanese Journal of Applied Physics Part 2-Letters & Express Letters*, vol. 42, pp. L435-L437, Apr 15 2003.

[121] R. Martins, E. Fortunato, P. Nunes, I. Ferreira, A. Marques, M. Bender, *et al.*, "Zinc oxide as an ozone sensor," *Journal of Applied Physics*, vol. 96, pp. 1398-1408, Aug 1 2004.

[122] G. Eranna, B. C. Joshi, D. P. Runthala, and R. P. Gupta, "Oxide materials for development of integrated gas sensors - a comprehensive review," *Critical Reviews in Solid State and Materials Sciences,* vol. 29, pp. 111-188, 2004.

[123] Y. Shimizu and M. Egashira, "Basic aspects and challenges of semiconductor gas sensors," *MRS Bulletin,* vol. 24, pp. 18-24, 1999.

[124] E. McAdams, A. Krupaviciute, C. Gehin, E. Grenier, B. Massot, A. Dittmar, *et al.*, "Wearable sensor systems: The challenges," in *Engineering in Medicine and Biology Society, EMBC, 2011 Annual International Conference of the IEEE*, 2011, pp. 3648-3651.

[125] S. Choi, N. Kim, H. Cha, and R. Ha, "Micro sensor node for air pollutant monitoring: Hardware and software issues," *Sensors,* vol. 9, pp. 7970-7987, 2009.

[126] H. G. Yeo, C. Yeager, X. Ma, J. I. Ramirez, K. G. Sun, C. Rahn, *et al.*, "Piezoelectric MEMs energy harvesters," in *ASME 2014 Conference on Smart Materials, Adaptive Structures and Intelligent Systems*, 2014, pp. V002T02A019-V002T02A019.

[127] P. Gründler and SpringerLink (Online service), *Chemical sensors : An introduction for scientists and engineers*. Berlin ; New York: Springer, 2007.

[128] L. Torsi, A. Dodabalapur, L. Sabbatini, and P. G. Zambonin, "Multi-parameter gas sensors based on organic thin-film-transistors," *Sensors and Actuators B: Chemical,* vol. 67, pp. 312-316, 9/1/ 2000.

[129] Q. H. Li, Y. X. Liang, Q. Wan, and T. H. Wang, "Oxygen sensing characteristics of individual ZnO nanowire transistors," *Applied Physics Letters,* vol. 85, pp. 6389-6391, Dec 27 2004.

[130] J. I. Ramirez, Y. V. Li, H. Basantani, and T. N. Jackson, "Effects of gamma-ray irradiation and electrical stress on ZnO thin film transistors," in *Device Research Conference, 2013. 71st DRC Conference Digest*, 2013, pp. 171-172.

[131] K. G. Sun, Y. V. Li, D. B. Saint John, and T. N. Jackson, "Ph-controlled selective etching of Al_2O_3 over zno," *ACS Applied Materials & Interfaces,* vol. 6, pp. 7028-7031, 2014.

[132] J. D. Prades, R. Jimenez-Diaz, F. Hernandez-Ramirez, S. Barth, A. Cirera, A. Romano-Rodriguez, *et al.*, "Ultralow power consumption gas sensors based on self-heated individual nanowires," *Applied Physics Letters,* vol. 93, p. 123110, 2008.

[133] S. Bang, S. Lee, J. Park, S. Park, Y. Ko, C. Choi, *et al.*, "The effects of post-annealing on the performance of ZnO thin film transistors," *Thin Solid Films,* vol. 519, pp. 8109-8113, Sep 1 2011.

[134] W.-T. Chen, L. Shih-Yi, K. Shih-Chin, Z. Hsiao-Wen, T. Chuang-Chuang, L. Jian-Hong, *et al.*, "Oxygen-dependent instability and annealing/passivation effects in amorphous In-

Ga-Zn-O thin-film transistors," *IEEE Electron Device Letters,* vol. 32, pp. 1552-1554, 2011.

[135] T. Hiramatsu, M. Furuta, H. Furuta, T. Matsuda, and T. Hirao, "Influence of thermal annealing on microstructures of zinc oxide films deposited by RF magnetron sputtering," *Japanese Journal of Applied Physics Part 1,* vol. 46, pp. 3319-3323, Jun 2007.

[136] G. Z. Xing, B. Yao, C. X. Cong, T. Yang, Y. P. Xie, B. H. Li, *et al.*, "Effect of annealing on conductivity behavior of undoped zinc oxide prepared by RF magnetron sputtering," *Journal of Alloys and Compounds,* vol. 457, pp. 36-41, Jun 12 2008.

[137] H. S. Kang, J. S. Kang, J. W. Kim, and S. Y. Lee, "Annealing effect on the property of ultraviolet and green emissions of ZnO thin films," *Journal of Applied Physics,* vol. 95, pp. 1246-1250, Feb 1 2004.

[138] J. S. Park, J. K. Jeong, Y. G. Mo, H. D. Kim, and S. I. Kim, "Improvements in the device characteristics of amorphous indium gallium zinc oxide thin-film transistors by ar plasma treatment," *Applied Physics Letters,* vol. 90, Jun 25 2007.

[139] Y. Ya-Hui, S. S. Yang, and C. Kan-Sen, "Characteristic enhancement of solution-processed In-Ga-Zn oxide thin-film transistors by laser annealing," *IEEE Electron Device Letters,* vol. 31, pp. 969-971, 2010.

[140] S. T. Meyers, J. T. Anderson, C. M. Hung, J. Thompson, J. F. Wager, and D. A. Keszler, "Aqueous inorganic inks for low-temperature fabrication of ZnO TFTs," *Journal of the American Chemical Society,* vol. 130, pp. 17603-17609, Dec 24 2008.

[141] R. G. Singh, F. Singh, V. Kumar, and R. M. Mehra, "Growth kinetics of ZnO nanocrystallites: Structural, optical and photoluminescence properties tuned by thermal annealing," *Current Applied Physics,* vol. 11, pp. 624-630, May 2011.

[142] S. T. Shishiyanu, T. S. Shishiyanu, and O. I. Lupan, "Sensing characteristics of tin-doped ZnO thin films as NO_2 gas sensor," *Sensors and Actuators B: Chemical,* vol. 107, pp. 379-386, May 27 2005.

[143] Y. S. Kim, S. C. Ha, K. Kim, H. Yang, S. Y. Choi, Y. T. Kim, *et al.*, "Room-temperature semiconductor gas sensor based on nonstoichiometric tungsten oxide nanorod film," *Applied Physics Letters,* vol. 86, May 23 2005.

[144] L. Valentini, I. Armentano, J. M. Kenny, C. Cantalini, L. Lozzi, and S. Santucci, "Sensors for sub-ppm NO_2 gas detection based on carbon nanotube thin films," *Applied Physics Letters,* vol. 82, pp. 961-963, Feb 10 2003.

[145] M. Bender, E. Gagaoudakis, E. Douloufakis, E. Natsakou, N. Katsarakis, V. Cimalla, *et al.*, "Production and characterization of zinc oxide thin films for room temperature ozone sensing," *Thin Solid Films,* vol. 418, pp. 45-50, Oct 1 2002.

[146] J. Brunet, A. Pauly, L. Mazet, J. P. Germain, M. Bouvet, and B. Malezieux, "Improvement in real time detection and selectivity of phthalocyanine gas sensors dedicated to oxidizing pollutants evaluation," *Thin Solid Films,* vol. 490, pp. 28-35, 10/21/ 2005.

[147] H. Bader and J. Hoigne, "Determination of ozone in water by the indigo method," *Water Research,* vol. 15, pp. 449-456, 1981.

[148] W. Ungier, M. Suffczynski, and J. Adamowski, "Phonon replicas of bound exciton recombination," *Solid-State Electronics,* vol. 21, pp. 1365-1367, 1978.

[149] T. N. Ng, W. S. Wong, M. L. Chabinyc, S. Sambandan, and R. A. Street, "Flexible image sensor array with bulk heterojunction organic photodiode," *Applied Physics Letters,* vol. 92, May 26 2008.

[150] K. J. Baeg, M. Binda, D. Natali, M. Caironi, and Y. Y. Noh, "Organic light detectors: Photodiodes and phototransistors," *Advanced Materials,* vol. 25, pp. 4267-4295, Aug 21 2013.

[151] D. A. Mourey, S. K. Park, D. L. A. Zhao, J. Sun, Y. Y. V. Li, S. Subramanian, *et al.*, "Fast, simple ZnO/organic CMOS integrated circuits," *Organic Electronics,* vol. 10, pp. 1632-1635, Dec 2009.

[152] Y. Y. V. Li, D. A. Mourey, M. A. Loth, D. L. A. Zhao, J. E. Anthony, and T. N. Jackson, "Hybrid inorganic/organic complementary circuits using PEALD ZnO and ink-jet printed dif-tesadt TFTs," *Organic Electronics,* vol. 14, pp. 2411-2417, Oct 2013.

[153] K. Arshak, A. Arshak, S. Zleetni, and O. Korostynska, "Thin and thick films of metal oxides and metal phthalocyanines as gamma radiation dosimeters," *Ieee Transactions on Nuclear Science,* vol. 51, pp. 2250-2255, Oct 2004.

[154] Y. Q. Qiu, J. V. Gigliotti, M. Wallace, F. Griggio, C. E. M. Demore, S. Cochran, *et al.*, "Piezoelectric micromachined ultrasound transducer (PMUT) arrays for integrated sensing, actuation and imaging," *Sensors,* vol. 15, pp. 8020-8041, Apr 2015.

[155] C. Yeager, "PZT thin films for piezoelectric mems mechanical energy harvesting," The Pennsylvania State University, 2015.

[156] K. G. Sun and T. N. Jackson, "Double-gate ZnO TFT active rectifier," in *Device Research Conference (DRC), 2014 72nd Annual*, 2014, pp. 269-270.

Vita

Jose Israel Ramirez

Ph.D. in Electrical Engineering **August 2015**

The Pennsylvania State University. University Park, PA.

Awards and Honors: Bunton-Waller Graduate Award 2009, Fred C. and M. Joanne Thompson Graduate Fellowship in Electrical Engineering 2010-2012, Corning Incorporated Fellowship 2010-2012, Luther B. and Patricia A. Brown Graduate Fellowship 2013, James R. and Barbara R. Palmer Fellowship in Electrical Engineering 2013, Graham Endowed Fellowship 2012-2015, Penn State Electrical Engineering Graduate Fellowship 2012-2014, Alfred P. Sloan MPHD Scholar 2014.

B.S. in Electrical Engineering **July 2009**

University of California, Riverside. Riverside, CA. July 2009

Thesis title: Design and development of Magneto Optical Kerr Effect Measurement Setup

NSF-IRES Research for Undergraduates (REU) at Tsinghua University and University of Electronics and Science of China UEST, Summer 2008.

Professional Activities:

Reviewer for Journal of the Society for Information Display, IEEE Transactions on Electron Devices, and Applied Physics Letters