The Pennsylvania State University

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ELECTRICAL CHARACTERIZATION OF GaN AND SiC SCHOTTKY DIODES/ NON MECHANICAL BEAM STEERING USING LIQUID CRYSTALS

A Thesis in

Electrical Engineering

by

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ABSTRACT

In this thesis we investigated the electrical characteristics of GaN schottky diodes fabricated on a commercial LED wafer using Inductively Coupled Plasma Reactive Ion etching (ICP-RIE) techniques. We also researched the characteristics of commercially available SiC schottky diodes. Two main electrical characterization techniques were used in the investigation of these diodes, Current - Voltage Characterization and Capacitance - Voltage Characterization. Using I-V characteristics the ideality and the Barrier height of the Schottky diode was determined and the C-V characteristics were used to calculate the doping concentration of the device. These measurements were done at room temperature as well as different temperatures ranging from 100K to 300K for GaN diodes and 133K to 433K for SiC diodes to observe the dependence of Barrier height and the Ideality factor on the temperature. It was concluded that for GaN the ideality factor decreases with the increase in temperature while the barrier height increases with increase in temperature. The values of barrier height for GaN at 120K is 0.44eV and at 300K it is 0.81eV and the ideality factor at 120K is 0.96 and at 300K it is 0.6. The carrier concentration of the SiC remains constant through the three regions while the carrier concentration of GaN device increases as the reverse bias increases. GaN diode was also measured at two different frequencies to observe if there is any change in the C-V profile and the profile was similar for the two frequencies.

Further this thesis comprises of a small novel device which is in the process of fabrication. It is a non-mechanical beam steerer which makes use of Liquid crystals to deviate a beam from its normal position. This thesis only includes the architecture used in the manufacturing of the device and the fabrication of a liquid crystal cell.

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Chapter 1
INTRODUCTION

The material semiconductor GaN (Gallium Nitride), SiC (Silicon Carbide) and other III-V semiconductors have gained importance since more than three decades and have been researched extensively. But only recently have they changed from materials of research interest to commercially important semiconductors. There are many studies of Schottky Contacts on GaN which have already been reported [1]–[5]. This is mainly due to their properties and exceptional robustness. The ability of the industry to grow high quality epitaxial layers on GaN / SiC has helped us fabricate these devices more conveniently. The large band gap of these materials, which extend from 0.7eV to 6.1eV, allow the realization of these heterostructures in various high-power, high-frequency and high-temperature electronic applications. The development of III-V nitride devices has enunciated the field of Light Emitting Diodes (LED) and Schottky Diodes. GaN a direct band gap III-V semiconductor with a band gap of 3.4eV makes it possible to emit blue (405nm) light without the use of non-linear optical frequency doubling [6]. Various structures have been proposed for the designs of Alternating Current LEDs for a low cost fabrication with high performance and quality of the device. These methods involve the use of different fabrication techniques like anti-parallel AC-LEDs, Wheatstone bridge circuit, and the separation growth of LED epitaxial layers and Schottky Barrier Diodes (SBDs). These fabrication techniques on different regions of the same substrate have been matured to overcome the problems of driving the LEDs with AC and also helped

achieve high breakdown voltage SBDs with high efficiency LEDs on the same wafer [7]–[13]. There are many groups who have paid a great deal of attention to the development of visible-blind ultraviolet (UV) detectors. These mainly involved the use of metal/GaN Schottky junctions [14]–[17].

However in order to realize the potential of these materials for a variety of high temperature , high frequency applications it is necessary to achieve a high quality thermally stable contact which should not worsen the device performance under extreme conditions of temperature and frequency. Generally a metal contact with a wide band gap semiconductor results in the formation of a rectifying contact. Achieving a good quality and a stable Schottky contact is a very intricate process.

In this thesis I present the characterization of GaN Schottky diodes which were fabricated on a commercial LED using ICP etching techniques and commercially available SiC Schottky diodes. The Capacitance-Voltage(C-V) and the Current-Voltage (I-V) characteristics of the Schottky barriers were investigated. Various techniques were used to determine the carrier concentration.

1.1 Thesis Overview

The work in this thesis describes the characterization of GaN Schottky diodes which were fabricated on a commercially available LED using ICP etching techniques and SiC Schottky diodes. I will also discuss the various techniques that were used to calculate the doping concentrations of the Schottky Diodes and also the effect of temperature on the various parameters of the diode.

CHAPTER 1 describes an overview of GaN and SiC devices, which includes the properties of these semiconductors, recent work and applications of Schottky Diodes.

CHAPTER 2 discusses the theory and operation of metal semiconductor contacts. It also deals with the definition of ohmic contacts.

CHAPTER 3 describes the fabrication methods used to integrate and fabricate a GaN Schottky diode on a commercially available LED, which mainly includes the experimental setup, etching procedures and the device design.

CHAPTER 4 discusses the characterization techniques used in calculating the doping concentrations and barrier height of the Schottky diodes.

CHAPTER 5 concludes the results obtained using various characterization techniques.

CHAPTER 6 includes a small deviation from characterization and involves a design of a non-mechanical beam steerer using liquid crystals.

CHAPTER 7 gives a brief summary of the thesis including the future prospects of this thesis work.

1.2 GaN and SiC semiconductor

The main reason to use GaN and SiC semiconductors is due to their ability to operate at high temperatures and the ability to deliver more power. GaN and its alloys has many advantages due to a wider range of bandgaps. Optoelectronic devices which are based on nitride as a ternary can operate at energies in mid-ultraviolet to all the way into infrared. The use of energy efficient blue LEDs in color displays makes them of prime importance in the optoelectronic industry. Due to a large discontinuity in AlGaN/ GaN interface it is possible to have an enhanced output power density and improved thermal

conductivity which helps these devices to operate effectively at higher temperature. This is due to the fact that the intrinsic carrier concentration of semiconductor materials decreases exponentially with temperature and hence wide band gap semiconductors can be intrinsic even over a wide range of temperatures. GaN has a high breakdown fields which makes it suitable for high power applications. The breakdown field of GaN is $3x10^6$ V/cm as compared to $3x10^5$ V/cm and $4x10^5$ V/cm for Silicon and Gallium Arsenide respectively [18]. The resonant tunneling diode which makes use of GaN is one of a notable device due to its Negative Differential Resistance.[19]

1.3 Applications of Schottky Diodes:

The Schottky diodes are used in various industries mainly as a diode rectifier, however their unique properties enable them to be used in variety of applications where normal diodes won't be able to provide a same level of performance.

- Light Emitting Diodes: Extensive research work and developments on III-V wide gap semiconductor resulted in commercial production of high power UV/green/blue light emitting diodes. Earlier this was not possible because the necessary color spectrum wasn't entirely covered by traditional semiconductors. It is expected that by 2030 this technology will replace the current technology and reduce the electricity consumption by 50%
- Bipolar Transistors: GaN technology also supports the fabrication of heterojunction bipolar transistors (HBT) which are primarily used in microwave devices. AlGaN/GaN

based heterostructures are reported to have good transconductance and saturation current

- RF Mixer and Detector Diode: The ability of faster switching has made Schottky diode viable to its own radio frequency applications. These applications mainly include high performance diode ring mixers and in addition to this the low turn on voltage, high frequency and low capacitance capability make them ideal RF detectors.
- Power Rectifiers: Due to low forward voltage drop and high current density these diodes are an ideal choice for high power applications over normal PN junction diodes. This in turn results in less dissipation of heat.

Chapter 2

Metal-Semiconductor Contacts

2.1 Introduction:

One of the critical components of semiconductor is the metal semiconductor contact, and it is very critical to have a good contact. Since there is a large mismatch between the Fermi levels of the metal and the semiconductor it can result in a high resistance rectifying contact, however an appropriate choice of materials can result in a low resistance Ohmic contact. An ideal metal semiconductor contact should have the following characteristics:

1. The metal and the semiconductor should be in intimate contact with each other i.e. there should not be any interfacial layer present in between the two materials.
2. There should not be any surface charges in between the metal and the semiconductor.
3. Metal and the semiconductor should not mix with each other.

So we can say that Metal Semiconductor contacts can either behave as Schottky barriers or Ohmic contacts.

Schottky barriers are the once which show rectifying characteristics i.e if we plot the I_V characteristics it is nonlinear when the external bias applied to the contact is changed. Whereas ohmic contacts are the ones which show a linear I-V behavior regardless of the polarity of the bias applied.

2.2 Schottky Barriers or Rectifying contacts:

Figure 2.1 shows an ideal energy band diagram of a metal and an n-type semiconductor before their contact. In quantifying the energy levels the vacuum level is used as a reference level. The parameter ϕm is the metal function generally measured in volts, the parameter ϕs is called as the semiconductor work function and χ is the electron affinity.

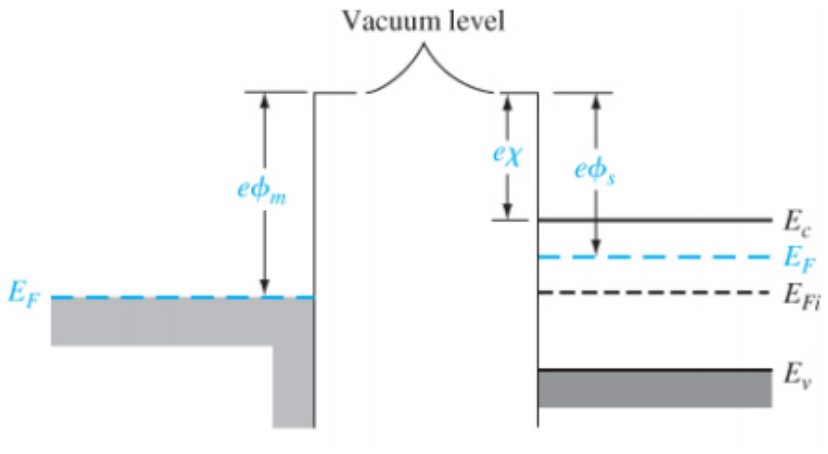

Figure 2.1: Energy band diagram of the metal semiconductor before contact is made [20]

Table 2.1 shows work functions of various metals are shown and table 2.2 shows the electron affinities of various semiconductors. In the first figure 2.2 we have assumed that the ϕm > ϕs, while the ideal metal semiconductor band diagram is shown in figure 2.1. We can see that before contact the Fermi level of the semiconductor was above the Fermi level of the metal. Now after the contact in order to get into equilibrium the electrons from the semiconductor flow into the lower energy states of the metal leaving behind positively charged donor atoms resulting in a space charge region (depletion region).

In the figure ϕBo is the ideal barrier height of the metal-semiconductor contact which can also be explained as the potential barrier seen by electrons in the semiconductor which try to move into a semiconductor.

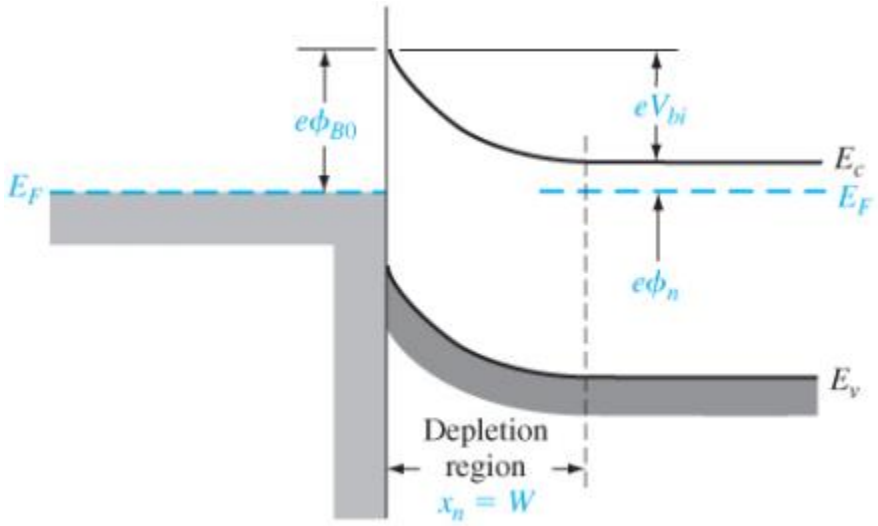

Figure 2.2: Ideal energy band diagram of metal-n-semiconductor junction for ϕm > ϕs[20]

Element	Work Function, ϕm (eV)
Ag, Silver	4.26
Al, Aluminum	4.28
Au, Gold	5.1
Cr, Chromium	4.5
Mo, Molybdenum	4.6
Ni, Nickel	5.15
Pd, Palladium	5.12
Pt, Platinum	5.65
Ti, Titanium	4.33
W, Tungsten	4.55

Table 2.1: Work Functions of different metals[20]

Element	Electron Affinity, χ (eV)
Ge, Germanium	4.13
Si, Silicon	4.01
GaAs, Gallium Arsenide	4.07
GaN, Gallium Nitride	4.01

Table 2.2: Electron Affinities of a few Semiconductors[20]

This barrier is known as the **Schottky barrier** and is given by the following formula,

$$\phi_{B0} = (\phi_m - \chi) \qquad (2.1)$$

On the semiconductor side Vbi is called as the built in potential barrier. This is similar to the barrier seen in a p-n junction diode by the electrons moving from conduction band in the semiconductor to the metal and this potential barrier is given by the formula.

$$V_{bi} = \phi_{B0} - \phi_n \qquad (2.2)$$

Which makes Vbi doping dependent.

Now if we apply a reverse bias that is the semiconductor is at a higher potential than the with respect to the metal then the barrier height increases with ϕBo remaining constant. Now if we apply a forward bias that is the metal being positive with respect to the semiconductor ϕbo remains constant with a decrease in barrier height. The energy band diagrams for these two cases are shown in the figure 2.3.

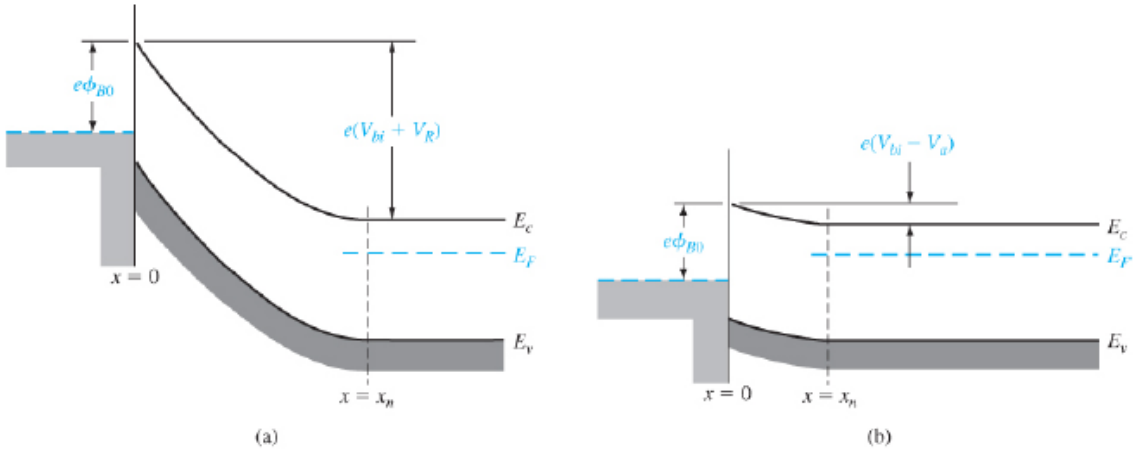

Figure 2.3: Ideal energy band diagram of metal-semiconductor junction (a) under reverse bias (b) under forward bias[20]

2.3 Ohmic Contacts:

Ohmic contacts are also metal to semiconductor contacts but in this case they are rectifying contacts. This contact is a low resistance junction which provides conduction in both directions between a metal and a semiconductor. There are two types of ohmic contacts, the first one is an ideal nonrectifying barrier and the second one is a tunneling barrier.

2.3.1 Ideal Nonrectifying Barriers:

Earlier we have considered a metal to n-type semiconductor contact with $\phi m > \phi s$. Now consider an opposite case where $\phi m < \phi s$, in the figure2.4(a) we can see the energy levels before contact and in the figure 2.4(b) we can see the energy levels after contact. To achieve equilibrium in such conditions electrons will flow from the metal into lower energy states of the semiconductor making the surface of the semiconductor more n-type. This excess electron charge at the surface of the semiconductor is the surface charge density, now if a positive voltage is applied to the metal there is no barrier for the electrons to flow from semiconductor to the metal. On the other hand if a positive voltage is applied to the semiconductor the effective barrier height for the electrons to flow into the semiconductor is approximately $\phi Bn = \phi n$, which is fairly small for a moderately doped semiconductor.

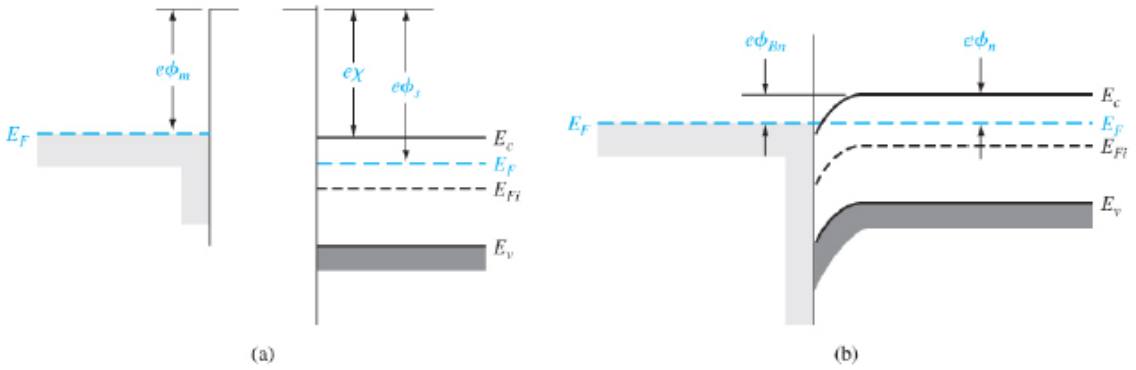

Figure 2.4: Ideal energy band diagram (a) before contact (b) after contact for metal n-type semiconductor where ϕm < ϕs[20]

Figure 2.5(a) shows the energy band diagram for the metal semiconductor ohmic contact when a positive voltage is applied metal. We can see that there is a downhill for the electrons and the electrons can easily flow into the metal. Figure 2.5(b) shows when the semiconductor is at a more positive bias with respect to the metal the barrier for the electrons is fairly small and the electrons can easily flow into the semiconductor. This junction is an ohmic junction.

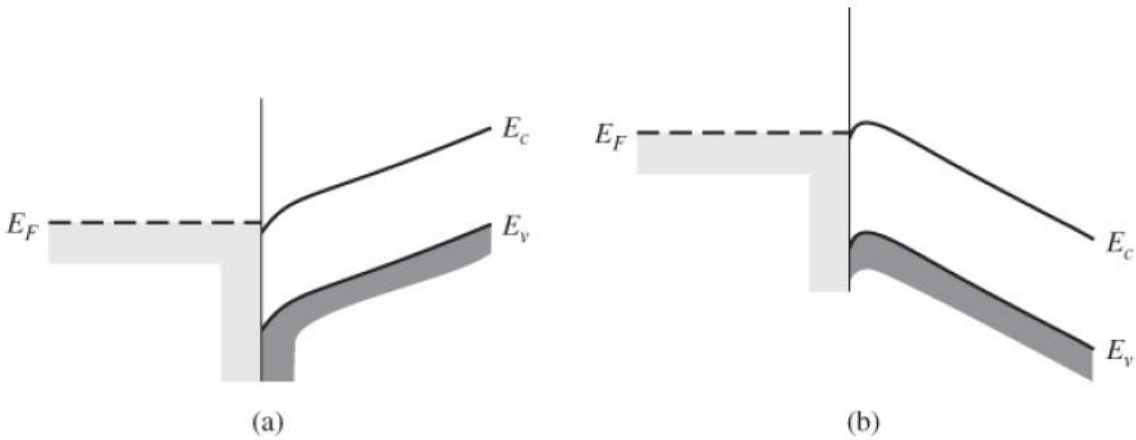

Figure 2.5: Ideal energy band diagram of a metal n-type semiconductor when (a) a positive voltage is applied to the metal and (b) when a positive voltage is applied to a semiconductor ϕm < ϕs[20]

Figure 2.6 shows an ohmic contact with a p-type semiconductor before and after contact.

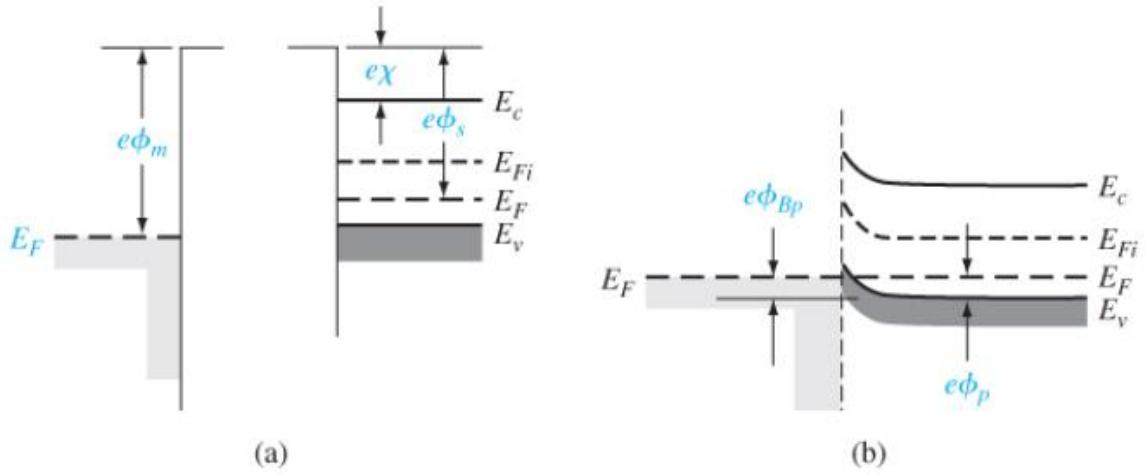

Figure 2.6: Ideal Energy Band diagram (a) before contact (b) after contact of metal and p type semiconductor when[20]

2.3.2 Tunneling Barrier:

The depletion layer in a rectifying or a schottky barrier contact is inversely proportional to the square root of the doping concentration in the semiconductor [20]. Thus the width of the doping concentration decreases as the doping concentration in the semiconductor increases and hence the probability of tunneling through the barrier increases as the doping concentration increases. Figure shows a junction in which metal is in contact with a heavily doped semiconductor.

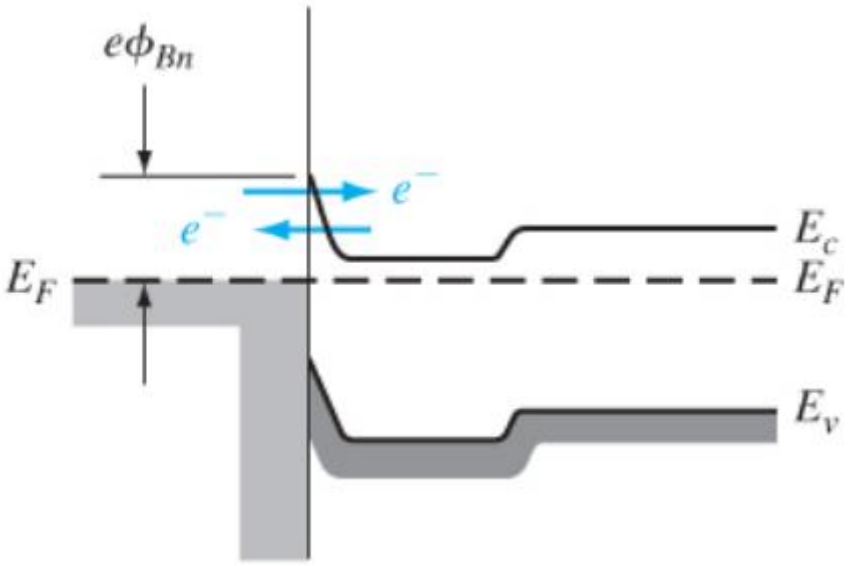

Figure 2.7: Energy band diagram of a heavily doped n-type semiconductor and metal junction[20]

The overall conclusion is that in the formation of Metal and n-type Semiconductor contacts if $\phi m > \phi s$ then the contact will be rectifying while if $\phi m < \phi s$ the contact will be ohmic.

	n-type Semiconductor	p-type Semiconductor
$\phi m > \phi s$	Rectifying	Ohmic
$\phi m < \phi s$	Ohmic	Rectifying

Table 2.3: Rectifying and Ohmic Contacts

Chapter 3

Fabrication of the Device

This Chapter gives a brief description of the experimental procedures used to integrate the Schottky barrier diodes on a commercially available LED chip. In addition to the fabrication procedures used this chapter also compares the device characteristics of the fabricated GaN Schottky Diodes vs commercially available SiC Schottky diodes. The Characterization mainly includes the I-V and C-V measurements at different temperatures as well as the room temperature to extract various diode parameters and to see the output behaviors of these diodes. This chapter will also give a future application of these GaN diodes where we plan to create a novel device which can be used for non-mechanical beam steering.

3.1 Structure of the LED

The GaN schottky diodes were fabricated on a commercial 2-inch LED wafer manufactured by a company in China. The material composition of the LED wafers is shown in the Figure 3.1 and the SEM image is shown in the Figure3.2. From top to bottom the wafer layers are: a 200mm p-type GaN capping layer (Na> 1x 10^{18}). a ~200 nm p-type (Na≈ 5×10^{17}cm-3) GaN layer; a multiple quantum well (MQW) emissive layer consisted by fifteen pairs of 2.5nm In0.1Ga0.9N/12 nm-GaN, a ~2.4 um n-type (Nd ≈ 1×10^{18}cm-3) GaN layer; and a ~2.5 um GaN buffer layer on a patterned sapphire substrate.

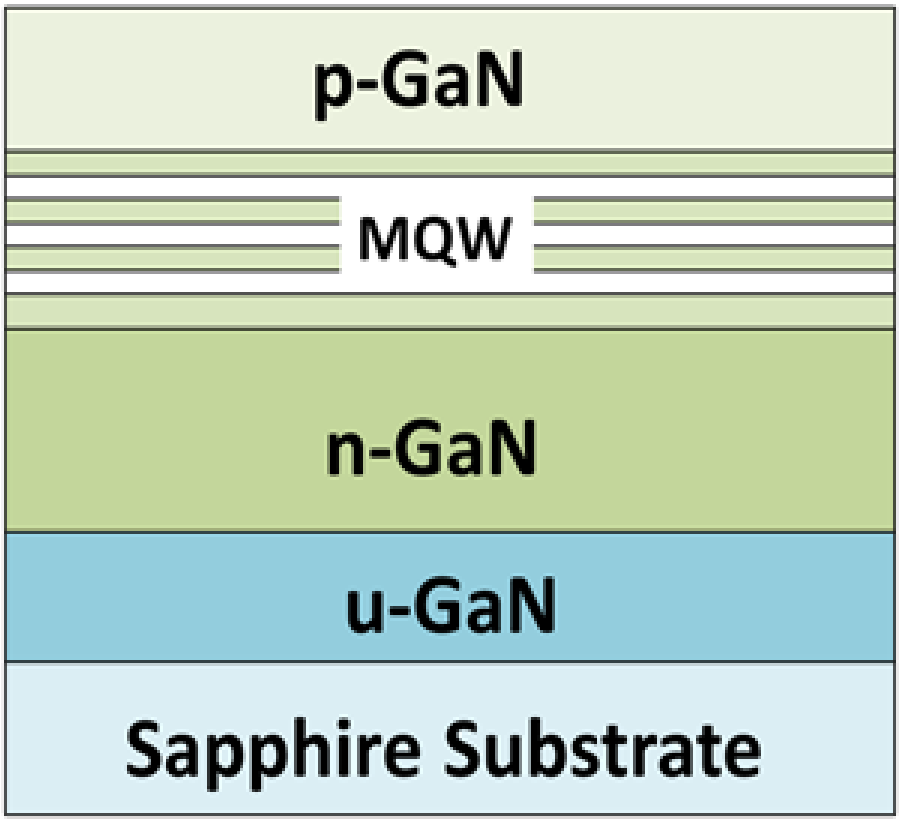

Figure 3.1: Structure of LED on the commercial wafer

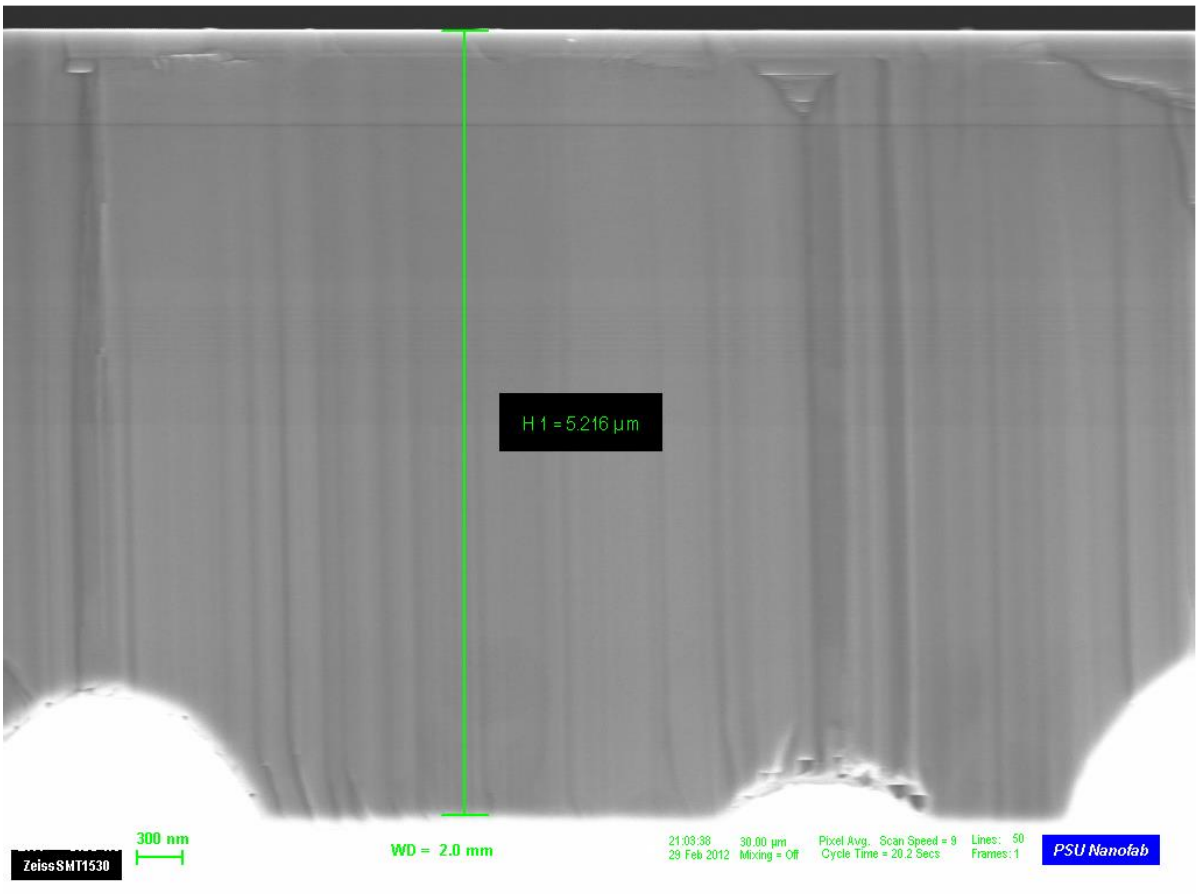

Figure 3.2: SEM picture of the LED on the commercial wafer

3.2 Schottky Diode Fabrication:

To fabricate the schottky diodes on a commercial LED wafers various techniques of etching, KOH treatments and depositions were used. The fabrication processes used in the making of the device are shown in the figure 3.3.

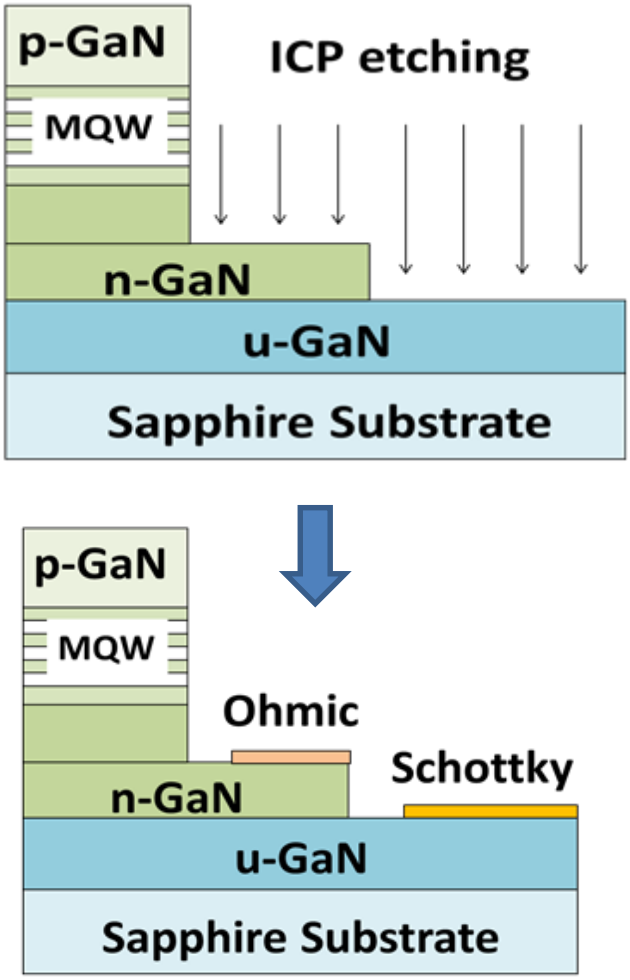

Figure 3.3: Fabrication process of Schottky Diode

The first step in the fabrication of the diode is to expose the n-type GaN using Chlorine based Inductive Coupled Plasma Reactive Ion Etching (ICP RIE) system by etching through selective regions of p-type GaN and MQW. The etch rate is 2 nm/s and the etch depth is about 1.2 μm. To make a schottky contact to the unintentionally doped GaN we need to dry etch down to the u-GaN, but care must be taken because ICP RIE will introduce etching defects and decrease the breakdown voltage of the SBDs. So in order to avoid these etching defects various post etching treatments like annealing and KOH surface treatment has been used. However all the methods are not entirely sufficient to produce a SBD on a commercial LED with a high enough breakdown voltage.

So in order to achieve this requirement a mixed etching technique was used. This technique was composed of three different etching cycles. In each cycle with the help of Chlorine based ICP RIE tool the schottky contact was dry etched and the other area was protected with the Ni etch mask. After drying this surface the device was exposed to a boiling 0.5 Molar KOH solution for 10 minutes for surface treatment. This helped in revitalizing the surface for next etch treatment which in turn reduced the accumulation of the etch defects. In order to further decrease the defects caused due to etching, the etch rates of the first two cycles and the etch rate of the last cycle was varied. The etch rate was set at 2 nm/s for the first two cycles, and the etch depth is 0.9 μm for each cycle. For the last mixed etching cycle, the etch rate is decreased to 0.2 nm/s and the etch depth is 0.1 μm. Due to this procedure the process time was not long and also due to the reduced etch rate of the last cycle the defects introduced were cut down to a great extent. Next the device was annealed at 750°C for 2 minutes in Nitrogen (N2) atmosphere with a rapid thermal annealing (RTA) system.

A Ti/Al/Ti/Au (10nm/40nm/40nm/100nm) metal layer was deposited on n GaN by e-beam evaporation serving as ohmic contacts followed by 500° C annealing for 1min in N2 environment. Schottky contacts with the contact area of 2.5×10^{-5} cm^{-2} are formed by depositing Ni/Al/Ti/Au (50nm/500nm/100nm/200nm) on u-GaN layer. Fabrication of these GaN diodes on a commercial LED wafer helped to achieve a faster switching capability which is a major part of bi-directional optical wireless communications OWC[21]. There are various metals which can be used for Schottky contacts amongst these metals are Pt[22]–[24], Pd[23]–[25], Au[26]–[29], Ni[28]–[31], Re[32] and Ag[29] Also, several metals have been used for the ohmic contact on n-GaN material and these metals are summarized in table 3.1.

Metallization(nm)	Annealing Conditions	Carrier Concentration(cm3)
Ti/Al/Ni/Au (15/220/40/50)	900°C, 30 sec	$4x10^{17}$
Ti/Al (20/100)	900°C, 30 sec	10^{17}
Ti/Al (35/115)	600 °C, 15sec	$5x10^{17}$
Ti (20)	975°C, 30 sec	$5x10^{17}$
Ti/TiN (5/200)	800°C, 60 sec	$7x10^{17}$
Ti/Ag (15/150)	No anneal	$1.7x10^{19}$
Ti/Ni (5/25)	1040°C,30 sec	$1x10^{18}$
Ti/Au (3/300)	No anneal	$4x10^{20}$
Ti/Pd/Ni (5/5/25)	990°C, 20 sec	$1x10^{18}$
TiN (200)	800°C, 60 sec	$7x10^{17}$
Al (150)	600°C, 60-480 sec in Ar/H2	$7x10^{17}$
Al (250)	No anneal	$5x10^{19}$
W (50)	600-1000°C,60sec	$1.5x10^{19}$
Zr/ZrN (20/80)	1000°C,60sec	$2x10^{18}$
Pd/Al (12.5/100)	650°C, 30 sec	$2.8x10^{17}$
Ta/Al (35/115)	600°C, 15sec	$7x10^{17}$

Table 3.1 : Report of Ohmic contact of n-GaN by different research groups[33]

3.3 Current-Capacitance Voltage Characterization and Measurements

This chapter describes the various equipment's that were used in characterization of the diodes, it also shows some trial runs performed on normal p-n junction diodes to test the efficiency of the equipment in performing various measurements. The Schottky diodes are tested in a micromanipulator. The SBD is placed on conducting chuck and is held firmly with the help of vacuum suction. With the help of a microscope two measurement probes are applied to SBD , the use of microscope is necessary for proper placements of the probes since the dimension of the devices are very small and are not visible to the naked eye. The probes connect to a Keithley 238 source measuring units and a Keithley 590 Capacitance voltage measuring unit. When connected to a power supply these units are capable of producing a voltage scan and measuring the currents and capacitances. These SMU's can be interfaced with a computer to tweak various parameters and also for an easy use.

There were two software's that were used for the measurement. The first software is called as the metric Interactive characterization software (ICS). This software allows the user to perform a lot of functions like device characterization, process monitoring, and failure analysis and process development. The software is capable of interfacing with the SMU's, and help control all the necessary parameters needed for experimentation by applying a certain voltage to a certain probe for a predefined amount of time. The software is also capable of providing sweeps of finite voltages, with a difference between data points specified by the software, while measuring a current/capacitance at each point.

Other equipment which was used to measure the Current Voltage characteristics at room temperature and also at a different temperatures ranging from 40 K to 320 K is the Keithley 2612 current source meter. The advantage of using Keithley 2612 over Keithley 238 is that 2612 provides a current range which is higher than 238. The sweeps of voltage and currents in this unit are created using a Lab tracer software. For different temperature measurements a Lake shore 336 temperature controller is connected to the prove station and the chamber is thermally evacuated and insulated. Helium gas is used to cool down the sample and control the temperature between 40 K and 320 K.

Other equipment's were used to measure the C-V and I-V at room temperature as well as different range of temperatures. The range of temperatures for this experiment was from liquid nitrogen (around 70 K) to 473 K. The device is place in a holder which is a small aluminum box called as a device holder. The device holder is further placed in a heater furnace dd9010. This furnace is then connected to a pA meter HP 4140, CD meter HP 4284 and a temperature controller HP 34401. Both the pA meter and the CD meter are connected to the furnace and the temperature controller through a switch NI6008. The temperature lowering in the furnace is down using liquid nitrogen which is flown through the pipes connected to the furnace. The temperature is detected and recorded using a K-type thermocouple.

There are three software's which were used to change the parameters, measure and collect the C-V and I-V data. The first program which was used is the Notepad, which was used to write the commands. To run these commands a second software known as GADD was used which did all the required measurements. Now to see the output graphs of C-V and I-V a third software called as Visualize was used. The notepad

output file could be opened in Visualize or the data could be opened in Microsoft Excel to plot the C-V and I-V curves.

Chapter 4

Current-Capacitance Voltage Characterization

In this chapter we will discuss the characterization techniques used to extract different parameters of the semiconductors. Out of all the characterization techniques discussed below this thesis mainly focuses on electrical characterization which further includes the capacitance and the current voltage characterization.

4.1 Semiconductor Characterization techniques:

Semiconductor Characterization mainly falls into three categories: [34]

1. Optical Characterization
2. Physical/Chemical Characterization
3. Electrical Characterization

4.1.1 Optical Characterization

These characterization techniques are generally used to measure parameters like the physical dimensions of the device, layer thickness, concentrations, impurity and

defect identification and absorption and reflection coefficients of the semiconductor. These techniques include the following:

- Optical microscopy which yields the images of the surface.
- Ellipsometery which measures the insulator thickness.
- Photoluminescence which is used for measuring shallow-level impurities.
- Raman spectroscopy which identifies itself to small-area organic contaminant characterization and stress measurements.
- Infrared reflectance which is used for epitaxial layer thickness measurements.

4.1.2 Physical/Chemical Characterization:

The Physical/Chemical characterization techniques are mostly used to find the spatial distribution of impurities which includes finding the density of impurities, their structural and visual information, the defect causing parameters, the composition of various compounds and various properties which are not amenable to electrical or optical characterization. These techniques generally include:

- Electron Beam technique : This technique mainly includes characterization using Scanning Electron Microscope (SEM), Transverse Electron microscope (SEM), Auger Electron Spectroscopy (AES) and Electron Microprobe (EMP).
- Ion Beam techniques: These techniques involve the use of Sputtering, Secondary ion mass spectroscopy (SIMS) and Rutherford backscattering (RBS).
- X-Ray techniques: This technique makes use of X-ray fluorescence (XRF), X-ray photoelectron spectroscopy (XPS), X-ray topography, X-ray diffraction.

- Chemical Etching.

The advantages of using Physical/ chemical methods of characterization is that they provide extremely high atomic resolution as compared to optical or electrical characterization but this advantage comes at the cost of sensitivity.

4.1.3 Electrical Characterization:

This characterization is one of the most important characterization techniques as it will give us the electrically relevant parameters of the semiconductors. Some of the most important parameters that can be extracted using electrical characterization are doping concentration, barrier heights, ideality factor, and resistivity and contact resistance. Among the electrical methods capacitance voltage, the spreading resistance and the Hall Effect techniques are most commonly used. This thesis will mainly focus on extraction of various parameters using the capacitance voltage and the current voltage measurement techniques.

4.2 Current Voltage Characteristics:

Schottky diodes made from high mobility semiconductors possess a J/V characteristics given by thermionic emission theory, provided that the forward bias is not to large. According to the thermionic emission theory,

$$I = I_s \left[\exp\left(\frac{qV}{kT}\right) - 1\right] \qquad (4.1)$$

Where Is is the saturation current given by,

$$Is = A_{eff} A^* T^2 \exp\left(-\frac{q\phi_B}{kT}\right) \qquad (4.2)$$

Where,

V is the applied voltage across the junction,

Aeff is the effective area of the diode

ϕB is the schottky barrier height of the diode

k is the Boltzmann constant,

T the absolute temperature,

A* is the Richardson constant, which is modified to take into account the effective mass of electrons in the semiconductor, quantum mechanical reflection of those electrons which are able to negotiate the barrier, and phonon scattering of electrons between top of the barrier and the surface of the metal.

Theoretically the value of Richardson's constant can be given by

$$A^* = \frac{4\pi q m^* k^2}{h^3} \qquad (4.3)$$

Where h is the planks constant and

m* is the effective mass of the semiconductor

For GaN the Richardson's constant is calculated to be 26.4 A/cm^{2}K^2[28]

In a practical condition most of the diodes do not behave ideally and show deviations from a normal thermionic behavior and, hence we need to consider a dimensionless parameter called as the ideality factor n, which is taken into account while measuring the I-V characteristics[35]. So the behavior of the diodes can be more closely described by the modified formula.

$$I = I_s\left[\exp\left(\frac{qV}{nkT}\right) - 1\right] \qquad (4.4)$$

Now plot of $\ln\left(\frac{I}{1-exp\left(-\frac{qV}{kT}\right)}\right)$ vs V will give us q/nkT as the slope and the extrapolated intercept on the y axis will give us the value of saturation current Is. With the extrapolated value of Is we can calculate the barrier height of the Schottky barrier as

$$\phi_b = \frac{kT}{q}\ln\left(\frac{AA^*T^2}{I_s}\right) \qquad (4.5)$$

4.3 Capacitance-Voltage Characteristics

A band diagram of an ideal Schottky diode i.e a diode without any interfacial layer is shown in the Figure 4.1.

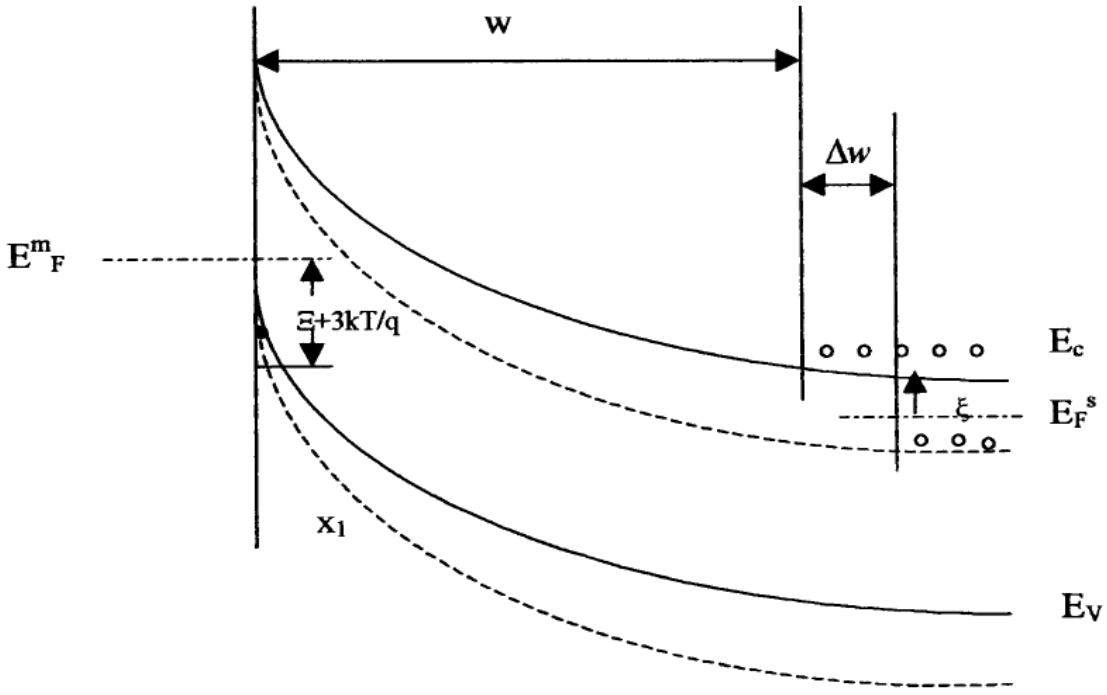

Figure 4.1 : Band diagram of an ideal Schottky diode[36]

In the figure the solid lines represent the reverse bias voltage Vr and the dotted lines represent the increment in the reverse bias which is Vr + ΔVr. The increase of the reverse bias will result in the movement of electrons in the conduction band of the semiconductor further away from the metal and the depletion width will increase from w to w + Δw. Adjacent to the metal near the metal semiconductor interface the concentration of holes will decrease as a result of the hole quasi-Fermi level coinciding with the Fermi level of the metal. Now similar to the concept of a parallel plate capacitor these variations in the charge in the depletion region gives rise to a capacitance.

There are three sources of charge in the barrier region:

1. A positive charge Qd in the depletion region due to the presence of uncompensated donors
2. A positive charge Qh which is constituted by the holes in the valence band and
3. A negative charge Qm whose presence can be attributed to the electrons on the surface of the metal.

The increase in the applied bias causes an increases in the total current in the depletion region due to conduction and a displacement current. The conduction current comprises of two components, one is the drift and the diffusion of electrons from the semiconductor to the metal represented as Jc1 and the other is due to the flow of carriers out of the depletion region as the bias is increased and is represented as Jc2. The displacement current density Jd arises due to the electric field in the depletion region which increases with time as the bias increases.

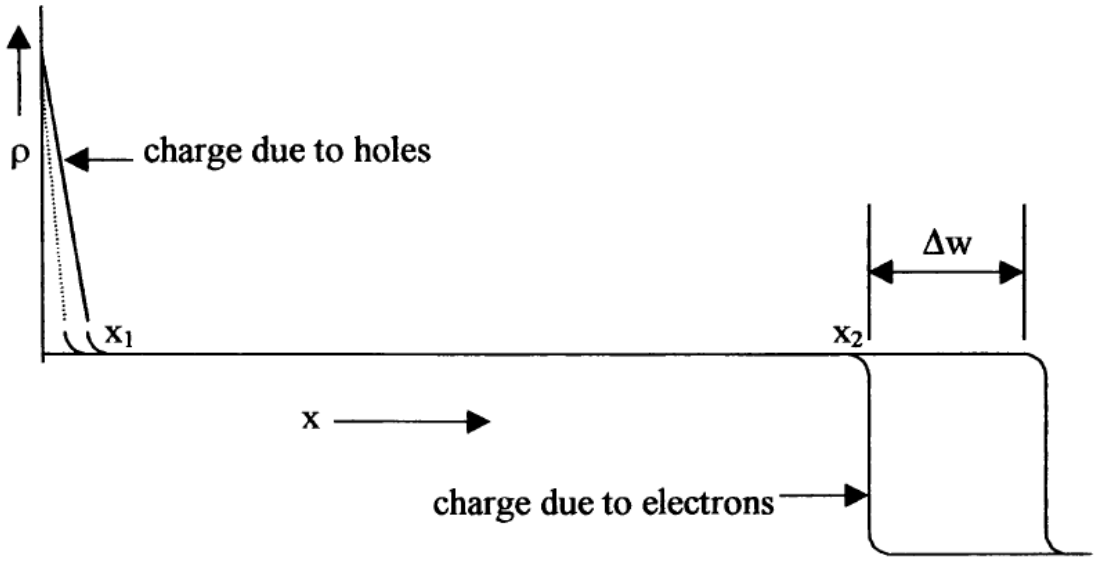

Figure 4.2 : Charge density due to the mobile carriers[36]

Figure 4.2 shows the charge density due to the mobile carriers i.e. electrons and holes. To the right of the plane which is at x = x1 the difference between the Fermi level of the metal and the valence band is greater than ξ + 3kT/q due to which the hole density at this place is a few percent lower than Nd. To the left of the plane which is x = x2 the electron density is a few percent lower than Nd. Hence in the region between x1 and x2 the charge density is due to the donors. The component of conduction current Jc2 is zero in this region and hence the capacitive current mainly constitutes the displacement current Jd given by formula

$$J_d = \frac{\varepsilon_s \partial E}{\partial t} \qquad (4.6)$$

From the electrical circuit definition of capacitance[37]

$$J_d = C\left(\frac{\partial \Delta V_R}{\partial t}\right) \qquad (4.7)$$

Where C is the differential capacitance per unit area.

From equation 4.6 and 4.7 we get

$$C\left(\frac{\partial \Delta V_R}{\partial t}\right) = \varepsilon_s \frac{\partial E}{\partial t} \qquad (4.8)$$

$$C = \varepsilon_s \frac{\partial E}{\partial V_R} \qquad (4.9)$$

Using Gauss's theorem the electric field is calculated to be

$$\varepsilon_s \Delta E = \Delta Q_d \qquad (4.10)$$

Differentiating both sides with respect to V_R we get

$$\varepsilon_s \frac{\partial E}{\partial V_R} = \frac{\partial Q_d}{\partial V_R} \qquad (4.11)$$

Now, substituting equation 4.11 in 4.9 we get

$$C = \frac{\partial Q_d}{\partial V_R} \qquad (4.12)$$

If we neglect the effect of minority carriers then we can express the differential capacitance in terms of the diffusion voltage and the donor density. In such conditions, at the interface between metal and the semiconductor, the top of the valence band is below the metal Fermi level by at least $\xi + 3kT/q$. Hence we can write the electric field to be as [36]

$$E_{max}^2 = \frac{2q}{\varepsilon_s}\left(N_d\left(V_d - \frac{kT}{q}\right) + \frac{kTN_d}{q}\exp\left(-\frac{qV_d}{kT}\right)\right) \qquad (4.13)$$

Where Vd is the diffusion voltage.

If we assume qVd > 3kT the last term in the bracket is negligible and we can write the equation as,

$$E_{max}^2 = \frac{2q}{\varepsilon_s}\left(N_d\left(V_d - \frac{kT}{q}\right)\right) \qquad (4.14)$$

The charge due to the uncompensated donors is given by Gauss's theorem as

$$Q_d = \varepsilon_s E_{max} \qquad (4.15)$$

Substituting 4.14 in 4.15 we get

$$Q_d = (2q\varepsilon_s N_d)^{\frac{1}{2}}\left(V_d - \frac{kT}{q}\right)^{\frac{1}{2}} \qquad (4.16)$$

Then from equation 4.12. We can write

$$C = \frac{\partial Q_d}{\partial V_r} = \frac{\partial Q_d}{\partial V_d} \qquad (4.17)$$

$$C = \left(\frac{q\varepsilon_s N_d A^2}{2}\right)^{\frac{1}{2}}\left(V_{do} - V_r - \frac{kT}{q}\right)^{-\frac{1}{2}} \qquad (4.18)$$

Where Vd = Vdo +VR

And Vdo is the diffusion voltage at zero bias condition.

Now squaring both sides of the equation and taking the inverse we get,

$$\frac{1}{C^2} = \frac{2}{qN_d K_s \varepsilon_0 A^2}\left(V_{do} + V_R - \frac{kT}{q}\right) \qquad (4.19)$$

This equation suggests that the plot of $1/C^2$ vs V would be a straight line where the slope of the graph would be inversely proportional to the carrier concentration. Hence we can write the carrier concentration as

$$N_d = \frac{2}{qK_s\varepsilon_0 A^2 slope} \qquad (4.20)$$

And the intercept on the x- axis will give Vo which is related to built in voltage by the equation,

$$V_{do} = V_o + \frac{kT}{q} \qquad (4.21)$$

Where T is the absolute temperature.

Then the barrier height of the Schottky can be calculated using the formula

$$\phi_B = q(V_{do} + V_n) \qquad (4.22)$$

Where $V_n = \frac{kT}{q}\ln(N_c/N_d)$,

And Nc is the effective density of states which is given by the equation

$$N_c = 2\left(\frac{2\pi m^* kT}{h^2}\right)^{\frac{3}{2}} \qquad (4.23)$$

Where m* is the effective mass of electron in GaN and is related by

$m^* = 0.22m_0$

Where m0 is the effective rest mass of the electron which is 9.11×10^{-31} kg.

Using these formulas the effective density of state for GaN is calculated to be

2.8×10^{18} cm^{-3}

Chapter 5

Results

In this thesis I present an investigation of Schottky diodes which are fabricated on a commercial LED chip. Their characteristics were investigated using I-V and C-V characteristics. The measurements on these diodes were done at room temperature as well as different temperatures. The first part of the result will discuss about the I-V Characteristics of the fabricated GaN diodes and the commercially available SiC diodes. These two devices are compared in terms of their barrier heights and ideality factors. The second part of the thesis focusses on the C-V characteristics of both the diodes. Doping concentrations of both the devices are calculated using the C-V characteristics and both of them are again compared in terms of their barrier height, but in this part the barrier height is calculated using the doping concentrations of the device.

5.1 Current/ Capacitance Voltage Characteristics of a Few Devices

To continue with the electrical characterization of the diodes some of the equipment's were tested to be compatible with the device. The following are the results from Keithley 238 and Kiethley 590. The following results contain the C-V characteristics and I-V characteristics of a normal P-n Junction Diode, Metal Oxide Semiconductor Capacitance (MOS CAP) and power MOSFETs. From these results it was concluded that we won't be able to measure the C-V characteristics of GaN Schottky Diodes as the capacitance range of these equipment's were too

large as compared to the Schottky Diodes and hence we moved on to measuring the characteristics of these devices on an HP-4284 CD meter.

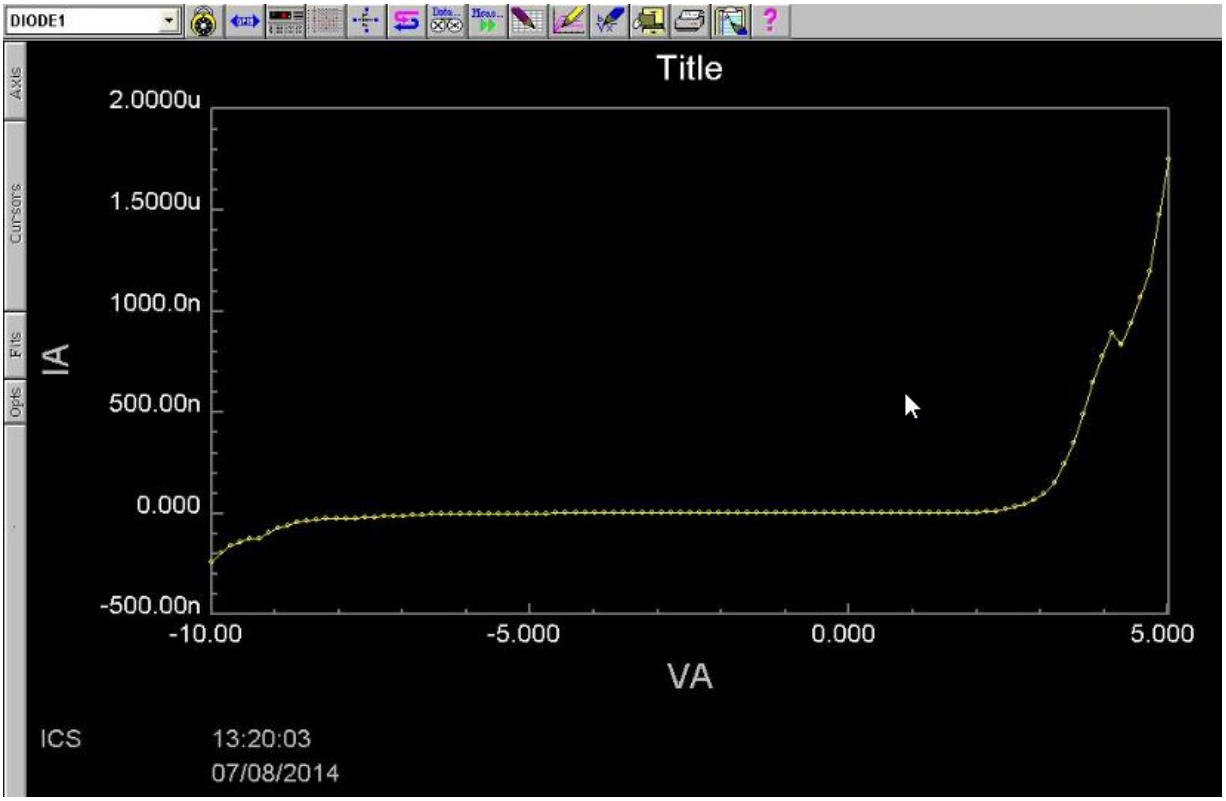

Figure 5.1: P-N junction diode I-V Characteristics

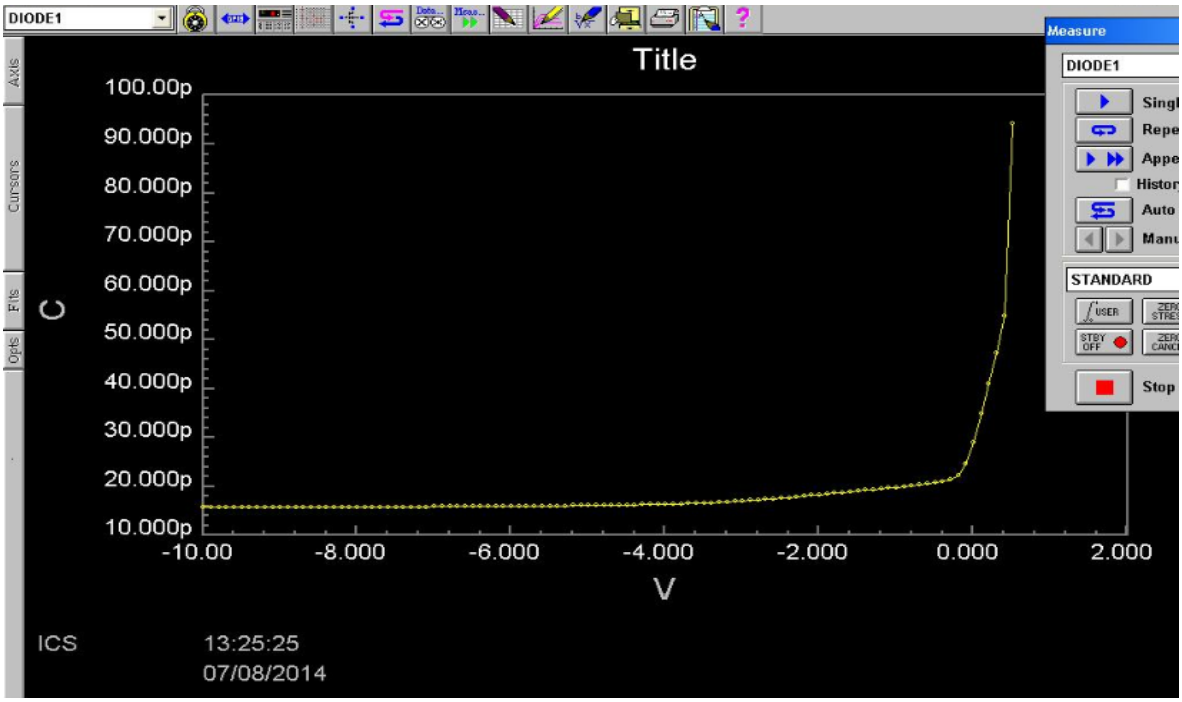

Figure 5.2 : P-N junction diode C-V characteristics

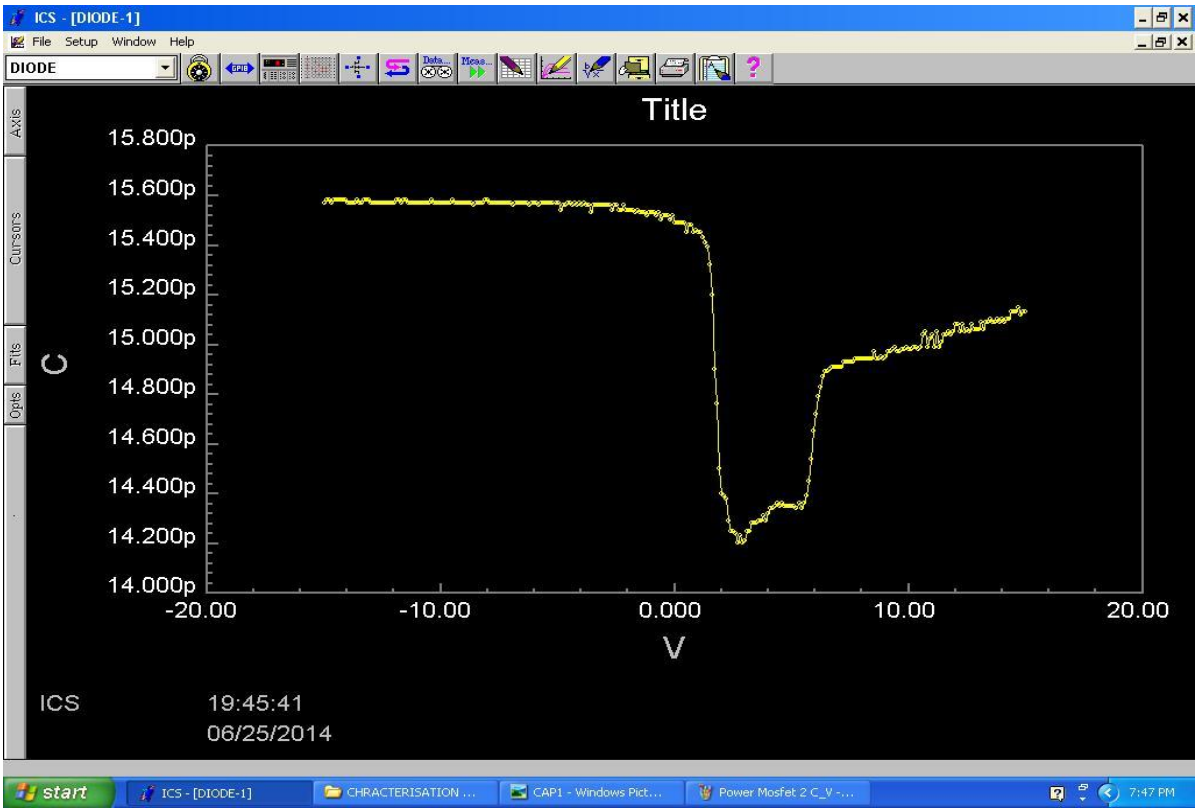

Figure 5.3 : C-V characteristics of a MOS Capacitor

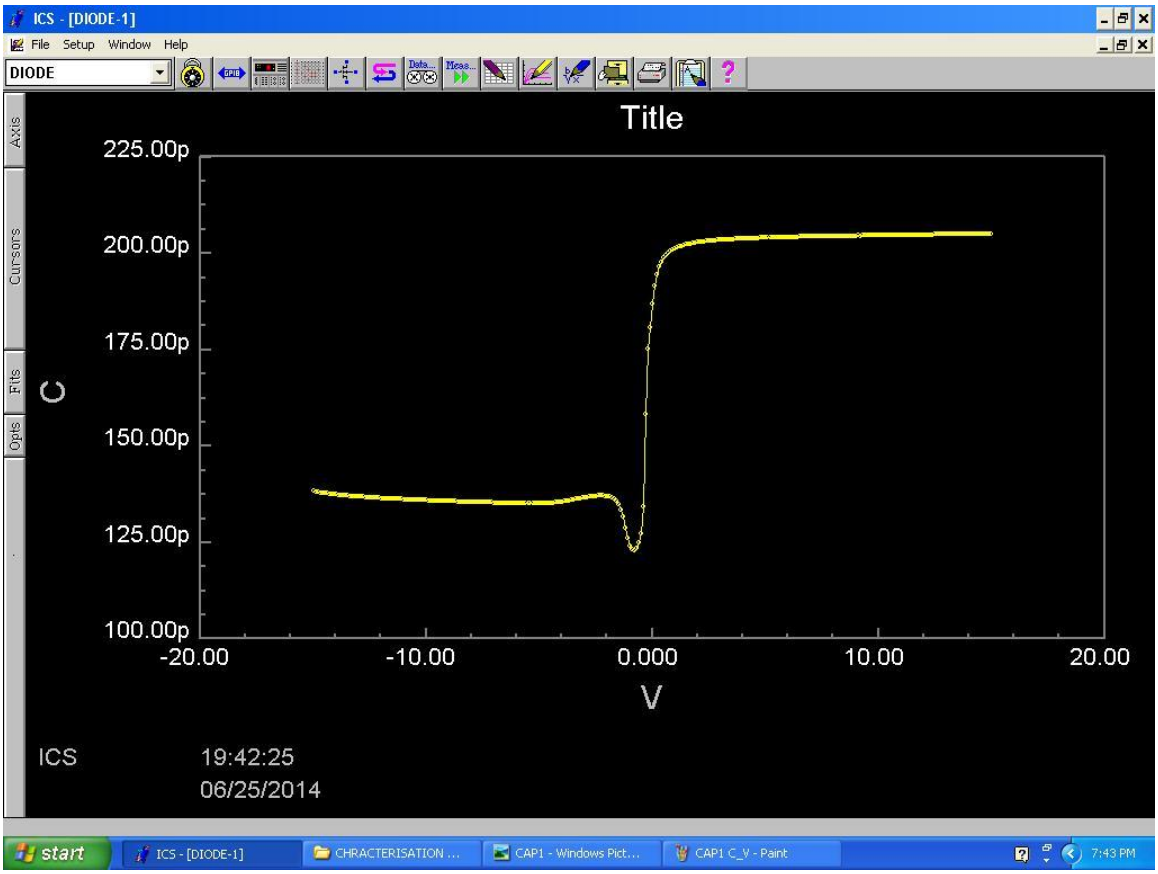

Figure 5.4 : C-V characteristics of a Power MOSFET

5.2 Current-Voltage Characteristics

This section summaries the Current- voltage characteristics of GaN and SiC diodes at different temperatures as well as the room temperature. The temperature scale involved in the measurement of these devices ranges from around 100K to 300K for GaN diodes and 113K to 433K for SiC diodes. These ranges were selected in order to observe the changes in the behavior of the GaN and SiC diodes with temperature. The ranges are different since the measurement was done on two different equipment's. Latter we will see the issues which arised due to the measurements done on SiC diodes with a different equipment. From the graphs plotted as shown in Figure 5.5 and Figure 5.6 it is visible that these behaviors are not changing much with respect

to the temperature and the turn on voltages for both these devices could be approximated to be around 0.5V.

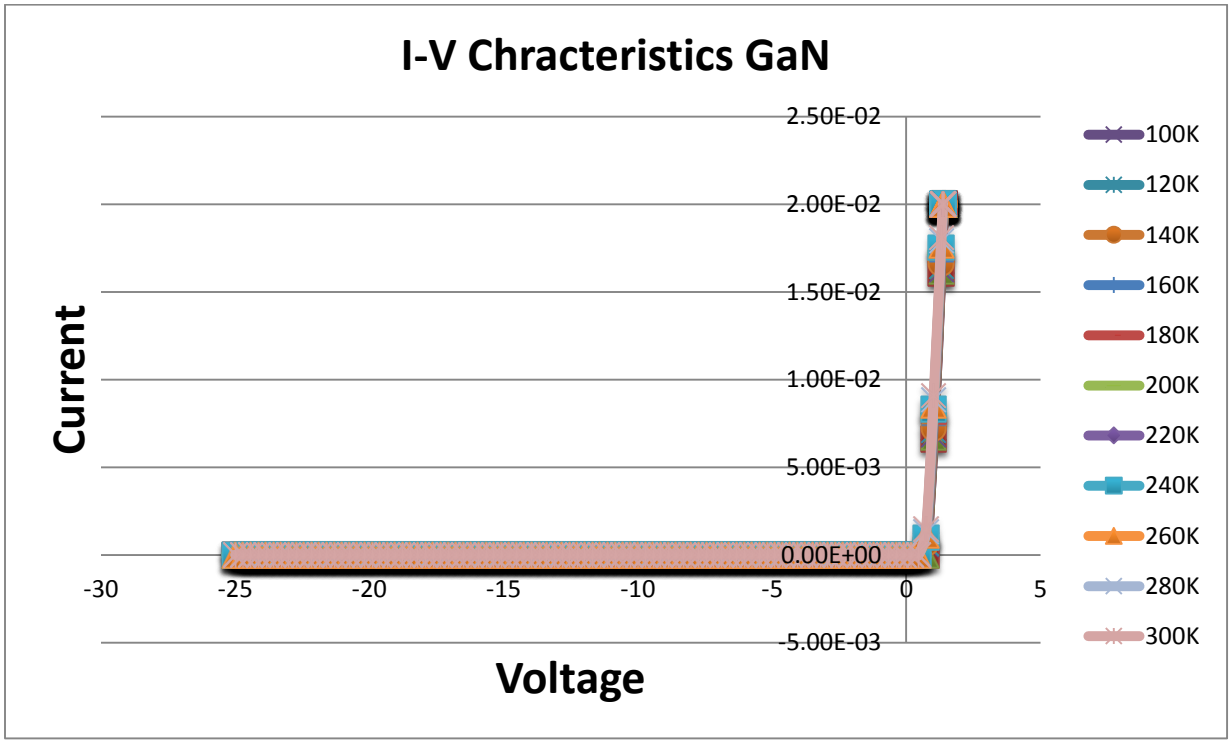

Figure 5.5: I-V Characteristics of GaN diode

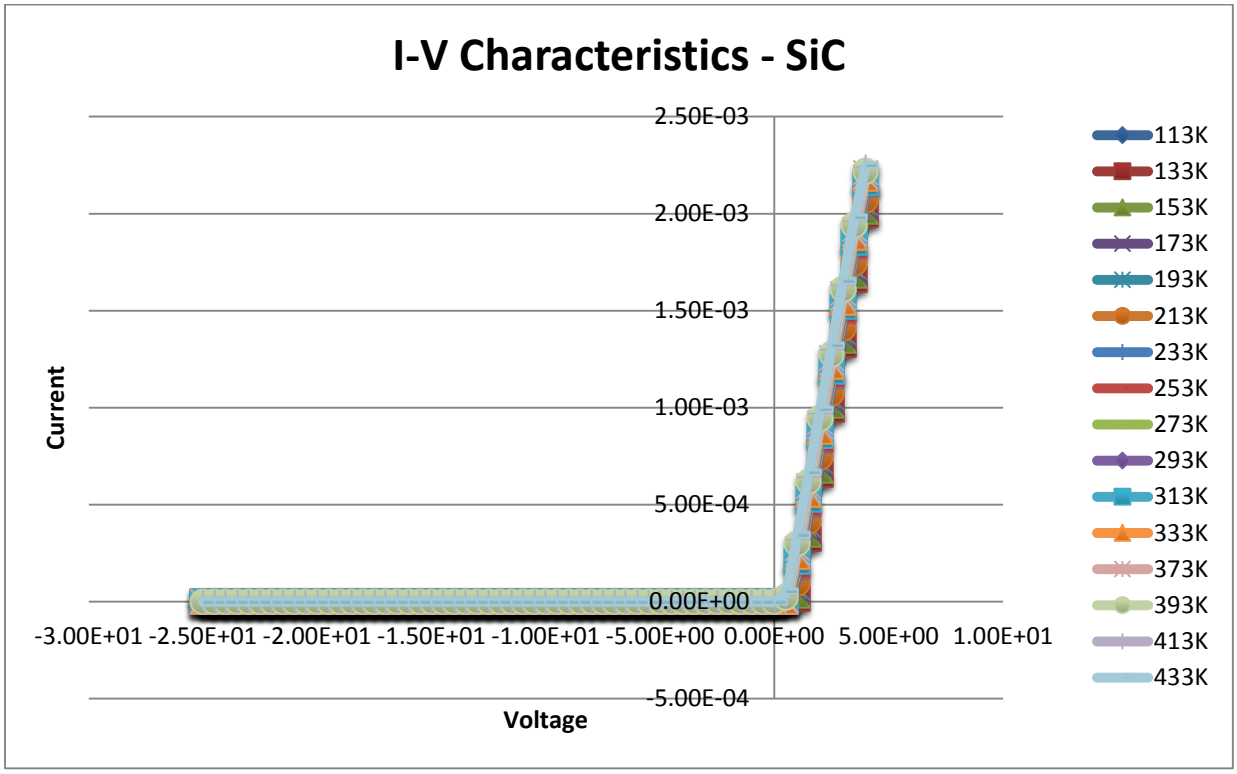

Figure 5.6: I-V Characteristics – SiC diode

There are some important parameters which can be extracted from these I-V curves. One such important parameters is the ideality factor of the diodes. Ideality factor is an important factor in characterization of the diodes as it allows us to determine the deviation of these devices from an ideal diode. It also tells us the fact that there are impurities and various defects in the device that can cause recombination and reduce the forward current. For an ideal diode the ideality factor is equal to 1. As discussed in chapter 4 the ideality factor can be calculated using the semilog I vs V curve which is shown in Figure 5.7 and Figure 5.8. Now if we plot the curve we see two different regions for both the SiC and GaN diodes. Region 1 is more accurate for the calculation of the ideality factor since the dominant mechanism of transport in this region is thermionic emission. While in the second region there are several other factors such as defects in the space charge region which yield inaccurate results of the ideality factor [38], [39]. Figure 5.9 and Figure 5.10 show the dependence of ideality factor on the temperature. Ideality factor is inversely

proportional to the temperature and this is verified for GaN diodes. For GaN the ideality factor at 120K is 0.96 and at 300K it is 0.6. The decrease in the ideality factor with temperature mostly shows that thermionic emission is the main reason of transport in GaN schottky diodes. Now for SiC diodes the measurements were done with voltage increments of 0.5V and as a result of this while calculating the barrier height, one of the point which was considered fell just inside region 2 and the mechanism of transport in this region affected the calculations of the ideality factor of SiC diodes. Hence we can see from Figure 5.10 that the ideality factor is not exactly proportional to the temperature for SiC diodes.

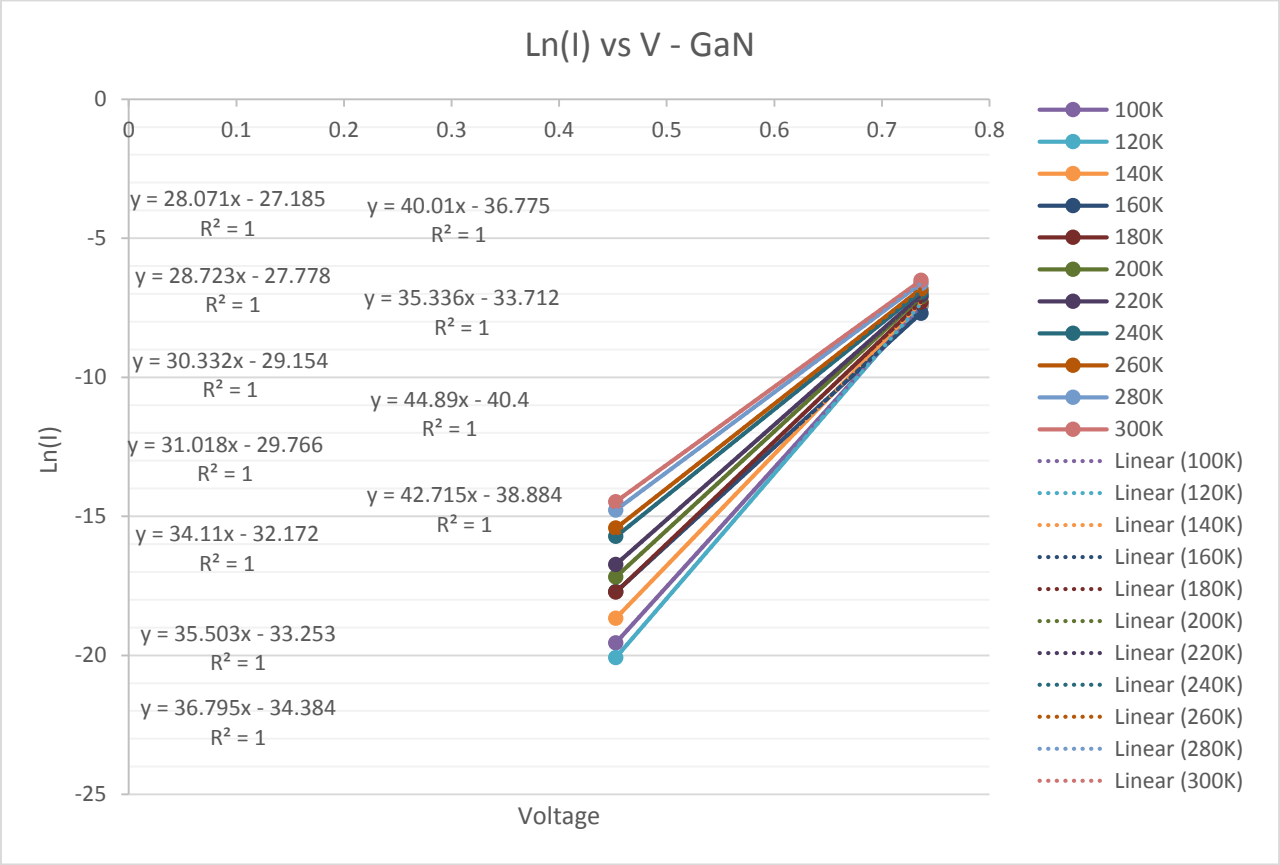

Figure 5.7: Semilog of I vs V for GaN diode

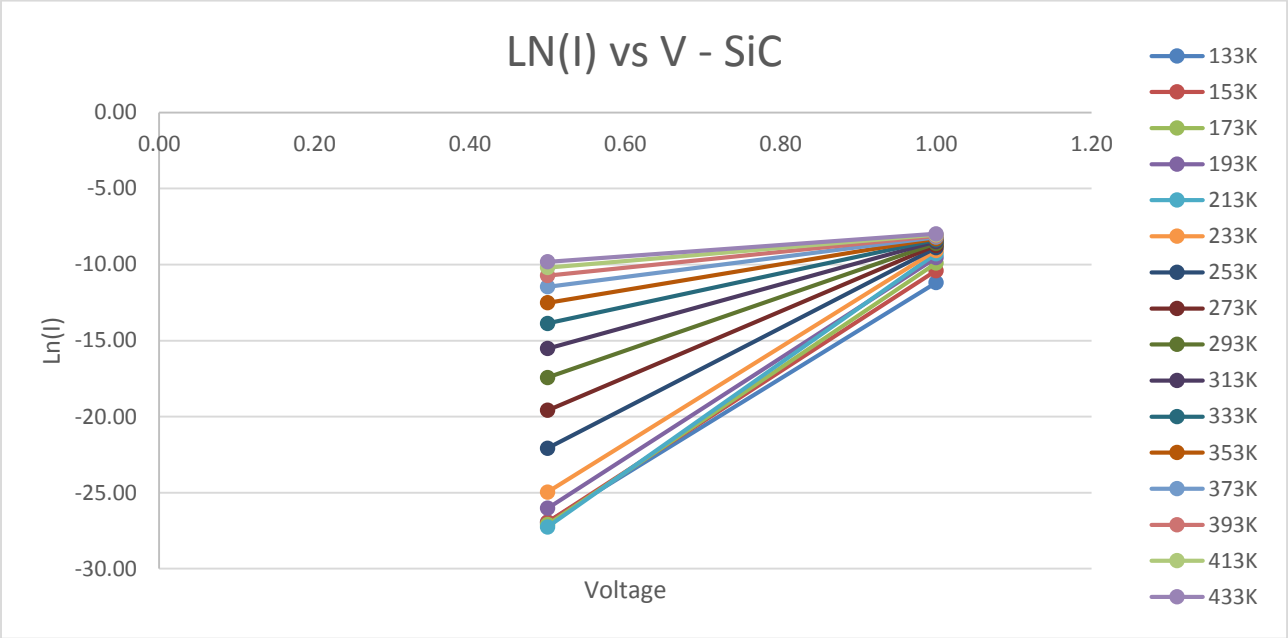

Figure 5.8: Semilog of I vs V for SiC diode

One more factor that can be derived using the I-V curves is the barrier height of the Schottky diodes. As discussed in chapter 4 using equation 4.5 we can derive the barrier heights of the Schottky diodes. All the parameters in the equation are known and the value of saturation current can be determined using the semilog I vs V curve and extrapolation the value of semilog I at V=0. Figure 5.9 and Figure 5.10 show the variation of the barrier height with the temperature. As we can see the barrier height is directly proportional to the temperature for GaN diodes. The values of barrier height for GaN at 120K is 0.44 and at 300K it is 0.81. The barrier height calculations for SiC were again affected due to the measurements which were done with the increments of 0.5V.

SiC		
Temperature in Kelvin	**Ideality Factor**	**Barrier Height**
133	0.89	0.54
153	0.76	0.63
173	0.66	0.73
193	0.62	0.79
213	0.52	0.92
233	0.53	0.93
253	0.57	0.89
273	0.61	0.85
293	0.66	0.81
313	0.71	0.77
333	0.78	0.73
353	0.85	0.70
373	0.92	0.67
393	0.96	0.67

GaN		
Temperature in Kelvin	**Ideality Factor**	**Barrier Height**
100	1.18	0.35
120	0.94	0.44
140	1.02	0.44
160	0.79	0.55
180	0.76	0.58
200	0.71	0.63
220	0.67	0.68
240	0.68	0.69
260	0.64	0.74
280	0.63	0.77
300	0.60	0.81

Table 5.1 : Ideality Factors and Barrier Heights of GaN and SiC diodes

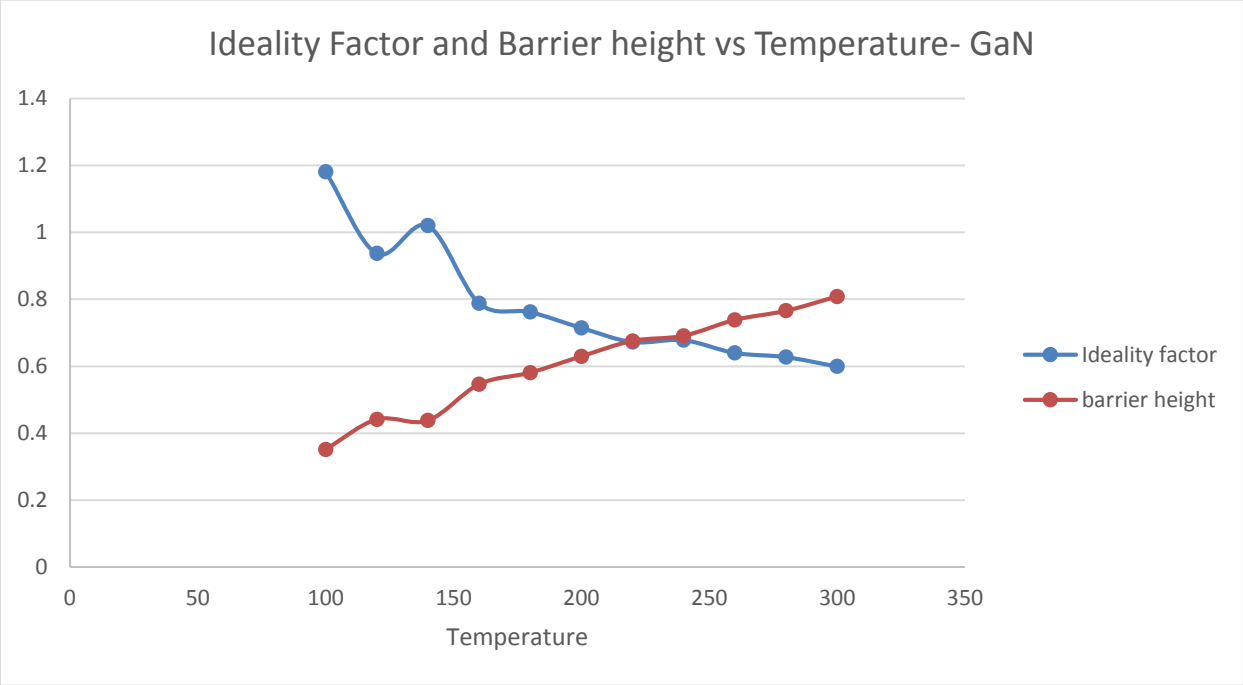

Figure 5.9: Ideality Factor and Barrier Height vs Temperature for GaN Diode

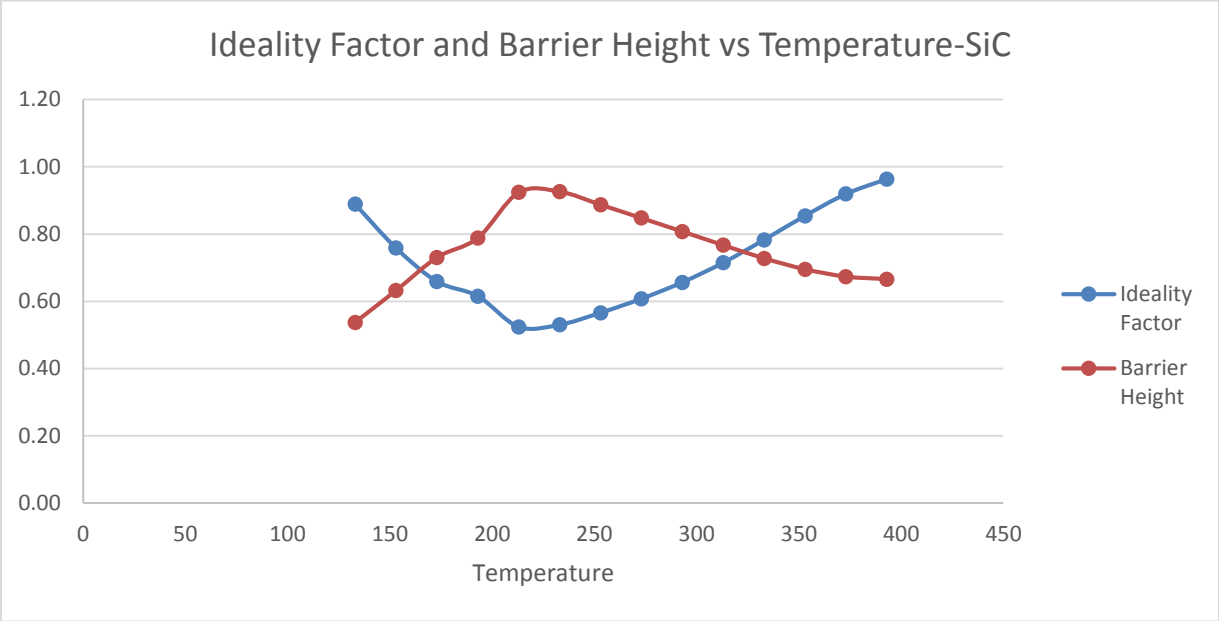

Figure 5.10: Ideality Factor and Barrier Height vs Temperature for SiC Diode

5.3 Capacitance Voltage Characteristics

This section comprises the results obtained using C-V characteristics on SiC and GaN Schottky diodes both at room temperature as well as different temperatures. Figure 5.11 and Figure 5.12 shows the room temperature characteristics of SiC and GaN samples respectively. From the plots of C-V characteristics it can be observed that the GaN capacitance is in the range of pico-Farads (pF) while the SiC capacitance is in the range of nano-Farads (nF).The capacitance of both the devices were measured at 1 MHz and the voltage sweep was from -25V to 0V. The GaN sample was also measured with a frequency of 100KHz just to see the effect of frequency on the GaN samples. The frequency results are shown in Figure 5.15 and they are equal for both 100 KHz and 1 MHz.a

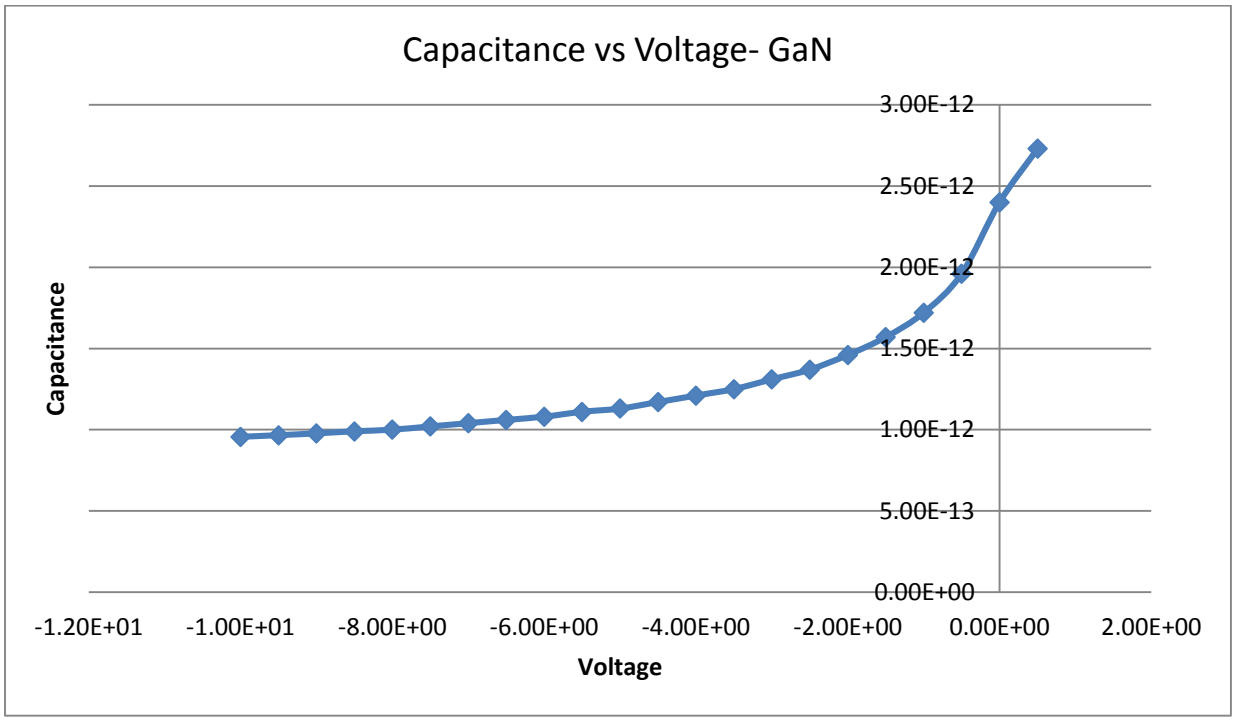

Figure 5.11 : Capacitance- Voltage Characteristics for GaN diode

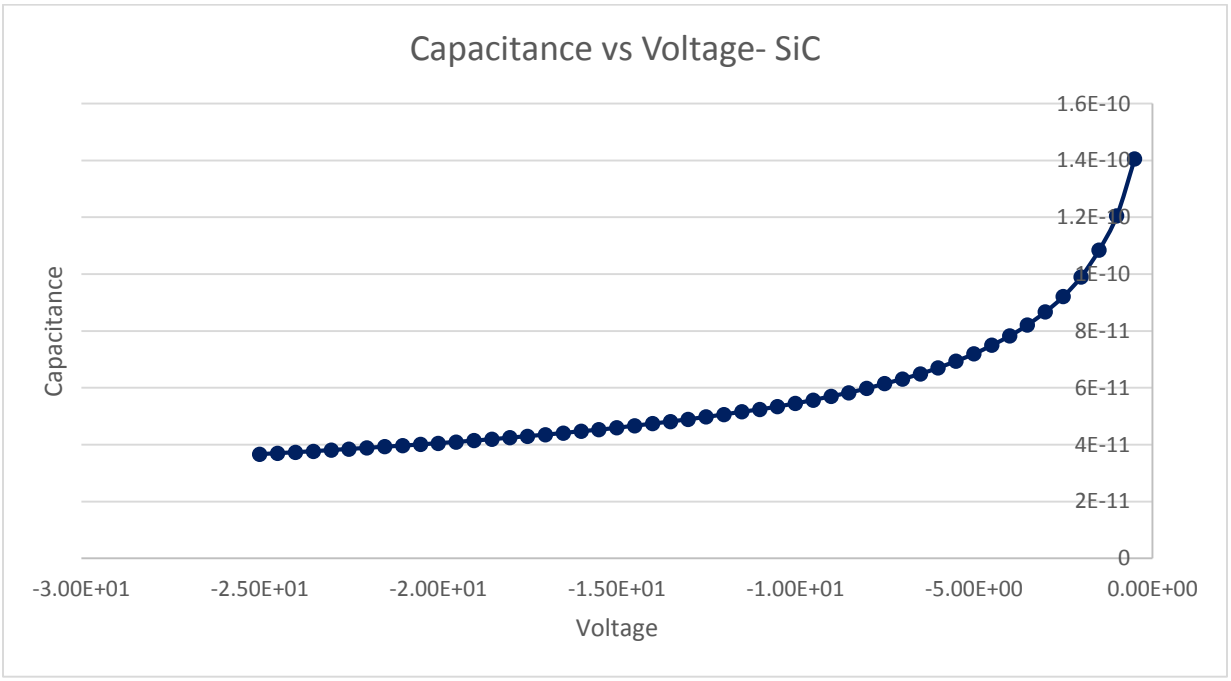

Figure 5.12 : Capacitance Voltage Characteristics of SiC diode

One of the most important parameters that can be determined using the C-V characteristics of the diode is the doping concentration. Using equation 4.20 as discussed in chapter 4 we calculated the doping concentrations using the slopes of 1/C2 vs V plots. Figure 5.13 and Figure 5.14 shows the 1/C2 vs V plots for both GaN and SiC respectively. Ideally the plot should be linear but as we can see in the case of GaN the plot seems to be a little deviated from its linear value. For this reason we have divided the plots into three regions of concern to see if there are any differences in the doping concentration values. From the Table 5.2 it is evident that for SiC shottky diodes there is no change in the doping concentration over the three regions of concern but for GaN we see changes in the doping concentration. These results were expected because if we look at the 1/C2 vs V plot it is perfectly linear for SiC shottky diodes while it is a little off from linear for GaN schottky diodes.

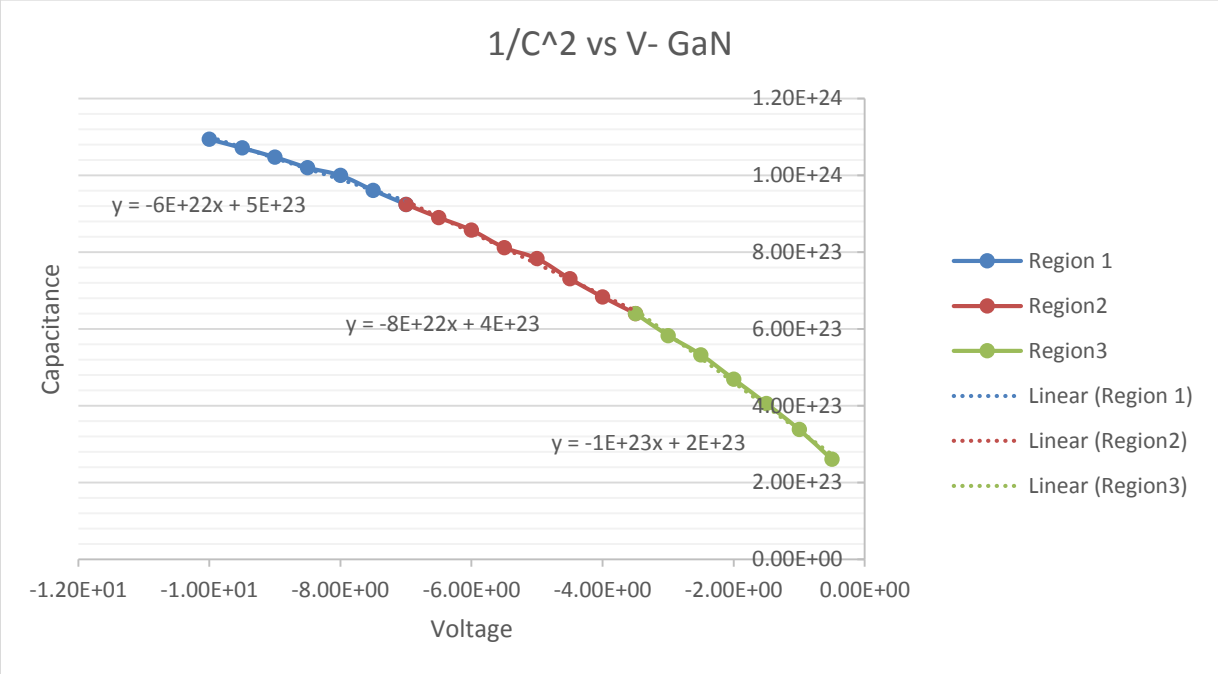

Figure 5.13 : 1/C^2 vs V for GaN diode

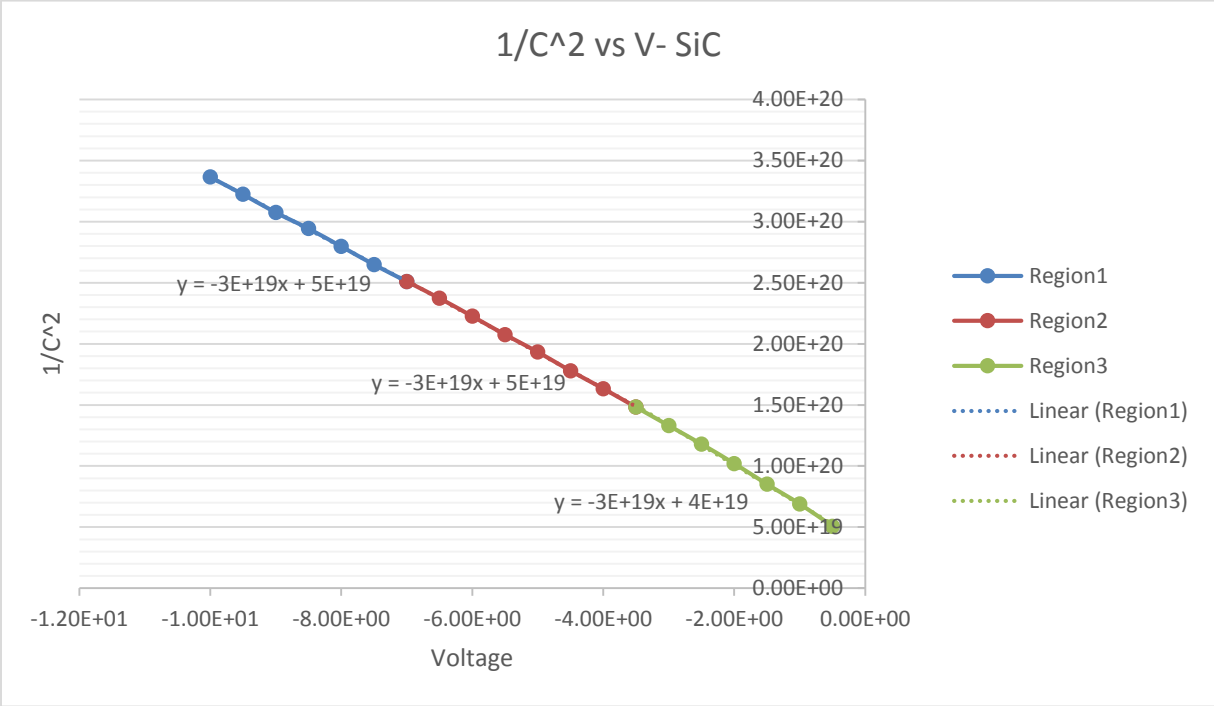

Figure 5.14 : 1/C^2 vs V for SiC diode

Region of Concern	Doping Concentration GaN / cm^3	Doping Concentration SiC / cm^3
Region 1	4.22E+17	8.45E+20
Region 2	3.17E+17	8.45E+20
Region 3	2.53E+17	8.45E+20

Table 5.2: Doping Concentration of GaN and SiC diodes

The doping concentration of GaN goes on increasing as the voltage changes from region to region. The main reason for this is the presence of defects mainly electron traps in the space charge region of the semiconductor. These defects can be caused to due to the ICP etching techniques which were used to etch the device. Another important reason can be cleaning of the device. Since there was a trench in the device after etching there might be chance that the

cleaning agents were not able to reach such critical dimensions leaving behind residues which may have caused the carrier concentration to change.

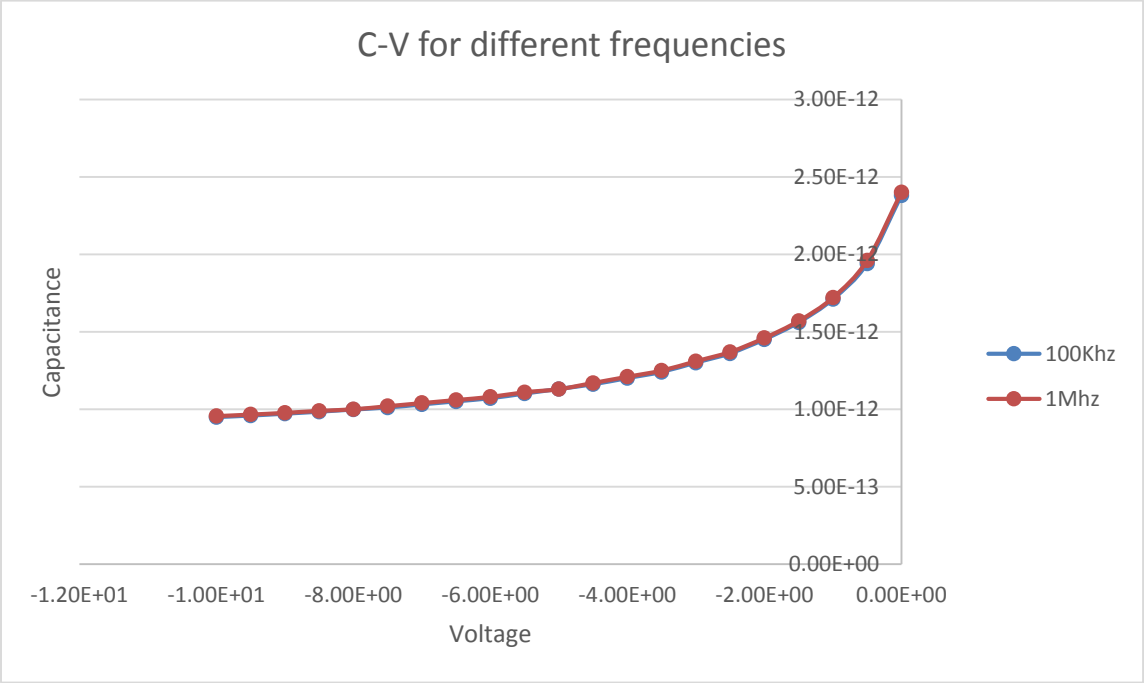

Figure 5.15 : C-V Characteristics for different frequencies on GaN diodes

Chapter 6

Non-Mechanical Beam Steering

In this part of thesis I present a novel technique that can be used for beam steering without using any mechanical methods. The technique makes use of liquid crystal properties for beam steering. Liquid crystals are known to have the largest electro-optical response and when combined with patterned electrodes it is capable of provide an analog non mechanical "Snell's Law type" beam-steerer[40].

6.1 Operating Principle and Architecture of the Device

For the past decades use of Liquid Crystals is one of the most commercially and technically successful techniques. Liquid Crystals are environmentally stable and inexpensive and are known to have the largest electro-optic response which is about the order of 10^5-10^6 pm/V[41]. The basic principle in the operation of typical Liquid crystal display is that a light transverse between a very thin layer of liquid crystals (<20 um) and transparent electrodes are used to apply electric field which in combination with the polarizers are used to block or transmit light. Using the same principal we have tried to architecture our device. As shown in the Figure6.1 we have sandwiched the Liquid crystals in between two ITO glass plates with one glass plate having ITO patterned in the shape of triangle using photolithography techniques. When we apply an electric field to these electrodes the liquid crystals beneath the pattern electrodes form a prism type shape in comparison with the other liquid crystals. Even the orientation of these liquid

crystals is different as compared to other liquid crystals which causes a refractive index change in these liquid crystals. We then use a glass prism to couple light into these glass plates , this light then passes through the liquid crystals which causes the beam to deviate from its normal angle due to the refractive index change in between the liquid crystals.

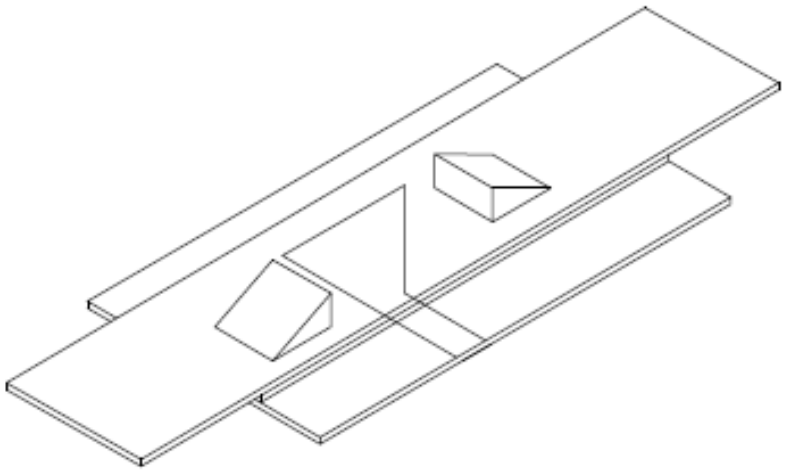

Figure 6.1 : Design of the Beam steerer.

The deviation of light through a prism is basically governed by snells law shown in figure and is given by

$$\frac{sin\theta 1}{sin\theta 2} = \frac{n1}{n2} \qquad (6.1)$$

Where n1 and n2 are the refractive indices of the two mediums in which the light is travelling. The greater the refractive index change more we get the deviation, hence we choose a liquid crystal with the largest refractive index possible [42].

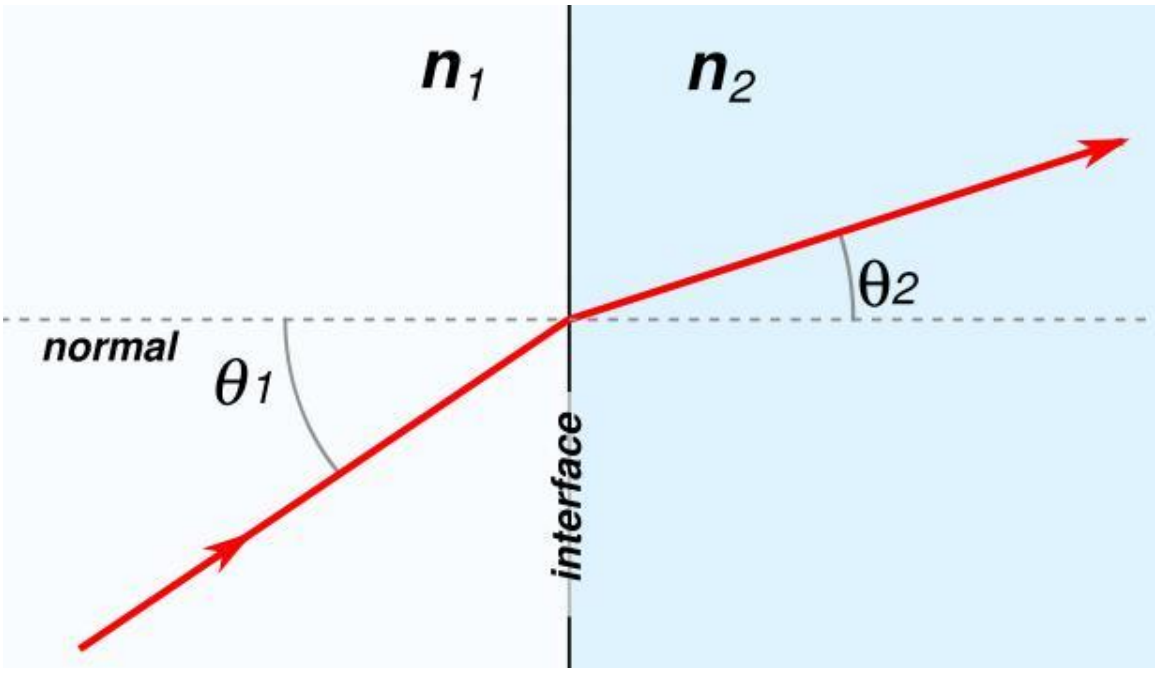

Figure 6.2 : Snells Law

If we know the change in the refractive index of liquid crystals we can calculate the change in the angle of deviation from the prism using the formula,

$$n = \frac{\sin(\frac{\delta + \alpha}{2})}{\sin(\frac{\alpha}{2})} \qquad (6.2)$$

Where,

δ is the deviation angle

n is the relative refractive index of the prism

α is the prism angle which is 45° in this case due to the geometry of the design.

6.2 Surface Alignment of the Liquid Crystals.

One of the major factor concerning a liquid crystal device is the alignment of the liquid crystals. There are four basic alignments as shown in the Figure 6.3. Our main concern is the parallel alignment. Now the method or the mechanism to obtain a stable alignment has been researched by many scientists. Kahn empirically described that the *"alignment is determined by the competition between the surface tensions of the liquid crystals and the substrate"*[42]. While there are many contradicting theories to this reported as well. Haler said that *"the dispersion force is considered as the only alignment factor and It is assumed the LC's align perpendicular to the free surface"*[43].Now the mechanism for parallel alignment is described as follows.

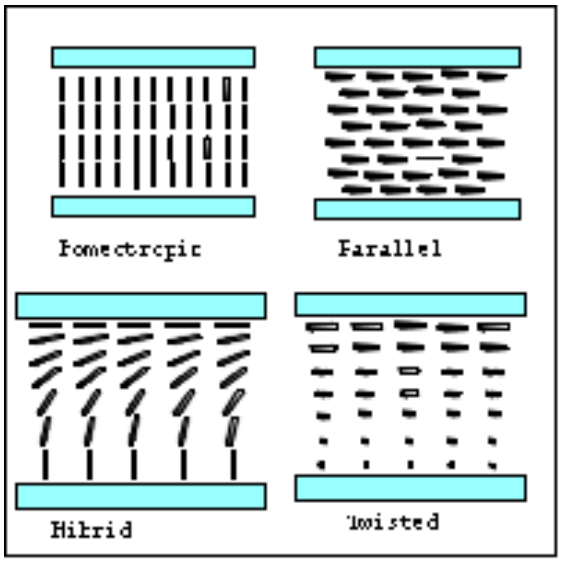

Figure 6.3 : Basic Alignment of Liquid Crystals

6.2.1 Parallel Alignment:

The basis of parallel alignment of liquid crystal is that the surface should be microscopically flat and the liquid crystal in use should not contain any amphiphilic impurity (reference) and in addition to this the surface polarity should be too low to absorb the impurity. To achieve this the surface is generally coated with a fluorinated material which gives us a low surface energy. Now with the help of coating a polymer we can obtain a stable parallel alignment by decreasing the polarity. However this alignment is random and to obtain a homogenous alignment unidirectional rubbing is necessary[44].

In this thesis the parallel alignment was tested using a polarized laser light. The polarized laser was passed through the liquid crystal cell and then the cell was rotated with an increments of 10 degrees and the intensity of light was recorded. When the polarization of light matches with the alignment of liquid crystals we get maximum intensity of light and when the polarization is perpendicular we get minimum intensity of light.

6.3 Manufacturing of the Liquid Crystal Device.

In this section I will describe the steps taken in order to fabricate the device. Some of the general requirements required for fabrication are described as follows.

a. Cleaning chemicals: acetone, IPA, 7X detergent 5% in DI water, DI water with resistivity larger than 10M ohms. The grade of chemicals to be used should be electronic grade.

b. Clean room: class 100.

c. Dress requirements: as per clean room class 100.

d. Clean room temperature: 17C-25C.

e. Humidity: 40-60

f. Cleaned tools: make sure each process step has its main clean tools such as beakers, Petri dishes, and tweezers.

g. Clean room tools: filters, syringes, towels, tweezers, swabs, etc., should be appropriate for class 100 clean room with emphasis on their ability not to generate any contamination being organic, particles or ions. Tools should be stored in appropriate containers per the procedure below.

h. Storage: make sure glass plates are stored in clean, dry locations.

Now the following are the steps followed in the preparation of the liquid crystal cell

1. Cleaning

This is one of the most important and main step in the sequence. It involves the following three main steps:

A) Ultrasonic Bath cleaning B) Bake C) UVO cleaning

Steps involved in Ultrasonic Bath:

1. Rinse the substrate in DI water for at least 30 seconds.
2. Put the substrate in detergent ultrasonic bath for 15 mins.
3. Rinse in DI water for 30 seconds.
4. Put the substrate in ultrasonic bath with DI water for 15 mins.
5. Put the substrate in ultrasonic bath with acetone for 15 mins.
6. Put the substrate in ultrasonic bath with IPA for 15 mins.
7. Rinse in DI water and visually examine the substrate.
8. Blow dry the substrates.
9. Heat the substrate for about 10 mins to remove any residual water (Baking).

10. Examine the substrate by visual inspection.

(NOTE: If the pieces are coated with resist then start from step 5)

Steps Involved in UVO cleaning:

(Generally used for energizing the substrate and it improves the adhesion of photoresists and polymers)

1. If the glass is coated with ITO, place it face up in the UVO cleaning machine.
2. Turn on the air knob by a quarter rotation.
3. Keep the substrate for 15-20 minutes.

2. Spin Coating

Used to uniformly coat the surface of the glass plate with a polymer. Coating the surface of the glass plate with a polymer helps in the orientation of the liquid crystals.

1. Place the clean substrate on the spinner, centered on the chuck with the side to be coated facing up.
2. Turn on the vacuum.
3. Check if the substrate is tightly attached and is not moving (if its moving try a different chuck). It is important that the substrate should not move as it spins at a very high speed.
4. Fill a clean syringe with adhesion promoter (AP-3000) and pour it uniformly on the substrate.
5. Turn on the spin coater for 20 seconds at 3000 rpm.
6. Fill a clean syringe with BCB: mesitylene (1:3) and pour it uniformly on the substrate.
7. Turn on the spin coater for 45 sec at 5000 rpm.

Annealing:

1. Carefully move the substrate to a hot plate and heat it at 100^0 C for 1 minute.
2. Then bake the substrate at 200^0 C for 12 hours.

3. Store the substrate in a clean and dry place.

3. Rubbing

For our purpose we use a manual rubbing technique. Steps followed in rubbing are as follows:

1. Put the Substrate on a hard surface or a stage for rubbing. Make a mark with a pen or marker on the side of the rubbing direction.
2. For the purpose of rubbing we use a black rayon cloth[45]. Stretch the rayon cloth on a cubical box which is generally easy to handle. Make sure the cloth is replaced after every 50 cells. Before using blow some dry N2 on the substrate to avoid any contaminants.
3. Rub unidirectionally around 70 times and do not apply any pressure just let the surface of the cloth touch the substrate lightly. Now to make sure you are rubbing in the same direction use a rigid surface or a wall on the left side to act as a guide for your hand.
4. Take the substrate out and blow some clean dry N2 on it.

4. Spacer Application and Assembly:

1. Clean the substrate assembly and the substrate of any dust particles.

2. Mix the spacers in the UV-61 glue and take it in a clean syringe.

3. Apply a line of dots a few centimeters away from each other on the glass substrate.

4. With the help of clean tweezers lay the second glass plate on the first one make sure that the rubbing directions are parallel to each other.

5. Press the substrate together until you see a fringe and then try to adjust the pressure so that you get one uniform fringe. To avoid any deformation apply a minimum adequate pressure to the spacers.

6. If the number of fringes is too large it means that you have some deformations in the substrate originating due to dirt or the substrate itself. If this is the case it is useless to continue, try to clean the surface and replace the spacers or start with new substrates.

7. If you are satisfied with the cell assembly then cure the glue with a UV light.

5. Liquid Crystal filling

1. Take the LC bottle out of the refrigerator around 3 minutes before you start.

2. Turn on the vacuum oven to about 3 degrees more than the clearing temperature of the liquid crystal (80 degrees Celsius for our application). Just take a note that it takes around half an hour for the vacuum oven to reach that temperature so turn on the oven half an hour early.

3. Put the substrate in a clean petri dish. Make sure that the oven is preheated.

4. With a sharp and a clean needle put a drop of LC near the edge of the two substrates. Now due to capillary action the LC will fill the gap in between the two Glass plates.

5. Immediately then put the petri dish in the oven and pump the oven down to 150mBar for 2 minutes and then slowly release the pressure to normal.

6. Cool down the substrate at the rate of 0.5 degree Celsius per min till around 60 degree Celsius and then turn off the oven. Take the sample out when the temperature is around 40 degrees Celsius.

7. Visually inspect the cell for cleanliness then inspect it under the polarizer.

6.4 Results Achieved by fabrication:

From the fabrication of liquid crystal cell we were successfully able to form a liquid crystal cell with a required orientation of liquid crystals inside the cell. As discussed in section 6.2.1 a parallel alignment was achieved by unidirectional rubbing and coating the surface with a

polymer. These results can be verified from the table 6.1. The table shows the polarization angle versus the intensity of laser light passing through the liquid crystal. When the polarization of the laser is aligned with that of the liquid crystal we can see the intensity as 0.38W while when the polarization of laser is perpendicular to that of the liquid crystal we can see the intensity of light at its minimum of 0.28W which indicates we have achieved a parallel alignment of liquid crystal. There were two readings of intensity taken and then their average was plotted against the polarization angle which is shown in figure 6.2. A cell gap of around 12um was achieved which was measured using a precision scale. We also found a way to couple the light into the glass plate with the help of prism.

Angles(deg)	Intensity 1	Angles(deg)	Intensity 2	Angles(deg)	Average Intensity
0	0.38	0	0.38	0	0.38
10	0.38	10	0.37	10	0.375
20	0.37	20	0.37	20	0.37
30	0.35	30	0.35	30	0.35
40	0.34	40	0.34	40	0.34
50	0.32	50	0.31	50	0.315
60	0.32	60	0.3	60	0.31
70	0.3	70	0.3	70	0.3
80	0.28	80	0.29	80	0.285
90	0.28	90	0.28	90	0.28
100	0.28	100	0.28	100	0.28
110	0.29	110	0.29	110	0.29
120	0.29	120	0.3	120	0.295
130	0.31	130	0.31	130	0.31
140	0.32	140	0.32	140	0.32
150	0.34	150	0.34	150	0.34
160	0.35	160	0.35	160	0.35
170	0.37	170	0.37	170	0.37
180	0.37	180	0.38	180	0.375

Table 6.1 : Polarization Angle vs the Intensity of Light

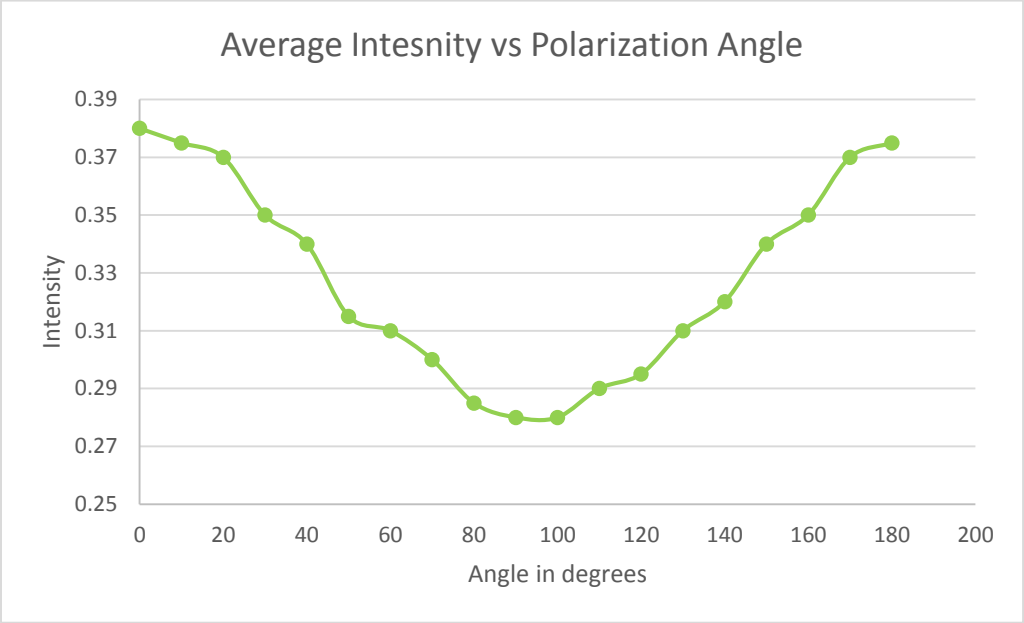

Figure 6.4 : Average intensity vs polarization Angle

Chapter 7
Conclusion and Future Work

7.1 Conclusion

The research done in this thesis focused on the electrical characteristics of Schottky barrier contacts using mainly two electrical characterization techniques. We used the I-V and C-V characteristics of the diode to extract some important parameters of the diode which include the ideality factor, barrier height and the doping concentration. All these techniques were performed under room temperature as well as varying temperatures ranging from 100K to 300K for GaN and 133K to 433K for SiC Schottky diodes. From these experiments some of the main conclusions that were derived are:

1. The ideality factor for GaN diodes is inversely proportional with temperature, while the ideality factor of SiC diode is not inversely proportional to temperature as the points considered for calculation were not in the linear regime.
2. The barrier height for SiC diode is directly proportional with temperature, while SiC Schottky diodes yielded incorrect results again since the points considered for calculation were outside the linear regime of the diode.
3. The carrier concentrations of the GaN diode were a little bit deviant in the three regions of consideration while the carrier concentration of SiC diode is same for all the three selected regions. The deviations is mainly due to the presence of traps which can be caused due to etching of the device.
4. Frequency curves of 100 KHz and 1 MHz did not show any difference in the C-V curves of GaN.

Furthermore the processing technique used for the fabrication of GaN diodes is unique. We used three etching cycles followed by a treatment of KOH to reach the unintentionally doped GaN

layer and form Schottky contacts. From the characterization experiments we can conclude that this resulted in the formation of good Schottky contacts on the diode.

From the fabrication of liquid crystal cell we were successfully able to form a liquid crystal cell with a required orientation of liquid crystals inside the cell. A cell gap of around 12um was achieved. We also found a way to couple the light into the glass plate with the help of prism.

7.2: Future Work

As the results of Ideality factor and the barrier height of SiC schottky diode were incorrect we need to perform the same experiment on Keithley 2612 source meter which was used for measuring the characteristics of GaN schottky Diodes. There are lot of deep level traps associated with GaN diodes due to the etching and cleaning processes. So we can perform DLTS (Deep level transient spectroscopy) to find out trap locations and once these are known we can also find activation energies of these traps.

The fabrication of the non-mechanical beam steerer can be continued to properly form a clear liquid crystal cell and then apply proper voltages to the designed electrode to observe the deviation of the coupled light beam.

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