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A HIGH-EFFICIENCY SWITCHED-CAPACITANCE HTFET CHARGE PUMP FOR LOW-INPUT-VOLTAGE APPLICATIONS

A Thesis in

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ABSTRACT

High-efficiency power delivery, as well as low-power circuit design continues to be an important concern in energy harvesting circuits and application that are limited by the battery capacity. This thesis presents a high-efficiency switched-capacitance charge pump in 20 nm III-V heterojunction tunnel field-effect transistor (HTFET) technology for low-input-voltage applications. It provides for higher efficiency than the conventional CMOS solution. The proposed circuit doubles the ratio of input voltage to output voltage, which is strongly related to its high efficiency. The state of art CMOS-based conventional switched-capacitance charge pump achieve power efficiency as 82% and output as 1.8V with 1.0V input voltage with 130nm technology.

The steep-slope and low-threshold HTFET device characteristics are utilized to extend the input voltage range to below 0.20 V. Meanwhile, the uni-directional current conduction is utilized to reduce the reverse energy loss and to simplify the non-overlapping phase controlling. Furthermore, with uni-directional current conduction, an improved cross-coupled charge pump topology is proposed for higher voltage output and power-conversion-efficiency (PCE). Simulation results show that the proposed HTFET charge pump achieves 90.4% and 91.4% power conversion efficiency with a 1.0 kΩ resistive load. The DC results obtained are 0.37 V and 0.57 V, when the input voltage is 0.20 V and 0.30 V, respectively.

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ACKNOWLEDGEMENTS

I would like to dedicate this dissertation to my parents whose love, support and understanding has always motivated me to strive for excellence.

I would like to express my heartfelt gratitude to my advisor, Vijaykrishnan Narayanan. His enthusiasm and constant encouragement in this exciting research of ultra-low-power HTFET based DC-DC converter was vital is my progress in research. I achieved intellectual as well as personal growth during the course of my research with him. I would like to convey my special thanks and appreciation to Ph.D. Xueqing Li and Ph.D candidate, Moon Seok Kim. They instilled in me the importance of collaborative research and self-learning.

Finally, I would like to acknowledge Prof. Kyusun Kim, and Dr. Suman Datta who introduced me to emerging devices that substitute CMOS-based FET and simulation tools which were instrumental in obtaining the thesis results.

Chapter 1 Introduction

Wearable biomedical devices requires portable, high efficient and wearable system design. The functions of wearable electric devices are able to empower environmental health monitoring and to respond to emergencies. Recently, the advanced rechargeable battery or high-density super battery has been able to accumulate power from external sources such as RF-energy, heat energy, light energy and vibrational energy with energy controllers. Direct-current-to-direct-current (DC-DC) converter is a part of the controller to extract energy from unusable energy and make it usable and fit into specific electric gadgets. The material implemented in wearable electric devices in the human body requires to be harmless. Also, it should be small in size thus requiring the use of nanotechnologies. The major concern for determining the size and weight is usually the energy consumption of integrated circuits and sustainability to meet the usage in the human body.

1.1 Emerging Devices for Energy Harvesting Systems

In the last few decades, the semiconductor industry follows Moore's law which reduces the cost of one transistor and increases the number of gates in a single chip. CMOS has been improved by new high mobility channel material (e.g. SiGe, III-V, etc) and new planar transistor structures such as multi-gate, silicon-on-insulator, FinFET enables better electrostatics with 1-D material (nanowire, carbon nanotube). CMOS-based high scaled devices faces power dissipation challenges due to parasitic internal resistance and capacitance. Over the last decade, the transistor architecture has gone through notable changes and various alternative models have been

proposed. Alternative transistor architectures which has much lower energy than that of MOSFET are suggested as novel mechanism or non-charging state variable.

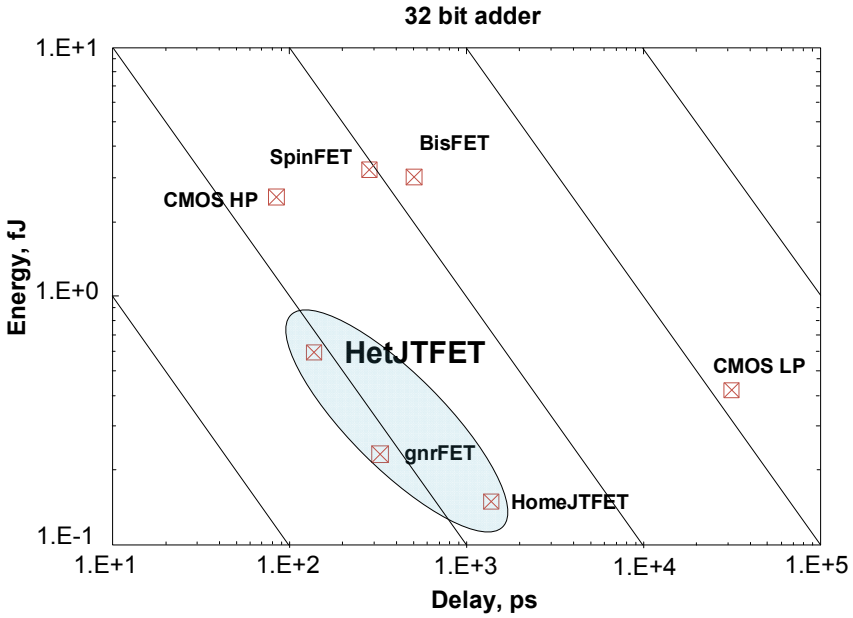


Figure 1-1. The benchmarking evaluation from [2].

Nikonov and Yang at Intel (Figure 1-1) reported performance evaluation for beyond-CMOS devices and CMOS extension devices [2]. CMOS extension devices operate charge-based device utilizing conventional field-effect mechanisms such as CMOS HP and CMOS LP. As a dominant transistor which has charge-based novel mechanism, tunnel FET (TFET) has lower energy than that of HP CMOS and shorter delay than that of LP CMOS. Differ from CMOS-based device, Tunnel FET (TFET) comprises tunneling as a channel transport mechanism. One beneficial model for Tunnel FET, III-V Heterojunction Tunnel FET (HTFET) can operate below 0.2V and has important characteristics such as steep subthreshold slope (SS). The pros and cons of the characteristics of this model in comparison with the original CMOS will be discussed in Chapter 2.

Harvesting energy from the human body environment by using thermoelectric generators (TEG) has a range of 10mV/K to 50mV/K which varies on its process and size. The output voltage generated with TEG's for body-wearable applications is as low as 50mV for temperature differences of 1-2K. The output voltage range of a single solar cell is 500-600mV outdoors and 100-200mV indoors [2]. The threshold voltage limits are higher than the generated voltage of the harvested energy. Thus a low-startup voltage step-up DC-DC converter is required to kick-start the system. The core part which determines the aggregate power efficiency is charge pump topology because other control designs can be optimized depending on the switch characteristics. The charge pump topology, however, results in different power efficiency. In the chapter 3, several designs of charge pump with HTFET would be discussed with pros and cons. However, this thesis does not cover the startup logic because it requires an inductor whose area is much larger than capacitance.

1.2 Self-powered Operation

With primary batteries, the operation of traditional electric devices is predictable due to the independent nature of the ambient condition. However, traditional batteries are limited by their lifetime and replacement in wearable biomedical devices. Also, aging effects reduce the usable capacity in the battery and generate harmful and toxic residues and disposal. The undesirable issues for wearable devices require self-powered system with sustainable operation, which is called energy harvesting system. Collected energy from the ambient environmental is then transformed to usable energy in storage. There are mainly four harvested energy sources, including RF-energy, vibrational energy, thermal energy and light energy.

The first source, RF-energy harvesting, uses a primary receiver antenna which produces the resonant states and works with an inductive link. Biomedical devices which implement secondary receiver antenna collect energy from inductive-based vibration energy generated from primary coil

outside of body. However, transmitting low power inductive energy is not preferable due to unpredictable coupling factor which is challenging due to coil misalignment. The other source of vibrational harvesting energy is exploited by surface charge generated by pressure, vibrations or force in piezoelectric energy harvesting systems [3] [4]. Thus, the harvesting device is useful in equipped footwear, not in human body because the power can be scavenged from human gait motion. The other issues in vibration harvesting source is that they are particularly sensitive to the frequency and have limited bandwidth for peak power.

On the other hand, thermal energy and light energy are promising in wearable biomedical devices (except for the restriction mentioned in Section 1.1). Thermal energy is harvested using TEGs which convert temperature difference into electric energy. Charge carries moves from hot end to cold end, which generate a quite-low voltage at the power load. Emerging device and startup system can guarantee robust operation. Light energy is dependent on the external environment, but the generated energy is not as it obtained directly in the form of DC voltage and produces no harmful waste.. In addition to this, the portable device produces a much higher power than other harvesting sources.

Self-powered systems must guarantee reliability in energy harvesting, efficient power conditioning and storage management. However, the generated power from energy harvesting varies because the power source depends on the ambient environment.

Figure 1-2. Energy harvesting application

As shown in Figure 1-2, energy harvesting application guarantees functionality of energy harvesting with desired power conversion efficiency. There are two different functionalities, namely, power conditioning and power management. Power conditioning system ensures the functionality and change to a desired regulated voltage. Power management system guarantees long system run time with efficient operation. The most important component in circuit level design is DC-DC converter.

1.3 Organization of Thesis

Chapter 2 discusses the TFET device characteristics and the circuit simulation module set-up used to simulate HTFET based DC-DC converter. The FINFET design which has a higher range of operation voltage is compared with the TFET design. Chapter 3 describes several types of DC-DC converter and discusses the advantages and disadvantages for each DC-DC converter. Based on these, the path of improving the performance of original DC-DC converters with TFET device is explained. The main challenge for designing a DC-DC converter would be discussed with simulation result comparisons in Chapter 4. Finally, the future work is discussed in Chapter 5.

Chapter 2

HTFET Characteristics and Modeling

In this section, the advantage and disadvantage of HTFET technology characteristics will be discussed along with comparisons with Si-FINFET. As a substitution for CMOS technology, HTFET is attractive because a lower threshold voltage with a low supply voltage. This enables less static power consumption while satisfying the performance metric. However, there is a key challenge by optimizing dynamic power due to internal parasitic capacitance in HTFET based phase generator. Recently, a TFET based digital and analog design has been proposed with significant performance improvement by voltage scaling and unconventional FET characteristic [3] [4] [5]. This section discusses the device characteristics, current purposed literature analysis and HTFET simulation module set-up.

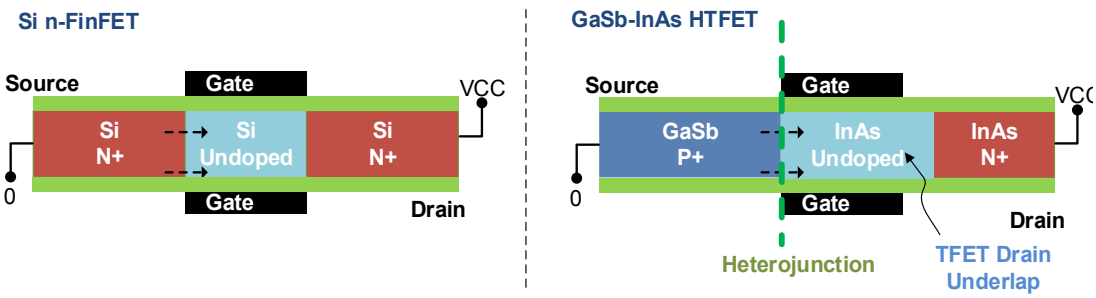


Figure 2-1. Device structure for n-type Si FinFET and n-type GaSb-InAs HTFET [8]

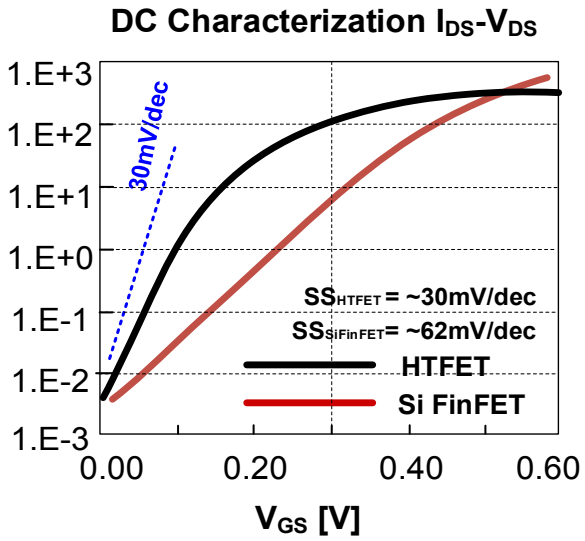


Figure 2-2. DC characterization HTFET and Si-FinFET sub-threshold slope

2.1 HTFET device characteristics

2.1.1 Step-slope with A Low Input Voltage

The motivation for the design of Steeper switching inter-band TFET is to structurally control on-state current and off-state current. In MOSFET, carriers have higher energy than the thermal electrostatic potential barrier which can then contribute to the on-state current (Ion). These carriers are distributed by the Fermi-Dirac probability and the energy slope of kT is achieved at source/drain p-n junction. This energy causes a slope higher than 60mV/dec (~2.3kT/q) at 300K in MOSFET [6] [7]. Different from the MOSFET, TFET has asymmetrical source/drain doping as shown Figure 2-3 and a structurally gated p-i-n tunnel diode. The gate voltage controls the band-to-band tunneling window through which carriers inject through at source/channel, and a sub-60mV/dec SS can be achieved when it opens. III-V material as well as heterojunction yields

higher energy efficiency with smaller SS and a larger on-state current of III-V HTFET, than that of the state-of-the-art CMOS technology at a low VCC (< 0.5V) [3]. As shown in Figure. 2-2, I-V curves illustrate that with the same off-state leakage current, TFET provides 7x larger switching current than MOSFET [7] [5] [8] [9].

2.1.2 Uni-directional Tunnel Conduction without Substrate Modulation

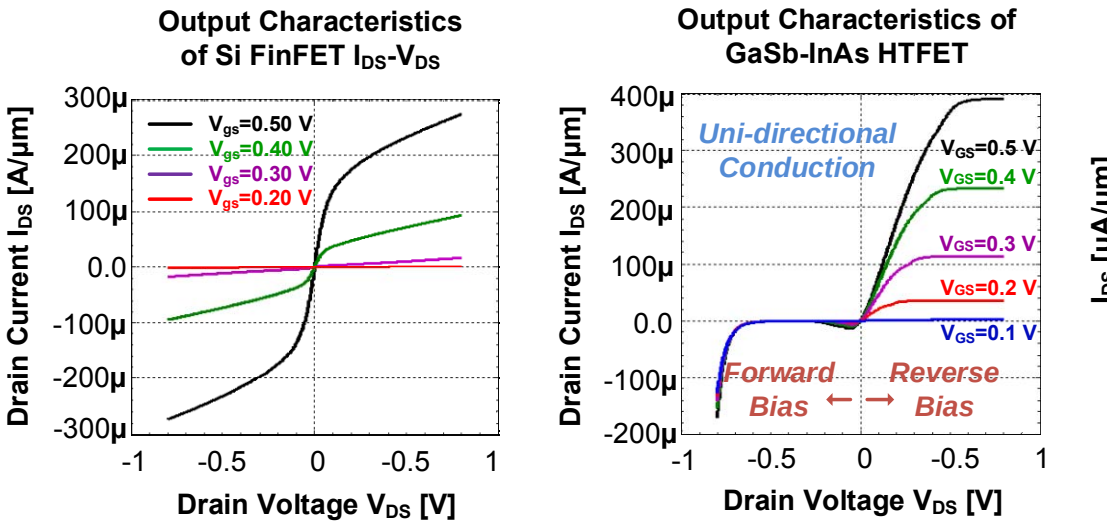


Figure 2-3. I-V curves for Si FinFET and HTFET [7] [5] [10].

MOSFET has a symmetrical source/drain structure, Figure.2-3 shows bi-directional conduction due to the asymmetrical p-i-n structure, TFET has unidirectional conduction. On-state current significantly increases before entering the saturation region as V_{DS} (reverse bias condition) increases and when V_{DS} is negative, there is negligible current between drain and source. TFET is not bounded by the top of energy barrier such as MOSFET and the source region in an n-type TFET is p+ doped, which induces the band-to-band tunneling as applying the gate-voltage. Thus,

TFET is controlled differently from source-channel energy barrier in MOSFET. (Figure 2-1) [7] [3] [5].

Unidirectional conduction is totally distinguished with the characteristic of MOSFET and this characteristic is the primary reason that results in the modification of bi-directional and uni-directional switching circuit design with TFET because it can suppress the reverse leakage current, thus achieving higher power efficiency.

2.1.3 Miller Effect in TFET

Different from MOSFET structurally, TFET reveals enhanced miller capacitance (Cgd) due to asymmetric and double gated structure. As shown in Figure 2-4, different capacitance characteristic is illustrated for MOSFET and TFET at 0.5V supply voltage. It is normalized to gate oxide capacitance on gate-to-source (Cgs), gate-to-drain (Cgd), and aggregation (Cgg) on TFET. While Cgs dominates total capacitance (Cgg) in MOSFET, Cgd (miller capacitance) dominates total capacitance in TFET. Miller capacitance causes voltage overshoot in the transient response, which degrades the dynamic energy performance. In high frequency devices, the effect of Miller capacitance has a strongly bad effect on time delay and energy performance with complicated switching node in TFET devices [11].

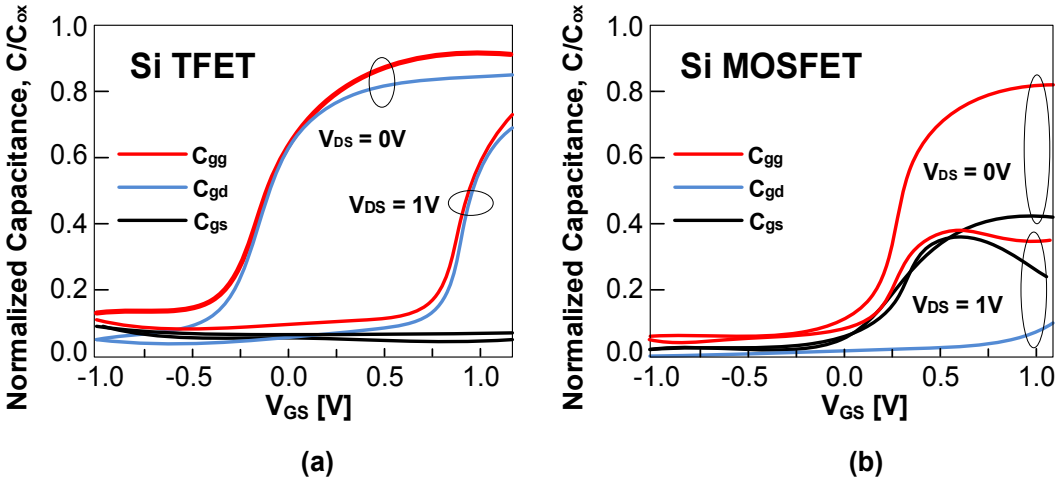


Figure 2-4. Capacitance-voltage characteristics showing the gate (Cgg), gate-to-source (Cgs) and gate-to-drain (Cgd) capacitances as a function of gate to source voltage, VGS, for (a) Si TFET and (b) Si MOSFET

For a component like an inverter buffer of DC-DC converter design with high frequency, miller effect is a challenge to overcome and compromise to optimization. However, [5] points out miller capacitance enhances the storage nodes coupling and helps with node recovery by radiation, thus achieving better soft error resilience in SRAM design.

2.2 HTFET-based Device Circuit Implementations

Currently, based on the TFET characteristic, the papers proposed suggest different circuit design for each device [3] [4] [5] The following three papers are reviewed with primary TFET characteristics for each device performance improvement.

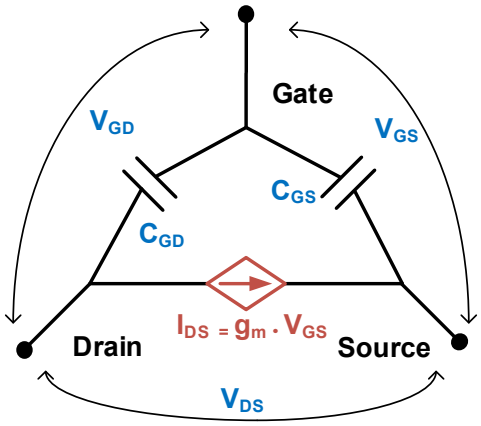
Vinay Saripalli's paper [3] proposed variation-tolerant TFET SRAM design using Schmitt-Trigger feedback approach in improving the read/write noise margin. TFET enables low-VCC

operation on SRAMs, thus it provides 1.2x reduction in dynamic power. TFET based SRAM provides 13x leakage power reduction compared to CMOS-based SRAM, thus reducing power consumption on his implementation. [3]

Matthew Cotter's paper [4] focus on performance characteristic by various TFET-based flip-flop designs. He addresses additional transistor requirements and evaluates performance on each modified design in comparison with Si-FinFet design. Transmission-gate flip-flop (TGFF) and Semi-Dynamic Flip-Flop (SDFF) employs the bi-directional property on the operations. Thus, unidirectional conduction of TFET-based design requires one additional transistor. The most critical performance improvement can be achieved in most notable pseudo-static D flip-flop (DFF) by transistor sizing with low power operation and not implementing feedback logic due to unidirectional conduction characteristic. Compared with FinFet-based DFF, he provides 67% reduction in dynamic power and 9x reduction in leakage energy. [4]

Huichu Liu's paper [5] pointed out the effect on modeling techniques and performance by diverse aspect of TFET analog devices compared to CMOS technology-based devices. An analog device takes advantage of steep switching of TFET to enable further energy saving by improving the circuit sensitivity. On the other hand, circuit design requires modification and optimization with unique characteristic of TFET which is described in chapter 2.1. The paper [5] has performance comparison on radiation resilience at low VCC between TFET and MOSFET and illustrates that due to miller effect, key challenge on low power CMOS circuit design soft error has been improved. [5]

2.3 HTFET Device Simulation Set-up



$$I_{DS} = g_m * V_{GS}$$

$$= \text{LookupTable}(V_{GS}, V_{DS})$$

$$I_{GD} = \frac{d}{dt}(C_{GD} * V_{GD})$$

$$I_D = \frac{d}{dt}(Q_D)$$

Figure 2-5. HTFET circuit-level Verilog-A model [3] [8].

TCAD Sentaurus is an optional tool used to build the accurate Verilog-A simulation model before a fully-developed compact SPICE model is available [12]. By calibrating experimental data based on fabricated III-V TFET data, it is able to simulate DC and transient characteristics accurately [13]. This thesis utilized this verilog-A simulation model with SPECTRA simulator for emerging device-based circuit design and performance analysis. TFET Verilog model data are simulated by referring look-up table with IDS(VGS, VDS), CGS(VGS, VDS), and CGD(VGS, VDS) as shown in Figure 2-5 [3] [8]. However, because Verilog-A simulation is based on reading three two-dimensional look-up table text file in every time, it takes a longer time than normal SPECTRA simulations with compact models.

Chapter 3

Kinds of DC-DC Power Converter and Kinds of Topology

3.1 Types of DC-DC Power Converters

There are two major step-up converter designs to consider for self-powered devices, switch mode power converter and switched-capacitance power converter. The following is a discussion on the two major power converter designs, i.e. the switch mode power converter and switched-capacitance power converter. [16]

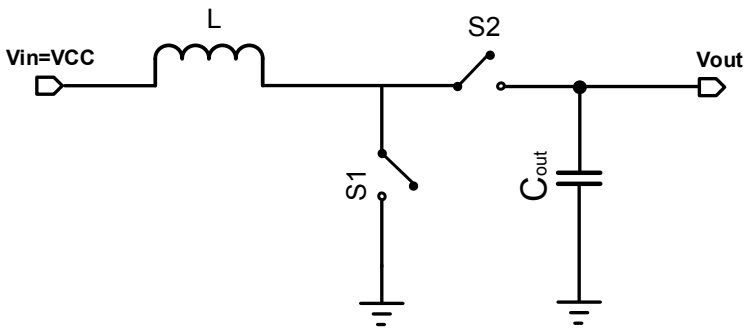


Figure 3-1. Power stage topologies of switch mode power converter for boost voltage converter.

3.1.1 Switch Mode Power Converter

Switch Mode Power Converter is broadly implemented because the controller generates stable output with varying input voltage in energy harvesting system. The design uses inductor for converting input energy into magnetic coils during one charge phase and converts DC voltage as the device need in the other phase. Other element needed for this design is the phase generator and feedback controller which controls phase controller or duty cycle of phase controller to obtain the

desired output voltage. The expected power conversion efficiency is over 90%, which is the primary advantage among DC-DC converter designs.

The primary power loss for the design is the switching transistor dissipation (dynamic power loss) in switching phases. The basic design has only two transistor switches for changing the phases. Including feedback control logic and phase generator, the design consumes more energy in controlling than the voltage doubler logic would, due to its complex design.

As a downside, most low-cost and space-limited devices have challenges due to sizable dimensions of the integrated inductor and insufferable electromagnetic interface (EMI). The state-of-the-art inductor, spiral inductor, has been proposed and is integrated with radio-frequency filter and voltage-controlled oscillators (VCO). However, it has limited quality factor (Q) which is related with the parasitics of the inductor. The resultant efficiency with spiral inductance is much lower than the commonly used external inductors. When it comes to on-chip design for dc-dc converter, switch mode power converter is not applicable.

3.1.2 Switched-Capacitor Power Converter

An alternative design for induction-based DC-DC converter, the switched-capacitance DC-DC converter is more applicable because an array of switches substitute the magnetic coils. Tthe array of capacitors store energy instead of the inductor. In other words, the pumping capacitor stores charge in one phase and transfers the energy to output power level in another phase.

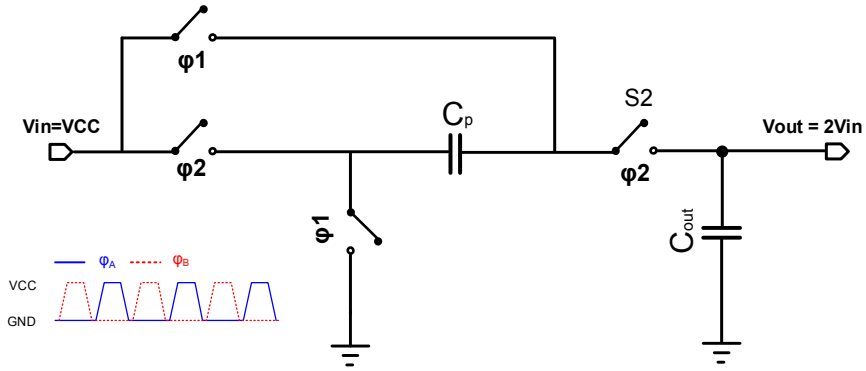


Figure 3-2. Circuit schematic of charge pump

The advantages of switched-capacitor DC-DC converter include a low fabrication cost, high switching frequency, medium-to-high conversion efficiency, and reduced voltage-mode electromagnetic interference (EMI). In addition, HTFET uni-direction tunnel conduction suppresses the reverse current and improves the conversion efficiency. The steep slope with low voltage and lower dynamic power loss as compared to CMOS technology design is also favorable.

However, switched-capacitance DC-DC converter is challenged with nonzero switch on-resistance which is related to the signal-dependent current spike. Hence, ultra-low voltage range device suffers from a much larger on-resistance on switch, which dissipates energy and reduces the power efficiency. The larger ratio between the effective gate width and the effective gate length of the switch has lower on-resistance value.

Another obstacle for the design is the parasitic capacitance that introduces a power loss (as shown in Chapter 2). This is a challenge for HTFET circuit design due to higher miller capacitance than that of FinFET. Existing commercial switched-capacitance DC-DC converters are fabricated with the use of off-chip capacitors to preserve high conversion efficiency. However, portable ultra-low voltage devices prefer on-chip design, which does not allow the

external capacitor. Hence, the complexity of design and how the design makes an effect on the on-resistance is principal for power conversion efficiency. A more complicated design increases the aggregate internal capacitance and dynamic power loss during switching of phases.

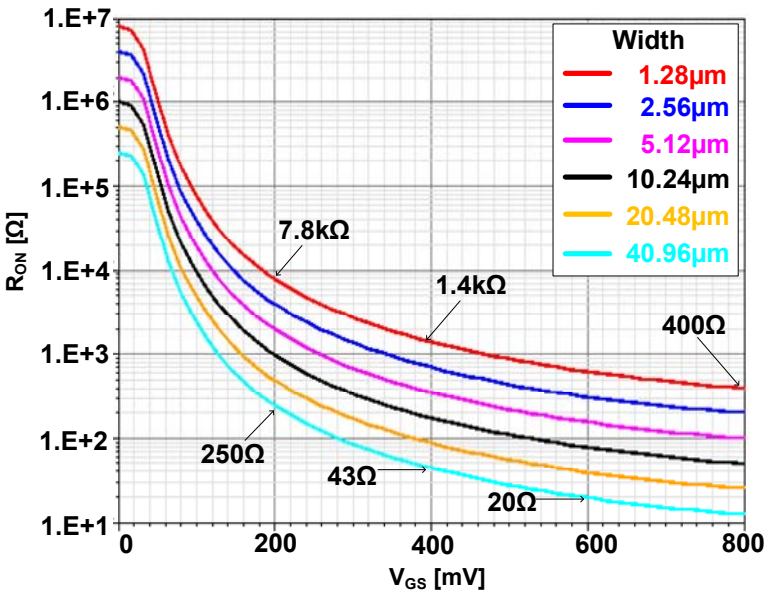


Figure 3-3. On-resistance of HTFET switches versus gate-source voltage VGS.

To maintain an accurate output voltage, another necessary component for the design is a closed loop feedback controller and phase generator to maintain a desired voltage level. The control logic power optimization is important issue for higher conversion efficiency.

3.2 Types of Switched-Capacitance Topology

3.2.1 Dickson charge pumps

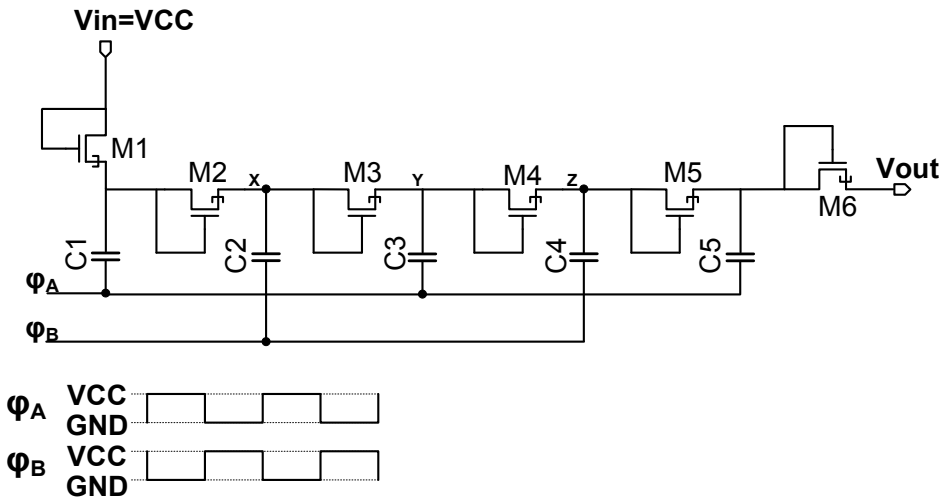


Figure 3-4. HTFET-based Dickson charge pump.

The most commonly used step-up switched converter topologies is the Dickson charge pump. A recently proposed start-up mechanism DC-DC converter used this topology and it has been improved since. The first proposed topology uses diodes as switches as illustrated in Fig 3-4. When φ_A decreases to a low voltage, the voltage on the top plate of the capacitor C1 is biased to (V_{in}-V_{thn}), where V_{in} is the power supply voltage and V_{thn} is the threshold voltage of an n-type switch. When φ_A increases to a high voltage, the voltage on the top plate of the capacitor C1 is biased to ($2V_{in} – V_{thn}$), while the voltage on C1 remains biased to closely (V_{in}-V_{thn}). When a higher voltage is set at the diode switch M2, C2 is charged as ($2V_{in}$-$2V_{thn}$). Finally, the output voltage of an N-stage Dickson charge-pump circuit is ideally generated as $N*(V_{in} – V_{thn})$.

The major drawback of the Dickson charge pump is the threshold voltage drop across each diode-connected transistor, which reduces the power conversion efficiency significantly. The on-resistance of each diode could be calculated by threshold voltage drop. For ultra-low-power applications, V_{in} is close to or below the threshold voltage range. The conventional Dickson charge-pump circuit will not work properly with high efficiency.

3.2.2 Dickson charge pumps with bootstrap control

To mitigate the voltage drop due to threshold voltage in the start-up stage, improved Dickson charge pumps are proposed. Static charge transfer switch is the one of the most enhanced technique.

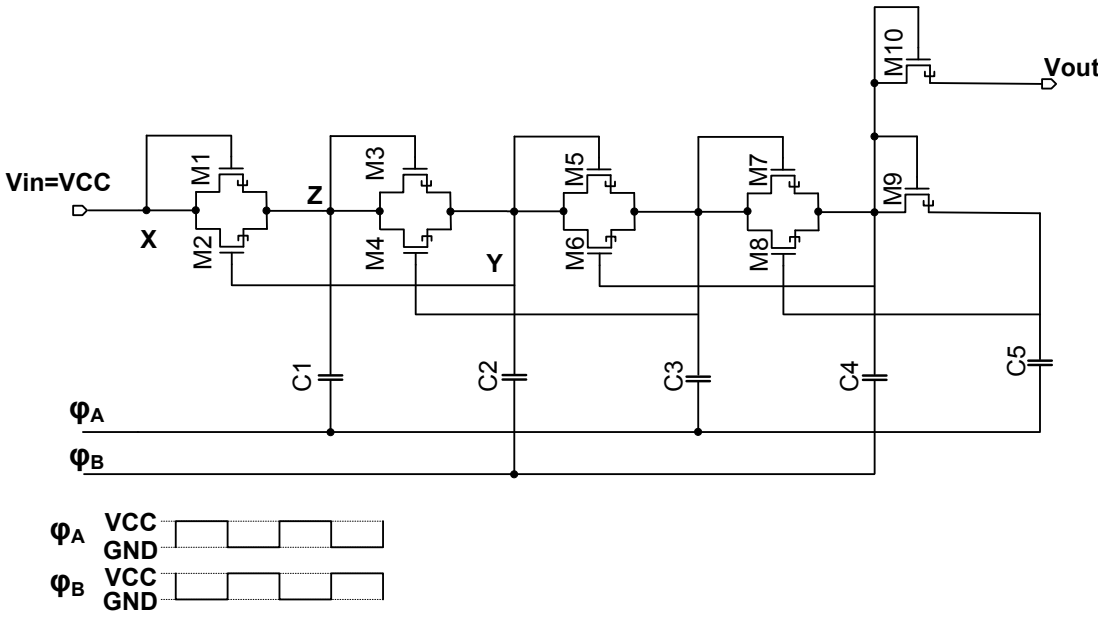


Figure 3-5. The HTFET-based improved Dickson charge pump.

As shown in Fig3-5, with the initial startup, V_{in} is set to the drain of two coupled N-type devices, with the top being a diode-connected N-type transistor and the other an N-type charge transfer switch whose operation is controlled by the top-plate voltage of capacitor C2. C1 is charged to (V_{in}- V_{th}), φ_A goes up to V_{dd} and ($2V_{dd}$ - V_{th}) has been biased in Z. Hence, Y has been biased by ($2V_{dd}$ -$2V_{th}$) and the input voltage of M2 has been supplied by ($2V_{dd}$- $2V_{th}$). Due to the subsequent higher input voltage on M2, the start-up threshold voltage is significantly reduced with higher efficiency. Similar to the bottom charge transfer, the bottom charge transfer supply increases by (V_{dd} - V_{th}) from the initially supplied input voltage to gate. The drawback for CMOS-based design is the bottom transfer switch cannot be completely turned-off after the charge from the later stages is transferred. However, HTFET-based design is not affected by leakage current due to a HTFET switched-capacitance characteristic, unidirectional tunnel conduction.

3.2.2 Cross-coupled Voltage Doubler

The Dickson charge-pump is a not complicated design and is straightforward, but the conversion efficiency is low especially in low-supply-voltage and is not area efficient. However, cross-coupled switched capacitance DC-DC converters cover less area and have higher conversion efficiency. Due to optimized on-resistance of switch, it is most widely used in ultra-low voltage application. Underlying theory, key parameters, and optimization of performance are discussed in the following.

The Circuit and Operation Theory

As shown in Figure. 3-6, the circuit operates can be described as follows. Assume φ_A and φ_B are non-overlapped phase control signals ranging from GND to VDD. When φ_A goes low and

φ_B goes high, V1 reduces to VDD and V2 increases to 2VDD. NM1 and PM2 are turned on while NM2 and PM1 are turned off. As a result, the output node is connected to node V2 through the on-state PM2, and the top plate of capacitor *C*1 is charged to VDD through the on-state NM1. Similarly, in the opposite phase, when φ_A goes high and φ_B goes low, NM2 is turned on and the top plate of capacitor *C*2 is charged to VDD and the output node is connected to V1 through PM1.

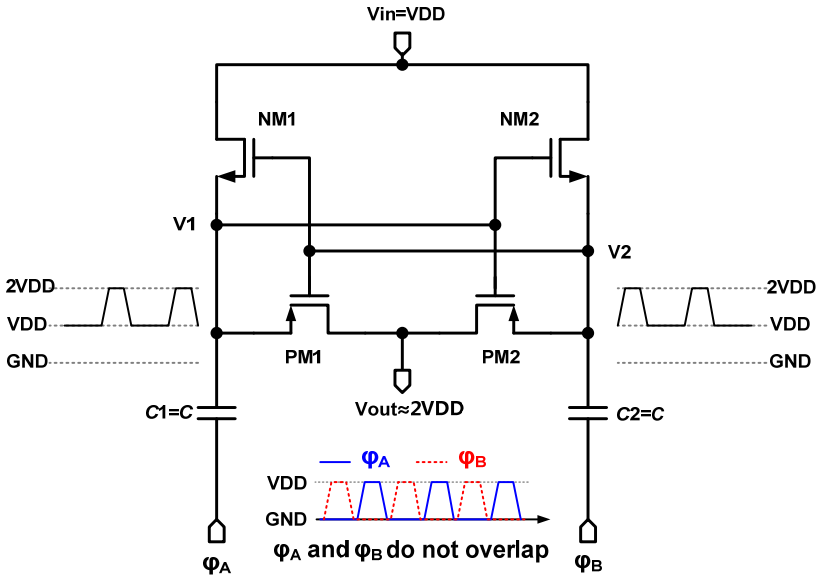


Figure 3-6. A conventional cross-coupled charge pump.

The PCE Analysis and Design Challenges

As the most critical parameter in the charge pumps, the power efficiency is given by [14] [15]

$$\eta = \frac{E_D}{E_L + E_D}, \qquad (1)$$

where E_L represents the lost energy as

$$E_L = 2C_s V_{in}^2 + 2C_p \Delta V_{out}^2, \qquad (2)$$

where ΔV_{out} is voltage drop due to R_O, C_P is pump capacitance ($C_p = C_1 = C_2$, in Figure 3-6) and C_s represents equivalent parasitic capacitance with each pump capacitance, which is called the total stray capacitance

$$C_S = \alpha \cdot C_p \qquad (3)$$

The Energy losses in equation (2) is expressed as the two kinds of loss, one due to parasitic capacitance, C_s and another due to pump capacitance, C_p. The losses usually limit the peak efficiency of the converter. A direct non-desirable effect on this process is the charge and discharge of two capacitance in every clock cycle. As an example, for gain setting 2, the parasitic capacitance C_s charges to V_{in} in switch-off state (phase 1) and to ground in switch-on state (phase 2), wasting an energy of $C_s V_{in}^2$. The pump capacitance charges V_{in} in phase 1 and discharge ΔV_{out} due to the output resistance including load resistance in phase 2. This causes an energy waste of $C_p \Delta V_{out}^2$. The schematic in Figure 3-6 is interleaved by two charge pump capacitance and the total losses every clock are expressed in equation (2). One of the major design snags with respect to the schematic is that parasitic capacitance directly effect the conversion efficiency. The load resistance R_L comprises of switch on-resistance and the simulated SC resistance. The SC resistance is driven by the switching of internal capacitance. ΔV_{out} depends on the total parasitic capacitance and the load resistance, R_L. To the first-order approximation, R_o can be expressed as

$$R_o \cong \begin{cases} \dfrac{1}{2 f_{clk}(1+\alpha)C_p}, & \text{iff } f_{clk} < f_{cutoff} \\ R_{on}, & \text{iff } f_{clk} \geq f_{cutoff} \end{cases} \qquad (4)$$

where t_{sw} represents the switching delay of non-overlapping clock, and f_{cutoff} is represented as [18].

$$f_{cutoff} = \left[2R_{on}(1+\alpha)C_p + 2t_{sw} \right]^{-1}. \qquad (5)$$

where f_{clk} represents switching frequency In equation (1), E_D represents the delivered energy as

$$E_D = 2\int_{V_{in}}^{2V_{in}} Q_c dv = \frac{V_{out}^{\ 2}}{f_{clk} R_L}, \qquad (6)$$

where Q_c is the charge delivered from each capacitor [19]. The output signal is interleaved by two phases, and accordingly, the delivered energy E_D is composed of energy from the two capacitors in two phases. In respect of the energy form only one capacitor (C1 or C2), when calculating delivered energy in each phase, voltage drop would be V_{in}.

In the steady state, the charge stored in each capacitor delivered to the load is

$$Q_c = 2C_p[V_{in} - (V_{out} - V_{in})] = \frac{V_{out}}{R_L} T_S. \qquad (7)$$

where T_S represents switching time **Error! Reference source not found.**. In the ideal case, V_{out}=2V_{in}. Considering the on-state resistance R_{on} of the switches PM1 and PM2, the output voltage of the charge pump becomes

$$V_{out} = 2V_{in} \frac{R_L}{R_L + R_{on}}. \qquad (8)$$

From equation (5), it is intuitive to notice the I-R drop voltage consumed by the non-zero R_{on}. The overall conversion efficiency of the cross-coupled charge pump is then expressed as [18]

$$\eta = \frac{1}{1 + \alpha \cdot C_p \cdot f_{clk} \frac{(R_L + R_0)^2}{2R_L} + 2C_p \cdot f_{clk} \frac{R_0^{\ 2}}{R_L}} \qquad (9)$$

From the equation (4) and (9), overall efficiency increases with f_{clk} until f_{clk} is larger than f_{cutoff}. When f_{clk} exceeds the f_{cutoff} limit, overall efficiency decreases with f_{clk}. For high efficiencies, practical range of frequency would be limited by f_{cutoff} [18].

Chapter 4

Cross-coupled charge pump design challenge

4.1 Improved Cross-Coupled Charge Pump Design

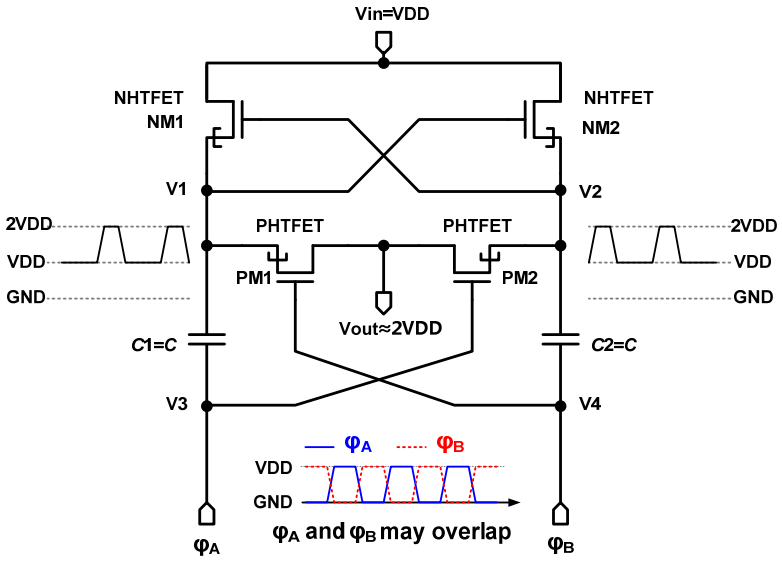


Figure 4-1. Proposed cross-coupled HTFET charge pump.

Figure 4-1 shows the proposed improved cross-coupled charge pump for the HTFET DC-DC converter. By exploring the steep-slope characteristic of HTFET in low-voltage region, and using the improved cross-coupled charge pump topology, the DC-DC converter outperforms conventional CMOS converters in three aspects: (a) the ability of low-input-voltage operation, (b) operation with overlapping clock and (c) improved cross-coupled charge simulated in Section 4, this advantages convey higher power efficiency.

4.1.1 Low-Input-Voltage Operation

HTFET which has low voltage operating due to low threshold voltage makes DC-DC converter operation with low voltage (>0.2). The characteristic of deep slop is critical role when voltage difference between voltage supply and threshold voltage.

4.1.2 Simplified Phase-Control Clock Generation

In conventional cross coupled charge pumps, the two phase control signals are usually designed to be non-overlapped to prevent the current leakage from the nodes V1 and V2 to VDD (Figure 4-1). On the contrary, in the HTFET based cross-coupled charge pump, such leakage current becomes negligible because of the uni-directional tunneling conduction. As shown in Figure 4-2, the amount of leakage charge during a phase-switching is less than 0.01 percent of the forward charge. Therefore, in the proposed DC-DC converter, the phase control clocks needs not be non-overlapping, and accordingly, circuit realizations are simplified and the power efficiency becomes higher by avoiding the non-overlapping phase generation.

4.1.3 Improved Cross-Coupled Charge Pump

Different from conventional cross-coupled charge pumps, in the proposed charge pump shown in Figure 4-1, the gate source in PM1 and PM2 connected to bottom of capacitance, which operate same as conventional converter because PM1 is connected when V4 is low and V1 is 2VDD, and PM1 is disconnected when V1 is VDD and V4 is VDD. The biased voltage in PM1 and PM2 is VDD in conventional converter, and 2VDD in proposed converter. Higher biased voltage would increase drain-to-source current which means that on-resistance is reduced. Increase drain-to-source current drives faster settling time shown as Figure 4-3. By the equation (9), reduced on-

resistance drives higher efficiency. By the equation from (8), output voltage in proposed converter is higher than conventional converter.

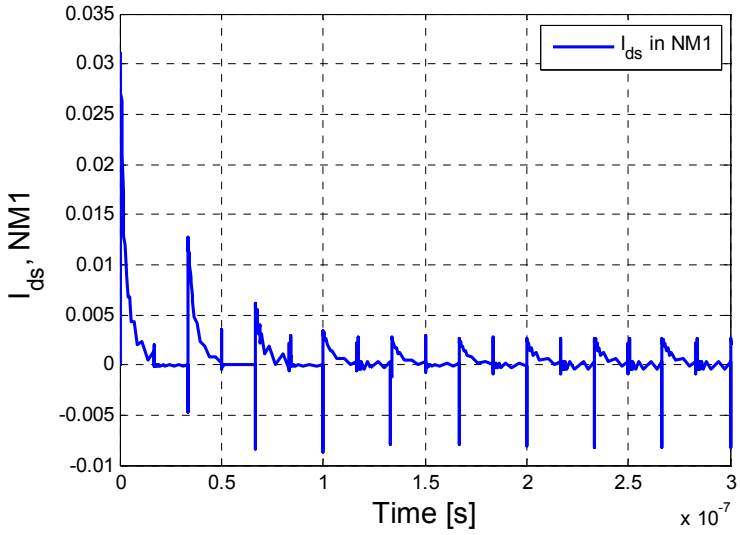


Figure 4-2. Current from drain to source of NM1 in Figure 4-1.

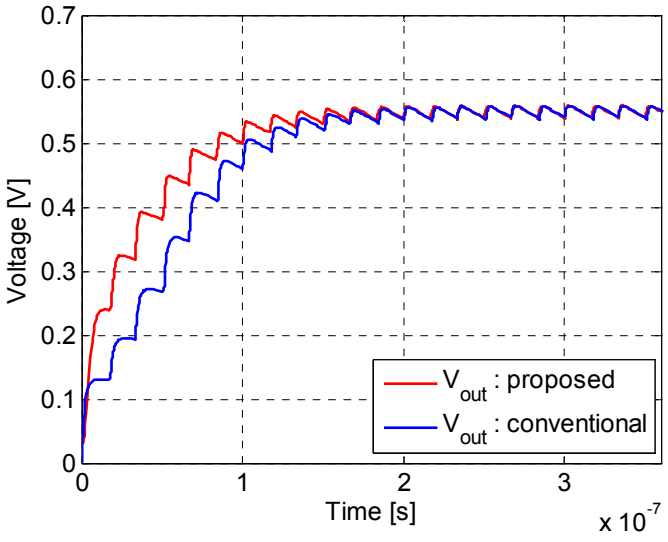


Figure 4-3. Settling time comparisons between proposed and conventional converter

4.2 HTFET Charge Pump Optimization

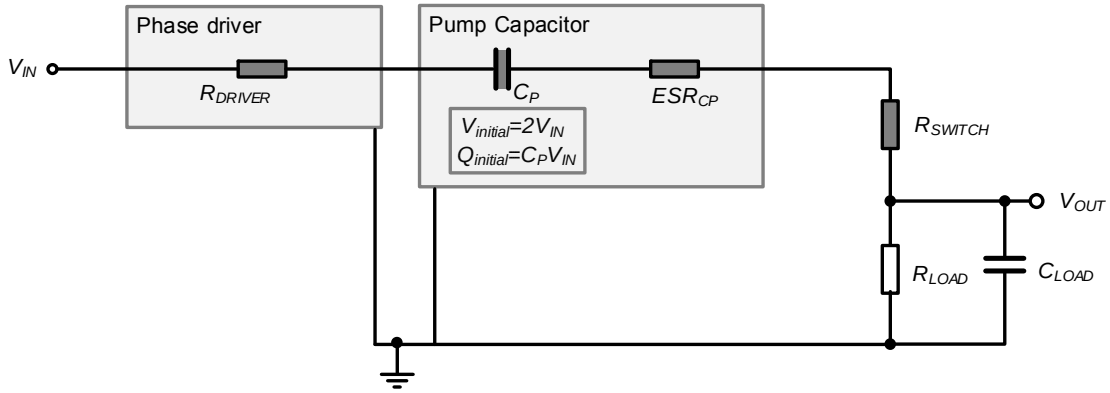


Figure 4-4. Equivalent simplified circuit of the charge pumps in Fig. 2-5 and Fig. 4-1.

Optimizations of the switch size and the pump capacitor C_P are presented for a high PCE. In the simulations, the phase control driver has the same transistor size as the switches in the charge pump. This setting is based on the fact that R_{DRIVER} of the phase driver and R_{SWITCH} of the switch are in series and affect the output in the same way, as illustrated in Figure 4-1. The phase control clock frequency f_{CLK} and the load resistance R_L are set to be 30 MHz and 1.0 kΩ, respectively.

Fig. 4-5 show the simulated PCE and DC output voltage V_{OUT} versus the pump capacitor C_P and the switch size, respectively. When C_P is less than 100 pF, the pumped charge through C_P is insufficient to drive the load, resulting in a low V_{OUT} and PCE. However, when C_P is too large, the PCE turns to drop due to two facts: (a) the delivered power to the load is not further increased even if C_P is further increased; (b) much larger phase generator power is consumed to drive such a larger C_P. In the applications with a certain input voltage, a trade-off between the capacitor area and optimum PCE can thus be made accordingly.

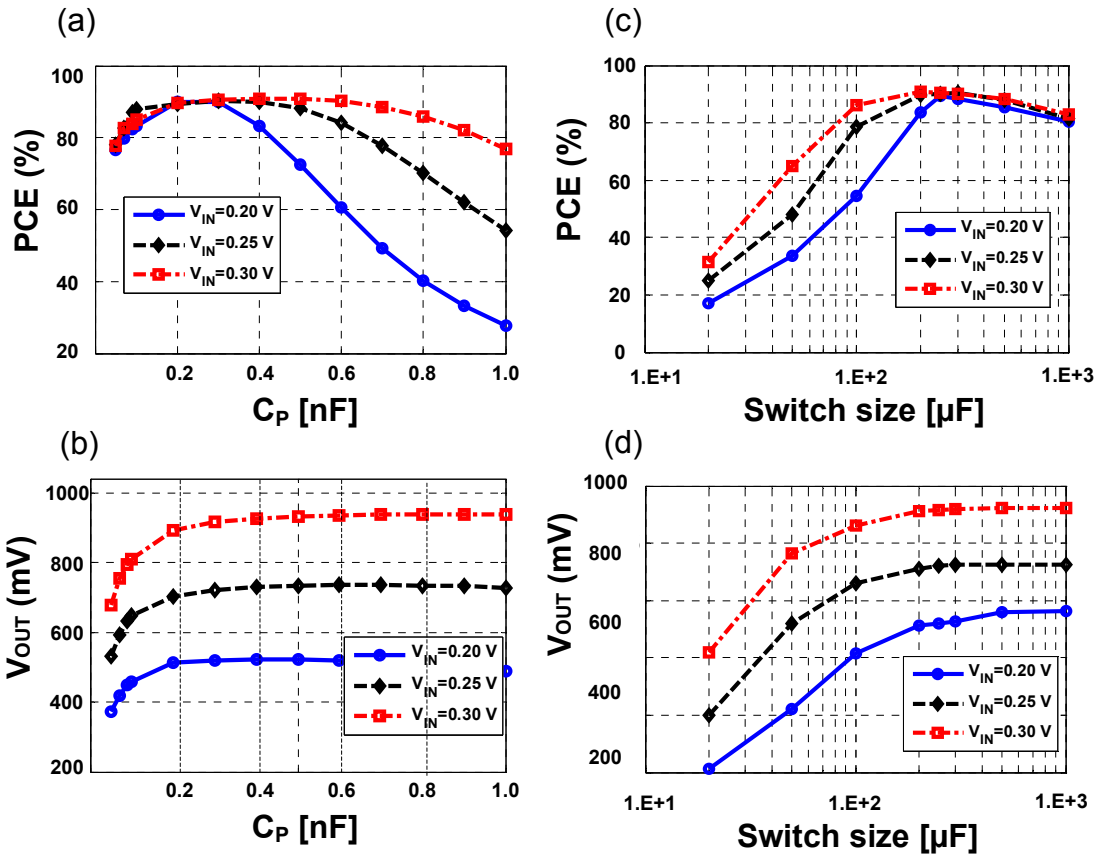


Figure 4-5. CP optimization of the proposed HTFET charge pump with 250 µm switch width: (a) PCE; (b) VOUT; Switch width optimization for the proposed HTFET charge pump with 300 pF CP: (d) PCE; (e) VOUT.

As for the switch size optimization, because a larger switch size has lower on-resistance, the V_{OUT} increases with the switch size. Similarly, to reduce the dominating conduction energy loss E_{COND} and obtain a high PCE, the transistor width needs to be large enough to make its on-resistance negligible. However, the PCE can be degraded by an excessively large transistor width which consumes more switching energy E_{SW}. When the input voltage V_{IN} is larger, this becomes more significant because E_{SW} is generally proportional to the square of V_{IN}.

After optimizations, the highest achieved PCE is larger than 90% for V_{IN} ranging from 0.20 V to 0.30 V. The maximum DC output voltage V_{OUT} is 0.37 V and 0.57 V, for a V_{IN} of 0.20 V and 0.30 V, respectively

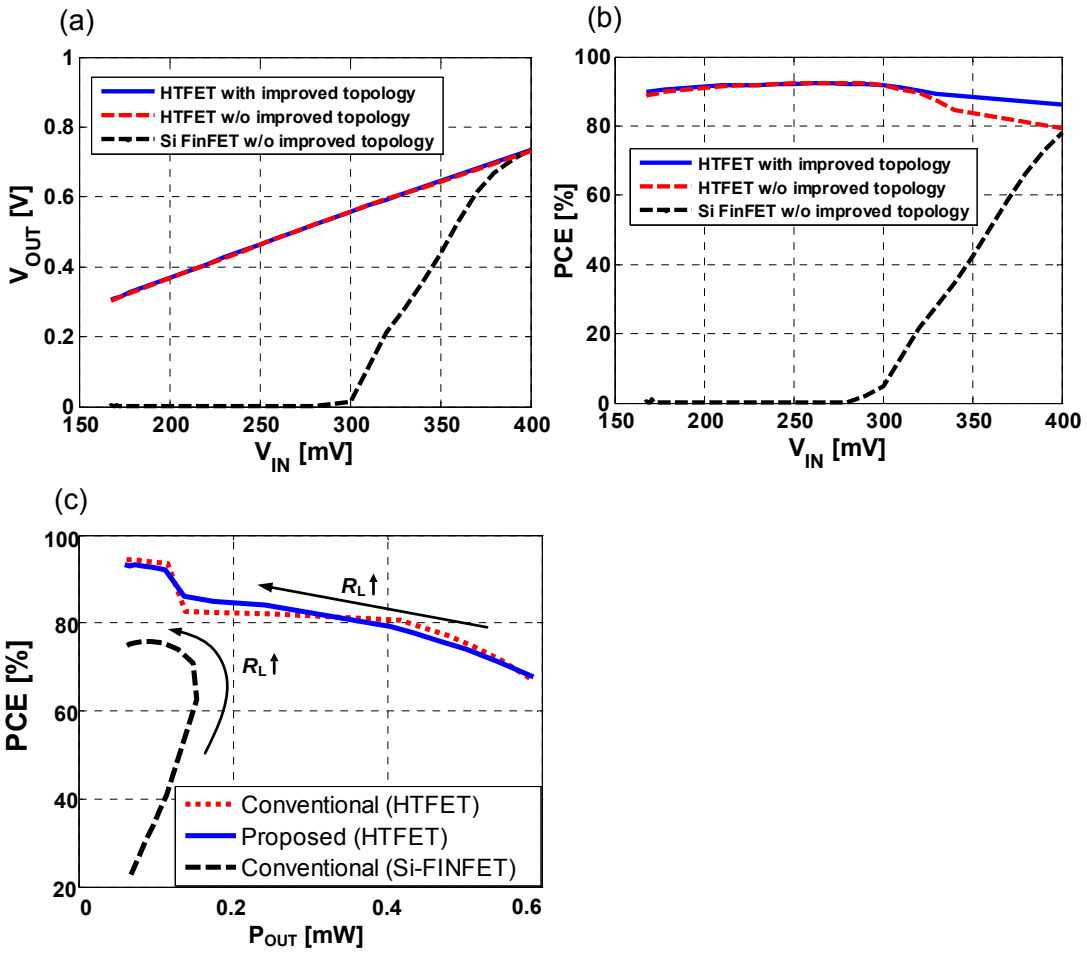


Figure 4-6. Performance comparisons: (a) PCE versus VIN; (b) PCE versus RLOAD.

4.3 Performance Benchmarking

Figure 4-6 shows the comparisons of simulated performance between the conventional Si FinFET charge pump and the proposed HTFET charge pump. In the simulations, the resistive load R_{LOAD}, the pump capacitor C_P, and the clock frequency f_{CLK} are set to be 1.0 kΩ, 300 pF and 30 MHz, respectively.

Figure 4-6 (a-b) shows the simulated V_{OUT} and PCE versus the input voltage V_{IN}. For V_{IN}<0.34 V, the conventional Si FinFET charge pump with switch size of 100 μm has a PCE less than 35% and V_{OUT} is lower than the input due to too large on-resistance of the switches. In this case, this charge pump is useless. In contract, the proposed HTFET charge pump with the same switch size has a PCE higher than 90% when V_{IN} is as low as 0.20 V. When V_{IN} is 0.20 V and 0.30 V, the V_{OUT} of the proposed HTFET charge pump is 0.37 V and 0.57 V, respectively.

Figure 4-6 (c) shows the simulated PCE versus the output power P_{OUT}. The change of the output power P_{OUT} is tuned by changing the output resistive load R_{LOAD}. When R_{LOAD} increases, the PCE gradually increases to its peak, and then drops when R_{LOAD} further increases. The PCE increases at first because a larger R_{LOAD} gathers more percentage of power with a size-fixed switch (see Figure 4-4). The PCE decreases after reaching its peak, because the output power turns to decrease with further increasing R_{LOAD}, while the input power is not decreasing. It is noted that with switches of the same size, the HTFET charge pump is able to deliver much more power with higher efficiency.

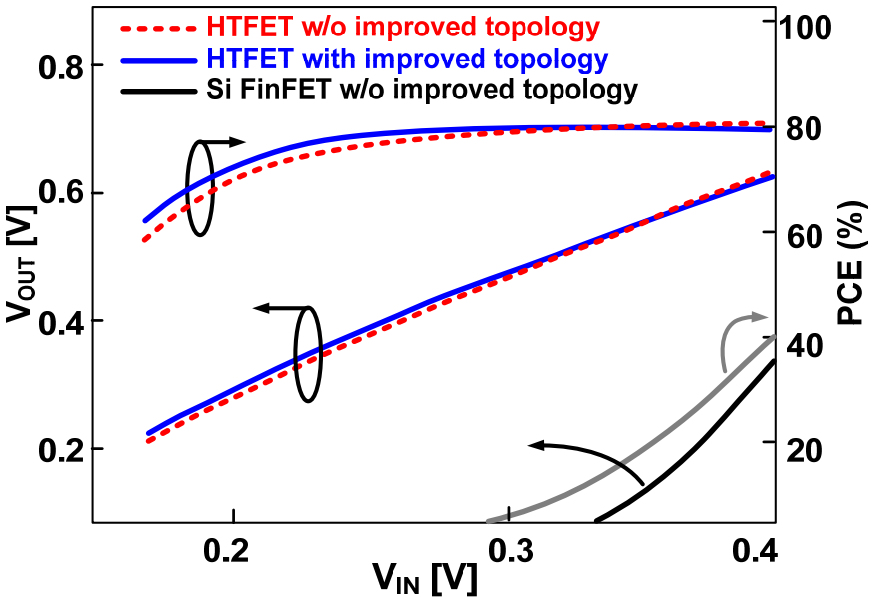


Figure 4-7. V_{OUT} and PCE comparisons with C_P=100pF and the switch size reduced to 20 μm.

Figure 4-7 also shows the PCE and V_{OUT} comparisons between the two HTFET charge pumps with and without the proposed cross-coupled topology. When the switch size is sufficiently large, the on-resistance is small and the performance is similar. When the switch size is small, e.g. 20 μm as shown in Figure 4-7, the proposed HTFET topology outperforms the convention topology with higher PCE and V_{OUT}, which is of significance in chip-area-restricted applications. For higher output voltage, the proposed charge-pump can be cascaded to build a high-efficiency 4× DC-DC converter.

Chapter 5 Conclusion

In this thesis, the HTFET device characteristics have been explored for performance enhancement in the proposed step-up switched-capacitance DC-DC voltage charge pump. Performance evaluation and design optimizations have been presented. Both theoretical and simulated results have shown that the proposed HTFET charge pump is superior to existing CMOS charges pumps with higher power efficiency at low input voltages. The improvement is achieved in part by the steep-slope switching, uni-directional tunneling conduction, and a simplified phase driver. The performance improvement is also achieved by the proposed novel cross-coupled charge pump topology to reduce the on-resistance. After design optimizations, the proposed charge pump achieves simulated power efficiency higher than reported CMOS charge pumps. Further fabrication and measurement work is of significance

Appendix

TFET-based DC-DC converter Spectra Simulation File

```
// Generated for: spectre
// Generated on: Dec 17 19:44:09 2013
// Design library name: heo
// Design cell name: dickson28
// Design view name: schematic
simulator lang=spectre
global 0
parameters br=4 \
        c_fly=80p \
        fsw=30M \
        r=3 \
        r_load=1000 \
        trf=10p \
        vin=300m \
        w=150

// Library name: heo
// Cell name: dickson28
// View name: schematic
V10 (vinb 0) vsource dc=vin type=dc
V11 (vinc 0) vsource dc=vin type=dc
R4 (vout 0) resistor r=r_load
C24 (net055 net022) capacitor c=c_fly
C25 (net042 net020) capacitor c=c_fly
C23 (vout 0) capacitor c=c_fly
V2 (clk 0) vsource type=pulse val0=0 val1=vin period=1/fsw rise=trf \
    fall=trf width=0.5*1/fsw-trf
I251 (net039 net037 0) NTFET_noisy_Multi W=w/br/br/br Nmb=1 Temp=300 \
    Gamma=1.2 Kox=12 L=6e-09 B=843000 eot=7e-10 Nit=1e+16 \
    Trap_depth=2e-09 attn=5e+09 Fano=2 DG_Ids_corr=2
I250 (net041 net039 0) NTFET_noisy_Multi W=w/br/br Nmb=1 Temp=300 \
    Gamma=1.2 Kox=12 L=6e-09 B=843000 eot=7e-10 Nit=1e+16 \
    Trap_depth=2e-09 attn=5e+09 Fano=2 DG_Ids_corr=2
I249 (net043 net041 0) NTFET_noisy_Multi W=w/br Nmb=1 Temp=300 Gamma=1.2 \
    Kox=12 L=6e-09 B=843000 eot=7e-10 Nit=1e+16 Trap_depth=2e-09 \
    attn=5e+09 Fano=2 DG_Ids_corr=2
I211 (clk vinb net037) NTFET_noisy_Multi W=w/br/br/br/br Nmb=1 Temp=300 \
    Gamma=1.2 Kox=12 L=6e-09 B=843000 eot=7e-10 Nit=1e+16 \
    Trap_depth=2e-09 attn=5e+09 Fano=2 DG_Ids_corr=2
I244 (net038 clk 0) NTFET_noisy_Multi W=w/br/br/br/br Nmb=1 Temp=300 \
    Gamma=1.2 Kox=12 L=6e-09 B=843000 eot=7e-10 Nit=1e+16 \
    Trap_depth=2e-09 attn=5e+09 Fano=2 DG_Ids_corr=2
I241 (net040 net038 0) NTFET_noisy_Multi W=w/br/br/br Nmb=1 Temp=300 \
    Gamma=1.2 Kox=12 L=6e-09 B=843000 eot=7e-10 Nit=1e+16 \
    Trap_depth=2e-09 attn=5e+09 Fano=2 DG_Ids_corr=2
I238 (net070 net040 0) NTFET_noisy_Multi W=w/br/br Nmb=1 Temp=300 \
    Gamma=1.2 Kox=12 L=6e-09 B=843000 eot=7e-10 Nit=1e+16 \
    Trap_depth=2e-09 attn=5e+09 Fano=2 DG_Ids_corr=2
I235 (net044 net070 0) NTFET_noisy_Multi W=w/br Nmb=1 Temp=300 Gamma=1.2 \
    Kox=12 L=6e-09 B=843000 eot=7e-10 Nit=1e+16 Trap_depth=2e-09 \
    attn=5e+09 Fano=2 DG_Ids_corr=2
I232 (net020 net044 0) NTFET_noisy_Multi W=w Nmb=1 Temp=300 Gamma=1.2 \
    Kox=12 L=6e-09 B=843000 eot=7e-10 Nit=1e+16 Trap_depth=2e-09 \
    attn=5e+09 Fano=2 DG_Ids_corr=2
I214 (net022 net043 0) NTFET_noisy_Multi W=w Nmb=1 Temp=300 Gamma=1.2 \
    Kox=12 L=6e-09 B=843000 eot=7e-10 Nit=1e+16 Trap_depth=2e-09 \
    attn=5e+09 Fano=2 DG_Ids_corr=2
I167 (vinc net042 net055) NTFET_noisy_Multi W=w Nmb=1 Temp=300 Gamma=1.2 \
    Kox=12 L=6e-09 B=843000 eot=7e-10 Nit=1e+16 Trap_depth=2e-09 \
    attn=5e+09 Fano=2 DG_Ids_corr=2
I168 (vinc net055 net042) NTFET_noisy_Multi W=w Nmb=1 Temp=300 Gamma=1.2 \
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        attn=5e+09 Fano=2 DG_Ids_corr=2
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        Gamma=1.2 Kox=12 L=6e-09 B=843000 eot=7e-10 Nit=1e+16 \
        Trap_depth=2e-09 attn=1.25e+10 Fano=2
I253 (net041 net039 vinb) PTFET_noisy_Multi W=w*r/br/br Nmb=1 Temp=300 \
        Gamma=1.2 Kox=12 L=6e-09 B=843000 eot=7e-10 Nit=1e+16 \
        Trap_depth=2e-09 attn=1.25e+10 Fano=2
I252 (net043 net041 vinb) PTFET_noisy_Multi W=w*r/br Nmb=1 Temp=300 \
        Gamma=1.2 Kox=12 L=6e-09 B=843000 eot=7e-10 Nit=1e+16 \
        Trap_depth=2e-09 attn=1.25e+10 Fano=2
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        Gamma=1.2 Kox=12 L=6e-09 B=843000 eot=7e-10 Nit=1e+16 \
        Trap_depth=2e-09 attn=1.25e+10 Fano=2
I243 (net038 clk vinb) PTFET_noisy_Multi W=w*r/br/br/br/br Nmb=1 Temp=300 \
        Gamma=1.2 Kox=12 L=6e-09 B=843000 eot=7e-10 Nit=1e+16 \
        Trap_depth=2e-09 attn=1.25e+10 Fano=2
I242 (net040 net038 vinb) PTFET_noisy_Multi W=w*r/br/br/br Nmb=1 Temp=300 \
        Gamma=1.2 Kox=12 L=6e-09 B=843000 eot=7e-10 Nit=1e+16 \
        Trap_depth=2e-09 attn=1.25e+10 Fano=2
I239 (net070 net040 vinb) PTFET_noisy_Multi W=w*r/br/br Nmb=1 Temp=300 \
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        Gamma=1.2 Kox=12 L=6e-09 B=843000 eot=7e-10 Nit=1e+16 \
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        attn=1.25e+10 Fano=2
I218 (net022 net043 vinc) PTFET_noisy_Multi W=w*r Nmb=1 Temp=300 Gamma=1.2 \
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        Kox=12 L=6e-09 B=843000 eot=7e-10 Nit=1e+16 Trap_depth=2e-09 \
        attn=1.25e+10 Fano=2
I201 (vout net020 net055) PTFET_noisy_Multi W=w*r Nmb=1 Temp=300 Gamma=1.2 \
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        attn=1.25e+10 Fano=2
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finalTimeOP info what=oppoint where=rawfile
modelParameter info what=models where=rawfile
element info what=inst where=rawfile
outputParameter info what=output where=rawfile
designParamVals info what=parameters where=rawfile
primitives info what=primitives where=rawfile
subckts info what=subckts  where=rawfile
saveOptions options save=all pwr=all currents=all
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bridging atomistic simulations and experimental results," in *IEEE VLSI Technology Symposium*, June 2012.

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