HETEROGENEOUS INTEGRATION OF III-V AND II-IV SEMICONDUCTOR SHEETS ONTO SILICON SUBSTRATES THROUGH ELECTRIC-FIELD ASSISTED ASSEMBLY FOR DEVICE APPLICATIONS

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by
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ABSTRACT

Market forces are creating a strong need to make value-added enhancements to silicon (Si) complementary metal-oxide semiconductor (CMOS) integrated circuit (IC) technology. One approach to achieve this goal is through continued scaling following Moore’s law. With the future of device scaling being relatively uncertain in the next 10-20 years, it is important to find new ways to add value to CMOS. Theoretical projections show that monolithic three-dimensional (3D) integration of compound semiconductor (CS) devices can enhance the performance and functionality of future CMOS-based IC’s. This becomes increasingly important with continued scaling. With each new technology node the interconnect pitch is reduced, increasing the RC delay. The net result is an increase in response time between circuit components, resulting in a greater need for 3D integration to minimize the length of the contact lines between CMOS and other non-digital functionalities. To achieve this complex goal, a flexible heterogeneous integration strategy is required that can incorporate a diverse selection of materials all onto a single substrate.

Electric-field assisted assembly is a promising technique that allows for fast, low temperature and versatile integration of a large variety of materials onto alternative substrates. In this technique, particles can be assembled from solution at high yields, achieving sub-micron alignment registration to predefined features on the substrate. The approach is not limited by mismatch in coefficient of thermal expansion (CTE) and lattice constant, offering the flexibility to apply materials at the device layer, or any subsequent layer in the CMOS backend.

In this dissertation research, electric-field assisted assembly of micron-sized compound semiconductor (CS) sheets is studied through a combination of experiment and finite element method (FEM) modeling. This work presents a clear picture of charge distribution within an assembled particle on the substrate, and uses the model to accurately predict the preferred assembly
position. The assembly position is confirmed experimentally, demonstrating reproducible sub-micron alignment accuracy with respect to patterned features on a substrate.

Through a combination of electric-field assisted assembly and top down fabrication, a novel heterogeneous integration strategy is demonstrated. As a proof of concept, this technique is used to create In$_{0.53}$Ga$_{0.47}$As fin geometry p$^+$-i-n$^+$ junctions directly on Si substrates. The as-etched fin devices are not rectifying, but with annealing at 350°C in N$_2$ for 20 minutes, the electrical properties are restored. This process is further developed to implement fin tunnel field-effect transistors (TFETs) and metal-oxide semiconductor field-effect transistors (MOSFETs) integrated on Si. While dry etch-induced damage degrades the TFET device performance, fin MOSFETs show considerably better device performance due to their majority carrier device operation. Fin MOSFETs have a subthreshold slope of 280mV/decade and an on/off ratio of $\sim 10^3$ at 100mV. Through technology aided computer design (TCAD) simulations, it is shown that MOSFET performance can be improved by implementing an optimized doping design.

To further emphasize the versatility of this heterogeneous integration strategy, solution-synthesized germanium selenide (GeSe) particles are assembled onto Si substrates. GeSe offers promise for phase change memory applications and non-toxic solar cells, due to its bandgap in the visible spectrum and use of earth-abundant non-toxic elements. GeSe nanobelts are measured both with 2-pt and 4-pt single particle measurements, and a resistivity of 360 Ω-cm is determined. This integration strategy is a reproducible technique for single particle measurements of solution-synthesized materials, something significantly lacking in the field. With such a technique, solution-synthesized particles can be evaluated for their use in future device applications.
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Chapter 1 Introduction

1.1 Motivation

As complementary metal-oxide-semiconductor (CMOS) chips continue to advance to provide high value-added enhancements, there are two approaches to take, as shown in Figure 1-1. The traditional “More of Moore” approach aims to continue scaling of transistors for digital logic applications following Moore’s law, which has resulted in a doubling of the number of transistors per chip approximately every two years.\(^1\) However, with the future of device scaling being relatively uncertain, there is a need for an alternative approach. The goal of the second “More than Moore” approach is to add new functionalities (analog/radio frequency, optical devices, and sensors) directly onto the CMOS chip.\(^2\)

To realize these complex integrated systems, it is necessary to find scalable strategies to heterogeneously integrate non-silicon (Si) materials directly onto CMOS with the versatility to add these materials both at the device layer and in the interconnect layers. This is illustrated schematically in Figure 1-2. With this integration, interconnect lines between CMOS and the newly added devices can be reduced, minimizing the interconnect delay between devices and improving circuit performance.\(^3\) The need to minimize interconnect length increases with scaling of CMOS. As CMOS is scaled, the pitch between metal lines is reduced, and the RC delay between interconnects increases.\(^4\) This delays the communication time between circuit components. As such, there is a growing interest in 3D device integration to minimize the response time between CMOS and these non-digital functions to create high performance scalable systems.\(^5\)

Compound semiconductors (CS) are of interest because of their tunable direct band gaps and high mobility, making them desirable for both optical devices and high speed transistors.\(^6\) However,
due to mismatches in lattice constants and coefficient of thermal expansion,\textsuperscript{7,8} direct implementation of these materials onto silicon is not a straightforward process. Section 1.2 will discuss several approaches that have been explored to achieve this level of integration on CMOS integrated circuits (IC’s).

![Figure 1-1](image)

Figure 1-1. “More of Moore” (traditional scaling of CMOS) vs. “More than Moore” (diversification of devices integrated directly on CMOS) image from “Moore than Moore” white paper 2010.\textsuperscript{2}

![Figure 1-2](image)

Figure 1-2. Schematic showing how CS integration on Si can add new functionality to CMOS IC’s.
The research in this dissertation focuses on demonstrating an electric-field assisted directed assembly technique to position micron-sized sheets of CS’s on arbitrary substrates. This overcomes the thermal budget and lattice mismatch constraints of other integration strategies that are being explored. Through a bottom-up/top-down hybrid strategy, indium gallium arsenide (In$_{0.53}$Ga$_{0.47}$As) fin tri-gate tunnel-field effect transistors (TFETs) and metal-oxide-semiconductor field effect transistors (MOSFETs) were fabricated on Si substrates as proof of concept devices. Additionally, this assembly approach also offers a standard platform to evaluate the viability of new solution-synthesized particles for device applications. In addition, solution-synthesized germanium selenide (GeSe) particles were integrated onto Si and evaluated for potential device applications. Integrating two different materials systems onto a common substrate through directed assembly demonstrates the versatility of this technique.

In this chapter, an overview of several of the well-studied CS-on-Si heterogeneous integration strategies will be provided. FinFETs will be introduced and motivated as a proof-of-concept device. Solution-synthesized semiconductors will be discussed for their potential use in device applications through directed electric-field assisted assembly. Lastly, the layout of the dissertation will be outlined.

1.2 Heterogeneous Integration Strategies

Heterogeneous integration of CS’s on Si has been achieved through a variety of techniques, including direct growth, wafer bonding, wafer packaging and transfer printing, each having benefits and limitations.
1.2.1 Direct growth

Epitaxial growth of thin films benefits from a lattice matched crystalline substrate for high quality films. Heterogeneous integration of CS’s on Si is highly desired for a number of applications.\textsuperscript{10,11} Most CS’s have large lattice mismatch (>8\% in In\textsubscript{0.53}Ga\textsubscript{0.47}As) with Si making it challenging to directly grow high-quality epitaxial films on Si (Fig. 1-4).\textsuperscript{12} The lattice mismatch between the film and growth substrate will induce strain within the film. Above the critical thickness of the material, defects will form to alleviate this strain.\textsuperscript{12} Additionally, Si has a large coefficient of thermal expansion (CTE) mismatch with many CS’s, which introduces strain within the film when cooling from the growth temperature.\textsuperscript{13} This can lead to cracking and delamination of films. With the formation of these defects, there is increased diffusion along the line of dislocation threads, leading to Si auto-doping from the substrate into the grown film.\textsuperscript{12} Low defect density films can be achieved through the use of metamorphic buffers\textsuperscript{14-15} and selective-area growth.\textsuperscript{16} However, these growth techniques require high growth temperatures and crystalline growth substrates, preventing their implementation in back-end processing, as is necessary for truly versatile integration.
Metamorphic Buffers

By depositing linearly composition graded thin films that gradually transition the lattice constant and CTE mismatch, CS films with low defect densities can be deposited on Si. These layers are known as metamorphic buffer layers.\textsuperscript{14,15} By using GaAs and In\textsubscript{x}Al\textsubscript{1-x}As buffer layers, In\textsubscript{0.7}Ga\textsubscript{0.3}As quantum well FETs have been demonstrated on Si.\textsuperscript{15}

Alternatively, using an approach known as Si-on-lattice-engineered-Si (SOLES), both CMOS and CS devices can be fabricated on a common substrate (Figure 1-4). In this approach, a Ge template layer is first deposited on a Si substrate. Ge has a very small lattice mismatch with GaAs and a similar CTE (Figure 1-3), making it an ideal template for CS growth. Additional metamorphic buffers can then be instituted to transition from the Ge template to the desired CS material. Next, an oxidized Si wafer is bonded on top of this Ge layer, and a Si device layer is formed with smart cut and chemical mechanical polishing. This results in a Si device layer on top...
of a Ge template layer.\textsuperscript{17} CMOS can be fabricated on the top Si, while windows can be opened to the buried Ge for low-defect density CS deposition.

![Schematic of heterogeneous integration of CS’s on CMOS using SOLES with metamorphic buffers. Copyright 2014 The Royal Society Publishing.](image)

Metamorphic buffers enable heterogeneous integration of CS’s and Si, but not without limitations. Thick metamorphic buffer layers (> 1μm)\textsuperscript{18} are required to achieve high quality films, with each film needing a tailored metamorphic buffer. This makes the process very specific and difficult to implement over a wide variety of materials systems. Due to the complexity of the buffers and high growth temperatures, it is difficult to implement this approach in back end of line as would be desired for optimal flexibility in 3D circuits.

\textit{Selective-Area Growth}

When depositing large area films, lattice and CTE mismatch become significant problems for high quality film growth as discussed before. Scaling the dimensions of the growth area reduces the strain energy within the crystal, extending the critical thickness of the film and minimizing defect generation.\textsuperscript{16} This approach allows for CS films to be directly deposited onto Si without the use of metamorphic buffers. However, in this process there are high densities of stacking faults that form during the growth process.\textsuperscript{19} Stacking faults act as electrically active charge centers that can
degrade device performance.\textsuperscript{20} Furthermore, selective area growth achieves the highest film quality on (111) Si,\textsuperscript{21} which is less desirable than (100) Si for use in CMOS, as it has a higher density of surface states.\textsuperscript{22}

Expanding upon this approach, Si fins are patterned and etched on a (100) Si substrate. The substrate is then coated with a SiO\textsubscript{2} layer and planarized with chemical mechanical polishing (CMP). The Si fin is then selectively etched in tetramethylammonium hydroxide (TMAH), removing the Si fin and exposing a v-shaped groove with (111) facets exposed.\textsuperscript{23} Using this template, InP is grown with metal organic vapor phase epitaxy (MOVPE) as a buffer layer followed by lattice-matched InGaAs growth.\textsuperscript{24} This technique has been expanded to form InGaAs finFETs and gate all around (GAA) nanowire FETs on Si.\textsuperscript{25} However, during growth of the III-V layers, Mg/Zn has been shown to diffuse into the isolation oxide, degrading device reliability.\textsuperscript{26} Additionally, this process requires 800\textdegree C pretreat temperatures and 550\textdegree C growth temperatures,\textsuperscript{23} greatly limiting the application base due to the high thermal budget.

1.2.2 Wafer bonding

Wafer bonding overcomes the limitations of lattice and CTE mismatch by growing the desired film on a matching, ideal substrate. Once a high quality film has been grown, it is bonded to a Si substrate by applying pressure at elevated temperatures. This approach can be used to deposit unprocessed large area films,\textsuperscript{27} shown in Figure 1-5a, as well as fully processed devices integrated using through Si vias (TSV),\textsuperscript{28} shown in Figure 1-5b. Both of these processes require high temperature and pressures, making them unsuitable for back end integration.
Large Area Film Bonding

In this approach, a high quality film is grown onto a lattice matched substrate and then the film is bonded to Si, either directly or through the use of the intermediate layer. The growth substrate is removed either by selective etching of a sacrificial layer, smart cut or chemical-mechanical polishing. Bond formation between layers does not rely on a one-to-one atomic mapping, allowing for lower defect densities than direct growth without buffer layers. There still can be a large CTE mismatch between the CS film and the Si substrate, greatly limiting the bonding temperatures. Additionally, outgassing during the bonding process can introduce voids within the bonded film. Integration of this process with state-of-the-art CMOS is complicated by the fact that most growth substrates for CS are 150mm or less, generations behind the 300mm used in
CMOS. This makes it challenging to integrate CS films over entire 300mm wafers using wafer bonding technology.

**Through Silicon Vias**

In a variation of wafer bonding, CS devices are fabricated on a lattice matched substrate, and completed all the way to the metallization step. Then a passivation layer such as SiO$_2$ is deposited and the device is bonded to a Si device wafer on SOI containing a similar passivation layer through a low temperature bond. Use of an intermediate layer lowers the bonding temperature to minimize the thermal budget. By completing a deep SiO$_2$ etch to reach the CS metallization, a via can be filled to connect the two device layers. Using a similar approach, layers can be stacked to form a heterogeneously integrated 3D IC.

While this approach can be used to integrate a variety of materials into a single chip, it does have similar problems to the other approaches. When integrating dissimilar materials, issues of stress between layers resulting from CTE mismatch can limit the processing and operating temperatures of the chip. Additionally, etching through substrate vias through CS substrates can be challenging. Therefore, this technique has not been widely used for heterogeneous integration of CS’s on Si; it is primarily used for 3D silicon chip formation.

### 1.2.3 Wafer Level Packaging

The most common approach to incorporate multiple functionalities on a single chip relies on integrating fully fabricated devices through die stacking. Chips are connected together by stacking and wire bonding (Figure 1-6) or through solder bump bonding. This allows chips to be processed on dissimilar substrates and then integrated together, overcoming limits of lattice
constant and CTE mismatch between materials. However, while this approach is straightforward and versatile, the leads between chips are very large. This causes large resistive losses, due to the large distances interconnects must cover, resulting in slower communication between chips. Furthermore, this integration strategy has a larger profile, limiting the ability to miniaturize chips.

Figure 1-6. (a) Schematic of multiple die stacking through wire bonding (b) SEM image of multiple dies stacked through wafer bonding. Copyright 2004 IEEE.

1.2.4 Novel Approaches

Transfer Printing

Using a technique known as transfer printing, CS’s can be transferred to virtually any substrate. In this technique, the desired film is grown on a lattice matched substrate, as shown schematically in Figure 1-7. In the growth process a sacrificial layer is included that can be selectively etched without attacking the target film. The film is then patterned into chiplets of a desired size. Next, the selective release layer is etched to form freestanding chiplets held to the substrate by posts. The chiplets are picked up with a polydimethylsiloxane (PDMS) stamp, using a fast peel rate, and stamped onto the desired substrate using a slow peel rate. This technique is extremely versatile, overcoming many of the challenges with heterogeneous integration discussed in previous sections, allowing integration of functional devices onto alternative substrates. However, this technique has limitations in precision of alignment of the particles with respect to
predefined features on the target substrate, with maximum registration accuracy in the micrometer range.\textsuperscript{42,43}

\begin{figure}[h]
\centering
\includegraphics[width=\textwidth]{figure1.png}
\caption{Schematic of transfer printing using a PDMS stamp.\textsuperscript{11} Copyright 2010 Nature Publishing}
\end{figure}

\textit{Electric-field Assisted Directed Assembly}

Electric-field assisted directed assembly begins with a solution of suspended particles.\textsuperscript{44-56} The particles are controllably placed onto a desired substrate by applying non-uniform electric fields. When a polarizable particle is placed in a non-uniform electric field (Figure 1-8a), it forms a dipole. When the electric field is non-uniform on the length scale of the dipole, the electric field at each end of the dipole will not be equal, resulting in a net force and torque on the particle.\textsuperscript{57,58} This is known as dielectrophoresis (DEP). Depending on the complex permittivity of the particle and solution, the particle will either experience negative DEP (particle moves away from regions of high electric field gradient) or positive DEP (particle moves toward regions of high electric field gradient).\textsuperscript{59} For heavily doped semiconductor particles in low conductivity solutions, the particles are more polarizable than the dielectric medium;\textsuperscript{44-48} therefore, positive DEP will be experienced, directing particles to regions of high electric field gradient.
By properly designing guiding electrode structures to have controlled regions of high electric field gradient, particles can be attracted to specific regions on a substrate. Once the particles are near the surface, electrostatic interactions between particles and the substrate align the particles to the electrode (bottom panel Figure 1-8a). The electrostatic interactions between particles will lead to the formation of uniformly spaced arrays (Figure 1-8b). The physics of this technique will be discussed in more detail in chapter 2. This technique is versatile and can be used for a wide range of materials, including metals, semiconductors, oxides, carbon nanotubes, and graphene. The process only requires patterning of guiding electrode structures, which can easily be integrated into the device layer or any step of back-end processing. In this dissertation research, electric-field assisted directed assembly of micron-sized CS sheets will be demonstrated with sub-micron registration accuracy, which surpasses the best available particle placement techniques.

Figure 1-8. (a) Schematic of nanowires being directed to a guiding electrode due to DEP. Once the nanowires reach the dielectric layer they rearrange to form uniform spacing due to electrostatic forces (b) Optical microscope images of assembled arrays of metal and semiconductor nanowires with uniform spacing. Copyright 2012 Annual Reviews Publications.
1.3 Fin Tunnel FET and MOSFET

Two electronic devices – In$_{0.53}$Ga$_{0.47}$As fin TFETs and MOSFETs – were chosen for a proof-of-concept demonstration of the electric-field assisted directed assembly heterogeneous integration strategy. The fin geometry is of particular interest because it allows for the implementation of a tri-gate device geometry. As Moore’s law is followed, channel length is continually scaled to smaller dimensions. When channel length is on the same order as the depletion regions of source and drain junctions, the channel becomes depleted by the source and drain junctions, resulting in loss of electrostatic control by the gate. A gate that wraps around the channel region, as in a finFET, provides better electrostatic control of the channel, leading to steeper sub-threshold slopes (Figure 1-9). For this reason, the devices used in this work will apply the fin geometry.

![Simulated plots of subthreshold slope vs. gate length for Si finFET’s and planar FET’s on SOI substrates.](image)

Figure 1-9. Simulated plots of subthreshold slope vs. gate length for Si finFET’s and planar FET’s on SOI substrates. Copyright 2006 IEEE.

While the MOSFETs and TFETs are primarily used in logic device applications, which will be in the device layer of CMOS, this platform can be extended to integrate new materials and devices onto Si. It is a reasonable expansion of this proof-of-concept to implement this integration
in the back end of line as well as at the device layer, making it an extremely versatile strategy. To emphasize the flexibility of this integration strategy, solution-synthesized particles were assembled using directed electric-field assisted assembly.

1.4 Solution-Synthesized Particles

Recently, semiconductor particles have been produced through colloidal synthesis processes, with a wide variety of materials\textsuperscript{64-67} and geometries being created.\textsuperscript{65,68} However, there has been very limited work achieving single particle electrical measurements. To evaluate these materials for future device applications, variation between particles must be evaluated; a goal that can be only achieved with single particle measurements. Electric-field assisted directed assembly provides an approach to rapidly integrate and evaluate the electrical properties of a wide variety of solution-synthesized materials. In this dissertation research, GeSe nanobelts growth through a one-pot colloidal synthesis are grown. GeSe has potential for use in phase change memory applications\textsuperscript{69-70} and solar cell applications due to its narrow band gap\textsuperscript{71} and non-toxic composition. These particles are assembled, electrically contacted, and characterized by 2-point and 4-point measurements. By comparison of the 2-point and 4-point measurements, a contact resistance for the 2-pt measurement can be approximated. This is an important characterization for evaluating the viability of this material for further applications.

1.5 Outline of Dissertation

Chapter 2 investigates electric-field assisted directed assembly of micron-sized semiconductor sheets that are fabricated from epitaxial grown device structures. Through use of finite element method (FEM) modeling, a clear picture of the charge distribution within an
assembled sheet is presented. Through a combination of modeling and experiment, precise sheet registration on a silicon substrate is demonstrated and explained. Lastly, through FEM studies, a self-limiting assembly mechanism is explained.

Chapter 3 summarizes the process used to assemble In$_{0.53}$Ga$_{0.47}$As sheets onto Si substrates, and to fabricate these sheets into devices. Through a hybrid top-down, bottom-up integration strategy, In$_{0.53}$Ga$_{0.47}$As p$^+\text{-}i\text{-}n^+$ and n$^+\text{-}i\text{-}n^+$ fins are fabricated on a Si substrate. p$^+\text{-}i\text{-}n^+$ fin junctions are demonstrated and characterized as a function of post-etch treatment conditions. Lastly, a gate stack is integrated on both fin types to form In$_{0.53}$Ga$_{0.47}$As finFETs and fin TFETs. Both devices show degraded device performance due to dry etch induced damage. However, the fin MOSFET, being a majority carrier device, shows significantly better device performance than the fin TFET. Technology computer aided design (TCAD) modelling is used simulate an equivalent device, demonstrating through proper channel doping design, the device performance can be improved.

Chapter 4 examines the effect of post-etch treatments to reduce the dry etch damage in In$_{0.53}$Ga$_{0.47}$As p$^+\text{-}i\text{-}n^+$ junction devices in an effort to minimize the effects of dry etch damage. The p$^+\text{-}i\text{-}n^+$ junction is a building block for the TFET and is a very good indicator of defects within a crystal. By using an optimized annealing procedure, the parasitic trap-assisted tunneling (TAT) current is mitigated, and the on-set of band-to-band tunneling (BTBT) is demonstrated. This indicates that a low trap state density in the forbidden band has been achieved, and will serve as a good building block for TFETs.

Chapter 5 investigates the directed assembly and integration of solution-synthesized GeSe nanobelts. After assembly, 2-point and 4-point metal contacts are integrated onto the nanobelts and electrical measurements are used to characterize the nanobelts. From these measurements, a contact resistance is approximated for the 2-point measurement. This strategy offers a standard platform for single-particle electrical characterization of solution-synthesized particles.
Lastly, chapter 6 will provide a summary of the dissertation, outlining the accomplishments of the work, and will suggest future experiments and research directions.

1.6 Bibliography


Y. Thean "An InGaAs/InP quantum well finfet using the replacement fin process integrated in an RMG flow on 300mm Si substrates," *Symposium on VLSI Technology Digest of Technical Papers*, 1-2 (2014).


Chapter 2 Electric-Field Assisted Directed Assembly of Semiconductors Sheets

2.1 Introduction

Electric-field assisted assembly offers a versatile means to heterogeneously integrate new materials and devices onto silicon (Si) substrates.\textsuperscript{1-6} In this assembly technique, long-range dielectrophoretic (DEP) forces attract particles from solution to the substrate,\textsuperscript{7-11} where they are aligned to the substrate by electric field interactions.\textsuperscript{12} The DEP response of particles in solution has been modeled.\textsuperscript{8,11,13-14} However, little work has been done to examine the short-range electric-field forces that act on a particle near the surface of the electrode.\textsuperscript{12} These forces are critical in determining the final placement of the particle on the substrate.

This chapter will combine experiment and theory to understand the process for assembling micron-sized compound semiconductor (CS) sheets with high registration accuracy to predefined features on a target Si substrate. It will consider the long-range DEP forces that attract particles from suspension to regions onto a target substrate, as well as the short-range field forces between the particles and the underlying electrode.

Section 2.2 will provide a brief overview of DEP-induced assembly of semiconductor sheets. Finite element method (FEM) modeling will be used to estimate the frequency dependence of DEP. In Section 2.3, the short-range forces on the sheet will be examined both experimentally and through FEM computation. A comprehensive model will be demonstrated, allowing for calculation of the charge distribution within an assembled sheet on the substrate. In Section 2.4, directed assembly into lithographically defined features will be introduced, and the field forces within and around these features will be examined with a FEM model. Through this model, the
electrically preferred sheet positioning will be determined, and compared to the experimentally observed assembly position. The model will be expanded to examine the interaction between a sheet assembled within a lithographically defined feature and a sheet outside of this feature. The research will be summarized in Section 2.5.

2.2 Dielectrophoretic Force

In electric-field assisted directed assembly, individual solution-suspended particles are attracted from the suspension toward a target substrate containing electrically biased guiding electrodes. By properly designing the guiding electrode geometry and optimizing the applied bias, particles will be assembled within lithographically defined features on the substrate as illustrated in Figure 2-1a. The long-range attractive force that drives the assembly process is DEP.

Figure 2-1. (a) Schematic of a wide-gap electrode structure containing two guiding electrodes of opposite bias. Sheets in solution are directed from solution toward the electrode edges and form a uniformly spaced array. (b) Schematic of polarizable particle in a non-uniform electric field, showing the formation of a dipole.
When a polarizable particle is placed in a non-uniform electric field, it will form a dipole as illustrated in Figure 2-1b. This can be described as an ideal dipole with positive charge \( q \) and negative charge \(-q\) separated by a distance \( \tilde{d} \). The net force and torque on the particle is given by:

\[
\vec{F}(\vec{r}) = q\vec{E}(\vec{r} + \tilde{d}) - q\vec{E}(\vec{r})
\]

(2-1)

\[
\vec{T}(\vec{r}) = \frac{\tilde{d}}{2} \times q\vec{E}(\vec{r} + \tilde{d}) - \frac{\tilde{d}}{2} \times \vec{E}(\vec{r})
\]

(2-2)

where \( \vec{r} \) is the spatial coordinate of the negative charge, and \( \vec{E} \) is the electric field. From equation 2-1, if the electric field is non-uniform on the length scale of the nanowire, i.e., \( q\vec{E}(\vec{r} + \tilde{d}) \neq q\vec{E}(\vec{r}) \), then the net force on the particle is non-zero. This is referred to as the DEP force. From equation 2-2, the net torque is zero when the long axis of the particle is parallel to electric field lines. Therefore, the torque will align particles parallel to the electric field lines.

Equation 2-1 can be simplified when \( \tilde{d} \) is small compared to the characteristic dimension of electric field non-uniformity using a Taylor series expansion:

\[
\vec{E}(\vec{r} + \tilde{d}) = \vec{E}(\vec{r}) + \tilde{d} \cdot \nabla \vec{E}(\vec{r}) + \ldots
\]

(2-3)

Neglecting higher order terms and applying equation 2-3 into equation 2-1 gives:

\[
\vec{F} = q\tilde{d} \cdot \nabla \vec{E} = \tilde{p} \nabla \vec{E}
\]

(2-4)

where \( q\tilde{d} = \tilde{p} \), the dipole moment. This is known as the DEP approximation. For a lossy dielectric ellipsoidal particle with a long axis (i.e., \( a \) and \( b \ll c \)), it can be assumed that the long axis of the particle will align along the electric field lines due to the torque acting on the particle. Applying this assumption, the force on the particle can be simplified to the force acting parallel to the long axis. Thus, the time averaged dipole moment can be approximated as:

\[
\langle \tilde{p}_{\text{eff}} \rangle_{||} = \frac{2\pi abc}{3} \varepsilon_m \text{Re}\left[\frac{\varepsilon_p - \varepsilon_m}{\varepsilon_m}\right] E_0_{||}
\]

(2-5)
where \(a, b\) and \(c\) are the dimensions of the particle, \(\varepsilon_p\) and \(\varepsilon_m\) are the complex permittivity of the particle and medium respectively and \(E_{0,||}\) is the electric field along the long axis. By applying the dipole moment into equation 2-4, the DEP force along the long axis can be determined by:

\[
\langle \vec{F}_{DEP}\rangle_{\text{Sheet}} = \frac{2\pi abc}{3} \varepsilon_m \text{Re}\left[\frac{(\varepsilon_p - \varepsilon_m)}{\varepsilon_m}\right] \nabla E_0^2
\]  

(2-6)

where \(\nabla E_0^2\) is the gradient of the electric field squared. From equation 2-6, it is clear that the magnitude of the DEP force is depends directly on the gradient of electric field squared. By designing guiding electrode structures with controlled regions of high electric field gradient, particles will be attracted from suspension to the substrate. While this equation is simply an approximation, the proportional dependence to \(\nabla E_0^2\) offers a convenient way to evaluate the relative efficacy of electrode structures in generating DEP forces.

For the guiding electrode structure used in this research, the characteristic length of the electric field is similar in size to the long axis of the particle. In this case, the DEP approximation breaks down and the Maxwell stress tensor (MST) method must be used to accurately calculate the electrical force and torque induced on a particle in a non-uniform field. Starting with the reduced quasi-electrostatic form of Maxwell equation, the surface force density at every point on the particle can be determined from:

\[
\vec{f} = \text{Re}(\varepsilon) \left(\vec{E}(\vec{E} \cdot \hat{n}) - \frac{1}{2} (\vec{E} \cdot \vec{E})\hat{n}\right)
\]  

(2-7)

By integrating the expression \(\vec{f}\) over the surface of the particle, the total force exerted on the particle by electric field can be calculated by:

\[
\vec{F} = \int_s \vec{f} \, dS
\]  

(2-8)

In this research, the MST analysis on individual semiconductor sheets suspended in an aqueous medium was conducted using COMSOL Multiphysics FEM computational software, Version 4.2 (Electric Currents Module). The 3D guiding electrode structure that was used in the
FEM model is shown in Figure 2-2. In this structure, 1µm thick Au guiding electrodes were placed on top a 10µm thick SiO₂ substrate. The electrodes were 40µm wide, 60µm long and separated by a 300µm gap; ±10V\text{peak-to-peak} was applied across the electrodes, respectively. Although particles can experience DEP in non-uniform direct current (DC) electric fields, the use of an alternating current (AC) bias minimizes the effect of field screening by a charge double layer in the solution. The electrodes were coated with a 100nm HfO₂ dielectric film, to isolate the electrodes from the solution. A 40µm thick layer of deionized (DI) water was placed on top of the HfO₂. Within the DI water, a single In₀.₅₃Ga₀.₄₇As sheet (10µm long, 620nm wide and 100nm thick) with conductivity 100 S/cm was placed above the positively biased electrode with the sheet long axis centered on the electrode edge. The spacing between the substrate and the sheet was defined by a variable z-spacing as seen in Figure 2-2b. A list of parameters used in the simulation are provided in table 2-1.

Figure 2-2. (a) 3D schematic of the simulation geometry used in this work, through the use of the finite element analysis software COMSOL Multiphysics version 4.2. (b) Cross-sectional magnified view of the region indicated by the red line in (a). An In₀.₅₃Ga₀.₄₇As sheet (620nm wide, 10µm long and 100nm thick) is placed at variable spacing above the positively biased electrode, centered along the electrode edge. All boundaries are set as insulators.
Table 2-1. List of parameters used in simulation.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sheet Dimensions (w,l,t)</td>
<td>0.62µm, 10µm, 100nm</td>
</tr>
<tr>
<td>Sheet Conductivity</td>
<td>100 S/cm</td>
</tr>
<tr>
<td>Sheet Dielectric Constant</td>
<td>11.6</td>
</tr>
<tr>
<td>DI Water Conductivity</td>
<td>$10^{-8}$ S/cm</td>
</tr>
<tr>
<td>DI Water Dielectric Constant</td>
<td>80</td>
</tr>
<tr>
<td>HfO₂ Conductivity</td>
<td>$10^{-12}$ S/cm</td>
</tr>
<tr>
<td>HfO₂ Dielectric Constant</td>
<td>18.6</td>
</tr>
<tr>
<td>HfO₂ Thickness</td>
<td>100nm</td>
</tr>
<tr>
<td>Au Electrode Thickness</td>
<td>1µm</td>
</tr>
<tr>
<td>Au Conductivity</td>
<td>$10^{5}$ S/cm</td>
</tr>
<tr>
<td>Negative Electrode Bias</td>
<td>-10V</td>
</tr>
<tr>
<td>Positive Electrode Bias</td>
<td>10V</td>
</tr>
</tbody>
</table>

Figure 2-3a shows a 2D cross-sectional plot of $\log(\nabla E^2)$ taken at the top surface of the substrate for a solution conductivity of $10^{-5}$ S/cm and an applied frequency of 1MHz. The high gradient regions at the edges of the electrode will facilitate sheet capture at the electrode edges due to DEP. To examine the DEP force on the sheet, the separation between the sheet and the top surface of the substrate was set to 35µm, and the particle was placed above the positively biased electrode. At this large distance from the surface, the calculated force can be viewed as a long-range force on the particle, which is dominated by DEP. In this model, the particle orientation was fixed with its long axis perpendicular to the electrode edge. With this configuration, the long axis of the particle was aligned parallel to the electric field lines to give zero torque on the particle.\(^8,11,15\) The applied bias was fixed at 20V\(_{pp}\) and the frequency was swept from 100Hz to 1MHz as the solution conductivity was varied from $10^{-7}$ S/cm to $10^{-5}$ S/cm.

Figure 2-3b shows a 2D cross-sectional X-Z plot of $\log(\nabla E^2)$ taken through the center of the sheet for a solution conductivity of $10^{-5}$ S/cm and 20V\(_{pp}\), 1MHz applied bias. From this plot it is clear that the characteristic length scale of the region of high electric field gradient is on the same
order of magnitude as the length of the particle. Here, the region of high electric field gradient at the electrode surface with $\log(\nabla E^2)$ greater than 15 has a radius of $\sim 10\mu m$ from the electrode edge, while the sheet length is 10µm. In this case, the higher order terms in equation 2-3 can no longer be ignored, and MST is necessary to accurately calculate the force acting on the particle.\(^{11}\)

Figure 2-3c plots the DEP force acting on the particle calculated using MST analysis. All solution conductivities studied exhibit the general trend of increasing force with increasing frequency. For solutions with conductivity $< 10^{-6}$ S/cm there is minimal frequency dependence in $F_{\text{DEP}}$; when the frequency is swept over four decades the magnitude of $F_{\text{DEP}}$ changes by only a factor of two. However, for more conductive solutions ($10^{-5}$ S/cm), there is a more significant frequency dependence with greater than one order of magnitude change over the same frequency range. Using a higher applied frequency (100kHz-1MHz) minimizes the voltage drop across the solution and maximizes the DEP force.

Figure 2-3. (a) X-Y cross-sectional plot of $\log(\nabla E^2)$ at 1MHz in a $10^{-5}$ S/cm solution, plotted on a constant scale with (b). (b) X-Z cross-sectional plot of $\log(\nabla E^2)$ at 1MHz in a $10^{-5}$ S/cm solution. The electric field gradient can be seen extending into the solution. Regions of high $\nabla E^2$ form at the electrode edges. (c) Plot of DEP force calculated by MST method as a function of frequency for varying solution conductivity. This force is calculated with a z-spacing of 35µm.
2.3 Short-Range Forces

Short-range electric-field forces act on the particle after it is captured by the guiding electrode structure. To study these forces experimentally, an interdigitated electrode structure was fabricated. Starting with a lightly doped n-type Si substrate, a 120nm Si$_3$N$_4$ film was deposited by low pressure chemical vapor deposition (LPCVD). Then 20nm/50nm Ti/Au electrodes were patterned by optical lithography and metal liftoff. These electrodes were 40µm wide and separated by a 300µm gap. On top of the electrodes, a 12nm film of HfO$_2$ was deposited by atomic layer deposition (ALD). A 20Vpp, 1MHz bias was applied to the interdigitated electrode structure capturing particles such that their long axis is perpendicular to the electrode edge (Figure 2-4a). Fixing the magnitude of the voltage and lowering the frequency in decade intervals results in the particles losing alignment along the electrode edge, as shown in Figure 2-4b-f. At 10 kHz, the particles lose their perpendicular alignment to the electrode edge. At 1 kHz and below, the particles drift away from the electrode edge and are no longer captured.

When the particles approach the electrode, charge is induced within the particle by capacitive coupling between the particle and the underlying biased electrode. This can be described by $Q_p = CV$, where $Q_p$ is the charge induced with the particle, $V$ is the applied voltage on the electrode and $C$ is the capacitance of the medium separating the particle and the underlying electrode.\(^{18}\) This charge results in an electrostatic attractive force between the particle and the underlying electrode described by:

$$F_{ES} \approx 2 \frac{Q_p Q_{el}}{4\pi\varepsilon_m r^2}$$  \hspace{1cm} (2-9)

where $Q_p$ is the charge on the particle, $Q_{el}$ is the charge on the electrode, $\varepsilon_m$ is the permittivity of the medium and $r$ is the distance between the two charges. As the frequency is lowered, the capacitive coupling between the particle and the underlying electrode decreases, reducing the charge induced
within the particle. When the induced charge became sufficiently small at low frequency, the particle is no longer held on the surface, and it begins to misalign or drift from the electrode edge.

Figure 2-4. (a)- (f) Dark field optical microscope images of assembled In$_{0.53}$Ga$_{0.47}$As sheets (620nm wide, 10µm long and 100nm thick) in deionized water. A high electric field gradient forms at the electrode edge, capturing particles. As the frequency is lowered, the particles drift away from the electrode edge.

To explain the experimental result shown in Figure 2-4, FEM simulation was applied with a small particle-to-substrate distance to examine the short-range forces acting on the particle. Two cases were examined: one with the z-spacing set to 10nm, and one with the z-spacing set to zero. For both of these cases, the magnitude of the force calculated by MST method is plotted vs. frequency at varying solution conductivity in Figure 2-5 a and b, respectively. When the particle is placed 10nm above the surface of the positive electrode edge, the force on the particle decreases with decreasing frequency, matching the behavior seen experimentally. This trend is magnified with increasing solution conductivity, with the maximum high frequency force saturating at $7.3 \times 10^{-10}$ N. When the particle is placed in direct contact with the substrate, the trend is reversed. With
increasing frequency the force on the particle decreases, which is opposite to what was seen experimentally. At high frequency all three solution conductivities saturate at a minimum force of \(1.9 \times 10^{-9}\) N. This result suggests that when the particle is pulled to the electrode edge by DEP, it does not come into direct contact with the substrate surface, but rather floats slightly above the surface. This agrees with other reports of nanowire capture in aqueous solutions, where a thin layer of solution between an assembled particle and alignment electrodes was verified through in-situ electrical measurements.\(^{18}\)

Figure 2-5. MST calculated force on a particle using the model described in Figure 2-2. (a) Magnitude of the force calculated for a z-spacing of 10nm plotted vs. frequency for varying solution conductivities. (b) Magnitude of the force calculated for a z-spacing of 0nm plotted vs. frequency for varying solution conductivities.

To examine this behavior further, a surface integral of charge density was taken across the bottom surface of the sheet. The resulting charge is plotted in Figure 2-6 for the two cases described above. In Figure 2-6a, the charge induced within the particle increases with increasing frequency, matching the experimental result in which the particle is held in place at the electrode edge at high frequency. At low frequency the surface charge is \(~1.8\text{nC/m}\), whereas at high frequency that value increases to \(~18\text{nC/m}\) across all three solution conductivities computed. The onset frequency for charge accumulation increases with increasing solution conductivity. However, when the particle
is placed in direct contact with the substrate (Figure 2-6b), the particle charge decreases with increasing frequency. This further suggests that the particle does not sit directly on the substrate, but rather floats slightly above with a thin DI water layer in between the particle and the substrate.\textsuperscript{12} The additional resistance and capacitance of the DI water layer is critical in providing the frequency response observed experimentally. At low frequency the resistance dominates, whereas at high frequency the capacitance dominates the DI water layer impedance.\textsuperscript{19-20} The frequency shift in charge accumulation seen with increasing solution conductivity, (Figure 2-6b) comes from an increase in the cross-over frequency from resistance dominated impedance to capacitive dominated impedance as the DI layer resistance decreases.\textsuperscript{20}

![Figure 2-6](image)

Figure 2-6. Using the model described in Figure 2-2 a surface integral is taken of charge across the bottom of the sheet for (a) z-spacing = 10nm and (b) z-spacing = 0.

To expand on the analysis of the charge response in the particle, the simulation for the z-spacing of 10nm was examined more carefully for a solution conductivity of $10^{-5}$ S/cm. A 2D cross-sectional cut of charge density was taken at the bottom surface of the sheet as the applied bias of 20Vpp was fixed and the frequency was varied. Figure 2-7a-c shows plots on a constant scale of 100Hz, 10 kHz and 1 MHz, respectively, where blue represents regions of negative charge and red represents regions of positive charge. From these plots, it is clear that with increasing frequency
the induced charge increases, matching the response shown in Figure 2-5. At 100Hz, there is a maximum positive charge density of 2740 C/m³ and a maximum negative charge density of -6330 C/m³. At 1MHz, both the peak positive and negative charge densities increase by two orders of magnitude to $2.80 \times 10^5$ C/m³ and $-6.13 \times 10^5$ C/m³, respectively. From Figure 2-7(c), the region of the sheet overlapping the positive electrode have a relatively uniform negative charge distribution along the edges of the sheet. This negative charge is opposite in sign to the positively biased electrode on which the particle sits, suggesting this charge is induced within the particle from the underlying electrode. The positive charge at the opposite end of the sheet is not uniformly distributed, but appears to accumulate toward the end of the particle. This suggests this charge results from charge polarization, as such charge will be primarily focused at the poles of the particle.

![Figure 2-7](image_url)

**Figure 2-7.** Plot of charge density in C/m³ for the bottom surface of the sheet in the model described in Figure 2-3, where the sheet is 10nm above the surface of the positively charged electrode. A solution conductivity of $10^{-5}$ S/cm is used with an applied bias fixed at 20Vpp at frequency (a) 100Hz, (b) 10 kHz, and (c) 1 MHz.

The electric-field forces due to the charge induced on the particle surface from the biased assembly electrodes are important in the final stages of the assembly process. This can be seen in Figure 2-8 through consecutive optical microscope images. Using the guiding electrode structure described in Figure 2-4, a bias of 20Vpp, 1MHz was applied to the assembly electrodes and the In$_{0.53}$Ga$_{0.47}$As particles suspended in DI water were dispersed onto the substrate. When the AC voltage is applied, a high electric field gradient forms at the edges of the electrodes and captures
particles from solution. As more particles are captured, they begin to form arrays of particles spaced along the electrode edge. When an additional particle approaches such an array, it aligns to the electrode gap in the space between two particles, and the array dynamically rearranges to form a new spacing. The mechanism for the rearrangement is described schematically in Figure 2-9. From the charge simulation shown in Figure 2-7, there is a positively and negatively charged region at either end of an assembled particle. The electric-field forces due to these charges result in a uniform array spacing when the particle density becomes high, as shown in Figure 2-9a. Both ends of adjacent particles in the array have equal sign charge, resulting in a repulsive force between particles. This is balanced by an attractive force acting diagonally between particles. When a new particle approaches the electrode edge, it too has a positive and negative pole due to polarization of the particle within the electric field. Initially, the repulsive force between two poles of equal sign push the particles apart. However, this is balanced by the attractive force acting diagonally to form a new spacing. This trend will continue with new incoming particles until the electrode edge is saturated by particles.

Figure 2-8. Dark-field optical microscope images showing the formation of a uniform spacing between particles along the electrode edge. After many particles have been captured, they begin to form uniformly spaced arrays. The formation of these arrays can be seen through consecutive dark field optical microscope images.
Figure 2-9. (a) A schematic of the spacing formed by electrostatic interactions between particles. Regions of equal sign charge have a repulsive force, while an attractive force exists between oppositely charged ends. These forces balance to form a uniform particle spacing. (b-c) When an additional particle is assembled in between two previously assembled particles, the electrostatic interactions between the existing particles and the incoming particle balance to form a new particle spacing.

2.4 Directed Assembly

To control particle placement on the substrate during electric-field assisted assembly, an additional dielectric layer containing lithographically defined depressions was added to the interdigitated guiding electrode structure,\textsuperscript{21-23} as shown in Figure 2-10a. The concentration of the electric field gradient within an array of 15µm long, 1µm wide wells patterned in an 800 nm thick PMGI dielectric layer was studied by COMSOL Multiphysics FEM simulation. Figures 2-10b and 2-10c show plots of $\log(\nabla E^2)$ taken at the top surface of the PMGI at 10 kHz and 1 MHz, respectively, with a fixed applied bias of 20V$_{pp}$. The results demonstrate that the field intensity is three orders of magnitude larger in the well as compared to the surrounding regions of the substrate. In addition, Figure 2-10d shows that the average value of $\log(\nabla E^2)$ increases with frequency. The $\nabla E^2$ increases more than three orders of magnitude over the frequency range shown. The $\nabla E^2$ should be maximized in the wells to achieve preferential particle placement, thus higher frequency applied biases (100 kHz-1 MHz) are used in these experiments.
Figure 2-10. (a) Schematic of the electrode structure that is used for the COMSOL modeling in figures b-d. A plot of the $\log(\nabla E^2)$ is shown for this model at 1 MHz (b) and 10 kHz (c). (d) Plot of average $\log(\nabla E^2)$ within the well versus frequency.

The structure in Figure 2-10 was fabricated for experimental validation of the directed assembly process. Starting with a lightly doped n-type Si substrate, a 120nm Si$_3$N$_4$ film was deposited with LPCVD. The interdigitated Ti/Au guiding electrodes were patterned with optical lithography and lifted off. A 12nm HfO$_2$ was deposited by ALD. Lastly, electron-beam lithography was used to pattern the 1$\mu$m by 15$\mu$m wells in an 800nm-thick PMGI layer deposited by spin coating. Using this structure, a $20V_{pp}$, 1MHz bias was applied across the guiding electrodes while the In$_{0.53}$Ga$_{0.47}$As sheets suspended in DI were dispersed on the substrate. Representative FESEM images collected after directed assembly was completed and the solution had dried, are shown in Figure 2-11. Minor shifting in sheet orientation may occur across the die due to the varying meniscus forces during the drying process.$^{24}$ To minimize experimental error, assembly results
were examined across four dies over a >200mm² total area. Over this area, meniscus forces are experienced in multiple directions, so a fixed shift to the mean position is not expected.

The image in Figure 2-11a confirm that the particles preferentially assemble and align within the lithographic wells. The alignment accuracy with respect to these features is determined by measuring the offset of the particles with respect to the edge of the electrode and the well. The x-dimension offset is determined as the difference from the center of the sheet to the edge of the electrode. The y-dimension offset is determined as the offset from the center of the sheet to the center of the well. The statistical variation in alignment accuracy determined by characterizing 40 assembly sites across four dies is presented in table 2-2. In the y-dimension, the particles showed a preference to center within the well. However, in the x-dimension particles consistently have ~4.2µm overlap of the particle across the electrode edge (-800nm center-to-center offset). As shown in Figures 2-11c and d, the preference is found regardless of well registration with respect to the edge of the electrode.

![Figure 2-11](image)

Figure 2-11. (a) A field emission scanning electron micrograph (FESEM) of an In₀.₅₃Ga₀.₄₇As assembled sheets within wells. Long range image demonstrating preferential assembly of tiles in wells. (b) The sheet shows a preference to center in the y-dimension and align with ~4.2µm overlapping along the electrode (-800nm offset from center) independent of the well misalignment with the electrode (c and d).
Table 2-2. Statistics of the x and y placement of assembled sheets in 40 sites across four dies.

<table>
<thead>
<tr>
<th>Center Offset</th>
<th>Mean</th>
<th>Standard Deviation</th>
</tr>
</thead>
<tbody>
<tr>
<td>X</td>
<td>-815nm</td>
<td>-209nm</td>
</tr>
<tr>
<td>Y</td>
<td>64.6nm</td>
<td>53.0nm</td>
</tr>
</tbody>
</table>

The alignment of the particle within the well was studied through COMSOL Multiphysics FEM simulations. Taking the model described in Figure 2-10, a particle was placed within the well with a z-spacing of 10nm above the surface. The applied bias was fixed at 20Vpp, 1MHz and the x-position was swept within the well +/- 2.5µm from electrode edge. The x-component of the force acting on the particle was calculated using the MST method. In Figure 2-12, a plot of force on the particle is plotted vs. x-position with corresponding \( \log(E^2) \) cross-sections taken at the top surface of the substrate. The force on the particle goes to zero at an x-position offset of ~0.8µm, which corresponds to a sheet overlap with the electrode edge of ~4.2µm. This agrees well with the experimental results given in table 2-2.

Figure 2-12. Plot of the x-component of the MST force acting on sheet vs. x-position as the y-position is fixed. Corresponding XY cross-sections of electric field gradient are plotted for 3 positions. As the particle is shifted in the well, an electrical restoring force returns the particle to a preferred position (~800nm offset from electrode edge) at which the force on the particle goes to zero.
The same model was used to sweep the y-position of the particle, and calculate the y-component of the MST force on the particle. The results plotted in Figure 2-13 show that force on the particle goes to zero when the particle was centered within the well, which also agrees with experimentally calculated position.

Figure 2-13. The y component of the MST force on the particle is plotted vs particle y-position, with the particle x-position fixed. As the particle is shifted in the y-dimension within the well, there is a restoring force directing the particle back into the center of the well. The restoring force goes to zero as the particle approaches the center of the well.

Although the particles preferentially assembled within the wells, additional particles were assembled on the thick dielectric layer near the wells. As shown in Figure 2-14a, the particles aligned along the electrode edge, but did not enter the well. It has been well documented that assembled conductive particles screen the local electric field, minimizing the capture probability of additional particles.\textsuperscript{12-13, 25} However, minimal work has been done to study electrostatic interactions between assembled particles on a substrate,\textsuperscript{12} particularly the interaction between a particle assembled within a well and one outside of the well. To better understand this behavior, a second particle was placed adjacent to an occupied well and centered along the electrode edge. The spacing between the second particle and the occupied well was swept from 8µm to 1.3µm, and the MST force acting on the second particle was calculated. Here the spacing is specified as the center-to-center distance between the particle and well. A 2D cross-section of \( \log(\nabla E^2) \) taken at the surface of the substrate is given in Figure 2-14b for a 6µm spacing between the second particle and the occupied well. A force acting in the positive y-direction will repel the particle from entering
the well, while a force in the negative y-direction will attract the particle. The y-component of the force acting on the second particle is compared for occupied and empty well cases in Figure 2-14c. When the well is occupied, a positive force acts on the particle as it approaches the well, repelling the particle from entering the well. This matches the experimental results that show single particles occupy a well with nearby particles not entering the well. When the well is empty, a negative y-component of force corresponds to an attractive force on the particle.

Figure 2-14. (a) FESEM of assembled In$_{0.53}$Ga$_{0.47}$As particles after drying. The assembly was completed in deionized water at 20V$_{PP}$, 1MHz using the electrode structure described in Figure 2-10. (b) A plot of $\nabla E^2$ simulated for a structure with a well occupied by a single particle and a second particle 6 µm away from the well. (c) The y-component of the MST force acting on the particle as a function of position is plotted. Two cases are shown, one when the well is occupied by a sheet and the second when the sheet is empty. The red lines represent a normalized $1/r^2$ and $-1/r^2$ dependence respectively (d) Integral of space charge density within the incoming sheet showing that the sheet has a negative charge build up induced form the positively biased underlying electrode.

To understand this more clearly, a volume integral of space charge density was taken within the particle (Figure 2-14d). This plot shows that a negative charge of -6.7aC is induced within the
particle from the positively biased underlying electrode, and the induced charge has minimal
dependence on the position of particle. As such, the increase in force acting on the incoming particle
from $8.62 \times 10^{-12}$ to $2.47 \times 10^{-11}$ is due to $1/r^2$ dependence of the electrostatic force, as seen in equation
2-9. The clear $1/r^2$ dependence for both the attractive (unoccupied) case and the repulsive
(occupied) case can be seen in the red lines plotted in Figure 2-14c. Due to this dependence, the
force drops off rapidly as the spacing between particle and well increase.

Figure 2-15 shows 2D cross-sectional plots of space charge density taken for the two cases.
When the well is empty, a positive charge density is present in the region overlapping the electrode,
resulting in an attractive force between the particle and the well. However, when the particle is
occupied, there is a negative charge induced in the occupying particle, as seen in Figure 2-15. This
negative induced charge results in a repulsive electrostatic force between the second particle and
the occupied well. This reduces the likelihood that multiple particles will occupy the same well,
minimizing one of the primary defects found in electric-field assisted assembly.26-27

![Figure 2-15. Plot of space charge density in C/m³ for an occupied and unoccupied well. An unoccupied well has a positive charge build-up in the area overlapping the positive electrode. The occupied well has a negative charge build-up in the same region. For this reason there is a repulsive force acting on particles approaching an occupied well whereas a positive force acts on particles approaching an unoccupied well.](image-url)
2.4 Summary and Conclusions

In this chapter assembly of In$_{0.53}$Ga$_{0.47}$As sheets to controlled positions on a Si substrate was demonstrated. Through a combination of experimental data and FEM modeling, the physics behind this assembly process was explained in detail, with a particular emphasis on the short-range forces acting on particles close to the assembly electrode. A comprehensive model demonstrating the complex charge distribution and interactions acting on a particle in the near surface was developed using FEM, offering an origin for the electrostatic interactions between particles on the assembled substrate.

Controlled particle placement was demonstrated through the use of patterned features that tightly fit the assembly particle geometry. A corresponding FEM model showed strong agreement with experiment in predicting alignment of particles on the substrate, verifying the validity of this model, particularly in the near surface regime. This model can be used in the assembly studies of other materials and geometries to predict future behavior. This work demonstrated that electrostatic interactions at the surface of the assembly substrate are critical in determining the final particle alignment.

Lastly, suppressing the formation of multiple particle occupancies at a single assembly site was demonstrated and explained through use of an FEM model. This model demonstrated the charge distribution within a well and subsequent interactions with an incoming particle. Through modulation of the charge density within an occupied well, multiple occupancies which are a known source of assembly defects, can be suppressed. With this approach, electric-field assisted assembly can be implemented to heterogeneously integrate new devices and materials onto alternative substrates, as will be discussed in chapter 3.
2.5 Bibliography


Chapter 3
Heterogeneous Integration of In$_{0.53}$Ga$_{0.47}$As Fin TFETS and MOSFETs onto Silicon Substrates

3.1 Introduction

Scaling of conventional complementary metal-oxide-semiconductor (CMOS) devices for higher performance is increasing chip power consumption, as illustrated in Figure 3-1a. As the gate length is scaled, the passive power consumed by the transistor increases and approaches that of the active power density, leading to an overall increased power demand.$^{1,2}$ The increased power demand is a major issue facing the semiconductor industry, particularly in mobile devices where limited energy is available. One way to overcome this challenge is to lower the operating voltage of the transistors to lower the power consumption. However, lowering the operating voltage results in a reduction of drive current and device performance. To achieve lower operating voltages without a reduction in performance, devices must have steep sub-threshold slopes$^3$ (Figure 3-1b). The metal-oxide-semiconductor field-effect transistor (MOSFET), the current workhorse of the semiconductor industry, is physically limited to sub-threshold slopes of 60mV/decade at room temperature because it relies on current modulation by emission over a barrier. The high energy tail of the Fermi-Dirac distribution of carriers has enough thermal energy to emit over the barrier, limiting the sub-threshold slope.$^4$
Figure 3-1. (a) Plot of subthreshold power density and active-power density with scaling of gate length. As the gate length continues to shrink, the leakage current becomes a greater issue. (b) A MOSFET is fundamentally limited to have a minimum subthreshold swing of 60mV/decade, preventing scaling of the operating voltage. The tunnel FET can achieve steeper subthreshold swing, allowing for low power operation.² Copyright 2002 IEEE. Copyright 2013 Phys.org.

The interband tunnel FET (TFET) is a device that modulates current by changing the width of a tunnel barrier, which in turn filters out the high and low energy tails of the Fermi-Dirac distribution of carriers. This enables sub-threshold slopes below 60mV/decade.³ The n-channel TFET is shown schematically in Figure 3-2a, which is composed of a p⁺-i-n⁺ junction with a gate voltage applied to the i-region. Figure 3-2b shows the band diagram of the TFET in the on (red) and off (blue) state. When no bias is applied to the gate, there is a high density of electrons in the valence band, but the tunnel barrier is too wide for carriers to tunnel to the drain. By applying a gate bias to lower the relative position of the channel, a narrow tunnel barrier forms, allowing carriers to tunnel from source to drain.⁵ The tunneling probability can be described with the Wentzel-Kramers-Brillouin (WKB) approximation,

\[ T = \exp \left( -\frac{4\sqrt{2m^*E_G}}{3q\hbar \xi} \right) \] (3-1)

where \( m^* \) is the carrier effective mass, \( \hbar \) is the reduced Plank’s constant, \( q \) is the charge of an electron, \( E_G \) is the material bandgap and \( \xi \) is the electric field across the junction.
From equation 3-1, to maximize the tunneling probability (and thus device on-current), materials that have a small band-gap, low effective mass and abrupt, degenerately doped junctions are desired. Compound semiconductors, such as In_{0.53}Ga_{0.47}As, which can be grown on a lattice matched InP substrate with abrupt junctions, are strong candidates for TFET devices. As such, a heterogeneous integration strategy is required to incorporate these devices with Si CMOS.

### 3.2 Heterogeneous Integration Strategy

Starting with molecular beam epitaxy (MBE)-grown material having abruptly doped junctions, sheets of In_{0.53}Ga_{0.47}As are released into a solution (Figure 3-3a, b) and assembled onto Si substrates using the electric-field assisted assembly (Figure 3-3c) technique described in chapter 2. These sheets are then processed using top-down fabrication to form fins (Figure 3-3d) and
characterized as p⁺-i-n⁺ junctions with I-V measurements (Figure 3-3e). Lastly, a gate stack is integrated to form fin TFETs. Fin MOSFETs are also fabricated, using an identical process, but with a n⁺-i-n⁺ doped starting layer. Using this approach, a wide variety of III-V compound semiconductors can be integrated onto Si. Additionally, an entire 3-inch wafer can be populated with material using a small area of the initial MBE-grown wafer, offering promise for low-cost integration of compound semiconductor materials.

The p⁺-i-n⁺ and n⁺-i-n⁺ In₀.₅₃Ga₀.₄₇As device stacks used in this research were grown by IQE, Inc. of Bethlehem, PA. Reactive ion etching of the In₀.₅₃Ga₀.₄₇As sheets and fins was completed by Dr. Ning Cao of University of California, Santa Barbara.

This integration process began with the MBE-grown In₀.₅₃Ga₀.₄₇As p⁺-i-n⁺ layer structure shown in Figure 3-4a, which has p⁺⁺ and n⁺⁺ delta doped layers on either side of the junction. Delta doping was used to maximize the tunneling probability by increasing electric field within the junction. Following MBE growth, the substrate was cleaned with an acetone/IPA rinse, and plasma-enhanced chemical vapor deposition (PECVD) was used to grow a 300nm SiO₂ film to
serve as a hard mask during high temperature RIE of the In$_{0.53}$Ga$_{0.47}$As sheets. Full process details can be found in appendix A.2. Next, 10µm long lines with 200nm to 100nm widths were patterned by electron-beam lithography, using Ma-N 2403 resist with a surpass 3000 adhesion layer. The lines were patterned using a multi-pass writing technique where one quarter of the dose was written four times; this alleviated edge roughness that forms from beam fluctuations. The pattern was transferred from the polymer resist layer to the oxide hard mask using a CF$_4$ based ICP-RIE etch. The resist was then removed using an O$_2$ plasma. Using the oxide hard mask, the 620nm In$_{0.53}$Ga$_{0.47}$As film was completely etched to form vertically standing sheets, via a Cl$_2$/H$_2$/Ar chemistry with substrate heating of 200ºC (Figure 3-4). Substrate heating was required because the InCl$_x$ etch by-product has increased volatility at elevated temperatures. The InP substrate was mounted onto a silicon carrier wafer for etching, as small pieces of the InP were used for etching.

![Figure 3-4](image.png)

Figure 3-4. (a) Schematic of MBE device structure used in this work. (b) Tilted FESEM image of etched sheet. (c) FESEM image of array of etched fins.

The sheets were released from the InP growth substrate using a selective wet etch (Figure 3-3b). After the RIE step, a 30s oxygen plasma was used to remove organic contaminants present from the mounting process. The sheets were then annealed in N$_2$ at 350ºC for 20 minutes in a rapid thermal anneal (RTA) furnace to reduce dry etch damage induced during RIE. Prior to release, the sheets were etched in 10:1 BOE for 2 minutes to remove the top etch mask and any SiO$_x$ deposited on the sidewalls during etching. The etched sheets were then placed in a (1:1) hydrochloric acid
and ethanol solution at room temperature, which selectively etched the InP substrate without attacking the In$_{0.53}$Ga$_{0.47}$As film. A dilute HCL solution was used to reduce the etch rate for controlled release of the sheets. Specifically, the sheets must be undercut without completely removing them from the underlying substrate so they can be sonicated into the IPA solution used for assembly (Figure 3-5b). If the sheet is not properly undercut, it may break during sonication (Figure 3-5c). After the initial undercut step in dilute HCl, the substrate was cleaned in ethanol to dissolve the solid etch byproducts that deposit on the substrate during etching. The substrate was immediately transferred into a centrifuge tube containing IPA and sonicated to release the sheets from the InP growth substrate. This left a dense population of In$_{0.53}$Ga$_{0.47}$As sheets in IPA. Full fabrication details can be found in appendix A.2.

![Diagram](image)

Figure 3-5. (a) Schematic cross-section of etched fins. (b) Schematic showing undercutting of fins with wet etch. (c) FESEM of InP substrate with incomplete undercut etch.

The In$_{0.53}$Ga$_{0.47}$As sheets were integrated onto a Si substrate using the electric-field assisted assembly process described in chapter 2. An interdigitated electrode structure coated in polyglutarimide (PMGI) dielectric layer was patterned with an array of 15µm by 1µm wells along
the electrode edges using electron-beam lithography. The sheets were dispersed on the substrate with a 20V$_{pp}$, 1MHz bias applied to the interdigitated guiding electrodes, and the sheets were preferentially assembled within the wells; full details can be found in appendix A.3. Figure 3-6b shows an assembled sheet within a well, where the vertically grown junction is positioned laterally on the substrate. The PMGI dielectric layer was removed via a liftoff process in a dimethylacetamide (DMAc) heated to 60°C, which removed any misaligned sheets from the substrate. This leaves clean In$_{0.53}$Ga$_{0.47}$As sheets in predefined locations on the Si substrate, without misaligned sheets remaining on the substrate (Figure 3-6a).

Figure 3-6. (a) Optical microscope image of assembled In$_{0.53}$Ga$_{0.47}$As sheets. (b) FESEM of sheet assembled within well. (c) Assembled sheet after removal of PMGI dielectric.

The doping junction (p$^+$-i-n$^+$ or n$^+$-i-n$^+$) runs parallel to the short axis of the sheet. To create a functional device, a single sheet must be assembled within the well such that the short axis of the center point is ±120nm from the center of the well. Misalignment greater than this will result in metal contacts shorting the channel region. As described in chapter 2, an alignment 1-sigma of ±53nm across the sheet short axis can be achieved through this assembly process, meeting the desired alignment constraints.

After the In$_{0.53}$Ga$_{0.47}$As sheets were positioned within the lithographically defined wells, they can be patterned and contacted to form In$_{0.53}$Ga$_{0.47}$As fins. In this process, a 60nm-thick SiO$_2$
hard mask was deposited on the cleaned Si substrate; a thinner oxide was used in this step because only 200nm to 100nm of In$_{0.53}$Ga$_{0.47}$As is being etched. Electron-beam lithography was then used to pattern 50nm wide lines across the In$_{0.53}$Ga$_{0.47}$As sheet in ZEP 520A resist using proximity effect correction (PEC). The pattern was transferred into the SiO$_2$ hard mask using a CF$_4$ etch, and the resist was removed in an O$_2$ plasma (Figure 3-7a). The In$_{0.53}$Ga$_{0.47}$As sheet was etched in a Cl$_2$/H$_2$/Ar chemistry, forming an array of fins, with a rectangular cross-section that is 50nm wide and 200nm to 100nm tall (Figure 3-7b). This allows for high density arrays of fins to be formed, with the only limitation in dimensions and pitch being the resolution limits of electron-beam lithography. In this case, a fin pitch of 150nm was demonstrated.

![Figure 3-7. (a) Schematic and FESEM image of patterned etch lines on In$_{0.53}$Ga$_{0.47}$As sheets. (b) Etched fins.](image)

After RIE, the sample was cleaned in an O$_2$ plasma to remove organic residue from the surface. The sample was then annealed in N$_2$ at 350°C for 20 minutes in an RTA furnace to reduce dry etch-induced damage. Source/drain contacts were patterned using electron-beam lithography with a PMMA/MMA double layer resist to achieve a lift-off profile. Prior to metal deposition, the sample was etched in 10:1 BOE for 30s to remove the SiO$_2$ hard mask from the contact area, followed by a 30s 10:1 (H$_2$O:HCl) dip to remove native oxides from the surface. The sample was immediately loaded into the evaporator and 150nm Ti/50nm Pd contacts were deposited using
electron-beam evaporation with substrate cooling to minimize heating of resist. Lift-off was completed by soaking the sample in acetone leaving contacted fin junctions. Full details of the device fabrication can be found in appendix B.1.

3.3 Electrical Characterization of Fin Diodes

Following lift-off, the In$_{0.53}$Ga$_{0.47}$As p$^+$-i-n$^+$ device sites were inspected optically to select devices to be measured electrically. From optical inspection, 828 of the 1200 device sites (69.0%) were occupied by a single sheet, and 418 of these sites (34.8%) had no metal overlap of the intrinsic channel region and good electrical contacts. This was determined by sweeping an applied voltage of -1V to 1V, and measuring the current through the fin, followed by FESEM inspection. The current compliance was set to 20 μA because higher current caused damage to the fin or metal contacts. Figure 3-8a shows a typical device fabricated from a 150 nm thick starting sheet with four 50 nm fins connected in parallel. The plot in black in Figure 3-8b shows a typical current density (J) versus V curve for a fin junction immediately after lift-off. The J-V properties are symmetric, demonstrating no rectifying behavior. During pattern definition with ICP-RIE, ions bombard the surface of the fin, breaking bonds and implanting atomic impurities within the crystal. Additionally, this damage can penetrate up to 500 nm into the crystal by a combination of ion channeling and radiation enhanced diffusion of defects. These defects act as electronic traps states, modifying the electrical behavior of the fin. Furthermore, as the diameter of the fins is scaled, the effects of surface trap states and surface roughness are enhanced, exacerbating the effects of these trap states.

Annealing the sample in N$_2$ for 20 minutes at 350°C in a RTA furnace provides thermal energy for bond reformation, reducing the defect density in the fin. The red curve in Figure 3-8b shows the In$_{0.53}$Ga$_{0.47}$As p$^+$-i-n$^+$ junction performance is significantly improved, with a two order
of magnitude reduction in reverse leakage current and ~1.5 order of magnitude increase in on-current. At 1V, the current density increased from 1.68kA/cm² to 52.6kA/cm², while at -1V the current density decreased from 1.88kA/cm² to 0.0181kA/cm².

Figure 3-6c plots the ideality factor of the annealed fin, which approaches 2.5 at 0.2V. An ideality factor greater than 2 suggests that the defect density within the fin is still large, leading to the enhanced recombination of carriers. Furthermore, while RTA steps were employed twice prior to deposition of source/drain contacts, these anneals were largely ineffective, based on the initial device measurement. This suggests that the non-rectifying device behavior must be due to surface leakage through trap states and conductive native oxides on the surface, as bulk crystalline damage should have largely recovered during the initial annealing steps. Historically the passivation of surface states in III-V compound semiconductors has been challenging, suggesting the fins are susceptible to generation of surface states during RIE.

Figure 3-8. Fin junction array: (a) FESEM image of fin array contacted with a Ti/Pd source/drain contact. (b) Plot of fin I-V before and after 20 minute anneal in N₂ at 350°C. (c) Ideality plot of annealed fin.
Initially, the annealing was completed in a forming gas (nitrogen and hydrogen) background because this process has been used to reduce the interface trap state density in In$_{0.53}$Ga$_{0.47}$As metal-oxide-semiconductor (MOS) capacitors.$^{19,20}$ It is believed that hydrogen reacts with catalytic metal contacts to form atomic hydrogen, cleaning the In$_{0.53}$Ga$_{0.47}$As surface.$^{20}$ However, when a forming gas was used, the Ti/Pd source drain contacts often delaminated (Figure 3-9c), making device reproducibility challenging. Hydrogen has been shown to degrade titanium alloys, forming dislocations and cracking with the formation of titanium hydrides.$^{21}$ To eliminate this problem, the forming gas was replaced by N$_2$ to overcome delamination. Fin junctions annealed in both environments were directly compared and show very similar J-V response (Figure 3-9a) and ideality factor (Figure 3-9b). The variation between the two cases can be attributed to device-to-device variation, which is typically significant in nanoscale devices.$^{22}$ In particular device-to-device variation in this work can be attributed to variations in the number of fins contacted,$^{23}$ surface roughness$^{24}$ and dimensional non-uniformity in patterning and etching.$^{25}$ By annealing the fins in a N$_2$ background, issues with contact delamination were resolved without sacrificing improvement in device performance.
Figure 3-9. (a) I-V and ideality (b) comparison of fin devices annealed in forming gas and N$_2$ ambient. (c) FESEM showing contact delamination occurring after anneal in forming gas.

To scale the dimensions of the fin, the thickness of the starting sheet was reduced from 200nm to 100nm. This cut the height of the fin in half. However, in scaling the dimensions of the fin, the effectiveness of the annealing step was reduced. For 200nm and 150 nm wide sheets, as seen in Figure 3-10b and c, the 350°C anneal was effective in improving device performance by lowering the reverse leakage current and improving the junction ideality factor. Any device variation between these two cases can be attributed to variations in the number of fins contacted, surface roughness and dimensional non-uniformity in patterning and etching. However, when the starting fin width was scaled to 100nm (Figure 3-10a), the annealing step was no longer effective. This suggests that with further scaling, the dry etch damage penetrates entirely through the fin and cannot be recovered with annealing. This challenge can be circumvented by patterning larger dimension fins with dry etching and scaling to smaller dimensions through a digital wet
In this research, the scaled fin devices were used for TFET device integration to minimize the device dimensions.

Figure 3-10. (a) Plot of as-etched and annealed fin p-i-n junction fabricated from a 100nm wide, (b) 150nm wide, and (c) 200nm wide starting sheet.

### 3.4 MOSFET and TFET Integration

The FIN TFETs were fabricated by depositing a gate dielectric and gate metal to electrostatically modulate the i-channel region. However, deposition of high-k dielectrics on In$_{0.53}$Ga$_{0.47}$As is not a straightforward process due to the complexity of the interface of this ternary compound.\textsuperscript{27} In$_{0.53}$Ga$_{0.47}$As has native oxides of poor electrical quality, which results in high interface trap densities.\textsuperscript{28} Therefore, it is critical to reduce native oxide present on the surface and passivate surface trap states to fabricate high quality FETs.
Figure 3-11. (a) Schematic of MOS capacitor used to analyze gate stack. (b) C-V plot for MOS capacitor with frequency sweep from 75 kHz to 2MHz.

The gate stack was first characterized with a planar MOS capacitor, which is shown schematically in Figure 3-11a, prior to implementation on the TFET device. This was done starting with the same MBE-grown In$_{0.53}$Ga$_{0.47}$As p$^+$/i/n$^+$ layer structure used for the TFET work. The sample was etched in a 20:1 citric acid:H$_2$O$_2$ solution for 280s to completely remove the top p$^+$-region, exposing the i-channel region. The substrate was then cleaned with acetone and IPA to remove organic contaminants, dipped in a 10:1 (H$_2$O:HCl) solution to remove native oxides, and immediately loaded into an atomic layer deposition (ALD) chamber heated to 300°C. Once loaded, tetramethylaluminum (TMA) was pre-pulsed to clean the surface because TMA has been shown to reduce the presence of As-O and Ga-O bonds$^{29,30}$ and passivate As dangling bonds.$^{27}$ Next, a thin 1nm Al$_2$O$_3$ film was deposited by pulsing TMA and H$_2$O to further passivate the surface. A 5nm HfO$_2$ film was deposited by pulsing water and tetrakis(ethylmethy lamino)hafnium (TEMAH). Lastly, a Ti/Pd gate was deposited with electron-beam evaporation using a shadow mask to define the pattern; full process details can be found in appendix B.2.

The MOS capacitor was characterized by sweeping the bias from -1.8V to 2V at frequency varying from 75 kHz to 2MHz. The C-V properties plotted in Figure 3-11b achieve a $C_{\text{max}}$ of
2.5\(\mu\)F/cm\(^2\) with an equivalent oxide thickness of 1.26nm. Using the conductance method,\(^{28}\) an interface trap density, \(D_{it}\), of 5.02\(\times\)10\(^{12}\) cm\(^{-2}\)eV\(^{-1}\) was calculated. This gate stack compares favorably with gate dielectrics deposited in a high vacuum system\(^{27}\) and exposed to in-situ cleaning,\(^{31,32}\) all of which should provide better interface control than the ex-situ cleaned low vacuum deposition done in this work.

The p\(^+\)-i-n\(^+\) fin TFET fabrication was completed by depositing the gate stack using this same process. Specifically, the etched surfaces were cleaned using Acetone and IPA followed by a 30s dilute dip prior to loading the sample into the ALD chamber. A TMA pre-pulse followed by ALD of 1nm Al\(_2\)O\(_3\) and 5nm of HfO\(_2\) completed the gate dielectric deposition. The gate dielectric conformally coated the entire sample surface, thereby acting as an electrical isolation layer between the source/drain contacts and gate. Using a PMMA/MMA resist stack, electron-beam lithography was used to pattern a gate metal to directly cover the fin and overlap with source and drain contacts to compensate for sheet placement error during assembly. The 150nm Ti/50nm Pd contacts were deposited with electron-beam evaporation, and the excess metal was lifted off in acetone. A finished TFET device is shown in the FESEM image in Figure 3-12a. Figure 3-12b shows a cross-sectional schematic of this device, with a top gate that overlaps source and drain contacts.

![FESEM image of a four fin TFET device](image)

![Cross-sectional schematic of fin TFET device](image)

Figure 3-12. (a) FESEM image of a four fin TFET device. (b) Cross-sectional schematic of fin TFET device.
The electrical properties of a typical TFET device is shown in Figure 3-13. Figure 3-13a plots the $J_{DS}$-$V_{DS}$ characteristics as the drain bias is swept from -1V to 1V at gate biases of -1V, -0.5V, 0V, 0.5V and 1V. Gate biases greater than ±1V caused the gate dielectric to break down and short the source and gate. At a gate bias of 0V (shown in blue), the response is consistent with the measurements of the unpassivated junctions without any gate bias (Figure 3-10a), with an on-off ratio of ~2. The drain current increased with increasing gate bias for all drain voltages measured.

The forward bias current at $V_{DS}$ of 0.5V increased from 158µA/µm at $V_{GS} = -1V$ gate bias to 1650µA/µm at $V_{GS} = 1V$. The reverse bias current at $V_{DS}$ of -0.5V increased from 121µA/µm at $V_{GS} = -1V$ to 1165µA/µm at $V_{GS} = 1V$.

BTBT tunneling should be the primary current mechanism in a TFET device. However, there is not a clear onset of negative differential resistance (NDR) in the forward bias, suggesting band-to-band tunneling (BTBT) is not prevalent in this gate bias range. Due to the high defect density, SRH generation-recombination and trap-assisted tunneling most likely dominate in this device, preventing a significant contribution from BTBT. Figure 3-13b shows a $J_{DS}$-$V_{GS}$ plot as $V_{GS}$ is swept from -1V to 1V, in 100mV intervals, at $V_{DS}$ of -100mV and -200mV. At $V_{DS}$ of -100mV, the on/off ratio is ~160 and the subthreshold slope is 660mV/decade. At $V_{DS}$ of -200mV the on/off ratio reduces to ~80 and the subthreshold slope decreases to 960mV/decade. This shows better subthreshold switching than other work on dry etched In$_{0.53}$Ga$_{0.47}$As nanoscale TFETs, but is still well above the 60mV/decade limit of MOSFETs. By reducing the defect density induced from dry etching the effect of parasitic current mechanisms can be mitigated, improving device performance.
The TFET is a minority carrier device, which relies on conduction through minority carriers that have a finite lifetime before they will recombine. Increased trap state densities from dry etch damage will greatly reduce that lifetime, resulting in a degradation in device performance. In contrast, MOSFET’s are majority carrier devices, and thus will have much less performance degradation with the presence of trap states. Due to the higher carrier density of majority carrier devices, recombination in trap states will have a smaller impact on device current than for minority carrier devices. For this reason, an In$_{0.53}$Ga$_{0.47}$As fin MOSFET was fabricated using an identical process to the one used for TFET fabrication. The only change was the doping profile of the starting material, now containing an n$^+$-i-n$^+$ doping profile, with n$^+$ ($5\times10^{19}$ cm$^{-3}$ Si-doped) source and drain both 260nm separated by a 100nm intrinsic channel. This highlights the flexibility of this technique, where entirely different device structures can be integrated onto the same Si substrate.
Figure 3-14. (a) $J_{DS}$-$V_{DS}$ plot at varying gate bias and (b) $J_{DS}$-$V_{GS}$ plot at varying $V_{DS}$ for In$_{0.53}$Ga$_{0.47}$As fin MOSFET.

Figure 3-14a shows typical output characteristics of an In$_{0.53}$Ga$_{0.47}$As MOSFET, which confirms the n-type enhancement mode properties of the device. The $J_{DS}$-$V_{GS}$ plots taken at $V_D$ of 100mV and 200 mV are shown Figure 3-14b. At $V_D$ of 100mV, the device has an on/off ratio of $\sim 10^3$ and a subthreshold slope of 280mV/decade. This is a one order of magnitude improvement in on/off ratio and a reduction of subthreshold slope by greater than a factor of two over the TFET at 100mV. A threshold voltage of -0.38V is extracted through the extrapolation in the linear region (ELR) method. This device shows a reduction in electrostatic control with increasing $V_{DS}$ as seen by the increase in subthreshold slope to 380mV/decade at 200mV. By comparison, state-of-the-art In$_{0.53}$Ga$_{0.47}$As nanowire FETs on lattice matched substrates demonstrated enhancement mode behavior with subthreshold slopes of 72-63mV/decade and threshold voltages of -0.12V to -0.5V. These devices also show a reduction in on/off ratio and increase in subthreshold slope within increasing $V_{DS}$. This work has a comparable threshold voltage, but the subthreshold slope is higher by approximately a factor of four. However, the state of the art nanowire is on a lattice matched InP substrate, not a Si substrate. Additionally, it has a wrap around gate that improves electrostatic control.
A Technology Computer-Aided Design (TCAD) Sentarus model was created to simulate the response of the In$_{0.53}$Ga$_{0.47}$As MOSFET. In this model, a 3D In$_{0.53}$Ga$_{0.47}$As finFET with a 100nm channel length, 50nm channel width and 75nm fin height was built. A source/drain doping of $10^{20}$ cm$^{-3}$ and an intrinsic channel with carrier density of $6 \times 10^{11}$ cm$^{-3}$ were used. Figure 3-15a compares the measured and simulated device properties, which confirms the close agreement between the two. In this case, the channel has a low carrier density, and thus the junction of the source-channel and drain-channel will have wide depletion widths to compensate the charge of the heavily doped source and drain. As $V_D$ is increased, the depletion width of the drain widens, hindering electrostatic control of the channel by the gate.

In Figure 3-15b, a plot is shown using the same model, but now modulating the channel doping. By increasing the channel doping from the intrinsic value to $10^{16}$ cm$^{-3}$, there is an improvement in the subthreshold slope at 0.2V from ~350mV/decade with an intrinsic channel to ~250mV/decade with a more heavily doped channel. Switching to an optimized design, such as using a moderately p-type doped channel and lightly doped-drain$^{10}$ to minimize the depletion width of the source-channel and drain-channel junctions, will improve electrostatic control of channel region. Additionally, transitioning from a finFET to a gate-all-around nanowire will improve electrostatic control of the channel region to improve device performance.$^{39}$ Implementation of these enhancements as well as reduction in the dry etch induced damage through the use a combined dry etch and wet etch patterning will push this device toward state-of-the-art performance.
Figure 3-15. (a) Comparison of measured devices to simulated $I_{DS}$-$V_{GS}$ plot. (b) Simulated plots of $I_{DS}$-$V_{GS}$ with different channel doping densities.

3.5 Summary and Conclusions

In this chapter, 50nm wide, 200nm tall p$^+$-i-n$^+$ fin junctions were integrated onto a Si substrate through a hybrid top-down bottom-up fabrication strategy. Initially after applying source/drain contacts, the junctions did not show rectifying behavior, but with the application of an N$_2$ anneal, rectifying behavior was revealed. As the height of the fin was scaled from 200nm to 100nm, annealing was no longer effective at restoring the device performance. This scaling limitation can be overcome by a combination of dry and wet etching.

Expanding upon this integration strategy, the In$_{0.53}$Ga$_{0.47}$As fin junctions were converted into TFETs through implementation of an Al$_2$O$_3$/HfO$_2$ dielectric layer and a Ti/Pd gate metal. This was a proof of concept demonstration, offering a versatile and low temperature integration scheme that can be used to integrate a wide variety of materials onto Si for integration with CMOS. Additionally, this approach allows the implementation of a high device density, with a fin pitch of 150nm demonstrated. However, dry etch induced damage generates leakage currents that prevented the onset of NDR. These devices did demonstrate switching behavior with an on/off ratio of ~160.
and a subthreshold slope of 660mV/decade at $V_{DS} = -100$mV. Through use of an optimized dry etch, surface damage can be minimized improving device performance.

In parallel to the TFET, an n$^+$/i/n$^+$ starting material was used in the same integration strategy to demonstrate an In$_{0.53}$Ga$_{0.47}$As finFET on Si. The MOSFET being a majority carrier device is much less susceptible to surface states, resulting in an improvement in device performance over the TFET. This device had on/off ratios of $\sim 10^3$ and a subthreshold slope of 280mV/decade at $V_{DS} = 100$mV. However, the device exhibited degraded performance at high drain bias due to depletion of the channel from the drain-channel junction. A Sentarus model confirms this effect, and further modeling demonstrates that through optimization of the device design, high drain bias device performance can be improved. Through a combination of improved device design and reduction of dry etch damage, the device performance can be improved to approach 60mV/decade subthreshold slope.

3.6 Bibliography


Chapter 4

Dry Etch Damage in In$_{0.53}$Ga$_{0.47}$As

4.1 Introduction

Dry etch damage is a significant factor in device performance degradation in the submicron In$_{0.53}$Ga$_{0.47}$As fin tunneling field-effect transistors (TFETs) and metal-oxide semiconductor FETs (MOSFETs) presented in Chapter 3. This damage is present in submicron compound semiconductor devices independent of substrate or integration strategy$^{1-2}$. Trap states derived from dry etch induced defects result in enhanced Schottky-Read-Hall (SRH) generation and trap-assisted tunneling (TAT) currents.$^3$ These non-ideal currents increase device off-current and degrade the sub-threshold slope of TFET devices.$^4-5$ The addition of trap states within the channel of MOSFETs will decrease channel mobility and degrade device performance.$^6$ The research presented in this chapter characterizes the extent of the dry damage and determines a post-etch annealing process to repair the damage.

During dry etching, ions bombard the crystal surface and penetrate into the compound semiconductor material, breaking bonds and forming defects.$^7$ Figure 4-1 shows a schematic of dry etch induced damage in a typical semiconductor crystal. In the near surface (region I), there is a high flux of ion bombardment, which results in a high density of defects and a variation from the bulk stoichiometry.$^8$ In some cases, the defect density is so large that the crystal structure is degraded and a thin amorphous film forms.$^7$ Deeper into the crystal (region II), the starting stoichiometry is retained, and there are point defects and a low density of defect aggregates.$^8$ The last region contains a low density of point defects and interstitials that can penetrate up to 500nm into the crystal.$^9$ The damage penetrates significantly deeper than expected for low energy incoming
ions that, in most plasmas, have energies less than 1keV. Deep level damage (region III) occurs due to a combination of channeling of incoming ions and radiation enhanced diffusion of defects. Plasmas containing hydrogen have been shown to have an increased depth of damage due to the low atomic mass and radius, with damage being reported up to 1.1µm into the material. Additionally, hydrogen has been shown to passivate dopants within semiconductors through the formation of hydrogen-dopant complexes.

While the deep level damage is generally not detectable by transmission electron microscopy (TEM), electronic device performance is extremely sensitive to very low defect densities. In this work, large-area mesa In$_{0.53}$Ga$_{0.47}$As p$^+$-i-n$^+$ tunnel junctions are fabricated on a lattice-matched InP substrate to quantify reactive ion etch (RIE) induced damage. This device is a precursor to the TFET that allows for the characterization of non-ideal current components. The p$^+$-i-n$^+$ In$_{0.53}$Ga$_{0.47}$As layer structure was grown by IQE, Inc. of Bethlehem, PA. RIE of the large-area In$_{0.53}$Ga$_{0.47}$As device mesas was completed by Dr. Ning Cao of University of California, Santa Barbara.

Figure 4-1. Schematic of different damage regions generated during reactive ion etching.
4.2 P⁺-I-N⁺ Mesa Devices

Starting with the molecular beam epitaxy (MBE) grown In₀.₅₃Ga₀.₄₇As film described in chapter 3, large area mesa isolated p⁺-i-n⁺ junctions were fabricated by dry etching, wet etching and a combination of both etch techniques. This allowed the dry etch induced damage to be directly compared to a wet etched control device that was not exposed to ion bombardment. The geometry of these large-area devices allow for the separation of non-ideal bulk and surface current components. Table 4-I summarizes the four sets of mesa devices fabricated. These devices were fabricated first by cleaning the as-grown In₀.₅₃Ga₀.₄₇As surface with acetone and IPA, and then depositing a 200nm silicon dioxide (SiO₂) hard mask by plasma-enhanced chemical vapor deposition (PECVD). Next, large-area 80µm x 320µm mesas were patterned using electron-beam lithography with Ma-N 2403 resist. The oxide hard mask was defined using a CF₄ ICP-RIE etch at 5°C; a low substrate temperature was used to reduce resist reflow. The resist was then stripped in an O₂ plasma.

Table 4-1. Table of different large area mesa diode conditions examined.

<table>
<thead>
<tr>
<th>Sample Name</th>
<th>Mesa Etch</th>
<th>Post Etch Treatment</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dry Etched</td>
<td>35s (1.4mTorr, 125/800W, Cl₂/H₂/Ar = 7.4/11.6/2sccm)</td>
<td>None</td>
</tr>
<tr>
<td>Dry + 180nm wet</td>
<td>28s (1.4mTorr, 125/800W, Cl₂/H₂/Ar = 7.4/11.6/2sccm)</td>
<td>3 minutes in 20:1 (citric acid:H₂O₂)</td>
</tr>
<tr>
<td>Dry + 350C RTA</td>
<td>35s (1.4mTorr, 125/800W, Cl₂/H₂/Ar = 7.4/11.6/2sccm)</td>
<td>20 minute RTA at 350°C in N₂ environment</td>
</tr>
<tr>
<td>Wet Etched</td>
<td>8 minutes in 20:1 (citric acid:H₂O₂)</td>
<td>None</td>
</tr>
</tbody>
</table>

Devices were fabricated using the different mesa etch conditions described in Table 4-1. All dry etching was completed in a Uniaxis VLR ICP-RIE with a Cl₂/H₂/Ar chemistry at a substrate temperature of 200°C. The In₀.₅₃Ga₀.₄₇As samples were mounted onto a 4-inch diameter silicon
(Si) carrier wafer using DOW CORNING® high vacuum thermal grease to maintain a controlled and reproducible sample temperature during etching. Following etching, post-etch treatments were implemented as described in Table 4-1. It should be noted that the “Dry + 180nm wet etch” condition was dry etched for seven seconds less than the other dry etched samples. This was done to leave n+ material at the base of the device (Figure 4-2c) because 180nm of In_{0.53}Ga_{0.47}As is removed during final wet etching step. Lastly, source and drain contacts were defined by electron-beam lithography using a PMMA/MMA resist stack. Immediately prior to deposition, the sample was dipped in 10:1 BOE for 3 minutes to remove the oxide hard-mask, followed by a 30s 10:1 (H_{2}O:HCl) dip to remove native oxides on the surface prior to contact deposition. The sample was immediately loaded into the evaporation chamber, and 50nm Ti/150nm Pd contacts were deposited using electron-beam evaporation. Lift-off in acetone was completed to remove excess metal, defining the contacts. Full fabrication details can be found in appendix C.

Figure 4-2. (a) Top view FESEM of large-area, dry etched p+-i-n+ junction devices. (b) Tilted FESEM of dry etched mesa sidewall. (c) Schematic cross-section of the device.
Figure 4-2a shows a top-view field emission scanning electron microscope (FESEM) image of a typical mesa isolated In$_{0.53}$Ga$_{0.47}$As dry etched junction device, while Figure 4-2b shows a tilted FESEM image of the same device confirming a smooth sidewall with minimal surface roughness. Figure 4-3a shows a typical current voltage (I-V) plot and corresponding ideality factor (Figure 4-3b) for the conditions described in Table 4-1. The red curve shows the properties of the dry etched device without any post-etch thermal or wet chemical treatment. The junction has a high reverse leakage current and an ideality factor of 2.24 at 0.3V, indicating the presence of a high trap state density$^{22}$ from dry etch induced defect formation. Removing 180nm of In$_{0.53}$Ga$_{0.47}$As from the mesa sidewall (green curve) results in a significant improvement in the forward bias response with a reduction in the ideality factor to 1.40 at 0.3V. By comparison, the wet etched control (black curve) shows an ideality factor of 1.23 at 0.3V. Despite the dramatic improvement in properties following the wet etch, the reverse bias leakage is still a factor of ten times larger than the wet etched control. This suggests that the dry etch damage penetrates deeper than 180nm into the bulk material because the junction performance following this etch is still worse than the wet etch control.

The dry etched mesa devices were annealed at 350°C for 20 minutes in a N$_2$ background (blue curve). This process results in a 2.5 orders of magnitude reduction in the reverse leakage current and an improvement in the ideality factor to 1.33 at 0.3V. The electrical properties of these junctions are comparable to the wet etch control. This suggests that annealing is able to repair the defects that act as trap states within the crystal. To further analyze this behavior, temperature dependent measurements were taken for junctions fabricated using these different processes.
4.3 Temperature Dependent Measurements

Low temperature measurements were used to separate the thermally dependent current mechanisms, and to identify the dominant sources of leakage present in each device type. The devices were placed into a LakeShore TTP6 Probe Station and pumped down to a pressure of $1 \times 10^{-6}$ Torr to remove moisture in the system for reliable low-temperature measurements. I-V characteristics were collected at sample stage temperatures ranging from 400K to 78.5K (350K to 100K for the wet etched control). At each step, the temperature was held for 30 minutes to allow the stage to equilibrate prior to measurement. Figure 4-4a shows a typical plot of the wet etched control at varying temperatures.

In the low reverse bias regime (>0.4V), the current decreases with decreasing temperature to a current floor of $4.2 \times 10^{-12}$A at 100K. At temperatures above 200K, the current is dominated by Schottky-Read-Hall (SRH) generation, where electron-hole pairs are generated through use of a mid-gap trap state as illustrated schematically in Figure 4-5a. SRH generation current has a temperature dependence of:
\[ I_{G-R}(T) \propto \frac{n_i}{\tau_{\text{eff}}} \propto \exp \left[ \frac{-E_T}{kT} \right] \]  

(4-1)

where \( n_i \) is the intrinsic carrier concentration, \( \tau_{\text{eff}} \) is the effective carrier lifetime, \( E_T \) is the trap state energy, \( k \) is Boltzmann’s constant and \( T \) is temperature.\(^{23}\) At low temperature, there is not enough thermal energy to generate electron-hole pairs, and the SRH current component is minimized.

Figure 4-4. (a) I-V plot for wet etched mesa devices at varying temperature. (b) Arrhenius plot of same device at two reverse bias voltages of -0.1V and -0.8V. There is a transition from a temperature dependent to a temperature independent region at low reverse bias voltage of -0.1V.

The temperature dependence of the current is demonstrated more clearly in the Arrhenius plot at low reverse bias (-0.1V, black points) that is shown in Figure 4-4b. At -0.1V, there is an exponential dependence of current on temperature at high temperatures (350K-250K) with slope corresponding to \(-E_T\) (Equation 4-1). In this region, \( E_T = 0.42\text{eV} \), which corresponds to approximately half the bandgap of In\(_{0.53}\)Ga\(_{0.47}\)As. This indicates that the dominant leakage mechanism is SRH generation through mid-gap trap states.\(^{24}\) At low temperatures (< 200K), the current is independent of temperature, and it approaches a minimum value. At these low temperatures, there is no longer sufficient thermal energy for a significant carrier generation, and subsequent generation current component. As such, the current is most likely due to diffusion of the intrinsic carriers.\(^{25}\)
At high reverse bias (< -0.4V) and low temperatures (<200K), a distinct exponential response is observed in the I-V, (Figure 4-4a), corresponding to direct band-to-band tunneling (BTBT). Tunneling current can be described using the Wentzel-Kramers-Brillouin (WKB) tunneling approximation:

\[ T_{WKB} = \exp \left( -\frac{4\sqrt{2m^*E_G}}{3qh\xi} \right) \]  

(4-2)

where \( m^* \) is the carrier effective mass, \( q \) is the charge of an electron, \( h \) is the reduced Planck’s constant, \( E_G \) is the bandgap of the material and \( \xi = \sqrt{\frac{q(\Psi_{bi}-V)N_A N_D}{2\varepsilon_s(N_A+N_D)}} \) is the electric field within the junction. In this equation, \( N_A \) and \( N_D \) are acceptor and donor density on either end of the junction, \( \Psi_{bi} \) is the built-in potential, \( \varepsilon_s \) is the semiconductor permittivity and \( V \) is the applied bias. From equation 4-2, it can be shown that \( T_{WKB} \propto \exp(-\frac{1}{\sqrt{-V}}) \), which is exponentially dependent on the inverse of the square root of the applied reverse bias voltage. Figure 4-4a overlays a calculation of \( T_{WKB} \propto \exp(-\frac{1}{\sqrt{-V}}) \) to the 100K I-V curve (gray curve), showing a strong agreement between experiment and theory. In this case, there is sufficient band bending that a finite tunnel barrier exists, and the onset of BTBT occurs, as demonstrated schematically in Figure 4-5b.

The temperature dependence is observed more clearly through the Arrhenius plot taken at high reverse bias (-0.8V, red points in Figure 4-4b). At high temperatures (350K to 250K), there is an exponential region with a large temperature dependence. The extracted activation energy of 0.29eV is less than half the mid-gap of In\(_{0.53}\)Ga\(_{0.47}\)As, suggesting that SRH generation is not the dominant current mechanism at high bias. The reduction in the slope of the Arrhenius plot suggests a contribution from a current mechanism with low temperature dependence such as BTBT. At low temperatures (< 200K), the current is nearly independent of temperature. The temperature dependence of BTBT current is due to changes in the bandgap of In\(_{0.53}\)Ga\(_{0.47}\)As as given by:
\( I_{\text{tun}}(T) \propto \exp\left(-E_G(T)^\frac{3}{2}\right) \),\(^{26}\) which is negligible over the temperature range studied here. This indicates that the dominant current component in this bias and temperature regime is BTBT, which is indicative of a low trap state density for high quality TFET and MOSFET devices.

Figure 4-5. (a) Schematic of Shockley-Read-Hall generation current mechanism. (b) Schematic of band-to-band tunneling mechanism.

The dry etched control sample was analyzed using the same procedure. Figure 4-6a shows the temperature-dependent I-V plots for the dry etched control. In contrast to the wet etched junction, a current floor is not reached as the temperature of the dry etched junctions is lowered in the low reverse bias regime (>0.4V). Instead, as shown by the calculated curve (gray curve), the current follows a \( T_{\text{WKB}} \propto \exp\left(-\frac{1}{\sqrt{-V}}\right) \) dependence over the entire bias regime at 78.5K. This suggests that a tunneling mechanism is present even at low bias. In wet etched control (Figure 4-4a), BTBT tunneling is not observed for reverse biases less than -0.4V, below which there is insufficient band bending for a significant direct tunneling component. This suggests that the dominant current mechanism in these dry etched junctions is due to trap-assisted tunneling (TAT). As shown in Figure 4-6c, carriers tunnel from the source to a trap-state within the band-gap, and then from that trap state to the drain.\(^{27}\) By using the trap state as an intermediate level, the effective tunnel barrier is reduced, and the onset of tunneling current occurs at lower reverse bias than BTBT.
By extracting the trap state energy from the high temperature regime of the Arrhenius plot in Figure 4-6b, trap state values of 0.17eV (at -0.8V) and 0.23eV (at -0.1V) are calculated. These energies correspond to ~E_g/3, matching other reported modeling of TAT in III-V compound semiconductor photodiodes.28

Figure 4-6. (a) I-V plot for dry etched mesa devices at varying temperature. (b) ln(I) vs. 1/kT plot taken at two voltages. (c) Schematic of trap-assisted tunneling current (d) Schematic of transition from TAT to diffusion current occurring at current valley.

Figure 4-6a shows the onset of negative-differential resistance (NDR) for the forward biased junction at low temperature (≤100K). This is a clear indicator that tunneling current23 dominates the properties of these p+-i-n+ junctions in this temperature and bias range. As the applied forward bias is increased, the band offset shifts to reduce the number of available states in the drain for tunneling. This results in a decrease in tunneling current between 0.05V and 0.15V. At higher forward bias, a transition occurs from TAT dominated to diffusion dominated current, as depicted in Figure 4-6d. This transition point results in a valley that is observed in the 78.5K measurement.
at approximately 0.15V. This non-ideal TAT current mechanism will degrade TFET performance by increasing the off-state current and reducing gate control.\(^4\)\(^5\) This current arises from a high trap state density induced during dry etching, and must be eliminated for high performance devices.

![I-V plot](image)

**Figure 4-7.** (a) I-V plot for dry etched + 350°C RTA mesa devices at varying temperature. (b) ln(I) vs. 1/kT plot taken at two voltages. There is a transition from temperature dependent current to a temperature independent region associated with a tunneling mechanism.

It has been shown that post dry etching thermal annealing is effective at partially restoring device performance.\(^29\)-\(^31\) This dissertation research annealed a dry etched mesa diode device at 350°C in N\(_2\) for 20 minutes prior to application of source and drain contacts. Figure 4-7a shows the temperature dependent I-V for a 350°C annealed dry etched mesa diode. In the low bias regime (>0.4V) at 100K, a current floor of \(~2.3 \times 10^{-12}\) A was reached, which is approximately a factor of two lower than the wet etched control (Figure 4-4a). The lack of a voltage-dependent current in the low reverse bias regime (-0.3V to 0V) suggests that the large TAT component, visible in the dry etched control, has been alleviated. As shown in the Arrhenius plots in Figure 4-7b, at low reverse bias (-0.1V, black points), a transition occurs from an exponential response at high temperature to a temperature independent region at low temperatures. A trap state energy of 0.42eV is calculated at high temperature, identical to the wet etched control. This suggests SRH generation current dominates in this regime, and TAT does not appear to be present.
The high reverse bias range in Figure 4-7a shows an exponential tunneling response at low temperatures (gray curve) that is comparable to the wet etched control. From the Arrhenius plot in Figure 4-7b at high reverse bias (-0.8V, red points), a transition occurs from a large temperature dependence at high temperature (400K-293K), to minimal temperature dependence at low temperature (≤250K). The trap state energy calculated in the high temperature regime is 0.42eV, suggesting that SRH dominates at high temperature. There appears to be a contribution from BTBT at high temperature in the wet etch control, as indicated by a deviation in trap state energy from $E_g/2$ to 0.29eV at -0.8V. This reduction in trap state energy from the mid-gap trap state suggests a contribution from a current mechanism with low temperature dependence such as BTBT in the wet etched control. The presence of a larger SRH current contribution in the annealed sample suggests a higher trap state density in this device.

From these low temperature measurements, it is apparent that the 350°C anneal can recover the junction performance to closely match the wet etched control. Annealing mitigates the large TAT current component that was clearly visible in the unaltered dry etched sample. However, the increase of the trap state energy from 0.29eV (wet etch control) to 0.42eV (350°C annealed) at high temperature and bias suggests that SRH generation current has a more significant contribution in the annealed sample. As such, to further optimize this anneal, the dependence on annealing temperature was studied.

4.4 Anneal Temperature Dependence

Annealing studies were completed on the dry etched junctions at different temperatures to understand the effect of thermal treatment on In$_{0.53}$Ga$_{0.47}$As $p^+$-$i$-$n^+$ junction recovery. A fixed ambient background gas and time interval were used, and the annealing temperature was changed. The mesa devices were fabricated in an identical manner to the 350°C annealed sample in section
4.2; all annealing was completed in N$_2$ background without passivation, prior to source/drain contact deposition. Annealing temperatures of 350°C, 400°C, 450°C, 490°C and 550°C were examined (Table 4-2) and compared to the wet etch control. A typical I-V curve and ideality factor is plotted for each condition in Figure 4-8a and b, respectively. The sample annealed at 550°C (light blue curve) had a high reverse leakage current and poor ideality factor compared to the wet etched control. This occurs because the high annealing temperature results in decomposition of the In$_{0.53}$Ga$_{0.47}$As surface, increasing the defect density on the surface and introducing trap states. The 490°C to 350°C annealed samples all have similar reverse bias behavior and ideality factor to the wet etched control, with a reverse leakage current of 10$^{-7}$-10$^{-6}$ at -1V and an ideality of 1.3-1.4 at 0.2V. This results in a two order of magnitude reduction in reverse leakage current at -1V as compared to the dry etched control.

Table 4-2. List of conditions in anneal temperature dependence study.

<table>
<thead>
<tr>
<th>Sample Name</th>
<th>Anneal Prior to S/D Deposition</th>
<th>Post S/D Anneal</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 min 350C RTA (before S/D)</td>
<td>1 minute RTA at 350°C in N$_2$ environment</td>
<td>None</td>
</tr>
<tr>
<td>5 min 350C RTA</td>
<td>1 minute RTA at 350°C in N$_2$ environment</td>
<td>4 minute RTA at 400°C in N$_2$ environment</td>
</tr>
<tr>
<td>10 min 350C RTA</td>
<td>1 minute RTA at 350°C in N$_2$ environment</td>
<td>9 minute RTA at 450°C in N$_2$ environment</td>
</tr>
<tr>
<td>20 min 350C RTA</td>
<td>1 minute RTA at 350°C in N$_2$ environment</td>
<td>19 minute RTA at 490°C in N$_2$ environment</td>
</tr>
<tr>
<td>20 min 350C RTA (before S/D)</td>
<td>20 minute RTA at 350°C in N$_2$ environment</td>
<td>None</td>
</tr>
<tr>
<td>40 min 350C RTA (before S/D)</td>
<td>40 minute RTA at 350°C in N$_2$ environment</td>
<td>None</td>
</tr>
</tbody>
</table>
Due to the similarity in response of the different annealing conditions, temperature dependent measurements are required to differentiate the mechanisms that contribute to the non-ideal current in these junctions. Samples were placed into a LakeShore TTP6 and first measured under atmospheric conditions. The measurement was repeated after the chamber was pumped down to $10^{-6}$ Torr to remove moisture from the chamber for repeatable low temperature measurements. Figure 4-9 compares I-V plots of each device collected before and after the system was evacuated. When the devices were placed under vacuum, the I-V properties of all devices annealed at 400°C or higher changed dramatically. For the 350°C annealed case (Figure 4-9a), the response in atmosphere and vacuum are nearly identical. However, in the 400°C (Figure 4-9b), 450°C (Figure 4-9c) and 490°C (Figure 4-9d) annealed cases, when placed under vacuum, the reverse leakage increases by nearly two orders of magnitude (4 orders in the 490°C case), and there is a noticeable degradation in the ideality factor. When the device is returned to atmosphere, the response returns to its initial behavior. Due to this unstable electrical behavior under vacuum, low temperature measurements cannot be taken on these samples.
The source of the variation between measurements taken in vacuum and under atmospheric conditions can most likely be attributed to the presence of As vacancies at the surface that occur due to selective outgassing of As at temperatures >300°C. Under atmospheric conditions, moisture from the air adsorbs onto the surface and passivates the trap states, minimizing surface leakage. However, when placed under vacuum, the moisture is removed from the surface, and the As vacancies are now unpassivated trap states that contribute to an increased leakage current. Increased trap state density will lead to enhanced SRH generation and TAT tunneling currents, increasing the magnitude of the reverse bias leakage current. Moisture passivation has been seen in InGaAs quantum dots, where increased humidity showed a reduction in sheet resistance. The
improved conductivity was attributed to moisture passivating surface trap states to improve carrier transport. As such, without a surface passivation layer or arsenic back pressure during annealing, temperatures above 350ºC will result in selective outgassing of As at the surface, resulting in electrical properties that are highly dependent on the surface.

![I-V curve graph](image)

Figure 4-10. Typical I-V curve for 350ºC annealed sample with varying P/A ratio.

To further analyze the effect of the annealing conditions on the non-ideal current, mesa devices with a nearly constant aspect ratio, but three different perimeter-to-area (P/A) ratios were fabricated. The devices described previously had the smallest P/A ratio of 312.5 cm⁻¹. Additional P/A ratios of 1367 cm⁻¹ and 5000 cm⁻¹ were achieved by fabricating mesas with dimensions 18µm × 78µm and 5µm × 20µm, respectively. A typical I-V curve for 350ºC annealed devices at varying P/A ratios taken at room temperature is shown in Figure 4-10. In the forward bias, it is assumed that there are only two mechanisms that contribute to the current: diffusion current with ideality factor of one and SRH recombination current with ideality factor of two. Therefore, the junction current can be expressed as:
where $J_{o1}$ is the saturation current density of the diffusion current, $J_{o2}$ is the saturation current density of the SRH recombination current, $k$ is Boltzmann’s constant, $T$ is measurement temperature, $q$ is the charge of an electron and $V$ is the applied bias. By fitting this equation to the experimental data for each anneal temperature and P/A ratio, values of $J_{o1}$ and $J_{o2}$ can be calculated. All measurements were taken at room temperature, so $q/kT$ is a constant value. $J_{o1}$ and $J_{o2}$ can be fit to each curve using the non-linear curve fit function in Origin 8.0. A representative I-V curve for each anneal temperature at all three P/A ratios is fit from 0V to 1V to determine saturation current densities. The diffusion (Figure 4-11a) and recombination (Figure 4-11b) saturation current densities are then plotted versus P/A ratio for each of the anneal conditions. For all conditions other than the 350ºC anneal, the diffusion saturation current shows little variation with P/A ratio. This suggests the diffusion current is a primarily bulk component as it does not increase with increasing surface area. However, the 350ºC annealed case shows a variation in diffusion current with P/A ratio, suggesting that there is a surface diffusion current component present as indicated by the increase in diffusion saturation current with increasing surface area.

The recombination current shows minimal P/A dependence in the wet etched control and 350ºC annealed sample suggesting a weak surface dependence to this current. This suggests that there is a lower surface trap state density resulting in a decreased surface dependence in recombination current. However, at anneal temperatures of 400ºC and above, there is a larger P/A dependence. This agrees with the vacuum dependent current variation shown earlier, suggesting that higher temperature anneals outgas surface elements leaving vacancies as trap states. These trap states act as recombination centers at the surface of the device. Thus, devices with larger surface area have a larger contribution from recombination current.
The diffusion saturation current is three orders of magnitude smaller than the recombination saturation current. From equation 4-3 it can be seen that at low forward bias, recombination current will dominate, but at high forward bias diffusion current will dominate. To demonstrate this, the cross-over voltage from recombination dominated to diffusion dominated current was calculated for each condition as a function of P/A. This was done using equation 4-3 and applying the saturation currents calculated from fitting of the I-V curves. By applying these constants, the voltage at which $J_{o1}(e^{qV/kT} - 1) = J_{o2}(e^{qV/2kT} - 1)$ can be determine for each condition.

The results are plotted below in Figure 4-11c. From this plot it can be seen that the cross-over voltage increases across all conditions with increasing P/A ratio. As the P/A ratio increases, the devices have more surface area. Recombination current has been shown in other studies to be a predominantly surface current mechanism, as such with increasing surface area there will be an increase in the recombination current component. This in turn increases the voltage at which a cross-over to diffusion dominated current occurs. The higher temperature anneals (400ºC and above) have a more significant change in cross-over voltage with increasing P/A. This further suggests an increased surface trap state density in the higher temperature anneals leads to a more significant contribution from the SRH recombination current. As mentioned before, outgassing of surface elements from higher temperature anneals will lead to increased surface trap states.
To compare the surface and bulk current contributions, the current in the device can be divided into two components, bulk and perimeter. These two current components can be expressed with the following equation to give the total current.

\[
\frac{I}{A} = J_{onB} \left( e^{\frac{qV}{n_B kT}} - 1 \right) + J_{onP} \left( e^{\frac{qV}{n_P kT}} - 1 \right) \left( \frac{P}{A} \right) 
\]  

(4-4)

where \(J_{onB}\) is the bulk saturation current, \(J_{onP}\) is the bulk perimeter current, \(n_B\) is the bulk ideality, \(n_P\) is the perimeter ideality, \(P\) is the perimeter of the device and \(A\) is the area of the device. By evaluating this equation over small step voltages to solve a linear system of equations as described in Dodd et al.\(^{36}\) these unknowns can be evaluated. Using this approach, \(J_{onP}\) (Figure 4-12a) and \(J_{onB}\) (Figure 4-12b) were calculated and plotted versus voltage for each condition. From these plots it
can be seen that for the wet etched control and the 350°C annealed samples the $J_{onB}$ is approximately two orders of magnitude larger than $J_{onP}$ in the low bias regime (0-0.4V). At 0.25V, the wet etched control has a $J_{onB}$ of $1.0 \times 10^{-6}$ and $J_{onP}$ of $8.8 \times 10^{-9}$, the 350°C annealed sample has a $J_{onB}$ of $2.8 \times 10^{-6}$ and $J_{onP}$ of $1.7 \times 10^{-9}$ at 0.25V. From this it can be seen that bulk diffusion current dominates in these two samples. By comparison for the 400°C annealed and above samples, $J_{onB}$ is undefined in the low bias regime, and perimeter recombination current dominates. This is further seen in Figure 4-12c which plots $n_P$ for all conditions. Annealing temperatures of 400°C and above have perimeter ideality factors in the range of 1.8-2, close to the ideality value of 2 that would be expected for recombination current dominated devices. This agrees with the plots shown in Figure 4-11b, suggesting a recombination dominated current at the surface of the devices, as seen by increasing recombination current with increasing surface area. The wet etched control has a lower perimeter ideality factor of 1.5 at 0.2V, suggesting a contribution from recombination current and diffusion current within the device perimeter. This matches with Figure 4-11, where the wet etched control showed nearly no change in diffusion or recombination current with changing P/A. Lastly, the 350°C annealed sample has an even lower perimeter ideality of 1.4 at 0.2V due to an enhanced diffusion current component with increasing P/A ratio. This further confirms that higher temperature anneals degrade the device perimeter current by creating a larger contribution from recombination current due to generation of surface trap states. From this analysis, 350°C is the maximum temperature that can be used without elemental outgassing, resulting in increased surface leakage currents. If higher temperature anneals are to be explored, surface passivation or an arsenic atmosphere must be used to prevent outgassing.
Figure 4-12. (a) \(J_{onP}\), (b) \(J_{onB}\) and (c) \(n_P\) plotted versus voltage for each of the anneal conditions.

4.5 Summary

By analyzing large-area In\(_{0.53}\)Ga\(_{0.47}\)As mesa p\(^+\)-i-n\(^+\) tunnel junctions fabricated on a InP growth substrate, the mechanism and extent of dry-etch induced damage can be determined. By removing 180nm from the sidewall of the etched mesa, it was determined that the dry etch damage extended greater than 180nm into the material. Additionally, through low temperature measurements, it was determined that the reverse leakage current in the dry etched sample is dominated by trap-assisted tunneling (TAT). By annealing the sample for 20 minutes at 350°C in a N\(_2\) environment, the TAT current component can be mitigated, allowing for the onset of band-to-band tunneling current. Analysis of different anneal temperatures shows that annealing at a temperature of 400°C and above results in outgassing of arsenic, increasing the surface state
density. This was determined by comparing atmosphere measurements to high vacuum measurements. The different annealing temperatures were further analyzing by comparing devices of varying perimeter-to-area ratios. Analysis of these devices showed an increased surface recombination current and increased perimeter current ideality in anneals above 400°C, demonstrating an increase in non-ideal surface currents in these high temperature anneals.

4.6 Bibliography


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Chapter 5

Single Particle Electrical Measurements of Solution-Synthesized GeSe Nanobelts by Use of Electric-Field Assisted Assembly

5.1 Introduction

As discussed in chapter one, colloidal synthesis of inorganic nanoparticles is a growing field. Recent work has shown the ability to grow a number electronically interesting semiconductor materials. However, the field lacks a robust strategy for single particle electrical measurements. Electric-field assisted assembly offers a fast and easy platform to electrically characterize single particles, allowing for evaluation of these materials systems for device applications. By deterministically placing these particles onto silicon (Si) substrates as described in chapter 2, top-down fabrication can be implemented to contact these particles for property characterization.

In this dissertation research, single particle measurements of GeSe nanobelts were completed through electric-field assisted assembly and subsequent top-down fabrication. GeSe has shown potential as an alternative material for photovoltaic devices. GeSe has a band gap in the solar spectrum (1.1-1.2eV) and contains less toxic elements than some of the other earth-abundant materials often used in nanoparticle solar cells. Additionally, there is interest in GeSe for use in resistive-switching materials and thermoelectrics. However, electric properties of GeSe nanostructures have not been extensively studied. In particular, single-particle electrical measurements of GeSe nanostructures have been limited by a lack of a robust characterization platform.

This chapter first discusses the synthesis of GeSe nanobelts through a colloidal one-pot synthesis process, as completed by Dr. Dimitri D. Vaughn II and Du Sun in Dr. Ray Schaak’s group. Next the particles were characterized by transmission electron microscopy (TEM) that was
completed by Dr. Dimitri D. Vaughn II. The particles are then integrated by electric-field assisted assembly and contacted for 2 and 4-point electrical measurements. Comparison of 2-point and 4-point measurements allow for an approximation of contact resistance in the 2-point measurement.

5.2 Nanobelt Single Particle Measurements

Figure 5-1. Schematic of one-pot synthesis technique.© Copyright 2000 Annual Reviews Publications.

GeSe nanobelts were grown through a one-pot colloidal synthesis technique. A 1M tri-n-octophosphine (TOP)-Se solution was prepared by mixing 10mMol of selenium powder in 10mL of TOP. Next, a solution of 0.10mmol GeI₄ was mixed with 10mL oleylamine and 0.75mL of oleic acid. The GeI₄ solution was added to a 100mL 3-neck round-bottom flask fitted with a condenser, thermometer and rubber septum (Figure 5-1). 0.1mL of the 1M TOP-Se solution was added, and the solution was stirred under vacuum at 120°C for ~5-10 minutes. It was then cooled to 80°C and purged with argon, next 1mL hexamethyldisilazane was added. The reaction vessel was heated to 320°C at 10°C/min; upon reaching 320°C, an additional 1mL of the TOP-Se solution was added and the solution was aged overnight (~12h). The solution was rapidly cooled by removing the heat source, and particles were precipitated out by adding 30mL of a 3:1:1 acetone/hexane/toluene
mixture. The suspension was centrifuged and rinsed 3 times in a 1:1 toluene/ethanol mixture.\textsuperscript{16} Lastly, the particles were suspended in 1.5mL of toluene.

![Figure 5-2. (a,b) TEM showing an amorphous shell surrounding a crystalline core (c) FESEM of GeSe nanobelts assembled onto a silicon substrate.\textsuperscript{16} Copyright 2012 American Chemical Society.](image)

To observe the crystal structure of the particles, a solution of cleaned nanobelts in toluene was drop-cast onto a Formar coated copper TEM grid. The nanobelts were then examined using a JEOL 1200 EX II TEM. From TEM the nanobelts had widths of 77nm $\pm$ 18nm and lengths of 1-25µm. The nanobelts have a crystalline core surrounded by an amorphous coating (Figure 5-2a-b), most likely germanium oxide as this has been known to passivate Ge based nanostructures\textsuperscript{17-18}

The nanobelts were then assembled onto a lightly doped p-type Si substrate coated with a 1.2µm thick thermally grown oxide isolation layer. Interdigitated Ti/Au assembly electrodes were fabricated (details in appendix) with a 5µm gap separating the two oppositely biased electrodes. A 10nm Al\textsubscript{2}O\textsubscript{3}/120nm SiO\textsubscript{2}/10nm Al\textsubscript{2}O\textsubscript{3} dielectric isolation layer was deposited on top of the metal electrodes with a combination of Atomic Layer Deposition (ALD) and Plasma-Enhanced Chemical Vapor Deposition (PECVD).\textsuperscript{16} This thick dielectric layer was used to electrically isolate the assembly electrodes from the assembled particle. The particles were assembled with electric-field assisted assembly by applying the toluene suspension of GeSe nanobelts to electrodes biased at
30\text{V}_{pp}, 100\text{kHz}.^{16} \text{Figure 5-2c} shows assembled GeSe nanobelts on this structure after the solution evaporated. Due to the large dispersion of nanobelt lengths, the optimized assembly structure from Chapter 2, which included lithographic depressions for particle placement, was not used. In this case, the as-grown particle suspension was diluted 1:100 in toluene, to achieve an approximate spacing between adjacent particles of 20\text{µm}.

Using electron-beam lithography with a PMMA/MMA resist stack, 15\text{µm} long 4-point contact lines were patterned with their position centered at the electrode gap. The 4-point contact lines were separated by a distance of 40\text{µm} along the electrode gap, relying on the density limited spacing to achieve single particle measurements. Each contact line was 1\text{µm} wide and separated by a 1.5\text{µm} gap. Immediately prior to metal deposition, the substrate was dipped in DI water to remove the native germanium oxide on the surface. 120\text{nm Ti/ 30nm Au} metal contacts were deposited using thermal evaporation. The devices were then optically inspected to find single nanowire devices. In order to optimize the device yield, an electrode structure as described in chapter 2 can be designed for the most commonly occurring dimensions of this poly-disperse suspension of
particles. This would allow for more precise spatial alignment of the particles, permitting a higher single-particle device yield.

An FESEM image of typical device is shown in Figure 5-3a. The nanobelt is contacted with 4 probes to allow for both 2-pt and 4-pt measurements. Prior to measurement, the nanobelt was purged in dry nitrogen for 24 hours to minimize the moisture adsorbed onto the surface, improving stability and reproducibility of the measurement. All measurements were taken using an Agilent 4156B precision semiconductor parameter analyzer and a pair of Keithley 6514 system electrometers. Two point measurements were taken by sweeping a voltage from -300mV to 300mV in 10mV increments between probes 2 and 3 of the 4-pt structure. 4-pt measurements were taken by forcing a current through probes 1 and 4, and measuring the differential voltage between probes 2 and 3 with electrometers. Each measurement was held for 100s to ensure that the differential voltage had time to stabilize. The stabilized voltage was averaged for each applied current value to plot a 4-pt I-V. By separating the applied current and measured voltage, the contact resistance can be isolated from the nanowire resistance.

A room temperature 2-pt and 4-pt J-V plot of the nanobelt in Figure 5-3a is shown in Figure 5-3b. The effect of surface accumulation or depletion due to surface charge that may be present on these nanobelts is neglected, and it is assumed that current flows uniformly through the nanobelt cross-section. Therefore, the current density is calculated by dividing the current by the nanobelt cross-sectional area. The nanobelt width is determined by FESEM and the thickness is determined by atomic force microscopy (AFM) (Figure 5-4). The nanobelt shown in Figure 5-3 is determined to be 196nm wide and 35nm thick. As seen from Figure 5-3b, the nanobelt 2-pt test structure exhibits ohmic (linear) J-V behavior, with a current density of 1A/cm² at 250mV. This corresponds to a total resistance of 4 x 10⁹ Ω, for a 1.9µm long segment. The 4-pt measurement had a 125mA/cm² current density at 9.6mV, corresponding to a resistance of approximately 1 x 10⁹ Ω, indicating a contact resistance of ~ 1.5 x 10⁹ Ω in the 2-pt measurement. From the 4-pt resistance
the nanobelt resistivity is calculated using $\rho = \frac{R_{4-pt} A}{L}$, where $A$ is the cross-sectional area of the particle and $L$ is the length of the measured segment, giving a value of approximately $360 \Omega \text{cm}$. This corresponds well with previously measured single-crystal GeSe samples synthesized by the Bridgman and sublimation techniques, showing values in the range of $0.9$ to $10^4 \Omega \text{cm}$ at room temperature in atmosphere.\textsuperscript{20-22} The test structure used in this work did not allow for gated measurements of the nanobelts, thus GeSe doping type could not be determined. Through use of an optimized substrate choice such as that used in chapter 3, back-gated measurements can be completed to further analyze the nanobelts.

Figure 5-4. (a) AFM Scan of contacted GeSe nanobelt (b) 2D line scan of region indicated by white line in (a).

5.3 Summary

Through electric-field assisted assembly, GeSe nanobelts were integrated onto a Si substrate and measured with 2-pt and 4-pt measurements. The particles exhibited similar resistivity to bulk single crystal GeSe films, suggesting that these materials should be suitable for electronic applications. This technique offers a quick and easy platform to characterize solution-synthesized
particles electronically. With further optimization of the assembly structure, high yield integration of solution-synthesized particle devices can be achieved.

5.4 Bibliography


Chapter 6

Summary and Future Work

6.1 Summary

In this dissertation research, directed electric-field assisted assembly was used to heterogeneously integrate new materials onto alternative substrates such as silicon (Si). Directed assembly offers advantages over other heterogeneous integration strategies because it is a fast, versatile, low temperature strategy\(^1\) that efficiently places material into tightly controlled positions.\(^2\) Directed assembly can overcome the challenges of mismatch in lattice constant and coefficient of thermal expansion\(^3\) existing for direct epitaxial growth. Additionally, this technique does not require the use of a crystalline substrate,\(^3\) expanding its application base.

Directed assembly allows for integration of thin sheets of materials that can be accurately and reproducibly placed both at the device layer and in the interconnect layers. This allows multiple material systems to be stacked into a 3D chip to integrate different device functionalities, including radio frequency (RF), sensors, and optical devices, onto a single chip. Additionally, it offers an approach to stack transistors vertically as an alternative to traditional scaling.\(^5\) With this integration, the interconnect lines between devices can shortened, reducing the interconnect delay between devices\(^6\) and improving circuit performance.\(^7\) This becomes even more important with continued scaling of complementary metal oxide semiconductor (CMOS) technology because as the metal pitch is scaled with smaller technology nodes, the RC delay between interconnects increases.\(^6\) As such, there is an increasing need to minimize the contact length between devices to improve circuit performance. For these reasons there is a rapidly growing need for 3D integration\(^8,9\) and directed assembly offers a novel approach of implementing this technology.
In chapter 2, micron-sized $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ sheets were assembled into predefined locations on a Si substrate with sub-micron registration accuracy. Through a combined experiment and theory, the assembly process was studied. First, the dielectrophoretic (DEP) force induced on the particles in non-uniform electric fields was modeled to examine the effects of solution conductivity on the frequency dependence of the force. It was shown that for the solution conductivity range examined ($10^{-7} - 10^{-5}$ S/cm), the DEP force increased with increasing frequency; this effect is magnified as the solution conductivity increased. The model was then modified to examine the frequency dependence of the short-range forces acting on a sheet aligned to the electrode edge. The model was compared to experimental results, and showed strong agreement between the two. Modeling of the charge distribution within the assembled sheet demonstrated that the induced charge led to electric-field interactions between assembled sheets that resulted in the formation of uniformly spaced sheet arrays along the guiding electrode edge.

Directed electric-field assisted assembly was demonstrated with lithographically defined features patterned into a dielectric layer. Through modeling of the near surface forces on an assembled sheet, a preferred alignment position was calculated. Experimentally measured assembly demonstrated reproducible sub-micron alignment accuracy, with mean position in both x and y dimensions matching the model. The model was then expanded to examine the electrostatic interactions between two sheets on the electrode edge, and it verified the self-limiting assembly behavior observed experimentally. In the future, this model can be used to predict assembly behavior of new materials and devices by simply modifying the particle geometry and electrical properties.

In chapter 3, $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ fin tunnel field effect transistors (TFETs) and metal-oxide-semiconductor field effect transistors (MOSFETs) were integrated onto a Si substrate through a combination of top-down fabrication and bottom-up assembly. Starting with an epitaxial grown layer structure, 10µm long, 620nm wide and 200-100nm thick sheets of $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ with $p^{+}$-$i$-$n^{+}$
and n*-i-n* doped junctions were patterned and released into solution. The sheets were assembled onto a Si substrate with the vertically grown junctions aligned laterally along the substrate. The assembled In$_{0.53}$Ga$_{0.47}$As sheets were patterned and etched into dense arrays of 620nm long, 50nm wide and 200-100nm tall fins. Lastly, source/drain contacts are applied through electron-beam lithography and metal evaporation. The resulting p*-i-n* junctions were characterized immediately following the integration process, and showed nonrectifying behavior. By implementing a 350°C anneal in N$_2$ for 20 minutes, the junction properties were improved and became rectifying. However, scaling of the starting sheet thickness from 200nm to 100nm results in junctions that cannot be recovered through annealing.

Both p*-i-n* and n*-i-n* doped fins were further processed by adding a dielectric and metal gate stack to form fin TFETs and MOSFETs with a 100nm channel length and a 50nm channel width. TFET device performance was hindered by a high density of trap states induced during dry etching, demonstrating a subthreshold slope of 660mV/decade and an on/off ratio of 160 at $V_{ds}$=-100mV. In contrast to TFET devices, Fin MOSFETs are majority carrier devices that are much less susceptible to the presence of trap states. As such, the Fin MOSFETs showed an improved device performance as compared to the Fin TFET devices, with a subthreshold slope of 280mV/decade and an on/off ratio of $\sim$10$^3$ for $V_{ds} = 100$mV. However, these devices exhibited degradation in performance at higher drain bias due to the use of heavily doped source/drain regions and lightly doped channel. This design resulted in a wide depletion region at the source/channel and drain/channel junctions, reducing gate control at high bias. Technology computer aided design (TCAD) modeling showed matching subthreshold slope at drain bias of 100mV and 200mV. Additionally, this model predicted that increasing the channel doping density would improve the high drain bias behavior by reducing the depletion width of the source/channel and drain/channel junctions.
In chapter 4, 80µm × 320µm In_{0.53}Ga_{0.47}As mesa p’-i-n’ tunnel junctions were fabricated directly on the lattice-matched InP growth substrate to examine the relative trap state density generated from dry etch damage. Electrical measurements are extremely sensitive to trap states and show changes in behavior to defect densities that are not detectable by other characterization techniques.\textsuperscript{10-11} The reverse bias current and forward bias ideality of dry etched samples were directly compared to a wet etched control sample that did not have dry etch induced defects. The dry etched sample showed a strong trap-assisted tunneling (TAT) component, an undesirable non-ideal leakage current.\textsuperscript{12-13} By removing material using a wet etch, the dry etch damage is shown to penetrate over 180nm into the bulk region of the device. Annealing the sample at 350ºC for 20 minutes in a N\textsubscript{2} background largely recovered the junction performance and eliminate the large TAT current. Studies of anneal temperature demonstrated that 350ºC for 20 minutes had the lowest perimeter ideality and most stable I-V under vacuum of the conditions examined.

In chapter 5, solution-synthesized GeSe nanobelts were characterized through single particle electrical measurements. GeSe has shown potential as a non-toxic material for solar cells due to its band gap in the solar spectrum (1.1-1.2eV) and use of earth abundant elements.\textsuperscript{14-17} Additionally, GeSe has been used as a thermoelectric\textsuperscript{18} and resistive switching\textsuperscript{19} material. However, electrical properties of GeSe nanostructures have not been studied extensively\textsuperscript{20-21} largely because there is a lack of a robust single particle electrical characterization platform.

In this work, GeSe nanobelts were assembled onto Si substrates by directed electric-field assisted assembly. Once assembled, 2-point and 4-point electrical test structures were formed using the nanobelts. The 2-point and 4-point electrical measurements were carried out in an N\textsubscript{2} background. From the measurements, the nanobelts were determined to have a resistivity 360Ω-cm, which is comparable to bulk values reported in literature.\textsuperscript{22-24} From the 2-point measurement, contact resistance was determined to be \( \sim 1.5 \times 10^9 \, \Omega \). This offers a standard platform for measuring
solution-synthesized particles, something significantly lacking in this field. Single particle measurements allow for evaluation of particles for future device applications.

### 6.2 Future Work

In order to improve the capability of this heterogeneous integration strategy, several modifications can be implemented to the assembly process. Assembly yield can be enhanced through use of a fluid cell based assembly approach. This approach has demonstrated extremely high single-particle assembly yields, and will allow for a uniform and reproducible density of particles to be applied to the surface over large areas. Additionally, a fluid cell based approach can be implemented to overcome the limitations of particle movement due to meniscus fluid currents by optimizing the drying procedure, allowing for more precise alignment of particles.

![Figure 6-1](image)

Figure 6-1. (a) A high density of particles applied to completely fill all designed wells. (b) A clean solution is used to rinse away undesired particles (not within wells). (c) The solution is replaced with low surface tension solvent to minimize meniscus current during drying.
In such an approach, the assembly process would be broken down into three steps: assembly, rinse and dry. Starting with an unbiased electrode structure containing lithographically define wells as described in section 2.5, a uniform suspension of particles can be applied to the substrate through a fluid cell. Once the particles are uniformly dispersed across the guiding electrode structure, the bias will be applied, and the particles will be aligned into wells. If bias is applied when the particle suspension is dispersed, there will a depletion of particles at the source of the flow leading to a non-uniform effective particle density across the substrate. The electrostatic force holding the particle to the surface will be much larger within the well than outside of it. In this case, the misaligned particles outside of the wells can be preferentially removed with proper tuning of fluid velocity. The solution must flow perpendicular to the electrode edge because flow parallel to the electrode edge will force particles along the electrode edge and into already occupied wells. Lastly, the solution can be replaced with a low surface tension solution for drying. In this approach, super-critical drying can be applied with a flow cell designed to handle high pressure. The assembly solution can then be replaced with liquid carbon dioxide and sublimated while the bias is maintained. This will prevent shifting of the particles during drying and allow for precise and reproducible placement of particles within the wells. This offers an approach to achieve high yields over large-area substrates.

Chapter 3 and 4 emphasized the need to alleviate dry etch damage in nanoscale compound semiconductor devices. There are two possible approaches to solve this problem. One approach is to modify the etch process to minimize the damage induced from etching. Work has shown that H\textsubscript{2} can result in deeper dry etch damage due to its small atomic mass and radius.\textsuperscript{28-29} Removal of H\textsubscript{2} from the dry etch has been shown to reduce dry etch damage in compound semiconductors. Additionally, work by Foad et al. shows that including noble gases (such as Ar used in this work) in the plasma increases damage depth.\textsuperscript{30} Noble gases add an increased physical component to etching, increasing the etch anisotropy. Use of a more chemical (less physical) etch process has
shown to reduce the extent damage from dry etching.\textsuperscript{30} Therefore, striking the optimal balance between low damage and high etch anisotropy is necessary to address this challenge. A second approach is to optimize the post-etch processing. As shown from chapter 4, anneals above 350\textdegree C in an N\textsubscript{2} ambient result in unstable surfaces from outgassing of arsenic. To overcome this problem, annealing can be either completed in an As\textsubscript{2} ambient or surface passivation can be used to prevent outgassing from the surface. Either of these approaches can allow for higher temperature anneals to be evaluated as a replacement to the 350\textdegree C anneal used in this work.

By optimizing the design of the MOSFET layer structure, the short channel effects seen in this research can be minimized. By reducing the doping density in the source/drain contacts and increasing the channel doping density, the depletion width of the source/channel and drain/channel junctions will be reduced. Doing so will minimize the degradation in device performance at high drain bias, by improving electrostatic control of the channel.\textsuperscript{31}

In chapter 5, GeSe nanobelts were measured with 2-pt and 4-pt measurements as a first step in evaluation of these particles. By using an optimized assembly device structure, as described in section 2.5, back-gated measurements can be completed to determine the particle dopant type. Using this same approach many other types of solution-synthesized particles\textsuperscript{32-36} can be characterized. With high yield single particle devices, large batch statistical analysis can be used to determine the variability in properties across particles. This is essential for evaluating solution-synthesized particles for device applications as reproducibility is paramount to any viable device.

6.3 Bibliography


Appendices

Appendix A

Assembly Electrode Fabrication and Assembly Setup

A.1 Assembly Electrode Fabrication

1. Start with 120nm Si$_3$N$_4$ LPCVD deposited on a double-sided polished n-type Si wafer

2. Spin resist for double layer optical lithography lift-off
   a. Acetone/IPA rinse, N$_2$ dry, bake at 110°C for 1 min
   b. Spin 4000 rpm for 45s with MicroChem PMGI SF6S, bake at 190°C for 5 mins
   c. Spin 4000 rpm for 45s with Shipley SPR3012, bake at 95°C for 1 min

3. Exposure pattern with GCA 8000 stepper
   a. Jobfile “SLBELEC” pass 1, exposure 0.5s, focus 0
   b. Use mask labelled “sml341”

4. Develop
   a. 1 minute in Microposit MF-CD-26 developer, agitate at 30s, DI rinse, N$_2$ dry
   b. 620s OAI Deep UV flood exposure
   c. 1 min MicroChem 101A developer, DI rinse, blow dry
   d. 1 min TePla M4L descum (680mTorr, 150sccm O$_2$, 50sccm He, 200W)

5. Deposit 10nm Ti/30nm Au with Kurt J. Lesker Lab-18 e-beam evaporator
   a. Lower substrate temperature to 5°C to prevent resist modification
6. Lift off 1 hour in Microposit Remover 1165 heated to 60°C, followed by 30 additional minutes in clean solution

7. Deposit 10nm HfO$_2$ film in Kurt J. Lesker 150 LX ALD
   a. Condition ALD chamber by depositing 10nm HfO$_2$
      i. 300°C, 0.76 Torr, TDMAH pulse 0.1s/12s delay, H$_2$O pulse 0.03s/12s delay, 106 cycles
   b. Acetone/IPA rinse, dry and load into chamber
   c. Deposit 10nm HfO$_2$, same recipe as above

8. Spin e-beam resist for wells
   a. Acetone/IPA rinse, N$_2$ dry, bake 110°C for 1 min
   b. Spin 4000 rpm for 45s with MicroChem PMGI SF11, bake 190°C for 5 mins
   c. Spin 3000 rpm for 50s with MicroChem PMMA A3, bake 180°C for 3 mins
   d. 10nm thermal Au evaporation in Kurt J. Lesker Lab-18

9. Pattern with Vistec EBPG5200 e-beam
   a. Job File “Wells”, 1030 μC/cm$^2$ dose
   b. 20s Transene Au TFA etchant, DI rinse, N$_2$ dry
   c. 2 min MicroChem Methyl Isobutyl Ketone (MIBK):IPA (1:3), 20s IPA, N$_2$ dry
   d. 2 min MicroChem 101A developer, DI rinse, N$_2$ dry
   e. 15s TePla M4L descum (100W, 150sccm O$_2$, 50sccm He, 400mTorr)
   f. Acetone soak for 5 mins to remove MicroChem PMMA EL11 followed by IPA rinse and dry
A.2 $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ p$^+$-i-n$^+$/n$^+$-i-n$^+$ sheet fabrication

1. Start with MBE grown 620nm $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ with a p$^+$-i-n$^+$ or n$^+$-i-n$^+$ doping profile on InP commercially grown by IQE.

2. Deposit ~300nm PECVD SiO$_2$ using an AMAT P-5000 PECVD Cluster Tool with “SIO2 WRDII” recipe for 142s.
   a. 300W, 300°C, 1400sccm N$_2$, 840 sccm N$_2$O, 20 sccm SiH$_4$

3. Following deposition, 1min TePla M4L descum to remove any organic residue for resist adhesion.
   a. 100W, 150sccm O$_2$, 50sccm He, 400mTorr

   a. Acetone/IPA rinse, N$_2$ blow dry, bake at 110°C for 1 min.
   b. 30s dip in DisChem Surpass 3000 adhesion promoter, 30s dip in DI water, N$_2$ blow dry.
   c. Spin 5000 rpm for 40s with MicroChem Ma-N 2403, bake at 90°C for 1 min.
   d. Deposit 10nm thermal Au with Kurt J. Lesker Lab-18 evaporator.

5. Pattern 100nm x 10μm sheets using Vistec EBPG5200 e-beam lithography.
   a. Job file name “LA_PIN”, 115μC/cm$^2$ dose, 5nA beam.
   b. 20s Transene Au TFA etchant dip, DI water rinse, N$_2$ blow dry.
   c. 1 min Microposit MF-CD-26 developer, DI rinse, N$_2$ blow dry.
   d. 5 mins M4L descum (100W, 150sccm O$_2$, 50sccm He, 400mTorr).

6. Oxide Etch.
   a. Versalock ICP-RIE recipe “SiO$_2$ w ZEP” for 115s.
      i. 900W ICP, 50W Substrate, 5°C substrate cooling, 40sccm CF$_4$, 5 mTorr.

a. Versalock ICP-RIE recipe “DCASH (Mayer)” for 30s

i. 100mTorr, RF1 25W, RF2 300W, O₂ 40sccm

8. Send sample to Dr. Ning Cao at UCSB

a. Etch using PlasmaTherm Uniaxis VLR (ICP#3) for 85s

i. 1.4mTorr, 125W substrate bias (157V), 800W ICP, 7.4sccm Cl₂, 11.6sccm H₂, 2sccm Ar. Substrate heated to 200°C

9. 20 minute Allwin21 AG610 RTA system at 350°C in N₂ ambient

a. Allow 5 minutes in N₂ for desorption of moisture on substrate

b. 60s ramp time from room temperature to 350°C

10. Release sheets with selective HCl wet etch

a. 2 minute 10:1 BOE to completely remove oxide hard mask

b. Mix (1:1) solution by volume of HCl:Ethanol

c. Add sample to solution for 70s

d. Place sample gently in clean ethanol solution for 5 minutes (repeat 3 times)

e. Directly place sample into solution of IPA or DI water in a centrifuge tube

f. Sonicate for 5 seconds and ensure substrate is clear of sheets through visual inspection

g. Remove substrate and allow to air dry

A.3 Assembly experimental setup

1. Contact electrode structure with source and ground probes

2. Blow sample with N₂ to remove dust from surface

3. Apply 5μL of solution uniformly across the entire surface of electrode using a pipette.
a. Solution is applied prior to application of bias to allow a uniform distribution of particles to form, unperturbed by applied bias.

4. Apply an AC bias $10V_{pp}$, 500Hz-1MHz. Optimal assembly conditions are $10V_{pp}$, 1MHz (conditions used in chapter 3).

5. Particles will assemble to regions of high electric field gradient, wait for solution to evaporate for a completely dry substrate.

6. Once solution is dried, remove bias and lift probes.

7. For high yield assembly used in chapter 3, this process is repeated for a total of three applications as seen in Figure A-1. This accounts for possible non-uniformity throughout the application of solution.
   a. The first application is applied left to right.
   b. The second application is applied right to left.
   c. The final application is applied entirely to the center of the die and allowed to flow outward across the die.

Figure A-1. Schematic of solution application process.
Appendix B

Fin TFET and MOSFET Fabrication

B.1 Fin diode fabrication

1. Starting with assembled sheets on substrate described in A.1, remove wells with 30 minutes in Dimethylacetamide (DMAc) heated to 60°C, DI rinse, N2 dry
2. Deposit 90nm SiO$_2$ with AMAT P-5000 PECVD Cluster Tool for 41s “SiO2 WRDII”
   a. 300W, 300°C, 1400sccm N$_2$, 840 sccm N$_2$O, 20 sccm SiH$_4$
   b. 10 minute clean and 2 minute condition prior to deposition
3. Pattern NW etch lines
   a. Descum substrate in TePla M4L to remove organic residue from mounting sample
      i. 30s M4L descum (100W, 150sccm O$_2$, 50sccm He, 400mTorr)
   b. Spin resist for e-beam patterning
      i. Acetone/IPA rinse, N$_2$ dry, bake 110°C for 1 min
      ii. Spin 5000 rpm for 40s with ZEONREX ZEP520A, bake 180°C for 3 mins
      iii. Deposit 10nm thermal Au with Kurt J. Lesker Lab-18 evaporator
   c. Vistec EBPG5200 e-beam writing
      i. Jobfile “NW etch lines”, dose 110μC/cm$^2$, 1nA beam
      ii. 20s, Transene Au TFA etchant, DI rinse, blow dry
      iii. 3 min n-amyl acetate, 1 min (8:1) MIBK:IPA, IPA rinse, N$_2$ dry
      iv. 15s TePla M4L descum (100W, 150sccm O$_2$, 50sccm He, 400mTorr)
   d. Oxide etch
i. Versalock ICP-RIE recipe SIO2 w ZEP, for 34s
   1. 900W ICP, 50W Substrate, 5°C substrate cooling, 40sccm CF$_4$, 5 mTorr

   e. Remove ZEP 520A
      i. Versalock ICP-RIE recipe DCASH, for 30s (100mTorr, RF1 25W, RF2 300W, O$_2$ 40sccm)

4. Etch into NWs at UCSB

   a. Etch using PlasmaTherm Uniaxis VLR (ICP#3) for 20s
      i. 1.4mTorr, 125W substrate bias (157V), 800W ICP, 7.4sccm Cl$_2$,
         11.6sccm H$_2$, 2sccm Ar. Substrate heated to 200°C

5. RTA Anneal

   a. Allwin21 AG610 RTA anneal at 350°C for 20 mins in N$_2$

6. Source/Drain E-beam lithography

   a. Spin Resist

   b. Vistec EBPG5200 e-beam patterning
      i. Job file “130508_NWSD”, 350μC/cm$^2$ dose
      ii. 20 Transene Au TFA etchant, DI rinse, blow dry
         iii. 1 min (1:1) MIBK:IPA, 20s IPA, blow dry
         iv. 15s M4L descum (100W, 150sccm O$_2$, 50sccm He, 400mTorr)

7. Source/Drain deposition

   a. 30s BOE 10:1 etch

   b. 30s (10:1) H$_2$O:HCl dip, DI rinse, N$_2$ dry, immediately load into Kurt J. Lesker Lab-18 evaporator

   c. Deposit 150nm Ti, 50nm Pd at 5°C, deposition broken into 50nm steps with 20 minutes waiting in between. This limits substrate heating
d. Lift off in acetone with minimum 3 hours soak time

8. Map NW positions and measure

B.2 MOS capacitor fabrication

1. Start with 620nm In\textsubscript{0.53}Ga\textsubscript{0.47}As p\textsuperscript{+}-i-n\textsuperscript{+} film on an InP substrate

2. Remove top p\textsuperscript{+} layer with 280s (20:1) citric acid etch:H\textsubscript{2}O\textsubscript{2} etch
   a. Dissolve (1:1) mass ratio anhydrous citric acid powder: DI water
      i. Allow minimum of 6 hours for solution to equilibrate at room temperature
   b. Mix citric acid solution with H\textsubscript{2}O\textsubscript{2} in 20:1 volume ratio
      i. Allow 15 minutes for heat of mixing to dissipate
   c. Add sample to solution and lightly agitate every 30s to prevent formation of bubbles on substrate.
   d. Rinse sample with DI water and blow dry

3. Deposit 1nm Al\textsubscript{2}O\textsubscript{3}/5nm HfO\textsubscript{2} gate dielectric with Kurt J. Lesker 150 LX ALD
   a. Precondition chamber with steps d-f
   b. Acetone/IPA rinse
   c. 30s (10:1) H\textsubscript{2}O:HCl, DI rinse, N\textsubscript{2} dry, immediately load into ALD
   d. Al\textsubscript{2}O\textsubscript{3} pre-pulse at 200°C (10 pulses, 12s delay time, 0.03 TMA pulse)
   e. Deposit 1nm Al\textsubscript{2}O\textsubscript{3} at 200°C (10 cycles, 12s delay time, 0.03s TMA pulse, 0.1 water pulse)
   f. Deposit 5nm HfO\textsubscript{2} at 200°C (21 cycles, 12s delay time, 0.1s TMDAH pulse, 0.1 water pulse)

4. Apply top Ti/Pd gate with a shadow mask using Kurt J. Lesker Lab-18
a. Tape sample into direct contact with shadow mask and mount onto sample holder
b. Load into evaporation system and deposit 50nm Ti/ 50nm Pd with e-beam evaporation

B.3 Gate dielectric implementation

1. Deposit 1nm Al₂O₃/5nm HfO₂ gate dielectric with Kurt J. Lesker 150LX ALD
   a. Precondition with steps d-f
   b. Acetone/IPA rinse
   c. 30s (10:1) H₂O:HCl, DI rinse, N₂ dry, immediately load into ALD
   d. Al₂O₃ pre-pulse at 200°C (10 pulses, 12s delay time, 0.03 TMA pulse)
   e. Deposit 1nm Al₂O₃ at 200°C (10 cycles, 12s delay time, 0.03s TMA pulse, 0.1 water pulse)
   f. Deposit 5nm HfO₂ at 200°C (21 cycles, 12s delay time, 0.1s TMDAH pulse, 0.1 water pulse)

2. Measure NW devices

3. Pattern gate
   a. Acetone/IPA rinse, N₂ dry, bake 110°C for 1 min
   b. Spin 4000 for 45s with MicroChem MMA EL11, bake 150°C for 3 mins
   c. Spin 4000 rpm for 45s with MicroChem PMMA A3, bake 180°C for 3 mins
   d. Deposit 10nm thermal Au with Kurt J. Lesker Lab-18
   e. Vistec EBPG5200 e-beam patterning Job file “NW_Gate”, 350μC/cm² dose, 5nA beam
   f. 20 Transene Au TFA etchant, DI rinse, blow dry
   g. 1 min (1:1) MIBK/IPA, 20s IPA, blow dry
h. 15s M4L descum (100W, 150sccm O₂, 50sccm He, 400mTorr)

4. Deposit 100nm Ti/50nm Pd with Kurt J. Lesker Lab-18 e-beam evaporation
   a. Set substrate temperature to 5°C to reduce resist reflow
   b. Deposit in 50nm deposition steps with a 20 minute delay in between to limit substrate heating

5. Lift-off in acetone
Appendix C

Large Area In$_{0.53}$Ga$_{0.47}$As Fin Diode Fabrication

1. Start with MBE grown In$_{0.53}$Ga$_{0.47}$As with a p$^+$-i-n$^+$ doping profile

2. Spin PMMA/MMA
   a. Acetone/IPA rinse, N$_2$ blow dry, bake at 110°C for 1 min
   b. Spin Hexamethyldisilazane (HMDS) at 5000 rpm for 40s, bake at 110°C for 1 min
   c. Spin MicroChem MMA EL11 at 5000 rpm for 40s, bake at 150°C for 90s
   d. Spin MicroChem PMMA A3 at 5000 rpm for 40s, bake at 180°C for 90s
   e. Deposit 10nm thermal Au with Kurt J. Lesker Lab-18

3. Pattern e-beam alignment markers with Vistec EBPG5200 using e-beam lithography
   a. Job file name “LargeArea_alignmentmarks”, 320μC/cm$^2$ dose
   b. 20s Transene Au TFA etchant dip, DI water rinse, N$_2$ blow dry
   c. 1 min MicroChem MIBK:IPA (1:1), 20s IPA, N$_2$ blow dry
   d. 15s TePla M4L descum (100W, 150sccm O$_2$, 50sccm He, 400mTorr)

4. Deposit 50nm Cr/ 50nm Pd with Kurt J. Lesker Lab-18 e-beam evaporator
   a. Liftoff in acetone overnight at room temperature
   b. Rinse with acetone/IPA and blow dry

5. Deposit ~200nm PECVD SiO$_2$ using AMAT P-5000 PECVD Cluster Tool with “SIO2 WRDII” recipe for 105s
   a. 300W, 300°C, 1400sccm N$_2$, 840 sccm N$_2$O, 20 sccm SiH$_4$

6. Following deposition, 1min TePla M4L descum to remove any organic residue to promote adhesion
   a. 100W, 150sccm O$_2$, 50sccm He, 400mTorr
7. Spin MicroChem Ma-N 2403
   a. Acetone/IPA rinse, N₂ blow dry, bake at 110°C for 1 min
   b. 30s dip in DisChem Surpass 3000, 30s dip in DI water, N₂ blow dry
   c. Spin 5000 rpm for 40s with MicroChem Ma-N 2403, bake at 90°C for 1 min
   d. Deposit 10nm thermal Au with Kurt J. Lesker Lab-18

8. Pattern mesas using e-beam lithography with Vistec EBPG5200
   a. Job file name “LargeArea_mesa”, 215μC/cm² dose
   b. 20s Transene Au TFA etchant dip, DI water rinse, N₂ blow dry
   c. 1 min Microposit MF-CD-26 developer, DI rinse, N₂ blow dry
   d. 5 mins TePla M4L descum (100W, 150sccm O₂, 50sccm He, 400mTorr)

9. Oxide Etch
   a. Versalock ICP-RIE recipe SiO₂ w ZEP for 115s
      i. 900W ICP, 50W Substrate, 5°C substrate cooling, 40sccm CF₄, 5 mTorr

10. Strip MicroChem Ma-N resist
    a. Versalock ICP-RIE recipe DCASH (Mayer) for 30s
       i. 100mTorr, RF1 25W, RF2 300W, O₂ 40sccm

11. Send sample to Ning at UCSB
    a. Etch using PlasmaTherm Uniaxis VLR (ICP#3) for 28-35s
       i. 1.4mTorr, 125W substrate bias (157V), 800W ICP, 7.4sccm Cl₂,
          11.6sccm H₂, 2sccm Ar. Substrate heated to 200°C

12. Remove 180nm from sidewall with 180s (20:1) citric acid etch:H₂O₂ etch (Optional)
    a. Dissolve (1:1) mass ratio anhydrous citric acid powder: DI water
       i. Allow minimum of 6 hours for solution to equilibrate at room temperature
    b. Mix citric acid solution with H₂O₂ in 20:1 volume ratio
i. Allow 15 minutes for heat of mixing to dissipate

c. Add sample to solution and lightly agitate every 30s to prevent formation of bubbles on substrate.

d. Rinse sample with DI water and blow dry

13. RTA Anneal (Optional)

   a. Anneal in Allwin21 AG610 RTA at specified temperature for 20 minutes in N₂ ambient

14. Source/Drain E-beam lithography

   a. Spin Resist

   b. E-beam patterning with Vistec EBPG5200

      i. Job file “LargeArea_mesa”, 350μC/cm² dose

      ii. 20 Transene Au TFA etchant, DI rinse, blow dry

      iii. 1 min (1:1) MIBK:IPA, 20s IPA, blow dry

      iv. 15s M4L descum (100W, 150sccm O₂, 50sccm He, 400mTorr)

15. Source/Drain deposition

   c. 4mins BOE 10:1 etch

   d. 30s (10:1) H₂O:HCl dip, DI rinse, N₂ dry, immediately load into evaporator

   e. Deposit 50nm Ti, 150nm Pd in Kurt J. Lesker Lab-18 evaporator

   f. Liftoff in acetone

16. Measure devices with Cascade MicroTech Summit Probe Station
Appendix D

GeSe 4-point Measurement Fabrication

D.1 Narrow-gap Ti/Au assembly electrode on silicon

1. Start with 1.2μm SiO₂ deposited on a double-sided polished n-Si wafer
2. Spin MicroChem PMGI SF-6S and Shipley SPR3012 for lift-off
   a. Acetone/IPA rinse, N₂ dry, bake at 110°C for 1 min
   b. Spin 4000 rpm for 45s with MicroChem PMGI SF6S, bake at 190°C for 5 mins
   c. Spin 3000 rpm for 35s with Shipley SPR3012, bake at 95°C for 1 min
3. Exposure pattern with GCA 8000 stepper
   a. Jobfile “SLKGEL” pass 1 and 5, exposure 0.5s, focus 0
   b. Use mask “sm341”
4. Develop resist
   a. 1 minute Microposit MF-CD-26 developer, deionized water rinse, N₂ dry
   b. 620s exposure in OAI Deep-UV
   c. 1 minute develop in MicroChem 101A developer, DI rinse, N₂ dry
5. Evaporate 20nm Ti/ 30nm Au with Kurt J. Lesker Lab-18
6. Lift-off with Microposit Remover 1165 stripper heated to 65°C, DI water rinse, dry
7. 10nm Al₂O₃/100nm SiO₂/10nm Al₂O₃ dielectric stack in Kurt J. Lesker 150LX ALD
   a. 10nm Al₂O₃
      i. Condition ALD chamber by depositing 10nm Al₂O₃ (200°C, 0.76 Torr, TMA pulse 0.03s/12s delay, H₂O pulse 0.1s/12s delay, 101 cycles)
ii. Acetone/IPA rinse, dry and load into chamber

iii. Deposit 10nm Al₂O₃, same recipe as above

b. Deposit 100nm SiO₂ with AMAT P-5000 PECVD Cluster Tool

i. 10 minute chamber clean O₂ plasma

ii. 10 minute chamber condition (300W, 300°C, 1400sccm N₂, 840 sccm N₂O, 20 sccm SiH₄)

iii. Acetone/IPA rinse, dry, Load into chamber

iv. 83s deposition of SiO₂

c. 10nm Al₂O₃ with Kurt J. Lesker 150LX ALD

i. Condition ALD chamber by depositing 10nm Al₂O₃ (200°C, 0.76 Torr, TMA pulse 0.03s/12s delay, H₂O pulse 0.1s/12s delay, 101 cycles)

ii. Acetone/IPA rinse, dry and load into chamber

iii. Deposit 10nm Al₂O₃, same recipe as above

D.2 4-point measurement fabrication

1. Start with the assembly electrode described in appendix E.1.

2. As grown solution of GeSe nanobelts is diluted 1:100 in toluene

3. Following procedure in appendix A.4, GeSe are assembled onto electrode using a single solution application

4. 4-point contacts were fabricated with e-beam lithography with Vistec EBPG5200

   a. Acetone/IPA rinse, N₂ dry, bake 110°C for 1 min

   b. Spin 4000 rpm for 45s with MicroChem MMA EL11, bake 150°C for 3 mins

   c. Spin 4000 rpm for 45s with MicroChem PMMA A3, bake 180°C for 3 mins
d. Deposit 10nm thermal Au with Kurt J. Lesker Lab-18 evaporator

e. E-beam patterning with Vistec EBPG5200 using job file “4-point GeSe”,
   350μC/cm² dose, 5nA beam

f. 20 Transene Au TFA etchant, DI rinse, blow dry

g. 1 min (1:1) MIBK:IPA, 20s IPA, blow dry

h. 15s TePla M4L descum (100W, 150sccm O₂, 50sccm He, 400mTorr)

5. Sample rinse held in water for 2 minutes immediately prior to loading into evaporation chamber

6. 120nm Ti, 30nm Au were deposited with thermal evaporation

7. Metal lifted off in acetone
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Publications and Presentations
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